Analysis and Design of Energy Efficient Frequency Synthesizers for Wireless Integrated Systems

by

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To My Family and Friends

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Abstract

Advances in ultra-low power (ULP) circuit technologies are expanding the IoT applications in our daily life. However, wireless connectivity, small form factor and long lifetime are still the key constraints for many envisioned wearable, implantable and maintenance-free monitoring systems to be practically deployed at a large scale. The frequency synthesizer is one of the most power hungry and complicated blocks that not only constraints RF performance but also offers subtle scalability with power as well. Furthermore, the only indispensable off-chip component, the crystal oscillator, is also associated with the frequency synthesizer as a reference.

This thesis addresses the above issues by analyzing how phase noise of the LO affect the frequency modulated wireless system in different aspects and how different noise sources in the PLL affect the performance. Several chip prototypes have been demonstrated including: 1) An ULP FSK transmitter with SAR assisted FLL; 2) A ring oscillator based all-digital BLE transmitter utilizing a quarter RF frequency LO and 4X frequency multiplier; and 3) An XO-less BLE transmitter with an RF reference recovery receiver. The first 2 designs deal with noise sources in the PLL loop for ultimate power and cost reduction, while the third design deals with the reference noise outside the PLL and explores a way to replace the XO in ULP wireless edge nodes. And at last, a comprehensive PN theory is proposed as the design guideline.

CHAPTER 1

Introduction

1.1. Ultra-low power radios in the Internet of Things

In the past few decades, advances in integrated circuit design has enabled numerous applications ranging from wearable health care monitoring systems to environmental sensing platforms and foreseen trillions of inter-connected IoT devices in the near future [1]. Long life time, low cost, small form factor and wireless capability are still the key constraints for many envisioned wearable, implantable and maintenance-free monitoring systems to be practically deployed in a large scale. Due to its relatively high-power consumption and indispensable external components, the radio often dominates the budget [2] of such devices, thus, reducing the power and cost of the radio sub-system can effectively increase operational lifetime, enable battery-less and maintenance free operation, and decrease the total size and cost of such devices. However, reducing radio power can be very challenging as there are important tradeoff between power consumption and performance metrics such as output power, sensitivity, and interference resilience.

Lots of research has been done to bring down the power consumption of the radio in the edge node while pushing all the computation and power in the base station with proprietary asymmetrical communication protocols [3-5]. But these designs either tradeoff power to significantly lower data rates, more severe interference and multiple access issues,

or suffer from an extra bulky and power-hungry aggregator as the interface to widely used computational platforms. They also do not comply with any existing wireless standard, limiting their widespread adoption. Thus, wireless standard compatibility of such devices is desirable as personal devices such as cell phones, personal computers and tablets with rich energy sources are the ideal base-stations of the inter-connected IoT devices in short range wireless sensor networks. It can provide excellent direct connectivity, local computing and data analysis efficiently without any extra interface. However, the power and performance tradeoff for such radio designs will become more stringent across all the layers including protocol, modulation, architecture and circuit design. Yet the bottom line is the same: deliver an effective amount of signal energy over the ubiquitous noise in all kinds of format. And the purpose of this thesis is to discover the bottom line of the tradeoffs, analyze the theoretical limits according to application emphasis, and offer several ULP radio chip prototypes with different techniques for verification.

1.2. Frequency modulation in ULP radios

Modulation scheme plays a very important role in reducing the power consumption of the radio as it is directly related to the complexity of the overall architecture and specifications of different sub-systems. Figure 1-1 shows the ULP radios publications dated back to 2005 [6]. Radios adopting a non-coherent modulation scheme such as on-off keying (OOK) or frequency-shift keying (FSK) show much more scalability in power consumption across different sensitivity levels, while others with coherent modulation schemes such as quadrature amplitude modulation (QAM) or phase-shift keying (PSK) are all relatively high power, despite a generally superior performance in sensitivity due to its better spectral efficiency and error probability performance over the same effective signal

to noise radio (SNR) [7] . Thus, coherent modulations are appealing in long range and high throughput applications with limited frequency band resources. But its stringent requirement in phase noise and power amplifier (PA) linearity makes it hard to reduce the power any further, making it inappropriate in ULP designs where power consumption is the primary concern.

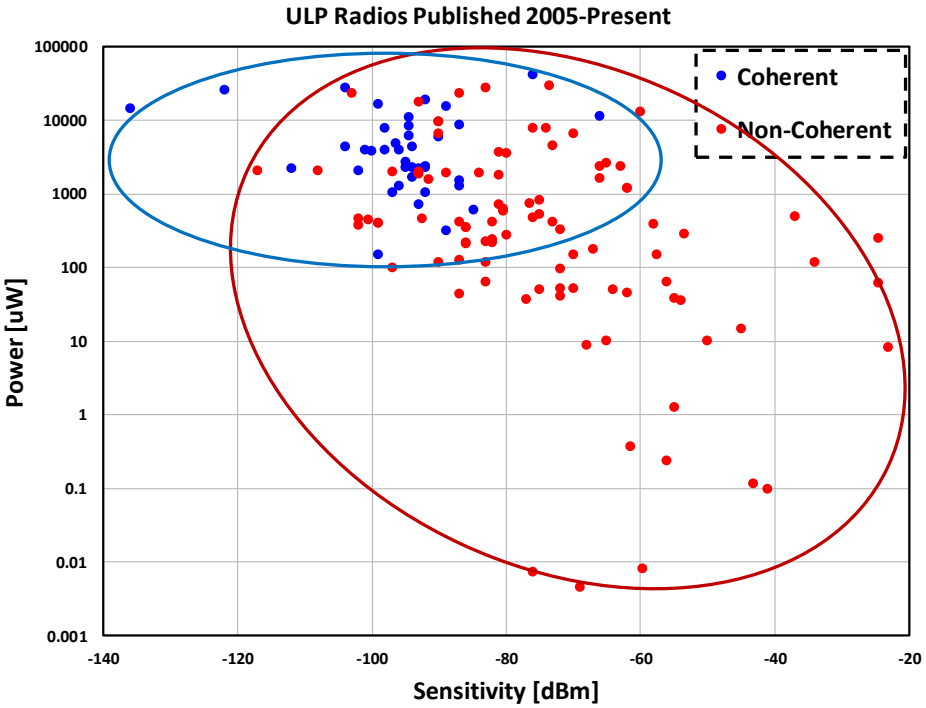


Figure 1-1. Power consumption vs sensitivity of coherent and non-coherent radios in recent publications

Among the non-coherent modulation schemes, even though OOK and relative pulse modulated transceivers tend to have a generally lower power consumption due to their simpler architecture and the duty cycle nature of such modulation, frequency modulations such as FSK are superior in several aspects. Due to the consecutive on-off switching of the OOK modulation, the bandwidth increases compared to FSK modulation using the same

data rate. Thus, FSK is more spectral efficient. The increased bandwidth requires a larger filter bandwidth which will increase the noise floor, and this will result in degradation in sensitivity. To achieve a similar sensitivity, data rate has to be sacrificed. Recent advances in pulse modulation-based radios, especially wakeup radios have brought the power consumption down to Nano Watt level [4, 8-11]. The overall power saving from duty cycling in a single edge node is achieved by trading off performances in data rate, sensitivity and interference resilience, making it less appealing in massive inter-connected sensor networks for IoT applications. As it solely emphasizes the lowest power while neglecting the tradeoffs from duty cycle, it has rarely been adopted in any widely used commercial standards.

Frequency modulation, on the other hand, could be a better fit in such applications. It not only cherishes benefits of the simple architecture from pulse modulated radios but can be very versatile in design as well. When targeted for the lowest power with least required performance in a lot of proprietary protocols, sub-system blocks such as the local oscillator can be designed as low power as the pulse modulated counter-part, using injection locked or even free running low power ring oscillators. And when performance is required, it can offer the decent spectral efficiency and network capacity and be compatible with several mainstream communication standards that are already widely adopted in existing personal mobile devices such as Bluetooth Low Energy (BLE). BLE utilizes Gaussian Frequency Shift Keying (GFSK) at 2.4GHz ISM band with 40 2 MHz wide channels [12] and its overall radio-frequency specification is also quite relaxed. BLE compliant transmitters consuming only a few hundred μW have been reported recently [13, 14], showing great

compatibility of FSK in standardized ULP radio designs and huge market opportunities of standard compatible wireless IoT devices with BLE's deep penetration in mobile platforms.

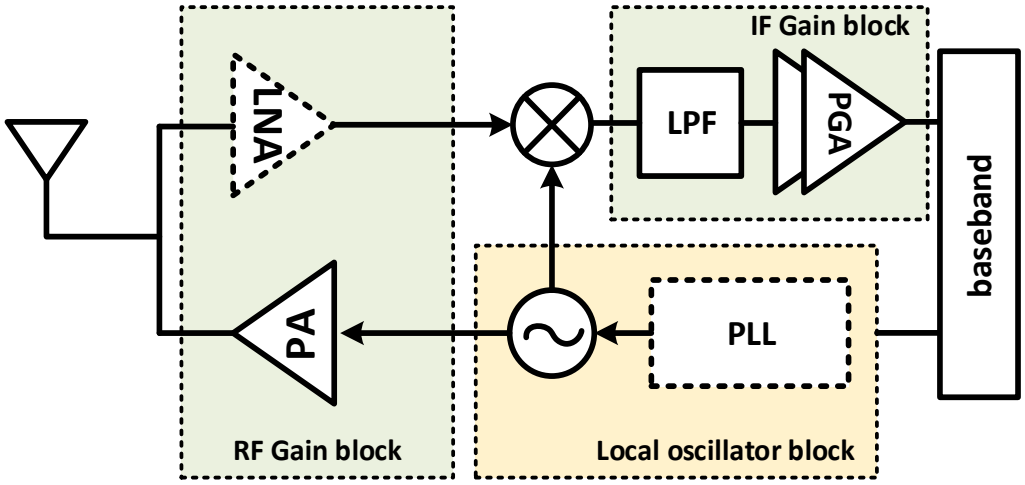


Figure 1-2. A generic frequency modulated ultra-low power transceiver architecture

The most power consuming circuit blocks in frequency modulated ULP radios can be defined in two categories: Signal Gain blocks and the local oscillator, as shown in Figure 1-2. The signal gain blocks are directly related to the link budget, which is a straightforward tradeoff between power consumption and effective communication range. Here we can take them as a unified block in the TX-RX link. In recent ULP RX designs, passive mixer first architectures have become more and more popular [Cornell paper] and achieve comparable noise figures of the RX signal chain. Thus, the power amplifier in such radios is dominating the power budget together with the local oscillator since the IF gain block and filtering circuit blocks consume much less power. The minimum output power of a transmitter can be found using Friis equation:

$$P_{TX} = P_{RX} - G_{ANT} - 20\log_{10}\frac{\lambda}{4\pi D} \qquad (1-1)$$

where D is the distance and λ is the wavelength. The path loss for 10 m for 2.4GHz signal is around 60dB while a 1-2 m path loss is around 40-50dB, theoretically. Taking BLE as an example, typical BLE RXs have a sensitivity close to -90dBm. Although environmental surroundings such as human body will possess extra loss, a -20dBm output power from a transmitter will be sufficient to communicate within 3 meters. The power consumption of that PA can be brought down to as low as 100μW.

The power and performance tradeoff of the local oscillator (LO) in frequency modulated ULP radios is much more complicated, as the LO introduced phase noise (PN) can either affect the effective SNR and bit error rate (BER) performance or impact the frequency modulation quality and RX blocker performance. There has yet been a unified theory targeted for phase noise requirement and performance tradeoffs in ULP FSK radio designs. In this thesis, instantaneous frequency variation (IFV) will be introduced to serve as an intuitive link between system level specifications in FSK radios and phase noise requirements for the LO, and theoretical limits for different levels of requirements will be provided as well.

1.3. Frequency synthesizer as an integral part of the RF transceiver

The design of frequency synthesizers in RF transceivers has been one of the most challenging parts of wireless system designs. On the one hand, it has to meet phase noise and spur performance requirements, as both affect the spectral purity of the local oscillator. In direct modulated transmitters, phase noise will directly affect the output spectrum. And in the receiver design, any excessive phase noise or spurs falling into the adjacent channels will result in potential SNR degradation due to reciprocal mixing. On the other hand, its power consumption has to be minimized due to limited power budget in a wireless system.

It is especially true for ULP radios where the LO could take more than half of the total power. Moreover, the synthesizer has to be fast enough in settling time in applications where frequency hopping is needed to combat various channel fading and interferences, such as BLE.

Thus, it becomes quite tricky and rigorous to design the frequency synthesizer for ULP radios that can offer just enough noise performance while consuming the minimum amount of power. It is good to design frequency synthesizer according to the most stringent requirement in a transceiver, such as the blocker and reciprocal mixing requirement in a receiver. However, its power consumption would be as high as a few milliwatts and make such design impossible to be adopted in a self-powered edge node where the total power budget is below a few hundred microwatts. Thus, it might be necessary to revisit the network protocols and system level architectures to create a standard compatible asymmetric communication, such as in BLE, where the edge nodes can be characterized as non-connectable transmit only devices in BLE advertising channels as long as the LO in the TX meets the FSK modulation specification in BLE. As will be disclosed in chapter II, the phase noise requirement from the BLE FSK modulation specification is much relaxed compared to general BLE designs and it enables the first reported ring oscillator based BLE designs with the total power less than 500 μW.

1.4. Thesis contributions

This thesis focuses on circuit and system designs for ULP frequency modulated radios with a special emphasis on phase noise theory analysis and energy efficient frequency synthesizer design. The goal is to bring standard compliance (such as BLE) into ULP radio design with a vision to bring the benefits of battery-less and maintenance-free operation to

the Internet of Things in a very expansive market. The main contributions of this thesis are in the following areas:

1. Phase noise analysis in ULP radios - A phase noise analysis in frequency modulated radios is proposed based on prior PN theories, which links the system level specifications in FSK, such as frequency deviation, data rate, modulation index, etc. to the phase noise requirement for the frequency synthesizer design. Instantaneous frequency variation (IFV) is introduced for such analysis. The analysis results in different phase noise limits corresponding to bit error rate (BER) performance, FSK modulation performance, and blocker performance for the guidance of system level characterization in proprietary protocols, and frequency synthesizer as well as its sub-circuits design in standard compliant radios.
2. Ring oscillator based ULP FSK transmitters – 2 prototype FSK TX chips are proposed and verified. The 1st FSK TX is designed at 2.4GHz for a battery-less 507nW SoC in correspond to the phase noise limit for BER performance. The 1st TX utilized an open loop ring oscillator with a SAR-assisted frequency locked loop for initial frequency calibration. The 2nd TX is a BLE compliant transmitter using a ring oscillator based ADPLL and a 4X frequency edge combiner in accordance with the phase noise limit in BLE modulation performance. The TX is the first reported RO based BLE design with a peak power of 486μW and 40X chip area saving while configured as advertiser talking to a phone.
3. Analysis of Phase Noise and Frequency Accuracy in Crystal-less Wireless Edge Nodes – A general theory associating phase noise and frequency accuracy in both short term and long term is proposed. As an extension to contribution 1, which

focuses more on the radio system level characterization, this section focuses more on phase noise shaping's impact on various kinds of jitters and frequency stability (such as Allan Deviation) in the local oscillator sub-system. The reference noise's impact is specifically analyzed for potential crystal oscillator replacement in ULP wireless edge nodes, such as RTC, RC oscillator and RF clock harvesting.

4. XO-less BLE transmitter design – This is a cooperative research project that includes several prototype chips based on the theory proposed in contribution 3. The contributions involved in this thesis include characterization of the noise requirement PLL reference for valid BLE communication; an ADPLL utilizing an embedded moving average filter for accurate frequency calibration with noisy reference (RC oscillator) and open loop LCVCO in prototype chip 1; and a RF clock recovery circuit incorporating with a back-channel BLE RX for coarse tuning in prototype chip 2.

CHAPTER 2

Phase noise in frequency modulated radios

Phase noise (PN) has always been a fundamental factor in the design of wireless communication systems. To meet the PN requirement, a relatively large amount of power is consumed in the local oscillator (LO), buffers, and RF frequency synthesizer. This is especially true for ultra-low power (ULP) radios, where the LO typically consumes 50%-80% of the total power. Some pulse modulations such as OOK allow us to design an ULP radio with a free running ring oscillator (RO) with relatively poor PN, or no oscillator at all. However, the low resilience of OOK to noise and interference limits the scaling of these radios for large numbers of personal area network nodes in IoT applications. Thus, it will be extremely helpful to clarify the relationship between the PN requirement and its influence on FSK and enable us to intrinsically save radio power.

FSK modulation and its BER performance has been well studied since modern communication systems came into use [15], [16], but in the presence of only AWGN channel noise. Ref [17] analyzed the effect of circuit imperfections and found that phase noise effectively adds a higher noise floor and only affects the BER when the carrier-to-noise ratio is high. However, it doesn't include a quantitative analysis of how phase noise directly affects the BER and which FSK parameter has a more significant impact on the phase noise requirement of a radio system. This chapter analyzes the direct relationship of

PN in a TX-RX link, as well as the PN profile in free-running LOs and locked PLLs, to FSK parameters such as frequency deviation (FD) and data rate (DR), using instantaneous frequency variation (IFV) as a link. It then offers a PN boundary for a given BER requirement for FSK radios. And from there, a more stringent PN requirement associated with frequency modulation specifications in FSK is derived and analyzed for standard compliant (such as BLE) ULP FSK transmitter designs. Finally, PN's influence in blocker tolerance and reciprocal mixing in FSK RX designs is analyzed in the aspect of noise power. With different levels of design concerns associated with system level specifications in FSK, the resulting PN requirements will be helpful for designers to effectively, efficiently and flexibly design the circuits with the lowest power to its physical limit while maintaining the desired performance.

2.1. Instantaneous frequency variation due to phase noise

In order to clarify the relationship between PN and frequency deviation in FSK, it's necessary to find out the relation between PN and real time frequency variation. The real time frequency variation is related to period jitter but must be treated as a random process, and cannot be directly inverted. Period jitter is the standard deviation of the normally distributed clock period around its mean value. Assume on average the clock has a period of T and thus a frequency of $F = 1/T$, and due to phase noise, at a random point in time, the instantaneous relationship between period and frequency is:

$$\mathrm{T} + \Delta\mathrm{t} = \frac{1}{\mathrm{F} + \Delta\mathrm{f}} \qquad (2-1)$$

Which can be rewritten as follows when delta_f is << F:

$$1+\frac{\Delta \mathrm{t}}{\mathrm{T}}=\frac{1}{1+\frac{\Delta f}{F}}\approx 1-\frac{\Delta f}{F} \qquad (2-2)$$

For RF frequency synthesizers, the center frequency is much larger than its frequency variations, thus by using the Taylor expansion, the relation can be further simplified as:

$$\Delta f \approx -F^2 \Delta t \qquad (2-3)$$

This indicates that frequency variation changes in the same way as period jitter. The frequency over time of a free running RO is measured using a Tektronix MDO4000C and shows that the distribution of frequency is Gaussian and that its standard deviation scales up with center frequency. This also implies that frequency variation and period jitter are ergodic and their time average is the same as the average over frequency or period space when there is no frequency drift.

The relationship of phase noise to period jitter has been well studied in [18]-[21] and the link between jitter to phase noise is:

$$\sigma_\tau^2 = \int_0^\infty S_\tau(f)df = \frac{1}{f_0^4}\int_0^\infty S_\phi(f) f^2 sinc^2\left(\frac{\pi f}{f_0}\right)df \qquad (2-4)$$

It can be further simplified as:

$$\sigma_\tau^2 = \frac{2}{\pi f_0^3}\int_0^\infty \mathcal{L}(f) f^2 df \int_0^\infty sinc^2(x)dx \qquad (2-5)$$

Where $\mathcal{L}(f)$ is the PN PSD. With only white noise taken into consideration, $\mathcal{L}(f)f^2$ is a constant. And as $\int_0^\infty sinc^2(x)dx = \pi/2$, thus, across the whole single side band (SSB), the relation between period jitter and PN can be simplified as:

$$\mathcal{L}(f) = \frac{\sigma_\tau^2 f_0^3}{f^2} \qquad (2-6)$$

With the approximation from period jitter to instantaneous frequency variation (IFV) as indicated in equation (2-3), the link between phase noise and IFV is:

$$\mathcal{L}(f) \approx \frac{\sigma_f^2}{f_0 f^2} \qquad (2-7)$$

(2-6) is the classical link between jitter and PN [18], with a relation to IFV in (2-7) when noise in the whole SSB is considered. This result shows that whenever the frequency variation of an oscillator is doubled, the phase noise will increase by 6dB. However, when it comes to the phase noise impact in radio circuit designs, we need to consider the noise filtering effect in the receiver. Assuming a brick wall filter in the RX with a bandwidth $\mathrm{BW_{rx}}$:

$$\sigma_\tau^2 = \frac{2}{\pi f_0^3}\mathcal{L}(f) f^2 \int_0^{\frac{BW_{rx}\pi}{f_0}} sinc^2(x)dx \qquad (2-8)$$

Since the RX bandwidth is much smaller than the carrier frequency, the integral of the squared sinc function can be approximated as:

$$\int_0^{\frac{BW_{rx}\pi}{f_0}} sinc^2(x)dx \approx Si\left(\frac{2BW_{rx}\pi}{f_0}\right) \approx \frac{2BW_{rx}\pi}{f_0} \qquad (2-9)$$

Thus, with the RX filter, the relation among jitter, PN and IFV can be modified as:

$$\sigma_\tau^2 = \frac{4BW_{rx}}{f_0^4}\mathcal{L}(f) f^2 \qquad (2-10)$$

$$\sigma_f^2 = 4BW_{rx}\mathcal{L}(f) f^2 \qquad (2-11)$$

This offers a simple intuition for circuit designers that once the RX filter BW is known, the PN spec at certain offset, say 1MHz, can be calculated directly from the system level requirements for the frequency modulated signal.

Next, we consider the case where a PLL affects the PN noise shaping. When the PLL has a bandwidth $\mathrm{BW_{pll}}$, and with all the PLL noise sources taken into account, the in-band PN can be approximated as a constant $\mathcal{L}_{\mathrm{in}}$. So (2-9) becomes:

$$\sigma_\tau^2 = \frac{2\mathcal{L}_{in}}{f_0^4}\int_0^{BW_{pll}} \frac{f_0^2}{\pi^2}\sin^2\left(\frac{\pi f}{f_0}\right)df \; + \frac{2\mathcal{L}_{in}f_{BW_{pll}}^2}{f_0^4}\int_{BW_{pll}}^{BW_{rx}} sinc^2\left(\frac{\pi f}{f_0}\right)df \quad (2-12)$$

Simplified as:

$$\sigma_\tau^2 = \left\{\begin{matrix}\frac{1}{2\pi^3 f_0}\left(\frac{2\pi BW_{pll}}{f_0} - \sin\left(\frac{2\pi BW_{pll}}{f_0}\right)\right) + \\ \frac{4}{f_0^4}\left(BW_{rx} - BW_{pll}\right)BW_{pll}^2\end{matrix}\right\}\mathcal{L}_{in} \quad (2-13)$$

$$\sigma_f^2 = \left\{\begin{matrix}\frac{f_0^3}{2\pi^3}\left(\frac{2\pi BW_{pll}}{f_0} - \sin\left(\frac{2\pi BW_{pll}}{f_0}\right)\right) + \\ 4\left(BW_{rx} - BW_{pll}\right)BW_{pll}^2\end{matrix}\right\}\mathcal{L}_{in} \quad (2-14)$$

Note that (2-13) and (2-14) show that the larger the PLL bandwidth, the larger the jitter and IFV. That is because in these equations, the in-band phase noise is set as a constant, and larger BW means a higher oscillator PN. On the other hand, larger BW means lower $\mathcal{L}_{\mathrm{in}}$ if the oscillator PN is preset. In PLL designs, the in-band PN is a more valuable spec than the oscillator spot PN at certain offset, since it also defines specs for other circuit blocks, which are also major PLL noise sources such as the reference, divider, TDC, and DAC, etc. For the $BW_{rx} < BW_{pll}$ case, the PN, jitter and IFV relations are shown as follows:

$$\sigma_\tau^2 = \frac{1}{2\pi^3 f_0}\left(\frac{2\pi \mathrm{BW_{rx}}}{f_0} - \sin\left(\frac{2\pi BW_{rx}}{f_0}\right)\right)\mathcal{L}_{in} \quad (2-15)$$

$$\sigma_f^2 = \frac{f_0^3}{2\pi^3}\left(\frac{2\pi BW_{rx}}{f_0} - \sin\left(\frac{2\pi BW_{rx}}{f_0}\right)\right)\mathcal{L}_{in} \quad (2-16)$$

This case is very useful for RO based designs where RO PN is the dominant noise source for PLL design and it needs to be regulated with a wide PLL bandwidth.

The above derivations show the relationship among PN, jitter, and IFV with only white noise taken into consideration. Introducing a flicker noise corner in the model will make the theoretical approximation much more complicated with very limited model accuracy improvement. As in PLL regulated cases, the in-band PN floor is contributed by different noise sources such as the TDC, DAC, and reference, thus, a flat noise floor is a straightforward and quite accurate representation. And in practical open loop LC oscillator based designs, the slow frequency drift due to flicker noise (<10 kHz within 1ms) will be recalibrated before each data packet.

2.2. Noise modeling in an FSK link

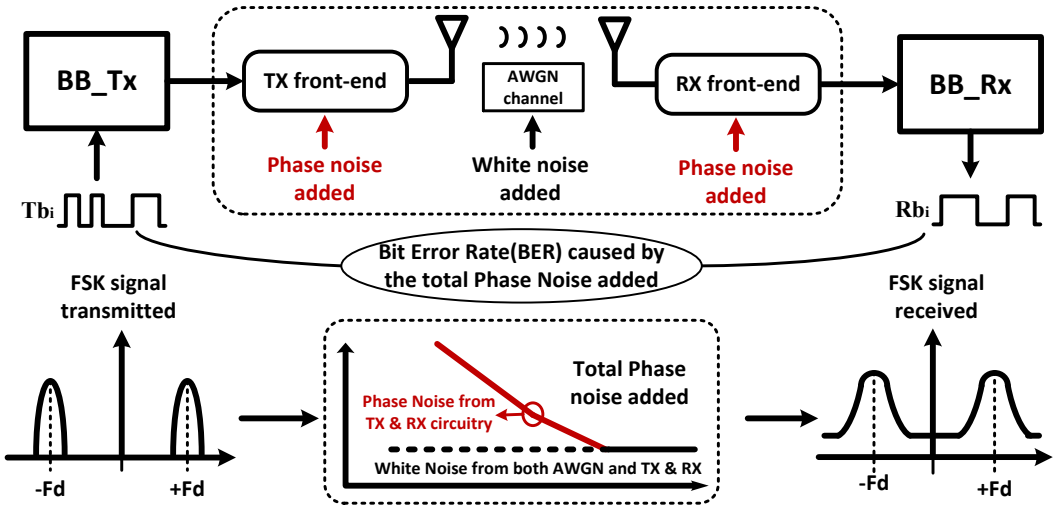


Figure 2-1 TX-Phase Noise-RX model for BER analysis in FSK

In order to verify the analysis of the phase noise influence on frequency variations and its impact on FSK parameters such as frequency deviation (FD) and data rate (DR), a

simple TX - phase noise - RX model was built. White noise in circuits can either affect the phase noise or increase the noise floor while the AWGN channel noise only affects the noise floor. It is more straightforward to model the total additive noise together when designing a communication link, as shown in Figure 2-1.

Transmitted data are directly FSK modulated and sent to the noisy circuits and channel, where phase noise is added mostly from the local oscillators (LO), and the noise floor is increased by both. Then the noisy signal is sent to the RX baseband for demodulation and the BER is calculated. This will offer a direct relationship between just LO phase noise and BER. We assume a representative FSK receiver implementation with a digital phase discriminator and frequency domain matched filter as shown in Figure 2-2.

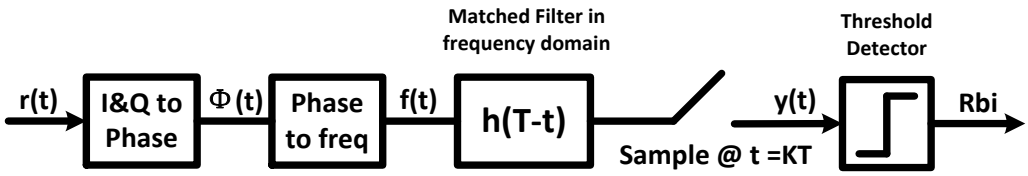


Figure 2-2 Matched filter receiver for FSK

Noting that phase noise will be independently added together from both TX and RX, so from the design prospective, the phase noise specifications for each radio could either be set from the model with a 3 dB margin, if the same synthesizer is used for both, or that one (e.g. TX in a sensor node) be directly set from this model if the other one, say RX in the base-station, has a much better PN performance for the purposes of blocker tolerance and reciprocal mixing.

Three cases representing different phase noise levels in different application focuses will be discussed in the following sessions. The 1st case discusses the phase noise effect in bit error rate (BER) when PN is the dominant noise source in a high SNR regime. The PN

is at a high level where the IFV is comparable to frequency deviation in a FSK radio and the BER performance will be directly impacted. It is useful to define the worst case PN limit in an FSK link for single channel communications in certain proprietary protocols where power consumption is the primary concern. Since the phase noise level is relatively high, its influence on the effective SNR loss will be discussed as well. The 2nd case talks about the PN effect to FSK modulation quality. In this case, the IFV due to PN is much smaller than the frequency deviation, thus BER performance won't be practically affected. However, the IFV in standardized protocols is restricted by certain modulation requirements such as eye diagram and modulation index. Bluetooth Low-Energy (BLE) is taken as an example in this analysis to show the PN limit in a BLE TX design for the lowest power. This limit is useful for ultra-low power standard compliant or compatible radio designs in low power wireless sensor networks. The 3rd case, to be comprehensive, discusses the phase noise requirement in standard compliant radio designs, especially receivers, specifically to deal with blockers and reciprocal mixings. This is always used in defining LO specifications in different communication standards for the purpose of optimal performance regardless of modulations. These 3 different levels of limits offer insights to PN's effect in FSK radios and flexibilities in the LO and its sub-circuit designs for a balanced power-performance tradeoff. Details will be discussed as follows.

2.3. Phase noise's effect to BER and effective SNR loss

As discussed in 2.1, the IFV due to the phase noise of the LO is ergodic and its time average is the same as the average over frequency space. The IFV follows the same distribution of the period jitter while scaling up with center frequency, and without significant spurious tones in the LO output, they all follow a Gaussian distribution in

general cases. In the high SNR regime, phase noise's effect to BER in the LO varies with different frequency deviations (FD) and data rates (DR).

The simulation results of PN vs BER at different FSK FD and DR are shown below. Figure 2-3 shows the phase noise added with different phase noise levels while the noise floor is kept the same at -110dBm, which is the same noise floor when capturing measured data with a MDO4000C spectrum analyzer. The phase noise is shaped by a simple type I order I PLL with a 1MHz BW to suppress flicker noise, thus the noise has a -10dB/dec rolloff in band and -20dB/dec rolloff out of band. The phase noise levels @ 1MHz offset are sampled as the X-axis for the PN vs BER plot.

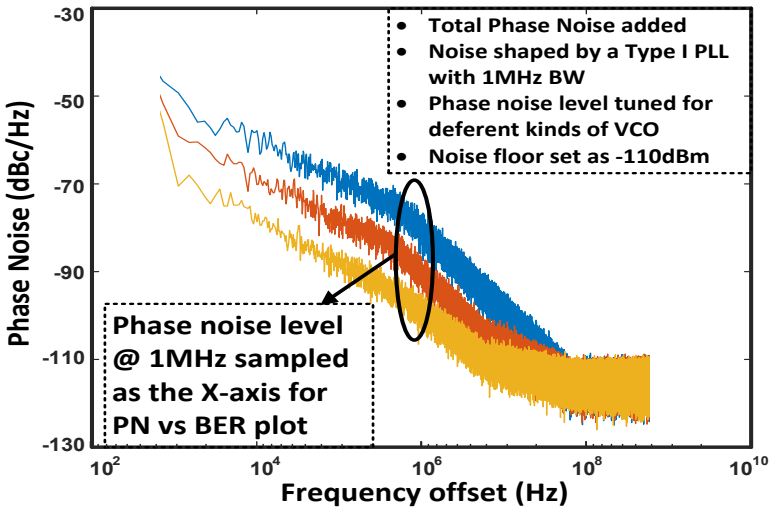


Figure 2-3 Total phase noises at different levels for simulation

Figure 2-4 shows how the BER changes with the FSK FD when the PN are kept the same for different traces. It shows that whenever the FSK frequency deviation is doubled, the phase noise requirement could be relaxed by 6dB to achieve the same BER, which agrees with previous analysis on phase noise over frequency variation. Meanwhile, if DR is doubled, as shown in Figure 2-5, phase noise should be 3dB better to achieve the same BER. The reason is that when doubling the data rate, energy per bit will be halved and thus

the total in band noise has to be reduced by 3dB to maintain the same E_b/N_0. The result is by increasing both the FSK frequency deviation (signal bandwidth) and the data rate by a factor of 2 while the modulation index remains the same, the spectral efficiency remains constant (bits/Hz), the PN specification could be relaxed by 3dB.

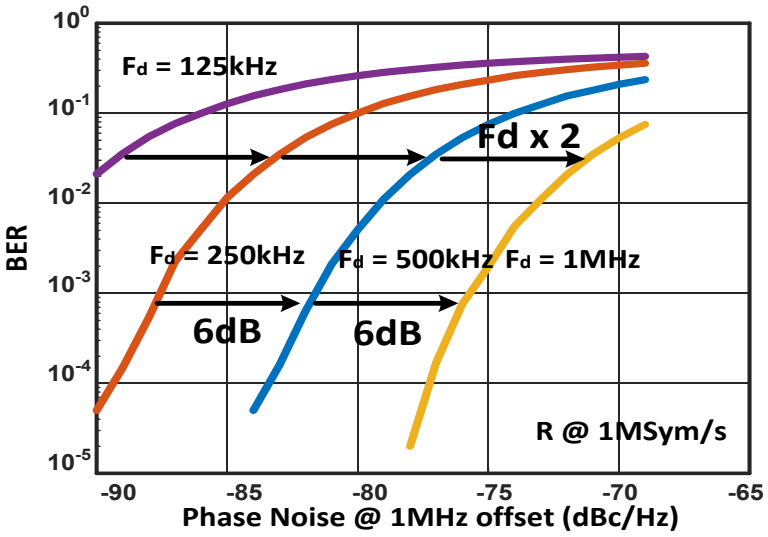


Figure 2-4 BER vs PN for different frequency deviations

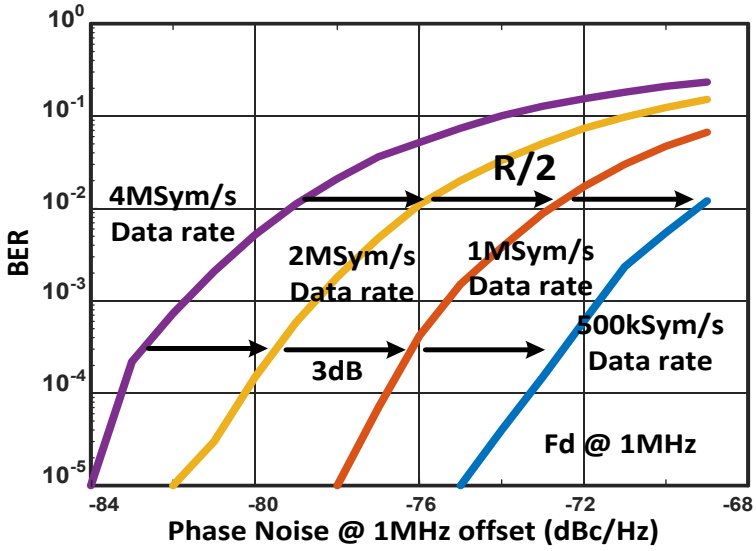


Figure 2-5 BER vs PN for different data rates

Figure 2-6 shows such a comparison using Bluetooth Low Energy (BLE) as an example. As in BLE 5.0, it supports a high data rate mode with 2Msym/s with a 1 MHz frequency deviation compared to previous BLE 4.2 where the DR is set to 1Msym/s with 500 kHz FD. So simply from the BER's perspective, the LO's phase noise requirement could be significantly relaxed as opposed to general designs considering the blockers in a typical BLE receiver. In order to achieve a BER smaller than 10^{-4}, BLE 4.2 only needs a type I PLL-with 1MHz bandwidth and a low power RO with -83 dBc/Hz phase noise @ 1MHz offset to meet the BER requirement. For the newly released BLE 5.0 in high data rate mode (2x the FD and DR of BLE 4.2), the phase noise requirement is about -80 dBc/Hz.

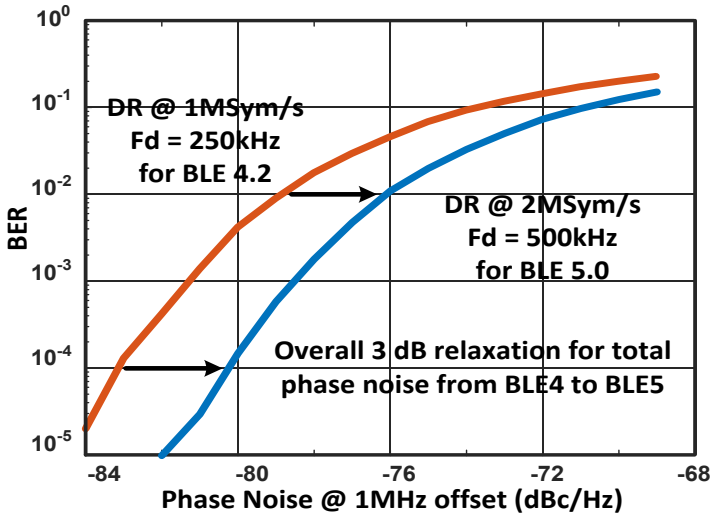


Figure 2-6 BER vs PN comparison for Bluetooth Low Energy applications

All the above results are based on the high SNR assumption and the contribution from white noise are ignored. However, as the excessive phase noise in these cases are high and can affect the effective SNR for receiver designs, especially when sensitivity is one

important concern, its impact has to be evaluated. The relationship between sensitivity and required SNR is as follows:

$$S_i = NF + N_f + SNR_e \qquad (2-17)$$

Where NF is the noise figure of the receiver and the N_f is the noise floor which is related to the receiver bandwidth:

$$N_f = -174 + 10\log_{10}(BW_{rx}) \qquad (2-18)$$

And the effective SNR can be divided into:

$$SNR_e = SNR_w - 10\log_{10}\left(1 + \frac{P_{PN}}{P_{AW}}\right) \qquad (2-19)$$

Where SNR_w is white noise referred SNR and P_{PN}, P_{AW} represent the noise power of phase noise and white noise, respectively. Using the same model in 2.2, the simulated PN vs SNR and PN vs effective SNR loss assuming a free running VCO with FD = 500 kHz and DR = 100 ksym/s are shown in Figure 2-7. An example of an ultra-low power FSK transmitter utilizing a free running ring oscillator and a SAR assisted frequency locked loop to verify the BER defined phase noise limit will be discussed in section 2.8.

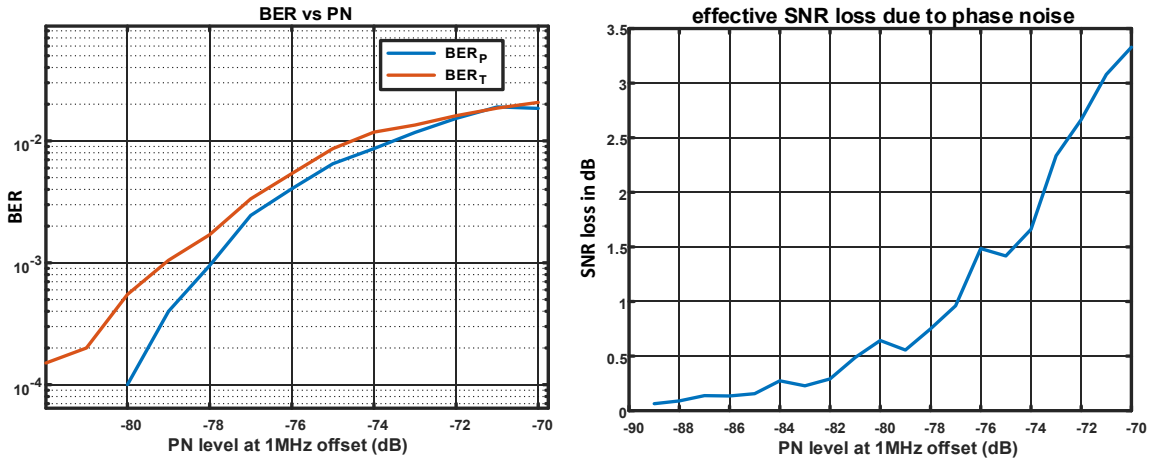


Figure 2-7 PN's effect on effective SNR loss

2.4. Phase noise's effect on frequency modulation

While BER can be a good indicator of whether an FSK transmitter communicates with a corresponding FSK receiver at the minimum requirement, it is not an effective way to evaluate the quality of the FSK communication. In most cases, there are certain specifications in the frequency modulation requirement. For example, as shown in Figure 2-8, BLE requires a > 370kHz minimum frequency difference for a ± 250 kHz frequency deviation and the zero crossing error has to be better than $\pm 1/8$ of a symbol period [12]. The IFV derived in session 2.1 can offer an intuitive link between spot/in-band phase noise to a system level spec in frequency modulated radios. This is because the $6\sigma_f$ of the IFV is approximately the peak-to-peak frequency error, and spot/in-band PN is a direct indicator of oscillator/PLL design.

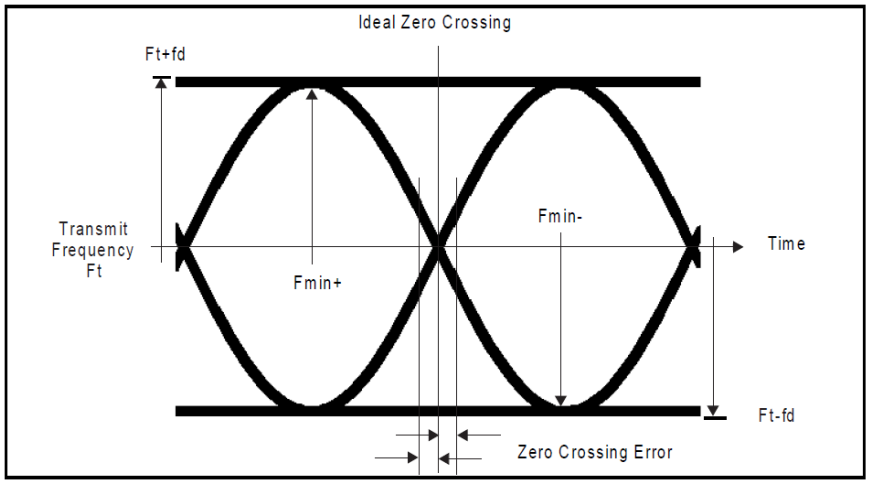


Figure 2-8. GFSK modulation requirement in BLE [12]

As BLE requires > 370kHz minimum frequency difference for a ± 250 kHz FD, a $3\sigma_f < 65kHz$ can be used to define the PN spec (40 kHz for GFSK but in the noise limited region, Gaussian shaping won't effectively improve the spectrum efficiency). Figure 2-9 shows that the resulting IFV vs PN. 2 cases are compared using open loop oscillators and

PLL regulated oscillators when the PLL bandwidth is set to 100kHz as a typical RF synthesizer design. The results are comparable, and it leaves a big margin to the 65kHz BLE requirement using LCVCO, which indicates an over-design in the LO noise-power penalty. The receiver filter bandwidth is set to 2 MHz, same as the BLE channel bandwidth. And as indicated in equation (2-10)-(2-16), the receiver filter bandwidth also has a significant impact on the resulting IFV with different LO phase noise shaping. Figure 2-10 shows the simulated IFV vs receiver bandwidth assuming a -110dBc/Hz VCO with a 100 kHz bandwidth PLL. Figure 2-11 further shows that with a wide band PLL to suppress the in-band PN, an ULP RO can also achieve the target. An example of the first reported ring oscillator based BLE transmitter designed at this theoretical phase noise limit will be discussed in detail in chapter 4.

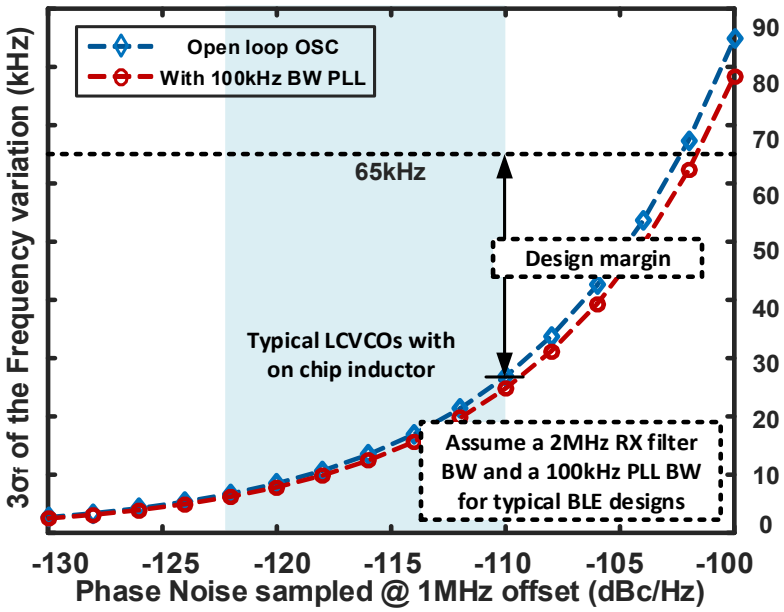


Figure 2-9 Simulated IFV vs LO phase noise between open loop oscillator and oscillator with 100kHz BW PLL.

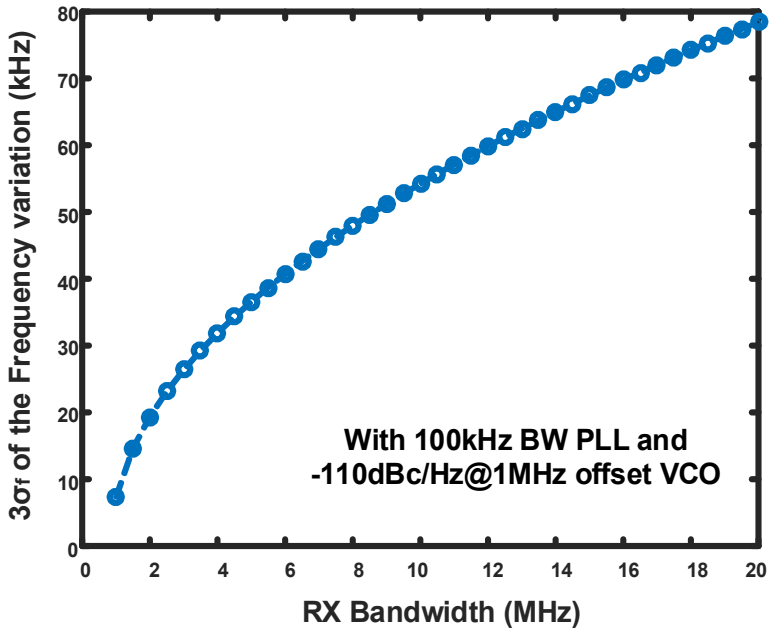


Figure 2-10 Simulated IFV vs RX filter bandwidth assuming a 100kHz PLL bandwidth

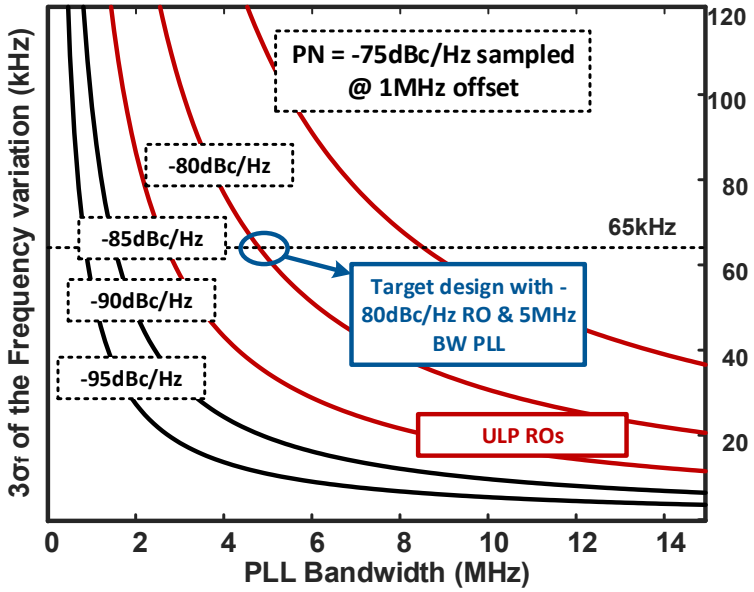


Figure 2-11 Simulated IFV vs PLL bandwidth for RO designs with varying phase noise

2.5. Phase noise's effect on blocker tolerance

The above analysis and simulation results show that in FSK transmitter designs, the phase noise requirements necessary to offer valid up-link/down-link communications or to

meet modulation specifications are much relaxed compared to state-of-the-art designs [13, 22]. The IFV can be a direct link between system level specifications such as frequency deviation to in-band/spot phase noise requirements in the LO sub-system design. However, for receiver designs, especially those without external narrowband RF filtering, PN has to be considered in a different way as well. Even with RF filters to filter out of band (OOB) interference, blocker from adjacent channels (ACI) can also degrade the noise figure when it mixes with LO phase noise [23-25], as shown in Figure 2-12. It deposits additive noise in the receive channel proportional to the blocker amplitude. This phenomenon is called "reciprocal" mixing. Thus, LO phase noise has to be specified from interference performance requirement in system level.

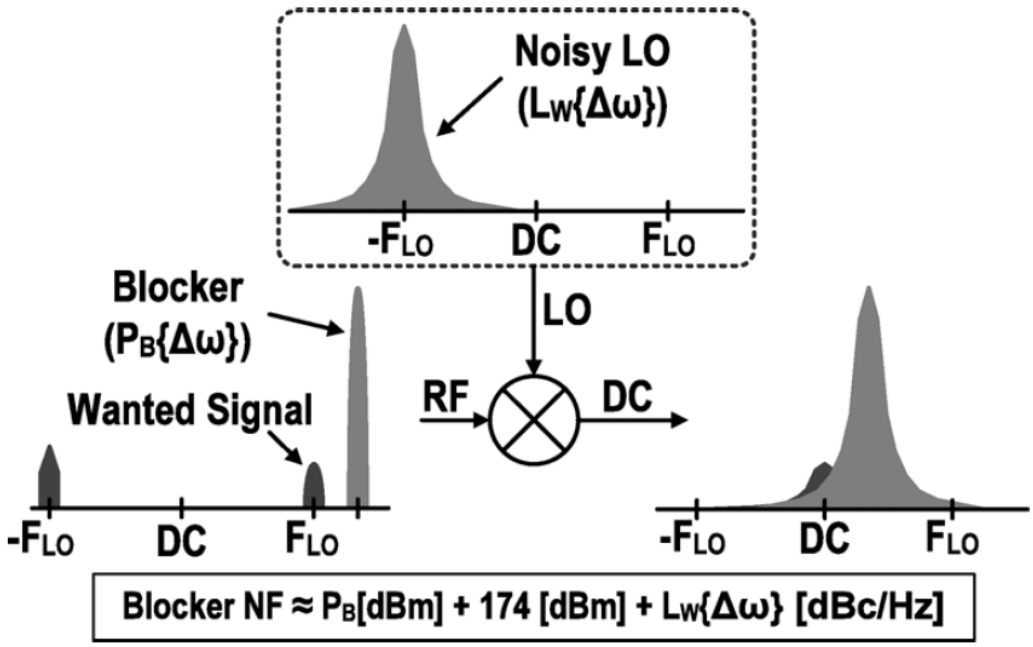


Figure 2-12 Noise degradation due to reciprocal mixing [23]

If we assume the LO has a PN characterized by $\mathcal{L}(f)$ and the blocker has a total power of P_B, then reciprocal mixing will add the following noise power to the signal:

$$N_{rm} = P_B + \mathcal{L}(f_B) + 10\log_{10}(BW) \quad (2-20)$$

Where N_{rm} is the in-band noise power introduced by reciprocal mixing and BW is the RX filter bandwidth. Assume the carrier power is P_C and the required SNR by the standard is SNR_m, then the PN requirement can be derived from the following equation:

$$\mathcal{L}(f_B) \leq P_C - P_B - 10\log_{10} BW - SNR_m \quad (2-21)$$

Taking BLE as an example again, the blocker specification is shown in Figure 2-13. So the phase noise requirement at certain offsets in BLE are:

$$\mathcal{L}(\Delta f = 1M) \leq -21 - (-15) - 63 - 9 = -79\ [dBc/Hz] \quad (2-22)$$

$$\mathcal{L}(\Delta f = 2M) \leq -21 - (17) - 63 - 9 = -110[dBc/Hz] \quad (2-23)$$

$$\mathcal{L}(\Delta f \geq 3M) \leq -21 - (-27) - 63 - 9 = -120\ [dBc/Hz] \quad (2-24)$$

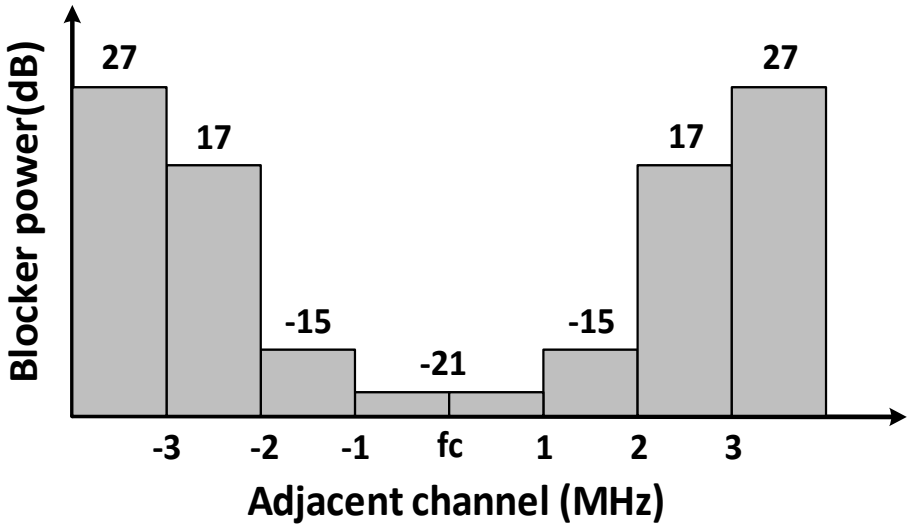


Figure 2-13 Blocker requirement for BLE

Thus, for LO designs in the BLE RX, the spot PN requirement is basically set by $\mathcal{L}(\Delta f = 4M)$ as the 2nd adjacent channel is 4MHz away. If using an LC VCO in the LO, a -108dBc/Hz spot PN at 1MHz offset can meet both requirements in modulation and blocker performance.

For ring oscillator based designs, large bandwidth PLL and extra noise cancelling techniques have to be adopted even though the modulation requirement can be easily met. A detailed example of BLE TRX using RO in the LO design will be discussed in chapter5.

2.6. Phase noise requirement in FSK TRX design and optimal FSK protocol for low power and short range communications

As analyzed above, phase noise in the local oscillator has multiple effects on frequency modulated radio designs. From the BER or modulation quality's perspective, the 3σ instantaneous frequency variation (IFV) represents the frequency error that can be directly compared to system required frequency deviation. This is helpful for ULP short range FSK transmitter designs as it sets the maximum phase noise limits that correspond to the possible minimum power consumption without violating FCC spectrum masks and standard specifications. On the other hand, LO phase noise in a receiver can degrade its noise performance due to reciprocal mixing. Every dB increase in blocker power must be compensated by a dB decrease in the phase noise in order to maintain the same SNR of the design [26]. Thus, better phase noise performance is always appreciated in the RX design unless energy efficient noise cancellation techniques [24,25] can be used.

In a certain protocol, the PN limit set by IFV and blocker can be very different. As in BLE, in order to achieve the 65 kHz 3σ IFV, an 80μW RO with -80dBc/Hz PN@1MHz offset can be used while the blocker specification would require the PN to be less than -110dBc/Hz @1MHz offset and it would be costly to use RO in such designs. But the power consumption of LCVCOs with on chip inductors cannot be reduced further down to several hundred of μW, no matter the performance, or the oscillation can't be sustained. Thus, a general LO solution for both transceiver designs will unavoidably results in extra power

penalty. Thus, standardized asymmetric communication, where the transmitter edge nodes and receiver base-station can be treated separately, will be ideal in a lot of low power applications. The transmitter and its LO on the edge node with limited power sources could be designed according to the IFV PN requirement for ultimate low power at its limit while the receiver base-station with sufficient energies can be designed using the blocker PN requirement for the sake of performance.

An interesting simulation result in section 2.3 shows that a 2 times increase in FSK frequency deviation will offer 6dB relaxation on phase noise requirement, while a doubled data rate will only require an extra 3dB when the noise out of the band is effectively filtered. So simply from the BER perspective, a 'wider' but 'faster' FSK modulation is preferred over the 'narrower' but 'slower' one in ultra-low power short range communications where sensitivity is not the primary concern and the LO power can be saved for a more relaxed PN requirement [22].

2.7. Examples of phase noise requirement from BER's perspective

This section shows examples for verifying the PN limit from the BER's perspective. To verify the accuracy of the system model, more cases are simulated and 2 reference measurement tests are executed. A VSG is used to verify the case for very good phase noise performance and a fabricated chip with a free running RO and a successive approximation (SAR) assisted frequency locked loop (FLL) is used to verify the case for very poor phase noise performance.

2.7.1. A ULP FSK TX with SAR assisted FLL for high PN case

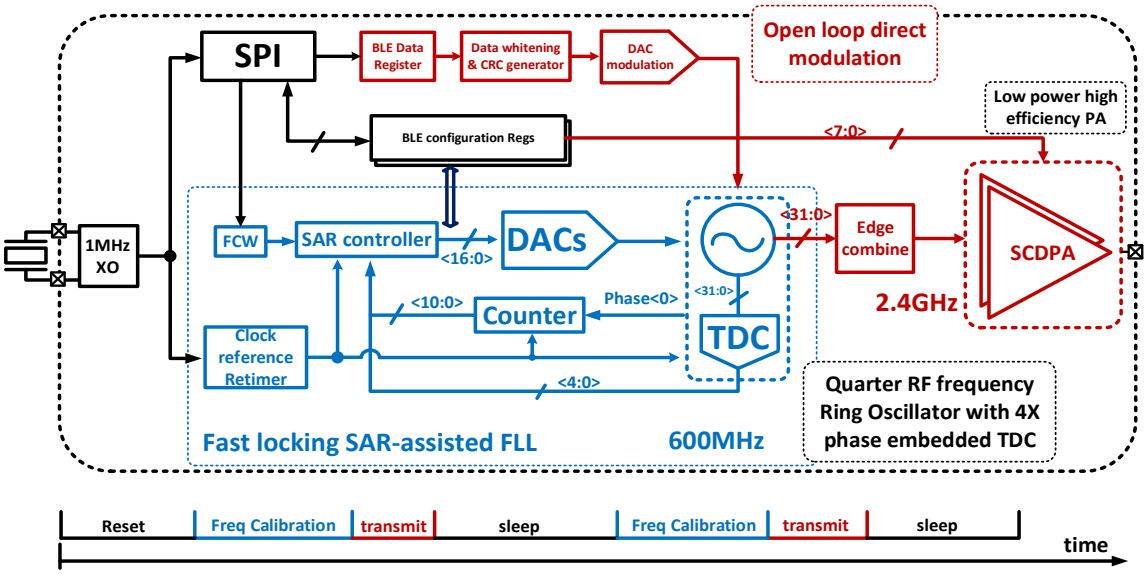


Figure 2-14 Block diagram of the proposed FSK transmitter

Figure 2-14 shows the block diagram of the proposed ULP FSK transmitter. Three major techniques are used to reduce the total power consumption below 1mW: 1) the TX only transmits in one advertising channel packet with open loop direct modulation after every

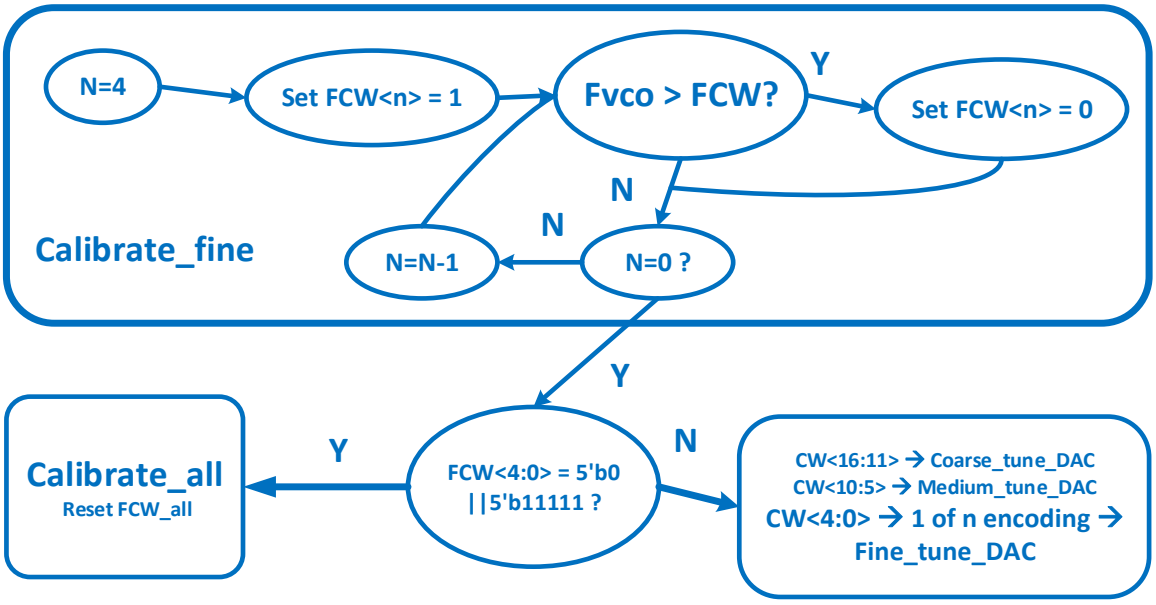


Figure 2-15 Frequency calibration algorithm of the SAR assisted FLL

frequency calibration cycle; 2) a SAR-assisted FLL is implemented by utilizing a RF/4 frequency ring oscillator (RO) with 4X phases; and 3) a switch-capacitor digital PA (SCDPA) is optimized for high efficiency below -5dBm. Figure 2-14 shows the proposed operation scheme and the TX architecture. After being woken up from sleep and configured, the TX will enter a frequency calibration state and the RO will be locked to 600.5MHz within 17µs for initial calibration. Once initially locked, the FLL can re-lock within 5µs using an abbreviated SAR loop. By using a SAR-assisted FLL controller, the exact value of phase error is no longer needed, so the feedback scheme is simplified as long as the sign of phase error is clear. Only the fine tune DAC is re-calibrated in a normal TX cycle after the initial calibration loop has run once, while other DACs are loaded with the previous registered value, achieving a 5µs settling time. However, if during any TX cycle when the fine tune DAC exceeds its boundary, as shown in Figure 2-15, the whole DAC bank will be reset and re-calibrated, resulting in a 23µs settling time.

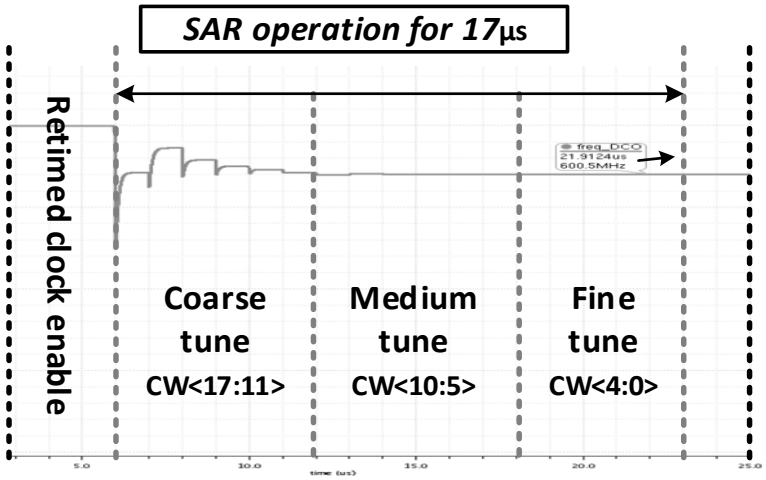


Figure 2-16 simulated frequency vs time of the FLL

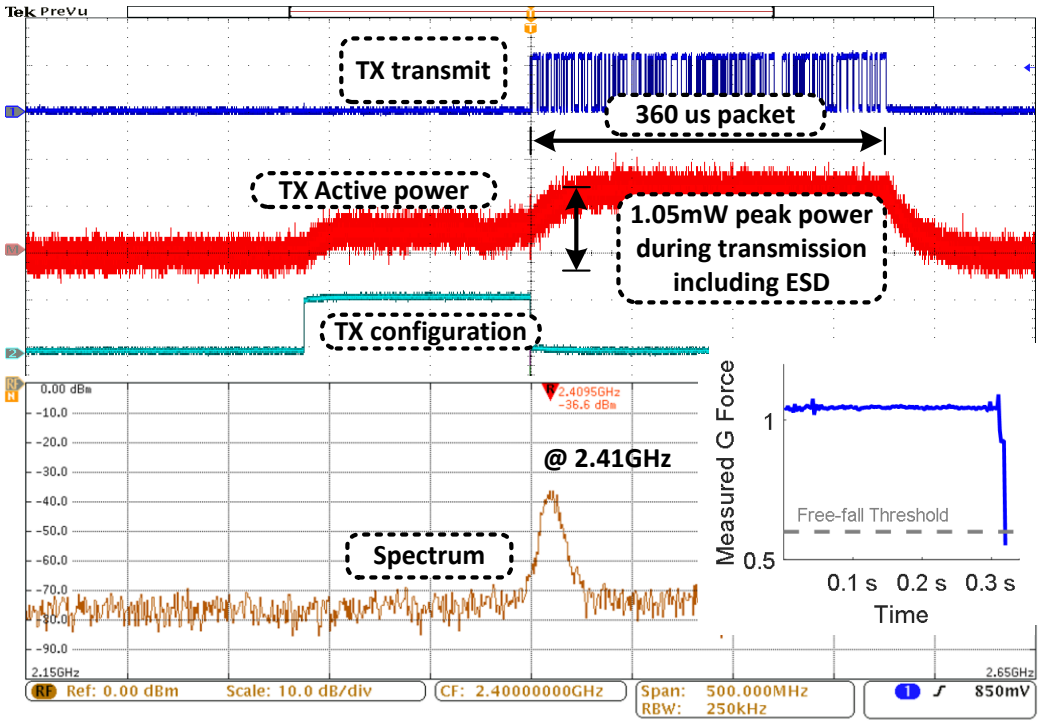


Figure 2-17. Measured transmission of one packet event

The simulated frequency change of the SAR assisted FLL is shown in Figure 2-16. The FLL locks in 17 µs after reset as the initial calibration. Figure 2-18 shows the transmitted data packet and the output spectrum at 2.41GHz. The TX active power at different states are also shown. During the TX configuration state (including data loading from a SPI master), the active power is 634 µW and during the packet transmission state, the total active power is 1.05 mW. During sleep, the SPI is powered off and all other blocks are power gated, giving a 160nW sleep power. The average power consumption of the whole TX, based on a 1s interval between 2 beacon events, is 433nW. The die photo of the test chip is shown in Figure 2-18

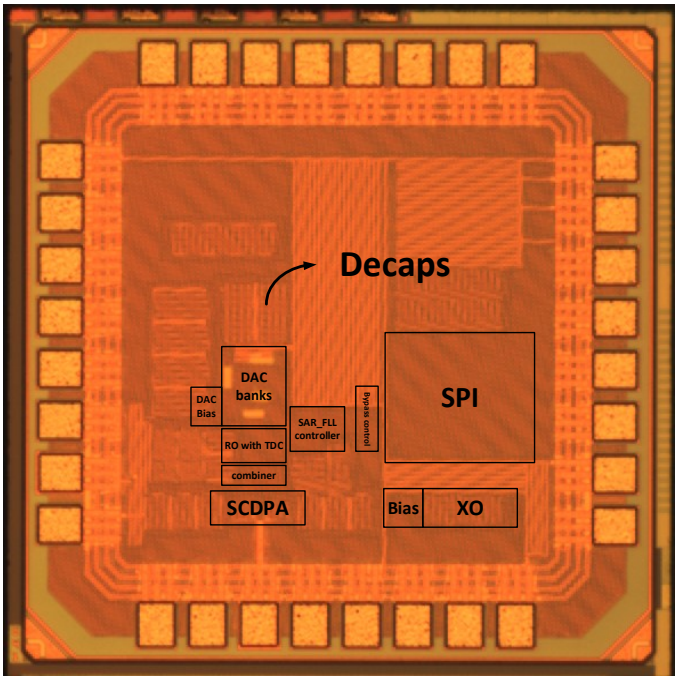


Figure 2-18 Die photo of the proposed FSK transmitter

2.7.2. AWG and VSG for low PN case

An Arbitrary waveform generator (AWG) and a vector signal generator (VSG) are used to generate FSK signals with good phase noise performance to verify the accuracy of the system model. Figure 2-21 shows the influence of both FSK FD and DR on the phase noise requirement. As can be seen for both cases, for a large range of phase noise levels, when FD is doubled, the phase noise requirement can be relaxed by 6dB. But for the influence of data rate, when phase noise is good, doubling DR will require more than a 3dB phase noise improvement. This can be explained by white noise falling into the bandwidth of the baseband filter when the PN is low, which will affect Eb/No, and a 3dB improvement in PN isn't enough to counter the loss of the bit energy. This also agrees with [4].

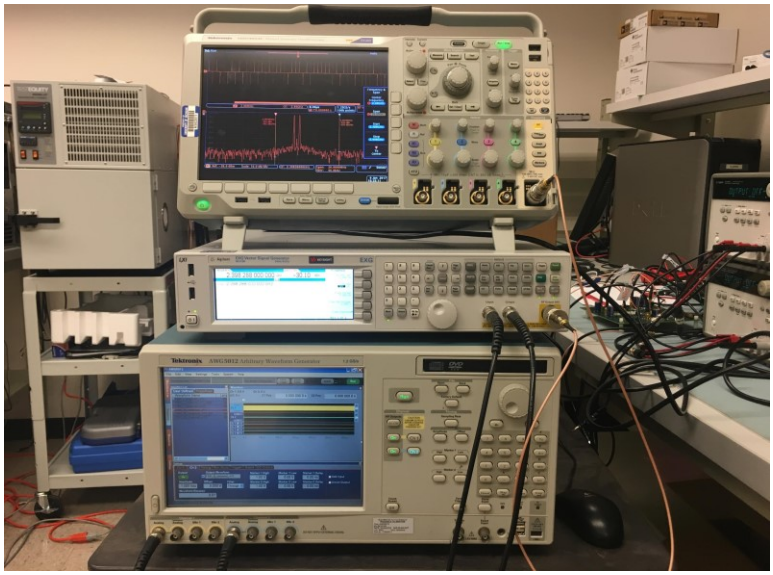


Figure 2-19 Measurement setup for low PN case

For the measurements of the low PN case, an AWG and VSG are used to generate the noisy FSK signal in RF and a mixed domain scope is used to capture the data for demodulation. The phase noise in simulation is set to the same level and noise shape but with the noise floor raised up to -110dBm. Since the PN of a VSG is too good and not tunable, extremely narrow FSK deviations are used to test the model. For the high phase noise case, the chip with a free running RO, which has a PN of -78dBc/Hz @ 1MHz offset, is tested, and compared to simulated results based on a free run RO phase noise shaping. The FD of the RO is fixed at 390 kHz. Decent agreement between simulation and measurement is achieved; measured (top left in black) and modeled (top right in blue) frequency vs time signals at the 2 different PN levels are also shown for visual comparison.

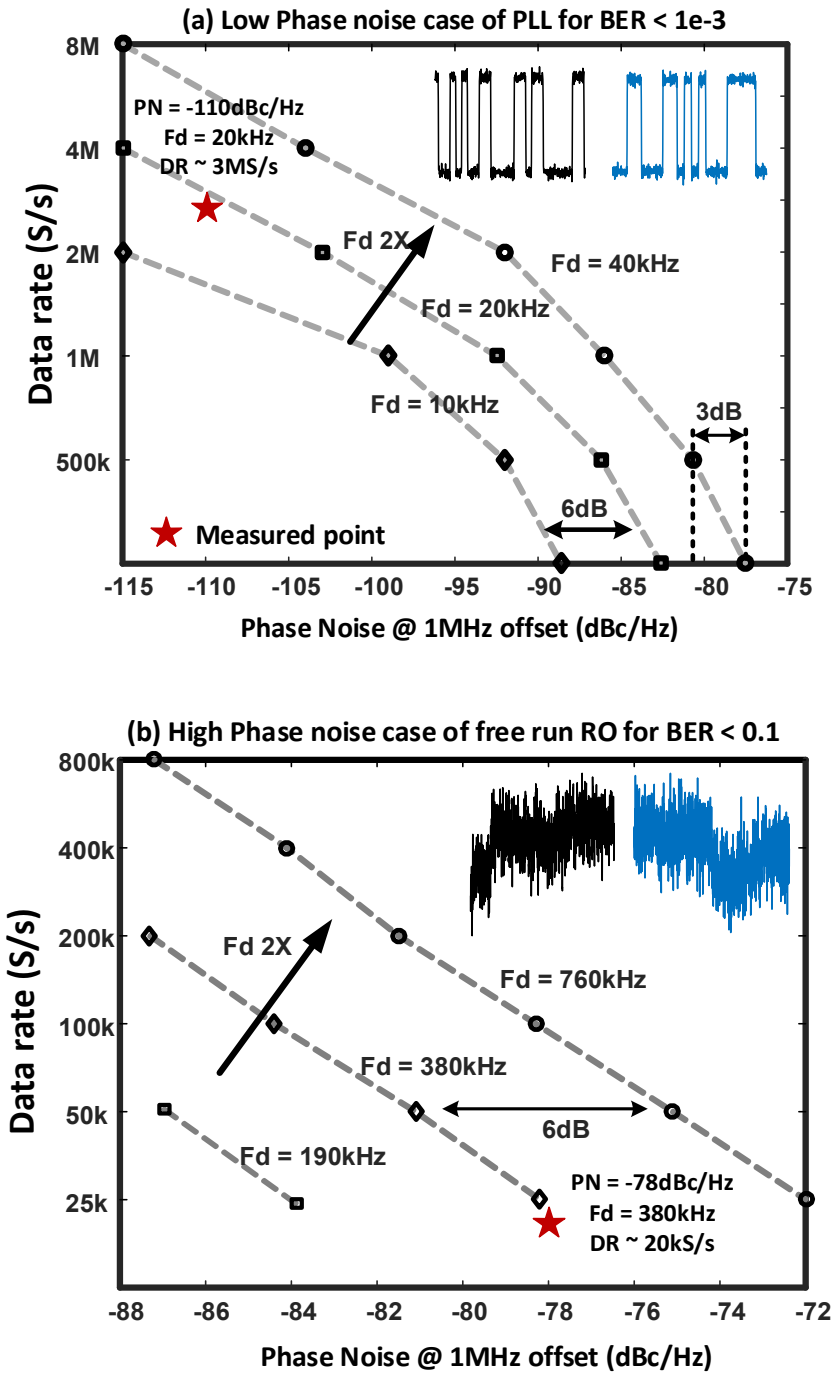


Figure 2-20 FSK FD & DR influence to PN and comparison between simulated and measured results (a) Low phase noise case, and (b) high phase noise case

CHAPTER 3

All digital frequency synthesizer design and modeling in FSK radios

The RF frequency synthesizer is one of the most important and complicated sub-systems in a wireless transceiver, and phase locked loops (PLL) are one of the most widely used architectures in frequency synthesizer designs. Numerous researches in PLL architecture and its sub-circuit blocks [27-42] have been done from different perspectives to enhance its performance and reduce its power. In FSK radios, PLL design is even more critical as it not only directly impacts the system performance in modulation and interference due to phase noise, but also often takes up to 50%-70% of the total power budget. Thus, based on the PN analysis in Chapter 2 from the transceiver level down to its PLL sub-system, it is beneficial to further explore the phase noise relationship between the PLL and its critical sub-circuit blocks as well as noise contributions from each block. Linking the specifications based on noise from the RF transceiver to the PLL sub-system, and further down to the cell level circuit blocks would be extremely helpful to circuit designers in architecture selection, circuit design and overall planning.

3.1. ADPLL architectures for wireless communication

The trend of using all-digital PLLs (ADPLL) in RF wireless communications started roughly a decade ago [43, 44]. The adoption of digital PLLs in clock generation for microprocessors and DSPs, and clock data recovery circuits in wireline communications

has become dominant as well due to its scalability with technology nodes. The bulky loop filter in analog PLLs costs too much area in state-of-the-art designs without offering superior performance. So in this thesis, I will focus on divider-less all-digital frequency synthesizer design and modeling in FSK radios.

There are generally 3 kinds of architectures used in digital frequency synthesizers adopted in wireless communications: ADPLL [43], multiplying delay locked loop (MDLL) [35]/injection locking clock multiplier (ILCM) [45], and digital sub-sampling PLL (SSPLL) [40, 75]. Among them, the ADPLL is the most traditional design that is still widely used in a lot of low power applications such as BLE and WiFi. The MDLL and ILCM are similar architectures that rely on edge replacement from a clean reference phase, thus achieving exceptional PN. But their performance is mainly determined by the reference quality and multiplication ratio, thus it is generally used in digital clocking generation and has gained more popularity recently in high frequency generation for 5G applications [45]. The SSPLL [46-48] replaces the traditional phase detector with a sub-sampling phase detector to sample the time difference as a voltage difference, which successfully removes the divider in the loop and enhances the in-band PN performance. Its digital version uses an ADC as the phase detector for voltage sampling [40].

Due to the edge realigned nature in the MDLL/ILCM, the output phase noise is only determined by the reference noise, VCO noise and locking bandwidth. The locking bandwidth is mainly determined by how frequently the edge is replaced in the MDLL or how strong the injection signal is in the ILCM [49]. It usually possesses a better in-band PN compared to ADPLLs as long as the locking bandwidth is larger. The SSPLL, on the other hand, also possesses superior in-band PN compared to a divider based ADPLL as

there is no noise up-conversion in the divider. However, both the MDLL/ILCM and the SSPLL need the initial frequency to be accurate beforehand, thus, they normally need extra frequency locking loops for pre-locking calibration, which makes them less efficient in low power designs. A divider-less ADPLL on the other hand, as shown in Figure 3-1, possesses no phase detector and no divider noise up-conversion as well, making it an ideal choice for ultra-low power FSK radio designs. The following chapter will be focusing on the noise analysis of the divider-less ADPLL.

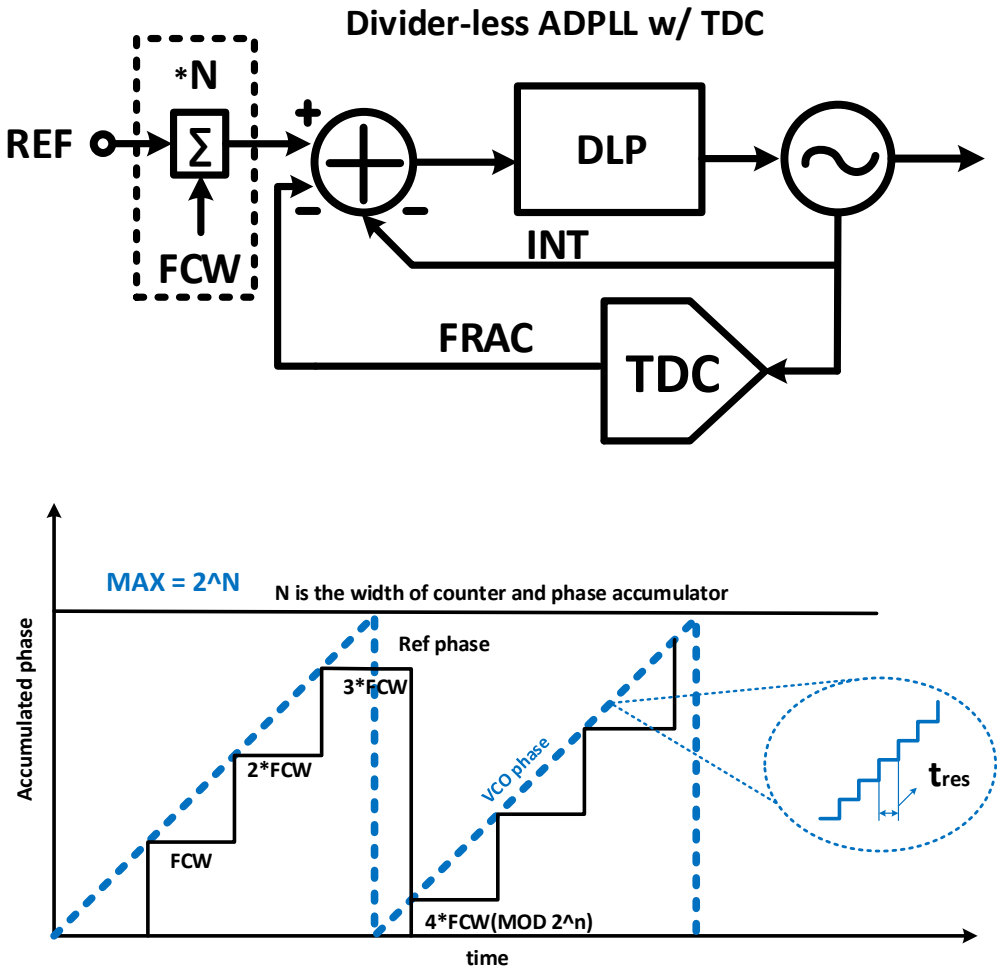


Figure 3-1 simplified block diagram of the divider-less ADPLL and its working principle

The working principle for the divider-less ADPLL is shown in Figure 3-1. Reference phase is accumulated every reference cycle and is multiplied by the frequency control word (FCW), which is set to the equivalent divide ratio in divider-based architectures. A counter accumulates the integer value of the VCO phase every VCO cycle and a TDC is used to sample the fractional value at the same time. Phase error is then calculated based on the difference between accumulated reference phase and VCO phase, and then fed into a digital loop filter. Thus, instead of dividing down the VCO phase for phase comparison, this design virtually multiplies the reference phase by N, so the noise from the TDC won't be up-converted and the in-band PN is enhanced. Reference noise, on the other hand, would still be up-converted at the PLL output.

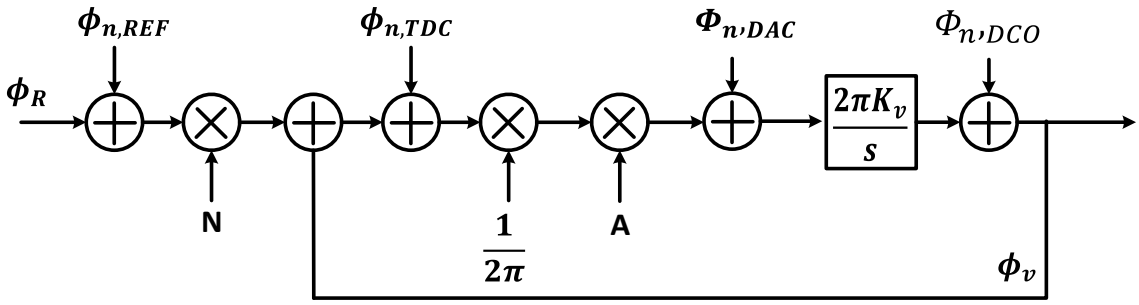


Figure 3-2 Noise model of a type I divider-less ADPLL

Figure 3-2 shows the phase domain model of a type-I divider-less ADPLL with its major noise sources, including reference noise, TDC noise, DAC noise, and oscillator noise. The open loop transfer function can be written as:

$$\mathrm{H(s)} = \frac{1}{2\pi}\mathrm{A} * \frac{2\pi\mathrm{K_v}}{\mathrm{s}} = \frac{\mathrm{AK_v}}{\mathrm{s}} \qquad (3-1)$$

Thus the closed loop transfer function is:

$$STF(s) = \frac{H(s)}{1 + H(s)} = \frac{\mathrm{AK_v}}{s + AK_v} \quad (4-2)$$

Showing a low pass filtering response. The noise from the reference, TDC and DAC are all low pass filtered. On the other hand, the DCO noise is high pass filtered by the following transfer function:

$$NTF(s) = \frac{1}{1 + H(s)} = \frac{\mathrm{s}}{s + AK_v} \quad (4-3)$$

The overall output phase noise is given by:

$$S_{\phi out} = N^2 STF^2 S_{\phi REF} + STF^2 S_{\phi TDC} + \frac{1}{A^2} STF^2 S_{\phi DAC} + NTF^2 S_{\phi DCO} \quad (4-4)$$

Where $S_{\phi out}$, $S_{\phi REF}$, $S_{\phi TDC}$, $S_{\phi DAC}$, $S_{\phi DCO}$ represent the phase noise spectra of the output, reference, TDC, DAC, and the DCO, respectively.

From the phase noise's perspective, the design of the PLL balances different noise sources with the corresponding transfer functions and optimizes for the best noise performance. Within the PLL bandwidth, the in-band PN is determined by the TDC noise floor, DAC noise floor and the high pass filtered DCO noise. Outside the PLL bandwidth, the PN is determined by the DCO noise alone (delta-sigma modulation noise is not considered here). Reference noise will affect the close-in PN at small frequency offset from the carrier (generally smaller than several kHz). As the TDC and DAC noise floor are determined by their own resolution, an in-band PN specification would be enough to determine their design requirements. And the spot phase noise outside the PLL bandwidth can be used to determine the DCO design as well.

3.2. TDC characterization

In open loop operation, the TDC noise floor is from the TDC quantization. Assume the TDC resolution is Δt_{res}, and this quantization noise is uniformly distributed, thus the variance of the timing uncertainty is:

$$\sigma_t^2 = \frac{\Delta t_{res}^2}{12} \qquad (4-5)$$

The standard deviation of introduced phase error is:

$$\sigma_\phi = 2\pi \frac{\sigma_t}{T_V} \qquad (4-6)$$

Where T_V is the period of the VCO. The phase noise floor of the TDC quantization is:

$$\mathcal{L}_{TDC} = \frac{(2\pi)^2}{T_v^2}\left(\frac{t_{res}^2}{12}\right)\frac{1}{f_{REF}} \qquad (4-7)$$

As a special case for the embedded TDC, which are widely used in low power ADPLL designs because it saves the power by not requiring an extra delay line and the delay normalization circuit, equation (4-7) can be simplified as:

$$\mathcal{L}_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{1}{2^N}\right)\frac{1}{f_{REF}} \qquad (4-8)$$

Where N is the number of bits of the TDC. Therefore, with a specific reference frequency, the TDC number of bits can be directly determined by the in-band PN specification. Figure 3-3 shows the filtered TDC noise floor with different resolutions.

The above analysis is the ideal case for the TDC noise floor. In practice, mismatch exists in the TDC delays between each stage. The mismatch due to layout is unavoidable and in the general cases, we can assume it as uniformly distributed. The TDC noise floor including mismatch is thus shown as follows:

$$\mathcal{L}_{\text{TDC}} = \frac{(2\pi)^2}{T_v^2}\left(\frac{t_{res}^2}{12} + \frac{\Delta_M^2}{3}\right)\frac{1}{f_{REF}} \qquad (4-9)$$

Where Δ_M is the mismatch offset from its average stage delay value. In embedded TDC designs, the TDC delay of each stage also suffers from the ring oscillator jitter, so the TDC noise floor will be raised further as a result of this. Since the RO jitter is normally distributed, the TDC noise floor, including oscillator jitter, can be rewritten as:

$$\mathcal{L}_{\text{TDC}} = \frac{(2\pi)^2}{T_v^2}\left(\frac{t_{res}^2}{12} + \frac{\Delta_M^2}{3} + \frac{2}{\pi}\sigma_\tau^2\right)\frac{1}{f_{REF}} \qquad (4-10)$$

Where σ_τ is the rms jitter of the RO. Figure 3-3 shows a 7-bit embedded TDC noise floor with and without the effects of mismatch and jitter.

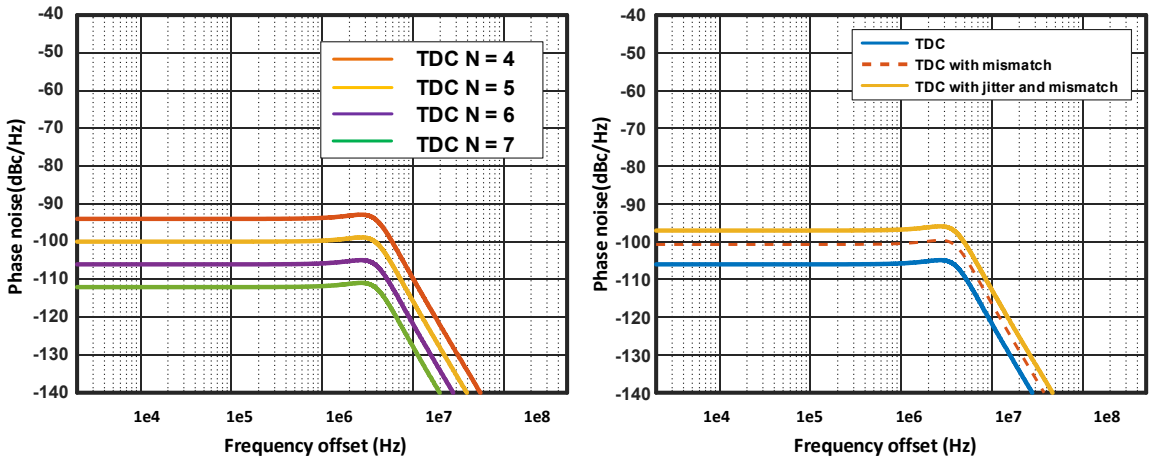


Figure 3-3 TDC noise floor with different TDC bits and non-idealities

3.3. DAC characterization

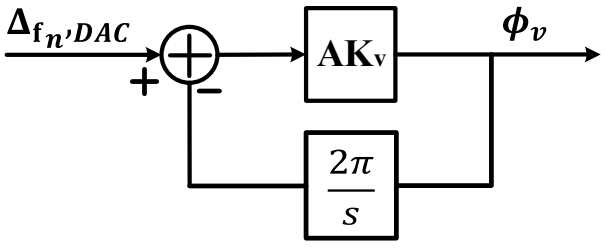


Figure 3-4 DAC quantization noise modeling

The DAC in the PLL offers a similar noise floor as the TDC, as it adds quantization noise in the digital control of the DCO tuning. But its noise's impact in the total in-band PN is relatively small compared to the TDC, since after noise filtering, the noise floor level is brought down by the loop filter. In a type I PLL, the noise floor is reduced by $20\log_{10} A$ according to equation (4-4). Its tuning LSB is related to the frequency resolution of the DCO, so its noise effect can be converted into the quantization effect in frequency domain. Assume the frequency resolution due to the DAC is Δf_{res}, thus the quantization noise variance is

$$\sigma_{\Delta f}^2 = \frac{\Delta f_{res}^2}{12} \qquad (4-11)$$

Thus, according to the closed loop transfer function for the DAC as shown in Figure 3-3, the DAC noise floor is

$$\mathcal{L}_{\text{DAC}} = \frac{(2\pi)^2}{12}\left(\frac{\Delta f_{res}^2}{A^2 K_v^2}\right)\frac{1}{f_{REF}} \qquad (4-12)$$

Considering the mismatch effect in the DAC design, similar to the TDC analysis, the DAC noise floor is

$$\mathcal{L}_{\text{DAC}} = \frac{(2\pi)^2}{A^2 K_v^2}\left(\frac{\Delta f_{res}^2}{12} + \frac{\Delta_M^2}{3}\right)\frac{1}{f_{REF}} \qquad (4-13)$$

Since the DAC value holds constant during each reference cycle, equations (4-12,13) need to by multiplied by the sinc function corresponding to the Fourier transform of the zero-hold operation [43], thus (4-12,13) can be rewritten as:

$$\mathcal{L}_{\text{DAC}} = \frac{(2\pi)^2}{12}\left(\frac{\Delta f_{res}^2}{A^2 K_v^2}\right)\frac{1}{f_{REF}}\left(sinc(\frac{\Delta f}{f_{REF}})\right)^2 \qquad (4-14)$$

$$\mathcal{L}_{\text{DAC}} = \frac{(2\pi)^2}{A^2 K_v^2}\left(\frac{\Delta f_{res}^2}{12} + \frac{\Delta_M^2}{3}\right)\frac{1}{f_{REF}}\left(sinc(\frac{\Delta f}{f_{REF}})\right)^2 \qquad (4-15)$$

Figure 3-5 shows the DAC noise floor with different frequency resolutions assuming a 32MHz reference clock.

In most cases for wireless communications, the DAC tuning resolution is related to the frequency tuning resolution. It is usually the modulation requirement in FSK radios that sets the DAC tuning LSB, and the resulting DAC noise floor is much lower compared to the TDC noise floor (such as in BLE).

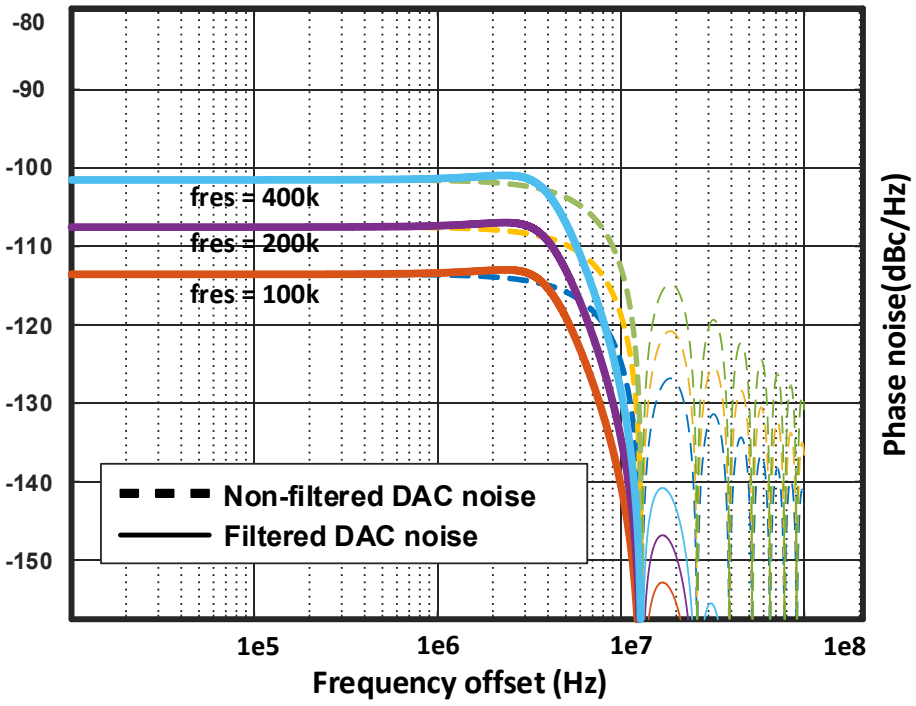


Figure 3-5 DAC noise floor with different frequency resolution

3.4. DCO choices

From the above analysis, the in-band PN defines the specifications of the TDC and DAC. Spot PN specifications from Chapter 2 can be directly used to define the oscillator design in a PLL. There have been numerous researches conducted on oscillators including phase noise, jitter analysis [18, 50-52], and design methodologies [53-55], etc. This section will only roughly talk about circuit choices according to design requirement for a given

FSK application. Figure 3-6 shows the power and phase noise comparison between LCVCOs and ROs based on a 40nm CMOS technology.

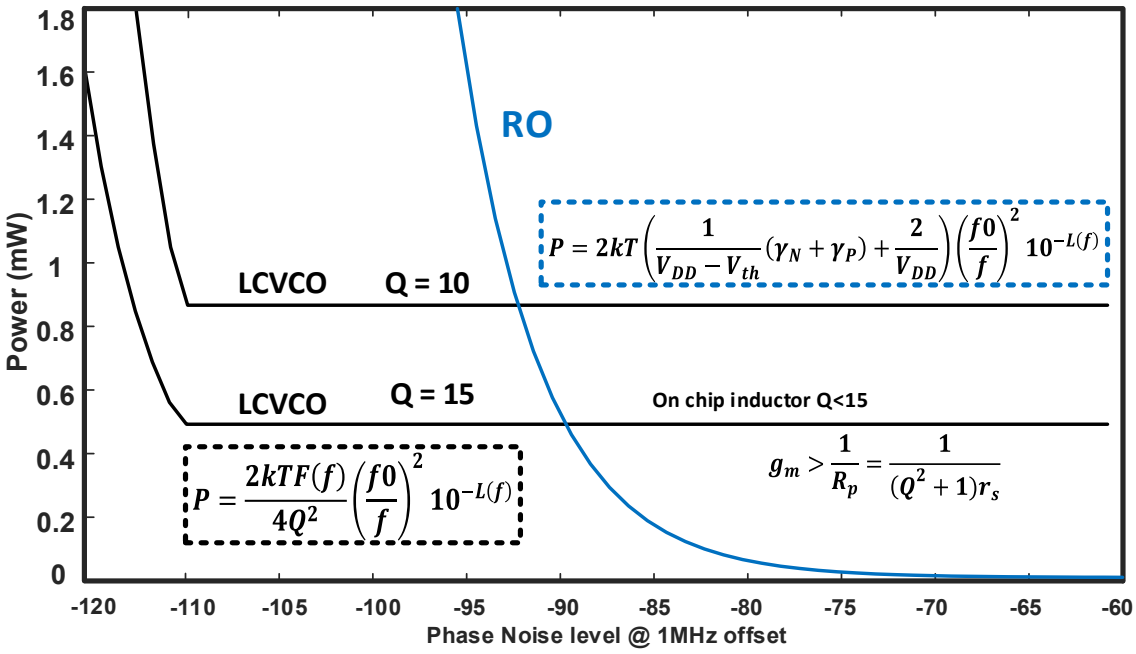


Figure 3-6 power vs phase noise between LCVCO and RO

LCVCOs, due to their inherent advantage in phase noise, are used in most of the standard compliant wireless transceivers. However, their minimum power consumption of >400µW is strictly limited by the quality factor of the integrated LC tank. In state-of-the-art processes, the quality factor of on-chip inductors is < 20, making it impossible to reduce the power consumption any further, no matter the performance, or the oscillation will not be sustained. On the other hand, ROs have the advantage of being able to trade off power for PN and they can further benefit from technology scaling. Recent publications show that ring oscillators can be successfully used in BLE designs with the lowest reported power and area [13]. Moreover, ROs can also be synthesized as all other blocks mentioned in previous sessions using current digital tools, making it possible to synthesize the whole

transmitter with an all-digital class-D power amplifier based on the specification links derived from transceiver level down to circuit blocks.

3.5. Reference noise's influence

In PLL designs, clock references are always treated as ideal sources and the reference noise is always ignored with decent divide ratios. This is because in typical PLL designs, crystal oscillators can offer excellent phase noise across the band and will be low pass filtered at the PLL bandwidth, making it negligible outside the PLL band. Even though the up-converted reference PN will eventually dominate the in-band PN at very small frequency offset, its PN level is still much lower compared to a free running VCO. However, since the reference noise up-conversion is unavoidable in either divider-based or divider-less PLLs and is scaled by the frequency multiplication ratio, as shown in Figure 3-7, it is still necessary characterize its influence in PN and IFV discussed in chapter 2.

As shown in Figure 3-7, with different divider ratio N, the reference noise is moved up by $20\log_{10} N$. Increasing N or using a high noise reference will increase the total noise even though other noise sources are properly regulated by the PLL. When the up-converted reference noise is still smaller than the free running VCO noise, the IFV can be considered as:

$$\sigma_f^2 < 4BW_{rx}\mathcal{L}_{VCO}(f)f^2 \qquad (3-16)$$

And when it exceeded the VCO noise, the IFV is thus:

$$\sigma_f^2 = 4BW_{rx}\mathcal{L}_{REF}(f)f^2N^2 \qquad (3-17)$$

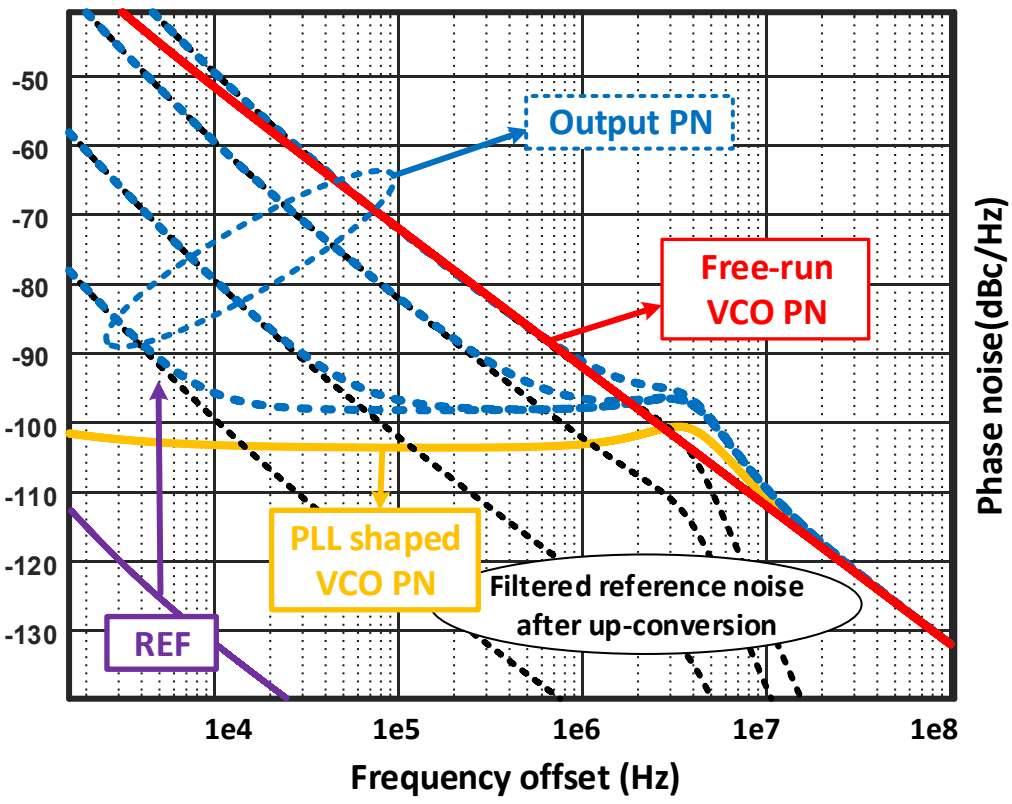


Figure 3-7 Reference noise's influence in total output PN

In PLL designs with proper reference, it is not likely to have the reference noise dominate the total output PN. However, crystal-less (XO-less) designs have been becoming desirable in a lot of standard compliant radio designs to further reduce the cost of wireless IoT product, by using an carefully calibrated LCVCO as the RF LO [14, 38]. They either use a kHz real time clock (RTC) or a relatively high frequency relaxation oscillator as the reference for RF frequency calibration, which will unavoidably result in a high PN up-converted reference because of the large N or noisy reference.

CHAPTER 4

An Ultra-Low Power Bluetooth Low-Energy Transmitter with Ring Oscillator Based ADPLL and 4X Frequency Edge Combiner

4.1. Introduction

Because of its versatility and practicality, Bluetooth Low-Energy (BLE) is becoming more popular as the wireless communication protocol for Internet-of-Things (IoT) applications [56-66]. The recently finalized Bluetooth 5.0 standard enables a faster data rate, more versatile advertising channel interactions, and an extended communication range [12], which makes BLE radios more adaptive in IoT designs. However, state-of-the-art BLE designs still consume an average of 4-5mW active power [56-61] while commercial BLE SoCs consume more than 10mW, limiting battery life and placing a ceiling on their adoption into IoT devices. In applications that require extended battery life or self-powered operation via energy harvesting such as wireless body sensor networks (WBSN), implantable medical devices, and disposable consumer electronics, BLE radios consume too much power to be adopted at a large scale. In such systems, ultra-low-power (ULP) radios with proprietary asymmetric communication protocols are used [67-70] to save power in the edge nodes while pushing all the computation and power into the base station. But these designs either suffer from a significantly lower data rate, more severe interference and multiple access issues, or an extra bulky aggregator. Thus, it's very beneficial to explore a way to further reduce the BLE radio's power consumption,

especially the BLE transmitter (TX), and enable a standard compatible asymmetrical communication with a sub-mW BLE TX in the edge-nodes and fully compliant BLE transceivers in a cellphone or tablet as the base station. It will not only save a significant amount of power and extend the lifetime of IoT SoCs, but could also help resolve the interference and base station issues in ULP wireless systems.

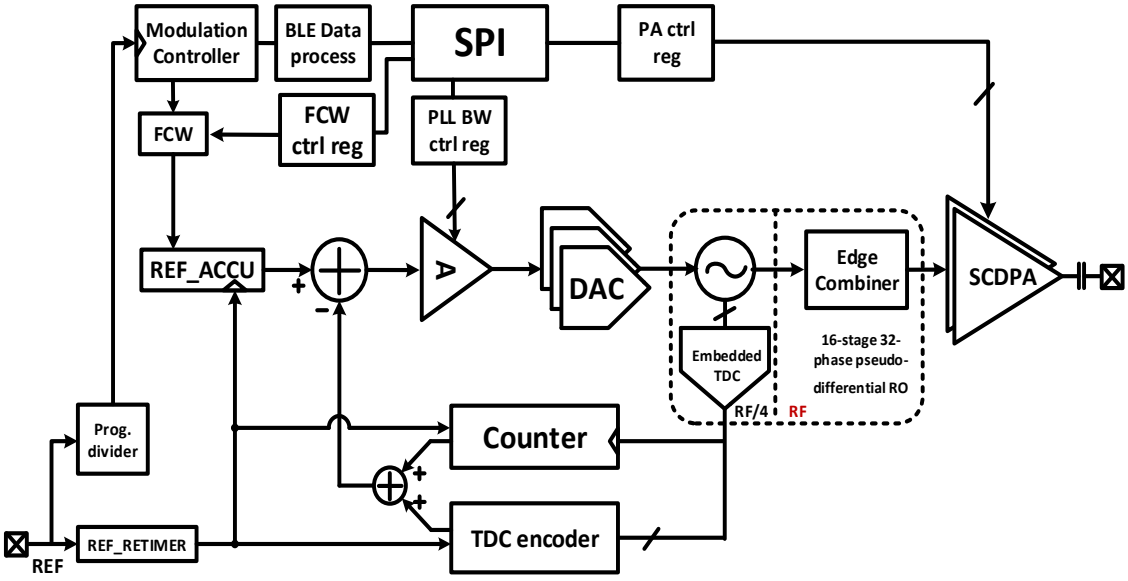


Figure 4-1 Block diagram of the proposed RO-based all-digital BLE transmitter

The bottleneck of further power reduction in BLE TX design mainly results from 2 building blocks: the local oscillator (LO) and the power amplifier (PA), which typically take more than 80% of the TX power consumption combined. Significant effort has been spent on the phase-locked loop (PLL) design for BLE [71-74]. Some state-of-the-art ADPLL designs have successfully broke through the 1mW barrier [72, 73]. But due to the use of LC voltage-controlled oscillators (LCVCO) which are implemented with on chip inductor whose quality factors are <20, power cannot be reduced further, no matter the performance, because oscillation cannot be sustained. A recent trend shows that more and more BLE designs prefer to use open-loop LCVCO designs with direct modulation [59,

65], since its phase noise (PN) performance is more than enough for BLE. In normal cases, the LO PN requirement for a BLE TRX is determined by the receiver (RX) side due to the requirements in RX sensitivity, blockers, and reciprocal mixing, and it's always better to have a better PN. But for a BLE TX-only prioritized design, the PN limit for the LO has not been studied. This is especially true if this TX is in an asymmetric network where the RX LO in the "base-station" is often overprovisioned with high PN tolerance.

This chapter will address this issue by giving a detailed analysis between phase noise and system level specifications for a transmitter, using a similar method as in [18, 22]. The relaxed PN limit for BLE TX will not only help bring down the TX power consumption to its physical limit, but also increases flexibility in BLE circuit design based on the application emphasis. Based on the analysis, we propose the first-ever reported RO-based BLE TX [24] with a ULP wideband type I ADPLL using a 32-phase $f_{RF}/4$ RO, which not only forms a 5-bit embedded TDC but also serves as a 4X frequency edge combiner. It reduces the PLL power and improves its PN at the same time. To further reduce PA power consumption, we utilize a switch-capacitor digital PA (SCDPA) [81] with a matching network optimized for low power operation achieving a high efficiency. The BLE TX consumes 486 μW while configured as a non-connectable advertiser, which is desirable for short-range TX-only beacon devices in an asymmetric BLE network. Its functionality has been validated by wirelessly communicating beacon messages to a mobile phone.

This chapter is an extension of [13], and is organized as follows. Section 4.2 discusses the system level design considerations. Section 4.3 talks about detailed circuit design and trade-offs to achieve low power and the required noise performance. Section 4.4 discusses

the measurement results and the comparison to the state-of-the-art. Finally, Section 4.5 draws the conclusion.

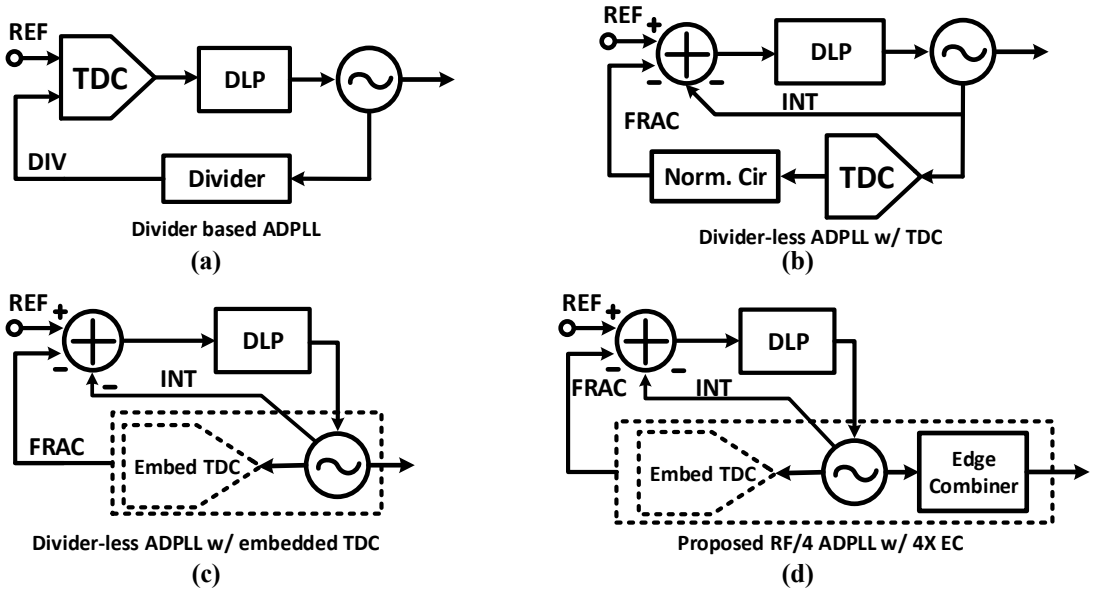


Figure 4-2 Simplified block diagram of different ADPLL architectures: (a) Divider based ADPLL with TDC as the PD. (b) Divider-less ADPLL with TDC. (c) Divider-less ADPLL with embedded TDC. (d) Proposed ADPLL with quarter frequency OSC and 4X edge combiner

4.2. System level analysis for the proposed RO based BLE TX

4.2.1. Proposed ADPLL architecture

In order to achieve the target PN using a noisy RO rather than the generally used LCVCO, the PLL design for the BLE transmitter is critical. Even though the major noise source is the VCO PN, other building blocks also need to be carefully dealt with, especially for low power designs. Figure 4-2 shows 4 different architectures of the TDC based ADPLLs. The divider based ADPLL [76] shown in Figure 4-2(a) needs a relatively high power divider and suffers from divider noise folding as well as reference noise up-conversion. For fractional operation, an extra Delta-Sigma Modulator (DSM) is needed for the divider. Thus, this is a relatively a power hungry choice. The divider-less ADPLL [77]

shown in Figure 4-2(b) directly uses a TDC to generate the fractional error. This architecture effectively removes the noise contributed from the divider and the DSM, but a TDC running at RF frequency consumes a significant amount of power as well, let alone an extra normalization circuit. Advanced designs [71, 72] in this architecture effectively reduce the TDC power consumption while maintain an excellent noise performance by introducing a DTC and snapshot circuit, but the timing misalignment and non-linearity of the DTC and TDC will introduce spurs. The pre-calibration circuit will result in extra power consumption, thus, making it hard for further power reduction. As for the architecture shown in Figure 4-2(c) with an embedded TDC [78], the power is saved by removing the explicit TDC and the normalization circuit. However, the TDC resolution is limited by the number of RO stages at high frequency, which will result in a relatively high in-band phase noise for high frequency applications.

Figure 4-2(d) shows the simplified block diagram of the proposed ADPLL to address the above issues. The detailed block diagram is already shown in Figure 4-1. To achieve the targeted frequency variation error with the RO, a 5MHz bandwidth ADPLL for aggressive in-band phase noise suppression is implemented. It features a fast settling time and direct reference phase modulation at the frequency control word (FCW) since the PLL BW is much larger than the modulation BW. The BW is programmable by changing the loop filter gain through a SPI interface, as shown in Figure 4-1. Several techniques are used to save the PLL power and enhance its in-band PN at the same time. The RO is designed at a frequency of $\frac{f_{RF}}{4}$ and implemented with a 16-stage pseudo-differential architecture with 32 phases directly used as an embedded TDC. Its phases are also used in a windowed edge combiner (EC) for 4X frequency multiplication to produce the 2.4GHz RF frequency.

The lower frequency RO further saves the power of the embedded TDC. It prevents the noise folding effect from happening in the divider based PLL, thus improving in-band PN performance. At the same time, the high power explicit TDC and its delay normalization circuits are also saved, and the TDC performance can be relaxed by dealing with the same amount of jitter at a lower frequency while maintaining the same resolution. The low frequency embedded TDC and the extra edge combiner consumes less power compared to the normal frequency embedded TDC design from simulation , and it can maintain the low flicker noise corner from the low frequency RO, which will again, enhance the in-band phase noise [79]. However, extra deterministic jitter will be introduced because of the mismatches in the different paths of the EC, as modeled in Figure 4-3. And due to periodical phase shifts, the EC will also introduce spurs at $\pm f_{RF}/4$ off the center frequency. Its negative effect will be analyzed in more detail in B.

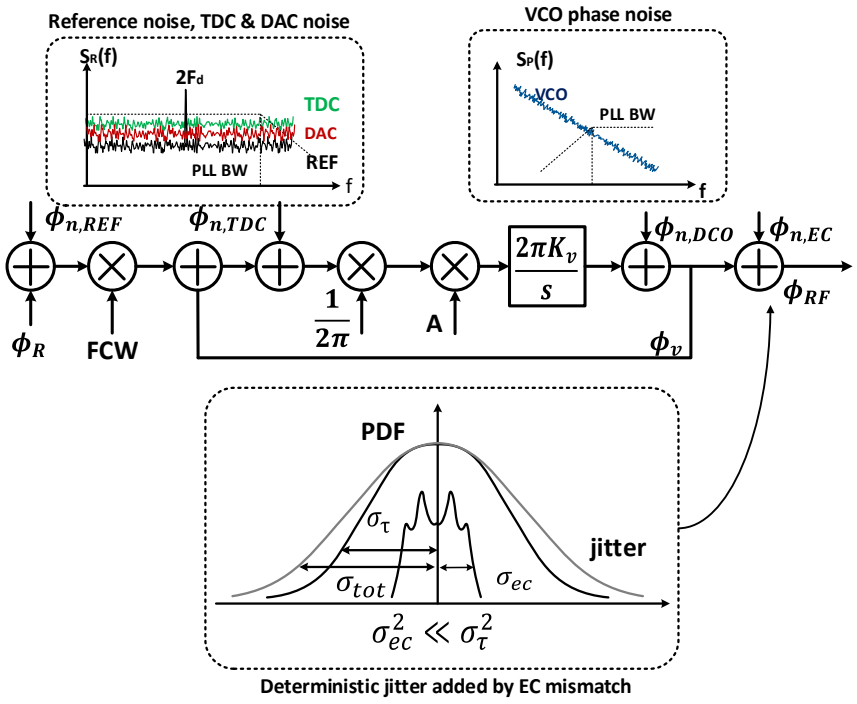


Figure 4-3 System level noise analysis with different noise sources including reference noise, TDC noise, DAC noise, VCO noise and EC noise.

4.2.2. Noise analysis with the edge combiner and the quarter RF frequency embedded TDC

Major noise sources are modelled for the PLL, as shown in Figure 4, including reference noise, TDC noise, DAC noise and RO phase noise. The PLL is designed to achieve a 5MHz BW with a -85dBc/Hz in-band PN after edge combining. In this design, the in-band PN is dominated by both the RO and TDC. The TDC noise floor is around -100dBc/Hz with the 5-bit resolution at quarter RF frequency, which is comparable to the in-band PN of the quarter frequency RO, as shown in Figure 4-4. Ideally, the relative noise floor difference between RO and TDC are the same with or without the quadruple effect. However, since the absolute delay offset due to layout mismatch, loading variation and RO jitter are the same, the actual TDC noise floor is slightly enhanced in the quarter frequency RO architecture due to the larger VCO period:

$$\mathcal{L}_{\mathrm{TDC}} = \frac{(2\pi)^2}{T_v^2}\left(\frac{t_{res}^2}{12} + \frac{\Delta_M^2}{3} + \frac{2}{\pi}\sigma_\tau^2\right)\frac{1}{f_{REF}} \qquad (4-1)$$

Where $\mathrm{t_{res}}$ and $\mathrm{T_v}$ is the TDC delay and the VCO period, and Δ_M correspond to the average mismatch. Here the mismatch is assumed as uniformly distributed. And for the embedded TDC, the jitter on the TDC edges follows the Gaussian distribution of the RO output. Since the delay, jitter and average mismatch are not correlated, the actual TDC noise floor with and without quarter frequency multiplication are shown in Figure 5 (a), assuming a 10ps rms jitter for the RO at 2.4GHz. And after frequency multiplication, the in-band PN at 2.4GHz output is slightly improved compared to a normal frequency embedded TDC as a reference (edge combined PN vs 2.4G RO w/ 3b-TDC PN). The DAC resolution is restricted by the modulation, thus, the DAC noise floor is pretty low. And

because of the divider-less nature of this design, its noise won't be up-converted as a problem.

The edge combiner, due to loading mismatch, will add a certain delay 'D' for each path. Thus the variance of the timing uncertainty from one path is:

$$\sigma_{\tau_{\mathrm{EC}}} = \frac{(D)^2}{12} \qquad (4-2)$$

In the worst case, there will be 3 phases with positive delay and 1 phase with negative delay, or vice versa. Thus the worst case delay is 3D in (16). The phase uncertainty is:

$$\sigma_{\phi_{\mathrm{EC}}} = \frac{2\pi\sigma_{\tau_{EC}}}{T_v} \qquad (4-3)$$

So the worst case phase noise introduced by the EC is:

$$\mathcal{L}_{\mathrm{EC}} = \frac{(2\pi)^2}{12}\frac{(3D)^2}{T_v^2}\frac{1}{f_V} \qquad (4-4)$$

It shows that the EC will add an extra non-filtered noise floor in the overall PN output due to the path delay from layout mismatch. But in practice its level is relatively low compared to other noise sources unless the farout PN is of concern. Monte Carlo simulations for the EC show that the average delay offset is around 1.5 ps, and 1.7ps calculated from indirect open loop PN measurement, which translates into an EC added noise floor of around -125dBc/Hz. Thus the EC noise basically doesn't contribute to the in-band PN. The far out phase noise floor discrepancies between simulated and measurement result shown in Figure 4-5 & (c) are mainly due to the instrumental noise.

From a time domain perspective, the EC-introduced jitter is much smaller than, and not correlated with, the random jitter from the high-PN RO. The windowed EC won't affect the overall RF performance in the random noise region. In this design, in order to balance the phases offset and improve the EC spur performance, dummies are added to each RO

phase output and the layout of the RO has been carefully designed with symmetry. Furthermore, extra loadings were added to each phase output after PEX extraction. Figure 4-5 shows the simulated PLL noise performance versus the model from the above analysis and Figure 4-6 shows the measured PN of the proposed ADPLL. The phase noise performance corresponds to a 68.1kHz $3\sigma_f$ IFV, which is close to the target design. The spur level is equal to $20\log(\Delta t/T_v)$ according to [80, 83], where Δt is the average delay mismatch associated with each combined output phase, so it can be estimated that the typical spur level is around -49dBc according to simulation. With this $f_{RF}/4$ RO and edge combiner architecture as well as the 5b embedded TDC, the PLL controller's power consumption is 253μW in a 40nm technology.

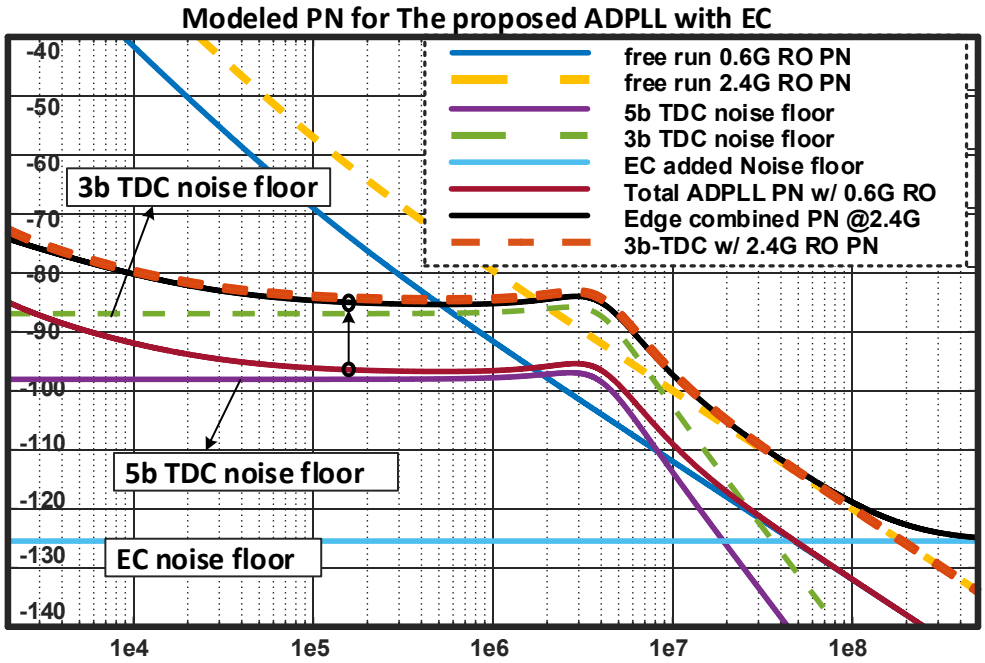


Figure 4-4 Noise performance of the proposed ADPL – Modeled different phase noise sources.

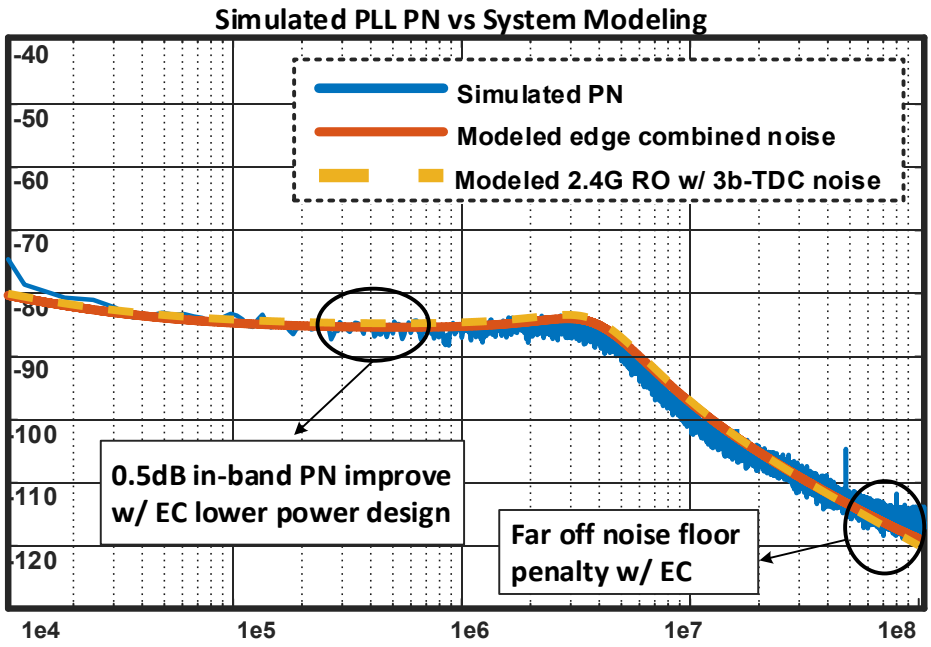


Figure 4-5 Noise performance of the proposed ADPLL – Simulated vs Modeled total phase noise.

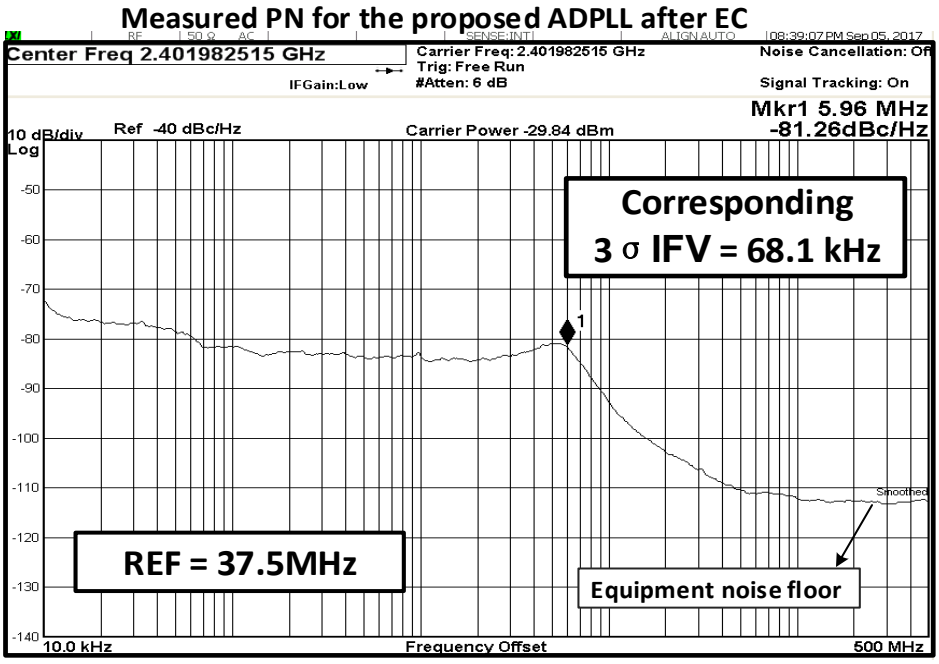


Figure 4-6 Noise performance of the proposed ADPLL – Measured phase noise with corresponding IFV

4.3. Circuit implementation

4.3.1. Ring oscillator

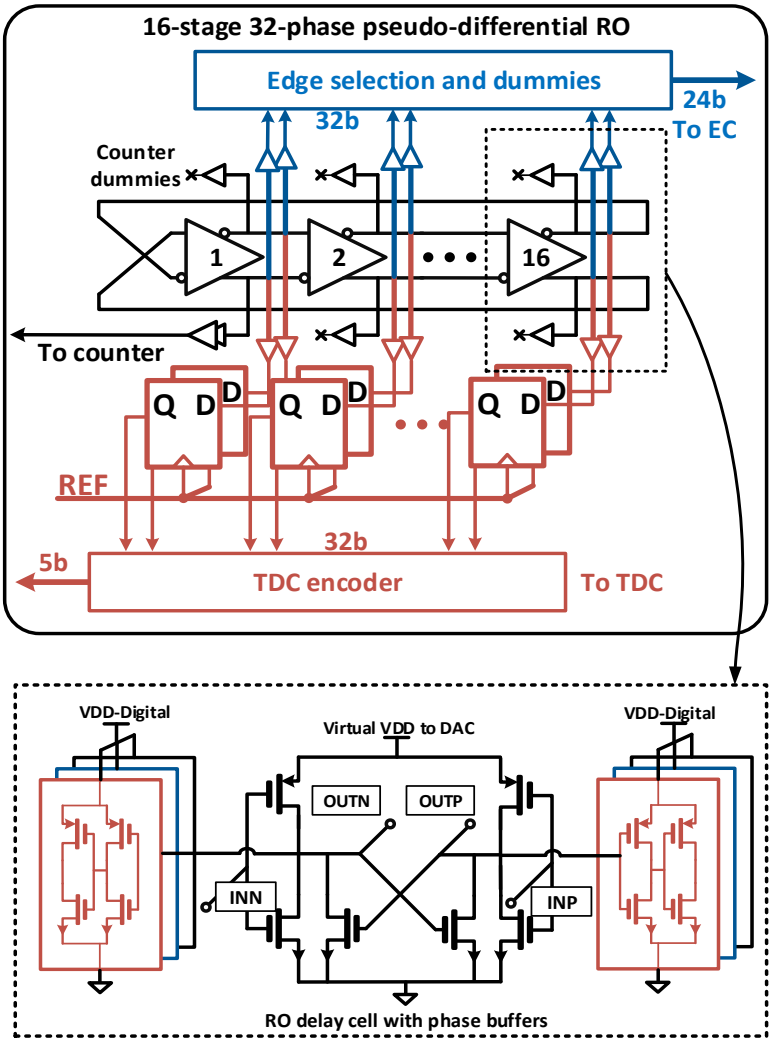


Figure 4-7. Proposed 16-stage pseudo-differential ring oscillator block and the RO delay cell with buffers

The detailed circuit design of the 16-stage pseudo-differential RO is shown in Figure 4-7. All the 32 phases are buffered out and directly sampled by 32 D flip-flops at the reference clock as an embedded TDC [78] without extra delay lines. Then the 32b outputs are encoded to form a 5b binary output as a fractional phase error sampler. One phase output is sent to the counter for integer phase error calculation, while the rest phases are

connected to dummies for a balanced output to minimize the TDC DNL. On the other hand, all phases are also buffered out to an edge selection circuit, where 24 of them are arranged and fed to the edge combiner while the other 8 phases are connected to dummies too. The RO cell is implemented with 2 inverter stages for each cell and NMOS-only cross couple pairs rather than cross coupled inverters for minimized loading. And each cell has 6 buffered outputs for TDC, EC and counter (or dummies). This helps achieve the best balance among speed, PN and power efficiency for the RO.

4.3.2. Current steering DAC

The current steering DAC for digital RO tuning is shown in Figure 4-8. The DAC is one of the most important circuit blocks for the PLL noise performance since supply and bias noise are critical to ring oscillator based designs. Since the PLL BW is very large for in-band PN suppression and direct reference phase modulation, the decap on the virtual VDD of the RO has to be fairly small to keep the PLL loop stable, thus plenty of noise from the supply and the bias network will pass through. To deal with this, the coarse DAC bank is designed at the edge of the triode region to minimize the noise gain while the medium and fine DAC banks are designed in the saturation region to keep the required tuning linearity while the PLL is locked. Additional large decaps are added to the gate of the DAC cells to filter the accumulated supply and bias noise. The medium and fine current steering DACs are 6b each that covers 70MHz range with approximately 20kHz LSB tuning step for the RO and the coarse DAC is 4b and can cover up to 300MHz.

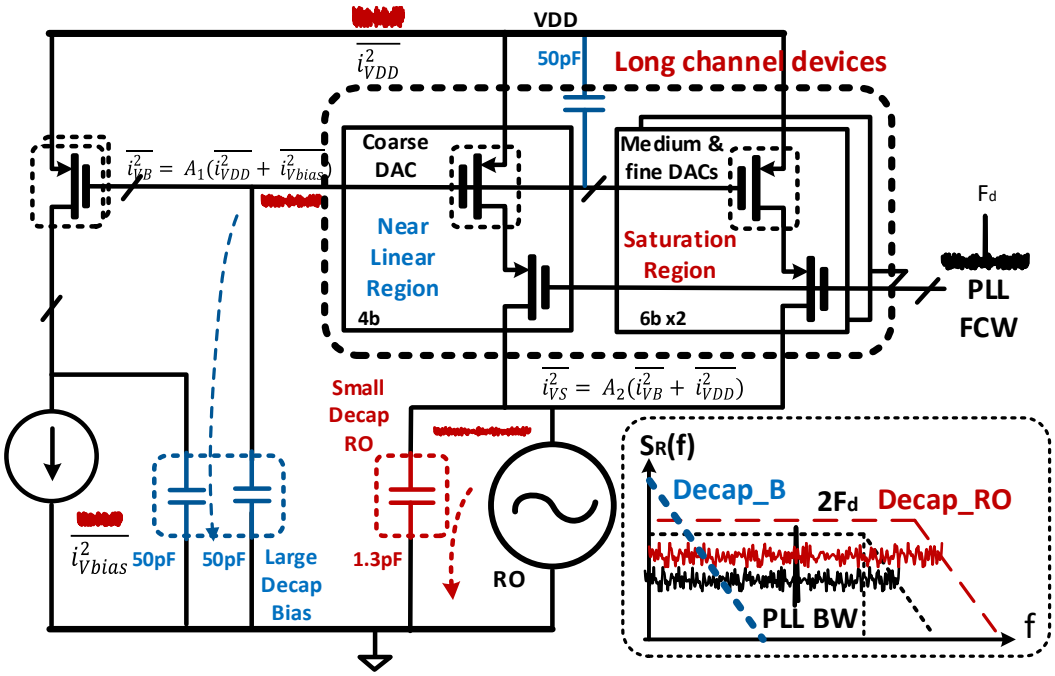


Figure 4-8 Current steering DAC for RO tuning and its major noise contributions

4.3.3. Edge combiner

Figure 8 shows the windowed edge combiner. In the 24 phases of the RO input, 6 phases are used for each rising and falling edge to be combined, in which the 2 windows are spaced by 4 RO delays and the window width is 5 delays to ensure all selected phases pass through in different PVT corners. Tristate gates are used to pass the selected phase and buffer the interference from other phases. The timing diagram for edge combining is shown in Figure 4-9. In this design, the EC consumes just 20μW from simulation and its added jitter is much smaller than the RO jitter itself, keeping the RF output in the random noise region. In applications where the EC jitter is comparable to the oscillator jitter, then it cannot be treated as working in the random noise region for frequency multiplication. Power has to be traded off for mismatch in the EC circuit design according to system requirement.

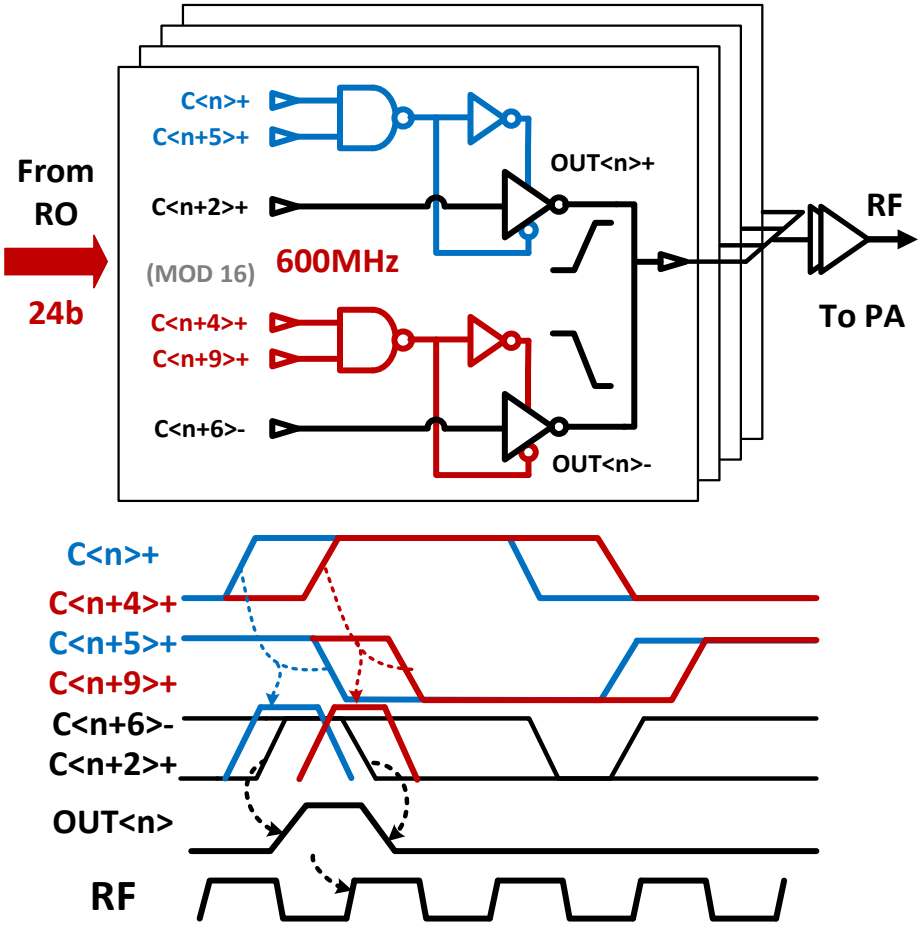


Figure 4-9 Schematic of the edge combiner block and its working principle

4.3.4. Switched capacitor digital power amplifier

A class-D switch-capacitor digital power amplifier [81] is utilized in this design due to its robustness, low cost and great performance in efficiency. Compared to other switching power amplifiers, even though the class-D does not possess the highest efficiency, it is more robust and less susceptible to driving transistor parasitics, PVT variations and matching. And with the supply sensitive ring oscillator implementation in the LO, class D is more reliable due to its relatively low output swing. As there is no on-chip resonant component, it is more suitable for low cost fully integrated solutions and can benefit from advances in technology scaling with better switches. The efficiency of this kind of PA is related to the ratio of the loading impedance and on-resistance of the driving transistor

minus the power of the harmonics, thus, it is more versatile in matching schemes to achieve the highest efficiency at a targeted output power based on application emphasis. For example, higher loading impedance results in a low maximum output power but helps with efficiency in low output power levels. Different from the typical SCDPA design [81], where series capacitors are within each PA cell, this design utilizes a shared capacitor bank to prevent extra output power loss due to the grounded capacitors in the off PA cells. As shown in Figure 4-10, the SCDPA is thermometer coded with 8-bit cells and is matched and optimized for the highest efficiency for -10dBm operation, which is sufficient for 2-3 meters short range communication.

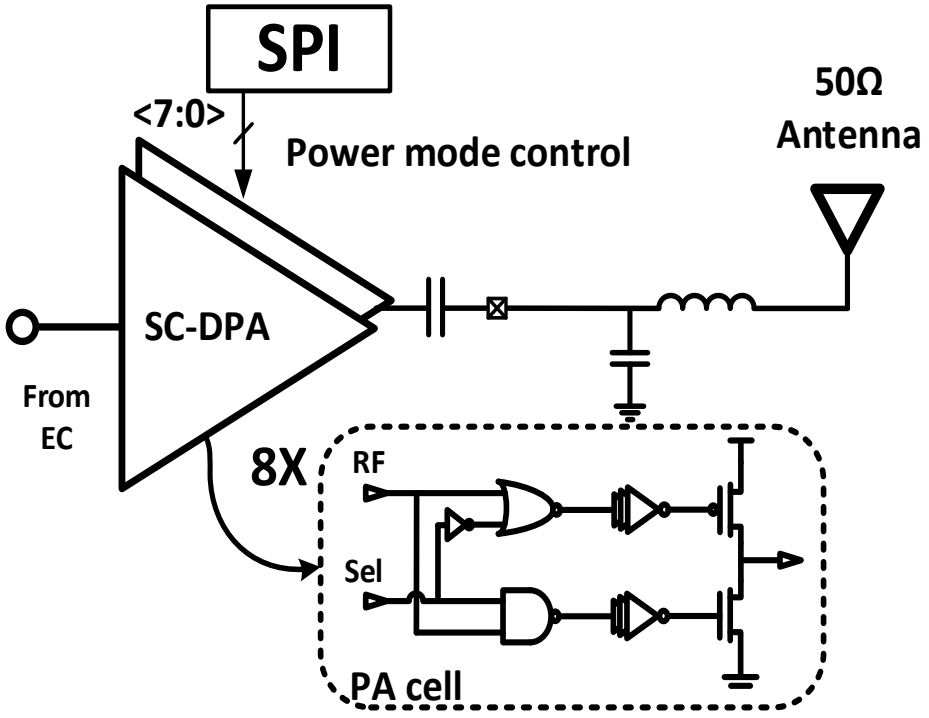


Figure 4-10 Programmable switch-capacitor digital power amplifier and schematic of the PA cell

4.4. Measurement results

The proposed BLE transmitter is fabricated in 40nm CMOS and the die photo of the prototype chip is shown in Figure 4-11. The core area of the TX is 0.0166mm2. The

measurement results are shown as follows. Figure 4-12 shows the measurement of the open loop (a) and closed loop (b) phase noise performance of the proposed ADPLL. When the RO is free running at 494MHz, the PN @ 1MHz offset is -95dBc/Hz and the EC output at around 2GHz is -83dBc/Hz, with the noise corner both at around 1MHz. The PN of the ADPLL is shown in (b). It's locked at 600.5MHz with a 37.5MHz reference. The PLL bandwidth is around 5MHz and the measured in-band PN of the oscillator and the EC output at 2.402GHz are -96dBc/Hz and -85dBc/Hz, respectively.

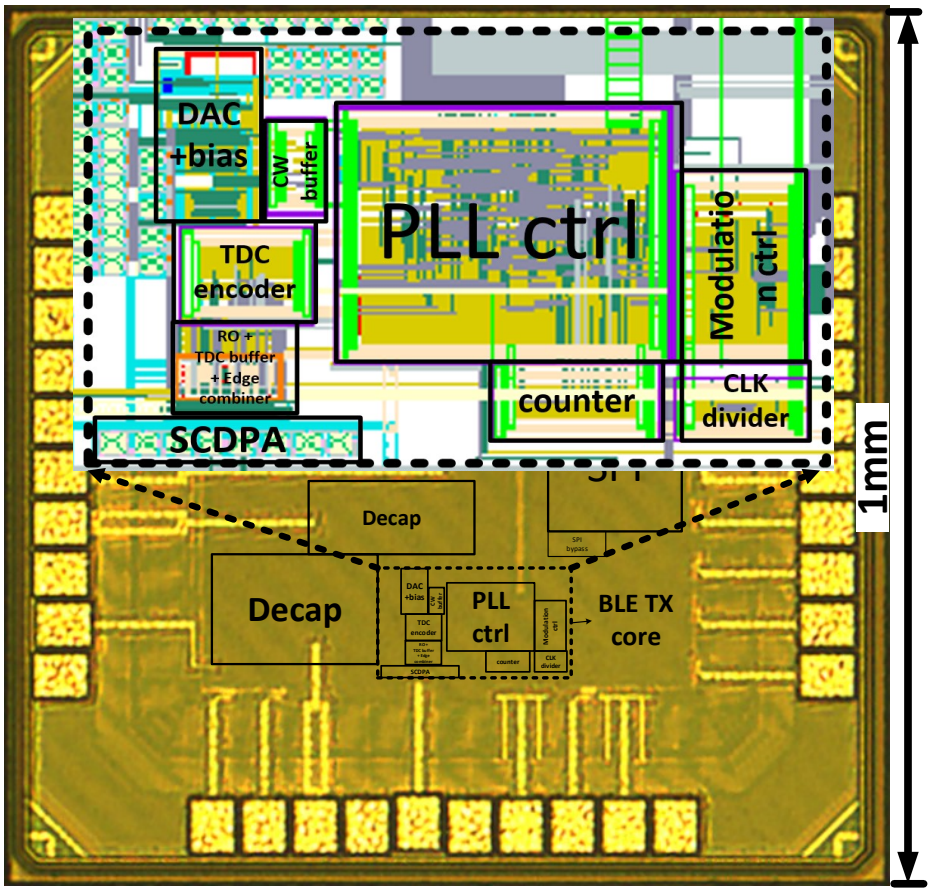


Figure 4-11 Die photo of the proposed BLE transmitter

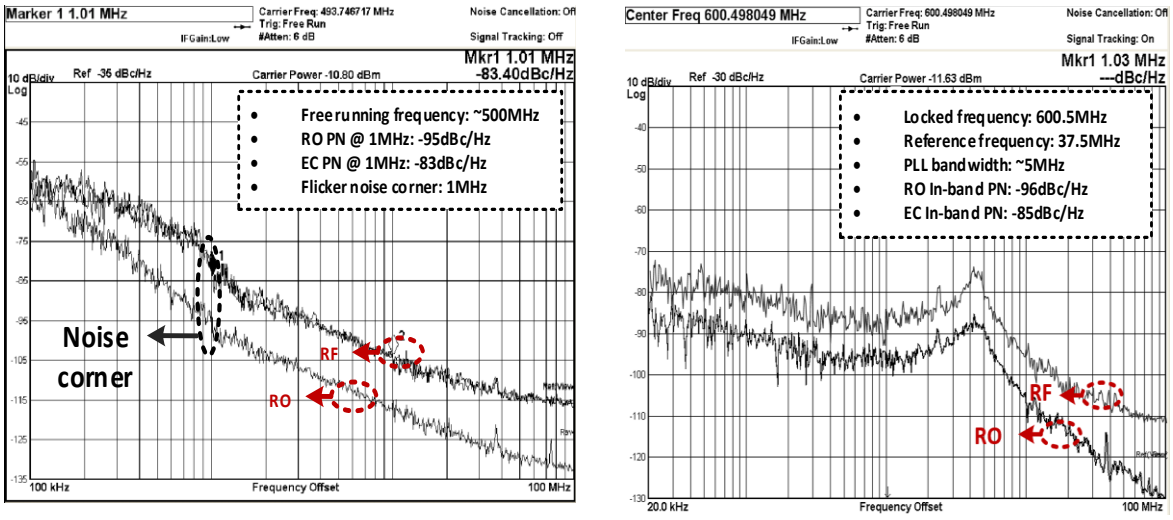


Figure 4-12 Measured phase noise comparison: (a) Free running RO compared to the RF output. (b) Closed loop RO compared to the RF output

The PLL outputs are directly measured at 600MHz shown in Figure 4-13. The reference spur is -55dBc and the fractional spur is -42.3dBc, as shown in Figure 4-13 (a) and (b), respectively. As can be seen from the frequency vs time diagram in Figure 4-14, due to the large bandwidth, the PLL locks within 400ns after reset from a 70MHz initial frequency offset.

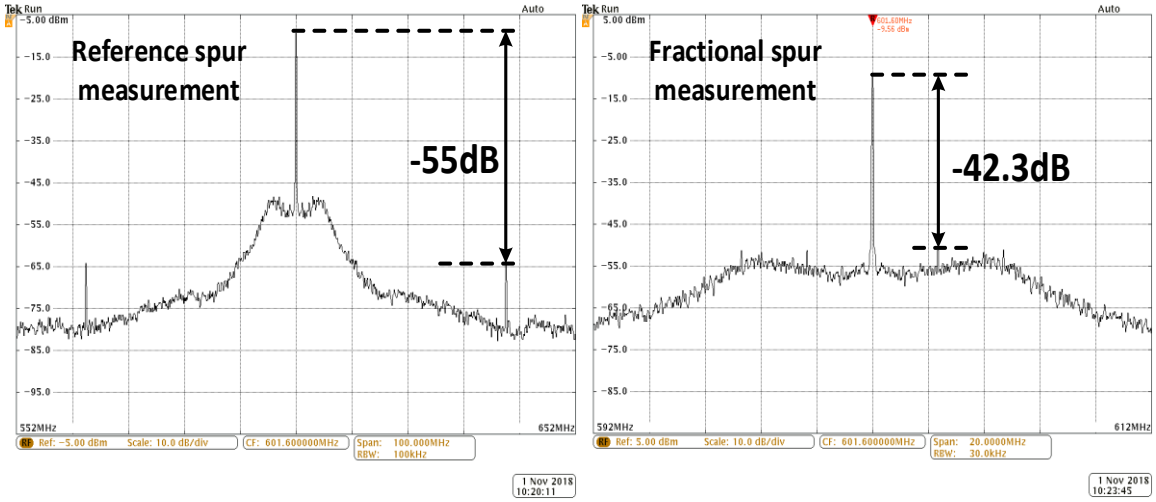


Figure 4-13 Measured PLL spurious performance and locking transient performance: (a) Reference spur measurement (b) fractional spur measurement

Figure 4-15 shows the SCDPA measurement showing the PA efficiency vs output power at different supply voltages. Using a 0.6V power supply, the PA consumes 107µW with a -19.2 dBm output power, yielding a 10.8% PA efficiency at the lower boundary of the BLE output power requirement. In its high-power mode with a 0.9V supply, it can deliver -3.3dBm while consuming 1.2mW with a 39% efficiency. The maximum efficiency of 41% is achieved at around -7.1dBm (@0.7V) output power with a 476 µW PA power consumption. Due to the non-linear nature of the SCDPA, an external matching network is used to suppress TX harmonic emissions. And the measured harmonic performance is shown in Figure 4-18. With the off chip matching network, both HD2 and HD3 are smaller than -42dBm with a 1.2V PA power supply, which complies with BLE requirements.

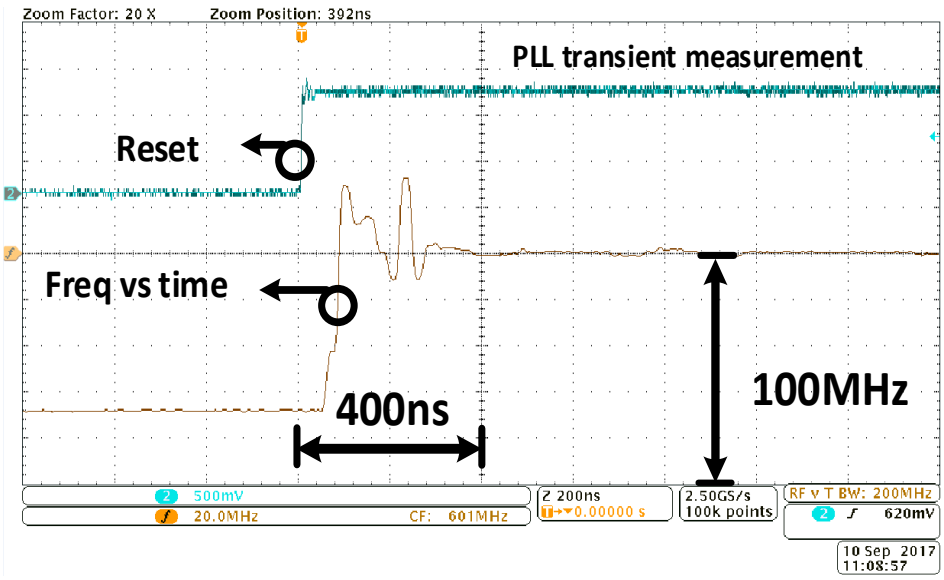


Figure 4-14 Measured PLL locking time

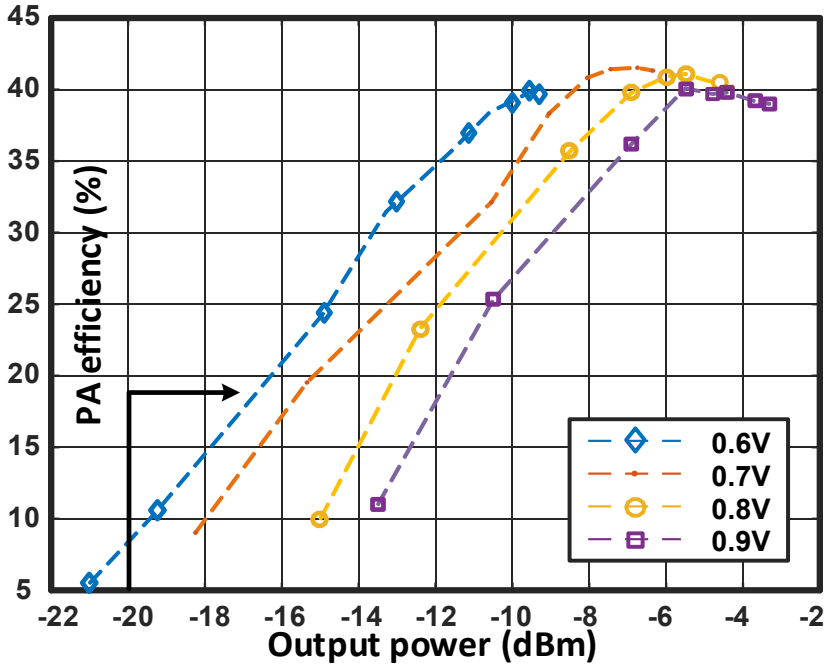
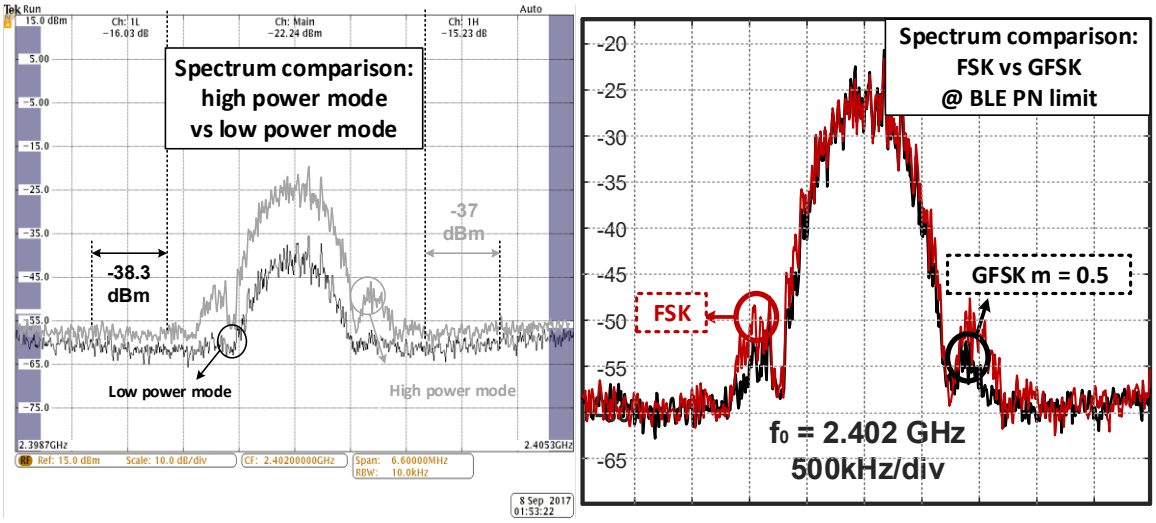


Figure 4-15 PA efficiency versus output power with different power supplies

The TX spectrum is measured while transmitting a repeated BLE packet. The spectrum output is compared using a 0.6V supply between high power mode with all 8 PA cells are turned on and low power mode with only 1 PA cell is enabled. It can be seen in Figure 4-16 (a) that both cases meet the BLE spectrum mask. A comparison of FSK and GFSK at the PN limit region is shown in Figure 4-16(b), showing that when operating at the PN limit region, FSK and GFSK basically have the same spectrum efficiency. This simplification in modulation could potentially help reduce the power consumption even more for low power applications such as self-powered sensors with power consumption as the primary concern and the targeted communication range is within 2–3 meters. The measured frequency vs. time for part of the BLE packets are also shown in Figure 4-17. The eye-diagram is plotted from the captured frequency domain signal. The phase noise from the RO-based design does degrade the eye performance, but as designed, both the

symbol timing and 3σ IFV barely meet the BLE communication limit. The FSK error is 9.1% for this design, which can be expected from the 68 kHz frequency variation.



(a) (b)

Figure 4-16 TX performance measurement: (a) Output spectrum in low-power and high-power mode. (b) Spectrum comparison of FSK and GFSK in the PN limit region.

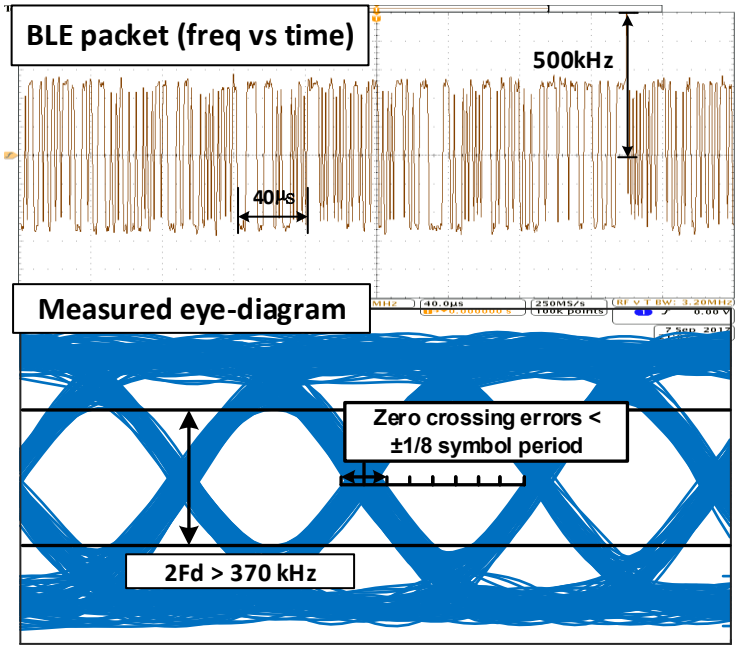


Figure 4-17 Captured BLE packets and eye diagram

The power breakdown is shown in Figure 19. While working at the low power mode with a 37.5MHz off chip reference, the RO with the DAC bias network consumes 126 µW, the PA consumes 107µW and the PLL blocks with the edge combiner consumes 253µW. In the highest power mode with 0.9V supply, the PA consumes 1.2mW. The all-digital RO based BLE TX consumes a total 486µW and 1.6mW in low-power and high-power mode. The comparison to the state-of-the-art is shown in Table I. As the first reported RO based BLE TX esign, it cherishes certain benefits compared to the LCVCO based designs. With the RO, the TX is able to work at the BLE PN limit without extra power-noise penalty. The LO block is able to achieve a power consumption of less than 400µW combined. This helps to enhance the TX efficiency regardless of the PA design. The core area is also considerably small with the RO implementation and can benefit even more with technology scaling, reducing the cost for massive IoT production. Yet for practicality, it's still better to leave some extra margin for the RO design according to the theory analysis in session II, since from the PLL measurement result, it can be seen that the PLL is at the edge of being unstable and the IFV is also a bit higher than the 65kHz target.

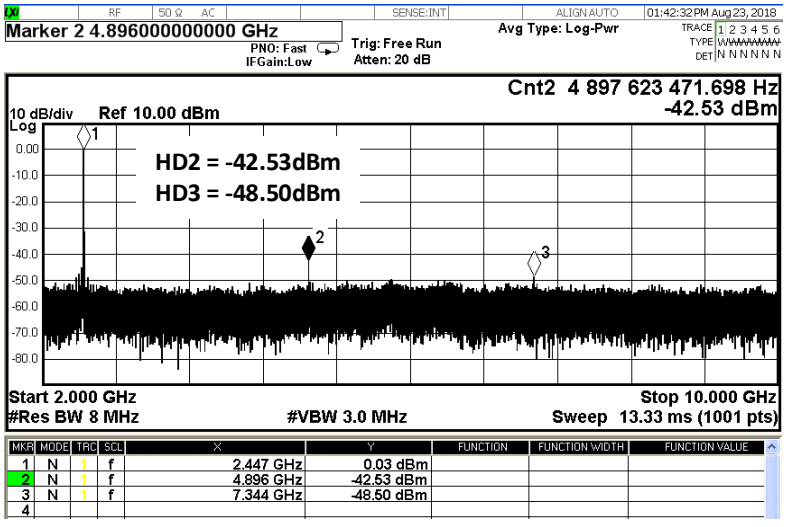


Figure 4-18 TX harmonic measurement with external matching network

Figure 4-20 shows the wireless test setup. Here, the BLE TX is configured to transmit an iBeacon message, which is picked up by the iBeacon app, and shows the correct packet information.

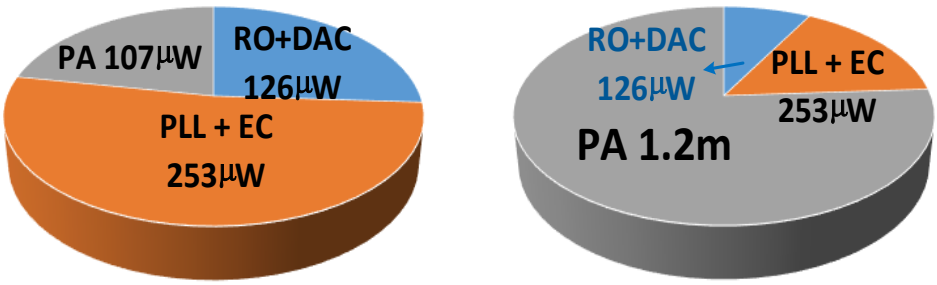


Figure 4-19 TX power breakdown in low-power and high-power mode

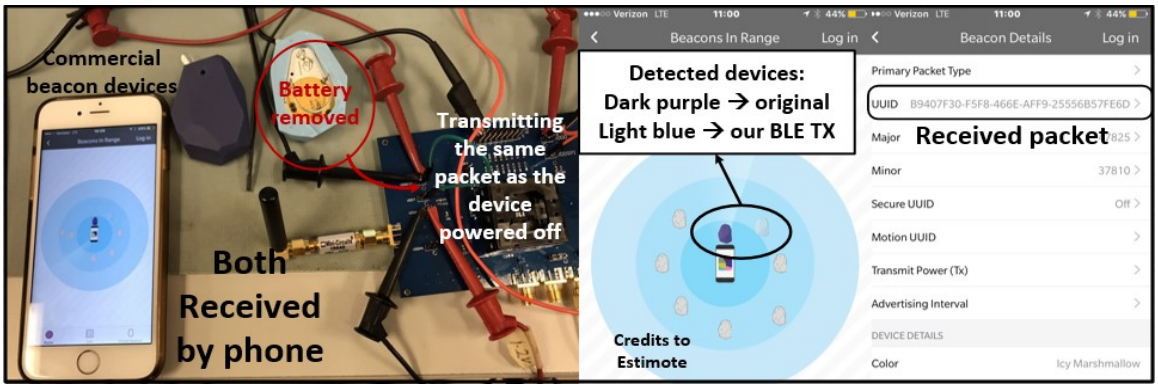


Figure 4-20 Phone connectivity measurement setup for the proposed BLE TX

4.5. Conclusion

In this work, a theory analysis for BLE phase noise requirement has been studied. Instantaneous frequency variation of the local oscillator due to phase noise under different circumstances is used as the link between system level specifications in BLE transmitter to circuit level design choices for the LO. And a phase noise limit is derived as the design baseline too. To verify the analysis, an all-digital RO-based BLE TX is designed and measured. The key techniques to reduce the power consumption while maintaining the

performance are: 1) a wideband all-digital phase-locked loop (ADPLL) featuring an quarter RF frequency RO, with an embedded 5-bit TDC; 2) a 4X frequency edge combiner to generate the 2.4GHz signal; 3) a switch-capacitor digital PA optimized for high efficiency at low transmit power levels. Measurement results show excellent agreement between theory analysis and circuit design, and proving RO is feasible for BLE TX design with low power.

The transmitter consumes 486μW in low power mode while talking to a phone and is extremely low cost due to the implementation with RO. Moreover, because of the all-digital nature of this design, it can further benefit from technology scaling.

Table 1: Performance summary and comparison with the state-of-the-art

	This work	JSSC15[1]	ISSCC15[2]	ISSCC15[3]	JSSC16[4]	ISSCC18[10]
Technology (nm)	40	55	40	40	28	28
LO Architecture	RO + ADPLL	LC + analog PLL	LC + ADPLL	LC + analog PLL	LC + ADPLL	LC + analog PLL
Supply voltage (v)	0.6-0.9	0.9-3.3	1	1.1	0.5/1	0.2
PLL REF frequency (MHz)	37.5	16	32	32	5/40	1
PLL settling time (μs)	0.4	15	15	N/A	14	N/A
PLL In-band PN (dBc/Hz)	-85	N/A	-90	N/A	-92/-101	-80
PLL FoM	-208.5	N/A	-220.9	N/A	-231.6	-227.2
Max output power (dBm)	@0.6V / @0.9V -9.4 / -3.3	0	-2/1	0	3	0
Max PA efficiency	41%*	30%	25%	<30%	41%	32%
TX Power consumption	0.49mW / 1.55mW @-19dBm / @-3dBm	10.1mW @0dBm	4.2mW @-2dBm	7.7mW @0dBm	4.4mW / 3.8mW** @0dBm / @-3dBm	4mW @0dBm
TX max efficiency	32% @-3dBm	15%	10%	13%	36%	25%
Core Area (mm^2)	0.0166	0.6***	0.6***	0.6***	0.65	0.53
FSK error	9.1%	N/A	4.8%	N/A	2.7%	2.2%
HD2 @ 0dBm	-42.5****	-49	-49	-52	-50	-49.6
# of ext. components	2	0	N/A	0	0	0

*With 0.7V PA power supply **Estimated from PA efficiency

***Estimated from die photo for only TX ****Measured with off chip matching network

CHAPTER 5

Phase Noise and Frequency Accuracy in Crystal-less Wireless Edge Nodes

This chapter presents a theory connecting phase noise and frequency accuracy in different time spans and explores the possibilities and limitations in crystal-less (XO-less) frequency calibration for wireless edge nodes from a noise perspective. N-period-average jitter is introduced as a link between spectral characterizations of phase noise and long term frequency stability normally evaluated by Allan Deviation. It is found that flicker noise coming from the reference in a frequency synthesizer is the dominant noise source to affect long term frequency accuracy. An average processing unit embedded in an ADPLL is proposed based on the N-period-average jitter concept to enhance frequency accuracy in the 'Calibrate and Open-loop' scenario. With this low cost block in ADPLL, the frequency calibration accuracy can be directly associated with the reference noise performance. Thus, the feasibility of an XO-less design with certain communication standard can be easily evaluated with the proposed theory. An XO-less BLE transmitter with a RF clock recovery receiver is presented in this chapter. While Chapter 2 focus more on the short term relationship among phase noise, jitter, and instantaneous frequency variation (IFV) from a wireless system's perspective, this chapter offers a more in-depth analysis of their relationship in a long term from a PLL designer's perspective.

5.1. Introduction

Throughout the past decade, numerous efforts have been put into low power and low cost wireless devices for ubiquitous inter-connected objects in the age of Internet of Things (IoT). However, in order to support billions to even trillions of connected devices, it still requires significant reduction in costs and form factor. External components, such as crystal oscillator (XO), matching network, and batteries always dominate the cost and size, as in [6], the XO and battery takes up to 2/3 of the whole prototype board of the miniaturized BLE transmitter even with the matching network removed from the design. Among all the external components, the XO is probably the most expensive (>$1) and bulky component (5×5 mm2), and it is also the most difficult one to remove from the system as an accurate frequency reference in the range of tens of megahertz is normally necessary for the local oscillator (LO) in general RF frontends.

Recent research in crystal-less radios dates back more than a decade ago [4, 90, 91]. The majority of such designs are based on pulse modulations in wideband communications for the highest energy efficiency in the edge nodes. In the transmitter side, ring oscillators are widely used as the LO for its low power and large tuning range [5, 69, 90, 91], since the impact of either jitter or frequency drift due to phase noise in such communication schemes is insignificant [93]. The receivers in such systems, on the other hand, are generally realized with energy detection architecture without LO just for wakeup and power reduction in a bunch of proprietary protocols.

Meanwhile, there are also plenty of researches targeting removing the XO in standard compliant or compatible radio designs such as in BLE and IEEE 802.15.4 [98,99] as an open loop LC oscillator can offer enough phase noise performance as long as the frequency

is calibrated at the start of every packet transmission [6, 98]. In such systems where the RF oscillator's phase noise can easily satisfy the communication requirement, instead of locking all the time during RF transmission, the PLL's role can be shifted to a simpler 'calibration' scheme and the frequency reference can be different from a typical megahertz XO. In [97], the PLL is locked to the incoming RF signal at 2.4GHz through the receiver chain, and in [94, 95], the LOs are injection locked to the RF signal, whose outputs were further used for demodulation based on the injection locking or pulling conditions. In a recent ADPLL design for BLE of [98], the high frequency XO is replaced with a 32 kHz real time clock (RTC) simply for calibration purpose as well. Although 32 kHz RTCs are generally made with a low frequency XO, the removing of the high frequency one still results in a reduction of cost and power.

All these researches show the possibility of replacing the high frequency XO in certain applications with other frequency reference sources such as RF signal, low frequency reference and even noisy but well characterized reference such as a temperature compensated RC oscillator. However, it still lacks a comprehensive analysis in how phase noise in the reference will impact the short term and long term frequency accuracy in a 'Calibration and Open-loop' scheme incorporating all the reference cases mentioned above. The primary goal of this paper is to provide a fundamental analysis of reference noise's impact on frequency accuracy and offer a calibration method to deal with it inside a typical type I ADPLL.

Section 5-2 summarizes the relationship among phase noise, different types of jitter, and frequency accuracy based on previous publications [100-111] as well as the relevant analysis in chapter 2. Then the impact of LO's phase noise shaping on frequency accuracy

in both short term and long term will be analyzed. Section 5-3 proposes an embedded digital filtering technique in the ADPLL loop filter targeted for the 'Calibration and Open-loop' scheme that can further filter the excessive phase noise coming from a non-XO reference. The effectiveness of the filtering technique will be assessed based on different types of noise sources from the reference in section 5-4. An example associated with BLE will be shown 5-5. Finally, section 5-6 draws the conclusion.

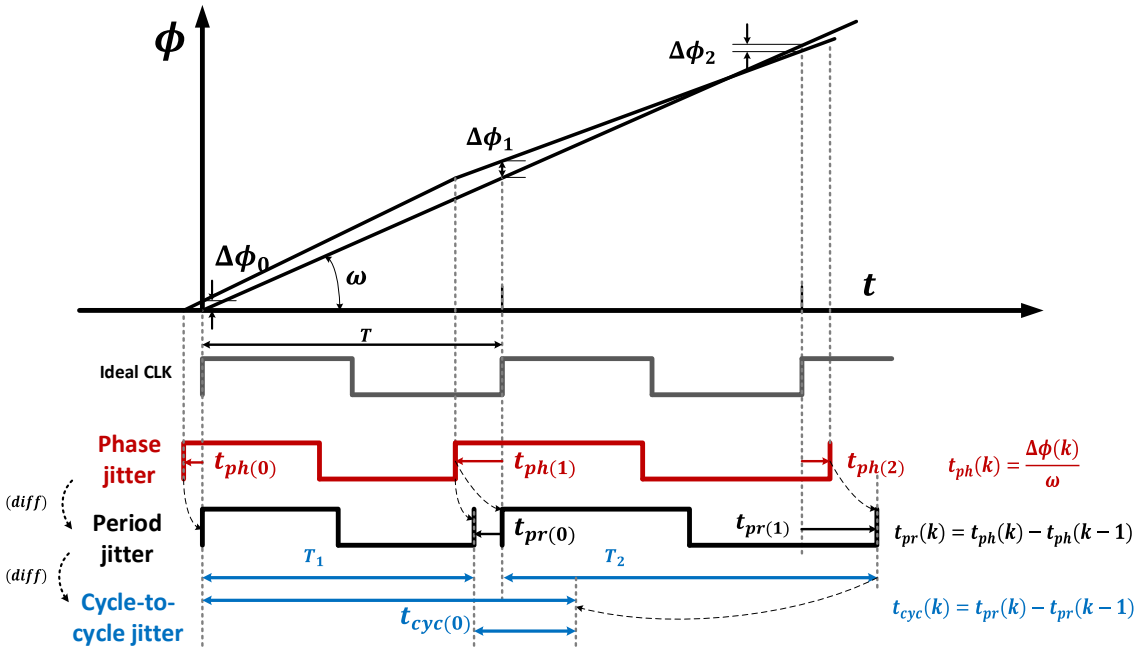


Figure 5-1 Phase jitter, period jitter and cycle-to-cycle jitter relationship associated with phase errors over time

5.2. Phase Noise, Jitter, and Frequency Accuracy

5.2.1. Short term frequency accuracy related to PN and jitter

Phase noise (PN) has been evaluated and analyzed from various perspectives such as numerical methods, mathematical and physical understandings, circuit design considerations and system level requirements, to name a few. Designers from different areas always have different angles towards the same question, resulting in various

interpretations. Wireless and RF circuit designers focus more on phase noise of the LO while wireline as well as the majority of digital and mixed signal circuit designers care more about jitter from the clock. On the other hand, interestingly enough, both system engineers making communication standards and circuit engineers designing clocking references, such as XO and relaxation oscillators, prefer to use frequency accuracy (such as Allan Deviation) as their benchmarking specifications. This makes the already difficult and somewhat obscure topic even harder to deal with as it requires a thorough understanding of PN from math and physics description, to system impacts and circuit implementation. In this session, we will review PN fundamentals and develop a simple yet still practical link among PN, jitter, and frequency accuracy for circuit designers using relatively simple mathematical descriptions.

Figure 5-1 shows the physical relationship among phase error, phase jitter $t_{ph}(k)$, period jitter $t_{pr}(k)$ and cycle-to-cycle jitter $t_{cyc}(k)$ corresponding to the kth cycle of the clock compared to an ideal clock. As can be seen in Figure 1, phase jitter is directly related to phase error (PE) over time, while period jitter is indirectly related to instantaneous frequency variations (IFV) as it is the differential value between consecutive phase jitters. Similarly, cycle-to-cycle jitter corresponds to error of the frequency change rate (EFCR), which can be quite useful in FMCW radars and spread spectrum clocks where the frequency is sawtooth or triangularly modulated. According to Wiener-Khintchin theorem assuming a stationary (at least almost stationary) process for the jitter, the relationship between phase noise and the jitters are:

$$\sigma_{\tau_{ph}}^2 = \frac{1}{2\pi^2 f_0^2}\int_0^\infty \mathcal{L}(f)df \qquad (5-1)$$

$$\sigma_{\tau_{pr}}^2 = \frac{2}{\pi^2 f_0^2}\int_0^\infty \mathcal{L}(f)\sin^2(\frac{\pi f}{f_0})\,df \qquad (5-2)$$

$$\sigma_{\tau_{cyc}}^2 = \frac{8}{\pi^2 f_0^2}\int_0^\infty \mathcal{L}(f)\sin^4(\frac{\pi f}{f_0})\,df \qquad (5-3)$$

Where $\mathcal{L}(f)$ is the PN PSD and $\sigma_{\tau_{ph}}, \sigma_{\tau_{pr}}$ and $\sigma_{\tau_{cyc}}$ are standard deviations of phase jitter, period jitter and cycle-to-cycle jitter, respectively. f_0 denotes the carrier frequency. Thus, the corresponding phase and frequency errors will be in a similar format but multiplied by f_0^4, as already shown in [26, 111]. To our interest, the equation evolves IFV is listed below as the simple link between phase noise, jitter, and short term frequency accuracy:

$$\sigma_f^2 = f_0^4\sigma_{\tau_{pr}}^2 = \frac{2f_0^2}{\pi^2}\int_0^\infty \mathcal{L}(f)\sin^2(\frac{\pi f}{f_0})\,df \qquad (5-4)$$

5.2.2. N-period jitter, N-period-average jitter, and Allan Deviation

For the long term frequency accuracy, phase noise's impact is more subtle as reference clocks are measured over a long period of time and some of the noise components are averaged out. We start the analysis from N-period jitter, which is defined as the deviation between the phase jitter compared to its N-th previous value. As a random process, the variance of the N-period jitter can be related to the autocorrelation function of PE [26, 50]:

$$\sigma_{\tau_{\mathrm{prN}}}^2 = \frac{2}{\omega_0^2}\left[R_\phi(0) - R_\phi(NT)\right] \qquad (5-5)$$

If we assume PE as a stationary process, as we did for eq. 2, the N-period jitter and PN's relation can be written as:

$$\sigma_{\tau_{prN}}^2 = \frac{2}{\pi^2 f_0^2}\int_0^\infty \mathcal{L}(f)\sin^2\left(\frac{\pi f N}{f_0}\right)df \qquad (5-6)$$

We define the N-period average jitter as the average value of the N-period jitter over the number of periods:

$$\mathbf{t_{prAVE}} = \frac{\boldsymbol{t_{prN}}}{N} \tag{5-7}$$

Which is still a jitter vector that can be related to frequency variations. This value is useful for the proposed frequency calibration technique for XO-less operations as will be discussed in session III. And it has a variance:

$$\sigma^2_{\tau_{prAVE}} = \frac{2}{\pi^2 f_0^2 N^2}\int_0^\infty \mathcal{L}(f)\sin^2\left(\frac{\pi f N}{f_0}\right)df \tag{5-8}$$

Using a similar expression to (5-4) can give us the relation between PN, N-period average jitter and long term frequency accuracy, and it is written as:

$$\sigma^2_{f_{AV}} = f_0^4\sigma^2_{\tau_{prN}} = \frac{2f_0^2}{\pi^2}\int_0^\infty \mathcal{L}(f)\sin^2\left(\frac{\pi f N}{f_0}\right)df \tag{5-9}$$

We could further derive the relation of PN to Allan Deviation using the same method. Similar to the N-period average jitter defined above, Allan Deviation (ADEV) uses an N-period average value over the total length of time as:

$$y = \frac{\boldsymbol{t_{prN}}}{NT_0} \tag{5-10}$$

And the Allan deviation is thus defined as:

$$\sigma_{\Delta y}(NT) = \frac{1}{NT_0}\sqrt{\frac{E\left[\left(t_{prN}(k) - t_{prN}(k+N)\right)^2\right]}{2}} \tag{5-11}$$

Its relation to PN can be calculated using Wiener-Khintchin Theorem as:

$$\sigma^2_{\Delta y}(NT_0) = \frac{4}{\pi^2 N^2}\int_0^\infty \mathcal{L}(f)\sin^4(\pi f N T_0)\,df \tag{5-12}$$

And interestingly enough, it can be directly related to the N-period cycle-to-cycle jitter with the multiplication of N-period's time:

$$\sigma_{\Delta y}(NT_0) = \frac{1}{\sqrt{2}NT_0}\sigma_{\tau cycN} \qquad (5-13)$$

The relationship among jitter, PN and long term frequency accuracy has thus been clear to us and it is surprisingly simple. The widely used Allan Deviation for characterizing clock frequency stability is simply the N-period cycle-to-cycle jitter with a coefficient related to the measuring time. Figure 5-2 shows their relationship in both short term and long term.

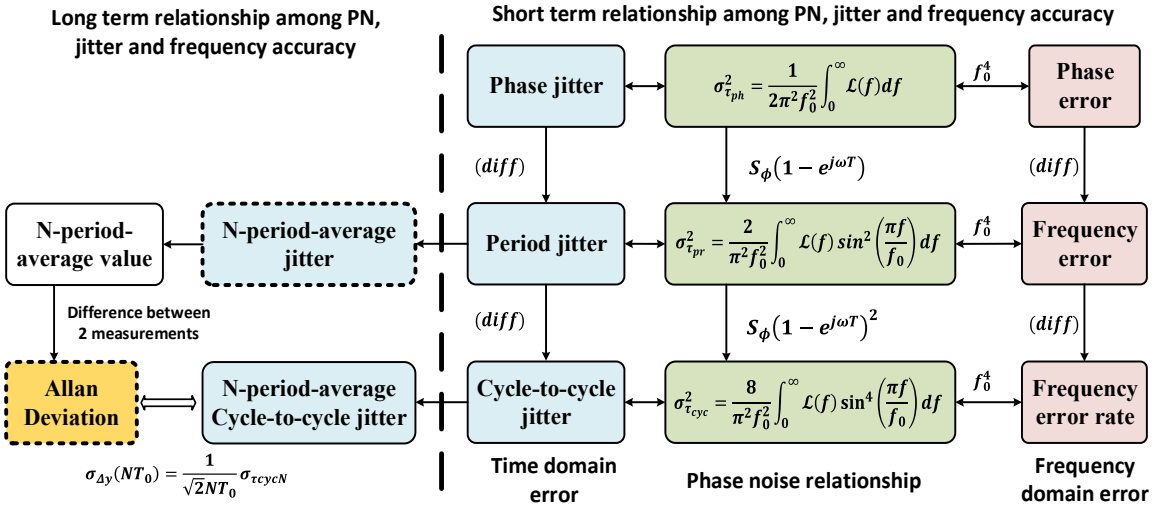


Figure 5-2 Physical relations among phase noise, jitter, and frequency accuracy in both short term and long term

5.2.3. Noise shaping's impact on long term frequency accuracy

The phase noise profile of a frequency synthesizer can be viewed as a superposition of different noise sources shaped in various ways from a mathematic point of view. Moving from the lower frequency offset to the higher end, PN is firstly dominated by a flicker PN profile $(1/f^3)$ coming from the frequency reference, then to a nearly flat PN profile coming

from either the shaped oscillator PN or charge pump (TDC for digital PLL), and further to a white PN profile from the oscillator ($1/f^2$), and eventually to a flat noise floor. Different kinds of noise shaping have very different influence on all the jitters mentioned above and eventually affect the frequency/phase change over time. The short term relationship among PN, jitter, and frequency accuracy associated with eq. (5-1~5-3) has already been demonstrated in a lot of previous publications, so in this session we will only focus on the long term frequency accuracy, such as the N-period-average jitter and Allan Deviation, due to PN and reveal how different PN profiles are accumulated and can be averaged over time.

Assuming system bandwidth of f_{BW}, and for the flat PN profile, the N-period-average jitter and Allan Deviation from eq.(8) and eq.(12) can be simplified as:

$$\sigma^2_{\tau_{prAVE}} = \frac{\mathcal{L}_0}{\pi^2 f_0^2 N^2}\left[f_{BW} - \frac{\sin\left(\frac{2\pi f_{BW} N}{f_0}\right)}{\frac{2\pi N}{f_0}}\right] \qquad (5-14)$$

$$\sigma^2_{\Delta y}(NT_0) = \frac{4\mathcal{L}_0}{\pi^2 N^2}\left\{\frac{3}{8}f_{BW} - \frac{\sin\left(\frac{2\pi N f_{BW}}{f_0}\right) - \frac{1}{8}\sin\left(\frac{4\pi N f_{BW}}{f_0}\right)}{\frac{4\pi N}{f_0}}\right\} \qquad (5-15)$$

Where $\mathcal{L}_0$ denotes the flat PN level. It shows that with a flat PN profile, both the N-period-average jitter and Allan Deviation decrease with the increase of the number of periods N in time. It actually decrease with $1/N$ in log-scale as shown in Figure 5-3 in the blue line, which corresponds to the 'white phase' region in a typical Allan-Deviation plot.

For a white PN profile, generally assumed in the majority of free running oscillators with white noise only, the corresponding phase noise follows:

$$\mathcal{L}(f) = \frac{\mathcal{L}_s f_s^2}{f^2} \qquad (5-16)$$

Where $\mathcal{L}_s$ is the PN value sampled at f_s offset to the carrier. This integration is rather complicated which involves certain approximations in exponential integrals [112]. The N-period-average jitter and Allan Deviation can be simplified as:

$$\sigma^2_{\tau_{prAVE}} \approx \frac{2\mathcal{L}_s f_s^2}{\pi f_0^3 N} Si(\infty) = \frac{\mathcal{L}_s f_s^2}{N f_0^3} \qquad (5-17)$$

$$\sigma^2_{\Delta y}(NT_0) \approx \frac{2\mathcal{L}_s f_s^2}{\pi N f_0} Si(\infty) = \frac{\mathcal{L}_s f_s^2}{N f_0} \qquad (5-18)$$

Where $Si(\infty) = \frac{\pi}{2}$ is the sine integral at infinity. Other secondary terms in (5-17) and (5-18) are neglected. The above two equations show that when only white noise is included in a free running oscillator, the N-period-average jitter and Allan Deviation will both decrease with time at the same rate following $\sqrt{N}$ as shown in Figure 3. This goes the same way as the 'white frequency' region in Allan-Deviation plot as well.

And finally for the flicker PN profile, which is unavoidable in low frequency offsets for all kinds of oscillators, can be treated in a similar way while still assuming that the jitter is a stationary process. The PN profile in such case can be written as:

$$\mathcal{L}(f) = \frac{\mathcal{L}_s f_s^3}{f^3} \qquad (5-19)$$

Substitute (5-19) in (5-8), we have:

$$\sigma^2_{\tau_{prAVE}} = \frac{2\mathcal{L}_s f_s^3}{\pi^2 f_0^2 N^2} \int_0^\infty \frac{\sin^2\left(\frac{\pi f N}{f_0}\right)}{f^3} df \qquad (5-20)$$

The above integral, however, will lead to non-converging results. Many theories have been developed in the past to explain the phenomenon of flicker noise yet it is still obscure and no explanation has been able to cover the fundamental origins. The stochastic process that involves flicker noise profile is actually non-stationary and simply apply the Wiener-

khintchin theorem is not 100% accurate. Actually even with only white noise, the calculation for phase jitter using equation (5-1) is not accurate as well since the integral involving a $1/f^2$ spectrum is also divergent and will result in a phase 'random walk' following the Wiener-Levy process. Thus, a frequency limit f_{min} towards the carrier is necessary for all the approximated calculation. As explained in [26], with the finite observation time in a measurement compared to the life time of the object, the noise can be treated as an almost-stationary process as the non-stationary behavior is dominated by all its 'past'. Another explanation is that although the spectrum of flicker noise will go to infinity with the frequency close to zero, the phase noise spectrum of an oscillator will actually saturate and show a Lorentzian spectrum profile. With or without the consideration of flicker noise, there will always be a noise corner below which the PN profile changes back to flat [100]. However, we cannot treat this flat PN profile the same as flat noise floor analyzed above. From a physical point of view, it is an ensemble behavior in time of the oscillator over the measurement time, rather than a different noise accumulation scheme. Thus, a low frequency limit below the noise corner of the Lorentzian spectrum will be meaningless in the frequency accuracy characterization. On the other hand, since the amount of energy in each decade across the given frequency range is the same for flicker noise, a low frequency limit in the same decade of the Lorentzian noise corner would be enough for frequency accuracy estimation.

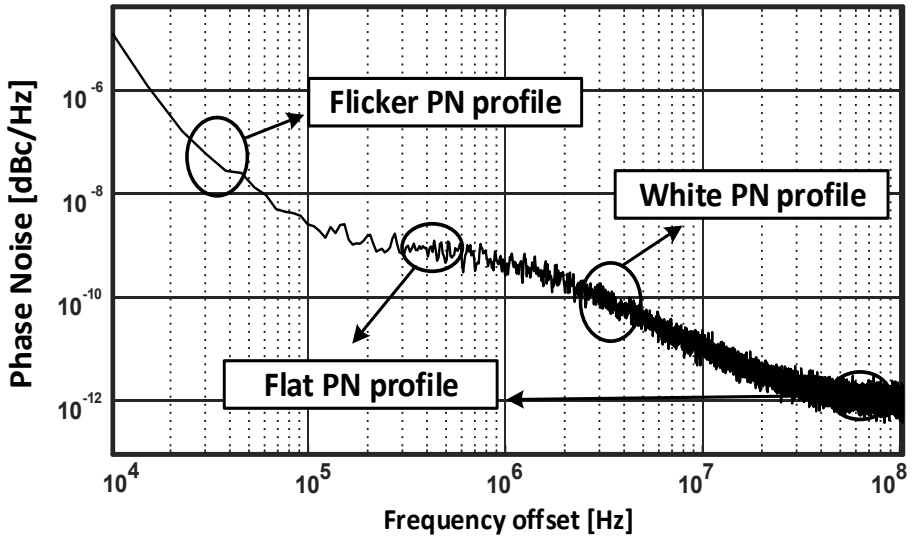
Thus, assuming f_{min} as the lower integration boundary, (20) could be rearranged as:

$$\sigma^2_{\tau_{prAVE}} \approx \frac{\mathcal{L}_s f_s^3}{f_0^4}\left[3 - 2\gamma - 2\ln\left(\frac{2\pi N f_{min}}{f_0}\right) + O(f^2)\right] \propto \ln\left(\frac{1}{N}\right) \qquad (5-21)$$

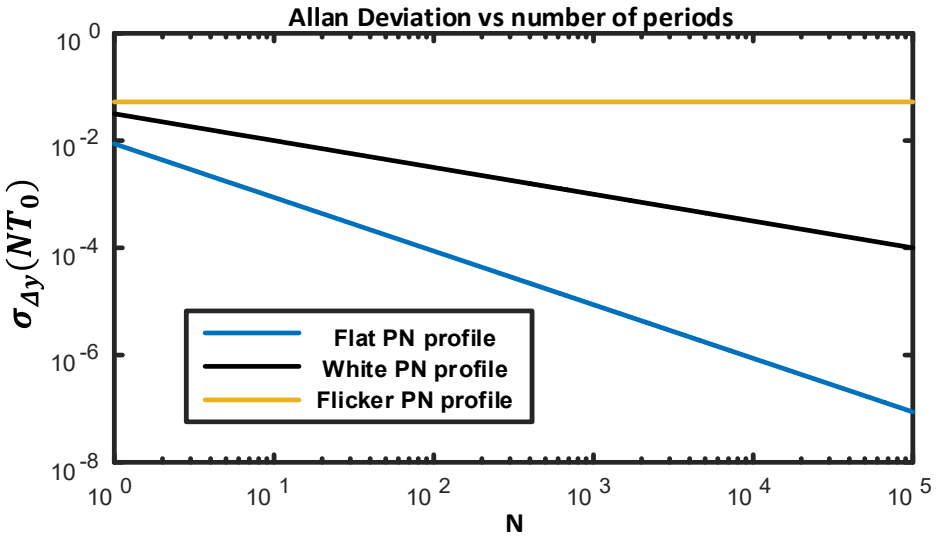
Where $\gamma \approx 0.5772$ is the Euler-Mascheroni constant [112]. In the same way, Allan Deviation can be simplified as the following form:

$$\sigma_{\Delta y}^2(NT_0) \approx \frac{4\mathcal{L}_s f_s^3}{f_0^2}[\ln(2) + O(f^2)] \qquad (5-22)$$

Equation (5-21) shows that the N-period-average jitter will almost keep unchanged yet still decrease with a rate of $\ln(1/N)$, while the Allan Deviation is a constant in a flicker noise profile. Their change over time N are shown in Figure 5-3 as well.



(a)



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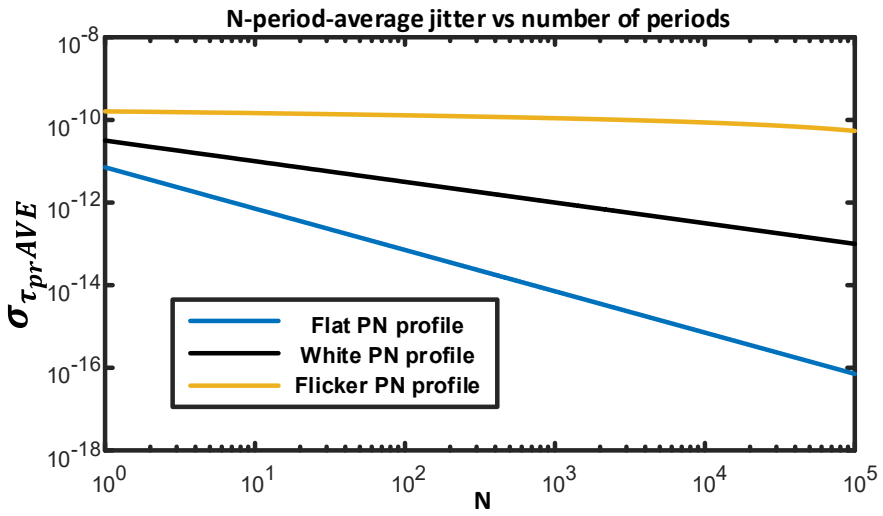


(c)

Figure 5-3 Flicker, white and flat PN profiles definition (a), N-period-average jitter (b), and Allan Deviation (c) vs time over flat, white and flicker PN profiles. For (b) and (c), all cases assume 1GHz center frequency with sampled PN=-120dBc/Hz @ 1MHz offset

It can be foreseen that if the PN with a spectrum like $1/f^{\alpha}$ and $\alpha > 3$, then both N-period-average jitter and ADEV will increase with time, which can be reflected in the typical Allan Deviation plot when the measurement time is very long. This could be resulted from changes in the external environment such as temperature and voltage, or could be some cross-correlation effect inside the oscillator, or could even because that the 'almost-stationary' assumption does not hold.

5.2.4. Flicker noise and limitation of averaging in frequency accuracy characterization

The above analysis shows that the time dependence of both N-period-average jitter and Allan Deviation to characterize oscillator's frequency accuracy varies with different PN noise profiles. As discussed above, frequency variations due to flat and white PN profiles

can be minimized with the increase of averaging or measurement time while flicker noise will stop that trend from a statistical point of view. Looking at the time domain, the frequency error over time with flicker PN profile has the 'memory' of all the past frequency errors while the white PN only affect the 'current' noise status. This could be verified through the autocorrelation function of each case. With white PN profile, the autocorrelation of frequency error $R_f(\tau)$ is an impulse at $\tau = 0$(or sinc function with limited bandwidth), and with flicker PN, it can be approximated as:

$$R_f(\tau) = \frac{C}{2\pi}[Ci(\omega_{BW}\tau) - Ci(\omega_{min}\tau)] \qquad (5-23)$$

Where C is a constant and $\omega_{BW}, \omega_{min}$ are the integration boundaries to assume it a stationary process.

With different measurement (averaging) time, the contribution of different PN profiles to frequency variation varies significantly. Intuitively, assume the PN sampling point in (5-17) and (5-20) is the same at the flicker noise corner for a free running oscillator, the N-period-average jitter due to white PN and flicker PN can be compared as follows:

$$\frac{\sigma^2_{\tau_{prAVE_{flicker}}}(N)}{\sigma^2_{\tau_{prAVE_{white}}}(N)} = \frac{f_c}{f_0} N \left[3 - 2\gamma - \ln\left(\frac{2\pi f_{min} N}{f_0}\right)\right] \qquad (5-24)$$

Which shows that the jitter contribution from flicker noise is only affected by the flicker noise corner and averaging time N. Figure 5-4 shows ratio of flicker PN jitter to white PN jitter in the N-period-average jitter over time with different flicker noise corners plotted in log scale. It can be seen that when N=1, white PN contributes the majority of period jitter variations while with the increase of averaging time, flicker PN becomes the dominant noise source. A smaller flicker noise corner will reduces the N-period-average jitter and results in more frequency accuracy.

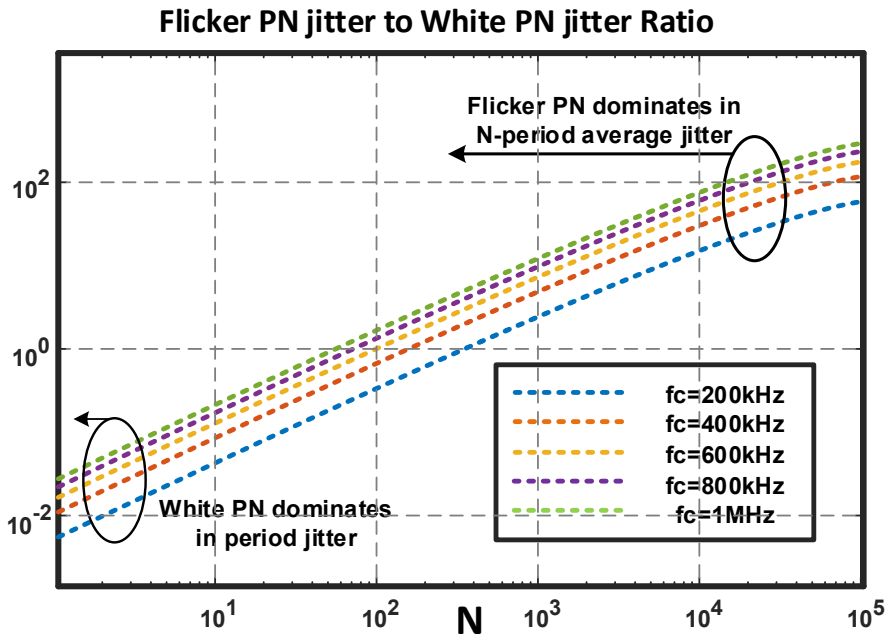
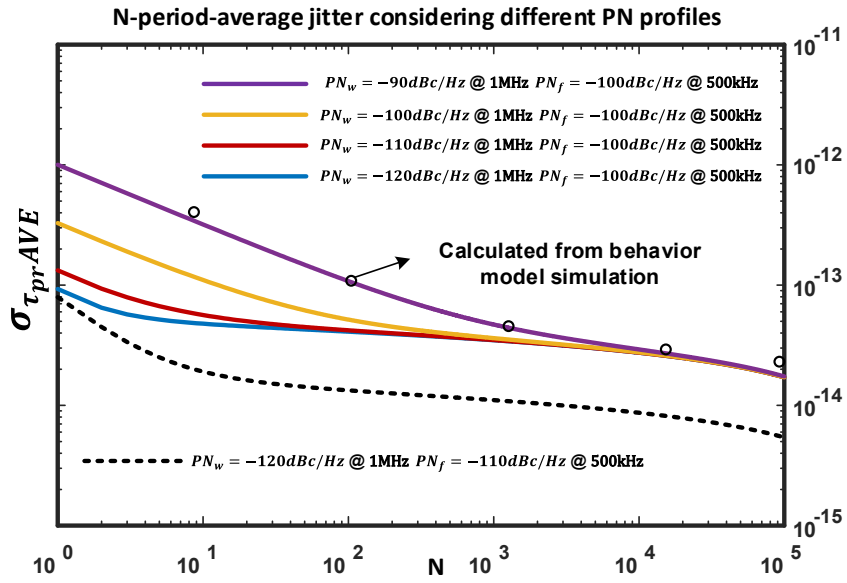
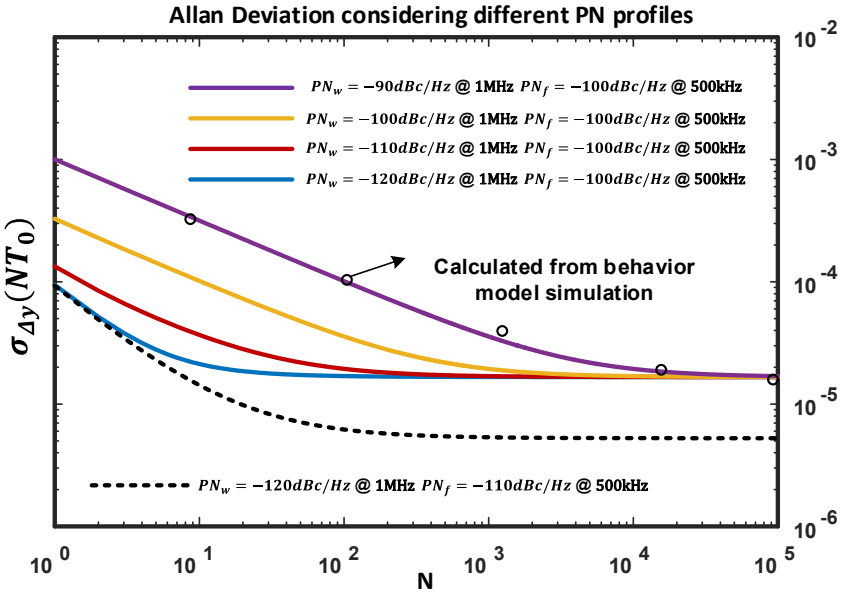


Figure 5-4 Ratio of flicker PN jitter and white PN jitter with f_0=1GHz and different flicker noise corners

So eventually, the frequency synthesizer's frequency stability over a long period of time is determined by the frequency reference's noise performance and limited by its flicker noise component no matter how much more noise was added by other noise sources in the PLL loop. The reference's PN is low pass filtered and up-converted by the frequency multiplication ratio, thus, in a long term, the frequency stability of the PLL output is a direct reflection of the reference's frequency stability. Figure 5-5 shows the simulated N-period-average jitter and Allan Deviation over time with different PN profiles. In the low frequency offset, their PN are all dominated by a flicker PN profile at the same level. And it can be seen that, after certain periods of time, all the PN profile converge at the same level.



(a)



(b)

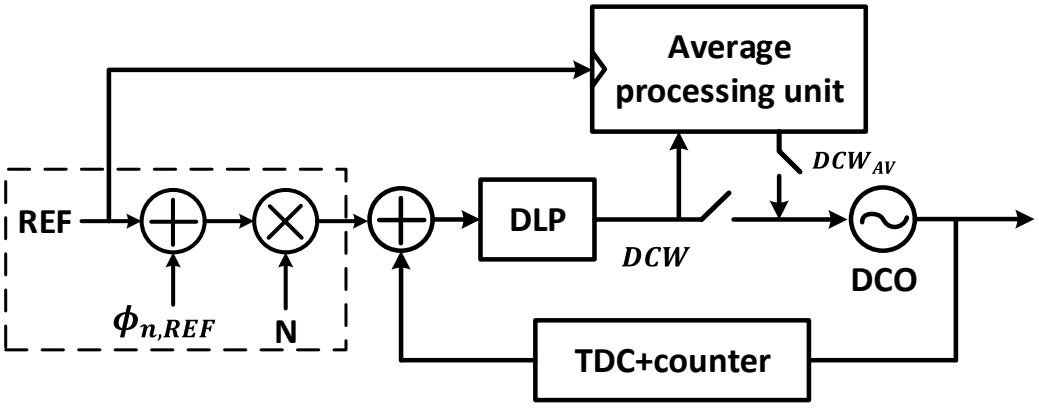
Figure 5-5 N-period-average jitter (a) and Allan Deviation (b) of typical open loop oscillator including flat, white and flicker PN profiles in different levels.

The above analysis and simulation show 3 important features in frequency average and measurement:

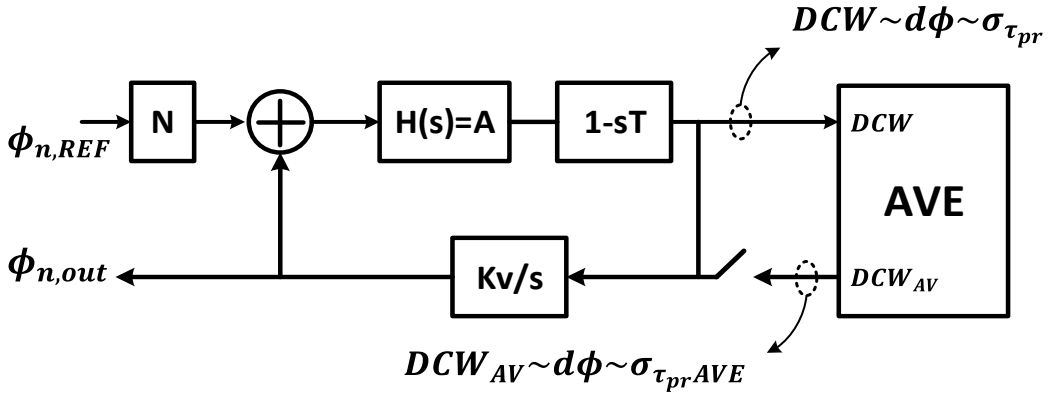
1. Flicker noise has a small impact compared to white noise in short term period jitter while it has a significant impact in the long term frequency accuracy
2. It is the flicker noise from the reference that dominate the long term frequency accuracy performance, and all other noise components in higher frequency offsets can be averaged out.
3. Frequency average can be helpful in frequency calibration if the long term frequency accuracy can be evaluated with N-period-average jitter. Reference's performance can thus be defined in the XO-less applications.

5.3. An Embedded Filter Technique in ADPLL for Frequency Calibration

As discussed in session II, the long term frequency accuracy is solely depended on reference's flicker noise after certain time's frequency average, thus, an embedded jitter average processing unit (APU) in an ADPLL can be used to calibrate RF frequency even when the reference is, to some extent, noisy. Figure 5-6 (a) shows the simplified block diagram of the proposed frequency calibration loop based on a divider-less ADPLL. The average processing unit is embedded in the digital loop filter and perform a windowed averaging algorithm in the digital control word (DCW) fed into a digital controlled oscillator. Only the reference noise is shown in the diagram as the dominant noise source over a long time since other noise could be averaged as discussed in session II. During the calibration state, the average processing unit is running in the background to collect the changing digital control word fed into the DCO while the ADPLL is in locking status. The DCW is a reflection of the phase error difference with one loop delay in the PLL. So the DCW corresponds to period jitter of the reference clock and DCW_{AV} corresponds to the N-period-average jitter defined in session II, which are all related to frequency errors.



(a)



(b)

Figure 5-6 (a) Block diagram of the proposed average processing unit embedded in ADPLL. (b) Corresponding continuous time behavior model of the proposed frequency calibration circuit considering only reference noise source

In the typical 'calibrate and open-loop' scheme where the RF oscillator's PN is better than the standard requirement such as BLE, using DCW_{AV} rather than DCW will result in a much more accurate 'releasing frequency' when open loop. During the locking status of a PLL, the DCW in real time is a random process normally following a Gaussian distribution if no significant spurs exist. The 'releasing frequency' could be anywhere within $\pm 3\sigma_{pr}$ of the carrier frequency. While the 'releasing frequency' by using DCW_{AV} is

within $\pm 3\sigma_{Npr_{AV}}$ of the carrier. And with enough time in the average process, $\sigma_{Npr_{AV}}$ could be much smaller than σ_{pr} depending on the noise performance of the reference itself. In another word, only the flicker noise of the reference contribute to frequency errors if using average process. And all noise sources will contribute errors in frequency if without.

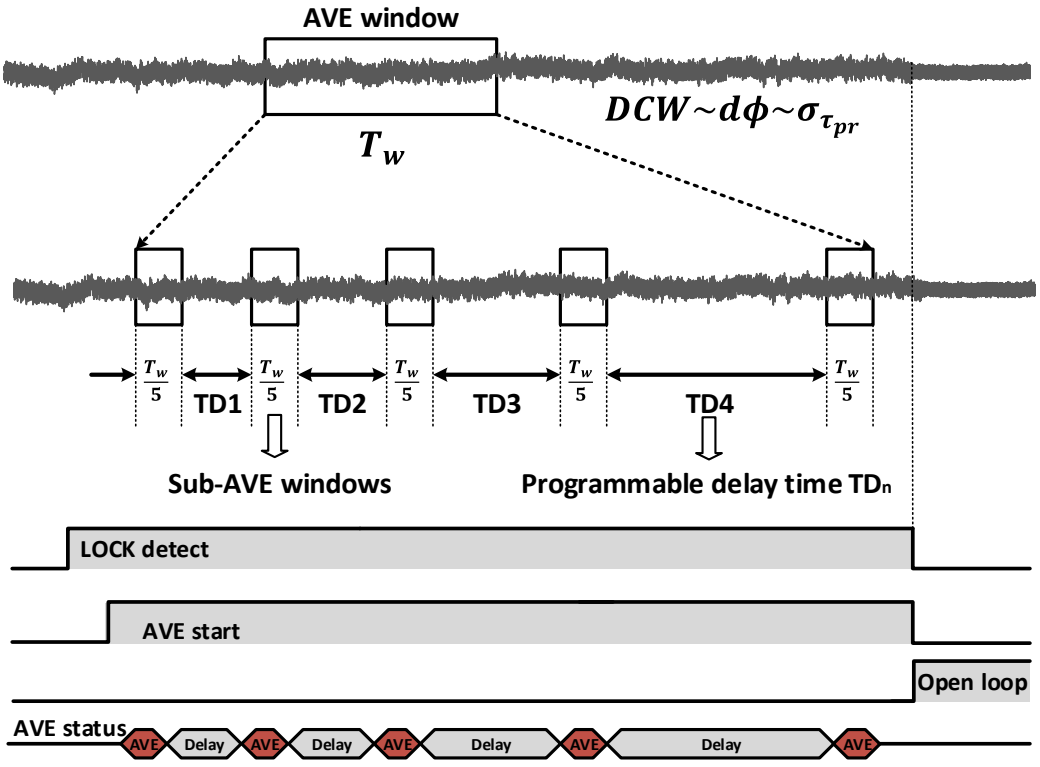


Figure 5-7 Programmable windowed average processing algorithm for the 'calibration and open loop' frequency calibration scheme in XO-less wireless edge nodes

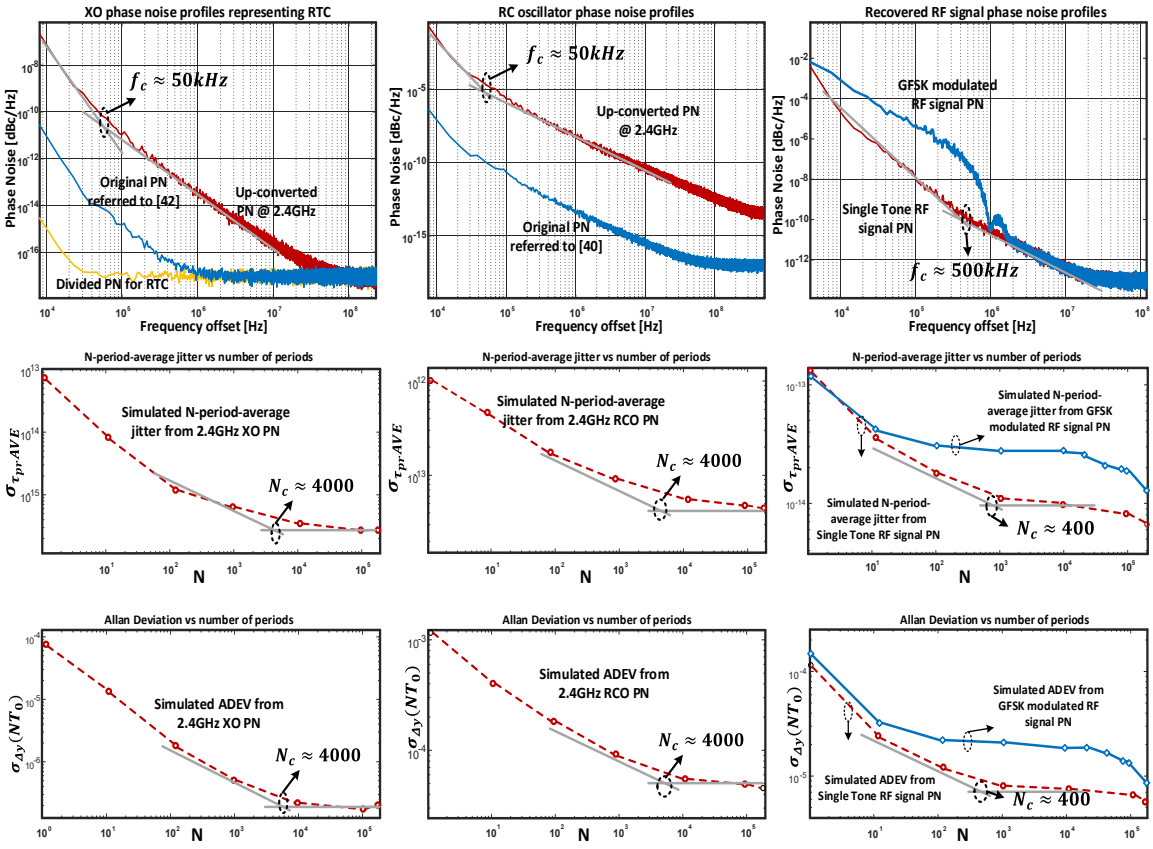
As analyzed in session II, longer averaging time would always help with the N-period-average jitter even when it exceeds the time constant associated with the flicker noise corner, which corresponds to:

$$N_c = \frac{\ln(2)\, f_0}{4 f_c} \qquad (5-25)$$

Where f_0 is the carrier frequency and f_c is the flicker noise corner. However, considering practical issues such as memory size, power and area of the APU, a total averaging time close to N_c is more efficient. On the other hand, spurious tones in the PLL will result in repetitive patterns in the DCW. Large fractional spurs below the flicker noise corner might result in slow fluctuation that couldn't be covered by the total averaging time. Thus in order to deal with potential large spurs, instead of averaging in one large window, it could be divided into several small windows separated by different time delays as shown in Figure 5-7. The waiting time between each average time window is programmable.

5.4. Different Types of References and XO-less Feasibility

The APU inside the ADPLL in session III could help reduce the 'releasing frequency' error down to a significantly lower level since only the flicker part of the reference noise would contribute to that error. On the other hand, we can also use the same method to directly define the required reference noise performance for frequency calibration where the 'calibrate and open-loop' scheme is feasible. As mentioned in session I, three kinds of references have been evaluated in the past to remove the high frequency XO as the PLL reference in the wireless edge nodes: RTC, RC oscillator and recovered RF signal. This session will evaluate all 3 cases with the help of the APU inside the ADPLL.



(a) (b) (c)

Figure 5-8 Simulated phase noise impact on N-period-average jitter and Allan Deviation for different noise sources: (a) XO representing RTC with excellent noise performance, (b) RC oscillator, (c) Recovered RF signal with and without modulation

RTC is widely used in SoCs for its digital clocking. Strictly speaking, RTC mostly uses crystal as well so it is an accurate reference source with excellent phase noise performance although operating at a low frequency. RC oscillators, on the other hand, are relatively noisy reference sources. And in order to use RC oscillator as a reference for frequency calibration, its frequency and temperature dependence shall be pre-characterized and an accurate temperature sensor shall be included in the design as well. This session will only focus on the noise part. The RF clock recovery case has a much more complicated

phase noise profile since the RF signal could be modulated. For example, in a BLE network, the RF signal saw by the receiver on the wireless edge node is GFSK modulated. The frequency variation depends on the data packet but the center frequency can be considered accurate as it is regulated by the XO in the transmitter. On the other hand, depending on the receiver architecture, the phase noise could be further up-converted through the mixer. In this paper, we will not consider this effect coming from the receiver path, but rather just focus on the original PN profile from the incoming RF signal whether it is modulated or not.

So from noise's perspective, the RTC represents a low PN profile, the RC oscillator represents a high PN profile and the recovered RF signal represents complex PN profile depending on its modulation format and noise up-conversion in the receiver path due to mixer. In overall, the modulation would affect the PN in relatively high frequency offset while and noise up-conversion will affect all its PN profile. And in all cases, it is still the flicker noise after up-converted with its multiplication ratio $N = f_{RF}/f_{ref}$. Figure 5-8 shows PN profiles of the 3 cases where the RTC is referred to an XO design from [42]. The RC oscillator is referred to [40] and the RF signal shows both single tone and GFSK modulated signals without considering noise up-conversion due to the mixer. The corresponding simulated frequency accuracy with their approximated averaging number of periods are also shown.

Figure 5-8 (a) shows a typical RTC design divided from a high frequency XO oscillator. For previous 32.768 kHz RTC designs, it's rare to report phase noise performance at such a low frequency. So [42] is chosen as an example of RTC for its 'excellent noise performance'. The blue line is its original measured phase noise at 38.4MHz and the yellow

line is the divided RTC noise performance. To be fair for all 3 cases, the red lines in all PN plots are up-converted to the same center frequency at 2.4GHz in ISM band. The corresponding N-period-average jitter and Allan Deviation of that RTC reference are shown below in Figure 5-8 (a) as well. As the flicker noise corner of the RTC is around 50 kHz, the resulting number of periods where ADEV turns flat is close to 4000. The behavior simulation using such PN profile shows a similar result.

Figure 5-8 (b) represents an excellent RC oscillator design. [114] reported its phase noise performance at 10MHz, which is redrawn in the blue line. The red is the up-converted PN at 2.4GHz as well. As can be seen from the NPAJ and ADEV plots, they also have a $N_c \approx 4000$ as the flicker noise corner is around 50 kHz as well. But since its noise performance is much worse than the RTC case in Figure 5-8 (a), both jitter performance and ADEV are around one magnitude worse than the RTC case.

The recovered RF signals were shown in Figure 5-8 (c). The single tone RF signal is directly coming from an open loop LC oscillator design at 2.4GHz while the other is GFSK modulated representing a general BLE packet. It has a 1Mbps data rate and 500 kHz frequency deviation. Although the PN performance could both be much better by incorporating a PLL design, the open loop cases shows the worst possible performance in the BLE compliant radios and shows a relatively high flicker noise corner. A PLL based design will eventually be limited by the frequency reference in the transmitter side. As seen from the jitter and ADEV plots, the two cases will converge with the increase of number of periods although the GFSK modulated case deviates from the single tone case in the middle. For the single tone case, the flicker noise corner is around 500 kHz and both the jitter and ADEV turns flat at around 400 periods. The jitter and ADEV plot for the GFSK

modulated case could be more complicated, since with the limited behavior simulation results, those regions have been masked by the blue line.

The above simulation results further show that it is the flicker part of the PN profile that eventually defines the frequency accuracy after calibration. Other noise sources only affect the time needed for the average process to achieve the flicker noise associated frequency accuracy. Figure 9 shows the relation between flicker PN and corresponding ADEV at 2.4 GHz. It can be seen that the RC oscillator from [115] shows a 2^{-5} ADEV while XO and RTC would offer around 6^{-9} ADEV. The RF signal, no matter modulated or not, would be able to offer better than 2^{-6} ADEV assuming no further noise up-conversion from the receiver. If we take BLE as an example, as it has been proved that an open-loop LC oscillator can meet BLE phase noise requirement [111], we could specify phase noise requirement of its reference from the analysis above. According to the Bluetooth standard [41], it requires $\pm 150\ kHz$ frequency offset, which corresponds to a 60ppm frequency accuracy requirement in Allan Deviation. It can be seen that all the example cases shown in Figure8 could meet this requirement, even the RC oscillator from [12]. To be more specific, any oscillator within 60ppm accuracy with accurately characterized temperature coefficient can be used as a frequency reference in an XO-less BLE edge nodes. The recovered RF modulated signal without considering the up-conversion effect in the receiver path would meet that requirement as well.

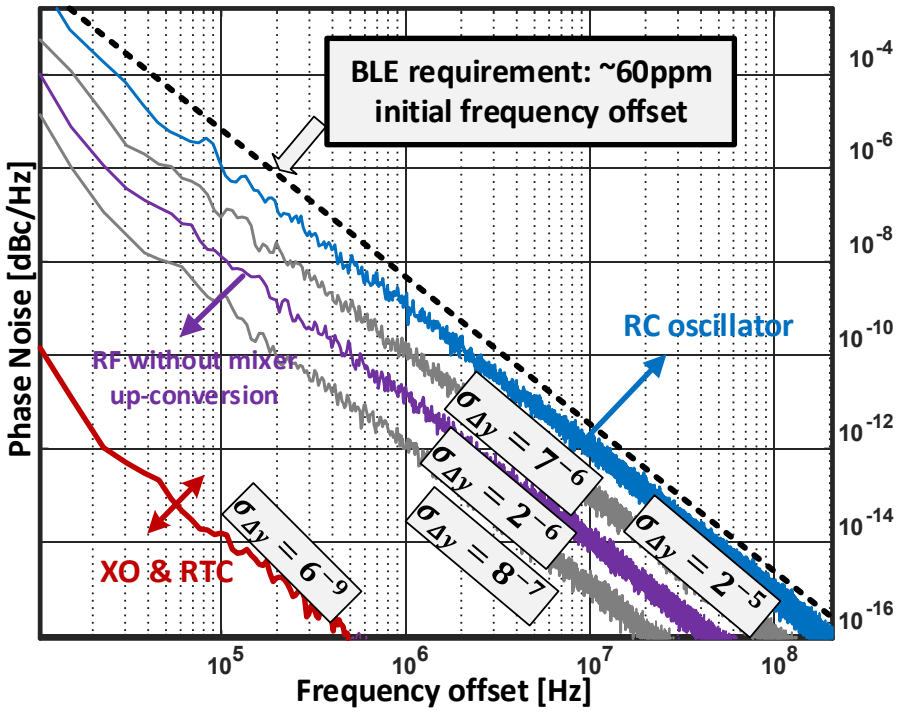


Figure 5-9 Typical range of Allan Deviation according to flicker noise of different noise sources, and requirement for the reference clock in Bluetooth Low-energy applications

5.5. An XO-less BLE transmitter with RF reference recovery receiver

Figure 5-10 shows the block diagram of the proposed XO-less BLE transmitter with the RF reference recovery receiver and its working scheme. It's a collaborated project with Abdullah Alghaihab and Yao Shi. The focus of this thesis is highlighted in green in Figure 5-10. A BLE back-channel receiver [85] is implemented to help with channel estimation and coarse frequency tuning of LO1. LO1 hops over the advertising channels of BLE during this period and oversamples incoming patterned advertising packets, and thus predicts when the BLE packet will come in CH. 39 and coarsely tune the frequency of LO1 to 2.48GHz within $\pm$ 1MHz accuracy. Then the RF reference recovery block will start the fine tuning of LO1. The RF BLE packet is down-converted to 8 MHz then amplified and filtered as the reference of both PLL1 for reference locking, and PLL2 for TX carrier

generation. As analyzed in the section 5.5, the GFSK modulation on the reference clock will result in extra phase noise but won't affect the frequency calibration accuracy providing enough averaging time in the PLL. The 2 PLLs utilizes the same recovered RF reference but are locked to 2 BLE ADV channels with different frequency control words (FCW). Their relationship with RF reference frequency can be summarized as follows:

$$f_{LO1} = \frac{FCW_1}{FCW_1 + 1} f_{RF} \qquad (5-26)$$

$$f_{LO2} = \frac{FCW_2}{FCW_2 + 1} f_{RF} \qquad (5-27)$$

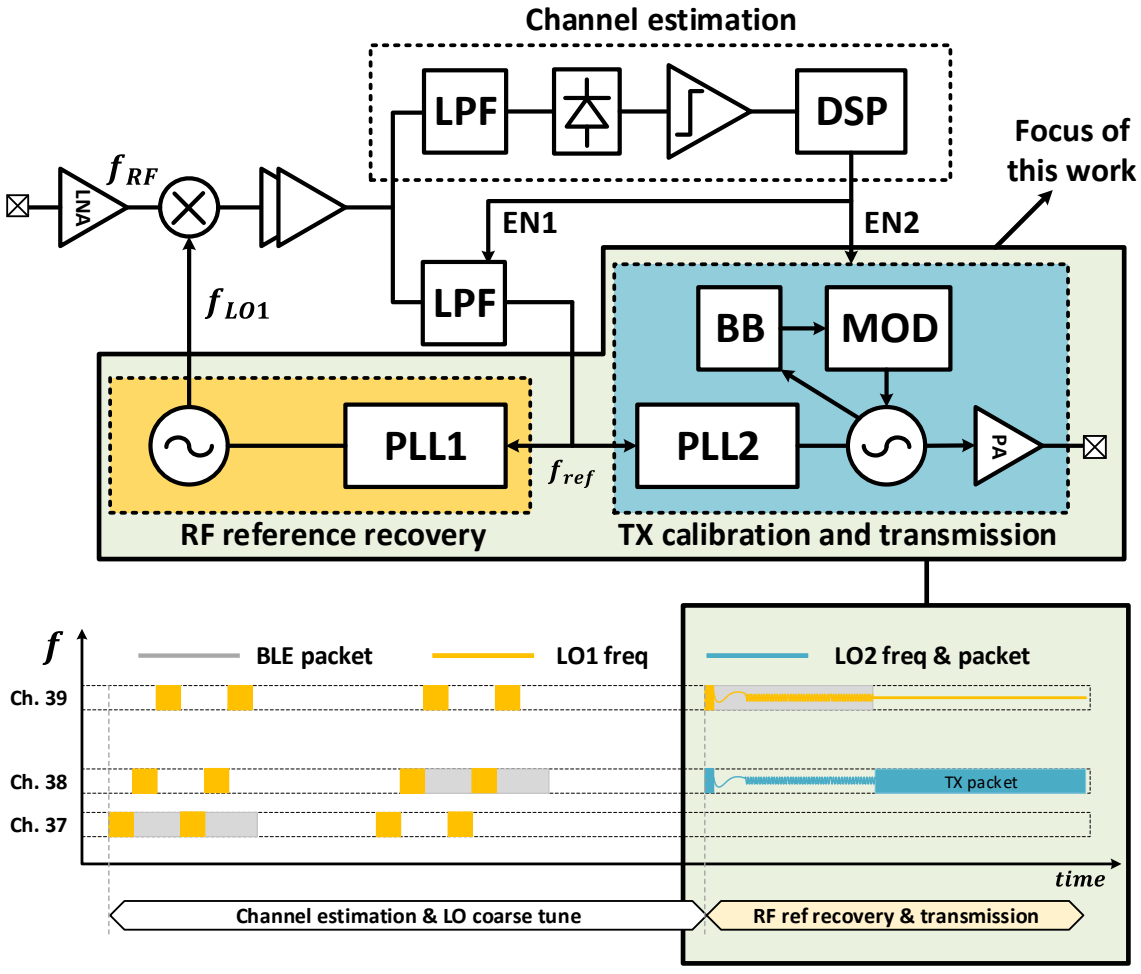


Figure 5-10 Block diagram of the proposed XO-less BLE transmitter with RF reference recovery receiver and timing diagram showing the frequency calibration scheme of the LOs

Once the frequency of LO2 is calibrated to the targeted BLE channel and the DCO control word (DCW) is acquired after the averaging process in the PLL, the PLL will be open loop. The DCO will be GFSK modulated by one BLE packet, which is clocked by a divided LO2 frequency.

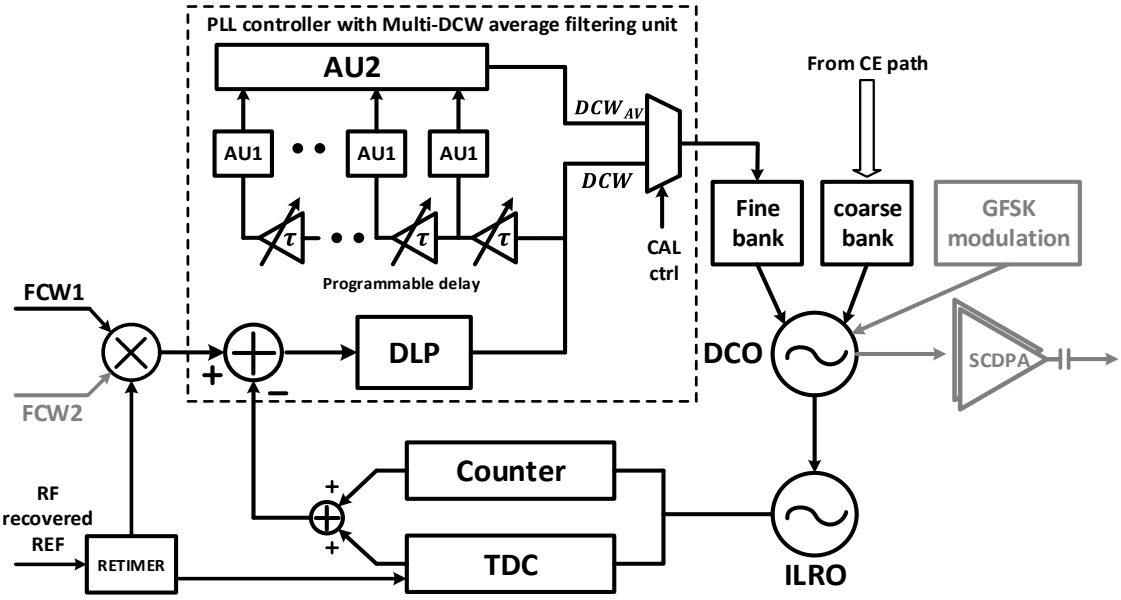


Figure 5-11 Block diagram of the proposed PLL with embedded multi-DCW average filtering unit

This section is going to be focusing on the yellow and blue blocks showing in Figure 5-10, including the PLLs, oscillators and the PA. Figure 5-11 shows the block diagram of the proposed PLL used in the RF reference recovery block and TX calibration and transmission block. It is based on the traditional type I divider-less ADPLL with a multi-DCW average-filtering unit (AU) embedded in the PLL controller. The AU performs average filtering with 2 stages. The first stage consists of several average sub-units controlled by programmable delays and programmable average time windows. As mentioned in section 5.3, the sub-units are chosen to get rid of large fractional-N spurs close to the carrier and the resulting DCW pattern associated with the spur position. The

second stage controls the total time for average filtering according to the flicker noise corner of the reference.

The PLL bandwidth is programmable as well, ranging between 20 kHz to 100 kHz. As analyzed in previous sections, the total phase noise seen by the AU is the sum of the PN coming from the reference, TDC and DCO. And the frequency calibration accuracy is only affected by the flicker noise coming from the reference. So the PLL bandwidth doesn't affect the overall noise performance. However, for this application, the minimum PLL bandwidth is defined by the total of PLL settling time and AU calculating time while the maximum PLL bandwidth is defined by the fine DAC tuning range of the LCDCO. As for incoming BLE packet for frequency calibration, the available calibration time is around 300μs and AU calculating time is at least tens of μs according to the flicker noise corner of the reference. Thus, the PLL shall be able to settle within 200 μs. On the other hand, as the reference carries GFSK modulation, the time varying DCW shall not exceed the fine DAC tuning range.

The LCDCO is using a typical CMOS architecture with both NMOS and PMOS cross coupled pairs as the negative resistance stage and a digitally tuned resistor tail, which is adopted from Yao Shi's previous design [117]. The tail resistor will help prevent the transistors enter triode region, thus improving the phase noise performance. The injection locked RO TDC is similar to the RO design in Figure 4-7. It has 6 pseudo-differential RO cells providing 12 TDC phases, which will result in a -80dBc/Hz in-band phase noise, as demonstrated in Chapter 3 & 4. Figure 5-12 shows the simplified circuit design of the LCDCO and the ILTDC. The PA is low power switched-capacitor digital PA and has the same design as Figure 4-10, which is optimized for low power efficiency as well.

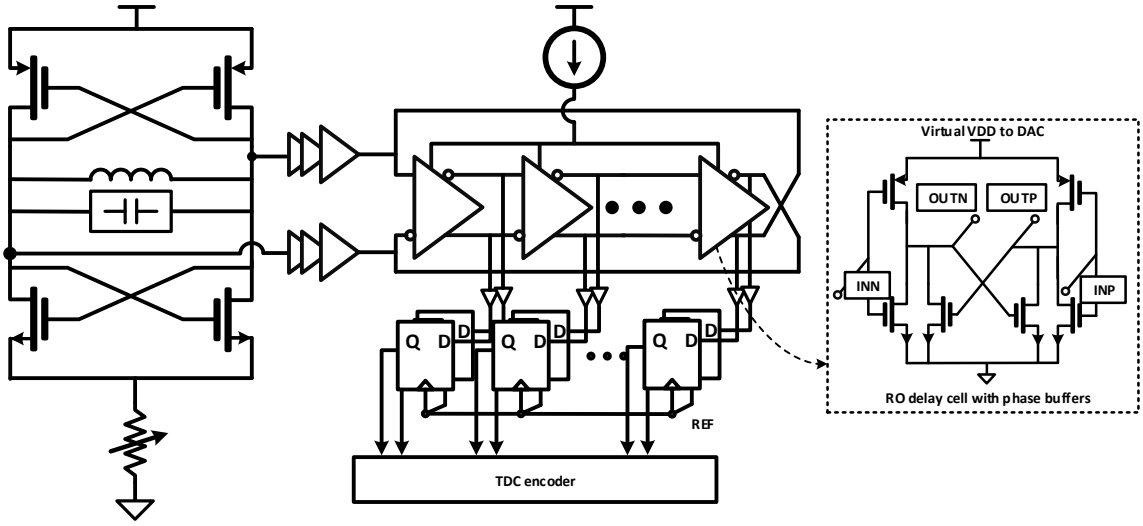


Figure 5-12 schematic of the LCDCO and the ILTDC

Simulation of the frequency accuracy improvement is shown in Figure 5-13. The top two figures are using single tone RF reference while the bottom two figures are using GFSK modulated RF reference with random bits. The phase noise setup is the same as the one shown in Figure 5-8. When single tone RF reference is used, the improvements of frequency accuracy is significant even if the averaging time is small. However, if the reference is modulated, with practical averaging time, the improvements is not as effective as single tone input. When N equals to 1024 with the 8MHz reference frequency in this design, the necessary averaging time is 128 μs, and the frequency can be easily calibrated into the standard required ±150 kHz frequency offset in packet transmission. When the averaging time is 16 μs with N equals to 128, there will be around 3% chance that the frequency offset will be larger than required.

Direct measurement of the frequency calibration accuracy is hard to achieve, as once the desired DCW is calculated and the PLL becomes open loop, the frequency accuracy will be again dominated by the total phase noise profile rather than the flicker phase noise profile as analyzed from previous sections. In order to achieve real time monitoring, an on-

chip jitter testing block shall be included in the design. Indirect measurements from the DCW could be used as the DCW is associated with period jitter (and N-period average jitter) and frequency errors in a PLL. But since it is a sub-sample system, the impact of sample and hold should be taken into account as extra noise would be folded at lower frequency offset [116]. In this design, as we didn't pull out enough signal through PADs of this measurement, this testing results would not be able to be included.

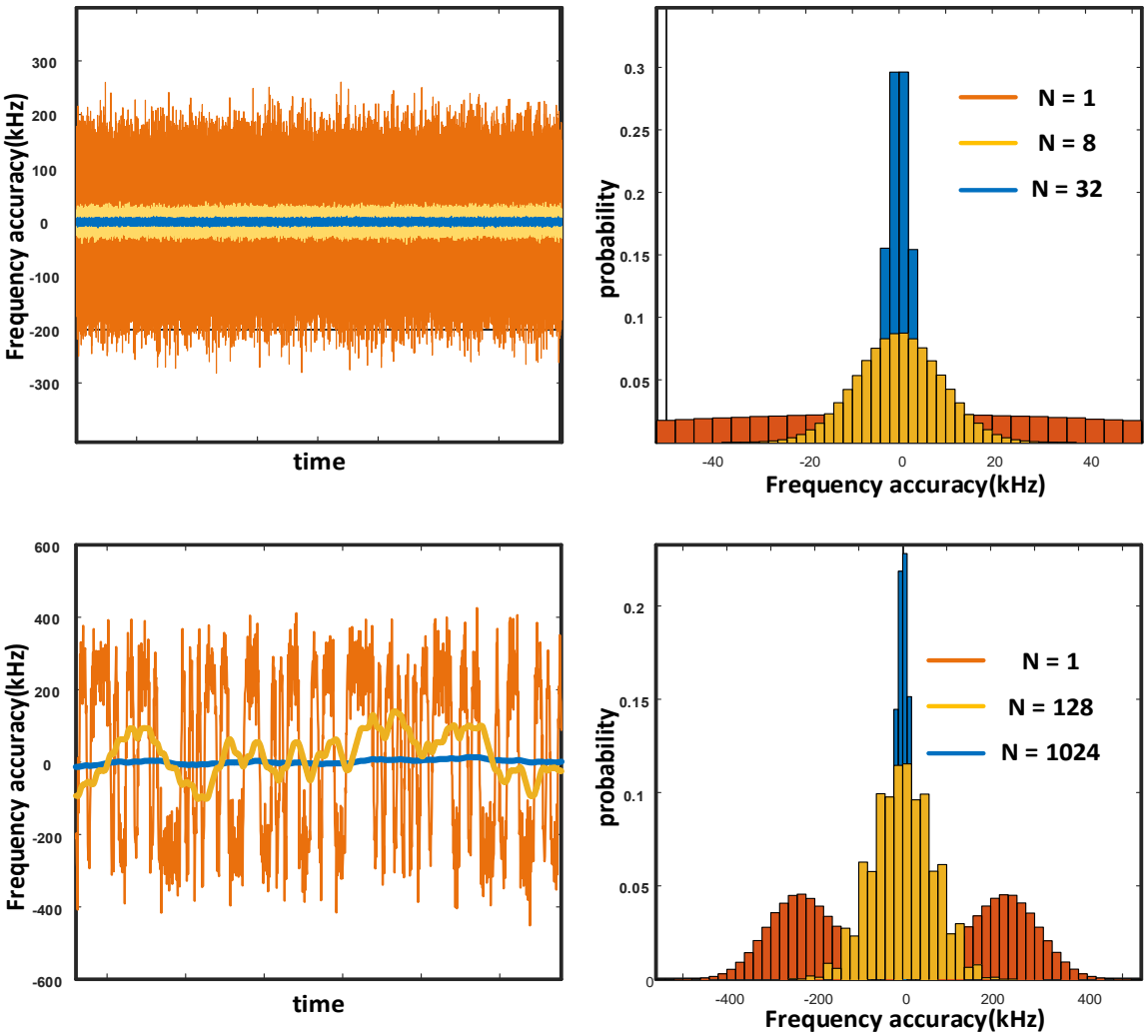


Figure 5-13 simulated frequency accuracy improvements of the AU with single tone and GFSK modulated RF reference

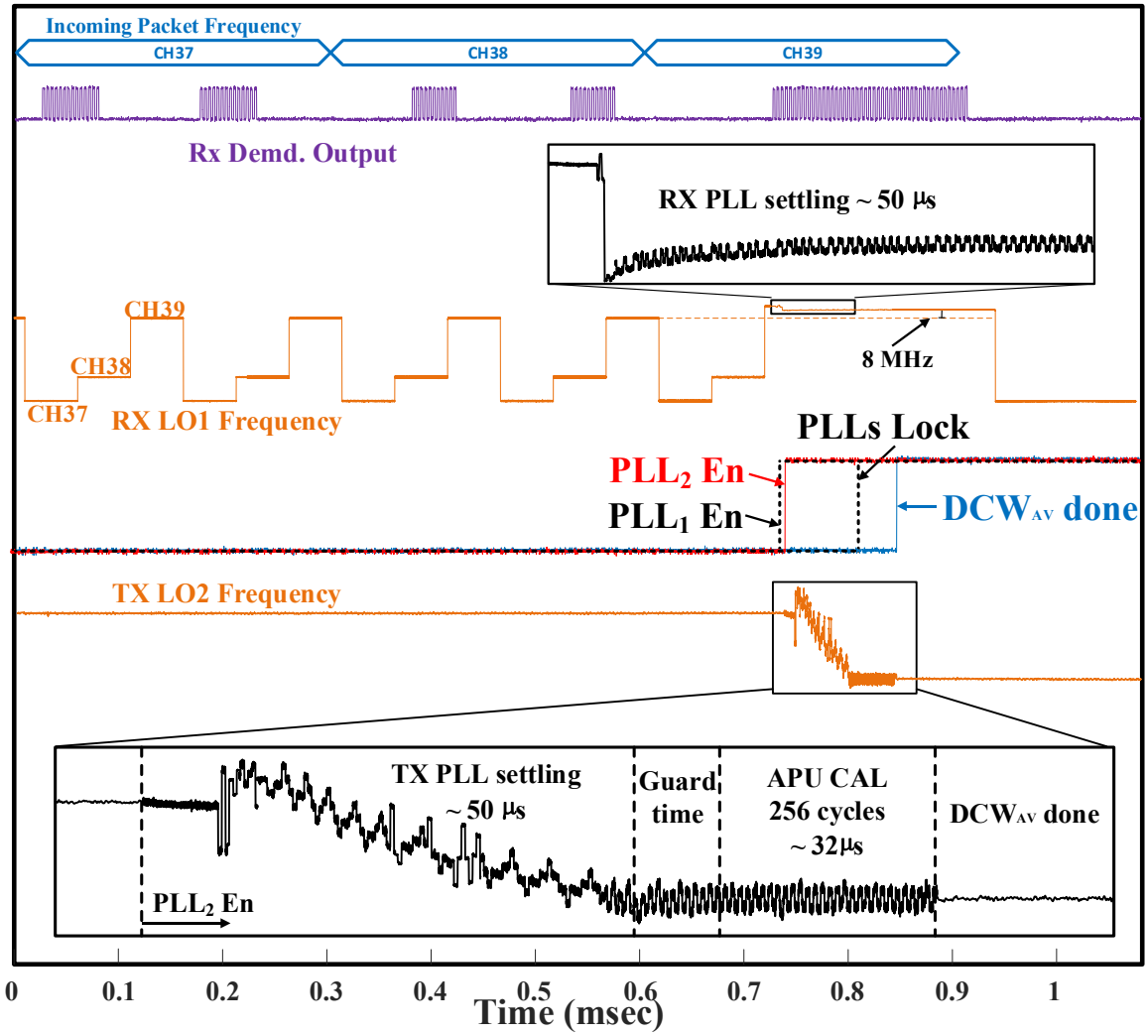


Figure 5-14 Measured frequency response of the TX/RX LOs over time

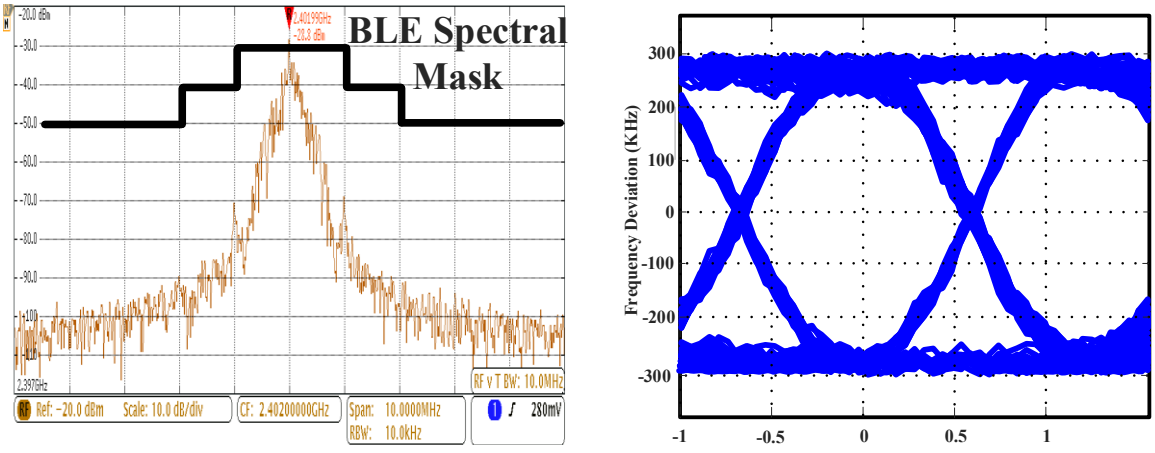


Figure 5-15 Measured BLE TX spectrum and eye-diagram

Figure 5-14 shows the measured frequency response of the TX/RX local oscillators over time. After channel estimation, LO1 is locked to 2.480 GHz while LO2 in the transmitter is locked to 2.402 GHz for beacon transmission. In this setup, the PLL settling time is 50 µs for both LOs using a small PLL BW to filter the FSK signal in the reference. After the PLL is locked with certain guard time for frequency settling, the APU embedded in the loop filter will calibrate the DCW for 256 reference cycles in 32 µs and generate a new DCW that settles the frequency closer to the target in one measurement. In this measurement, the FSK reference is consecutive 1 and 0s. Figure 5-15 shows the spectrum measurement of the BLE TX and eye-diagram. The die photo of the proposed XO-less BLE TX is shown in Figure 5-16.

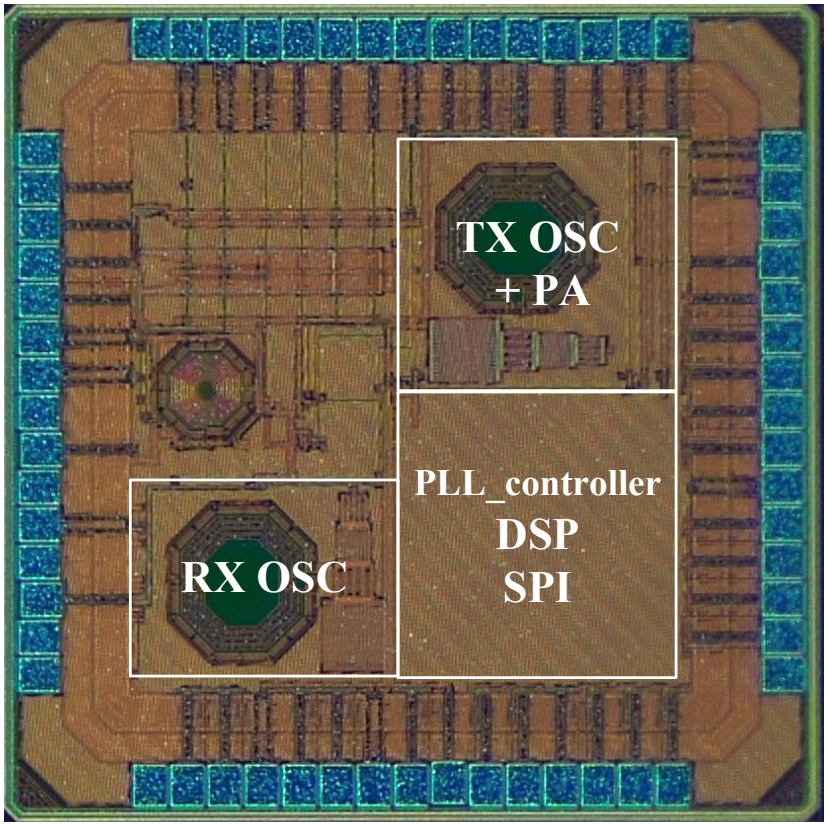


Figure 5-16 Die photo of the proposed XO-less BLE TX with RF reference recovery receiver

5.6. Conclusion

In this paper, phase noise and frequency accuracy has been analyzed for XO-less wireless edge nodes. The relationship among phase noise, different kinds of jitter, and both short term and long term frequency accuracy has been analyzed considering different phase noise profiles. It has been found that flicker noise plays an important role in defining how accurate the frequency of an oscillator could be over a long period of time. N-period-average jitter is introduced to characterize the long term frequency accuracy together with the widely used Allan Deviation.

In order to filter other noise sources and reach the flicker noise associated frequency accuracy limit in the frequency calibration process, we propose an embedded average processing unit in ADPLL by using the N-period-average jitter concept and thus directly link the frequency reference in a PLL to the overall calibrated frequency accuracy. Different frequency references XO has been evaluated through behavior model simulation. The results show that although XO based RTC offers significantly better performance compared to recovered RF reference and RC oscillators, the latter two can actually be used in frequency calibration even in some wireless communication standards, such as BLE. With the help of the APU, state-of-the-art RC oscillator could be used as a crystal replacement in the low cost wireless edge nodes designs. However, this paper only considers phase noise's impact on frequency accuracy without taking PVT variations into account. Thus, when design RC oscillator based systems, it has to be pre-characterized and a temperature sensor has to be included as well. The recovered RF signal, on the other hand, is more promising in the XO-less edge node designs as the incoming signal from a base station is already characterized. The modulation wouldn't necessarily affect the

frequency calibration result providing enough time for the average process. But the tradeoff is actually in the receiver design. Designers have to balance between receiver sensitivity, blocker performance and the mixer noise up-conversion.

CHAPTER 6

Conclusions

Frequency synthesizer is one of the most important and sophisticated sub-system in radio designs and the key building block for further power and cost reduction in ultra-low power wireless integrated systems. Phase noise, as the primary specification in PLL and frequency synthesizer designs, is hard to be directly linked with radio design tradeoffs due to its complexity and the lack of a thorough system level interpretation. Thus, in order to reduce the radio power consumption to its physical limit while maintaining the standard required performance with sophisticated modulations, low power frequency synthesizer design is critical and has to be assisted with clear theoretical guidelines. On the other hand, removing the crystal oscillator in standard compliant radios such as BLE is appealing yet proved to be more challenging, and the limiting factor points to phase noise and PLL design as well. This thesis addresses the above issues by proposing system-focused phase noise theories, novel system architectures and low power circuit techniques.

The phase noise theories proposed in this dissertation can be separated into 2 parts. Chapter 2 and Chapter 3 can be viewed together as a top-down approach analyzing phase noise, jitter, and the resulting IFV in typical frequency modulated radio systems and PLL sub-systems. All noise sources in an ADPLL, such as the DCO, TDC, DAC, and reference, will contribute to a complex output phase noise profile that contribute to IFV. This IFV, as

a stationary process in frequency domain, represents the short term frequency errors over time and can affect frequency modulated wireless systems directly in various ways. It can be directly associated with bit error rate (BER) and modulation index etc., and further associated with SNR and sensitivity, making PN of the PLL sub-system a direct variable in link budget calculation from the radio system's point of view. In standard compliant radios, the IFV can be directly linked to standard specifications such as modulation eye diagram as well. The benefits of the use of IFV in frequency modulated wireless systems are 3-folded. The first is it offers a different angle in LO design for wireless transceivers. Apart from the generally known idea associating LO PN to RX blocker tolerance due to reciprocal mixing, this method of PN analysis enables FSK radios to be designed in a different way, especially transmitters in the ULP wireless edge nodes. The second is it offers a set of benchmarking specifications from the radio system, down to PLL sub-system, and further down to circuit blocks, making it easier for circuit designers to do tradeoffs between different circuit blocks. The third one is subtle but rather appealing to novel digital radio design methodologies. Although not demonstrated in this dissertation, but as part of a big project related to my research work, the top-down 'specification tree' would be helpful in fully autonomous wireless SoC design and synthesis. Such all linked 'specification tree' would be the baseline for automation tools in circuit design.

The second part of the proposed PN theory is a 'time extended' version of Chapter 2&3, but focusing more on frequency accuracy and stability of PLL due to its different PN sources, especially the reference noise. A more comprehensive relationship among different kinds of jitter, phase noise and frequency/phase error is summarized. As discussed in chapter 2, IFV is related to period jitter and represents the short term frequency error,

N-period-average jitter can be used to define long term frequency error and the N-period cycle-to-cycle jitter defines the long term frequency error rate. And it is found that the commonly used Allan Deviation (ADEV) in characterizing frequency accuracy is N-period-average cycle-to-cycle jitter divided by the total measurement time. Chapter 5 further reveals that it is the flicker noise in the reference of the total PLL output PN profile which dominate the frequency accuracy and stability. Other noise components from the PLL could be averaged out in measurement, or in other words, removed by a simple averaging algorithm. The unfiltered, low frequency flicker PN from the reference will eventually dominate the long term frequency accuracy and stability of the frequency synthesizer. This PN analysis would be able to help evaluate different kinds of references impact on long term PLL frequency accuracy as long as the PN profile of the reference itself is clear.

Several chip prototypes were implemented as demonstrations of the proposed PN theory. And they are all designed with state-of-the-art power-performance efficiency in their technology nodes. The first prototype is a 2.4GHz FSK transmitter in 65nm technology. It utilizes a SAR-assisted all-digital frequency locked loop and ultra-low power ring oscillator for frequency calibration and a switched-capacitor digital power amplifier for data transmission. It consumes 634μW in low power mode and is integrated with a battery-less SoC in a continuous sensing and post processing wearable SiP. This chip shows how the IFV due to PN affect the BER of an FSK communication system with different data rate, frequency deviation in a high SNR regime.

The second prototype is an all-digital ring oscillator-based Bluetooth low-energy transmitter for ultra-low-power radios in short range Internet-of-Things. The proposed

transmitter features: 1) a wideband all-digital phase-locked loop with a quarter RF frequency RO and an embedded 5-bit TDC; 2) a 4 x frequency edge combiner to generate the 2.4-GHz signal; and 3) a switch-capacitor digital PA optimized for high efficiency at low transmit power level. These help reduce the power consumption and improve PN performance at the same time, and also enhance the TX efficiency for short range communications. The TX is prototyped in 40-nm CMOS, occupies an active area of 0.0166mm^2, and consumes 486 μW in its low power mode while configured as a non-connectable BLE advertiser. As the first reported RO based BLE transmitter, it achieves a 10X power reduction and 40X chip area compared to state-of-the-art BLE transmitter designs that has been validated by wireless communication to a mobile phone. The TX design uses the PN theory proposed in Chapter 2 and finds the IFV limit associated with BLE modulation requirement, bringing down the TX power consumption and cost down to its physical limit.

The third prototype is an XO-less BLE transmitter with an RF reference recovery receiver in 40nm CMOS. The focus of this design is to use a typical ADPLL with an embedded average processing unit to extract the correct frequency control words for valid BLE data transmission in the target advertising channel, even with the received RF signal as its reference. The contribution of this work has to be closely related to the PN theory proposed in Chapter 5. The multi-DCW average filtering unit embedded in the loop filter of the ADPLL could filter the noise effect from white PN, flat PN, spurs and modulation introduced noise pattern and retrieve the accurate frequency information from the reference assuming the reference frequency follows a stationary random process. This cost-effective

APU unit in ADPLL could help frequency calibration with different kinds of XO replacement, such as RTC, RC oscillator and the recovered RF reference.

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