Interface Engineering and Practical Applications of Amorphous Silicon Based Opto-electronic Devices for Large-Area Electronics

by

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Dedication

To my whole family, my friends

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Abstract

In this dissertation, we extensively studied intrinsic amorphous silicon (a-Si) hybrid structure with inorganic / organic materials and explored the potential practical applications. Meanwhile, we still stepped into the various transparent electronic devices, including the transparent organic TFTs and memristors based on the developed transparent ultrathin metal film electrodes.

Top cathode contacts based on the conjugated organic materials were developed in our group, we further developed the air-stable cathode contacts based on the Polyethylenimine (PEI) and ZnO interlayers. We found the dipole induced in the PEI layers is highly related to the surface properties of the adjacent interlayers. The dipole between ZnO / PEI interlayers is supposed to be overcome by another one induced between PEI and cathode metal. Then we move to the investigation on the bottom anode contacts. We analyzed the band diagram and the carrier lateral transportation of the WO_x / a-Si interfaces. We found the WO_x / a-Si interface is able to to support centimeter-scale non-electrode area, without the additional conductive layers. From the developed anode and cathode contacts, we further characterized the electrical performance of the a-Si devices as photodetectors (PD), and re-designed device structure towards the applications of in-screen fingerprint scanners. The a-Si PDs with top cathode contacts based on ZnO NPs and PEI interlayers can achieve the LDR up to 190 dB, and at least 4 orders for the illuminations < 50 Lux. The current sequence in the short linear arrays exhibited good ratio up to 2 orders. The inverted a-Si PD with bottom cathode contacts were developed and characterized to fulfill the requirements of the architecture design for the sensing arrays. The ZnO and MoOx are employed as the ETL and HTL. The current leakage and LDR are analyzed for different a-Si

thicknesses and device areas. Finally, the optimized a-Si PD arrays are fabricated on the LTPS TFT backplanes. In order to meet the development opportunities for the neuromorphic computation, innovative artificial synapses were demonstrated based on the interactions between the a-Si and PEI interlayers. The hysteresis and timing dependent plasticity of the artificial synapses can be excited by light illumination, coupled with electrical pulse stimuli. The device design is promising to serve as fundamental elements for neuromorphic functionalities towards the simultaneous visual information process in large-area electronics or IoT.

Transparent electronics is the hot research area to promote the information interactions. We also fabricated transparent devices based on the ultrathin transparent metal films and the corresponding optical management. Transparent resistive switching devices were demonstrated based on ultrathin doped Ag films and optically optimized dielectric / metal / dielectric structure. The overall transparency is higher than 80%, and the device conductance modulation is found to be analog and continuous. Transparent organic TFTs were achieved based on ultrathin Cu-based composite electrodes with Ni seeding and capping layers. The transparency is up to 71.4 % for the source/drain regions and even higher for the overall transparency.

Finally, based on the developed a-Si photodetectors, we proposed the potential development optimizations. The first one is the transparent a-Si optoelectronic devices based on all-inorganic interlayers. Then the optical design can be further conducted to modulate the absorption spectrum of a-Si active layers as well as the exterior apparent colors.

Chapter 1 Introduction and Background Review

1.1 Basic Properties of Amorphous Silicon

Silicon (Si) is a chemical element with the atomic number of 14, which defines the properties as tetravalent metalloids and semiconductors. It is a hard and brittle crystalline solid with a blue-grey metallic lustre, as shown in Figure 1.1. Silicon is the eighth most common element in the universe by mass, but very rarely occurs as the pure element in the Earth's crust, most widely distributed in dusts, sands, planetoids, and planets as various forms of silicon dioxide (silica) or silicates. More than 90% of the Earth's crust is composed of silicate minerals, making silicon the second most abundant element in the Earth's crust (about 28% by mass) after oxygen. [1]

Figure 1.1 Silicon ingot after preliminary purifications. (Reproduced from [1]).

Si is a fourfold coordinated atom that is normally tetrahedrally bonded to four neighboring silicon atoms. According to the organization of the atom lattice, we can

classify it as crystalline silicone, poly-crystalline silicon, and amorphous silicon, as shown in Figure 1.2. In the crystalline silicon, the tetrahedral structure continues over a large range, thus forming a well-ordered crystal lattice. In the poly-crystalline silicon, the ordered tetrahedral structure only continues over a short range, just like the tight stacking of small grains. However, it forms a random orientation in a long range. In the amorphous silicon, the long range order is not present. Rather, the atoms form a continuous random network. [2]

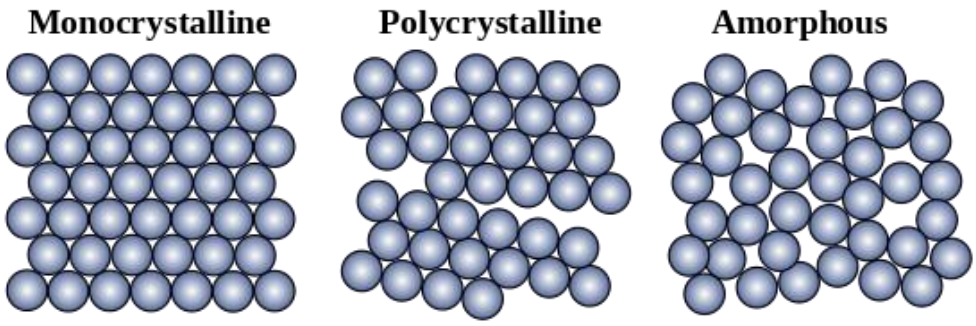

Figure 1.2 The atom lattice for the monocrystalline, polycrystalline and amorphous materials, which are long range ordered, short range ordered and disordered, respectively. (Reproduced from [2]).

Silicon is the important and fundamental semiconductor materials in the integrated circuit industries. The silicon can be doped by phosphorus (P) atoms (5 valence electrons) or boron (B) atoms (3 valence electrons). The P atom can contribute a free electron to the Si lattice to form a closed and paired outer shell with neighboring Si atoms, creating the excess n-type carriers, and demoted as N-doping. On the contrary, the B atom will take an electron away from the Si lattice to form a closed and paired outer shell with neighboring Si atoms, creating the excess p-type carriers and demoted as P-doping.[3] Utilizing different doping types and profiles, we can create N-channel or P-channel FETs on Si wafers, and thus build the complete hierarchy of the integrated circuits from the fundamental devices.[4] As promoted by the stringent requirement for a lower cost and the continuous evolving of the photo-lithography technology, the channel length is gradually shrinking to only 1s nanometers, as predicted or guided by the Moore's law.[5] Besides being used as semiconductor material in the FETs for the

purpose of logic calculation, the crystalline Si is also a fundamental semiconductor materials for the opto-electronic devices or chips, such as the Si photodiodes or CMOS image sensors embedded in the DSLR cameras.[6-8]

Polycrystalline Si is becoming an important semiconductor candidate for the transistors used in the active matrix driving the high resolution and large area Flat Panel Display screens, because of its high mobility and easy fabrication process from the amorphous Si. Moreover, polycrystalline Si has been widely used in the solar cell industries, as a basic semiconductor material for the standard 6 inch square solar cell panels. The panels can be assembled to make the large-scale solar cell plants and provide power for houses, offices, or even factories.[9]

Amorphous Si (a-Si) was the dominant semiconductor material for the commercialized thin-film transistors (TFTs) fabricated for the active matrix backplanes in TFT-LCDs, owing to its low cost and easy deposition.[10] Meanwhile, a-Si is also extensively used in the solar cells. Because of the low deposition temperature, it can be deposited on a variety of rigid or flexible substrates, such as glass, metal or even PI films, as shown in Figure 1.3.[2] However, it is suffering a low efficiency because of the high trap density, determining its main target market is the customer electronics with low power consumptions, such as calculators or digital watches, as shown in Figure 1.4.

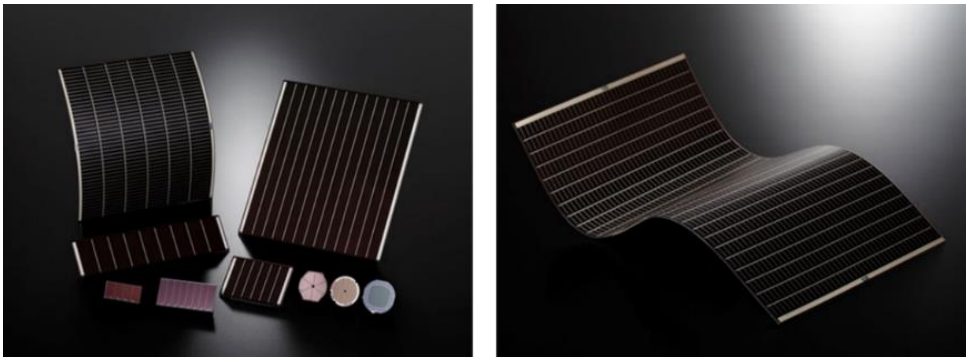

Figure 1.3 Solar cells based on a-Si, fabricated on the rigid or flexible substrates. (CopyRight @ Amorton)

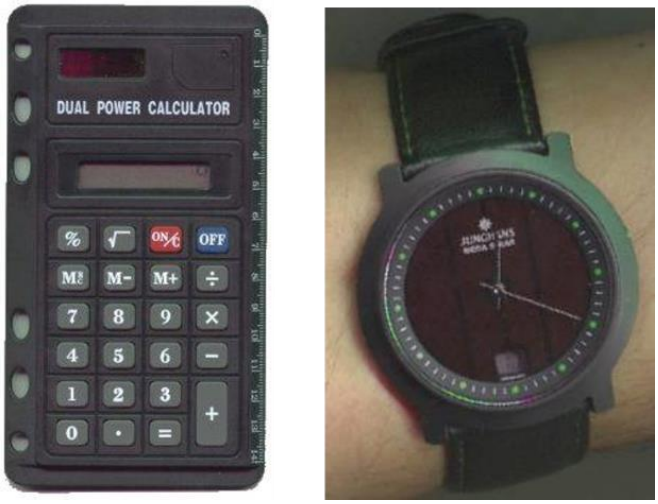

Figure 1.4 Customer electronic products (calculators and watches) equipped with a-Si solar cells. (Reproduced from [2])

Although the silicon atoms have 4 valence electrons ready to be paired with the neighbor atoms, not all the atoms within a-Si are fourfold coordinated in a-Si. Part of the Si atoms have unpaired valence electrons and the corresponding dangling bonds due to the disordered nature of the material, as shown in Figure 1.5. The dangling bonds mean the defects in the random network of the atom lattice, which limits the electrical performance of a-Si used for transistors, solar cells or photodiodes. Fortunately, the dangling bonds can be passivated by hydrogen (H) atoms, since H atoms have one valence electron, which can be paired with the unpaired valence electron in the dangling bonds. Just because of the H passivation, a-Si can be named as Hydrogenated amorphous silicon (a-Si:H), which has a sufficiently low amount of defects, particularly in the protocrystalline growth regime. People usually use the short name “a-Si” instead of “a-Si:H”, without special notifications, since the hydrogenated a-Si is a standard deposition process for a-Si. However, hydrogenation is highly related to light-induced degradation of the material, described as Staebler–Wronski effect (SWE). The most favoured explanation is the H bond switching model, where the weak Si-Si bonds can be broken by the non-radiative energy released from the recombination of the photo-excited electrons and holes, and a back-bonded H atom prevents the restoration of the broken bond by a bond switching event.[2, 11-13]

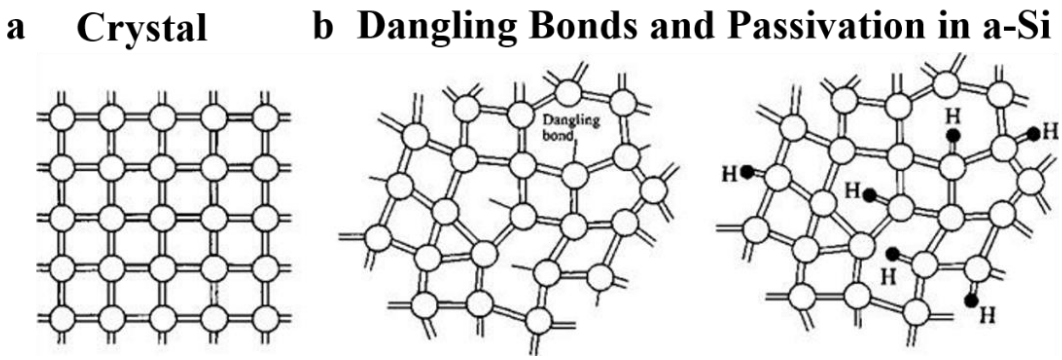

Figure 1.5 Schematic structures of crystalline silicon, amorphous silicon, the dangling bonds in the amorphous lattice and the corresponding hydrogenation passivation for the dangling bonds. (Reproduced from [2]).

As we know, the a-Si is just named from its long-range structure disorder, which means the wave functions for the random atom lattice can not be sufficiently and uniformly overlapped, resulting in no sharp edges for the conduction bands and valence bands. Referring to the band diagram shown in Figure 1.6, there are band tails near the band bottom or top, which behaves as shallow traps and plays an important role for the carrier transportation. Meanwhile, the dangling bonds create defect states in the mid-gap, thus create a secondary conductive pathway and introduce additional leakage for the a-Si devices.[14]

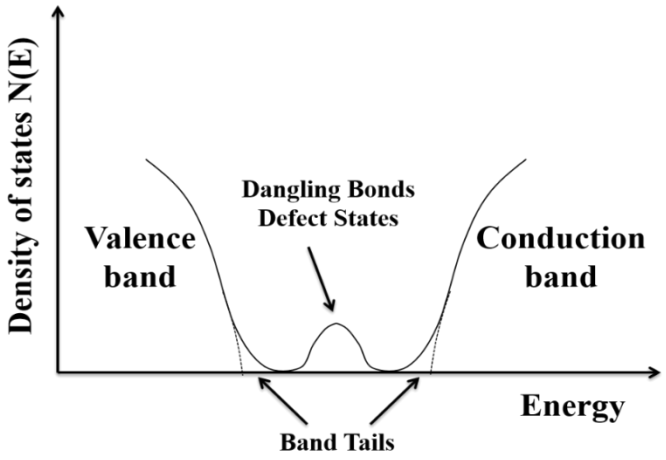

Figure 1.6 Schematic density of states distribution for amorphous silicon, showing the bands, the band tails, and the defect states in the band gap. The dashed curves are the equivalent density of states in a crystalline silicon. (Reproduced from [14])

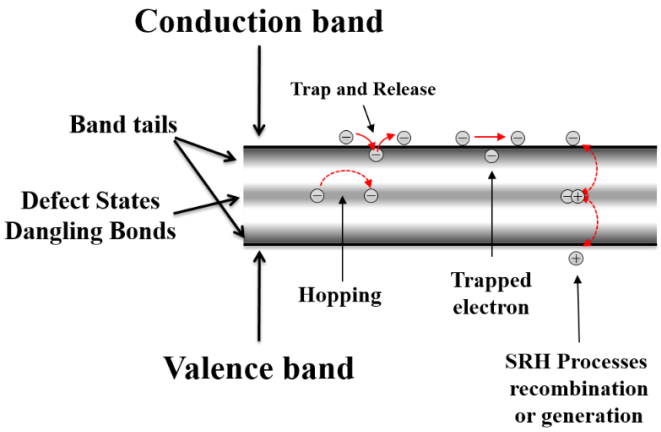

Figure 1.7 Schematic illustration of the conduction mechanisms related to the amorphous silicon. (Reproduced from [14])

There are several electronic processes related to the conduction / valence bands, band tails as well as the defect states induced by dangling bonds, as shown in Figure 1.7. We use electron transportation as an example to clarify the electronic processes. Usually, the electron transportation occurs near the bottom edge of the conduction band, which defines the mobility of the electrons. Because of the shallow traps in the band tails, the electrons can get trapped, then released through the thermal excitation, which is mainly considered as ohmic conduction. When the electrons approaching a trap filled by a trapped electron, they will go over the traps without being trapped, indicating a higher mobility or conductance, which occurs during the strong injection or generation of carriers in a-Si. Moreover, the defects induced by the dangling bonds are very deep from the band edges. If electrons dropped to those states, it is possible for them to hop between the adjacent states through the tunneling processes, which can be promoted at elevated temperatures, and will produce unexpected leakage between the interlayers or contacts sandwishing the a-Si layers. The traps or defects distributed between the conduction band and valence band can serve as the centers to assist Shockley-Read-Hall (SRH) processes, including the recombination or generations, which will adversely affect on the opto-electronic conversion efficiency and increase the current leakage.[15]

1.2 PECVD Deposition of Amorphous Silicon

Chemical Vapor Deposition (CVD) is the standard method for the deposition of a-Si, including the Low Pressure CVD (LPCVD) and Plasma Enhancement CVD (PECVD). PECVD is utilizing the plasma atmosphere to provide additional energy for the reactive gas, thus requiring a lower process temperature, compared with the LPCVD. The chuck temperature in PECVD chamber is usually in 200 – 400 °C, while the LPCVD is around 425 – 900 °C. The energy supplied by plasma provides the key advantage of reduced process temperatures for PECVD, compared to LPCVD where all of the energy for reaction is supplied thermally. Therefore, the PECVD allows the deposition on a large variety of substrates, including on glass, metal, or even plastic films. As shown in Figure 1.8, the reactant gases flow to the process chamber through a shower head which is a large perforated metal plate located above the sample, and produce a uniform distribution of the gas flow over the sample surface. The 13.56 MHz RF power is used to generate the plasma, and the electrons with high energy in the plasma ionize or dissociate the reactant gases to generate more chemical reactive radicals. These radicals react to form the thin films of deposition on top of the sample. The following equations are the typical reactions for the Si-based materials, including silicon nitride, silicon oxide, silicon oxynitride, as well as a-Si. The Plasmatherm 790 is the equipment model for the a-Si films we are using, which includes PECVD and RIE chambers at the same time, as shown in Figure 1.9. [16]

$$SiN_x : SiH_x + NH_x \longrightarrow SiN_x\left(+H_2\right)$$

$$SiO_x : SiH_x + N_2O \longrightarrow SiO_x\left(+H_2 + N_2\right)$$

$$SiON_x : SiH_x + N_2O + NH_3 \longrightarrow SiON_x\left(+H_2 + N_2\right)$$

$$aSi : H_x : SiH_x \longrightarrow Si\left(+H_2\right)$$

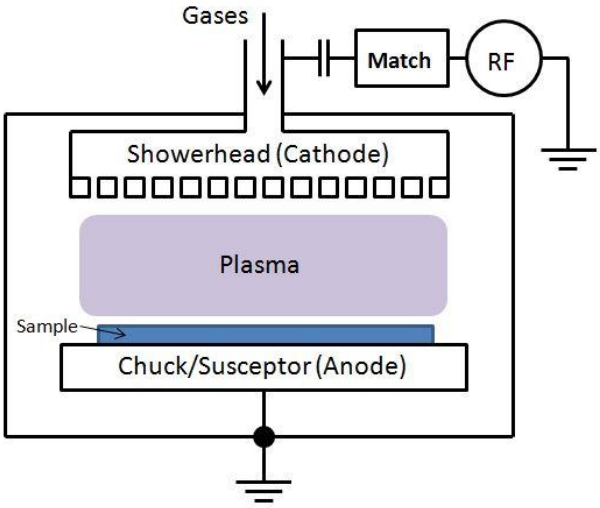

Figure 1.8 PECVD chamber structure, including the chuck, sample, shower head and the gas supplying. (Reproduced from [16])

The quality of a-Si active layers is highly related to the deposition conditions. The pressure is determined by the collisions of the gas molecules, which greatly influence the location of the reactions, in the gas flow or on the sample surface. A proper gas flow rate can maintain the supplying of the reactive radicals, and get rid of the depletion. RF power is used to control the dissociation rate, then determines the deposition rate. Meanwhile, the substrate temperature also influences the reaction speed on the sample surface. The deposition rate is supposed to be optimized to guarantee the quality of the a-Si films.

Figure 1.9 PECVD Plasmtherm 790 for a-Si deposition, which is used for the a-Si active layers in the devices we worked on.

1.3 Working Principles of the Solar Cells and Photodiodes

Both of Solar Cells and Photodiodes are used to convert the light illuminations to the electricity, and share the same fundamental working principles to maximize the collection efficiency of the photo-generated carriers. However, solar cells are used to provide power to the external load, while the Photodiode is used to detect the light intensity from the external illumination, which determines the different characterization specifications or optimization aims.

As shown in Figure 1.10, the basic devices of a-Si Solar Cells or Photodiodes are composed of transparent substrate and anode, hole transportation layer (HTL), a-Si active layer, electron transportation layer (ETL) and the top cathode metal. Usually, p-doping and n-doping a-Si interlayers are used for the HTL and ETL, respectively, to form the p-i-n structure. The generation and separation of the photo-generated electron-hole pairs mainly occur in the a-Si layer since the highest electric field drops in the a-Si layer, and the HTL or ETL are used to form good contacts with anode or cathode maximizing the carrier collection efficiency. Anode is usually placed at the incident illumination side allowing the holes to traverse a shorter average distance to the anode because of its lower mobility than the electrons. [17, 18]

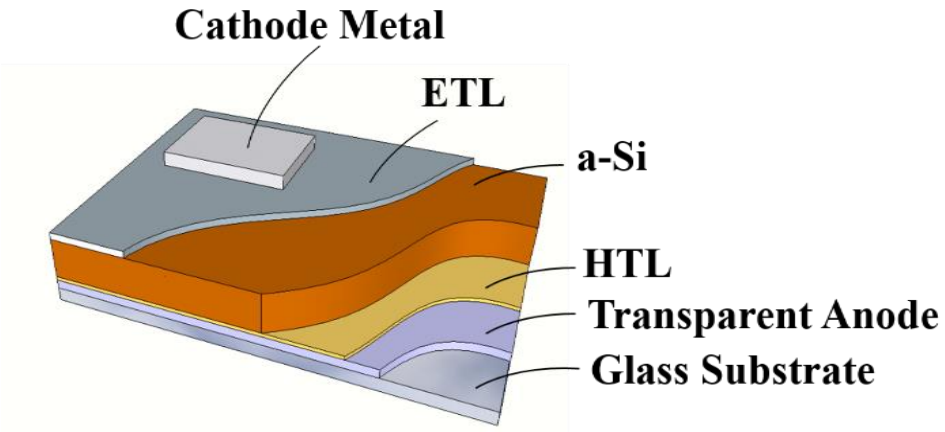

Figure 1.10 The schematic illustration of the devices, for the solar cells or photodiodes, which includes the substrates, transparent anode, HTL, active layer, ETL and the top cathode metal.

Conventionally, the p-doped and n-doped a-Si layers are used as HTL and ETL, respectively. The dopants are introduced during the PECVD deposition of a-Si layers

with the gas phase molecular containing P or B atoms, such as PH_3 or BH_3.[19] The P atom can contribute one excess electron, while the B atom can contribute one excess hole. Correspondingly, the Fermi levels will be modulated to approach to the CB in n-doped layer, and to the VB in p-doped layer. The biggest advantage of the doped a-Si layers is the homo-junctions to the sandwished intrinsic a-Si active layers, which means compatible deposition processes, and good affinity or contacts by doping dose profile modulations. However, some drawbacks still exist. Firstly, the doped a-Si layers need a certain thickness to contain sufficient dopants and realize the roles in the electronic structure as contacts, typically weak 10s nm. The light illumination for the intrinsic a-Si layer will be reduced because of the similar band gap and absorption coefficients of the doped or intrinsic layers, thus resulting in the unnecessary efficiency reduction. Moreover, the electron-hole pairs are still generated in the doped layer, and they will be recombined quickly, because of the high excess carriers, the recombination centers induced by the ionized dopants, as well as the low electric field. Therefore, the photons absorbed in the doped layers do not actually contribute to the photo-electric conversion.[14]

People started to consider apply various metal oxides as HTL for the a-Si devices, which can reduce the light absorption of HTL layers and promote more new electronic properties of the a-Si devices. As shown in Figure 1.11, the authors investigated the interface properties between Moly Oxide or Tungsten Oxide and a-Si layers, and the corresponding thermal stability.[20, 21] Although the metal oxides expand the device design and optimization space, it also means introducing the challenges at the same time for the device design, lifetime or reliability, even for the process compatibility during the commercialization. Most works of this dissertation are based on the heterojunctions of a-Si layers, and we investigate the interactions between metal oxide and a-Si for the devices towards various application scenarios.

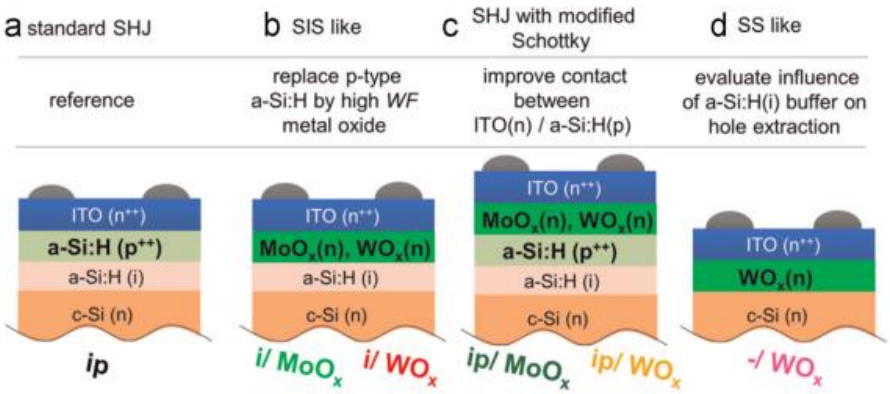

Figure 1.11 Schematic of investigated front sides which form the hole selective contact of simple planar solar cells. Above the sketches is the motivation for the respective structure. Below the sketches the acronyms used throughout this work to distinguish between the different structures are shown. (Reproduced from [20])

1.4 Compact Model for Solar Cells or Photodiodes

The opto-electrical behaviors of the devices are indeed based on the fundamental device physics, and the device modeling can simplify the physical processes and promote the simulations for the fast device design and mechanism explanations. On the other hand, the external systems are more interested in the electrical properties related to the terminals, such as anode/cathode for diode-based devices, or source/drain/gate for the transistor-based devices, not in the detailed electronic processes inside of the devices. Therefore, the compact models are created to provide a conceptual view for the opto-electrical behaviors related to the terminals for the external circuits.

As shown in Figure 1.12, the compact model for the solar cells and photodiode are almost identical, where the basic components include a diode (D1) with a forward current I_d representing the device configuration for the active layer sandwished by the HTL/anode and ETL/cathode, and a current source representing the photocurrent (I_{ph}), without considering the parasitic series resistance (R_s) and shunt resistance (R_{sh}). The biggest difference is the polarity of the applied voltage. The cathode of the diode in the model need to be grounded, and the other terminal was applied by the voltage (V_a). In the solar cell mode, $V_a > 0$, D1 is forward biased with a current I_d and the I_{ph} is counteracted by the I_d. If the net current (I_{ph}-I_d) > 0, it will follow out to the V_a, which

means the model is providing power to the external loads. In the photodiode mode, V_a < 0, the D1 is reversed biased with a negative I_d (I_d < 0) and the net current (I_{ph}-I_d) > 0. The net current still flows out to the V_a terminal, which means the model is receiving power supply from external sources. Therefore, they are sharing quite similar device structures, but the solar cells work in the fourth quadrant, and photodiodes work in the third quadrant.

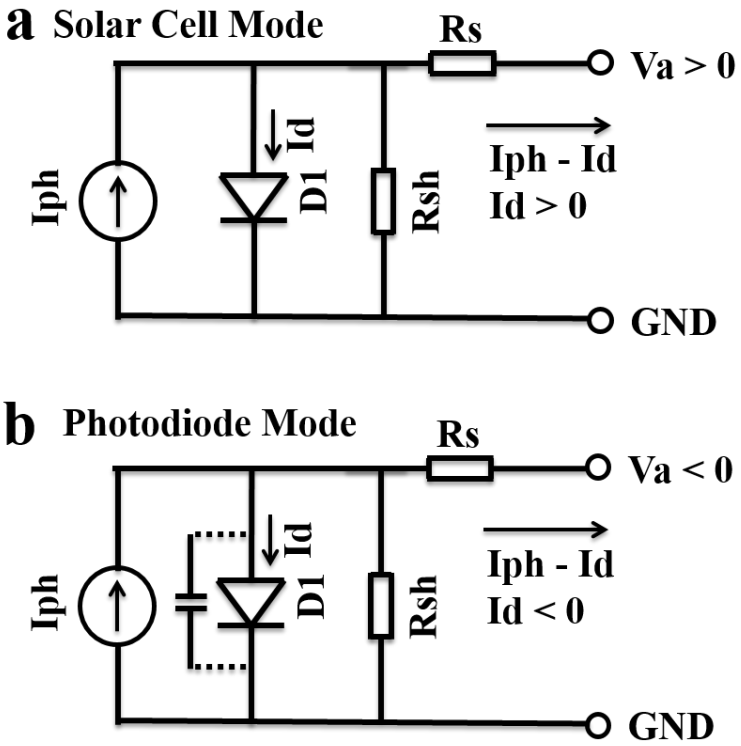

Figure 1.12 Equivalent circuits of solar cells (a) and photodiodes (b). They are sharing almost identical equivalent circuits, including a current source, a diode, shunt resistance and series resistance. On the other hand, the equivalent circuit of photodiode also includes a capacitor for the transient response characterizations. (Reproduced from [22, 23])

Let us further discuss the details for the model. The photodiode (D1) is the key component, representing the recombination through SRH processes or band-to-band transitions. Sometimes, people use two diodes in the model to accurately simulate the opto-electrical behaviors, since different recombination modes occur for the different biases or illuminations. For example, the SRH recombination is limited by the minority carriers under low injection, while it is limited by both types of the carriers under high

injection. Moreover, if other recombination or conduction mechanisms are taken into account, such as Auger recombination or tunneling conductions through the barriers, it becomes more challenging for the modeling.[24, 25] Anyway, the one-diode model will give a fast simulation or evaluation for the electrical analysis.

Both of solar cells and photodiodes are producing photocurrent (I_{ph}), which stems from the generation and separation of the photo-generated electron-hole pairs, mainly occurring in the photoactive layers, such as in the intrinsic a-Si layers of a-Si devices. Then the electron-hole pairs separate, diffuse through HTL and ETL, then get collected to the anode or cathodes to form the I_{ph} for the external circuits. Sometimes, the contacts for electrons or holes are not equally perfect, which means one type carriers can not be efficiently collected, resulting in the S-shaped IV curves and a reduced conversion efficiency.[26, 27] The I_{ph} is usually well proportional to the light illumination intensity, however, it will be limited by the diode leakage current or the measurement precision under ultra-low illumination, and deviates from the linearity under ultra-high illumination because of the voltage-drop on the series resistance.

Back to the R_s and R_{sh}, they are key parameters to maximize the photo-conversion efficiency. R_s is the resistance connected in series to the anode or cathode, which is usually determined by the contact properties, including the energy band matching, surface traps, surface dipoles induced in the interlayers, and so on. R_{sh} is the resistance connected in parallel to the diode, which is determined by the film quality of the active layers, or the band diagram of the whole device structure. The film with bad quality may contain pin-holes, resulting in the unexpected leakage under voltage biases. If the overall band diagram of the device was not well matched, it will create the electron leakage current to the anode or vice versa. For solar cells, R_s consumes the power generated by the I_{ph}, and R_{sh} equivalently increases the recombination rate for the photo-generated carriers, reducing the I_{ph} and fill factor, therefore small R_s and high R_{sh} are demanded to achieve a high photo-conversion efficiency. On the other hand, in photodidoes, the net current (I_{ph} - I_d) is constant for a certain illumination since the reversed current ($I_d < 0$) for D1 is constant. At this point, R_s is impeding the net current

to flow to the V_a terminal, and R_{sh} is the additional conductive pathway for the leakage from GND to V_a, in addition to the net current (I_{ph} - I_d), which increases the dependence on the external applied voltage V_a. A stable net photo current is required for the photodiodes under reversed bias, to maximize the linearity and create a reliable range for the external circuit design.

Besides the static performance, dynamic or transient performance is also important for photodiodes. Therefore, a capacitor needs to be added in the modeling in parallel to the D1, a shown in Figure 1.12b. The capacitor is mainly from the junction capacitance, also from the parasitic capacitors related to the device electrodes in the measurement setup. Increasing the thickness of the photoactive layer is a straightforward method to reduce the capacitor, which will also facilitate the restriction of the leakage current, equivalently increasing R_{sh}.

1.5 Extensive Devices Based on a-Si Active Layers

Although a-Si deposition technologies have been developed for decades and were the previous dominant TFT technologies in the active matrixes of TFT-LCDs, right now it is still enabling the integration with various material systems, such as 2D materials, perovskites or conjugated polymers, to further extend the adversity of a-Si devices. In this thesis, we also describe various investigations and applications for a-Si based devices, such as the conductance modulation based on the metal oxide/a-Si interface, and the photo excited artificial synapses based on the a-Si / PEI interface. In the following, we are going to describe some works from the reported literatures to show the big picture of the versatile a-Si based devices.

Prof. Lemme group developed the multispectral photodetector based on the hybrid graphene / a-Si device architecture, and they even achieved flexible devices on the Au coated polyimide films, because of the low deposition temperature of a-Si. As shown in Figure 1.13, the single- and bi-layer graphene transparent conductive anodes are deposited by CVD. Various a-Si based semiconductors are deposited sequentially to

achieve the continuously modulated band gap to expand the light absorption band and maximize the responsivity, incorporating the broadband transmission of the graphene. The device allows single pixel detection of UV to visible light, and the maximum of photo-responsivity is up to 0.239 A/W.[28]

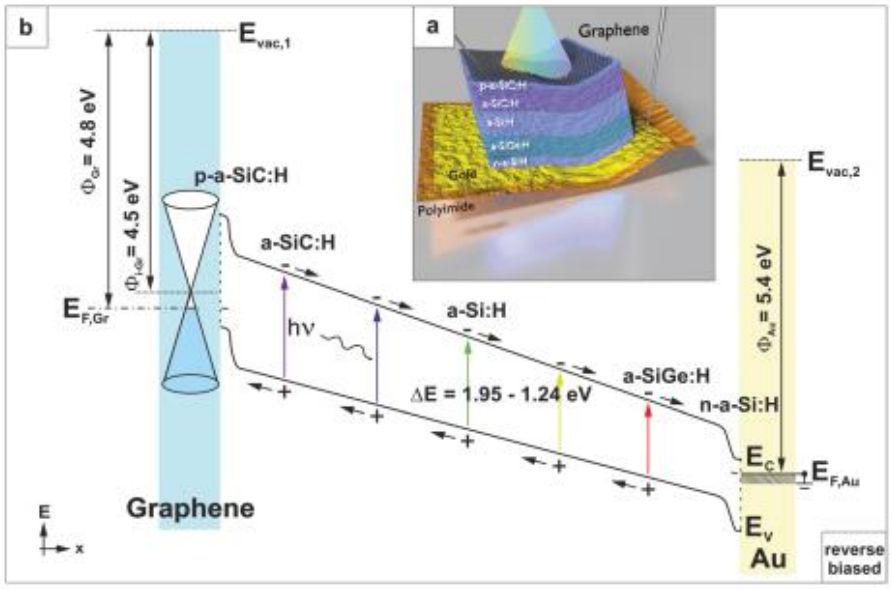

Figure 1.13 Schematic cross-section of a multispectral photodiode on polyimide substrate and energy band diagram of a gradually doped a-Si / graphene multispectral photodetector in reverse bias conditions. (Reproduced from [28])

People achieved high speed Molybdenum Disulfide (MoS_2) a-Si heterojunction photodetectors, as shown in Figure 1.14.[29] This device is basically a photo-transistor, and the channel materials are 60 nm mechanically exfoliated MoS_2 covered by 100 nm a-Si. The electron-hole pairs are generated by the absorption of photons in a-Si layers. The photogenerated electrons diffuse to the a-Si/MoS_2 interface and subsequently get swept into the MoS_2 layer. Due to the higher mobility of electrons in MoS_2, 2 or 3X higher than that of a-Si, the photoresponse for the a-Si / MoS2 photodetectors are much faster, compared to the ones based on a-Si only. If the photodetector were used in the flat-panel X-ray imagers, the fast response allows shorter x-ray exposure to patients which helps to reduce the health hazards.

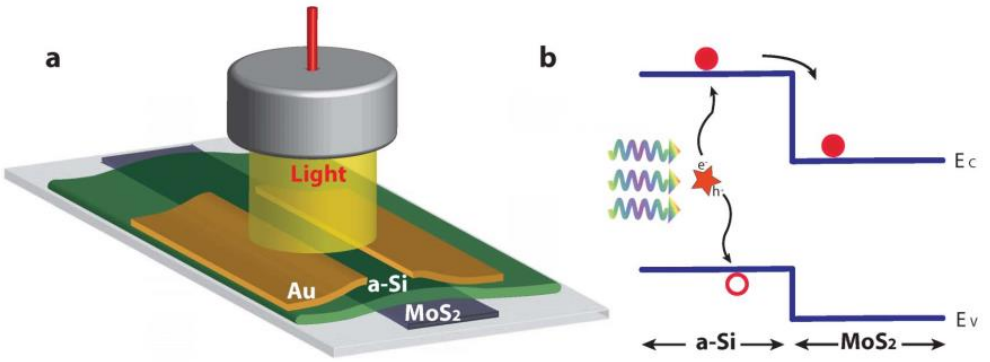

Figure 1.14 Operation concept of molybdenum disulfide a-Si heterojunction photodetector. (a) schematic and (b) energy band diagram of a-Si / MoS_2 heterojunction MSM photodetector. The light is incident from a-Si side, optical absorption occurs in a-Si, and photogenerated electrons diffuse to the underlying MoS_2 layer and are transferred across the MoS_2 layer toward a metal contact. (Reproduced from [29])

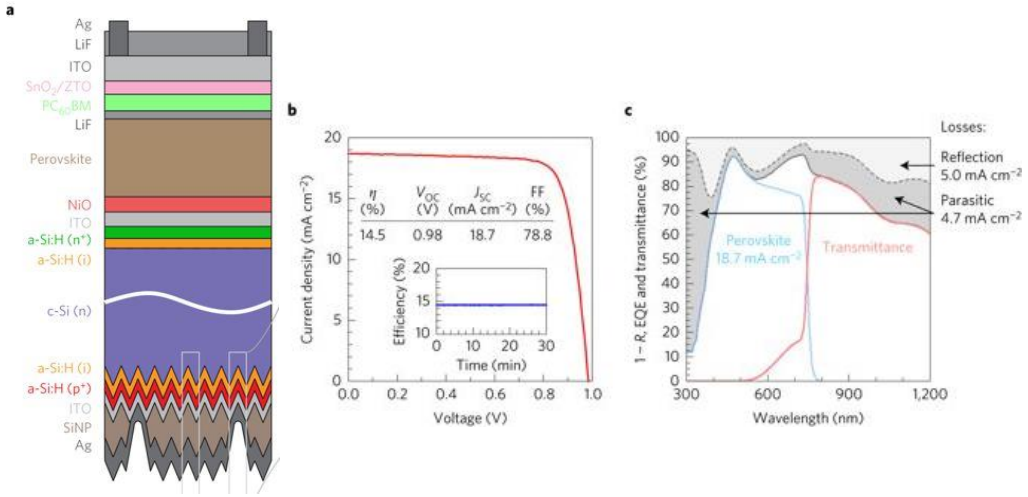

Figure 1.15 Design and performance of the perovskite/silicon tandem cell. IV characterizations and the efficiency at the maximum power point (inset) of the perovskite solar cell with illumination through the SnO_2 side. Total absorbance (1-R, where R is the reflectance; dashed grey line), EQE (solid blue line), and transmittance (solid red line) of the perovskite solar cell. (Reproduced from [30])

Moreover, the a-Si solar cells can also serve as a platform to be integrated with other solar cell technologies and achieve the tandem device designs for high power conversion efficiency. As shown in Figure 1.15, the transparent perovskite solar cells are integrated with the Si-based solar cells with a-Si passivation layers.[30] The rapid

rise of perovskite solar cells with record single junction efficiencies of over 22% can be ascribed to the combinations of unique properties, and they are becoming increasingly attractive for the use in tandem solar cells due to their wide, tunable bandgap and solution processability. In this work, the authors improved the efficiency of monolithic, two-terminal perovskite/silicon tandems to 23.6% by integrating an infrared-tuned silicon heterojunction bottom cell with the recently developed caesium formamidinium lead halide perovskite.

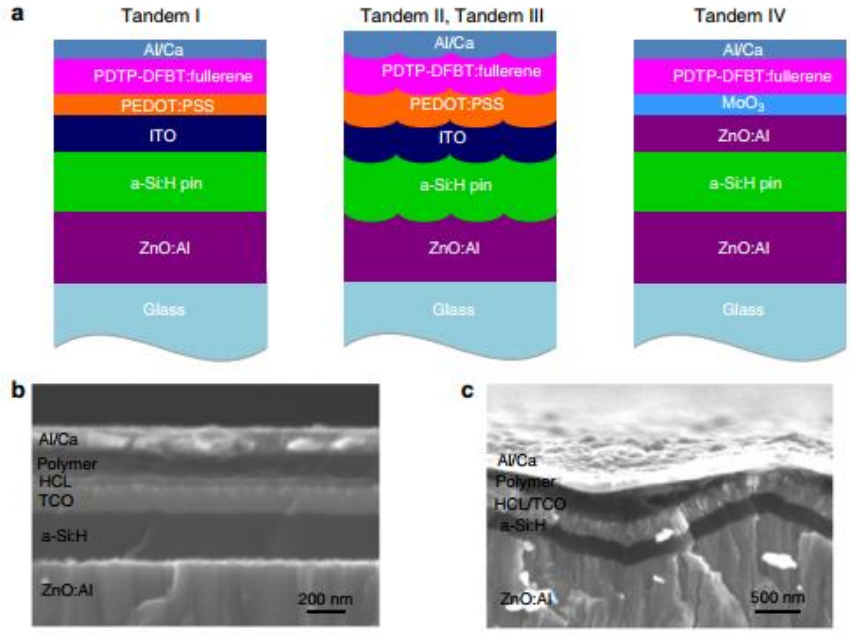

Figure 1.16 The structures of polymer / a-Si tandem cells. (a) The schematic of tandem architectures constructed. Tandem I and IV have flat surface morphology, whereas Tandem II and III have textured morphology. Tandem I, II and II used ITO/PEDOT:PSS to connect the two sub-cells, while Tandem IV employed ZnO:Al/MoO_3. (b) Typical cross-sectional scanning electron microscopic (SEM) images of a tandem cell made on a flat surface such as Tandem I and IV. (c) Typical cross-sectional SEM images of a tandem cell made on a textured surface such as Tandem II and III. (Reproduced from [31])

Conjugated polymers has been considered as excellent candidate materials for fabricating low-cost, light weight and flexible solar cell devices. People have demonstrated the integration of single junction a-Si and organic solar cells, to achieve a high power conversion efficiency of 10.5%, which is much higher than either of the two single junction solar cells, as shown in Figure 1.16.[31] Such high-efficiency thin-

film tandem cells are optimized by optical management and interface engineering of fully characterized front and back cells without sacrificing photovoltaic performance in both cells. They used AZO or ITO as interfacial conducting layers between a-Si and polymer cells, to promote electrical conduction, working as a cathode for the front sub-cell and as an anode for the back one. ITO was paired with PEDOT:PSS, while AZO was with MoO_3, as the strong acidic PEDOT:PSS etches ZnO:Al during a deposition process.

The a-Si solar cell device structure can also be applied as photocathode for the direct solar-to-hydrogen conversion via water splitting.[32] The solar cell was adapted to provide sufficient photovoltage to drive both the hydrogen and oxygen evolution reactions. In the standalone solar water-splitting systems, silicon based thin film technology stands out due to its chemical resistance, earth abundance and low cost production, presenting a promising pathway to the sustainable solar hydrogen production. Under operation of the device, the electrons are injected from the rear side (Pt layer) of the photocathode into the electrolyte for the hydrogen evolution reaction and thus the holes are transferred from the TCO front contact (SnO_2:F) of the photocathode to the anode (RuO_2) for the oxygen evolution reaction, as shown in Figure 1.17. However, this is a wired architecture since the photoanode is wired with the photocathode.

Based on the same working principle, people also demonstrated the wireless configuration to make the system more compact, as shown in Figure 1.18.[33] The authors use a triple junction, a-Si solar cells to interface the hydrogen- and oxygen-evolving catalyst made from an alloy of earth-abundant metals and a cobaltlborate catalyst, respectively. The wireless cell was constructed by deposition of the hydrogen-evolving catalyst, NiMoZn, onto the steel-backing substrate of the a-Si cell, and the oxygen-evolving catalyst on the top side. The cell architecture dictated that O_2 bubbles evolved from the illuminated anode at the front face and bubbles of H_2 evolved from the cathode at the back of the wireless cell.

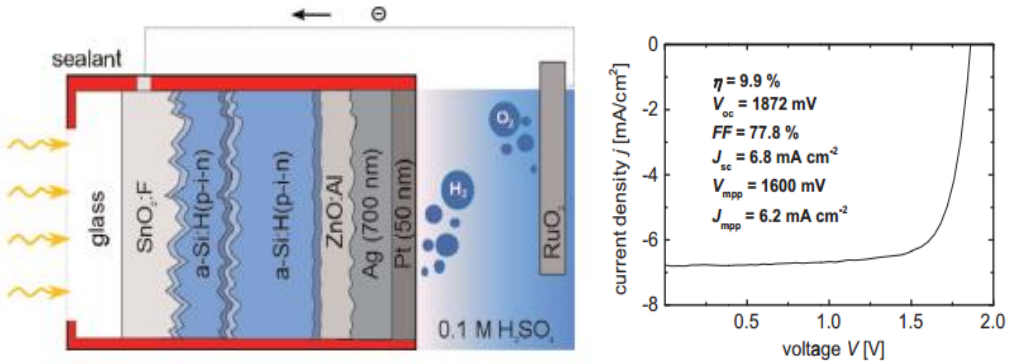

Figure 1.17 Schematic illustration of the integrated PV–EC device under operation with the a-Si / a-Si photocathode and a RuO_2 anode. Hydrogen evolution occurs at the rear side of the a-Si photocathode. Photocurrent–voltage measurement of the investigated a-Si tandem junction solar cell with a ZnO:Al/Ag back reflector. (Reproduced from [32])

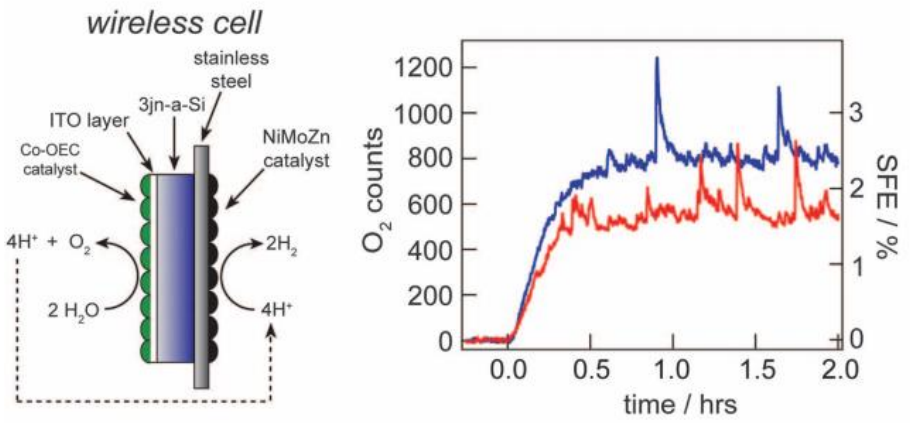

Figure 1.18 MS signal and SFE values for a wireless Co-OEC | 3jn-a-Si | NiMoZn cell under AM 1.5 illumination in 1 M KBi (red trace) and in 0.5 M KBi and 1.5 M KNO_3 (blue trace). The cell was illuminated over the 2 hours of the experiment; MS signal corresponds to the concentration of O_2 in the carrier gas of the cell. The spikes in the data originate from sudden release of gas bubbles that were adhered to the cells, resulting in a temporary increase of the O_2 concentration in the headspace. SFE values were calculated as described in the SOM. (Reproduced from [33])

1.6 Auger Electron Spectroscopy (AES)

The Auger effect is a physical phenomenon in which the filling of an inner-shell vacancy of an atom is accompanied by the emission of an electron from the same atoms. When a core electron is removed, leaving a vacancy, an electron from a higher energy level may fall into the vacancy, resulting in a release of energy. Although most often

this energy is released in the form of an emitted photon, the energy can also be transferred to another electron, which is ejected from the atom; this second ejected electron is called an Auger electron. Upon ejection, the kinetic energy of the Auger electron corresponds to the difference between the energy of the initial electronic transition into the vacancy and the ionization energy for the electron shell from which the Auger electron was ejected. These energy levels depend on the type of atom and the chemical environment in which the atom was located, as shown in Figure 1.19. Auger electron spectroscopy involves the emission of Auger electrons by bombarding a sample with either X-rays or energetic electrons and measures the intensity of Auger electrons that result as a function of the Auger electron energy. The resulting spectra can be used to determine the identity of the emitting atoms and some information about their environment.[34]

The AES is a surface characterization technique with an analysis depth of around 5 nm and a high lateral resolution down to 8 nm. Meanwhile, it can be equipped with an ion bombardment sputtering tool to achieve a depth profile to track the information of several atoms in the sample. The electrons in atoms are localized in different shells, such as K, L, M, N, and up to valence band (V), with different energy. Taking O atoms as an example, its atomic number is 8, and 8 electrons are localized in the K and L shells, where 2 in K, 2 in L1, 2 in L2 and 2 in L3. If the Auger transition involves the electrons in K, L1, L3, then the kinetic energy (KE) of the Auger electron is $KE = E_K - E_{L1} - E_{L3}$, where KE is independent of the mechanism of initial core hole formation. The Auger transition also involve the electrons come from other shells, denoted as LMM, MMV or NNV and so on.

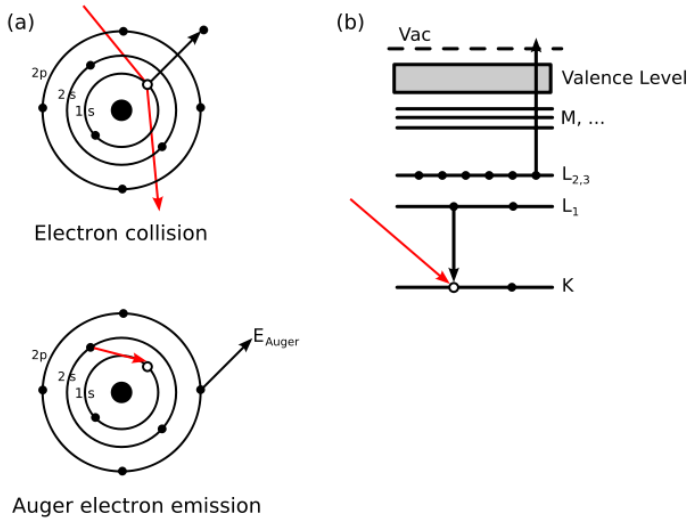

Figure 1.19 Two views of the Auger process. (a) illustrates sequentially the steps involved in Auger deexcitation. An incident electron (or photon) creates a core hole in the 1s level. An electron from the 2s level fills in the 1s hole and the transition energy is imparted to a 2p electron which is emitted. The final atomic state thus has two holes, one in the 2s orbital and the other in the 2p orbital. (b) illustrates the same process using X-ray notation, $KL_1L_{2,3}$. (Reproduced from [34])

The energy of the electrons in different shells will be influenced by the internal or external chemical environment. As shown in Figure 1.20, the KLL peak group for the Si atoms in SiO2 is left shifted compared to those in the elemental Si sample, which is because the electrons of the external shells are paired with O atoms, and the energy of the electrons the inner shells is increased due to the stronger attraction from the positive atom core. Similar principles also apply to the analysis for the different ionized atoms with same shells, such as the Na, F and O as shown in Figure 1.20. The AES peaks of the atoms with higher atomic number are right shifted because the energy of the electrons in all the shells are increased due to the higher positive charge in the atom core. Meanwhile, each transition mode will generate a peak group because each shell will be divided as several subshells, and the peak ratio is also highly related to the chemical state of the atoms. In this thesis, we extensively use AES to characterize the atomic ratio and chemical states for the O atoms in various metal oxides, which facilitates the verifications of the interfacial property analysis. [35-37]

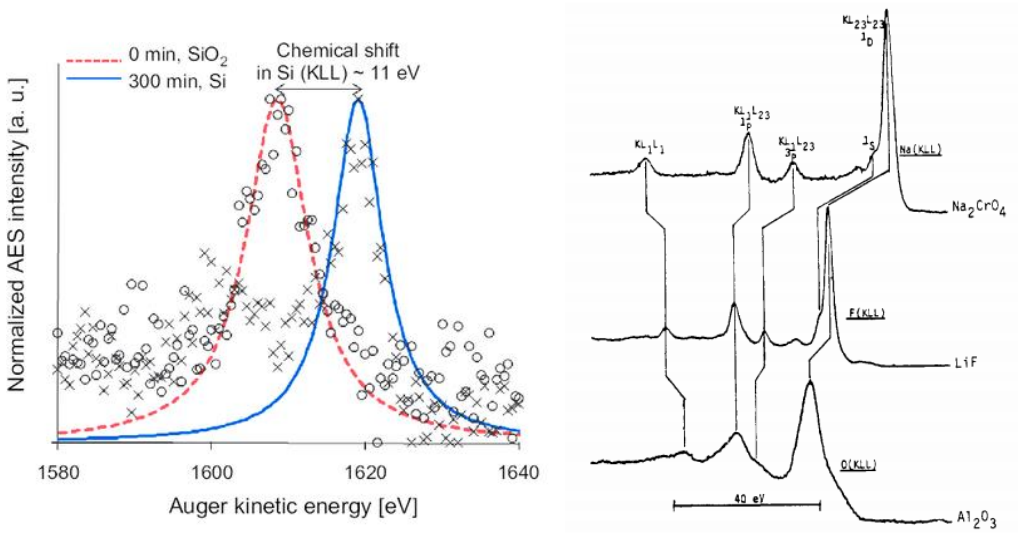

Figure 1.20 Non-smoothed Si AES peaks for silicon oxide (circles) and for elemental Si (crosses) with fitted main components using pseudo-Voigt functions. The comparison of sodium, fluorine, and oxygen KLL Auger Lines. (Reproduced from [35, 36])

1.7 Overview of the Transparent Electronics

As the Internet of Things is rapidly developing and gradually promoting the evolution of everyone's lifestyle, people are interacting with the surrounding and manipulating the information in real time, which enables the potential opportunities of the transparent electronics and the systems on glasses, beyond the conventional Si-based electronics. The transparent electronics require the electronic devices to be see-through, or convert the conventional opaque electronic systems to be translucent, such as transparent displays, transparent solar cell panels, and smart windows.[38-42] In this thesis, we are dabbling into the transparent electronic devices, including the transparent organic transistors and transparent memristors, based on the ultrathin metal-film electrodes and the corresponding optical optimizations. In the following, a few works from the reported literatures are described to show the state-of-the-art technologies for transparent electronics.

The transparent solar cell devices with angle insensitive transmissive colors were developed in our group, as shown in Figure 1.21. The cathode and anode contacts are employing various metal oxide and organic hybrid interlayer stacks, with the optimized optical management. The intrinsic a-Si were used here as the active layer for the photo

carriers generation, meanwhile the great angle tolerance of the transmitted color is due to the negligible optical phase associated with light propagation in a-Si layers. All of the blue, green or red solar cell panels, the a-Si layer is much thinner than the typical charge diffusion length, so most photogenerated carriers are extracted to the electrodes. This work provides the solutions to realize energy harvesting colored solar cell panels for the exterior decorations.[43]

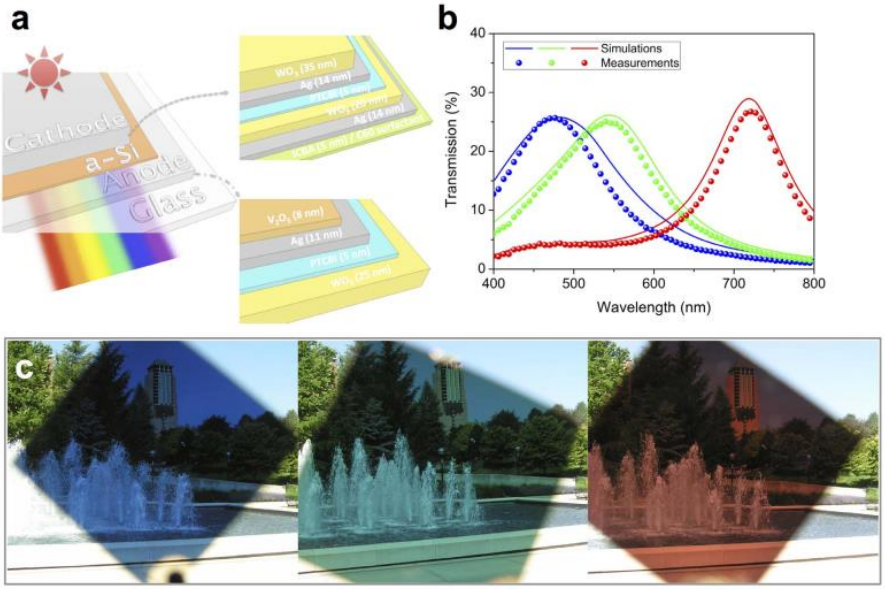

Figure 1.21 Device structure and optical property. (a) A schematic diagram of proposed structure. The cathode is composed of dielectric-metal-dielectric (DMD) and organic layers, and only DMD structure for the anode. The ultra-thin a-Si layer thickness is 6, 11, and 31 nm for blue, green, and red, respectively. (b) Calculated and measured transmission spectra of individual colors (blue, green, and red) at normal incidence. (c) Photographs of distinct blue, green, and red colors by the fabricated devices. (Reproduced from [43])

Organic Solar Cells are important emerging solar cell technologies for the customer electronic products due to the light and potential flexible profile, and it can also be modified for the transparent profile. As shown in Figure 1.22, Prof. Forrest group achieved the semitransparent solar cells based on the non-fullerene acceptor. The key step for the overall transparency lies in the top electrode, since the bottom electrode and other interlayers are basically transparent. Here, they used ultra-thin Ag films as the top anode. It has a higher transmission at the shorter wavelength band, giving it a slightly bluish tint.[44]

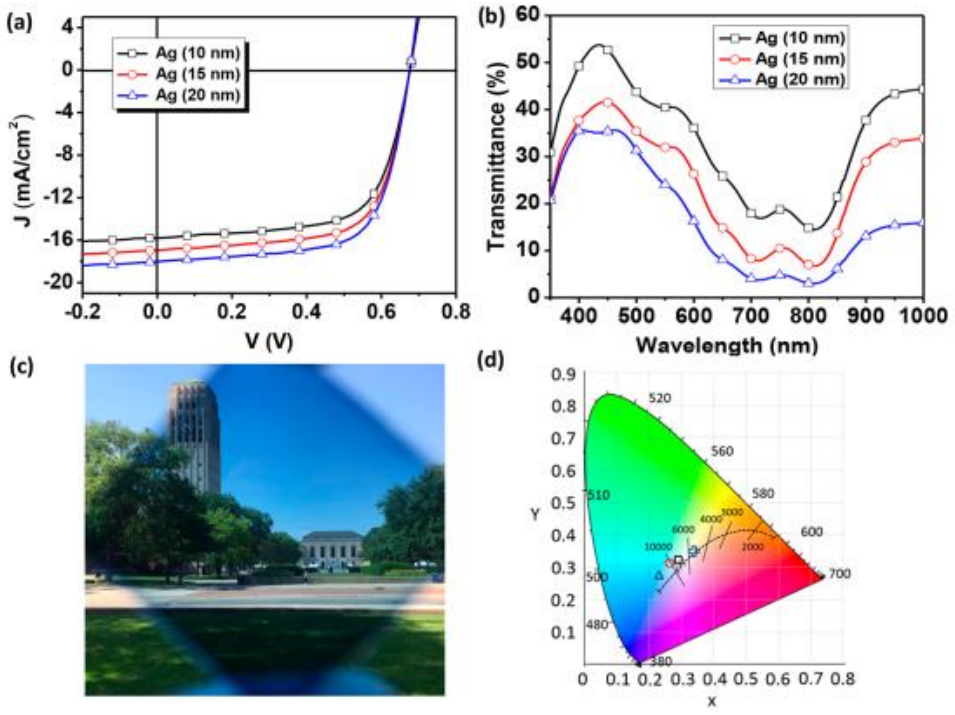

Figure 1.22 a) IV characterizations for the semitransparent solar cell devices with different Ag electrode thicknesses. b), Transmission spectra of the corresponding devices. c), out door image through the semitransparent device with 10 nm Ag. d), the CIE coordinates of the transmission spectra of the devices with different Ag thicknesses, under AM 1.5G illumination. (Reproduced from [44])

Besides the colored solar cell panels, people explored more on the colorless transparent solar cell panels, as shown in Figure 1.23. The authors developed fully invisible solar cells by selectively absorbing ultraviolet and near infrared light, which allows the surfaces in our daily life surroundings to be tuned into solar harvesting arrays without the sacrifice of the functions or aesthetics. The light in ultraviolet and infrared takes over two thirds of the light available for energy harvesting, and the demonstrated transparent solar cell panel achieved the practical efficiencies over 10% with a visible transparency up to 90%. The luminescent solar concentrators are employed for the power conversions in ultraviolet or infrared bands, where the phosphorescent luminophores consisting of hexanuclear metal halide nanoclusters are used for ultra-violet light, and the organic salt derivatives are used for near infrared light.[45, 46]

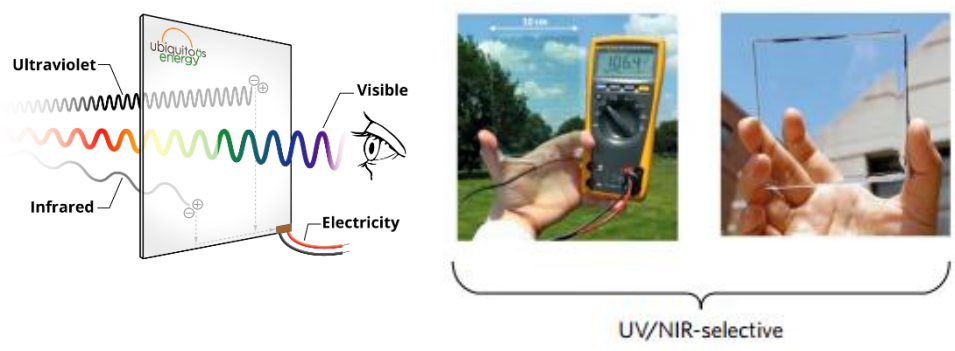

Figure 1.23 Working principle of the commercialized visible transparent solar cell panels. Diagram of a wavelength-selective TPV and a large-area, wavelength-selective TPV module. Diagram of a wavelength-selective LSC and a wavelength-selective LSC module. (Reproduced from [46])

Transparent solar cells panels are used for the energy harvesting at any surface in the daily life surroundings. On the other hand, the transparent display panels embedded with the ambient environments will give rise to further information interactions between human and surroundings, such as augmented reality, smart surgical glasses or smart windows, which enables transparent light emitting devices to be the hot topic in the transparent displays.[47] As shown in Figure 1.24, Prof. Dae-Hyeong Kim group utilized the Quantom Dot light emitting devices to realize the transparent display devices. Both of the bottom and top electrodes are ITO, and the PEDOT:PSS/TFB and ZnO are used as the HTL and ETL, respectively. The ultrathin nature of Tr-QLEDs allows the conformal integration, and the high resolution patterning of red, green, and blue (513 pixels in.−1) shows the potential of the full-color transparent display.[48]

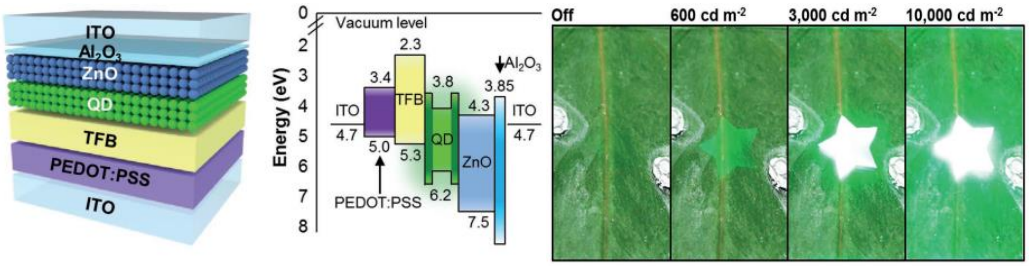

Figure 1.24 Schematic illustration of the device structure and energy-band diagram of the Transparent QLED. The band edges are estimated by ultraviolet photoelectron spectroscopy. Effect of brightness on vividness of the display under ambient light. (Reproduced from [48])

The active matrix is the critical component to drive the light emitting pixels in the flat panel displays, which is actually built up by the thin-film transistors (TFT). Therefore, the Transparent TFTs have attracted great attention to further fulfill the transparent display panels, moreover the unique properties of which are expected to greatly extend the portfolio of modern electronic applications. As shown in Figure 1.25, Prof. Seunghyup Yoo achieved excellent organic transparent TFT device based on the DPh-BTBT and the optical optimization for the source/drain electrodes. In the electrodes, an ultrathin Ag layer (a 15 nm Ag layer in this study) enables efficient lateral conduction, an outer dielectric layer (ZnS) covering the Ag layer enhances the transparency using a destructive interference effect, and an inner dielectric layer (WO_3) provides efficient hole injection into the channel from the Ag electrode.[49]

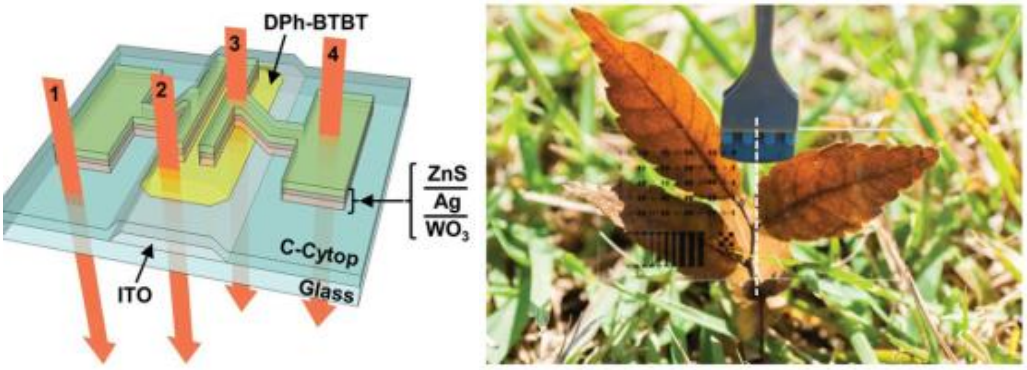

Figure 1.25 Structure of the proposed transparent DPh-BTBT TFTs. The numbers 1–4 indicate four optically distinct positions under consideration. The photograph on the right side shows both conventional and transparent samples (1 in. × 1 in.) containing the full TFT array structure. (Reproduced from [49])

The transparent electronics created more opportunities for the extensive information interactions, but it still requires information storage or processing, which gives rise to the development space for the transparent memristors. As shown in Figure 1.26, Prof. Ram S. Katiyar group developed transparent memristors based on the top graphene electrodes. The main active layer is 15 nm Al_2O_3, deposited by ALD, and the top graphene electrodes are transferred from the Cu/graphene by PMMA coating to the ITO/Al_2O_3, then get etched with the Au hard masks. In the on-state, the IV relationship follows the ohmic conduction, while in the off-state, the nonlinear behavior is

dominated by the interface-limited Schottky charge transportation. The switching mechanisms are due to the O ions or vacancies interaction between oxide and graphene layer. [50]

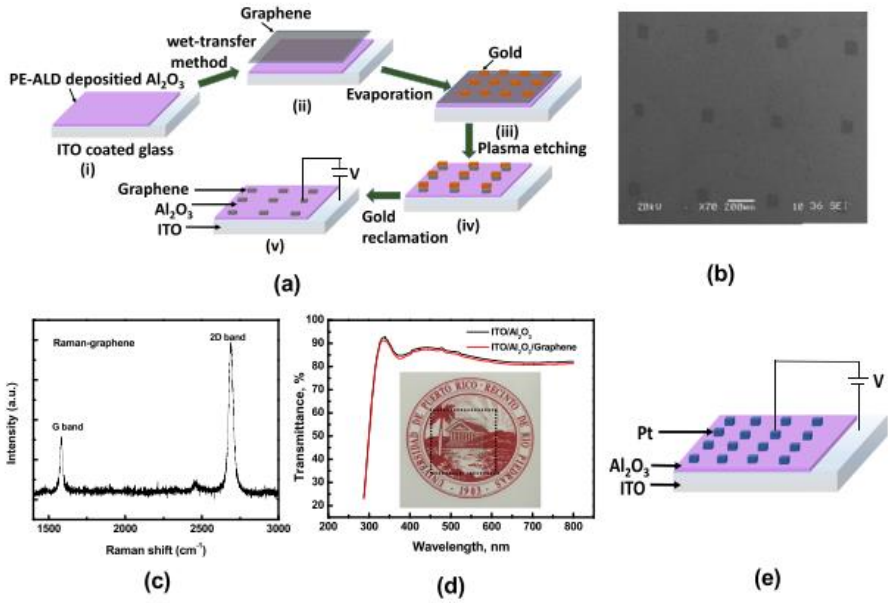

Figure 1.26 (a) Fabrication process of the ITO/Al_2O_3/G device (b) SEM image of graphene square dots on the Al_2O_3 layer. (c) Raman spectra of graphene on Al_2O_3 showing G- and 2D-bands. (d) Optical transmission spectra of ITO/Al_2O_3 and ITO/Al_2O_3/G samples and the inset shows the ITO/Al_2O_3/G sample placed on the university logo. (e) Schematic of ITO/Al_2O_3/Pt capacitor. (Reproduced from [50])

1.8 Dissertation Organization

We further the investigations on the device design and applications of the a-Si devices previously developed in our group. Moreover, we still stepped into the various transparent electronic devices, including the transparent memristors and organic TFTs based on the developed transparent ultrathin metal film electrodes and the corresponding optical management. The organization of the dissertation is described as follows.

In Chapter 2, we reported the surface properties for the Polyethylenimine (PEI) and the adjacent layers. Dipoles will be induced along the ZnO/PEI interface, pointing from ZnO to PEI, which will facilitate the work-function lowering of bottom cathodes. However, for the top cathode contacts in the normal-type devices, we found that the

dipole induced across the PEI layers is highly related to the surface properties of the layers adjacent to it. The obtained results revealed the ZnO/PEI interlayers also work well as top cathode contacts. The reported dipole between ZnO/PEI which is supposed to increase the barrier, is actually overcome by another dipole induced along the interface between the PEI and cathode metals. The fabrication of ZnO/PEI interface is based on solution and low-temperature processes, which gives rise to other promising cathode contact alternatives as top cathode contacts of devices, especially for those with semi-transparency, even flexibility.

In Chapter 3, the interface conductivity and oxygen deficiency for WO_x/a-Si contacts are reported. The ITO transparent electrode extensively used in large-area electronics is becoming more and more expensive, and the metal mesh is a popular backup alternative for the replacement of ITO. However, the local conductivity for the non-conductive area in the metal meshes has to be compensated. In this work, we systematically analyzed the interfacial properties of the WO_x/a-Si interfaces, including the band diagram and the carrier lateral transportation. We found the WO_x/a-Si interface is able to support centimeter-scale non-electrode area, without the additional conductive layers compensating the low local conductivity. The hypothesis and characterizations reported here can be used to determine more details for the exact definition of the device areas and secure better device designs. More significantly, it gives rise to the further possibilities of devices with semi-transparency, ultra-sparse metal mesh electrodes, and so on.

In Chapter 4 and 5, we characterized the photodetectors based on the developed interlayers for a-Si devices, especially the detection under low illumination towards the in-screen fingerprint scanners. In this work, we employed top ZnO NPs and PEI interlayers. High LDR are achieved up to 190 dB, and at least 4 orders for the illuminations < 50 Lux. In order to show the clear current ratio between the adjacent a-Si PD pixels, short linear arrays are fabricated, and the current sequence in the arrays exhibited good ratio up to 2 orders. Finally, peripheral circuits are built up based on the Arduino microcontrollers to fast acquire the current detected by the short linear arrays,

which can clearly show the patterns mimicking the groves and valleys of the fingerprints. The inverted a-Si PD with bottom cathode contact interlayers are developed and characterized to fulfill the requirements of the architecture design for the sensing arrays. The ZnO and MoO_x are employed as the ETL and HTL for the inverted a-Si PDs. The current leakage and LDR get analyzed with different a-Si thicknesses and device areas. The a-Si PD arrays with pixel areas are fabricated based on the photo-lithography processes in order to extract accurate current leakage and LDR. Finally, the optimized a-Si PD arrays are fabricated on the LTPS TFT backplanes.

In Chapter 6, innovative artificial synapses were demonstrated based on the interactions between the a-Si and PEI interlayers. The hysteresis and timing dependent plasticity of the artificial synapses can be excited by light illumination, coupled with electrical pulse stimuli. The device design is promising to serve as fundamental elements for neuromorphic functionalities towards the simultaneous visual information process in large-area electronics or IoT.

In Chapter 7, we achieved transparent resistive switching devices to promote neuromorphic computing for the transparent electronic systems. The devices are based on ultrathin doped Ag films and optically optimized dielectric/metal/dielectric structure. The overall transparency is higher than 80%, and the device conductance modulation is found to be analog and continuous. Under consecutive pulse stimulus with different durations, the device finally stabilized at different conductance levels, acting as different potentiation or depression levels in terms of neuromorphic functionalities.

In Chapter 8, transparent organic TFTs were obtained based on the ultrathin metal film electrodes. In order to achieve higher transparency, the overall pixel aperture ratio need to be further improved, therefore, transparent TFT are demonstrating the potentials to breakthrough the aperture ratio limited by the conventional opaque components in TFTs of the active matrix. In this work, we developed ultrathin Cu-based composite electrodes with Ni seeding and capping layers, which enables better film continuity, conductivity, contact properties and stability. Based on the Ni/Cu/Ni electrodes, the optically optimized transparent Pentacene TFTs with ITO gate and PS-PAN bi-layer

gate insulator exhibited excellent transparency, up to 71.4 % for the source/drain regions and even higher for the overall transparency.

Lastly, in Chapter 9, based on the developed a-Si photodetectors, we proposed the potential development optimizations. The first one is the transparent a-Si optoelectronic devices based on all-inorganic interlayers. Then the optical design can be further conducted to modulate the absorption spectrum of a-Si active layers as well as the exterior apparent colors.

Chapter 2 The Influence of Interfacial Materials on the Dipole Induced in Polyethylenimine Layer of Cathode Contacts

Abstract

Recently, the Znic Oxide (ZnO) and Polyethylenimine (PEI) are extensively used in cathode contacts of the inverted organic light emitting or solar cell devices. Dipoles will be induced along the ZnO/PEI interface, pointing from ZnO to PEI, which will facilitate the work-function lowering of bottom cathodes. However, for the top cathode contacts in the normal-type devices, we found that the dipole induced across the PEI layers is highly related to the surface properties of the layers adjacent to it. The obtained results revealed the ZnO/PEI interlayer also work well as top cathode contacts. The reported dipole between ZnO/PEI which is supposed to increase the barrier, is actually overcome by another dipole induced along the interface between the PEI and cathode metals. The fabrication of ZnO/PEI interface is based on solution and low-temperature processes, which gives rise to other promising cathode contact alternatives as top cathode contacts of devices, especially for those with semi-transparency, even flexibility.

2.1 Introduction

The interfacial materials are very important to the opto-electrical performance enhancement for the organic light emitting or solar cell devices, as well as for organic transistors. In order to improve the charge transportation efficiency, lowering barriers at contacts is a critical point for the interface engineering that leverages all the interlayers. For the anode side, people commonly employ PEDOT:PSS or metal oxides to increase the work function of anodes to make a better band diagram matching

between anode and the LUMO of organic semiconductor or the valance band of inorganic semiconductor[51-53]. On the other hand, for the cathodes, people usually use LiF/Al, $CsCO_3$/Al, or directly use thin low work-function metals, such as Ca, to achieve a better band diagram matching between cathodes and HOMO or conduction band [54-57]. The cathode contact optimization is much more challenging since the interfacial materials used there are usually air-sensitive, which will gradually get deteriorated and result in the irreversible degradation of the devices. Several years ago, people discovered a universal method to produce air-stable low work-function electrodes with Polyethylenimine (PEI). Starting from that point, the compound interlayer ZnO/PEI is becoming more and more popular as cathode interfacial layers for organic opto-electronic devices.[58] Many groups extensively conducted research works and investigations on it, and various methods were used to achieve the ZnO/PEI interlayer, where ZnO interlayer can be prepared directly by sputtering, or by synthesis and spincoating of nano particles.[47, 59-61] PEI was typically diluted in the solutions and spincoated on the ZnO interlayer, or even mixed with the ZnO nanoparticles solutions. In these works, PEI can affectively modulate the work function (WF) of the ZnO interlayer as well as the cathode contacts. The WF lowering effect is mainly due to the interfacial dipoles between the ZnO and PEI, and the molecular dipole of the PEI layer. People commonly claimed that the dipoles come from the protonated amine groups in the PEI layer, and its electrical attraction with anions of ZnO layers.[62, 63] However, very few reports revealed that it is due to the neutral amine groups.[58] Moreover, some studies showed that individual PEI interlayers were also used to lower the WF together with various cathode metals(Ag, Al, Au), and the dipole between the PEI and metal was verified, which is claimed to be due to the charge transfer between PEI and metal surface.[58, 64] At this point, the working principle of the dipole between PEI and ZnO or metal are still necessary to be further investigated.

Here, we would like to report on the investigation for the ZnO/PEI interface based on amorphous silicon (a-Si) solar cells, which will give more information to the further interface engineering. As a classic semiconductor material for large area electronics, a-

Si has been widely used in the active-matrix backplanes for flat panel display technologies, or the solar cells for eco-friendly energy generations.[65-70] Promoted by the dramatic industrial development, the fabrication of the a-Si devices is becoming more and more mature and low-cost. The work we are discussing is also significant to explore more versatility and enhance the opto-electrical performance of a-Si devices.

According to the conventional a-Si solar cell device designs, people usually use p-doped or n-doped a-Si interlayers to obtain better contacts for anodes and cathodes.[71-73]. The doped layers are commonly 10s nm and have similar band gaps with the intrinsic a-Si layers, which means the doped layers will have considerable light absorptions, but produce less photo-generated electrons and holes because of its low electric field to separate the excitons, and the corresponding enhanced recombination on the dopant sites, consuming the photo-generated electrons and holes. Therefore, we employed device structures based on hetero-junctions with vanadium oxide (V_2O_5) and ZnO/PEI interlayers instead of the p-doped or n-doped a-Si interlayers, in order to achieve high optical absorption of the sandwiched intrinsic a-Si layers. Based on the a-Si solar cell devices, we did IV characterizations for various cathode contacts, and obtained the surface characterizations with Auger Electron Spectroscopy (AES) to determine the relationship for surface properties, the induced dipoles and the electrical characterizations. Then we come up with some new understanding for the dipoles induced in ZnO/PEI interlayers.

2.2 Device Structure and Fabrication

As shown in Figure 2.1, the devices are based on the well-developed V_2O_5 anode contacts for a-Si solar cells in our group,[43] where the typical structure is ITO/V_2O_5/a-Si/cathode contacts. At the beginning, we used the ITO substrates (Kaivo Optoelectronic Tech.), which will be thoroughly cleaned by sequential ultrasonic agitations in detergent, DI water, acetone, and isoproponal alcohols, followed by dry blowing with nitrogen gun and 10 min oxygen plasma treatment under 150 °C. Then 8 nm V_2O_5 (purchased from Sigma Aldrich) was deposited in the thermal evaporator

(MBraun) with a rate of 0.3 Å/s under 3.0×10^{-6} mBar. The intrinsic a-Si layers were 60 nm, deposited in the PECVD (PlasmaTherm 790) with a rate of 0.8 Å/s under 260 °C. The Zinc Oxide nanoparticles (ZnO NPs) were synthesized based on the previous report,[60]. The ZnO NPs were finally dispersed in butanol with a concentration of 12 mg/mL, and PEI was dissolved in 2-methoxyethanol (0.2 wt%). The ZnO NPs were spincoated twice at 3000 rpm for 30 s, then immediately annealed at 90 ℃ for 10 min. The PEI layers were spincoated only once with the same procedure with ZnO NPs. The thicknesses of ZnO NPs and PEI layers were 15 nm and 10 nm, respectively. Finally, the 100 nm Aluminum top electrodes were deposited in thermal evaporator with a rate of 0.5 Å/s. In order to scrutinize the functions and interactions for different interlayers, five types of samples were utilized, as shown in Figure 2.2b.

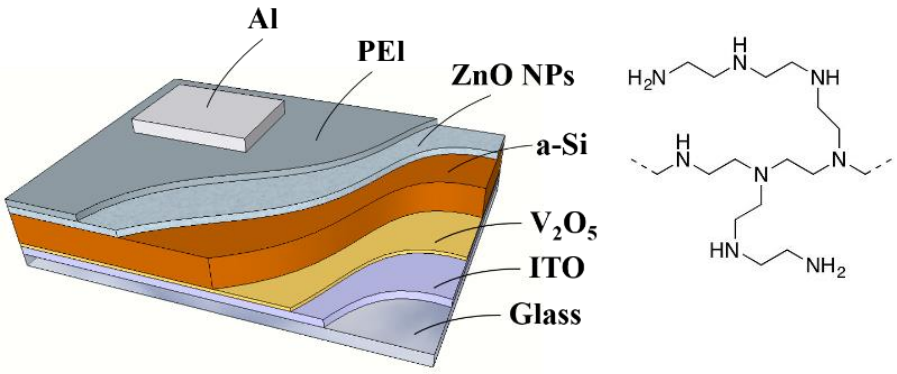

Figure 2.1 The schematic of the devices, which are fabricated based on ITO substrates, deposition of V_2O_5 and a-Si, spin-coating of ZnO NPs and PEI, and the final thermal evaporation of top Al electrodes. The inset is the chemical structure of the PEI interlayer.

2.3 Characterizations for Surface Morphology and IV Behaviors

At the very beginning, the surface morphologies of different stacked layers for the V_2O_5, a-Si, PEI and ZnO NPs were characterized. Figure 2.2-a1 and Figure 2.2-a2 are AFM images for V_2O_5 and V_2O_5 / 60 nm a-Si, respectively. The roughness of V_2O_5 layer is 1.45 nm, which increased a little bit to 1.72 nm after the PECVD deposition of 60 nm a-Si, indicating that the a-Si layer has a very good film uniformity and the 60 nm a-Si cannot fully cover the roughness of the beneath V_2O_5 layer. Figure 2.2-a3 shows the surface morphology of 10 nm PEI spin-coated on a-Si layer, and the

roughness greatly decreased by 0.87 nm and down to 0.85 nm. That is probably due to that PEI is a polymer with good leveling properties, sufficiently covering the roughness of the beneath a-Si layer. Figure 2.2-a4 and Figure 2.2-a5 are the surface morphologies of ZnO NPs on PEI and a-Si layers, respectively. The roughness for PEI / ZnO NPs is 3.45 nm, much higher than the 0.85 nm (for PEI only), which reveals the granule feature of ZnO NPs and also indicates that the inorganic ZnO NPs cannot form sufficient physical contacts on the smooth organic PEI layers. The roughness for a-Si / ZnO NPs is 2.85 nm, increased from 1.72 nm (for a-Si only), showing that a-Si / ZnO basically follows the surface morphology of a-Si and the increased roughness is due to the granule feature of ZnO NPs.

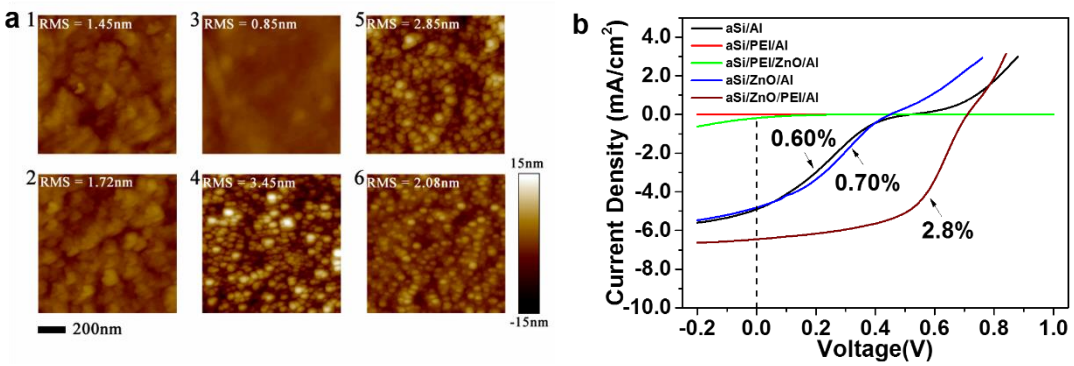

Figure 2.2 (a) The surface morphologies for different stacked interlayers. (a1) and (a2) are 8 nm V_2O_5 (RMS=1.45 nm) and 60 nm a-Si on V_2O_5 (RMS = 1.72 nm). (a3) 10 nm PEI spin-coated on the a-Si layer (RMS = 0.85 nm). (a4) 15 nm ZnO NPs spin-coated on (a3) PEI layer (RMS = 3.45 nm). (a5) 15 nm ZnO NPs spin-coated on the a-Si layer (RMS= 2.85 nm). (a6) 10 nm PEI spin-coated on the ZnO NPs layer (RMS = 2.08 nm). (b) The IV characterizations for different cathode contacts. The highest power conversion efficiency (PCE) comes from the a-Si/ZnO/PEI/Al with 2.8%. The a-Si/Al and a-Si/ZnO/Al have a similar PCE, 0.6% to 0.7%. For the devices with PEI spin-coated directly on a-Si, a-Si/PEI/Al and a-Si/PEI/ZnO/Al, the efficiencies are negligibly small.

The Figure 2.2-a6 shows the surface morphologies of PEI film spin-coated on the ZnO-NPs layers. The roughness is 2.08 nm, decreased from 2.85 nm (for a-Si/ZnO NPs), but much greater than 0.85 nm (for a-Si/PEI), indicating that the PEI layer can well cover the surface of ZnO NPs layers and reduce the roughness by 0.78 nm at the main time. Therefore, the PEI layers can form sufficient physical contacts on the top

surface of ZnO NPs. These surface morphology characterizations verified the significant variations for the different contact interlayers composed of ZnO NPs and PEI, which will provide the evidence to the optimized result and the corresponding mechanism hypothesis discussions.

Table 2.1 The extracted parameters for the different devices

	V_{oc}(V)	J_{sc}(mA/cm^2)	R_s(ohm×cm^2)	FF(%)	PCE(%)
aSi/Al	0.52	4.86	520	23	0.6
aSi/PEI/Al	0.50	7.1×10^{-4}	7.0×10^{6}	8.0	3.0×10^{-5}
aSi/PEI/ZnO/Al	0.50	0.179	3.0×10^{5}	9.0	7.6×10^{-3}
aSi/ZnO/Al	0.44	4.64	150	32	0.7
aSi/ZnO/PEI/Al	0.71	6.43	26	55	2.83

The IV characteristics for different samples were measured under AM 1.5G solar illumination, and the corresponding extracted parameters were listed in the Table 2.1. The results reveal that the PEI interlayers can greatly improve the power conversion efficiency (PCE) under certain conditions. As shown in Figure 2.2b and Table 2.1, the PCE for pure Al cathode is 0.6% and the serial resistance (R_s) is 520 ohm×cm^2, which is due to the large energy barrier between conduction band (CB) of a-Si and WF of Al. The ZnO NPs are often used as cathode interlayers for ITO electrodes to achieve inverted OLED or solar cell devices.[47, 59, 60, 62] While our results show that the ZnO/Al cathode did not give rise to an obvious improvement, compared with pure Al cathode, where its PCE is 0.7% and R_s is 150 ohm×cm^2. The reduced R_s shows the cathode contact for the ZnO/Al cathode is much better than those for pure Al cathode, corresponding to the reduced S-curve effect. However, it did not result in a great PCE improvement. According to the comparison of the WF of Al and CB of ZnO NPs, the almost identical energy level (around 4.2 eV) can form a good contact between ZnO NPs and Al electrodes but cannot lower the energy barrier between CB of a-Si and Al cathode. This also indicates the reason why the source/drain electrode for ZnO thin-film transistors are usually Al.[74-76]

Furthermore, the pure PEI or the ZnO/PEI compound interlayers can provide another possible route to achieve lower barriers for the cathode contacts in a-Si solar cells. Briefly speaking, in the reported results, the PEI interlayers are commonly used for the bottom cathode electrode, where the typical structure is ITO/ZnO/PEI, and the dipole along the PEI surface is pointing from ZnO to PEI, which means the dipole will contribute to decrease the WF of ITO to achieve a lower barrier.[47, 59-61] Therefore, according to the dipole direction and sequence of stacked layers, the devices with PEI/Al and PEI/ZnO/Al cathodes were fabricated to verify whether the conventional PEI interlayer can work for the top cathode contacts. In these devices, the PEI interlayers were directly spin-coated on the a-Si surface, then spincoating of the ZnO NPs solution and deposition of Al layers. As shown in Figure 2.2b and Table 2.1, these devices did not show noticeable PCEs, and the serial resistances are infinitely large. The only difference is that the PEI/ZnO/Al cathode have slightly noticeable IV behaviors of solar cells, corresponding to a little lower R_s, which means the electrical dipole between PEI and ZnO NPs may exist and produce a little lower barrier than the device with PEI/Al cathode. However, the two types of devices did not form a sufficient low barrier, compared to pure Al and ZnO/Al cathodes discussed above. Moreover, considering PEI as a polymer insulator and taking the possibility of tunneling into account, the possible dipoles in PEI interlayers were not that large to produce a sufficient charge tunneling through it. The limited dipole moment in PEI layer in PEI/ZnO/Al cathode can be attributed to the granule feature of the ZnO NPs, which cannot form sufficient and uniform contacts on PEI surface, as shown in Figure 2.2a. Therefore, the PEI/ZnO/Al cathode is supposed to work much better than pure Al or ZnO/Al, but it failed to obtain the expected PCE.

Finally, we decided to give a shot to the a-Si/ZnO/PEI/Al, which is supposed to increase the energy barrier between the CB of a-Si and WF of Al because of the dipole direction between the ZnO NPs and PEI layers. However, the results show a much better performance, far beyond other cathode candidates in this work, where the PCE is

around 2.8 % and R_s is around 26 ohm×cm^2, corresponding to the unnoticeable S-curve effect.

According to the reported results for the interaction between ZnO and PEI layers in OLED or OPVs, the dipole direction is pointing from ZnO to PEI, and the WF of ZnO layers will be reduced, equivalently the WF of PEI will be increased. Based on this theoretical analysis, the devices with ZnO/PEI/Al top cathode are not supposed to work because of the greatly increased barriers for the cathode contacts, as shown in Figure 2.3-a1. Actually, the obtained results is much better than the expected, revealing that the corresponding barrier for the cathode contacts is lowered and the overall dipole direction should be pointing from PEI to ZnO, as shown in Figure 2.3-a2. The theoretical analysis seems to be contradictive to the obtained results, therefore it is definitely significant to find a hypothesis to accommodate these solid experimental results.

2.4 Further Analysis for the Dipole Induced in PEI Interlayers

As we known, the PEI behaves like a base in aqueous solutions, because it has property of strong affinity for protons owing to a great number of nitrogen atoms in amino groups. There is strong electrostatic interaction between the protonated amino groups and particles charged negatively.[60, 63] As we known, the ZnO is a typical ionic crystals, correspondingly there is a huge density of oxygen ions (O^{2-}) on the surface.[77] Therefore, the protonated amino groups will be strongly adsorped on the ZnO surfaces during the spincoating of PEI solutions, resulting in a higher density of protonated amino groups on the ZnO/PEI interface, compared to the a-Si/SiO_x/PEI/Al interface. Moreover, charge transfer is supposed to occur across the PEI/metal interfaces, resulting in a negatively charged layer along PEI/Al interfaces, as schematically illustrated in Figure 2.3-b1.[58, 64] Finally, there are two dipoles across the bottom and upper surface of PEI interlayers in ZnO/PEI/Al. The first one is based on the positively charged protonated amino groups and negatively charged O^{2-} groups across the ZnO/PEI interface, with very short interaction distance. The other one is

based on positively charged protonated amino groups along ZnO/PEI interface and the negatively charged groups along the PEI/Al interface, with a much longer interaction distance. The dipole moment depends on the product of the involved charge quantity and the corresponding interaction distance, as shown in the inset equation of Figure 2.3.

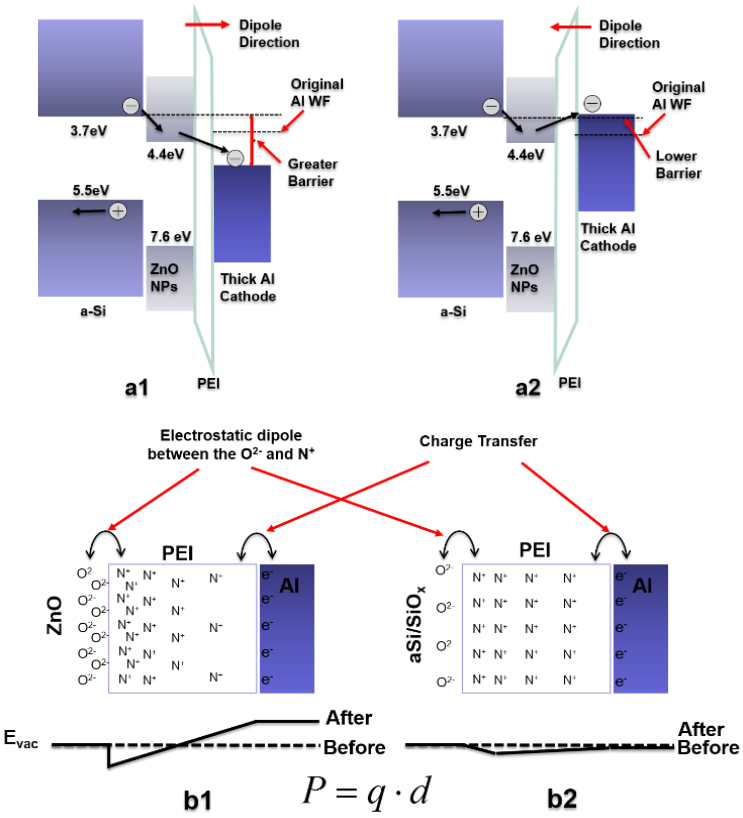

Figure 2.3 (a)The theoretical energy level diagram (a1) based on the reported results between ZnO NPs and PEI spin-coated on it, and the resulting greater barrier for the cathode contacts, (a2) the proposed diagram showing the optimized performance based on a-Si/ZnO NPs/PEI/Al contacts, and the resulting lowered barrier. (b) The distribution of the protonated amino groups in PEI interlayer and the electrons transferred to electrode metal surface, the induced dipole and the corresponding vacuum energy level for (b1) ZnO/PEI/Al and (b2) a-Si/SiO_x/PEI/Al, where SiO_x is the nature oxide layer on the a-Si surface. The equation is shown for the definition of the dipole moment, where P is the dipole moment, q is the charge quantity involved in the dipole, and d is the charge separation distance.

Assuming the charge amount involved in the two dipoles is comparable because the positive charged groups are mainly the protonated amino groups, then for a-

Si/ZnO/PEI/Al contacts the dipole with a longer interaction distance overcome the one with a shorter interaction distance. Therefore, the dipole between PEI/Al is dominant, inducing a great level shift and WF lowering for the Al cathode, as shown in the vacuum energy level (E_{vac}) of Figure 2.3-b1.

Moreover, we also have to consider the physical contact features between ZnO NPs and PEI interlayers. According to the surface morphology analysis, the roughness for ZnO/PEI is 2.08 nm, lower than the 2.85 nm (for a-Si/ZnO), indicating PEI can well follow the ZnO NPs surfaces resulting in a good face-to-face contacts and the sufficient electrostatic interactions between O^{2-} on the surface of ZnO NPs and the protonated amino groups along the ZnO/PEI interface. On the contrary, the roughness for PEI/ZnO is 3.45 nm, much higher than the 0.85 nm (for PEI only), indicating PEI/ZnO is kind of the face-to-point contact, which cannot form a sufficiently large dipole across them because of less involved charge quantity.

As shown in Figure 2.2, the electrical performance for ZnO/PEI/Al is quite different from the a-Si/PEI/Al, which can be due to the unique surface properties of ZnO and a-Si. Different from ZnO, it is inevitable to generate ultrathin nature silicon oxide layers on the top a-Si surface, where the silicon and oxygen atoms are connected together by covalent Si-O-Si bonds, which means the silicon oxides are covalent compounds.[78] Thus, the density of negatively charged (O^{2-}) on the a-Si/SiO_x surface is much lower than that of ZnO NPs, which will be demonstrated by the AES analysis later. Therefore the protonated amino groups would not be able to strongly adsorp on the a-Si/SiO_x surface, resulting in a more uniform distribution of protonated amino groups across the PEI layers, as shown in Figure 2.3-b2. The dipole moment across SiO_x/PEI layers is becoming much smaller than that across ZnO/PEI layers because a less charge quantity involved. The dipole across PEI/Al layers is also becoming much smaller because of the overall shorter interaction distance. There is not a dominant dipole, and the two dipoles will counteract with each other, resulting in a smaller level shift and a smaller WF lowering for the Al cathode, as shown in Figure 2.3-b2. Moreover, considering the limited charge tunneling through the 10 nm PEI layer under the small net dipole, the

efficiency for a-Si/SiO_x/PEI/Al will be further degraded, thus down to an unnoticeable value as we obtained.

2.5 Surface Analysis by AES and IV Curves for Other Cathodes

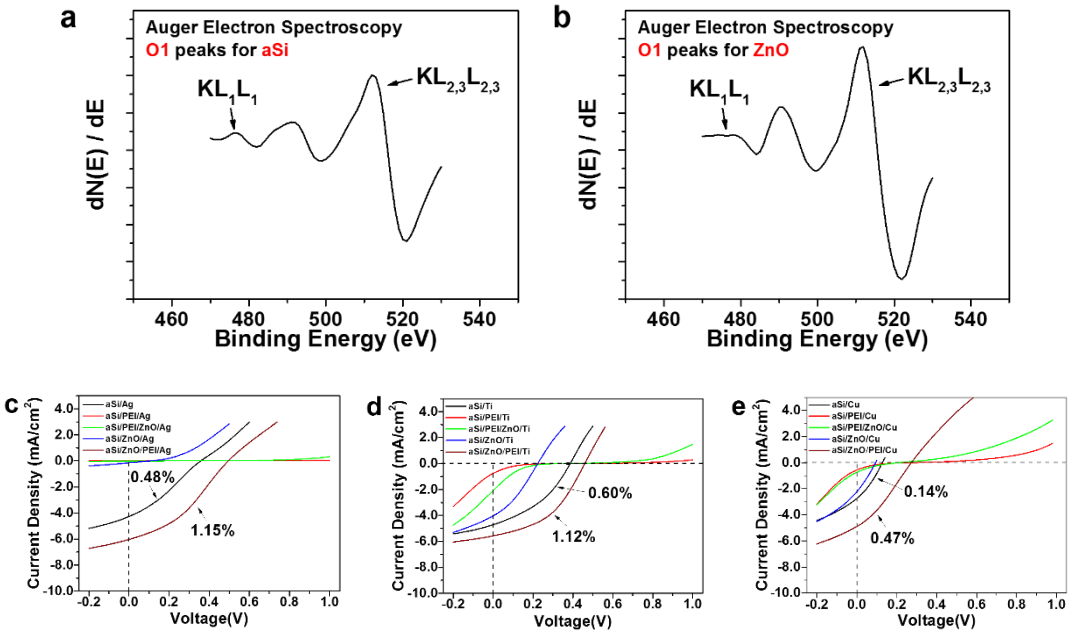

Figure 2.4 Auger Electron Spectroscopy (AES) characterizations for the O atom chemical state on the surface of a-Si (a) and ZnO NPs (b). The IV characterizations for devices based on ZnO/PEI interlayers, but with Ag (c), Ti (d), Cu (e) cathode metals. The highest efficiency was obtained in the a-Si/ZnO/PEI/(Ag, Ti, Cu)with 1.15%, 1.12%, 0.47%, respectively. They are much higher than those for a-Si/PEI/(Ag, Ti, Cu) or a-Si/PEI/ZnO/(Ag, Ti, Cu).

As we discussed above, the overall dipole for the cathode contacts, ZnO/PEI/Al greatly depends on the negatively charged groups, especially O^{2-} ions, along the interface beneath the PEI layer. Auger Electron Spectroscopy (AES) surface analysis was conducted to verify the chemical state and density for the O atoms on on the surface of ZnO NPs or a-Si. As shown in Figure 2.4a and Figure 2.4b, the distinctive O1 peak group were acquired, which includes three peaks corresponding to the KL_1L_1, $KL_1L_{2,3}$ and $KL_{2,3}L_{2,3}$ transitions. The intensity ratios depends on the atomic charges of the L_1 and $L_{2,3}$ orbitals localized at the oxygen sites, and the atomic charges are determined by the chemical bonding of the oxygen to other elements.[35-37] The atom number of

O is 8, and there are 8 electrons localized in the K and L shells, where 2 in K, 2 in L_1, 2 in L_2 and 2 in L_3. For the ionic oxide crystals, another 2 electrons from cations will fill the remaining 2 empty orbitals in L_3 subshell and form O^{2-} ions, thus more electrons will be involved in the Auger transitions and the probability of transition $KL_{2,3}L_{2,3}$ will become higher. On the contrary, the 2 electrons in L_3 subshell will be shared with other elements in the covalent oxide compound materials, thus the probability of transition $KL_{2,3}L_{2,3}$ will be reduced. Therefore, if the oxide material is more ionic, the intensity ratio between $KL_{2,3}L_{2,3}$ and KL_1L_1 will be higher.[37] As shown in Figure 2.4a and Figure 2.4b, the intensity ratio for ZnO is much higher than that for the SiO_x on the surface of a-Si, which means the chemical state of the O atoms in ZnO NPs is more ionic than the O atoms in the surface SiO_x. Moreover, the intensity is also proportional to the atom concentration, therefore, the O^{2-} density in ZnO NPs is also much higher. The AES analysis corresponds to the previous IV characterizations and hypothesis for the interface dipoles and barriers.

Aside from the bottom interface of the PEI to ZnO, the interface between PEI and the top cathode metal also plays an important role in the formation of the overall dipole. The devices based on ZnO/PEI interlayers, but with different cathode metal (Ag, Ti, Cu), were fabricated as well, as shown in Figure 2.4(c-e). These devices with the ZnO/PEI/metal contacts facilitate to achieve the best PCE, exhibiting similar results with the Al cathode, where 1.15% for Ag, 1.12% for Ti, and 0.48% for Cu. It verifies that the charge transferring commonly exists along the interface between PEI and metal, and induces an additional dipole, besides the one along the ZnO/PEI interface.[58, 64] Considering the different WF for pure Ag, Ti and Cu, as well as the possible fermi pinning effect when depositing the metal on PEI layer, the optimized PCE is quite different, but much lower than that for Al cathode.

2.6 Conclusion

In this work, we further investigated the dipole induced along the interface between to PEI and the adjacent ZnO or metal layers, based on amorphous silicon solar cells.

We found the dipole induced in the solution-processed PEI is highly related to the surface properties of the interlayers beneath it. The popular ZnO/PEI contacts was usually used to achieve lower contact barrier at the bottom cathodes, because of the dipole pointing from ZnO to PEI. In this work, we found the same structure also work well as top cathode contacts (ITO/V_2O_5/a-Si/ZnO/PEI/cathode metal). Although the reported dipole between ZnO/PEI is supposed to increase the barrier, which is actually overcome by another dipole induced across the PEI/metal interlayer. The proposed mechanisms will provide additional evidence for the interface engineering related to PEI, and also introduce other possible options for the cathode contacts on top side of the devices, especially for the devices with semi-transparency, even flexibility, because of the solution and low-temperature processes used for ZnO NPs and PEI interlayers.

Chapter 3 Interfacial Modulation of Metal Oxide Enabling Centimeter Scale non-Electrode Area for Solar Cell Devices

Abstract

Large-area electronics are drawing the attentions extensively from industry and academia, demonstrating its compelling forms for a large range of realization scenarios. The ITO transparent electrode extensively used in large-area electronics is becoming more and more expensive, and the metal mesh is a popular backup alternative for the replacement of ITO. However, the local conductivity for the non-conductive area in the metal meshes has to be compensated. In this work, we systematically analyzed the interfacial properties of the WO_x/a-Si interfaces, including the band diagram and the carrier lateral transportation. We found the WO_x/a-Si interface is able to to support centimeter-scale non-electrode area, without the additional conductive layers to compensate the local conductivity. The hypothesis and characterizations reported here can be used to determine more details for the exact definition of the device areas and secure better device designs. More significantly, it gives rise to the further possibilities of devices with semi-transparency, ultra-sparse metal mesh electrodes, and so on.

3.1 Introduction

Large-area electronics are drawing the attentions extensively from industry and academia, demonstrating its compelling forms for a large range of application scenarios outside those employing the conventional monocrystalline Si and III-V semiconductors.[79-84] Solar cell and organic light emitting devices (OLED) are the critical and basic components for applications integrated with energy harvesting and

information displaying, meanwhile many new materials, fabrication processes and device structure are being developed, extending the application boundary of the optoelectronic devices.[18, 85-91] Transparent electrodes are required for the two types of devices, to promote the interactions between the active layer in the devices and external environments. For Solar Cell devices, light beams have to go through the transparent electrode and excite the photo-generated electron-hole pairs in the active layer, and the transparent electrodes is used to collect the photo-generated carriers and build up the power source for the external loads. For the OLED devices, the excitons generated in the active layer will produce photons through radiative recombination, which go through the transparent electrodes and show light illumination to external environments. Indium Tin Oxide (ITO) is the most widely used transparent electrode, because of its excellent transparency, conductivity and stability. However, the storage of indium in earth is becoming more and more limited, inevitably increasing cost and constrains for the further mass production of the opto-electronic devices, including the Solar Cells and OLEDs. In recent decades, people showed wide and demanding needs for the potential alternative materials of ITO, therefore many various transparent electrodes candidates have been developed, including other cost-efficient conductive oxides, ultra-thin metal films, carbon-based electrodes, metal mesh and so on.[47, 92-98] Among them, the metal mesh is a popular backup alternative, due to its easy fabrication, including nano-imprinting, electroplating, photo-lithography, even solution-coating of nanowires.[96-102] Theoretically speaking, however, the metal mash is not that satisfactory for Solar Cells and OLEDs, because of the large non-conductive area between the conductive pathways, which could dramatically increase the contact resistance and reduce the carrier collection or injection efficiency. As a result, the local conductivity for the non-conductive area has to be compensated. Conductive polymer, such as PEDOT:PSS, was usually used to be coated on the metal meshes for this purpose.[103-106]

In Solar Cells and OLEDs, carrier collection or injection needs to sequentially go through various interlayers, and the corresponding carrier transportation direction is

perpendicular to the interlayers, which can be called as vertical transportation. On the other hand, in another class of (opto-) electronics devices, Field Effect Transistors (FETs), are employing the lateral transportation, because the carriers are mainly going along the channel interlayer, and the interface properties between channel material and gate insulator will greatly influence on the overall electrical performance in terms of mobility, on-off ratio, or subthreshold swing.[107-110] Meanwhile, we also found the on-off ratio of Pentacene FETs will greatly reduced after blanket deposition of the source/drain contact interlayer MoO_x, and the most possible reason is that the lateral conductivity along the interface between MoO_x and channel material Pentacene was increased. This can be considered as the creating of a secondary channel, which is not controlled by gate field.

As we see, the device with vertical transportation are essentially composed by the sequentially stacking of different interlayers, which creates a large room to investigate the lateral interfacial properties, but people unfortunately paid much less attention or efforts to it. Forrest group reported quite meaningful and interesting findings about the centimeter-scale electron diffusion in photoactive organic hetero-structures, because of the blocking electrons in a certain interlayer and the corresponding reduced recombination.[111]

In this work, we stepped a little further and are going to report on our findings about the interfacial conductivity for a certain interface in solar cell devices, which can enable centimeter-scale non-electrode area. We investigated the interface between the tungsten oxide (WO_x) and amorphous (a-Si), and measured the opto-electrical performance for the corresponding a-Si solar cell devices, incorporating ultra-sparse ITO or metal meshes. The results for the lateral interfacial conductivity motivate people to determine more details for the exact definition of the device areas and secure better device designs. Meanwhile, it gives rise to the further possibilities of devices with semi-transparency, ultra-sparse metal mesh electrodes, and so on.

3.2 Device Structure and Fabrication

The basic device structure is shown in Figure 3.1, where ITO coating glass pieces were used as substrates and the bottom anode, patterned by photo-lithography and followed by etching in hydrochloric acid for 4 min. We also prepared W or Ni meshes as the bottom anode for the further demonstrations. Next step is the preparation for the HTL, WO_x, formed by oxidation from ultrathin W film (8-10 nm) deposited by sputtering. The 60 nm a-Si layer was used as the active layer, deposited by PECVD PlasmaTherm 790 with a rate of 0.8 Å/s under 260 °C. Top cathode interlayers were fabricated by spin-coating of ZnO nanoparticles and PEI solutions, followed by the annealing under 100 °C for 10 min in air. The final top electrode is Al, deposited by thermal evaporation and shadow masks with the window area of 1.0 × 1.4 mm.

The period of the ITO meshes is 420 × 420 um, and the corresponding etching area (ITO-free area) increases from 100 × 100 um to 410 × 410 um. We define the window ratio as the percentage of the ITO-free area to one ITO period, for example, 5.67% for 100 × 100 um (100×100 / 420×420 = 5.67%).

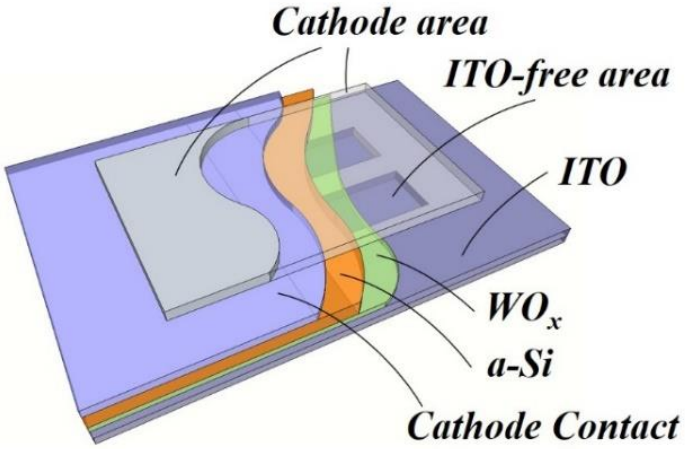

Figure 3.1 The schematic illustration of the a-Si solar cell device structure. ITO glass pieces were employed as substrate and anode, WO_x as HTL, 60 nm a-Si as active layer, then cathode interlayers and cathode metals.

3.3 The a-Si Solar Cell Devices with Different ITO Window Ratios

The top view images and the corresponding window ratios were shown in Figure 3.2a, where the ITO windows are square with different edges and the top electrodes were fully covered by the bottom ITO mesh areas. The corresponding IV characterizations were summarized in Figure 3.2b, where the the Photo-Conversion Efficiency (PCE) remains around 3.5 % for the 60-nm a-Si, which is not that high because the thickness we were using is much less than that for the regular a-Si photovoltaic devices.

It is necessary to point out that the large range of the window ratio does not change the PCE and the related parameters a lot, which reveals that some additional lateral carrier conduction pathways exist in the neat WO_x regions, maintaining the original transportation efficiency for the carrier injection and collections.

More detailed parameters for different ITO windows are extracted and summarized in Figure 3.2(c,d). As the window ratio increases, the open circuit voltage (V_{oc}) decreases from 0.60 V to 0.51 V, probably due to the reduced overall work-function of anode covering the neat WO_x areas and ITO/WO_x areas. The workfunction (WF) of anode needs to be as close to the valance band of a-Si as possible in order to maximize the collection efficiency of photo-generated holes and the corresponding PCE. The V_{oc} is the voltage bias used to maintain the balanced counteract for the carrier injection into a-Si and photo-generated carrier collection at the anodes/cathodes. The bottom ITO anode is composed of the ITO/WO_x regions and neat WO_x regions, and the WF of the anode is the overall WF for the two regions. The reduced V_{oc} indicates the reduced overall WF, and the higher WF for ITO/WO_x than that for WO_x. The short current density (J_{sc}) increased from 11.2 to 13.2 mA/cm^2, which is roughly proportional to the light absorption of a-Si layers, due to the the increased overall transparency of ITO mesh and the modulated cavity effect. As shown in Figure 3.2f, the light absorption from 450 to 600 nm for the devices without ITO electrodes was much higher than those with ITO electrodes, and slightly higher absorption was also obtained for the wavelength from 650 to 750 nm.

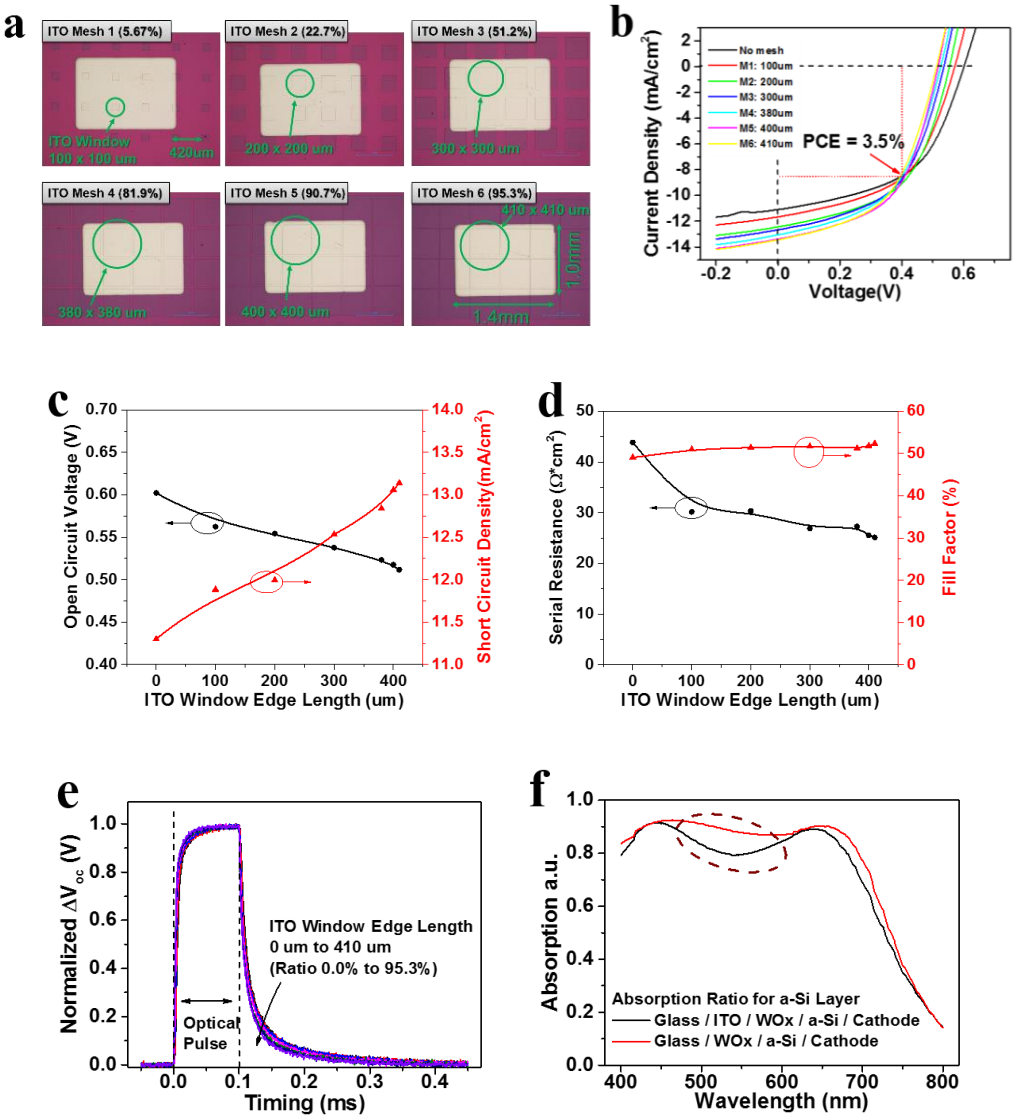

Figure 3.2 The top view of a-Si solar cells with different window ratios and the corresponding electrical characterizations. (a) The top view images of the a-Si solar cells, the ITO window edge increases from 100 um to 410 um, and corresponding window ratio increases from 5.67% to 95.3%. (b) IV characterizations for these a-Si solar cells, where the Photo-Conversion Efficiency (PCE) remains around 3.5 % for the 60-nm a-Si. (c, d) The dependence of open circuit voltage, short current density, serial resistance and fill factor on the ITO window edge. (e) The normalized transient photo-voltage response under 0.1 ms optical pulses and different ITO window ratio for the further diffusion length extractions, where the rise decay time constant was calculated based on the stretched exponential function. (f) The calculated light absorption of the a-Si active layers in the solar cell device with or without ITO electrodes.

Moreover, the fill factor (FF) was well maintained at a constant value of around 50%, which is because of the overall balance between the decreased V_{oc} and increased J_{sc}, as shown in the Figure 3.2d. The dependence of the serial resistance (R_s) on the window ratio was also obtained, which decreases from 43 to 26 ohm×cm^2. At the anode contacts, the electrons will be injected from ITO into the WO_x layer and transported to the WO_x/a-Si interface, where the electrons get recombined with the photogenerated holes, which is equivalent to collect the photo-generated holes at the ITO anode, as shown in the Figure 3.3a. The reduced R_s is probably due to the schottky barrier lowering by charge imaging effect and the confinement of the carriers in the separated interlayers, which will be discussed in details later.

The diffusion and transient response for the photo-generated carriers in the a-Si active layers were characterized, as shown in Figure 3.3e. The Transient Photo Voltage (TPV) responses were recorded under 0.1 ms optical pulses for different ITO window ratios. As we see, the exponential decays are almost identical to each other and the extracted diffusion lengths are around 90 nm, comparable to the reported typical diffusion length for a-Si.[112] The diffusion length is much smaller than the dimension of the ITO window edge, indicating the photo-generated holes were collected or recombined locally along the WO_x/a-Si interface, rather than at the ITO meshes after transporting through the ITO-free regions. Moreover, the exponential TPV response is a little faster for the higher window ratio, which coincides with the reduced R_s and the slightly lower corresponding time constant. The comprehensive understanding of the reduced R_s and the corresponding faster TPV response will be related to the further lateral conductivity measurement and the interface characterizations.

3.4 Investigation on the Interfacial Properties of WO_x/a-Si

As shown in the Figure 3.3a, the anode contacts are composed of ITO anode, WO_x interlayer, then a-Si active layer by PECVD deposition on WO_x. The electrons will be injected from ITO into the WO_x layer and get recombined with the photogenerated holes at the WO_x/a-Si interface. WO_x is well known for its non-stoichiometric

properties, as the lattice can withstand a considerable number of oxygen vacancies (V_{ox}). The existence of V_{ox} behaves like donors and contribute the mid-gap energy levels, resulting in the narrow conduction band near 4.4 to 4.6 eV.[113] The typical WF of ITO is around 4.7 to 5.0 eV, therefore the contact between ITO and WO_x is not perfectly ohmic. The barrier for the electron injection through this interface can be lowered due to the charge imaging effect, which could be the main reason for the reduced R_s as ITO window ratio increases. The higher ratio means narrow ITO meshes and increased density of the injection current, therefore the barrier for the ITO/WO_x regions will be further reduced since the barrier lowering monotonically depends on the charge involved.

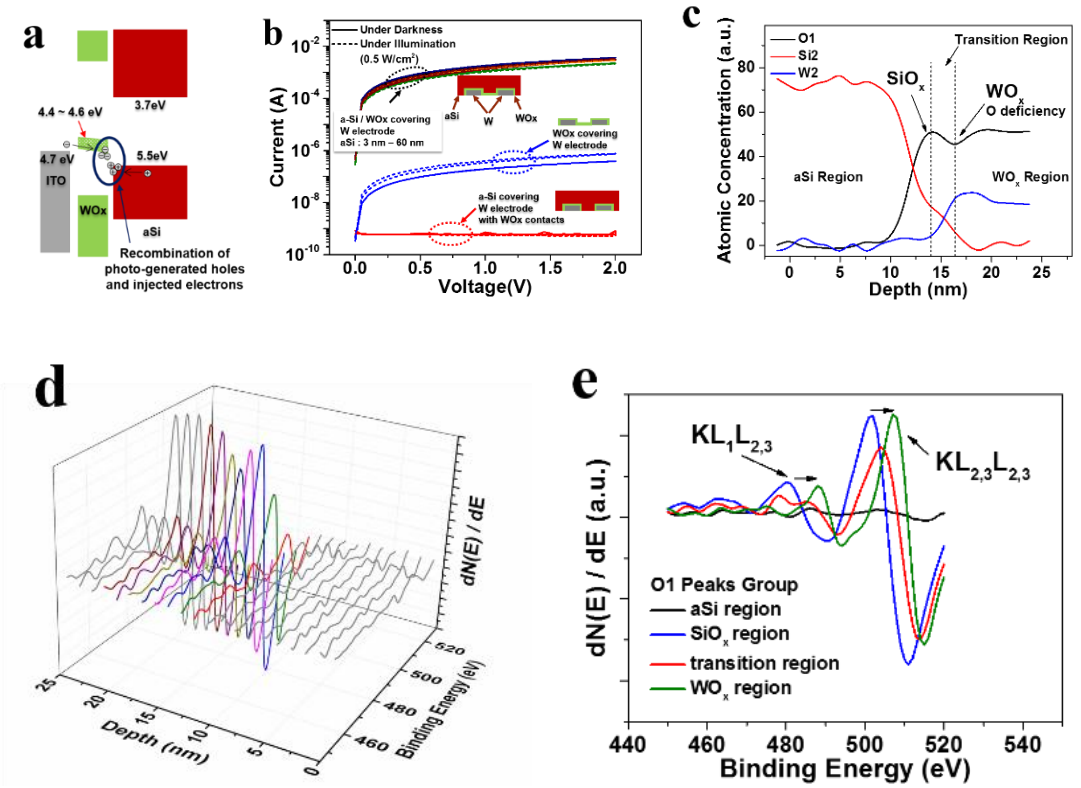

Figure 3.3 (a) The schematic illustration of the band diagram for the anode contacts. (b) The lateral conductivity measurement for the WO_x/a-Si interfaces, including the IV sweeps for different WO_x and a-Si contacts, w. / w.o. light illumination of 0.5 W/cm^2, including the a-Si with separated WO_x contacts, neat blanket WO_x, and stacked blanket WO_x and a-Si. (c) Atomic concentration depth profile obtained by the Auger Electron Spectroscopy (AES). (d) AES O1 peak groups profile for O atoms along WO_x/a-Si interface. (e) The detailed comparison of O1 peak groups for the transition region from the top a-Si layer to the bottom WO_x layer.

As discussed above, the well maintained efficiency for the carrier injection and collections will be highly related to the lateral interfacial properties of WO_x/a-Si. As shown in Figure 3.3b, the lateral conductivity of WO_x/a-Si interface were measured in details for different thicknesses of the top a-Si layer on WO_x, based on the interdigitated electrode configuration with a channel length and width of 50 um and 1200 um, respectively. The WO_x interlayer used here is either oxidized directly from the surface to W electrodes, or from the blanket ultrathin (8-12 nm) W films covering the W electrode areas. Finally, the a-Si layer is deposited on the whole sample, covering the W electrode areas, as shown in the inset images of Figure 3.3b. Firstly, control samples of a-Si layer on W electrodes with separated WO_x contacts were prepared, and the measured resistance is around 1.0×10^{10} Ω either under darkness or illumination (0.5 W/cm^2). The a-Si layer behaves like insulators because of the low carrier concentrations under darkness, meanwhile the photo-generated carriers cannot be transported to the W electrodes because of the limited mobility and diffusion length. Then, the samples with blanket WO_x covering W electrodes were prepared. The measured resistance is around 6.67×10^6 Ω under darkness, and decreased a little bit under illumination, probably because the photons in the light illumination excite the electrons transporting through the V_{ox} sites distributed in the WO_x layer.

In order to achieve the WO_x/a-Si interfaces, the a-Si layers with the thickness from 3 nm to 60 nm were deposited on the blanket WO_x, i.e. the WO_x/a-Si layer covers the interdigitated W electrode areas. The Hall-Effect measurement shows that the carrier type in the samples of blanket WO_x and WO_x/a-Si is electron, and the concentration in WO_x/a-Si is at least 2 order higher than that for blanket WO_x, which well agrees with the hypothesis and analysis for the transportation mechanisms around anode contacts. The resistance measured for the samples of WO_x/a-Si remains around 6.70×10^2 Ω, either under darkness or illumination (0.5 W/cm^2), roughly 4 order lower than that for blanket WO_x, even on the samples with only 3 nm a-Si on WO_x. Therefore, we can conclude that the intrinsic or photo-generated carriers in the a-Si layers on the WO_x layer do not contribute the high conductance, and the surface properties of the WO_x

may be greatly modulated upon the PECVD deposition of a-Si layer, even with a thickness of only 3 nm.

Auger Electron Spectroscopy (AES) characterizations were conducted in order to investigate the WO_x/a-Si interface, as shown in Figure 3.3(c-d). We prepared the samples with 15 nm a-Si on the WO_x interlayer, and the depth profile for the atomic concentration was obtained by AES measurement after each removal of the outer layer by ion sputtering. Figure 3.3a depicted the profiles for Si (Si2 peaks), W (W2 peaks) and O (O1 peaks) under the depth up to 25 nm, covering the transition regions at around 15 nm. In the outer layer, Si atoms is dominant, with negligible concentrations for O and W atoms. However, the concentration for Si atoms drops in the transition regions, and O atoms arises to a peak before the upraise of W atom concentration, which means there is a very thin silicon oxide (SiO_x) interlayer existing between the outer a-Si and inner WO_x layers. The SiO_x interlayer may be formed upon the deposition of the outer a-Si layer, since the beneath WO_x can be treated a good source of O atoms for the highly reactive Si radicals in the PECVD chamber. This is verified by the valley of O atom concentration immediately after the peak, and the valley is coupled with the upraise of the W atom concentration, which indicates the top surface of WO_x layer was greatly reduced, and an oxygen deficiency or high density V_{ox} region was created there. This region with high density of V_{ox} will be responsible for the high interfacial conductance for WO_x/a-Si interface, as illustrated in the Figure 3.3b.

The distribution of O atoms is critical for the transition regions from the outer a-Si to the inner WO_x layer, therefore further characterizations for the O1 peaks were summarized in Figure 3.3(d,e). The serial dN(E)/dE curves were depicted in Figure 3.3d under different depths, where the negligible amplitude corresponds to the outer a-Si layer, then the amplitude goes through the uprising to a peak, reducing at a valley and recovering, corresponding to the ultrathin SiO_x interlayer, transitional region with high density of V_{ox}, and the inner WO_x layer. The chemical environment will influence the signature AES peaks of the elemental atoms. The shifts for $KL_1L_{2,3}$ and $KL_{2,3}L_{2,3}$ transition in O1 peak were illustrated in Figure 3.3e, which can be attributed to the

electrical interaction between the cations (such as Si^{4+}, W^{6+}) and the negatively charged O atoms. The W cations are more positively charged than Si cations, thus pushing electrons in the external shell of O atoms further from the vacuum energy level and resulting in the higher binding energy. Moreover, the mixed O1 peaks and intermediate shift can be observed in the transition region, which is due to the inter-diffusion of the SiO_x and WO_x layers.

3.5 The a-Si Solar Cell Devices Based on Ultra-sparse Metal Meshes

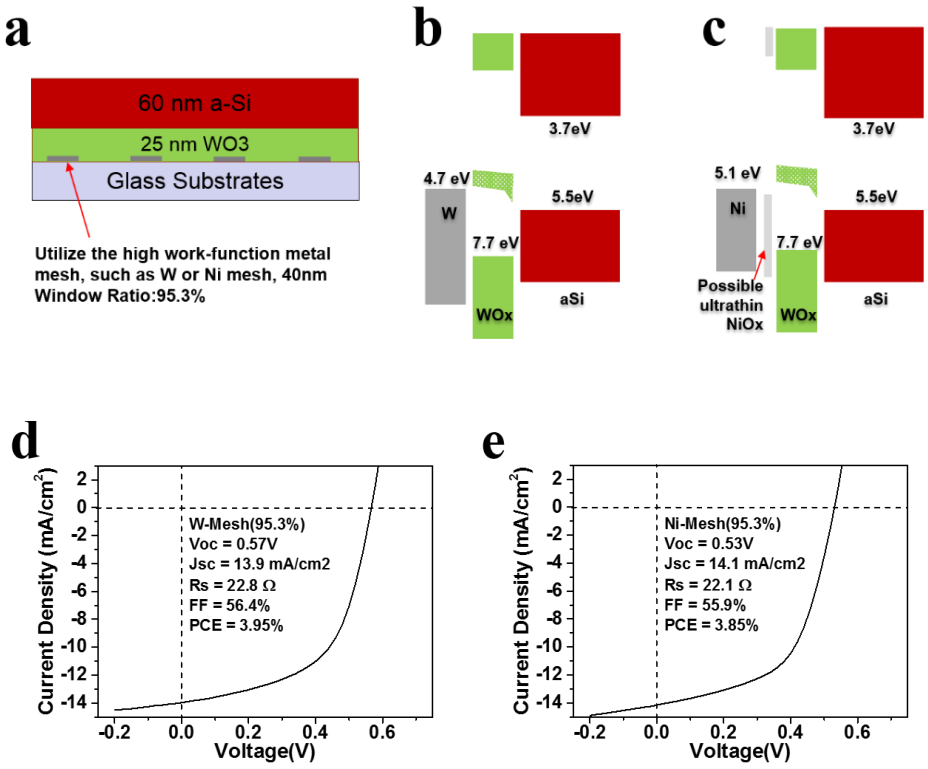

Figure 3.4 Device design, IV characteristics and the corresponding band diagram illustration for the a-Si solar cell devices based on ultra-sparse W or Ni metal meshes. (a) The cross section of the device, where W or Ni metal meshes were fabricated by lithography and the following lift-off processes, then WO_x interlayer was prepared by the oxidation from ultrathin W films. (b, d) The band diagram for the anode contacts on the W meshes and the corresponding IV sweeps. (c, e) The band diagram for the anode contacts on the Ni meshes and the corresponding IV sweeps, where ultrathin NiO_x may be produced during the oxidation of the WO_x.

The purpose of ITO electrode used in the Solar Cells or OLEDs is to create a highly transparent side of the devices. Meanwhile, the high ITO window ratio (95.3%) would not degrade the PCE performance of our a-Si devices, as discussed above. Considering the tiny ITO area portion in the ITO meshes, it will be of a significant meaning to replace the ITO meshes with other metal meshes and achieve an overall transparency up to 95.3%, higher than the conventional ITO coated glasses. The a-Si solar cell devices based on ultra-sparse W or Ni meshes were fabricated, in order to fulfill the applications of WO_x/a-Si interfaces. The W or Ni metal meshes were patterned by the photo-lithography, and finalized after the following lift-off processes. The WO_x layer is obtained similar with that on ITO meshes, just oxidation from the blanket ultrathin W films. In the W meshes, there will be a gradual transition region from metal W to the outer WO_x, which means a better affinity and lower barrier between metal W and WO_x. On the other hand, Ni is also used because of its high WF to facilitate carrier lowering at the anode side. Moreover, the possible ultrathin NiO_x interlayer will further mediate the barrier between Ni and WO_x. As shown in Figure 3.4(d,e), the 60 nm a-Si solar cell devices exhibit pretty good PCE (around 3.8% to 3.9%), a little higher than that based on ITO meshes. The comparable (even better) opto-electrical performance reveals metal meshes own great potential for the replacement of conventional ITO substrates, incorporating the interface with a high later conductivity.

3.6 Dimension Limitation for the Non-Electrode Area

As discussed above, the WO_x/a-Si interfaces can sufficiently support the collection of photo-generated carriers even under ultra-sparse meshes with window ratio up to 93.5%. The a-Si solar cell size for the commercial applications could be up to 10s cm scale, therefore it is necessary to further investigate the dimension limitation for the window or non-electrode area, not only to increase overall transparency and the light absorption, but also to reduce the fabrication cost for the electrode or electrical connections.

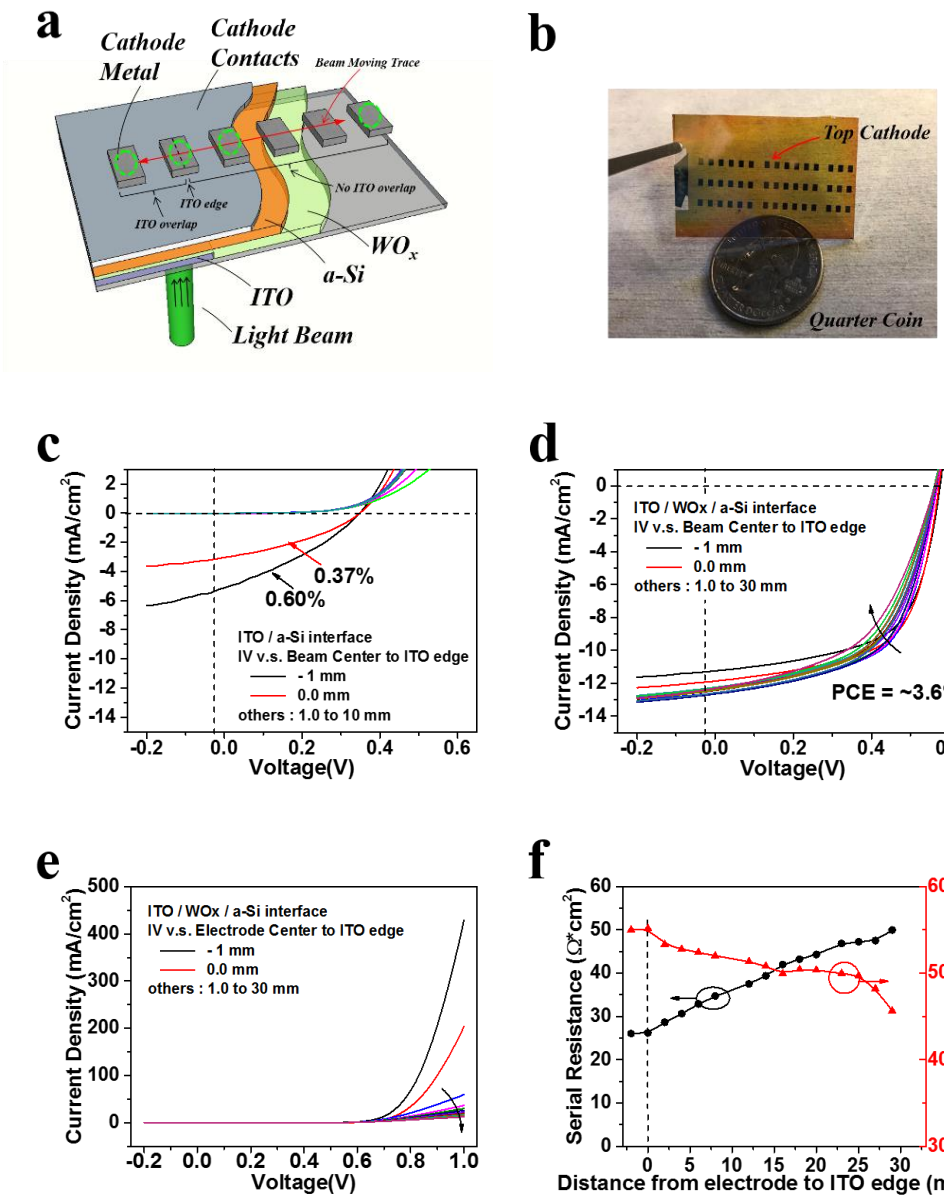

Figure 3.5 Investigation of the dimension limitation for the non-electrode area. (a) The schematic illustration of the sample, including the ITO / ITO-free area, and separated top electrodes. (b) The sample images for the 60 nm a-Si solar cell devices on large substrate pieces. (c, d) The IV sweeps under AM 1.5 illumination for the devices on the sample without WO_x interlayer (c) or with WO_x interlayer (d). (e) The IV sweeps under darkness for the devices shown in (d). (f) Summarization of the serial resistance and fill factor with x-axis of the distance to the ITO edge.

As shown in the Figure 3.5(a,b), the a-Si solar cell devices were fabricated on the large substrate pieces with one end narrowly covered by ITO. The ITO coating layer was patterned by photo-lithography processes, followed by blanket deposition of WO_x

and a-Si layers, as well as the cathode contacts and the separated cathode metal islands (1×1.4 mm^2). The cathode islands are aligned in several lines, and stretches from the ITO area to the ITO-free area. The light beam is slightly greater than the area of a cathode island, and moves from the end covered by ITO to the other one.

The IV characteristics under AM 1.5 illumination were compared for the samples w. / w.o. WO_x interlayers in the Figure 3.5(c,d). The WO_x interlayer works as HTL, and a huge barrier will exist between ITO and a-Si if no WO_x, resulting in a much smaller J_{sc} and PCE. Moreover, when the light beam moves out of the ITO area, the J_{sc} reduces to be negligible, indicating no lateral conductive pathways exist to facilitate the lateral transportation of photogenerated carriers to the ITO anode. On the contrary, with WO_x HTL interlayers, the J_{sc} and PCE can be well maintained, even for the device with a distance of 25 mm to the ITO edge. Further than the 25 mm, the R_s and FF just started to be gradually deteriorated, but still maintaining smooth IV curves and reasonable PCE, as shown in Figure 3.5f. The IV sweeps under darkness further verified the gradually increased R_s, since the current density under a forward bias is gradually decreasing. After symmetrizing the sample configuration, the dimension limitation is the ITO-free area is up to 5.0 cm, which is also the area dimension for the sufficient charge collection based on the WO_x/a-Si interface.

3.7 Conclusion

In this work, we developed the a-Si solar cell devices base on WO_x HTL and ZnO/PEI ETL. We systematically analyzed the interfacial properties for the WO_x/a-Si interface, including the band diagram and the carrier lateral transportation. The conductivity of the WO_x/a-Si interface is several orders higher than that of the standalone WO_x or a-Si layers, which is sufficient to support centimeter-scale non-electrode area. The hypothesis and characterizations reported here can be used to determine more details for the exact definition of the device areas and secure better device designs. More significantly, it gives rise to the further possibilities of devices with semi-transparency, ultra-sparse metal mesh electrodes, and so on.

Chapter 4 Top Cathode Contacts for a-Si Photodetectors towards Fingerprint Sensing Array

Abstract

For the mobile device screens, the fingerprint scanner is a hot development direction because of its importance for the biometric authentication. Among the various fingerprint sensing technologies, the in-screen fingerprint scanners are drawing extensive attentions, with the advantages of the compatibility with the mature a-Si processes and TFT arrays. In this work, we extend the applications and investigations of the a-Si devices with top ZnO NPs and PEI interlayers for the scenarios as photodetectors in the in-screen fingerprint sensing. High LDR are achieved up to 190 dB, and at least 4 orders for the illuminations < 50 Lux. In order to show the clear current ratio between the adjacent a-Si PD pixels, short linear arrays are fabricated, and the current sequence in the arrays exhibited good ratio up to 2 orders. Finally, peripheral circuits are built up based on the Arduino microcontrollers to fast acquire the current detected by the short linear arrays, which can clearly show the patterns mimicking the groves and valleys of the fingerprints.

4.1 Introduction

Besides the solar cells, there are many other practical applications for a-Si devices, such as a-Si TFT array for LCD panels, a-Si sensor arrays for Radiography, as well as the a-Si photodetectors array for fingerprint scanners.[114-119] In the research and development area for the mobile device screens, including the smart phones or tablets, the fingerprint scanner is a popular development direction because of its great potential application in the biometric authentication. People have developed a lot of the

fingerprint sensing technologies, such as ultra-sound detections, capacitive sensors, tactile MEMS, and so on.[120-123] In order to achieve better user experience of reading and operating, people further require a higher screen ratio for the mobile devices, therefore the integration or accommodation of the fingerprint scanners is a challenge for the system architecture design. Some developers placed the fingerprint scanners on the back side of the mobile phone, which introduces additional limitations for the usage habits and exterior protections. Under these circumstances, the in-screen fingerprint scanners are gradually becoming a hot development area, with the advantages of compatibility with the mature a-Si processes, and active integrations with the TFT arrays on the panels, bigger screen ratio for the full screen display.

The a-Si based photodetectors (PDs) are widely used in the development of the in-screen fingerprint sensing arrays.[124-127] Compared with the conventional p-i-n device design, the a-Si PDs in our groups are employing the hetero-structures, which will reduce the light absorption by the doping layer, and promote the carrier generations in the a-Si layer. In this work, we extended the applications of the ZnO/PEI cathode contacts to the a-Si PD, and fully characterized the properties under darkness to minimize the current leakage and transient performances to improve the working speed.

4.2 Device Design and Fabrication

As shown in Figure 4.1, we employed a similar device design, as used in the previous work, which is based on the metal oxide anode/cathode contacts. However, tungsten oxide (WO_x) is used here for the anode contacts, since it is found the WO_x oxidized from the ultra-thin W metal films provide a higher efficiency than the V_2O_5 interlayers deposited by the thermal evaporation, probably due to less cross-contamination in the chamber, or better band diagram matching. The basic device structure is ITO/WO_x/a-Si/cathode contacts. At the beginning, ITO substrates (Kaivo Optoelectronic Tech.) are thoroughly cleaned by sequential ultrasonic agitations in detergent, acetone, methanol and isoproponal alcohols, followed by dry blowing with nitrogen gun and 10 min oxygen plasma treatment under 150 °C. Next step is to

fabricate the WO_x layers, which is done by the oxidation from ultrathin W film (8-10 nm) deposited by sputtering. The intrinsic a-Si layers were deposited in the PECVD (PlasmaTherm 790) with a rate of 0.8 Å/s under 260 °C. The Zinc Oxide nanoparticles (ZnO NPs) were synthesized based on the previous report [59]. The ZnO NPs were finally dispersed in butanol with a concentration of 12 mg/mL, and PEI was dissolved in 2-methoxyethanol (0.2 wt%). The ZnO NPs were spin-coated twice at 3000 rpm for 30 s, then immediately annealed at 90 °C for 10 min. The PEI layers were spin-coated only once with the same procedure with ZnO NPs. The thicknesses of ZnO NPs and PEI layers were 15 nm and 10 nm, respectively. Finally, the 100 nm Aluminum top electrodes were deposited in thermal evaporator with a rate of 0.5 Å/s.

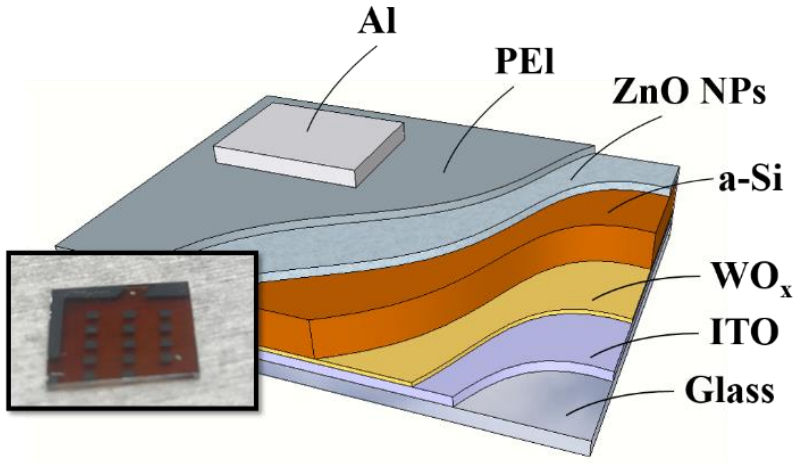

Figure 4.1 The schematic of the device design, which are fabricated based on ITO substrates, oxidation forming WO_x and PECVD deposition of a-Si, spin-coating of ZnO NPs and PEI, and the final thermal evaporation of top Al electrodes. The inset is sample image with separated top Al cathode islands.

4.3 Opto-electrical Characterizations for the Large Area a-Si PD

At the very beginning, we fabricated the samples with patterned top cathodes by shadow masks just to get fast verifications, where the active area is 1.4 mm^2. The IV characterizations were obtained under darkness or illumination (AM 1.5), as shown in Figure 4.2. The J_{sc} = 10.97 mA/cm^2, V_{oc} = 0.63 V and the corresponding PCE = 3.56%, which is pretty good for the 60 nm a-Si, indicating the anode contacts (WO_x) and cathode contacts (ZnO NPs / PEI) works well. Moreover, the R_{sh} and R_s is pretty good,

and the corresponding FF is around 51.6%, as shown in Figure 4.2a. The leakage current is highly related to the R_{sh}, since the R_{sh} is the resistance directly connected to the anode and cathode in the standard PV compact model. We obtained a flat leakage current around 0.0 V under darkness, as shown in the Figure 4.2b. The independence of applied voltage means the carrier generation under darkness is not strongly related to the electrical field across the interlayers, meanwhile the hole leakage to the cathode and electron leakage to the anode are negligible, which will facilitate to achieve the high current ratio under various illumination levels.

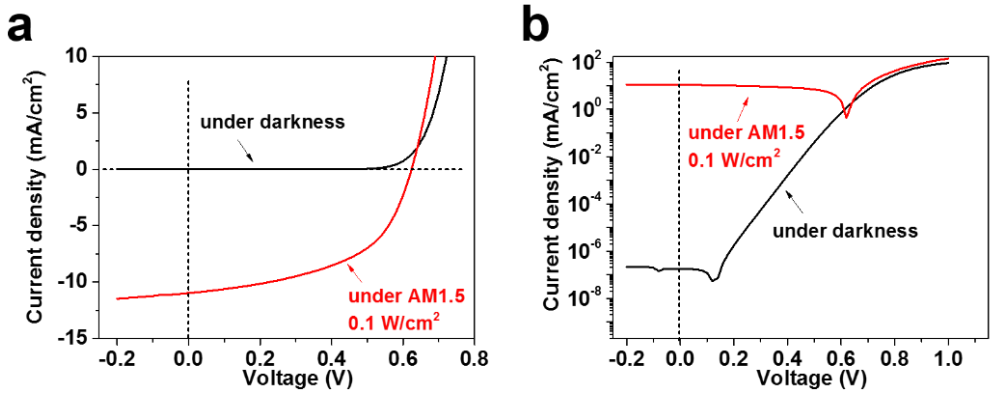

Figure 4.2 IV characterizations for the devices with top cathodes, in linear scale (a) and in log scale (b), where the J_{sc} = 10.97 mA/cm^2, V_{oc} = 0.63 V and the corresponding PCE = 3.56%.

The linear dynamic range (LDR), responsivity and external quantum efficiency (EQE) were characterized under various irradiance, as shown in Figure 4.3. The light source is white LED units, and the spectrum was depicted in Figure 4.3a. It includes a sharp peak at 454 nm, a typical blue light, and a wide band for green to yellow light. The apparent white light is obtained the combination of the blue light, and the light emitted from the yellow phosphor excited by the blue light. The white LED unit was coupled to the holder to ease the mounting of the samples with bottom illumination, and the light intensity was controlled by the Keithley Source-meter 2400 with a log scale sequence. In order to accurately characterize the ultra-small current, we use semiconductor analyzer HP 4156A to measure the photo current (I_{ph}) from a calibrated Si photodiode and the a-Si PD devices. The irradiance is the light power exposed to a

unit area under the unit of W/cm^2, and it can be calculated from the spectrum of the light source and the responsivity of the calibrated Si photodiode. The irradiance is proportional to the I_{ph} measured from the Si photodiode. Moreover, it is also critical to maximally reduce the environment light to achieve a better darkness.

The obtained LDR is at least 190 dB, which is comparable with the reported LDR for Si-based PD, and the linear range is down to the minimal I_{ph}, indicating the leakage current can be accurately characterized without the limitations from the equipment capability or precision. Moreover, the ratio under low illumination (< 50 Lux) is important for the applications towards fingerprint sensing, which is around 4 orders. The responsivity and the EQE can be calculated from the spectrum, irradiance and I_{ph}, as shown in the following equations, where P_{in} is the irradiance, e is the charge quantity of a electron, h is the plank constant, c is the light velocity, λ is the wavelength, $I(\lambda)$ is the spectrum. The responsivity is up to 0.212 A/W, and the corresponding EQE is up to 48%. The responsivity is highly proportional to the EQE, and they are following quite similar curves as shown in Figure 4.3c and Figure 4.3d. Considering mid-gap states induced by the dangle bonds and the tailing band formed by the amorphous feature of the atomic lattices, the photo-generated carriers are being recombined through Shockley-Read-Hall (SRH) processes, as the electron-hole pairs are being generated. At ultra-low illumination, the generation rate is much lower than the recombination rate, therefore the responsivity and EQE are close to zero. As the illumination increases, the carrier generation and recombination get balanced with each other, then the responsivity and EQE reached a stabilized status. If the illumination continues to increase, the generation rate is much higher than the recombination rate, and the recombination gets saturated. Therefore, the collection efficiency of the photo-generated carriers are upraised, producing a even higher responsivity and EQE, which is indicated around the high illumination end of the curves shown in Figure 4.3c and Figure 4.3d.

$$R = \frac{I_{ph}}{P_{in}} \quad (A/W)$$

$$EQE = \frac{I_{ph}/e}{\int\left(\frac{\lambda}{hc}P_{in}\frac{I(\lambda)\frac{hc}{\lambda}}{\int\frac{hc}{\lambda}I(\lambda)d\lambda}\right)d\lambda} = \frac{I_{ph}}{e}hc\frac{\int(I(\lambda)/\lambda)d\lambda}{\int(P_{in}I(\lambda))d\lambda}$$

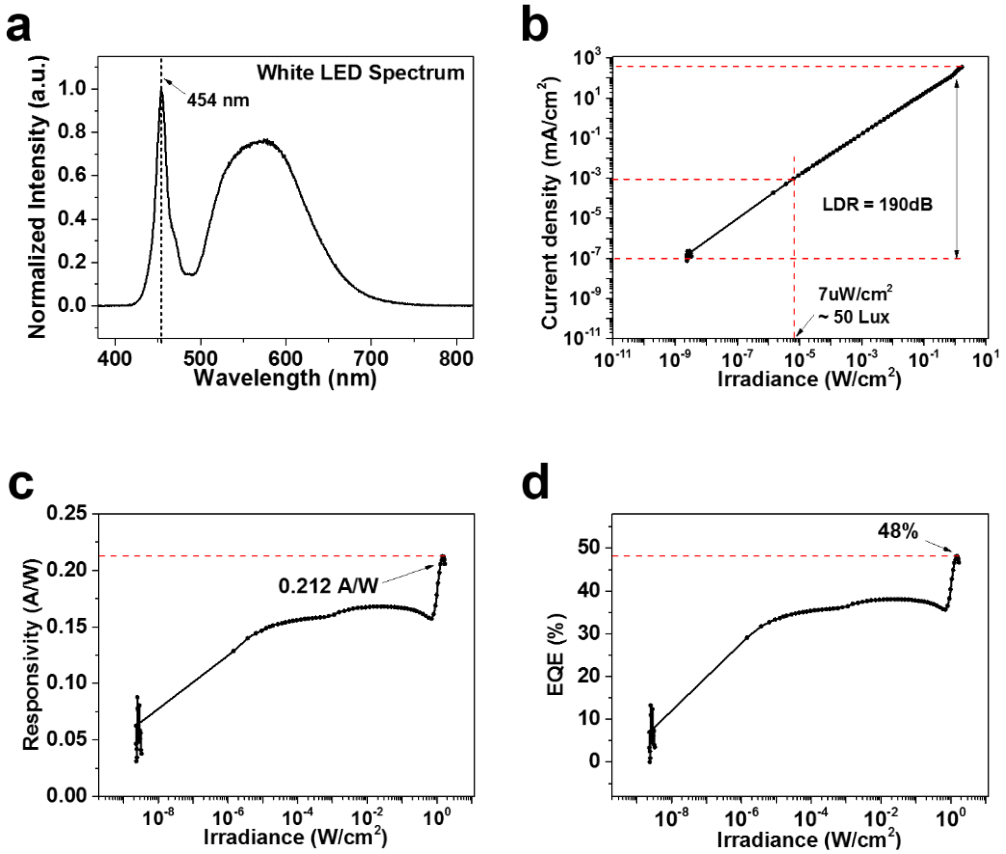

Figure 4.3 The characterizations for the linear dynamic range, responsivity and external quantum efficiency, under the x-axis of irradiance from white LEDs. (a) Spectrum of the white LED. The obtained current ratio (linear range) is at least 190 dB (b), the responsivity up to 0.212 A/W (c), and the corresponding average EQE is up to 48% (d).

Green light is the highest visual perception point in the Luminous Efficiency Function. The LDR, responsivity and EQE are characterized again under the illumination of green light, as shown in Figure 4.4. The spectrum of the green LED unit is depicted in Figure 4.4a, where the peak wavelength is 530 nm with a 100 nm FWHM.

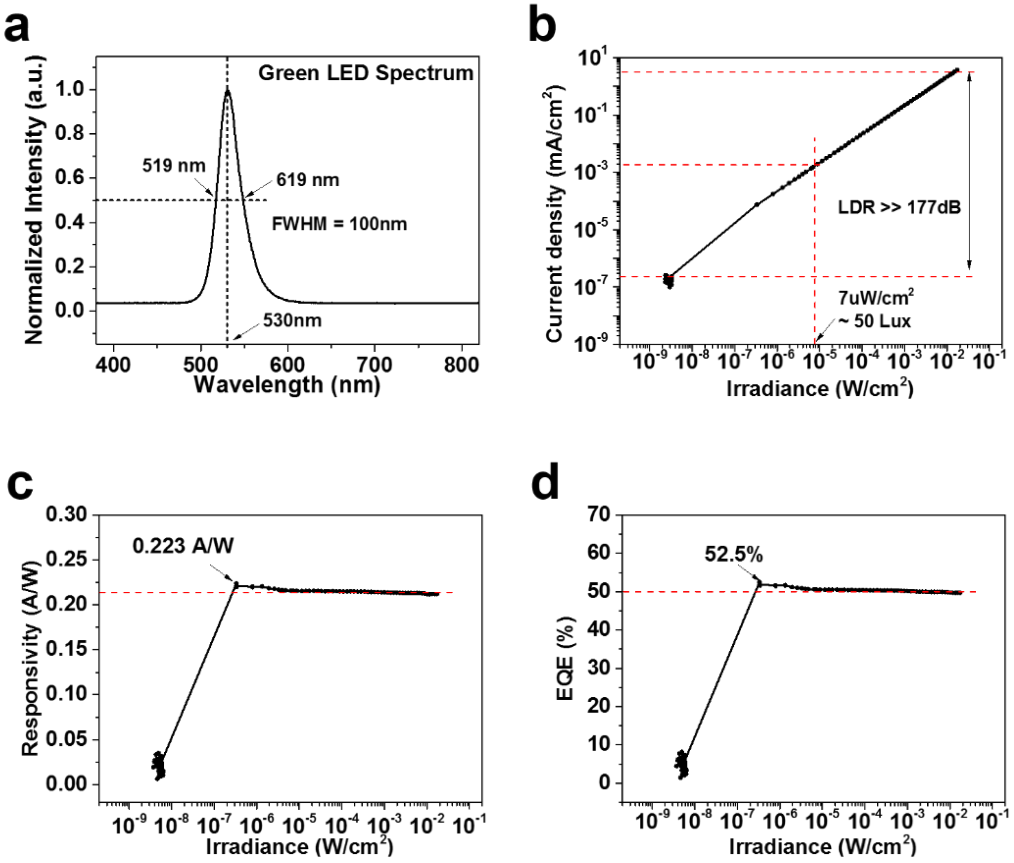

Figure 4.4 The characterizations for the linear dynamic range, responsivity and external quantum efficiency, under the x-axis of irradiance from green LEDs. (a) Spectrum of the green LED. The obtained current ratio (linear range) is at least 177 dB (b), the responsivity up to 0.223 A/W (c), and the corresponding average EQE is up to 52.5% (d).

The measured LDR is 177 dB, a little lower than that for the illumination of white light, because the light intensity of green LED is much lower, and it cannot reach up the illumination where the non-linear effects happened due to the IR-drop across the serial resistance. The actual LDR is supposed to be much higher than 177 dB. The current ration under the illumination < 50 Lux is well maintained, still around 4 orders. The obtained responsivity and EQE are up to 0.223 A/W and 52%, respectively, which are a little higher than that for white light. The responsivity and EQE calculated here are just average values for the whole spectrum of the light source, and it has a higher value for the green light since the responsivity is higher in the wavelength range near 530 nm. The responsivity stabilized at a relative constant value, because the photo-

carrier generation and recombination get balanced, as discussed above. Since the green LED unit used here has a much lower light emitting intensity, the curve did not stretch out to the saturation status of the recombination process, and achieve a better responsivity.

The responsivity and EQE under different wavelengths are measured and analyzed. The setup is composed of light source (solar simulator), monochromator, Keithley Source-meter 2400, and calibrated Si photodiode. The monochromator can be controlled by Labview program, and transmits a mechanically selectable narrow band of wavelength, where the center wavelength sweeps from 400 nm to 800 nm. The Si photodiode was connected to the source-meter 2400 to measure the photo-current when the monochromator is sweeping. The power density and photon flux of the transmitted lights can be calculated by considering it as a mono-color light because of its narrow band. Then the a-Si PD sample is mounted to the setup, and the flow of the collected electrons can be calculated based on the measured photo-current. Finally, the extracted responsivity and EQE are illustrated in the Figure 4.5. The the edge of the conduction or valance bands of a-Si are not that sharp as that for c-Si because of the band tails, and the forbidden gap between the equivalent CB and VB is around 1.7 eV, larger than that for c-Si. Therefore, the absorption and corresponding responsivity are much lower at the long-wavelength end. As shown in Figure 4.5, the a-Si PD mainly absorbs the light with a wavelength less than 600 nm. The peak at 550 nm is probably due to the light resonance and the corresponding FB cavity effects in the a-Si PDs.

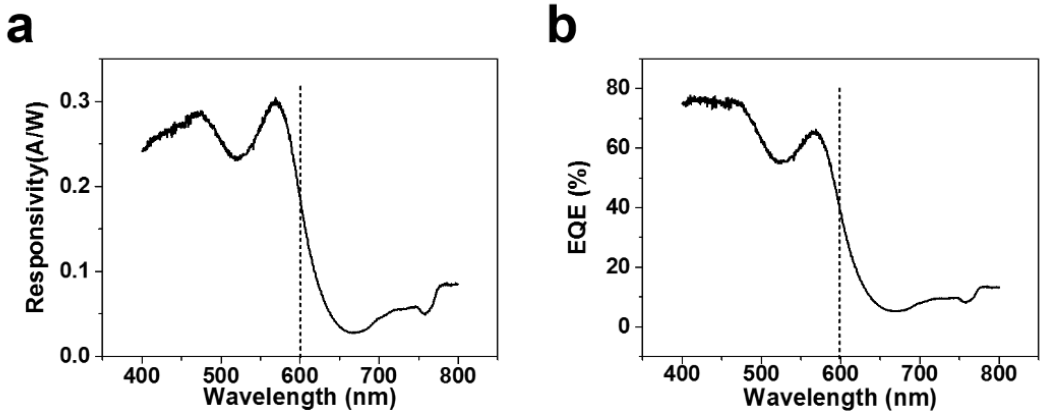

Figure 4.5 The responsivity and EQE under the x-axis of wavelength.

The peak responsivity and EQE are quite similar to the conventional a-Si PIN PD.[128] Moreover, because of the transparent anode interlayers (WO_x), the absorption of the shorter wavelength was enhanced.

Transient response the photocurrent are measured to extract the bandwidth, as shown in Figure 4.6. The light source is LED, driven by function generators. The photocurrent is converted to voltage by the OP AMP and a feedback resistance. The frequency of the light pulse is gradually increased to compare the amplitude and the rise and fall edges. The rise time (t_r) is counted for the response increases from 10% to 90% of the whole amplitude, which is 0.37 us. The bandwidth (BW) can be extracted from the equation $BW = 0.35/t_r = 0.93$ MHz. The shot noise (i_s^2) and thermal noise (i_{th}^2) can be derived based on the BW, the dark current and shunt resistance based on the extraction procedure described in [129], the obtained $i_s^2 = 3.52 \times 10^{-26}$ A^2 and $i_{th}^2 = 9.94 \times 10^{-25}$ A^2. Then the extracted Noise Equivalent Power (NEP) is 4.78×10^{-12} W for the BW of 0.93 MHz, and the corresponding specific detectivity (D*) is 2.47×10^{13} Jones, which are comparable to the a-Si PIN PD, but better than the organic photo detectors because of the lower leakage current.[130-132]

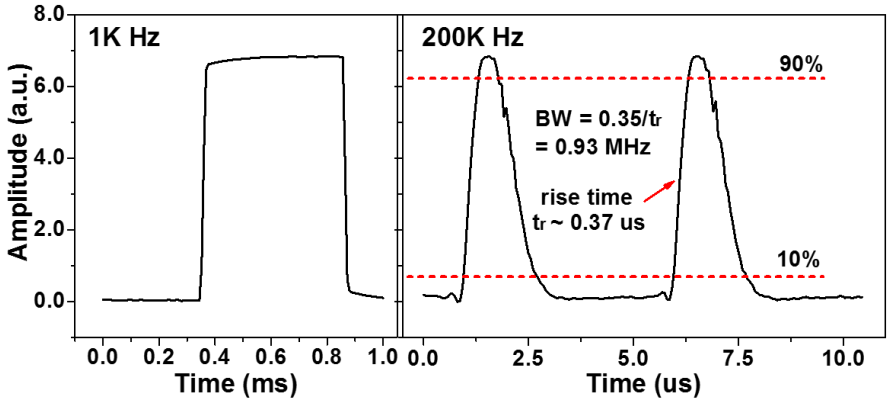

Figure 4.6 The transient response and the bandwidth under the rectangular waveform stimuli of the light source.

4.4 Fabrication and Characterizations of a-Si PD Short Linear Array

Moreover, the short linear arrays are fabricated in order to investigate the opto-electrical performance of the small size devices and the optical interference between the adjacent pixels, as shown in Figure 4.7. Each sample includes 16 a-Si PDs (pixels)

covering a length of 2 mm, and the 18 contact pads for the peripheral circuits, where 16 of them are for the top cathode contacts of the 16 pixels and the rest 2 are for the bottom anode contacts. The corresponding peripheral circuits are used to detect the photocurrent based on the operational amplifier (OP AMP) and Arduino microcontrollers. The OP AMP is used to detect the photocurrent and convert it to voltage. The Arduino microcontrollers are employed to digitize the voltage by the embedded ADC, and the data will be sent to the user interface terminals at the laptop. The short linear arrays are fabricated based on the lithography processes, since each layer needs to be patterned to minimize the electrical interference between the pixels.

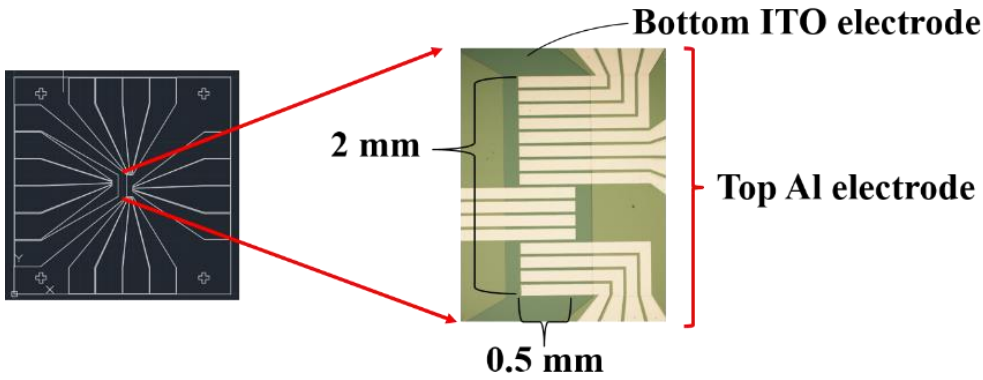

Figure 4.7 The layout and image for the short linear array, composed of 16 pixels (a-Si PD) and contact pads for the peripheral circuits. The area of each pixel is 100 um × 500 um, the length covered by the 16 pixels is 2 mm, and the sample size is 2 cm × 2 cm.

The gap between the adjacent pixels is very small, only 50 um, which will be much smaller in the real scenarios of in-screen fingerprint sensing. Therefore, minimizing the optical interference for the adjacent pixels is an important design or measurement specification. Figure 4.8a depicted the schematic illustration of the test configuration for the a-Si PD arrays partly covered by the light beam with a light intensity of AM 1.5 (0.1 W/cm^2). The light was guided from the solar simulator and masked by a small steel sheet with a 1.3 mm hole. The light beam covers the # 1 to #8 pixels, and a thinner (0.7 mm) glass pieces with ITO coating were used as substrates in order to reduce the reflection through the substrate mode.

The comparison of the measured photocurrents is shown in the Figure 4.8b. The photocurrent is proportional to the device area, and the current density is almost identical to the large area devices (in Figure 4.2). The photocurrent starts to reduce from #5, which could be ascribed to the light non-uniformity within the beam. From # 8 to # 16, the photocurrent is reduced by around 2 orders, indicating a good suppression for the possible optical interference between the adjacent pixels.

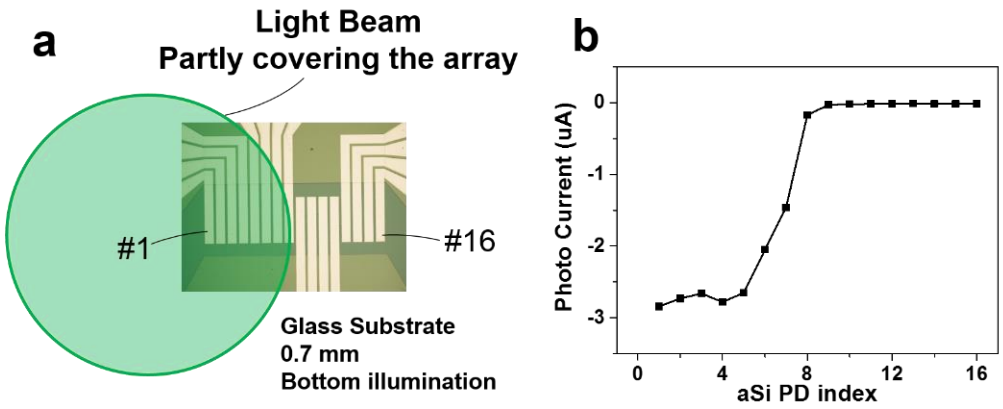

Figure 4.8 (a) Schematic illustration of the test configuration for a-Si PD array. The intensity of the light beam is AM 1.5 (0.1 W/cm^2), which comes from the solar simulator and masked by a small steel sheet with a 1.3 mm hole. The light beam covers the # 1 to #8 pixels, and 0.7 mm glass pieces with ITO coating were used as substrates. (b) Comparison of photocurrent obtained from the 16 pixels.

Figure 4.9 illustrated the detailed IV curves for the selected pixels #4, #7 and #12. The overall current under higher voltage (0.8 V to 1.0 V) is determined by the carrier density and the corresponding conductance. Higher forward current occurs for the pixel #4, indicating the higher photo-carrier generation rate. The IV curves are also depicted under a log scale to better differentiate the current around zero-bias to weak reverse bias, as shown in Figure 4.9b. The fully illuminated pixel #4 has a photocurrent 2 order higher than the masked pixel #12, which well agrees with the previous discussion illustrated in Figure 4.8b. However, the photocurrent of pixel #12 is still higher than that for the leakage current measured under darkness, by more than 3 orders, which indicates that photocurrent ratios for the adjacent pixels can be counted by orders, but still limited by the light scatterings or reflections through the substrates from the illuminated area to the masked area.

The LDR and responsivity are characterized for the individual a-Si PD in the short linear array under various irradiance, as shown in the Figure 4.10. The LDR is up to 192 dB, current ratio is well maintained at around 4 orders under the illumination < 50 Lux, and linear range stretches to the darkness, which is almost identical to the results for the large area pixels, indicating a good proportionality about the area. The responsivity is also comparable, but a little lower than 0.2 A/W, which is probably due to the possible contaminations introduced in the wet processes in the photo-lithography procedures.

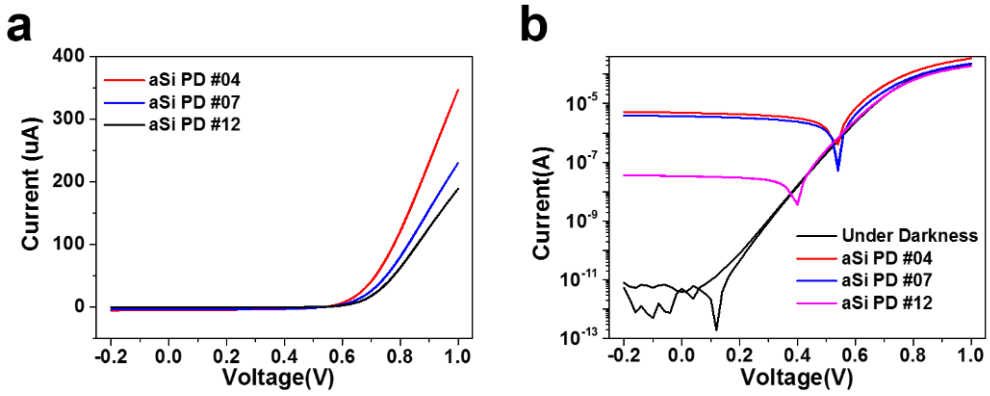

Figure 4.9 Selected IV curves for the a-Si PD arrays partly covered by the illumination of AM 1.5(0.1 W/cm^2), in the linear scale (a) and log scale (b).

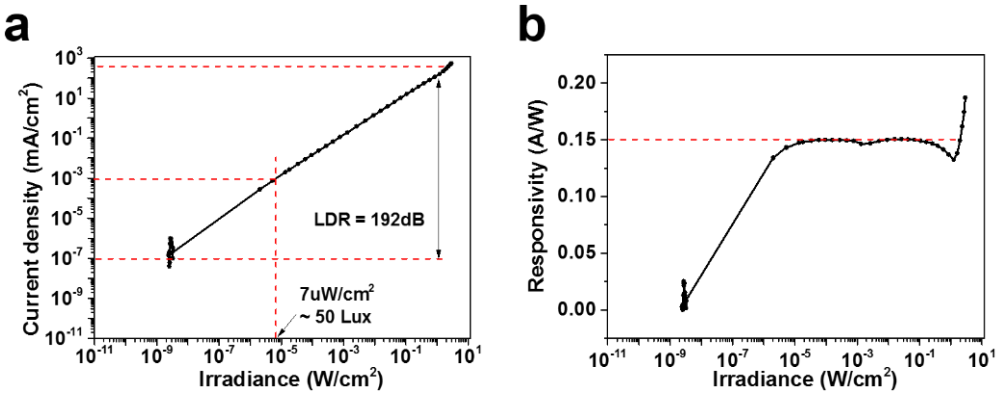

Figure 4.10 The characterizations for the linear dynamic range (a) and responsivity (b) for the individual a-Si PD in the short linear arrays.

The current ratio for the adjacent pixels in the short linear array are also compared under the illumination of 50 Lux, as shown in Figure 4.11. The photo-current for

masked pixel #12 is comparable to the leakage current under darkness, indicating the light absorption and losing occur during the scatterings or reflections through the substrates, and the low illumination is not able to overcome the optical loss. However, the current ratio is still well maintained at higher than 1 order, comparing the pixel #4 and pixel #12. The curve for the photocurrent sequence also depicts the optical loss, where the curve gradually reduces from the illuminated area to the masked area, with a lower slop around the light beam boundary. Therefore, higher background illumination will facilitate the data processing and maintain the image fidelity for the in-screen Fingerprint Sensing.

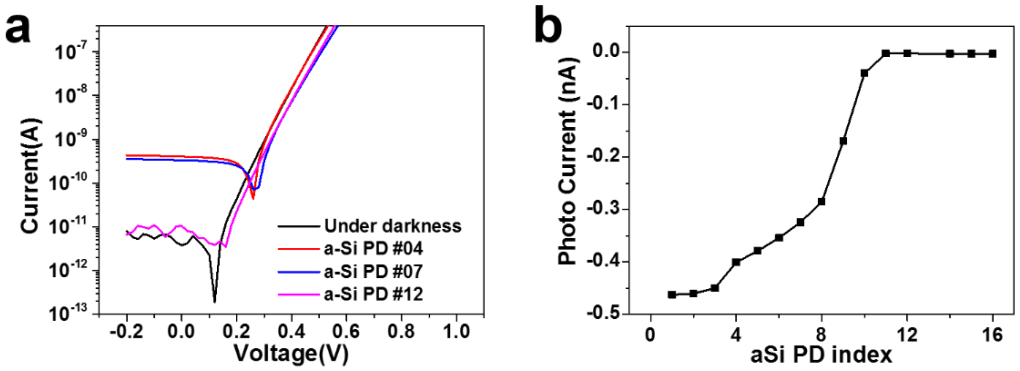

Figure 4.11 (a) Selected IV curves for the a-Si PD arrays partly covered by the illumination of 50 Lux, in log scale. (b) Comparison of photocurrent obtained from the 16 pixels.

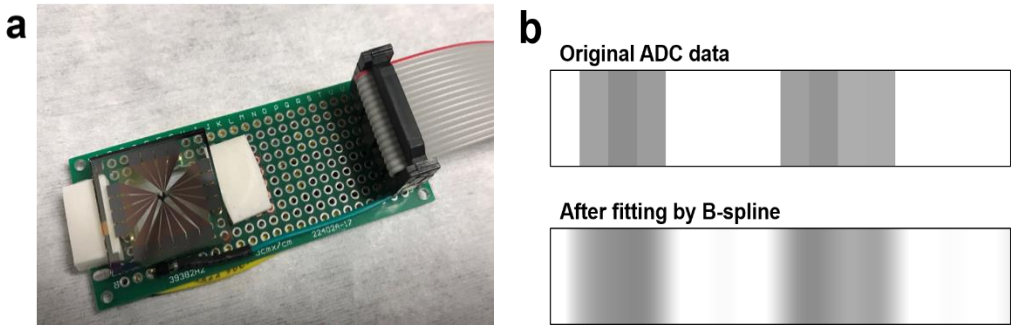

Figure 4.12 (a) Peripheral socket for the mounting of the short linear array sample. (b) The original ADC data collected by the Arduino microcontroller and the data after fitting by B-spline model in the user interface developed on the laptop. The short linear array was masked by two black lines drawn by a fine marker to mimic the surface reflection difference caused by the groves or valleys of fingerprints.

In order to mimic the detection for the fingerprint sensing, peripheral circuits includes the coupling socket, photocurrent detection module, data conversion and communication module, as well as the user interface on laptop. The coupling socket is basically a breadboard with 18 spring probes to connect the pads located around the edge of the short linear array samples, as shown in Figure 4.12a. Photocurrent detection module is composed of OP AMP and multiplexers, where the multiplexer is used to switch the connections to a certain pixel, and the OP AMP is used to convert the photocurrent to a certain voltage through a feedback resistance. Therefore, the output voltage from the OP AMP is proportional to the detected photocurrent. Arduino microcontrollers are employed to digitize the voltage through the embedded ADC and transmit the ADC data to the user interface developed on the laptop. Finally, the data was shown as banners with different grey levels, including the original data from ADC and the data after fitting by the B-spline model.

We use fine black marker to draw two lines over some pixels to mimic the surface reflection difference caused by the groves or valleys of Fingerprints. After illuminating the sample with an appropriate intensity, we obtained the data banner with distinct two groves, as shown in Figure 4.12b. The results verified the feasibility of the develop a-Si PD for the potential applications of fingerprint sensing.

4.5 Conclusion

The a-Si devices with top cathode contacts fabricated based on the ZnO NPs and PEI interlayers are further characterized for the application scenarios as photodetectors, especially towards the in-screen fingerprint sensing. High LDR are achieved up to 190 dB, and at least 4 orders for the illuminations < 50 Lux. The responsivity and EQE are depicted as the axis of irradiance and analyzed based on the SRH processes. In order to show the clear current ratio between the adjacent a-Si PD pixels, short linear arrays composed of 16 pixels are fabricated. The current sequence in the arrays exhibited good ratio up to 2 orders. However, further optical design need to be involved to minimize the reflections or scattering through the substrates. Finally, peripheral circuits are built

up based on the Arduino microcontrollers to fast acquire the current detected by the short linear array, which can clearly show the patterns mimicking the groves and valleys of the fingerprints.

Chapter 5 Inverted Device Design of a-Si Photodetectors for the Integration with TFT Array Backplanes

Abstract

The in-screen Fingerprint scanners usually require the sensing arrays to be composed of 10s to 100s K photodetectors to acquire the high-resolution patterns. Therefore, the inverted a-Si PD with bottom cathode contacts are developed and characterized to fulfill the requirements of the architecture design for the sensing arrays. The ZnO and MoO_x are employed as the ETL and HTL for the inverted a-Si PDs, respectively. The current leakage and LDR get analyzed with different a-Si thicknesses and device areas. The a-Si PD arrays with device areas down to the actual pixel level are fabricated based on the photo-lithography processes in order to extract accurate current leakage and LDR. Finally, the optimized a-Si PD arrays are fabricated on the LTPS TFT backplanes for the further demonstration after integration with the peripheral IC chips.

5.1 Introduction

The normal type device design with top cathode contacts has been discussed, and the demonstration of the short linear arrays verifies the potential applications for the fingerprint sensing. However, the practical systems can not work only based on the standalone individual a-Si PD devices, and the accurate fingerprint pattern acquiring requires 10s to 100s K a-Si PDs (pixels) in the sensing panel to work together based on a matrix architecture.[133] Each a-Si PD in the matrix needs to be addressed and measured, which has to be realized by another matrix, TFT matrix, including the

peripheral current amplifier or converter modules. There is a switching TFT in each a-Si PD pixel to control the connection between the internal pixel circuits and the external peripheral circuits. The gate terminals of the switching TFTs located in the same row are connected together by word lines, and the drain terminals of the switching TFTs located in the same column are connected together by data lines, thus each switching TFT are connected by two lines with external peripheral circuits. The word lines are used to control the on or off status of the switching TFTs, and only one row of the matrix is switched on. Correspondingly, the pixel information only in that row can be read out through the data lines in that time slot, and another row in the next time slot. The total time used to sweep all the rows is the frame time, usually counted as refresh frequency, which is 60 or 120 Hz for the typical flat panel display screens.[134-136]

The pixel circuit are quite different for different application scenarios, such as only a capacitor for the TFT-LCDs, and current driving or compensation circuit for OLEDs and so on.[137-140] As for the a-Si PD pixel, it includes a storage capacitor (C_{st}) and an a-Si PD, as shown in Figure 5.1a. Under illumination, the a-Si PD will generate photocurrent to charge C_{st}, and the charge in C_{st} will be subsequently transferred to an external charge-sensitive amplifier during the readout phase when the switching TFT is turned on. Since the photocurrent is proportional to the illumination intensity (irradiance) which determine the charge quantity stored in C_{st}, thus the read-out voltage from the whole panel can provide the mapping of the illumination, which is actually used to recognize the fingerprints.

As we discussed, the a-Si PDs need to be actively integrated with the TFT matrix, thus the process or architecture compatibility is becoming a critical factor for the device design of the a-Si PDs and the fabrication of the TFT matrix. As shown in Figure 5.1a, the anode of the a-Si PD has to be grounded, and the cathode is connected to the source terminal of the switching TFT. The TFT matrix is usually located beneath the a-Si PD array, since the fabrication procedure of TFT need high temperature processes, which is highly possible to deteriorate the electrical performance of the a-Si PDs if it is fabricated on top of a-Si PDs. Such an architecture determines the cathode of a-Si PD

has to be on the bottom side. Moreover, the ground electrode is usually the common electrode applied the lowest voltage in the panel. In order to minimize the fabrication cost and enlarge the pixel area, the ground electrode is prepared by the blanket deposition through the whole panel on the top side, as shown in Figure 5.1b. Considering all the limitations and strategy together, the inverted device design for the a-Si PD need to be developed for the further integration with the TFT backplane based on the LTPS processes.

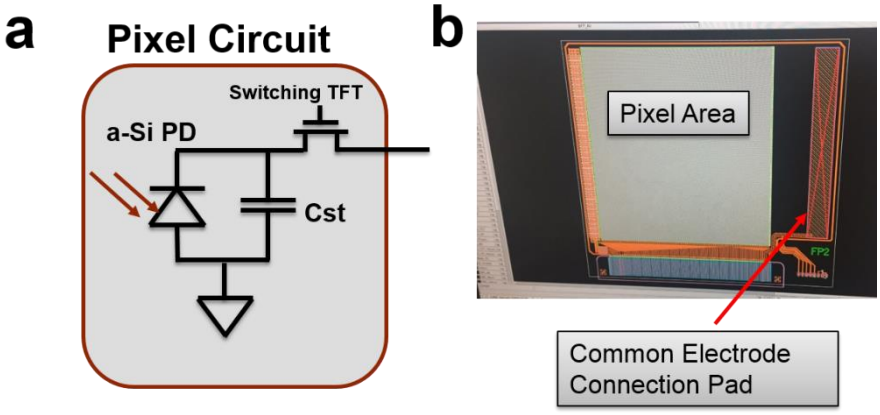

Figure 5.1 (a) The pixel circuit for the a-Si PD matrix, where the switching TFT is fabricated on the beneath and interfacing the a-Si PD with a connection pad. (b) The layout design for the demo of the fingerprint sensing based on the a-Si PDs. The right area is the connection pad for the common electrode, and the bottom side fine pad is for the future IC chip bonding. The TFT backplane comes from the collaborative side (China Star Opto-electronic Tech.)

5.2 Device Structure and Fabrication

The inverted device design developed for the demo integrated with LTPS backplane is shown in Figure 5.2. The ITO coated glass pieces are used as the substrate, since the connection pads reserved in the TFT backplane are ITO. ZnO and MoO_x are used as ETL and HTL, respectively. The active layer a-Si is deposited by PECVD under the substrate temperature of 260 °C. The 40 nm ZnO can be deposit by ALD or Sputtering, and the 50 nm MoO_x is deposited by thermal evaporation. The top anode are prepared with 100 nm Ag, Ni or Mo, where Ag and Ni are deposited by thermal or e-beam evaporation, and Mo is deposited by sputtering. Mo anode is further investigated since it is compatible with the processes of the TFT-LCD production line.

The transparent ITO cathode and metal anode are used for the bottom illumination, and the a-Si PD array will be mounted to the color filter side in the TFT-LCD screen, which will inevitably increase the fabrication cost, since there are two array panels, one is for the LCD pixel, and the other is for the a-Si PD pixel. Therefore, the transparent ITO can be replaced by metal Ti, and metal anode can be replaced by the transparent ITO to realize the top illumination configuration, which can be integrated with the TFT array for the LCD pixels.

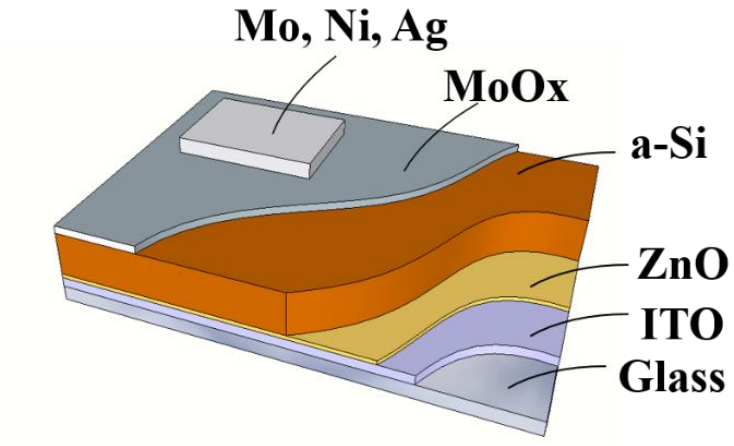

Figure 5.2 Device design with inverted architecture. The ITO coated glass pieces are used as the substrate, since the connection pads reserved in the TFT backplane are ITO. ZnO and MoO_x are used as ETL and HTL, respectively. The top anode will be prepared with Ag, Ni or Mo, where Mo anode will be further investigated since it is compatible with the processes of the TFT-LCD production line.

5.3 IV Characterizations for Large Area Devices

Firstly, IV characterizations are obtained for the devices with Ag, Ni or Mo anode, under darkness or illumination AM 1.5 (0.1 W/cm^2), and the device area is defined by the top electrode (1.4 mm^2), as shown in Figure 5.3. Figure 5.3(a-c) are depicted in the linear scale, where the V_{oc} is around 0.44 to 0.47 V, and the J_{sc} is 8.85 mA/cm^2 for Ag anode, 6.71 mA/cm^2 for Ni anode, 7.81 mA/cm^2 for Mo anode, respectively. Both V_{oc} and J_{sc} are smaller than those with top cathodes, indicating a much smaller PCE. It is probably due to the bottom cathode contacts is not good as the top, since there no additional interlayers to further reduce the barrier between ZnO and CB of a-Si. In the devices with top cathode contacts, we utilized the dipole moment induced in the PEI

interlayer, and achieve good IV performance. However, there is no such polymer layers which can endure the deposition of a-Si layer under 260 °C. As shown in Figure 5.3d, the IV curves are also depicted under a log scale to show the leakage current under darkness, and the corresponding current ratio. The large current ratio was maintained between the darkness and illumination, while the leakage current under the reversed bias got increased a lot, which is a challenge for the peripheral circuit design.

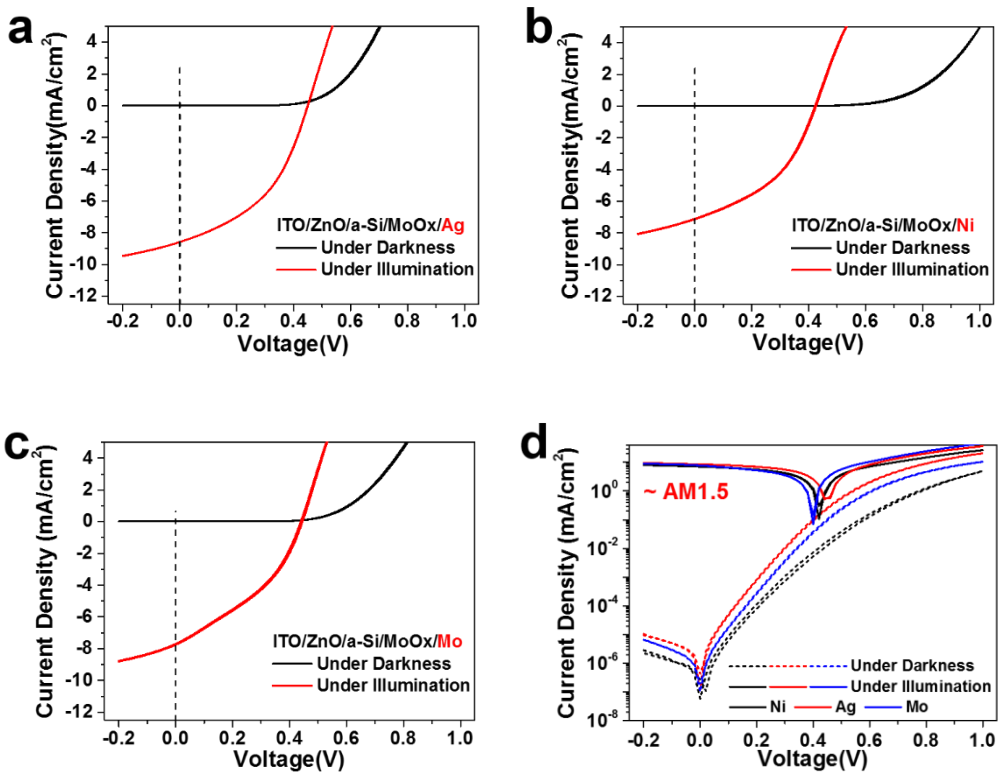

Figure 5.3 IV characterizations for the devices with Ag, Ni and Mo anode, respectively, under darkness or illumination AM 1.5 (0.1 W/cm^2). The curves are also depicted under a log scale to show the leakage current under darkness, and corresponding current ratio (d).

As shown in Figure 5.4a, the inverted a-Si PD devices with top Mo anodes are further characterized in details. LDR data were obtained under the reversed biases from 0.0 V to -0.2 V. Under zero-bias, the a-Si PDs own highest LDR and it stretches to the lowest illumination, indicating the ultra-small current is not limited by the measurement precision. However, as the reversed bias increases, the measured minimal current is increased, because of the increased leakage current. The analysis based on the band

diagram will give more explanations to the increased leakage, as shown in Figure 5.4b. The bottom cathode contacts includes the ITO electrode, and ZnO ETL which is directly contacting the a-Si layer. The WF of ITO is around 4.8 eV, and the WF of ZnO is closed to the CB around 4.4 eV, since ZnO interlayer is usually heavily n-doped. Theoretically speaking, the barrier between the ZnO and a-Si is pretty high, up to around 0.7 eV, which is also means the barrier is not that large sufficiently to block the hole transportation to the cathode, especially after considering the dangling bonds and band tails of the a-Si. Under the reversed biases, a triangle well will be formed around the VB of a-Si and ZnO interface, which increases the possibility for hole transportation to the cathode through the Thermionic emission, Thermionic-Field emission or Field emission, building a conductive pathway connecting the bottom cathode and top anode. This pathway is equivalent to electron injection from cathode to the VB of a-Si layer, which can be modeled by the shunt resistance in the standard PV model. The extracted shunt resistance are only 207, 205 and 123 $\Omega \cdot cm^2$ for Ag, Ni and Mo anode, respectively.

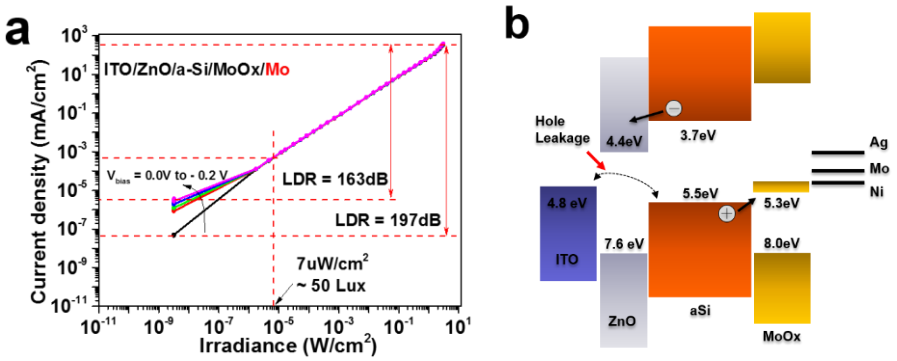

Figure 5.4 (a) LDR characterizations for the a-Si PD with top Mo anode under reversed bias from 0.0 V to -0.2 V. (b) The illustration of the band diagrams to show the possible current leakage through the ZnO / a-Si interfaces, and the main reasons for the increased leakage under a reversed bias.

The responsivity and EQE are measured for the developed inverted a-Si PD devices, as shown in Figure 5.5. The responsivity and EQE follow the similar tendency, compared with those measured for the a-Si PD devices with top cathodes, and they are much lower at the long-wavelength end because of the equivalent band gap (1.7 eV)

higher than the crystalline silicon. The inverted a-Si PDs mainly absorb the light with a wavelength less than 600 nm. However, there is no peaks at 550 nm, which indicating the different optical interactions within the a-Si PD device structure from those with top cathode contacts discussed in previous chapter.

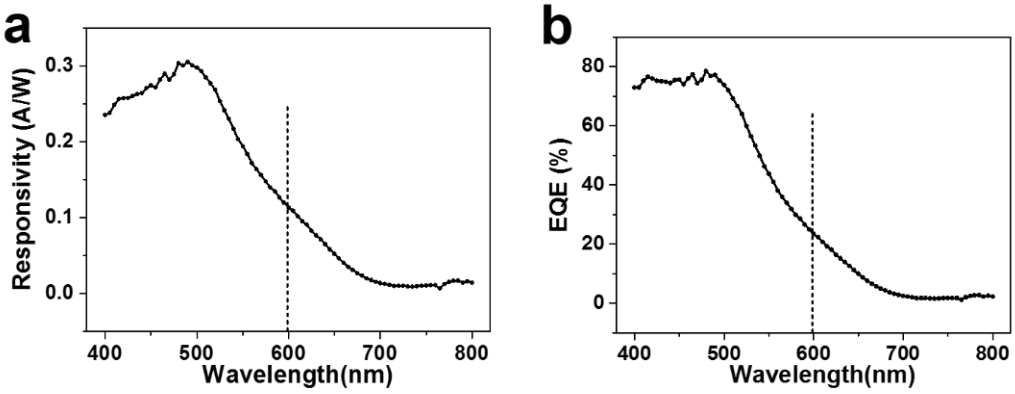

Figure 5.5 The responsivity (a) and EQE (b) of the developed inverted a-Si PD devices under the x-axis of wavelength.

5.4 Fabrication and Characterizations for Pixel Devices

The a-Si PD matrix and integration with the TFT backplane is not capable to work based on the large area devices. We further fabricated and characterized the opto-electronic performance of the a-Si PD devices with the comparable pixel area (down to 50 um × 50 um), and the fabrication procedure is shown in Figure 5.6a. All the layers are patterned by photo-lithography processes, but with different etching methods, where ITO and ZnO layers are etched by HCl, a-Si layer is etched by RIE etching, and final top anode contacts is formed lift-off process or RIE etching. As shown in the top view of the layout design, ITO and ZnO are patterned with the identical mask, and the area of a-Si layer is a little bigger than the designed device area (cathode and anode overlapping area) in order to insolate the possible direct connection between the cathode and anode due to the limited alignment resolution during the photo-lithography processes. Finally, the pattern of the HTL and top anode metal are identical to each other, which are formed by lift-off processes or RIE etching. Figure 5.6b showed the

image of the a-Si PD devices, including the linear array and the individual devices with different areas (from 50 um × 50 um to 200 um × 200 um).

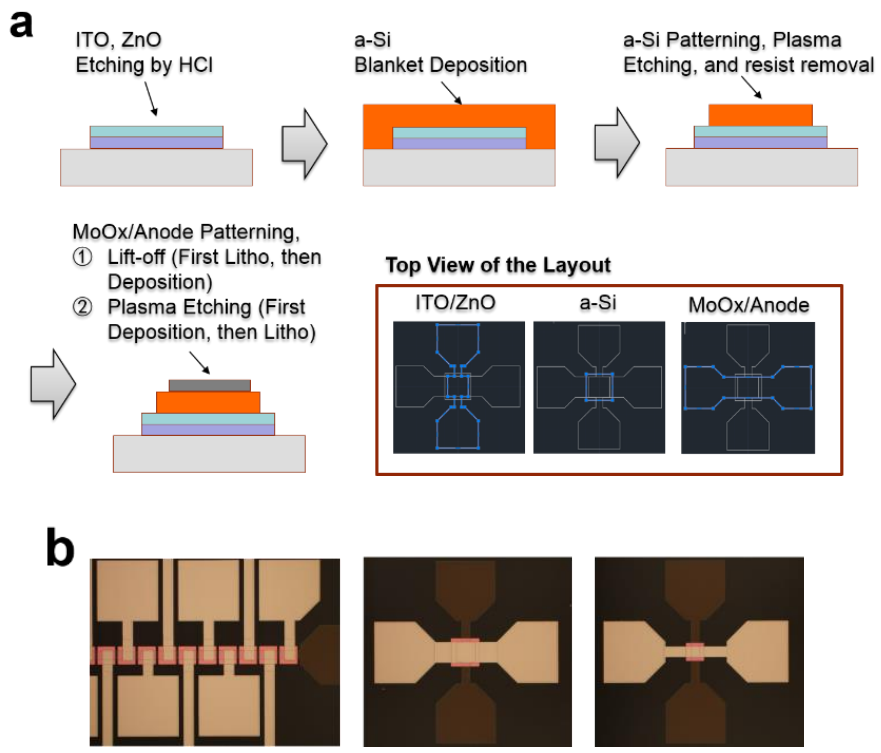

Figure 5.6 (a) Fabrication procedure and main layout design for the small area a-Si PDs (down to 50 um × 50 um). All the layers are patterned by photo-lithography processes, but with different etching methods, where ITO and ZnO layers are etched by HCl, a-Si layer is etched by RIE etching, and final top anode contacts is formed lift-off process or RIE etching. (b) The image of the a-Si PD devices, including the linear array and the individual devices with different areas.

IV characterizations for the small area inverted a-Si PD devices under darkness or under illumination (AM 1.5, 0.1 W/cm^2) are shown in Figure 5.7, where the device area are different (50 um × 50 um to 200 um × 200 um). The IV curves measured under darkness is depicted in Figure 5.7a with a log scale, quite proportional to the area, including those under reversed biases. The good proportionality reveals the uniformity of the devices, and the current leakage does not come from the random shortage sites caused by particle contaminations or improper experiment operations, which well agrees with the previous discussion for the hole leakage through the cathode contacts. The IV curves measured under illumination are depicted in Figure 5.7b with a linear

scale. The photo currents at zero-bias are also quite proportional to the device area. All of the curves reached the zero-current point at around 0.3 V (V_{oc} = 0.3 V), which is lower than the previous large area devices (1.4 mm^2, without photo-lithography processes), probable due to the possible surface modifications happened for ZnO or a-Si layers during the wet processes of the photo-lithography patterning, thus inducing the WF modification and the corresponding V_{oc} shift. However, the V_{oc} is not a critical parameter to the application of the a-Si PDs, and the current ratio under various illumination will be more important.

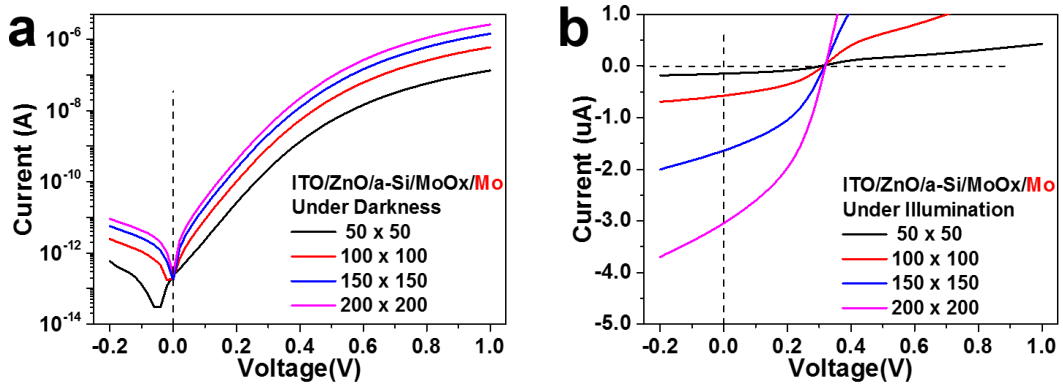

Figure 5.7 IV characterizations for the developed inverted a-Si PDs under darkness (a) and under illumination (AM 1.5, 0.1 W/cm^2) (b). The active area of the devices measured here is from 50 um × 50 um to 200 um × 200 um.

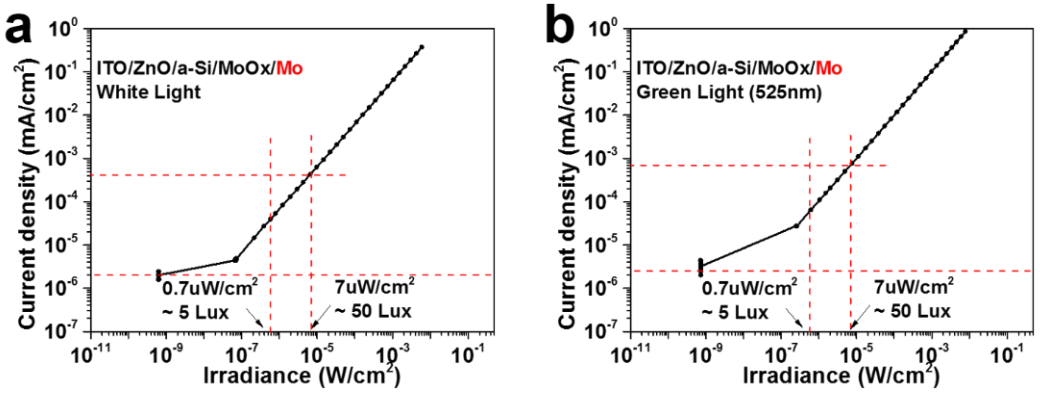

Figure 5.8 LDR characterizations for the small area a-Si PD with top Mo anode under white (a) or green (b) illuminations.

The LDR characterizations are illustrated in the Figure 5.8, under white or green illuminations. The big difference from the previous LDR results is the huge deviation

from the linearity of the current under zero-irradiance. That is because of the limitation of the equipment precision. The small device area means a proportionally decreased leakage current, which is easily beyond the equipment measurement capability. However, the current ratio under the illumination < 50 Lux is maintained higher than 2 orders, which is the basic requirement for the in-screen fingerprint sensing. Moreover, we can observe the upshift of the linear regime in the Figure 5.8b, compared to the Figure 5.8a, indicating a higher responsivity and EQE for the green light (peak wavelength = 530 nm).

It is very important to solve the deviation from linearity and measure the actual current leakage. We use the strategy of assembling 10s a-Si PD devices together, and measure the total leakage current or the total photo current, just to reproduce the linearity down to the zero-irradiance.

The layout of the new masks for the photo-lithography is shown Figure 5.9, which includes the region for the assembling arrays and the individual a-Si PD pixels. The device number in one assembling array is 10, 20, 40, 80, 100, respectively, and the number in the line of individual pixels is 40. All of the a-Si PD devices designed here are identical, with an active area of 50 um × 50 um. Each assembling array has its own anode and cathode test pad for hard probe needles, while the line of the individual a-Si PD devices has a common cathode with 3 test pads, and each a-Si PD has an individual anode test pad.

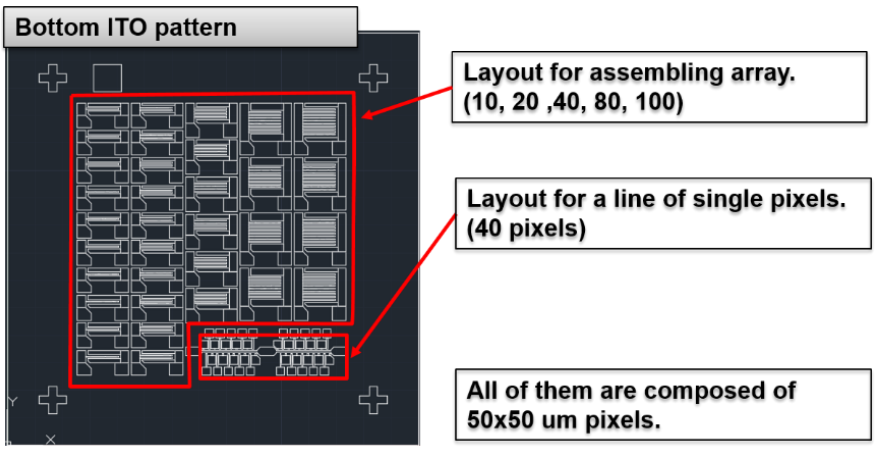

Figure 5.9 Photo mask layout design for the assembling arrays to measure the actual current leakage under darkness for the individual a-Si PD device with a active area of 50 um × 50 um.

In order to further restrict the possible hole leakage to the cathode, we increased the a-Si thickness to 120 nm and 180 nm to verify the influence of the a-Si thickness. Figure 5.10 illustrated the IV characterizations under darkness or illumination, for the a-Si PD devices with different assembling number. All of the currents under darkness or illumination are quite linear to the assembling number, indicating the good uniformity of the fabricated devices. The V_{oc} of different curves converges to 0.3 V, identical to the result shown in Figure 5.7. Comparing the lowest leakage current in Figure 5.10a and Figure 5.10b, the thicker a-Si layers do facilitate the restriction of the possible hole leakage, and the leakage is reduced by around 1 order after increasing the a-Si thickness from 120 nm to 180 nm.

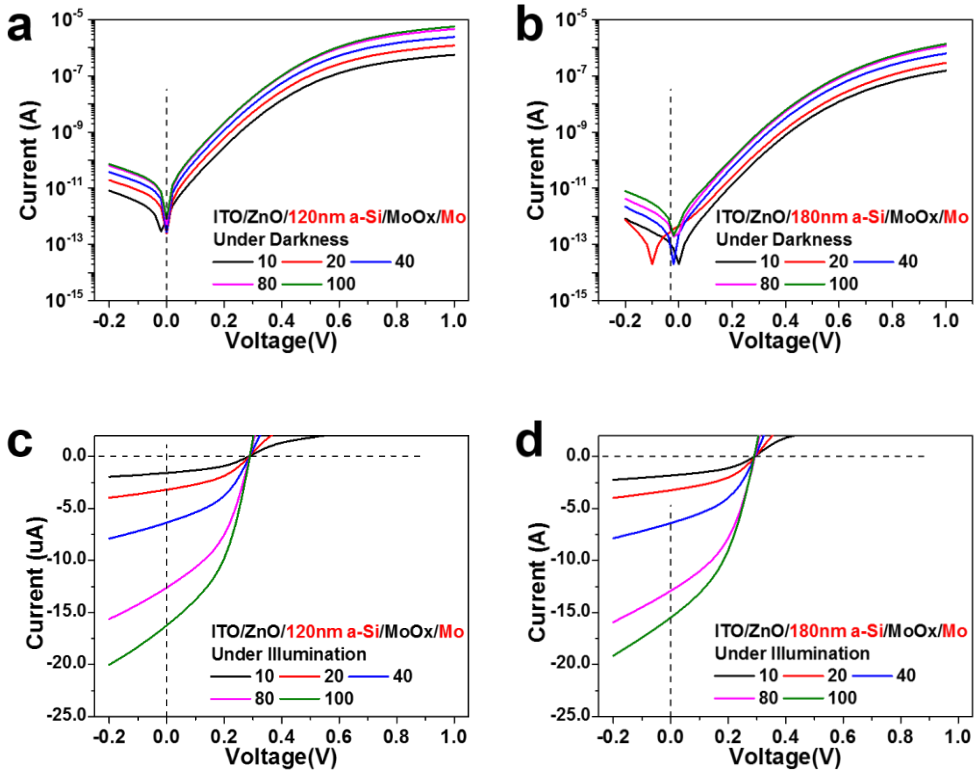

Figure 5.10 IV characterizations for the devices with different assembling number under darkness or illumination AM 1.5 (0.1 W/cm^2).

Sequentially, the LDR characterizations are obtained again to show the relationship between the linearity deviation and assembling number, as shown in Figure 5.11. The linearity get improved as the assembling number increased, since the total measured current gradually enters into the range of the equipment measurement capability.

Thicker 180 nm a-Si layer reduced the leakage current and further improve the linearity. As shown in Figure 5.11b, the obtained current ratio for the illumination < 50 Lux is around 4 orders, far beyond the basic requirement for the in-screen fingerprint sensing.

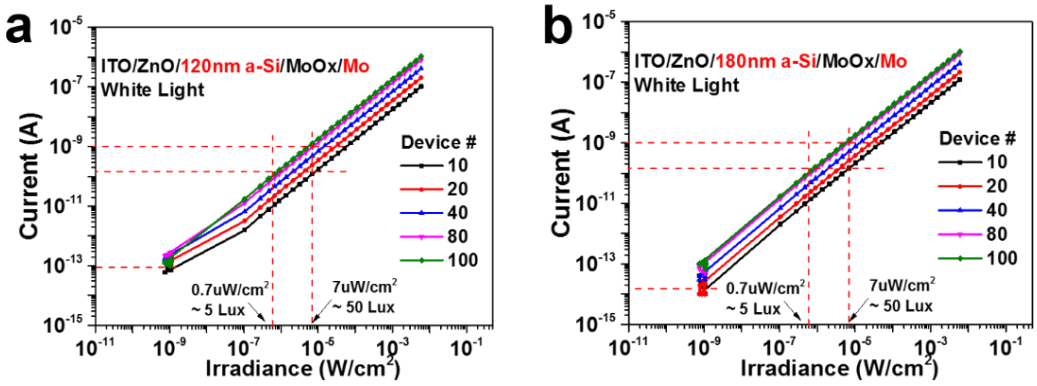

Figure 5.11 LDR characterizations for the a-Si PD devices under assembling numbers of 10, 20, 40, 80 and 100, respectively.

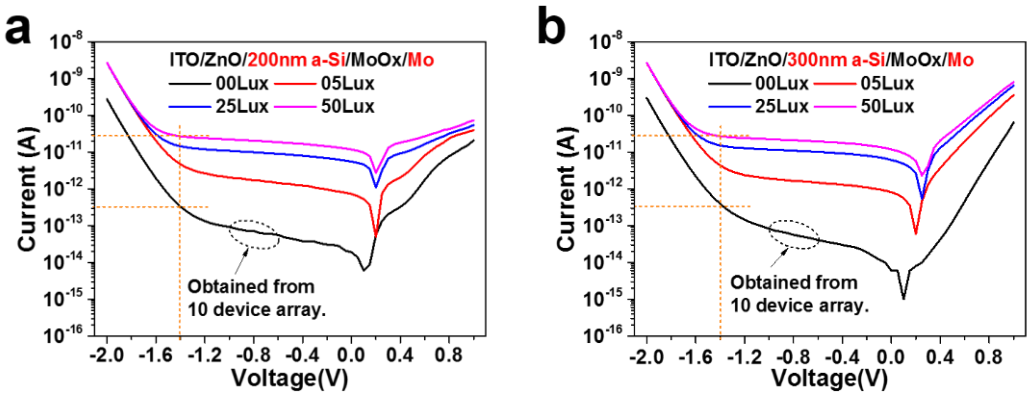

Figure 5.12 The leakage current under reversed biases for the a-Si PD devices with a-Si thicknesses of 200 nm (a) or 300 nm (b).

Furthermore, the thickness of a-Si continued to be increased to 200 nm and 300 nm in order to investigate the leakage current under reversed bias, as shown in Figure 5.12. The leakage current under zero-irradiance (darkness) is actually obtained from the assembling array of 10 devices. As we see, the dependence of the leakage on the reversed bias is greatly reduced, compared to those in Figure 5.10, which reveals that the thicker a-Si layer effectively increase the shunt resistance. The photo currents under 5, 25, 50 Lux are 8.1×10^{-13} A, 6.18×10^{-12} A, 1.19×10^{-11} A and 7.4×10^{-13} A, 5.54×10^{-12} A, 1.18×10^{-11} A for 200 nm and 300 nm a-Si, respectively, maintaining a good

proportionality to the illumination and pretty flat until they are overcome by the leakage current, as shown the final convergence around the reversed bias -1.8 V. The photo current for 300 nm a-Si is a little lower than those for the 200 nm a-Si, probably because of longer transportation beyond the diffusion distance and the corresponding increased photo carrier recombination. However, for the application towards the fingerprint sensing, the current ratio is more critical than the absolute photo current. As a result, the available reversed bias range for the current ratio > 2 orders under illumination < 50 Lux is increased to around -1.4 V, which give a good tolerance for the further peripheral circuit design.

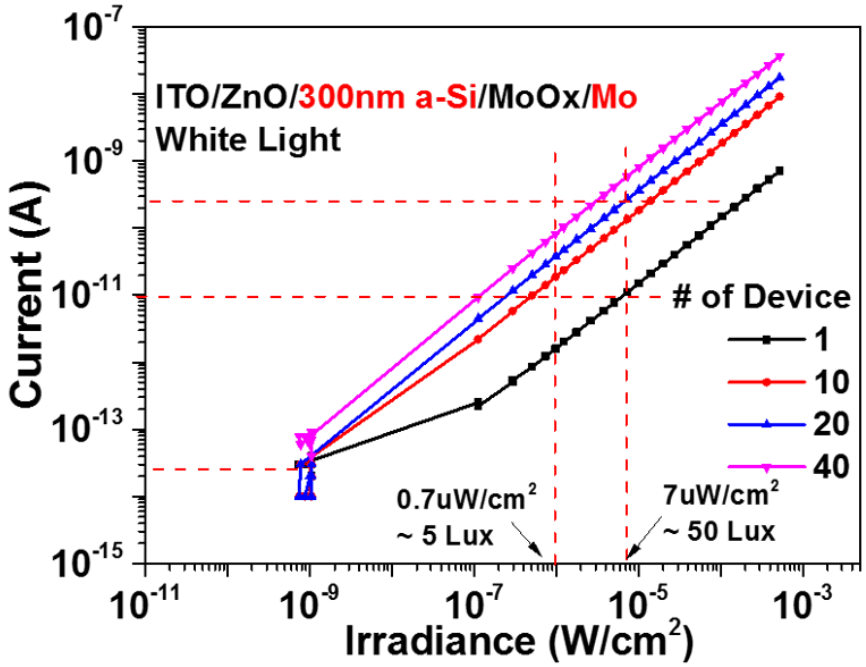

Figure 5.13 LDR characterizations for the a-Si PD devices with the a-Si thickness of 300 nm under assembling numbers of 1, 10, 20, 40.

The LDR is characterized for the devices with 300 nm a-Si layer under the assembling number of 1, 10, 20 and 40, as shown in Figure 5.13, where the photo current was obtained under zero-bias to maximize the current ratio. As we see, the linearity get improved as the assembling number increased, since the total measured current gradually increase to match the the equipment measurement capability. The current ratio for the illumination < 50 Lux is still maintained at around 4 orders, similar to the previous results. Considering the leakage under the reversed bias and the effective

linearity, we proceed with the further fabrication of such devices for the integration with the LTPS TFT backplanes.

As shown in Figure 5.14, the completed a-Si PD matrix on the TFT backplane includes 160 × 130 pixels, and it is semi-transparent to the naked eyes since each pixel area includes the transparent region for the backlight, and the opaque region for the a-Si PD. The microscopic images for a small area or individual devices in the a-Si PD matrix are shown in the Figure 5.14c and Figure 5.14d. The active area of each a-Si PD is 20 um × 50 um, comparable to that of a TFT-LCD pixel. The a-Si PD is only covering part of one pixel region, the rest are transparent through the TFT backplane, which leaves a window for the backlight to go through the liquid crystal layer and the color filters mounted on the front plane. The completed TFT backplanes integrated with the a-Si PDs are ready for the future IC chip bonding and the corresponding image acquiring and recognition for the in-screen fingerprint sensing.

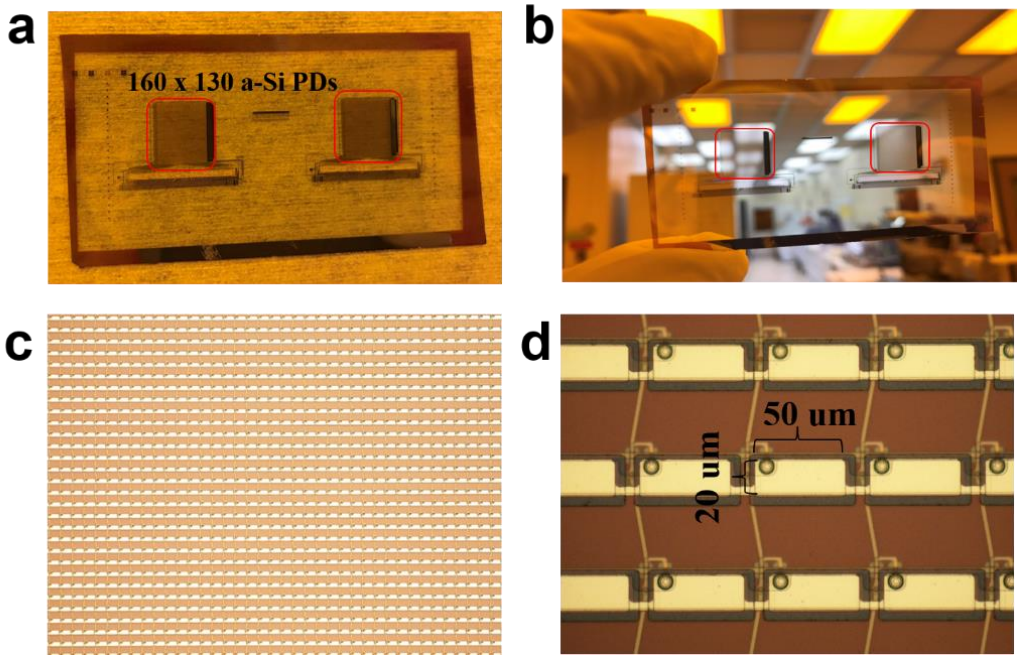

Figure 5.14 Integration of the a-Si PD matrix with the TFT backplane for the TFT-LCDs. (a, b) The a-Si PD matrix fabricated on the TFT backplane (c, d) The microscopic images of the a-Si PD matrix and the dimension of individual device.

5.5 Conclusion

The inverted a-Si PD with bottom cathode contact interlayers are developed and characterized to fulfill the requirements of the architecture design for fingerprint sensing. The ZnO and MoO_x are employed as the ETL and HTL. The current leakage and LDR get analyzed with different a-Si thicknesses and device areas. The a-Si PD arrays with pixel area are fabricated based on the photo-lithography processes in order to extract accurate current leakage and LDR. Finally, the optimized a-Si PD arrays are fabricated on the LTPS TFT backplanes.

Chapter 6 Photo Excited Artificial Synapses Based on Amorphous Silicon and Polyethylenimine Interfaces

Abstract

Innovative artificial synapses were demonstrated based on the interactions between the amorphous silicon and polyethylenimine interlayers. The hysteresis and timing dependent plasticity of the artificial synapses can be excited by light illumination, coupled with electrical pulse stimuli. The device design is promising to serve as fundamental elements for neuromorphic functionalities towards the simultaneous visual information process in large-area electronics or IoT.

6.1 Introduction

As the Internet of Things (IoT) is vigorously developing, huge amount of data are being produced every second and moment, which generates a demanding requirement for the data processing simultaneously on site.[141-143] Power and computation capability of the IoT systems are limited for one individual unit used in data acquiring because of the cost or space issue for a mass deployment, thus they have to be equipped with a high computation speed under a low power consuming. The neuromorphic network / computing are drawing extensive research and engineering interests due to its excellent capabilities of mimicking human intelligence and the brain functions of highly efficient massive parallel information processing.[144]

In order to promote the practical application for the neuromorphic network, various artificial synapses were developed as the fundamental elements. Prof. Joshua Yang Group developed memristors with diffusive dynamics to emulate the plasticity in

the accumulations and extrusion of Ca^{2+} ions triggered by pre- and post- spikes in the bio-synapses.[145] They systematically characterized the transient response and the corresponding retention for the memristor based on Au/ SiO_xN_y:Ag, MgO_x:Ag, HfO_x:Ag/ Au device designs, and the conductive filaments are composed of the Ag ions. It is found that the dynamic properties of Ag ions are quite different from the previously reported memristors based on migrations of Ag ions, because the migration, filament breaking and clustering of Ag ions are quite fast in the spontaneous relaxation, and the retention can be well maintained just for 10s ms. Therefore, the dynamic properties of Ag ions in the dielectric films are quite different, according to the specific localized environments. Prof. Salleo employed another material system to develop low-voltage artificial synapses.[146] Flexible organic electrochemical devices were fabricated for the neuromorphic computing, where the conductivity of backbones in PEDOT:PSS mixed with PEI solution can be modulated by the cation injection from the electrolyte gate dielectric layers.

These works are using single device to mimic bio-neuromorphic behaviors instead of the integration of multiple various electrical components, which will further facilitate the system miniaturization and power efficiency improvement. However, people usually focus on the hysteresis of the artificial synaptic devices triggered only by the electrical signals, lacking the involvement of other physical stimuli.[147-152] Here we report on innovative photo excited artificial synapses (PEAS) enabling the integration of the neuromorphic functionality for the visual information process simultaneously on site in IoT systems, meanwhile it opens the possibilities for artificial synaptic devices incorporating the capability of sensing moistures, light intensity and so on. The obtained PEAS is derived from the amorphous silicon (a-Si) photodiode structure by employing pure Polyethylenimine (PEI) as cathode contact interlayer. It is found that the light illumination is critical to IV hysteresis, and the a-Si / PEI interfaces is able to trap the photo-generated carriers, thus modulate the dipole moment across the PEI layer and the corresponding the overall current response / plasticity.

6.2 Device Structure and Fabrication

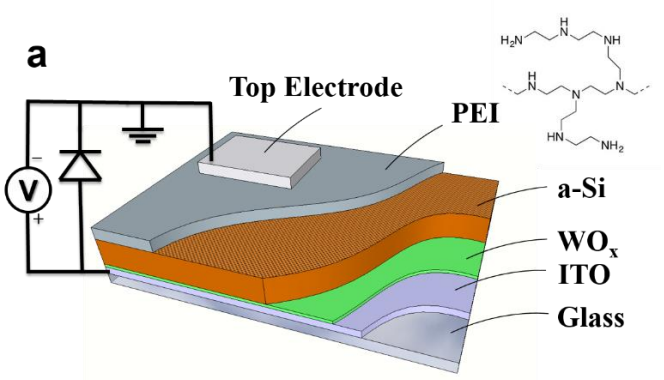

Figure 6.1 Schematic illustration of the PEAS device design, equivalent circuit and the chemical structure of the polymer PEI (inset).

The PEAS devices were fabricated based on the a-Si photodiode device design, as shown in Figure 6.1a. Indium Tin Oxide (ITO) coated glass pieces were used as substrate and transparent anode. Then Tungsten Oxide (WO_x) was used as the anode contacts and hole transportation layer (HTL), which is around 30 nm obtained from the oxygen oxidation from the thin W metal by Rapid Thermal Processing. The intrinsic a-Si layer was deposited by PECVD with a rate of 0.8 Å/s at 260 °C, as the photo-active layer to absorb the incident light illumination and generate the electron-hole pairs. In order to enhance the charge storage along the a-Si / PEI interface, 5 nm Ag was deposited by thermal evaporator on the a-Si layers before spin-coating PEI, to form condensed and isolated Ag nano-particles. The PEI solution was prepared by diluting the pure PEI purchased form Sigma Aldrich to 5 wt% with the solvent of 2-Methoxyethanol at first, then to the required concentration from 0.4 wt% to 1.0 wt%. The prepared PEI solution was spin-coated on the a-Si layers in the glovebox at 3000 rpm for 40 s, followed by annealing at 100 °C for 15 min. The final cathode metal is 100 nm Ag, deposited by thermal evaporator with shadow masks to form the separated cathode metal islands.

The fabricated samples will be placed on a holder mounted with LED unit or an

optical fiber coupled to solar simulator. The light intensity of LED unit was controlled by Keithley 2400 source-meter, and the optical fiber can be opened or closed manually. All the measurement were conducted under room temperature and air ambient.

6.3 IV Sweep Hysteresis and Mechanisms

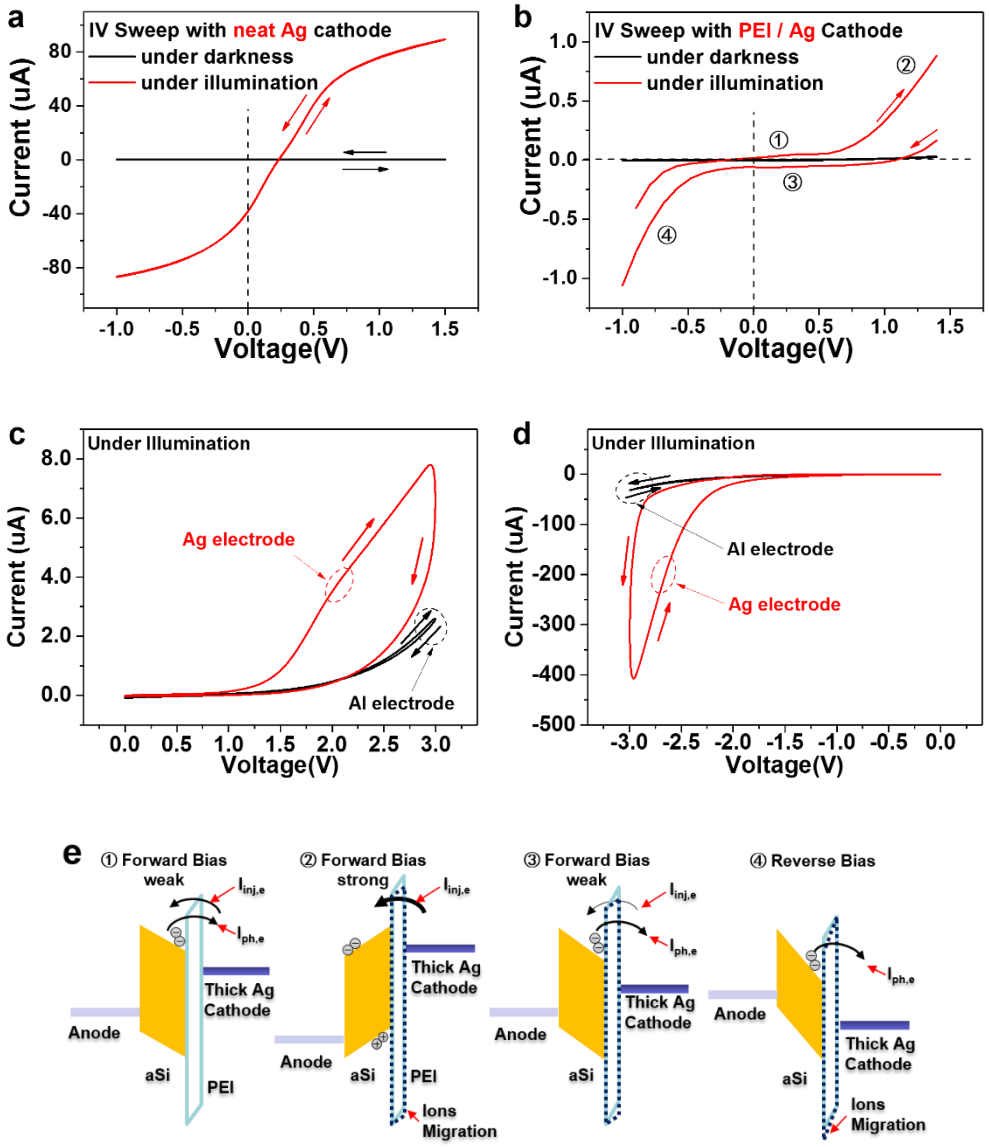

Figure 6.2 IV characteristics and corresponding hysteresis for the device (a) with neat Ag cathode and (b) with PEI/Ag cathode, under darkness or under illumination AM 1.5, 0.1 mW/cm^2). (c, d) Positive or negative IV sweeps for neat Ag and Al electrodes under illumination. (e) Schematic illustration for the proposed mechanism of the hysteresis obtained in the IV sweep characterizations under illumination.

The WO_x used as HTL in the devices is also a typical active material in memristors because of its steadily substoichiometric feature and the oxygen vacancies (V_{ox}).[153, 154] Control samples were fabricated with neat Ag cathode in order to verify whether the V_{ox} in the devices can contribute the IV hysteresis. From the additional Auger Electron Spectroscopy analysis, the W:O ratio is close to the 20:58 and there is a ultrathin transitional O deficiency layer along WO_x/aSi interface. As shown in Figure 6.2a, the current response of the control samples remains negligibly low under darkness, and it has pretty good anode and cathode contacts to support decent current flow and opto-electronic conversion efficiency under illumination (AM 1.5), importantly no hysteresis compared with those of ITO/WO_x/a-Si/PEI/Ag. It revealed that the electric field across the WO_x layer is not that large enough to stimulate the migration of V_{ox}, because of the high resistivity of a-Si layer where the electric field mainly drops.

The PEI interlayer is around 40 nm, working as an insulator at the cathode contacts, blocking the electron injection from the cathode and photo-generated electron collection to the cathode, which will amplify minor interactions between PEI and its adjacent interlayers. As shown in Figure 6.2b, it generates a much higher hysteresis under illumination, compared with that under darkness. Under illumination, the photo generated electron-hole pairs are produced in the a-Si layer, which will form electron or hole photo current ($I_{ph,e}$, $I_{ph,h}$), collected by the cathode or anode, respectively. From our previous works, we found that the WO_x can form good anode contacts with a-Si, therefore the cathode contact is the main limitation factor and dominating the overall current response. Further analysis will focus on the carrier transportation near the cathode contacts.

The cathode contact interlayer, PEI, is a polymer with high density of amine groups, which could be protonated and induce dipole to change the workfunction (WF) of electrode.[60] The possible movement of the protonated amine groups in chains or branches connected to the PEI backbones may induce additional dipole change and modulate the current response. Moreover, the Ag electrodes are popular electrodes for the memristors because of the high mobility and migration of the Ag ions.[145, 155]

Control samples with PEI/Ag or PEI/Al cathode contacts are measured to clarify the obtained hysteresis is dominated by the movement of protonated amine groups or the migration of Ag ions. The Al electrodes are employed here because of its low WF which is supposed to facilitate the cathode contacts, meanwhile it is assumed that the Al ions or atoms will not diffuse into the PEI interlayer since no related works can provide sufficient verifications by now. As shown in Figure 6.2(c,d), the hysteresis for the samples with PEI/Ag contacts is much greater than that for PEI/Al either in positive or negative sweeps, which revealed that the migration of the Ag ions in PEI dominates the hysteresis, while the protonated amine groups only induce a negligible hysteresis.

The obtained hysteresis is basic behaviors for the PEAS devices, and the related mechanisms are proposed, as illustrated in Figure 6.2e. The polarity of the current response near the zero voltage was flipped from positive to negative during the forward and backward sweeps (0 V to 3 V to 0 V), as shown in Figure 6.2b. Therefore, whole sweeps were divided into 4 segments, labeled by circled 1 to 4. From the weak forward bias ① to the strong forward bias ②, the electron injection current ($I_{inj,e}$) is balancing and finally overcoming the photo-electron current ($I_{ph,e}$), therefore the net current is positive and keeps increasing. During this period, the Ag ions in PEI migrate towards the PEI/Ag interface, which will reduce the overall dipole and increase the barrier for $I_{inj,e}$. Therefore in the weak forward bias ③, the $I_{ph,e}$ gradually surpasses $I_{inj,e}$, resulting in a net negative current. Finally, in the reverse bias ④, the Ag ions will migrate towards the a-Si/PEI interface, which increases the overall dipole and facilitates the collection of $I_{ph,e}$, meanwhile the conductive pathways composed by Ag ions stretching from the Ag electrodes to the a-Si surface will further improve the conductance.

The hysteresis were analyzed based on the dipole moment modulated by the Ag ions in PEI layer, then more detailed conduction mechanisms still need to be analyzed for each branch in the initial positive and negative IV sweep curves. As shown in Figure 6.3(a-d), the voltage-current relationships were fitted by the various conduction models.

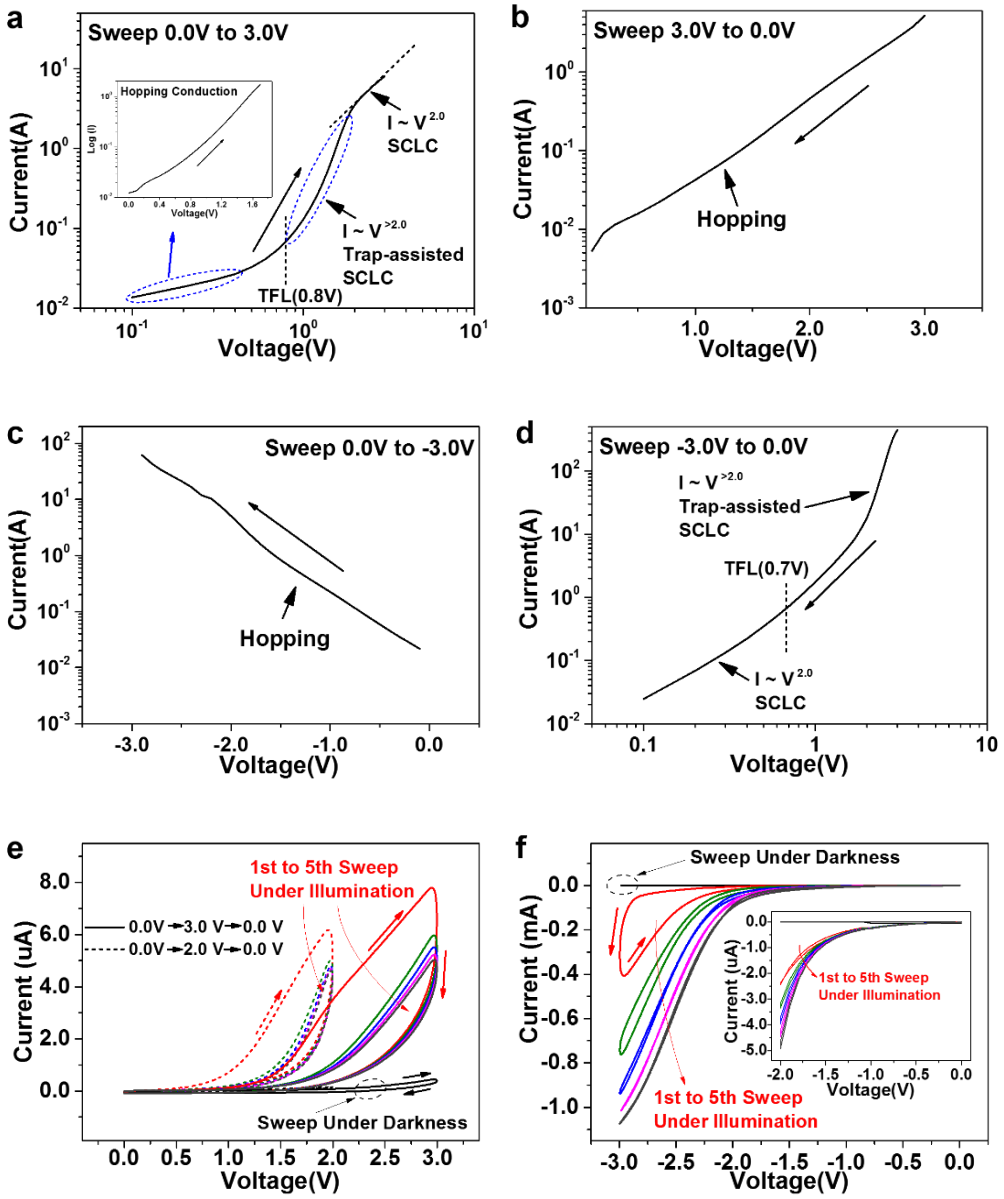

Figure 6.3 The conduction mechanism analysis for initial sweeps, (a) 0.0 V to 3.0 V, (b) 3.0 V to 0.0, (c) 0.0 V to -3.0 V, (d) -3.0 V to 0.0 V. Further consecutive IV sweeps, where (e) is for positive sweep up to 2 V or 3 V, (f) for negative sweep down to -2V (inset) or -3V.

At the beginning of the branch from 0.0 to 3.0 V, the electrons are injected to the a-Si layer through hopping processes, indicating the deep trap states facilitate the charge transportations, as shown in Figure 6.3a. As the voltage increases to 3.0 V, the energy level gap between conduction band (CB) of a-Si and WF of cathode is reduced, then electrons will be injected through the trapping and releasing through the shallow traps

and the transportation is dominated by Space Charge Limited Current (SCLC), where the Trap Filled Limit (TFL) current started at 0.8 V, corresponding to the trap density of 1.41×10^{10} / cm^3. During the backward sweep from 3.0 to 0.0 V, the dipole in PEI was reduced, and the energy level gap between CB of a-Si and WF of cathode was enlarged, and the hopping conduction becomes dominant again, indicating the transportation through the deep states, as shown in Figure 6.3b. As the voltage continues to be reduced into the negative side (0.0 to -3.0 V), the Ag ions in the PEI layer will migrate towards the a-Si/PEI interface, which creates additional trap states. The electron transportation is still dominated by the hopping processes, but the current is much higher than that for the positive backward branch (3.0 to 0.0 V), as shown in Figure 6.3c. In the negative backward branch (-3.0 to 0.0 V), the dipole induced in PEI is increased due to the Ag ion migration towards a-Si/PEI surface, and SCLC is the dominant electron transportation model, where the TFL current started at -0.7 V, corresponding to the trap density of 1.24×10^{10} / cm^3, very close to that in the positive sweeps, as shown in Figure 6.3d.

Furthermore, we also compared the multiple consecutive IV sweep under ±2.0 V or ±3.0 V, as shown in Figure 6.3(e,f). The sweeps showed continuous conductance modifying process, which will facilitate to mimic the behavior of neuron synapses. Under the positive sweeps, the forward branches continue to decrease, behaving like depression in neurobiology. However, the backward branches almost follow the same curve, indicating the hopping process through the deep states get less influenced by the dipole modulations. Additionally, the overlapping of these loops indicates that the device has limited retentions. On the other hand, under negative sweeps, the current responses keep increasing, behaving like potentiation in neurobiology. However, the hysteresis is reducing as the sweeps continue, indicating the saturation of Ag ions migration and accumulation along the a-Si/PEI interface, and the saturation of dipole moment modulation and the extraction for photo-current or the leakage current.

6.4 Current Response under Pulse Stimuli

In bio-neurobiology, the synapses are stimulated by the pulses (spikes) coming from pre/post- axons or dendrites instead of certain potentials or sweeps. Therefore, the current response under the pulse stimuli were characterized in order to mimic the bio-synapse response to the spikes. As shown in Figure 6.4a, the current response sequence for 20 cycles were obtained, where a complete cycle includes a positive pulse (3 V, 100 ms), a reading (0.5 V), a negative pulse (-3 V, 100 ms) and another reading. The pulses were applied under darkness or illumination (AM 1.5), but the reading only under darkness. As we see, the current response under illumination is greater than those under darkness, especially for the current response after negative pulses. Besides the amplitude of the current responses, it is also necessary to pay attentions to the polarity. The current response is negative after positive pulse, but it is positive after negative pulses.

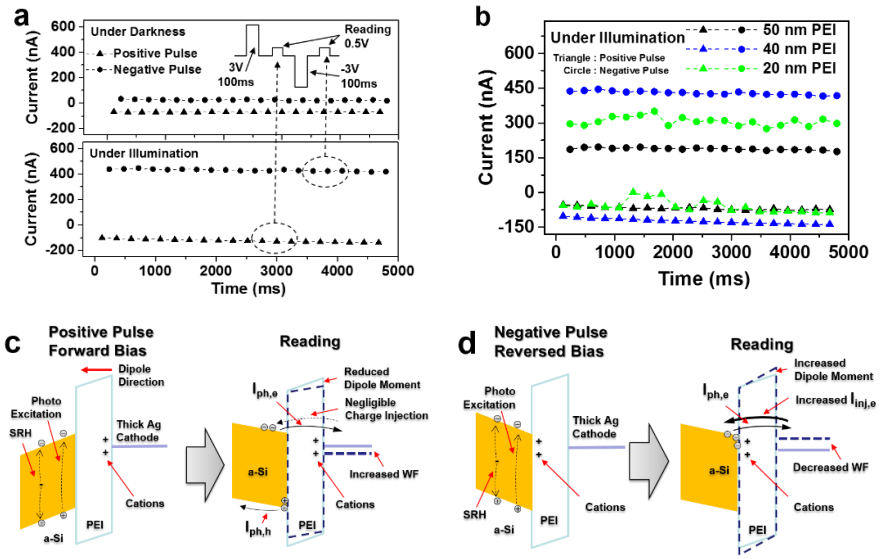

Figure 6.4 (a) Current response after 100 ms pulse stimuli under darkness or illumination, and the inset is a complete cycle (positive pulse, reading, negative pulse, reading), where the pulse is applied under darkness or illumination, and reading is only conducted under darkness. (b) The comparison of current responses for the PEAS devices with different PEI thicknesses (20 nm, 40 nm, 60 nm). (c, d) The proposed mechanisms for the current response after positive or negative pulse stimuli.

Considering the reading under darkness and the time gap between the stimulus pulses and the reading voltage, more carrier generation, trapping and releasing mechanisms need to be involved in the analysis for the current response, compared to that under continuous sweeps. Under light illumination, photo-generated carriers are produced, while under darkness, the additional carriers will be also generated by the Shockley-Read-Hall (SRH) processes through the mid-gap states, as shown in Figure 6.4c. Both of the illumination and electric field will facilitate the carrier generation in the a-Si layer. As discussed above, the Ag ions migrate to the PEI/Ag interface under forward biases, and the dipole across the PEI layer is reduced, therefore the carrier injection from the cathode metal to the a-Si was restrained. The negative current response is obtained mainly due to the collection of the carrier generated in the a-Si layer. Under illumination, the photo excitation is dominant in the carrier generation, while the SRH process is dominant and comparable under darkness, which verifies the comparable but slightly lower current responses after positive pulses under darkness. On the other hand, the positive current responses are obtained after negative pulses, which is due to the enhancement of carrier injection from the cathode, as shown in Figure 6.4d. Under negative pulses Ag ions migrate towards the a-Si/PEI interface, increasing the dipole moment induced in PEI layer, which is further strengthened by the light illumination because of the increased conductivity in a-Si layer and corresponding increased electric field across the PEI layer.

The PEAS devices with different PEI thicknesses were also fabricated and characterized, as shown in Figure 6.4b, where the current response for 20 or 50 nm PEI were lower than that for 40 nm PEI. Thicker PEI increases the barrier at cathode side, and reduces the carrier injection and collection. However, thinner PEI means a shorter interaction distance and a lower moment of the electrical dipole induced in PEI layers, which is not helpful to facilitate the carrier injection. Thinner PEI also means a shorter transportation distance for carriers generated in a-Si layer to cathode metal, which reduces the quantity of the carriers trapped in a-Si layer or a-Si/PEI interface, and results in a lower negative current after the positive pulses.

The a-Si layer is the photo-active material in the PEAS devices, and the relationship between the a-Si thickness, light intensity and current response were characterized, as shown in Figure 6.5. The thicknesses of a-Si used here are 20 nm, 60 nm, and 120 nm, and the PEI is 40 nm. Each measurement sequence includes 20 cycles, under the different light intensity exponentially increasing from the estimated 2.5×10^{-8} to 0.5 W/cm^2. It is found that the current response arises as the light intensity increases, but it commonly started from around 1.7×10^{-4} W/cm^2 and saturated at 5×10^{-3} W/cm^2. The lower bound is probably due to the recombination rate for the carriers generated in a-Si layer, while the upper bound may be due to the capability of charge trapping and the saturation of the dipole moment modulation for the PEI layer. Thicker a-Si layer can increase the light absorption and the photo-generated carriers, however, it means a higher serial resistance and a lower current response. Thinner a-Si layer strengthen the electrical field across the PEI layer, which facilitates the migration of Ag ions even under darkness, therefore reducing the current response ratio under darkness or illumination. The optimal or balanced results for a higher current ratio is 60 nm a-Si and ±3 V pulse voltage.

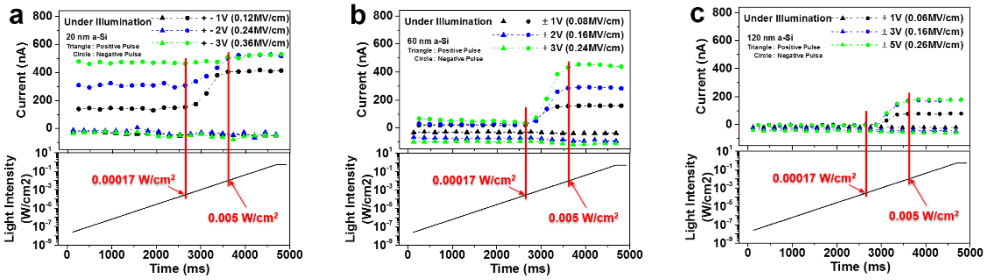

Figure 6.5 The current response for pulse stimuli, under increasing light intensity, different pulse voltage, and different a-Si thicknesses, 20 nm (a), 60 nm (b), 120 nm (c). Each sequence is coupled with the light intensity exponentially increasing from 2.5×10^{-8} to 0.5 W/cm^2.

6.5 Response Decay and Timing Dependent Plasticity

Besides the amplitude of the current response after pulse stimuli, the decay behavior are also important for the further applications of mimicking bio-synapses. The current response after pulses under illumination are measured and fitted based on a typical

stretched-exponential function of time, as shown in Figure 6.6c. Current response after a negative pulse is dominated by the charge injection from cathode, and the decay behaviors are determined by the re-distribution of Ag ions and the corresponding relaxation of the dipole moment modulation. On the other hand, the current response after a positive pulse is mainly from the collection of the carriers generated in the a-Si layer, and the decay depends on the relaxation of the trapped carriers. As we see, the time constant is 154 ms and 100 ms for the current response after a negative or positive pulses, respectively, which is comparable with the decay or relaxation for EPSP and IPSP of the bio-synapses.[156, 157]

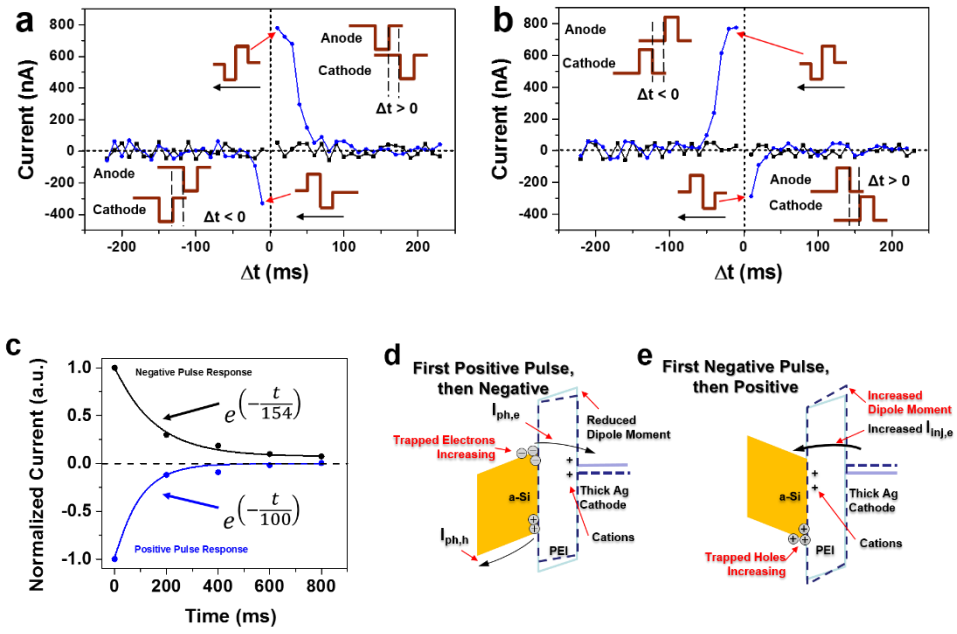

Figure 6.6 Timing dependent plasticity for the pre- / post-spikes without overlapping, under darkness (black) or illumination (blue). Pre- / post-spikes are identical, and both are negative (a) or positive (b). (c) Decay characteristics for the normalized current response after negative or positive pulses. (d, e) The proposed mechanisms for the timing dependent plasticity highly related to the charge attractions, carrier trapping and releasing.

Based on the obtained decay behavior, the timing dependent plasticity was further characterized for the pre- / post- spikes with different timing gaps, as shown in Figure 6.6(a,b). The pre- / post-spikes are identical (100 ms, +3 or -3 V) and applied to the anodes and cathodes, respectively. Here, Δt is used to show the separation for the pre-

/ post-spikes, defined as the time difference between the leading edge of the pre-spike and the tailing edge of the post-spikes, or vice versa.

Under darkness, the current response is very small and kind of independent of the net pulse, resulting in no plasticity, however, the illumination significantly triggered the plasticity of PEAS devices. $\Delta t > 0$ means the pre-spike goes earlier than the post-spike, while $\Delta t < 0$ means the post-spike goes earlier than the pre-spike. When Δt approaches to 0.0 ms, the net pulse is pre-spike (post-spike) immediately followed by post-spike (pre-spike), and the corresponding polarity gets flipped immediately when the highest current response is obtained. As $|\Delta t|$ increases, the separation of pre- / post-spikes becomes bigger, and the current responses gradually declines, which follows the asymmetric hebbian or asymmetric anti-hebbian learning rules, just like the timing dependent plasticity in neurobiology.

When both of the pre- / post- spikes are negative (-3 V), the asymmetric hebbian learning rule can be produced, as shown by the blue lines in Figure 6.6a, while if the spikes are positive (+3V), the asymmetric anti-hebbian learning rule can be produced, as shown in Figure 6.6b. Both of the highest negative current response comes from the positive-negative flipping net pulse, which is due to the enhancement of the carrier generation and trapping. The illumination produces a great amount of electro-hole pairs, and the positive pulse facilitates the hole trapping in a-Si layer or along the a-Si/PEI interface. During the releasing of the trapped holes, the negative pulse shift the band and facilitate the electron trapping, especially under the electrical attractions between the trapped holes and electrons, as shown in Figure 6.6d. Finally, the total current for the carrier collection to the anode and cathode are increased, which will be gradually declined as the separation of the spikes increases. On the other hand, both of the highest positive current response comes from the negative-positive flipping net pulse, which is due to the enhancement of the carrier injection. Under the negative pulse, the Ag ions migrate towards the a-Si/PEI interface, and the dipole moment is increased, while the following positive pulse facilitates the trapping of holes along the a-Si/PEI interface, the dipole moment is further increased, and the carrier injection is further strengthened.

6.6 Conclusion

By incorporating the a-Si/PEI interface, Photo Excited Artificial Synapses were achieved. Coupled with electrical pulse stimuli, light illumination will trigger the IV hysteresis and timing dependent plasticity. These features is quite significant to enable the integration of the neuromorphic functionality, especially for the visual information process simultaneously for large-area electronics or IoT.

Chapter 7 Highly Transparent Resistive Switching Devices Based on Optically Optimized Dielectric / Metal / Dielectric Structure

Abstract

In the era of Internet of Things (IoT), transparent electronics are facing more potential opportunities and advancing towards the integration with various optoelectronic devices. In order to facilitate the instant and on-site data processing, we achieved transparent resistive switching devices to promote neuromorphic computing for the transparent electronic systems. The devices are based on ultrathin doped Ag films and optically optimized dielectric/metal/dielectric structure. The overall transparency is higher than 80%, and the device conductance modulation is found to be analog and continuous. Under consecutive pulse stimulus with different durations, the device finally stabilized at different conductance levels, acting as different potentiation or depression levels in terms of neuromorphic functionalities.

7.1 Introduction

As the rapid development of the transparent display panel and near-eye displays, the scientific researchers and industrial engineers are showing remarkable attentions to the extensive transparent electronics, such as transparent OLED, transparent transistors, transparent solar cell devices, including the transparent amorphous silicon (a-Si) decorative solar cells[43, 47, 49, 158, 159]. After scrutinizing the active interlayers of these devices, the fabrication of electrodes with high transparency and high conductivity is the crucial step. Under such circumstances, various transparent electrodes are being developed such as PEDOT:PSS, transparent conductive oxide

(TCO), carbon-based nano-materials, metal meshes, silver nanowires.[47, 92-98] Among these alternative candidates, the ultra-thin doped silver films are showing its unique promising advantages of ease-deposition, low-temperature process, potentially flexible profile, and so on.[160-162] On the other hand, based on the ultra-thin silver films, the Dielectric/Metal/Dielectric (DMD) sandwished structure will further improve the optical transparency. In this sandwished design, many metal oxide is often serving as the dielectric materials, such as Molybdenum Oxide (MoO_x), Tungsten Oxide (WO_x) or so, which will also facilitate the improvement of the electrical performance of the related optoelectronic devices.[163, 164]

Now in the era of Internet of Things (IoT), transparent electronics are advancing towards versatile perspectives, being integrated with various optoelectronic devices and producing "System-on-Glass".[165] Transparent electronics is enabling the integration of intelligent functionalities with the display technologies or architecture exteriors. In order to achieve instant data processing for these systems, neuromorphic computing on glass will become powerful methods, especially based on analog resistive switching devices. The work we are showing here is to investigate the possibilities of neuromorphic computing for transparent electronics. Incorporating the ultra-thin doped silver films and the DMD structure, the resistive switching devices were achieved not only with a high transparency, but also revealing the analog switching behavior due to the migration of metal ions from the metal electrodes.

7.2 Device Structure and Fabrication

The device architecture schematic was shown in Figure 7.1a, where WO_x was employed as the main active material for the resistive switching devices. The ITO coating glass pieces were used as substrates, and the ITO patterns were formed by photo-lithography and followed by being etched in hydrochloric acid (HCl) for 4 min. The ultrathin (12 nm) W films were blanketly deposited by DC sputtering, and 30 nm WO_x films were obtained from the oxidation of the W films by annealing in oxygen atmosphere under 375 °C for 1 min. The top electrodes is 8 nm Cu-doped-Ag (Cu:Ag)

film, deposited by co-sputtering, where the Cu:Ag ratio was optimized to be 0.03:1. The top electrode patterns were prepared by photo-lithography and the lift-off. Typical cross-bar architecture was used to achieve the overlapping of the top and bottom electrodes, and form the active device area defined by the the overlapping area (3 um x 3 um). Finally, the 65 nm Al_2O_3 antireflective coatings were deposited on top of the devices by thermal evaporation, to further increase the overall transparency.

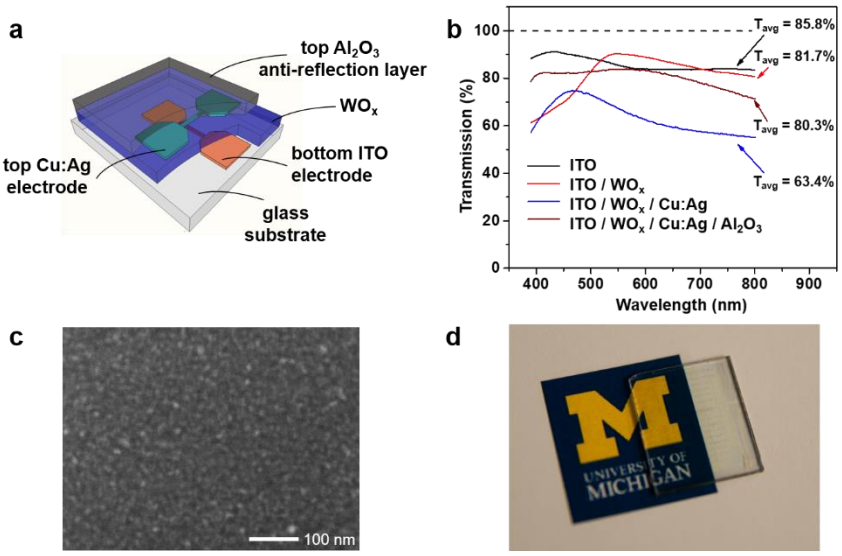

Figure 7.1 (a) The schematic of the resistive switching devices, fabricated from ITO substrate, deposition of thin W metal films and following oxidation, then deposition of ultrathin doped Ag films and the top Al_2O_3 anti-reflection layer. (b) The transmission spectrum for different stacked layers, from pure ITO substrate to the finalized ITO/WO_x/ultrathin doped Ag/Al_2O_3. (c) SEM characterization of the Cu doped Ag films with a scale bar of 100 nm. (d) The demonstration of the high transparency for the sample placed on the University of Michigan logos.

As shown in Figure 7.1b, the transmission spectrum for different stacked layers were measured, and the average transparency was calculated based on the spectrum of the wavelength range from 400 nm to 800 nm. As we see, the average transparency for neat ITO substrates are 85.8%, and reduce to 80.3% and 63.4% after deposition of WO_x layers and Cu:Ag electrodes, due to the increased optical absorption of the interlayers and reflection from the metal/air interface. In order to restrain the reflection and increase the overall transparency, optical simulations were conducted based on the transfer-matrix method. The optimized thickness for the Al_2O_3 anti-refection layer is

65 nm, leading to the transparency improvement by 18.3%, up to 81.7%, as shown in Figure 7.1b.

The thickness of the Cu:Ag films we were using here is 8 nm, with the sheet resistance of less than 20 ohm/sq. As shown in the SEM characterizations obtained by Hitachi SU8000, the surface morphology of the Cu:Ag is very continuous and smooth. The morphology for ultrathin neat Ag films is not stable and has a tendency of evolving into discontinuous islands in air.[161] The doping of Cu into the Ag film by co-sputtering is revealed to be an effective method to restrain the evolution of neat Ag films into island-like morphologies, leading to higher conductivity and transparency. Figure 7.1d shows the corresponding overall transparency of the real samples on top of the University of Michigan logo.

7.3 IV Sweeps for the Devices Based on Ultrathin Doped Metal Films

The WO_x can be fabricated by different methods, and commonly used as active materials for the resistive switching devices, because of conductive filaments formed by the migration of the oxygen vacancies (V_{ox}).[153, 154] The V_{ox} can be generated by deficient oxidation of W films or out-diffusion of oxygen atoms from WO_x films. Moreover, the V_{ox} are positively charged and accumulate along the interface to the top electrode in the WO_x films. On the other hand, the metal electrodes are often used as the ion source to achieve the abrupt or analog conductance modulation for the memristors or artificial synapses, due to the formation of conductive filaments induced by the migration of metal ions from the top electrode.[145] Therefore, in the resistive switching devices fabricated in our work, the migration of the V_{ox} and metal ions will follow the same direction under same electric field, which means both of them will migrate to the bottom electrode if a positive voltage was applied to the top electrode. The overall conductance change or hysteresis will be attributed to the complicated processes highly related to the migration of V_{ox} and metal ions. In the following, the IV sweep behaviors are compared at first, then the reasons for the hysteresis are further investigated based on different top electrodes.

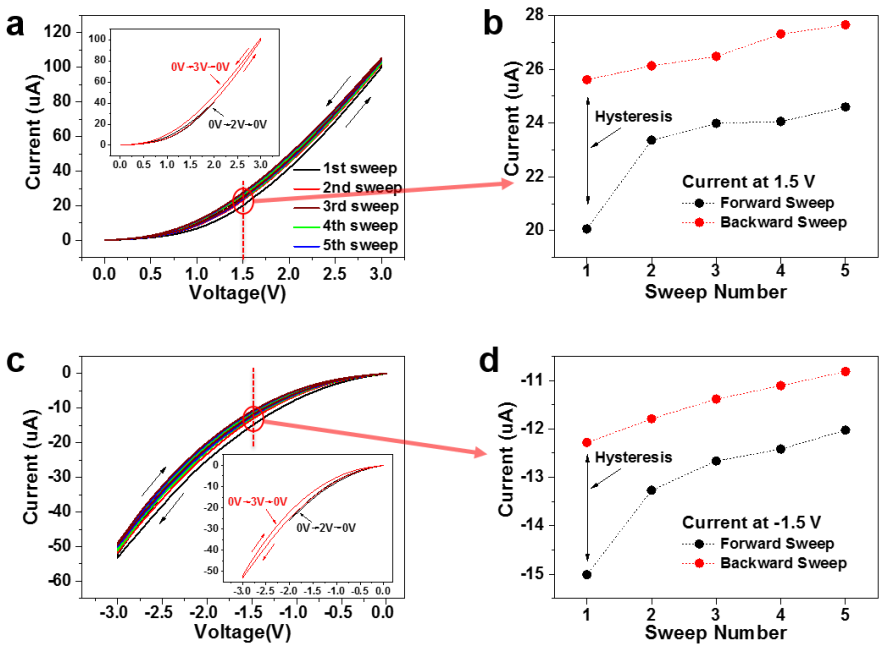

Figure 7.2 The consecutive IV sweep characterization under positive voltages (a) or under negative voltages (c), and the inset is the hysteresis comparison of the sweep to 2.0 V or 3.0 V (a, inset), or to -2.0 V or -3.0 V (c, inset). In order to depict the hysteresis under consecutive sweeps, (b) the intersect points at 1.5 V in the positive sweeps were measured and listed, and (d) the intersection points at -1.5 V in the negative sweeps.

The consecutive IV sweeps and hysteresis characterizations were obtained with Keithley source-meters under a sweeping rate of 2 V/s for both polarities, and the voltage sweeping is from 0.0 V to ±2.0 or ±3.0 V. As shown in Figure 7.2a inset, the hysteresis for the positive sweep to 2.0 V or 3.0 V were compared. Sweeping to 2.0 V did not produce noticeable hysteresis, probably due to the electric field induced under 2.0 V was not sufficiently high for the migration of V_{ox} or metal ions. On the other hand, there are much higher hysteresis in the sweeping to 3.0 V, which reveals that the 3.0 V could be the threshold voltage for the electric field to induce the conductance change. Then the results for 5 consecutive IV sweeps were shown in the Figure 7.2a, and the intersection points at 1.5 V for forward sweeps (0.0 V to 3.0 V) and backward sweeps (3.0 V to 0.0 V) were exhibited in Figure 7.2b to compare the hysteresis for different sweeping sequences. For each sweep, the forward sweep current is lower than the backward sweep current, which is the direct consequence of the formation of the conductive filaments, but under gradual growth not abrupt change. The first sweep

shows a higher hysteresis than the followings, which means that the conductance can be maintained for a certain time duration before a complete recovery. Moreover, the hysteresis are overlapped between the consecutive sweeps, probably due to short term relaxation process towards the less conductive states. Afterwards, the conductance for the consecutive sweeps keep gradually increasing, which is from long term accumulative responses for the continuous positive voltage biasing.

Similar behaviors also exist for the consecutive negative IV sweeps, as shown in Figure 7.2c and Figure 7.2d. The IV sweep to -2.0 V did not produce much less hysteresis than that for the IV sweep to -3.0 V. Moreover, for the 5 consecutive IV sweeps to -3.0 V, the forward sweep currents are higher than the corresponding backward sweeps, which is due to gradual breakup of the conductive filaments induced by the migration of V_{ox} or metal ions back to the top electrodes when negative voltage was applying. After comparing the intersection points at -1.5 V, the first sweep hysteresis is higher than the followings, and there is also overall modulation tendency to less conductivity, probably also due to the short term relaxation processes and long term accumulative responses for the continuous negative voltage biasing.

7.4 Verification for the Origin of the Hysteresis

As we discussed previously, the overall conductance change or hysteresis can be produced by the complicated migration processes of V_{ox} and metal ions. In order to further verify the physical working principle of the IV sweep hysteresis, the resistive switching devices with different top electrodes were fabricated and characterized, as shown in Figure 7.3. Thick (~ 100 nm) Pd and Ag electrodes were fabricated under the same photo-lithography and lift-off processes. Pd is inert electrodes, often used in the memristors to prevent the possible metal ion diffusion from electrode or the interaction between the V_{ox} and the electrodes.[153, 154] As shown in Figure 7.3a and Figure 7.3b, control sample of ITO/WO_x/Pd did not produce noticeable hysteresis in the 5 consecutive IV sweeps to 3.0 V. On the contrary, the hysteresis for the devices with Ag electrode is much higher. Figure 7.3c and Figure 7.3d depicted the IV sweeps under

negative bias, and similar results were obtained, where the hysteresis for Pd electrodes is much smaller than those for Ag electrodes. Therefore, the film properties of the WO_x used in the devices of ITO/WO_x/Pd or Ag may be quite different from the typical WO_x memristors made of (W/WO_x/Pd) reported previously, even under the same oxidation processes.[154] The density or activity of V_{ox} in WO_x grown on ITO coated substrate pieces may be much lower and thus inducing much less conductance change.

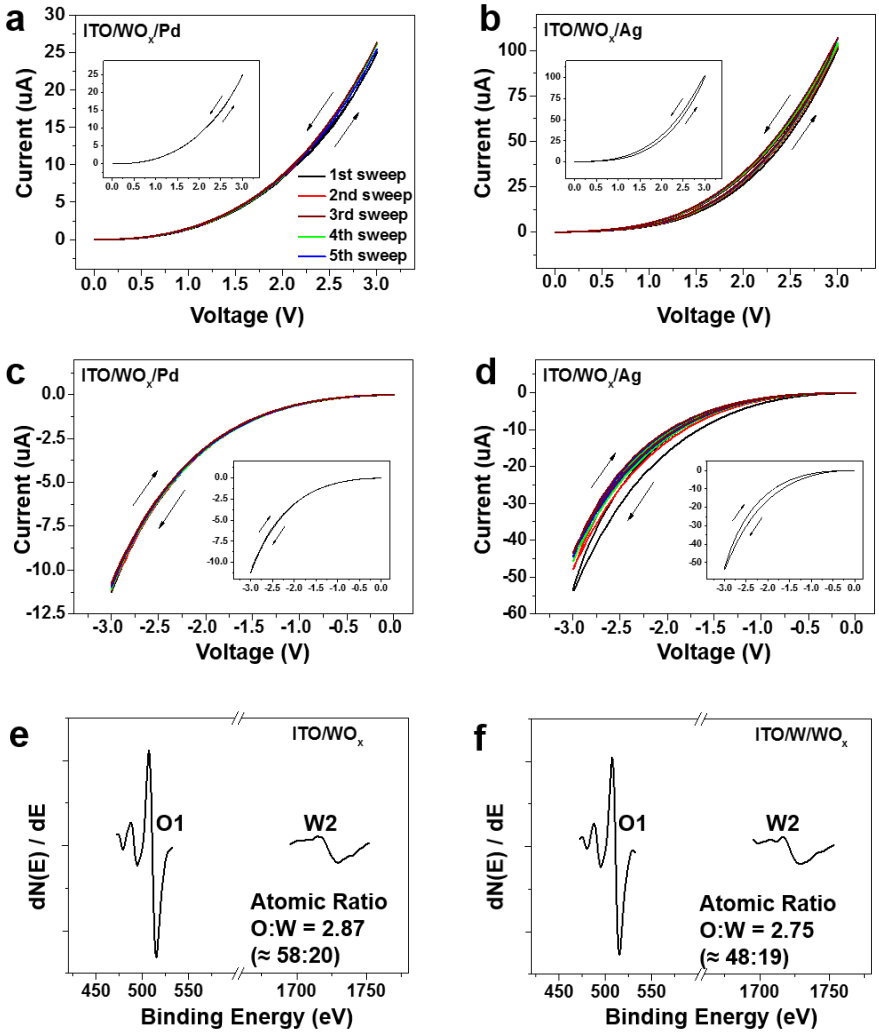

Figure 7.3 The consecutive IV sweep characterization for control samples with top thick Pd electrodes (a, c), or with top thick Ag electrodes (b, d), where positive sweeps are shown in (a) and (b), the negative sweeps in (c) and (d). Moreover, the very first IV sweep were separately shown in the insets for each image, for the purpose of more clear illustrations. Further characterization and comparison of the oxidation states for WO_x films were obtained with Auger Electron Spectroscopy (AES), where (e) is for the thin WO_x films grown on ITO substrates and (f) is for the WO_x films grown on the top surface of the thick W films.

The oxidation states can be extracted from the stoichiometry information obtained form Auger Electron Spectroscopy (AES) characterizations, as shown in Figure 7.3e and Figure 7.3f. We compared the WO_x films grown from ultrathin W (~ 12 nm) on ITO (ITO/WO_x) or directly from the top surface of thick W film (~ 100 nm) (W/WO_x). The atomic ratio of O:W for ITO/WO_x is 2.87 a little higher than that for W/WO_x (2.75), which reveals that the ITO may serve as a secondary O source, besides the O_2 atmosphere, and producing more thorough oxidation for WO_x films, thus fewer V_{ox} as well as much less conductance change. For WO_x films, there is a series of common stable oxides, such as WO_3, $WO_{2.9}$ ($W_{20}O_{58}$) $WO_{2.72}$ ($W_{18}O_{49}$), and WO_2, and metastable metastable states referred to as the "Magnéli phases" which comprise a series of substoichiometric phases.[166-168] Among them, $W_{18}O_{49}$ was reported to be readily observed in a distinct forms as nanowires, nanorods, nanobelts and so on. As the oxidation or atomic ratio increases close to WO_3, the films transit from being metal-like, semiconductor-like to insulator-like, which means the higher oxygen deficiency will contribute higher density of V_{ox} and the corresponding higher conductivity. In the obtained W/WO_x film, it is close to the stable configuration $W_{18}O_{49}$, on the other hand the ITO/WO_x is close to another stable configuration $W_{20}O_{58}$, therefore, the obtained device of ITO/WO_x/Pd did not show similar hysteresis effects like that of W/WO_x/Pd, just because of the influence of bottom ITO substrate and corresponding different oxidation states of WO_x films.

As discussed above, the IV hysteresis for ITO/WO_x/Ag is much higher than that for ITO/WO_x/Pd, as shown in Figure 7.3(a - d), which is primarily due to the migration of Ag ions from Ag electrode into the WO_x films. It created conductive paths for electrons, which enables the Poole-Frenkel Emission transportation by trapping and detrapping through a series of traps produced by the migration and localization of Ag ions. These results provide a direct evidence for the conduction mechanism of the IV behavior shown in Figure 7.2(a - d)

7.5 Conduction Mechanisms and Continuous Resistive Switching

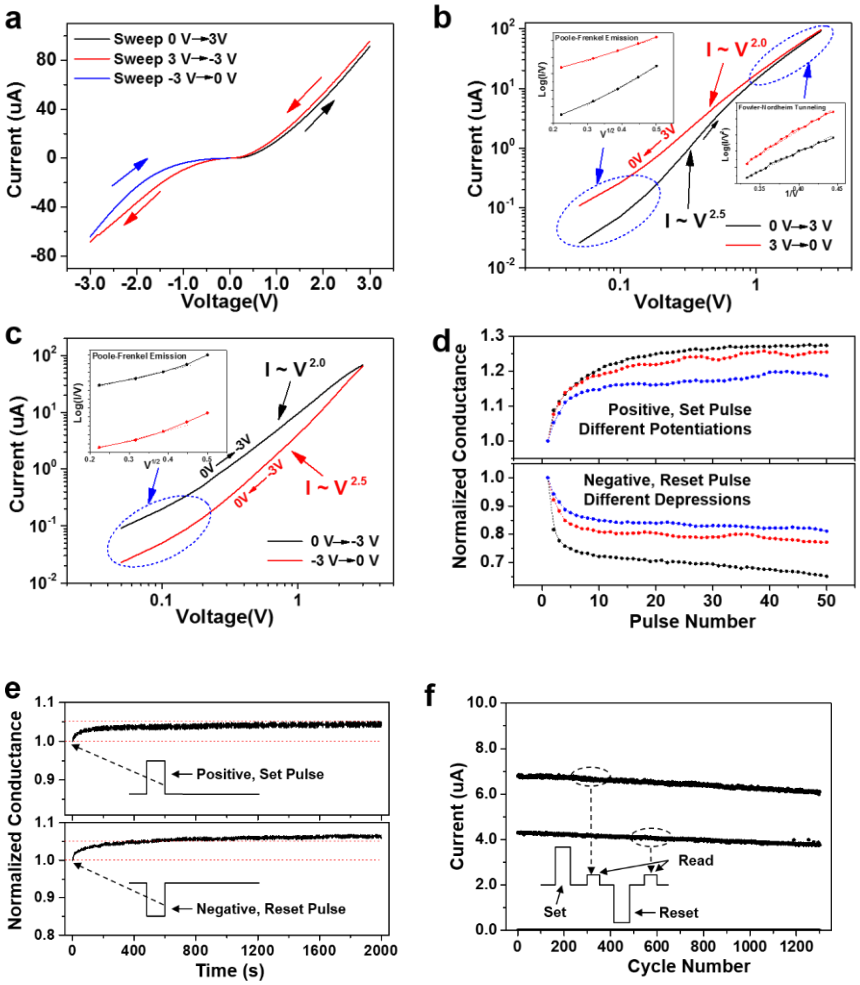

Figure 7.4 (a) The continuous IV sweeps for both polarities, with the voltage sweeping from 0.0 V to 3.0 V, then to -3.0 V, finally back to 0.0 V. (b, c) Conduction mechanism analysis for the both polarities by the linear fitting for the IV curves in a logarithmic scale, where (b) is for positive bias, and (c) is for negative bias. (d) The normalized conductivity response for 50 consecutive pulses with different durations, 1.0 ms (black), 0.5 ms (red), 0.2 ms (blue). The upper image is for the 3.0 V pulse voltage and lower one is for -3.0 V pulse voltage. (e) The retention characterization for 3.0 V (upper image) or -3.0 V (lower image) pulse stimulus with 10 ms duration. (f) The cycle endurance measurement, where a complete cycle is composed of 3.0 V 5 ms pulse stimulus, 0.5 V reading, then -3.0 V 5 ms pulse stimulus, 0.5 V reading.

After discussing the mechanisms for the hysteresis behaviors, more detailed electrical characterizations were measured, as shown in Figure 7.4. At first, the continuous IV sweeps for both polarities were conducted, where the voltage starts from

0.0 V to +3.0 V, then reverses to -3.0 V, finally goes back to 0.0 V. Both Polarities exhibit the hysteresis, and the negative bias has a much higher hysteresis than the positive bias, as shown in Figure 7.4a. It revealed that electric field under negative bias will stimulate the backward migration of metal ions more sufficiently. Conduction mechanisms for the both polarities were further analyzed by the linear fitting for the IV curves in a logarithmic scale, as shown in Figure 7.4(b-c) and the inset images.[169, 170] Under weak positive bias (left end of the curves), Poole-Frenkel Emission (PF Emission) can provide the most close fitting and dominate the charge transportation. As the bias increases, the conduction transits to Space Charge Limited Current (SCLC). The logarithmic slope for the forward sweep is around 2.5, higher than the 2.0 of backward sweep, indicating the trap-assisted SCLC is dominant in forward sweep, while after filling traps under the positive bias the typical SCLC is dominant for the backward sweeps. As the bias further increases to around 3.0 V, the logarithmic slope drops and Fowler-Nordheim tunneling best fits the IV behavior, indicating the carrier tunneling through the triangle barrier around the trap under high positive electric field. Under the negative bias, it has quite similar behaviors. Under the low bias, PF Emission is dominant, as shown in the inset of Figure 7.4c. As the bias increases, the negative forward sweep just follows the positive backward sweep, where the typical SCLC is dominant indicated by the logarithmic slope of 2.0. Then, the trapped carriers get released gradually under the negative bias, and the trap-assisted SCLC became dominant again under the backward sweep.

Figure 7.4d exhibits the normalized conductivity response for 50 consecutive pulses with different durations, where the amplitude of the pulse is 3.0 V and the duration is 1.0, 0.5 and 0.2 ms. The reading process is executed immediately after the pulse stimulus, and the reading voltage is 0.5 V. Under the positive pulses, the initial conductance responses follow similar gradient, revealing that the initial formation of the conductive filament does not need long duration probably due to the high mobility of metal ions in the WO_x films. However, different pulse durations will produce

different stabilized conductance which means different potentiation levels in terms of neuromorphic functionalities. Longer duration will produce higher conductance standing, which means higher potentiation level. On the other hand, the initial conductance response shows higher gradient slope for the negative pulse stimulus, which well corresponds to the higher hysteresis for the negative bias than positive bias shown in Figure 7.4a. Moreover, the higher pulse duration induces higher gradient slope as well as lower stabilized conductance, and these behaviors well mimic the different depression levels. The dependence of final conductance on the pulse duration time is probably due to the localized Joule heating, a longer pulse duration produces a higher Joule heating, which will induce more active migration of metal ions through the atomic lattice, also promote the releasing from traps and the tunneling for carriers.[171-173]

The retention characteristics were measured under 0.5 V reading voltage immediately after the ±3.0 V pulse stimulus with 10 ms duration, as shown in Figure 7.4e. The conductance for both positive and negative pulses was normalized to that of the very first reading, respectively. They have similar initial increasing stages, and finally stabilize at a certain level by 4.0 % to 6.0 %, which indicates that after modifications of the conductive filaments by the pulse stimuli, intrinsic diffusion of metal ions from the top electrodes still exist, giving rise to the additional growths. However, the final stabilized normalized conductivities are slightly different for positive pulse (4.0 %) or negative pulse (6.0 %). It reveals that the metal ion intrinsic diffusion for conductive filaments under negative bias are higher than that for the positive bias, which also corresponds to the higher hysteresis under negative bias shown in Figure 7.4a.

Finally, the cycle endurance was characterized, as shown in Figure 7.4f, where the pulse amplitude is 3.0 V and the duration is 5 ms, and 0.5 V reading was executed after each of the pulse stimuli. The cycle endurance was actually testing the hysteresis endurance, therefore the conductivity ratio for the positive or negative pulses is only around 1.6, which can be well maintained even after 1200 complete cycles. The overall decreasing of the conductance is probably due to the slightly imbalanced modulation

for the conductive filaments between the positive and negative pulse stimuli, and the conductance response for the negative pulse can not be completely recovered by the following positive pulse.

7.6 Conclusion

In this work, based on the optically optimized dielectric/metal/dielectric structure, we achieved transparent resistive switching devices. The metal doping to the ultrathin Ag films greatly improve the surface morphology, which gives rise to the high average transparency, higher than 80 %. Moreover, the migration of metal ions from the doped Ag films produce the conductance modification, which was found to be analog and continuous, functioning as appropriate behaviors for the prevalent neuromorphic computing. Under consecutive pulse stimulus with different durations, the device finally stabilized at different conductivity levels, acting as different potentiation or depression levels in terms of neuromorphic functionalities. The developed transparent resistive switching devices will enable the integration of neuromorphic functionalities to the transparent electronics, especially for multifunctional display screens, the "System-on-Glass" or Internet of Things.

Chapter 8 Air-Stable Ultrathin Copper Based Composite Metal Electrodes for Transparent Organic Thin Film Transistors

Abstract

Nowadays transparent electronic devices greatly promote the adventure and development of the innovative display technologies with see-through functionalities. In order to achieve higher transparency, the overall pixel aperture ratio need to be further improved. Transparent Thin Film Transistors (TFT) are demonstrating the potentials to breakthrough the aperture ratio limited by the conventional opaque TFTs in the active matrix. In this work, we developed ultrathin Cu-based composite electrodes with Ni seeding and capping layers, which enables the Cu films with continuity, conductivity, contact properties and stability. Based on the Ni/Cu/Ni electrodes, the optically optimized transparent Pentacene TFTs with ITO gate and PS-PAN bi-layer gate insulator exhibited excellent transparency, up to 71.4 % for the source/drain regions and even higher for the overall transparency.

8.1 Introduction

Nowadays, extensive innovative transparent electronic devices are drawing considerable attentions from academia or industries, which greatly promotes the adventure and development of the innovative display technologies, such as transparent display panel, near-eye displays or even augmented reality systems.[159, 165, 174] In order to achieve higher transparency, the overall pixel aperture ratio need to be further improved, which brings more challenges for the active matrix. Transparent Thin Film Transistors (TFT) are demonstrating the potentials to breakthrough the aperture ratio limited by the conventional opaque TFTs in the active matrix. Compared with the

conventional Si-based active materials in TFTs, the organic semiconductors give rise to higher transparency because of the large bandgap and the corresponding less visible light absorption.[49, 175, 176] Besides that, they also own other unique advantages, such as low-temperature fabrications, solution processes and intrinsic flexibility, which will provide versatile application possibilities for the pixel driving or data processing in the transparent electronics.

Considering the optical properties of the different layers in organic TFTs, the transparency of electrodes is turned out to be the biggest challenges. The gate electrode is only used to create a voltage bias for the channel modulation and separated from the channel semiconductor with gate insulators, therefore much more transparent conductive film materials can be used, such as ITO, graphene, PEDOT:PSS and so on.[174, 177-180] On the other hand, the source or drain electrodes need to directly contact the channel semiconductor, and the electrode material selections will be limited by the contact properties, fabrication temperature, patterning complexity or so.

In this work, based on the reported Pentacene TFTs with thick Cu source and drain electrodes,[181, 182] we increased the transparency by reducing the electrode thickness and improved the contact properties and stability by introducing Ni seeding and capping layers. Furthermore, the optically optimized transparent Pentacene TFTs with ITO gate and PS-PAN bi-layer gate insulator exhibited excellent transparency, up to 71.4 % for the source/drain regions and even higher for the overall transparency.

8.2 Device Structure and Fabrication

The basic device structure is bottom gate, top source/drain contact architecture, as shown in Figure 8.1a. The ITO coating glass pieces were used as substrates as well as the bottom gate, patterned by photo-lithography and followed by etching in hydrochloric acid for 4 min. The gate insulator was the Polyactylonitrile (PAN) - Polystyrene (PS) bi-layer design. The 530 nm thick PAN layer was formed by spin-coating a PAN solution in N,N-dimethylformamide with a concentration of 50 mg/mL at 2500 rpm for 60 s, followed by an annealing process at 140 ℃ for 30 min in glovebox.

Then the PS solution in toluene of 5 mg/mL concentration was spin-coated on top of the PAN layer, and annealed at 80 °C for 10 min in glove box as well. The 40 nm thick Pentacene film was used as channel semiconductor, fabricated by thermal evaporation with a deposition rate of 0.2 Å/s. Then the source/drain contact interlayer MoO_x was also deposited by thermal evaporation with a rate of 0.3 Å/s. The Cu-based composite metal electrodes were deposited by E-beam evaporation, and the corresponding channel width is 1200 um, length 50 um.

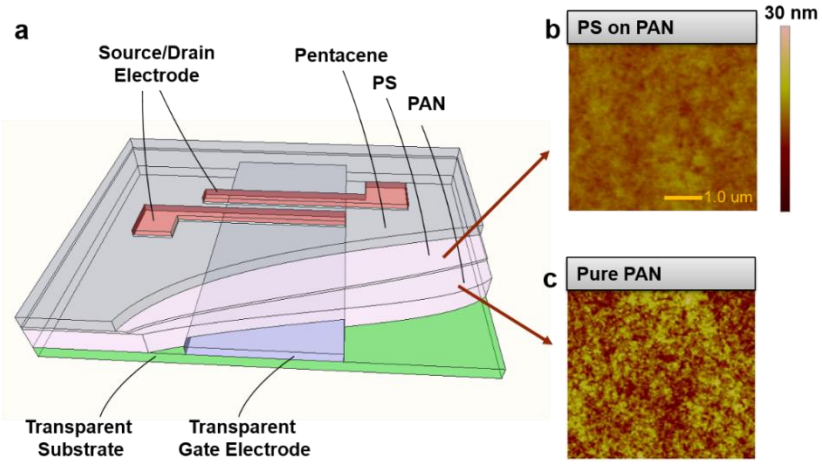

Figure 8.1 (a) The schematic illustration of the transparent Pentacene TFTs, with a structure of ITO gate/ PS-PAN bi-layer gate insulator / 40nm Pentacene / MoO_x / Cu-based source/drain. (b) and (c) are the AFM characterizations for PS-PAN bi-layer and pure PAN, respectively. The roughness of PS-PAN is 1.08 nm, reduced from 3.01 nm for pure PAN.

The PS-PAN bi-layer gate insulator is also the combination of high-k (PAN, 5.5) and low-k (PS, 2.5), which allows a higher tolerance for thicker gate insulator with benefits of reducing the gate leakage and operating voltage. Moreover, the PAN surface morphology will be greatly improved by PS coating, as shown in the Figure 8.1b and Figure 8.1c. The surface roughness of pure PAN is 3.01 nm, which will reduce to be 1.08 nm by PS coating, due to the excellent leveling properties of the PS. The benzene ring embedded in the chains of PS will show better affinity to pentacene and facilitate its crystal growth with less defects.[183] Due to the contribution from these three aspects, the mobility of the Pentacene TFT based on PS-PAN (> 0.2 $cm^2/V{\cdot}s$) is much higher than that for pure PAN (0.012 $cm^2/V{\cdot}s$).

8.3 Transmission and Surface Morphologies

As typical hole transport layers, molybdenum oxide (MoO_x) is often used in the organic light emitting device (OLED), organic solar cell (OSC), and even organic TFTs to improve the contact properties of anodes or source/drain electrodes.[181, 184-186] From the results we obtained, the improvement due to the inserted MoO_x interlayer was verified where the mobility of Pentacene TFTs with MoO_x interlayer is much higher that those without MoO_x. Pentacene is considered to be one of the standard semiconductors for organic TFTs, and Au is often used as source/drain electrodes due to its high workfuncion (WF) matching the Pentacene HOMOs. However, people found Cu electrodes will produce equivalent or superior electrical performance for Pentacene TFTs because of its lighter atom weight, less bombardment impact to the source/drain contacts during the evaporation, and also because of the corresponding narrower trap distribution.[181, 182] On the other hand, the lower price of Cu will greatly reduce the material cost, and ultrathin Cu films also own pretty good transparencies among metals. As a result, we employed Cu as the basic material for ultrathin composite transparent electrodes, and verified its electrical and optical properties on glass or MoO_x interlayers.

Table 8.1 The thermal and air-stability characterization

	R.T (Ω/□)	**80 °C Air, 30s**	**150 °C N_2, 5min**	**150 °C Air, 5min**
8 nm Cu	31.2	35.5	56.8	∞
0.5 Ni /7.5 Cu	32.8	31.7	42.3	88.6
0.5 Ni/ 7 Cu /0.5 Ni	22.8	22.3	23.8	23.1

After balancing the film conductivity and transmission, we firstly investigated the air-stability of Cu films, as listed in Table 1. The sheet resistance (R_{sh}) is measured by 4-point probe, as deposited and after each consecutive annealing step, including 80 ℃ for 30s in air, 150 ℃ for 5 min in N_2, and finally 150 ℃ for 5 min in air. For the pure 8 nm Cu film, the measured R_{sh} for the 4 steps are 31.2 Ω/□, 35.5 Ω/□, 56.8 Ω/□, and ∞ Ω/□, respectively. The results revealed that the ultrathin Cu film is very unstable in

air, probably due to its high sensitivity to the oxygen and humidity in air. Seeding layer is commonly used to improve the surface morphology of the ultrathin Ag films.[187-189] We decided to use 0.5 nm Ni as seeding layer for the ultrathin Cu films, because Ni is quite adhesive to the substrate, often used as adhesive layer for Au films, then it owns a high WF (5.04 – 5.35 eV) and its oxides is often working as anode interlayers, which will most likely give rise to further improvement for the source/drain contacts. The measured R_{sh} for the 0.5 nm Ni / 7.5 nm Cu films is 32.8 Ω/□, 31.7 Ω/□, 42.3 Ω/□ and 88.6 Ω/□, respectively. The stability is greatly improved, and it maintains high conductivity especially after the final 150 °C annealing in air. However, the top Cu surface is still under the potential adverse influence of exposing in air, since the R_{sh} keeps increasing during the consecutive annealing steps. Therefore, additional 0.5 nm Ni capping layers were deposited after depositing 0.5 nm Ni / 7 nm Cu. The measured R_{sh} for the 0.5 nm Ni / 7.0 nm Cu / 0.5 nm Ni (Ni/Cu/Ni) films is 22.8 Ω/□, 22.3 Ω/□, 23.8 Ω/□ and 23.1 Ω/□, respectively. It revealed that the Ni capping layer is a very good insulation and protection against air for the beneath Cu film, and achieving excellent stability and robustness together with the Ni seeding layer.

In order to facilitate the following fabrication of pentacene TFTs, we further characterized the ultrathin pure Cu or Ni/Cu/Ni composite electrodes on glass or 8 nm MoO_x interlayers, by optical transmission, SEM and AFM, as shown in Figure 8.2. The 400 - 800 nm transmission spectrum, average transmission (T_{avg}) and R_{sh} were summarized in the Figure 8.2a. For the pure Cu film, T_{avg} is 64.0 % on glass and 52.0 % on MoO_x, respectively. However, the R_{sh} is infinite for the pure Cu film on MoO_x, which indicated that its surface morphology is not continuous. On the contrary, the Ni/Cu/Ni composite electrode did not behave quite differently, where the T_{avg} is around 60% and R_{sh} is 22 to 25 Ω/□ either on glass or MoO_x. It is predicted that the Ni seeding layer is also helpful to form a good isolation against the beneath MoO_x for the ultrathin Cu film.

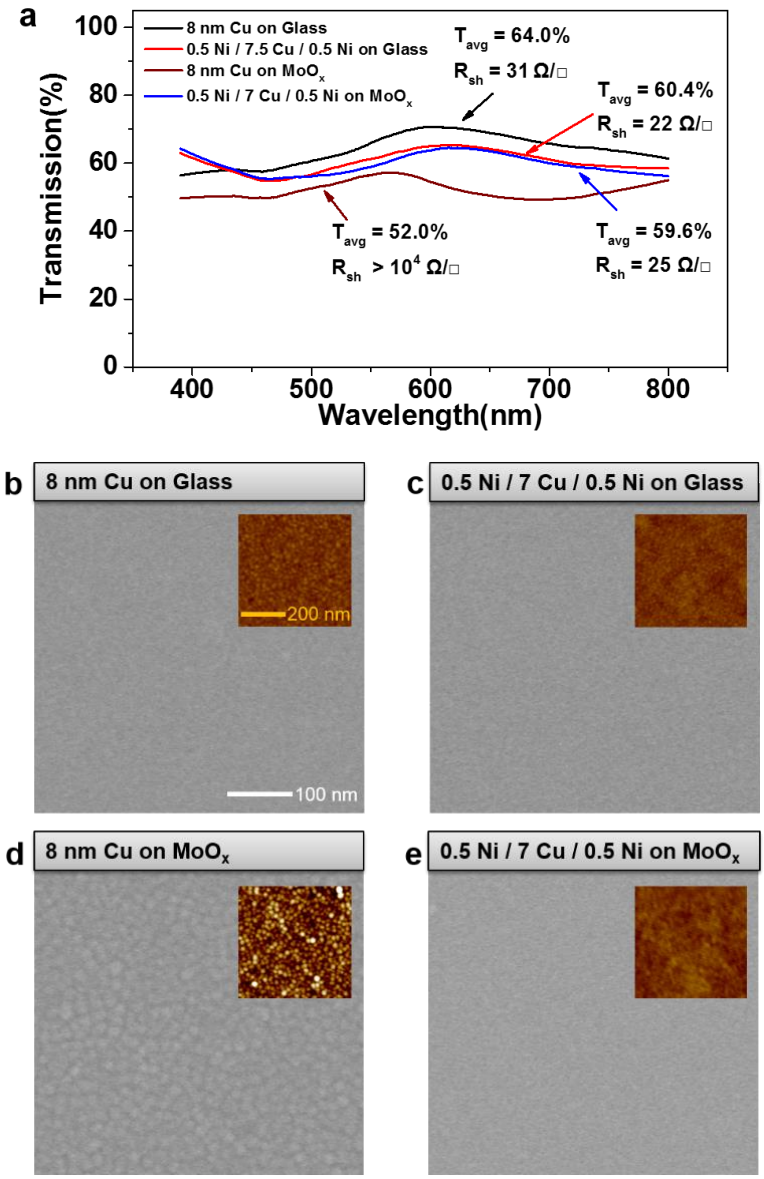

Figure 8.2 (a) The transmission spectrum, average transmission (T_{avg}) and the sheet resistance (R_{sh}) for ultrathin pure Cu or Ni/Cu/Ni films on glass or MoO_x layer. (b) - (c) are the SEM images of the ultrathin pure Cu or Ni/Cu/Ni films on glass, (d) and (e) are SEM images of the films on MoO_x. The insets in (b)-(e) are the corresponding AFM characterizations.

The SEM and AFM characterizations are providing further evidences to the interactions between the MoO_x and Cu films. As shown in Figure 8.2b and Figure 8.2d, the SEM image of pure Cu films on glass shows smooth morphologies with slight granule feature, however, the pure Cu films on MoO_x was deteriorated into the discontinuous islands morphologies, with quite clear grain boundaries in SEM images. The AFM characterizations correspond the SEM images, where the roughness for pure

Cu films on glass or MoO_x are 0.383 nm and 1.02 nm, respectively. Therefore, the MoO_x films do not induce the growth of continuous or smooth Cu films, probably due to the seeding density of the initial Cu film growth on MoO_x is too sparse for such thin thicknesses. As a result, the Ni/Cu/Ni composite electrodes were introduced with 0.5 nm Ni seeding and capping layer to promote the continuity and stability. As shown in the Figure 8.2c and Figure 8.2e, the Ni/Cu/Ni films on the glass or MoO_x exhibit dense and continuous morphologies, and invisible grain boundaries in SEM images. The AFM characterizations show the reduced roughness correspondingly, where 0.228 nm and 0.287 nm for the Ni/Cu/Ni films on glass and MoO_x, respectively. The equivalent roughness and morphologies for Ni/Cu/Ni films on the two different substrates further prove the equivalent transmission spectrums and the R_{sh} of Figure 8.2a.

8.4 IV Characterizations and Contact Resistance

The electrical characteristics of the devices were obtained by Keithley 4200 SCS under room temperature and ambient environment. The first step is to compare the 30 nm Cu and the Ni/Cu/Ni source/drain electrodes, here the Si wafers with 300 nm SiO_2 layer were employed as substrates and bottom gate / gate insulator. The 40 nm Pentacene layers were deposited on the PS coated gate insulator. The Figure 8.3a and Figure 8.3b are transfer curves with linear or logarithmic scales, where the 8.0 nm MoO_x interlayer produced higher drain current responses, forming the better contacts both for pure 30 nm Cu and Ni/Cu/Ni electrodes, due to the induced Ohmic contacts and the protection against the diffusion and other possible chemical reactions between semiconductor and metal electrodes.[186] The mobility and on/off ratio for pure 30 nm Cu electrodes are 0.086 $cm^2/V\cdot s$ and 1.53×10^6, meanwhile they are improved to be 0.27 $cm^2/V\cdot s$ and 3.8×10^6 for Ni/Cu/Ni electrodes. Correspondingly, the output curves for Ni/Cu/Ni electrodes are showing clear linear and saturation regimes, and the current response is higher than that for pure 30 nm Cu electrodes.

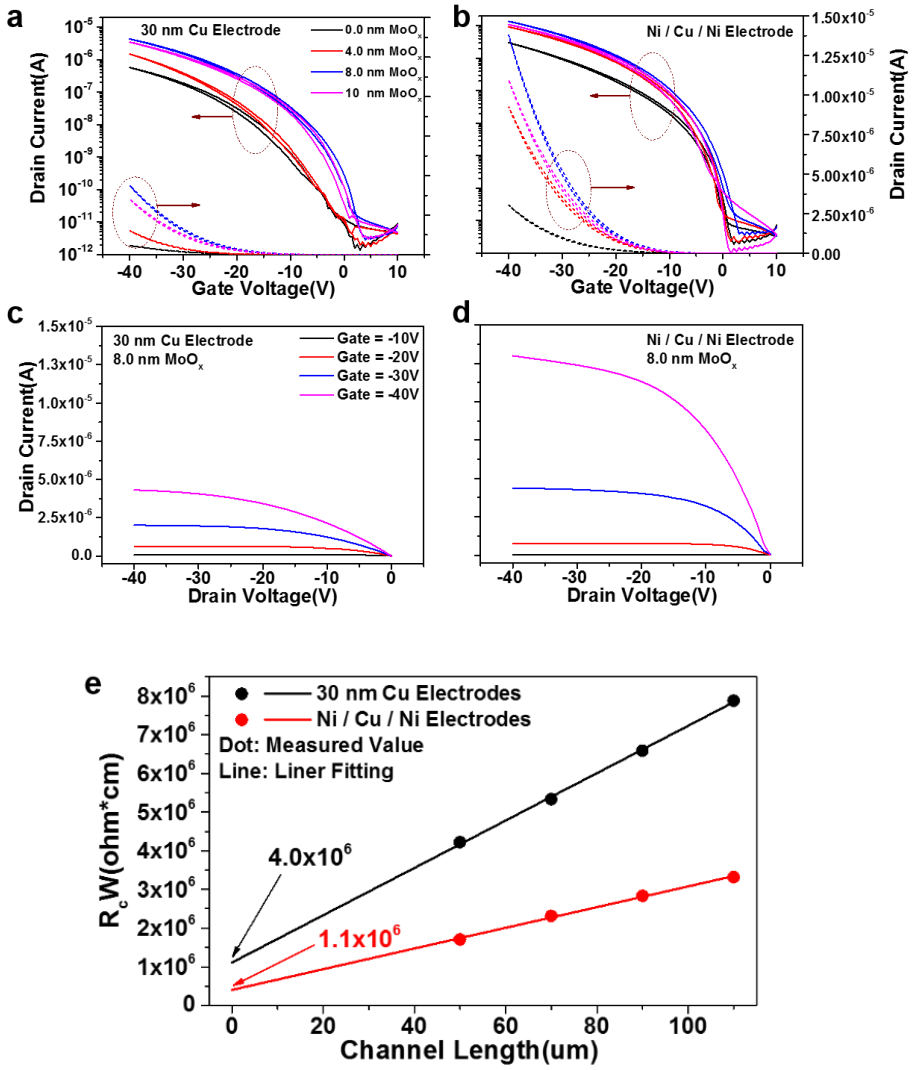

Figure 8.3 (a) and (b) are transfer curves with linear or logarithmic scales for pure 30 nm Cu and ultrathin Ni/Cu/Ni source/drain electrodes with different thickness MoO_x interlayers. (c) and (d) are the output curves for the Pentacene TFTs with 8 nm MoO_x interlayer. (e) depicts the extraction for the contact resistance based on Transmission Line Method with different channel length from 50 um to 110 um.

The contact properties between Pentacene and source/drain can be explicitly characterized by contact resistance, which will greatly influence the mobility, trans-conductance even the stability.[182, 190, 191] Using the transmission line method (TLM), we measured and analyzed the contact resistance based on the Pentacene TFTs with different channel length from 50 um to 110 um. The intersection points of the linear fitting lines at y-axis of 0.0 um channel length are the contact resistance, which

is extracted from the dependence of the total resistance on channel length, as shown in Figure 8.3e. The contact resistance for Ni/Cu/Ni is 1.1×10^6 Ω·cm, much less than 4.0×10^6 Ω·cm for pure Cu electrodes, corresponding to the improved transfer and output curves. As a result, the Ni/Cu/Ni electrodes will produce much better contacts than pure Cu electrodes, because of Ni seeding layer and its possible oxide, good adhesive to the MoO_x, smooth morphologies as well as the lower R_{sh}.

8.5 Demonstration of Transparent Pentacene TFTs

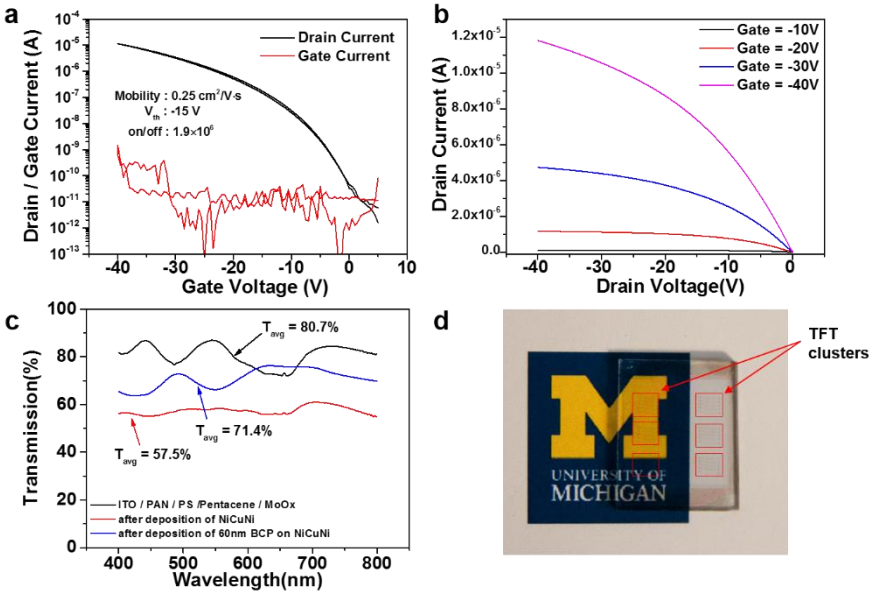

Figure 8.4 (a, b) The transfer and output characterizations for the transparent Pentacene TFTs with ITO gate and PS-PAN bi-layer gate insulator. (c) The transmission spectrums for different stacked layers, especially after deposition of Ni/Cu/Ni electrode or BCP anti-reflection layer. (d) The transparency of the sample covering the University of Michigan logo.

Based on the developed MoO_x and Ni/Cu/Ni source/drain electrodes, we demonstrated transparent Pentacene TFTs fabricated on ITO substrate and PS-PAN bi-layer gate insulator, as shown in Figure 8.4. Moreover, the transparency was further improved by optical simulation and the top 60 nm Bathocuproine (BCP) anti-reflection layer. Figure 8.4a and Figure 8.4b are the transfer and output curves for the transparent TFTs. The mobility and on/off ratio are 0.25 $cm^2/V\cdot s$ and 1.9×10^6, respectively, which

are comparable with the control samples based on SiO_2/Si substrate. Negligible hysteresis was observed for the forward and reverse sweeps, revealing the negligible ion movement or dipole exchange in the PAN gate insulator. The gate leakage was remaining at low level, smaller than the drain current by over 4 orders, which indicates large band barrier between gate insulator and Pentacene, and low charge percolation through the gate insulator. Figure 8.4c and Figure 8.4d exhibit the transmission spectrums for different stacked layers and transparent Pentacene TFT clusters on samples covering the university logo. The overall transmission before deposition of Ni/Cu/Ni electrodes is up to 80.7%, since the material from ITO, PS-PAN, Pentacene and MoO_x are highly transparent. It reduced to 57.5 % due to the light absorption or reflection of Ni/Cu/Ni electrodes. After optical optimization simulations, we found the thermal evaporation of 60 nm BCP is a convenient method to fabricate the anti-reflection coating on top of the Ni/Cu/Ni electrodes. As a result, the overall transmission was improved to 71.4 % due to the reduced reflection or absorption.

8.6 Conclusion

In summary, we developed ultrathin Cu-based composite electrodes with better contact properties and stability by introducing Ni seeding and capping layer. On the commonly used MoO_x hole-transporting layer or contact interlay for Pentacene TFTs, the developed Ni/Cu/Ni electrodes greatly improved the film growth with a better continuity and conductivity, compared to the near-zero conductivity for ultrathin pure Cu films on MoO_x. The extracted contact resistance for Ni/Cu/Ni is also much lower than that for pure Cu. The optically optimized transparent Pentacene TFTs with ITO gate and PS-PAN bi-layer gate insulator exhibited excellent transparency, up to 71.4 % for the source/drain regions and even higher for the overall transparency.

Chapter 9 Summary and Future Plan

9.1 Summary

In this dissertation, we extensively studied intrinsic amorphous silicon (a-Si) hybrid structure with inorganic/organic materials based on the a-Si devices previously developed in our group, and explored the practical applications. Meanwhile, we still stepped into the various transparent electronic devices, including the transparent organic TFTs and memristors based on the developed transparent ultrathin metal film electrodes.

The top cathode contacts were developed in our group based on the conjugated organic semiconductor. In order to get rid of the potential degradation in air, we investigated the air-stable top cathode contacts based on the the Polyethylenimine (PEI) and ZnO interlayers in Chapter 2. Dipoles will be induced along the ZnO/PEI interface, pointing from ZnO to PEI, which will facilitate the work-function lowering of bottom cathodes. However, for the top cathode contacts in the normal-type devices, we found that the dipole induced across the PEI layers is highly related to the surface properties of the layers adjacent to it. The obtained results revealed the ZnO/PEI interlayer also work well as top cathode contacts. The reported dipole between ZnO/PEI which is supposed to increase the barrier, is actually overcome by another dipole induced along the interface between the PEI and cathode metals. The fabrication of ZnO/PEI interface is based on solution and low-temperature processes, which gives rise to other promising cathode contact alternatives as top cathode contacts of devices, especially for those with semi-transparency, even flexibility.

After discussing the top cathode contacts, we further investigate the bottom anode

contacts in Chapter 3. The interface conductivity and oxygen deficiency for WO_x / a-Si interlayer are reported. The ITO transparent electrode extensively used in large-area electronics is becoming more and more expensive, and the metal mesh is a popular backup alternative for the replacement of ITO. However, the local conductivity for the non-conductive area in the metal meshes has to be compensated. In this work, we systematically analyzed the interfacial properties of the WO_x/a-Si interfaces, including the band diagram and the carrier lateral transportation. We found the WO_x/a-Si interface is able to to support centimeter-scale non-electrode area, without the additional conductive layers to compensate the conductivity. The hypothesis and characterizations reported here can be used to determine more details for the exact definition of the device areas and secure better device designs. More significantly, it gives rise to the further possibilities of devices with semi-transparency, ultra-sparse metal mesh electrodes, and so on.

The a-Si was the dominant semiconductor for the active matrix backplane in TFT-LCDs. Nowadays, a-Si photodetectors are good candidates in the in-screen fingerprint scanners. In Chapter 4 and 5, we characterized the photodetectors based on the developed interlayers for a-Si devices, especially the detection under low illumination towards the in-screen fingerprint scanners. In this work, we employed top ZnO NPs and PEI interlayers. High LDR are achieved up to 190 dB, and at least 4 orders for the illuminations < 50 Lux. In order to show the clear current ratio between the adjacent a-Si PD pixels, short linear arrays are fabricated, and the current sequence in the arrays exhibited good ratio up to 2 orders. Finally, peripheral circuits are built up based on the Arduino microcontrollers to fast acquire the current detected by the short linear arrays, which can clearly show the patterns mimicking the groves and valleys of the fingerprints. The inverted a-Si PD with bottom cathode contact interlayers are developed and characterized to fulfill the requirements of the architecture design for the sensing arrays. The ZnO and MoOx are employed as the ETL and HTL for the inverted a-Si PDs. The current leakage and LDR get analyzed with different a-Si thicknesses and device areas. The a-Si PD arrays with pixel areas are fabricated based

on the photo-lithography processes in order to extract accurate current leakage and LDR. Finally, the optimized a-Si PD arrays are fabricated on the LTPS TFT backplanes.

The neuromorphic computation, especially towards the artificial intelligence industries, allows a huge development room for the artificial synaptic devices. In Chapter 6, innovative artificial synapses were demonstrated based on the interactions between the a-Si and PEI interlayers. The hysteresis and timing dependent plasticity of the artificial synapses can be excited by light illumination, coupled with electrical pulse stimuli. The device design is promising to serve as fundamental elements for neuromorphic functionalities towards the simultaneous visual information process in large-area electronics or IoT.

Transparent electronics is another hot research area to promote the information interactions between humans and the ambient environments. We also fabricated transparent devices based on the ultrathin transparent metal films and the corresponding optical management. In Chapter 7, we achieved transparent resistive switching devices to promote neuromorphic computing for the transparent electronic systems. The devices are based on ultrathin doped Ag films and optically optimized dielectric/metal/dielectric structure. The overall transparency is higher than 80%, and the device conductance modulation is found to be analog and continuous. Under consecutive pulse stimulus with different durations, the device finally stabilized at different conductance levels, acting as different potentiation or depression levels in terms of neuromorphic functionalities. In Chapter 8, Transparent organic TFTs were obtained based on the ultrathin metal film electrodes. In order to achieve higher transparency, the overall pixel aperture ratio need to be further improved, therefore, transparent TFT are demonstrating the potentials to breakthrough the aperture ratio limited by the conventional opaque components in TFTs of the active matrix. In this work, we developed ultrathin Cu-based composite electrodes with Ni seeding and capping layers, which enable better film continuity, conductivity, contact properties and stability. Based on the Ni/Cu/Ni electrodes, the optically optimized transparent Pentacene TFTs with ITO gate and PS-PAN bi-layer gate insulator exhibited excellent

transparency, up to 71.4 % for the source/drain regions and even higher for the overall transparency.

Finally, based on the developed a-Si photodetectors, there are still further development optimizations. The first one is the transparent a-Si optoelectronic devices based on all-inorganic interlayers, to improve the air-stability and process computability with the production lines. After the device optical design, the absorption peak of the a-Si devices can be modulated to a certain wavelength. We have completed the designs based on different thickness of top ITO electrodes and MoO_x HTL, for the absorption peaks located at 450 nm and 540 nm. Moreover, we can also employ the DMD structure for the top transparent anode, then modulate the absorption spectrum by changing the top MoO_x capping layer.

9.2 All-inorganic Transparent a-Si Optoelectronic Devices

The transparent solar cell devices with angle insensitive transmissive colors were developed in our group, based on the conjugated organic semiconductors. However, the organic semiconductors will suffer the degradation by the percolation of Oxygen or Moisture from the contacting with air. Here we demonstrated transparent a-Si devices based on the inverted device design developed for the a-Si PD matrix in in-screen fingerprint scanners. We employed the transparent ITO electrodes for both of the bottom cathode and top anode, then the ETL and HTL are ZnO and MoOx, respectively. The image of the samples are illustrated in Figure 9.1.

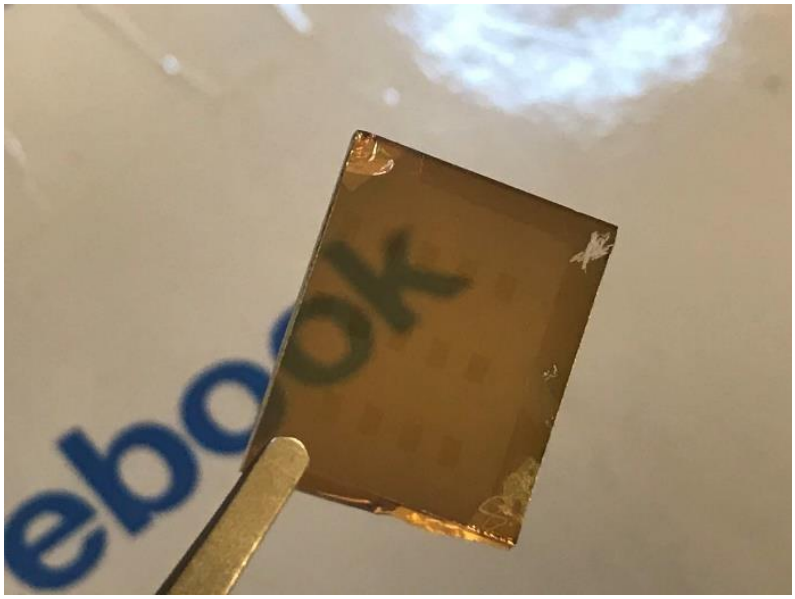

Figure 9.1 Transparent a-Si photodetector devices with ITO electrodes.

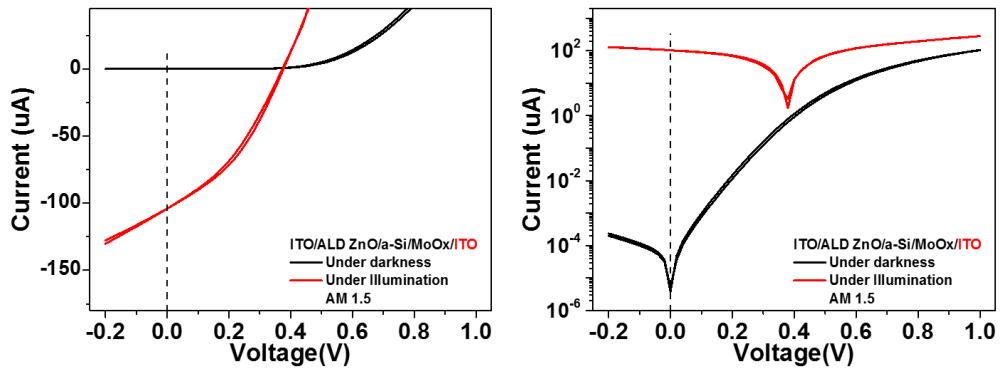

Figure 9.2 IV characterizations for the transparent a-Si devices under darkness and illumination, in linear scale or log scale.

The IV characterizations for the transparent a-Si devices are depicted in Figure 9.2. There are clear power-conversion behaviors, and the current ratio for the application is pretty good. However, the band diagram and thickness for a-Si and the corresponding interlayers are still need to be improved to further suppress the leakage current under reverse biases and increase the power-conversion efficiency. Moreover, the apparent device color can also be modulated by carefully changing thickness of various functional interlayers.

9.3 Thickness Modulation of Transparent Top Anode and HTL

We ever investigated the a-Si photodetectors towards the in-screen fingerprint scanners. However, the overall fabrication cost will greatly depend on the location of the sensing array, on the TFT back plane side or on the Color Filter (CF) front plane side. At this point, we only developed the bottom illuminated device design, which is compatible for the fingerprint scanner mounted to the CF front plane side. It means a secondary active matrix, besides the original TFT active matrix driving the LCD pixels, and double cost for the corresponding fabrication. Therefore, people would like to mount the sensing array together with the original TFT active matrix on the backplane side, which will require the top illumination configuration for the TFT-LCD screens. Therefore, we also achieved the optical design for the top illuminated a-Si photodetectors based on the bottom Ti cathode and top ITO anode, as shown in Figure 9.3 and Figure 9.4. The thickness for Ti cathode, ZnO ETL and a-Si active layers are 100 nm, 50 nm, and 300 nm, respectively, while the top MoO_x HTL and ITO anode can be modulated to a certain absorption peak. Ideally, all of the interlayers, including cathode and anode metals, and the corresponding ETL and HTL, can be deposited by sputtering to match processes procedure in the production line. In order to improve the blue light absorption, 50 nm MoOx and 104 nm ITO are employed, and the corresponding absorption peak is at 450 nm. For the green light, we are using 60 nm MoOx and 143 nm ITO, and the corresponding absorption peak is at 540 nm.

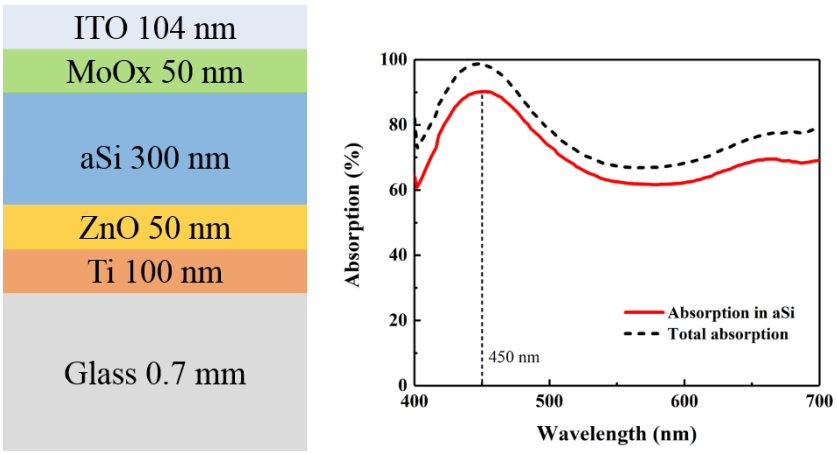

Figure 9.3 Top illumination a-Si device design and the corresponding absorption spectrum with a peak located at 450 nm.

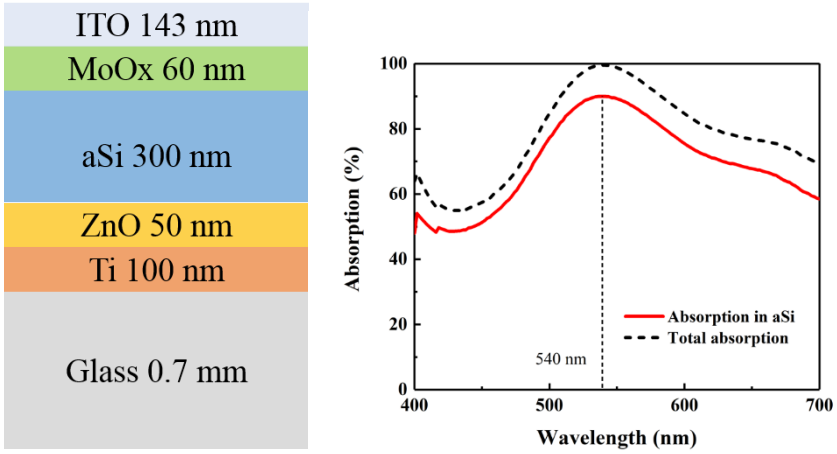

Figure 9.4 Top illumination a-Si device design and the corresponding absorption spectrum with a peak located at 540 nm.

9.4 Dielectric / Metal / Dielectric for the Top Anode of a-Si PD

ITO is the prevailing transparent electrode used in the optoelectronic devices, even in the flat panel display industries. However, the scarcity of the indium will promote the upraising of the indium and the corresponding fabrication cost. Under such circumstances, our group put huge efforts to the development of the transparent ultrathin doped Ag films, and improve the overall transmission based on the Dielectric / Metal / Dielectric.[163, 164, 192] At this point, we continue to investigate the availability of the optical design based on the transparent ultrathin doped Ag anode.

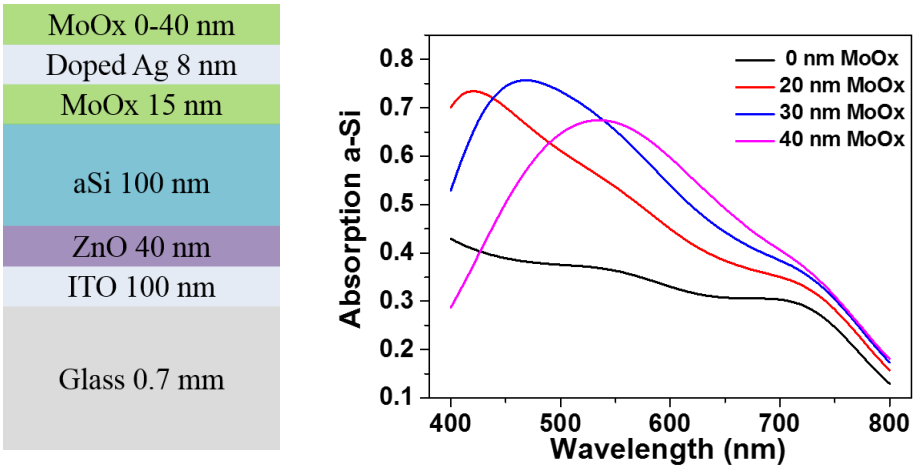

Figure 9.5 Transparent a-Si device designs based on bottom ITO cathode and the transparent top DMD configuration (MoO_x / Doped Ag / MoO_x), and the corresponding transmission spectrums.

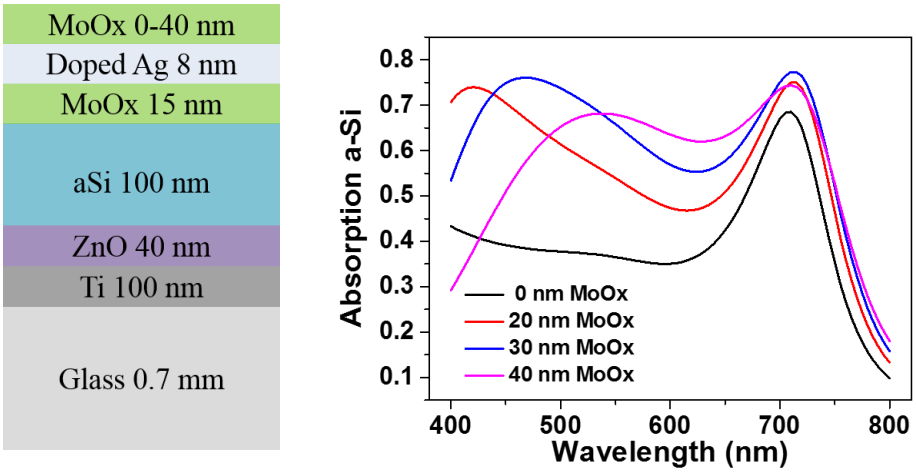

Figure 9.6 Top illumination a-Si device designs based on reflective bottom Ti electrode and the transparent top DMD configuration (MoO_x / Doped Ag / MoO_x), and the corresponding transmission spectrums.

The top illuminated device structure are shown in Figure 9.5 and Figure 9.6, the inner MoO_x and doped Ag used in the DMD are 15 nm and 8 nm, respectively, while the outer MoO_x increased from 0 nm to 40 nm. The absorption spectrums are depicted together with the device structure illustrations. As we see, the DMD top anode structure can significantly facilitate the light absorption in a-Si layer, because of the reduced reflection on the transparent ultrathin doped Ag surface. Meanwhile, the absorption peak can be modulated by changing the outer MoO_x interlayers. As the thickness increases from 20 nm to 40 nm, the peak wavelength moves from 420 nm, 470 nm to

540 nm, as shown in Figure 9.5. Considering the EQE spectrum of a-Si layer, the 30 nm MoO_x layer and 470 absorption peak will produced highest opto-electronic conversion efficiency, since the a-Si owns a higher EQE at shorter wavelength and the absorption peak value is higher at 470 nm than those at 420 nm or 540 nm. Meanwhile, the 100 nm Ti cathode also can be used instead of the transparent ITO cathode, as shown in Figure 9.6. The absorption spectrums at shorter wavelength are almost identical to those with ITO cathode, while there is another absorption peak near 710 nm due to the reflection of the bottom Ti cathode, which can actually be modulated to achieve the top illuminated a-Si photodetectors working at the near Infrared band.

Appendices

A. Labview Program of the Data Acquiring for Solar Cells

LabVIEW offers a graphical programming approach that helps us visualize every aspect of your application, including hardware configuration, measurement data, and debugging. This visualization makes it simple to integrate measurement hardware from any vendor, represent complex logic on the diagram, and design custom engineering user interfaces.[193] Therefore, we designed our own Labview Programs to figure out the data acquiring and storage for the IV characterizations of solar cells, extensively the static performance of the opto-electronic devices. As shown in Figure A1, the equipment we would like to use can be selected through the drop-down list of the VISA resource name, under the standard light illumination for solar cell measurement. Then the start, stop and step voltage for forward and backward sweeps can be set as well. Meanwhile, there is another parameter NPLC used to determine the sweep speed, and the calculated estimation of the total time, number of total test points and sweep rate can be indicated on the interface. The IV curves will be drawn in the right graph after each sweep finished. Then the data is stored in *.tdms files, a specific data file format developed by the NI, under the filename set in the lower long blank.

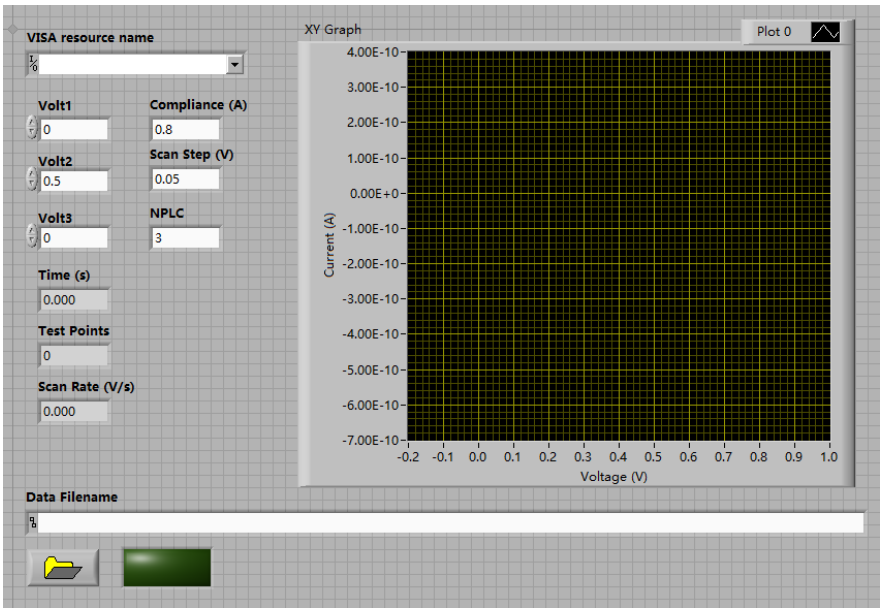

Figure A1. Image of the Labview User Interface of the data acquiring for the IV characterizations of solar cell devices.

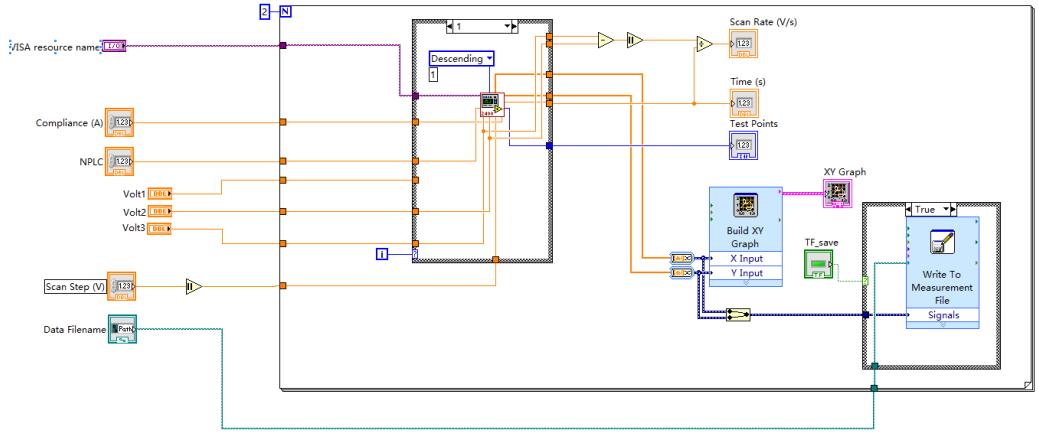

Figure A2. The block diagram configuration and connections of the Labview User Interfaces for the solar cell characterizations.

B. Matlab User Interface for the Solar Cell Data Analysis

After obtaining the raw data in the solar cell characterizations, we still need to do the post data analysis to extract the specification parameters. Thus we developed the Matlab User Interface to do the data analysis for the data files obtained in Labview Programs. As shown in Figure B1, the data files can be loaded in a separated message window by clicking the menu item "Open Files", and the file names will be shown in the left list. The parameters including, V_{oc}, I_{sc}, J_{sc}, PCE, V@PCE, I@PCE, FF, R_s and R_{sh} will be calculated automatically based on the pre-set area and illumination, and the results will be listed in the lower table. The V_{oc} and R_s are extracted from the point of intersection with the X-axis, then the I_{sc}, J_{sc} and R_{sh} are extracted from the point intersection at the Y-axis, and the PCE is extracted at the point with highest product of applied voltage and measured current. We can select a certain data file in the list to show its IV curve in the middle graph and the corresponding parameters in the right panel. Finally, the extracted parameters for those selected data files can be saved in one excel file by clicking the menu item "Save Result".

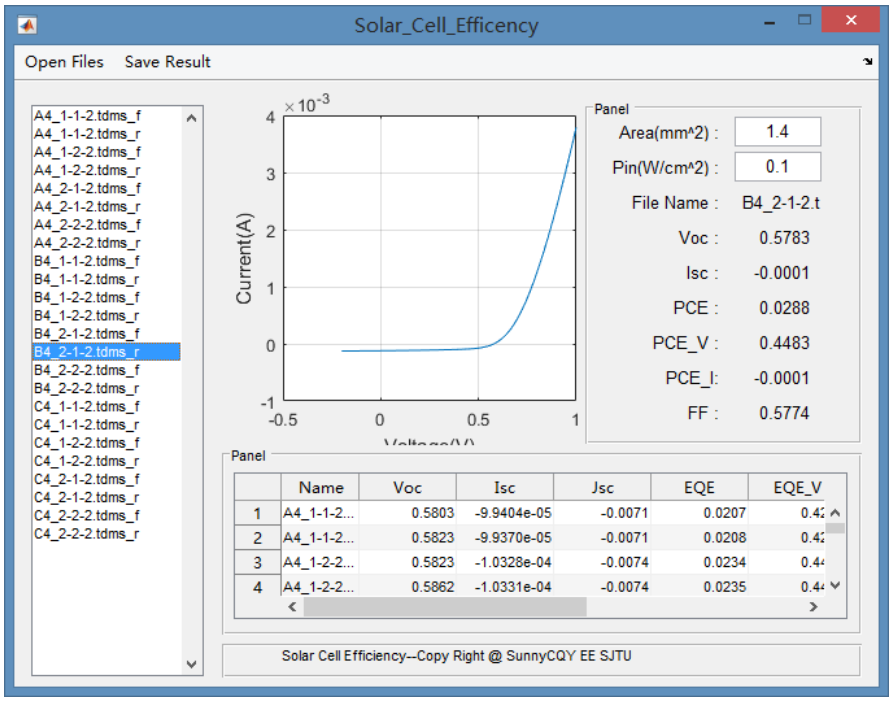

Figure B1. Matlab User Interface for the post data analysis.

```
% --------------------------------------------------------------------
function o_files_Callback(hObject, eventdata, handles)
% hObject    handle to o_files (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)
set(handles.f_list,'String',{});
global Pathname data_init result
[Filename,Pathname,Filterindex] =
uigetfile('*.tdms','MultiSelect','on');
if Filterindex==0
    return;
end
N_files = size(Filename,2);
set(handles.f_list,'Value',1);

if(iscell(Filename))
    f_list0 = Filename';
else
    f_list0 = {Filename};
    N_files = 1;
end
data_init=cell(N_files*2,2);
result=zeros(N_files*2,9);
f_list =cell(N_files*2,1);

for i=1:N_files
    f_name = f_list0{i};
    my_tdms_struct = TDMS_getStruct([Pathname,f_name]);
    L = length(fieldnames(my_tdms_struct));
    if(L == 2)
        Volt = my_tdms_struct.Untitled.Untitled.data;
        Curr = my_tdms_struct.Untitled.Untitled_1.data;
        L_volt = length(Volt );
        Volt_f = Volt(1:(L_volt/2));
        Curr_f = Curr(1:(L_volt/2));
        f_list{(i-1)*2+1} = [f_name,'_f'];
        data_init{(i-1)*2+1,1}=[f_name,'_f'];
        data_init{(i-1)*2+1,2}=[Volt_f',Curr_f'];
        Volt_r = Volt((L_volt/2 + 1):end);
        Curr_r = Curr((L_volt/2 + 1):end);
        f_list{(i-1)*2+2} = [f_name,'_r'];
        data_init{(i-1)*2+2,1}=[f_name,'_r'];
        data_init{(i-1)*2+2,2}=[Volt_r',Curr_r'];
    elseif(L == 3)
```

```
        Volt_f = my_tdms_struct.Untitled.Untitled.data;
        Curr_f = my_tdms_struct.Untitled.Untitled_1.data;
        f_list{(i-1)*2+1} = [f_name,'_f'];
        data_init{(i-1)*2+1,1}=[f_name,'_f'];
        data_init{(i-1)*2+1,2}=[Volt_f',Curr_f'];
        Volt_r = my_tdms_struct.Untitled_1.Untitled.data;
        Curr_r = my_tdms_struct.Untitled_1.Untitled_1.data;
        f_list{(i-1)*2+2} = [f_name,'_r'];
        data_init{(i-1)*2+2,1}=[f_name,'_r'];
        data_init{(i-1)*2+2,2}=[Volt_r',Curr_r'];
    end
end
set(handles.f_list, 'String',f_list);
calculation(handles);
refresh_fig(1,handles);
refresh_table(handles);


% --------------------------------------------------------------------
function s_files_Callback(hObject, eventdata, handles)
% hObject    handle to s_files (see GCBO)
% eventdata  reserved - to be defined in a future version of MATLAB
% handles    structure with handles and user data (see GUIDATA)
global Pathname
table_data=get(handles.uitable1,'Data');
if isempty(table_data)
    table_data=cell(0,9);
end
table_data = [{'File Name '}, {'Voc(V)'}, {'Isc(A)'}, {'Jsc(A/cm2)'},
{'PCE'},{'V at PCE(V)'},...
    {'I at PCE(A)'}, {'Fill Factor'}, {'R_series(ohm*cm2)'},
{'R_shunt(ohm*cm2)'}; table_data];
index = strfind(Pathname,'\');
if(length(index) > 1)
    index = index(end-1);
end

FolderName = Pathname((index+1):end-1);
xlswrite([Pathname,FolderName,'_Result.xls'],table_data);
```

Figure B2. Code samples for the module of loading data files and the module of saving results to the excel files.

Bibliography

[1] Wikipedia Silicon
[https://en.wikipedia.org/wiki/Silicon]

[2] Wikipedia Amorphous Silicon
[https://en.wikipedia.org/wiki/Amorphous_silicon]

[3] Wikipedia Doping(Semiconductor)
[https://en.wikipedia.org/wiki/Doping_(semiconductor)]

[4] R. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *IEEE Transactions on Electron Devices,* vol. 39, pp. 1704-1710, 1992.

[5] R. Xie, P. Montanini, K. Akarvardar, N. Tripathi, B. Haran, S. Johnson, *et al.*, "A 7nm FinFET technology featuring EUV patterning and dual strained high mobility channels," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 2.7.1-2.7.4.

[6] E. F. Zalewski and C. R. Duda, "Silicon photodiode device with 100% external quantum efficiency," *Applied Optics,* vol. 22, pp. 2867-2873, 1983.

[7] L. G. McIlrath, "A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion," *IEEE Journal of Solid-State Circuits,* vol. 36, pp. 846-853, 2001.

[8] I. Inoue, N. Tanaka, H. Yamashita, T. Yamaguchi, H. Ishiwata, and H. Ihara, "Low-leakage-current and low-operating-voltage buried photodiode for a CMOS imager," *IEEE Transactions on Electron Devices,* vol. 50, pp. 43-47, 2003.

[9] Wikipedia Polycrystalline_silicon
[https://en.wikipedia.org/wiki/Polycrystalline_silicon]

[10] M. Katayama, "TFT-LCD technology," *Thin Solid Films,* vol. 341, pp. 140-147, 1999.

[11] P. Agarwal and S. C. Agarwal, "Thermal equilibrium, the Staebler-Wronski effect and potential fluctuations in lithium-doped hydrogenated amorphous silicon," *Philosophical Magazine B,* vol. 80, pp. 1327-1346, 2000/07/01 2000.

[12] A. Kolodziej, "Staebler-Wronski effect in amorphous silicon and its alloys," *OPTO-Electronic Review,* vol. 12, p. 21, 2004.

[13] M. Stutzmann, W. B. Jackson, and C. C. Tsai, "Kinetics of the Staebler–Wronski effect in hydrogenated amorphous silicon," *Applied Physics Letters,* vol. 45, pp. 1075-1077, 1984.

[14] R. A. Street, "Hydrogenated Amorphous Silicon," 2010.

[15] R. Pagano, D. Corso, S. Lombardo, G. Valvo, D. N. Sanfilippo, G. Fallica, *et*

al., "Dark Current in Silicon Photomultiplier Pixels: Data and Model," *IEEE Transactions on Electron Devices*, vol. 59, pp. 2410-2416, 2012.

[16] LNF Wiki [http://lnf-wiki.eecs.umich.edu/wiki/Plasma_enhanced_chemical_vapor_ deposition]

[17] M. A. Green, "Thin-film solar cells: review of materials, technologies and commercial status," *Journal of Materials Science: Materials in Electronics*, vol. 18, pp. 15-19, 2007.

[18] T. D. Lee and A. U. Ebong, "A review of thin film solar cell technologies and challenges," *Renewable and Sustainable Energy Reviews*, vol. 70, pp. 1286-1297, 2017.

[19] R. T. Croswell, A. Reisman, D. L. Simpson, D. Temple, and C. K. Williams, "Planarization Processes and Applications III. As‐Deposited and Annealed Film Properties," *Journal of The Electrochemical Society*, vol. 147, pp. 1513-1524, April 1, 2000 2000.

[20] M. Bivour, J. Temmler, H. Steinkemper, and M. Hermle, "Molybdenum and tungsten oxide: High work function wide band gap contact materials for hole selective contacts of silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 142, pp. 34-41, 2015.

[21] Z. Liang, M. Su, Y. Zhou, L. Gong, C. Zhao, K. Chen, *et al.*, "Interaction at the silicon/transition metal oxide heterojunction interface and its effect on the photovoltaic performance," *Physical Chemistry Chemical Physics*, vol. 17, pp. 27409-27413, 2015.

[22] Wikipedia Solar Cell [https://en.wikipedia.org/wiki/Solar_cell]

[23] Wikipedia Photodiode [https://en.wikipedia.org/wiki/Photodiode]

[24] PVEducation.org Ideality Factor [https://www.pveducation.org/pvcdrom/solar-cell-operation/ideality-factor]

[25] P. T. Landsberg, "Trap‐Auger recombination in silicon of low carrier densities," *Applied Physics Letters*, vol. 50, pp. 745-747, 1987.

[26] R. Saive, C. Mueller, J. Schinke, R. Lovrincic, and W. Kowalsky, "Understanding S-shaped current-voltage characteristics of organic solar cells: Direct measurement of potential distributions by scanning Kelvin probe," *Applied Physics Letters*, vol. 103, p. 243303, 2013.

[27] W. Tress, A. Petrich, M. Hummert, M. Hein, K. Leo, and M. Riede, "Imbalanced mobilities causing S-shaped IV curves in planar heterojunction organic solar cells," *Applied Physics Letters*, vol. 98, p. 063301, 2011.

[28] D. S. Schneider, A. Bablich, and M. C. Lemme, "Flexible hybrid graphene/a-Si:H multispectral photodetectors," *Nanoscale*, vol. 9, pp. 8573-8579, 2017.

[29] M. R. Esmaeili-Rad and S. Salahuddin, "High Performance Molybdenum Disulfide Amorphous Silicon Heterojunction Photodetector," *Sci. Rep.*, vol. 3, 2013.

[30] K. A. Bush, A. F. Palmstrom, Z. J. Yu, M. Boccard, R. Cheacharoen, J. P. Mailoa, *et al.*, "23.6%-efficient monolithic perovskite/silicon tandem solar cells with improved stability," *Nature Energy*, vol. 2, pp. 17009, 2017.

[31] J. Kim, Z. Hong, G. Li, T.-b. Song, J. Chey, Y. S. Lee, *et al.*, "10.5% efficient

polymer and amorphous silicon hybrid tandem photovoltaic cell," *Nature Communications,* vol. 6, pp. 6391, 2015.

[32] F. Urbain, V. Smirnov, J.-P. Becker, U. Rau, J. Ziegler, B. Kaiser, *et al.*, "Application and modeling of an integrated amorphous silicon tandem based device for solar water splitting," *Solar Energy Materials and Solar Cells,* vol. 140, pp. 275-280, 2015.

[33] S. Y. Reece, J. A. Hamel, K. Sung, T. D. Jarvi, A. J. Esswein, J. J. H. Pijpers, *et al.*, "Wireless Solar Water Splitting Using Silicon-Based Semiconductors and Earth-Abundant Catalysts," *Science,* vol. 334, pp. 645-648, 2011.

[34] Wikipedia Auger Electron Spectroscopy [https://en.wikipedia.org/wiki/Auger_electron_spectroscopy]

[35] C. D. Wagner, D. A. Zatko, and R. H. Raymond, "Use of the oxygen KLL Auger lines in identification of surface chemical states by electron spectroscopy for chemical analysis," *Analytical Chemistry,* vol. 52, pp. 1445-1451, 1980.

[36] A. Domanowska, B. Adamowicz, P. Bidzinski, A. Klimasek, J. Szewczenko, GuttT, *et al.*, "Analysis of chemical shifts in Auger electron spectra versus sputtering time from passivated surfaces," *Optica Applicata,* vol. 41, pp. 441-447, 2011.

[37] R. Weiβmann, "Intensity ratios of the KL1L1, KL23L23 oxygen Auger lines in different compounds," *Solid State Communications,* vol. 31, pp. 347-349, 1979.

[38] J. F. Wager, "Transparent Electronics," *Science,* vol. 300, pp. 1245-1246, 2003.

[39] Wikipedia See-through display [https://en.wikipedia.org/wiki/See-through_display]

[40] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-Film Transistor Fabricated in Single-Crystalline Transparent Oxide Semiconductor," *Science,* vol. 300, pp. 1269-1272, 2003.

[41] T. Riedl, P. Gorrn, and W. Kowalsky, "Transparent Electronics for See-Through AMOLED Displays," *Journal of Display Technology,* vol. 5, pp. 501-508, 2009.

[42] T. Q. Trung, S. Ramasundaram, B.-U. Hwang, and N.-E. Lee, "An All-Elastomeric Transparent and Stretchable Temperature Sensor for Body-Attachable Wearable Electronics," *Advanced Materials,* vol. 28, pp. 502-509, 2016.

[43] J. Y. Lee, K.-T. Lee, S. Seo, and L. J. Guo, "Decorative power generating panels creating angle insensitive transmissive colors," *Scientific Reports,* vol. 4, p. 4192, 2014.

[44] Y. Li, J.-D. Lin, X. Che, Y. Qu, F. Liu, L.-S. Liao, *et al.*, "High Efficiency Near-Infrared and Semitransparent Non-Fullerene Acceptor Organic Photovoltaic Cells," *Journal of the American Chemical Society,* vol. 139, pp. 17114-17119, 2017.

[45] R. R. Lunt and V. Bulovic, "Transparent, near-infrared organic photovoltaic solar cells for window and energy-scavenging applications," *Applied Physics Letters,* vol. 98, p. 113305, 2011.

[46] C. J. Traverse, R. Pandey, M. C. Barr, and R. R. Lunt, "Emergence of highly

transparent photovoltaics for distributed applications," *Nature Energy,* vol. 2, pp. 849-860, 2017.

[47] M. Zhang, S. Hofle, J. Czolk, A. Mertens, and A. Colsmann, "All-solution processed transparent organic light emitting diodes," *Nanoscale,* vol. 7, pp. 20009-20014, 2015.

[48] K. Choi Moon, J. Yang, C. Kim Dong, Z. Dai, J. Kim, H. Seung, *et al.*, "Extremely Vivid, Highly Transparent, and Ultrathin Quantum Dot Light‐Emitting Diodes," *Advanced Materials,* vol. 30, p. 1703279, 2017.

[49] H. Moon, H. Cho, M. Kim, K. Takimiya, and S. Yoo, "Towards Colorless Transparent Organic Transistors: Potential of Benzothieno[3,2-b]benzothiophene-Based Wide-Gap Semiconductors," *Advanced Materials,* vol. 26, pp. 3105-3110, 2014.

[50] S. Dugu, S. P. Pavunny, T. B. Limbu, B. R. Weiner, G. Morell, and R. S. Katiyar, "A graphene integrated highly transparent resistive switching memory device," *APL Materials,* vol. 6, p. 058503, 2018.

[51] Y. Kwon, Y. Kim, H. Lee, C. Lee, and J. Kwak, "Composite film of poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) and MoO3 as an efficient hole injection layer for polymer light-emitting diodes," *Organic Electronics,* vol. 15, pp. 1083-1087, 2014.

[52] S. Murase and Y. Yang, "Solution Processed MoO3 Interfacial Layer for Organic Photovoltaics Prepared by a Facile Synthesis Method," *Advanced Materials,* vol. 24, pp. 2459-2462, 2012.

[53] I. A. de Castro, R. S. Datta, J. Z. Ou, A. Castellanos-Gomez, S. Sriram, T. Daeneke, *et al.*, "Molybdenum Oxides – From Fundamentals to Functionality," *Advanced Materials,* pp. 1701619.

[54] H. Siemund, F. Bröcker, and H. Göbel, "Enhancing the electron injection in polymer light-emitting diodes using a sodium stearate/aluminum bilayer cathode," *Organic Electronics,* vol. 14, pp. 335-343, 2013.

[55] J. Liang, X. Guo, L. Song, J. Lin, Y. Hu, N. Zhang, *et al.*, "Transparent perovskite light-emitting diodes by employing organic-inorganic multilayer transparent top electrodes," *Applied Physics Letters,* vol. 111, p. 213301, 2017.

[56] J. Huang, Z. Xu, and Y. Yang, "Low-Work-Function Surface Formed by Solution-Processed and Thermally Deposited Nanoscale Layers of Cesium Carbonate," *Advanced Functional Materials,* vol. 17, pp. 1966-1973, 2007.

[57] G. G. Andersson, M. P. de Jong, F. J. J. Janssen, J. M. Sturm, L. J. van Ijzendoorn, A. W. Denier van der Gon, *et al.*, "Influence of a partially oxidized calcium cathode on the performance of polymeric light emitting diodes," *Journal of Applied Physics,* vol. 90, pp. 1376-1382, 2001.

[58] Y. Zhou, C. Fuentes-Hernandez, J. Shim, J. Meyer, A. J. Giordano, H. Li, *et al.*, "A Universal Method to Produce Low–Work Function Electrodes for Organic Electronics," *Science,* vol. 336, pp. 327, 2012.

[59] H. H. Kim, S. Park, Y. Yi, D. I. Son, C. Park, D. K. Hwang, *et al.*, "Inverted Quantum Dot Light Emitting Diodes using Polyethylenimine ethoxylated modified ZnO," *Scientific Reports,* vol. 5, pp. 8968, 2015.

[60] S. Höfle, A. Schienle, M. Bruns, U. Lemmer, and A. Colsmann, "Enhanced Electron Injection into Inverted Polymer Light-Emitting Diodes by Combined Solution-Processed Zinc Oxide/Polyethylenimine Interlayers," *Advanced Materials*, vol. 26, pp. 2750-2754, 2014.

[61] Y.-H. Kim, T.-H. Han, H. Cho, S.-Y. Min, C.-L. Lee, and T.-W. Lee, "Polyethylene Imine as an Ideal Interlayer for Highly Efficient Inverted Polymer Light-Emitting Diodes," *Advanced Functional Materials*, vol. 24, pp. 3808-3814, 2014.

[62] A. K. K. Kyaw, D. H. Wang, V. Gupta, J. Zhang, S. Chand, G. C. Bazan, *et al.*, "Efficient Solution-Processed Small-Molecule Solar Cells with Inverted Structure," *Advanced Materials*, vol. 25, pp. 2397-2402, 2013.

[63] H. Kang, S. Hong, J. Lee, and K. Lee, "Electrostatically Self-Assembled Nonconjugated Polyelectrolytes as an Ideal Interfacial Layer for Inverted Polymer Solar Cells," *Advanced Materials*, vol. 24, pp. 3005-3009, 2012.

[64] T. M. Khan, Y. Zhou, A. Dindar, J. W. Shim, C. Fuentes-Hernandez, and B. Kippelen, "Organic Photovoltaic Cells with Stable Top Metal Electrodes Modified with Polyethylenimine," *ACS Applied Materials & Interfaces*, vol. 6, pp. 6202-6207, 2014.

[65] T. Tsujimura, Y. Kobayashi, K. Murayama, A. Tanaka, M. Morooka, E. Fukumoto, *et al.*, "4.1: A 20-inch OLED Display Driven by Super-Amorphous-Silicon Technology," *SID Symposium Digest of Technical Papers*, vol. 34, pp. 6-9, 2003.

[66] C. Kyuha, H. Mun Pyo, K. Chi Woo, and K. Innum, "Needs and solutions of future flat panel display for information technology industry," in *Digest. International Electron Devices Meeting*, 2002, pp. 385-388.

[67] H. Lee, J. Yoo, C. Kim, I. Chung, and J. Kanicki, "Asymmetric Electrical Properties of Corbino a-Si:H TFT and Concepts of Its Application to Flat Panel Displays," *IEEE Transactions on Electron Devices*, vol. 54, pp. 654-662, 2007.

[68] D. E. Carlson and C. R. Wronski, "Amorphous silicon solar cell," *Applied Physics Letters*, vol. 28, pp. 671-673, 1976.

[69] Y. Tawada, K. Tsuge, M. Kondo, H. Okamoto, and Y. Hamakawa, "Properties and structure of a‐SiC:H for high‐efficiency a‐Si solar cell," *Journal of Applied Physics*, vol. 53, pp. 5273-5281, 1982.

[70] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, *et al.*, "24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer," *IEEE Journal of Photovoltaics*, vol. 4, pp. 96-99, 2014.

[71] W. Qarony, M. I. Hossain, M. K. Hossain, M. J. Uddin, A. Haque, A. R. Saad, *et al.*, "Efficient amorphous silicon solar cells: characterization, optimization, and optical loss analysis," *Results in Physics*, vol. 7, pp. 4287-4293, 2017.

[72] A. V. Shah, H. Schade, M. Vanecek, J. Meier, E. Vallat-Sauvain, N. Wyrsch, *et al.*, "Thin-film silicon solar cell technology," *Progress in Photovoltaics: Research and Applications*, vol. 12, pp. 113-142, 2004.

[73] H. Iida, N. Shiba, T. Mishuku, A. Ito, H. Karasawa, M. Yamanaka, *et al.*, "High efficiency a-Si:H p-i-n solar cell using a SnO2/glass substrate," *IEEE Electron*

Device Letters, vol. 3, pp. 114-115, 1982.
[74] H. C. You, "Transistor Characteristics of Zinc Oxide Active Layers at Various Zinc Acetate Dihydrate Solution Concentrations of Zinc Oxide Thin-film," *Journal of Applied Research and Technology,* vol. 13, pp. 291-296, 2015.
[75] A. Bashir, P. H. Wöbkenberg, J. Smith, J. M. Ball, G. Adamopoulos, D. D. C. Bradley, *et al.*, "High-Performance Zinc Oxide Transistors and Circuits Fabricated by Spray Pyrolysis in Ambient Atmosphere," *Advanced Materials,* vol. 21, pp. 2226-2231, 2009.
[76] D. Kälblein, H. Ryu, F. Ante, B. Fenk, K. Hahn, K. Kern, *et al.*, "High-Performance ZnO Nanowire Transistors with Aluminum Top-Gate Electrodes and Naturally Formed Hybrid Self-Assembled Monolayer/AlOx Gate Dielectric," *ACS Nano,* vol. 8, pp. 6840-6848, 2014.
[77] P. Jinjoo, L. Seunghyup, and Y. Kijung, "Photo-stimulated resistive switching of ZnO nanorods," *Nanotechnology,* vol. 23, pp. 385707, 2012.
[78] O. Hisashi, M. Kouji, T. Yukichi, and I. Tadashi, "Structure of the Natural Oxide of Amorphous Silicon," *Japanese Journal of Applied Physics,* vol. 25, p. 1773, 1986.
[79] S. Khan, L. Lorenzelli, and R. S. Dahiya, "Technologies for Printing Sensors and Electronics Over Large Flexible Substrates: A Review," *IEEE Sensors Journal,* vol. 15, pp. 3164-3185, 2015.
[80] T. Sekitani and T. Someya, "Stretchable, Large-area Organic Electronics," *Advanced Materials,* vol. 22, pp. 2228-2246, 2010.
[81] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic Thin Film Transistors for Large Area Electronics," *Advanced Materials,* vol. 14, pp. 99-117, 2002.
[82] G. Eda and M. Chhowalla, "Chemically Derived Graphene Oxide: Towards Large-Area Thin-Film Electronics and Optoelectronics," *Advanced Materials,* vol. 22, pp. 2392-2415, 2010.
[83] M. Stoppa and A. Chiolerio, "Wearable Electronics and Smart Textiles: A Critical Review," *Sensors,* vol. 14, 2014.
[84] J. A. Rogers, T. Someya, and Y. Huang, "Materials and Mechanics for Stretchable Electronics," *Science,* vol. 327, pp. 1603-1607, 2010.
[85] S. K. Hau, H.-L. Yip, and A. K. Y. Jen, "A Review on the Development of the Inverted Polymer Solar Cell Architecture," *Polymer Reviews,* vol. 50, pp. 474-510, 2010.
[86] S. A. Vanalakar, G. L. Agawane, S. W. Shin, M. P. Suryawanshi, K. V. Gurav, K. S. Jeon, *et al.*, "A review on pulsed laser deposited CZTS thin films for solar cell applications," *Journal of Alloys and Compounds,* vol. 619, pp. 109-121, 2015.
[87] B. Parida, S. Iniyan, and R. Goic, "A review of solar photovoltaic technologies," *Renewable and Sustainable Energy Reviews,* vol. 15, pp. 1625-1636, 2011.
[88] E. Fresta and R. D. Costa, "Beyond traditional light-emitting electrochemical cells – a review of new device designs and emitters," *Journal of Materials Chemistry C,* vol. 5, pp. 5643-5675, 2017.
[89] S. Ho, S. Liu, Y. Chen, and F. So, "Review of recent progress in multilayer

solution-processed organic light-emitting diodes," *Journal of Photonics for Energy,* vol. 5, pp. 1-17, 17, 2015.

[90] Y. Liu, C. Li, Z. Ren, S. Yan, and M. R. Bryce, "All-organic thermally activated delayed fluorescence materials for organic light-emitting diodes," *Nature Reviews Materials,* vol. 3, p. 18020, 2018.

[91] J.-H. Jou, S. Kumar, A. Agrawal, T.-H. Li, and S. Sahoo, "Approaches for fabricating high efficiency organic light emitting diodes," *Journal of Materials Chemistry C,* vol. 3, pp. 2974-3002, 2015.

[92] Y. Xia, K. Sun, and J. Ouyang, "Solution-Processed Metallic Conducting Polymer Films as Transparent Electrode of Optoelectronic Devices," *Advanced Materials,* vol. 24, pp. 2436-2440, 2012.

[93] Y. H. Kim, C. Sachse, M. L. Machala, C. May, L. Müller-Meskamp, and K. Leo, "Highly Conductive PEDOT:PSS Electrode with Optimized Solvent and Thermal Post-Treatment for ITO-Free Organic Solar Cells," *Advanced Functional Materials,* vol. 21, pp. 1076-1081, 2011.

[94] S. Pang, Y. Hernandez, X. Feng, and K. Müllen, "Graphene as Transparent Electrode Material for Organic Electronics," *Advanced Materials,* vol. 23, pp. 2779-2795, 2011.

[95] M. W. Rowell, M. A. Topinka, M. D. McGehee, H.-J. Prall, G. Dennler, N. S. Sariciftci, *et al.*, "Organic solar cells with carbon nanotube network electrodes," *Applied Physics Letters,* vol. 88, p. 233506, 2006.

[96] M.-G. Kang and L. J. Guo, "Nanoimprinted Semitransparent Metal Electrodes and Their Application in Organic Light-Emitting Diodes," *Advanced Materials,* vol. 19, pp. 1391-1396, 2007.

[97] L. Hu, H. S. Kim, J.-Y. Lee, P. Peumans, and Y. Cui, "Scalable Coating and Properties of Transparent, Flexible, Silver Nanowire Electrodes," *ACS Nano,* vol. 4, pp. 2955-2963, 2010.

[98] T. L. Belenkova, D. Rimmerman, E. Mentovich, H. Gilon, N. Hendler, S. Richter, *et al.*, "UV induced formation of transparent Au–Ag nanowire mesh film for repairable OLED devices," *Journal of Materials Chemistry,* vol. 22, pp. 24042-24047, 2012.

[99] A. Khan, S. Lee, T. Jang, Z. Xiong, C. Zhang, J. Tang, *et al.*, "High-Performance Flexible Transparent Electrode with an Embedded Metal Mesh Fabricated by Cost-Effective Solution Process," *Small,* vol. 12, pp. 3021-3030, 2016.

[100] J. W. Huh, D. K. Lee, H.-J. Jeon, and C. W. Ahn, "New approach for fabricating hybrid-structured metal mesh films for flexible transparent electrodes by the combination of electrospinning and metal deposition," *Nanotechnology,* vol. 27, p. 475302, 2016.

[101] X. Chen, W. Guo, L. Xie, C. Wei, J. Zhuang, W. Su, *et al.*, "Embedded Ag/Ni Metal-Mesh with Low Surface Roughness As Transparent Conductive Electrode for Optoelectronic Applications," *ACS Applied Materials & Interfaces,* vol. 9, pp. 37048-37054, 2017.

[102] K.-T. Park, H.-J. Kim, M.-J. Park, J.-H. Jeong, J. Lee, D.-G. Choi, *et al.*, "13.2% efficiency Si nanowire/PEDOT:PSS hybrid solar cell using a transfer-imprinted

Au mesh electrode," *Scientific Reports,* vol. 5, p. 12093, 2015.
[103] Y.-H. Liu, J.-L. Xu, S. Shen, X.-L. Cai, L.-S. Chen, and S.-D. Wang, "High-performance, ultra-flexible and transparent embedded metallic mesh electrodes by selective electrodeposition for all-solid-state supercapacitor applications," *Journal of Materials Chemistry A,* vol. 5, pp. 9032-9041, 2017.
[104] X. He, R. He, Q. Lan, W. Wu, F. Duan, J. Xiao, *et al.*, "Screen-Printed Fabrication of PEDOT:PSS/Silver Nanowire Composite Films for Transparent Heaters," *Materials,* vol. 10, 2017.
[105] J. W. Han, B. Jung, D. W. Kim, K. T. Lim, S.-Y. Jeong, and Y. H. Kim, "Transparent conductive hybrid thin-films based on copper-mesh/conductive polymer for ITO-Free organic light-emitting diodes," *Organic Electronics,* vol. 73, pp. 13-17, 2019.
[106] M. Gruber, A. Müller, V. Jovanov, M. J. Walter, and V. Wagner, "Direct Visualization of Charge-Extraction in Metal-Mesh Based OPV Cells by Light-Biased LBIC," *IEEE Journal of Photovoltaics,* vol. 7, pp. 1042-1049, 2017.
[107] C. Zhang, P. Chen, and W. Hu, "Organic field-effect transistor-based gas sensors," *Chemical Society Reviews,* vol. 44, pp. 2087-2107, 2015.
[108] Y. Chu, X. Wu, J. Lu, D. Liu, J. Du, G. Zhang, *et al.*, "Photosensitive and Flexible Organic Field-Effect Transistors Based on Interface Trapping Effect and Their Application in 2D Imaging Array," *Advanced Science,* vol. 3, p. 1500435, 2016.
[109] P. J. Diemer, Z. A. Lamport, Y. Mei, J. W. Ward, K. P. Goetz, W. Li, *et al.*, "Quantitative analysis of the density of trap states at the semiconductor-dielectric interface in organic field-effect transistors," *Applied Physics Letters,* vol. 107, p. 103303, 2015.
[110] R. Liguori, H. Usta, S. Fusco, A. Facchetti, G. D. Licciardo, L. D. Benedetto, *et al.*, "Insights Into Interface Treatments in p-Channel Organic Thin-Film Transistors Based on a Novel Molecular Semiconductor," *IEEE Transactions on Electron Devices,* vol. 64, pp. 2338-2344, 2017.
[111] Q. Burlingame, C. Coburn, X. Che, A. Panda, Y. Qu, and S. R. Forrest, "Centimetre-scale electron diffusion in photoactive organic heterostructures," *Nature,* vol. 554, p. 77, 2018.
[112] C. Tang, Z. Yan, Q. Wang, J. Chen, M. Zhu, B. Liu, *et al.*, "Ultrathin amorphous silicon thin-film solar cells by magnetic plasmonic metamaterial absorbers," *RSC Advances,* vol. 5, pp. 81866-81874, 2015.
[113] Z.-F. Huang, J. Song, L. Pan, X. Zhang, L. Wang, and J.-J. Zou, "Tungsten Oxides for Photocatalysis, Electrochemistry, and Phototherapy," *Advanced Materials,* vol. 27, pp. 5309-5327, 2015.
[114] C. Lin, C. Wu, P. Chen, P. Lai, J. Yu, C. Chang, *et al.*, "Optical Pixel Sensor of Hydrogenated Amorphous Silicon Thin-Film Transistor Free of Variations in Ambient Illumination," *IEEE Journal of Solid-State Circuits,* vol. 51, pp. 2777-2785, 2016.
[115] C. Lin, C. Wu, C. Lee, F. Chen, Y. Lin, W. Wu, *et al.*, "Alternately Controlled Optical Pixel Sensor System Using Amorphous Silicon Thin-Film Transistors,"

IEEE Transactions on Industrial Electronics, vol. 66, pp. 7366-7375, 2019.

[116] L. Wang, H. Ou, J. Chen, and K. Wang, "A Numerical Study of an Amorphous SiliconDual-Gate Photo Thin-Film Transistor for Low-DoseX-Ray Imaging," *Journal of Display Technology,* vol. 11, pp. 646-651, 2015.

[117] Y. C. Kim, K. H. Kim, D.-Y. Son, D.-N. Jeong, J.-Y. Seo, Y. S. Choi, *et al.*, "Printable organometallic perovskite enables large-area, low-dose X-ray imaging," *Nature,* vol. 550, p. 87, 10/04/online 2017.

[118] X. Liu, H. Ou, J. Chen, S. Deng, N. Xu, and K. Wang, "Highly Photosensitive Dual-Gate a-Si:H TFT and Array for Low-Dose Flat-Panel X-Ray Imaging," *IEEE Photonics Technology Letters,* vol. 28, pp. 1952-1955, 2016.

[119] Y. Liao, C. Chang, C. Lin, J. You, H. Hsieh, J. Chen, *et al.*, "Flat panel fingerprint optical sensor using TFT technology," in *2015 IEEE SENSORS*, 2015, pp. 1-4.

[120] Y. Lu, H. Tang, S. Fung, Q. Wang, J. M. Tsai, M. Daneman, *et al.*, "Ultrasonic fingerprint sensor using a piezoelectric micromachined ultrasonic transducer array integrated with complementary metal oxide semiconductor electronics," *Applied Physics Letters,* vol. 106, p. 263503, 2015.

[121] H. Tang, Y. Lu, X. Jiang, E. J. Ng, J. M. Tsai, D. A. Horsley, *et al.*, "3-D Ultrasonic Fingerprint Sensor-on-a-Chip," *IEEE Journal of Solid-State Circuits,* vol. 51, pp. 2522-2533, 2016.

[122] B. W. An, S. Heo, S. Ji, F. Bien, and J.-U. Park, "Transparent and flexible fingerprint sensor array with multiplexed detection of tactile pressure and skin temperature," *Nature Communications,* vol. 9, p. 2458, 2018.

[123] H. Ma, Z. Liu, S. Heo, J. Lee, K. Na, H. B. Jin, *et al.*, "On-Display Transparent Half-Diamond Pattern Capacitive Fingerprint Sensor Compatible With AMOLED Display," *IEEE Sensors Journal,* vol. 16, pp. 8124-8131, 2016.

[124] J. Lan, A. Cole, J. VanZandt, A. Dickinson, F. v. d. Ven, N. Bird, *et al.*, "Fingerprint imager based on a-Si:H active-matrix photo-diode arrays," in *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*, 2000, pp. 419-422.

[125] S. Heck and H. M. Branz, "Fingerprints of two distinct defects causing light-induced photoconductivity degradation in hydrogenated amorphous silicon," *Applied Physics Letters,* vol. 79, pp. 3080-3082, 2001.

[126] M. Vieira, M. Fernandes, P. Louro, Y. Vygranenko, A. Fantoni, R. Schwarz, *et al.*, "Image capture devices based on p–i–n silicon carbides for biometric applications," *Journal of Non-Crystalline Solids,* vol. 299-302, pp. 1245-1249, 2002.

[127] X. Zhou, M. Zhang, Y. Xu, W. Zhou, K. Wang, A. Nathan, *et al.*, "39-2: Highly Sensitive a-Si:H PIN Photodiode Gated LTPS TFT for Optical In-Display Fingerprint Identification," *SID Symposium Digest of Technical Papers,* vol. 49, pp. 490-493, 2018.

[128] G. De Cesare, A. Nascetti, and D. Caputo, "Amorphous Silicon p-i-n Structure Acting as Light and Temperature Sensor," *Sensors,* vol. 15, 2015.

[129] I. UDT Sensors, "Photodiode Characteristics and Applications."

[130] J. U. Ha, K. Kim, S. Yoon, K. M. Sim, J. Cho, and D. S. Chung, "Synergetic Effect of a Surfactant on the Facile Fabrication and High Detectivity of an Inverted Organic Bulk Heterojunction Photodiode," *ACS Photonics,* vol. 4, pp. 2085-2090, 2017.

[131] M. Biele, C. Montenegro Benavides, J. Hürdler, S. F. Tedde, C. J. Brabec, and O. Schmidt, "Spray-Coated Organic Photodetectors and Image Sensors with Silicon-Like Performance," *Advanced Materials Technologies,* vol. 4, p. 1800158, 2019.

[132] D. R. Santos, R. R. G. Soares, V. Chu, and J. P. Conde, "Performance of Hydrogenated Amorphous Silicon Thin Film Photosensors at Ultra-Low Light Levels: Towards Attomole Sensitivities in Lab-on-Chip Biosensing Applications," *IEEE Sensors Journal,* vol. 17, pp. 6895-6903, 2017.

[133] B. Liu, X. Shi, S. Cai, X. Cai, X. Lan, G. Chen, *et al.*, "71-2: Novel Optical Image Sensor Array Using LTPS-TFT Backplane Technology as Fingerprint Recognition," *SID Symposium Digest of Technical Papers,* vol. 50, pp. 1004-1006, 2019.

[134] Y. Chen, D. Geng, and J. Jang, "P-24: Integrated Gate Driver for 2700-ppi 8K 120Hz Displays using a-IGZO TFTs," *SID Symposium Digest of Technical Papers,* vol. 49, pp. 1268-1271, 2018.

[135] T. Li, K. Xie, Q. Wang, H. Tan, Y. Shen, and M. Chen, *Research on colorimetric characterization of LCD based on cubic polynomials curve model* vol. 11048: SPIE, 2019.

[136] T. Li, K. Xie, Q. Wang, Y. Zhang, and Z. Zhu, *Research on colorimetric characterization of LCD based on the steepest descent method* vol. 11048: SPIE, 2019.

[137] K. Watanabe, K. Toyotaka, H. Shishido, S. Kawashima, K. Kusunoki, Y. Nakazawa, *et al.*, "P-7: A 65-in. 8K LCD and OLED Display Using Cloud-Aligned Composite Oxide-Semiconductor (CAC-OS) FET," *SID Symposium Digest of Technical Papers,* vol. 48, pp. 1250-1253, 2017.

[138] K. Kusunoki, S. Kawashima, K. Watanabe, K. Toyotaka, R. Hatsumi, S. Yoshitomi, *et al.*, "37-1: Liquid Crystal Display Panel with a Pixel Including Oxide Semiconductor Field-Effect Transistor Memory (Pixel AI)," *SID Symposium Digest of Technical Papers,* vol. 50, pp. 512-515, 2019.

[139] X.-H. Xia, W.-J. Wu, G.-M. Li, L. Zhou, L.-R. Zhang, H.-L. Ning, *et al.*, "Letter: A new compensation pixel circuit with metal oxide thin-film transistors for active-matrix organic light-emitting diode displays," *Journal of the Society for Information Display,* vol. 23, pp. 233-239, 2015.

[140] C. Fan, Y. Chen, C. Yang, Y. Tsai, and B. Huang, "Novel LTPS-TFT Pixel Circuit with OLED Luminance Compensation for 3D AMOLED Displays," *Journal of Display Technology,* vol. 12, pp. 425-428, 2016.

[141] J. Gubbi, R. Buyya, S. Marusic, and M. Palaniswami, "Internet of Things (IoT): A vision, architectural elements, and future directions," *Future Generation Computer Systems,* vol. 29, pp. 1645-1660, 2013.

[142] A. Zanella, N. Bui, A. Castellani, L. Vangelista, and M. Zorzi, "Internet of

Things for Smart Cities," *IEEE Internet of Things Journal,* vol. 1, pp. 22-32, 2014.

[143] L. D. Xu, W. He, and S. Li, "Internet of Things in Industries: A Survey," *IEEE Transactions on Industrial Informatics,* vol. 10, pp. 2233-2243, 2014.

[144] C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, *et al.*, "Analogue signal and image processing with large memristor crossbars," *Nature Electronics,* vol. 1, pp. 52-59, 2018.

[145] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, *et al.*, "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nature Materials,* vol. 16, p. 101, 2016.

[146] Y. van de Burgt, E. Lubberman, E. J. Fuller, S. T. Keene, G. C. Faria, S. Agarwal, *et al.*, "A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing," *Nature Materials,* vol. 16, p. 414, 2017.

[147] C. Wang, W. He, Y. Tong, and R. Zhao, "Investigation and Manipulation of Different Analog Behaviors of Memristor as Electronic Synapse for Neuromorphic Applications," *Scientific Reports,* vol. 6, p. 22970, 2016.

[148] L. Qingjiang, A. Khiat, I. Salaoru, C. Papavassiliou, X. Hui, and T. Prodromakis, "Memory Impedance in TiO2 based Metal-Insulator-Metal Devices," *Scientific Reports,* vol. 4, p. 4522, 2014.

[149] M.-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, *et al.*, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5−x/TaO2−x bilayer structures," *Nat Mater,* vol. 10, pp. 625-630, 2011.

[150] S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin, and Q. Xia, "Nanoscale memristive radiofrequency switches," *Nat Commun,* vol. 6, 2015.

[151] Y. Aoki, C. Wiemann, V. Feyer, H.-S. Kim, C. M. Schneider, H. Ill-Yoo, *et al.*, "Bulk mixed ion electron conduction in amorphous gallium oxide causes memristive behaviour," *Nat Commun,* vol. 5, 2014.

[152] J. J. Yang, M. D. Pickett, X. Li, A. A. OhlbergDouglas, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal//oxide//metal nanodevices," *Nat Nano,* vol. 3, pp. 429-433, 2008.

[153] T. Chang, S.-H. Jo, K.-H. Kim, P. Sheridan, S. Gaba, and W. Lu, "Synaptic behaviors and modeling of a metal oxide memristive device," *Applied Physics A,* vol. 102, pp. 857-863, 2011.

[154] C. Du, W. Ma, T. Chang, P. Sheridan, and W. D. Lu, "Biorealistic Implementation of Synaptic Functions with Oxide Memristors through Internal Ionic Dynamics," *Advanced Functional Materials,* vol. 25, pp. 4290-4299, 2015.

[155] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Letters,* vol. 10, pp. 1297-1301, 2010.

[156] S. Li, N. Liu, X.-h. Zhang, D. Zhou, and D. Cai, "Bilinearity in Spatiotemporal Integration of Synaptic Inputs," *PLOS Computational Biology,* vol. 10, p. e1004014, 2014.

[157] N. Ghaffarian, M. Mesgari, M. Cerina, K. Göbel, T. Budde, E.-J. Speckmann,

et al., "Thalamocortical-auditory network alterations following cuprizone‐induced demyelination," *Journal of Neuroinflammation*, vol. 13, p. 160, 2016.
[158] V. Bulovic, G. Gu, P. E. Burrows, S. R. Forrest, and M. E. Thompson, "Transparent light-emitting devices," *Nature*, vol. 380, p. 29, 1996.
[159] Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. B. Mannsfeld, J. Chen, *et al.*, "Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method," *Nat Commun*, vol. 5, 2014.
[160] C. Zhang, D. Zhao, D. Gu, H. Kim, T. Ling, Y.-K. R. Wu, *et al.*, "An Ultrathin, Smooth, and Low-Loss Al-Doped Ag Film and Its Application as a Transparent Electrode in Organic Photovoltaics," *Advanced Materials*, vol. 26, pp. 5696-5701, 2014.
[161] D. Gu, C. Zhang, Y.-K. Wu, and L. J. Guo, "Ultrasmooth and Thermally Stable Silver-Based Thin Films with Subnanometer Roughness by Aluminum Doping," *ACS Nano*, vol. 8, pp. 10343-10351, 2014.
[162] H. Kang, S. Jung, S. Jeong, G. Kim, and K. Lee, "Polymer-metal hybrid transparent electrodes for flexible electronics," *Nat Commun*, vol. 6, 2015.
[163] B. Tian, G. Williams, D. Ban, and H. Aziz, "Transparent organic light-emitting devices using a MoO3/Ag/MoO3 cathode," *Journal of Applied Physics*, vol. 110, p. 104507, 2011.
[164] K. Hong, K. Kim, S. Kim, I. Lee, H. Cho, S. Yoo, *et al.*, "Optical Properties of WO3/Ag/WO3 Multilayer As Transparent Cathode in Top-Emitting Organic Light Emitting Diodes," *The Journal of Physical Chemistry C*, vol. 115, pp. 3453-3459, 2011.
[165] J. W. Seo, J.-W. Park, K. S. Lim, J.-H. Yang, and S. J. Kang, "Transparent resistive random access memory and its characteristics for nonvolatile resistive switching," *Applied Physics Letters*, vol. 93, p. 223505, 2008.
[166] D. B. Migas, V. L. Shaposhnikov, and V. E. Borisenko, "Tungsten oxides. II. The metallic nature of Magnéli phases," *Journal of Applied Physics*, vol. 108, p. 093714, 2010.
[167] D. B. Migas, V. L. Shaposhnikov, V. N. Rodin, and V. E. Borisenko, "Tungsten oxides. I. Effects of oxygen vacancies and doping on electronic and optical properties of different phases of WO3," *Journal of Applied Physics*, vol. 108, p. 093713, 2010.
[168] R. Chatten, A. V. Chadwick, A. Rougier, and P. J. D. Lindan, "The Oxygen Vacancy in Crystal Phases of WO3," *The Journal of Physical Chemistry B*, vol. 109, pp. 3146-3156, 2005.
[169] T. Chiang and J. F. Wager, "Electronic Conduction Mechanisms in Insulators," *IEEE Transactions on Electron Devices*, vol. 65, pp. 223-230, 2018.
[170] F.-C. Chiu, "A Review on Conduction Mechanisms in Dielectric Films," *Advances in Materials Science and Engineering*, vol. 2014, p. 18, 2014.
[171] S. Kumar, M. D. Pickett, J. P. Strachan, G. Gibson, Y. Nishi, and R. S. Williams, "Local Temperature Redistribution and Structural Transition During Joule-Heating-Driven Conductance Switching in VO2," *Advanced Materials*, vol. 25, pp. 6128-6132, 2013.

[172] Y. Meng Lu, M. Noman, Y. N. Picard, J. A. Bain, P. A. Salvador, and M. Skowronski, "Impact of Joule heating on the microstructure of nanoscale TiO2 resistive switching devices," *Journal of Applied Physics,* vol. 113, p. 163703, 2013.

[173] J. L. Tedesco, L. Stephey, M. Hernández-Mora, C. A. Richter, and N. Gergel-Hackett, "Switching mechanisms in flexible solution-processed TiO2memristors," *Nanotechnology,* vol. 23, p. 305206, 2012.

[174] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, pp. 488-492, 2004.

[175] J.-M. Choi, D. K. Hwang, J. H. Kim, and S. Im, "Transparent thin-film transistors with pentacene channel, AlOx gate, and NiOx electrodes," *Applied Physics Letters,* vol. 86, p. 123505, 2005.

[176] J. Lee, D. K. Hwang, J.-M. Choi, K. Lee, J. H. Kim, S. Im, *et al.*, "Flexible semitransparent pentacene thin-film transistors with polymer dielectric layers and NiOx electrodes," *Applied Physics Letters,* vol. 87, p. 023504, 2005.

[177] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Gonçalves, A. J. S. Marques, L. M. N. Pereira, *et al.*, "Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature," *Advanced Materials,* vol. 17, pp. 590-594, 2005.

[178] Q. Cao, S. H. Hur, Z. T. Zhu, Y. G. Sun, C. J. Wang, M. A. Meitl, *et al.*, "Highly Bendable, Transparent Thin-Film Transistors That Use Carbon-Nanotube-Based Conductors and Semiconductors with Elastomeric Dielectrics," *Advanced Materials,* vol. 18, pp. 304-309, 2006.

[179] K. Pei, Z. Wang, X. Ren, Z. Zhang, B. Peng, and P. K. L. Chan, "Fully transparent organic transistors with junction-free metallic network electrodes," *Applied Physics Letters,* vol. 107, p. 033302, 2015.

[180] S.-J. Kim, J.-M. Song, and J.-S. Lee, "Transparent organic thin-film transistors and nonvolatile memory devices fabricated on flexible plastic substrates," *Journal of Materials Chemistry,* vol. 21, pp. 14516-14522, 2011.

[181] C.-a. Di, G. Yu, Y. Liu, Y. Guo, Y. Wang, W. Wu, *et al.*, "High-Performance Organic Field-Effect Transistors with Low-Cost Copper Electrodes," *Advanced Materials,* vol. 20, pp. 1286-1290, 2008.

[182] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi, "Contact-metal dependent current injection in pentacene thin-film transistors," *Applied Physics Letters,* vol. 91, p. 203508, 2007.

[183] C.-a. Di, G. Yu, Y. Liu, Y. Guo, X. Sun, J. Zheng, *et al.*, "Effect of dielectric layers on device stability of pentacene-based field-effect transistors," *Physical Chemistry Chemical Physics,* vol. 11, pp. 7268-7273, 2009.

[184] W. Wei, H. Jinhua, Y. Jun, and X. Wenfa, "MoO3 Modification Layer to Enhance Performance of Pentacene-OTFTs With Various Low-Cost Metals as Source/Drain Electrodes," *Electron Devices, IEEE Transactions on,* vol. 61, pp. 3507-3512, 2014.

[185] D. Kumaki, T. Umeda, and S. Tokito, "Reducing the contact resistance of

bottom-contact pentacene thin-film transistors by employing a MoOx carrier injection layer," *Applied Physics Letters,* vol. 92, p. 013301, 2008.

[186] C.-W. Chu, S.-H. Li, C.-W. Chen, V. Shrotriya, and Y. Yang, "High-performance organic thin-film transistors with metal oxide/metal bilayer electrode," *Applied Physics Letters,* vol. 87, p. 193508, 2005.

[187] V. J. Logeeswaran, N. P. Kobayashi, M. S. Islam, W. Wu, P. Chaturvedi, N. X. Fang, *et al.*, "Ultrasmooth Silver Thin Films Deposited with a Germanium Nucleation Layer," *Nano Letters,* vol. 9, pp. 178-182, 2009.

[188] W. Chen, K. P. Chen, M. D. Thoreson, A. V. Kildishev, and V. M. Shalaev, "Ultrathin, ultrasmooth, and low-loss silver films via wetting and annealing," *Applied Physics Letters,* vol. 97, p. 211107, 2010.

[189] N. Formica, D. S. Ghosh, A. Carrilero, T. L. Chen, R. E. Simpson, and V. Pruneri, "Ultrastable and Atomically Smooth Ultrathin Silver Films Grown on a Copper Seed Layer," *ACS Applied Materials & Interfaces,* vol. 5, pp. 3048-3053, 2013.

[190] P. V. Pesavento, K. P. Puntambekar, C. D. Frisbie, J. C. McKeen, and P. P. Ruden, "Film and contact resistance in pentacene thin-film transistors: Dependence on film thickness, electrode geometry, and correlation with hole mobility," *Journal of Applied Physics,* vol. 99, p. 094504, 2006.

[191] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Metal/graphene contact as a performance Killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance," in *2009 IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1-4.

[192] D.-T. Nguyen, S. Vedraine, L. Cattin, P. Torchio, M. Morsli, F. Flory, *et al.*, "Effect of the thickness of the MoO3 layers on optical properties of MoO3/Ag/MoO3 multilayer structures," *Journal of Applied Physics,* vol. 112, p. 063505, 2012.

[193] National Instrument [https://www.ni.com/en-us/shop/labview.html]