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# High-Performance Zinc Tin Oxide TFTs with Active Layers Deposited by Atomic Layer Deposition

*Christopher R. Allemang, Tae H. Cho, Orlando Trejo, Shantam Ravan, Robin E. Rodríguez, Neil P. Dasgupta,* and Rebecca L. Peterson**

**New deposition techniques for amorphous oxide semiconductors compatible with silicon back end of line manufacturing are needed for 3D monolithic integration of thin-film electronics. Here, three atomic layer deposition (ALD) processes are compared for the fabrication of amorphous zinc tin oxide (ZTO) channels in bottom-gate, top-contact n-channel transistors. As-deposited ZTO films, made by ALD at 150–200 °C, exhibit semiconducting, enhancement-mode behavior with electron mobility as high as 13 cm$^2$ V$^{-1}$ s$^{-1}$, due to a low density of oxygen-related defects. ZTO deposited at 200 °C using a hybrid thermal-plasma ALD process with an optimal tin composition of 21%, post-annealed at 400 °C, shows excellent performance with a record high mobility of 22.1 cm$^2$ V$^{-1}$ s$^{-1}$ and a subthreshold slope of 0.29 V dec$^{-1}$. Increasing the deposition temperature and performing post-deposition anneals at 300–500 °C lead to an increased density of the X-ray amorphous ZTO film, improving its electrical properties. By optimizing the ZTO active layer thickness and using a high-*k* gate insulator (ALD $Al_2O_3$), the transistor switching voltage is lowered, enabling electrical compatibility with silicon integrated circuits. This work opens the possibility of monolithic integration of ALD ZTO-based thin-film electronics with silicon integrated circuits or onto large-area flexible substrates.**

## 1. Introduction

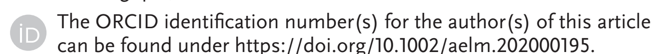
Transparent amorphous oxide semiconductors (TAOSs) are gaining traction in thin-film transistor (TFT) applications because the overlap of metal *ns* orbitals allows for superior electron transport in TAOS films compared to amorphous-Si and organic semiconductors.[1] The high optical transparency, amorphous morphology, and large-area process capability of TAOS films have led to their commercial application in display backplanes.[2,3] One of the most important future applications of TAOS is back end of line (BEOL) 3D monolithic integration on top of silicon complementary metal oxide semiconductor integrated circuits (CMOS ICs).[4] However, this application requires a temperature budget of less than approximately 450 °C,[5] an electron mobility of greater than 20 cm$^2$ V$^{-1}$ s$^{-1}$, normally-off enhancement-mode behavior, and switching voltages (the difference between the threshold voltage and turn-on voltage) of a few volts or less to provide sufficient current drive and supply-voltage compatibility with CMOS ICs. Indium gallium zinc oxide (IGZO) is one of the most extensively researched TAOS and has been manufactured commercially.[6] Zinc tin oxide (ZTO) is an attractive alternative to IGZO because it consists of the earth-abundant elements zinc and tin, instead of comparatively scarce and costly indium and gallium.[7]

ZTO can be deposited using solution processing[8] or vacuum-based processes like pulsed laser deposition,[9] sputtering,[10–12] and atomic layer deposition (ALD).[13,14] In this study, ALD—a self-limiting, vapor-phase deposition method—is used as a low-temperature process that allows precise control of semiconductor film interfaces, stoichiometry, and thickness.[15,16] Binary metal oxides (e.g., ZnO) are grown by ALD by exposing the substrate surface to a metal precursor that reacts with surface functional groups, followed by an oxidizing step such as oxygen plasma, water, hydrogen peroxide, or ozone to incorporate oxygen and react with the metal precursor ligands. By repeating this process in a cyclic manner, the thickness of the film can be controlled with sub-nm precision. Ternary oxides can also be deposited using ALD by combining two binary processes into a supercycle.[17–19] A supercycle combines and repeats the different binary ALD processes to deposit a multi-component film with the desired composition, as shown in **Figure 1**a.

Previous reports on high-performance TFTs with a-IGZO,[20,21] indium zinc tin oxide,[22,23] or indium gallium zinc tin oxide[24] channel materials deposited by ALD showed field-effect mobilities as high as 74, 26.8, and 46.7 cm$^2$ V$^{-1}$ s$^{-1}$, respectively, but contained scarce and costly indium and required a more complex quaternary or quinary alloy process. There have been several reports of indium-free ternary ZTO deposited by

C. R. Allemang, S. Ravan, Prof. R. L. Peterson
Electrical Engineering and Computer Science Department
University of Michigan
Ann Arbor, MI 48109-2122, USA
E-mail: blpeters@umich.edu

T. H. Cho, Dr. O. Trejo, R. E. Rodríguez, Prof. N. P. Dasgupta
Department of Mechanical Engineering
University of Michigan
Ann Arbor, MI 48109-2125, USA
E-mail: ndasgupt@umich.edu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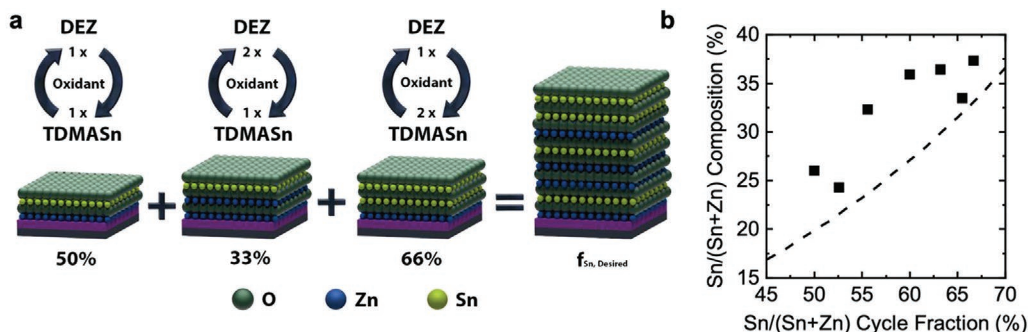


**Figure 1.** a) Schematic representation of a ZTO ALD supercycle. The supercycle is composed of sub-supercycles with $f_{Sn}$ = 50%, 33%, and/or 66%, shown left to right. These sub-supercycles can be combined in any order and repeated as needed within the supercycle to obtain the desired $f_{Sn}$ for the final ZTO film. b) Tin composition, $c_{Sn}$, obtained from XPS taken after 200 s sputtering, as a function of tin cycle fraction, $f_{Sn}$, for ZTO films deposited at 150 °C using the thermal ALD process. Experimental data is shown in symbols. The dashed line indicates the fit using the rule of mixtures (Equation (1)).

ALD,[25–32] but only two previous studies have described TFTs made using ALD ZTO.[13,14] These studies used $H_2O_2$ as the oxidant, resulting in as-deposited films that are highly conductive (always on).[13] The authors found that post-deposition anneals at 350 °C, or above, and low tin content were necessary to achieve transistors with on/off ratios of >$10^9$ or field-effect mobility >11 cm$^2$ V$^{-1}$ s$^{-1}$.[13,14] The observed transition from conducting to semiconducting behavior was attributed to a decrease in oxygen vacancies that occurs upon annealing.[13]

In this study, to achieve as-deposited semiconducting films with low oxygen vacancy concentrations, three ALD process are investigated. The first ZTO ALD process uses $H_2O$ as the oxidant with thermal ALD processes for both metal precursors. The second process, which yields higher mobility films, uses an $H_2O$ oxidant for the zinc-related steps and oxygen plasma for the tin-related steps within each supercycle. The third approach uses oxygen plasma for both zinc and tin precursor oxidation steps. Hereafter, these are referred to as the "thermal," "hybrid," and "plasma" ALD ZTO process, respectively. For all three approaches, as-deposited films show semiconducting behavior, with the hybrid process achieving a record-high field-effect electron mobility for an ALD ZTO process of >22 cm$^2$ V$^{-1}$ s$^{-1}$.

In addition, prior work on ALD ZTO TFTs has been limited to the use of thermal $SiO_2$ as the gate insulator, which is not compatible with BEOL integration nor with flexible substrates. Here, to obtain switching voltages sufficiently low to be electrically compatible with CMOS ICs, a thin ZTO layer (<10 nm) and a high-$k$ ALD-deposited $Al_2O_3$ thin-film is used as a bottom gate insulator. The ALD ZTO processes demonstrated here, with temperatures <450 °C, enable future use in BEOL and other applications requiring large-area monolithic integration of thin-film electronics.

## 2. Results and Discussion

### 2.1. ALD Growth of Zinc Tin Oxide

The ZTO ALD processes in this study use diethylzinc (DEZ) and tetrakis(dimethylamino)tin (TDMASn) as precursors. The tin cycle fraction, $f_{Sn}$, characterizes the ternary ZTO deposition process. Here, $f_{Sn}$ is defined as the percentage of the total metal precursor steps within one supercycle that use the tin precursor. In ALD ZTO, the tin composition is usually lower than the tin cycle fraction because the $SnO_x$ cycles deposit fewer atoms than the ZnO cycles.[25,27,28,30,32] Also, the composition and cycle fraction are not linearly related, and the net ternary growth-per-cycle (GPC) is reduced compared to its binary constituents because ZnO typically has a reduced GPC when deposited after a $SnO_x$ cycle. This effect has been attributed to suppression of ZnO nucleation and growth on $SnO_x$ surfaces.[28,30,31]

One strategy to overcome the suppressed growth of one ALD material on another is to use a nanolaminate approach, where $f_{Sn}$ is controlled by the relative thickness of each binary oxide discrete layer, which may be subsequently annealed to drive interdiffusion.[19,33] However, in ternary ALD ZTO processes, this approach can cause the formation of discrete ZnO and $SnO_x$ inclusions.[30] Therefore, to minimize the suppression of ZnO growth and achieve a well-mixed amorphous and homogeneous film, a tailored supercycle strategy was developed that minimized the sequential pulsing of a single cation precursor.[34] Specifically, all of the supercycles are composed of sub-supercycles consisting of low numbers of ZnO to $SnO_x$ cycles, that is, 1:1 ($f_{Sn}$ of 50%), 1:2 ($f_{Sn}$ of 33%), or 2:1 ($f_{Sn}$ of 66%). The approach is illustrated schematically in Figure 1a. Using this method, we aim to achieve atomic-level intermixing resulting in a solid solution of amorphous ZTO.

The resulting ZTO thin films were analyzed using ellipsometry, X-ray photoelectron spectroscopy (XPS), grazing incidence X-ray diffraction (GIXRD), and X-ray reflectivity (XRR). The thickness values of all ZTO films analyzed in this paper are reported in Table S1, Supporting Information. After removing adventitious surface carbon, the films are free of carbon impurities within the XPS detection limit of approximately 0.1 at% (Figure S1a, Supporting Information). Compositional analysis of XPS data is used to analyze the tin composition, $c_{Sn}$, in the bulk of the thin film as a function of $f_{Sn}$. The tin composition was varied from 20% to 40% by varying the $f_{Sn}$ from 45% to 67%, as this range yields optimal semiconductor properties for solution-processed, sputtered, and ALD ZTO.[14,35,36] The results for films deposited at 150 °C using the thermal ALD process can be found in Figure 1b, and compared to the rule of mixtures given by Equation (1):[27]


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$$c_{\mathrm{Sn}} = \frac{n_{\mathrm{SnO_2}} \dfrac{\rho_{\mathrm{SnO_2}} r_{\mathrm{SnO_2}}}{M_{\mathrm{SnO_2}}}}{n_{\mathrm{SnO_2}} \dfrac{\rho_{\mathrm{SnO_2}} r_{\mathrm{SnO_2}}}{M_{\mathrm{SnO_2}}} + n_{\mathrm{ZnO}} \dfrac{\rho_{\mathrm{ZnO}} r_{\mathrm{ZnO}}}{M_{\mathrm{ZnO}}}} \tag{1}$$

where the density of $SnO_2$ is $\rho_{SnO_2}$ = 6.85 g cm$^{-3}$, $\rho_{ZnO}$ is the density of ZnO, 5.6 g cm$^{-3}$, $M_{SnO_2}$ is the molar mass of $SnO_2$, 150.7 g mol$^{-1}$, $M_{ZnO}$ = 81.4 g mol$^{-1}$ is the molar mass of ZnO,[37] and the measured GPC of zinc oxide, $r_{ZnO}$, and tin oxide, $r_{SnO_2}$, deposited by thermal ALD at 150 °C is 0.6 and 1.6 Å cycle$^{-1}$, respectively. The $n$ values are the number of binary cycles within one supercycle. Figure 1b shows that the ALD ZTO processes used here do not strictly follow the rule of mixtures, which is in agreement with previous studies.[27,32] Nonetheless, the supercycle design approach used here allows for precise tuning of the film composition, and yields ZTO ternary alloy amorphous oxide films with $c_{Sn}$ values across the range of interest for active electronic devices.

To verify the amorphous phase of the films, GIXRD patterns for as-deposited ZTO with various compositions are shown in **Figure 2**a. Films with $c_{Sn}$ = 18% and 21% ($f_{Sn}$ = 33% and 45%, respectively) are X-ray amorphous, showing only a single broad peak centered around 2$\theta$ of 35°. This broad peak, which has been observed in other works on amorphous or mostly amorphous ZTO,[29,38] encompasses the hexagonal wurtzite ZnO peaks at 2$\theta$ = 31.8° (100), 34.4° (002), and 36.3° (101).[39] Note, ZTO films that appear X-ray amorphous may still have small (<10 nm) crystallites in an amorphous matrix, due to the large diffraction volume sampled by GIXRD.[29] Films with higher zinc content ($c_{Sn}$ = 14%, $f_{Sn}$ = 25%) show this broad peak in addition to multiple distinct crystalline peaks, indicating the formation of larger nanocrystallites. Figure 2b shows the GIXRD patterns for the $c_{Sn}$ = 21% film deposited at 200 °C before and after post-deposition annealing. Both the as-deposited and 500 °C-annealed films are amorphous. This result is expected because the crystallization temperature of ZTO is typically >600 °C,[38,40] much higher than that of binary ZnO or $SnO_2$. These results indicate the success of the sub-supercycle approach to ensure atomic-level intermixing of zinc and tin within an amorphous metal oxide matrix, as long as $c_{Sn}$ is greater than 14%.

### 2.2. Electrical Properties of ALD ZTO Thin-Film Transistors

To achieve high-mobility semiconducting ALD ZTO films, the optimal tin composition was determined. Thermal ALD ZTO films were deposited at 150 °C with various tin compositions, followed by a 500 °C anneal in air. For comparison, ZnO ($c_{Sn}$ = 0%) films were made using a binary thermal ALD process and annealed in an identical manner. Bottom gate, top contact transistors were fabricated (**Figure 3**a). Transfer curves are shown in Figure 3b and Figure S2, Supporting Information. For ZTO films, the field-effect mobility, $\mu_{FE,}$ is maximum for a tin composition of 21%. Lower mobility values are observed in ZTO films with lower or higher tin fractions (Figure 3c), in agreement with prior results using other ZTO deposition methods.[35,36] The observed mobility roll off at low tin fractions is likely due to the formation of ZnO nanocrystallites, consistent with the XRD observations in Figure 2a.[8] While binary ZnO has reasonably high mobility, the mobility of ZnO TFTs has a larger device-to-device variation and a larger subthreshold slope (SS) of 2.15 V dec$^{-1}$ compared to the ZTO SS of 0.57 V dec$^{-1}$ for $c_{Sn}$ = 21%.

To study the impact of the oxidizing species in the ALD process, the thermal and hybrid ALD processes were used to deposit ZTO at 150 °C with $f_{Sn}$ = 45%. Transistor behavior was evaluated for as-deposited film. Transfer curves and effective mobility are shown in **Figure 4** and Figure S3, Supporting Information, and extracted device parameters are reported in **Table 1**. For both ALD processes, TFTs made with as-deposited ZTO films exhibit semiconductor field-effect behavior. Both as-deposited ALD ZTO devices operate in enhancement mode with turn-on voltages, $V_{ON}$, above 0 V. In contrast, a prior report of as-deposited ALD ZTO TFTs made with $H_2O_2$ as an oxidant showed conducting behavior with no observable field-effect,[13] similar to previous results on ALD $SnO_{x,}$[41] due to a high concentration of oxygen vacancies. The extracted electron mobility achieved in as-deposited hybrid ALD films is 2.19 cm$^2$ V$^{-1}$ s$^{-1}$, whereas the thermal process yields a much lower electron mobility of 9.90 × 10$^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$. Nonetheless, ALD ZTO TFTs made with as-deposited hybrid films deposited at 150 °C exhibit a large positive turn-on voltage, a kink in sub-threshold $I_D$, and a large SS (Figure 4b). These TFT features indicate that the ZTO active layer has a large number of defects or trap states.[42] The physical origin of these states, and the reasons for the improved behavior of the hybrid process, are discussed below.

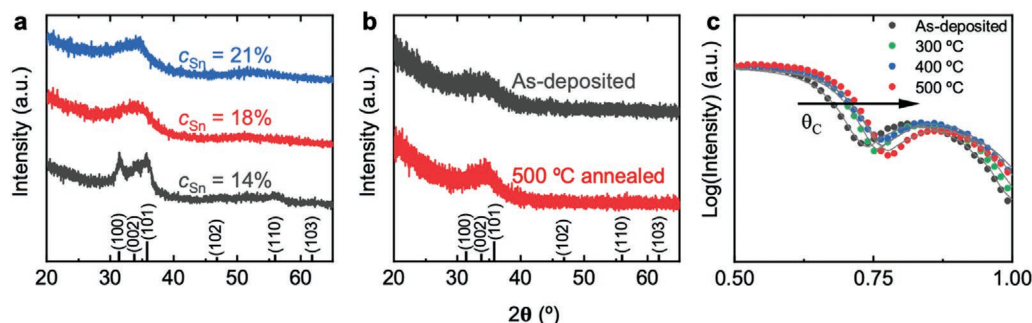


**Figure 2.** GIXRD patterns of thermal ALD ZTO: a) As-deposited at 150 °C with various tin composition; and b) deposited at 200 °C with 21% tin composition, showing curves for as-deposited film and film annealed at 500 °C. ZnO peak positions (JCPDS No. 36–1451) are shown at the bottom. c) Normalized XRR of films deposited by thermal ALD at 150 °C with 21% tin composition. The open symbols are measured data and the lines indicate fit.

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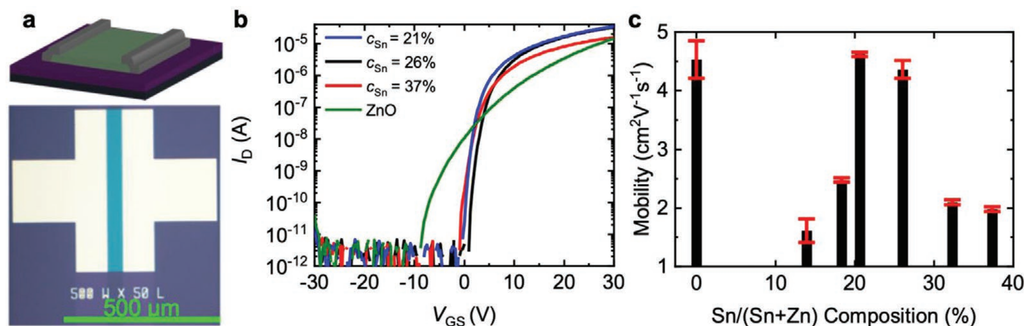


**Figure 3.** a) Top: schematic illustration of a TFT and bottom: top-down microscope image of a fabricated device. b) Transfer curves of films deposited at 150 °C using the thermal ALD ternary ZTO and binary ZnO processes and annealed at 500 °C. All TFTs have W/L of 10 and $V_{DS}$ = 1 V. The legend indicates the tin composition obtained by XPS. c) Field effect mobility as a function of tin composition, extracted from the transfer curves shown in (b) and Figure S2, Supporting Information. Error bars indicate standard deviation based on measurement of at least four different transistors for each composition.

To improve the electrical properties of the films, post-deposition anneals were performed on the ZTO layer before applying metal contacts. For both thermal and hybrid ALD films, anneals at 300, 400, or 500 °C increase the field-effect mobility, decrease the sub-threshold slope, and shift the $V_{ON}$ value toward zero volts. The higher the annealing temperature, the greater the improvements (Figure 4c and Table 1). For thermal ALD ZTO, the mobility dramatically increases from 9.90 × $10^{-4}$ cm$^2$ V$^{-1}$ s$^{-1}$ for as-deposited films to 5.44 cm$^2$ V$^{-1}$ s$^{-1}$ after a 500 °C anneal. TFTs made using hybrid ALD ZTO annealed at 500 °C exhibits a mobility of 15.5 cm$^2$ V$^{-1}$ s$^{-1}$, which is greater than any previously-reported value for ALD ZTO (Table S2, Supporting Information). After a 500 °C anneal, both thermal and hybrid ALD ZTO TFTs show a turn-on voltage and hysteresis of <1 V, with sub-threshold slopes of 0.57 and 0.29 V dec$^{-1}$, respectively. Sub-threshold slopes above the Boltzmann limit (60 mV dec$^{-1}$ at room temperature) are known to be caused by charge traps at or near the dielectric-semiconductor interface.[43] The more rapid turn-on with increased anneal temperature thus reflects a reduction in interface charge trap density.

To further improve the as-deposited performance of the ALD ZTO films, the deposition temperature was increased to 200 °C. The TFT transfer curves are shown in **Figure 5**. Table 1 shows the extracted transistor parameters. The hybrid ALD process at 200 °C results in excellent as-deposited film properties: a mobility of 13.8 cm$^2$ V$^{-1}$ s$^{-1}$ and sub-threshold slope of 0.43 V dec$^{-1}$. In contrast, ZTO deposited using the thermal ALD process decreases by approximately ten times to 9.56 × $10^{-5}$ cm$^2$ V$^{-1}$ s$^{-1}$ when deposition temperature is increased from 150 to 200 °C. Both thermal and hybrid ALD ZTO deposited at 200°C show improvement after post-deposition annealing. The best TFT performance, with a mobility of 22.0 cm$^2$ V$^{-1}$ s$^{-1}$ and a sub-threshold slope of 0.28 V dec$^{-1}$, is observed for the hybrid 200 °C process followed by a 500 °C anneal.

It should be noted that the TFTs made with a ZTO deposition temperature of 200 °C and a 400 °C post-deposition anneal show nearly identical behavior to the devices made with films annealed at 500 °C (Figure 5 and Table 1). This result indicates the technological compatibility of ALD ZTO with monolithic integration on silicon CMOS at the BEOL, which typically has a thermal budget of <450 °C.[5] If an even lower temperature budget is required, for example, for integration on flexible substrates, as-deposited films made with the hybrid ALD process at 200 °C can be used.

For comparison with the hybrid and thermal processes, additional ZTO films were made using an all-plasma ALD process at 200 °C with $f_{Sn}$ = 45%. The resulting TFT curves are shown in Figure S4, Supporting Information. The effective mobility of the as-deposited and 500 °C annealed plasma ALD ZTO films are 13.4 and 22.7 cm$^2$ V$^{-1}$ s$^{-1}$, respectively. These mobility values

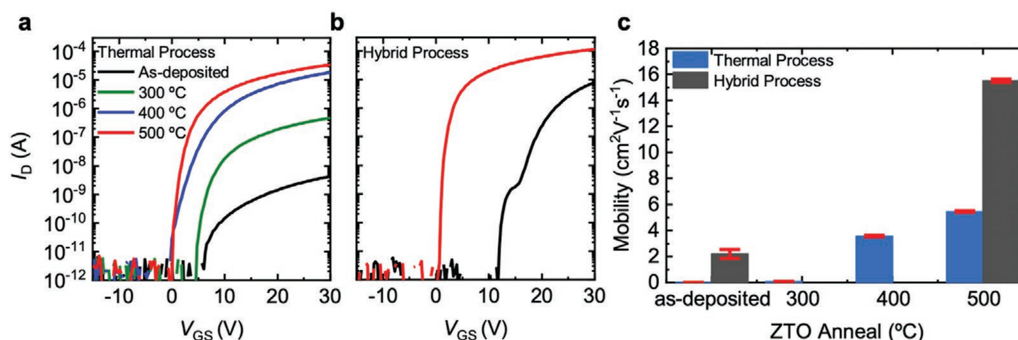


**Figure 4.** Transfer curves of ALD ZTO TFTs deposited at 150 °C with $f_{Sn}$ = 45% versus post-deposition anneal temperature for: a) ZTO deposited using the thermal ALD process, and b) ZTO deposited using the hybrid ALD process. c) Field effect mobility as a function of anneal temperature, extracted from the transfer curves shown in (a) and (b). Error bars indicate standard deviation from measurements of at least five different transistors for each condition. All TFTs have W/L of 10 and $V_{DS}$ = 1 V. The 500 °C curve in (a) is the same as the $c_{Sn}$ = 21% curve in Figure 3b.


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**Table 1.** Electrical properties of ALD ZTO TFTs discussed in this work. The corresponding *I–V* curves are shown in Figures 4 and 5. The ZTO layers were deposited with $f_{Sn}$ = 45%.

| ALD type (deposition temperature) | Post-deposition anneal temperature | $\mu_{FE}$ [cm$^2$ V$^{-1}$ s$^{-1}$] | *SS* [V dec$^{-1}$] | $\Delta V_C$ [V] | $V_{ON}$ [V] |
|---|---|---|---|---|---|
| Thermal (150 °C) | As-deposited | $9.90\times10^{-4}$ | 2.2 | N/A | 7.4 |
| Thermal (150 °C) | 300 °C | $8.76\times10^{-2}$ | 0.89 | 4.6 | 5.4 |
| Thermal (150 °C) | 400 °C | 3.54 | 1.2 | 1.3 | 1.1 |
| Thermal (150 °C) | 500 °C | 5.44 | 0.57 | 0.89 | 0.54 |
| Hybrid (150 °C) | As-deposited | 2.19 | 0.68 | 3.1 | 10 |
| Hybrid (150 °C) | 500 °C | 15.5 | 0.29 | 0.87 | 0.66 |
| Thermal (200 °C) | As-deposited | $9.56\times10^{-5}$ | 4.6 | N/A | 23 |
| Thermal (200 °C) | 400 °C | 16.1 | 0.37 | 1.7 | 3.1 |
| Thermal (200 °C) | 500 °C | 17.5 | 0.30 | 1.1 | 1.8 |
| Hybrid (200 °C) | As-deposited | 13.8 | 0.43 | 3.4 | 4.6 |
| Hybrid (200 °C) | 300 °C | 18.8 | 0.31 | 1.4 | 2.3 |
| Hybrid (200 °C) | 400 °C | 22.1 | 0.29 | 0.95 | 1.1 |
| Hybrid (200 °C) | 500 °C | 22.0 | 0.28 | 0.53 | –0.78 |

are nearly identical to those of the hybrid ALD ZTO process (Table 1). However, the as-deposited plasma ALD ZTO TFT *I–V* curve shows an early turn-on near –14 V, indicating the presence of a conduction path with low mobility, possibly created by oxygen plasma damage within the film.[44] Similar behavior has been observed following the plasma treatment of TAOS films.[44,45] The increased mobility and shift of the turn-on voltage to near zero following post-deposition annealing indicates that this damage is recovered during annealing.[44] Nonetheless, even after annealing, the plasma ALD ZTO films have a SS of 0.36 V dec$^{-1}$, between the values obtained for the thermal and hybrid process, and $\Delta V_C$ of 1.03 V, larger than that of the other two processes. The larger sub-threshold slope and hysteresis may be due to traps in the film or at its interfaces that cannot be resolved by annealing.[46] The hybrid process clearly offers the best as-deposited and annealed TFT performance.

In summary, a dramatic improvement in ZTO electrical properties observed with 1) post-deposition annealing; 2) an increase of the deposition temperature from 150 to 200 °C; and 3) the use of the hybrid process instead of pure thermal or plasma-enhanced ALD processes. To develop a mechanistic understanding of the chemical and structural origins of these improvements, XRD, XPS, and XRR measurements were performed.

Improvements resulting from post-deposition annealing of ALD ZTO have been attributed to a change in the local atomic arrangement within the channel layer in a previous work.[14] However, in this study, XRD analysis shows that both the thermal ALD and hybrid ALD ZTO films remain amorphous after a 500 °C anneal (Figure 2b and Figure S5e, Supporting Information). Therefore, no phase change is occurring during the post-deposition anneal. XPS depth profiling indicates that Zn and Sn concentrations are highly uniform through the bulk of the film, and the $c_{Sn}$ values are comparable for the thermal and hybrid 200 °C processes, both before and after post-deposition annealing (**Figure 6**a). Thus, the observed increases in mobility cannot be attributed to a change in phase or bulk stoichiometry.

Another mechanism that has been previously proposed for ALD ZTO is that annealing decreases the concentration of oxygen vacancy defects.[13] Therefore, to quantify the oxygen-related states, the oxygen O 1s XPS peak was measured for several films after Ar sputtering of the surface to remove adventitious carbon. The O 1s peak was deconvoluted into three components: 1) metal-oxide bonding (M-O), at 530.1 ± 0.1 eV; 2) oxygen-deficient regions ($V_O$), at 531.1 ± 0.1 eV; and 3) hydroxyls (M-OH), at 532.1 ± 0.2 eV.[47–50] These peak locations are indicated by vertical dotted lines and the Gaussian fits are plotted in Figure 6b and Figure S1b,c,d,e, Supporting Information. Table S3, Supporting Information, lists the atomic percentages of each oxygen component. For all films, the oxygen vacancy concentrations are between 3.7 and 5.4%, and do not change significantly after annealing; they remain constant within ±1.2%. Thus, a reduction in oxygen vacancies cannot explain the drastic increase in mobility of the annealed thermal ALD ZTO films.

The hydroxyl concentration in the films is much higher in the as-deposited 150 °C thermal films compared to the 200 °C as-deposited films (Table S3, Supporting Information). We attribute this difference to a more complete dehydrogenation of surface functional groups during the ligand-exchange reactions at elevated deposition temperatures.[51] Electrically, the as-deposited 150 °C thermal ALD films exhibited large $V_{ON}$, comparatively low mobility and large hysteresis, but these undesired features are eliminated or reduced after a 500 °C post-deposition anneal (Figure S6, Supporting Information and Table 1). The reason for the improvement is clear: the anneal causes a decrease in the hydroxyl concentration in the films, and a corresponding increase in the M-O concentration (Table S3, Supporting Information). As shown in a previous report on solution-processed ZTO,[52] hydroxyls contribute defect states that act as electron traps. By post-deposition annealing, the M-OH concentration in the ALD ZTO films is reduced and TFT behavior improves.

However, as shown in Table S3, Supporting Information, a decrease in M-OH concentration cannot explain the higher


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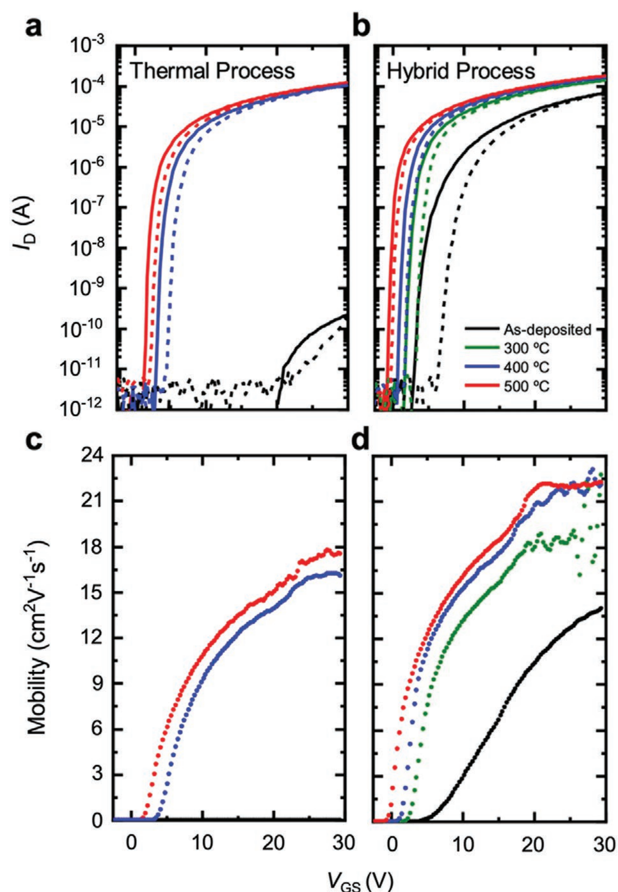


**Figure 5.** a,b) Transfer curves of ALD ZTO TFTs made with 21% tin composition films deposited at 200 °C and with various post-deposition anneal temperatures. Forward *I–V* curves are indicated by solid lines and reverse curves are indicated by dashed lines. c,d) Effective mobility extracted from the forward *I–V* curves. TFTs shown in (a,c) were made using the thermal ALD ZTO process while those in (b,d) used the hybrid ALD process. For all TFTs, W/L = 10 and $V_{DS}$ = 1 V.

mobility observed for hybrid 200 °C ALD ZTO films compared to those deposited using a thermal process. Therefore, an additional factor must be contributing to this dependence of mobility on the oxidizing species used during the ALD process. Prior work on sputtered ZTO showed that mobility increased upon the densification of the film.[53] To assess film density, XRR was performed on several ALD ZTO samples (Figure 2c, Figure S5a–d and Table S4, Supporting Information). The XRR spectra show that after annealing at 500 °C, the 200 °C thermal ALD ZTO film density increases from 5.1 to 5.9 g $cm^{-3}$. Ellipsometry confirms the XRR results, showing that the thermal ALD ZTO film decreases in thickness from 9.9 to 8.8 nm upon 500 °C annealing (Table S1, Supporting Information). Similarly, annealing at 500 °C increases the density of the thermal ALD ZTO film that was deposited at 150 °C from 5.0 to 5.7 g $cm^{-3}$. Clearly, increasing the ALD deposition temperature and/or adding a post-deposition anneal both induce an increase in film density that correlates with the observed increase in electron mobility.

In fact, for all films characterized, the ZTO film density correlates positively with mobility, $r(7) = .894$, $p = .00116$, while the sub-threshold slope correlates negatively with density, $r(7) = .745$, $p = .021$ (Figure S7, Supporting Information). These correlations indicate that densifying the ZTO film not only improves electron transport within the active layer, but also reduces the density of interfacial states at the gate insulator-semiconductor interface, improving the switching properties of the TFT.

Film densification can also be used to explain the differences in electrical properties observed between the thermal and plasma-enhanced ALD ZTO processes (Table 1 and Table S2, Supporting Information). For ZTO films deposited at 200 °C, the density is significantly lower in thermal processes compared to plasma-enhanced ALD processes (further details in Table S4, Supporting Information). These results are consistent with previous reports of plasma-enhanced ALD of silicon nitride films, where plasma exposure during growth lead to an increase in film density.[54] Thus the excellent behavior of as-deposited hybrid ALD ZTO TFTs, compared to thermal ALD with the same deposition and anneal temperatures, can be attributed to the denser amorphous films achieved using the plasma-enhanced ALD process.[55]

Previous work on ALD ZTO TFTs has been limited to the use of gate insulators that consist of ≥100 nm of thermally-grown $SiO_2$.[13,14] Devices driven with $SiO_2$ are limited by low

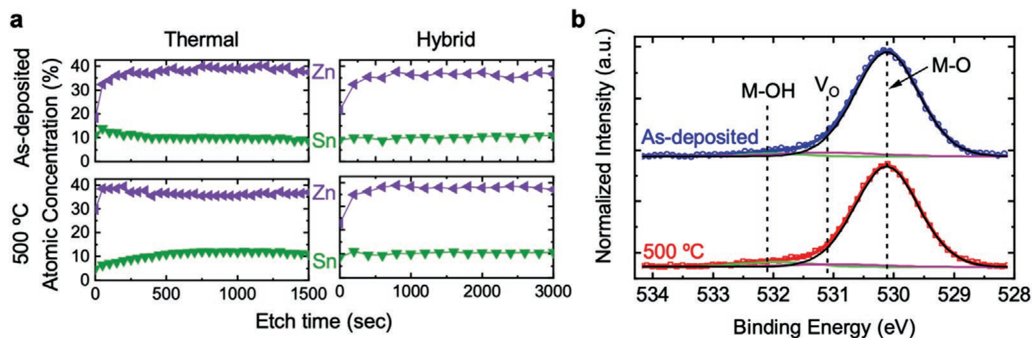


**Figure 6.** a) Zn and Sn concentrations as a function of depth, obtained by XPS for $c_{Sn}$ = 21% ZTO films: as-deposited (top row), 500 °C annealed (bottom row), deposited at 200 °C using thermal ALD (left) and hybrid ALD (right). b) O 1s XPS analysis after 750 s of argon sputtering of the same thermal ALD films as-deposited (blue circles) and after 500 °C anneal (red squares) in (a). The solid line indicates the fit using the atomic percentages of metal-oxygen bonds (black), M-O, oxygen vacancies (pink), $V_O$, and metal-hydroxide bonds (green), M-OH, listed in Table S3, Supporting Information. The XPS curves shown in (b) were normalized to the M-O peak height of each film.

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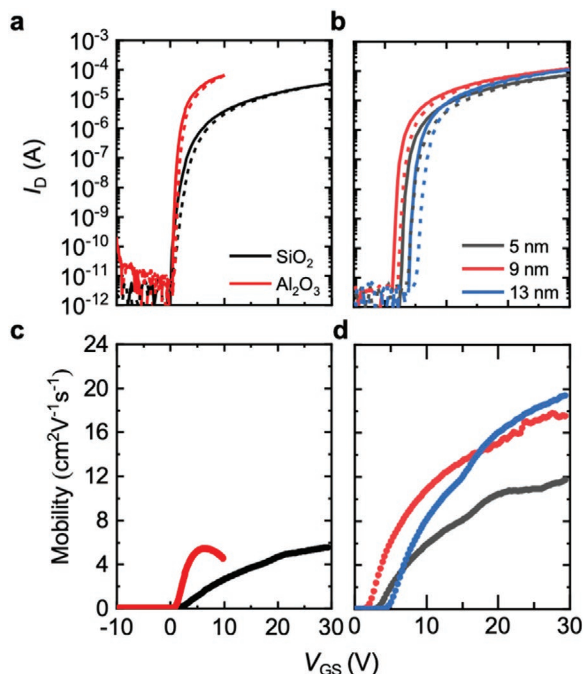


**Figure 7.** Transfer curves of TFTs made with ALD ZTO films deposited using the thermal process and annealed at 500 °C. All films have 21% tin composition. a) TFT *I–V* behavior for films deposited at 150 °C with two different gate insulators: 100 nm thermal $SiO_2$ or 30 nm ALD $Al_2O_3$. Note, the $SiO_2$ data is the same as that shown for the 500 °C anneal in Figure 4a and the $V_{GS}$ range for the $Al_2O_3$ film was reduced to prevent dielectric breakdown. b) TFT *I–V* behavior for films deposited at 200 °C with different ZTO layer thicknesses. Note, the trace labeled 9 nm is the same as that shown in Figure 5a. For (a) and (b), Forward *I–V* curves are indicated by solid lines and reverse curves are indicated by dashed lines. c,d) Effective mobility extracted from the forward *I–V* curves shown in parts (a) and (b).

oxide capacitance due to the low dielectric constant of $SiO_2$, and thermally-grown $SiO_2$ is incompatible with monolithic integration with Si CMOS and flexible substrates. Using high-*k* dielectrics deposited by ALD, such as $HfO_2$,[56] $ZrO_2$,[57] and $TiO_2$,[58] can increase the gate capacitance, resulting in higher on-current, smaller operating voltages, and compatibility with BEOL integration.

To compare the effects of the gate insulator material, thermal ALD ZTO TFTs were fabricated using either $SiO_2$ or $Al_2O_3$ as the gate dielectric. The ZTO film had a tin composition of 21%, was deposited at 150 °C, annealed at 500 °C, and the thickness was measured to be approximately 22 nm. Transfer curves are shown in **Figure 7**a, and Table S5, Supporting Information, shows the extracted electrical parameters. The increased capacitive coupling of approximately 30 nm $Al_2O_3$ yields a peak mobility of 5.39 cm$^2$ V$^{-1}$ s$^{-1}$, very similar to the maximum mobility of 5.44 cm$^2$ V$^{-1}$ s$^{-1}$ for ZTO on $SiO_2$. However, the peak mobility occurs at a much lower voltage for devices made using $Al_2O_3$.

Furthermore, the use of $Al_2O_3$ reduces the switching voltage, $V_{switch}$. $V_{switch}$ is defined as the difference between the threshold voltage, extracted for the linear regime, and the turn-on voltage. By using an $Al_2O_3$ gate insulator instead of $SiO_2$, $V_{switch}$ is reduced from 6.84 to 2.06 V, respectively (Table S5, Supporting Information). In addition, the $Al_2O_3$-ZTO TFTs exhibit a much steeper subthreshold slope of 0.23 V dec$^{-1}$. As predicted, the fast turn-on of the $Al_2O_3$-ZTO TFTs decreases their switching voltage, thereby enabling their future electrical integration with BEOL Si CMOS, which runs at supply voltages of a few volts. In the future, ZTO and $Al_2O_3$ deposition processes can occur in situ, that is, within the same ALD vacuum environment, which should further improve the switching and turn-on properties of the devices.[59] In addition to improving the switching and turn-on properties of the devices, optimizing substrate preparation and the insulator deposition process may improve field-effect mobility to more closely rival quaternary indium-containing ALD TFTs.[60]

Prior work, using different deposition techniques or semiconductor oxides, has shown that active-layer thickness must be optimized to obtain good TFT stability[61] and enhancement mode behavior.[62] To investigate the effect of ZTO layer thickness on TFT behavior, three identical devices were fabricated using 5, 9, and 13 nm ZTO films deposited using the thermal ALD process at 200 °C with post-deposition annealing at 500 °C. Transfer curves and plots of effective mobility are shown in Figure 7b and Figure 7d, respectively, with extracted device parameters tabulated in Table S6, Supporting Information. For this ALD recipe, all devices have enhancement-mode behavior. Both the 9 and 13 nm thick films have a mobility >17 cm$^2$ V$^{-1}$ s$^{-1}$. However, the mobility decreases for the 5 nm thick device. All three films have a similar GPC (Figure S8, Supporting Information) and refractive index (Table S6, Supporting Information). This indicates that nucleation-limited growth likely does not explain the reduced mobility of the 5 nm thick device. Instead, the reduced mobility could possibly be attributed to the increased influence of carrier scattering at the top surface.[63]

Interestingly, for some of the ALD ZTO recipes used, device performance degrades for thicker films. TFT behavior for thermal ALD ZTO deposited with $f_{Sn}$ = 50% at 130 °C and annealed at 500 °C is shown in Figure S9, Supporting Information. The approximately 50 nm film exhibits a significantly reduced mobility, increased SS, and more negative turn-on voltage compared to approximately 15 nm films made using the same process. Similar trends with channel thickness have been reported previously for amorphous silicon, IGZO, and ZnO TFTs, and may be associated with surface depletion layers or other back-channel effects, or, in some cases, with vertical gradients in semiconductor film trap densities.[63] Therefore, the thickness of the high mobility ZTO film should be optimized alongside the gate dielectric process to obtain the best TFT properties. Based on previous results on solution-processed ZTO,[64] TFTs fabricated with ALD ZTO are expected to benefit from $O_3$-based ALD $Al_2O_3$ back channel passivation to minimize threshold voltage shifts due to bias stress.[65] This could be a fruitful area for future work.

## 3. Conclusion

In conclusion, an ALD supercycle approach to deposit high quality amorphous ZTO films was demonstrated. Three different deposition processes were studied: $H_2O$-based thermal, hybrid $H_2O/O_2$ plasma, and all-plasma. All processes yield as-deposited semiconducting films, due to a low concentration of oxygen vacancies, with enhancement-mode behavior and


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electron mobility as high as 13.8 $cm^2 V^{-1} s^{-1}$. For all processes, increasing the ALD deposition temperature and the post-deposition annealing temperature improves the ZTO electrical properties, due to film densification. The best performance was seen for hybrid ALD ZTO films with $c_{Sn}$ = 21% deposited at 200 °C and annealed at 500 °C with $\mu_{FE}$ = 22.0 $cm^2 V^{-1} s^{-1}$ and SS = 0.28 V $dec^{-1}$. The better behavior of hybrid thermal/plasma ALD ZTO films compared to those deposited by thermal ALD or all-plasma ALD is attributed to the densification of the film and reduction of hydroxyl states, while avoiding the plasma damage that may come from an all-plasma process. Moreover, nearly the same performance was observed when the hybrid ALD film was annealed at 400 °C: $\mu_{FE}$ = 22.1 $cm^2 V^{-1} s^{-1}$ and $SS$ = 0.29 V $dec^{-1}$. This indicates the compatibility of these ALD processes with the thermal budget at the silicon CMOS back-end-of-line. Finally, by using an ALD $Al_2O_3$ gate insulator and choosing an optimal ZTO film thickness of 9 to 13 nm, transistors with rapid turn-on and low switching voltage were obtained, enabling supply voltage compatibility with silicon ICs. The results shown here pave the way for future monolithic integration of multi-functional ZTO electronics on top of silicon CMOS or onto large-area flexible substrates.

## 4. Experimental Section

*ZTO ALD Process*: ZTO deposited using the $H_2O$-based thermal process was grown using a custom-built, flow-type thermal ALD tool.[66] Films deposited using the hybrid and plasma processes were grown using a Veeco Fiji G2 flow-type ALD tool. Binary ZnO and $SnO_x$ cycles were repeated to generate ternary ZTO films with a desired thickness and tin cycle fraction. For all binary ZnO and $SnO_x$ cycles, DEZ (thermal: Sigma Aldrich, St. Louis, MO, ≥52 wt% Zn basis; plasma/hybrid: Strem Chemicals, Inc., Newburyport, MA, 95%) and TDMASn (thermal: Strem Chemical, Inc., Newburyport, MA, 99%; plasma/hybrid: Strem Chemicals, Inc., Newburyport, MA, 99%) were used, respectively. For thermal ALD processes, deionized $H_2O$ was used as the oxidant. For the hybrid process, $SnO_x$ cycles were oxidized with 300 W $O_2$ plasma while ZnO cycles were performed with thermal $H_2O$. The all-plasma process used 300 W $O_2$ plasma. Ultra-high purity Ar (GGI International, LLC, Washington, PA, 99.999%) was used as the carrier gas with a flow rate of 10 sccm during pulses and purges during the $H_2O$-based thermal process. The ZTO ALD films were deposited with a substrate temperature set to 150 or 200 °C. Pulse length saturation curves for $H_2O$-based thermal process DEZ and TDMASn binaries, shown in Figure S10, Supporting Information, were obtained by measuring film thickness by spectroscopic ellipsometry. More specific details about the ALD process can be found in Table S7, Supporting Information.

*Device Fabrication*: Heavily doped $n^+$ silicon was used as the gate electrode for all TFTs. For devices with a $SiO_2$ gate insulator, 100 nm thermal oxide was grown on the silicon substrates. For the devices with $Al_2O_3$ gate insulator, approximately 30 nm of $Al_2O_3$ was deposited using trimethylaluminum (TMA; Strem Chemical, Inc., Newburyport, MA, 99%) and an $O_2$ plasma-based ALD process at 150 °C in an Oxford OpAL ALD system. The ZTO was deposited as described above and patterned by wet etching for device isolation. The films were then annealed at 300, 400, or 500 °C on a hotplate in a custom-built moisture-controlled glovebox flowing compressed air with humidity <20% RH.[52] After annealing, approximately 100 nm of molybdenum was deposited by sputtering and patterned by lift-off for source/drain ohmic contacts.

*Materials Characterization*: Ellipsometry (J. A. Woollam M-2000) was performed to measure the thickness of the ALD thin films on Si (100) substrates, using a Cauchy model (wavelength range: 400–1600 nm). Data can be found in Table S1, Supporting Information. GIXRD (Rigaku Smartlab X-ray Diffractometer) was used at a grazing incidence of 1°, to reduce the signal of Si (100) substrate and amplify the signal from the thin film, to analyze the crystallinity of the ZTO films for $2\theta$ from 20° to 70°. XPS was performed using a Kratos Axis Ultra XPS, with a monochromatic Al source (10 mA, 12 kV) and a pass energy of 20 eV and step size of 0.1 eV on a spot size of 700 µm by 300 µm. For all scans, a charge neutralizer was used. The XPS curves were analyzed with CasaXPS software. To account for charge compensation, the C 1s peak at 284.5 eV was used to calibrate the energies. Each peak was analyzed using Gaussian-Lorentzian curves with a full-width half max less than two and a linear background. To analyze ZTO film composition, the area under the Zn $2p_{3/2}$ (near 1021.8 eV), Sn $3d_{5/2}$ (near 486.2 eV), and O 1s XPS peaks was integrated. The relative sensitivity factors used here were 3.726, 4.725, 0.780, and 0.278 for Zn $2p_{3/2}$, Sn $3d_{5/2}$, O 1s, and C 1s, respectively. For depth profiling, Ar sputtering was used with an energy of 1 kV and extractor current of 100 µA with measurements taken every 50 s. XRR (Rigaku Smartlab) was used to measure film density. Data was taken from 0° to 5° $2\theta$ using Cu-target X-ray generator, SC-70 (scintillation counter) detector, 44 mA and 40 kV with 10 mm length limiting slit. Scan step size was set to 0.01° and the speed was set to 0.4° $min^{-1}$. Pre-optical and sample alignment were performed before measuring. XRR data was analyzed using GlobalFit 2 Rigaku software version 2.0.10.0.

*Electrical Measurements*: A Keysight B1505A power device analyzer was used to take electrical measurements in the dark at room temperature. All data were taken with 3 PLC integration, with continuous voltage sweeps. *I–V* curves were taken first in the forward direction, by sweeping $V_{GS}$ negative to positive, and then immediately following in the reverse direction, sweeping $V_{GS}$ positive to negative. For $I_D$–$V_{GS}$ curves, three curves were measured consecutively, and the third measurement is reported here. Because 100 nm thick thermal $SiO_2$ was used for the gate, the gate current is below 100 pA for all TFT measurements shown here (Figure S4, Supporting Information). The field-effect mobility, $\mu_{FE}$, is extracted using the equation $\mu_{FE} = (dI_D/dV_{GS})L(WC_{ox}V_{DS})^{-1}$ where *W, L,* $\mu$, and $C_{ox}$ refer to the channel width, channel length, electron mobility, and oxide capacitance, respectively, and $dI_D/dV_{GS}$ is the slope of the $I_D$–$V_{GS}$ curve in the linear region.[52] The mobility was extracted using a gate voltage range of 27 V < $V_{GS}$ < 30 V with $V_{DS}$ = 1 V for all transistors, unless otherwise specified. The saturation mobility for a given $V_{GS}$–$V_T$ was anticipated to be similar to the linear mobility extracted from the same $V_{GS}$–$V_T$ (Figure S11, Supporting Information). Unless otherwise specified, device parameters and *I–V* curves are shown for $V_{DS}$ = 1 V. Positive drain current is shown in all *I–V* plots; data points which seem to be below the coordinate axis or appear missing indicate current flowing out of the drain ($I_D < 0$). Note that the noise floor of the measurement setup is several pA. Hysteresis, $\Delta V_C$, is defined as the difference in the value of $V_{GS}$ at which $I_D$ = 100 nA for forward and reverse sweeps. Sub-threshold slope, SS, is the inverse of the logarithmic rate of device current turn-on, in units of Volts per decade of current. The turn-on voltage, $V_{ON}$, is defined as the value of $V_{GS}$ where SS is minimum.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict Of Interest

The authors declare no conflict of interest.

## Author Contributions

R.L.P. and N.P.D. co-led this project. R.L.P. supervised C.R.A. and S.R., while N.P.D. supervised T.H.C., O.T., and R.E.R. C.R.A. conducted the design and fabrication of devices and performed $I$–$V$ measurements and device analysis. T.H.C. performed the GIXRD, XRR, and XPS characterization. T.H.C. and C.R.A. contributed to XPS analysis. C.R.A., O.T., S.R., R.E.R., and T.H.C. contributed to the development of ALD processes used here. C.R.A., R.L.P., T.H.C., and N.P.D. contributed to the preparation of the manuscript.

## Keywords

amorphous oxide semiconductors, atomic layer deposition, thin-film transistors, zinc tin oxide

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[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* **2004**, *432*, 488.
[2] H. Hosono, in *2017 75th Annual Device Research Conf. (DRC)*, IEEE, Piscataway, NJ **2017**, pp. 1–2.
[3] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, G. Tröster, *Appl. Phys. Rev.* **2016**, *3*, 021303.
[4] Y. Son, B. Frost, Y. Zhao, R. L. Peterson, *Nat. Electron.* **2019**, *2*, 540.
[5] S. Sedky, A. Witvrouw, H. Bender, K. Baert, *IEEE Trans. Electron Devices* **2001**, *48*, 377.
[6] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.
[7] P. Schlupp, F.-L. Schein, H. von Wenckstern, M. Grundmann, *Adv. Electron. Mater.* **2015**, *1*, 1400023.
[8] C. Kim, N.-H. Lee, Y.-K. Kwon, B. Kang, *Thin Solid Films* **2013**, *544*, 129.
[9] H. Frenzel, A. Lajn, M. Grundmann, *Phys. Status Solidi RRL* **2013**, *7*, 605.
[10] S. Weng, R. Chen, W. Zhong, S. Deng, G. Li, F. S. Y. Yeung, L. Lan, Z. Chen, H. Kwok, *IEEE J. Electron Devices Soc.* **2019**, *7*, 632.
[11] O. Lahr, Z. Zhang, F. Grotjahn, P. Schlupp, S. Vogt, H. von Wencks tern, A. Thiede, M. Grundmann, *IEEE Trans. Electron Devices* **2019**, *66*, 3376.
[12] O. Lahr, S. Vogt, H. von Wenckstern, M. Grundmann, *Adv. Electron. Mater.* **2019**, *5*, 1900548.
[13] B. D. Ahn, D.-W. Choi, C. Choi, J.-S. Park, *Appl. Phys. Lett.* **2014**, *105*, 092103.
[14] J. Heo, S. Bok Kim, R. G. Gordon, *Appl. Phys. Lett.* **2012**, *101*, 113507.
[15] S. M. George, *Chem. Rev.* **2010**, *110*, 111.
[16] N. P. Dasgupta, H.-B.-R. Lee, S. F. Bent, P. S. Weiss, *Chem. Mater.* **2016**, *28*, 1943.
[17] R. W. Johnson, A. Hultqvist, S. F. Bent, *Mater. Today* **2014**, *17*, 236.
[18] E. Kazyak, K.-H. Chen, K. N. Wood, A. L. Davis, T. Thompson, A. R. Bielinski, A. J. Sanchez, X. Wang, C. Wang, J. Sakamoto, N. P. Dasgupta, *Chem. Mater.* **2017**, *29*, 3785.
[19] A. R. Bielinski, S. Lee, J. J. Brancho, S. L. Esarey, A. J. Gayle, E. Kazyak, K. Sun, B. M. Bartlett, N. P. Dasgupta, *Chem. Mater.* **2019**, *31*, 3221.
[20] M. H. Cho, H. Seol, A. Song, S. Choi, Y. Song, P. S. Yun, K.-B. Chung, J. U. Bae, K.-S. Park, J. K. Jeong, *IEEE Trans. Electron Devices* **2019**, *66*, 1783.
[21] J. Sheng, T. Hong, H.-M. Lee, K. Kim, M. Sasase, J. Kim, H. Hosono, J.-S. Park, *ACS Appl. Mater. Interfaces* **2019**, *11*, 40300.
[22] J. Sheng, J.-H. Lee, W.-H. Choi, T. Hong, M. Kim, J.-S. Park, *J. Vac. Sci. Technol., A* **2018**, *36*, 060801.
[23] I.-H. Baek, J. J. Pyeon, S. H. Han, G.-Y. Lee, B. J. Choi, J. H. Han, T.-M. Chung, C. S. Hwang, S. K. Kim, *ACS Appl. Mater. Interfaces* **2019**, *11*, 14892.
[24] I. M. Choi, M. J. Kim, N. On, A. Song, K.-B. Chung, H. Jeong, J. K. Park, J. K. Jeong, *IEEE Trans. Electron Devices* **2020**, *67*, 1014.
[25] A. Hultqvist, C. Platzer-Björkman, U. Zimmermann, M. Edoff, T. Törndahl, *Prog. Photovoltaics* **2012**, *20*, 883.
[26] M. Kapilashrami, C. X. Kronawitter, T. Törndahl, J. Lindahl, A. Hultqvist, W.-C. Wang, C.-L. Chang, S. S. Mao, J. Guo, *Phys. Chem. Chem. Phys.* **2012**, *14*, 10154.
[27] M. N. Mullings, C. Hägglund, J. T. Tanskanen, Y. Yee, S. Geyer, S. F. Bent, *Thin Solid Films* **2014**, *556*, 186.
[28] J. T. Tanskanen, C. Hägglund, S. F. Bent, *Chem. Mater.* **2014**, *26*, 2795.
[29] J. Lindahl, C. Hägglund, J. T. Wätjen, M. Edoff, T. Törndahl, *Thin Solid Films* **2015**, *586*, 82.
[30] C. Hägglund, T. Grehl, J. T. Tanskanen, Y. S. Yee, M. N. Mullings, A. J. M. Mackus, C. MacIsaac, B. M. Clemens, H. H. Brongersma, S. F. Bent, *J. Vac. Sci. Technol., A* **2016**, *34*, 021516.
[31] A. J. M. Mackus, C. MacIsaac, W.-H. Kim, S. F. Bent, *J. Chem. Phys.* **2017**, *146*, 052802.
[32] S. Lee, S. Kim, S. Shin, Z. Jin, Y.-S. Min, *J. Ind. Eng. Chem.* **2018**, *58*, 328.
[33] C. N. Ginestra, R. Sreenivasan, A. Karthikeyan, S. Ramanathan, P. C. McIntyre, *Electrochem. Solid-State Lett.* **2007**, *10*, B161.
[34] A. J. M. Mackus, J. R. Schneider, C. MacIsaac, J. G. Baker, S. F. Bent, *Chem. Mater.* **2019**, *31*, 1142.
[35] W. Hu, R. L. Peterson, *J. Mater. Res.* **2012**, *27*, 2286.
[36] M. G. McDowell, R. J. Sanderson, I. G. Hill, *Appl. Phys. Lett.* **2008**, *92*, 013502.
[37] W. M. Haynes, in *CRC Handbook of Chemistry and Physics, 97th Edition (Internet Version 2017)* (Eds: W. M. Haynes), Taylor & Francis, Boca Raton, FL **2017**.
[38] D. L. Young, H. Moutinho, Y. Yan, T. J. Coutts, *J. Appl. Phys.* **2002**, *92*, 310.
[39] T. Tynell, M. Karppinen, *Semicond. Sci. Technol.* **2014**, *29*, 043001.
[40] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, D. A. Keszler, *Appl. Phys. Lett.* **2005**, *86*, 013503.
[41] D.-W. Choi, W. J. Maeng, J.-S. Park, *Appl. Surf. Sci.* **2014**, *313*, 585.
[42] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, H. D. Kim, *Appl. Phys. Lett.* **2008**, *93*, 123508.
[43] D. W. Greve, *Field Effect Devices and Applications : Devices for Portable, Low-Power, and Imaging Systems*, Prentice Hall, Upper Saddle River, NJ **1998**.
[44] K.-S. Son, T.-S. Kim, J.-S. Jung, M.-K. Ryu, K.-B. Park, B.-W. Yoo, K. Park, J.-Y. Kwon, S.-Y. Lee, J.-M. Kim, *Electrochem. Solid-State Lett.* **2009**, *12*, H26.
[45] J.-S. Kim, M.-K. Joo, M. X. Piao, S.-E. Ahn, Y.-H. Choi, H.-K. Jang, G.-T. Kim, *J. Appl. Phys.* **2014**, *115*, 114503.
[46] W. Hu, R. L. Peterson, *Appl. Phys. Lett.* **2014**, *104*, 192105.
[47] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, *Nat. Mater.* **2011**, *10*, 45.
[48] S.-J. Seo, Y. H. Hwang, B.-S. Bae, *Electrochem. Solid-State Lett.* **2010**, *13*, H357.
[49] C. Donley, D. Dunphy, D. Paine, C. Carter, K. Nebesny, P. Lee, D. Alloway, N. R. Armstrong, *Langmuir* **2002**, *18*, 450.
[50] Y. Zhao, L. Duan, G. Dong, D. Zhang, J. Qiao, L. Wang, Y. Qiu, *Langmuir* **2013**, *29*, 151.
[51] C. Guerra-Nuñez, M. Döbeli, J. Michler, I. Utke, *Chem. Mater.* **2017**, *29*, 8690.

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[52] Y. Son, A. Liao, R. L. Peterson, *J. Mater. Chem. C* **2017**, *5*, 8071.
[53] B. Yang, S. Oh, Y. J. Kim, S. J. Han, H. W. Lee, H. J. Kim, S. Kim, H. K. Park, J. Heo, J. K. Jeong, *IEEE Trans. Electron Devices* **2014**, *61*, 2071.
[54] J. Provine, P. Schindler, Y. Kim, S. P. Walch, H. J. Kim, K.-H. Kim, F. B. Prinz, *AIP Adv.* **2016**, *6*, 065012.
[55] H. B. Profijt, S. E. Potts, M. C. M. van de Sanden, W. M. M. Kessels, *J. Vac. Sci. Technol., A* **2011**, *29*, 050801.
[56] S. Y. Lee, S. Chang, J.-S. Lee, *Thin Solid Films* **2010**, *518*, 3030.
[57] T.-J. Ha, A. Dodabalapur, *Appl. Phys. Lett.* **2013**, *102*, 123506.
[58] A. Kumar, S. Mondal, K. S. R. K. Rao, *J. Mater. Sci.: Mater. Electron.* **2016**, *27*, 5264.
[59] Y. Song, R. Xu, J. He, S. Siontas, A. Zaslavsky, D. C. Paine, *IEEE Electron Device Lett.* **2014**, *35*, 1251.
[60] S. F. Nelson, C. R. Ellinger, D. H. Levy, *ACS Appl. Mater. Interfaces* **2015**, *7*, 2754.
[61] L.-C. Liu, J.-S. Chen, J.-S. Jeng, *ECS Solid State Lett.* **2015**, *4*, Q59.
[62] D. A. Mourey, M. S. Burberry, D. A. Zhao, Y. V. Li, S. F. Nelson, L. Tutt, T. D. Pawlik, D. H. Levy, T. N. Jackson, *J. Soc. Inf. Disp.* **2010**, *18*, 753.
[63] Y. Wang, X. W. Sun, G. K. L. Goh, H. V. Demir, H. Y. Yu, *IEEE Trans. Electron Devices* **2011**, *58*, 480.
[64] C. R. Allemang, R. L. Peterson, *IEEE Electron Device Lett.* **2019**, *40*, 1120.
[65] S.-J. Yoon, N.-J. Seong, K. Choi, W.-C. Shin, S.-M. Yoon, *RSC Adv.* **2018**, *8*, 25014.
[66] N. P. Dasgupta, J. F. Mack, M. C. Langston, A. Bousetta, F. B. Prinz, *Rev. Sci. Instrum.* **2010**, *81*, 044102.


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