Empirical noise performance of prototype active pixel arrays employing polycrystalline silicon thin-film transistors

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Purpose: In the spirit of overcoming the signal-to-noise limitations of active matrix, flat-panel imagers (AMFPIs) which employ array circuits based on a-Si:H thin-film transistors (TFTs), an empirical investigation of the noise properties of prototype active pixel arrays based on polycrystalline silicon (poly-Si) TFTs is reported. Like a-Si:H, poly-Si supports fabrication of large area, monolithic x-ray imaging arrays and offers good radiation damage resistance, while providing electron and hole mobility orders of magnitude higher. Compared to pixel circuits typically consisting of a single addressing switch in an AMFPI array, the pixel circuit of an active pixel array includes an amplifier that magnifies the imaging signal prior to readout by external acquisition electronics. Also, while readout erases signal stored in the pixels for AMFPI arrays, active pixel arrays allow multiple nondestructive readout, which can be used to reduce noise. The prototype arrays investigated in this paper were developed to explore the effect of variation in amplifier design on noise.

Methods: A pair of prototype arrays incorporating single-stage and two-stage poly-Si pixel amplifiers were examined. The arrays incorporate various amplifier designs in which dimensions of some of the three (or four) poly-Si TFTs per pixel circuit for the single-stage array, and some of the five poly-Si TFTs for the two-stage array, were varied. The arrays were operated using a recently developed electronic data acquisition system that allows variation of operational conditions such as voltages and timing of control signals. The arrays were operated in the absence of radiation in various correlated multiple sampling modes, with and without the injection of charge directly into the pixel circuits for measurements of in-pixel gain and pixel noise. Pixel noise, referred back to the input of the pixel amplifier, was compared to predictions generated by a sophisticated circuit simulation model.

Results: Across the various pixel circuit designs, the median in-pixel gain for the single-stage and two-stage arrays was measured to be $\times 9.3$ and $\times 25$, respectively. These gain levels were sufficient to reduce the contribution of external noise, defined as the electronic additive noise in the absence of noise contributions from circuitry in the pixel and referred back to the input of the pixel amplifier, to less than 340 e. As a result, median pixel noise results as low as ~695 e and 866 e, acquired using eight samples, were observed from the best-performing single-stage and two-stage designs, respectively. While the magnitude of pixel noise predicted by simulation was lower than the measured results, there was generally good agreement between simulation and measurement for the functional dependence of noise on operating voltages, timing, and sampling mode.

Conclusions: The single-stage and two-stage arrays examined in this study demonstrated pixel noise well below that typically demonstrated by AMFPIs. Through proper design, it should be possible to maintain the noise levels observed in this study irrespective of the size and pitch of an active pixel array. Further reduction in pixel noise may be possible through more optimized pixel circuit design, faster readout, or improvements in fabrication. [https://doi.org/10.1002/mp.14321]

Key words: active pixel arrays, correlated multiple sampling, noise performance, polycrystalline silicon thin-film transistors

1. INTRODUCTION

In the current era of x-ray imaging, applications that involve the capture of a single or a series of projection images (e.g., for radiography, fluoroscopy, mammography, etc.) are increasingly well-served by a variety of compact, electronic, solid-state imaging technologies offering real-time readout. One of these technologies, the active matrix, flat-panel imager (AMFPI), became ubiquitous following its initial conception in the late 1980s and commercial introduction around the turn of the century. Beyond projection imaging, AMFPIs facilitated the successful development and clinical implementation of the volumetric imaging techniques of tomosynthesis (e.g., for digital breast tomosynthesis, DBT) and cone-beam computed tomography, CBCT (e.g., for breast computed tomography, BCT, and kilo-voltage CBCT in the radiation therapy environment, kV-CBCT).[1–3]

Active matrix, flat-panel imagers consist of three principal components: a substrate on which a two-dimensional array of addressable pixels has been fabricated; an overlying x-ray converter material; and an external electronic acquisition system to control operation of the array. The converter takes the form of a photoconductor (typically amorphous selenium, a-Se) electrically coupled to the pixel circuits, or a scintillator (e.g., needle-like cesium iodide, CsI:Tl) optically coupled to photosensors incorporated into the pixels — for *direct* or *indirect detection* of the incident radiation, respectively. Active matrix, flat-panel imager pixel circuits typically consist of an addressing switch in the form of a single thin-film transistor (TFT), the drain of which is coupled to some form of pixel storage capacitor (e.g., a simple capacitor or a p-i-n photodiode for direct and indirect detection, respectively). The pixels are arranged in rows and columns, with the gate and source of each pixel TFT connected to gate and data address lines, respectively. The acquisition system controls the conductivity of the pixel TFTs via the gate lines — allowing accumulation of imaging signal in the pixel storage capacitors, followed by readout of that signal via the data lines, one row of pixels at a time. Preamplifiers located in the acquisition system magnify the imaging signals delivered by the data lines prior to digitization of those signals. The TFTs and photodiodes in AMFPI arrays are typically fabricated from hydrogenated amorphous silicon (a-Si:H) — a thin-film semiconductor material allowing fabrication of very large area, monolithic AMFPI arrays (currently up to ~43 × 43 cm^2) as well as displays for cell phones, computer screens, and televisions.

While AMFPIs provide valuable clinical information, their imaging performance can be limited by a relatively large magnitude of electronic additive noise (~1000 to 3000 e) compared to the size of the imaging signal (less than ~1000 e per interacting x-ray).[4] In particular, under conditions of low dose per image frame (such as those encountered in fluoroscopy, DBT, BCT or kV-CBCT), this results in an unfavorably low signal-to-noise ratio which reduces detective quantum efficiency and affects image quality.[4–6] The dominant source of additive noise is the preamplifier — which contributes a fixed (base) noise plus an amount that increases in proportion to the capacitance of the data line.[7] Since the data line capacitance of AMFPI arrays is largely due to the long data line length, ranging from ~20 to 43 cm on clinical devices (with capacitance further increasing with decreasing pixel-to-pixel pitch due to increased overlap of data and gate lines per unit data line length), the result is a large additive noise contribution.

There are, in general, two obvious strategies for overcoming this signal-to-noise limitation: direct reduction of the electronic additive noise or enhancement of the signal. Concerning the former strategy, substitution of the a-Si:H semiconductor material used for the addressing TFT in AMFPI pixels with a semiconductor offering higher mobility can allow reduction of the size of that TFT. This would decrease data line capacitance and, as a result, reduce the additive noise from preamplifiers. Examples of such semiconductors are indium gallium zinc oxide (IGZO) and low-temperature, laser-recrystallized polycrystalline silicon (poly-Si) — both of which were previously developed for fabrication of monolithic, large area displays. In a demonstration of this strategy, a prototype AMFPI array incorporating IGZO (which has an electron mobility approximately an order of magnitude higher than that of a-Si:H) exhibited reduced electronic additive noise, as low as ~700 e.[8]

Concerning the alternative strategy of enhancing the signal, two general approaches are being investigated. One approach focuses on the substitution of present AMFPI x-ray converters with alternatives that offer significantly (i.e., order of magnitude) higher imaging signal per x-ray interaction — such as provided by CsI:Tl coupled with a-Se operated under conditions of avalanche multiplication, or by various forms of polycrystalline HgI_2.[9–16]

The second approach is to incorporate an amplifier in the pixel circuit so as to magnify the imaging signal prior to readout — a concept commonly referred to as active pixel. Indirect detection active pixel arrays fabricated with crystalline silicon (c-Si) semiconductor have been extensively developed and are often referred to as active pixel sensors. Such devices improve signal-to-noise performance and have been successfully introduced to (or are under investigation for) applications such as dental imaging, imaging of extremities, and BCT.[17–19] However, c-Si does not lend itself to fabrication of the very large, monolithic arrays facilitated by a-Si:H, and c-Si circuits do not offer the high degree of radiation damage resistance offered by a-Si:H circuits. For that reason, the possibility of creating arrays with active pixel circuits has been investigated with a-Si:H [20–22] as well as with IGZO.[23,24] Our group has been exploring the use of poly-Si which offers electron and hole mobilities on the order of 10^2 cm^2/V-s — approximately 10^2 and 10^4 times higher than those of a-Si:H, respectively. The considerably higher mobilities of poly-Si (which are about an order of magnitude lower than those of c-Si) allow creation of sophisticated, CMOS-type circuits containing both n-type and p-type transistors. Poly-Si TFTs also demonstrate good radiation damage resistance, though less than that of a-Si:H TFTs.[25] By comparison, IGZO offers n-type mobilities only about an order of magnitude greater than a-Si:H and, like a-Si:H, provides only n-type transistors.

In this paper, the empirical noise performance of small area, active pixel prototype arrays incorporating poly-Si TFTs is reported and the results are compared with simulation predictions from a recently published circuit modeling formalism. The pixel circuits include both single-stage and two-stage amplifiers. While pixel circuits with single-stage amplifiers have the merit of simplicity, requiring as few as two transistors per pixel for a reset switch and a source-follower amplifier, pixel circuits with two-stage amplifiers (which require a minimum of one additional transistor such as for a common-source amplifier) can offer advantages — such as increased flexibility in design to attain a desired level of amplification, resulting in higher signal gain which can contribute toward lower noise.[26] Building upon the knowledge obtained from a first generation of poly-Si active pixel

demonstration arrays (which incorporated only two pixel circuit designs and multiplexing circuitry which restricted operation),[27] the pixel circuits examined in this study represent an exploration of various circuit design possibilities featuring variation in TFT dimensions and faster readout. This facilitated examination of pixel noise as a function of pixel circuit design over a wide range of operational conditions.

2. MATERIALS AND METHODS

2.A. Description of prototype active pixel arrays

Two prototype active pixel arrays were examined in this study: one with pixels incorporating single-stage amplifier circuits and the other with pixels incorporating two-stage amplifier circuits. These are hereafter referred to as the single-stage and two-stage arrays. Each array has a pixel pitch of 150 μm with the pixels arranged in 32 rows by 64 columns. The pixels along each row and column are addressed by means of gate lines and data lines, respectively. Figure 1 illustrates the general pixel circuit for each array, as well as connections to gate and data lines. Each data line is connected to an additional capacitor (data not shown), resulting in a total data line capacitance (C_{DATA}) of ~10 pF. The single-stage and two-stage arrays are based on pixel circuits that incorporate three (or four) and five TFTs per pixel, respectively — similar to that of previously reported, first-generation active pixel arrays, but without the inclusion of a photodiode structure that would allow the detection of incident x-rays.[27] As seen in Fig. 1, the two pixel circuits each have a reset transistor (TFT_{RST}), a source-follower transistor (TFT_{SF}), and an addressing transistor (TFT_{ADDR}), while the two-stage pixel circuit includes an additional common-source amplifier stage consisting of two transistors (TFT_{AL} and TFT_{CSA}) and an additional capacitor, C_{ST}. Half of the single-stage pixels also have a bias transistor, TFT_{BIAS}. Instead of the photodiode included in the first-generation arrays,[27] both pixel circuits include a pixel storage capacitor (C_{PIX}) with a nominal capacitance of 1 pF. For purposes of characterizing performance, a controlled amount of charge can be electronically injected to the pixels using the V_{BIAS} input — thereby providing signal simulating the effect of x-rays interacting with, for example, an x-ray converter positioned over an indirect detection array. Finally, for both arrays, each data line is connected to two transistors (TFT_{READ} and TFT_{DLRST}) located at the periphery of the array substrate.

Each array includes a number of pixel circuit designs which are primarily differentiated by variations in TFT width-by-length dimensions (labeled W/L and given in units of μm/μm). Note that the dimensions of each of TFT_{ADDR}, TFT_{READ}, and TFT_{DLRST} are fixed at 30/2×5, 50/10, and 50/10, respectively. (TFT dimensions where L is shown as a product indicate that the TFT is comprised of a multi-gate structure — where the first number designates the number of gates, and the second number the length of each gate.) Also, note that the inclusion of different pixel circuit designs on a given array was implemented to allow direct comparisons of the performance of various designs — free from potential process variations from array to array. For both arrays, design varies row-by-row and column-by-column. Table I indicates the row-by-row variations in blocks of eight designs — with a total of eight distinct variations in TFT_{SF} and TFT_{RST} dimensions for the single-stage array, and six distinct variations (with two variations repeated) in TFT_{CSA}, TFT_{AL}, and TFT_{SF} dimensions for the two-stage array. In each array, these blocks of eight designs are repeated four times over the 32 rows of the array. The column-by-column design variations are simpler. For the single-stage array, the pixel circuit alternately includes and excludes TFT_{BIAS}. For this study, the TFT_{BIAS} transistor was disabled by keeping it in the nonconducting state — allowing the results for pixels with and without this transistor to be combined, thereby increasing the number of pixels for which results of a given design are reported. For the two-stage array, the W/L dimensions of TFT_{RST} in the pixel circuit alternate between 6/3×5 and 6/10. The design variations were distributed across the area of each array in this manner so as to allow fabrication nonuniformities (which mainly originate from laser recrystallization of a-Si:H material to form poly-Si)[28] to affect pixels of all designs in a generally similar manner. Figure 2 shows microphotographs of several pixels in the single-stage and the two-stage arrays.

Figure 3 shows a picture of the two-stage array connected to peripheral printed circuit boards by means of wire bonds. Those circuit boards contain gate drivers, external preamplifiers, and other circuitry used to read out signals from the array pixels — controlled by a recently developed, modular, FPGA-based electronic acquisition system. Details of the features and operation of such arrays have previously been described in Refs. [27,29] and are summarized as follows. As indicated in Fig. 1, externally generated, digital control signals RESET, DLREAD, DLRESET, and ADDRESS are applied to the gates of TFT_{RST}, TFT_{READ}, TFT_{DLRST}, and TFT_{ADDR}, respectively, and are switched between −1 and 15 V. The supply voltages, V_{CC} and V_{CSA}, the external preamplifier reference voltage, V_{REF}, the grounding voltage, V_{GND}, and the data line reset voltage, V_{DLRST}, are set to 6, 6, 2.4, 2.5, and 2.05 V, respectively. The pixel reset voltage, V_{RST}, and the active load voltage, V_{AL}, were varied from 2.25 to 5.5 V and from 2.75 to 5.5 V, respectively. For both arrays, amplification is performed by means of TFT_{SF} which charges the data line to a voltage approaching that of the gate contact of TFT_{SF} whenever TFT_{ADDR} is made conducting. This charge remains stored in C_{DATA} (i.e., in the data line capacitance) until the read transistor (TFT_{READ}, located on the periphery of the array) is made conducting for a short time — resulting in the transfer of charge to the feedback capacitor (C_{FB}) of the external preamplifier.[30] For the two-stage array, additional amplification is provided to the gate of TFT_{SF} by means of the common-source amplifier stage, which transfers the charge from C_{PIX} to $C_{PIX\text{-}FB}$. A first-order approximation for the magnitude of the resulting charge amplification, referred to as in-pixel gain, is given by the ratios C_{DATA}/C_{PIX} and $C_{DATA}/C_{PIX\text{-}FB}$, corresponding to nominal amplification values of ×10 and ×30 for the single-stage and two-stage arrays, respectively.

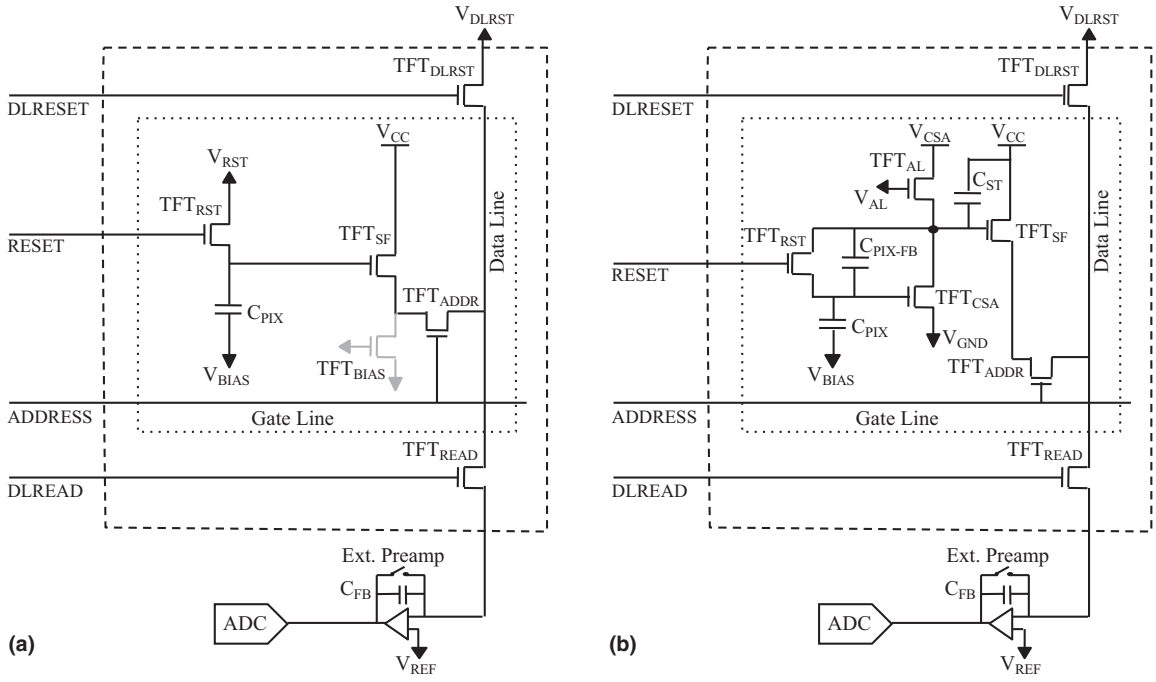

FIG. 1. Diagrams of the pixel circuit along with address lines and peripheral readout electronics for each of the two arrays examined in this study incorporating (a) a single-stage and (b) a two-stage amplifier. In both diagrams, circuit components located within each array pixel are bounded by the dotted box, components on the periphery of the array are bounded by a dashed box, and acquisition electronics external to the array are located outside the dashed box. Labels DLRESET and DLREAD refer to digital control signals globally provided to every data line on the array, ADDRESS refers to a digital control signal provided to the addressing transistor, TFT_{ADDR}, in each pixel along a given gate line, and RESET refers to a digital control signal globally applied to all pixels. V_{DLRST}, V_{RST}, V_{AL}, V_{BIAS}, V_{CC}, V_{CSA}, V_{GND}, and V_{REF} are global analog voltages. Note that for the single-stage array, half of the pixels include an additional transistor (TFT_{BIAS}, shown in gray). See text for further details.

TABLE I. Summary of the row-by-row variations in the width and length dimensions (W/L, in units of μm/μm) of TFTs for the single-stage pixel circuit designs (left side of table) and for the two-stage designs (right side of table) — along with the design identifiers used in this paper.

Single-stage designs			Two-stage designs			
Design ID	TFT_{SF}	TFT_{RST}	Design ID	TFT_{CSA}	TFT_{AL}	TFT_{SF}
SSD-1	200/5	6/3×5	TSD-1	400/10	10/30	30/10
SSD-1a	200/5	6/10	TSD-2	400/5	10/30	30/10
SSD-2	200/10	6/3×5	TSD-3	260/5	10/30	200/10
SSD-2a	200/10	6/10	TSD-4	260/10	10/30	200/10
SSD-3	200/20	6/3×5	TSD-5	260/5	20/60	30/10
SSD-3a	200/20	6/10	TSD-6	260/10	20/60	30/10
SSD-4	400/10	6/3×5	TSD-1	400/10	10/30	30/10
SSD-4a	400/10	6/10	TSD-2	400/5	10/30	30/10

2.B. Methodology for characterization of signal and noise performance

For each prototype array, characterization of the signal and noise performance of the various pixel circuit designs was carried out by operating the array at 31.25 data frames per second — with each frame consisting of eight acquisition samples. Each array was therefore entirely read out at a rate of 250 times per second. Figure 4 shows the timing diagram for a single acquisition sample. For each sample, the pixels were read out one gate line at a time by switching on the TFT_{ADDR} transistors of all the pixels along that line for a time interval of t_{ADDR} (referred to as the addressing time and ranging from 2 to 47 μs) and subsequently switching on the TFT_{READ} transistors for all data lines — resulting in the sampling of the charge stored in the capacitance of each data line by the external preamplifiers. As illustrated in the figure, the 32 gate lines of an array were read out consecutively at the rate of one gate line every 100 μs (which allows time for t_{ADDR}, as well as 11 μs for switching on TFT_{READ} and 11 μs for resetting the data line voltage by means of TFT_{DLRST}). In addition, for each acquisition sample, eight virtual gate lines were read out prior to readout of the gate lines of the array, as described above, but without switching on TFT_{ADDR}. Readout of these virtual gate lines allowed estimation of the contribution of external noise, defined as the electronic additive noise in the absence of noise contributions from circuitry in the pixel. (External noise includes the contribution of noise from the external preamplifier.) As indicated in the figure, the total time required for each acquisition sample, including the readout of both virtual and array gate lines, was 4 ms. Note that, for each data frame, reset of all array pixels is performed globally by switching on all reset transistors (TFT_{RST}) for 200 μs during readout of the virtual gate lines in the first sample.

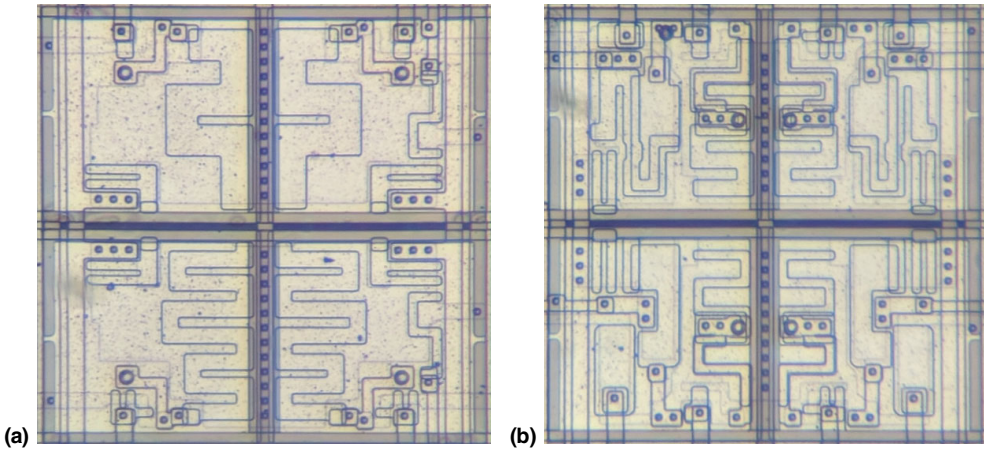

FIG. 2. Microphotographs of four adjacent array pixels corresponding to (a) single-stage pixel circuit designs SSD-3a (upper row) and SSD-4 (lower row), without (left column) and with (right column) the TFT_{BIAS} transistor; and (b) two-stage designs TSD-4 (upper row) and TSD-5 (lower row), with TFT_{RST} W/L dimensions of 6/10 (left column) and 6/3×5 (right column). [Color figure can be viewed at wileyonlinelibrary.com]

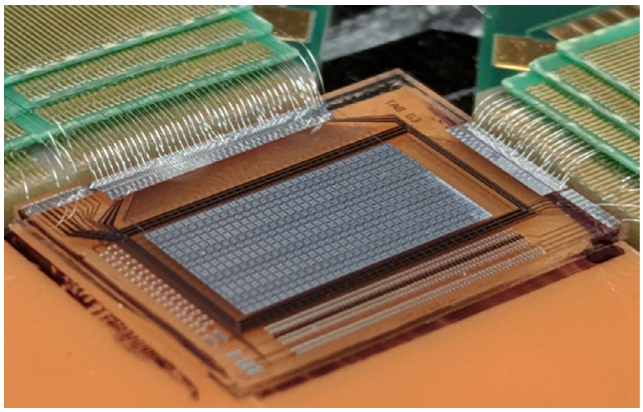

FIG. 3. Photograph of the two-stage prototype array mounted to peripheral printed circuit boards. [Color figure can be viewed at wileyonlinelibrary.com]

The eight acquisition samples obtained for each data frame were used to perform correlated multiple sampling (CMS) and the timing of those samples is shown in Fig. 5. For some of the measurements, the V_{BIAS} voltage was changed between samples #4 and #5 to inject charge into the pixels so as to simulate an x-ray exposure. For that reason, samples #1 through #4 are considered pre-exposure samples and samples #5 through #8 are considered post-exposure samples. Pixel signal was measured using three different CMS modes: CMS 1-1 which involves the subtraction of one pre-exposure sample from one post-exposure sample; and CMS 2-2 and CMS 4-4 which involve the subtraction of the average of two or four pre-exposure samples from the average of two or four post-exposure samples, respectively.

Characterization of signal and noise performance for the various designs involved measurement of pixel signal for a number of operating conditions, with each condition corresponding to a given addressing time, CMS mode, and set of operating voltages. For each condition, pixel signal was obtained at V_{BIAS} injection levels of +42 mV, −42 mV, and with no injection. (Note that a 42 mV injection at C_{PIX} provides a signal equivalent to an exposure of ~20 μR — corresponding to the use of a Hamamatsu 600 HL CsI:Tl converter with carbon backing using a 72 kVp x-ray spectrum (corresponding to RQA5 in IEC 61267) and a photodiode with 100% fill factor.) Determination of electronic additive noise (referred to as pixel noise in this paper) involved measurement of pixel signal with no charge injection. For each pixel and operating condition, the value of pixel noise, expressed in units of electrons [rms], was calculated from the standard deviation in pixel signal over 2000 frames of data. In order to facilitate comparison with the noise performance of AMFPIs, the result was then divided by the in-pixel gain which refers the measurement back to the input of the pixel amplifier. In this study, pixel noise is reported in terms of the median value among pixels of a given design. Determination of in-pixel gain involved measurement of pixel signal at the three charge injection levels. For each pixel and operating condition, the value of in-pixel gain was calculated from the average value of the slope obtained from a linear fit of these three signal levels plotted as a function of the injected charge. Note that the reported results exclude nonfunctional pixels and, for a given operating condition, pixels exhibiting nonlinear behavior that exceeds 30%.

2.C. Methodology for computer simulations of pixel noise

Computer simulations, based on the formalism detailed in Ref. [29], of the noise of individual pixels having circuits corresponding to the various pixel circuit designs of the prototype arrays were performed for the purposes of comparison with the measured results. The simulations employed the same timings, voltage levels, frame rate, and correlated multiple sampling modes as those used for the array measurements. For each simulation, the input signal was provided by adding a pulsed current source across C_{PIX} resulting in a

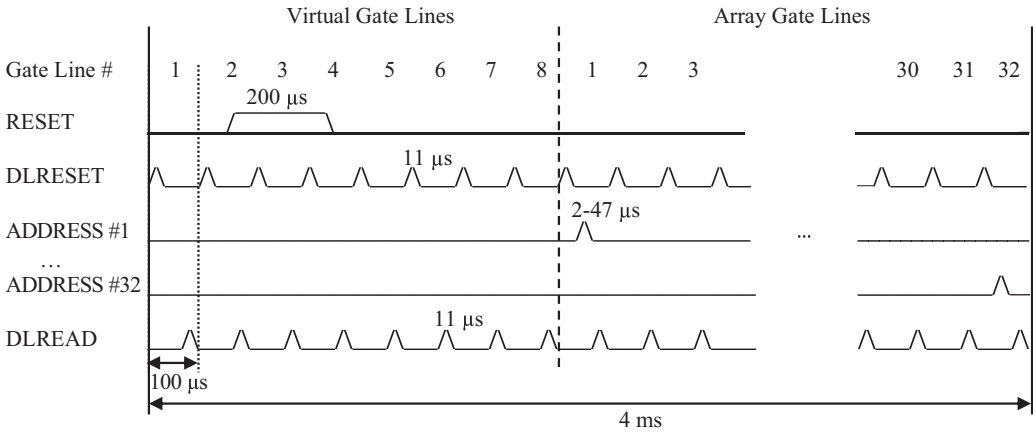

FIG. 4. Timing diagram for a single acquisition sample. For readout of each of the virtual and array gate lines, the timing for switching DLRESET and DLREAD is shown. In addition, the timing for switching ADDRESS for array gate lines #1 and #32 during the acquisition sample is also shown. The vertical-dashed line drawn through the figure delineates readout of the virtual gate lines from readout of the array gate lines, and the vertical-dotted line indicates the 100 µs used to read out each gate line. See text for further details.

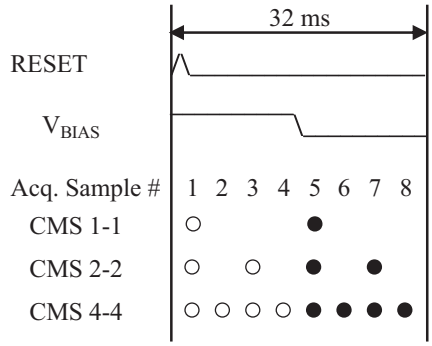

FIG. 5. Diagram illustrating the timing of the RESET control signal, the V_{BIAS} voltage and the eight acquisition samples obtained for each data frame read out from the arrays. In addition, the diagram indicates which samples were used for each correlated multiple sampling mode explored in this study (i.e., CMS 1-1, CMS 2-2, and CMS 4-4) — where the open and solid circle symbols refer to the pre-exposure and post-exposure samples, respectively. Note that the change in V_{BIAS}, which was employed for some of the measurements, was timed to occur between samples #4 and #5. See text for details.

signal similar to that provided by the −42 mV V_{BIAS} injection for the prototype arrays. The circuit simulations employed a transistor model based on the same parameter values employed in Ref. [29] where a subset of these values was derived from measurements obtained from individual poly-Si test TFTs. Noise performance was characterized in terms of thermal and flicker (also referred to as 1/f) noise components modeled as current sources between the drain and source of each transistor in the circuit.

3. RESULTS

3.A. In-pixel gain performance of the prototype arrays

Figures 6(a) and 6(b) show maps of the in-pixel gain for the pixels in the single-stage and two-stage arrays, respectively. For each array, the results were obtained at the operating condition that produced the lowest noise (reported in the following section). The median value of these in-pixel gain results is approximately ×9.3 and ×25 for the single-stage and two-stage arrays — within 10% and 20% of the nominal values (given in Section 2.A) of ×10 and ×30, respectively.

Careful examination of the maps in Fig. 6 reveals a number of interesting trends related to variations in the pixel circuit designs and in the orientation of pixel circuits across the arrays. First, for both arrays, the in-pixel gain is seen to vary from horizontal line to horizontal line, with the pattern repeating every eight lines — corresponding to the effect on performance as a result of the distribution of the various designs (see Table I). Next, the checker-board pattern along each horizontal line of the two-stage array corresponds to the effect on performance due to pixel-by-pixel alternation in the dimensions of the TFT_{RST} transistor between 6/3×5 and 6/10. In addition, intermittent pairs of adjacent pixels along horizontal lines of the single-stage array are observed to exhibit similar in-pixel gain. This intermittent pattern is the result of the combination of two factors: (a) the orientation of the circuits within the pixels is such that TFT_{SF} transistors are located physically close to each other for pairs of pixels along each horizontal line (as seen in Fig. 2(a)); and (b) the sweep of the laser beam used in creating the poly-Si material was slightly angled with respect to the direction of the horizontal lines (which is evident in the map of the zero-mean of the estimated threshold voltage of the TFT_{SF} transistors for this array — not shown, but similar to that shown in Ref. [31] for another array having the same pixel circuit designs). As a result of these two factors, variation in in-pixel gain among the pixels is reduced for those pairs of neighboring pixels for which the laser happened to pass over both TFT_{SF} transistors in a given sweep.

Figure 7 shows 3-D plots of in-pixel gain for CMS 4-4 mode plotted as a function of t_{ADDR}, as well as a function of

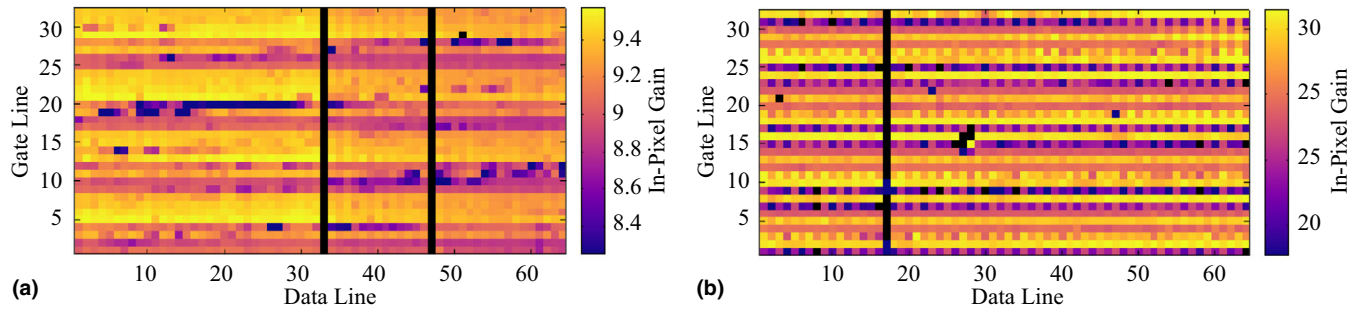

FIG. 6. Maps of the in-pixel gain for pixels of (a) the single-stage array and (b) the two-stage array. The results were obtained at t_{ADDR} of 47 μs and for CMS 4-4 mode. In addition, V_{RST} and V_{AL} were set to 3.25 and 3.5 V for the single-stage array and two-stage array, respectively. Note that the black lines correspond to nonfunctional data lines while individual black pixels correspond to nonresponsive pixels as well as to pixels with signal response exhibiting more than 30% nonlinearity. [Color figure can be viewed at wileyonlinelibrary.com]

V_{RST} and V_{AL} for a single-stage and two-stage pixel design, respectively. The results correspond to the median values obtained from pixels with design SSD-1 for the single-stage array [Fig. 7(a)] and from pixels with design TSD-1 for the two-stage array [Fig. 7(b)]. For both pixel designs, in-pixel gain is seen to increase with increasing t_{ADDR} — due to the increase in signal following charge integration on the data line capacitance, C_{DATA}. For the two-stage design, in-pixel gain remains high (i.e., at or above approximately ×19) over the range of t_{ADDR} used in the measurements. This is not the case for the single-stage design where in-pixel gain values were found to be low under some conditions, especially for small t_{ADDR}. For the single-stage design, in-pixel gain exhibits a quasi-bell-shaped behavior as a function of V_{RST} — with in-pixel gain values remaining relatively constant for V_{RST} in the range of 3.25 to 4.5 V, and dropping at small and large V_{RST}. The drop at low V_{RST} is due to the TFT_{SF} transistor becoming less conductive when the V_{RST} value approaches the threshold voltage of the transistor, while the drop at high V_{RST} is due to an increasingly sublinear response of the external preamplifier for V_{RST} values above 4.5 V. For the two-stage design, in-pixel gain exhibits a saddle-like behavior as a function of V_{AL}, remaining relatively constant for V_{AL} in the range of 3.0 to 4.25 V — with an overall trend of generally increasing with increasing V_{AL}. Note that similar behavior for in-pixel gain was observed from the other designs for both arrays and for the other CMS modes.

3.B. Pixel noise performance of the prototype arrays

Pixel noise measurement results are reported for the half of the pixels in each array having a triple-gate TFT_{RST} transistor with W/L dimensions of 6/3×5 — which provides lower leakage current leading to slightly better noise performance than pixels having a single-gate TFT_{RST} transistor with W/L dimensions of 6/10. Given the distribution of pixel circuit designs in the array as described in Section 2.A, results are therefore shown for designs SSD-1, SSD-2, SSD-3, and SSD-4 for the single-stage array and for designs TSD-1 to TSD-6 on every other data line for the two-stage array.

Figure 8(a) shows measured pixel noise as a function of V_{RST} for the single-stage array. The results were obtained at t_{ADDR} of 47 μs and for CMS 4-4 mode. For all designs, pixel noise is seen to exhibit the lowest values for V_{RST} in the range of 3.25 to 3.75 V. At small and very large V_{RST}, pixel noise is seen to increase significantly due to a large decrease in the in-pixel gain (e.g., see Fig. 7(a)), diminishing the effectiveness of the active pixel circuit. A comparison of the results in Fig. 8(a) for the various designs indicates that SSD-1 (which has the smallest area, given by W × L, as well as the shortest length, L, for the TFT_{SF} transistor) exhibits the highest pixel noise. This is a result of increased flicker noise, which is inversely proportional to the transistor area (see eq. (1) in Ref. [29]), as well as increased leakage and subthreshold currents, which generally increase with decreasing length of the TFT_{SF} transistor[32] — both leading to higher noise from the source-follower stage. SSD-3 and SSD-4, each having a TFT_{SF} transistor four times larger in area than that of SSD-1, generally provide the lowest pixel noise — with median values down to ~695 e for SSD-3. Despite having the same TFT_{SF} area as SSD-3, the somewhat higher pixel noise exhibited by SSD-4 can be attributed to the shorter length of that transistor.

Figure 8(a) also shows the measured external noise where, for each value of V_{RST}, the result has been scaled by the appropriate in-pixel gain in order to provide meaningful comparisons with the measured pixel noise results for SSD-1. The shape of the external noise is generally similar to that of pixel noise — with relatively constant values except for sharp increases at low and high V_{RST} as a result of decreasing in-pixel gain. Results for the external noise corresponding to other designs, which are not shown in the figure, are very similar, except for some deviations at small and large V_{RST} due to relative variations in the in-pixel gain. For all designs, the magnitude of external noise (as low as ~312 e for SSD-1) is small compared to pixel noise, demonstrating the effectiveness of the single-stage design for reducing the relative contribution of this noise source.

Figure 8(b) shows results for simulated pixel noise corresponding to the same designs and operating conditions as those of the measured results reported in Fig. 8(a). These simulated noise results include flicker and thermal noise

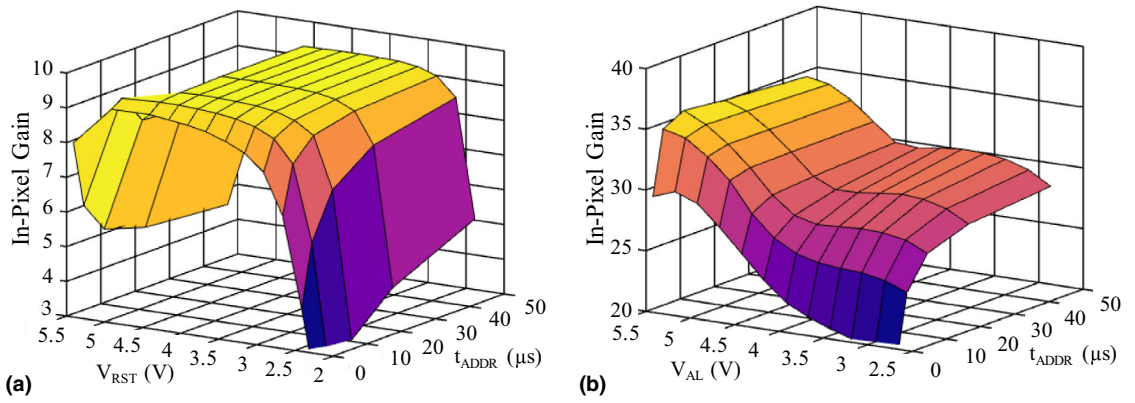

FIG. 7. Plots of in-pixel gain for pixels corresponding to (a) pixel circuit design SSD-1 of the single-stage array and (b) design TSD-1 of the two-stage array, plotted as a function of V_{RST} and V_{AL}, respectively, as well as a function of t_{ADDR}. See text for further details. [Color figure can be viewed at wileyonlinelibrary.com]

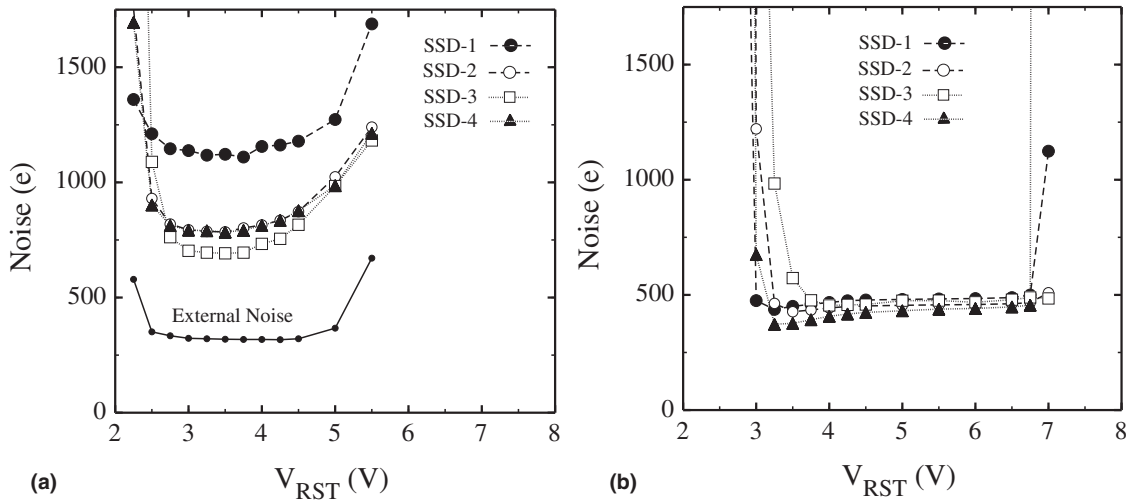

FIG. 8. (a) Measured and (b) simulated pixel noise as a function of V_{RST} for four of the pixel circuit designs of the single-stage array. The measured external noise corresponding to SSD-1 is also shown in (a). See text for further details.

contributions as well as the measured contribution of external noise (such as shown in Fig. 8(a)) — all added in quadrature. Note that, while the general shape and trend of the measured pixel noise are reproduced by the simulations, the magnitude of the simulated noise is significantly lower. This difference can be mainly attributed to the fact that the simulations employ signal and flicker noise parameter values[29] obtained from a different poly-Si wafer with well-performing individual test TFTs that have different characteristics than those of the TFTs of the prototype array — including lower leakage and subthreshold currents. The lower leakage and subthreshold currents in the simulations lead to lower noise from the source-follower stage, resulting in a reduced contribution to pixel noise. This reduced contribution makes the relative contribution of external noise to the simulation results more significant — further reducing the difference in performance between the various designs, as seen in Fig. 8(b). Finally, note that the simulated results in Fig. 8(b) appear shifted along the x-axis (i.e., to higher V_{RST} values) compared to the measured results in Fig. 8(a). This shift is a reflection of differences in the mean threshold voltage of the TFTs in the array and the threshold voltage used in the simulation model.

Figure 9(a) shows measured pixel noise as a function of V_{AL} for the two-stage array. The results were obtained at t_{ADDR} of 47 µs and for CMS 4-4 mode. The measured external noise, scaled by the appropriate in-pixel gain so as to correspond to TSD-1, is also shown. For all designs, pixel noise is seen to exhibit a slight increase with increasing V_{AL} over most of the range of V_{AL} considered. For the highest V_{AL}, pixel noise increases sharply due to significant reduction in current flow through TFT_{AL}, rendering the circuit inefficient in transferring charge from C_{PIX} to $C_{PIX\text{-}FB}$. TSD-5 and TSD-6 generally exhibit the lowest pixel noise — with TSD-6 providing median values as low as ~866 e. As seen in the figure, the measured external noise is even lower (down to ~151 e for TSD-1) than that of the single-stage array due to the higher in-pixel gain provided by the pixel circuit — rendering the relative contribution of external noise insignificant.

Figure 9(b) shows results for simulated pixel noise corresponding to the same designs and operating conditions as

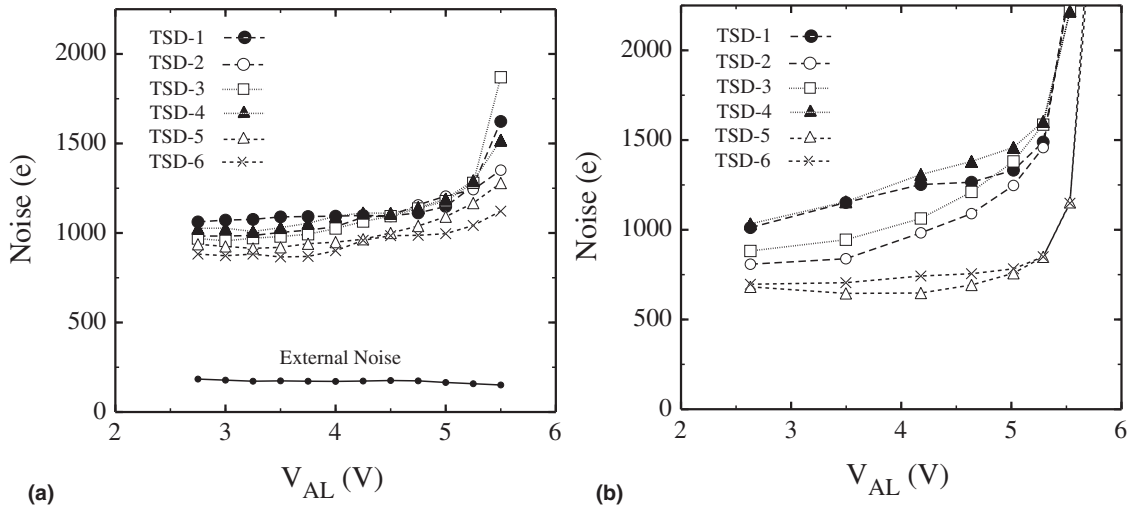

FIG. 9. (a) Measured and (b) simulated pixel noise as a function of V_{AL} for the six pixel circuit designs of the two-stage array. The measured external noise corresponding to TSD-1 is also shown in (a). See text for further details.

those of the measured results reported in Fig. 9(a). These simulated noise results are in generally better agreement with their measured counterparts compared to the situation for the single-stage designs. As was the case for the single-stage array, the two-stage array came from a different wafer compared to the TFTs used to provide the parameters in the simulations. (Note that the single-stage and two-stage arrays came from separate wafers while all parameters used in the simulations came from TFTs on yet another wafer.) While the measured performance of the TFTs in the two-stage array is believed to be closer to the performance of the TFTs used in the simulations, the reason for the better agreement can mainly be attributed to the combination of two other effects. First, the relative noise contributions from the source-follower stage are reduced by virtue of the additional factor of three in gain provided by the common-source amplifier stage. Second, unlike the situation for the single-stage array, the common-source amplification stage was generally operated in a regime where the current is much greater than leakage and subthreshold currents, making the circuit less prone to the noise attributed to those currents. Interestingly, the diminished influence of the source-follower stage is demonstrated by the fact that designs TSD-3 and TSD-4 have no apparent advantage in noise performance — despite featuring much larger TFT_{SF} transistors than the other four designs. TSD-5 and TSD-6 generally show the lowest noise — believed to be a consequence of employing the TFT_{AL} transistor having the largest area. This is an indication that, for TSD-1, TSD-2, TSD-3, and TSD-4, the flicker noise originating from TFT_{AL} dominates that from TFT_{CSA}.[29] Finally, the narrower spread of the measurement results compared to the simulation results may be a consequence of additional noise affecting the measurements — which is not accounted for in the simulations. One possible candidate for such additional noise is

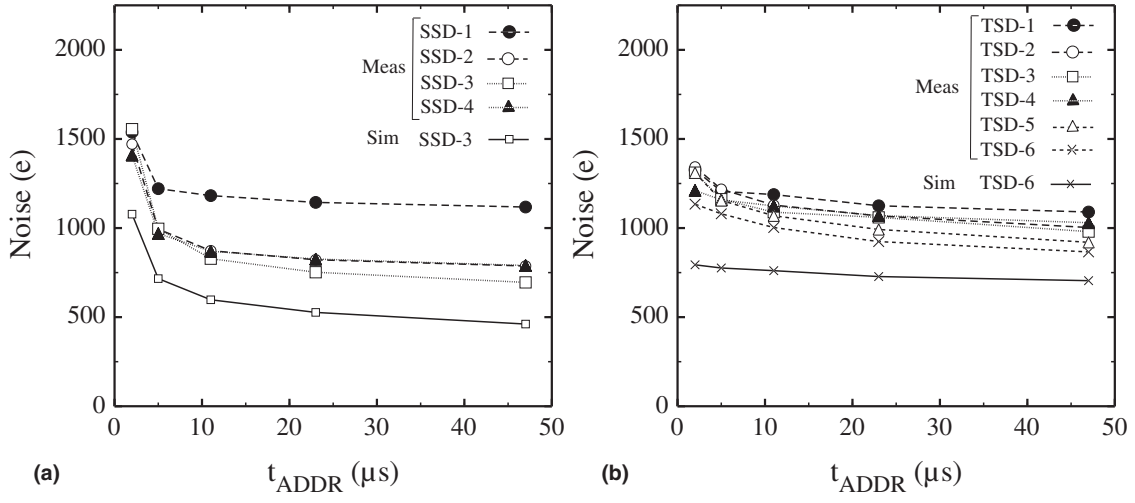

FIG. 10. Measured pixel noise as a function of t_{ADDR} for various pixel circuit designs of (a) the single-stage array and (b) the two-stage array. For purposes of comparison, simulated pixel noise is also shown for designs SSD-3 and TSD-6 for the single-stage and two-stage arrays, respectively.

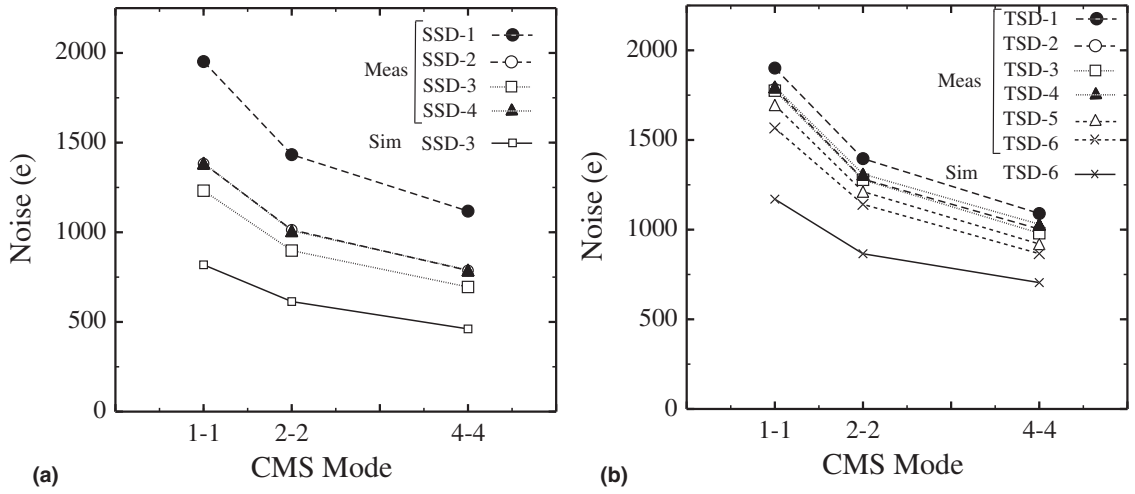

FIG. 11. Measured pixel noise as a function of CMS mode for various pixel circuit designs of (a) the single-stage array and (b) the two-stage array. For purposes of comparison, simulated pixel noise is also shown for designs SSD-3 and TSD-6 for the single-stage and two-stage arrays, respectively.

voltage fluctuations on the supply rail (V_{CSA}) for the common-source amplifier.

Figure 10(a) shows measured pixel noise as a function of t_{ADDR} for SSD-1, SSD-2, SSD-3, and SSD-4 of the single-stage array. The results were obtained at V_{RST} of 3.25 V and for CMS 4-4 mode. For purposes of comparison, simulated pixel noise for SSD-3 at V_{RST} of 4.5 V and for the same mode is also shown. Note that different values of V_{RST} were used for the measurements and simulations in order to establish meaningful comparisons. The choice of different values of V_{RST} is a reflection of differences in the mean threshold voltage of the TFTs in the array and that of the simulation model, as mentioned in the discussion of the results of Fig. 8. These values were determined from curves of the average in-pixel gain across all reported designs as a function of V_{RST} — which exhibit a shift between measured and simulated results similar to that observed between the results in Figs. 8(a) and 8(b). The values correspond to the lowest V_{RST} for which the average in-pixel gain exhibits only minor dependence on V_{RST} (i.e., Δ(in-pixel gain)/$\Delta V_{RST} \leq 0.125\ V^{-1}$) — resulting in values of V_{RST} for the measured and simulated results that correspond to similar response of the circuit, irrespective of the differences in TFT threshold voltage. Both the measured and simulated pixel noise decrease with increasing t_{ADDR} due to increasing charge integration and settling on C_{DATA}. Short addressing times truncate the integration of charge on C_{DATA} resulting in reduced in-pixel gain, reduced noise filtering, and an operation point that is more susceptible to jitter in t_{ADDR} — which in turn lead to increased pixel noise. Note that design SSD-3 outperforms the other designs for addressing times of 11 μs and longer, as is apparent in Fig. 8(a) for t_{ADDR} of 47 μs for reasons explained for those results. However, this is not the case at addressing times shorter than 11 μs — a consequence of SSD-3 having the smallest ratio of W/L which results in slower charge integration on C_{DATA}.

Figure 10(b) shows measured pixel noise as a function of t_{ADDR} for designs TSD-1 to TSD-6 of the two-stage array. For purposes of comparison, simulation results for TSD-6 are also shown. All results were obtained at V_{AL} of 3.5 V (where pixel noise is lowest) and for CMS 4-4 mode. Similar to the situation for the measured single-stage results in Fig. 10(a), the measured pixel noise for the two-stage array is seen to decrease with increasing t_{ADDR}. However, for the simulation results, such decrease is not significant, as demonstrated by a weak dependence of pixel noise on t_{ADDR} for addressing times of 11 μs and longer — a behavior that may be attributed to the reduced influence of TFT_{SF} on pixel noise in the two-stage designs. The stronger dependence of the measured pixel noise on t_{ADDR} observed at shorter addressing times may be a result of additional noise sources not accounted for in the simulations, such as voltage fluctuations on V_{CSA} and jitter in t_{ADDR}.

Figure 11 shows measured pixel noise as a function of CMS mode for t_{ADDR} of 47 μs for the same designs as in Fig. 10. Results are reported for the single-stage array at V_{RST} of 3.25 V in Fig. 11(a) and for the two-stage array at V_{AL} of 3.5 V in Fig. 11(b). For purposes of comparison, simulated pixel noise for SSD-3 at V_{RST} of 4.5 V and TSD-6 at V_{AL} of 3.5 V (as in Fig. 10) using the same t_{ADDR} is also shown. As expected, measured pixel noise is seen to improve with the number of samples used — as also predicted by the simulation results.[29] By employing correlated multiple sampling, the subtraction of pre-exposure from post-exposure samples removes the contributions of any noise components that are correlated with time, such as pixel kTC reset noise and low-frequency flicker noise. However, for CMS 1-1 mode, where one pre-exposure sample is subtracted from one post-exposure sample, the contribution of any uncorrelated noise (such as external noise, line noise and higher-frequency flicker noise) is doubled geometrically due to this subtraction. When a

larger number of pre- and post-exposure samples are averaged before subtraction (i.e., for CMS 2-2 mode and CMS 4-4 mode), pixel noise is progressively reduced through reduction of the uncorrelated noise.

4. DISCUSSION AND CONCLUSIONS

Results from an empirical investigation of the noise performance of a pair of prototype active pixel arrays, employing poly-Si TFTs and operated in the absence of radiation, have been reported. Among the various pixel circuit designs examined, median pixel noise values as low as ~695 e for single-stage design SSD-3 and 866 e for two-stage design TSD-6 have been observed — well below the ~1000 to 3000 e values exhibited by current clinical AMFPI systems. Moreover, while AMFPI noise increases with increasing array size or with decreasing pixel pitch, it should be possible, through proper design, to maintain the levels of noise observed from the prototype arrays irrespective of array size and pitch. This advantageously lower level of noise derives from the fact that the in-pixel amplification and correlated multiple sampling capabilities provided by active pixel arrays can reduce the relative contribution of noise outside of that originating from the pixel circuitry — which is referred to as external noise in this study and which, for both active pixel and AMFPI arrays, is dominated by the noise of the external preamplifier. The measured median in-pixel gain for the prototype arrays was found to be ×9.3 and ×25 for the single-stage and two-stage arrays, respectively — values large enough to render external noise insignificant, particularly for the two-stage array. As a result, the contribution of external noise was estimated to be lower than 340 e for both arrays, far less than the lowest median pixel noise for either array. Note that the higher pixel noise exhibited by the two-stage array compared to the single-stage array, which is in line with expectations from the simulations, is a simple consequence of the fact that the pixel circuit designs for the two-stage array are not fully optimized.[29] Also note that the pixel noise performance reported in the present study would be very similar to that for arrays designed with the same pixel circuits as in this study, but capable of being operated with radiation by using (for example) a-Si:H photodiode in place of C_{PIX} in each pixel — since measurements of additive noise are conducted in the absence of an injected signal or radiation.

While the noise performance of the prototype arrays is encouraging, it is still inferior to that offered by c-Si active pixel sensors. Although further tuning of TFT dimensions to allow larger TFT_{SF} transistors for single-stage pixel circuits (or larger TFT_{AL} and TFT_{CSA} transistors for two-stage pixel circuits) may lead to some improvement in noise performance, such an approach is constrained by the finite space available within a pixel. A more promising approach may lie in focusing on the reduction of flicker noise through better fabrication techniques — given that, as indicated by the simulations, TFT flicker noise is generally the dominant contributor to pixel noise.[29] In a previous study, it was shown that noise power spectral density values from individual poly-Si test TFTs, of the type used in the prototype arrays and simulations, vary significantly,[29] leading to less-than-desirable overall noise performance. This suggests that reduction in process variations (for example, originating from the laser recrystallization process) could improve noise performance. In addition, flicker noise could also be reduced through faster readout, where acquisition samples would be obtained closer in time — allowing correlated multiple sampling to be more efficient by reducing noise over a wider frequency range. Faster readout could be made possible through improved mobility of poly-Si TFTs and/or through the use of schemes that allow pipelined or more parallel readout. Flicker noise could also be reduced through improvement in the in-pixel amplification circuit by, for example, replacing the TFT_{AL} transistor with a resistor as well as adding a low-pass resistor in front of C_{ST} for the two-stage pixel circuit, as explored in a previous simulation study.[29]

In this study, the prototype arrays were operated at 31.25 fps, allowing the acquisition of eight samples per frame. The time required for each sample was 4 ms, corresponding to the readout of a total of 40 gate lines. In a clinical imaging system employed, for example, for fluoroscopy, the number of gate lines would be on the order of a thousand, which would necessitate the reduction of time required for readout of each gate line from the current 100 μs to ~4 μs in order to maintain a frame rate of 30 fps with eight acquisition samples per frame. Such a short readout time would necessitate the use of addressing times shorter than 4 μs, since t_{ADDR} is only a portion of the readout time. However, as seen in Fig. 10, pixel noise performance deteriorates for short t_{ADDR} due to truncation of signal during charging of the data line. Therefore, in order to maintain the use of longer addressing times, readout schemes involving pipelining or parallel readout such as dual-sided readout would be necessary. An alternative readout scheme, which employs a simpler control sequence, would involve current readout instead of voltage readout.[20] In that readout scheme, signal is sampled directly by the external preamplifier where the pixel circuit is directly coupled to the virtual ground input of the preamplifier, effectively shunting the data line capacitance to ground and thus allowing faster readout speed. Through exploration of these various strategies for lower noise and faster readout speed, poly-Si-based active pixel arrays could potentially achieve noise levels similar to those offered by c-Si active pixel sensors.

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CONFLICT OF INTEREST

The authors have no conflict to disclose.

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