Efficient and Interference-Resilient Wireless Connectivity for IoT Applications

by

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Abstract

With the coming of age of the Internet of Things (IoT), demand on ultra-low power (ULP) and low-cost radios will continue to boost tremendously. The Bluetooth-Low-energy (BLE) standard provides a low power solution to connect IoT nodes with mobile devices, however, the power of maintaining a connection with a reasonable latency remains the limiting factor in defining the lifetime of event-driven BLE devices. BLE radio power consumption is in the milliwatt range and can be duty cycled for average powers around 30μW, but at the expense of long latency. Furthermore, wireless transceivers traditionally perform local oscillator (LO) calibration using an external crystal oscillator (XTAL) that adds significant size and cost to a system. Removing the XTAL enables a true single-chip radio, but an alternate means for calibrating the LO is required. Innovations in both the system architecture and circuits implementation are essential for the design of truly ubiquitous receivers for IoT applications.

This research presents two porotypes as back-channel BLE receivers, which have lower power consumption while still being robust in the presents of interference and able to receive back-channel message from BLE compliant transmitters. In addition, the first crystal-less transmitter with symmetric over-the-air clock recovery compliant with the BLE standard using a GFSK-Modulated BLE Packet is presented.

Chapter 1. Introduction

1.1 Evolution of Computing Devices

Since the invention of the transistor in 1947, the design and fabrication technologies for electronics have astronomically advanced in a relatively short period of time. With every new breakthrough, new applications get introduced as the chips become more powerful and their cost reduces. The large mainframes used in the 1950s were developed into smaller and more powerful workstation within the next decade. Afterwards, personal computers were introduced in the 1980s and later became commonly used in daily life in developed nations. The emergence of the internet as a publicly available service in the 1990s helped connectivity play a more important role in driving the direction of technology. With the explosive growth of smart phones and tablet PCs in the 2000s, the number of connected devices exceed the word population and it has continued to grow to become multiple connected devices per person with the biggest contribution to this

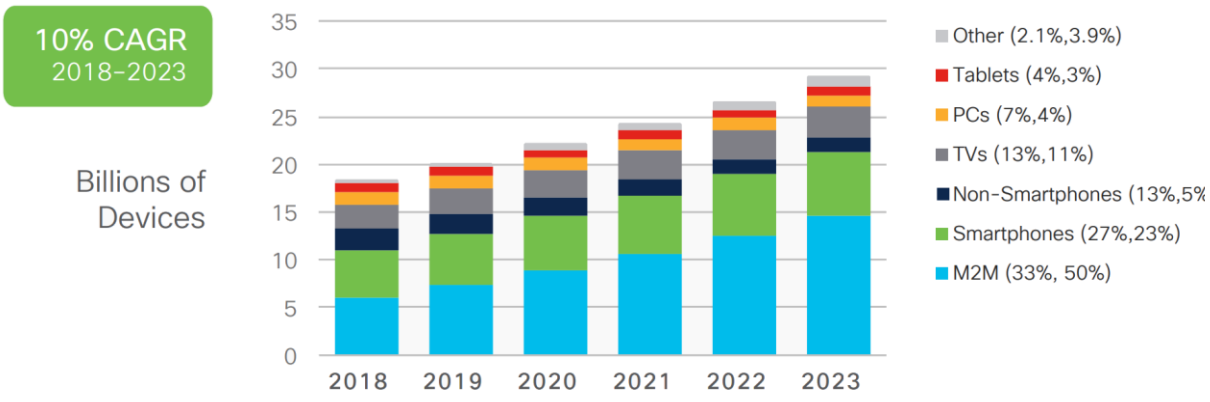


Fig.1.1 The estimated number of connected devices exceeded one per person in 2008 [1].

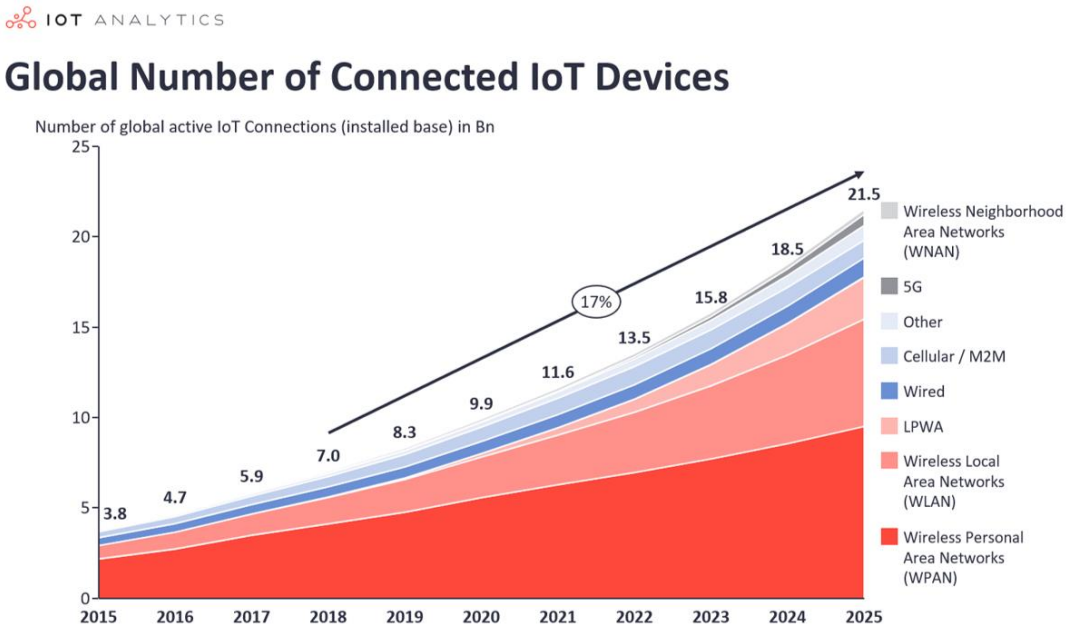


Fig.1.2 Global number of IoT connected devices [2].

increase coming from machine to machine (M2M) commutations (Fig.1.1) [1]. Consequently, internet of things (IoT) is expected to drive a significant portion of the growth in the number of connected devices over the next decade [2].

1.2 IoT Emerging Applications

IoT technologies are evolving rapidly to reach new applications replacing older technologies or creating new areas that haven't been explored before. For instance, sensing and actuation are becoming more ubiquitous than ever before thanks to the growing number of connected devices, especially those using personal or local level communication networks (Fig.1.2) [3]. Different commercial products are being introduced in the market for diverse applications, including, but not limited to: smart homes, cars, factories and healthcare. An example application for healthcare is using smart electronic devices to help monitor critical physiological parameters. Beyond sensing, the node can be used to interpret the data and alert the user if any abnormality is detected. Similar to most other IoT applications, these electronic devices have

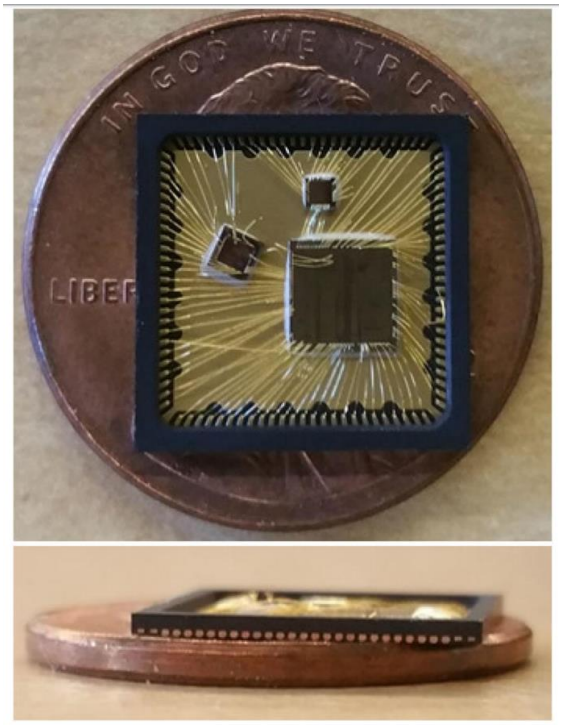


Fig.1.3 Bonded SiP (setup unit). The radio is on the top, the SoC on the bottom and the memory on the left [4].

stringent requirements when it comes to their size, cost and energy efficiency. In addition, these devices are expected to connect using adopted commination standards which allows them to seamlessly integrate with the existing infrastructure.

These promising potential applications have motivated a lot of research efforts recently to focus on designing new systems with a performance that meets these applications' requirements. For instance, [4] presents an ultra-low-power (ULP) wireless sensing heterogeneous system-in-package (SiP) including: a system-on-chip (SoC) , a non-volatile memory and a FSK transmitter (Fig.1.3). The average power reported is around 1.02µW which enables it as a self-powered platform. Moreover, [5] demonstrates a battery-powered single-chip SoC solution to monitor multiple vital signs (Fig.1.4). Readouts of EKG and bio-impedance are included among multiple other sensor interfaces. When all sensors readouts are enabled, the average consumed power is 769µW. This includes an on-chip BLE 4.2 radio to transmit data using the BLE standard in burst

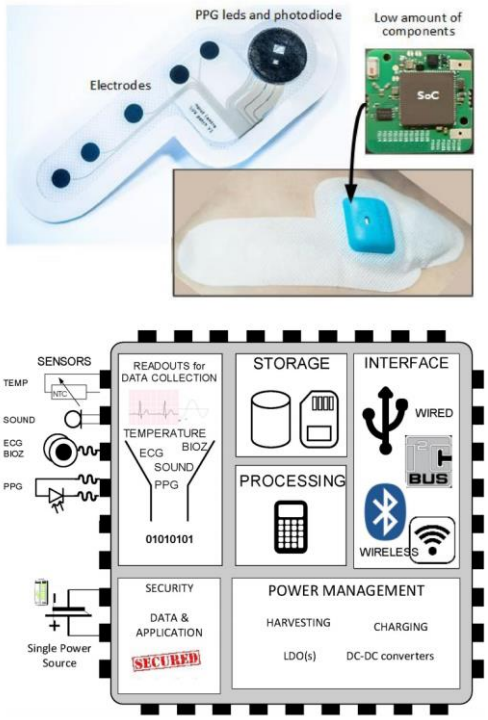


Fig.1.4 Single-Chip SoC With BLE Vital Sign Monitoring [5].

mode. This SoC provides a solution for remote health monitoring using wirelessly connected wearable devices. Furthermore, [6] shows an energy harvesting based low-power SoC for machine health monitoring (Fig.1.5). The self-powered system integrates: a processor, accurate reference oscillator, digital processing and a wake-up receiver while consuming an average power of 89.1µW. Such a system eliminates the battery dependency, which would create a challenge if deployed in large numbers and had to be replaced frequently, and help forecast machine failures to increase their efficiency and reduce cost.

1.3 Wireless connectivity for IoT Devices

Efficient wireless connectivity is an important requirement for IoT applications and has attracted a lot of research interest recently since it's the most energy intensive task [7]. The radios designed for such applications need to be low power while still supporting sufficient communication range and co-existing with other radios that share the same frequency band. In

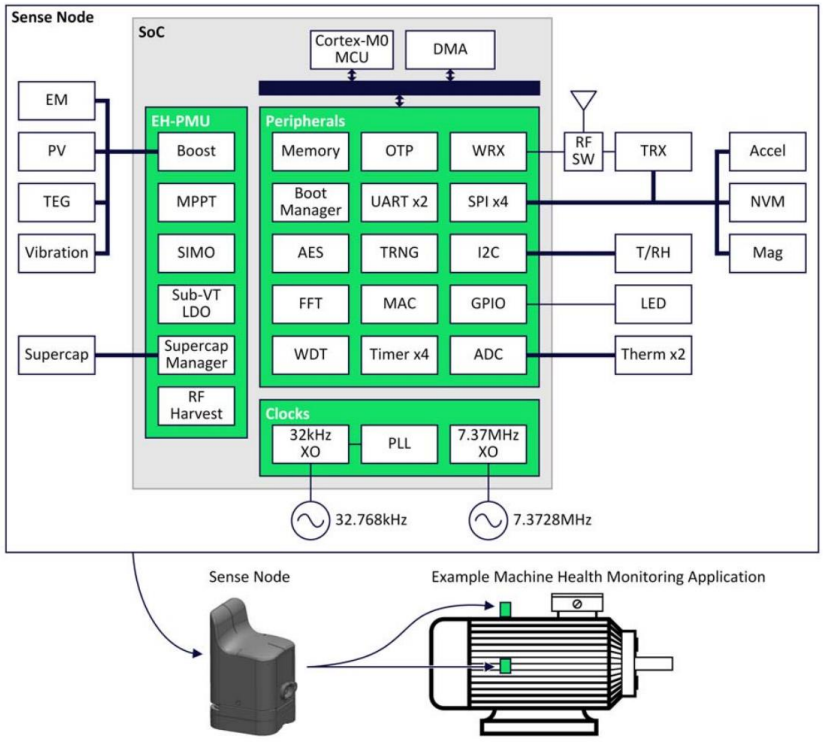


Fig.1.5 ULP SoC for continuous machine health monitoring wireless self-powered system [6].

addition, supporting adopted communication standards is key for ubiquitous integration with the existing infrastructure. This chapter presents a review of the recent design trends and techniques in ultra-low power radios for IoT applications.

Innovations in both the system architecture and circuits implementation are essential for the design of truly ubiquitous receivers for IoT applications. RF interference will increase since the limited bandwidth is shared with a rapidly growing number of IoT devices using multiple heterogeneous wireless communication standards. Integrated solutions for interference rejection pose a real challenge in ULP radio design since they typically require high power and will increase the receiver total power significantly, especially with narrowband channels [8, 9]. The design challenge in radios for IoT applications is to minimize the power consumption with an adequate sensitivity level in a congested frequency spectrum using highly integrated solutions while still being compatible with an adopted communication standard [10, 11].

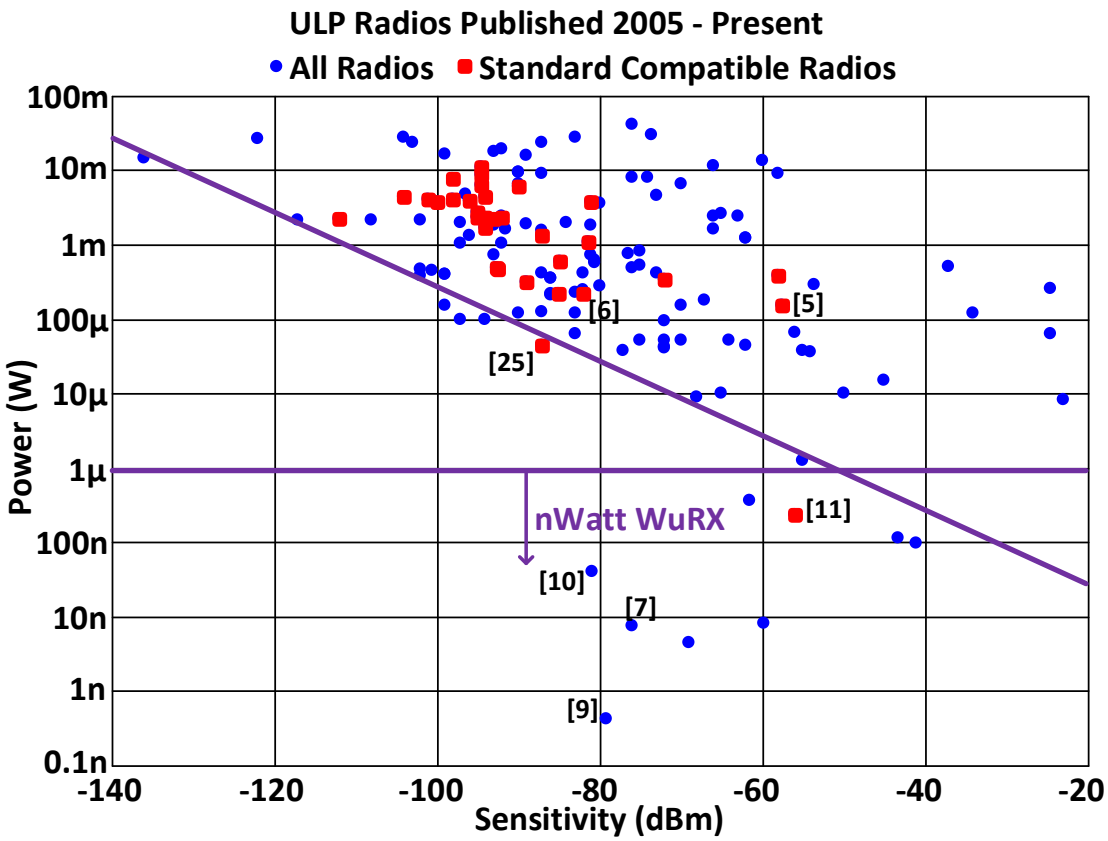


Fig.1.6 Ultra-low power radio survey: sensitivity vs. power.

Multiple approaches to reduce the receiver's power consumption have been reported recently [12–17]. These primarily tackle the most power hungry blocks such as the RF local oscillator (LO) and RF low noise amplifiers (LNAs). For example, RF energy detection is used to convert the incoming RF signal to DC without using any RF local oscillators, which leads to significant power reduction. In addition, removing active RF gain will lower the power further [18]. Furthermore, mixer-first architectures, for example, avoid using RF gain but still use an RF LO to down-convert the signal to baseband which efficiently enhances the receiver's sensitivity and selectivity performance since gain and filtering is done at baseband [12, 13, 19–23].

1.4 Ultra-Low Power Radios Design Trends

A survey of ULP radios published in top tier circuits journals and conferences is done to

identify the research directions in their design and its limitations [24] . Fig.1.6 shows the power vs sensitivity (range) trade-off for the recent 179 published ULP receivers. With the exception of nanowatt wake-up radios, an empirical line with a slope of ½ bounds the performance. This implies the power will increase by a factor of 10 for a 10x increase in the receiver range (assuming a path-loss coefficient of 2). When the sensitivity is normalized to the data rate, however, the power vs sensitivity trade-off becomes more settled since nanowatt radios have relatively low data rates (Fig.1.7). In both figures, standard compliant radios clearly tend to be higher power. This is expected since most standards nowadays have stringent requirements on sensitivity, interference rejection and frequency accuracy. To achieve these specifications, high power receiver blocks might become required such as LNAs, active filters with sharp frequency response and phase

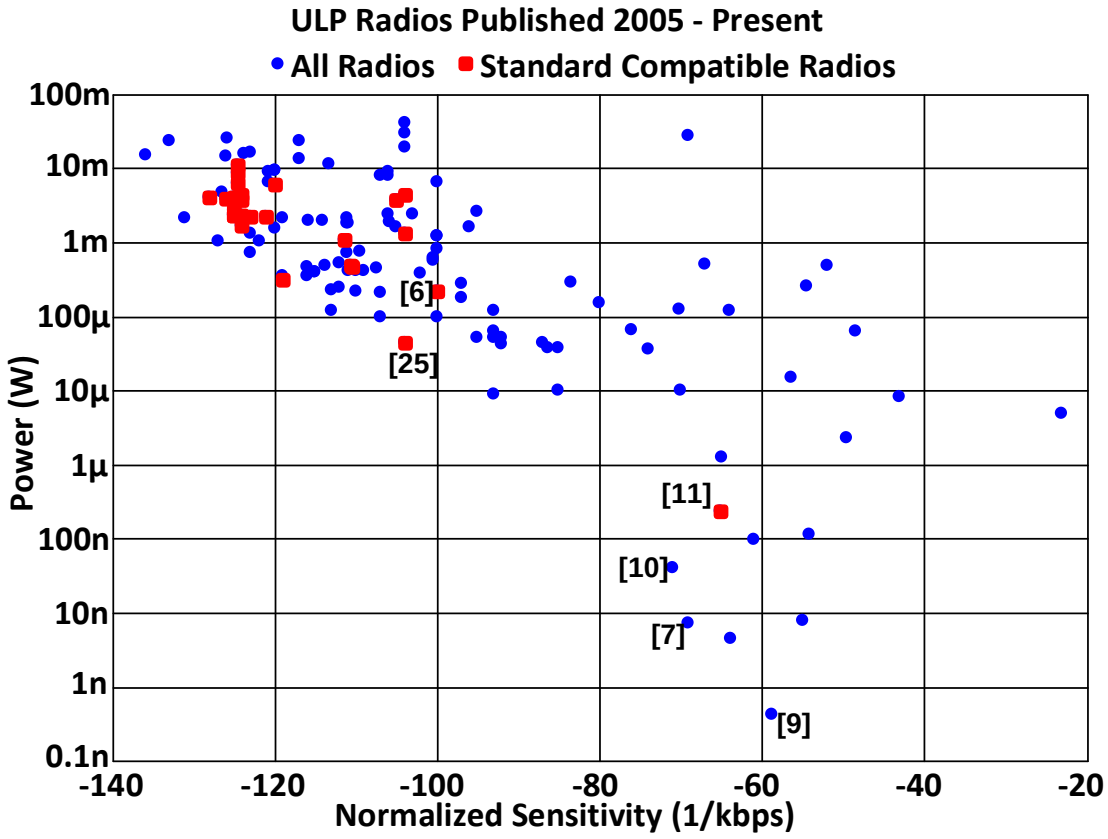


Fig.1.7 Ultra-low power radio survey: normalized sensitivity vs. power.

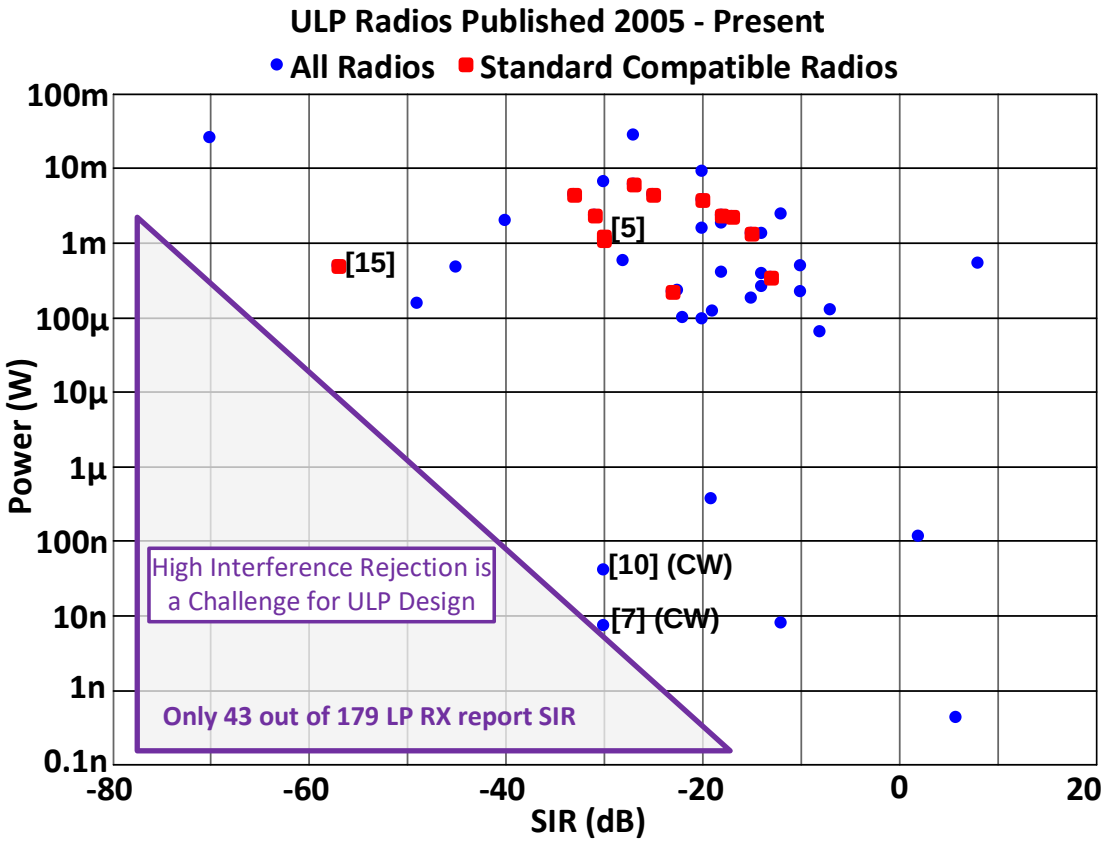


Fig.1.8 Ultra-low power radio survey: SIR vs. power.

locked loops (PLLs) with accurate crystal frequency references.

The signal to interference rejection (SIR) performance of ULP receivers is shown in Fig.1.8. The trade-off can be clearly be observed where only a few standard compliant ULP radios report their selectivity performance, and they consume at least 100s of µWatts. This can be attributed to that active filtering requiring high power to synthesize a high Q filter response, which is done traditionally by cascading multiple active filter stages. On the other hand, off chip passive filtering is possible but will mean lower system integration and increased cost. For example in [25, 26], off-chip RF MEMS are used to enhance the selectivity performance of the radio. Network level solutions, such as hopping the frequency to avoid collisions, can boost the effective blocker rejection performance as will be discussed in section 3.

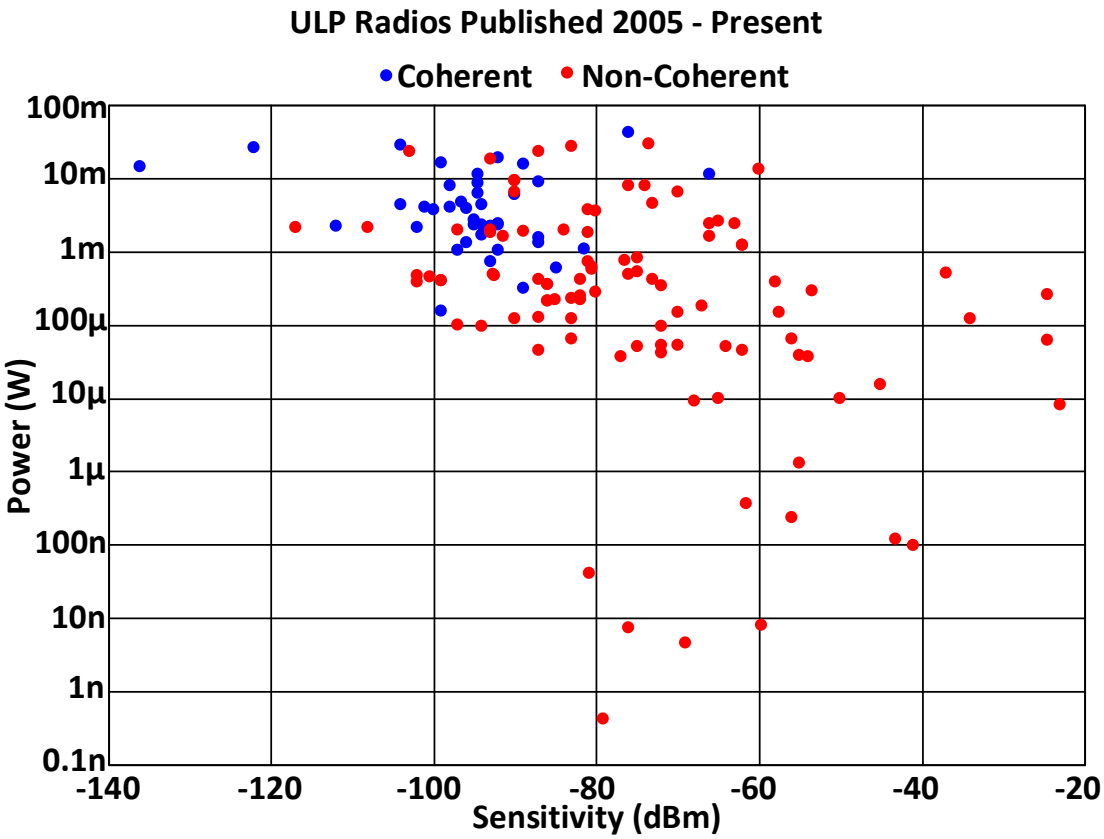


Fig.1.9 Ultra-low power radio survey: sensitivity vs. power for coherent and non-coherent modulation

The modulation scheme plays an important role in the specifications of the radio and hence its power consumption [9]. As seen in Fig.1.9, coherent commination requires significantly higher power to demodulate. This is because the carrier phase is needed for coherent detection which necessitates using a PLL in the receiver. In particular, Fig.1.10 shows that more than two-third of the published receivers use either on-off keying (OOK) or frequency shift keying (FSK) as their modulation scheme due their simpler detection requirements which help in keeping the power consumed lower. On the other hand, more complex modulations, such as: orthogonal frequency-division multiplexing (OFDM) and quadrature amplitude modulation (QAM), are only used in a few published receivers. Their reported power consumption is in the 100s of µWatt to few milliwatts which is in the upper power range of ULP radios as defined in this survey.

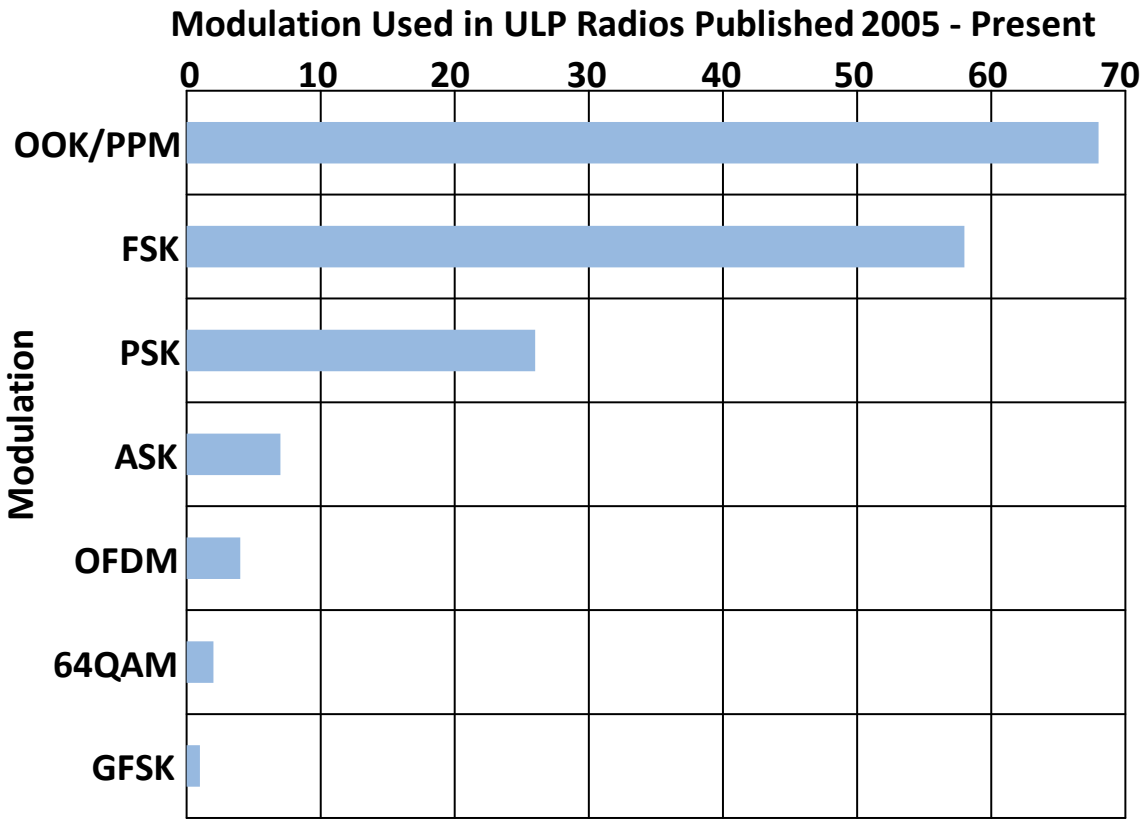


Fig.1.10 Ultra-low power radio survey: modulation used in ULP published radios.

The following design trends are observed in recent publications:

1.4.1 Nanowatt wake-up radios:

By utilizing an all passive RF front-end, the RX power can be reduced significantly to the nanowatt level. This is achieved using an RF envelope detector to convert the incoming signal to DC (Fig.1.11). However, an RF envelope detector has a large bandwidth which limits the sensitivity of such architecture to less than -60 dBm [18] due to the high noise bandwidth. The sensitivity can be further improved by ~ 20dB by using a high Q transformer at the front-end which provides passive gain and filtering [14, 17] (Fig.1.11). With this architecture, the integrated interference mitigation techniques used are mostly limited to continuous wave interferes (CW) which can be characterized as an additional DC offset for the comparator [25]. This assumption is

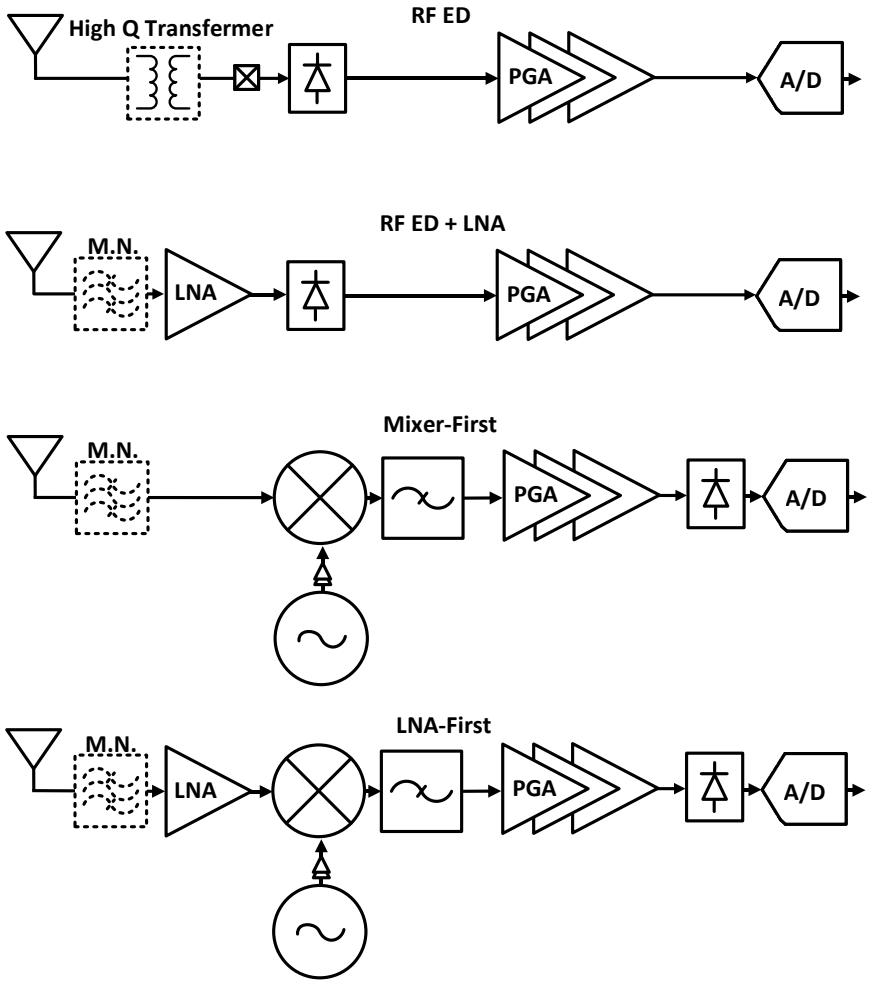


Fig.1.11 Low power radio architectures.

not valid for all wireless channels since they experience some level of signal fading which makes these techniques less effective in a real environment. Another limitation of this architecture is it does not support high frequencies due to the large shunt capacitance in RF detectors [27]. Fig.1.12 shows that all radios consuming less than 10 μW operate at a frequency lower than 3 GHz. Subthreshold analog and digital logic are common to achieve sub 1-μW power levels [11]. For very low data rates, a bit level duty cycled have been reported [25]. This allows for improved sensitivity levels with low average power using duty cycling.

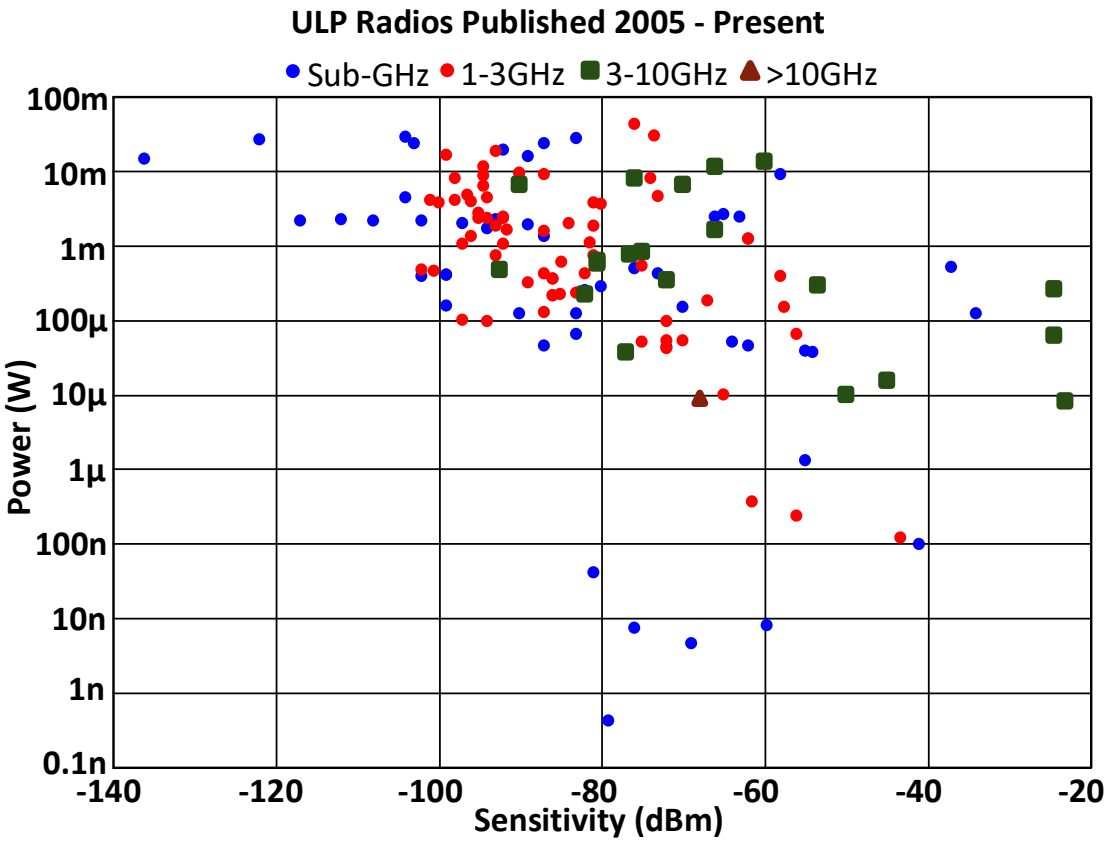


Fig.1.12 Ultra-low power radio survey: sensitivity vs. power for different RF operating frequencies.

1.4.2 Mixer-first radios for selectivity:

Another design trend to save power is to avoid using active RF gain (LNA) while using a mixer as a first stage instead [28–32] (Fig.1.11). Since the first RX stage dominates its noise performance, mixer-first radios suffer from higher noise figure (NF), when optimized for low power consumption, which degrades their sensitivity (range). Nevertheless, this architecture can still achieve decent selectivity levels with a sub-mW power budget [33]. In so-called mixer-first receivers, the dominant block in terms of power consumption is the local oscillator and its buffers. In order to reduce the LO power, the conventional LC oscillator can be replaced with a ring oscillator (RO) especially in more advanced CMOS nodes [34]. However, ROs have worse frequency stability making it harder to design the radio without a significant performance

degradation in its sensitivity and/or selectivity [12]. Alternatively, an LC oscillator can have its inductor off-chip to overcome the limited quality factor for on-chip inductors resulting in a significant power reduction by up to 75% compared with fully on-chip LC oscillators [20]. Although these off-chip inductors can be found in very small form factors, it is not a fully integrated solution, which might not suit some IoT applications.

1.4.3 LNA-first radios for long range:

Long range applications require sensitivity levels beyond -100dBm. To achieve this, a LNA-first topology is usually used. Similar to RF ED based wake-up radios; bit-level duty cycling was applied also in LNA first radios [35] to reduce the average power. In addition, lower supply voltages have been used to improve the power efficiency of LNAs [36]. In [37], a low voltage quadrature LNA was adopted in a current-reuse topology resulting in a power consumption of 600µW for the RF front-end, transimpedance amplifier and baseband filter.

1.4.4 Standard compatibility for widespread adoption:

Low-power radios consuming sub-µWatt of active power have been presented recently as in [38–41]. However, their deployment with current infrastructure is lagging because they lack the compatibility with existing communication standards. In addition, sub-µWatt radios typically suffer from worse interference rejection performance compared with their higher power standard compliant counterparts, leading to less reliable communication in real environments. Traditional standard compliant receivers consume higher active power, which makes them less appealing for IoT applications. Recent academic publications have attempted to tackle this power and performance tradeoff. For example, [42] presents a Bluetooth Low Energy (BLE) compatible radio, but lacks channel selectivity which is required in real world applications. An 802.11 g/n compatible wake-up receiver is presented in [19] but the adjacent channel interference (ACI)

rejection is only 20 dB for a wide channel bandwidth of 20MHz. On the other hand, [43] does achieve good inference rejection performance with SIR of -49 dB but utilizes a non-standard compatible spread spectrum technique, limiting adoption.

The BLE communication standard offers a low power answer when looking for ways to link IoT nodes with mobile devices. Nevertheless, and similar to other existing communication standards, the active power required to maintain a connection with a reasonable latency remains the limiting factor in defining the battery lifetime of event-driven BLE devices. Specifically, state-of-the-art BLE radio power consumption is still in the milliwatt range [10, 44–47] and can be duty-cycled for average powers around 30μW, but at the expense of long latency. A recent work [36] presents a 382μW BLE receiver by utilizing a 0.18V supply voltage. Although this is a remarkably low power consumption, it does only include the RF and analog front-end. Similarly, [48] reports a sub-0.6V, 330μW BLE receiver front-end. For both designs and to be used in a real system, the active power consumed in symbol detection, baseband processing and oscillator frequency calibration (i.e. using PLL or FLL) would need to be added to fairly assess the system power budget.

Given the clear power and performance trade-off discussed in this section, one of the challenges in ULP design is to still be able to communicate through an existing adopted standard. There are two design approaches to overcome the power and performance trade-off. The first relies on embedding a back-channel message in standard compliant BLE packets. The RX can detect the sequence in which BLE advertising channel are used and the timing gaps between them. This message is then demodulated to back-channel symbols. The second approach utilize the wake-up low power mode in existing standards such as the IEEE 802.11ba standard to relax the receiver specifications while still being able to receive messages from standard compliant Wi-Fi

transmitters.

1.5 Contributions

This work contributes to building more efficient wireless radios in terms of power, cost and area. Analysis, characterizations and measurement results are presented in this work as follows:

1.5.1 Analysis of Circuit Noise and Non-ideal Filtering Impact on Energy Detection Based Ultra-Low-Power Radios Performance

Circuit imperfections, especially in power hungry blocks, i.e. the local oscillators (LO) and band pass filters (BPFs), pose a real challenge for ultra-low power (ULP) radios designers considering their tight power budget. Chapter 2 presents an investigation on the effects of circuit non-idealities on the bit-error rate (BER) performance of On-off keying (OOK) and Gaussian Frequency-shift Keying (GFSK) energy-detection based wakeup radios. In particular, it analyzes the impact of phase noise and frequency offset in the LO, BPFs bandwidth and roll-off, noise figure (NF) on ULP receivers' performance. This contributes to the ongoing research in designing ULP wireless nodes by demonstrating the tradeoffs between these non-idealities and the receiver's sensitivity level and selectivity and show some design guidelines for energy detection (ED) based ULP radios.

1.5.2 Enhanced Interference Rejection Bluetooth Low-Energy Back-Channel Receiver With LO Frequency Hopping

Chapter 3 presents two prototypes of low power back-channel Bluetooth Low-Energy (BLE) wake-up receivers. The receivers scan the BLE advertising channels for modulated advertising channel patterns by hopping the local oscillator (LO) frequency. The back-channel

message is modulated in the sequence of the three advertising channels in each advertising event. This makes the wake-up via back-channel messaging compatible with the BLE standard, so it can be generated by a commercial off-the-shelf device. The first proposed receiver uses a dual-mixer to down-convert the RF input to reduce the ring based local oscillator (LO) power consumption by operating it at half the RF frequency. The second prototype aims to achieve faster channel hopping using a more stable and lower noise LC based oscillator. The receivers have -57.5/-82.2 dBm sensitivity while consuming 150 µW/1.2 mW.

1.5.3 Frequency Accuracy of Open-Loop LC Oscillators for Low Power Radios: Modeling and Measurements

In Chapter 4, an LC oscillator is modeled and fabricated in CMOS 40nm and its frequency accuracy is analyzed over process, supply voltage, and temperature (PVT) variations and over time. Performance is compared to the BLE specification as an example application commonly targeted by ultra-low power (ULP) radios. When the temperature coefficient (TC) of the coil loss is precisely modeled, the simulation results are close enough to the measurements for analysing the oscillator open-loop performance across voltage and temperature variations. The results show that frequency calibration for each chip is required to compensate for process and temperature variations in order to be able to run the oscillator open-loop and still comply with the BLE standard. When the temperature is stable, the frequency shift in the free running LC oscillator is measured to be less than ± 40ppm over a period of 16 hours, which meets the BLE specification.

1.5.4 A Crystal-Less BLE Transmitter with -86dBm Frequency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet

A crystal-less BLE transmitter and back-channel receiver with over-the-air clock recovery

is presented in Chapter 5. The transceiver calibrates its local oscillators from a received BLE packet, which is detected using the back-channel receiver, and meets the clock accuracy and interference rejection ratios specified in the BLE standard. The receiver has a -86dBm sensitivity and adjacent channel interference rejection of 18dB. The two PLLs lock in less than a combined 100µs using the 8MHz recovered reference. The crystal-less transmitter with clock recovery meets all BLE requirements for SIR, making this a reliable solution for removing the crystal oscillator even in densely populated networks. This work is the first reported symmetric crystal-less transceiver, where both the received and transmitted messages are compliant with the same communication standard (BLE).

Chapter 2. Analysis of Circuit Noise and Non-ideal Filtering Impact on Energy Detection Based Ultra-Low-Power Radios Performance

2.1 Introduction

Enabling ubiquitous receivers for IoT applications requires additional effort at both the system architecture and circuit design levels. The main challenge is to minimize the power consumption while still having an adequate sensitivity level in frequency congested spectrum, and using highly integrated solutions [8]. One increasingly popular approach to reduce the receiver's power consumption is to use a mixer-first architecture. This is because RF low noise amplifiers (LNAs) power consumption is usually in the milliwatt range and hence they are avoided in ULP radios to save power [49]. As a result, the receiver power becomes dominated by the local oscillator (LO) [50]. Integrated solutions for interference rejection can also take a significant proportion of the receiver power, especially in the case of narrower channel bandwidths [10, 51].

In practice, each of the receiver blocks show some degree of non-ideality. Optimizing the design of these blocks for closer to ideal performance can come at the expense of a higher power consumption, which represents a challenge for ULP receivers design. However, since certain blocks make up a higher proportion of the total power, this analysis is focused on exploring the design trade-offs for these blocks to facilitate the design of power efficient receivers for energy stringent applications.

In this chapter, we analyze these circuits' imperfections for two types of modulation schemes: On-Off-Keying (OOK) and Frequency-shift-keying (FSK). These are selected because they are the most commonly used in ULP receivers [24]. OOK can be very attractive when designing ULP radios due its simplicity. Also, FSK/GFSK are widely used nowadays in many

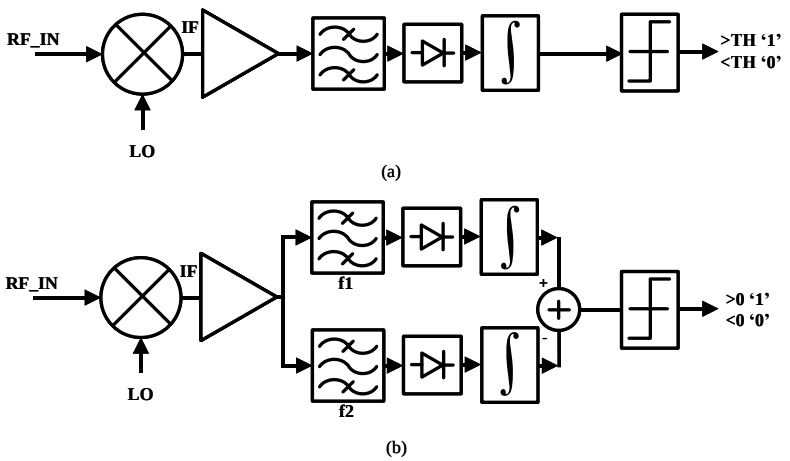


Fig.2.1 Block Diagram of ED based mixer-first receiver for (a) OOK and (b) FSK

existing communication standards. Simplified block diagrams for mixer-first energy detection (ED) based OOK and FSK radios used for this analysis are shown in Fig.2.1.

The rest of the chapter is organized as follows: section 2 starts with a brief description about the non-idealities which will be analyzed in this chapter. Section 3 presents the receiver model including the different sources of non-idealities. The implications of these imperfections are analyzed in section 4. Finally, the conclusion is drawn in section 5.

2.2 Background

This analysis addresses some non-idealities in the main power hungry blocks in ULP receivers. In this section, the sources of these non-idealities within the scope of this chapter are presented.

2.2.1 Band-pass Filters

The frequency spectrum which ULP radios operate in is shared with other transmitting devices, and hence, interference can degrade the receiver performance. On-chip higher order filtering of adjacent-channel signals can be very expensive in terms of power since it usually requires more stages, and higher-Q filters. This analysis aims to explore the implications of the

filter bandwidth and order on the bit-error-rate (BER) performance and blocker rejection ratio of the receiver. The term "filter bandwidth" is defined as the 3-dB bandwidth throughout this analysis.

2.2.2 LO

LC oscillators are used widely in transceiver design since they enjoy better frequency stability and low phase noise when compared with ring oscillators [52]. However, unlike ring oscillators, their power consumption doesn't scale with more advanced technology [53]. This led to more interest in using ring oscillators in ULP radio design to take advantage of technology scaling to minimize the power consumption. On the other hand, ring oscillators still suffer from lower frequency stability and higher phase noise which pose a challenge in lowering the power consumption. Since there is a clear trade-off between the oscillator power consumption and its phase noise [54], the impact of phase noise and LO frequency offset on energy detection receivers is analyzed in this chapter to help minimizing the oscillator power consumption while still meeting the target specifications.

2.2.3 Analog blocks along signal path

Since RF LNAs are usually avoided to achieve sub mW receivers, more attention has to be paid to the receiver noise figure (NF). The overall NF in mixer-first receivers is dominated by the mixer and the first intermediate-frequency (IF) stage given large enough gain is provided to the input signal. Low noise RF mixers, as the receiver's first stage, have been proposed in the literature [55]. However, they require more RF buffers to drive the multi-phase LO outputs which are part of the mixer design to reduce the NF, thus increasing power. This shows another clear trade-off between the power consumption and improving the gain/NF performance of the receiver. In section IV, the required E_b/N_0 constant BER is demonstrated under multiple other circuit

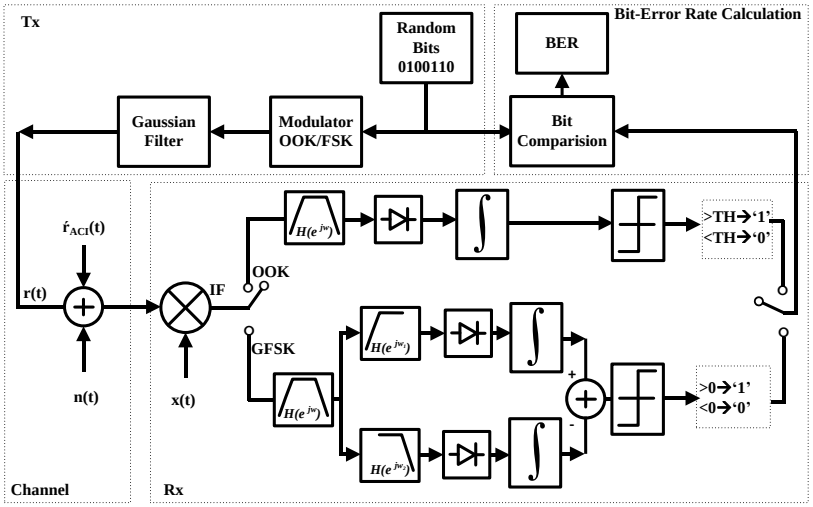


Fig.2.2 Block Diagram of the System Model used in this analysis for (a) OOK and (b) GFSK

imperfections. This can provide a guidance to estimate the required NF for certain sensitivity target.

2.3 Receiver Modeling

Fig.2.2 shows the model of an energy detection based ULP wakeup radio used in this analysis. First, the input RF signal is down converted to baseband frequency assuming ideal mixing with noisy oscillator. Then, the signal is amplified using ideal amplifier model. The signal is then filtered by non-ideal BPF. After that and using ideal blocks, the signal is rectified before integrating the energy over the symbol period. Finally, a 1-bit comparator is used to digitize the signal. The discrete time simulation is done in MATLAB with an oversampling ratio of 250. Blocks with imperfections that are not discussed in this chapter are simulated with ideal models and are not within the scope of this chapter.

The oscillator phase noise is modeled by shaping the noise in the frequency domain before converting the oversampled signal into the time domain. The phase noise shaping relative to the carrier is similar to what is shown in [56]. Phase noise values ranging from -80 dBc/Hz to -110 dBc/Hz at 1MHz offset are simulated. This range is representative of the phase noise change that

could be achieved by moving from a ring oscillator to an LC oscillator. An LO frequency offset implies a shift in its center frequency from the one desired.

The oversampled signal is then filtered by a Butterworth digital filter which is used to simulate the analog filter in ULP radios. Different practical filter bandwidths and orders are simulated to get better insight into how bandwidth trades off with ED ULP radios performance. Filters of orders: 1, 2 and 3 are simulated since higher orders would be a challenge to design in highly integrated ULP wake-up radios.

Additive white Gaussian noise (AWGN) is added to simulate the added noise by both the channel and the receiver blocks along the signal path. Theoretical optimum receivers for OOK and non-coherent FSK are already presented in the literature [57]. Since the goal of this analysis is to simulate a suboptimum energy detection based receivers including circuits' imperfections, a degradation in E_b/N_0 is expected for a certain target BER.

The received signal $r(t)$ is expressed as:

$$r(t) = Ae^{j(\omega_c+\omega_i)t} \tag{1}$$

where A is the signal peak amplitude, ω_c is the carrier frequency, ω_i represents the frequency modulation in the case of GFSK. The adjacent channel interference $\acute{r}_{ACI}$ has a similar form, but with a different amplitude and carrier frequency. The additive noise $n(t)$ has a normal distribution which can be expressed as $\mathcal{N}(0, \sigma^2)$.

The LO signal $x(t)$ can be expressed as:

$$x(t) = e^{j(\omega_0+\varepsilon)t+\varphi(t)} \tag{2}$$

where ω_0 is the oscillating signal frequency, ε is the frequency offset and $\varphi(t)$ which is a random variable representing the LO phase noise.

2.4 Analysis of Receiver Sensitivity and Selectivity

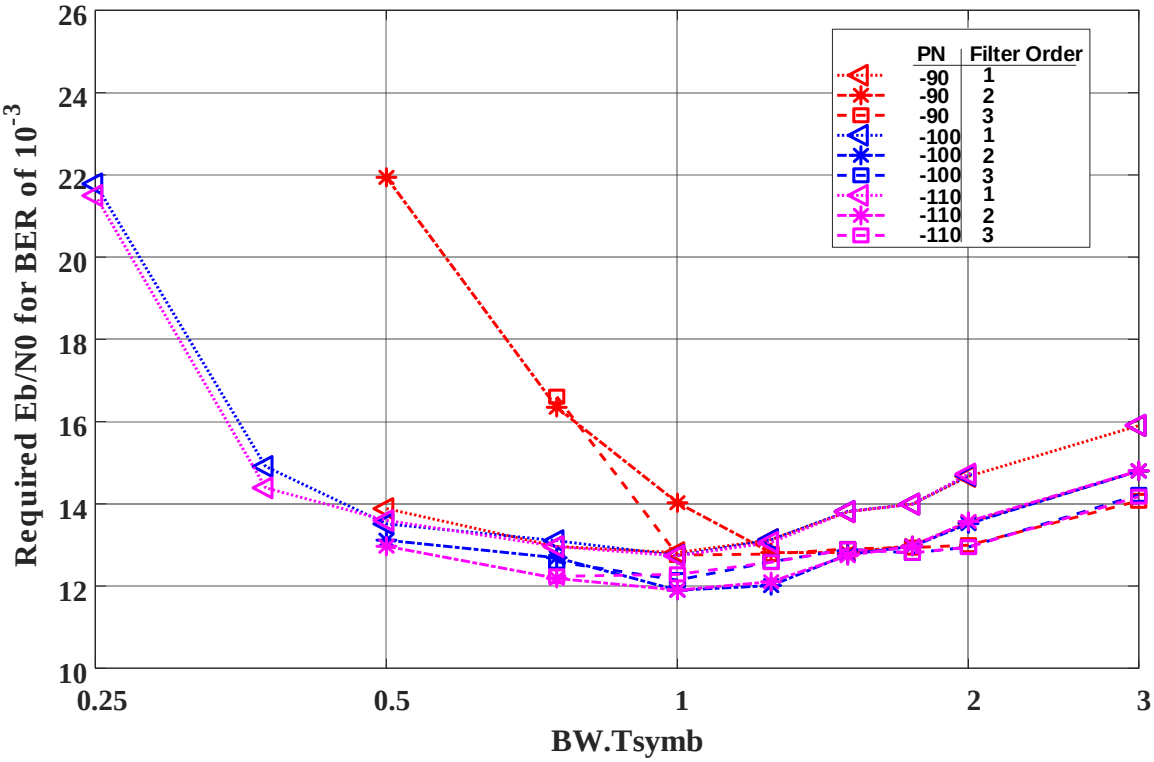


Fig.2.3 BT_{symb} impact on OOK performance for different Phase Noise Levels at 1MHz offset (dBc/Hz) and Filter Orders

In this section, the impact of the circuits' imperfections on the receiver sensitivity is analyzed first. Then, the analysis of their impact on selectivity is discussed later in this section.

2.4.1 Sensitivity Analysis

2.4.1.1 Effect of Bandpass Filter Bandwidth and Order

The influence of the filter to signal bandwidths ratio BT_{symb} and the filter order is presented in this subsection. The required E_b/N_0 for constant BER of 10^{-3} is used to compare the receiver performance with different filter specifications. The simulation results are shown in Fig.2.3 and Fig.2.4 for OOK and GFSK respectively. The two figures can be divided into two main regions. First, with $BT_{symb} \ll 1$, part of desired signal energy is filtered which leads to a higher E_b/N_0 requirement to achieve constant BER performance. On the other hand, in the second

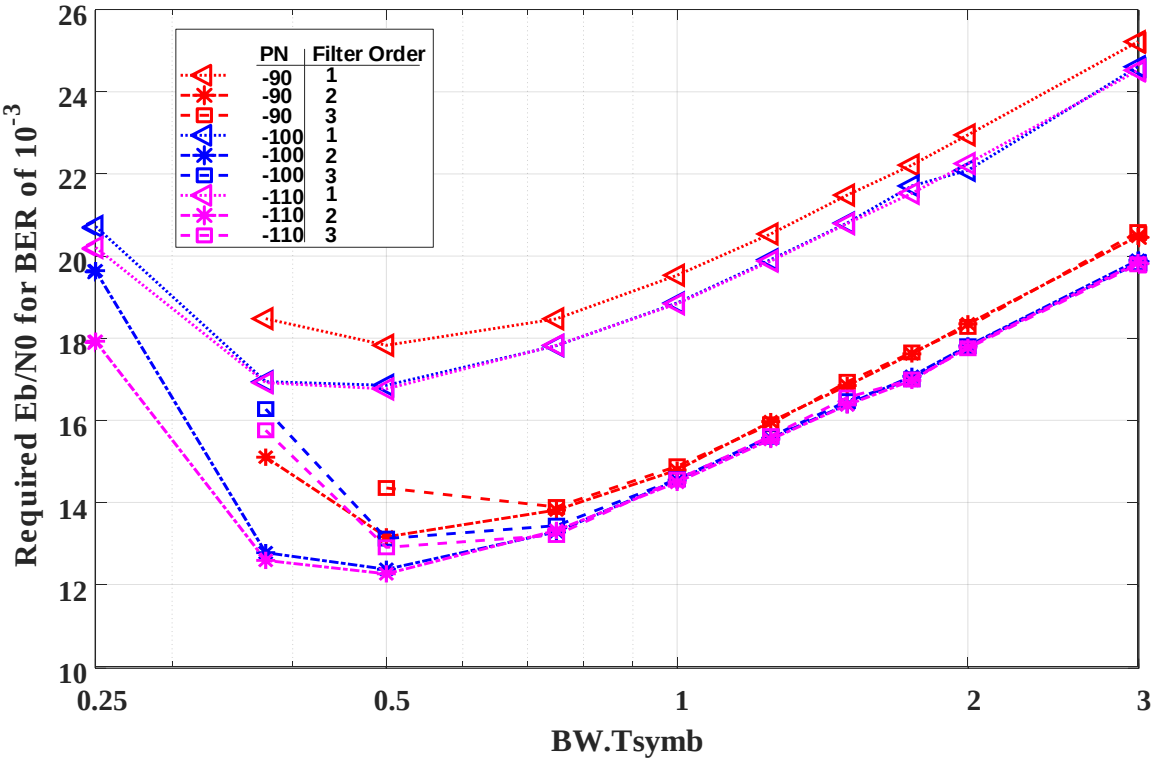


Fig.2.4 BT_{symb} impact on GFSK performance for different Phase Noise Levels at 1MHz offset (dBc/Hz) and Filter Orders

region, where $BT_{symb} \gg 1$, the in-band noise dominates and higher order filters achieve optimum BER performance. For GFSK, and as shown in Fig.2.4, relaxed filters can degrade the receiver sensitivity performance compared with higher order filters. This is a result of leaked energy increasing with relaxed filters from the frequency representing the other bit. In general, it can be concluded from these two figures that there exist an optimum BT_{symb} point which maximizes the receiver sensitivity for a given modulation specification. The optimum BT_{symb} point doesn't depend strongly on the phase noise level, but it sets the minimum E_b/N_0 for constant BER of 10^{-3}. The optimum BT_{symb} is 1 and 0.5 for OOK and GFSK, respectively. For the rest of this section, all simulations are based on the optimum BT_{symb} of for modulation scheme.

2.4.1.2 Effect of Oscillator Phase Noise and frequency offset

The impact of phase noise on the receiver performance can vary significantly based on

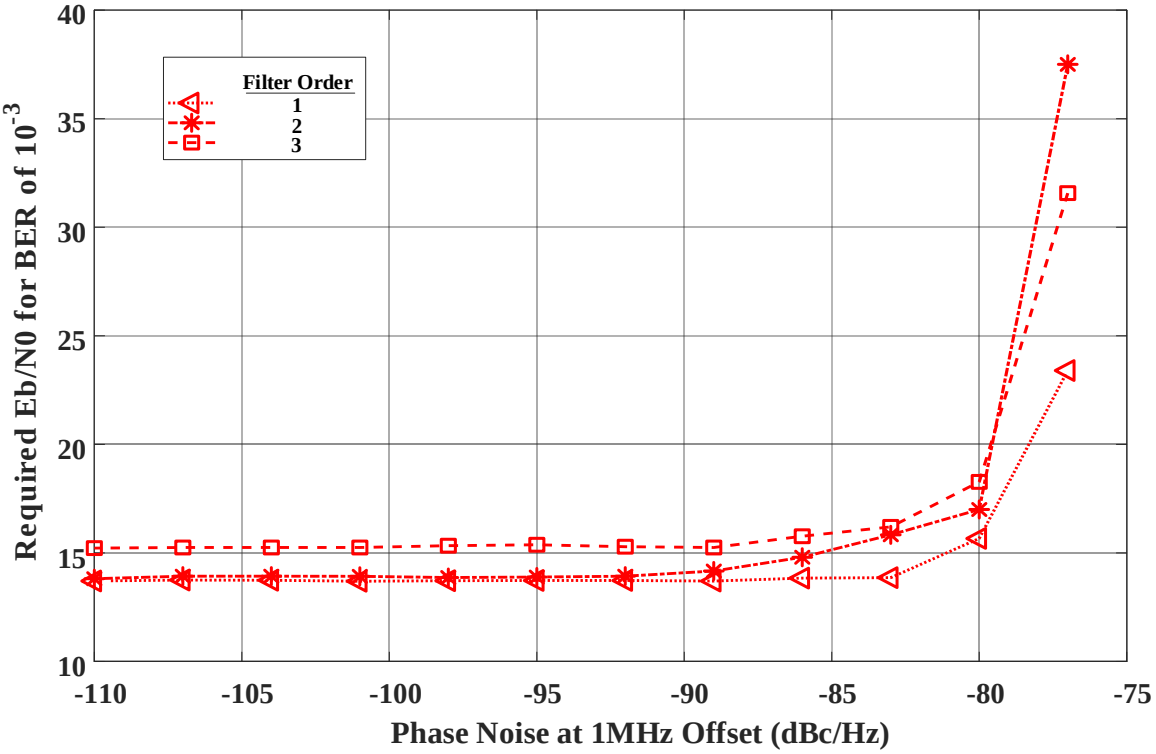


Fig.2.5 Impact of Phase noise on OOK performance for different Filter Orders

many factors: i.e. filter to signal bandwidth ratio, filter order, and modulation characteristics. Based on Fig.2.3 and Fig.2.4, it can be observed that as the filter bandwidth becomes higher than the signal's, the receiver sensitivity penalty because of phase noise becomes less significant. This is attributed to phase noise spreading the signal energy over a wider bandwidth which requires a higher filter bandwidth for the same BER performance. In order to quantify phase noise impact for different filter orders and modulation characteristics, the required E_b/N_0 for a BER of 10^{-3} is simulated for each parameter.

The performance of OOK receivers under phase noise is shown in Fig.2.5. Phase noise levels as high as -80 dBc/Hz at 1MHz offset can be tolerated without any major sacrifice with respect to the receiver sensitivity. This implies that the LO power can be significantly reduced by relaxing its phase noise while having the same receiver sensitivity.

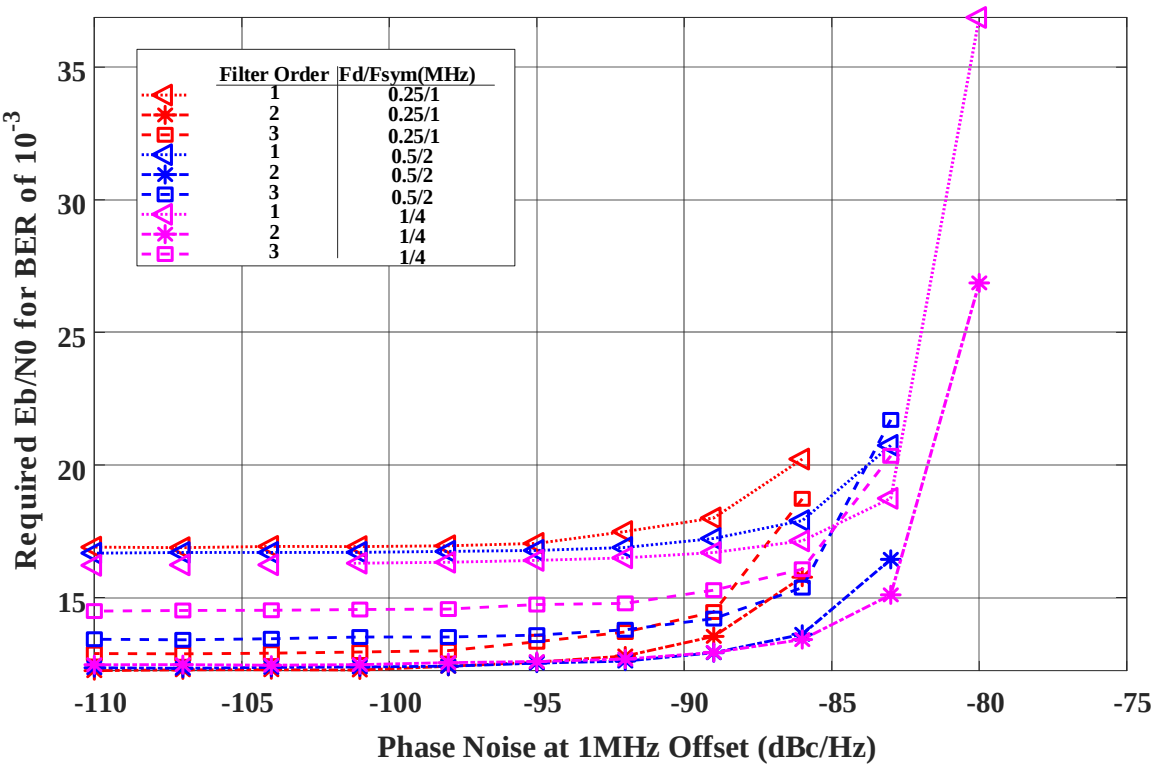


Fig.2.6 Impact of Phase noise on GFSK performance for different Filter Orders and Frequency Deviations with Modulation Index =0.5

Fig.2.6 shows the phase noise impact on a GFSK receiver assuming a modulation index of 0.5 as required in the Bluetooth Low Energy (BLE) specifications. Unlike in OOK, phase noise has a much stronger impact on BER performance. Fig.2.7 demonstrates that increasing the modulation index can significantly push the limits to phase noise levels higher than -80 dBc/Hz at 1MHz offset.

In that case, receivers using GFSK with relaxed low power ring oscillators and modulation index of 1 can be used since they tolerate a phase noise of – 77 dBc/Hz at 1MHz with less than 3 dB sensitivity penalty compared with higher power LC oscillators. The reason higher modulation index helps in relaxing the phase noise specification is that it corresponds to higher frequency deviation for GFSK, and hence can tolerate more signal spreading caused by LO phase noise. However, this means lower frequency spectral efficiency.

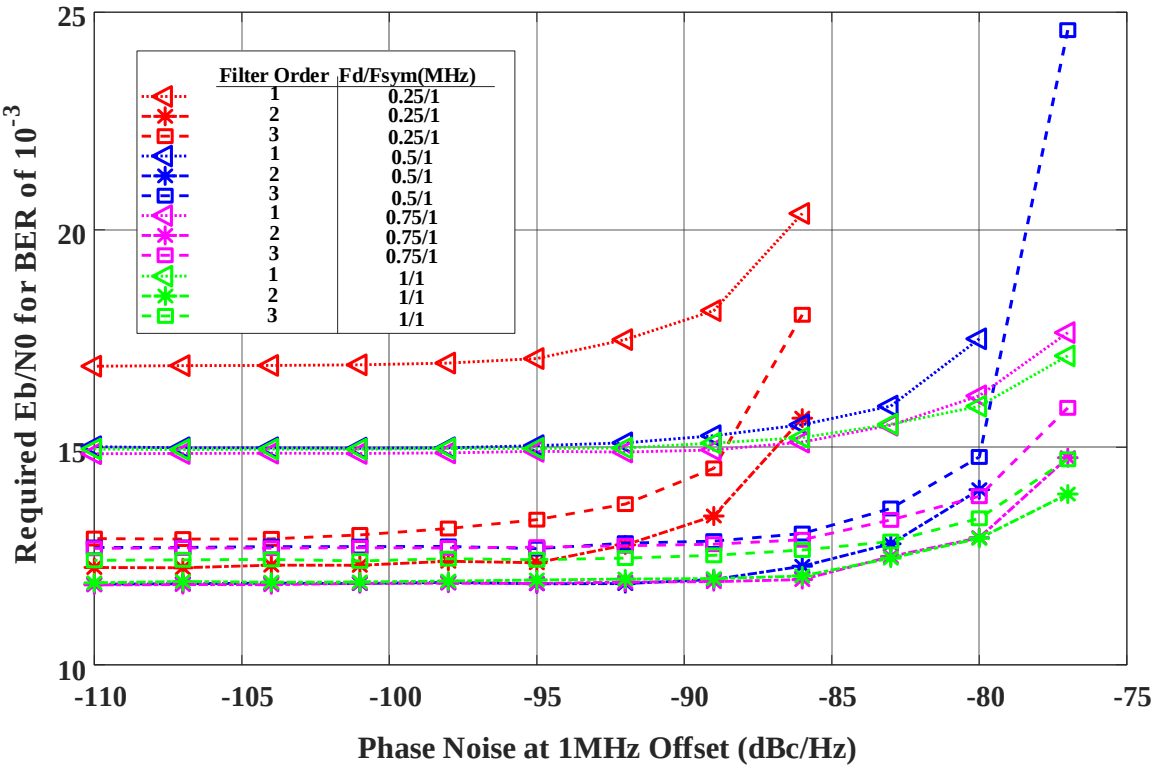


Fig.2.7 Impact of Phase noise on GFSK performance for different Filter Orders and Modulation Indexes

Besides LO frequency stability, which can be quantified by its phase noise, LO frequency accuracy will also affect the receiver sensitivity. Fig.2.8 shows the impact of LO offset in terms of the excessive required E_b/N_0 for constant BER of 10^{-3} for OOK. The performance degradation is a function of the frequency offset over filter bandwidth ratio. For GFSK, Fig.2.9 shows that LO offset impact depends on the frequency offset over frequency deviation ratio. In both modulation schemes, relaxed filters help tolerate more offset in the LO frequency. This can result in a major power reduction in the LO calibration power budget. When lower GFSK modulation indexes are used, i.e. $\ll 1$, the LO offset specification become much stricter, which is a similar conclusion to what was found with respect to phase noise. When phase noise is considered in addition to frequency offset, OOK outperforms GFSK as shown in Fig.2.8 and Fig.2.9. This higher sensitivity to LO imperfections in GFSK is a results of it relying on comparing the energy of two frequency

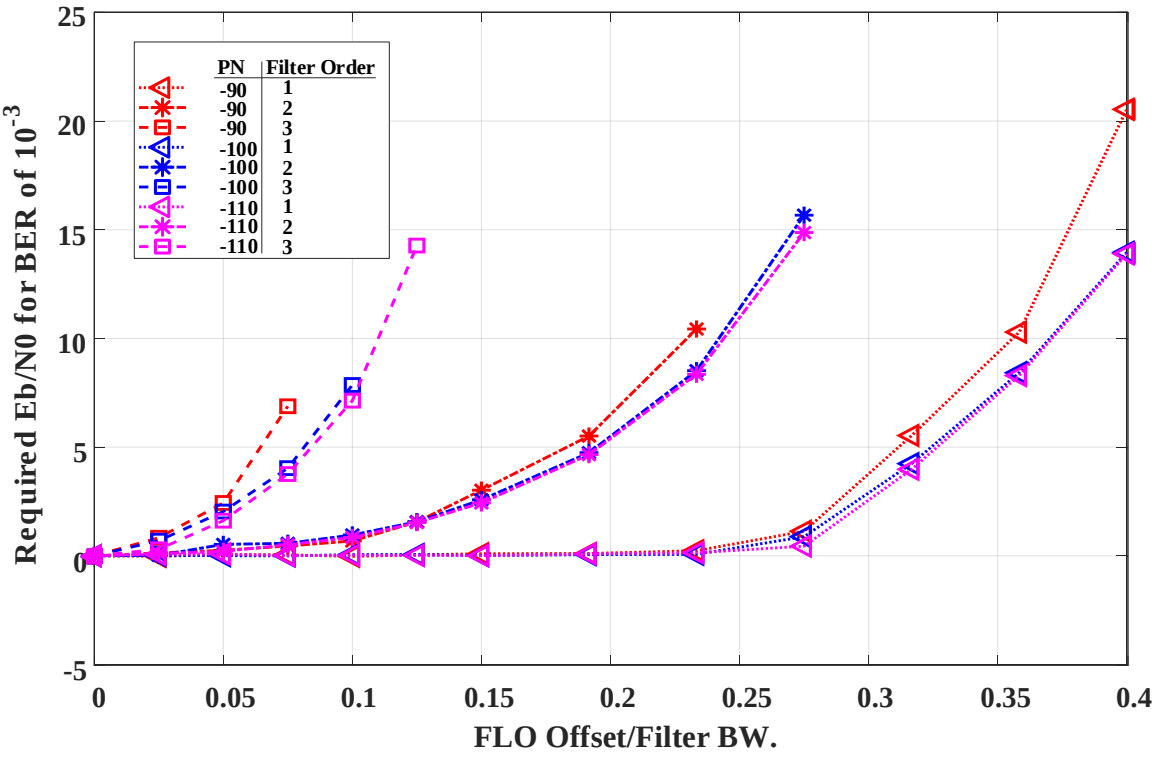


Fig.2.8 Impact of LO Offset on OOK performance for Phase noise Levels at 1MHz offset (dBc/Hz) and Filter Orders

bands that can shift with any change in LO frequency.

2.4.1.3 Effect of Noise Figure

The maximum receiver noise figure to achieve a certain target sensitivity can be calculated for a given BT_{symb} product, phase noise level, and filter order based on the required E_b/N_0 presented in this section. The maximum receiver NF_{max} is given by:

$$NF_{max}(dB) = S_n(dBm) - (-174(dBm)) - \frac{E_b}{N_0}\,(dB) + 10\log_{10}(T_{sym}) \qquad (3)$$

where S_n is the target sensitivity in dBm, and -174 dBm/Hz is the thermal power density at room temperature. Based on Eq.3, any improvement in the NF of the receiver will relax required E_b/N_0 for certain target receiver sensitivity.

2.4.2 Selectivity Analysis

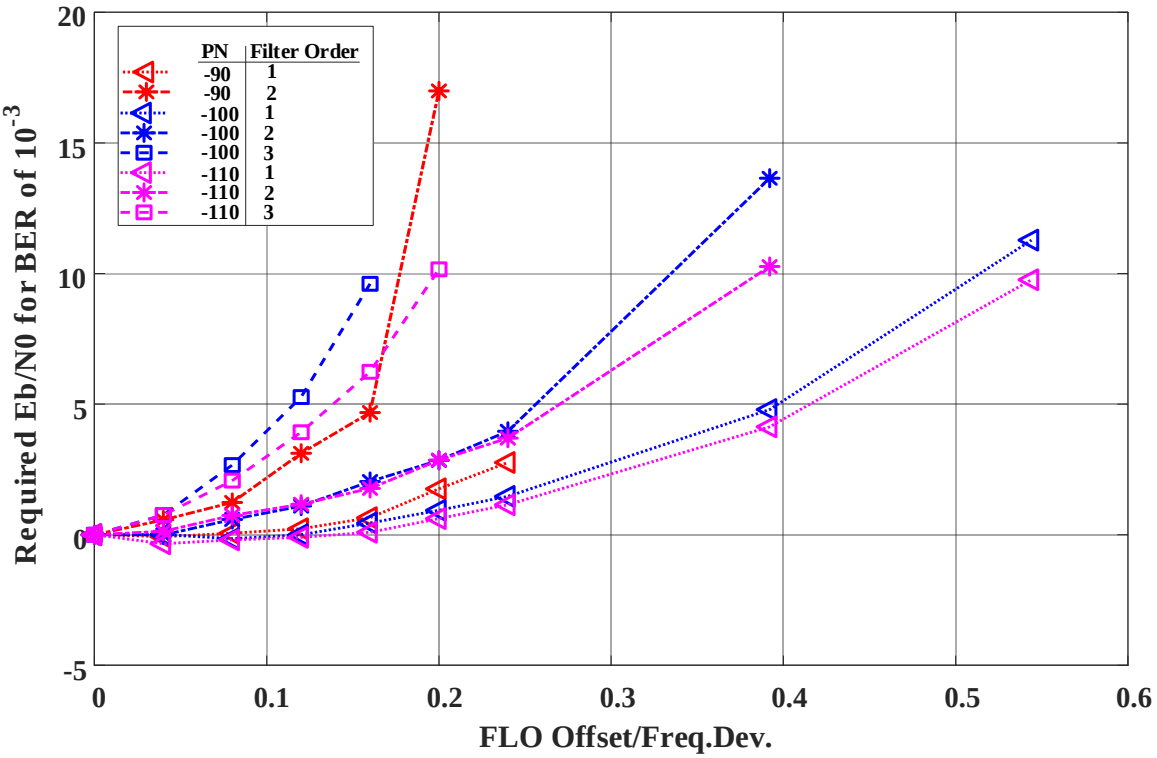


Fig.2.9 Impact of LO Offset on GFSK performance for Phase noise Levels at 1MHz offset (dBc/Hz) and Filter Orders

The second important measure of the receiver performance is the receiver selectivity. In this analysis, that is quantified by simulating the signal to interference ratio (SIR) at different blocker frequency offsets from the desired signal. The blocker has the BLE modulation characteristics. Fig.2.10 and Fig.2.11 show the SIR for OOK and GFSK respectively. These results imply that the filter order and the phase noise level have an impact on the blocker rejection performance of the receiver. When the Bluetooth-low-energy standard is used, the channel bandwidth is 2MHz and hence, both figures show the first five adjacent channels.

When comparing the SIR levels of GFSK receivers in Fig.2.11 with the interference performance in the BLE 5.0 standard also shown in Fig.2.11, only a higher order filter with low phase noise level can meet the blocker performance specified in the standard. With existing integrated CMOS solutions, this presents a challenge in the design of ULP receivers since such

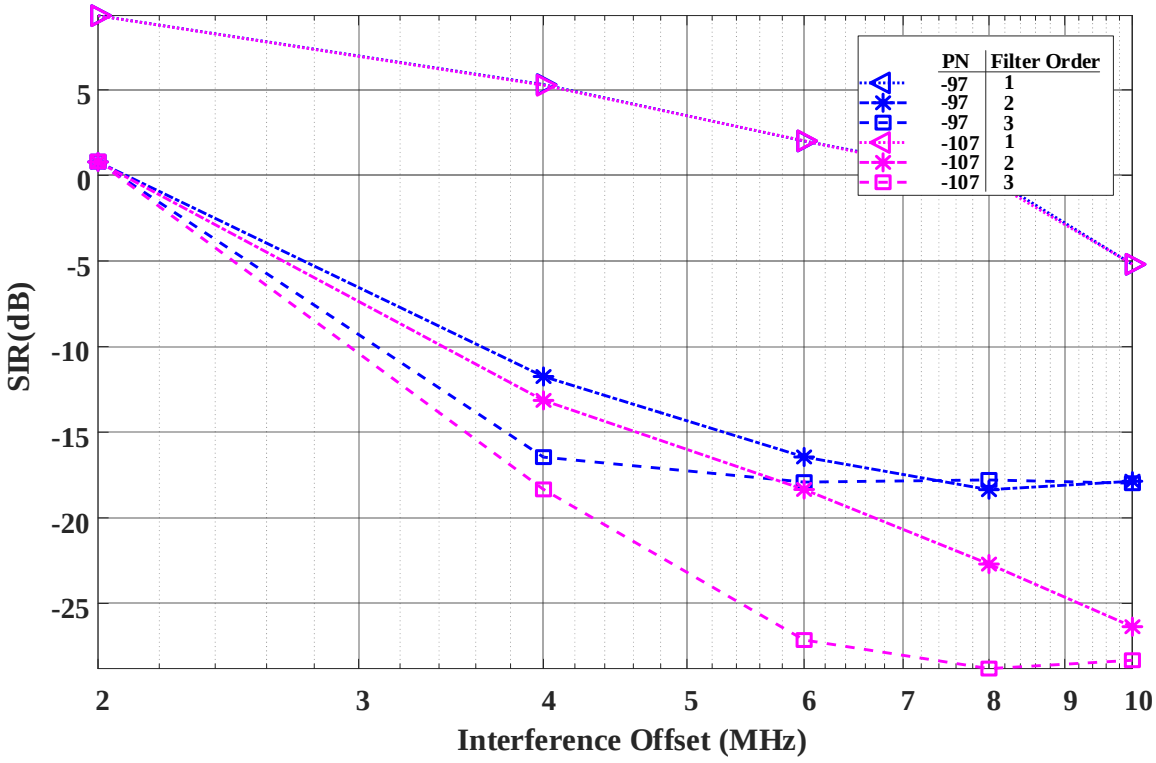


Fig.2.10 SIR for OOK receivers with different Phase noise Levels at 1MHz offset (dBc/Hz) and Filter Orders

solutions have a power consumption that starts in the order of hundreds of microwatt [58]. Moreover, when designing filters with sharper roll-off to improve the blocker rejection performance, other factors become more critical, such as LO offset. As a result, the overall power consumption can increase significantly. Although off-chip filtering could be used, it's not an attractive option when considering IoT applications where highly integrated solutions are essential.

2.5 Conclusion

In this chapter, an analysis of some critical circuit imperfections and their impact on ULP receivers is presented. First, for a given modulation specification there exists an optimum BT_{sym} that maximizes the receiver sensitivity. For instance, the optimum bandwidth for ED based OOK receivers is the same as its input signal data rate. Designing an LO with a phase noise better than a certain limit makes little to no impact on ED based receivers' sensitivity. The phase noise limit

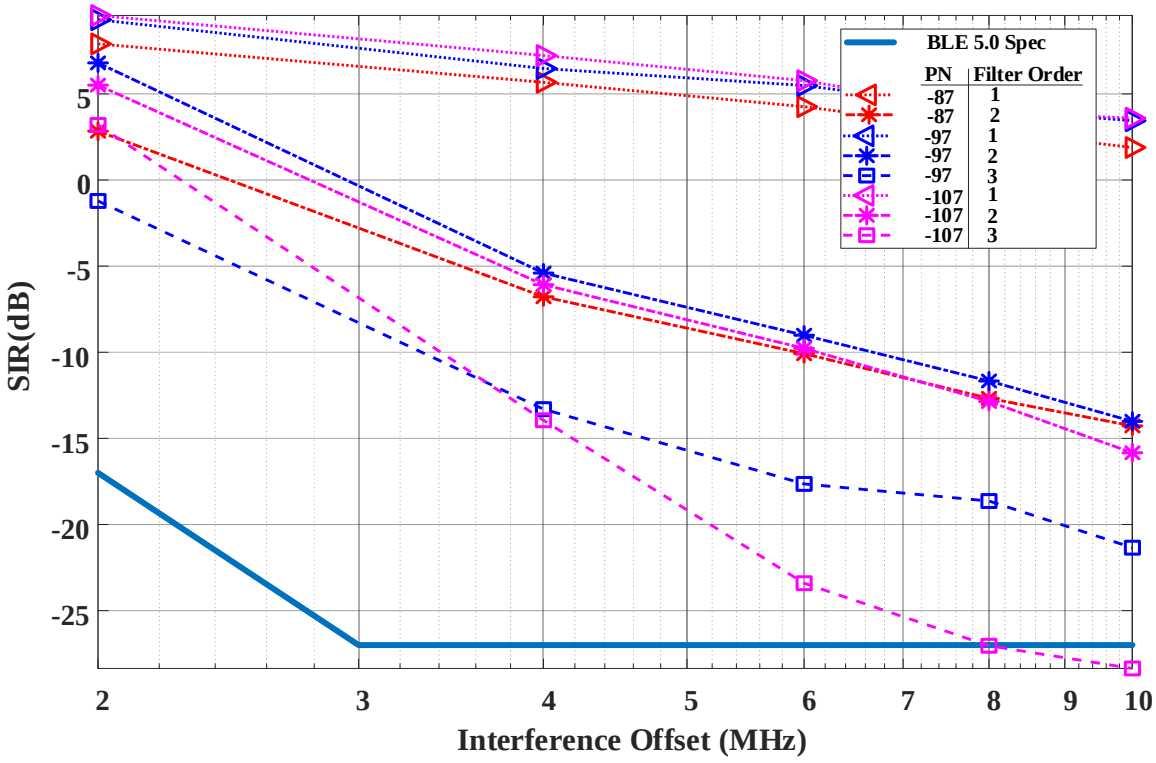


Fig.2.11 SIR for GFSK receivers with different Phase noise Levels at 1MHz offset (dBc/Hz) and Filter Orders

is a function of the modulation specification and filter order. For example, for GFSK, the LO phase noise can be relaxed to -85 dBc/Hz, which can be achieved using a low power ring oscillator, by increasing modulation index to 1 while maintaining the same sensitivity performance. Because of the trade-off between phase noise and power, this will result in substantial power savings.

For selectivity, when designing the filter roll-off, a trade-off exists between the receiver SIR performance and its power consumption. Also, this analysis showed that highly integrated ED based ULP radio architectures suffer from weak blocker rejection and still cannot meet popular wireless communication standards tailored for lowering the power consumption like Bluetooth-low-energy. To meet the demand of future radios designed for IoT applications, more innovation is needed in both system and circuit levels to overcome this challenge. In particular, new wake-up oriented wireless communication standards which can tolerate higher blocker power will bridge the gap between the existing ULP radios and communication standards. One option to achieve

such relaxed blocker performance would be to invert the current standard from repeatedly transmitting advertising packets, which lead to a more congested spectrum, to listening and checking for pre-define wake-up message.

To conclude, ED based ULP receivers, by using the appropriate modulation characteristics and the optimum filter bandwidth, can achieve high sensitivity in the presence of LO imperfections. However, they suffer from worse than typical interference performance specified in common wireless communication standards. The interference performance can be improved at the expense of higher power consumption.

Chapter 3. Enhanced Interference Rejection Bluetooth Low-Energy Back-Channel Receiver With LO Frequency Hopping

3.1 Introduction

ULP radios consuming nano-Watts have been presented recently as in [38]. However, they lack the compatibility with existing communication standards, which introduces a barrier to their deployment with current infrastructure. Nano-Watt radios typically also have poor signal-to-interference ratio (SIR). [42] presents a Bluetooth Low Energy (BLE) compatible radio, but with no channel selectivity. In [19], an 802.11 g/n compatible wake-up receiver is presented. However, the adjacent channel interference (ACI) rejection is only 20 dB for a wide channel bandwidth of 20 MHz. In contrast, [43] has an SIR of -49 dB but uses a non-standard compatible spread spectrum technique, limiting adoption.

The BLE standard provides a low power solution to connect IoT nodes with mobile devices, however, the power of maintaining a connection with a reasonable latency remains the limiting factor in defining the lifetime of event-driven BLE devices. BLE radio power consumption is in the milliwatt range [10, 44] and can be duty-cycled for average powers around 30μW, but at the expense of long latency. A recent work presents the concept of BLE back-channel (BC) communication as a wakeup mechanism that bridges the gap between ULP and standard compliant BLE radios [18]. This provides a low-power receive mode without compromising on latency but it is also susceptible to interference in the crowded 2.4 GHz band as it senses the signal without discriminating between sources using different BLE channels.

This work presents two designs of BLE back-channel receivers that include channel select filters to improve ACI rejection as shown in Fig.3.1. Both receivers are BLE compatible and can

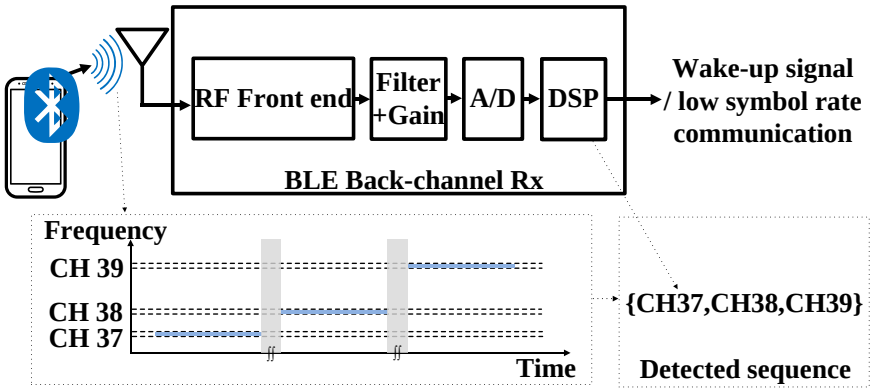


Fig.3.1 Basic block diagram of BLE back-channel receiver with one advertising event as input.

be used with off the shelf BLE transmitters. The first chip is a 150 µW ring oscillator (RO) based receiver with a dual-mixer front-end to save power by using an LO at half the RF frequency. The second chip is a 1.2 mW LC oscillator based receiver with a RF low-noise-amplifier (LNA) resulting in enhanced frequency stability of the oscillator and improved sensitivity. As a result, the second prototype can support faster frequency hopping. In both designs, channel selectivity is improved by 1) using direct-conversion with narrow baseband filtering (1 MHz) and by 2) defining each BC message based on the presence of packets in three channels instead of only one, which reduces the impact of blockers. Both BC receiver (BC RX) implementations use FSK communication by detecting the hopping sequence on the three BLE advertising channels, which can be specified in any sequence according to the BLE standard. Consequently, these receivers can wake-up from a BLE compatible message sent by a mobile device.

The ring oscillator (RO) based BC receiver was introduced first in [34]. In this chapter, a new LC oscillator based BC RX that can achieve faster hopping is demonstrated with fully integrated digital baseband. Additional details about the wake-up algorithm are presented in this chapter.

This chapter is organized as follows. Section 2 explains the concept of back-channel BLE communication. More details about the interference rejection performance are given in section 3.

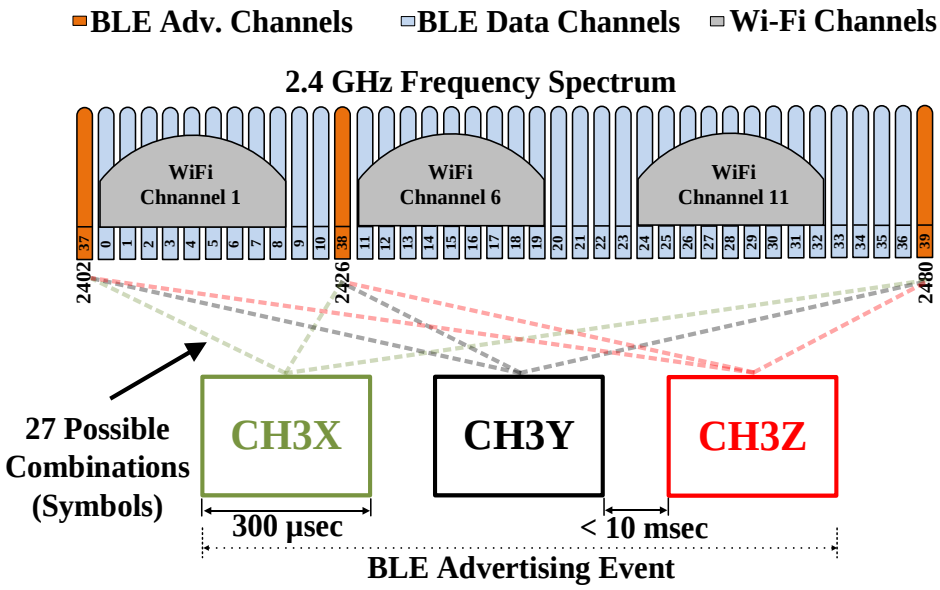


Fig.3.2 The structure of Single BLE Advertising Event

The receivers' architectures are presented in section 4. Sections 5 and 6 explain about the circuits' implementation for the ring based and LC based receivers, respectively. Section 7 presents the measurement results for both prototypes. Finally, the conclusion is drawn in section 8.

3.2 Back-channel BLE Communication

The structure of a BLE advertising event is shown in Fig.3.2. An advertising event consists of three packets separated by less than 10 msec. These packets are transmitted on any of the three BLE advertising channels: CH37, CH38 and CH39 located at the frequencies 2402, 2426 and 2480 MHz, respectively. Each packet length can be between 128 to 376 µsec (Fig.3.2 shows a 300 µsec packet for illustration). Based on the BLE standard, the delay between advertising events varies in the range from 20 msec to 10.24 sec in addition to up to 10 msec of pseudo-random delay to reduce the probability of collisions. With BC modulation, the information is encoded into the sequence order of the three transmitted advertising channels to represent one BC message in a single advertising event. This allows for a total of 27 possible channel combinations (messages) in one

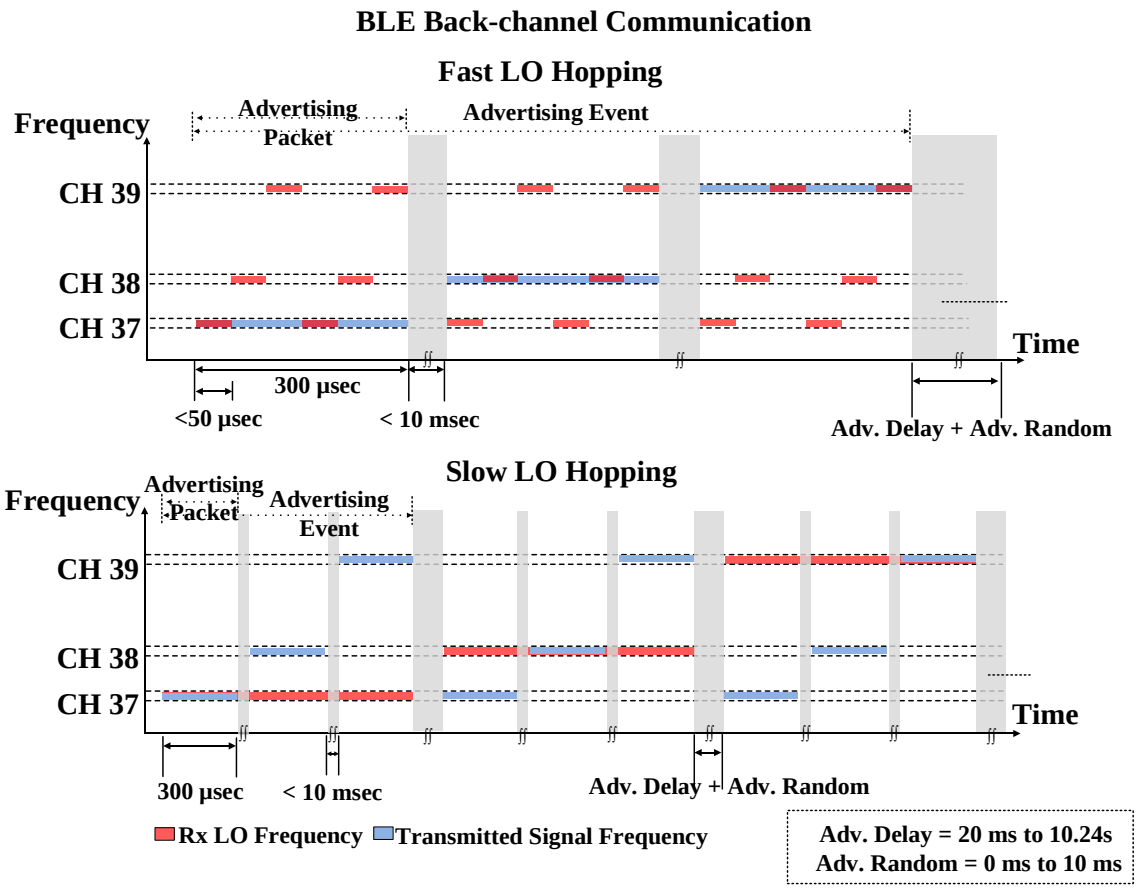


Fig.3.3 The concept of back-channel communication in fast and slow modes.

advertising events which last for one millisecond. Moreover, as an additional feature to this design, a pre-defined sequence of BC messages can be used as a wake-up message. The message is valid when the received message time-stamps are within the allowed time gaps defined by the BLE standard [34].

In back-channel BLE communication, the receiver is designed to detect the existence of packets in the three BLE advertising channels. This is implemented by detecting the energy in one advertising channel at a time. To achieve the targeted selectivity and improve the interference rejection, the receiver bandwidth is limited to 1 MHz, which allows filtering out adjacent BLE channels. To cover all three BLE advertising channels (78 MHz apart), the RX frequency controller hops the oscillator frequency between the three advertising channels' frequencies. Depending on

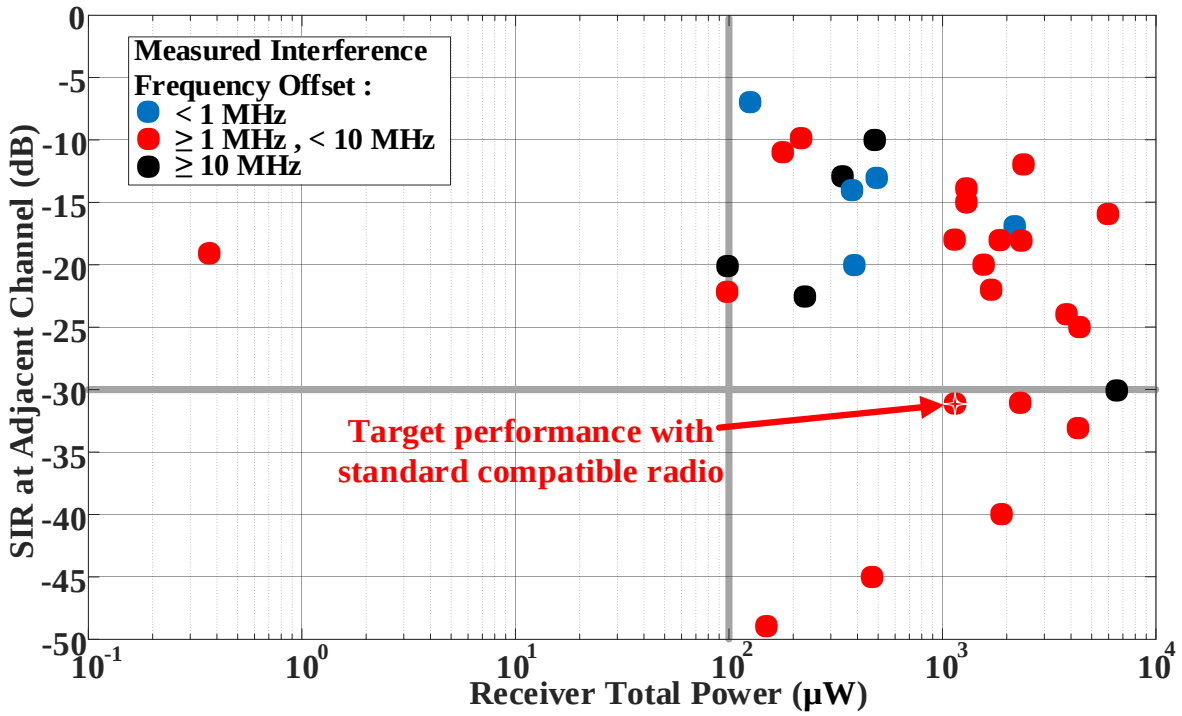


Fig.3.4 Survey of low power radios' SIR performance vs. RX total power consumption

the LO frequency hopping speed, the back-channel communication uses either a fast or slow mode as shown in Fig.3.3. In the fast mode, and since the receiver is detecting the energy of advertising channels successively, the LO hopping period between all three channels should be less than $T_{packet}/2$ to ensure capturing each packet's energy for a certain channel. On the other hand, in the slow mode, the hopping period should be at least $T_{event}/2$ to ensure capturing a complete advertising event comprising transmissions in all three channels. To achieve the fast hopping, and because the receiver has a narrow bandwidth to help its selectivity performance, the LO frequency has to be stable enough to detect the energy in a short time window. In our prototypes, An LC oscillator, which has around 20 dB improvement in phase noise at 1 MHz offset compared with the RO, was used to implement the fast hopping exploiting its superior frequency stability even when running open loop. On the other hand, a ring oscillator with a frequency-locked loop (FLL) was used to implement the slow hopping for the advantage of its lower power consumption.

3.3 Interference Rejection Performance

Fig.3.4 shows the interference rejection performance for the state of the art low power radios published recently [24]. The color of the marker represent the interference offset frequency at which the measurement was reported. The figure shows that most papers that report their ACI rejection performance are consuming more than 100 µW. In addition, most reported blocker rejection ratios are worse than 30 dB (SIR > -30dB). The source of this limitation is that on-chip higher order filtering of adjacent-channel signals can be very expensive in terms of power since it usually requires multiple active stages (i.e. op-amp or gm stages) to realize high -Q filters.

In this chapter, we propose exploiting frequency diversity gain from the multi-channel advertising events discussed in section 2 to improve the blocker rejection performance. Assuming fast LO hopping, and when any single advertising channel is jammed by a nearby strong interferer, the transmitted message can be estimated from the remaining two advertising channels. This is done by setting the required threshold for a valid BC message to be two-thirds of the maximum which allows estimating the received BC message from just two out of three channels. The proposed interference rejection solution is possible since the frequency gaps between the three channels are 24 MHz and 54 MHz, which are relatively large compared with the receiver's bandwidth of only 1 MHz. As a typical strong blocker such as WiFi only affects a single advertising channel, BC modulated messages achieve improved BLE/non-BLE blocker rejection performance using only relaxed low-power baseband filters.

3.4 Receivers Architecture

3.4.1 Ring based Receiver

Fig.3.5 shows the top level block diagram of the ring based BLE back-channel receiver. A mixer-first architecture is used with a ring oscillator to reduce the total power consumption. A dual

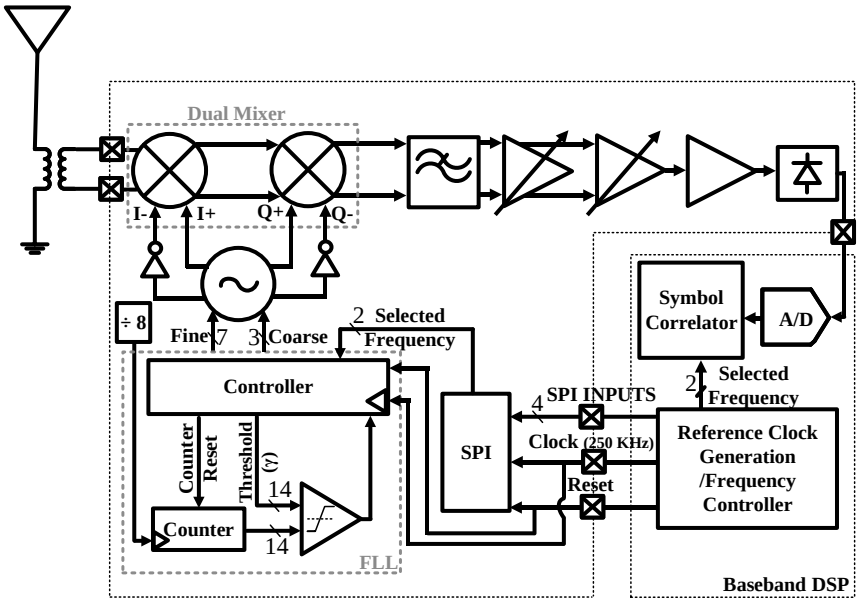


Fig.3.5 Block diagram of the RO based BLE back-channel receiver (prototype I).

mixer is used to set the LO at half of the input RF frequency, leading to significant power savings in the LO and its buffers (Fig.3.6). The direct down-converted baseband signal is then amplified and filtered to enhance the receiver selectivity. The signal is then envelope-detected before digitizing it. The FLL programming for a specific frequency hopping sequence is performed by the external baseband DSP through SPI (Fig.3.5). Off-chip, the receiver digitized output is correlated with pre-defined templates for each possible BC message by the external baseband DSP. Different BC messages can be defined based on the frequency hopping sequence of advertising events and their timing gaps. In addition, an off-chip balun is used to filter out-of-band blockers,

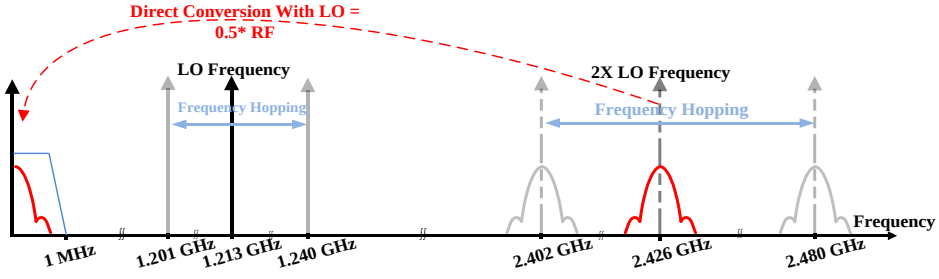


Fig.3.6 Frequency spectrum of RF signal down-conversion with dual mixer in prototype I.

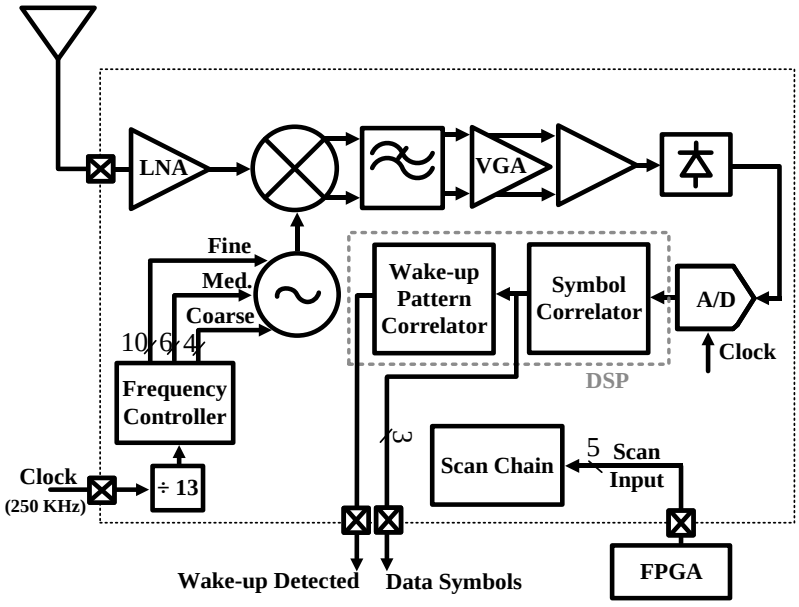


Fig.3.7 Block diagram of the LC oscillator based BLE back-channel receiver (prototype II).

especially at the LO fundamental frequency which is 1.2 GHz.

3.4.2 LC based Receiver

The top level block diagram of the LC based BLE back-channel receiver is shown in Fig.3.7. This architecture enables the fast frequency hopping by utilizing an RF LNA and an LC oscillator to reduce the noise and improve the frequency stability, respectively. The receiver selectivity is enhanced by limiting the baseband amplifiers bandwidth to 1 MHz. After detecting the signal envelope, a one-bit comparator is used to digitize the signal. The comparator digital output is correlated with pre-defined templates for each possible BC message by the on-chip DSP. These templates can be programmed thorough scan-chain. The frequency hopping for a specific frequency sequence is performed by an on-chip frequency controller programmed through the scan-chain.

3.5 Ring Based Receiver Circuits Design

3.5.1 RF Front-end

The RO based RF front-end schematic is shown in Fig.3.8. Similar to recent low power radios [28, 37, 53, 59], a mixer-first architecture was used to minimize the power. A ring type oscillator was selected to take advantage of the technology scaling for reducing power consumption [53]. The dual mixer has two passive stages in series driven from the same LO signal source. This effectively performs a two-step down-conversion of the RF signal. Since the mixers are passive switches to save power, the LO phases have to be different between the two stages to effectively down-convert the signal at twice the LO frequency.

I/Q LO phases are required to achieve the optimum conversion gain, but Fig.3.8 shows that some mismatch in phases is acceptable. The plot in Fig.3.8 also shows that LO phase difference could be up to -30° off from optimum with less than 2 dB signal loss compared with ideal IQ phases. Taking advantage of this trade-off to save power, this design replaces the more traditional, but higher power, differential I/Q ring oscillator with a single-ended ring oscillator having an odd number of stages. The single-ended ring doesn't produce I/Q outputs, but, with 5 stages, the losses from I/Q mismatch are only 1.1 dB of the signal. To characterize the impact of mismatch and process variation on the dual mixer conversion gain, a Monte Carlo simulation is run as shown in Fig.3.9. The result shows a standard deviation of about 0.5 dB only. The noise figure of the RF front-end is simulate to be 9 dB. The noise can be reduced by resizing the mixer transistors at the expense of higher power consumption in the LO buffers.

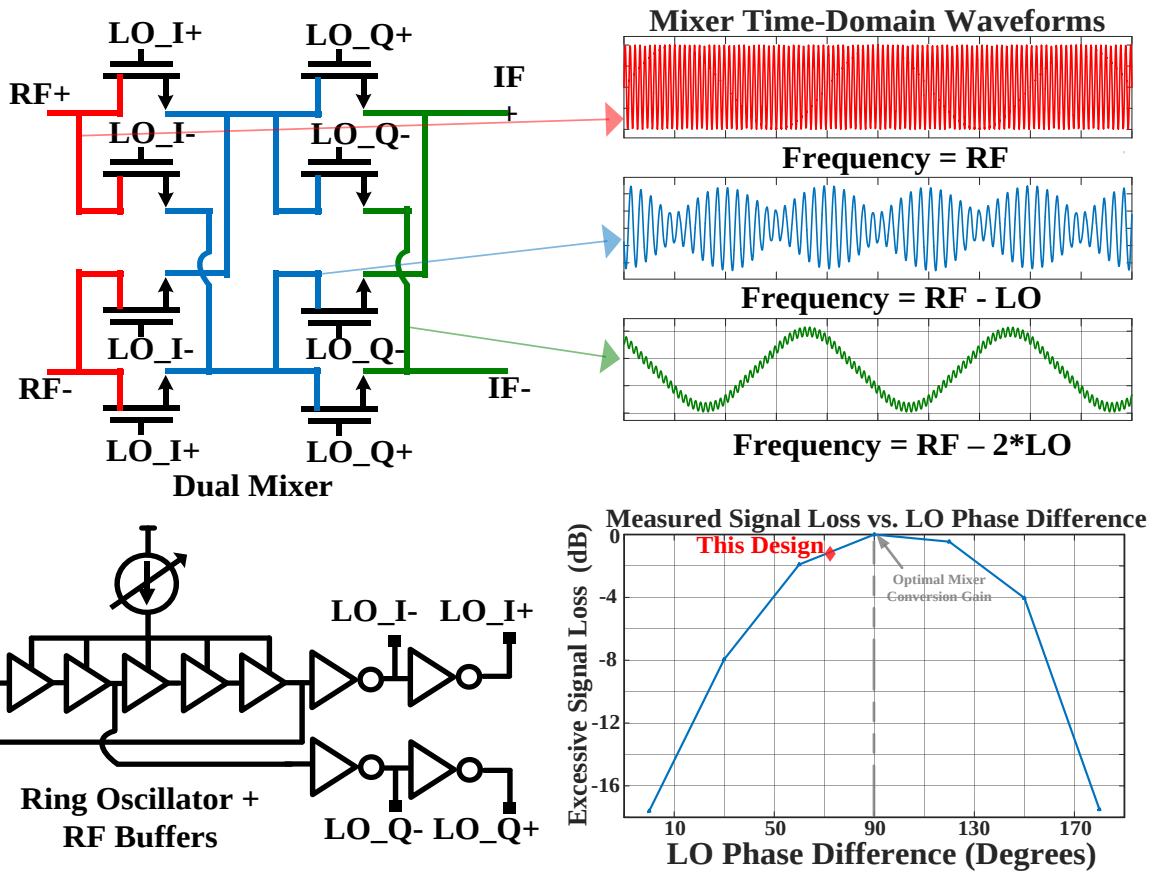


Fig.3.8 Prototype I RF front-end circuits: dual mixer and its input, intermediate and output time domain waveforms. Ring oscillator and RF buffers. Mixer excessive loss due to LO phase compared with ideal I/Q.

This design directly down-converts the RF signal at 2×LO frequency to baseband. A current DAC with coarse and fine tuning bits is used to calibrate the oscillator frequency over process, voltage, and temperature (PVT) variations. The tuning bits are also used to hop the oscillator frequency between the three advertising channels using an integrated FLL within 100 kHz resolution. The FLL is based on a counter for the number of the divided LO cycles in one reference clock period, and then comparing that to a target value based on the desired frequency and updating the LO current DAC control bits accordingly.

3.5.2 Analog Baseband

The directly down-converted signal is low-pass filtered at baseband. The filter is 3rd order

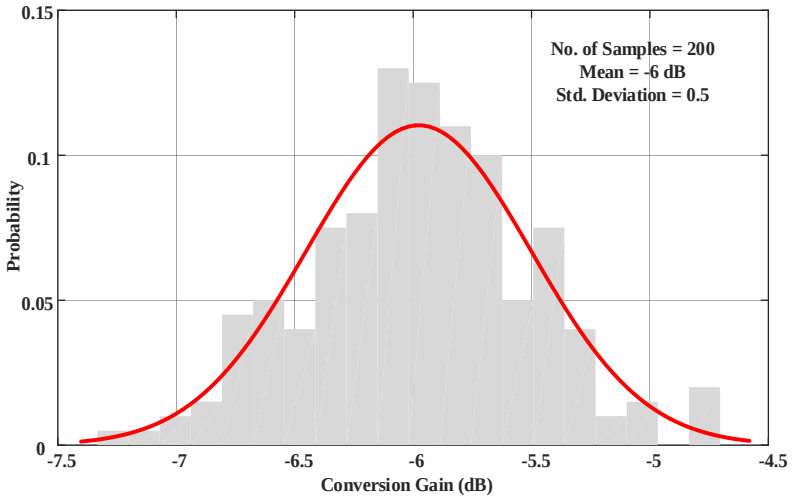


Fig.3.9 Monte Carlo simulation of the conversion gain of the dual mixer in prototype I.

with a bandwidth of 2 MHz at RF, which is the bandwidth of all BLE channels. This channel selectivity allows the receiver to tolerate, up to a certain extent, adjacent channel interference. Then, the baseband amplifiers provide up to 65 dB of signal gain. Each baseband amplifier input is AC couple to remove any DC offset due to the high gain. A source follower based envelope detector is then used to rectify the signal before digitizing it. As a result of using simple direct-conversion, the analog baseband is simulated to consume 30µW only.

3.5.3 Digital Baseband

The envelope detector output is processed off-chip where the signal is first digitized using a one bit comparator. The comparator output is then over-sampled by a factor of 10 to find the packet boundary while the LO frequency is hopping. The bit sequence is correlated with pre-defined templates representing different BC messages. A wake-up message can be embedded in a BC messages pattern as additional feature of this communication scheme.

3.6 LC Based Receiver Circuits Design

3.6.1 RF Front-end

The RF front-end schematic of the LC based receiver (prototype II) is shown in Fig.3.10. In order to minimize the receiver noise, a LNA first architecture is used. Passive switches are used to directly convert the LNA output to baseband. Direct-converting instead of having an intermediate frequency (IF) avoids having to deal with the image. The passive mixer has a simulated noise figure and conversion gain of 8 dB and -4 dB, respectively.

An LC oscillator was selected due to its superior frequency stability. Its schematic is shown in Fig.3.10 (b). A complementary cross-coupled pair featuring current reuse was used, resulting in low power consumption of 500 μW. A digitally-switched resistor is implemented as the tail current, since resistor has much lower flicker noise than a MOS transistor. Thus, low phase noise at low frequency region is achieved, which benefits frequency stability. The frequency of the LC oscillator is tuned through digitally-switched capacitor array. The overall frequency tuning range is 2300 to 2510 MHz with resolution of only 20 kHz which is achieved by using ~300aF unit capacitors for fine tuning. Such fine resolution not only ensures coverage of each BLE channel, but also enables this LC oscillator to be reutilized in a BLE-compliant transmitter.

The frequency variation across a temperature range of -20ºC to 60ºC degree is measured to be 150 ppm/ºC, which makes small temperature changes tolerable in the proposed wake-up receiver, since the baseband bandwidth is 1 MHz. On average, the shift in frequency is measured to be 20 ppm/mV. In addition, the maximum frequency shift is measured to be ±40 ppm from the average frequency over 16 hours. Therefore, the digital frequency control words for three BLE advertising channels are trimmed only once for the first time, when the chip is powered up, and kept constant during future operation.

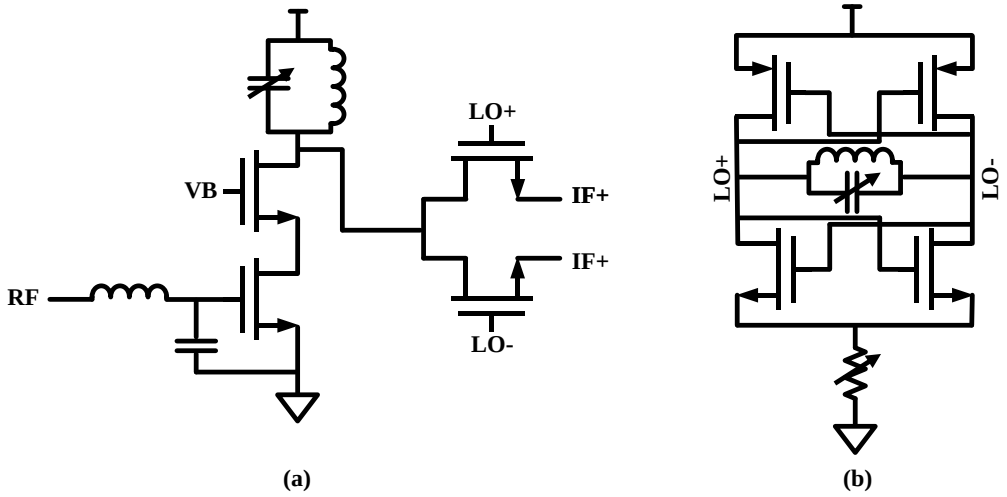


Fig.3.10 Prototype II RF front-end circuits: (a) LNA and passive mixer. (b) LC oscillator.

3.6.2 Analog Baseband

The baseband amplifiers provide up to 70 dB of gain distributed over three stages. These amplifiers low-pass filter the signal at baseband. The baseband filter is a 3rd order low-pass filter with a bandwidth is 1 MHz and corresponds to 2 MHz at RF because direct down-conversion is used. This narrow bandwidth along with the low phase noise of the LC oscillator improve the adjacent channel interference rejection. Each baseband amplifier input is AC couple to remove any DC offset as a results of the high gain. An envelope detector followed by an integrator, both shown in Fig.3.11(a,b), are then used to rectify and integrate the signal. The signal is digitized after a one bit comparator shown in Fig.3.11(c). The comparator sampling frequency is 250 kHz, which is more than 10 times faster than the oscillator hopping frequency. The narrow-band analog baseband circuits are simulated to consume 220 μW only as a results of using direct-conversion with the simpler low-pass as opposed to band-pass filtering.

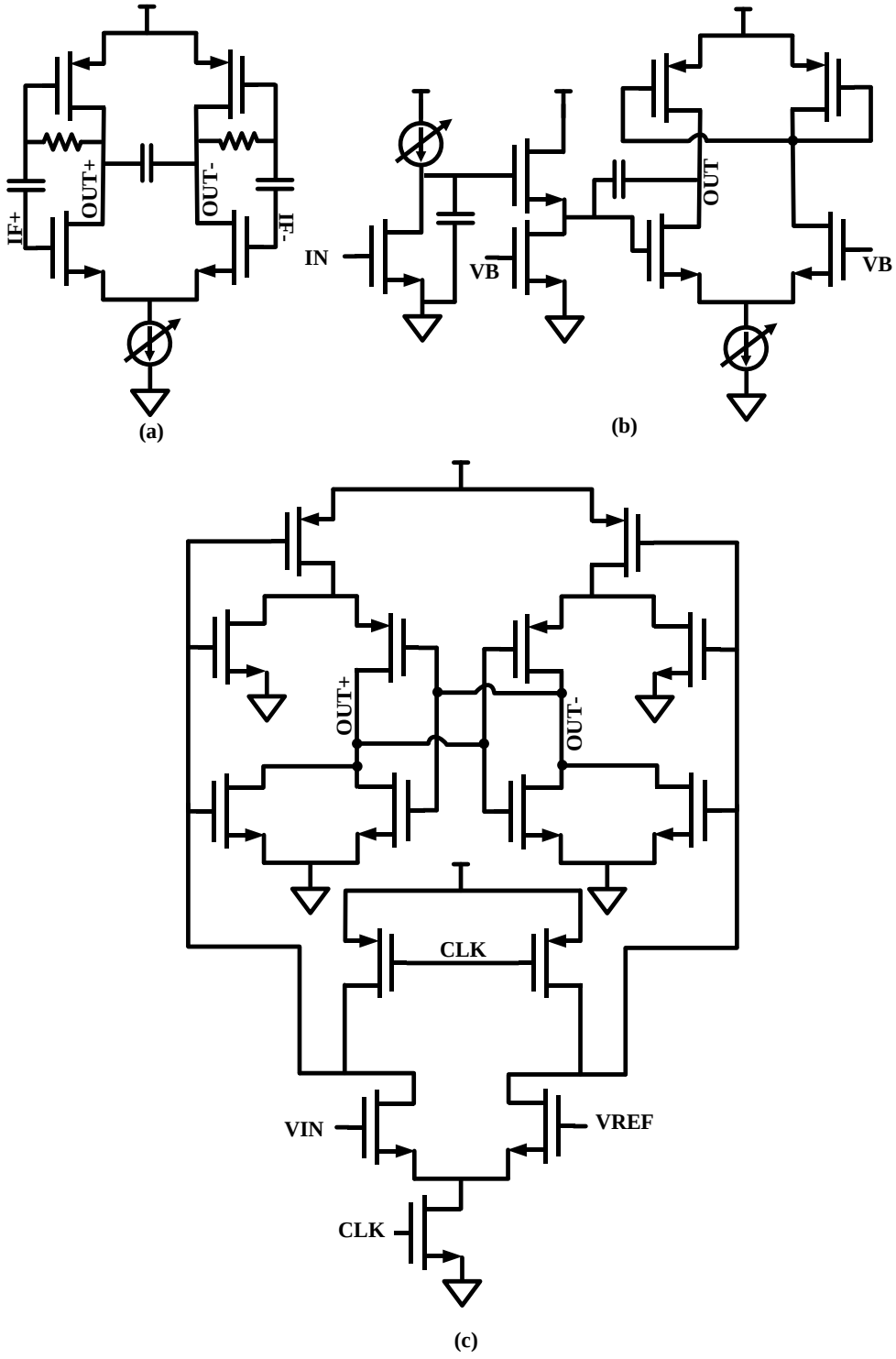


Fig.3.11 Prototype II baseband circuits: (a) first amplifier stage. (b) envelope-detector and integrator. (c) comparator. Bias circuits not shown

3.6.3 Digital Baseband

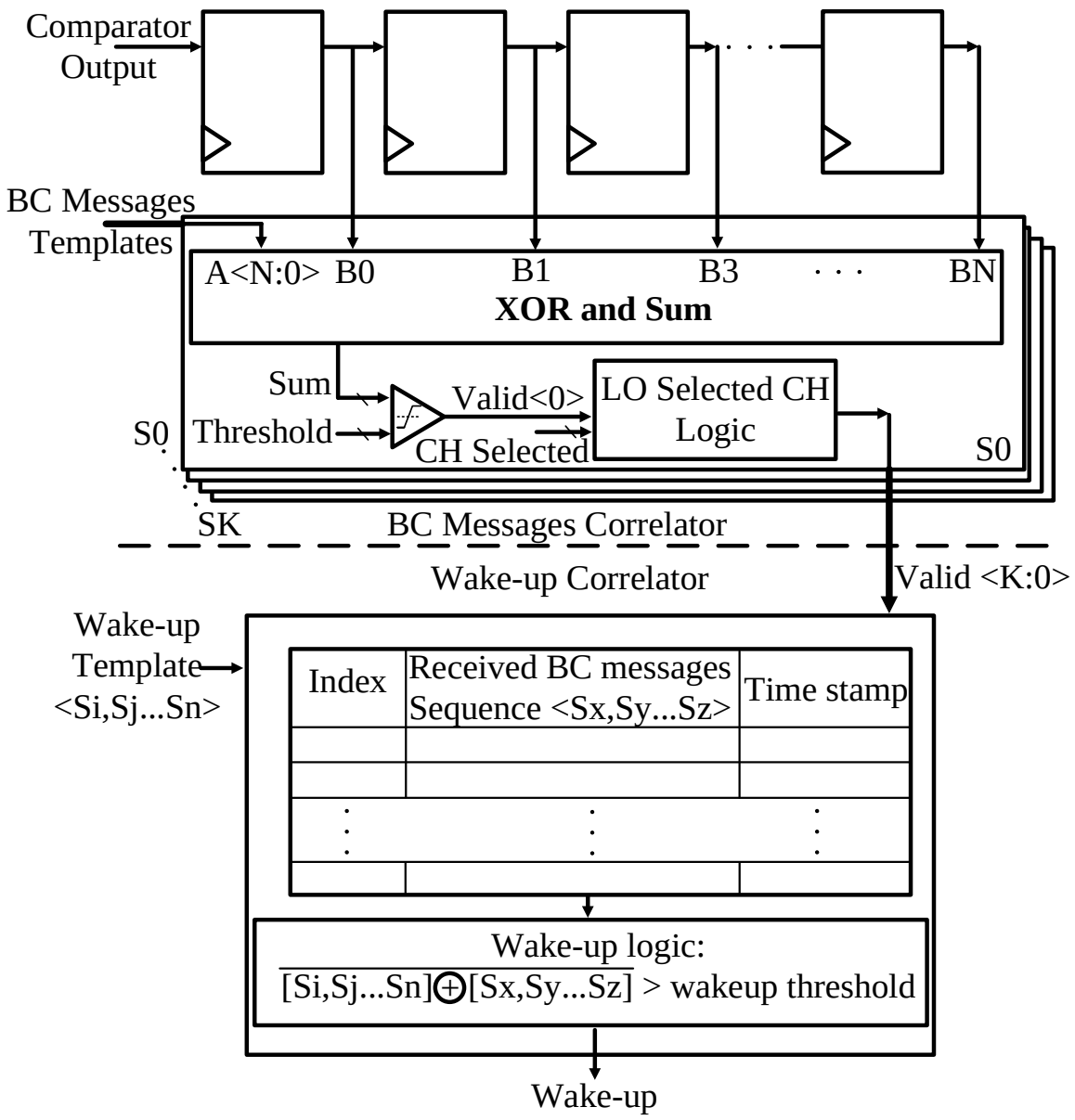


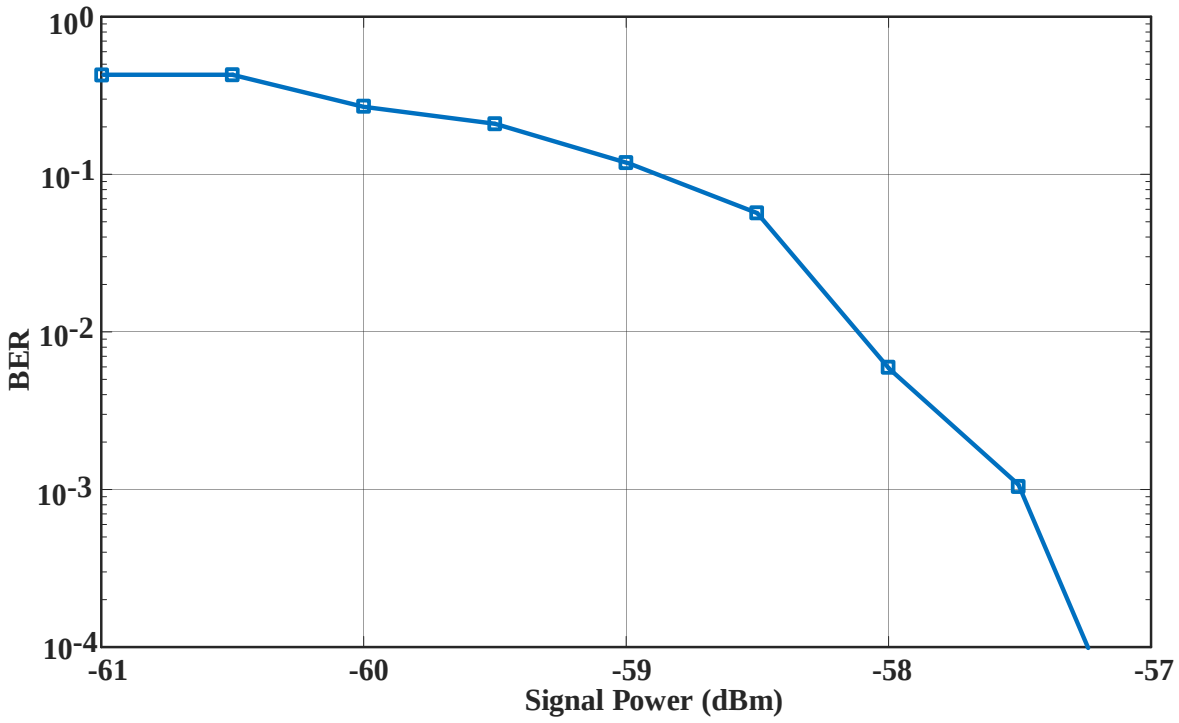
Fig.3.12 Digital baseband implementation on prototype II.

The oversampled comparator output is processed on-chip. The digital processing can be divided into two main correlators as shown in Fig.3.12: 1) BC message correlator; 2) wake-up pattern correlator. In the BC messages correlator, the bit sequence sampled by the comparator is correlated with pre-defined binary sequence templates representing potential BC symbols. When a valid message is detected, the message index is passed to the second correlator. Using the second correlator, a wake-up message is identified from a specific pattern of BC messages with pseudo-

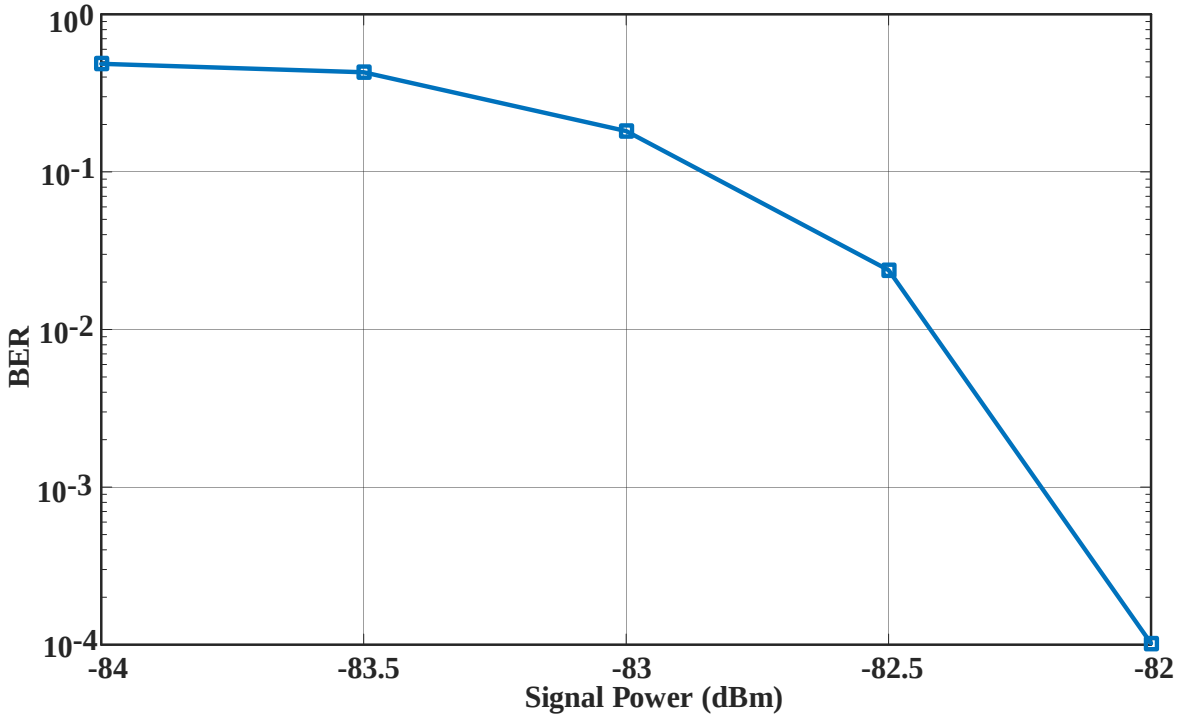
random time gaps as allowed by the BLE standard, as explained in section 2. A pseudo-random delay between advertising events helps avoid collisions, but it complicates BC message detection. To address this challenge, each new valid BC message which is part of the wake-up pattern is stored in a new array in the wake-up correlator, since it could potentially be part of a wake-up message. Simultaneously, any existing array expecting the same message index as its next message, based on the predefined pattern (template), will get updated by adding the new message to the received messages sequence. For this update to happen, the difference between the time stamps of the new and previous messages has to be within the allowed time gaps set by the BLE specifications, which include a pseudo-random part. Additionally, the time stamp gets updated every time a new message is added to the received message sequence. Once enough BC messages are received to pass the programmable threshold, the wake-up signal is asserted.

3.7 Measurement Results

The RO back-channel receiver was fabricated in a 65 nm LP CMOS process. The bit error rate (BER) performance, which is measured at a 112.5 kbps data rate, in Fig.3.13 (a) shows the receiver has a sensitivity of -57.5 dBm for a BER of 10^{-3}. Fig.3.14 (a) demonstrates the signal-to-interference (SIR) performance, which is measured with a wanted signal 3 dB over the sensitivity level and with a GFSK modulated interferer throughout this chapter. The interference rejection was measured to be -4, -20, and -30 dB for the 1^{st}, 5^{th}, and 10^{th} BLE adjacent channels, respectively. Fig.3.15 (a) shows the output waveform of the receiver in the slow hopping mode. The waveform demonstrates the receiver ability to selectively listen to the different advertising channels and detect if any transmitted packet exists at these channels. The sequence of advertising packets and events is considered to be valid when the timing gaps between packets are within the limits set by



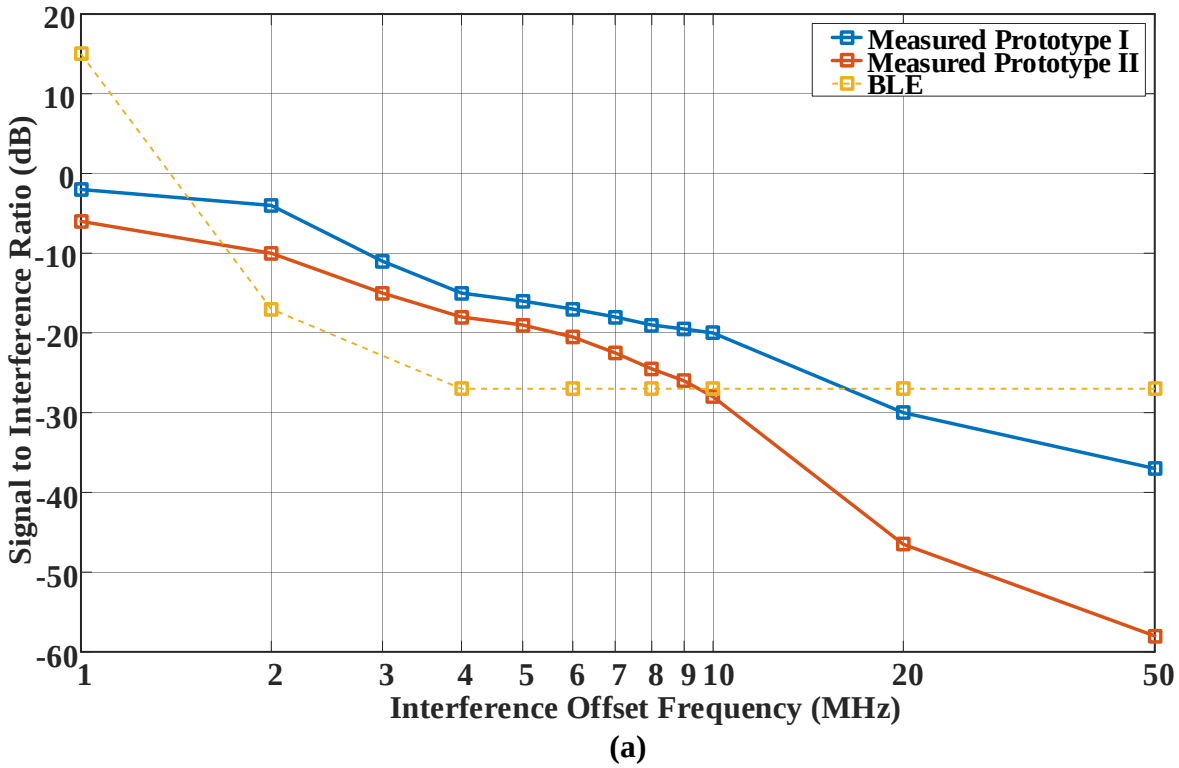
(a)



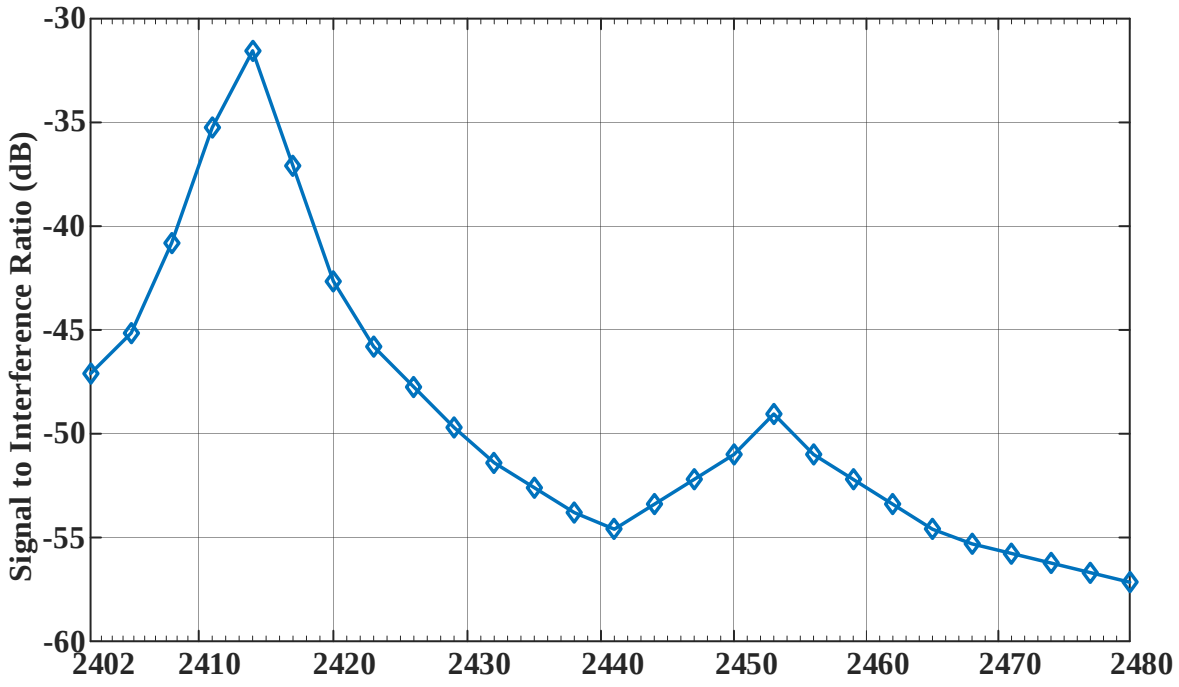
(b)

Fig.3.13 Measured receiver BER vs. signal power: (a) prototype I. (b) prototype II.

the BLE standard.



(a)



(b)

Fig.3.14 Measured signal-to interference ratio for (a) prototypes I and II vs. interference offset frequency. (b) prototype II vs. BLE channels assuming BC message communication with frequency hopping.

The total power consumption is 150 µW using 0.9 V and 1.1 V supplies for digital and

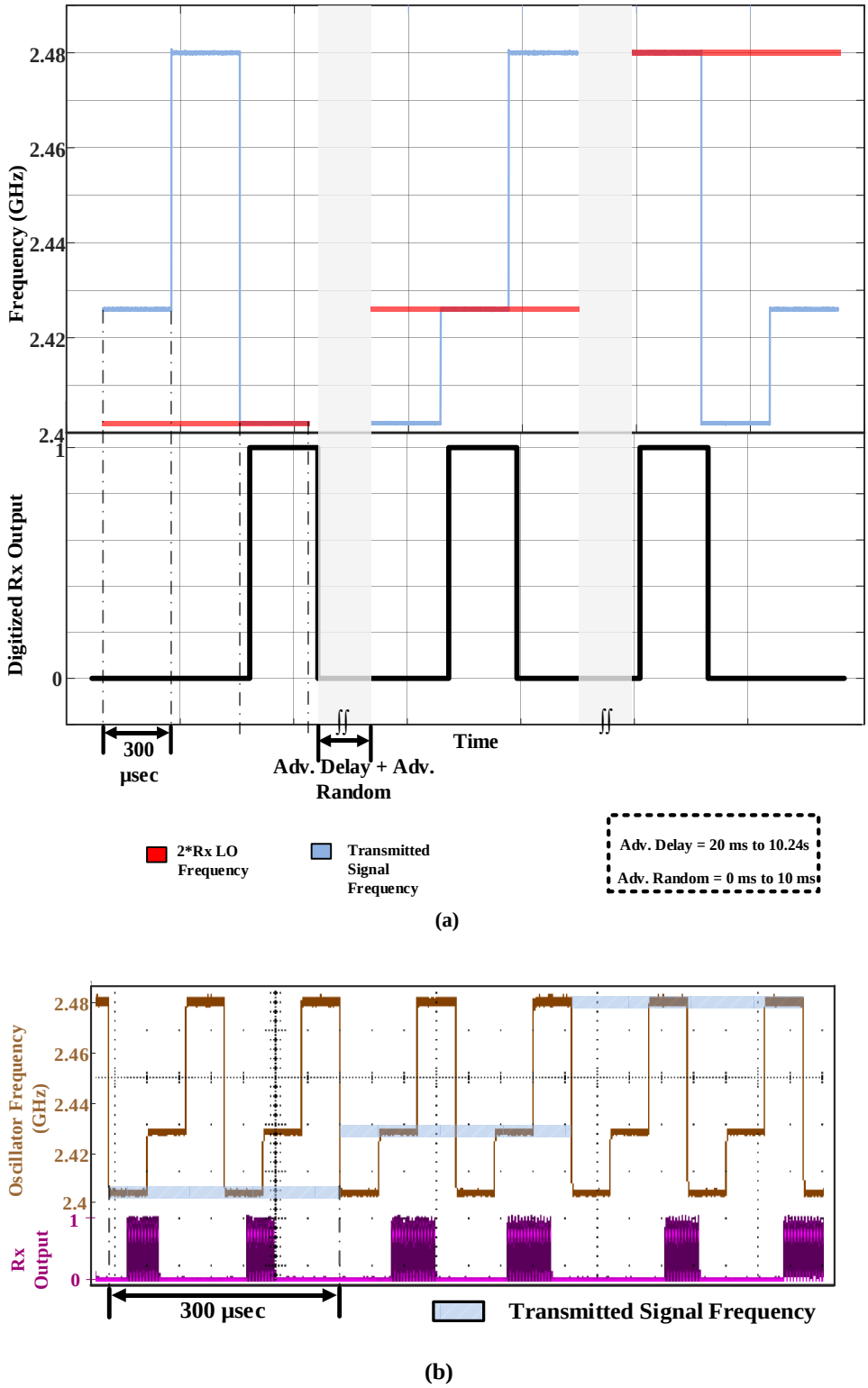


Fig.3.15 (a) Measured prototype I LO frequency and transmitted signal frequency. Digitized receiver output. (b) Measured prototype II oscillator frequency and comparator output.

analog blocks, respectively, with 120 µW dissipated by the LO (including its buffers) that runs at

1.2 GHz, the digital FLL, and the LO frequency dividers. The analog baseband consumes the remaining 30 μW.

The second prototype, which uses an LC oscillator, was fabricated in a 40nm CMOS process. Fig.3.13(b) shows the BER performance of the receiver, which achieves a sensitivity of -82.2 dBm for a BER of 10^{-3}. The BER is measured at a data rate of 250 kbps. The SIR performance for a single advertisement channel is shown in Fig.3.14 (a). The measured rejection ratios are -6, -28, and -46 dB for the 1^{st}, 5^{th}, and 10^{th} BLE adjacent channels, which does not satisfy BLE's single channel block rejection performance (yellow line). On the other hand, Fig.3.14 (b) shows the much improved (-32dB or lower) SIR performance when back-channel message level communication is used with the message threshold set at two thirds of its maximum value, as explained in section 3. This measurement was done by sweeping the interferer frequency across the BLE frequency band while the desired signal is hopping its frequency between the three advertising channels. The worst case rejection ratio is -32 dB at 2414 MHz, which is the middle channel between CH37 and CH38. This result is expected since CH37 and CH38 are closer to each other than CH9. Including the worst case, the rejection ratio at all BLE channels is better than the blocker rejection requirements as set in the BLE specifications. This performance is achieved by an energy detection receiver architecture and without using any high power high-Q filters or off-chip components for filtering. The comparator output along with LO hopping between the three adverting channels is shown in Fig.3.15 (b) when a BLE advertising event is received. The figure shows that the LC oscillator hopping speed is 6 times faster than the received packets hopping, which is required in the fast hopping mode. The short delay to turn-on the comparator output is a result of the relatively slow rise time of the envelope detector. It has no impact on the operation of the system since it is compensated for in the digital baseband. Fig.3.16 shows that the open loop

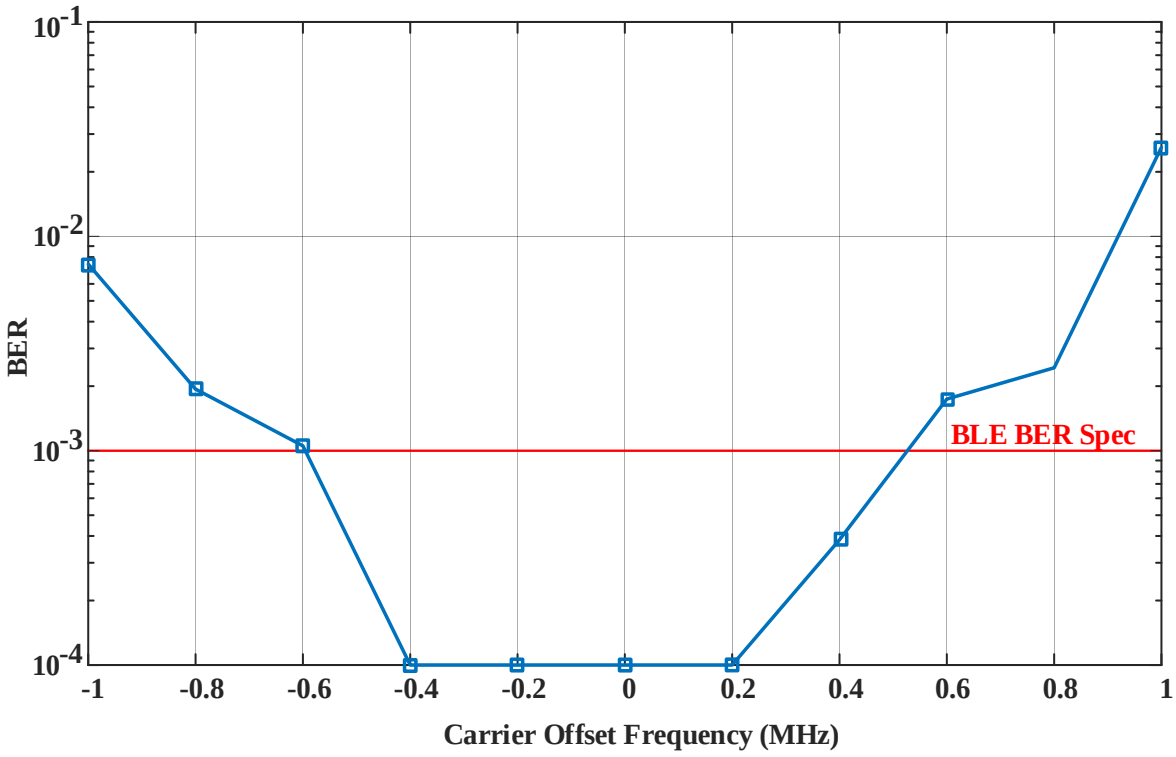


Fig.3.16 Measured BER when carrier frequency offset in prototype II.

LC oscillator used in prototype II can tolerate up to ± 0.5 MHz of frequency offset with BER < 10^{-3} making this operation possible over small voltage and temperature variations. The relaxed frequency offset specification is due to using BC modulation as opposed to demodulating each BLE packet on the bit level.

The second prototype consumes 1.2 mW using 0.9 V and 1V supplies for digital and analog blocks, respectively. The dominating blocks are the LC oscillator and the LNA, which dissipate 500 µW and 380 µW, respectively. The remaining 320 µW is consumed by the analog and digital baseband. The power breakdown of both prototypes is shown in Fig.3.17. In both prototypes, the frequency generation uses the highest percentage of power.

Table 3-1 shows a comparison between this work and the state-of the art. Prototype I consumes the lowest power compared with all other receivers that have channel selectivity in the 2.4 GHz band. To the best of our knowledge, it is the first sub-mW receiver that includes a BLE

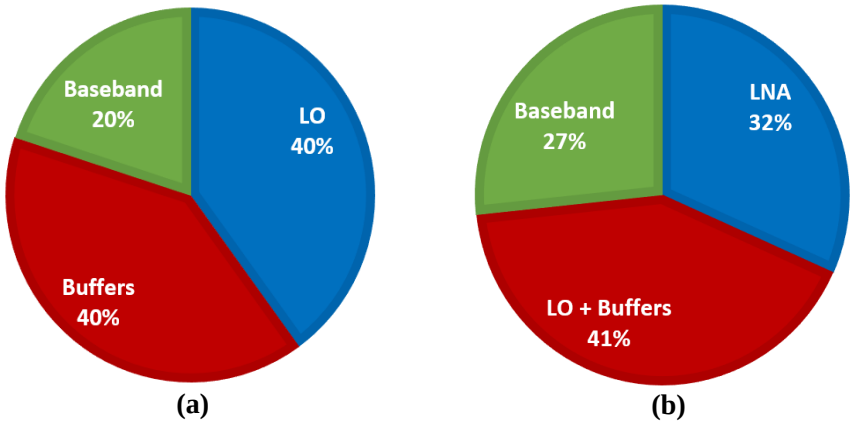


Fig.3.17 Power consumption breakdown for (a) prototype I. (b) prototype II.

compatible frequency hopping mechanism. Prototype II demonstrate fast hopping to capture the received packets' frequency sequence on a single BLE advertising event basis. Fig.3.18 shows the die photos of the chips, which have areas of 1.1 and 1 mm^2.

3.8 Conclusion

Two BLE back-channel receivers fabricated in CMOS 65nm/40nm are presented in this

Table 3-1 Performance Summary And Comparison With The State Of Art.

	This Work		[18]	[37]	[59]	[10]	[42]	[60]	[61]
	I	II							
Active Power [µW]	150	1200	0.58	600	227[1]	5500	390	2600	3040
RF Input Frequency [MHz]	2400		2400	2400	2400	2400	2400	2400	2400
WRX Supply [V]	0.9/1.1	0.9/1	0.5/1	0.8	0.6	0.6/1.1	2	1	0.8
Sensitivity [dBm]	-57.5[2]	-82.2[2]	-39[2]/56[2]	-84.9/ -84.2	-83	-90	-58	-94	-95
WRX Modulation	FSK		BLS/ CDMA	-	OOK	GFSK	Const. Envelope	GFSK	GFSK
Rx Data Rate [kbps]	112.5	250	8.192	-	1000	1000	-	1000	1000
BC Message Period [ms]	1	1	-	-	-	-	-	-	-
Technology[nm]	65	40	65	130	65	65	90	65	40
Die Area [mm^2]	1.1	1	2.25	1.2	1.17	9	1.24	1.64[4]	0.8[4]
BLE Compatible Frequency Hopping	YES (slow)	Yes (fast)	No	No	No	No	No	No	No
Adjacent Channel SIR (dB) @ 2/3MHz	-4/-11	-10/-15	-	-	8/-1	-24[5]/-27[3,5]	-	-31[5]/-36[5]	-18[5]/-24[3,5]
Channel Selectivity	YES		NO	YES	YES	YES	NO	Yes	Yes

[1]Uses External Inductors for VCO and LNA. / [2] Measured at Rx Data Rate reported in this table / [3] Interpolated/ [4] TRX Area
[5] Measured ACR based on the sensitivity and data rate defined in the BLE standard.

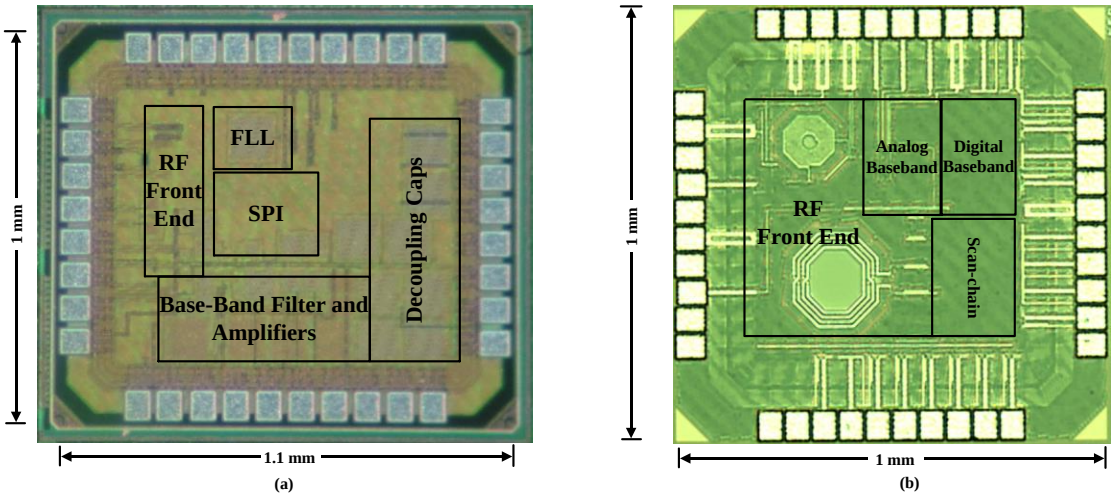


Fig.3.18 Die micrograph for (a) prototype I. (b) prototype II.

chapter. The receivers can decode messages embedded in advertising events sent by commercial BLE devices. Prototype I achieves a low power performance by using a dual-mixer as the first stage to reduce the frequency of the LO. Faster frequency hopping is implemented with prototype II by utilizing an LC oscillator for its low phase noise and better frequency stability. To make the receiver more robust to interference, both prototypes have channel selectivity which is done by hopping the LO frequency while limiting the receiver corresponding RF bandwidth to be the same as that of the BLE channel. The receivers consume 150 µW/1.2 mW with a sensitivity of -57.5/-82.2 dBm.

Chapter 4. Frequency Accuracy of Open-Loop LC Oscillators for Low Power Radios: Modeling and Measurements

4.1 Introduction

Frequency synthesisers represent a significant portion of the power consumption in ultra-low power (ULP) radio designs. A large part of that power goes to regulating the oscillator frequency in a PLL or FLL to ensure it does not drift away from the desired frequency because of PVT variations or with time. Communication standards usually specify a maximum allowed frequency drift. For example, Bluetooth Low-Energy (BLE) specifies the maximum allowed clock frequency drift in active and sleep modes to be ±50ppm and ±500ppm, respectively. Open-loop

Table 4-1 PERFORMANCE SUMMARY OF THE STATE OF ART OPEN-LOOP TRANSMITTERS.

		[62]	[63]	[64]	[65]	[66]
Power consumption (mW)	Open loop	1.537	0.8	3.6/5.5	-	0.566
	Closed loop	-	1.6	4.4/6.3	4.5	0.606
Center Frequency (GHz)		2.85	2.3	2.3	N/A	2.48
Tuning range (%)		18	22	22	N/A	4.4
Open –loop Phase Noise @ 100 KHz offset (dBc/Hz)		-92.1	-94	-94	N/A	-97
Measured PVT Variations		Temp. Only (95 ppm/^{o}C)*	N/A	N/A	N/A	N/A

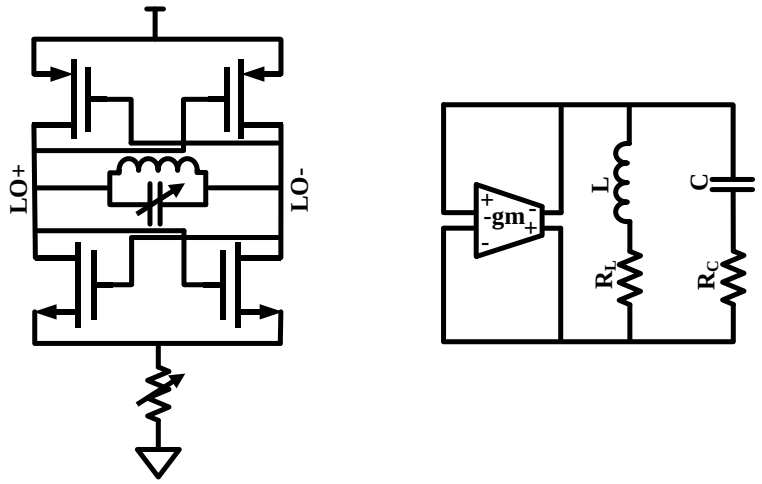
*Near room temperature

operation of radio oscillators has emerged recently as a way to further lower the power consumption in standard compliant transmitters [62–66]. In addition to power savings, open-loop operation could lead to crystal-less radios which, in addition to being lower power, reduces the overall system cost and size. To highlight how recent this trend is, Table 4-1 summarizes the performance of all transmitters using open-loop oscillators, all reported in the last 2 years. None of this work has reported variations over PVT, or the long-term stability of the oscillators. Hence, further study on this performance is prudent.

Analyzing the frequency accuracy of oscillators operating when running open-loop is essential to understand the opportunities and limitations of using them in ULP radio design. In [67, 68], the measured frequency accuracy with respect to temperature is shown. Similarly in [62], the frequency deviation with respect to temperature and time are presented. Nevertheless, these results are still not adequate to analyze how much an open-loop oscillator frequency can drift across PVT variations and with time and its impact on designing standard compliant radios that must meet stringent frequency accuracy specifications.

In this chapter, we include a model and detailed characterization of the frequency accuracy of an open-loop LC oscillator fabricated in CMOS 40nm. The results show the simulated and measured oscillator frequency shift over PVT variations and with time. The same measurement was repeated using 10 different chips to evaluate the impact of process variation on the frequency shift. The average measured temperature coefficient was 150ppm/ºC between -20 ºC to 60 ºC. The oscillator frequency shifts on average by ± 1000ppm when the supply voltage varies by ±%5 from the nominal voltage.

This chapter is organized as follows. Section 2 explains the circuit model of the LC oscillator under test and presents simulation results of the LC tank impendence variations with



(a) **(b)**

Fig.4.1. (a) LC oscillator circuit implementation. (b) LC oscillator model including loss in the LC tank.

respect to temperature. Section 3 presents the measurement setup and results for frequency shift over PVT and with time. These results are analysed in section 4 by assessing the reliability of open-loop operation in standard compliant low-power radio design. Finally, the conclusion is drawn in section 5.

4.2 LC Oscillator Circuit Model and LC Tank Simulations Results

An LC oscillator was selected due to its superior frequency stability and phase noise. Its schematic is shown in Fig.4.1 (a). A complementary cross-coupled pair featuring current reutilization was used, resulting in a measured power consumption of 500 μW. A digitally-switched resistor is implemented as the tail current, since resistors have much lower flicker noise than MOS transistors. Thus, low phase noise at low frequency offsets is achieved, which benefits frequency stability. The frequency of the LC oscillator is tuned through a digitally-switched capacitor array. The overall frequency tuning range is 2300 to 2510 MHz with a measured resolution of 20 kHz. This resolution was chosen to target the BLE standard. It supports all BLE channels with sufficient resolution for GFSK modulation.

The ideal LC tank natural resonant frequency is given by:

$$\omega_0 = \sqrt{\frac{1}{LC}} \tag{1}$$

however, when the tank loss is included in the model as shown in Fig.4.1(b), the resonant frequency becomes dependent on the tank loss [67]:

$$\omega(T) = \omega_0 \sqrt{\frac{CR_L^2(T) - L}{CR_C^2(T) - L}} \approx \omega_0 \sqrt{1 - \frac{CR_L^2(T)}{L}} \tag{2}$$

where R_L and R_C represent the loss in the inductor and the capacitor, respectively, and T is temperature. The tank loss is temperature dependent and is the dominant source of frequency shift when temperature is not stable [67]. In particular, the inductor loss variation is the most significant factor in shifting the frequency. This is because in integrated LC tanks at radio frequencies, the inductor value L is normally in the nH range, which is much larger than the capacitor value C, in the pF range. This leads to a much bigger impact by R_L on frequency drift with temperature compared with R_C. More details about the impact of the non-ideality in the active devices, which implement the negative resistance and its dependency on bias, are presented in [67, 69].

In order to improve the accuracy of the oscillator frequency shift simulations, the temperature coefficient (TC) of the oscillator components should be precisely accounted for in the model used in simulations. The temperature dependency of the passive elements used in Eq.2 is simulated across a temperature range from -20ºC to 60ºC. Fig.4.2 shows that both L and C vary by around 1000ppm. However, since they have opposite slopes of change with temperature, $\sqrt{1/LC}$ stays close to constant. In addition, $/L$, which could contribute to the frequency shift based on Eq.2, varies by around 2000ppm. On the other hand, Fig.4.3 illustrates that R_C and R_L vary by

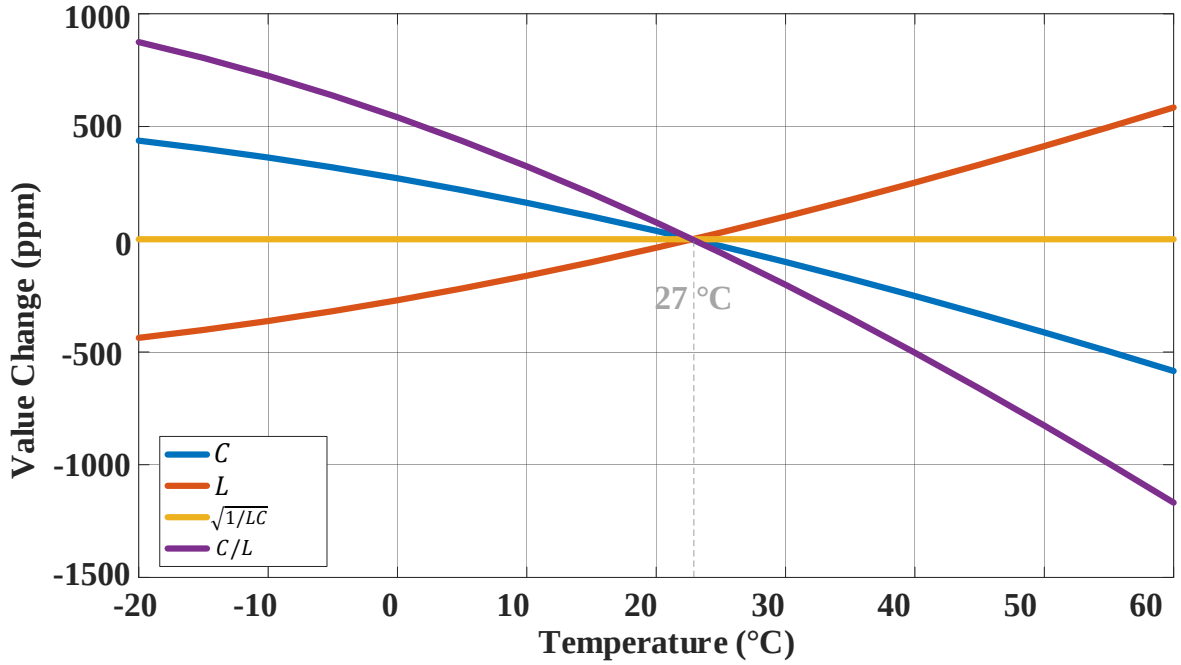


Fig.4.2. Simulated $C, L, \sqrt{1/LC}$ *and* C/L change with respect to temperature.

around 300000ppm and 150000ppm, respectively. Nevertheless, R_L still has much greater impact on the frequency drift as explained earlier. These simulation results confirm that R_L is the dominant factor in the frequency change with temperature. This is further verified by simulating the resonant

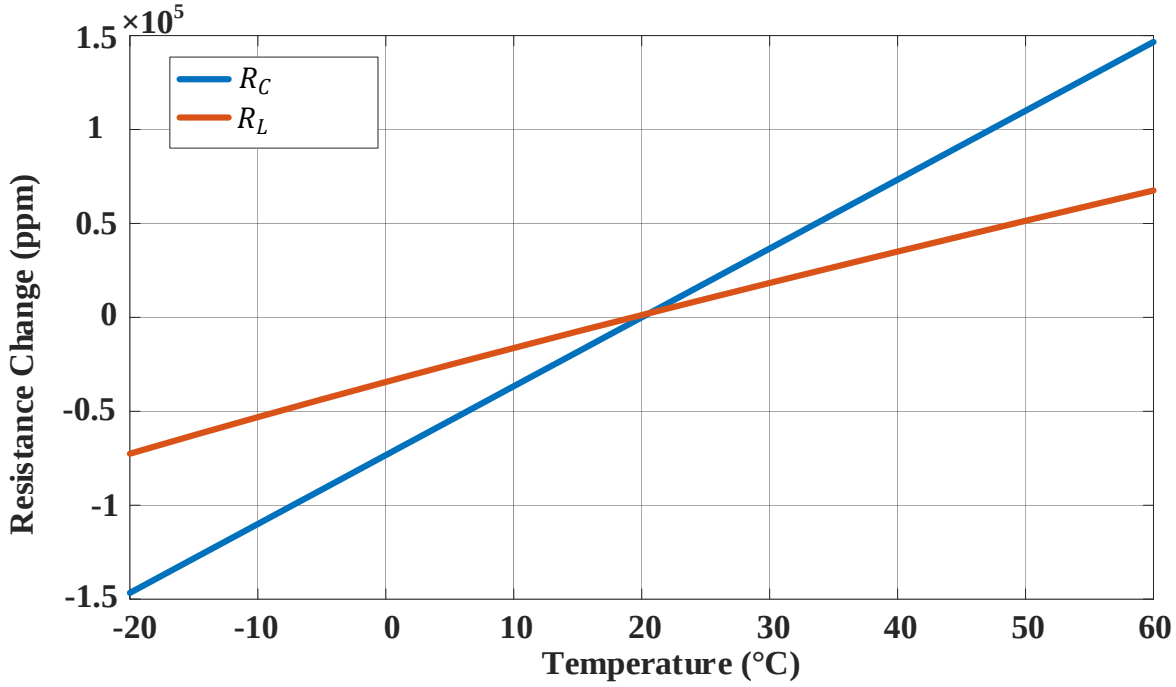


Fig.4.3. Simulated LC tank loss change with respect to temperature.

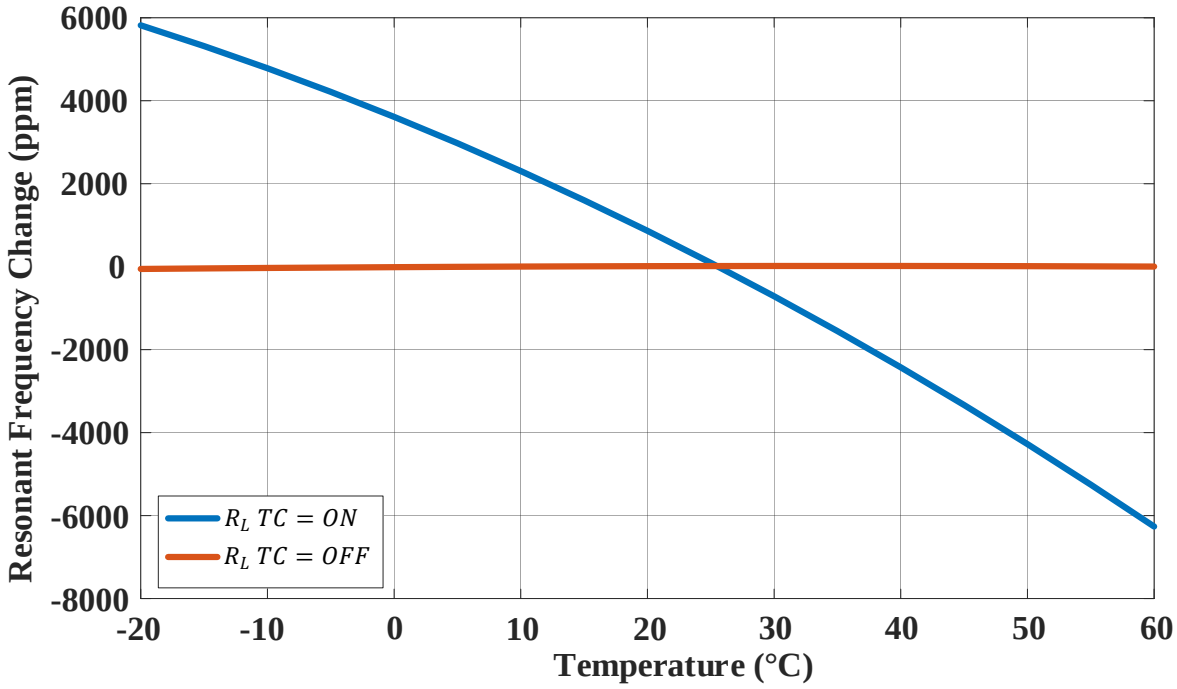


Fig.4.4. Simulated LC tank resonant frequency change with respect to temperature.

frequency of the LC tank with and without the TC of R_L as shown in Fig.4.4. The figure demonstrates that the frequency shift becomes negligible when the effect of R_L dependency on temperature is not included in the model. Consequently, an accurate model that captures the correct TC of the loss in the coil is required in any temperature dependent simulation of an LC oscillator. In our model, the TC of R_L is estimated based on [70] to be 0.006Ω/ ºC. This number was based on the technology parameter of TSMC CMOS 40nm and is a function of the material and dimensions of the metal used to synthesize the inductor on chip.

4.3 Measurement Setup and Results

Fig.4.5 shows the measurement setup where a host PC controls an Opal Kelly XEM3001 FPGA, an Agilent E3631A voltage source, and a TestEquity107 temperature chamber. Also, the host reads the measured frequency spectrum with an Agilent N9020A signal analyzer. The FPGA is used to set the chip's configuration bits though the scan chain. These bits include the oscillator's

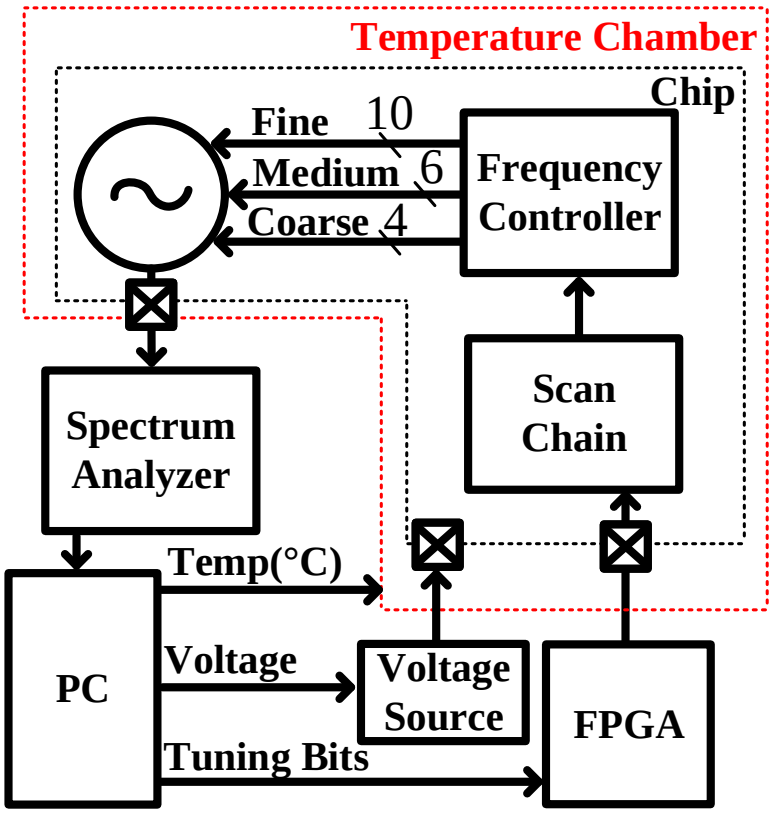


Fig.4.5. Measurement setup.

coarse, medium and fine tuning bits.

The measured frequency tuning range of the LC oscillator is shown in Fig.4.6 for three temperatures: -10ºC, 20ºC and 40ºC. The tuning range is about 210 MHz or around 10% of the center frequency. The frequency dependency on temperature is shown in Fig.4.7 for the temperature range from -20ºC to 60ºC. The calculated frequency shift, which is based on Eq.2, matches the simulations very closely up to 40ºC. At higher temperatures, the impact of non-ideality in the active devices starts to become significant which introduces more frequency shift than what the simplified model predicts as seen in Fig.4.7. The frequency shift was measured for ten different chips. The measured average temperature coefficient of the oscillator frequency drift, which matches simulations within less than 15ppm, is around 150ppm/ºC. The variance of the measured samples increases beyond 35 ºC as shown by the size of the bars in Fig.4.7. Both the supply voltage

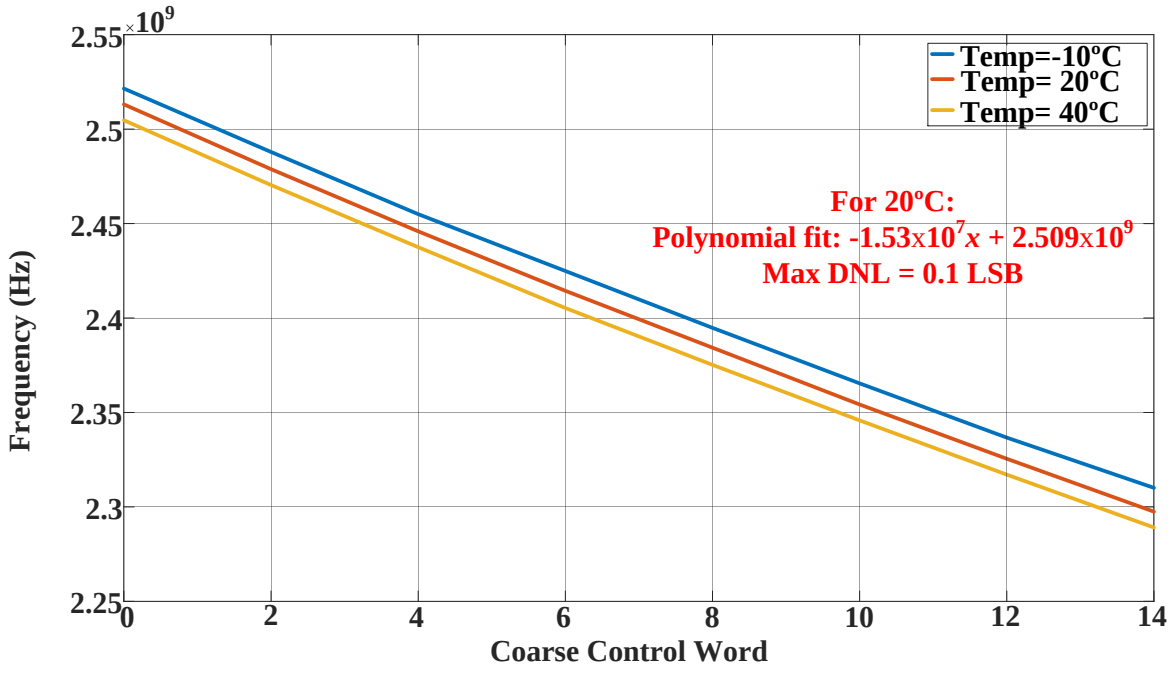


Fig.4.6. Measured oscillator frequency tuning range at:-10ºC, 20ºC and 40ºC.

and oscillator control word were fixed during this part of the experiment. This result shows that the variation over temperature exceeds the +/-50ppm requirement for BLE, therefore calibration for temperature is required for open-loop operation. Furthermore, any temperature calibration must

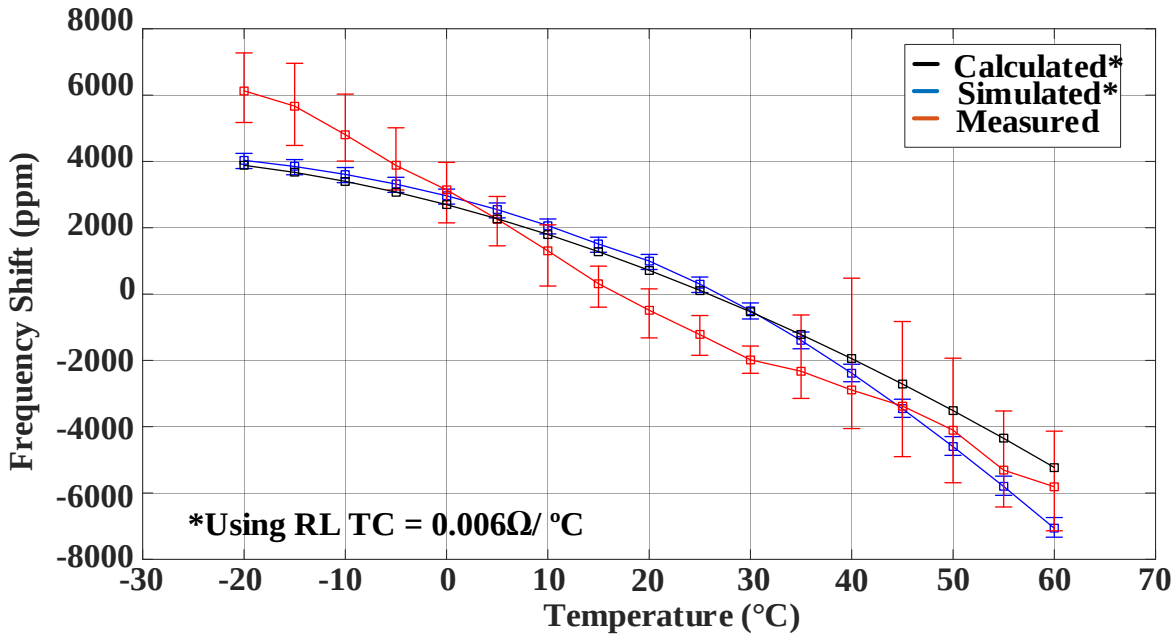


Fig.4.7. Calculated, Simulated and Measured frequency shift with respect to temperature

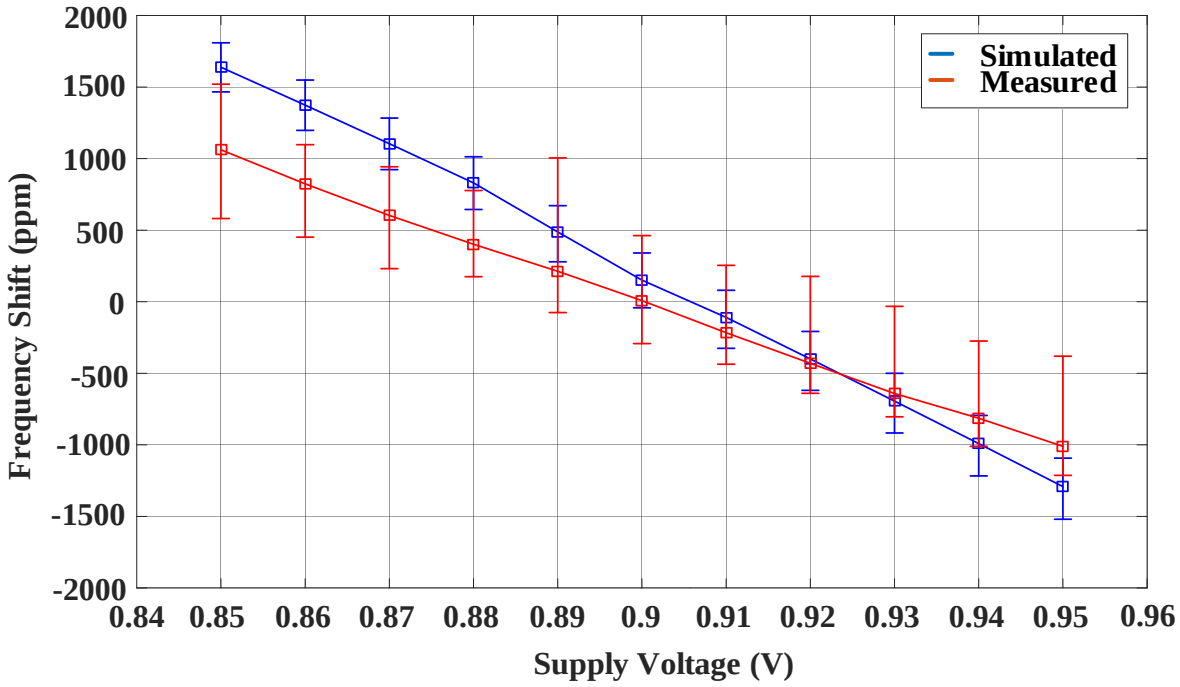


Fig.4.8. Simulated and Measured frequency shift with respect to supply voltage.

be tuned to account for process variation as shown by the spread of the results in Fig.4.7.

Fig.4.8 shows the simulated and measured frequency shift with respect to the supply voltage. As in the temperature sweep experiment, the shift in frequency is measured across ten chips. On average, the shift in frequency is measured to be 25ppm/mV. This is within less than 10ppm from the simulated average frequency shift. Temperature and oscillator control word were held constant for this part of the experiment. This result shows the supply must be kept within +/-2mV to meet the +/-50ppm requirement.

To characterize the impact of process variation, the initial frequency is measured for the same ten chips under the same controlled temperature (20 ºC) and supply voltage. Moreover, all the chips were programmed with the same oscillator control word. The frequency variation is shown in Fig.4.9. Over ten chips, the measured frequency spread is 22 MHz or about 9000ppm. This result shows that process variation must also be calibrated for open-loop operation.

To demonstrate how the frequency drifts with time, the Allan standard deviation is

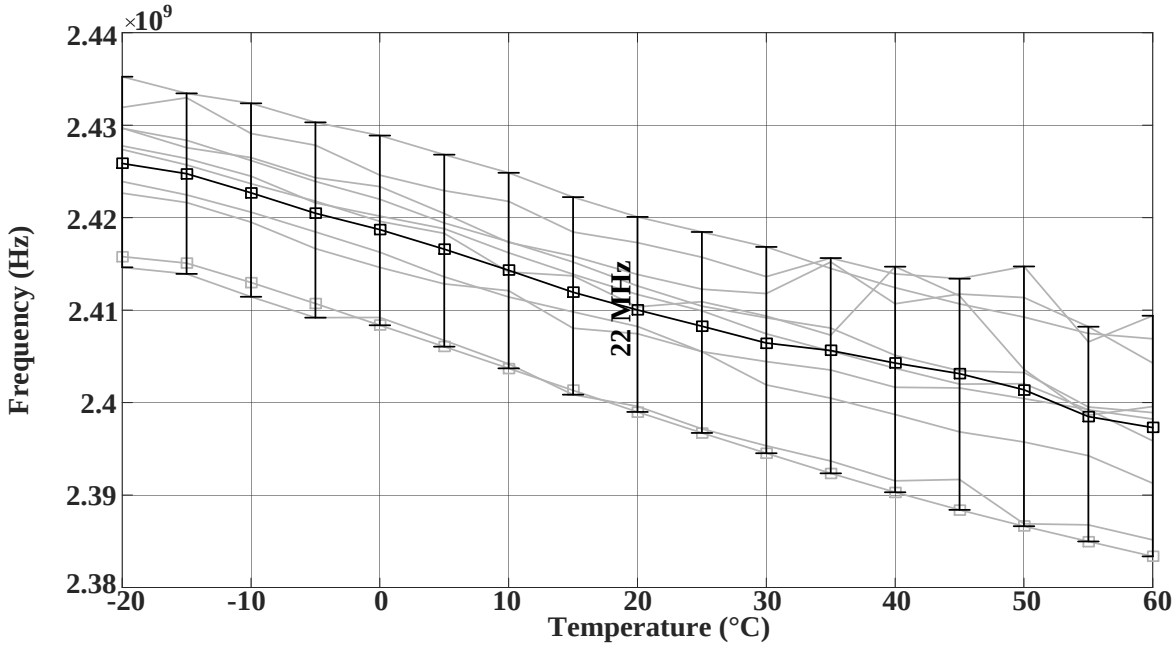


Fig.4.9. Measured initial frequency of ten chips with respect to temperature.

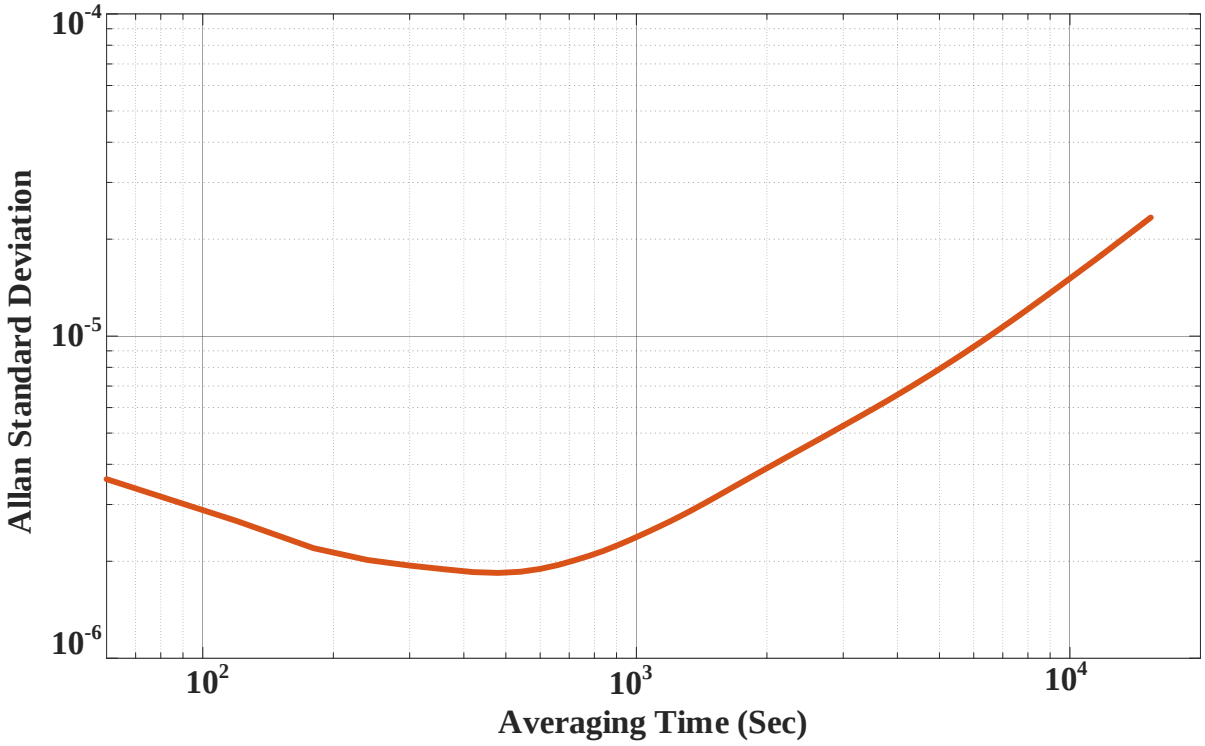


Fig.4.10. Measured Allan standard deviation.

calculated for a range of averaging time windows as shown in Fig.4.10. This is based on measuring

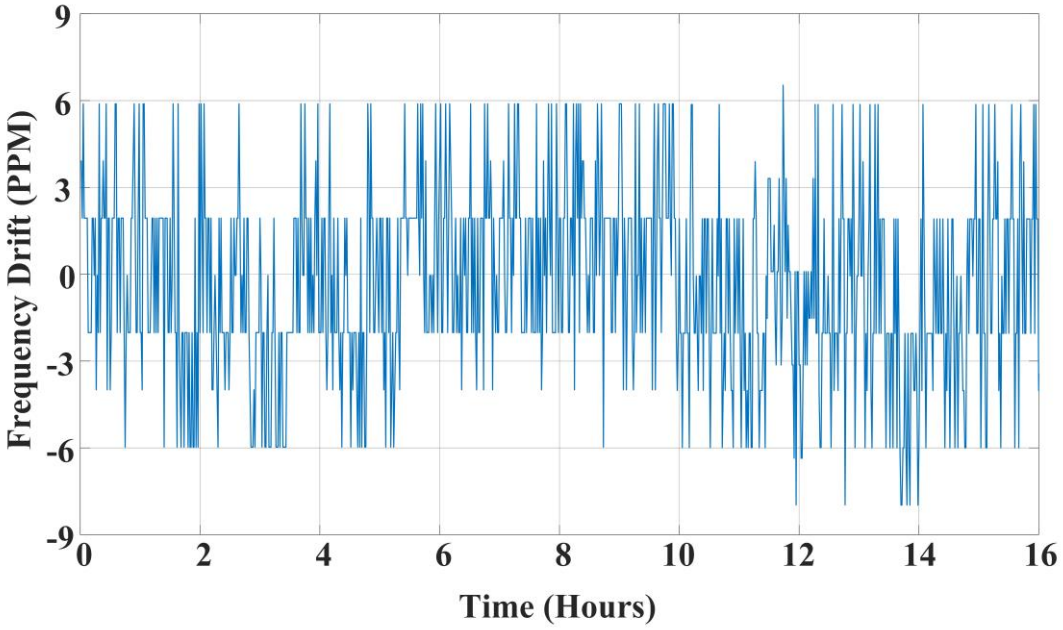


Fig.4.11. Measured frequency shift over 16 hours.

the instantaneous oscillator frequency every one minute over a period of 16 hours as in Fig.4.11. Over that time, the maximum frequency shift is measured to be less than ±10ppm from the average frequency.

4.4 Analysis of Measured Drift

In this analysis, the measurement results are compared with BLE specifications to evaluate the efficacy and the limitations of using open-loop oscillators in standard compliant radios. The BLE standard was chosen because it provides a solution to connect IoT nodes with mobile devices [12]. Also, in BLE, the carrier is modulated using Gaussian Frequency-Shift-Keying (GFSK) which makes this open-loop frequency accuracy analysis applicable. The following paragraphs describe the calibration required to achieve open-loop operation of a BLE radio.

The measured process variation of the center frequency of 22 MHz (9000ppm) necessitates an initial frequency calibration for each chip. In the oscillator under test here, the initial accuracy can be calibrated to better than ±10ppm as a result of the fine tuning resolution of

the capacitor bank. The measured temperature and voltage coefficients were 150ppm/ºC and 25ppm/mV, respectively. If these parameters vary such that the frequency shift is more than ±50ppm, frequency compensation has to be implemented to meet the BLE specifications. For example, temperature compensation can be implemented using a temperature sensor and a look-up table to adjust the oscillator control word to maintain the frequency when the temperature changes. The temperature sensor should have a resolution of 0.3 ºC or better to meet the BLE specifications for frequency accuracy. Such a temperature sensor can be fully integrated with very low power like in [71].

Fig.4.11 shows that the maximum oscillator frequency shift over a period of 16 hours in room temperature and using a typical power supply. The drift is less than the BLE specification of ±50ppm. In addition, the frequency drift is less than ±8ppm over a period of one second as in Fig.4.12, which can include multiple BLE advertising events.

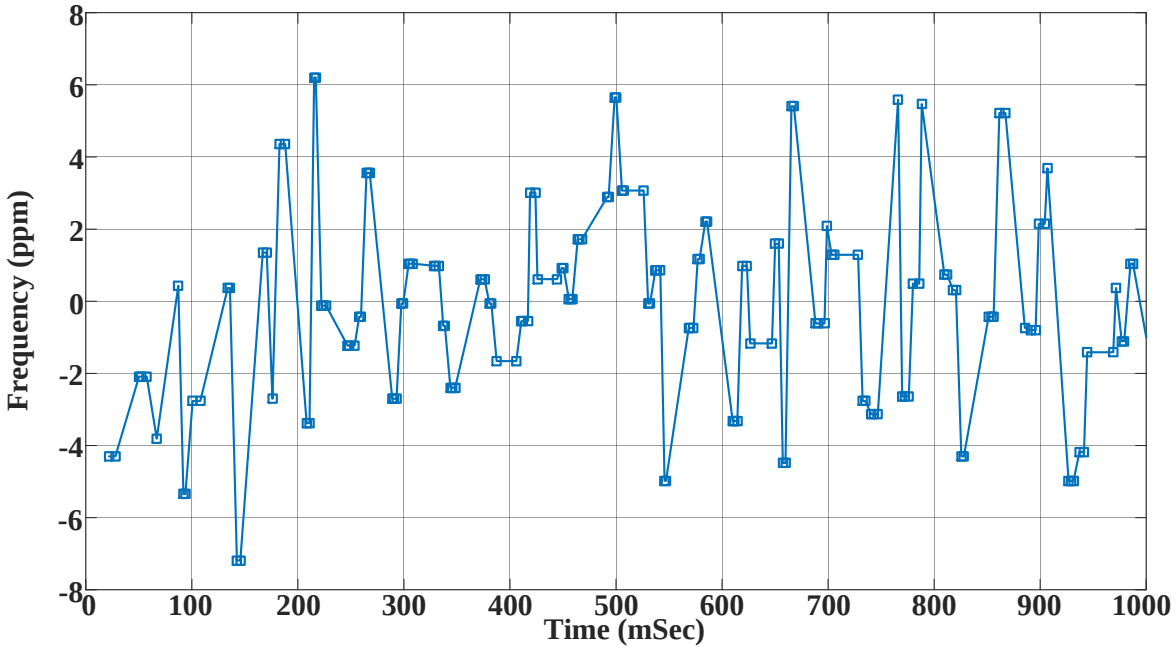


Fig.4.12. Measured frequency shift in one second.

4.5 Conclusion

The frequency accuracy of an LC oscillator fabricated in CMOS 40nm is characterized in this chapter. For both voltage and temperature variations, the measurements and simulations results match closely when the TC of the loss in the coil is accounted for accurately in the oscillator model. The initial frequency in 10 samples is found to vary by around 1% due to process variation. Also, the temperature coefficient is measured to be 150ppm/^{o}C. The measured oscillator frequency shifts by less than ±10ppm over period of 16 hours and less than less than ±8ppm over one second, which meets the BLE specification. This implies that BLE compliant open-loop operation is feasible with frequency calibration to compensate for process and temperature variations.

Chapter 5. A Crystal-Less BLE Transmitter with -86dBm Frequency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet

5.1 Introduction

Wireless transceivers traditionally perform local oscillator (LO) calibration using an external crystal oscillator (XTAL) that adds significant size and cost to a system. Removing the XTAL enables a true single-chip radio, but an alternate means for calibrating the LO is required. Integrated references like on-chip LC [67] or relaxation [72] oscillators are either high power or have PVT sensitivity too high for wireless standards. Multiple crystal-less radios address this challenge [73–76]. [73] replaces the XTAL with an FBAR resonator, which is still not fully-integrated. [74, 75] recover a reference clock from a received signal but take 100s of ms to lock and are thus highly susceptible to interference. [76] uses an open-loop LC oscillator to reduce power but has insufficient frequency accuracy for wireless standards.

This chapter presents the first crystal-less transmitter with symmetric over-the-air clock recovery compliant with the BLE standard. The novelty of this work is 1) a frequency-hopping back-channel receiver to detect advertising events from a broadcaster while rejecting interference; 2) an architecture with two fast-locking PLLs and selective baseband filter to recover a reference clock from a received packet and then transmit a GFSK-modulated BLE packet on any channel, and 3) an ADPLL with averaging controller to recover a stable reference from a GFSK-modulated data-whitened signal. The crystal-less transmitter with clock recovery meets all BLE requirements for SIR, making this a robust solution for removing the XTAL even in densely populated networks.

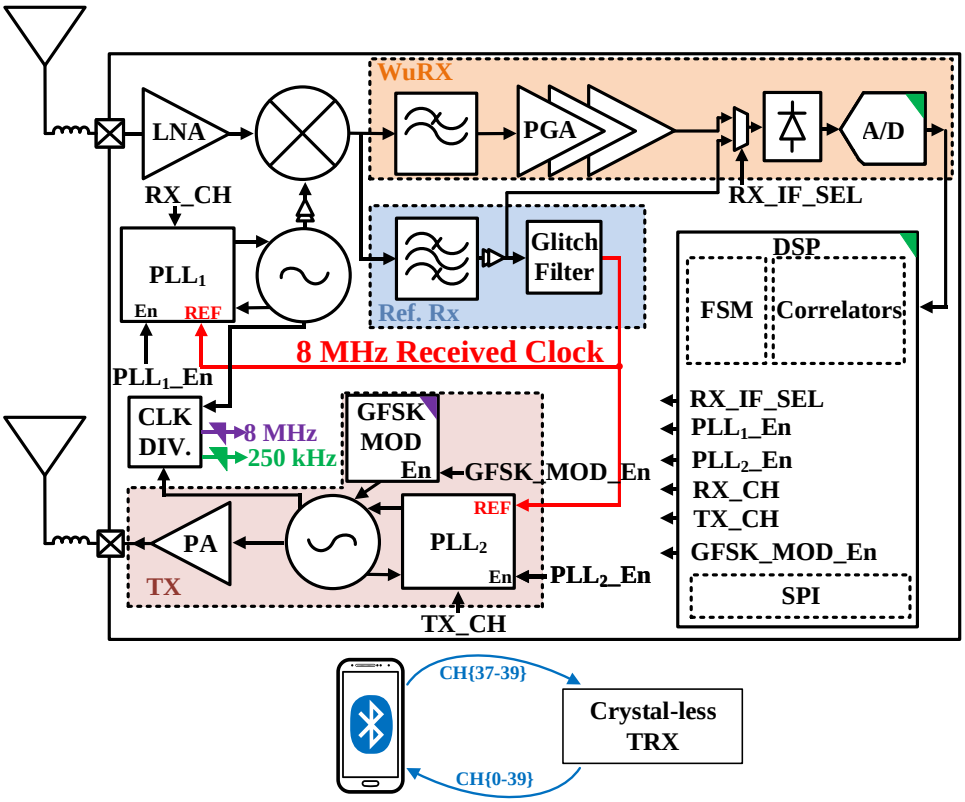


Fig.5.1. Block diagram of the crystal-less transceiver.

5.2 Over-the-Air Frequency Calibration

The fully-integrated crystal-less transceiver is shown in Fig.5.1, which receives and transmits BLE compliant messages. The transceiver includes two local oscillators: LO_1 for the receiver and LO_2 for the transmitter. The receiver consists of two RX signal paths mixed down by LO_1: 1) a back-channel (BC) direct conversion path for detecting advertising (ADV) events, and 2) a clock recovery path with an intermediate frequency of 8MHz producing the reference for PLL_1 and PLL_2. The transmitter comprises a second PLL_2 with LO_2, a GFSK modulator for open-loop modulation, and a digital PA. Both LOs are on-chip LC oscillators, are trimmed only once for process variation, and when in BC scanning mode operate open-loop without any reference. This is sufficient for a divided LO_2 to clock the digital baseband and for LO_1 to frequency hop between ADV channels in the energy-detection BC path (Fig.5.2) and detect an ADV event (a sequence of

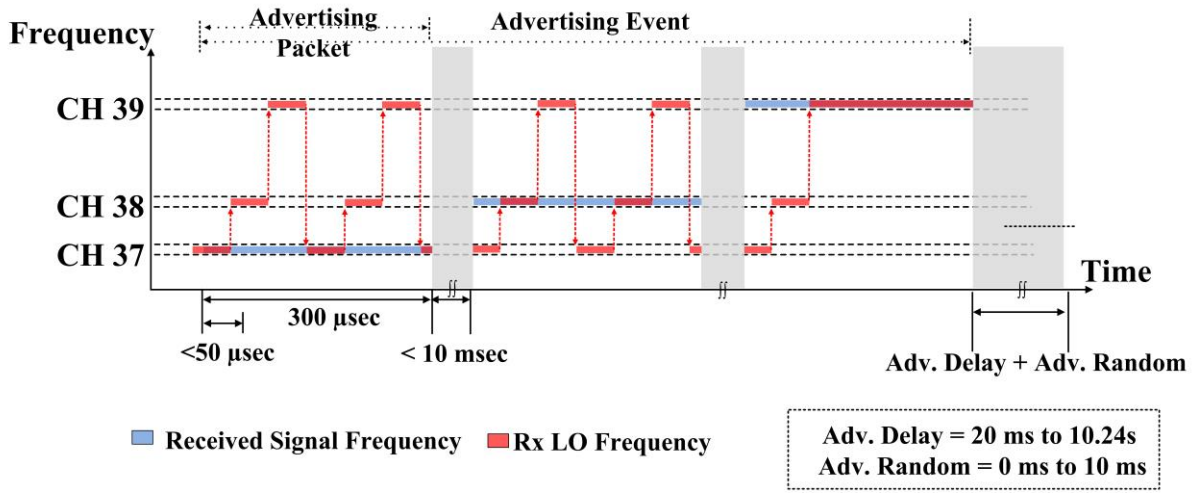


Fig.5.2. LO_1 frequency hopping during a BLE advertising event.

3 packets on the ADV channels). Upon detecting the 3rd packet in an ADV event, PLL_1 is enabled and locks LO_1 within 50µs to the 8MHz reference recovered from the packet by using a novel averaging controller immune to GFSK-modulated signals. Lock detect of PLL_1 then enables PLL_2 to lock LO_2 in less than 50µs to the 8MHz recovered reference with the LO_2 RF centered on any of the 40 BLE channels. The 8MHz reference is only present while the 3rd packet is being received, therefore both PLLs must lock before it ends. Finally, after the 3rd packet ends, the chip switches from RX to TX mode, and LO_2 is used in open-loop to transmit a GFSK-modulated BLE-compliant packet in the desired channel.

Fig.5.3 shows the state diagram and waveforms for the transient operation of the transceiver detecting an ADV event, recovering the 8MHz reference, then transmitting a packet. The process begins with the RX back-channel path enabled, scanning the 3 BLE ADV channels for a predefined advertising channel hopping sequence and packet length as in [12]. These channels are CH37, CH38, and CH39 at 2402, 2426, and 2480MHz, respectively. LO_1 hops between channels every 50µs to oversample and detect the energy of ADV packets. Since the BC RX is only scanning for energy in the ADV channels, the LO frequency accuracy is relaxed, and the

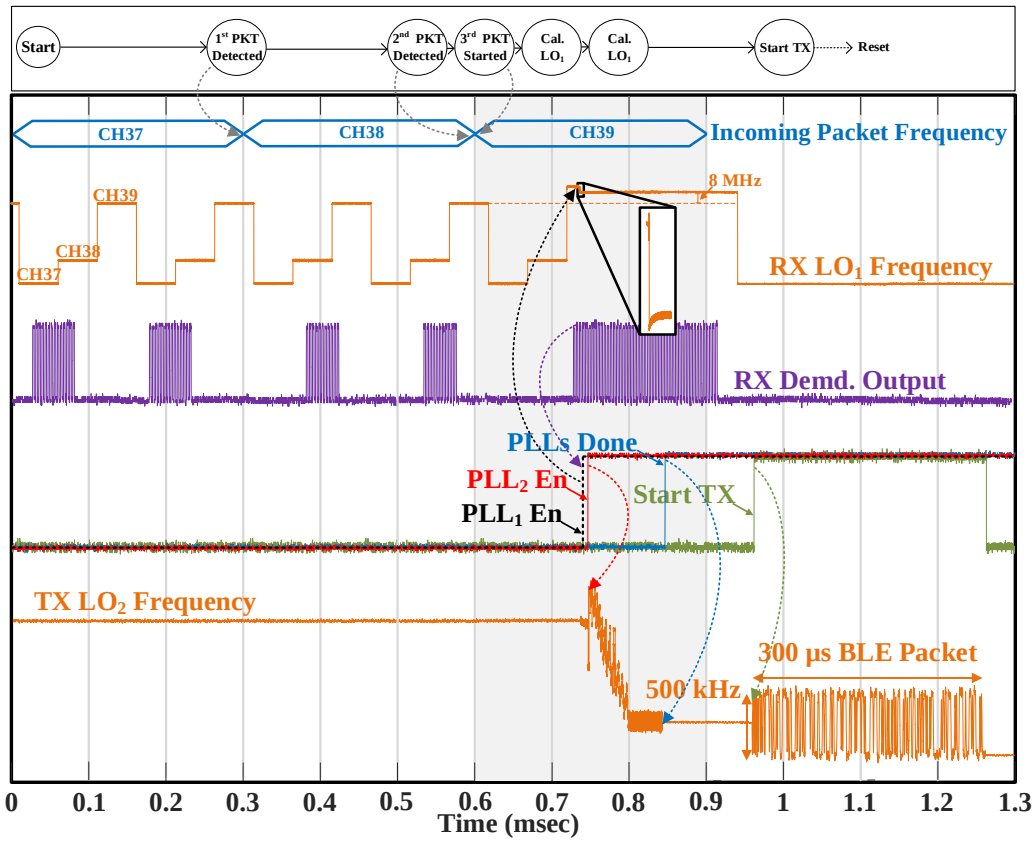


Fig.5.3. TRX operation state diagram. Measured waveforms of the TX/RX LOs frequencies calibration and sending one BLE advertising packet afterwards.

ADV event can be detected with LO_1 hopping open-loop. In addition, using direct-conversion simplifies the baseband filtering and gain and reduces this path's power consumption. Once the BC demodulator detects the intended ADV event by correlating the digitized signal with programmable templates, the receiver switches to the 2nd RX path to recover a clock reference from the last incoming packet. This ensures that neither of the two PLLs are enabled until a valid ADV event is detected, eliminating false wakeups and erroneous transmissions.

In the clock recovery path, the BLE packet is down-converted to an IF of 8MHz and filtered by a 6th order BPF with a bandwidth of 2MHz, removing interferers on adjacent channels. This filter is trimmed only once for process variation. A glitch filter removes short pulses that might exist, e.g. from noise. This signal then becomes the reference for the 2 PLLs, only present while

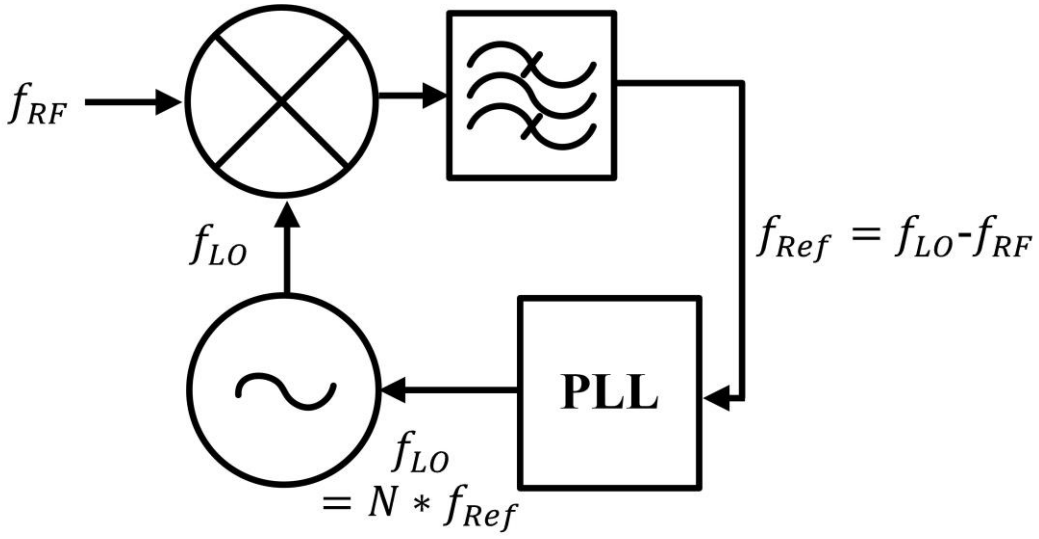


Fig.5.4. Mixer-PLL$_1$ loop transfer function.

receiving the packet. An 8MHz reference is sufficient for a combined PLL lock time less than one ADV packet, meaning the TX LO is ready before the end of the ADV event. 8MHz also relaxes the required BPF center frequency and quality factor. Using two LOs allows for receiving and transmitting on different BLE channels and for optimizing each PLL controller.

Fig.5.4 demonstrates the different frequencies of the signals which are generated in the mixer-PLL loop. The lower side IF ($f_{LO} - f_{RF}$) is selected since the upper side ($f_{RF} + f_{LO}$) is going to be out of the BLE band at f_{RF} =2.496GHz when the third packet uses CH39. This is because the oscillator frequency (f_{LO}) is chosen such that $f_{LO} > f_{RF}$ to ensure the image frequency doesn't fall within the BLE band, and instead, gets filtered by the RF front-end. When taking into account these design considerations, the following equation holds:

$$f_{LO} = \frac{N}{N-1} f_{RF} \quad (1)$$

where N is the PLL multiplication ratio ($N = f_{LO}/f_{Ref}$). A fractional-N PLL is used to enable the flexibility of choosing which BLE channel to use.

To analyze the stability of the new loop shown in Fig.5.4, the closed-loop transfer function is derived as function of the band-pass filter and PLL individual transfer functions:

$$TF_{closed} = \frac{OUT(s)}{IN(s)} = \frac{f_{LO}(s)}{f_{RF}(s)} = \frac{f(s)P(s)}{f(s)P(s)-1} = \frac{NUM_{cl}(s)}{DEN_{cl}(s)} \quad (2)$$

where $f(s)$ and $P(s)$ are the band-pass filter and PLL closed-loop transfer functions, respectively. NUM_{cl} and DEN_{cl} are the closed-loop transfer function numerator and denominator, respectively. On the other hand, the open-loop transfer function is:

$$TF_{open} = \frac{OUT(s)}{IN(s)} = \frac{f_{LO}(s)}{f_{RF}(s)} = f(s)P(s) = \frac{NUM_{op}(s)}{DEN_{op}(s)} \quad (3)$$

where NUM_{op} and DEN_{op} are the open-loop transfer function numerator and denominator, respectively. Substituting (3) into (2) :

$$TF_{closed} = \frac{NUM_{cl}(s)}{DEN_{cl}(s)} = \frac{NUM_{op}(s)}{DEN_{op}(s)} \times \frac{DEN_{op}(s)}{NUM_{op}(s)-DEN_{op}(s)} \quad (4)$$

Based on (4), the new poles in the system are the roots of $(NUM_{op}(s) - DEN_{op}(s))$. Assuming both the band-pass filter and PLL are designed to be stable when functioning independently, the new poles would also have to be designed to be in the left half plane to maintain the stability of the closed-loop system.

5.3 Calibration for Process and Temperature Variations

A one-time calibration is done for each chip to compensate for process variations and find the polynomial coefficients for temperature compensation. This applies to two major circuit blocks in the system: 1) the local oscillators, and 2) the band-pass filter. For the oscillators, both LOs, which are on-chip LC oscillators, are trimmed first for process variation. This process consists of finding the coarse digital control word for the three BLE advertising channels. That is 1-point for each advertising channel (total of 3 points). When temperature changes, the oscillator frequency will shift as shown in Fig.5.5. In this figure, the red line represents the measured LO center

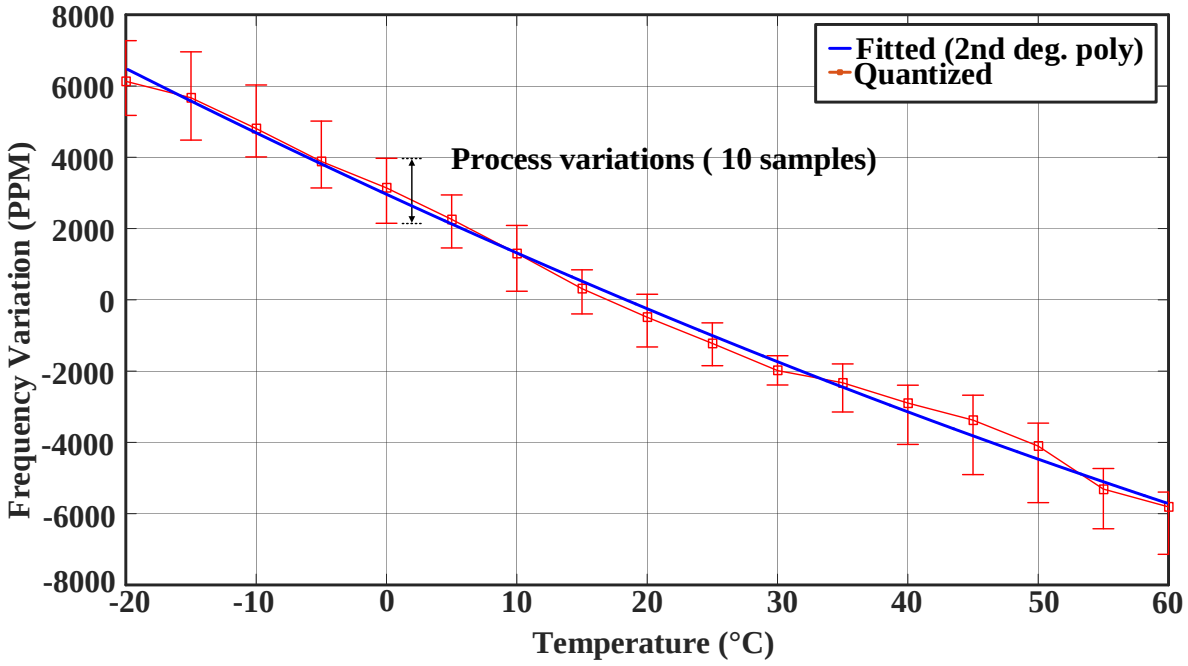


Fig.5.5. Fitted and Measured oscillator frequency shift with respect to temperature.

frequency variation as function of temperature and the blue line represents the fitted second degree polynomial. As the figure demonstrates, a second degree fitting is sufficient to get to better than 1000 ppm frequency accuracy needed to start the crystal-less operation. Consequentially, when temperature changes, it is sufficient to meet the accuracy system requirements for the LOs' center frequency by using: 1) a temperature senor with better than 0.3˚C resolution, and 2) a second degree polynomial fitting (2-point calibration), where the coefficients are calculated based on two measured points during the on-time calibration. Similarly, the second critical block, which is the band-pass filter, is also trimmed first to compensate for processes variations. This is done by tuning the filter's RC network to calibrate its center frequency to 8MHz and bandwidth to 2MHz. Fig.5.6 shows the measured filter center frequency shift in as the black line and the 2nd degree fitting as blue line. The curve with fitted coefficients tracks the measured center frequency of the band-pass filter with enough accuracy to recover the clock from the correct channel without degrading the interference performance. Moreover, this temperature compensation technique applies also to the

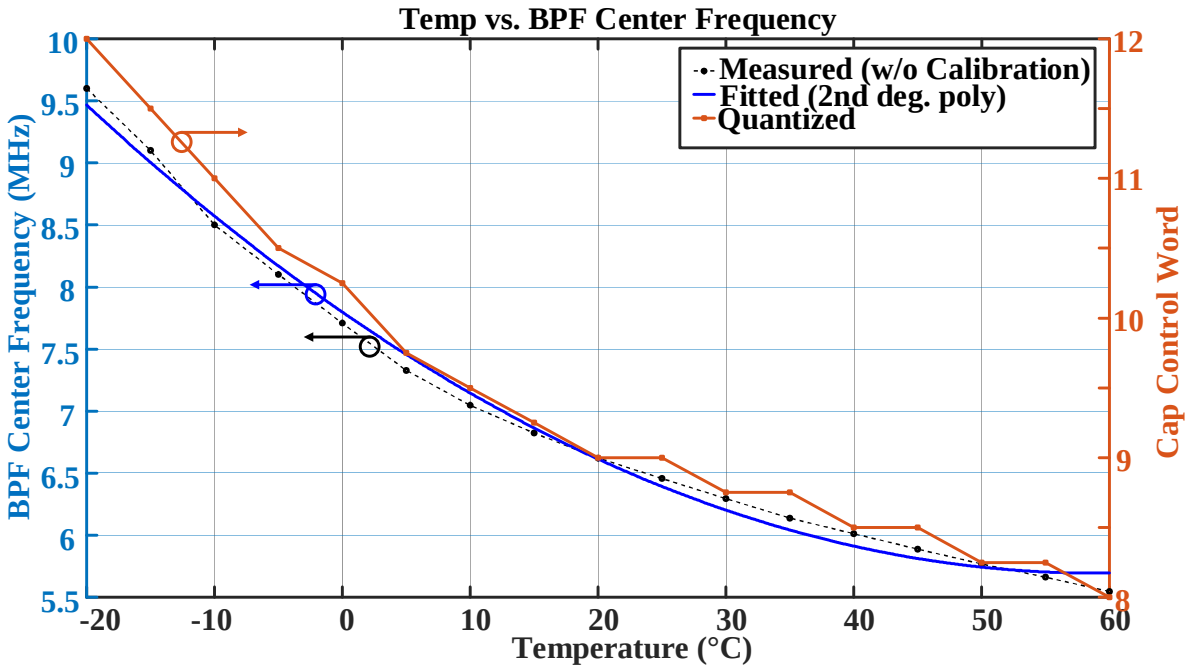


Fig.5.6. Fitted and Measured BPF center frequency shift with respect to temperature.

band-pass filter bandwidth as shown in Fig.5.7. Although the measured shift in the filter bandwidth is small (around 200kHz or 10% of the nominal bandwidth), which will not impact the basic functionality of the clock recovery or the PLL locking operation, it is still desired to calibrate the bandwidth of the filter to become closer to the nominal value to maintain the required adjacent channel rejection.

These results imply that with just a second order polynomial fitting and a temperature senor we can compensate for the temperature variations in both the LO and filter, which are the most critical blocks for clock recovery in our crystal-less operation. This is part of a one-time calibration step needed when a new chip is powered up to account for both process and temperature variations.

5.4 Circuits Implementation

5.4.1 Phased-Locked Loops (PLLs)

Fig.5.9 shows a simplified block diagram for both PLLs for reference recovery from the

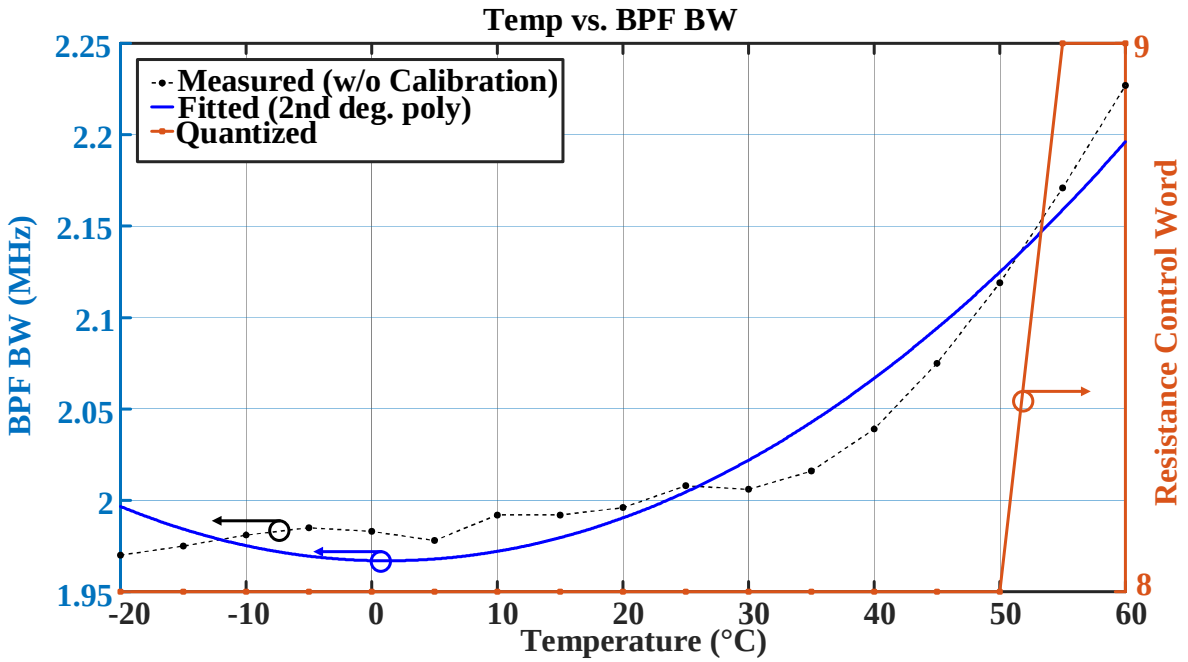


Fig.5.7. Fitted and Measured BPF bandwidth shift with respect to temperature.

BLE packet and TX transmission. It is a type-I ADPLL with an embedded averaging processing unit (APU) to calibrate the digital control word (DCW) while the PLL is locked. The APU is required because the 8MHz reference is a data-whitened, GFSK-modulated BLE packet, and the FM needs to be removed. The frequency accuracy increases with increasing averaging time, and with enough PLL cycles, the influence from GFSK modulation is minimized. The PLLs in the RX/TX paths are controlled by different frequency control words (FCW) and work at separate frequencies. This reduces mutual coupling between the 2 LOs and enables the TX to transmit in any channel.

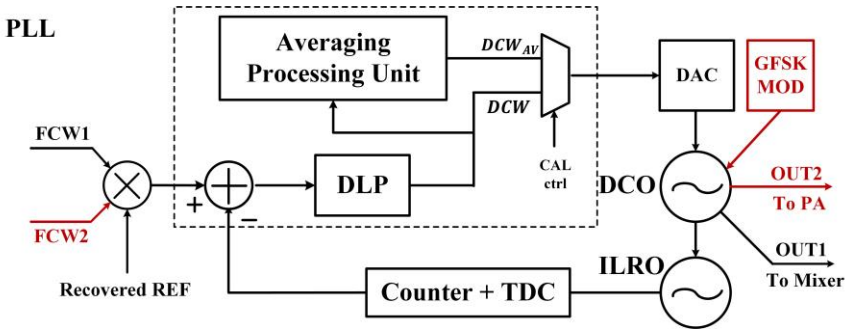


Fig.5.8. PLL block diagram.

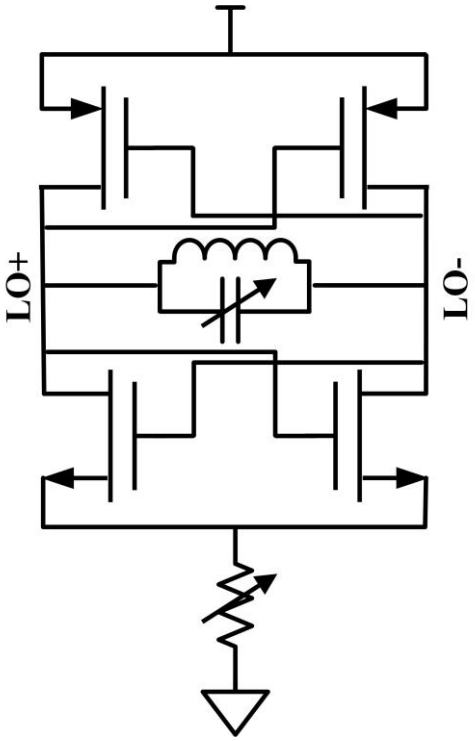


Fig.5.9. LC oscillator circuit.

5.4.2 LC Oscillators

The LC oscillator (Fig.5.9) uses both NMOS and PMOS cross-coupled pairs for negative resistance and a digitally tuned resistor tail, which helps keep the transistors out of triode and improves phase noise. The frequency of the LC oscillator is tuned through digitally-switched capacitor array. The overall frequency tuning range is 2300 to 2510 MHz with resolution of better than 20 kHz across the tuning range. This is achieved using ~300aF unit capacitors for fine tuning.

Such fine resolution not only ensures coverage of each BLE channel, but also enables this LC oscillator to be frequency modulated with smooth transitions between symbols using a Gaussian filter. This required specification in the BLE standard helps suppress the sidebands in the signal spectral power density and results in lower adjacent channel interference.

In order to be able to run the transmitter oscillator open-loop while transmitting a BLE packet, its frequency drift needs to stay within the standard specifications. As Fig.4.11 shows, the maximum oscillator frequency shift over a period of 16 hours in room temperature and using a typical power supply is less than the BLE specification of ±10ppm. In addition, the frequency drift is less than ±8ppm over a period of one second as in Fig.4.12, which can include multiple BLE advertising events. In the system presented in this chapter, the oscillator can be calibrated before transmitting any packet with minimal time gaps (as low as few micro-seconds). After calibration, the oscillator frequency drift will stay small enough for at least few hours if temperature is stable. When the temperature changes, it is sufficient to meet the system requirements for both LOs BPF by using a temperature senor with better than 0.3˚C resolution and second degree polynomial fitting (2-point calibration) as explained earlier.

5.4.3 Low-Noise Amplifier and Mixer

The RF front-end schematic is shown in Fig.5.10. The low noise amplifier utilizes a common-source narrow-band topology. As opposed to a mixer-first architecture, a LNA-first topology is used to achieve better noise performance, especially for the clock recovery path, since added noise by the circuits will directly increase the recovered clock jitter and will require longer averaging time in the PLL to filter out the excess noise as explained earlier. The receiver NF is optimized further with a gate inductor to control the LNA input impedance and optimize it for minimum NF. The output of the LNA is down-converted using a passive mixer as shown in

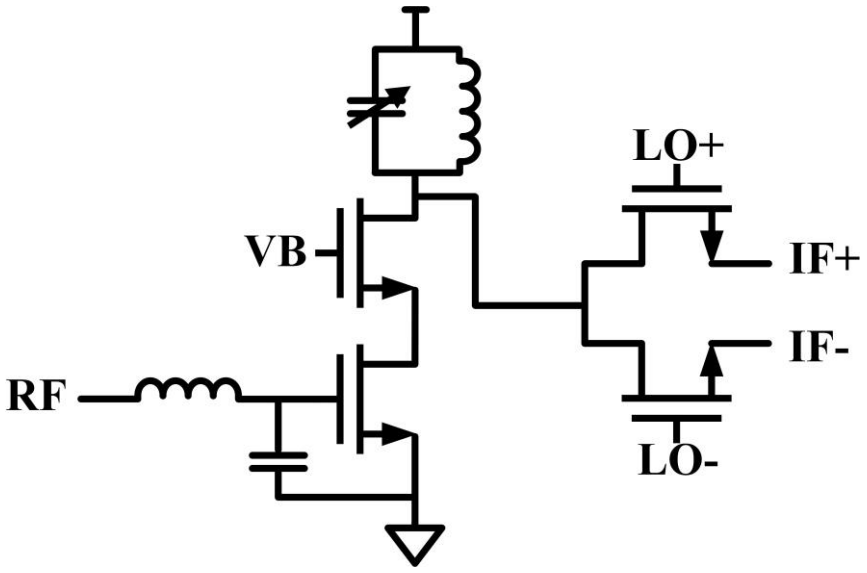


Fig.5.10. LNA and passive mixer circuit.

Fig.5.10. The mixer has differential outputs at baseband to enhance noise immunity at the baseband blocks down the signal chain.

Before feeding the recovered reference is fed into the PLLs, a digital glitch filter is used to clean the clock signal from short pulses (glitches) that might exist because of noise or unwanted signals bursts. The filer works by delaying any toggling on the clock signal by a programmable time interval (τ). If the clock signal switch its value and stays steady for a duration$\geq \tau$, the glitch filter will pass this change to its output. Otherwise, the change is considered to be an unwanted short pulse and is filtered out. Theses glitches are unwanted since they might affect the PLL locking time and introduce high switch activity (power) in the ADPLL which this clock signal is driving.

5.4.4 Band-pass Filter

The 6^{th} order active RC BPF is synthesized by cascading three 2^{nd} order biquads (Fig.5.11). Each biquad stage is fully differential using the Tow-Thomas topology for its lower sensitivity to parasitic. An active RC filter is used as opposed to a gm-C filter because of its superior linearity

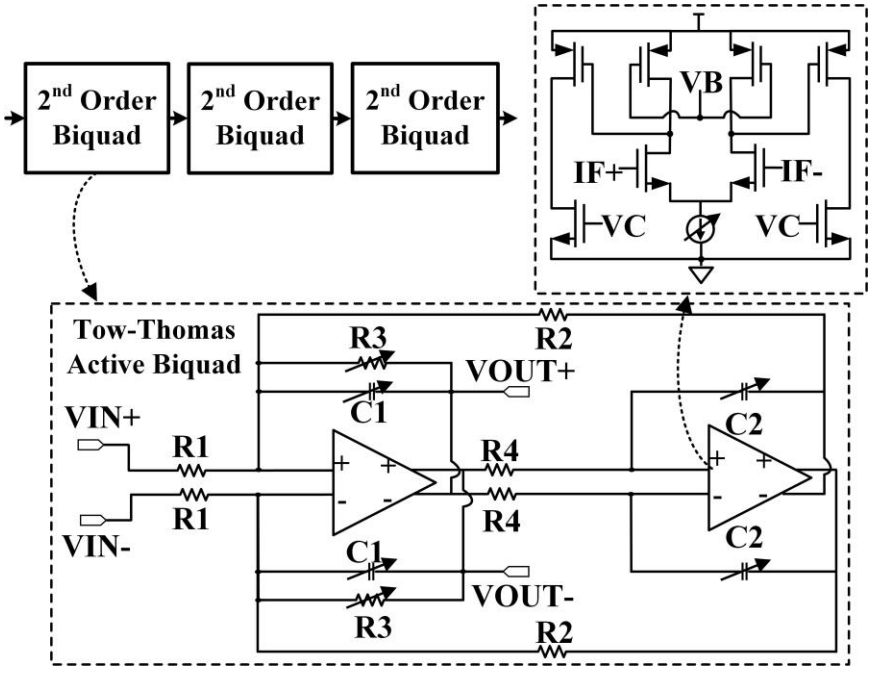


Fig.5.11. 6th Order Active RC BPF circuit (bias and CMFB are not shown).

since its first-order transfer function show that the filter center frequency and bandwidth is dependent on passive devices (resistors and capacitors), which are inherently linear, rather than active devices (transistors) in the gm-C topology. Each biquad stage will add two poles to the system which correspond to ±40dB/decade filter roll-off. Although higher order filter stages with more poles are possible, they are avoided in this design to maintain stability more reliably.

5.4.5 Analog Baseband for Back-channel Receiver Path

The baseband amplifier circuit is shown in Fig.5.12. It utilizes an inverter-based common source topology with resistive feedback for bias. This topology takes advantage of both NMOS and PMOS transconductance to boost the gain without power penalty. In addition, the bias feedback makes the amplifier less sensitive to bias offset.

Fig.5.13 shows the envelope-detector and integrator circuits used to rectify the baseband signals into DC. The integrator output, which will act as a low-pass filter, will be a slowly changing voltage that is proportional to the RF input level. The settling time of this detector has been designed to support the data rate specified by the received data, but without overdesigning so it

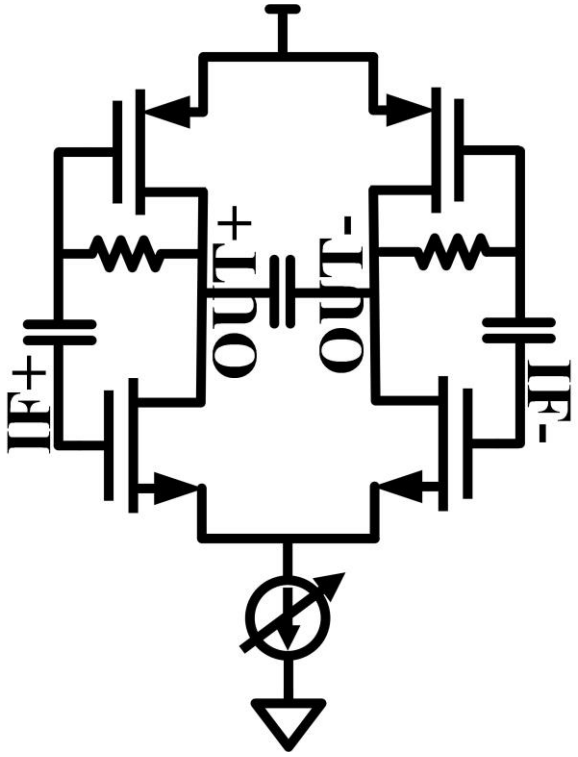


Fig.5.12. Baseband amplifier circuit.

doesn't consume high currents. The output of the integrator is then digitized using a one-bit comparator similar to the one shown in Fig.3.11(c).

5.4.6 Power Amplifier

In TX mode, a switched capacitor digital PA [77] improves efficiency at low power levels. This circuit architecture allows low power consumption while providing the needed output power set by the BLE standard. In addition, no on-chip inductors are needed for its operation which save silicon area (cost) and simply the design by eliminating any additional tuning circuits to compensate for PVT variations.

5.4.7 Digital baseband

A one bit comparator is used to quantize the received back-channel signals. Instead of using multi-bit analog-to-digital converter (ADC), the one comparator is used since the back-channel

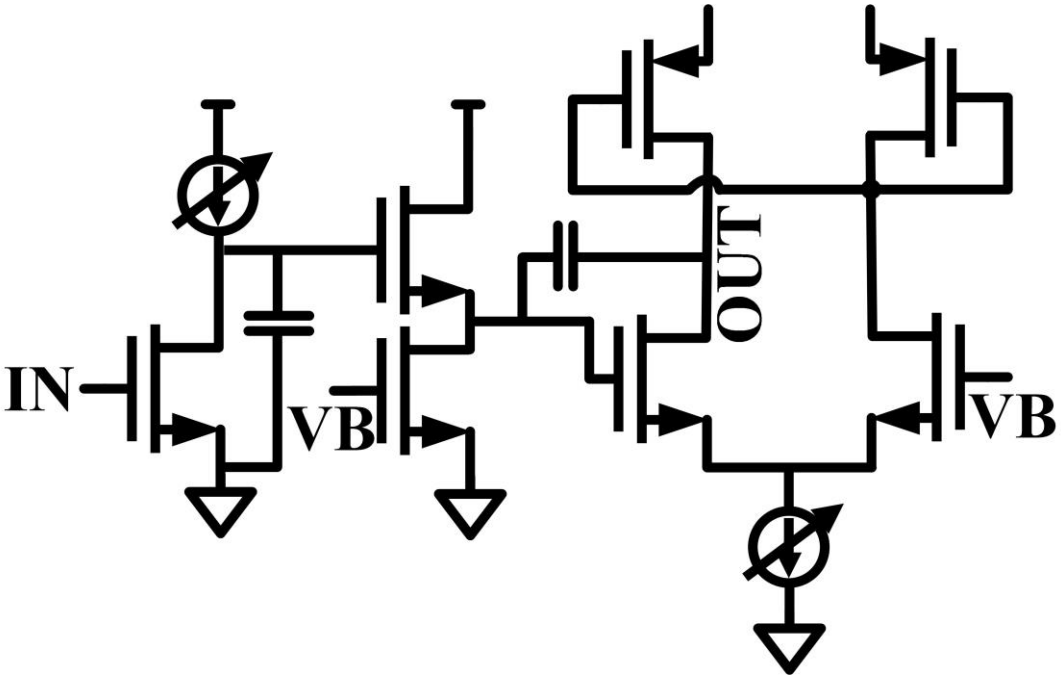


Fig.5.13. Envelope-detector and integrator circuits.

embedded message is encoded in whether or not energy is present on a specific channel during a predefined time interval. This will simplify the digital baseband since it will lower the amount of data to be processed. However, in order to correctly identify the beginning and end of each received packet with sufficient accuracy, the comparator sampling clock should be such that at least two samples are received during each packet. The oversampled comparator output is fully processed on-chip. The received data processing starts by scanning for the beginning of a valid BC message. As shown in Fig.5.3, the packet scanning start by looking for the 1st, 2nd and the beginning of the 3rd packet which combined constitutes one BLE advertising event. In the BC messages correlator, the bit sequence sampled by the comparator is correlated with pre-defined binary sequence templates representing potential BC symbols. The predefined BC message is identified from a specific pattern of BC messages with pseudo-random time gaps as specified by the BLE standard. A pseudo-random delay between advertising events helps avoid collisions, but it complicates BC messages detection. To address this challenge, each new valid BC packet which

is part of the predefined BC message is stored in a new array in the BC correlator, since it could potentially be part of a valid BC message. Simultaneously, any previously received packet(s) which could have the new packet as the next part of its BC message, based on the predefined pattern (template), will get updated by adding the new packet to the received messages sequence. For this update to happen, the difference between the time stamps of the new and previous packet has to be within the allowed time gaps set by the BLE specifications, which include the pseudo-random delay as defined in the standard. Additionally, the time stamp gets updated every time a new packet is added to the received message sequence. During this detection phase, the receiver oscillator frequency is hopped between the BLE advertising events such that it can cover all three channel at least twice during a one packet duration. Once a complete BC message is received with the BC correlator coefficients above the programmable threshold, the PLL is enabled. In this detection phase, the frequency controller freezes the receiver oscillator frequency such that the IF frequency is 8MHz to properly recover the clock reference frequency. When the PLLs lock to the recovered clock reference, the controller will disable them and enable the GFSK modulator, after a programmable delay, to transmit one or more BLE packets.

5.5 Measurement Results

The transceiver was fabricated in a 40nm CMOS process. The measured sensitivity is -86dBm and -94dBm at a BER of 10^{-3} for the BC and clock recovery paths, respectively (Fig.5.14 and Fig.5.15). Thus, the system sensitivity is limited by the clock recovery path. The SIR when receiving back-channel messages (Fig.5.16) was measured to be -18dB, -51dB, and <-60dB for the 1^{st}, 5^{th}, and 10^{th} adjacent channels, respectively, meeting the BLE specifications for blocker rejection. The SIR when recovering a reference clock is -20dB and <-60dB for the 1^{st} and 2^{nd} adjacent channels, respectively, as a result of the sharp roll off in the BPF frequency response

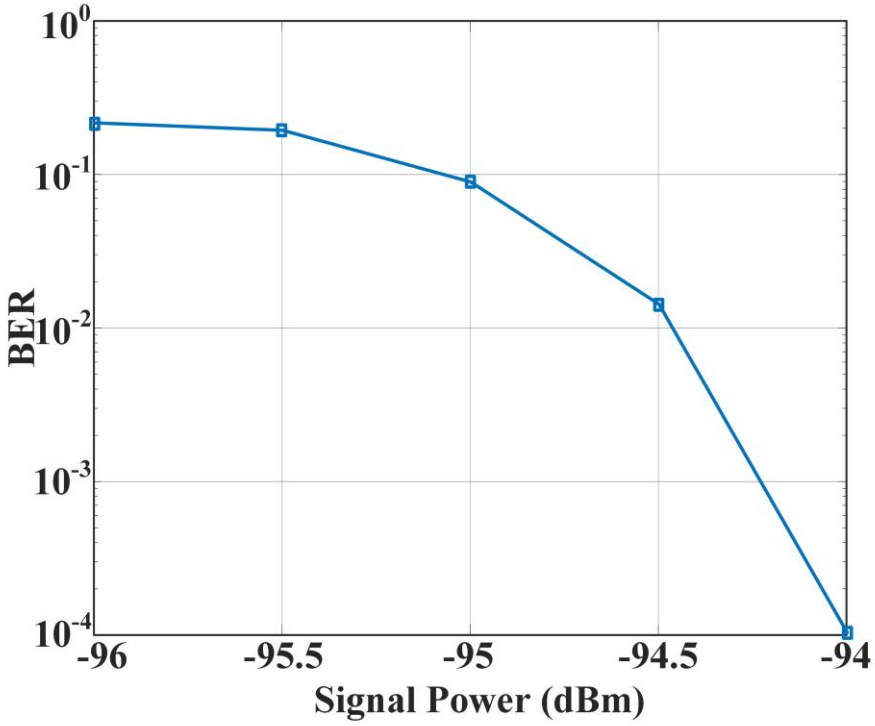


Fig.5.14. Measurement results: BC receiver BER vs. signal power.

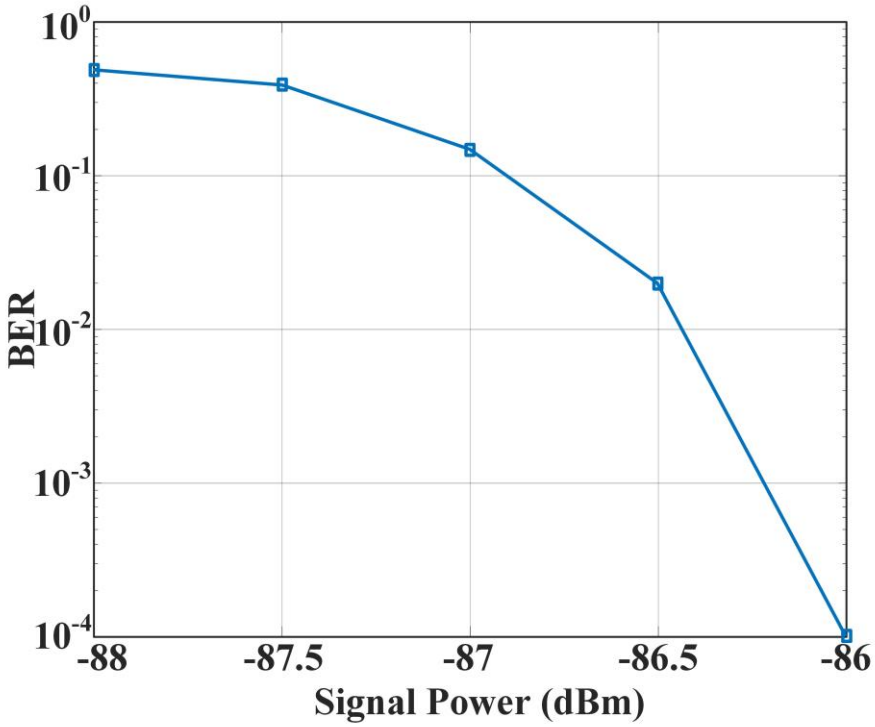


Fig.5.15. Measurement results: clock recovery receiver BER vs. signal power.

(Fig.5.17). The interference rejection performance is measured with a wanted signal 3dB over the

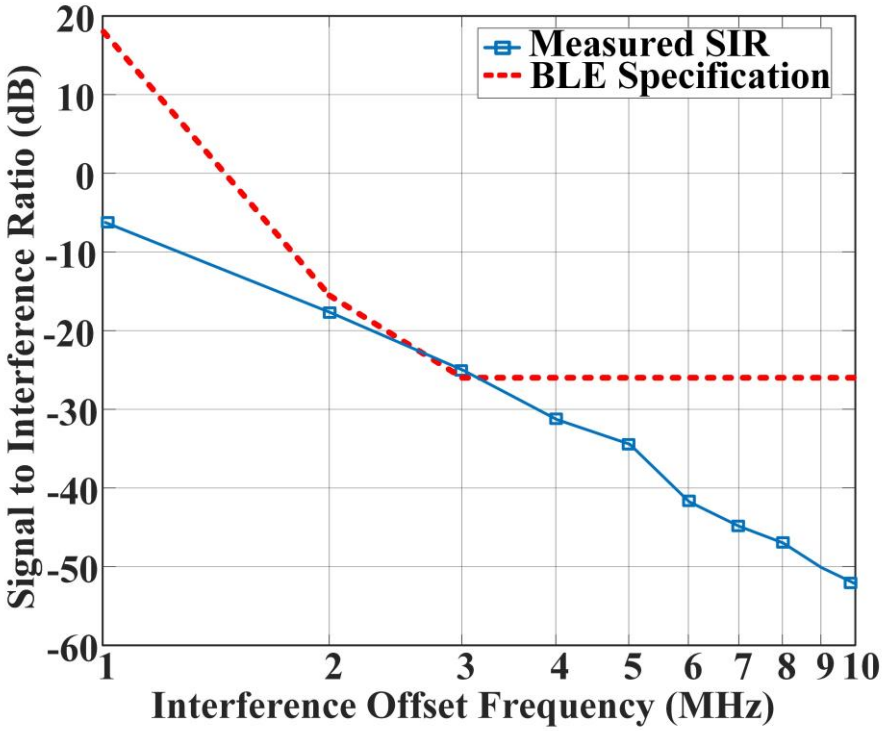


Fig.5.16. Measurement results: signal-to interference ratio vs. interference offset frequency.

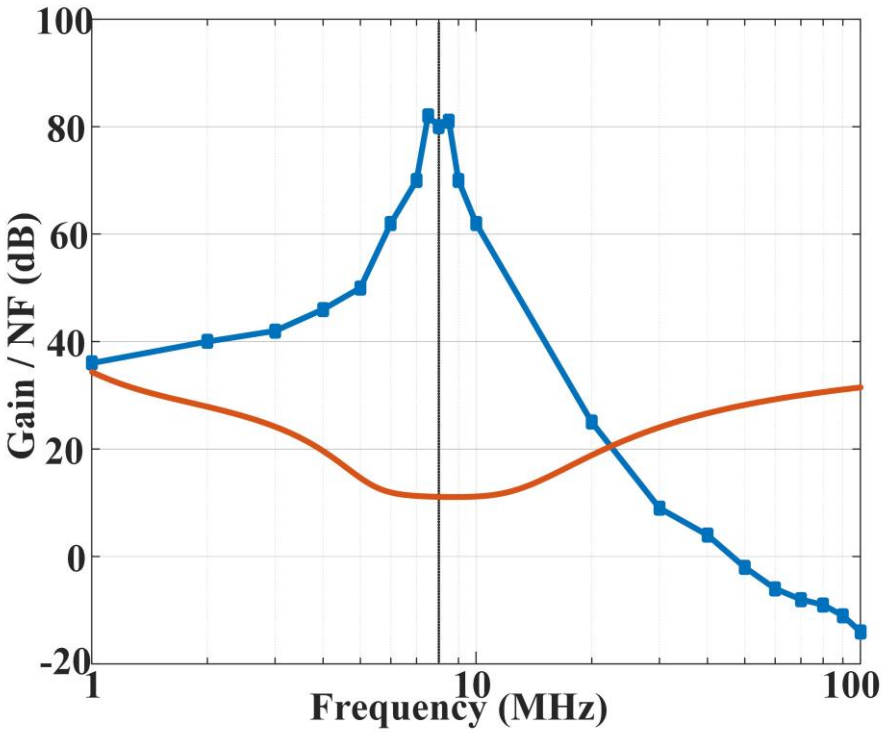


Fig.5.17. Measurement results: RF front-end + NF gain and NF.

reference sensitivity level where both the wanted and interferer signals are GFSK modulated as

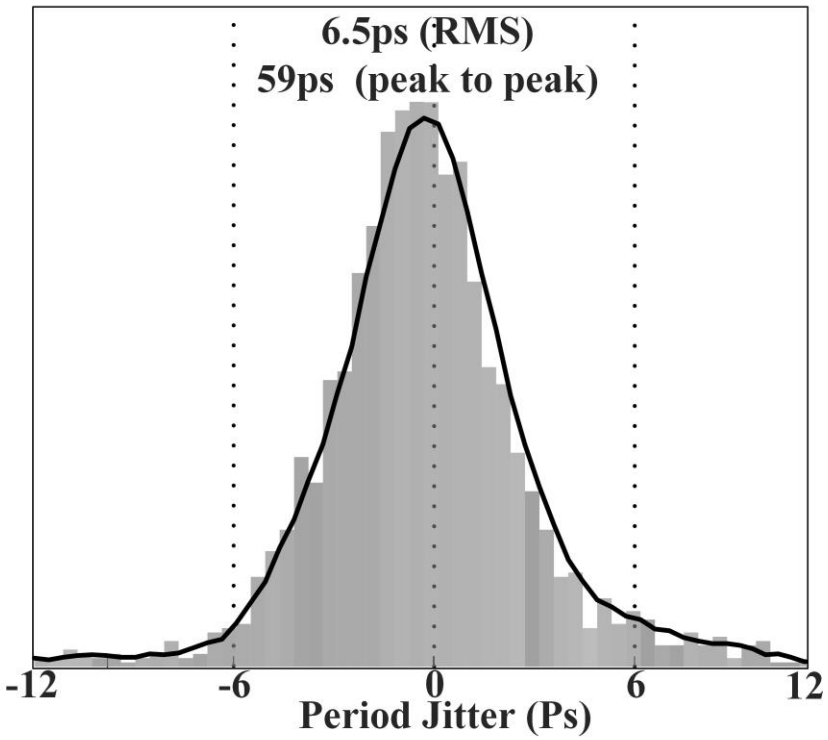


Fig.5.18. Measurement results: received 8 MHz clock jitter.

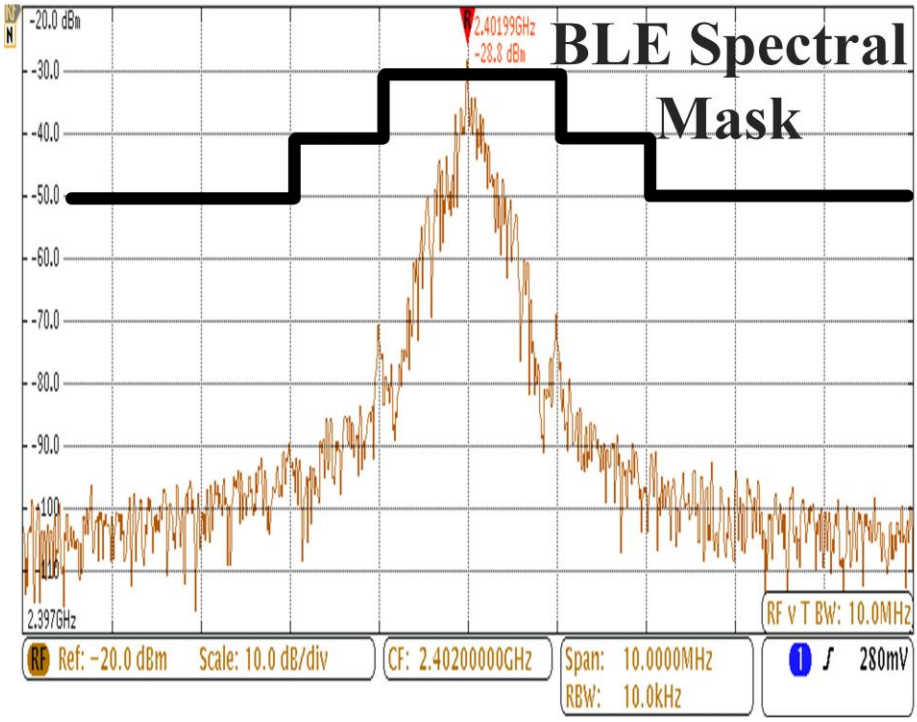


Fig.5.19. Measurement results: TX output spectrum.

defined in the BLE standard.

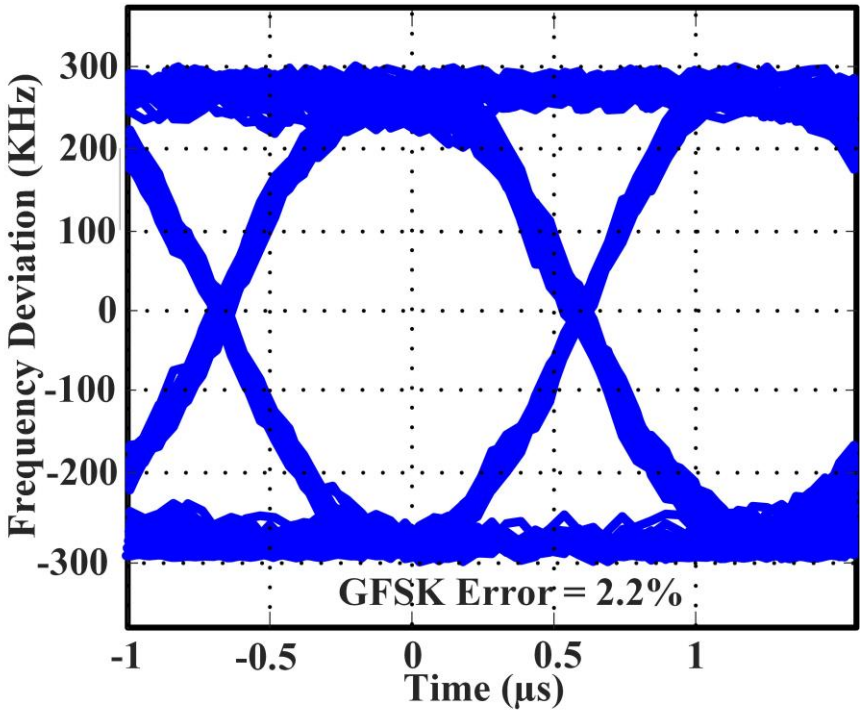


Fig.5.20. Measurement results: eye diagram.

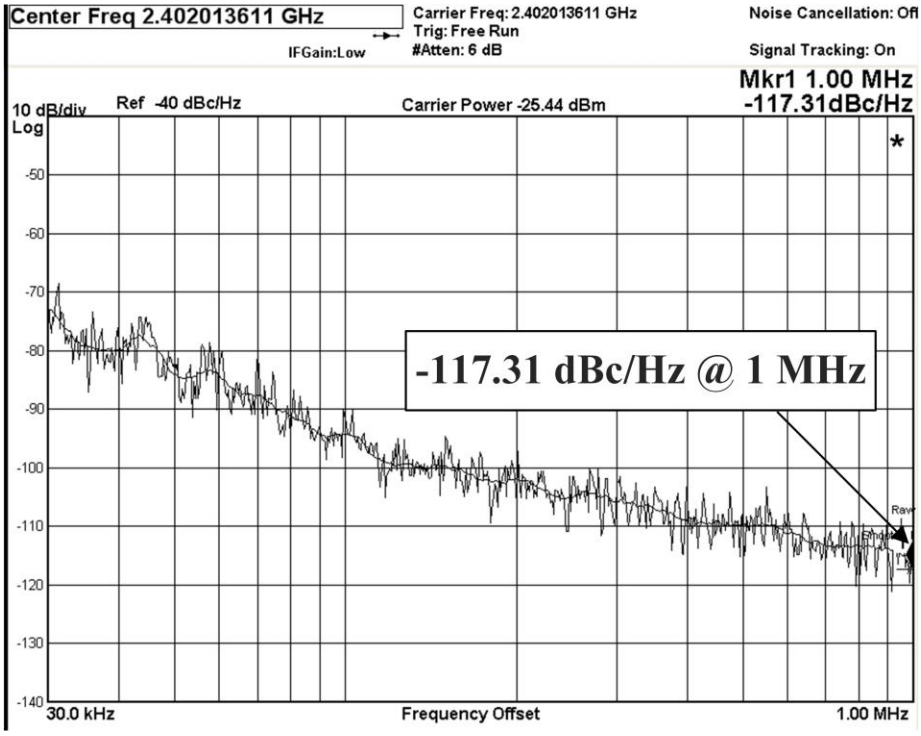


Fig.5.21. Measurement results: phase noise.

The NF of the clock recovery path is less than 12dB (Fig.5.17). This is critical to minimize

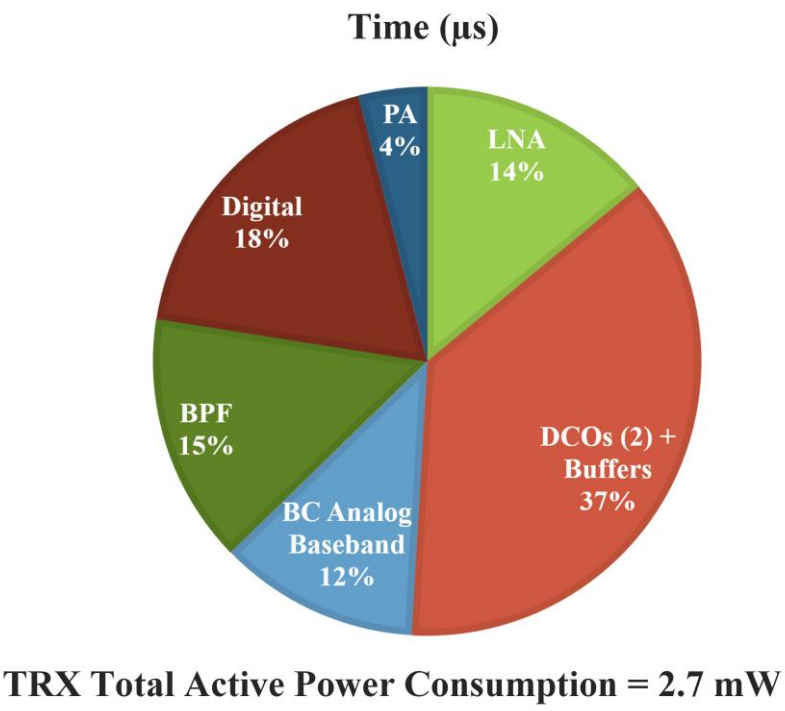


Fig.5.22. Measurement results: transceiver power breakdown.

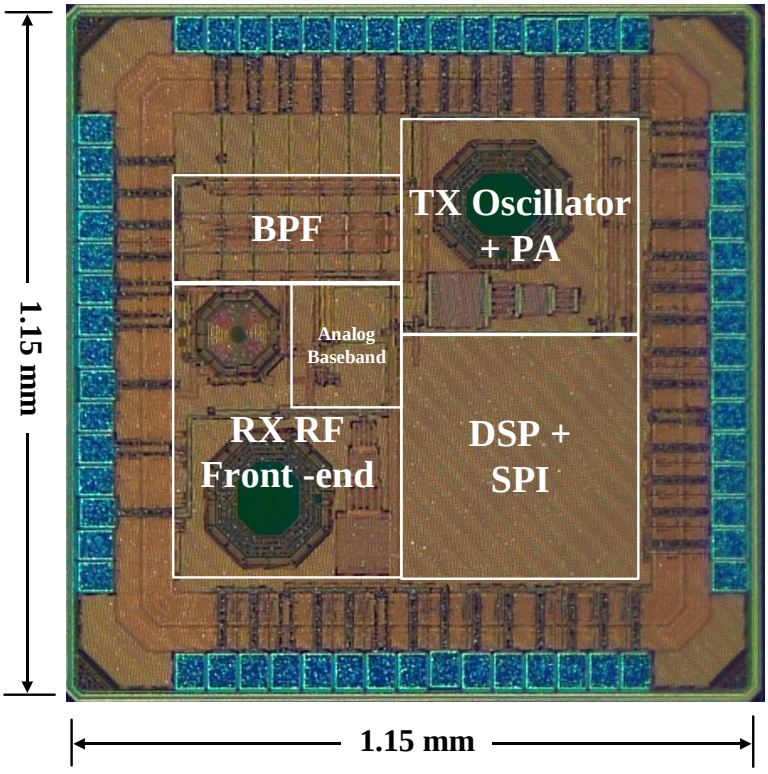


Fig.5.23. Die micrograph.

the RMS jitter in the recovered clock, which is measured at 6.5ps (Fig.5.18) and is comparable to

crystal oscillators operating at similar frequencies. The GFSK TX output spectrum is shown in Fig.5.19 along with the BLE spectral mask. The measured eye diagram of the TX output packet is shown in Fig.5.20, where the clock driving the GFSK modulator is divided down from open-loop RX LO_1. The free running LC oscillator archives -117dBc/Hz phase noise at 1MHz offset (Fig.5.21). The overall power breakdown of the TRX shows that the RF LOs and buffers consume the highest power percentage (37%) of the total active power of 2.7mW (Fig.5.22).

Table 5-1 shows a comparison between this work and state-of-the-art. This is the first reported symmetric crystal-less transceiver, where both the received and transmitted messages are compliant with the same communication standard (BLE). This work has the fastest reported frequency calibration time of all crystal-less radios. It outperforms previous designs in interference rejection through high-Q filtering and by enabling PLLs only after detecting a valid ADV event when a BLE packet is known to be present. Fig.5.23 shows the die photo of the chip, which has an

Table 5-1 PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF ART.

		This Work		VLSI 2019 [75]	VLSI 2019 [73]	TCAS-I 2012 [74]
		TX	RX			
Active Power [mW]	Analog	0.6	1.6	1.877	3.9	20.4
	Digital	0.5				
RF Frequency [MHz]		2402-2480	2402-2480	2400	2400	2400
Voltage Supply		0.9/1		1.5	1.3-1.6	1.8
Sensitivity		N/A	-86	-83.5	N/A	-65
Modulation		GFSK	BC-FSK	GFSK(TX)/ OQPSK(RX)	GFSK	QPSK
Die Area		1.33		3.06	N/A	2.7
BLE Compatible Frequency		YES		No	No	No
Adjacent Channel SIR (dB) @		N/A	-18/-24	N/A	N/A	N/A
Channel Selectivity		N/A	Yes	Yes	N/A	No
Technology		40		65	65	180
Frequency Calibration Method		Received BLE Packet		Received 802.15.4 Packet	FBAR	Received QPSK Signal
Frequency Locking Time		< 100		N/A	N/A	800000
Comm. Standard (TX/RX)		BLE/ BC-BLE		BLE/ 802.15.4	BLE/ N/A	No/ N/A
Fully Integrated		Yes		Yes	No	No

area of 1.33mm^2.

5.6 Conclusion

A crystal-less BLE transmitter with back-channel receiver fabricated in CMOS 40nm is presented in this chapter. The receivers can decode messages embedded in advertising events sent by commercial BLE devices. Once an advertising event is detected, the RX clock recovery path is enabled and the extracted clock is used to calibrate the LO frequency using two APU assisted PLLs. After calibrating the LO frequency, the transmitter sends a programmable BLE packet on any BLE channel. The receiver meets the interference rejection requirements specified in the BLE standard. The transceiver consumes 2.7 mW with a sensitivity of -86 dBm.

This work is done collaboratively with my colleagues Xing Chen and Yao Shi. Xing wrote the PLL code. Yao designed the oscillator.

Chapter 6. Conclusion

6.1 Summary

With the coming of age of the Internet of Things (IoT), demand on ultra-low power radios will continue to boost tremendously. Circuit imperfections, especially in power hungry blocks, i.e. the local oscillators (LO) and band pass filters (BPFs), pose a real challenge for ultra-low power (ULP) radios designers considering their tight power budget. Chapter 2 presents an investigation on the effects of circuit non-idealities on the bit-error rate (BER) performance of On-off keying (OOK) and Gaussian Frequency-shift Keying (GFSK) energy detection-based wakeup radios. In particular, it analyzes the impact of phase noise and frequency offset in the LO, BPFs bandwidth and roll-off, noise figure (NF) on ULP receivers' performance. This contributes to the ongoing research in designing ULP wireless nodes by demonstrating the tradeoffs between these non-idealities and the receiver's sensitivity level and selectivity and show some design guidelines for energy detection (ED) based ULP radios.

Chapter 3 presents two prototypes of low power back-channel Bluetooth Low-Energy (BLE) wake-up receivers. The receivers scan the BLE advertising channels for modulated advertising channel patterns by hopping the local oscillator (LO) frequency. The back-channel message is modulated in the sequence of the three advertising channels in each advertising event. This makes the wake-up via back-channel messaging compatible with the BLE standard, so it can be generated by a commercial off-the-shelf device. The first proposed receiver uses a dual-mixer to down-convert the RF input to reduce the ring based local oscillator (LO) power consumption by operating it at half the RF frequency. The second prototype aims to achieve faster channel

hopping using a more stable and lower noise LC based oscillator. The receivers have -57.5/-82.2 dBm sensitivity while consuming 150 µW/1.2 mW.

In Chapter 4, an LC oscillator is modeled and fabricated in CMOS 40nm and its frequency accuracy is analyzed over process, supply voltage, and temperature (PVT) variations and over time. Performance is compared to the BLE specification as an example application commonly targeted by ultra-low power (ULP) radios. When the temperature coefficient (TC) of the coil loss is precisely modeled, the simulation results are close enough to the measurements for analysing the oscillator open-loop performance across voltage and temperature variations. The results show that frequency calibration for each chip is required to compensate for process and temperature variations in order to be able to run the oscillator open-loop and still comply with the BLE standard. When the temperature is stable, the frequency shift in the free running LC oscillator is measured to be less than ± 10ppm over a period of 16 hours, which meets the BLE specification.

A crystal-less BLE transmitter and back-channel receiver with over-the-air clock recovery is presented in Chapter 5. The transceiver calibrates its local oscillators from a received BLE packet, which is detected using the back-channel receiver, and meets the clock accuracy and interference rejection ratios specified in the BLE standard. The receiver has a -86dBm sensitivity and adjacent channel interference rejection of 18dB. The two PLLs lock in less than a combined 100µs using the 8MHz recovered reference.

6.2 Applications for Presented ULP and Crystal-less Radios

One interesting application of the back-channel receiver is to use it in a BLE fitness tracking device. It can be utilized as either a main radio for low data-rate communication or to wake-up another higher power radio which supports higher data-rates. These types of devices can help monitor critical physiological parameters. Beyond sensing, the node can be used to interpret

the data and alert the user if any abnormality is detected which will result in less data transmitted over-the-air. This allows for duty-cycling the radio to reduce the average power which will increase the battery lifetime significantly as shown in Table 6-1. The table shows that the presented 150 µW BC receiver can run on a single battery with 1% duty-cycling for more than 10 years, which is longer than the typical lifetime of personal heath tracking devices.

On the other hand, the presented crystal-less transceiver, doesn't require any off-chip components (Table 6-1), which makes it a good candidate for connecting disposal medical devices though BLE. It will not only eliminate the additional cost and power consumption of the crystal, but also its volume. This enables a fully-integrated and small factor true single-chip solution. Although this system has lower battery lifetime compared with low-power back-channel receivers, it can support much higher data-rates (up to 2Mbps) by using it as ADPLL based receiver also which allows for more sleep time and smaller duty-cycling rate.

Table 6-1 APPLICATIONS EXAMPLE SUMMARY.

		0.15mW BC Rx	1.2mW BC Rx	Crystal-less TRX
Power [mW]	Active	0.15	1.2	2.7
	Sleep	0.001		
RF Frequency [MHz]		2402-2480		
Range* [m]		8	200	200
Die Area [mm^2]		1.1	1	1.33
Off-chip Components		Matching network + crystal	Matching network + crystal	None
Interference Rejection		Moderate	Good	Excellent
Comm. Standard		BC-BLE	BC-BLE	BLE/ BC-BLE
Battery Lifetime** [Years] (1% duty-cycling)		> 20	5.7	2.65

*Assuming 0dBm TX and free space path loss. **Assuming a typical coin battery capacity of 650mWhr.

6.3 Future Directions

In order to further reduce the power consumption of radios compliant with adopted communication standards, such as: BLE, additional innovation on the circuit and system level can be introduced. A potential candidate to enhance the current state-of-art performance is the low power zero-IF BLE receiver which has its top-level block diagram shown in Fig.6.1. A direct-conversion topology is used to eliminate the image frequency which exists in all other higher intermediate frequencies. Although this will necessitate using two signal phases with ninety degrees phase difference to be able to demodulate BLE packets, it results in net power saving by removing the more power hungry traditional image rejection filter. Furthermore, a passive mixer-first RF front-end is used since utilizing a LNA will lead to higher power consumption than the targeted sub-300μW budget. In order to achieve such a remarkably low power consumption, a number of power reduction techniques have been adopted in the design of this receiver which will be explained in detail the remainder of this section.

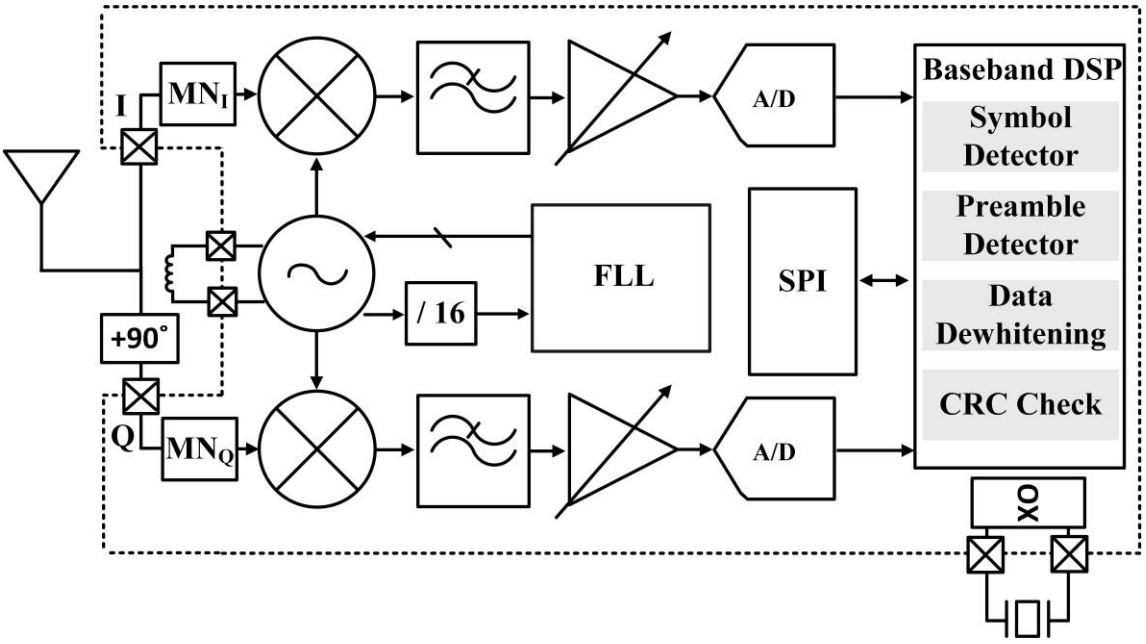


Fig.6.1. Block diagram of the zero-IF BLE receiver.

First, the ninety degrees phase shift is introduced by splitting the received RF signal into two paths off-chip and using a longer transmission line trace for one of signal paths. The additional trace length corresponds to a $\frac{\pi}{4}$ phase shift at the frequency of operation for the BLE standard (2.4GHz). Since the demodulator can tolerate few degrees of phase mismatch between the two signal phases, this design can be used to cover the complete BLE band (2.402GHz -2.480GHz) without any additional tuning for each specific channel. This method helps in avoiding designing a significantly higher power quadrature oscillator local oscillator.

Second, a high-Q off-chip inductor is used to reduce the required active transconductance in the LC oscillator, and therefore, its power consumption. Since the oscillator circuit dominates the power consumption of the receiver, this technique will reduce the system overall power significantly.

Third, and to calibrate the oscillator frequency, a simpler counter based frequency locked loop (FLL) is used to maintain the frequency to be within the BLE specification. A more traditional PLL would require much higher power without gaining any significant improvement in the receiver performance.

This work is being developed with my colleagues Omar Abdelatty (chip lead) and Yaswanth Kumar. To the author's best knowledge, these techniques could help achieve the lowest reported BLE receiver power which include processing the received packet for the data dewhitening and CRC check.

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