IET Electrical Systems in Transportation

Research Article

IET Journals
The Institution of Engineering and Technology

SiC + Si three-phase 48 V electric vehicle battery charger employing current-SVPWM controlled SWISS AC/DC and variable-DC-bus DC/DC converters

ISSN 2042-9738
Received on 9th October 2017
Revised 12th February 2018
Accepted on 19th March 2018
E-First on 24th April 2018
doi: 10.1049/iet-est.2017.0083
www.ietdl.org

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Abstract: Wide-bandgap (WBG) devices such as SiC and GaN switches are regarded as next-generation power semiconductors, due to their superior performance over conventional Si devices, for instance, a low switching loss and high thermal conductivity. Its bottleneck, however, is the high cost, which is critical for renewable energy and automotive industries. This study adopts SWISS AC/DC rectifier topology for the three-phase 380–480 VAC along with an isolated DC/DC converter, indicating such topology can maximise the advantages of Si (low conduction loss) and SiC (high switching loss), altogether thereby yielding the high performance and low cost. A novel space-vector pulse width modulation (SVPWM) was proposed to control such a current-source power factor correction, where only two SiC devices were adopted for the DC-bus voltage control. The closed-loop control of the grid current is realised for the unity power factor. Such topology further allows the DC-bus voltage to be varied with the output voltage, thereby minimising the system loss. A final prototype was built to charge a 48 V battery at 11 kW. Experimental results validated the effectiveness of such battery charger design.

1 Introduction

With electric vehicles (EVs) becoming popular, a growing interest in high power density and high-efficiency battery chargers exhibits. A conventional design approach is the power factor correction (PFC) controller + an isolated DC/DC [1–4], as shown in Fig. 1 for the single-phase design and Fig. 2 for the three-phase design. An AC/DC part converts the grid voltage to the DC voltage and realises the PFC, a DC/AC part transforms the DC to a high-frequency AC on the primary side of the transformer, and another AC/DC part rectifies the induced high-frequency AC to a DC for the battery charging. Given that the grid-side AC/DC is a boost-type converter, the DC-bus voltage needs be higher than the grid peak voltage.

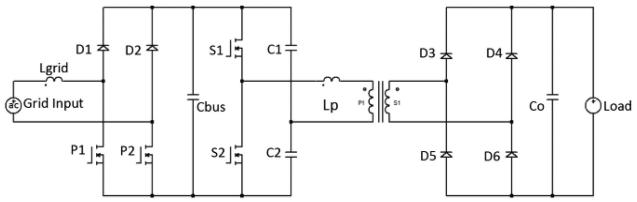

Fig. 1 *Conventional single-phase isolated charger*

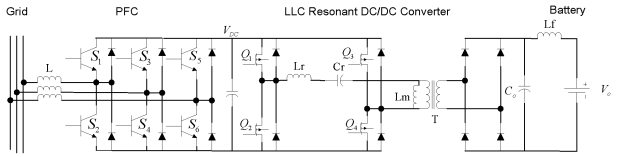

Fig. 2 *Conventional three-phase isolated charger*

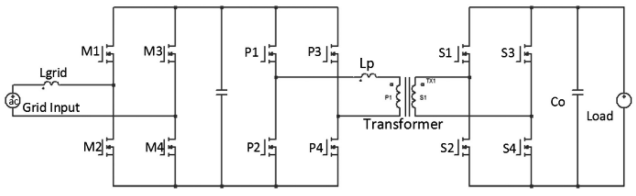

Fig. 3 *Charger topology used in [6]*

Such a boost-type PFC faces the challenge when the input is three-phase 380–480 VAC. The DC-bus voltage needs be boosted to 600 V or higher, yielding a bulky DC-bus capacitor, a high insulation requirement, and high-voltage rating switches, e.g. 1200 V, which usually have much higher switching and conduction loss than 600 V devices. One possible solution is to use three single-phase chargers to form one three-phase charger. Each single-phase module could adopt either the conventional design like Fig. 1 or other novel topology, e.g. a single-phase bidirectional isolated zero voltage switching (ZVS) AC–DC converter proposed in [5]. Such a topology merges two stages (PFC + DC/AC) into one stage, thereby eliminating the bulky DC-bus capacitor. To avoid back-to-back switches, Everts *et al*. [6] further utilise a topology shown in Fig. 3, where the front-end rectifier stage (M_1–M_4) operates at the grid frequency simply converting the sinusoidal waveform into a double-line-frequency single-polarity DC voltage. The dual active bridge (DAB) stage (P_1–P_4, S_1–S_4) takes care of the power factor and power delivery altogether. Even though such topology has a double-line-frequency output current ripple, such ripple could be eliminated once three single-phase modules together form a three-phase charger, as shown in Fig. 4. However, its cost is a major concern due to large amount of switches.

Consider the charging application for 48 V electric carts in the airport transportation. Such a charger is a typical off-board type, which has less space requirement than on-board chargers, however, is very cost sensitive. When receiving three-phase 380–480 VAC, we propose to employ a buck-type rectifier named as SWISS rectifier [7] along with a DAB [8, 9] to form the overall charger, as shown in Fig. 5.

Even though the grid-side AC/DC employs six diodes and three back-to-back connected switches, all these switches/diodes commutate the current at very low frequency, e.g. grid frequency, making the regular low-conduction-loss Si insulated gate bipolar transistor (IGBT) as a qualified candidate. A high switching frequency is only demanded for S_h and S_l to reduce the size of the DC-bus inductor and capacitor, where wide-bandgap (WBG) semiconductor devices such as SiC MOSFETs and GaN HEMTs are perfect candidates [10, 11]. The topology shown in Fig. 5

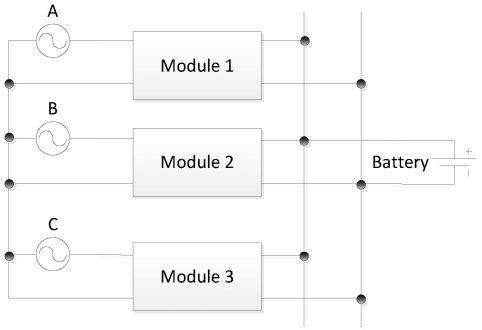

Fig. 4 *Three-phase charger using single-phase modules*

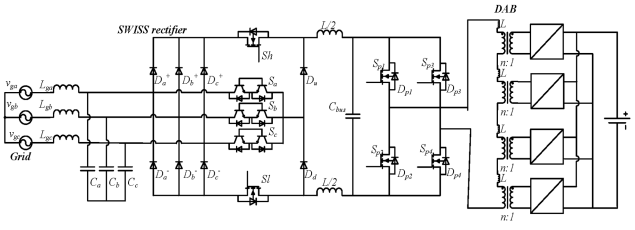

Fig. 5 *Proposed 11 kW/48 V battery charger for airport transportation*

reduces the amount of SiC MOSFETs, positioning such design a cost-effective approach. Furthermore, by lowering the DC-bus voltage to ∼400 V, such topology allows 650 V Si/SiC to be used for S_{p1}–S_{p4} with a 400 V transformer. To facilitate the transformer design and assembly, this paper adopts the matrix transformers at the DAB stage. To charge a 48 V battery pack, each transformer has the turn ratio of 100:48 V. At last, secondary-side switches undertake the low voltage (24–72VDC) and high current (∼160 A), making conventional Si MOSFETs a perfect candidate.

To realise the unity power factor, Section 2 proposes a space-vector pulse width modulation (SVPWM) control for the PFC part, with current closed-loop control, which will enhance the dynamic response and control accuracy. In Section 3, a variable DC-bus voltage control was proposed for the DAB stage to deal with the challenges of the wide-output voltage range, e.g. 24 V–72 VDC for the battery pack. Compared to others using multiple phase shifts or variable switching frequency (VSF) [12–14], such control is easy to implement, facilitates the realisation of the soft switching of all DC/DC switches within the whole-power/voltage range, and minimises the system loss at the ultra-low power [15]. Section 4 is the experimental validation. Section 5 is the conclusion.

2 Current SVPWM for power factor correction

Different from the conventional three-phase two-level voltage-source inverter (VSI) using SVPWM control, where only six switches are employed with eight voltage vectors, the SWISS PFC topology is a current-type converter using eight active switches. Current space vectors need be defined accordingly.

Define switching states as (S_a S_b S_c, S_h S_l). Here, $S_i = 1$ ($i = a, b, c, h, l$) means the switch is on and $S_i = 0$ means off. To avoid any potential short circuit of the grid side, at any moment only one of the three switches (S_a S_b S_c) is on, i.e. $S_a + S_b + S_c = 1$.

Assume the three-phase voltage is

$$\begin{Bmatrix} v_a \\ v_b \\ v_c \end{Bmatrix} = \begin{Bmatrix} V_m \sin[\omega * t] \\ V_m \sin\left[\omega * t - \frac{2\pi}{3}\right] \\ V_m \sin\left[\omega * t + \frac{2\pi}{3}\right] \end{Bmatrix} \tag{1}$$

To realise the unity power factor, all the grid current need be aligned with the voltage, i.e.

$$\begin{Bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{Bmatrix}_{\text{ref}} = \begin{Bmatrix} I_m \sin[\omega * t] \\ I_m \sin\left[\omega * t - \frac{2\pi}{3}\right] \\ I_m \sin\left[\omega * t + \frac{2\pi}{3}\right] \end{Bmatrix}_{\text{ref}} \tag{2}$$

Now converting the three-phase current to the α–β coordinate

$$\begin{Bmatrix} i_\alpha \\ i_\beta \end{Bmatrix} = T_{abc/\alpha\beta} \begin{Bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{Bmatrix}, \quad \text{here } T_{abc/\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3}$$

Furthermore

$$\begin{Bmatrix} i_\alpha \\ i_\beta \end{Bmatrix}_{\text{ref}} = T_{abc/\alpha\beta} \begin{Bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{Bmatrix}_{\text{ref}} = \begin{Bmatrix} \sqrt{\frac{3}{2}} I_m \sin(\omega t) \\ -\sqrt{\frac{3}{2}} I_m \cos(\omega t) \end{Bmatrix} = \rho \cdot e^{j\theta} = \sqrt{\frac{3}{2}} I_m e^{j(\omega t - (\pi/2))} \tag{4}$$

Equation (4) forms the current reference vector. For the specific angle ωt, all feasible switching states are listed in Table 1. Take $90° < \omega t < 120°$ as an example. Here, S_b is on, while S_a and S_c remain off. Switching states are determined by S_h and S_l, i.e. (010, 11), (010, 10), (010, 01), and (010, 00). If we select (010, 11), both S_h and S_l are on, resulting in $i_{ra} = I_{\text{dc}}$, $i_{rb} = 0$, $i_{rc} = -I_{\text{dc}}$. Therefore

$$\begin{Bmatrix} i_\alpha \\ i_\beta \end{Bmatrix} = T_{abc/\alpha\beta} \begin{Bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{Bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{Bmatrix} I_{\text{dc}} \\ 0 \\ -I_{\text{dc}} \end{Bmatrix} = \begin{Bmatrix} \sqrt{\frac{3}{2}} I_{\text{dc}} \\ \frac{1}{\sqrt{2}} I_{\text{dc}} \end{Bmatrix} = \sqrt{2} I_{\text{dc}} e^{j(\pi/6)}$$

When (010, 10) is selected, S_h is on and S_l is off. Therefore, $i_{ra} = I_{\text{dc}}$, $i_{rb} = -I_{\text{dc}}$, $i_{rc} = 0$, i.e.

$$\begin{Bmatrix} i_\alpha \\ i_\beta \end{Bmatrix} = T_{abc/\alpha\beta} \begin{Bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{Bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{Bmatrix} I_{\text{dc}} \\ -I_{\text{dc}} \\ 0 \end{Bmatrix} = \begin{Bmatrix} \sqrt{\frac{3}{2}} I_{\text{dc}} \\ -\frac{1}{\sqrt{2}} I_{\text{dc}} \end{Bmatrix} = \sqrt{2} I_{\text{dc}} e^{j(-(\pi/6))}$$

Similarly, (010, 01) results in $\begin{Bmatrix} i_\alpha \\ i_\beta \end{Bmatrix} = \sqrt{2} I_{\text{dc}} e^{j((\pi/2))}$ and (010, 00) will result in $\begin{Bmatrix} i_\alpha \\ i_\beta \end{Bmatrix} = 0$. Given the fact we have overall 12 sectors, one sector per 30°, there are 4*12 = 48 switch states in total. By eliminating redundancies, 24 independent space vectors are left.

Still take the sector ($90° < \omega t < 120°$) as an example. Among four switch states, only three of them are used to realise the unity PFC, i.e. (010, 10), (010, 11), and (010, 00). All switching states and their converted current vectors are shown in Fig. 6*a*. Since the DC-bus inductor is acting as the current source and the goal is to control the current of the three-phase grid, essentially such SVPWM is a current-control type.

Table 1 List of switching states

ωt, °	S_a	S_b	S_c	S_h	S_l	i_{ra}	i_{rb}	i_{rc}	ωt, °	S_a	S_b	S_c	S_h	S_l	i_{ra}	i_{rb}	i_{rc}
90–120	0	1	0	1	1	I_{dc}	0	$-I_{dc}$	270–300	0	1	0	1	1	$-I_{dc}$	0	I_{dc}
$V_{ga}>V_{gb}>V_{gc}$	0	1	0	1	0	I_{dc}	$-I_{dc}$	0	$V_{gc}>V_{gb}>V_{ga}$	0	1	0	1	0	0	$-I_{dc}$	I_{dc}
—	0	1	0	0	0	0	0	0	—	0	1	0	0	0	0	0	0
—	0	1	0	0	1	0	I_{dc}	$-I_{dc}$	—	0	1	0	0	1	$-I_{dc}$	I_{dc}	0
120–150	0	1	0	1	1	I_{dc}	0	$-I_{dc}$	300–330	0	1	0	1	1	$-I_{dc}$	0	I_{dc}
$V_{ga}>V_{gb}>V_{gc}$	0	1	0	1	0	I_{dc}	$-I_{dc}$	0	$V_{gc}>V_{gb}>V_{ga}$	0	1	0	1	0	0	$-I_{dc}$	I_{dc}
—	0	1	0	0	0	0	0	0	—	0	1	0	0	0	0	0	0
—	0	1	0	0	1	0	I_{dc}	$-I_{dc}$	—	0	1	0	0	1	$-I_{dc}$	I_{dc}	0
150–180	1	0	0	1	1	0	I_{dc}	$-I_{dc}$	330–360	1	0	0	1	1	0	$-I_{dc}$	I_{dc}
$V_{gb}>V_{ga}>V_{gc}$	1	0	0	1	0	$-I_{dc}$	I_{dc}	0	$V_{gc}>V_{ga}>V_{gb}$	1	0	0	1	0	$-I_{dc}$	0	I_{dc}
—	1	0	0	0	0	0	0	0	—	1	0	0	0	0	0	0	0
—	1	0	0	0	1	I_{dc}	0	$-I_{dc}$	—	1	0	0	0	1	I_{dc}	$-I_{dc}$	0
180–210	1	0	0	1	1	0	I_{dc}	$-I_{dc}$	0–30	1	0	0	1	1	0	$-I_{dc}$	I_{dc}
$V_{gb}>V_{ga}>V_{gc}$	1	0	0	1	0	$-I_{dc}$	I_{dc}	0	$V_{gc}>V_{ga}>V_{gb}$	1	0	0	1	0	$-I_{dc}$	0	I_{dc}
—	1	0	0	0	0	0	0	0	—	1	0	0	0	0	0	0	0
—	1	0	0	0	1	I_{dc}	0	$-I_{dc}$	—	1	0	0	0	1	I_{dc}	$-I_{dc}$	0
210–240	0	0	1	1	1	$-I_{dc}$	I_{dc}	0	30–60	0	0	1	1	1	I_{dc}	$-I_{dc}$	0
$V_{gb}>V_{gc}>V_{ga}$	0	0	1	1	0	0	I_{dc}	$-I_{dc}$	$V_{ga}>V_{gc}>V_{gb}$	0	0	1	1	0	I_{dc}	0	$-I_{dc}$
—	0	0	1	0	0	0	0	0	—	0	0	1	0	0	0	0	0
—	0	0	1	0	1	$-I_{dc}$	0	I_{dc}	—	0	0	1	0	1	0	$-I_{dc}$	I_{dc}
240–270	0	0	1	1	1	$-I_{dc}$	I_{dc}	0	60–90	0	0	1	1	1	I_{dc}	$-I_{dc}$	0
$V_{gb}>V_{gc}>V_{ga}$	0	0	1	1	0	0	I_{dc}	$-I_{dc}$	$V_{ga}>V_{gc}>V_{gb}$	0	0	1	1	0	I_{dc}	0	$-I_{dc}$
—	0	0	1	0	0	0	0	0	—	0	0	1	0	0	0	0	0
—	0	0	1	0	1	$-I_{dc}$	0	I_{dc}	—	0	0	1	0	1	0	$-I_{dc}$	I_{dc}

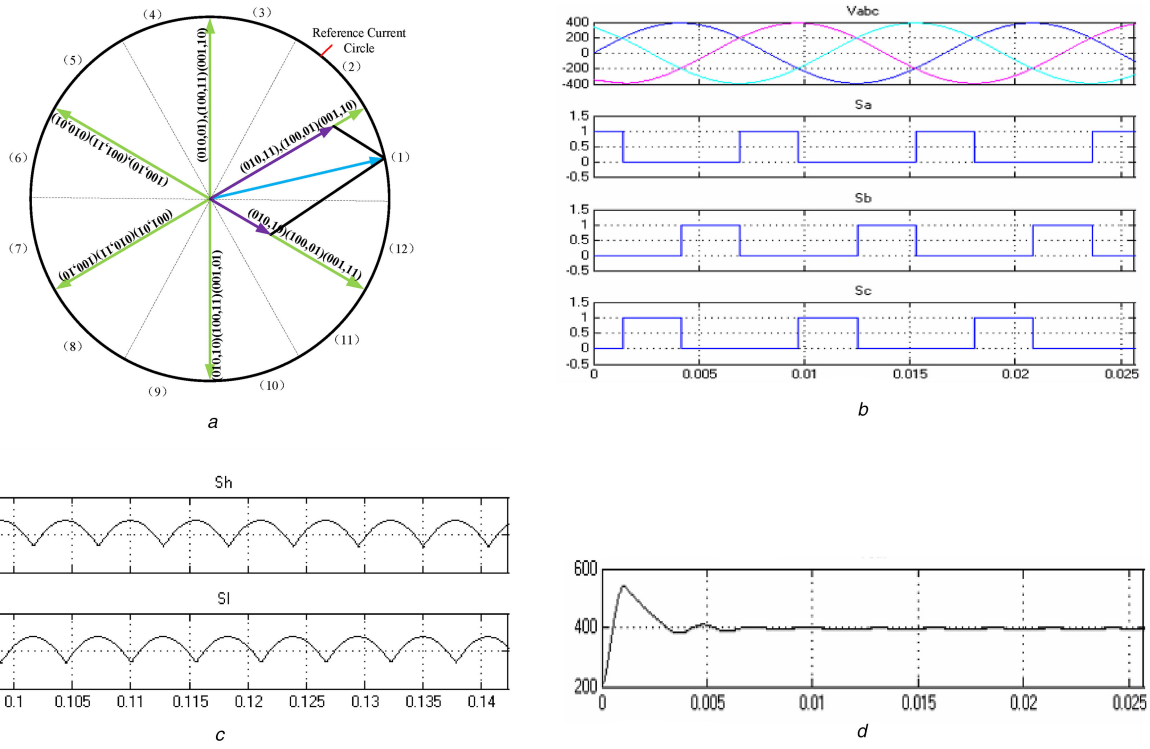

Fig. 6 *Control algorithm of the current SVPWM based on SWISS rectifier*

(a) Distribution of the current space vectors, ***(b)*** Switching states of S_a, S_b, and S_c, ***(c)*** Duty cycle of S_h and S_l, ***(d)*** DC-bus voltage control

The above analysis also indicates that S_a, S_b, and S_c are only changing the state every 1/6 of the grid period. Conventional Si IGBTs or MOSFETs are sufficient for such three switches. For S_h and S_l, the high switching frequency is required to increase the power density, where SiC devices are adopted.

For the sector ($90°<\omega t<120°$), here $\theta = \omega t - 90°$, i.e. $0<\theta<30°$. T_1, T_2, and T_0 are defined as the time interval of the switch state (010, 11), (010, 10), and (010, 00), respectively. T_s is the switching period. Therefore

$$\begin{cases} T_0 + T_1 + T_2 = T_s \\ T_1 \cdot \sqrt{2} I_{dc} e^{j((\pi/6))} + T_2 \cdot \sqrt{2} I_{dc} e^{j(-(\pi/6))} = T_s \cdot \sqrt{\frac{3}{2}} I_m e^{j\theta} \end{cases} \quad (5)$$

i.e.

$$\begin{cases} T_1 = \sin\left(\theta + \dfrac{\pi}{6}\right) \cdot M \cdot T_s \\ T_2 = \sin\left(\theta - \dfrac{\pi}{6}\right) \cdot M \cdot T_s \\ M = \dfrac{\sqrt{3}\, I_m}{2 I_{dc}} \end{cases} \tag{6}$$

The duty cycles of S_h and S_l are $(T_1 + T_2)/T_s$ and T_1/T_s, respectively. Simulation results are shown in Fig. 7*a*, indicating that the unity power factor has been realised.

Fig. 6*b* verifies that the grid switches S_a, S_b, and S_c are operated at the low frequency. Fig. 6*c* shows the corresponding duty cycles and Fig. 6*d* shows the DC-bus voltage is limited to 400 V, low enough to apply 650 V Si/SiC on the DC/DC primary side.

With the proposed SVPWM control, a new control structure proposed shown in Fig. 7*a*. The I_d and I_q are both closed-loop controlled. These two extra inner current control loops not only make the phase current sinusoidal but also in phase with the voltage. The controlled *d*/*q* current of the AC/DC side are shown in Fig. 7*c*, where $I_d = 0$ that confirms the phase currents and voltages are in phase with each other.

There are some current spikes shown in Fig. 7*b*, which also present in I_d in Fig. 7*c*. That is because the switches (S_a S_b S_c) have some delay caused by the software implementation, resulting the switches state fall behind the grid voltage. Take the boundary of the sector ($60° < \omega t < 90°$, $V_{ga} > V_{gc} > V_{gb}$) and sector ($90° < \omega t < 120°$, $V_{ga} > V_{gb} > V_{gc}$) as an example. Within sector ($90° < \omega t <$

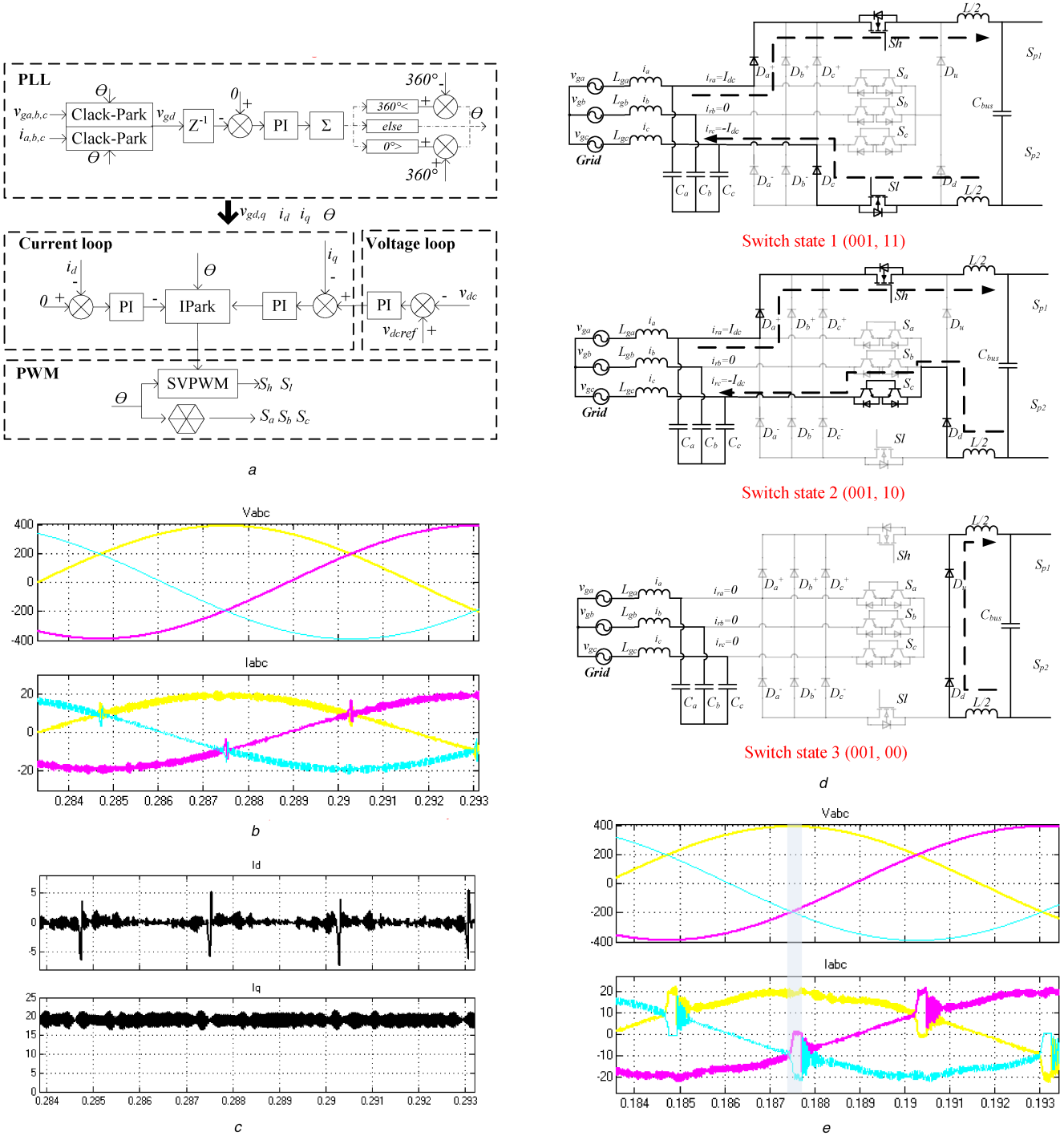

Fig. 7 *Simulation model and waveforms of the SWISS PFC*

(a) Control structure, ***(b)*** Simulated grid voltage and current under proposed SVPWM, ***(c)*** I_d and I_q, ***(d)*** Three-switch states at the boundary of sectors ($60 < \omega t < 90°$ $V_{ga} > V_{gc} > V_{gb}$) and ($90 < \omega t < 120°$, $V_{ga} > V_{gb} > V_{gc}$), where (S_a S_b S_c) did not change immediately, ***(e)*** Grid voltage and current waveform once (S_a S_b S_c) is given a little more delay

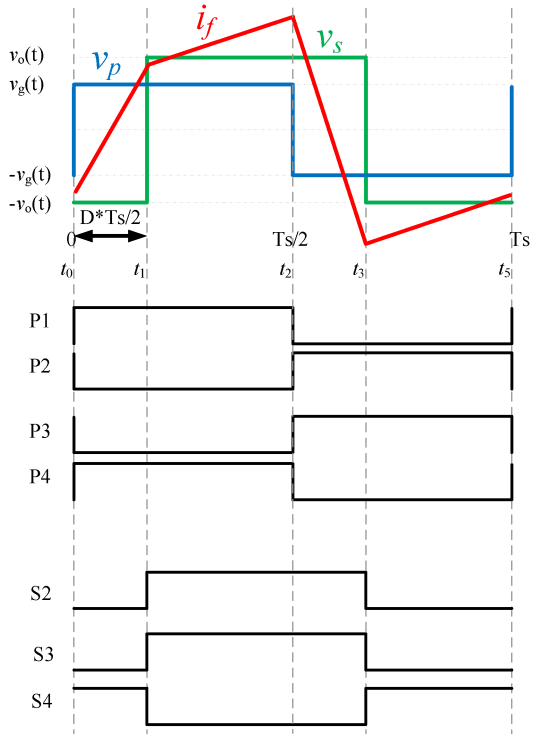

Fig. 8 *SPS control of the DAB*

120°), we need switch states (010, 10), (010, 11), and (010, 00) listed in Table 1 to realise the unity PFC. (i_{ra} i_{rb} i_{rc}) will be (I_{dc} 0 $-I_{dc}$), (I_{dc} $-I_{dc}$ 0), and (0 0 0), respectively. Therefore, the average value of (i_{ra} i_{rb} i_{rc}) will be $(T_1 + T_2)/T_s \cdot I_{dc}$, $-T_2/T_s \cdot I_{dc}$, and $-T_1/T_s \cdot I_{dc}$.

At the transition when $\omega t = 90°$, the switches (S_a S_b S_c) should have changed from (001) to (010). However, due to the delay of the software execution, (S_a S_b S_c) will still keep the same as previous sector (001) for a moment, yielding the switch state of (001, 10), (001, 11), and (001, 00), as shown in Fig. 8*a*. Accordingly, (i_{ra} i_{rb} i_{rc}) is (I_{dc} 0 $-I_{dc}$), (I_{dc} 0 $-I_{dc}$), and (0 0 0), given in this sector $V_{ga} > V_{gb} > V_{gc}$. Therefore, the average values of (i_{ra} i_{rb} i_{rc}) are $(T_1 + T_2)/T_s \cdot I_{dc}$, 0, and $-(T_1 + T_2)/T_s \cdot I_{dc}$. Distortions appear on i_b and i_c.

Owing to existence of the LC filter at the grid side, the grid currents i_b will increase gradually towards 0 and i_c will decrease gradually towards $-(T_1 + T_2)/T_s \cdot I_{dc}$. To verify this result, we set a little more delay for switches (S_a S_b S_c) during the section transitions. The current spikes become more obvious, as shown in Fig. 7*e*.

3 Variable DC-bus control for ZVS on of the DC/DC converter

Each secondary side of the DC/DC stage in Fig. 5 is one H-bridge. To simplify the control strategy, all four H-bridges on the secondary side are synchronous. Therefore, such design essentially is a DAB-based isolated DC/DC converter, which is widely used for offering the inherent bidirectional power flow capability, electrical isolation, high reliability, and ease of realising the soft-switching control. Various modulations of DAB converters have been proposed, e.g. dual-phase-shift (DPS) and VSF modulation. However, it leads to the high control complexity. In this paper, we will only focus on the conventional single phase-shift (SPS) between the transformer primary and secondary, applying the constant switching frequency (CSF), shown in Fig. 8. Here, $D\varepsilon$ [0, 1].

Assume the DC-bus voltage is V_{in}, the battery voltage is V_o and the turn ratio is n:1. Given that

$$i_{Lsps}(t_0) = \frac{-V_{in} + nV_o \cdot (1 - 2D)}{4 \cdot f_s \cdot L_s} \tag{7}$$

$$i_{Lsps}(t_1) = \frac{V_{in} \cdot (2 \cdot D - 1) + nV_o}{4 \cdot f_s \cdot L_s} \tag{8}$$

To ensure ZVS of the primary side, we need $i_{Lsps}(t_0) \leq 0$, i.e.

$$D > 0.5\left(1 - \frac{V_{in}}{nV_o}\right) \tag{9}$$

While for the secondary side, to secure ZVS, we need $i_{Lsps}(t_1) \geq 0$, i.e.

$$D > 0.5\left(1 - \frac{nV_o}{V_{in}}\right) \tag{10}$$

For the conventional boost-type PFC, V_{in} is always higher than the grid peak voltage. When the battery voltage is low, (10) can only be achieved at the heavy load when D is large. When the battery voltage is high, (9) is difficult to meet unless the output power is high. Losing ZVS at the light-load operation is one of the major demerits of the DAB. For a 48 V battery pack, the operational voltage could vary from 24 to 72 VDC, resulting in the difficulty to realise the ZVS within the whole voltage and power range. However, with the assistance of the SWISS rectifier, such challenge could be resolved.

3.1 Securing ZVS

With the SWISS buck-type PFC, it is possible to vary the output of the PFC, i.e. the input voltage of the DAB to secure ZVS for both sides. The direct way is to let $V_{in} = nV_o$, making (9) and (10) true at any power level to secure the ZVS operation. Since in this paper four identical transformers are adopted, the equation is revised as $V_{in} = nV_o$. Here, $n = 100{:}48$.

Shown in Fig. 9 are the simulation verifications with the variable DC-bus control used to secure ZVS.

The top plot of each figure is the secondary-side switch current (blue) and voltage (purple). The bottom plot represents the primary-side switch voltage and current. If at the falling edge of the purple line, the blue line (current) remains negative, it indicates that ZVS turn-on is realised. As shown in Figs. 9*a* and *b*, with the fixed input voltage, the ZVS turn-on is lost when the battery voltage is low. Fig. 9*c* indicates that the ZVS can be gained back once the DC-bus voltage is lower as well. Fig. 9*d* shows the proposed DC-bus voltage for the full-range battery voltage.

3.2 Minimising the loss

In addition, such a variable DC voltage control can bring forth another benefit, i.e. minimising the power loss at the DAB stage at the ultra-low output power. When the power is low, the phase shift D is small as well. By assigning $V_{in} = nV_o$, the current values in (7)–(8) are both close to zero. This leads to a close-to-zero current flowing through the transformer and DAB stage, which further results in no switch conduction loss and transformer winding loss.

The simulation results are shown in Fig. 10. When $V_{in} \simeq 4nV_o$ ($V_{in} = 400$ V, $V_o = 48$ V, $D = 0$), the transformer current and the output power are both close to zero, as shown in Figs. 10*a–c*, respectively.

When $V_{in} \neq 4nV_o$ ($V_{in} = 200$ V, $V_o = 60$ V, $D = 0$), although PWM signals on both DAB sides are perfectly aligned, i.e. zero phase shift, still there is some transformer current flowing through switches, causing the conduction loss and winding loss. More importantly, it is very hard to implement a near-zero power output, as shown in Figs. 11*a–c*.

4 Experimental validation

Some key elements are listed in Table 2.

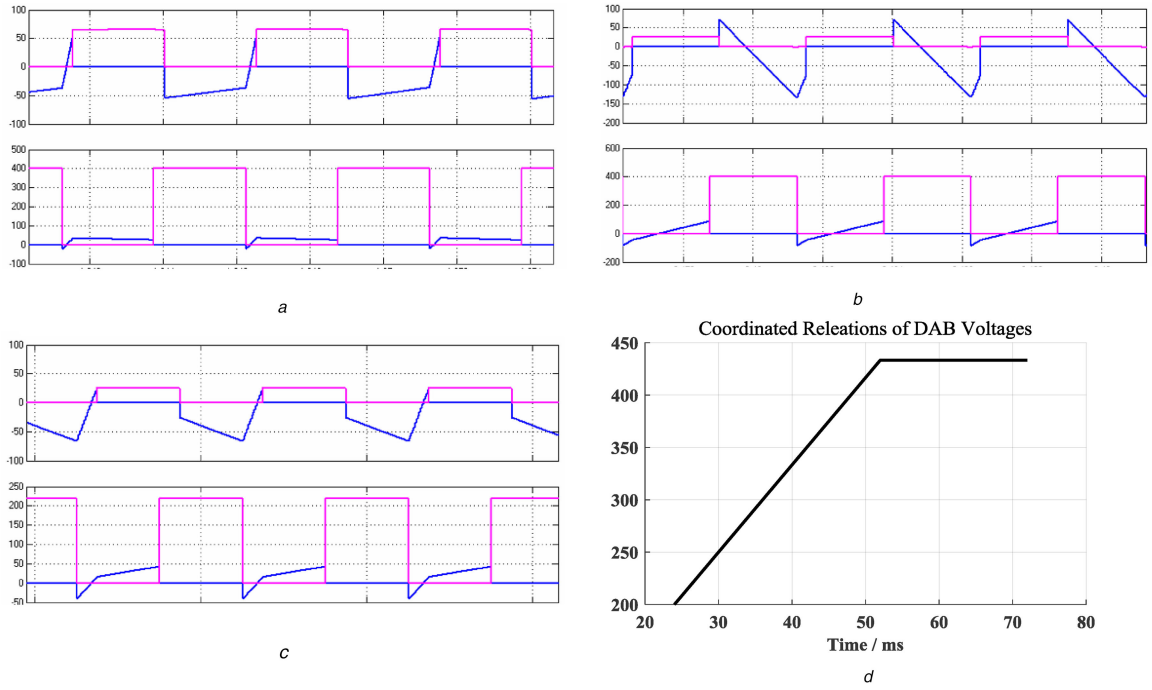

Fig. 9 *Simulation voltage and current waveform of the DAB part*

(a) $V_{bus} = 400$ V, $V_o = 65$ V, $I_o = 160$ A. ZVS secured (2 µs/div), ***(b)*** $V_{bus} = 400$ V, $V_o = 24$ V, $I_o = 160$ A. ZVS not secured for secondary (2 µs/div), ***(c)*** $V_{bus} = 220$ V, $V_o = 24$ V, $I_o = 160$ A. ZVS secured again (5 µs/div), ***(d)*** Proposed DC-bus voltage versus the battery output voltage

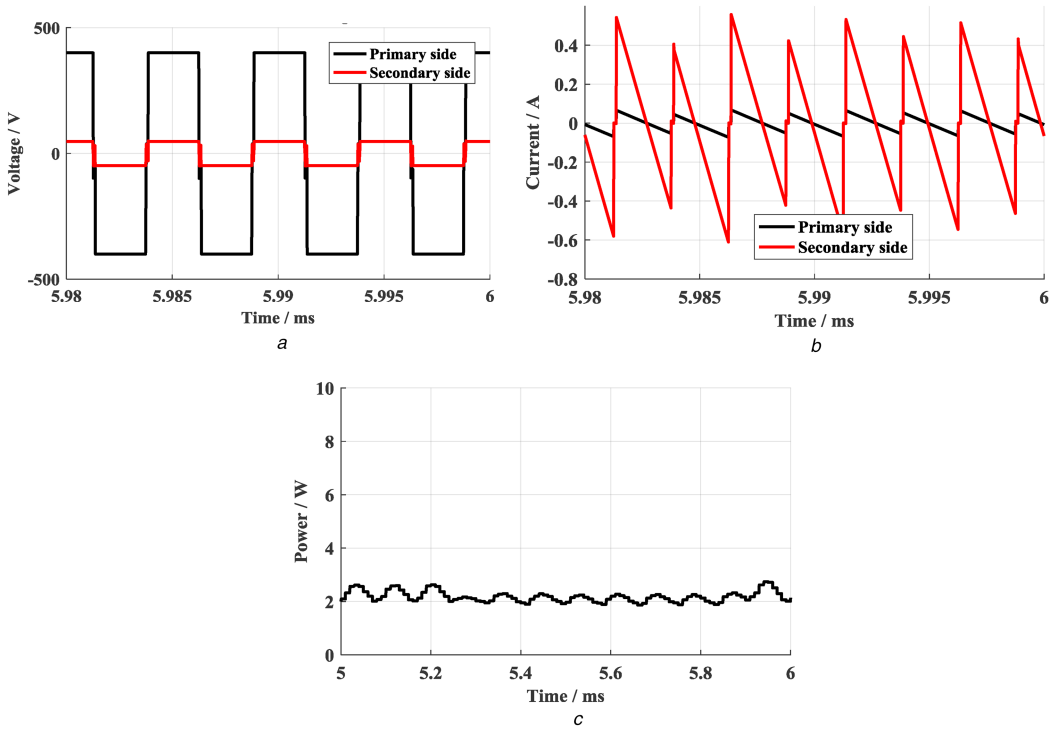

Fig. 10 *Simulation voltage and current of the DAB transformer when* $V_{in} = 4nV_o$

(a) Transformer voltage at both sides ($V_{bus} = 400$ V, $V_o = 48$ V, $D = 0$), ***(b)*** Transformer current at both sides ($V_{bus} = 400$ V, $V_o = 48$ V, $D = 0$), ***(c)*** DAB output power ($V_{bus} = 400$ V, $V_o = 48$ V, $D = 0$)

The actual prototype is shown in Fig. 12. The overall power density (PFC + DC/DC) is ~1.6 kW/L. The test conditions are shown in Table 3. Waveforms of the full power (1–11 kW) are shown in Figs. 13*a–c*. Each phase voltage and current are perfectly aligned, i.e. unity power factor. The current spikes do appear, as predicted in the previous analysis, which is caused by the delay of the control implementation.

It is worthwhile to revisit that most of the switches we used in the PFC stage are Si devices to keep the cost down. Only four SiC MOSFETs and two SiC diodes are used to maximise the system performance. SiC MOSFETs are chosen as the DC-bus switches S_h and S_l. As a comparison, one 1200 V Si IGBT from Infineon with similar voltage and current ratings is selected, as shown in Fig. 14. Note Si Cool MOSFET will not fit in this application because the grid voltage can go to 480 VAC while the majority of Si Cool MOSFETs is rated at 650 V. A 900 V Si Cool MOSFET is still rare.

At the rated power of 11 kW, the switching current is ~27.5 A. If one IGBT is selected to replace two SiC MOSFETs in parallel for S_h and S_l, the switching loss of IGBT is 7.5 mJ, in contrast to

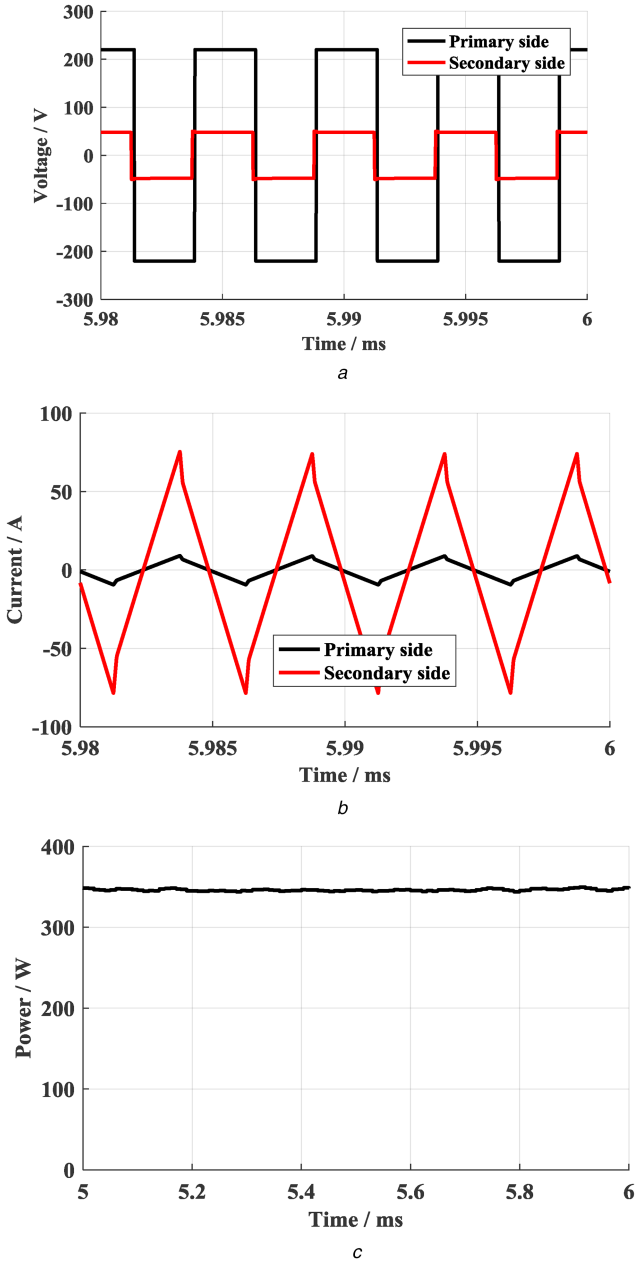

Fig. 11 *Simulation voltage and current of the DAB transformer when* $V_{in} \neq 4nV_o$

(a) Transformer voltage at both sides ($V_{bus} = 220$ V, $V_o = 48$ V, $D = 0$), ***(b)*** Transformer current at both sides ($V_{bus} = 220$ V, $V_o = 48$ V, $D = 0$), ***(c)*** DAB output power ($V_{bus} = 220$ V, $V_o = 48$ V, $D = 0$)

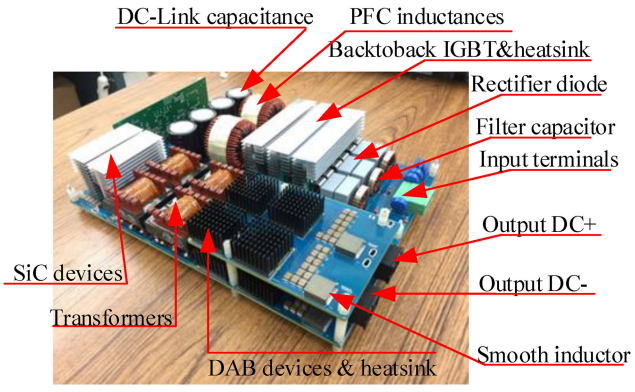

Fig. 12 *Final prototype of the charger (PFC + DCDC)*

~600 µJ for two SiC MOSFETs, which adds the extra power loss of 483 W, representing ~4.4% of the efficiency drop. Furthermore, the increased power loss will increase the size of the heatsink. It is possible for the pure Si IGBT-based solution to reach the high efficiency as well, as long as the switching frequency is reduced to <10 kHz. As can be seen in Fig. 12, the PFC inductor is already one of the largest components. Reducing the switching frequency by using Si IGBT will lower the power density.

Lastly, DC-bus variation is tested to show the alteration of the power loss. As shown in Figs. 15*a* and *b*, both of the figures represent the phase-shift equal to 0, which theoretically will result in no power delivery. However, when the $V_{in} = nV_o$, as shown in Fig. 15*b*, the current circulating through the charger is close to zero, much smaller than $V_{in} \neq nV_o$, shown in Fig. 15*a*. Here, purple and blue represent the primary and secondary voltage of one transformer, respectively. Green is the transformer current.

Table 2 Key switches of the final charger prototype

Parts	Parameters	Number
PFC grid-side diodes	1200 V/75 A	6
PFC grid-side IGBTs	1200 V/75 A	6
DC-bus switches S_h and S_l	900 V/36 A	4
DC-bus diodes D_d and D_u	1200 V/20 A	2
DAB primary-side switches	900 V/36 A	8
DAB secondary-side switch	150 V/155 A	32
DC-bus inductors	350 µH	2
DC-bus capacitors	200 µF	2
output capacitors	100 µF	1
transformers	3 kW, turn ratio = 2:1	4

Table 3 Test condition

Parameters	Values
input voltage	3Φ 380 VAC
output voltage	22–72 VDC
rated power	11 kW
PFC switching frequency	75 kHz
DAB switching frequency	150 kHz
transformer turn-ratios	100:48
transformer leakage inductance	0.6 µH

5 Conclusions

A 48 V/11 kW battery charger made of a buck-type SWISS rectifier and a DAB DC/DC converter was realised in this paper. SiC MOSFETs are used for the DC-bus switches, while Si IGBTs are applied for the grid-side switches, aiming at the high efficiency, high power density, and low cost. A novel current-type SVPWM consisting of 18 independent current vectors was proposed to control the PFC section. Based on which the current closed-loop control is proposed aiming at the unity power factor at any load.

To secure the ZVS turn-on for all DAB switches, a variable DC-bus voltage control is proposed. Such control strategy not only secures ZVS but also reduces the circulating current at the light-load operation, thereby minimising the conduction loss at the light-load operation and approach nearly zero output power. At last, an engineering prototype was designed to verify the proposed software and hardware. At the present stage, the current spikes exist on the grid side, due to the time delay of the software execution. To improve the current quality, we propose to adopt the high-control-bandwidth microcontroller such as FPGA in the future.

6 Acknowledgment

The authors would like to thank the support of Arun Patel from Minit Charger.

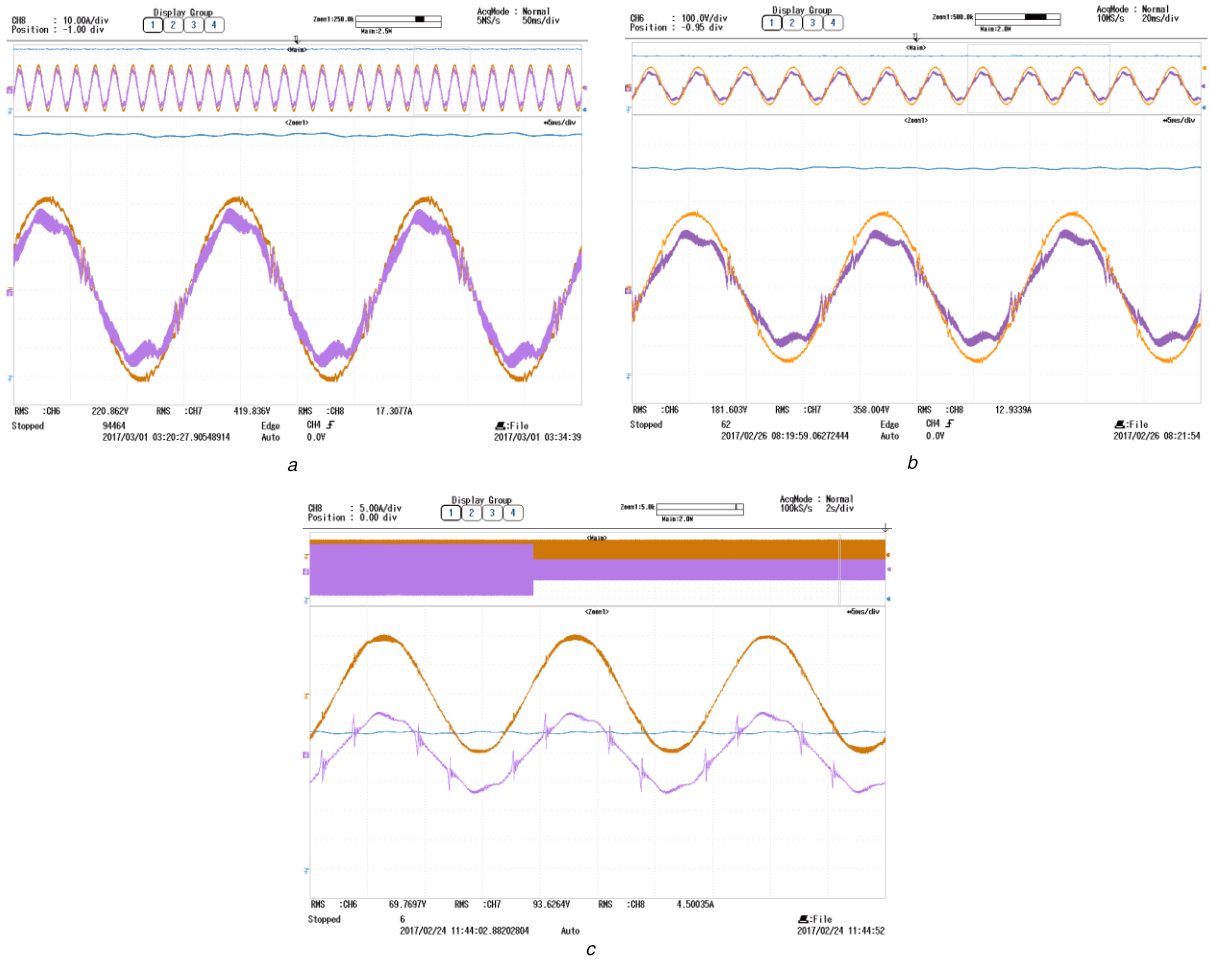

Fig. 13 *Experimental waveform of the PFC stage*
(a) PFC phase voltage and current at 11 kW, ***(b)*** PFC phase voltage and current at 7 kW, ***(c)*** PFC phase voltage and current at 1 kW

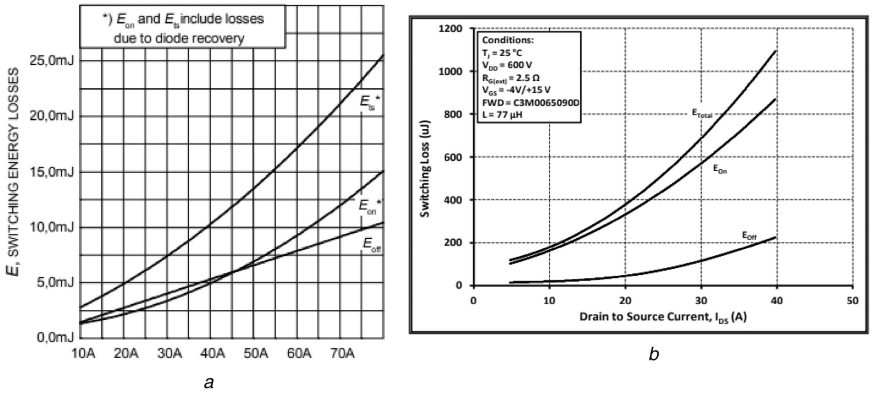

Fig. 14 *Switching loss comparison of the Si IGBT and SiC MOSFET*
(a) Switching loss of 1200 V/75 A IGBT (IKW40T120), ***(b)*** Switching loss of 900 V/36A SiC (C3M0065090D)

a *b*

Fig. 15 *Experimental voltage and current of the DAB transformer at different V_{in} and V_o*

(a) Phase-shift is zero, $V_{\text{in}} \neq nV_{\text{o}}$, ***(b)*** Phase-shift is zero, $V_{\text{in}} = nV_{\text{o}}$

7 Reference

[1] Yungtaek, J., Jovanovic, M.M.: 'Fully soft-switched three-stage AC–DC converter', *IEEE Trans. Power Electron.*, 2008, **23**, (6), pp. 2884–2892

[2] Sungho, K., Kang, F.-s.: 'Multi-functional on-board battery charger for plug-in electric vehicles', *IEEE Trans. Ind. Electron.*, 2014, **62**, (6), pp. 3460–3472

[3] Shin, C.-J., Lee, J.-Y.: 'An electrolytic capacitor-less bi-directional EV on-board charger using harmonic modulation technique', *IEEE Trans. Power Electron.*, 2014, **29**, (10), pp. 5195–5203

[4] Bai, H., Taylor, A., Guo, W., *et al.*: 'Design of an 11 kW power factor correction and 10 kW ZVS DCDC converter for a high-efficiency battery charger in electric vehicles', *IET Power Electron.*, 2012, **5**, (9), pp. 1714–1722

[5] Jauch, F., Biela, J.: 'Single-phase single-stage bidirectional isolated ZVS AC-DC converter with PFC'. 15th Int. Power Electronics and Motion Control Conf. and Exposition, EPE-PEMC 2012 ECCE Europe, LS5d.1-8, Novi Sad, Republic of Serbia, 2012

[6] Everts, J., Krismer, F., Keybus, J., *et al.*: 'Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC–DC converters', *IEEE Trans. Power Electron.*, 2014, **29**, (8), pp. 3954–3970

[7] Soeiro, T.B., Friedli, T., Kolar, J.W.: 'Swiss rectifier- A novel three-phase buck-type PFC topology for electric vehicle charging'. IEEE Applied Power Electronics Conf. and Exposition (APEC), 2012, pp. 2617–2624

[8] Mi, C., Bai, H., Wang, C., *et al.*: 'Operation, design, and control of dual H-bridge based isolated bidirectional DC–DC converter', *IET Power Electron.*, 2008, **1**, (3), pp. 176–187

[9] Krismer, F., Kolar, J.W.: 'Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application', *IEEE Trans. Ind. Electron.*, 2010, **57**, (3), pp. 881–891

[10] Hudgins, J.L.: 'Power electronic devices in the future', *IEEE J. Emerging Sel. Top. Power Electron.*, 2013, **1**, (1), pp. 11–17

[11] Barbee, W., Barkley, A., Cole, Z., *et al.*: 'A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices', *IEEE Trans. Power Electron.*, 2014, **29**, (5), pp. 2606–2617

[12] Bai, H., Mi, C.: 'Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC–DC converters using novel dual-phase-shift control', *IEEE Trans. Power Electron.*, 2008, **23**, (6), pp. 2905–2914

[13] Lingxiao, X., Diaz, D., Shen, Z., *et al.*: 'Dual active bridge based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple'. Applied Power Electronics Conf. and Exposition (APEC), Long Beach, California, 2013, pp. 1920–1925

[14] Krismer, F., Round, S., Kolar, J.W.: 'Performance optimization of a high current dual active bridge with a wide operating voltage range'. Power Electronics Specialists Conf., Jeju, South Korea, 2006

[15] Bai, H., Mi, C.C., Gargies, S.: 'The short-time-scale transient processes in high-voltage and high-power isolated bidirectional DC-DC converters', *IEEE Trans. Power Electron.*, 2008, **23**, (6), pp. 2648–2656