Implementations of Low-Power µProcessor System for Miniaturized IoT Applications

by

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Dedication

To my family,

with love and gratitude

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Abstract

Thanks to technical progress in integrated circuits, dominant computing classes have shrunk in size throughout the history of computing. As a result, handheld portable devices have the largest market volume among all the computer classes to date. In view of this miniaturizing trend, it is likely that millimeter-scale computers become the next widely used computer class. Miniaturized wireless sensing devices will be enablers for the Internet of Things (IoT), including many practical applications such as health monitoring and industrial sensing. Due to the small form factor, however, these types of devices have limited battery size and capacity, therefore energy efficient operation is a key requirement. Also, they are used in a wide range of environments leading to varying operating conditions, with different performance requirements across time. Consequently, dynamic and/or application-specific power management techniques are necessary for these types of devices. In this context, this dissertation focuses on implementing low-power μprocessor systems with novel power management techniques for miniaturized wireless sensors to achieve energy efficiency and extend their lifetime.

First, this dissertation presents a dynamic power management technique for the IoT μprocessor, which enables on-chip closed-loop minimum-energy-point tracking and hence guarantees energy-optimal operation at all times. Based on the observation that the ratio of leakage power to dynamic power can be an accurate indicator for the optimal operating point, the implemented system dynamically tracks the minimum energy operating points by adjusting supply voltage and body bias with very low hardware overhead. Secondly, this dissertation presents a μprocessor system designed for use in mm-scale sensing platforms for high temperature

applications. It features a deep sleep-mode that allows the complete system to retain full 16-kB SRAM contents with 0.54μW at 125˚C, which is 26× lower than the baseline design. A custom SRAM was designed and used for low leakage. The last two parts present essential sub-blocks required for low-power μprocessor systems: a wide-range level converter and a switched-capacitor DC-DC converter. Since the low-power digital systems often employ sub-threshold or near-threshold design techniques, a wide-range level converter is needed to interface between the blocks. By using the leakage biasing technique, the proposed level converter offers robust operation across a wide range of low and high supply voltages as well as PVT variations. An integrated DC-DC converter is also necessary for the low-power digital systems to support multiple power domains. In this dissertation, a switched-capacitor DC-DC generation tool is presented as a part of efforts in analog design automation. Based on the theoretical analyses, the proposed DC-DC generation tool directly finds the optimal design parameters and generates a netlist and its layout automatically from the given input specifications.

Chapter 1 **Introduction**

1.1 Background

Since the beginning of the era of electronic computer opened by the advent of vacuum tubes in the early 20th century, scientists and engineers have made a continuous effort in miniaturizing the electronic components and eventually the computer itself. The invention of the integrated circuit (IC) in the late 1950s was a great achievement of that effort [1]. The integrated circuit that is based on the metal-oxide-silicon (MOS) transistor invented in 1959 made building high-density circuits on a single chip possible. By the end of the 1960s, a single MOS integrated circuit could contain 100 or more logic gates, which leads to an attempt to integrate the complete computer processor onto a single MOS IC chip [2]. In 1971, the Intel 4004 was released, marking the world's first μprocessor that is a computer processor implemented on a single IC chip. Since then, as Gordon E. Moore predicted [3], the number of devices per silicon die has been increasing, and it reaches tens of billions these days. These continuing advances in the field of integrated circuits significantly contribute to the miniaturization of computers as well as the improvement of computing power. Smartphones and smartwatches being used presently are good examples of this, which are more powerful than workstations a couple decades ago while being completely portable. In other words, technical progress in integrated circuits has led to a new computer class, i.e. handheld portable devices, which eventually has the largest market volume among all the computer classes. In view of the fact that prevalent computing classes have been shrinking in size since the beginning of computer history, it is probable that millimeter-scale computers become the next widely used computer class.

In 1999, the concept of “Smart Dust” was proposed [4], envisioning a millimeter-scale sensor node with a focus on mobile networking and applications layers. Since then, wireless sensor nodes have been a popular topic of research. Also, in the early 2010s, the term “internet of things” (IoT) started to gain popularity. Underlying the IoT is wireless sensor technology, which allows the sensor to collect information about the surroundings. Recent research works have shown that the miniaturized wireless sensing devices enable the IoT for many practical applications such as health monitoring and industrial sensing. Due to the small form factor, however, these types of devices have limited battery size and capacity, therefore efficient energy consumption is a key requirement. In this context, this dissertation focuses on implementing low-power μprocessor systems for miniaturized wireless sensors to achieve an energy-efficiency and hence extend their lifetime.

1.2 Organization

The dissertation is composed of 2 chapters (chapter 2 and 3) introducing low-power μprocessor systems implemented for two different miniaturized IoT applications and the other two chapters (chapter 4 and 5) presenting essential sub-blocks required for low-power μprocessor systems: a wide-range level converter and a switched-capacitor DC-DC converter.

Chapter 2 presents a dynamic power management technique for the IoT μprocessor, which enables on-chip closed-loop minimum energy point (MEP) tracking. By using a combination of dynamic voltage scaling (DVS) and adaptive body biasing (ABB), the proposed method offers energy-optimal operation with a given fixed operating frequency determined by application demands. Based on the observation that the ratio of leakage power to dynamic power can be an accurate indicator for the optimal operating point, the implemented system dynamically tracks the minimum energy operating points by adjusting supply voltage and body bias with very low

hardware and power overhead. A custom DC-DC converter for supply voltage regulation and charge-pumps for body bias generation were implemented with the proposed method in a Cortex-M0 processor. Since SRAM is included in the same energy optimization loop as the processor, a custom SRAM was designed to match processor speed. The design is fabricated in a MIFS 55-nm deeply depleted channel (DDC) CMOS and the proposed approach achieves energy consumption within 4.6% of the optimal at 1 MHz across 5 process corners and temperatures from −20°C to 125°C. The fabricated processor achieves 6.4 pJ/cycle at 0.55V and 500 kHz clock frequency.

Chapter 3 presents a µprocessor system designed for use in mm-scale die-stacked sensing platforms for high temperature applications. A compact DC-DC converter is incorporated with a 16-kB custom SRAM for self-sufficient memory data retention, enabling a platform-level deep sleep mode. The proposed system is fabricated in a USJC 55-nm deeply depleted channel (DDC) technology that is deliberately shifted to the slow corner, allowing the complete sensing platform to retain full memory contents with 0.54µW during sleep mode at 125˚C, which is 26× lower than without the proposed techniques.

In chapter 4, a synchronous wide-range clocked level converter (LC) that converts sub-threshold input signals to high I/O voltages for ultra-low power (ULP) SoCs is presented. By biasing the circuit using NMOS leakage current, the design offers robust operation across a wide range of low and high supply voltages as well as PVT variations. The design was fabricated in 55-nm CMOS process and shows 60.5fJ (V_{DDH}=2.5 V) switching energy, marking a 2.6× improvement over prior works.

Chapter 5 proposes a new switched-capacitor DC-DC design methodology. Based on the theoretical analyses of the energy optimal operation of the switched-capacitor DC-DC converter, the proposed method directly finds the optimal design parameters from the given input

specifications. Exploiting cell-based design approach [5] and the design parameters found by the proposed method, the proposed DC-DC generator generates a netlist and the layout within a few hours from the user specifications. With a 14nm FinFET technology, the proposed DC-DC converter was verified, and a generated DC-DC converter achieves 75% efficiency.

Finally, chapter 6 concludes all the works and shows publications and patents on these works.

Chapter 2 **A Self-tuning IoT Processor for Energy Optimal Operation**

2.1 Introduction

Wireless sensors for internet-of-things (IoT) applications have become a prominent computing class these days and are typically severely power constrained. Miniaturization is one of the main trends in such applications, and thus the power budget of wireless sensors is becoming more restricted due to the shrinking battery size [4], [5]. At the same time, a long battery life is essential for wireless sensors in many IoT applications, leading to the requirement for energy-efficient operation along with energy harvesting [6]. Since its invention, dynamic voltage scaling (DVS), which dynamically scales the supply voltage and clock frequency for time-varying computational loads, has been widely adopted for energy-efficient operation [7]. However, DVS is ineffective when leakage power is dominant since leakage current is, to the first order, only linearly reduced by the supply voltage. In contrast, adaptive body biasing (ABB) is able to exponentially reduce leakage current by adjusting the threshold voltage (V_{th}) of the transistors [8]. Recently, closed-loop ABB control was also demonstrated in [9] without energy minimization. Energy-optimal operation therefore can be achieved by using a combination of DVS and ABB such that dynamic energy and leakage energy are at the optimal trade-off point [10], [11].

Since IoT devices are deployed in a wide range of environments, the operating conditions for factors such as temperature and workload are unpredictable and vary widely. Meanwhile, energy-efficient operation must be guaranteed in all possible cases. Due to the dependence of leakage on temperature and workload fluctuations over time, runtime adjustment is indispensable for energy-optimal operation of IoT devices. Minimum energy point (MEP) tracking has been

demonstrated in [12]. However, the embedded DC-DC converter must stop its operation during energy sense cycles, which may lead to timing errors and failure of the system or require a large voltage margin for safe operation if performed infrequently. In addition it only adjust supply voltage and not body bias which is critical in wide ranging operating conditions.

In this chapter, we make the key observation that at the optimal energy operating point, the ratio of leakage to dynamic power is a nearly constant value across temperature, process variation, and workload. We refer to this as the optimal leakage ratio. We derive the optimal leakage ratio value from basic MOSFET characteristics and show that it results in an energy-per-cycle value within 4.6% of the optimal energy operating point across PVT conditions. We then show how the leakage ratio can be efficiently and simply measured by counting the modulated frequency of a DC-DC converter and comparing the count obtained at two different clock frequencies. The proposed method was implemented in a Cortex-M0 processor in MIFS 55-nm deeply depleted channel (DDC) CMOS, which has a large body coefficient that we can exploit to compensate for leakage power across a wide range of PVT variations [13], with a custom DC-DC converter for supply voltage regulation and charge pumps for body bias generation. A control loop dynamically measures the leakage ratio and processor speed using a critical-path replica and automatically adjusts the body bias and supply voltage. Measurements demonstrate that the design can maintain the optimal ratio across a wide temperature range, from −20°C to 125°C and 5 process corners from split-wafer lots. The processor achieves 6.4 pJ/cycle, and operates at 100 kHz–6 MHz for IoT applications.

2.2 Optimal Leakage Ratio

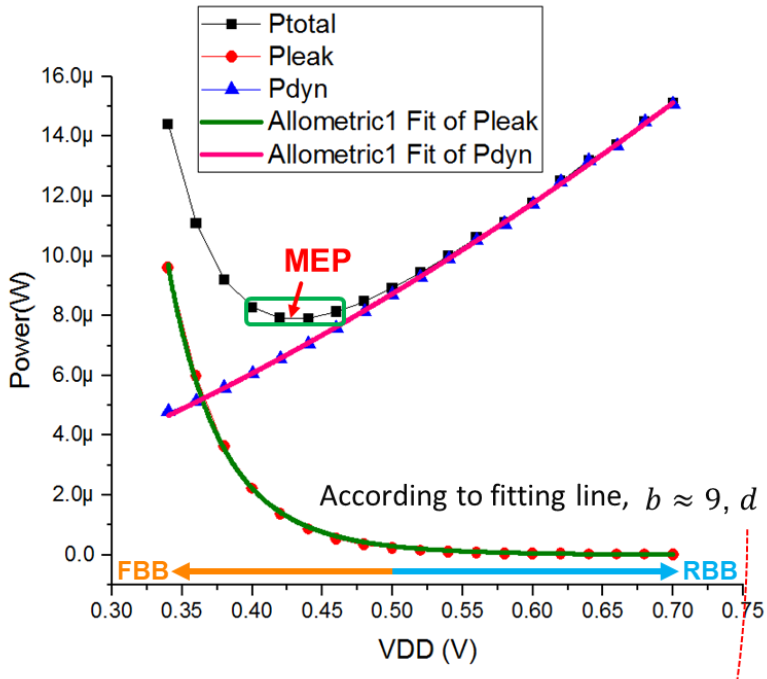
For a typical digital circuit, there is a particular combination of supply voltage and V_{th} that minimizes total energy consumption [14], [15]. Since the supply voltage and V_{th} determine the

operating frequency of the circuit, there is a specific operating frequency corresponding to that minimum energy point [16]. However, for a given fixed V_{th}, the total energy can only have a local minimum corresponding to a particular supply voltage. Similarly, for a given fixed operating frequency, the total energy shows a local minimum at a particular set of supply voltage and V_{th}, which is referred to as the minimum energy point, or MEP, in this chapter since we are targeting the system that determines its operating frequency not based on energy consumption but on application demands. The proposed architecture will find the MEP for a given fixed operating frequency. The optimal leakage ratio is also calculated and measured for a given fixed operating frequency.

2.2.1 Derivation

Figure 2.1 provides a derivation of the optimal leakage ratio in a test digital circuit at 10 MHz clock frequency and 25°C. V_{th} is implicitly set to maintain an operating frequency of 10 MHz. Theoretically, the MEP occurs when the slopes of the dynamic and leakage powers become equal and opposite. Dynamic power is composed of switching power proportional to V_{DD}^2 and short-circuit power [17]. If short-circuit power is not negligible compared to switching power, dynamic power cannot be accurately modeled as a simple quadratic with supply voltage. Hence, we use a power model $y = cV_{DD}^d$ to fit the dynamic power (Figure 2.1, Equation 2.2), and d would be a little less than 2. We also use a power model $y = aV_{DD}^{-b}$ (Figure 2.1, Equation 2.1) to fit the leakage power, similar to [10], to facilitate the derivation. Although leakage power is best described by a complex exponential equation, in the region we are interested in, which is near the MEP, it can be expressed with a simpler power function. Combining these two expressions and minimizing the power by setting the slopes equal, we find that the ratio of dynamic power to leakage power at MEP is b/d, which is 5.6 at 10 MHz clock frequency and 25°C in the test circuit,

leading to the P_{leak}/P_{total} ratio of 1/6.6, i.e. 15%. Note that the optimal ratio of 1/6.6 is not a universal constant value but is specific to a given operating condition. However, due to the shallow minima in power near the MEP, we found that we could apply this ratio across a wide range of operating condition, as explained in the chapter 2.2.2 Variation across temperature and workload.



According to fitting line, $b \approx 9$, $d \approx 1.6$

Assume $P_{leak} = aV_{DD}^{-b}$ $(a, b \text{ is } const.)$ (2.1)

$P_{dyn} = cV_{DD}^{d} f$ $(c, d \text{ is } const.)$ (2.2)

Then $P_{total} = aV_{DD}^{-b} + cV_{DD}^{d} f$ (2.3)

Minimize P_{total} : $\frac{dP_{total}}{dV_{DD}} = 0$ (2.4)

From (3), (4), $-abV_{DD}^{-b-1} + cdV_{DD}^{d-1} f = 0 \rightarrow \frac{cV_{DD}^{d} f}{aV_{DD}^{-b}} = \frac{b}{d}$ (2.5)

From (1), (2), (5), and $b \approx 9$, $d \approx 1.6$

$$\left(\frac{P_{dyn}}{P_{leak}}\right)_{@MEP} = \left(\frac{cV_{DD}^{d} f}{aV_{DD}^{-b}}\right)_{@MEP} = \frac{b}{d} \approx 5.6 \rightarrow \left(\frac{P_{leak}}{P_{total}}\right)_{@MEP} \approx \frac{1}{6.6}$$

Figure 2.1 Derivation of optimal leakage ratio based on the simulation results at 10 MHz clock frequency and 25˚C (V_{th} is implicitly set to maintain an operating frequency of 10 MHz)

2.2.2 Variation across temperature and workload

Total power has a shallow minima as shown in Figure 2.1; note that V_{th} is implicitly set to maintain an operating frequency of 10 MHz. In the green box in Figure 2.1, the boundary points at the left and right are within 4.7% of the minimum. Since the leakage power rises rapidly at low V_{DD} to become comparable to the dynamic power near the MEP, the ratio of leakage power to dynamic power changes quickly near the MEP. At the left and right edges of the green box, the ratios of dynamic power to leakage power are approximately 3:1 and 14:1, respectively. As a result, the ratio of the leakage power to dynamic power is very sensitive across this range, while MEP power is not. The ratio fluctuates depending on temperature and workload as shown in Figure 2.2; note again that V_{th} is implicitly set to maintain the target frequency. However, due to the shallow minima and high sensitivity near the MEP, if the system maintains an optimal leakage ratio, it can be guaranteed that the system is at or near the MEP. The P_{leak}/P_{total} ratio of 15% yields power within 1% from the minimum at 10 MHz clock frequency across temperature, as confirmed in Figure 2.3(a). Even at 100 kHz clock frequency, where leakage power is much more dominant than at 10 MHz, the P_{leak}/P_{total} ratio of 15% yields power within 4.6% and 3% from the minimum at 25°C and -20°C, respectively. (Due to the huge leakage power, the P_{leak}/P_{total} ratio of 15% is not achievable even with the maximum reverse body bias at 125°C and 100 kHz clock frequency.) We find that the ratio can be a very accurate indicator for the optimal operating point and therefore leverage this ratio to find MEP, and hence our proposed approach essentially uses the ratio of dynamic to leakage power as a proxy for minimum energy.

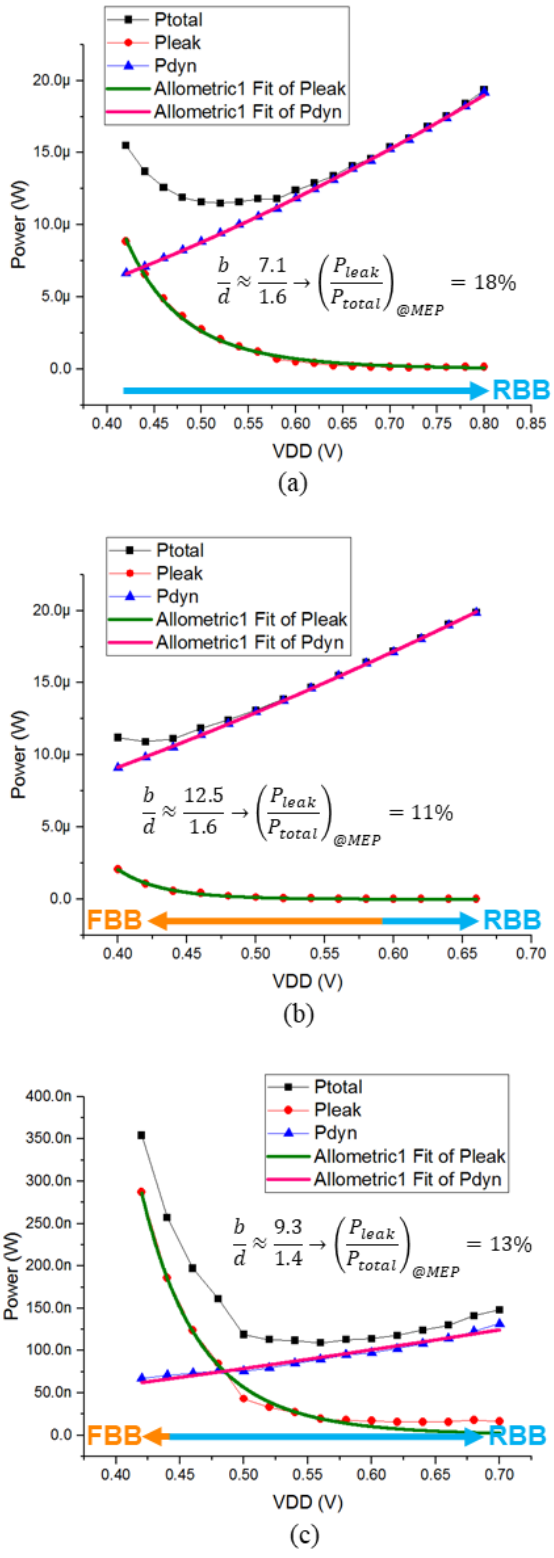
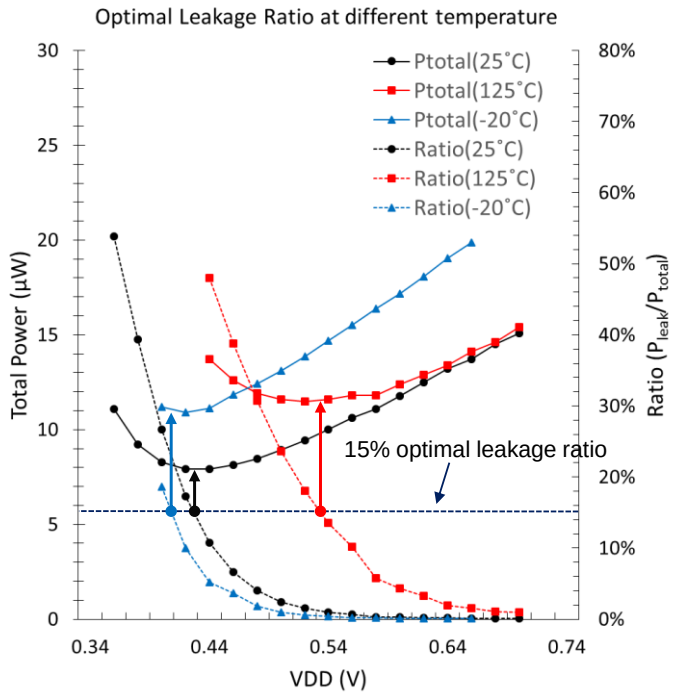
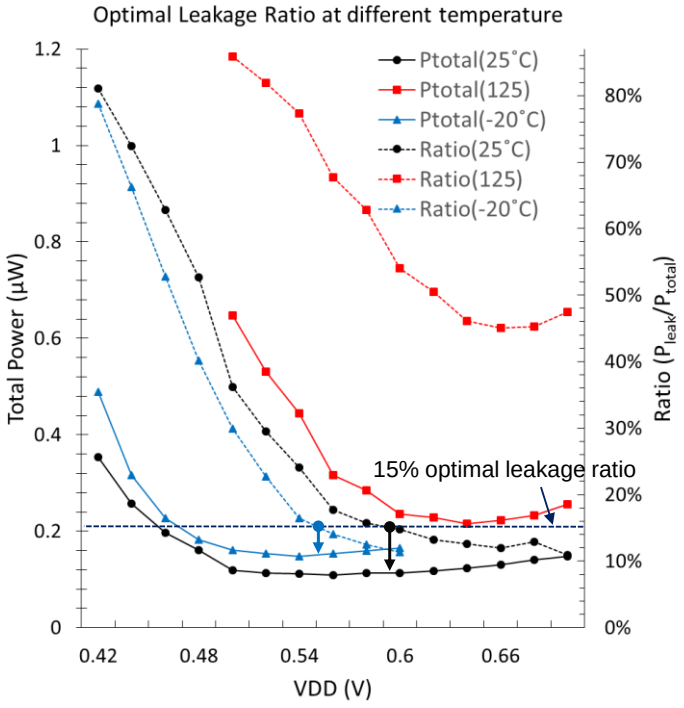


Figure 2.2 Variation of the optimal leakage ratio at different conditions (V_{th} is implicitly set to maintain the target frequency): (a) 10 MHz clock frequency and 125˚C, (b) 10 MHz clock frequency and -20˚C, (c) 100 kHz clock frequency and 25˚C



(a)



(b)

Figure 2.3 Plot shows total power is within (a) 1% of optimal at derived 15% leakage ratio across temperature at 10 MHz clock frequency, (b) 4.6% and 3% of optimal at 15% leakage ratio at 25˚C and -20˚C, respectively, at 100 kHz clock frequency (V_{th} is implicitly set to maintain the target frequency. Due to dominant leakage power, the optimal leakage ratio cannot be achieved even with maximum reverse body bias at 125˚C)

2.3 Architecture for Measurement the Ratio

The overall system architecture is shown in Figure 2.4 and consists of a configurable DC-DC converter, which supplies the processor and memory, and two bias-voltage generators for adjusting V_{th}. In order to tune the processor operation to the optimal leakage ratio (1/5.6), we need to measure both the leakage and dynamic power of the processor, which we accomplish by monitoring the frequency of the DC-DC converter. The DC-DC converter-supplied current is determined by its flying cap size (C_{fly}), dropout voltage (ΔV), and frequency. At runtime, the flying cap size is constant, and ΔV is regulated to its optimal value, i.e. ΔV_{opt}, which is determined based on the sizes of the flying capacitor and the parasitic capacitor [18] by using a pulse skipping scheme with a comparator, clock gating cell and voltage reference. The total loss of the DC-DC converter is minimized at ΔV_{opt}, and hence DC-DC converter efficiency is maximized. As illustrated in Figure 2.4, whenever the output voltage of the DC-DC converter, i.e. V_{out}, drops below the reference voltage, gclk toggles, and constant charge is transferred to the output, which equals $2 \cdot \Delta V_{opt} \cdot C_{fly}$. Therefore, the output current of the DC-DC converter is proportional to its effective gated clock frequency, implying that we can determine how much charge is flowing through the DC-DC converter by counting the gated clocks.

Since the dynamic current is proportional to the clock frequency, the following two equations can be derived by modulating the processor clock frequency occasionally between normal frequency and half of normal frequency to measure its leakage-to-dynamic current ratio.

$$I_{dyn}/2 + I_{leak} = 2 \cdot \Delta V \cdot C_{fly} \cdot f_{gclk\_slow} \quad (2.1)$$

$$I_{dyn} + I_{leak} = 2 \cdot \Delta V \cdot C_{fly} \cdot f_{gclk\_norm} \quad (2.2)$$

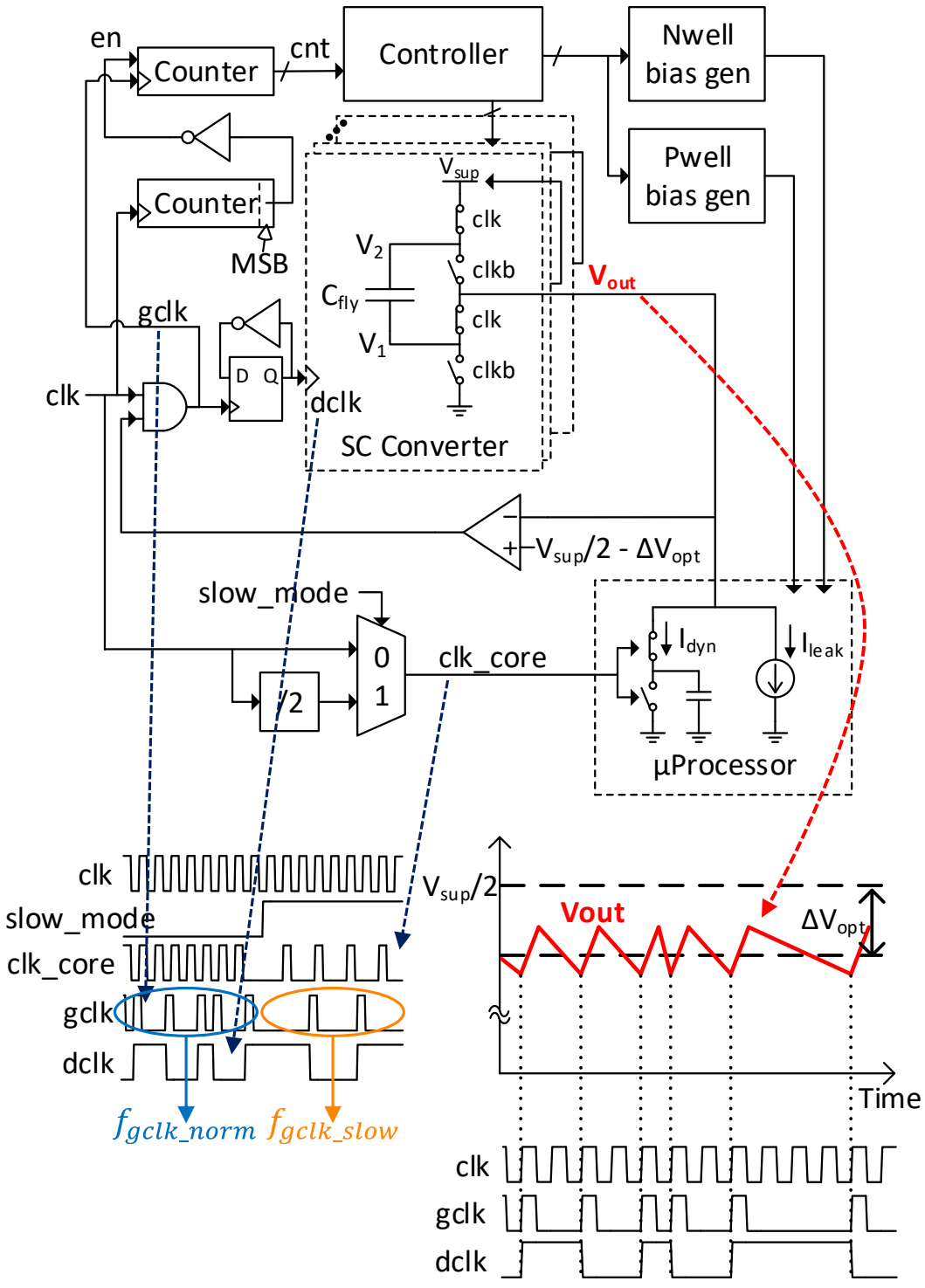


Figure 2.4 Proposed approach to measure the ratio of leakage power to dynamic power and achieve the desired ratio of CNT_{slow} and CNT_{norm}

We define CNT_{norm} and CNT_{slow} to be the number of gclk cycles counted during a given time period with normal frequency and half of normal frequency, respectively. Since the desired optimal leakage ratio is 1/5.6 for this system, the ratio of CNT_{slow}/CNT_{norm} ($R_{CNT\ 16}/FF_{16}$) should be 0.58 (i.e., $R_{CNT\ 16} = 94_{16}$), as derived in the following equations:

$$\frac{f_{gclk\_slow}}{f_{gclk\_norm}} = \frac{CNT_{slow}}{CNT_{norm}} \tag{2.3}$$

$$From\ (2.1), (2.2), (2.3), \frac{\frac{I_{dyn}}{2} + I_{leak}}{I_{dyn} + I_{leak}} = \frac{CNT_{slow}}{CNT_{norm}} \tag{2.4}$$

$$Since\ \frac{I_{leak}}{I_{dyn}} = \frac{1}{5.6} \rightarrow \frac{\frac{I_{dyn}}{2} + I_{leak}}{I_{dyn} + I_{leak}} = \frac{3.8}{6.6} = 0.58 \tag{2.5}$$

$$From\ (2.4), (2.5), \frac{CNT_{slow}}{CNT_{norm}} = 0.58 = \frac{94_{16}}{FF_{16}} \tag{2.6}$$

By tracking this optimal leakage ratio, the system determines if it is at the MEP with very low hardware and power overhead.

2.4 Implemented System

Figure 2.5 shows a detailed block diagram of the implemented system. The system has two power domains: 1.2 V and the DC-DC output power domain. The 1.2 V power domain supplies the DC-DC converter, body bias generators, clock generator, and controller. All of the blocks within this power domain use extremely low leakage (ELL) thick-gate-oxide devices to achieve low leakage power across all corners and temperatures. The DC-DC output power domain includes the target system, namely an ARM Cortex-M0 processor and associated 8 kB SRAM. Since SRAM is included in the same MEP tracking loop as the processor, a custom SRAM was designed to match the processor speed.

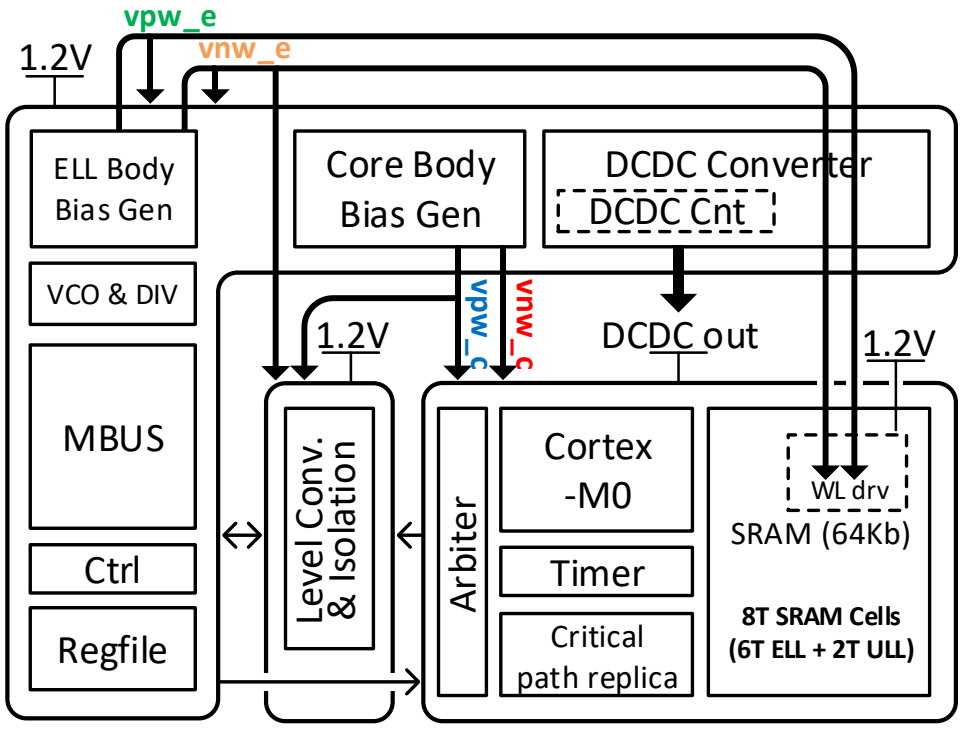


Figure 2.5 Top level block diagram

2.4.1 DC-DC Converter

The proposed system has a reconfigurable switched-cap DC-DC converter that is composed of 6 stages of 2-to-1 converters, a voltage reference, a non-overlapping clock generator, a clocked-comparator, a clock gating cell, and a 24-bit ripple counter as illustrated in Figure 2.6. The output resolution of the voltage reference is $1.2\ \mathrm{V}/2^7 \approx 10\ mV$, and consequently the same as for the DC-DC converter. By cascading 6 stages of the 2-to-1 converters, the DC-DC converter has a conversion ratio resolution of $1.2\mathrm{V}/2^6 \approx 20\ mV$, and hence it can guarantee high efficiency across a wide output voltage range [19], [20], which is required for energy-efficient operation of the whole system. In addition, due to the large V_{th} of ELL devices, we adopt a new body-controlled transmission gate for the configuration switches in the DC-DC converter to ensure small on-resistance and large off-resistance across all corners and a wide temperature range even when the intermediate voltage between the 2-to-1 converters is approximately half V_{DD}. When the body-

controlled transmission gate is turned off, its body is connected to V_{DD} for PMOS and ground for NMOS as normal. But when it is on, its body is shorted to the input node to achieve small on-resistance due to forward body bias. According to the simulation, on-resistance of the body-controlled transmission gate is approximately ×4000 times smaller than that of the common transmission gate of the same size when its input and V_{DD} is 0.6V and 1.2V, respectively.

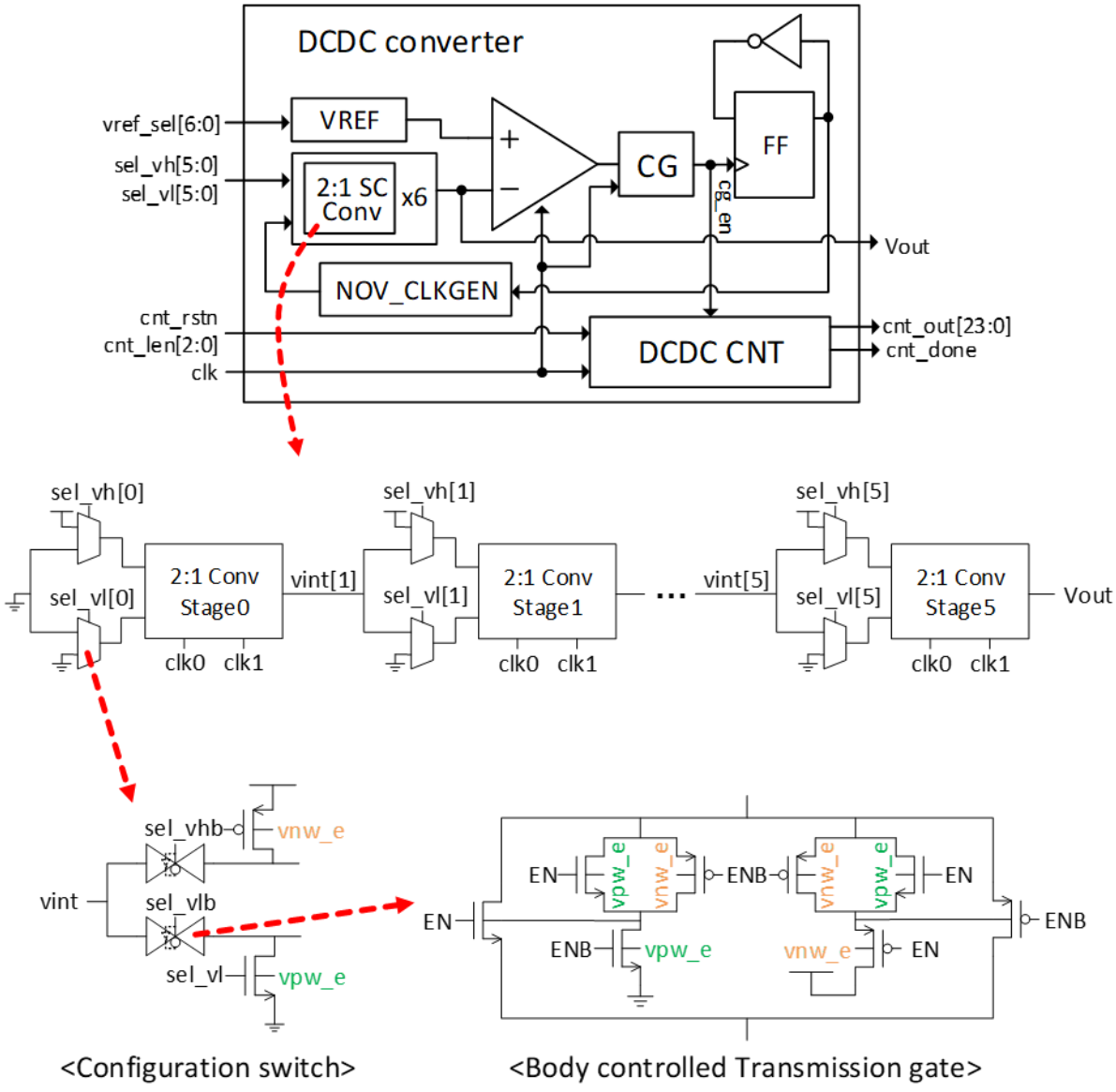


Figure 2.6 Block diagram of DC-DC converter with the schematic of body-controlled transmission gate

2.4.2 Body Bias Generators

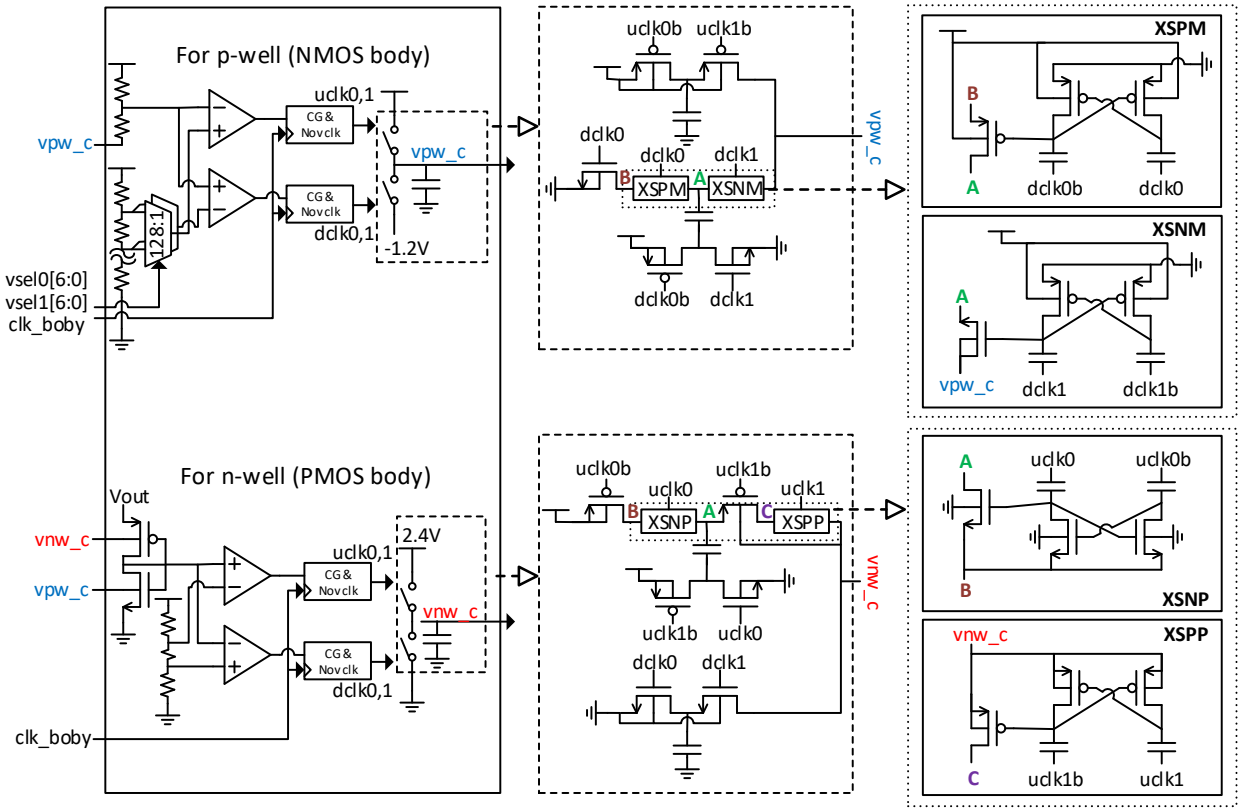


Figure 2.7 Body bias generator for the processor and SRAM

As shown in Figure 2.7, there are two charge-pumps for the processor and SRAM: one for p-well and the other for n-well. The output voltage ranges of the p-well and n-well charge-pumps are from -1 V to 0.3 V and from 0 V to 2.2 V, respectively. In the p-well charge-pump, a voltage reference sets the upper and lower boundaries of the p-well bias voltage, which is regulated through the feedback. On the other hand, the n-well charge pump automatically adjusts its output voltage to match the V_{th} of PMOS and NMOS [21], and hence, the system is able to compensate for skewed corners as well. Also, from a system level point of view, since the n-well body bias voltage can be deducted from the parameters that a controller should handle, the system can be simple; there are two parameters left to be controlled, i.e. V_{DD} and the p-well bias voltage. The local mismatch of the two stacked diodes in the n-well charge pump to sense the difference in V_{th} of

PMOS and NMOS could impact the system performance, in contrast with the local mismatch of all other gates the power of which tends to average out to its mean value in the whole system's power. Hence, larger transistors were used for the two stacked didoes. The charge pumps were also designed to avoid leakage paths through the power and/or body since the system supports both forward and reverse body bias to enable MEP operation across all process and temperature corners. In each charge-pump, there are an up-pump and a down-pump, whose operations are mutually exclusive. When pumping charge down, the down-pump is running while the up-pump is turned off. In this case, for the p-well charge-pump, two PMOS transistors in the up-pump effectively cut off the path from the body to V_{DD}. But when pumping charge up, the up-pump is running and the down-pump is turned off, and there is a leakage path from the body to ground through the source to the well junction diode in the XSNM switch. Hence, we added an additional NMOS transistor in the down-pump to cut-off that path. Similarly, two additional PMOS transistors were added to the n-well charge-pump.

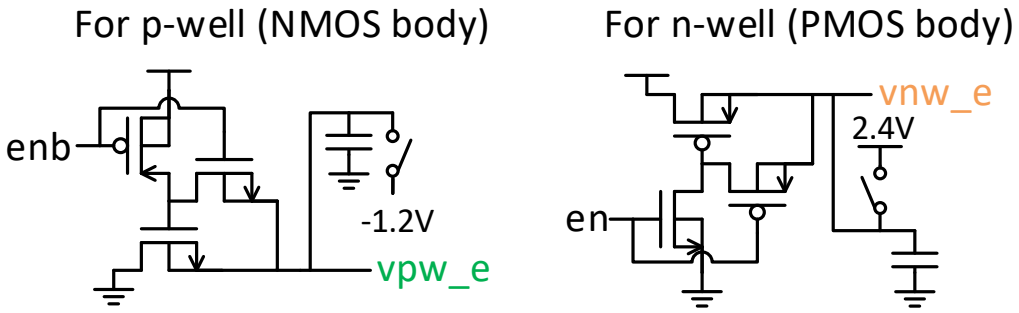


Figure 2.8 Body bias generator for the 1.2 V domain block with 3-transistor switches

Body bias generators for ELL devices are designed for reverse body bias only, and hence it uses a down-pump and an up-pump from the p-well bias generator and n-well bias generator, respectively, for the processor. In addition to that, to prevent a current path from the body to power or ground when the charge pumps are running, 3-transistor switches are used as shown in Figure

2.8. By default, the charge pumps for ELL devices are turned off, and the 3-transistor switches are turned on. At extremely high temperatures, such as 125°C, and at the FF corner, where the leakage of ELL devices becomes significant, this body bias generator is enabled to limit leakage.

2.4.3 SRAM

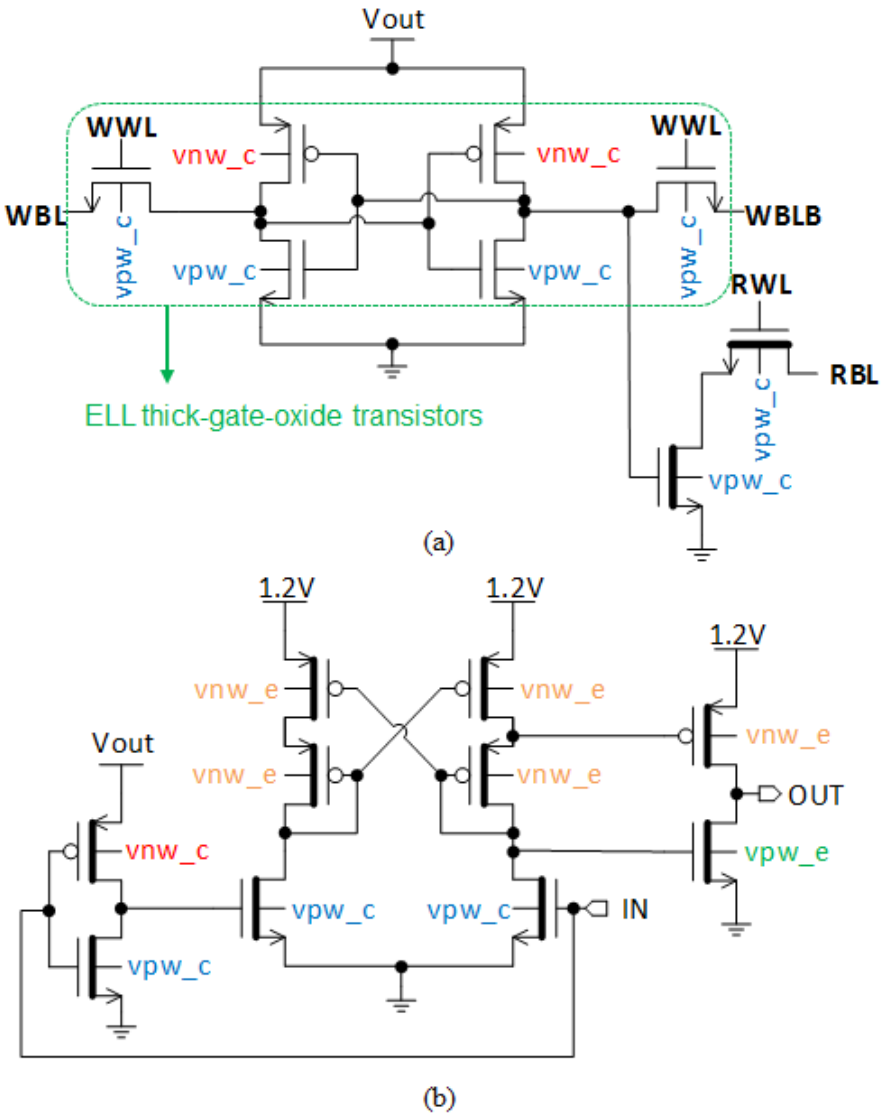


Figure 2.9 (a) SRAM 8T bitcell (b) Level converter for word line drivers

A custom 8-kB SRAM is implemented to support the Cortex-M0 processor. To minimize the leakage power, the SRAM bit cell was designed with ELL thick-gate-oxide devices as shown

in Figure 2.9(a). In the proposed system, since the processor and SRAM share the same power domain, the SRAM was designed to match processor speed for all possible combinations of supply voltage and body bias voltage. To accelerate its read speed, therefore, an 8T SRAM bit cell was adopted, and its read path was designed with thin-gate-oxide transistors despite the area penalty due to the design rules between two different types of transistors. Word line drivers are boosted using the 1.2 V supply to accelerate the write speed as well as the read speed. Hence, level converters are required to connect the input signals in the DC-DC output power domain to the word line drivers. Since the speed of the level converters must be fast enough and follow the same trend depending on the supply voltage and body bias voltage as the processor, a split-control level converter was adopted [22] with its body of two input NMOS transistors connected to vpw_c (body bias for the processor), as shown in Figure 2.9(b).

2.5 Control Algorithm

Figure 2.10 describes the control algorithm to find the MEP of the system. The target range of $R_{CNT\,16}$ (explained in the chapter 2.3 Architecture for Measurement the Ratio) is 90_{16}–98_{16}, within which the operating power is within 4.6% of optimal. For $R_{CNT\,16}$ greater than 98_{16}, the leakage power is too large, indicating that we should increase V_{DD} and apply further reverse body bias. On the contrary, for $R_{CNT\,16}$ smaller than 90_{16}, the leakage power is too small, indicating that we should apply further forward body bias first before decreasing V_{DD} to prevent the processor from exiting its functional voltage window; the further forward body bias applied beforehand must compensate or overcompensate for the following V_{DD} reduction, and therefore we set the amount of further body bias with a sufficient margin. A critical-path replica is used to detect how close to the boundary of the functional voltage window the processor is operating. Two thresholds for the number of errors detected, which are statistical sampled with multiple observations, on the path

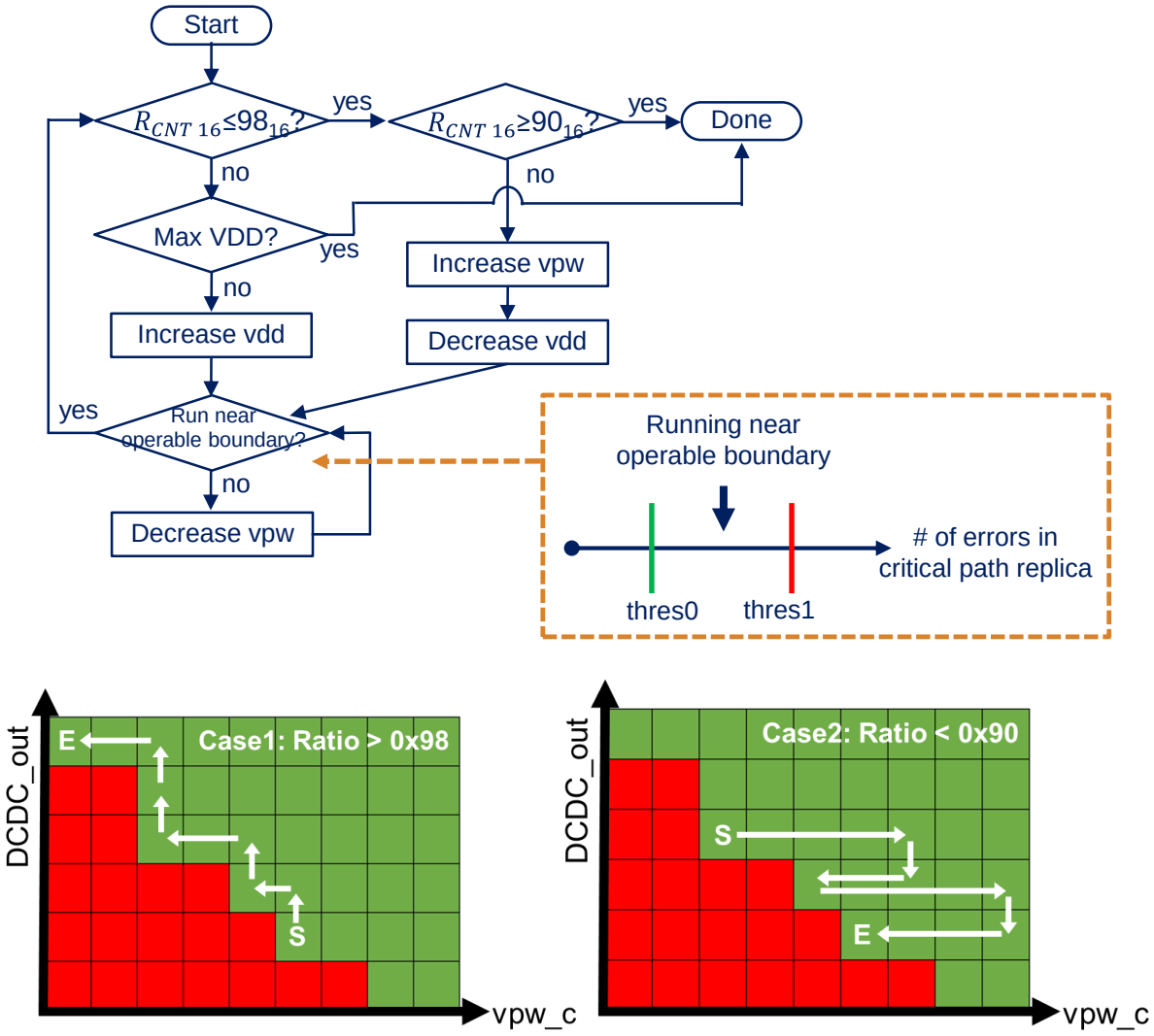


Figure 2.10 Algorithm describing system operating loop and two example cases

delay of this replica circuit are used to tune the processor close to the maximum operating frequency while maintaining functionality. Also note that the critical-path replica necessitates a margin for mismatch and this margin is more significant at low voltage. Therefore, critical-path replica was designed to be have a wide tunable range and tuned to have a large margin.

Figure 2.11 includes oscilloscope traces demonstrating the fully automated control loop running on the test chip. The system finds the MEP at 60°C from a default non-optimal starting point. Then, as temperature gradually changes from 60°C to 10°C, the system automatically adjusts its V_{DD} and body bias in the direction of the MEP. As the temperature drops, the leakage power is

reduced and forward body bias is automatically applied to maintain the optimal leakage ratio, while V_{DD} is decreased to lower dynamic power. These changes are made while maintaining safe operation in the functional voltage window using the critical-path replica.

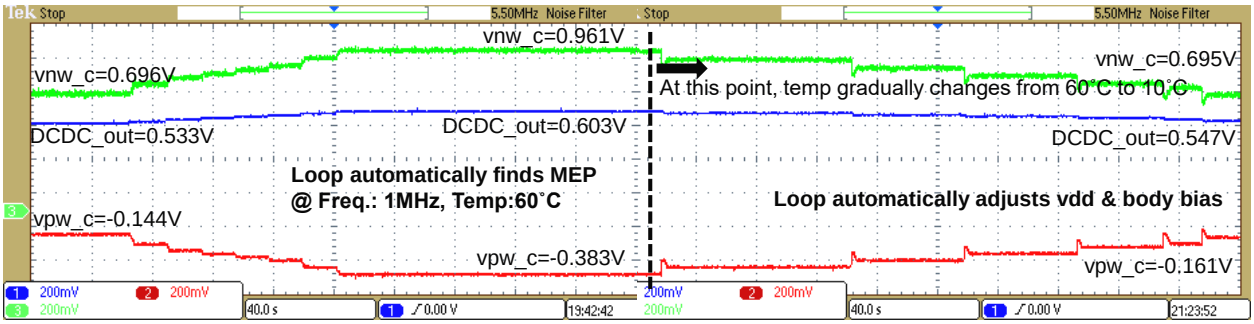


Figure 2.11 Measured automatic adjustment for DC-DC output voltage and body bias

2.6 Measurement Results

The design was tested at TT/FF/SS/FS/SF corners as well as across a wide temperature range from -20°C to 125°C. Various target frequencies were chosen ranging from 100 kHz to 6 MHz; the DC-DC converter designed with ELL thick-gate-oxide transistors had a maximum frequency of 6MHz, which also limited the system frequency to 6MHz. In Figure 2.12, the red bars indicate the power consumption on the left y-axis, and the blue bars indicate the ratio of power using the proposed approach to the true MEP found via exhaustive search. Since the frequency is fixed at 1 MHz, power is equivalent to the energy. The amount of energy per cycle varies with the corner and temperature, with FF corner at 125°C having the worst energy-per-cycle value due to its extreme leakage, as shown in Figure 2.12. Finally, the proposed approach achieves power consumption within 4.6% of optimal at 1 MHz across all mentioned processes and temperatures.

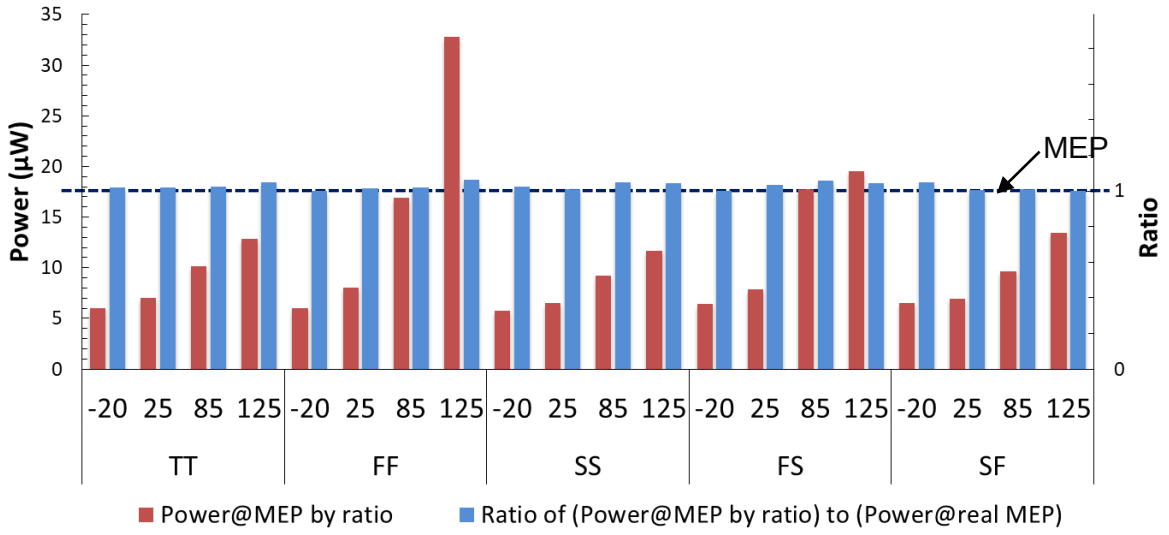
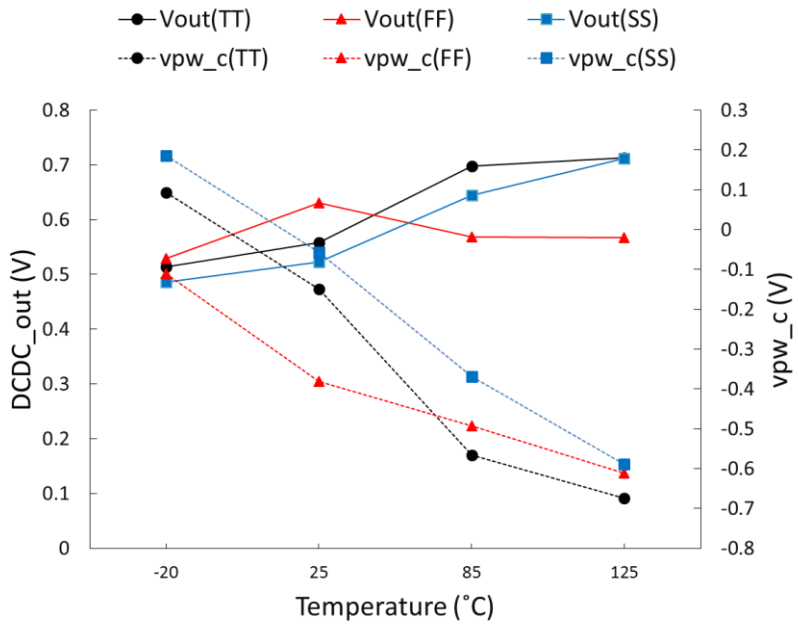
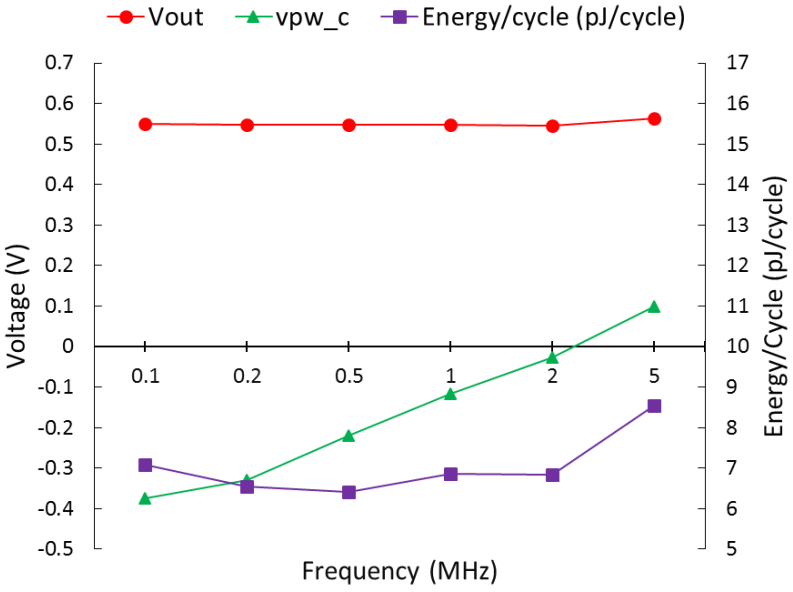


Figure 2.12 Power measurement across process and temperature

Figure 2.13 shows the optimal V_{DD} and body bias values across target frequencies and temperatures. As the temperature increases, to maintain a constant frequency, the system calls for a larger V_{DD} and applies more reverse body bias to suppress the exponentially rising leakage. But at high temperature and FF corner, even significant reverse body bias cannot effectively suppress leakage. Hence, the system is always leakage-dominated and cannot achieve the desired leakage ratio. At a fixed temperature, the optimal V_{DD} is nearly constant, while body bias adjusts as frequency varies as shown in Figure 2.13 (b).



(a)



(b)

Figure 2.13 (a) DC-DC output voltage and vpw_c (Pwell body bias for the processor and SRAM) measurement across temperature (clock frequency: 1 MHz) (b) DC-DC output voltage, vpw_c, and energy/cycle measurement across frequency (TT corner, 25°C)

In Figure 2.14, the Shmoo plot shows that R_{CNT} gradually changes according to the V_{DD} and body bias and indicates the optimal value at the selected operating point, which is right next to the optimal point picked by optimization. The pie chart gives the power breakdown of the system in Figure 2.15. Together, the processor, SRAM, and DC-DC onverter consume about 92% of the total power. In addition, clock generation and interface with other parts of the system account for 7% of power consumption, and body bias generation and the MEP controller are responsible for the remaining 1.2%. Overall, the overhead from the proposed approach is estimated to be about 1.2% including the body bias generation.

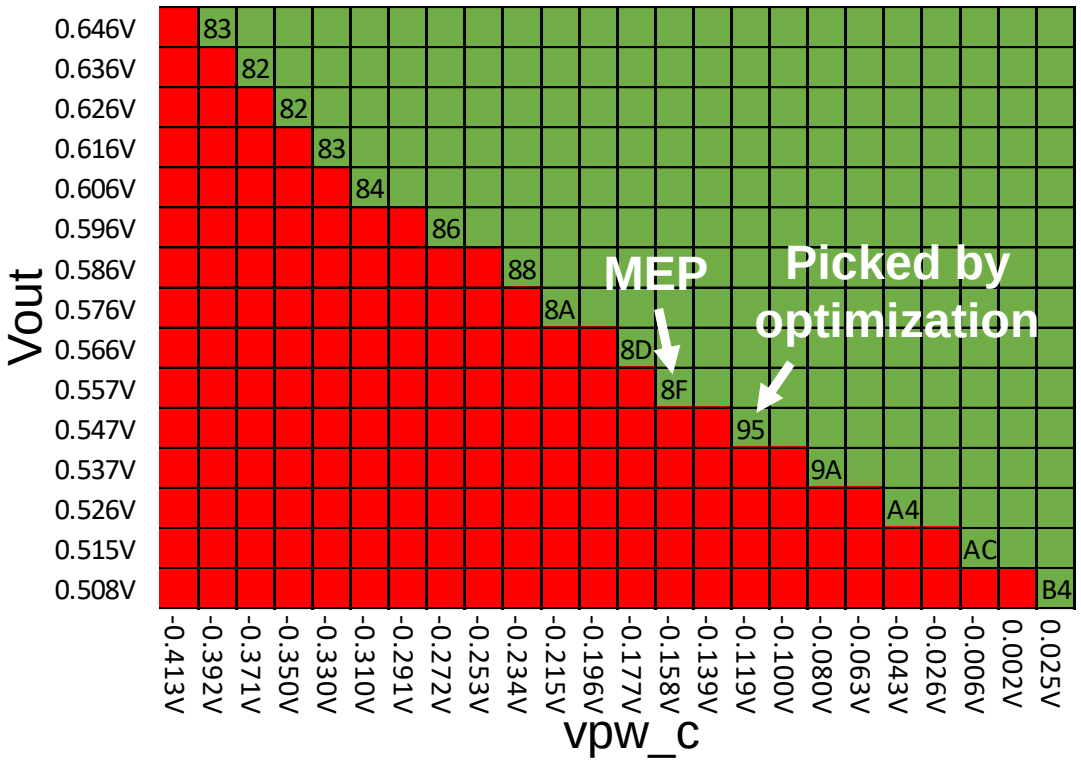


Figure 2.14 Shmoo plot with R_{CNT} distribution across operating points (TT corner, clock frequency: 1 MHz, 25°C)

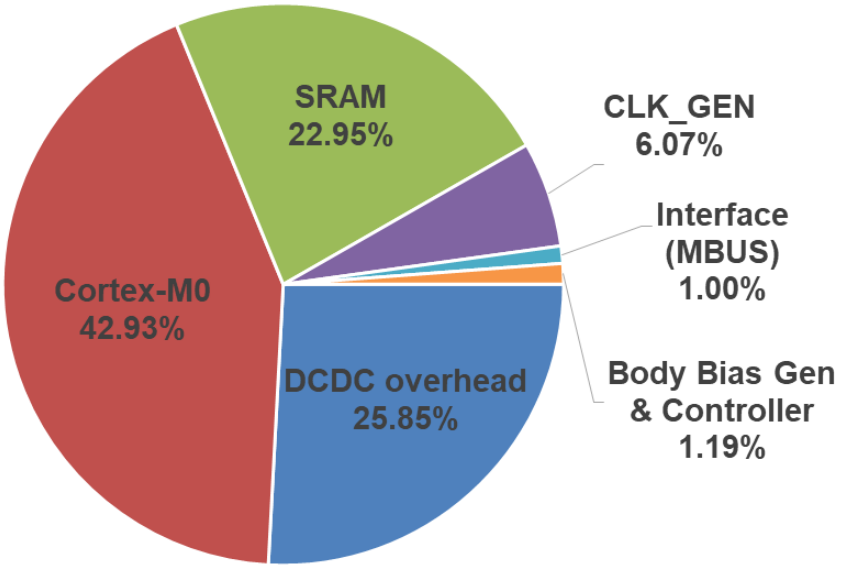


Figure 2.15 1.2 V power breakdown (TT corner, clock frequency: 1 MHz, 25°C)

Table 2-1 Comparison Table of IoT Processors

	This work	Myers [23]	Bol [24]	Salvador [25]	Lallement [26]	Bol [6]
Technology	55nm	65nm	65nm	90nm	22nm FD-SOI	28nm FD-SOI
CPU	ARM Cortex-M0	ARM Cortex-M0+	MSP430 compatible (16b)	ARM Cortex-M3	ARM Cortex-M0+	ARM Cortex-M0
Dynamic power management	On-chip Closed-loop MEP-tracking	On-chip Closed-loop Voltage-scaling	On-chip Closed-loop Voltage-scaling	On-chip Closed-loop Voltage-scaling	Off-chip Open-loop Adaptive-bodybias	On-chip Closed-loop Adaptive-bodybias
Tested Corners	TT,FF,SS,FS,SF	TT	TT,FF,SS	TT,FF,SS,FS,SF	N/A	TT
Tested Temperature	-20°C ~ 125°C	25°C ~ 70°C	-40°C ~ 85°C	-40°C ~ 120°C	-10°C ~ 60°C	25°C
Low Voltage Memory	8Kbyte	8Kbyte	none	none	12 KB	32 KB
Operating Voltage	0.48V ~ 0.75V	0.19V ~ 1.2V	0.32V ~ 0.48V	0.5V ~ 1.0V	0.4V ~ 0.8V	0.4V
Operating Frequency	100kHz ~ 6MHz	29kHz ~ 66MHz	8MHz ~ 71MHz	1MHz ~ 20MHz	13MHz ~ 651MHz	40MHz ~ 80MHz
Minimum Energy Per Operation	6.4pJ/cycle @ 0.55V, 500kHz	11.7pJ/cycle @ 0.35V, 750kHz	7pJ/cycle @ 0.4V, 25MHz	23pJ/cycle @ N/A, 5MHz	1.13pJ/cycle @ 0.42V, 20MHz	3pJ/cycle @ 0.4V, 48MHz

Table 2-1 compares this design to other small IoT processors. The proposed approach offers closed-loop MEP-tracking via clock frequency modulation embedded in the DC-DC converter and the lowest energy consumption, 6.4pJ/cycle, among the listed commercial processors. Figure 2.16 provides the die photo and the sensor node platform that adopts the proposed system.

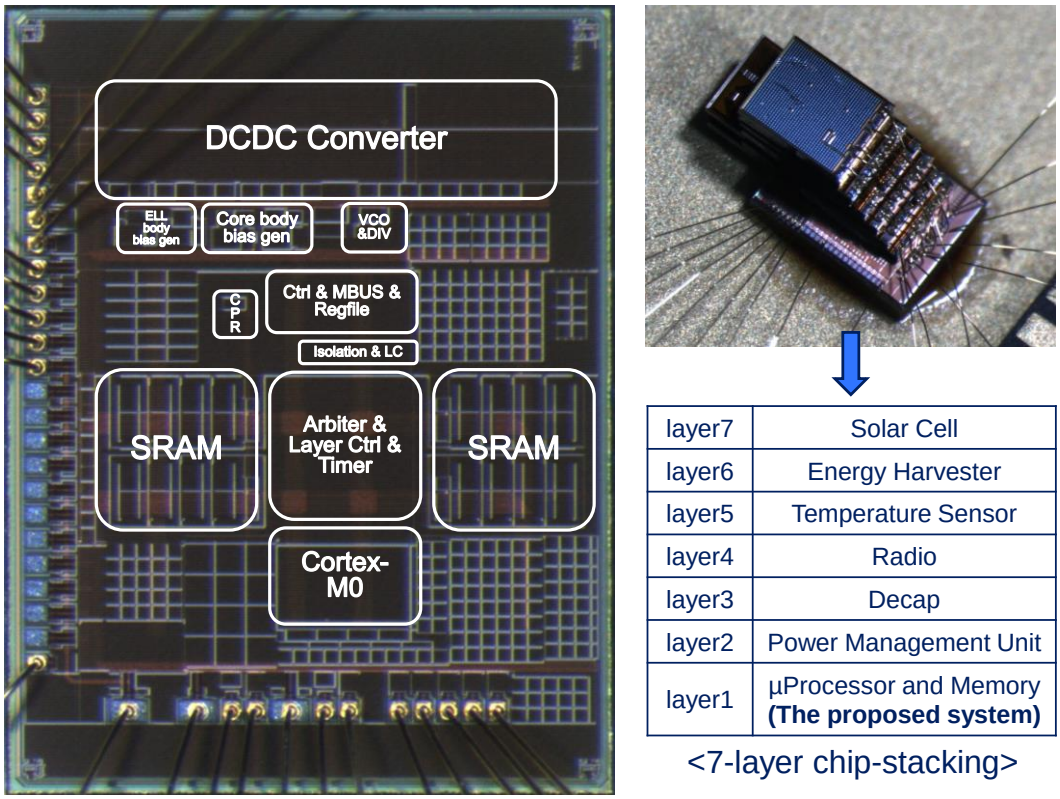


Figure 2.16 Die photo and sensor node platform that adopts the proposed self-tuning µprocessor system

2.7 Feasibility across Technology

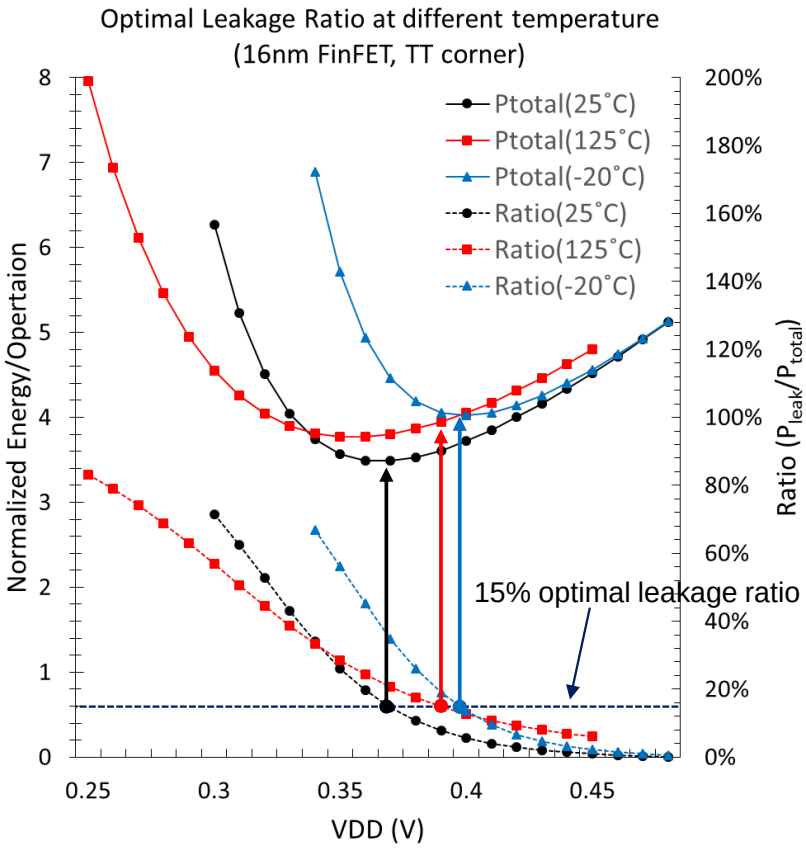


Figure 2.17 A 15% ratio yields energy/operation minimum at 25°C, -20°C and within 4.7% from the minimum at 125°C (TT corner, 16-nm FinFET process)

In order to check the applicability of the proposed ratio-based MEP approach to other technologies, we simulated a typical digital circuit in a 16-nm FinFET process. Since the body coefficient of this process is too small to exploit ABB, only DVS is applied and hence frequency depends solely on the supply voltage. Figure 2.17 describes the results. The proposed ratio-based MEP method achieves minimum energy/cycle at −20°C and 25°C, but it yields 4.7% higher energy/cycle than its minimum at 125°C with TT corner. We also simulated SS and FF corners at −20°C, 25°C, and 125°C. A fixed ratio of 15% yields energy/operation within 1% from the minimum except for only two cases: 4.7% (TT 125°C) and 26% (FF 125°C). This simulation

result shows that the optimal leakage ratio deviates from the normal levels when leakage is very high; in the DDC process, this can be somewhat compensated for using reverse body bias, however only up to its maximum value. Hence, these simulation results support that the proposed ratio-based MEP approach can be also applied to the advanced FinFET process; however, results can be improved using some correction when leakage is dominant, such as at very high temperatures and/or in fast process corners. Also note that running the circuit on the MEP with scaling V_{DD} only leads to unguaranteed clock frequency and speed. This can be acceptable in some applications but needs to be assessed carefully. In addition, the proposed technique would be easily applicable to the fully depleted silicon on insulator (FD-SOI) process that has the ability to be used with a wide range of body biasing [9].

2.8 Conclusion

In this chapter, the concept of optimal leakage ratio is introduced. Based on that, a runtime MEP tracking system is implemented in Cortex-M0 processor with a custom DC-DC converter, body bias generators and SRAM in 55-nm DDC process. The proposed approach requires very low area and power overhead, and achieves 6.4 pJ/cycle at 0.55V and 500 kHz clock frequency. Further, the introduced optimal leakage ratio technique is shown to be applicable to advanced FinFET technologies as well as the DDC process of the test chip.

Chapter 3 **A µProcessor Layer for mm-Scale Die-Stacked Sensing Platforms Featuring Ultra-Low Power Sleep Mode at High Temperature**

3.1 Introduction

Miniaturized wireless sensor nodes are inherently energy constrained due to their small form factor batteries, and thus must be designed with ultra-low power consumption to ensure sufficient lifetime [23], [24]. Recently, mm-scale wireless sensor nodes have become viable for emerging applications that experience high temperatures, such as down-hole sensors for shale oil mining; these devices log temperature and pressure during hydraulic fracturing [25]. High temperatures significantly deteriorate sensor lifetime, largely due to exponential leakage increases. Therefore, it is necessary to improve the energy efficiency of such sensors at high temperature. Leveraging the intermittent data processing in most sensing applications, duty cycling via power gating is typically used to reduce overall energy consumption. In this case, the sleep power will dominate the overall energy consumption because the sensor will be in sleep mode most of the time. At high temperature, due to the increased leakage current, the sleep power becomes more dominant in the overall energy consumption as shown in Figure 3.1. The sleep power is mainly determined by the always-on components, such as program and data memories required to hold its data even in sleep mode. While embedded non-volatile memories are appealing for their near zero-power retention, they have high write energy and often have low endurance at high temperature such as 125˚C, introducing memory refresh overhead. In the proposed system, therefore, we deploy an always-on custom SRAM that is deliberately shifted to the slow corner by the foundry to minimize memory leakage while maintaining bitcell size. An integrated compact DC-DC

converter and negative body-bias charge pump in the SRAM enables the primary power management unit (PMU) for the entire sensor node to be shut down during sleep mode, significantly reducing overall leakage at high temperature.

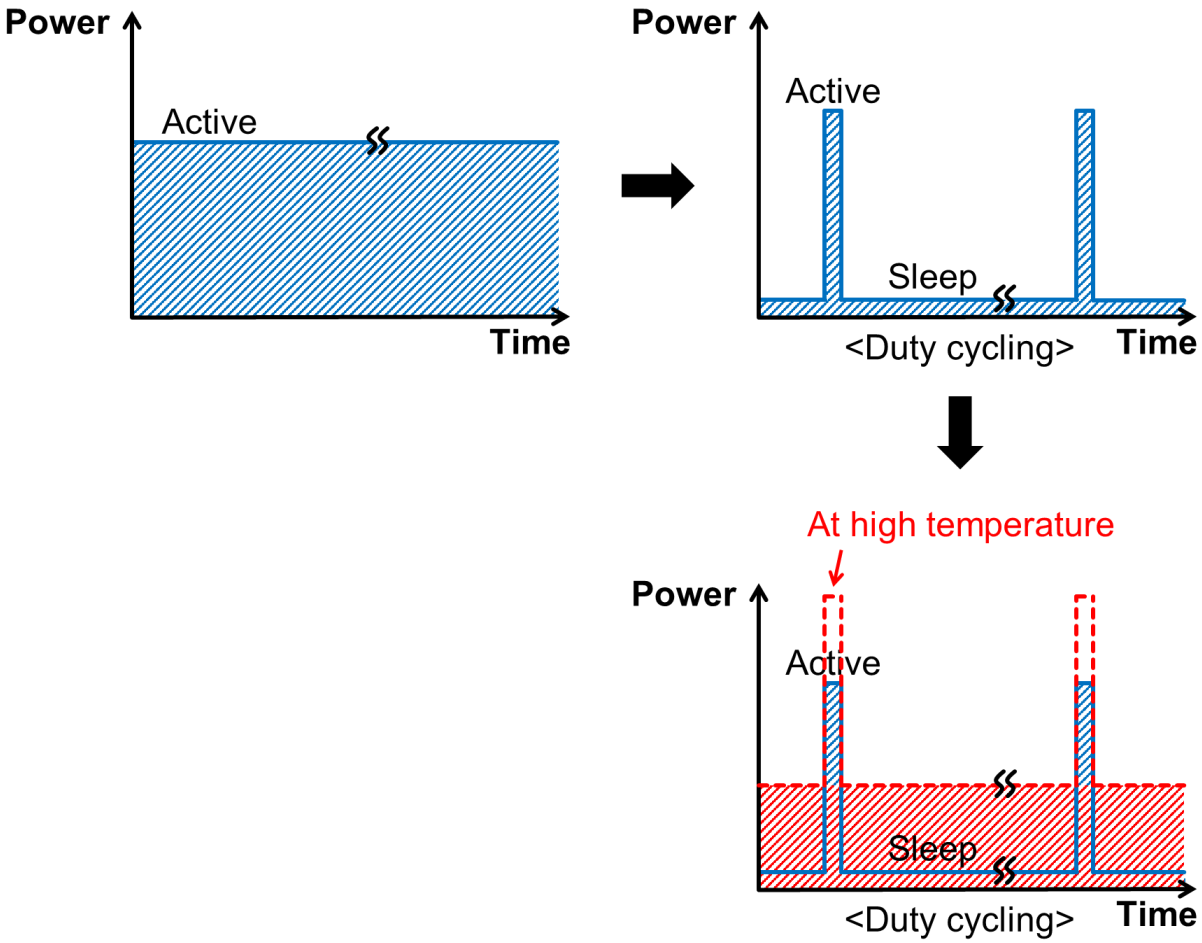
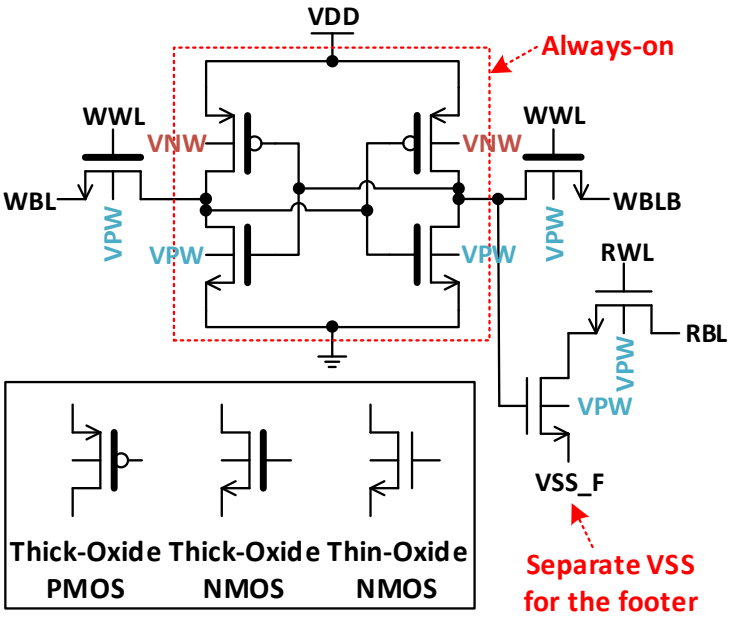
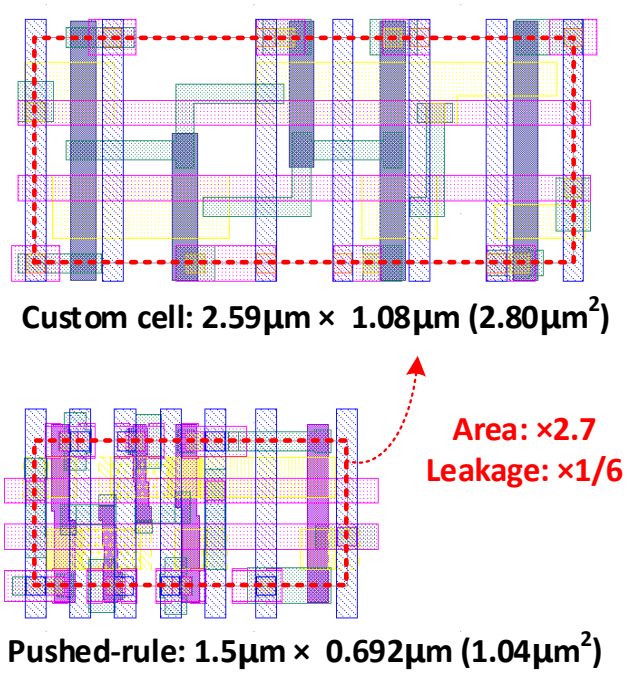


Figure 3.1 Duty cycling via power gating reduces energy consumption. In this case, the sleep power dominates the overall energy consumption. At high temperatures, the sleep power becomes more dominant in the overall energy consumption.

3.2 Low Leakage SRAM design



(a)



(b)

Figure 3.2 8T SRAM bitcell: (a) schematic (b) its layout

Figure 3.2 shows the schematic and layout of the 8T SRAM bit cell deployed in the proposed system. Since the target application has 0.6V and 1.2V supply voltages, the SRAM operates at 0.6V. The cross-coupled inverters that hold data are designed with thick-gate-oxide transistors as the sub-fW leakage targets are infeasible using thin oxide devices due to both their higher subthreshold and gate leakages. On the fabrication side, the wafer is shifted to the slow corner for about 4× leakage reduction by thinning the undoped layer and increasing the dopant concentration of the screen layer in the DDC transistor [13] as described in Figure 3.3. The layout is drawn using logic rules rather than pushed rules, sacrificing 2.7× area for 6× lower leakage. The measured SRAM cell leakage is 0.89fW/bit and 1.4pW/bit at 25˚C and 125˚C, respectively. To our knowledge, this represents the first sub-fW SRAM bit cell as shown in Figure 3.4. The cell area is also competitive when accounting for the fact that thick-gate-oxide transistors do not scale as well as thin-gate-oxide transistors in advanced technologies.

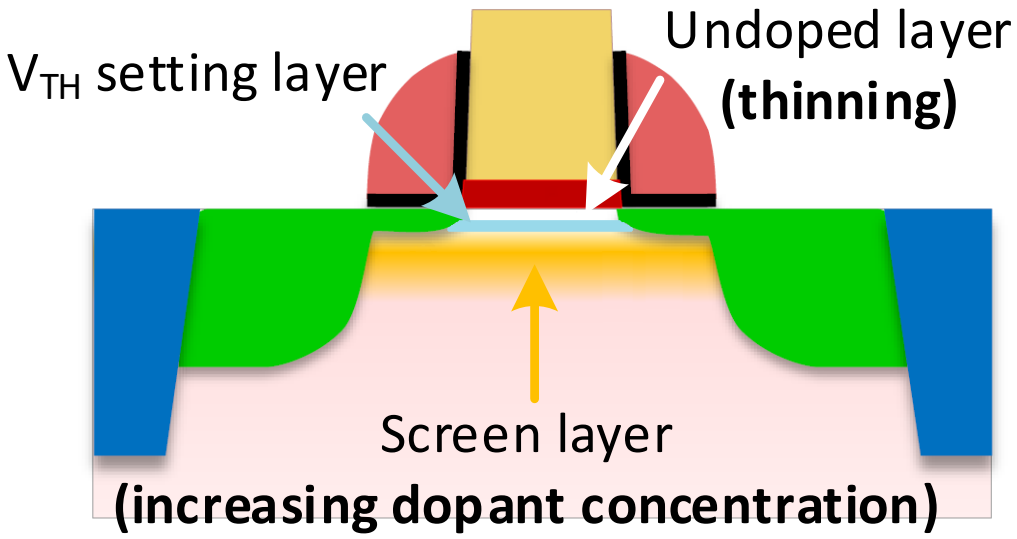


Figure 3.3 An adjusted fabrication process in a DDC transistor for leakage reduction

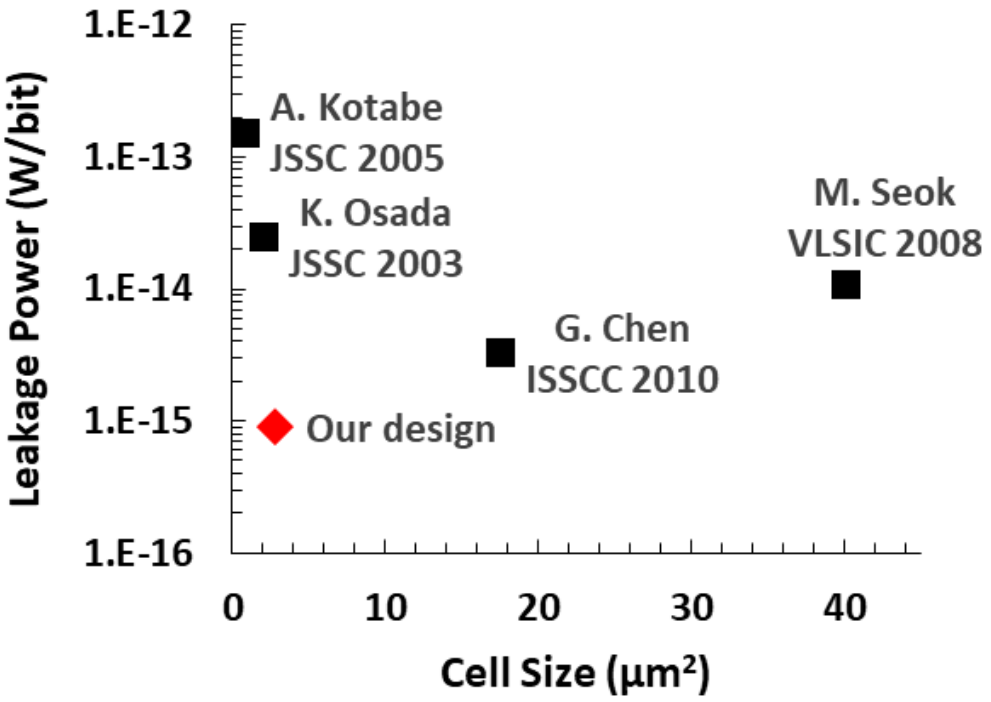


Figure 3.4 SRAM bitcell leakage comparison scatter plot with the previous work at 25˚C (measurement) [20], [30], [30], [30]

At high temperature, parasitic BJT leakage shown in Figure 3.5 can be triggered by small voltage differences between source/drain and p/n-well bias caused by IR drop. Previous test chips showed that this parasitic BJT leakage current can be significant (~1µA). To avoid this potential leakage, the system generates a negative p-well body bias (VPW) and an n-well body bias (VNW) higher than VDD during the sleep mode. These biases are applied to the SRAM array to ensure the emitter-base junctions remain reverse biased at all times. In addition, according to the measurement results shown in Figure 3.6, this reverse body biasing further reduces SRAM sub-threshold leakage, canceling the power overheads of generating the bias voltages. The leakage power from SRAM VPW node in Figure 3.6 includes overhead of negative voltage generation. Word-line drivers are boosted using 1.2V supply to compensate for slow transistors. The two thin-gate-oxide read transistors are power-gated by a header and footer and act to accelerate read speed

by 30×. Note that a footer is necessary to eliminate junction leakage from p-well to NMOS grounded source in the read transistors, which reduces −0.1V VPW generation power by 39% according to the simulation results.

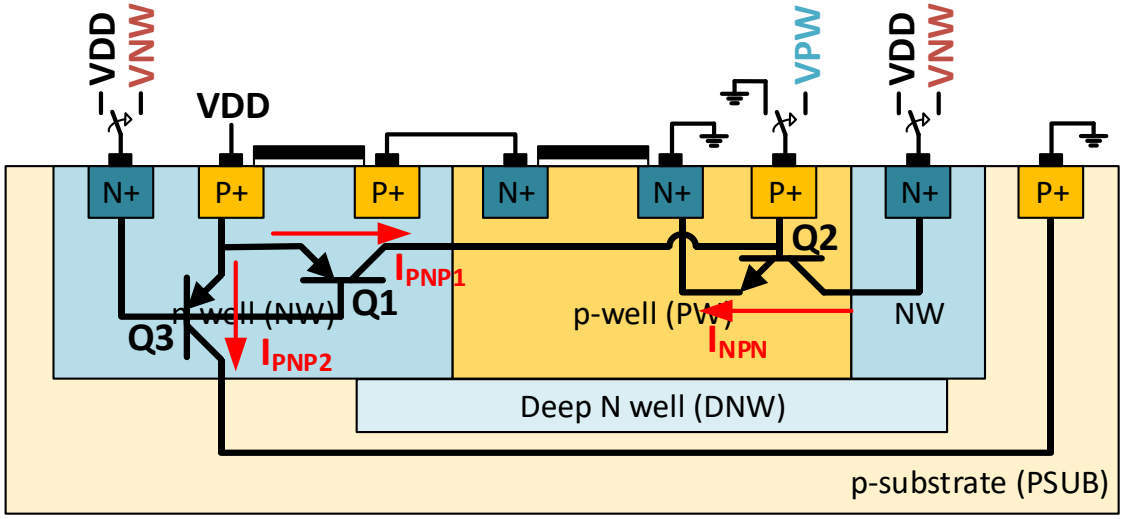


Figure 3.5 Body biasing for the SRAM cell array to reduce the leakage through the parasitic BJTs

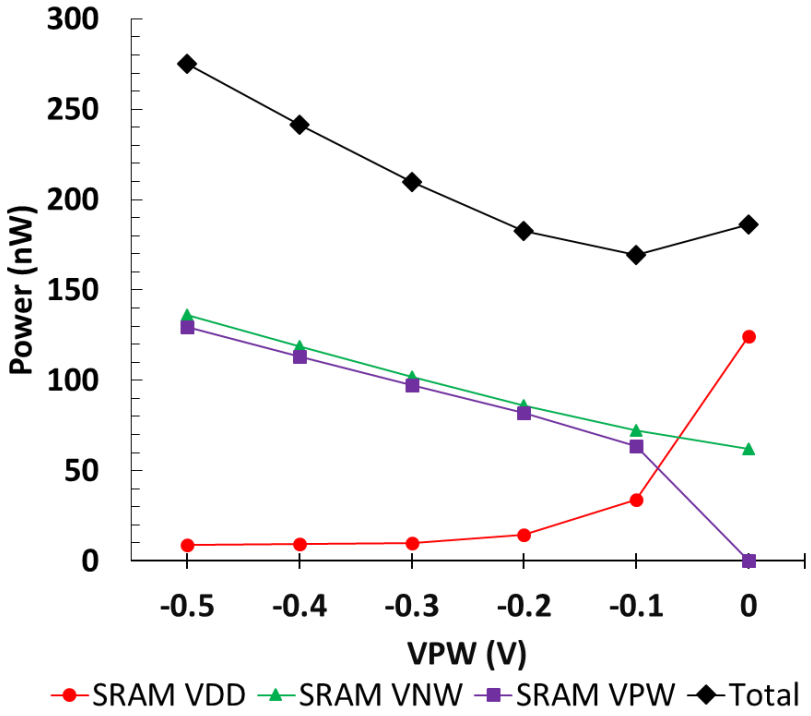


Figure 3.6 SRAM leakage power measurement from each node with reverse body biasing at 125˚C (measurement)

3.3 Proposed µProcessor System

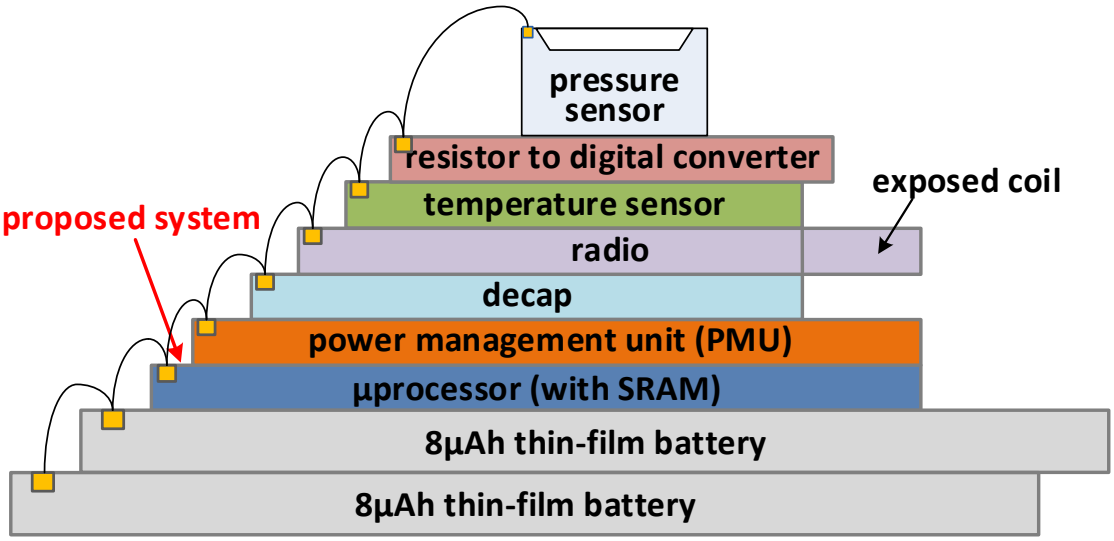


Figure 3.7 mm-scale die-stacked wireless sensing platform with the proposed µprocessor layer

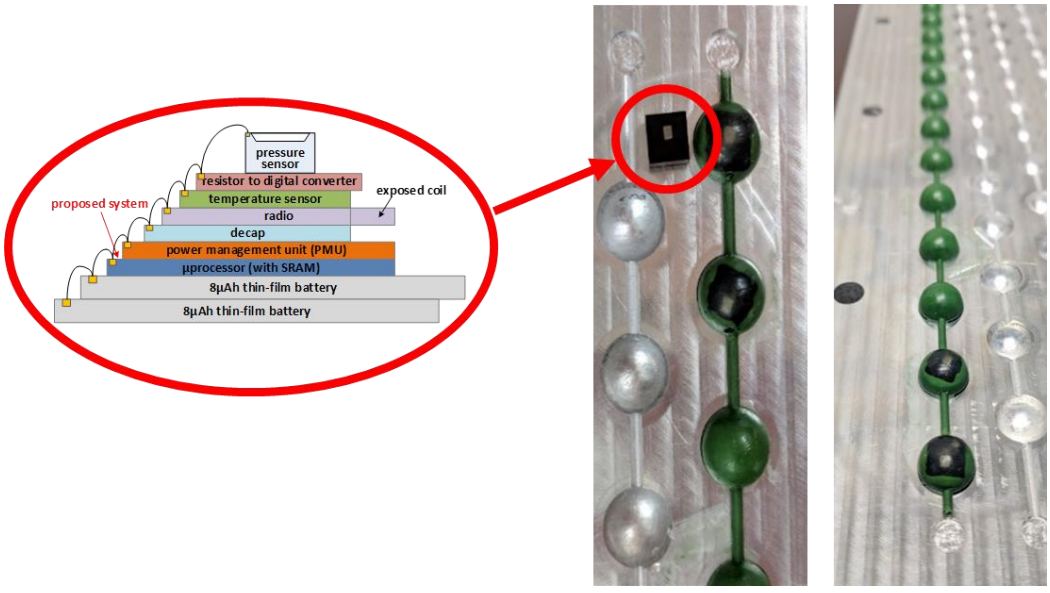


Figure 3.8 Encapsulation of the sensors

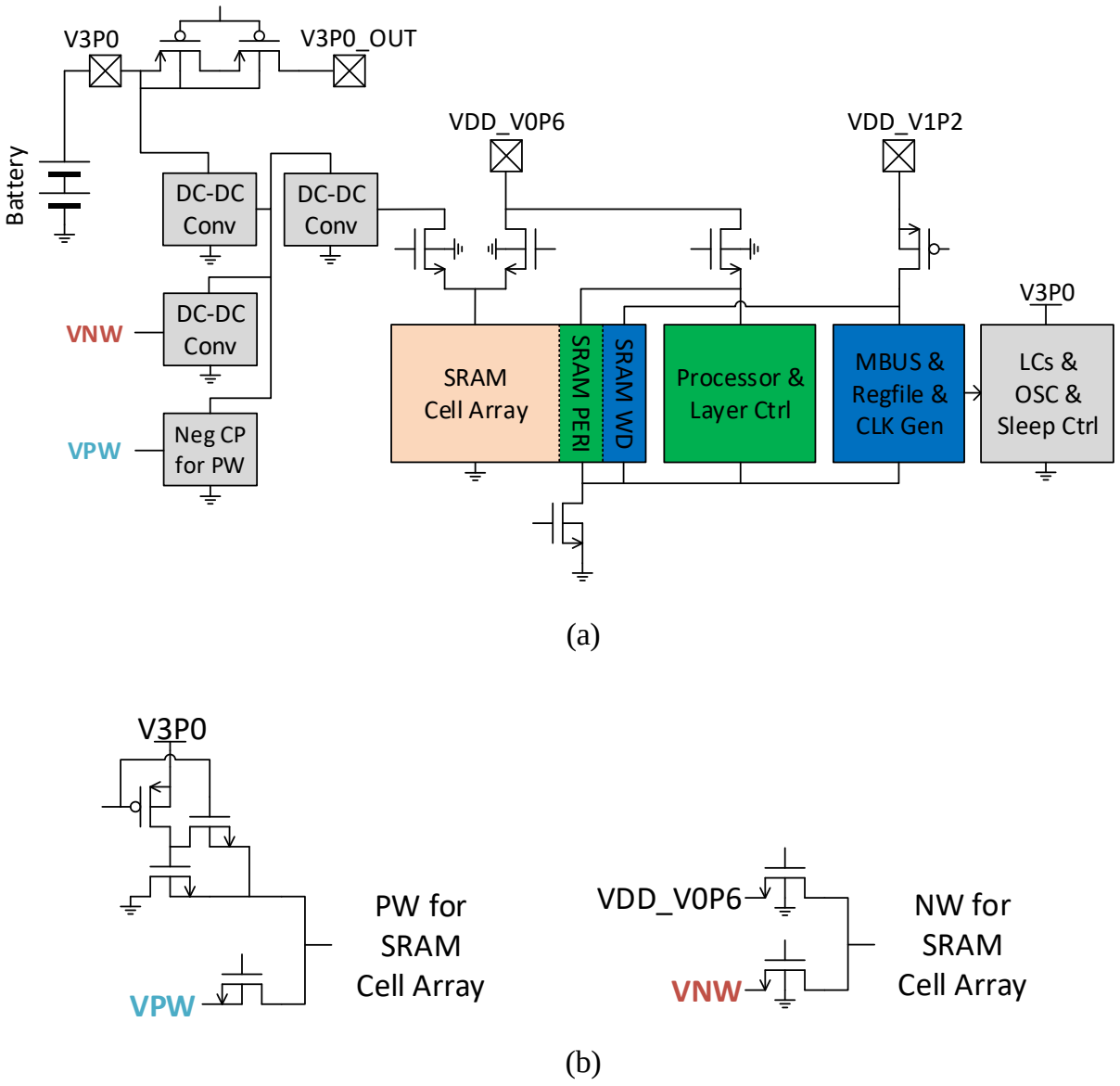


Figure 3.9 (a) Overall block diagram of the proposed system, (b) Switches for SRAM cell array body biasing

As a master layer for the mm-scale die-stacked sensing platform depicted in Figure 3.7, the proposed system in Figure 3.9 includes a Cortex-M0 processor with a custom SRAM, a sleep controller, a power gate for the battery, a negative charge-pump, and DC-DC converters. Since the complete stacked system is encapsulated by a metal or epoxy package after die-stacking as shown in Figure 3.8, each layer has an intentionally reduced ESD circuit since it only needs to protect for stress during wire-bonding. At 125˚C, even small ESD power clamps and IO cells leak

significantly (>80nW per each layer). Therefore, the proposed system completely cuts off battery power for all the other layers during the sensor's sleep mode. Consequently, 0.6V and 1.2V layer power from the PMU is not available during the sleep mode. Hence, the proposed system internally generates power for SRAM data retention with a dedicated DC-DC converters which consists of 2:1 switched-capacitor converters with a regulation loop and a negative charge pump. All power gate switches depicted in Figure 3.9 are controlled by the sleep controller. The power gates for 0.6V domain are designed with NMOS transistors because the gate control signal comes from the sleep controller powered by the battery (>2.2V). Since the sleep controller is always-on, it is designed with the least leaky IO devices trading off area for power. The sleep controller also controls the reset signals for other blocks. To prevent a current path from the p-well to ground when VPW is at negative voltage, a three-transistor switch is used as depicted in Figure 3.9 (b) [26].

The pie chart in Figure 3.10 shows the sleep power breakdown at 125˚C; DC-DC converters and a charge-pump supplies the SRAM at around 50% efficiency. As an example of use-case, a program alternates the system between sleep and active mode. Once the processor wakes up from the sleep mode, a variable assigned to the memory initialized during the program loading is increased by 1 and its value is sent out through Mbus [27] to demonstrate correct data retention, as shown in Figure 3.11. Figure 3.12 shows a die photo and chip summary. The total sleep power of the proposed system is 0.54μW at 125˚C which is 5× better than previously implemented M^3HT system [25] while increasing SRAM by 5.3×, marking 26× better sleep power per SRAM bit. Since the sleep controller shuts-off all other layers in the system, it produces a

constant standby power, regardless of the number of layers in the system making it applicable to simple and complex systems alike.

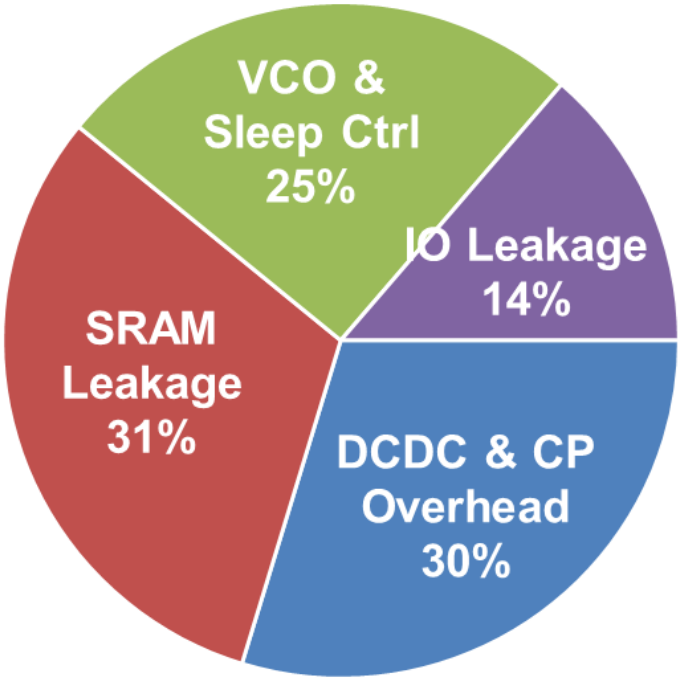


Figure 3.10 Sleep power breakdown at 125˚C (measurement)

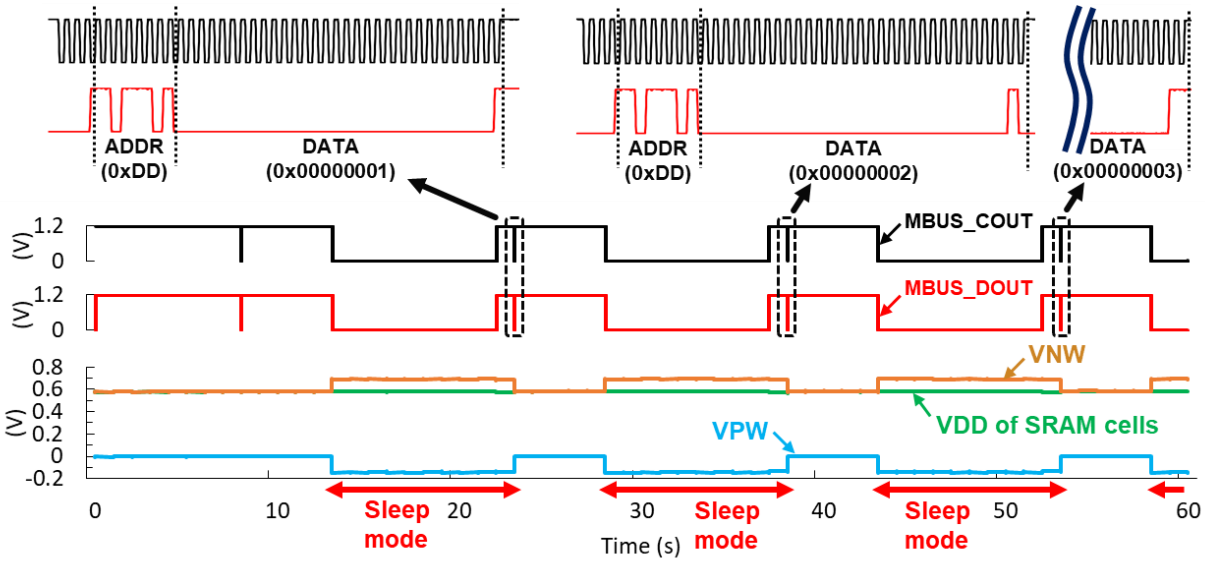


Figure 3.11 Measured waveform for monitoring mode change (Wake-up→Sleep→Wake-up→...) at 125˚C; The µprocessor sends a message on Mbus after waking up with the data saved before going to sleep mode, which is an example of use-case of the proposed system (measurement)

Technology	55nm DDC process
Die Size	2600µm x 1080µm
CPU	ARM Cortex M0
On-chip Memory	16KB SRAM
SRAM Bitcell Leakage Power	**0.89fW @ 25˚C** **1.4pW @ 125˚C**
Supply Voltage	Nominal: From PMU layer: 1.2V, 0.6V Sleep Mode: From Battery: 2.2V~3.3V (SRAM power is internally generated)
Frequency	Processor: 200kHz DC-DC and CP: 1kHz ~ 100kHz
Sleep Power	**0.54µW @ 125˚C**

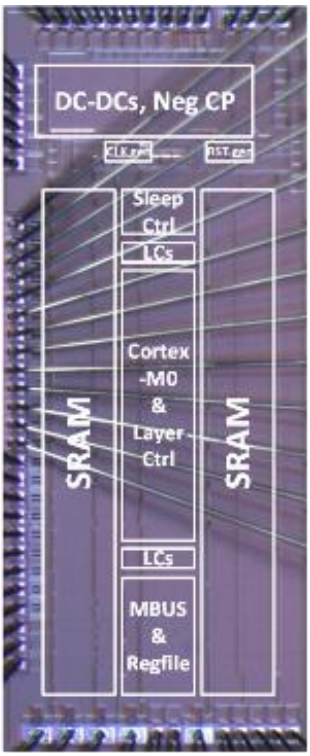


Figure 3.12 Die photo and chip summary

3.4 Conclusion

Sleep power is critical for the lifetime of sensors with power gates and sleep modes, particularly for high temperature applications where leakage currents dominate. This chapter presented a µprocessor system that features ultra-low power sleep mode at high temperature. The proposed system incorporates a 16-kB custom SRAM, an internal DC-DC converter and charge-pumps that allow the complete sensing platform to retain full memory contents with 0.54µW during sleep mode at 125˚C, which is 26× lower than without the proposed techniques.

Chapter 4 **A Wide-Range Leakage-Biased Synchronous Level Converter for ULP SoCs**

4.1 Introduction

Modern ultra-low power (ULP) SoCs often employ sub-threshold or near-threshold design techniques but also require higher voltage domains for RF, I/O, and other circuits. As a result, wide-range level conversion is needed to interface between the blocks in a ULP SoC. However, the design of a robust level converter (LC) that can operate at sub-threshold or near-threshold voltage is challenging. Conventional DCVS-type designs suffer from severe contention between strong pull-up devices and weak pull-down devices, leading to high PVT sensitivity of delay and power and poor robustness.

Consequently, several new approaches have been proposed to achieve a robust wide-range LC. One design effectively reduces contention between pull-up and pull-down devices [28]; however, it employs dynamic operation and requires a keeper bias voltage, increasing design complexity and rendering the conversion range inflexible post-design, thereby limiting dynamic voltage and frequency scaling (DVFS). Several other approaches employ a current-driven amplifier structure [29, 30, 31, 32], which provides relatively robust operation but increases power consumption, particularly static and instantaneous short-circuit power, especially at fast corner and high temperature. Although some works [31, 32, 33, 34] show good energy and delay performances, they do not support high I/O voltages (>1.8 V), which makes robust LC design more challenging and requires thick gate-oxide transistors. At the same time, most level conversions occur at a timing boundary, i.e., after a sequential element such as a flip-flop or latch, due to large delay spread among devices operating at different voltage domains. The aforementioned

approaches are all asynchronous LCs and hence require an additional sequential element, forgoing possible efficiency improvement by integrating level conversion within a sequential element itself [35]. To address these limitations and achieve a low-power and robust wide-range synchronous LC, this work proposes a new leakage-biased LC (LBLC) integrated with a latch [36].

4.2 Leakage-Biased Level Converter

4.2.1 Motivation

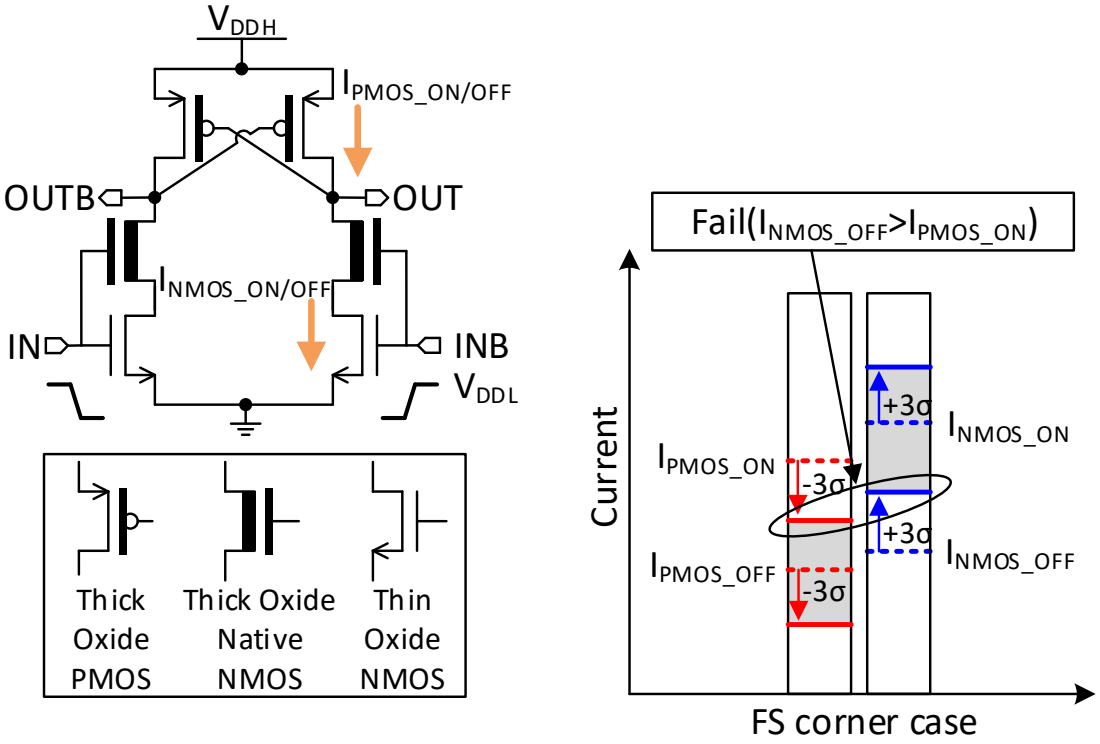


Figure 4.1 DCVS-type LC and its current margin plots at FS corner

To guarantee the functionality of a conventional DCVS-type LC (Figure 4.1) in sub-threshold or near-threshold operation, the low-voltage domain NMOS transistors should be large enough to overcome the strength of the high-voltage domain PMOS pull-up transistors [28]. However, in the fast-slow (FS) corner, or at high temperatures, the off-state current of such large NMOS transistors may become larger than the PMOS on-current, causing functional failure. This

two-sided constraint is the main challenge in designing a robust wide-range LC. Therefore, a good design should guarantee that the transistor on-current is always much larger than the off-current of complementary transistors. These requirements provide the motivation for the proposed LBLC.

4.2.2 LBLC Core Block

Figure 4.2(a) shows the core block of the LBLC. The design removes contention between PMOS and NMOS using tail (M2) and pre-charge (M11 and M14) transistors that are controlled with a low-voltage domain clock signal. In an analog sense, LCs can be viewed as a specific type of comparator with input that swings between V_{DDL} and ground, and hence we can draw parallels to clocked comparators [37] (i.e., dynamic comparators) that are widely used in many applications. However, clocked comparators rely on pre-charge PMOS devices with sources tied to V_{DDH}, meaning that the clock must itself toggle at the higher supply voltage. This incurs a large power penalty due to high clock switching activity, which is incompatible with the sub-threshold and near-threshold applications where wide-range LCs are necessary. Again taking a more analog perspective, one option would be to dc-bias the clock signal at V_{DDH} and initiate a V_{DDL} magnitude downward swing to turn on the pre-charge devices. However, given the high voltage tolerance requirements for the wide-range LCs, thick gate-oxide transistors are used as pre-charge devices, with threshold voltage that exceeds V_{DDL} (i.e., $|V_{THP}| > V_{DDL}$). To solve this problem, the proposed LBLC generates the bias voltage for the pre-charge PMOS transistors (M11 and M14) using a current mirror, which consists of M1, M5, and M8. Since M1's leakage current is the reference (noting that M5 is a native device with $V_{TH} \sim 0$), V_{BIAS} is set to the value at which M8 conducts the same current as M1 leakage, and varies its value according to PVT variations to ensure the robustness of the proposed LC. Figure 4.2(b) shows the V_{CTRL} signal, which is dc-biased by V_{BIAS} and exhibits a V_{DDL} magnitude voltage down-swing by exploiting cross-coupled M9 and M10 with

ac-coupling capacitors. V_{CTRL} turns pre-charge devices M11 and M14 on and off. Since M11 and M14 gate voltages are set to V_{BIAS} during the off state, i.e., tracking thin gate-oxide transistor leakage I_{NMOS_OFF}, they can be turned on with a small V_{DDL} voltage swing despite their large threshold voltage. Also, using this structure, I_{PMOS_OFF} and I_{NMOS_OFF} remain equal across PVT, which guarantees that the NMOS and PMOS on-currents are always larger than the PMOS and NMOS off-currents, respectively, as described in Figure 4.2(c). In other words, owing to the proposed leakage biasing approach, the LBLC meets the requirements for robust LC design explained in the chapter 4.2.1 Motivation.

To ensure the junction leakages of M9 and M10 do not alter the dc-bias level of V_{CTRL}, the bodies of M9 and M10 are connected to V_{BIAS} while the bodies of all other NMOS and PMOS transistors are connected to ground and V_{DDH}, respectively. The basic operation of the proposed LBLC is as follows: Initially, CLK is low, and two complementary outputs, OUT and OUTB, are both pre-charged to V_{DDH}. CLK then goes high. If IN=V_{DDL}, then M3 discharges OUTB, turning on M13; otherwise M4 discharges OUT, turning on M12 (INB is a complementary signal of IN). Note that thick native NMOS devices prevent breakdown in the higher transconductance thin gate-oxide NMOS transistors.

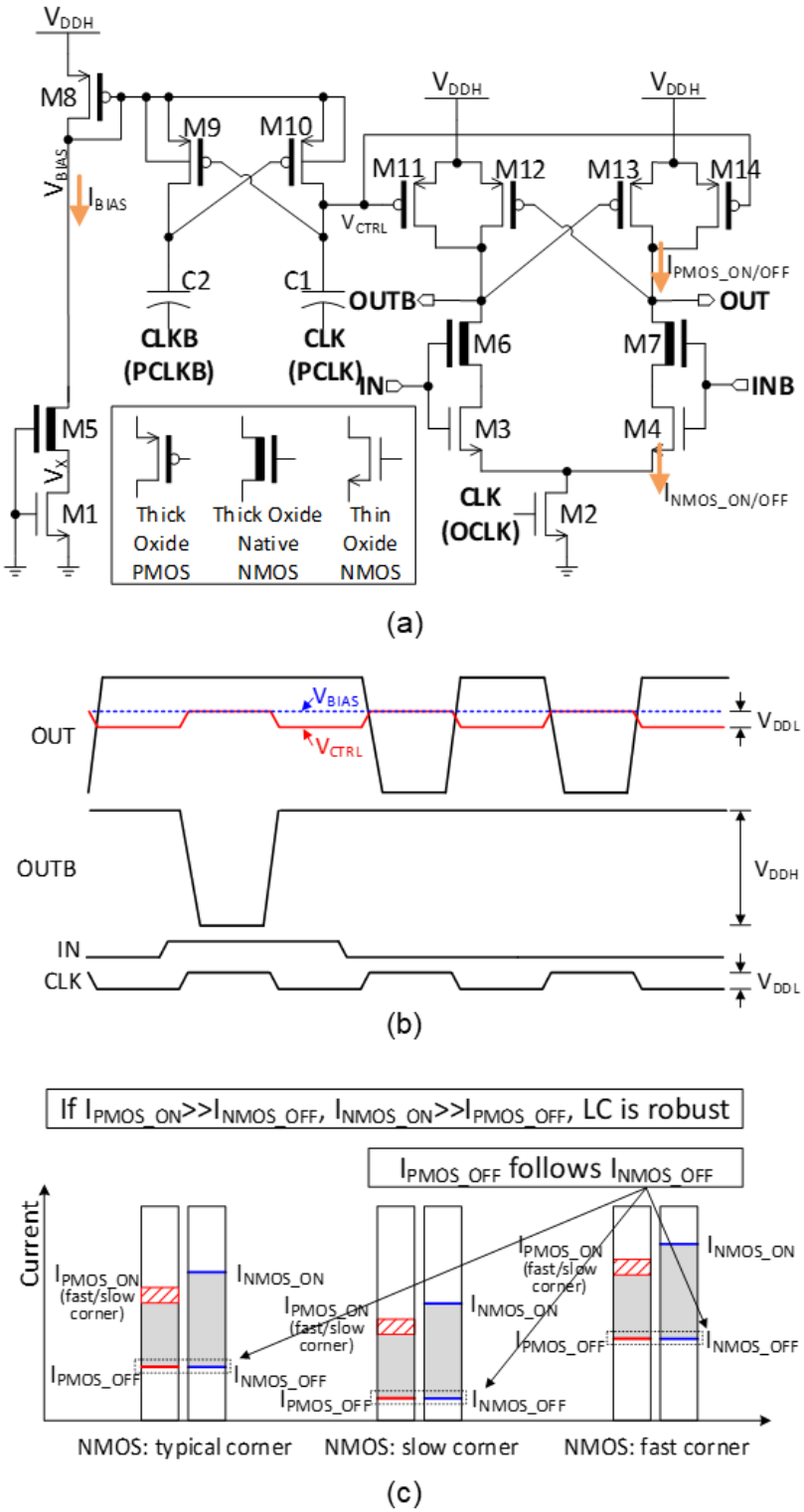


Figure 4.2 (a) LBLC core block. (b) Waveform of the LBLC's signals. (c) LBLC's current margin plots indicate that I_{PMOS_ON}>>I_{NMOS_OFF} and I_{NMOS_ON}>>I_{PMOS_OFF} for any case. The red shaded region represents the variation in PMOS on-current caused by the difference in on/off current ratio of each process corner.

4.2.3 LBLC with a SR latch and COD block

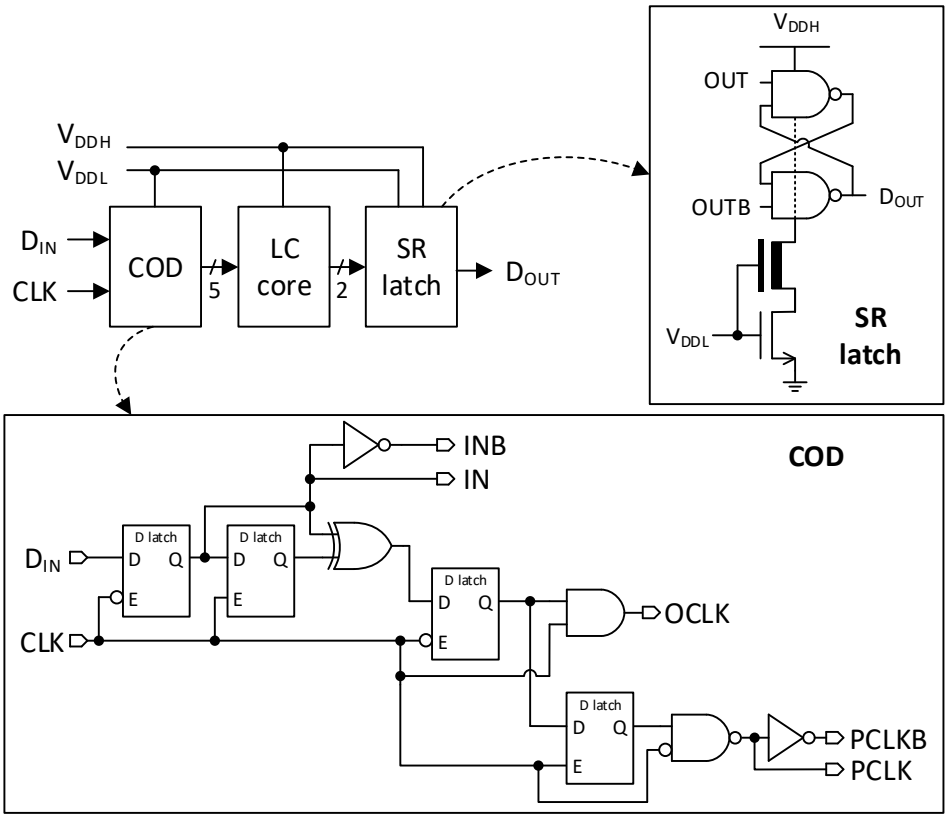


Figure 4.3 Overall block diagram of LBLC, consisting of a clock-on-demand (COD), LC core, and SR latch.

Since two complementary outputs, OUT and OUTB, are both high during pre-charge, i.e., when CLK is low, an SR latch follows the LC core block to hold the output during this pre-charge period as shown in Figure 4.3. To prevent the SR latch, i.e., static logic gates, from wasting power during the input transition, an NMOS transistor biased by V_{DDL} is inserted so that the SR latch output slew rate matches that of the LC core block.

For the proposed LC core block to function as a level-converting flip-flop, a single negative D latch must precede it. However, due to the pre-charge, the LC core block consumes switching power every clock cycle even if the input does not change. This degrades the energy efficiency in low data activity scenarios. To address this, a clock-on-demand (COD) block is incorporated, as

depicted in Figure 4.3, and pre-charge is avoided in cases where the input data does not toggle. The COD generates an OCLK pulse only if the input data changes; a downward PCLK pulse then follows it in the next half clock cycle for the pre-charge, as shown in Figure 4.4. Note that PCLK remains high during the idle state to prevent V_{CTRL} from leaking up to the value of V_{BIAS} with low PCLK and disrupting the next few pre-charges in cases of long idle times. In addition, since both the tail and pre-charge transistors are turned off during the idle state, i.e., OCLK is low and PCLK is high as shown in Figure 4.4, M8 should have a longer length and/or smaller width than M11 and M14 to guarantee that the leakages of the pre-charge transistors are larger than that of the tail transistor, thereby preventing OUT or OUTB from leaking down during the idle state.

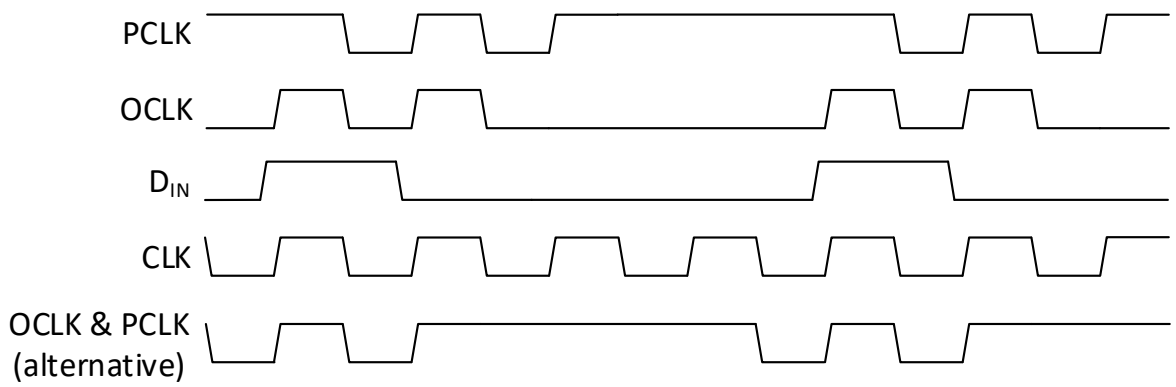


Figure 4.4 Waveforms of the OCLK and PCLK signals generated from the COD block. The alternative OCLK and PCLK signals are also depicted.

An alternative way to avoid tristate on OUT and OUTB is by activating a pre-charge half clock cycle before the input data change and making clock pulses only if the input data changes as described on the bottom waveform in Figure 4.4. In this case, however, an additional sequential element preceding the LC core might be required to predict the following input data. Logic gates used for COD operate in the low-voltage domain, and therefore their power consumption is negligible compared to the high-voltage domain component of LC power. More specifically, in the worst case (activity factor α=0.5), the overhead of the COD block is 6%, 10%, and 20% of the

total LC power for 3.3V, 2.5V, and 1.8V V_{DDH}, respectively. The savings are more significant. If α=0.25, COD saves 45%, 42%, and 34% of the total LC power for 3.3V, 2.5V, and 1.8V V_{DDH}, respectively. If α=0.1, the savings rise to 76%, 74%, and 68%. The COD-related area is 21% of the total LC area.

4.3 Simulation and Measurement Results

The current margin plot of the LBLC from the simulation is shown in Figure 4.5. I_{PMOS_OFF}, i.e., the off-current of the pre-charge transistors, follows I_{NMOS_OFF} as expected because it is biased by the NMOS leakage current. Consequently, the proposed LBLC is able to guarantee its robustness across PVT variations.

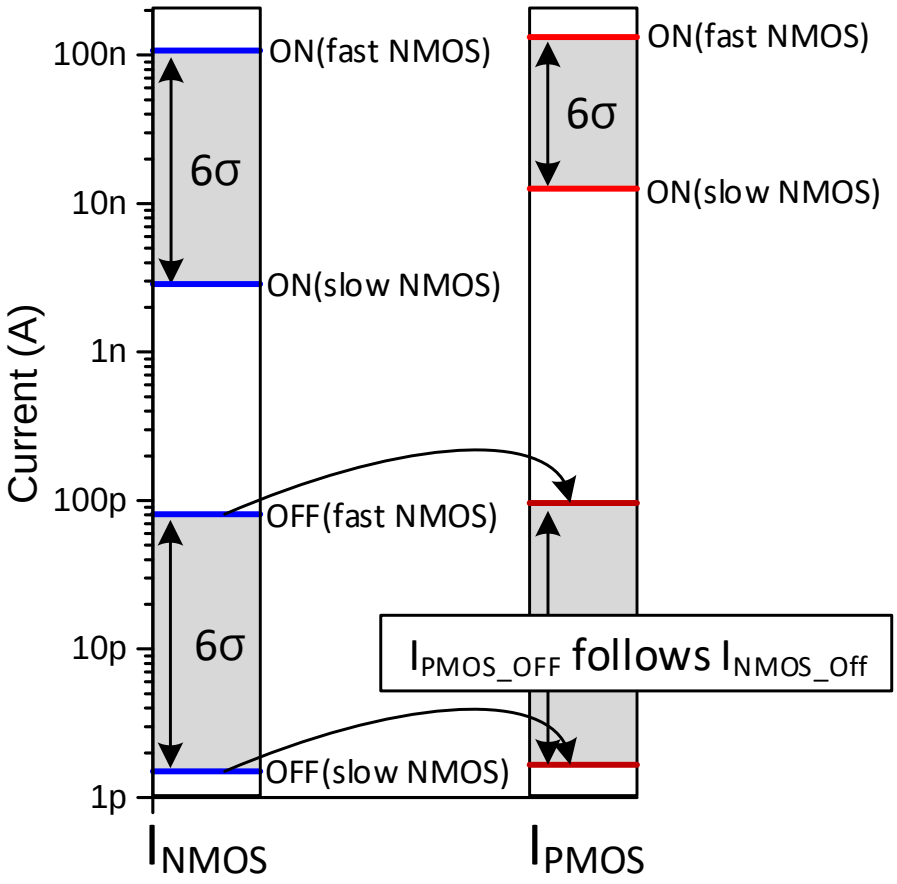


Figure 4.5 Current margin plot (simulation results, temp=25°C)

The proposed LBLC is fabricated in a 55-nm CMOS process, and its performance is verified through measurements of 31 dies (15 TT, 4 FF, 4 FS, 4 SS, 4 SF corner chips). For a fair comparison, the previously proposed LC^2 [28] (with a preceding DFF) was fabricated in the same process, which operates using 2.5 V as V_{DDH}. Figure 4.6 shows the measured delay and power. The LBLC consumes 2.6× lower power than [28] on average with comparable speed and flexible V_{DDH}. The delay was measured by the stochastic time-to-digital converter (TDC) integrated with the LBLC as shown in Figure 4.7(a). The nominal voltage of the low-threshold voltage (LVT) digital standard cells used in the test structure is 0.9 V. The maximum tolerance voltage of those standard cells is 1.8 V; hence, the output of the LBLC is followed by an inverter made of thick gate-oxide devices to prevent the breakdown of thin gate-oxide devices. The test structure generates a periodic pulse signal, i.e., PULSE in Figure 4.7(b), the width of which indicates the C-to-Q delay of the LC. The following TDC produces a histogram of the PULSE signal by sampling and accumulating the signal at the edge of the asynchronous internal oscillator clock and then calculates the C-to-Q delay: C-to-Q delay = 2 × (period of CLK) × (frequency of PULSE HIGH) / (total sample size). Note that since the delays of the logic gates in the test structure are much faster than that of LC, they are negligible in measuring the LC delay. Specifically, even the delay of *inv_clock* under V_{DDL} is less than 1% of the LC delay in the simulation. Figure 4.8 shows the power and delay across temperature, with the LBLC showing similar speed as [28]. At high temperature, the LBLC's power increases rapidly due to the increasing leakage of the thin gate-oxide transistors. However, its total power is still smaller than [28] even at 80°C with a frequency of 100 kHz. Table 4-1 compares the results obtained for the LBLC with other works, and Figure 4.9 shows a test chip die photo. Note that V_{DDH} in [32] is 1.1 V, which is lower than 1.8–3.3 V, the target V_{DDH} of the others.

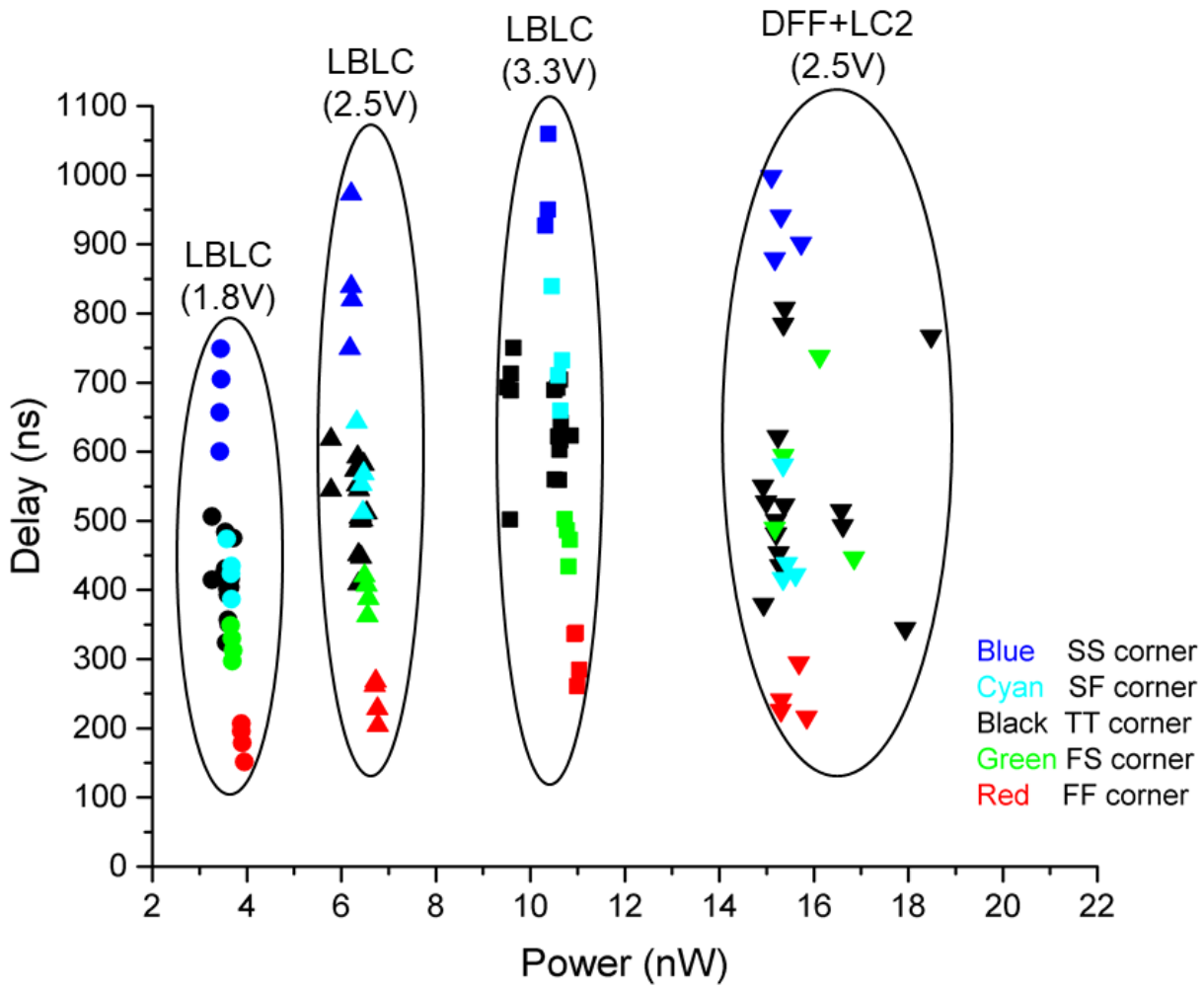


Figure 4.6 Test chip delay and power distribution (freq=100 kHz, temp=25°C, α=1)

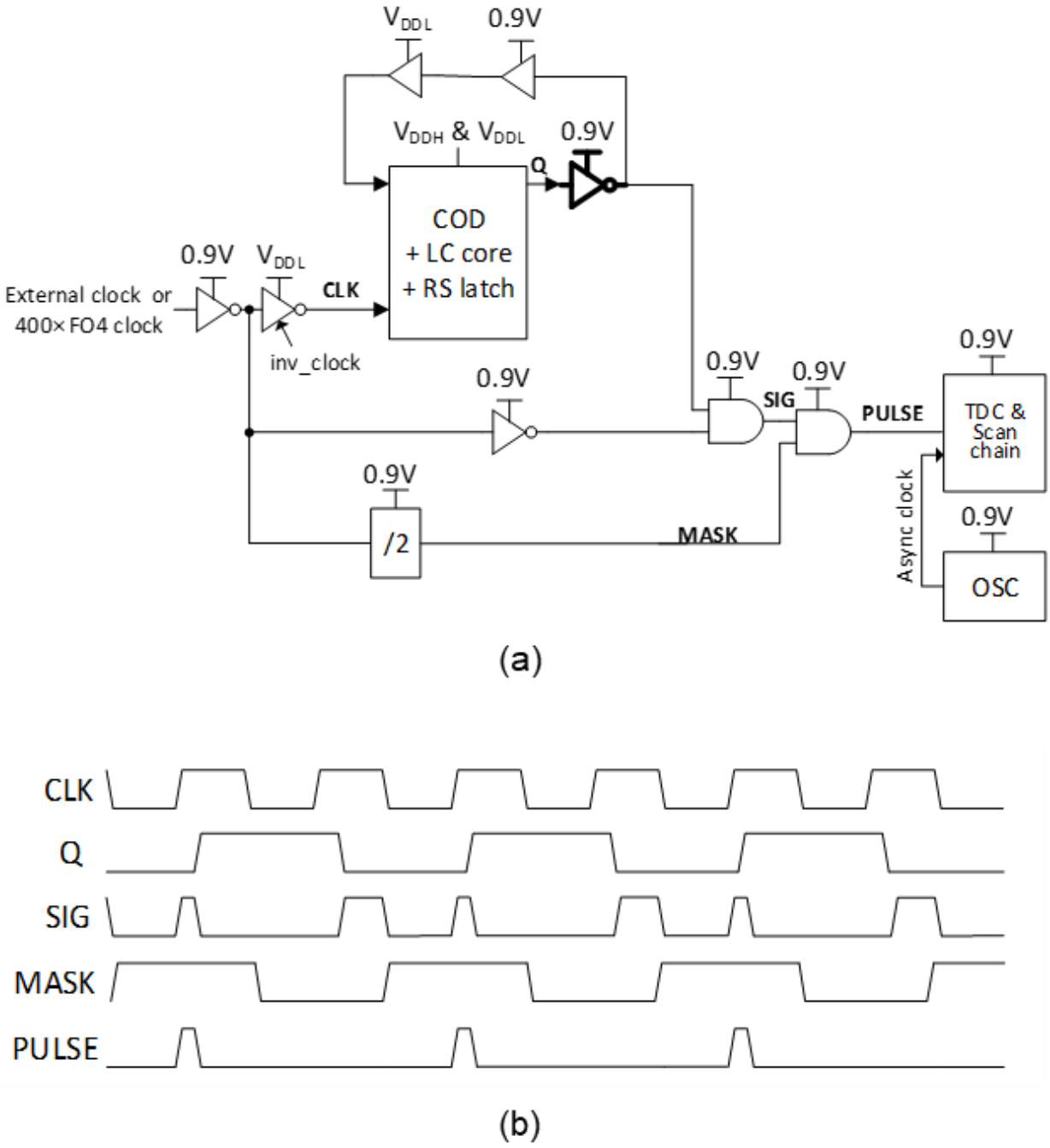
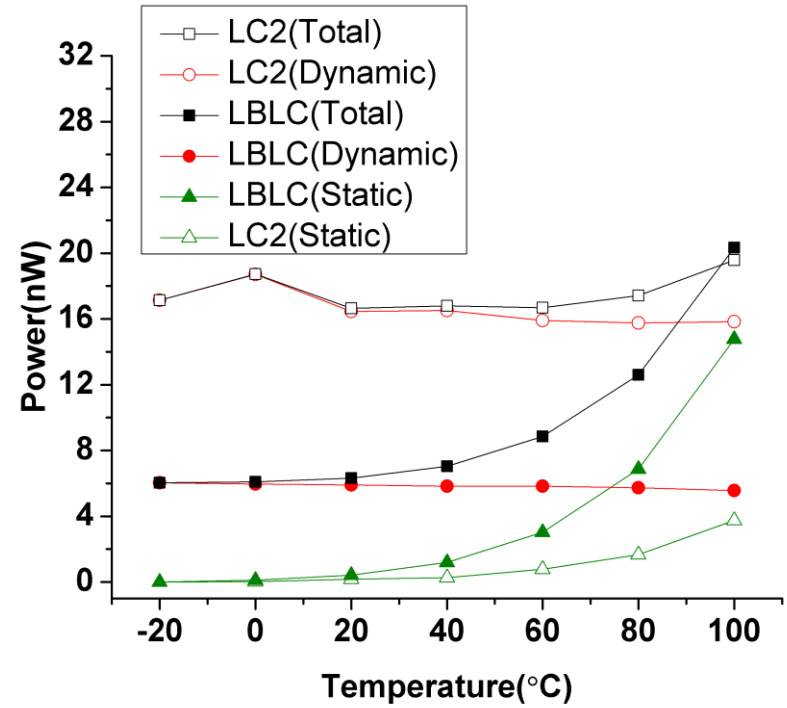
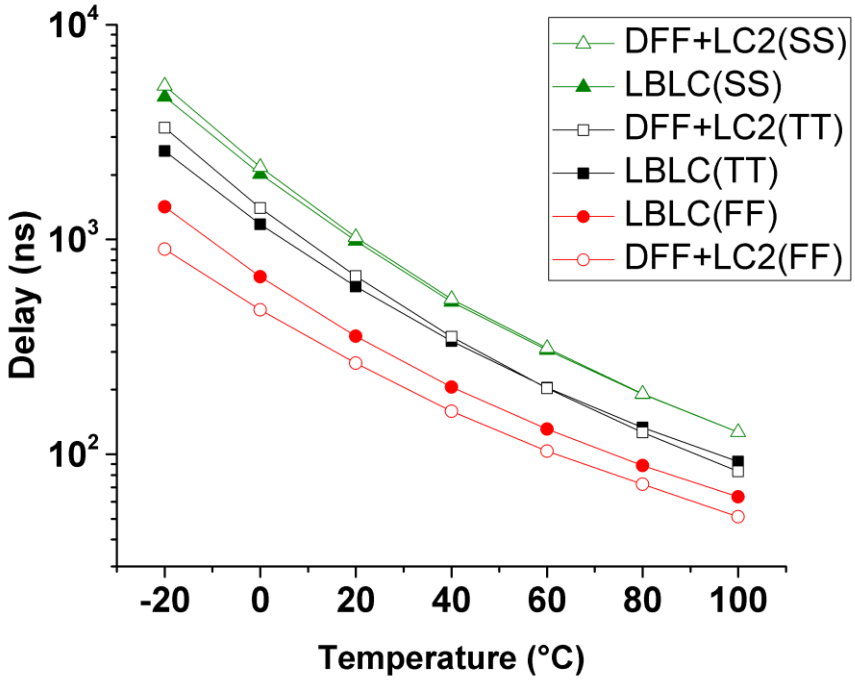


Figure 4.7 (a) Test structure for the delay of LBLC. (b) Waveform of the signals generated from the test structure.



(a)



(b)

Figure 4.8 Temperature sweep for (a) power (TT corner, freq=100 kHz, α=1) (b) delay (TT, SS, FF corner).

Table 4-1 Comparison Table of Level Converters (Average of TT Corner Chips)

	Proposed LBLC	DFF + Kim [25]	Kim [25]	Osaki [26]	Zhou [27]	Lotfi [29]
Technology	55nm	55nm	130nm	0.35µm	0.18µm	40nm
Conversion	0.3V to 1.8-3.3V	0.3V to 2.5V	0.3V to 2.5V	0.4V to 3V	0.3V to 1.8-3.3V	0.35V to 1.1V [a]
Type	LCFF	LCFF	Static	Static	Static	Static
Clk to Q delay (0.3V to 2.5V)	523ns (17.4FO4)	546ns (18.2FO4)	Delay: 41.51ns (2.38FO4)	-	Delay: 168ns (1.04FO4)	Delay: 15.5ns (>1.17FO4)
Static Power	234pW (1.8V) 256pW (2.5V) 282pW (3.3V)	159pW	475pW	230pW	160pW (1.8V) 340pW (2.5V) 970pW (3.3V)	550pW (1.1V)
Energy/ Transition	33.1fJ (1.8V) 60.5fJ (2.5V) 99.5fJ (3.3V)	158fJ	229fJ	5.8pJ	39fJ (1.8V) 188fJ (2.5V) 954fJ (3.3V)	4.2fJ
Area	154µm^2	152µm2 (/w diodes)	102µm^2	1880µm^2	153µm^2	8µm^2

[a] 1.1V is not a high I/O voltage for which thick gate-oxide transistors are necessary. Accordingly, [4] was designed with thin gate-oxide transistors only, unlike the others.

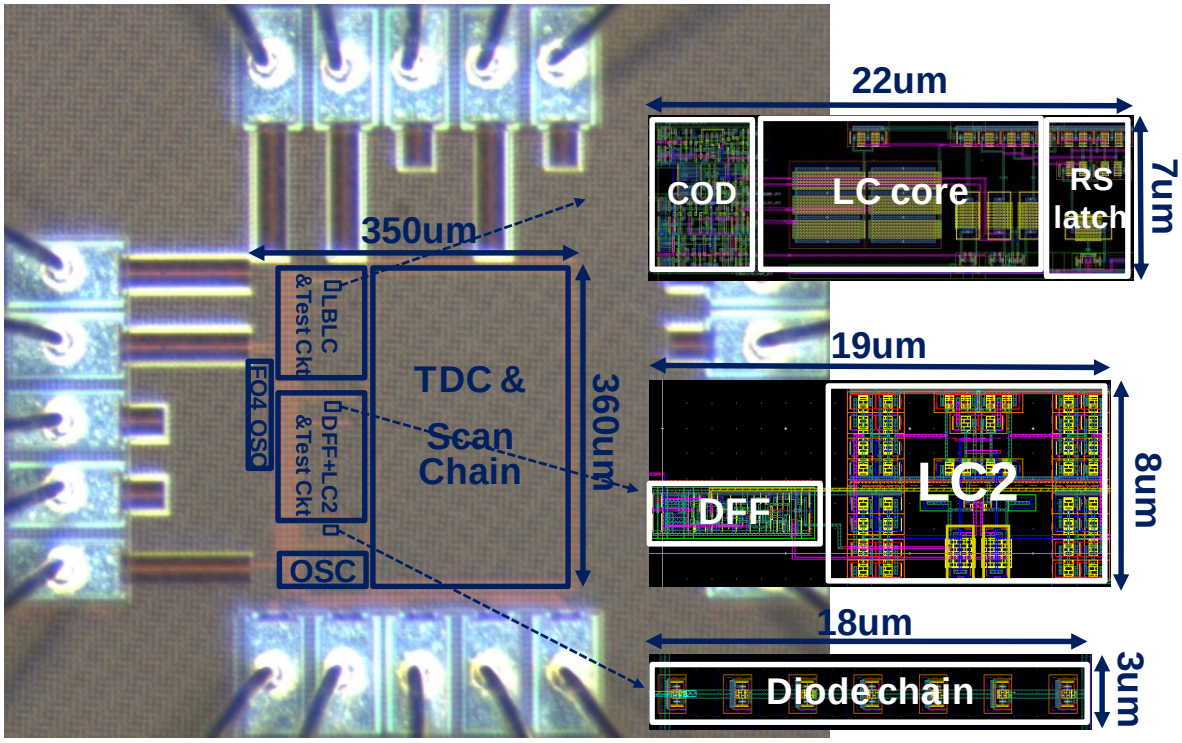


Figure 4.9 Die photo and layout of LBLC, LC^2 and its diode-chain

4.4 Conclusion

In this chapter, a new leakage-biased level converter, i.e., LBLC, is presented. The proposed LBLC has the lowest energy/transition compared with previously proposed LCs that support high I/O voltages (>1.8 V) while also inherently supporting flexible voltage levels. Given a typical ULP 32b MCU energy/cycle of 6.4 pJ [26], the LBLC allows for 32b up-conversion to I/O voltages within 5% of this total energy budget.

Chapter 5 **A Switched-Capacitor DC-DC Converter Generator Design**

5.1 Introduction

The continuing scaling in CMOS technology is mainly driven by the persistent demand for both performance and energy efficiency in electronic devices. For the same reason, the *system-on-a-chip*s (SoCs) in those devices have become more complex and requires more functional blocks including analog components that have labor-intensive design processes in particular with cutting edge FinFET technologies. While digital design flows have been automated, analog design flows are still mostly relied on manual design. As technology advances, design rules are getting more complicated due to the dependencies across the layers, and consequently custom layout has become more expensive and time-consuming. Therefore, there is a growing need for automation in analog circuit design to lower the design costs and satisfy the tight time-to-market constraints that are required in modern SoC design [38], [39], [40].

Today's SoCs have a lot of different voltage domains along with the various functional blocks. As a result, an integrated DC-DC converter has become a fundamental block for the modern SoCs. Hence, as an attempt to achieve fully automated analog design, we propose a design methodology for the automated generation of switched-capacitor DC-DC converters in this paper. The proposed DC-DC generator generates a netlist based on the user input specifications. Then it also automatically generates a layout using commercial synthesis and place and route tools in accordance with the netlist. This chapter is organized as follows. Chapter 5.2 introduces the switched-capacitor DC-DC architecture adopted by the proposed DC-DC generator. Chapter 5.3

presents how the generator finds the optimal design parameters. Chapter 5.4 describes how the generator works. Chapter 5.5 presents the simulation results and chapter 5.6 concludes the work.

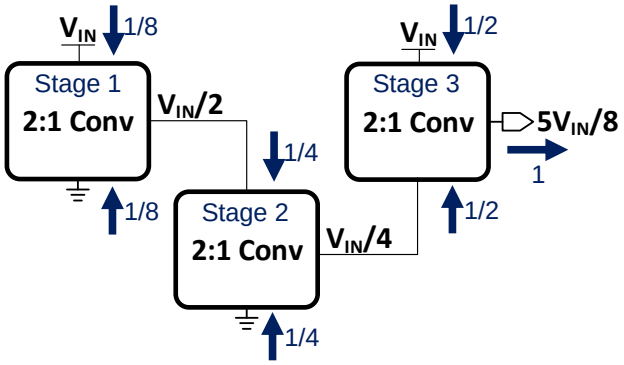
5.2 DC-DC Converter Architecture

Switched-capacitor DC-DC converters have recently become strong candidates for on-chip power converters, due to its CMOS process compatibility, good efficiency, and scalability of load power and frequency [19]. However, they are only capable of a finite number of conversion ratios, and increasing the number of ratios using standard topologies such as the ladder topology requires a significant increase in its complexity. To address this issue, a successive-approximation (SAR) switched-capacitor DC-DC converter was proposed in [19], which cascades multiple stages of 2:1 converters and provides a large number of conversion ratios without notable hardware overhead. A recursive switched-capacitor (RSC) DC-DC converter that alleviates cascading losses in the SAR switched-capacitor DC-DC converters was also proposed in [20]. In this work, we utilize the RSC DC-DC converter as a basic architecture of the auto-generated DC-DC converter.

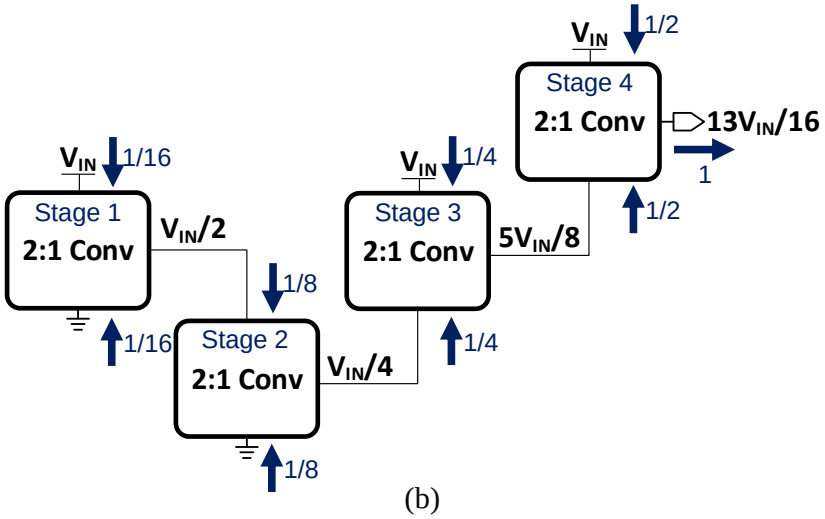
The RSC DC-DC converters have 2:1 converters for their building blocks as shown in Figure 5.1. The conversion ratios of those converters are determined by the configuration of the cascading 2:1 converters. As shown in Figure 5.1, a N-stages converter can have a conversion ratio of $m/2^N$, where $m < 2^N$. Also, note that the current flow through N^{th}-stage is twice that through $(N-1)^{th}$-stage, which leads to the binary-weighted 2:1 converters sizing. The 2:1 converter consists of *flying cap*s, *PMOS switch*es, and *NMOS switch*es as depicted in Figure 5.2(a). The four clock signals come from the non-overlapping clock generator designed using standard logic gates as described in Figure 5.3(a). It generates two non-overlapping clock signals, i.e. clk0 and clk1, and their inverted signals, i.e. clk0b and clk1b. It is powered by V_{IN}, and hence the clock signals are in V_{IN} voltage domain. Hence, the gate control signals for the *PMOS/NMOS switch*es have V_{IN}

magnitude voltage swing exploiting cross-coupled transistors and ac-coupling capacitors as shown in Figure 5.2(b), (c).

In sum, there are four unit building blocks in the DC-DC converter, which are *flying cap*, *PMOS switch*, *NMOS switch*, and non-overlapping clock generator. We define these blocks as auxiliary cells [40]. Similar to standard digital cells, auxiliary cells are basic functional blocks and created once for each technology and reused. Ultimately, the proposed generator determines the configuration of the 2:1 converters in the DC-DC converter along with the number of stages, and finds the optimal sizes of *flying cap*s, *PMOS switch*es and *NMOS switch*es for the 2:1 converters.



(a)



(b)

Figure 5.1 RSC DC-DC converters and their charge flow (a) The configuration of 3-stages for 5/8 conversion ratio (b) The configuration of 4-stages for 13/16 conversion ratio

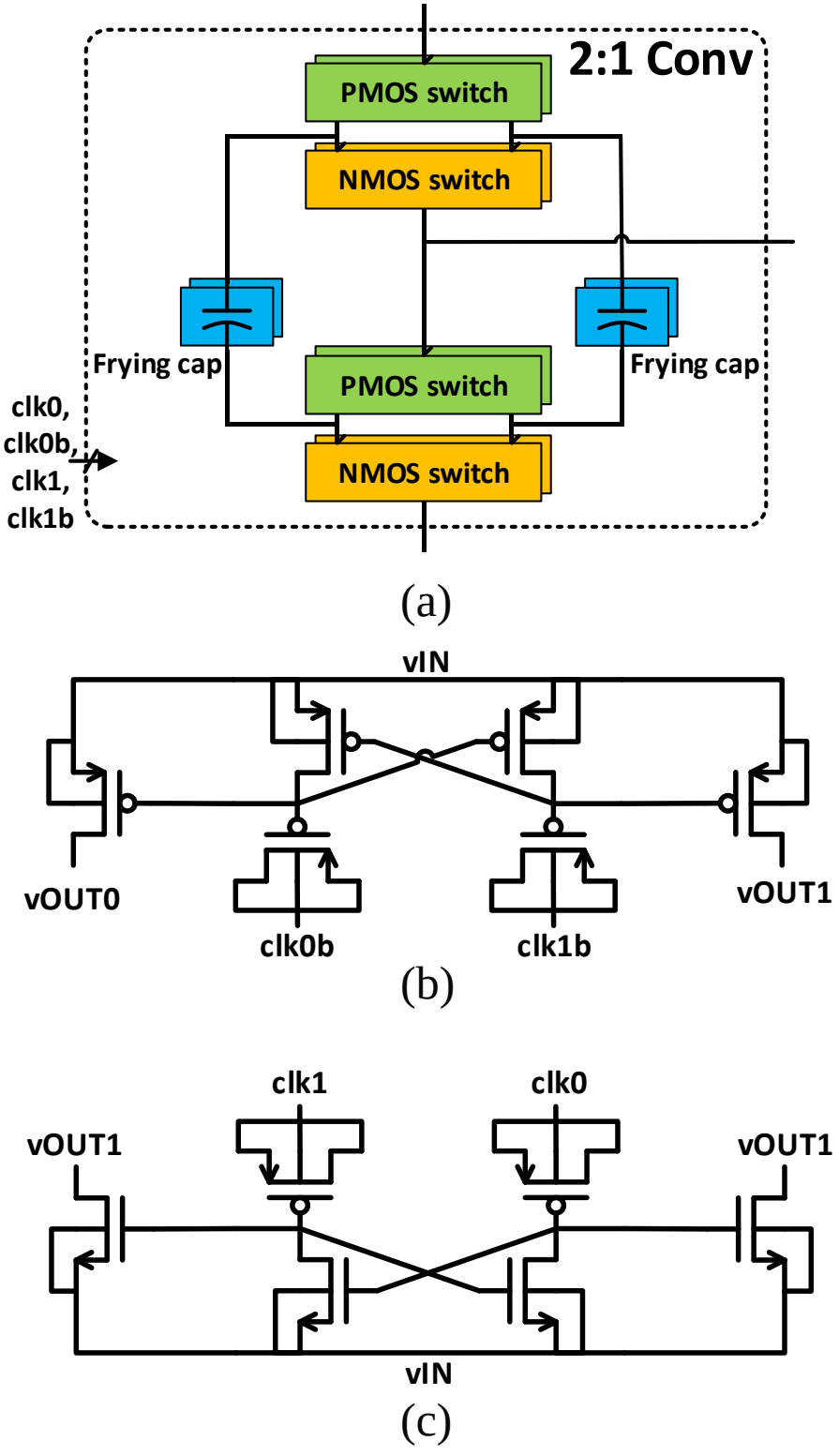


Figure 5.2 (a) The structure of 2:1 converter (b) Schematic of PMOS switch (c) Schematic of NMOS switch

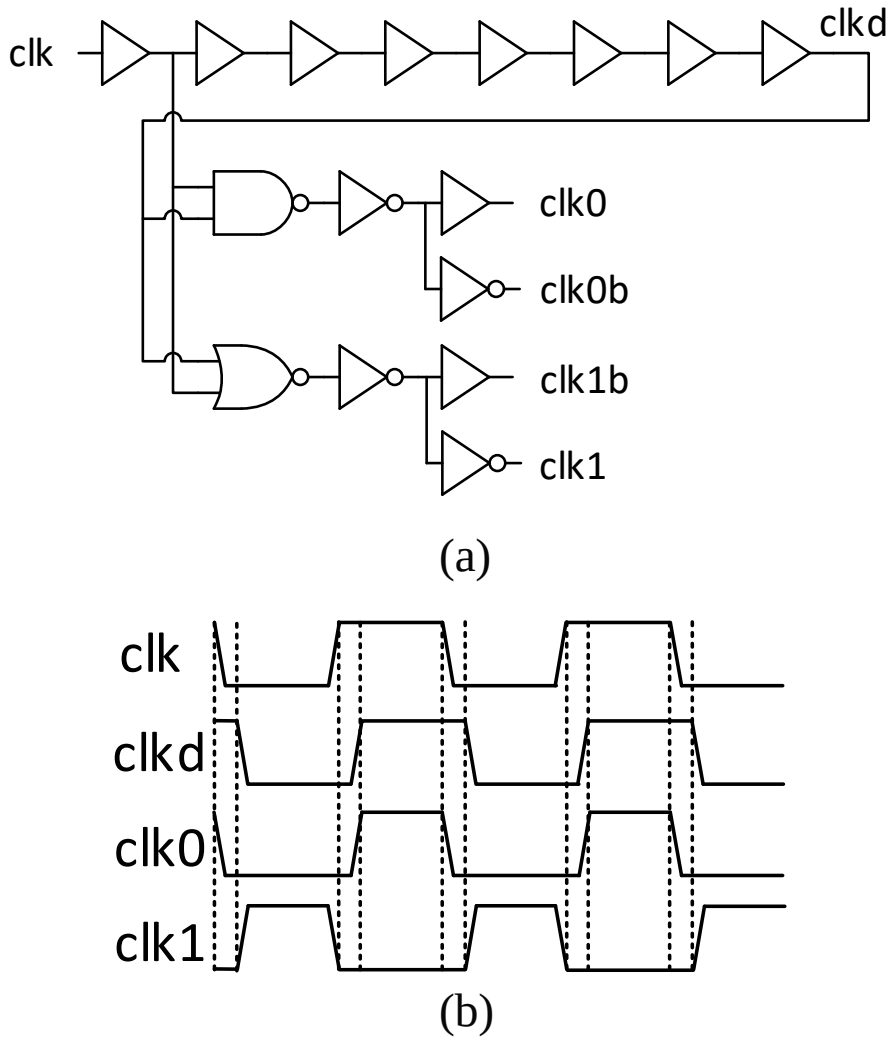


Figure 5.3 (a) The schematic of a non-overlapping clock generator (b) The output waveform of the non-overlapping clock generator

5.3 Optimal Design Parameters for DC-DC Converter

In this section, we show that there exists an optimal conversion ratio which gives maximum conversion efficiency, and also introduce how we find the optimal sizes of the switches in the 2:1 converters. Based on these analyses, technology parameters, and the user inputs such as the desired output voltage, load current and clock frequency, the proposed generator decides configuration

and the sizes of the *flying cap*s, *PMOS switch*es and *NMOS switch*es in the DC-DC converter so as to maximize the energy efficiency.

5.3.1 Optimal Conversion Ratio

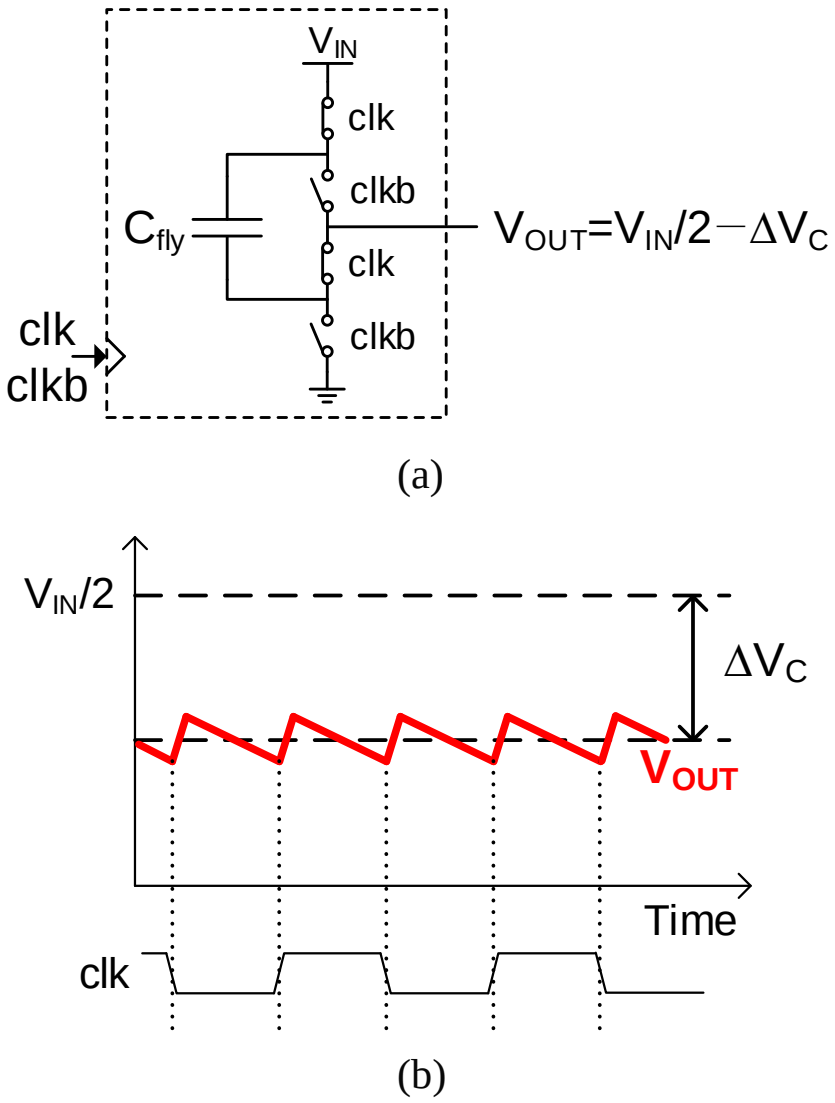


Figure 5.4 (a) Simplified schematic of the 2:1 converter (b) The output waveform of the 2:1 converter

In [18], the optimal conversion ratio was derived for the self-oscillating voltage doubler. A similar analysis can be applied to derive the optimal conversion ratio for the single 2:1 converter. The output voltage, i.e. V_{OUT} in Figure 5.4, must be an exact half V_{IN} if the load current is zero.

On the other hand, if load current is not zero, there must be a voltage drop, i.e. ΔV_C in Fig. 4, at the output node. The charge drawn from V_{IN} is proportional to ΔV_C, and the input power P_{IN} can be written as follows.

$$P_{IN} = (2C_{FLY}\Delta V_C f_{CLK})V_{IN} \tag{5.1}$$

A large ΔV_C indicates that conduction loss is dominant in total loss. Conversely, a small ΔV_C indicates that switching loss is dominant requiring higher clock frequency to supply the load current with given flying capacitors. To maximize the conversion efficiency, conduction loss and switching loss should be balanced. Assuming the output voltage is stable and the switches are ideal, conduction loss L_C is the same as the charge sharing loss. When two charged capacitors C_1 and C_2 having potentials V_1 and V_2 respectively are connected to each other, the charge sharing loss is described as the equation below.

$$Loss\ of\ sharing = \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}(V_1 - V_2)^2 \tag{5.2}$$

In the 2:1 converter shown in Fig. 4, charges are transferred twice every clock cycle. Therefore, from (5.2), conduction loss L_C can be written as below, assuming $C_1 = C_{FLY}, C_1 \ll C_2$, and $\Delta V_C = V_1 - V_2$.

$$L_C \approx C_{FLY}{\Delta V_C}^2 f_{CLK} \tag{5.3}$$

Switching loss L_S is the dynamic power consumed in the parasitic capacitors in the converter, and hence can be written as below.

$$L_S \approx \left(\sum_{para\ caps} C_j V_{SWING_j}^2\right) f_{CLK} = C_{EFF} V_{IN}^2 f_{CLK} \tag{5.4}$$

where C_j is every parasitic capacitor, and V_{SWING_j} is the voltage swing of each parasitic capacitor. C_{EFF} is defined as below.

$$C_{EFF} = \left(\sum_{para\ caps} C_j \frac{V_{SWING_j}^2}{V_{IN}^2} \right) \tag{5.5}$$

Assuming $\Delta V_C \ll V_{IN}$, $C_{EFF} = C_{PAR}/4$ for the 2:1 converter, where C_{PAR} is the sum of all parasitic capacitors. The ratio of these losses to input power can be written as below.

$$\frac{L_{TOTAL}}{P_{IN}} = \frac{L_C + L_S}{P_{IN}} = \frac{\Delta V_C}{2V_{IN}} + \frac{C_{EFF} V_{IN}}{2C_{FLY}\Delta V_C} \tag{5.6}$$

From (5.6) and the inequality of arithmetic and geometric means, the lower bound of L_{TOTAL}/L_{IN} can be calculated as below.

$$\frac{\Delta V_C}{2V_{IN}} + \frac{C_{EFF} V_{IN}}{2C_{FLY}\Delta V_C} \geq 2\sqrt{\frac{\Delta V_C}{2V_{IN}} \frac{C_{EFF} V_{IN}}{2C_{FLY}\Delta V_C}} = \sqrt{\frac{C_{EFF}}{C_{FLY}}} \tag{5.7}$$

Since the equality holds if and only if the two left terms are equal to each other, total loss is at minimum when

$$\frac{\Delta V_C}{2V_{IN}} = \frac{C_{EFF} V_{IN}}{2C_{FLY}\Delta V_C} \Rightarrow \Delta V_C = V_{IN}\sqrt{\frac{C_{EFF}}{C_{FLY}}} \tag{5.8}$$

Therefore, there is a constant optimal ΔV_C for the maximum conversion efficiency, which is determined by the ratio between C_{EFF} and C_{FLY}. For a general N-stages DC-DC converter, the input power $P_{IN(N)}$ can be written as follows.

$$P_{IN(N)} = \left(\sum_{i=1}^{N} 2\alpha_i C_i \frac{\Delta V_C}{N} f_{CLK} \right) V_{IN} \tag{5.9}$$

α_i is 1 if stage i has V_{IN} as its input, or 0. For example, $\{\alpha_1, \alpha_2, \alpha_3, \alpha_4\} = \{1,0,1,1\}$ in Figure 5.1(b). C_i is the parasitic capacitance of the stage i. Since the size of each stage is proportional to the current flow, we assume voltage drops in the stages are equally distributed.

Hence, a voltage drop in each stage is written as $\Delta V_C/N$. Consequetnly, conduction loss for the N-stages DC-DC converter $L_{C(N)}$ can be written as below.

$$L_{C(N)} \approx \sum_{i=1}^{N} C_i \left(\frac{\Delta V_C}{N}\right)^2 f_{CLK} = C_{FLY} \left(\frac{\Delta V_C}{N}\right)^2 f_{CLK} \tag{5.10}$$

Switching loss $L_{S(N)}$ is the same as (5.4). However, since C_{EFF} is dependent on the configuration, the value of C_{EFF} for N-stages DC-DC converters will be different from $C_{PAR}/4$ for the 2:1 converter. From, (5.4), (5.9), and (5.10).

$$\frac{L_{C(N)}}{P_{IN(N)}} = \frac{C_{FLY}\frac{\Delta V_C}{N}}{2(\sum_{i=1}^{N} \alpha_i C_i) V_{IN}} \tag{5.11}$$

$$\frac{L_{S(N)}}{P_{IN(N)}} = \frac{C_{EFF} V_{IN}}{2(\sum_{i=1}^{N} \alpha_i C_i)\frac{\Delta V_C}{N}} \tag{5.12}$$

As shown in (5.8), the two above terms are equal to each other when the total loss at minimum.

$$\frac{C_{FLY}\frac{\Delta V_C}{N}}{2(\sum_{i=1}^{N} \alpha_i C_i) V_{IN}} = \frac{C_{EFF} V_{IN}}{2(\sum_{i=1}^{N} \alpha_i C_i)\frac{\Delta V_C}{N}} \Rightarrow \Delta V_C = N \cdot V_{IN} \sqrt{\frac{C_{EFF}}{C_{FLY}}} \tag{5.13}$$

Therefore, there is still a constant optimal ΔV_C for the maximum conversion efficiency even with a general N-stages DC-DC converter, which is determined by the characteristics of the flying capacitors and the configuration of the DC-DC converter.

5.3.2 Optimal Conversion Ratio

In the previous section, we assume the switches are ideal. However, the switches have finite conductance, and hence there is a voltage drop across the switches. The optimal switch size can also be achieved when conduction loss and switching loss are balanced. Let the equivalent

parasitic capacitance and resistance of the switches in the DC-DC converter be C_{SW} and R_{SW}, respectively. Then the conduction and switching loss due to the switches are as follows.

$$L_{SW\_Conduction} = I_{LOAD}\Delta V_R = I_{LOAD}^2 R_{SW} \tag{5.14}$$

$$L_{SW\_Switching} = C_{SW} V_{IN}^2 f_{CLk} \tag{5.15}$$

ΔV_R and I_{LOAD} is a voltage drop due to the switches and load current at the output, respectively. Let $k = R_{SW}C_{SW}$. Then k is a constant determined by the technology. The total loss is the sum of these two losses and can be written as below using k.

$$L_{SW} = I_{LOAD}^2 R_{SW} + \frac{k}{R_{SW}} V_{IN}^2 f_{CLk} \tag{5.16}$$

At minimum,

$$\frac{\partial L_{SW}}{\partial R_{SW}} = I_{LOAD}^2 - \frac{k V_{IN}^2 f_{CLk}}{R_{SW}^2} = 0 \Rightarrow R_{SW} = \frac{V_{IN}}{I_{LOAD}}\sqrt{k f_{CLk}} \tag{5.17}$$

The optimal R_{SW} is proportional to $\sqrt{f_{CLk}}$, which is also proven in the graph of L_{SW} in Fig. 5. Moreover, as shown in Figure 5.5, the lower F_{CLk} is the better efficiency is.

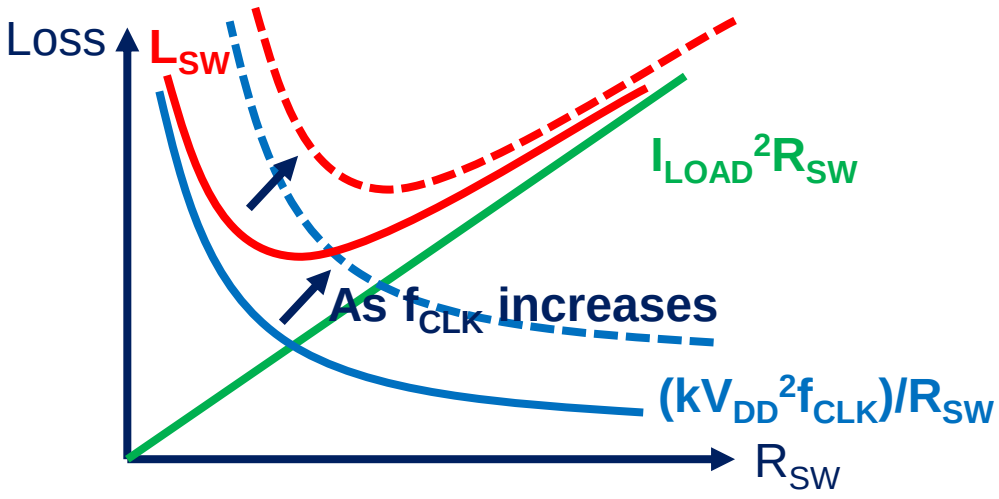


Figure 5.5 Graph of L_SW shows optimal R_SW is proportional to $\sqrt{f_{CLK}}$.

In other words, given a fixed load current, efficiency is better when using larger frying capacitors. Note that as long as $\Delta V_R \ll V_{IN}$, the loss due to the switches is independent of the loss due to the flying capacitors calculated in the previous section.

5.4 DC-DC Converter Generation

The proposed DC-DC generator requires three input parameters: the output voltage (V_{OUT}), load current (I_{LOAD}), and input clock frequency (f_{CLK}). Based on these input parameters and the analyses in the section III, the generator determines three design parameters: the configuration, the number of *flying cap*s (N_{FLY_CAP}), and the number of *PMOS/NMOS switch*es (N_{SW}). Internally, the DC-DC generator requires additional five technology parameters for the given technology: input voltage (V_{IN}), capacitance of the unit flying capacitor (C_{U_FLY}), resistance of the unit switch (R_{U_SW}), $\sqrt{R_{U\_SW}C_{U\_SW}}$ (k_{sqrt}), and ΔV_C. All these five technology parameters were obtained beforehand through the simulation with the auxiliary cells. First, the configuration is determined to have a conversion ratio of $(V_{OUT} + \Delta V_C)/V_{IN}$. Second, from (5.18), size of the flying capacitors, i.e. N_{FLY_CAP}, in the last stage is determined by the equation in (5.19) .

$$I_{LOAD} = 2C_{FLY(last\ stage)}\frac{\Delta V_C}{N}f_{CLK} \tag{5.18}$$

$$N_{FLY\_CAP(last\ stage)} = \frac{N \cdot I_{LOAD}}{2\Delta V_C f_{CLK} C_{U\_FLY}} \tag{5.19}$$

The number of *flying cap*s in the other stages are set to be binary-weighted. Lastly, the number of *PMOS/NMOS switch*es connected in parallel in the last stage is determined from (5.20) as below.

$$N_{SW(last\ stage)} = \frac{I_{LOAD} R_{U\_SW}}{k_{sqrt} V_{IN} \sqrt{f_{CLK}}} \quad (5.20)$$

Since the resistances of *PMOS switch* and *NMOS switch* are balanced to each other, the number of *NMOS/PMOS switch*es are the same. They were separated for the purpose of layout flexibility. The number of switches in the other stages are also set to be binary-weighted. From these three design parameters, i.e. N_{FLY_CAP}, N_{SW}, and the configuration, the proposed DC-DC converter generates a DC-DC netlist composed of the auxiliary cells: *flying cap, PMOS switch, NMOS switch*. In addition to that, the non-overlapping clock generator is also added to the netlist. It is made of the digital standard cells, and hence its library file is also made from the digital standard cell library. Based on this library file, a place and route tool automatically adds clock buffers properly between the output of the non-overlapping clock generator and all clock input pins of the switches during the layout generation.

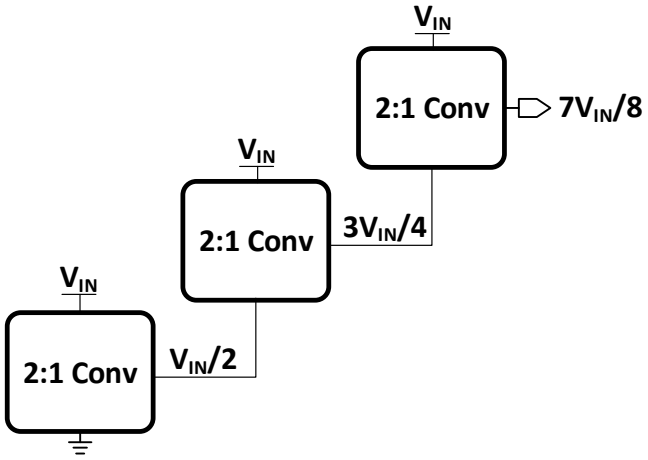
5.5 Simulation Results

The proposed DC-DC generator has been written by Python, and verified with a 14nm FinFET technology. It requires a JSON file as an input, which specifies the module name and input specifications, i.e. load current, output voltage, and clock frequency as shown in Figure 5.6 (a). The Python code generates a netlist based on the input specifications, and also generates Tcl files that include the design parameters and timing constraints. The Tcl files are transferred to the synthesis and place and route tools. With the above input parameters in Figure 5.6 (a), the design parameters made by the generator are as follows: The configuration is *'111'* which means stacking-up three 2:1 converters as shown in Figure 5.6 (b), and $N_{FLY\_CAP(last\ stage)}$ =160, $N_{SW(last\ stage)}$=35. V_{IN} is 0.8 in this technology. Figure 5.7 shows the layout generated with these design parameters, whose area is 190μm×470μm. It takes a few hours from the input specifications

to the final layout. According to the post-PEX simulation results, the generated DC-DC converter achieves 75% efficiency.


```
{
    "module_name": "DCDC_TOP_0p62V_2p0mA",
    "generator": "dcdc-gen",
    "specifications": {
        "Iload (mA)": 2.0,
        "Output voltage (V)": 0.62,
        "Clock frequency (kHz)": 40000
    }
}
```


(a)



(b)

Figure 5.6 (a) An input JSON file for the proposed DC-DC converter. (b) The configuration of the DC-DC converter generated with this JSON file.

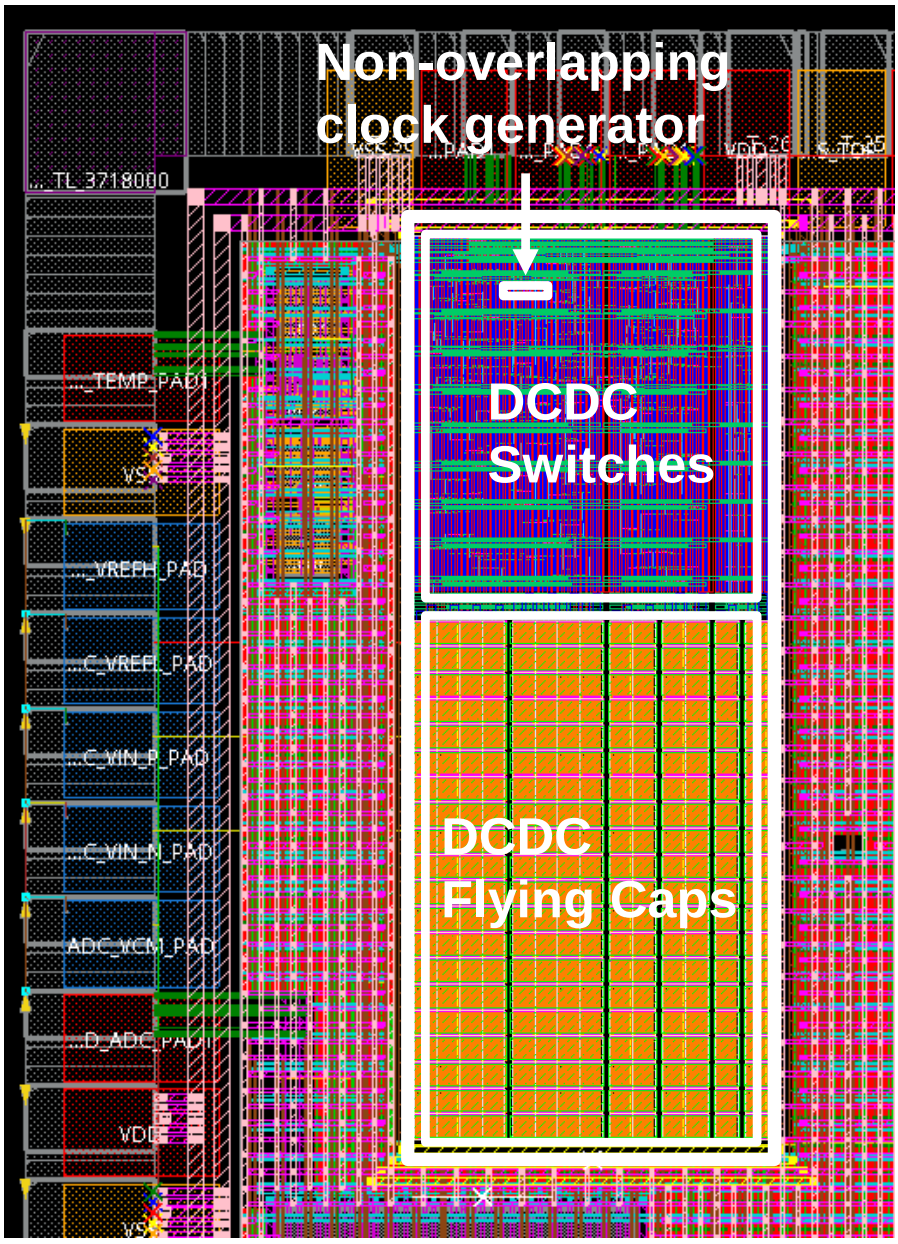


Figure 5.7 A layout of the generated DC-DC converter

5.6 Conclusion

In this chapter, a new switched-capacitor DC-DC converter design methodology was presented. The proposed method finds optimal design parameters from the input specifications, based on the theoretical analyses of the energy optimal operation. Given the input specifications, the proposed DC-DC generator makes an optimal netlist and its layout on the cell-based analog design approach [5] within a few hours.

Chapter 6 **Conclusions**

This dissertation introduces the implementations of low-power μprocessor systems with novel power management techniques in chapter 2 and 3, which offer energy efficiency in miniaturized sensors. In chapter 4 and 5, the dissertation introduces essential sub-blocks for low-power μprocessor systems, which are a wide-range level converter and a switched capacitor DC-DC converter.

Chapter 2 presents a novel on-chip closed-loop MEP tracking method that guarantees energy optimal operation at all times. The main contribution of this work is introducing a new concept of optimal leakage ratio, and leveraging it to find the optimal operating points. The proposed approach requires very low area and power overhead, but shows a great accuracy according to the measurement results. The fabricated processor achieves 6.4 pJ/cycle at 0.55V and 500 kHz clock frequency, which was the lowest energy per cycle among the commercial μprocessors when we presented the work in *ISSCC* 2019.

Chapter 3 presents a μprocessor system that features platform-level deep sleep-mode at high temperature. Due to the limited battery size and exponentially increased leakage, it is challenging for miniaturized sensors to have long enough lifetime at high temperature. To solve this issue, we designed a new SRAM bitcell and achieved the lowest bitcell leakage with a competitive size. The proposed system guarantees a constant 0.54μW of the sensor sleep power at 125˚C, which is 26× lower than the baseline design.

In chapter 4, a new leakage-biased wide-range level converter is presented. For low performance and extremely power constrained applications, sub-threshold circuits are commonly

used. In this case, a wide-range level converter is necessary to convert sub-threshold input signals to high I/O voltages. By biasing the circuit using the leakage current, the proposed level converter offers robust operation across a wide range of low and high supply voltages as well as PVT variations. It shows 60.5fJ (V_{DDH}=2.5 V) switching energy, marking a 2.6× improvement over prior works

In chapter 5, a new design methodology for switched-capacitor DC-DC converter is presented. The proposed method directly finds optimal design parameters from the input specifications based on the theoretical analyses, and therefore can be easily deployed in the analog circuit generator. Exploiting cell-based design approach [5] and the proposed design methodology, we designed a switched-capacitor DC-DC generator that generates a netlist and the layout within a few hours from the input specifications.

Although all of these new techniques presented in this dissertation were researched and invented for miniaturized wireless sensor applications, applicability of the proposed techniques and designs is not limited to the usage for the miniaturized sensors. The concept of optimal leakage ratio can probably be used to find the optimal operation points in high performance circuits as well with dynamic voltage and frequency scaling (DVFS). The sleep power reduction can effectively reduce the total power consumption in any applications that have intermittent data processing. A wide-range level converter is necessary for the sub-threshold operation in any applications. Moreover, since most of today's SoCs have multiple voltage domains, a DC-DC converter is a fundamental block in modern SoCs. We hope this work can contribute to various circuit systems, not being limited to low-power digital circuits for miniaturized sensors.

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