Multiple-element Direct Digital Beamforming
For Next Generation Wireless Communication Systems

by

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Abstract

Emerging wireless networking standards such as WiFi-6E optimize capacity using Orthogonal Frequency-Division Multiple Access (OFDMA), and multi-user multiple-input multiple-output (MU-MIMO). This work explores direct-digital-to-RF transmitters and phased array for next-generation wireless systems. Prototypes devices demonstrate the new techniques. Contributions include: 1) using delta-sigma modulation (DSM) to generate a low bit-width digital signal so that small and high-linearity DAC can be used, 2) different filtering strategies to eliminate the DSM quantization noise, including N-path filtering and FIR filtering, 3) developing a complete flow for the DSM design and implementation, prototyping a filter-free DSM NTF to directly meet the spectral mask, 4) circuit techniques to enhance the efficiency of the DDRF system, including B2T encoding, H-bridge DAC, and current dumping, 5) a frequency-plan methodology for the DDRF system that considers image duplication during up-sampling, noise folding during up-mixing, and digital automation bottlenecks.

The first prototype is an 8-element digital beamforming RF modulator that allows accurate steering of multiple independent beams. The key to its efficiency is the pairing of area-efficient bandpass $\Delta\Sigma$ modulation with N-path filtering to suppress quantization noise. Beamforming Digital Signal Processing (DSP) is enabled by careful frequency management, facilitating efficient digital phase shifting, up-sampling, and up-conversion. A 40-nm CMOS prototype generates two 1.2 GHz beams, with 40 MHz RF bandwidth. The prototype consumes 128 mW and occupies an active area of only 0.19 mm^2, which is only 16 mW and 0.02 mm^2 per element. This represents an

order-of-magnitude improvement in the area and power consumption per element compared to state-of-the-art digital to RF modulators.

The second work extends the bandwidth and frequency range of digital-phase-shifting direct-digital-to-RF TX, paving the way for use in MU-MIMO wireless networking applications. A sigma-delta modulation chain enables an inherently linear 1b RF DAC. Low-loss FIR filtering suppresses delta-sigma DAC noise. An H-bridge combines current-DAC, FIR-filtering, and RF up-conversion for efficiency. A 28 nm CMOS 8-element 6 GHz beamforming TX has a per-element area of 0.01 mm^2 and a per-element power of 47.5 mW.

Noise-shaping is essential for DDRF, but filtering out-of-band (OOB) quantization noise is difficult at 6 GHz for WiFi 6E. We present a filter-free DDRF architecture in the third prototype that realizes targeted noise-shaping (TaNS) to meet the spectral mask. We apply TaNS to attenuate noise at an offset of 2-10xBW, moving it far out-of-band. The prototype is fabricated in 28nm CMOS with an active area of 0.022 mm^2, achieves 80 MHz RF bandwidth, and shows the feasibility of 64-QAM modulation up to 281 Mbps.

Chapter 1 Introduction

High-speed wireless communication system is vital for many applications (e.g., WiFi, Internet of things and autonomous driving) because of the need for high speed, high bandwidth low latency, and high efficiency. This chapter introduces several concepts including beamforming techniques, direct digital to RF conversion, and delta-sigma modulation. These are essential concepts and techniques for high-speed wireless communication. These techniques are elaborated in three sections in this chapter and applied in three prototypes. Section 1.4 analyzes the design trade-offs in three subsections and Section 1.5 outlines of the rest of this dissertation.

1.1 Transmit Beamforming Techniques

Transmit beamforming is essential for high-speed wireless communication, especially for 5G and Multiple-Input Multiple-Output (MIMO) wireless systems. Multiple, accurate, independent beams are vital for MIMO systems. Beamforming also reduces the per-element TX power requirement. A large number of antennas produces a narrower beam with higher energy density, but this also requires more accuracy in the beam direction. These requirements are best met by digital beamforming.

WiFi-6E is the next generation of WiFi. MU-MIMO and OFDMA are two key technologies that enhance WiFi-6E. MU-MIMO (multi-user, multiple-input, multiple-output) allows a router to communicate with multiple devices simultaneously. OFDMA allows one transmission to deliver data to multiple devices simultaneously. Transmit beamforming is essential for high-speed wireless communication, especially for MU-MIMO in WiFi-6E. Digital beamforming has the

critical advantages of supporting multiple beams and facilitating fast switching of beams. However, challenges of beamforming for WiFi-6E include the wide channel bandwidth of 160MHz and the high RF frequency. Because of the need for multiple elements, a compact, low-power solution is essential.

There are few publications on TX beamforming systems for 6 GHz WiFi-6E. [1] is a switched-capacitor power amplifier (SCPA) with four elements and targets an RF frequency range of 1.45-2.15 GHz. [1] delivers a high output power thanks to the power-combining of capacitor branches. However, a drawback is the large chip area of 5 mm^2 due to the large 10-bit switched-capacitor array and on-chip matching network. [2] is a current-mode digital PA (IDPA) with four elements that targets the 3-7 GHz RF frequency range. The prototype in [2] combines a switched-mode digital power amplifier, and feed-forward controlled dynamic matching network for high efficiency. The prototype in [2] has a large die area of 8.6mm^2 because of the large DAC array and digital buffer chain.

Previous work gives some insights into how to implement the digital phase shifter, which is a vital component of a beamforming system. In [1], a multi-phase injection-locked ring oscillator combines with a multi-phase logic decoder to provide precise phase resolution. [2] utilizes a digital phase shifter for phase modulation. Digital phase-shifting, along with a high-resolution current-DAC (I-DAC), leads to low phase error. Both [1] and [2] are polar systems and require extra cordic processing.

Complex weight multiplication (CWM) is a natural choice for phase shifting in cartesian systems with I and Q inputs like our prototypes. CWM is advantageous over digitally-controlled delay lines because delay lines can be hard to control and are sensitive to the supply voltage. Furthermore, the power consumption of controlled delay lines can become high as frequency

increases [3]. CWM, on the other hand, can be very precise in controlling the phase with much higher efficiency.
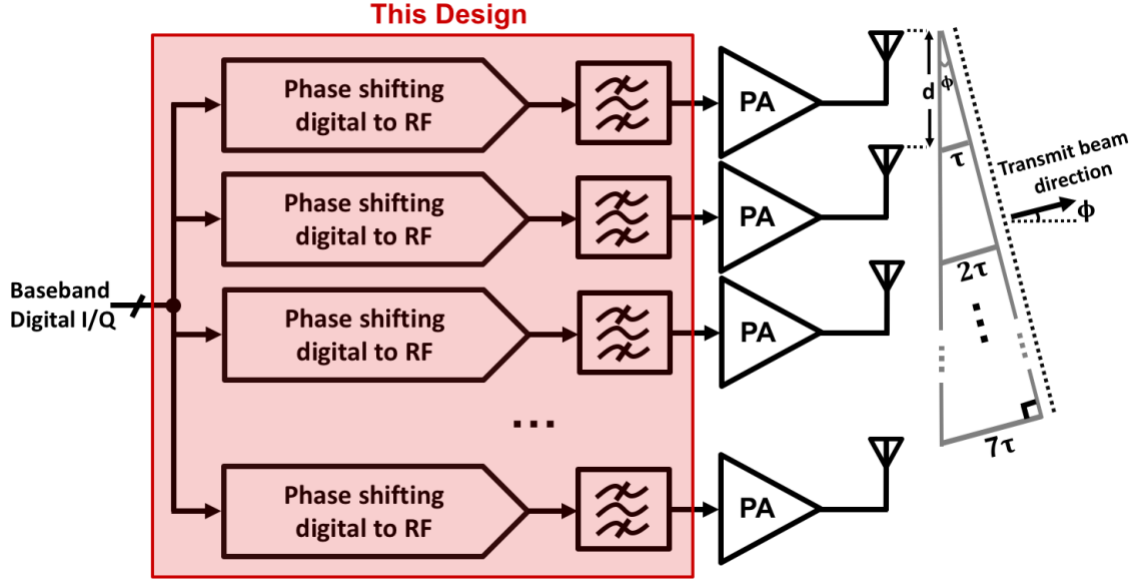
Figure 1.1: Complete beamforming TX model used for calculating the desired phase shift.

Figure 1.1 shows an overview of a general beamforming TX architecture. We consider the phase shift for each element in the array. We also review the general digital-beamforming architecture. Figure 1.1 shows a general model of the transmit beamforming system. The model has eight identical DDRF transmitters, each with a different phase-shift. For a desired beam angle of ϕ, we derive the desired phase shift for each channel as follows:

Assuming the element spacing is d, then the time delay difference between adjacent channels should be $\tau = d \cdot sin\phi/c$, The delay for each channel can be represented as:

$$\tau_k = k \cdot d \cdot sin\phi/c \quad k = 0,..,7 , \tag{1}$$

in which k stands for the antenna element index and c is the speed of light.

The antenna spacing, d, is usually chosen to be $\lambda/2$ for a reasonable beam width and to avoid a grating lobe [4]. Then with $d = \lambda/2$ and $f_c = c/\lambda$ (f_c is carrier frequency), we get:

$$\tau_k = 0.5k \cdot sin\phi \,/f_c \,, \quad k = 0,..,7 \tag{2}$$

Our desired transmit signal at the kth element can be represented as:

$$x_k(t) = \cos\big(2\pi f(t - \tau_k)\big) = \cos\left(2\pi ft - 2\pi f\tau_k\right) \tag{3}$$

For narrow-band beamforming, we can approximate the incident wave frequency with the carrier frequency, which yields $f \approx f_c$. Then we obtain the desired phase for each channel to be shifted as:

$$\theta_k = 2\pi f\tau_k \approx 2\pi f_c\tau_k = \pi k \cdot sin\phi, \quad k = 0,..,7 \tag{4}$$

This phase shift can ultimately be implemented using complex weight multiplication (CWM). If using digital controlled delay lines, it is easy to derive from (2) that τ_k can reach 3.5 ns for a 1 GHz RF frequency. Cascades of delay cells are needed, and in addition a separate voltage supply might be necessary for precise delay control. Furthermore for higher digital sampling frequencies, each delay cell may consume a lot of power.

Figure 1.2 shows the CWM phase-shifting operation in more detail. The desired phase shift, θ, for each channel is calculated from the desired angle for the main transmit lobe(s) as given by (4). Phase shifting is implemented with complex weight multiplication (CWM). The fractional bandwidth and the number of elements are small enough so that phase-shift is a good approximation to time delay. As a rule of thumb, phase-shifting is sufficient if the bandwidth is less than 10% of the carrier frequency [5]. In CWM, we multiply the I and Q inputs by $\cos\theta$ and $\sin\theta$, respectively, and add to form the shifted, I', data stream. Similarly, we multiply by $\sin\theta$ and $\cos\theta$, respectively, and add to form the shifted Q' data stream. We multiply with two sets of weight coefficients to form two independent beams and then add these together to form the multi-beam phase-shifted I/Q baseband data. In the first prototype of the beamforming TX, one set of I/Q input

is fed from off-chip because the chip is I/O limited. In the second and third prototypes, two different sets of I/Q input are fed into the phase-shifters because on-chip SRAM avoids chip I/O limited anymore.
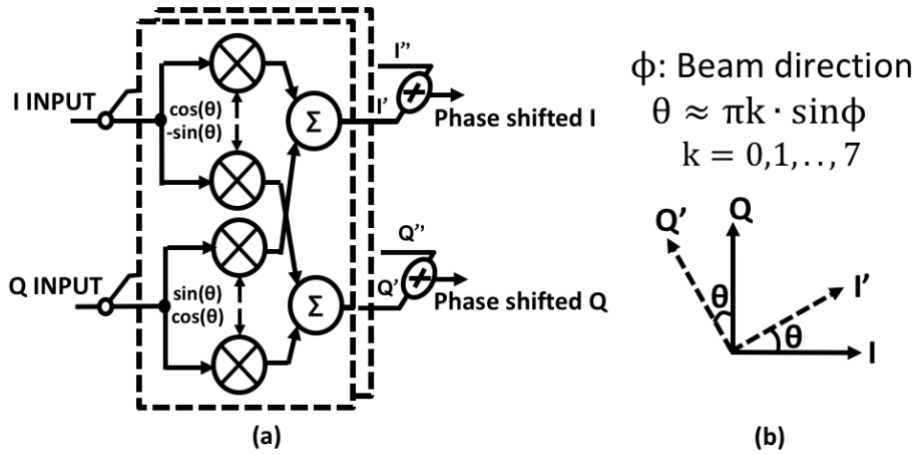
Figure 1.2: Phase shifting using complex weight multiplication (CWM).

1.2 Direct Digital RF (DDRF) System

In conventional analog beamforming, the multiple analog stages in the transmit signal chain all contribute to non-linearity, mismatch, and noise, which are big challenges to beam accuracy. In particular, the mixer and PA stages are significant contributors to non-linearity in a conventional transmitter. For example, as shown in Figure 1.3 (a), the amplitude imbalance of the I/Q modulated signals may lead to variation in the transconductance in the analog mixer [6]. Further challenges are the finite dynamic range of the V-to-I stage and switch pair, as well as the phase noise and spur added by the LO signal [7]. Insertion loss in the signal path and the difficulty in forming multiple simultaneous beams are additional concerns with analog beamforming.

The requirements for beam accuracy and multiple beams are best met by digital beamforming. The challenges of analog transmission motivate mixer-less digital-to-RF transmit schemes, especially so for beamforming systems. Digital Direct to RF transmission avoids analog

non-idealities, since the up-mixing, along with the phase-shifting, can be digital. Digital phase-shifting also facilitates multiple simultaneous beams. Further, a mostly-digital architecture is scaling friendly. However, conventional digital transmit beamforming requires extensive DSP, large DACs, up-converters, and filters, and so tends to be large and power-hungry.

Digital-direct RF is an attractive emerging approach because it is easy to configure, and with fewer analog components, a digital direct RF architecture is usually smaller and more power-efficient. The main challenge for DDRF at very high RF frequency is the difficulty of synthesizing logic that can operate at high speeds. The clock rate can reach four times of the RF frequency for quadrature mixing. Timing mismatch in the DAC at this clock rate can cause large non-linearities. Another problem is that it is extremely hard to design an analog bandpass filter at high RF frequency without using inductance. We need a bandpass filter to attenuate out-of-band spurs.
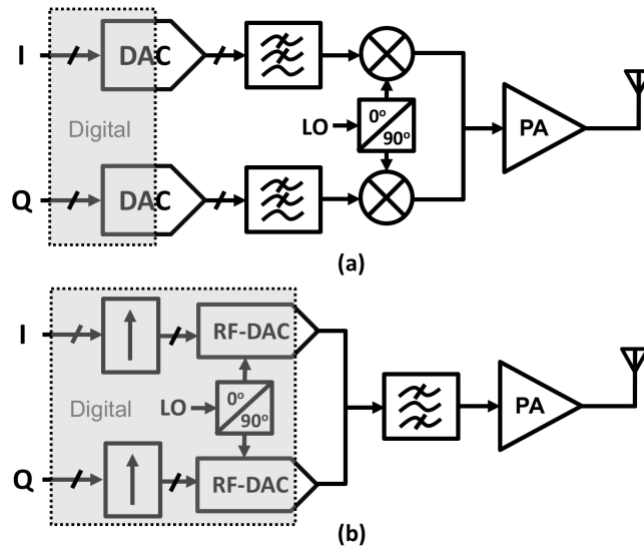
Figure 1.3: Conventional TX versus digital-direct-to-RF TX.

While impressive progress has been made on standalone DDRF transmitters [8]-[10], existing approaches require too much die area and consume too much power to be practical for

transmit beamforming. Efficiency is very challenging for practical DDRF. Most current DDRF architectures require a high DAC resolution for high SNR. This high DAC resolution complicates the DAC design and results in a large die area. In other cases, off-chip filtering or calibration is needed. [8] uses a smaller 10-bit DAC and programmable $\Delta\Sigma$ modulator with out-of-band notch filtering for a 0.82 mm^2 area. [9] delivers charge through a 12b resistive DAC and occupies 0.22 mm^2, but requires off-chip DSP for charge calculation. [10] uses bandpass digital $\Delta\Sigma$ modulation but requires off-chip analog filtering to suppress the substantial shaped quantization noise. Existing DDRF schemes have high power consumption in the range of 150 mW to 380 mW. The die area of these DDRF implementations ranges from 0.2 to 1.3 mm^2 per element. The large amount of DSP, the high digital signal processing speed, and the significant DAC size restrict these schemes to single-element use, and none support transmit beamforming.

	[8]	[9]	[10]
Architecture	$\Delta\Sigma$ + MS DAC	RQDAC	Bandpass $\Delta\Sigma$
DAC resolution [bits]	10	12	1
Power consumption [mW]	150 @ 900 MHz	24.8 (not including off-chip DSP) @ 2.4GHz	139 @ 700MHz
Active area [mm^2]	0.82	0.22	5.2
Technology [nm]	28	28	130

Table 1.1: DDRF transmitters.

1.3 Delta-Sigma Modulator

Delta-sigma modulation (DSM) is a commonly used method for converting an analog signal into a digital signal. It is also used for encoding a high bit-width digital signal into a low-bit one. A DSM trades in-band resolution for a high sampling rate and moves quantization noise out-of-band through noise-shaping. DSMs are widely applied in the wireless communication
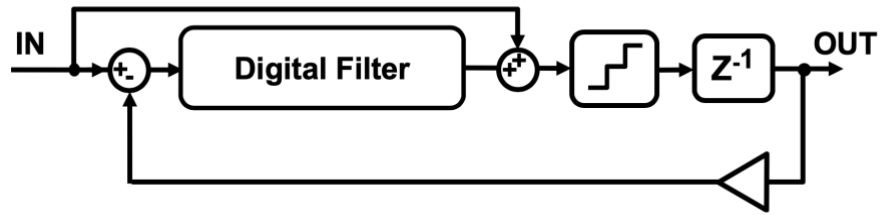
system.

Figure 1.4: Block diagram of a digital DSM.

Digital DSMs are a popular choice for DDRF systems. Figure 1.4 shows a general form of a digital DSM. An advantage is that digital DSMs are highly programmable, and this is highly desired in DDRF systems - All of the filter coefficients can be programmable if needed. Also, the low-bit bitstream output leads to a smaller DAC array and enables easier matching. A single-bit DSM with single-bit DAC is inherently linear. Several previous works take advantage of the inherent linearity of a single-bit DAC. In [8], a 16-bit baseband input is converted to 10-bits; since it remains a long bit-width after the conversion, extra mismatch-shaping is used, and the 10-bit DAC still occupies a significant die area. This high-resolution DSM itself consumes 53mW at a 1.8GS/s sampling frequency. On the other hand, a DSM with a low bit-width output saves power because it makes the implementation of the quantizer and the feedback path much simpler. In [11], a MASH DSM converts a 14-bit input to a 3-bit output. It is interesting that this DSM is configurable to be bandpass or highpass, depending on the RF output frequency needed. The MASH modulator architecture with pipelined bit unit cells ensures the DSM sampling frequency can be made high enough to support high bandwidth if needed. Although this is not the most efficient way to implement a DSM, it makes it possible to synthesize a 3GS/s DSM in 130 SiGe BiCMOS.

Similarly, in our work, balancing the efficiency of DSM and the possibility of synthesizing

at the targeted sampling frequency are the main challenges. Technology scaling increases the potential clock rate for the digital circuit and eases the digital automation bottleneck. This facilitates more aggressive techniques, e.g., a higher-order NTF. Various techniques can also facilitate a faster sampling rate, e.g., pipelining within a bit unit, time interleaving (TI), and so on. These techniques inevitably involve design trade-offs. Time interleaving a DSM requires N times as much hardware to realize interleaving with polyphase decomposition [12] or using a straight-forward parallel architecture. Extrapolation [13] can save the extra hardware but sacrifices input bandwidth because the extrapolation does not create any new input information. Furthermore, as the sampling rate is pushed higher, automatic place-and-route requires extensive clock tree buffering to enable long wire routing when synthesizing the digital DSM. Chapter 3 provides more details on the digital DSM design, including the design of the noise-transfer function (NTF), dithering, and time interleaving techniques. Chapter 3 also elaborates on the digital DSM design in each prototype.

1.4 Design Considerations

In designing a beamforming TX system, various aspects are considered, including power and area budget, target carrier frequency and bandwidth, and the desired spectral mask. We discuss this in three sections.

1.4.1 Power and Area Budget

As mentioned, existing single-stripe DDRF architectures consume more than 150 mW and occupy 0.2 mm^2 per element. The high power and area mean that these are not good candidates for multi-element operation. Existing multi-element designs are also huge, more than 5mm^2. Our

work's main goals are to achieve an order of magnitude improvements in both the power and area compared with other work targeting similar applications and frequency ranges. This requires careful frequency planning throughout the transmit stripe to optimize the power budget allocation. Chapter 2 elaborates on the frequency plan. For the compact area, we favor an inductor-less design because inductors are very bulky and dominate the area, especially in a multi-element architecture.

1.4.2   Carrier Frequency and Bandwidth

The carrier frequency and bandwidth are basic specifications of wireless communication system design. In general, a higher frequency introduces challenges. For a 1.2 GHz RF frequency, thanks to its high Q, an N-path filter can well handle the shaped quantization noise generated by a DSM. The N-path filter also provides out of band attenuation. However, N-path filtering is not practical for a 6 GHz RF frequency.

At RFIC 2018, we presented an architecture that utilizes a bandpass delta-sigma modulator to generate the 1.5-bit noise-shaped bitstream and an N-path filter to attenuate the shaped noise. Our RFIC 2018 work targeted an RF frequency of 1GHz. Quadrature mixing requires the modulator to run at a sampling rate four times the RF frequency. For WiFi-6, this would require a 24 GHz clock rate. It is impossible to synthesize digital circuity to run at this high clock rate in 28nm CMOS. An alternative is to break the constraint between the sampling rate and center frequency (i.e., fs =4 fc). In our most recent prototypes, we place the baseband DSM before up-mixing, and therefore any fc = n*fs/2 is appropriate. Although this relaxes the digital clock rate, as mentioned, the design of the N-path filter is extremely challenging for a 6 GHz RF. Severe duty cycle errors and duty-cycle reduction in the non-overlap clock generation are particular problems.

A bandwidth below 10 MHz would require a 400MS/s sampling rate to achieve an over-sample ratio (OSR) of 20 (typical for a low-bit or single-bit DSM). A 400MHz rate is feasible for

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logic synthesis and within limitations of chip IO speed. An 80MHz bandwidth requires a sampling rate of 3.2GS/s for an equivalent OSR. This high rate is a bottleneck for digital automation. Furthermore, a 3GS/s sampling rate exceeds IO speed for on-chip SRAM, not to mention off-chip data delivery. Even if SRAM IO can reach 3GS/s, an extremely long lookup table (LUT) would be needed if there is no pre-upsampling. Therefore up-sampling is essential, and this also necessitates other design considerations (e.g., image attenuation).

1.4.3 Meeting the Mask – targeted noise shaping (TaNS)

The spectral mask is one of the most common ways to evaluate a TX design. The spectral plot contains information such as output power, adjacent channel leakage, and out-of-band attenuation.

Noise-shaping is essential for DDRF because it enables high in-band SNR with a small, low-resolution DAC. Noise-shaping facilitates excellent in-band modulation accuracy (i.e., EVM) by relocating quantization noise from in-band to out-of-band (OOB) but requires filtering of adjacent-channel and OOB emissions to meet spectral mask requirements. The two main challenges for noise-shaping DDRF at a 6 GHz carrier frequency are: (1) the aggressive high-frequency bandpass filters needed to attenuate the shaped out-of-band quantization noise and (2) the difficulty of synthesizing logic that operates at such high speeds. We present: (1) a filter-free, noise-shaping DDRF architecture that targets noise-shaping (TaNS) to meet spectral mask requirements and avoids the complexity and power/area cost of a bandpass filter and (2) a fully synthesizable DDRF architecture in the third prototype.

Filtering of OOB quantization noise is essential to satisfy the spectral mask for noise-shaping DDRF schemes but is very difficult at 6GHz. Inductor-based filters are bulky and

constrained by the quality factor of inductors. N-path filters suffer from limited dynamic range, are sensitive to non-ideal clocking, and are restricted to frequency ranges below 3GHz. Combining digital filtering (e.g., FIR filtering) with digital noise shaping is an attractive alternative [14]. However, high-bandwidth FIR filters do not provide sufficient attenuation at frequency offsets of 1-3x the signal bandwidth to satisfy the spectral mask. A narrower band FIR response requires either a large number of taps or a long tap delay. A long tap delay causes more repetition in the spectrum, while a larger number of taps is a challenge for high-speed digital circuitry. Other DDRFs use Nyquist DACs [15] or make do with moderate noise shaping [8] - all at the cost of a large DAC array and extensive post-calibration for the mismatch.
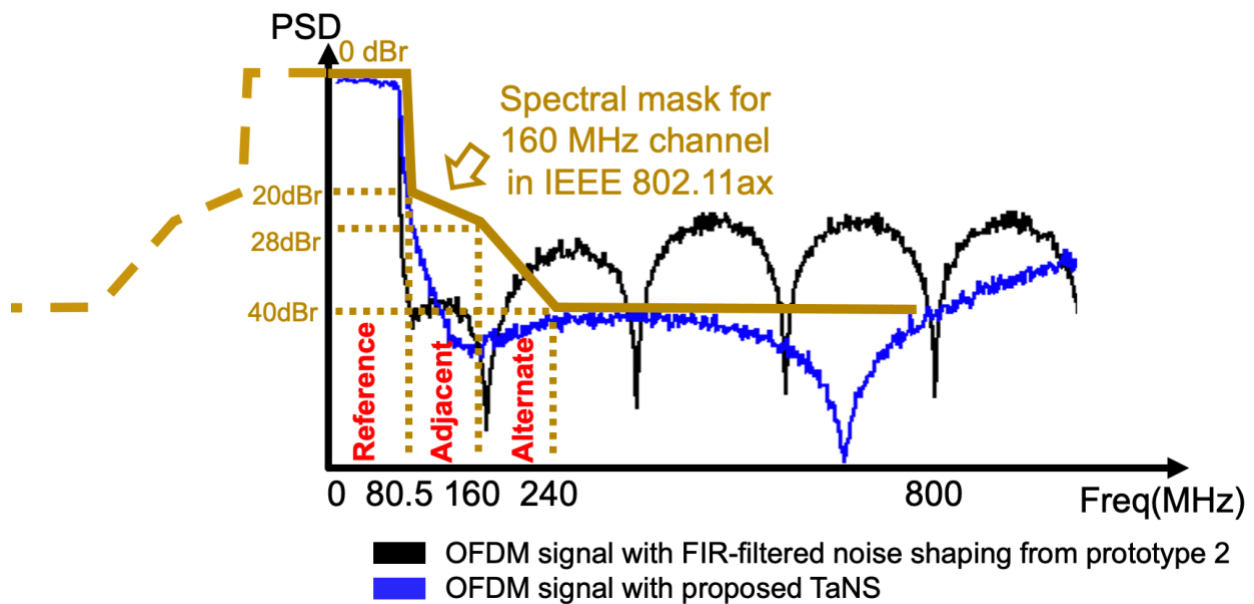
Figure 1.5: (gold) 802.11ax spectral mask, (black) OFDM signal with conventional noise-shaped DDRF and FIR filtering does not meet and mask (black), and (blue) TaNS DDRF meets the required mask without filtering.

We introduce targeted noise shaping (TaNS) to meet the WiFi 6 spectral mask without filtering. To motivate TaNS, Figure 1.5 superimposes the OFDM signal spectrum from a noise-shaped DDRF with FIR filtering in our second prototype on the required 802.11ax spectral mask. This traditional approach fails for alternate-channel noise - it places too much noise between 1x

BW and 10x BW but is too conservative beyond 10x BW. Figure 1.5 also shows that the spectrum from our TaNS architecture meets the mask without filtering. Critically, TaNs DDRF moves noise from 2-10x BW to far out-of-band, where the output matching network and antenna easily filter it.

We show more details about the design of TaNS NTF in Chapter 3.4.3.

1.5 Thesis Overview

This dissertation is organized as follows. Chapter 2 discusses the frequency plan based on the standard that trying to meet, including the bandwidth, RF center frequency, etc. In Section 2.2, we discuss the frequency plan for the prototypes. We discuss the transmit stripe block placement strategy first and analyze potential issues including image duplication and noise folding. Solutions are proposed to solve these issues. Chapter 3 demonstrates a design flow for digital DSM from the NTF characterization to the implementation consideration. Chapter 3 also discusses dithering and introduces the time-interleaving and polyphase decomposition. In Chapter 3.4, we discuss the DSMs used in three prototypes. Chapter 4 discusses the DAC and RF filter design. The filter is to suppress the shaped the out-of-band quantization noise generated by DSM. We present the DAC and filter structures for the three prototypes. Chapter 5 presents the die micrographs, test setups, and measurement results for the three prototypes. Chapter 6 concludes the dissertation and suggests future work.

Chapter 2 Frequency Plan

2.1 Introduction

A frequency plan is essential to optimize the power budget allocation throughout the transmit stripe. Good frequency planning directly determines design feasibility, and a detailed frequency plan is essential before the final implementation. We discuss the frequency plan in this chapter mainly for two frequency ranges: an RF frequency around 1 GHz and an RF frequency around 6 GHz. Table 2.1 gives an overview of the specifications of the prototypes. These are the main guidance in architecting the TX array systems and finalizing the frequency plan. While the first prototype is not specifically designed to meet a particular standard, it does meet the specifications of some of the LTE and WiFi standards. The frequency range is 0.8-1.2 GHz, and the RF bandwidth is 40 MHz, which matches the intermediate LTE and WiFi specifications. For LTE, TS36.104 [16] specifies an 8% in-band transmit EVM requirement for 64-QAM for the wide area base station. For WiFi, the 64-QAM EVM requirement is -22 dB, or 7.94% [17], which is close to LTE specification. [1] The second and third prototypes are designed for the 6 GHz frequency range of WiFi-6. Emerging wireless networking standards such as WiFi 6 (802.11 ax), optimize capacity using Orthogonal Frequency-Division Multiple Access (OFDMA), and multi-user multiple-input multiple-output (MU-MIMO). WiFi-6E proposes a 20/40/80/160 MHz RF bandwidth over a 5.925-7.125 GHz carrier range with an indoor transmit power of 0 dBm (15 dBm outdoors).

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[1] Coding Rate=2/3, for OFDM 802.11a/g legacy devices and 802.11n devices.

	Prototype 1	Prototype 2	Prototype 3
RF frequency	0.8-1.2 GHz	Around 6 GHz	Around 6 GHz
RF Bandwidth	40	160 MHz	160 MHz
Input data rate	200MS/s	375MS/s	375MS/s
Technology	40 nm	28 nm	28 nm
Beamforming	8 channels	8 channels	N/A

Table 2.1: Specifications for the three prototypes.

2.2 Frequency Plan Based on Prototypes
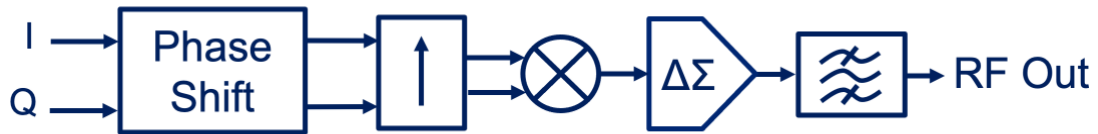
Figure 2.1: A common DDRF transmit stripe showing essential blocks.

Before diving into the frequency plans for each prototype, we consider the common essential blocks of DDRF and beamforming systems. These include the phase shifter, up-sampler, up-mixer, filter, and DAC, as shown in Figure 2.1. The phase shifter performs phase rotation for different transmit channels determining the overall beam direction. Phase shifting can be very energy-intensive because it requires complex multiplication operations. The up-sampler is the main frequency-domain conversion block, and as a bridge to the RF domain it upsamples the baseband signal. The up-mixer up-converts the baseband signal to RF frequency. The DAC converts the up-mixed digital signal to the analog domain. In a DDRF system, the DAC is usually

one of the final blocks, connecting to the power amplifier (PA) or directly to the antenna. In our work, we target a small DAC with high linearity. A digital DSM before the DAC converts the high bit-width digital signal to a low bit-width. In DSM, a large OSR is essential, requiring a high sampling rate. This requires that DSM be placed after at least one stage of up-sampling. At the same time, the DSM is a bottleneck for logic synthesis. A reasonable sampling rate for DSM should be carefully chosen.

A bandpass filter is usually required to meet the OOB spectral mask requirements. This filter is usually implemented as part of the output matching network. In our work, as mentioned, DSM is applied before the output DAC and therefore, the near-in in-band shaped quantization noise must be attenuated. For this reason, our system requires a more aggressive bandpass filter. There is some flexibility in where we can place this filter – it can be before or after the DAC. In our first prototype, we use an N-path at the end of the transmit chain. In the second prototype, we mitigate the challenges of designing a 6 GHz inductor-less bandpass filter by using two baseband digital lowpass filters before the DACs.

The placement of the up-mixer and the DAC can also be exchanged or combined. In our first prototype, there is a quadrature mixer before the DAC. In the second prototype, we implement a mixing DAC by using a four-phase 6 GHz clock to control the switch driver of the DAC. Other mixing techniques to enhance the output power of a higher Nyquist zone are also investigated.

2.2.1   First Prototype: 0.8-1.2 GHz RF Center Frequency

Our digital beamforming approach combines efficient digital-to-analog conversion with compact and efficient digital beamform processing. The key to our approach is the combination of bandpass digital to analog conversion and N-path filtering. A bandpass $\Delta\Sigma$ modulator directly generates the analog RF signal. The 1.5-bit DAC, driven by the $\Delta\Sigma$ modulator, is both very

compact and inherently linear. The out-of-band quantization noise is suppressed using a small on-chip N-path filter, eliminating the need for off-chip filtering. The combination of a digital bandpass ΔΣ modulator along with a 1.5-bit DAC facilitates an order-of-magnitude reduction in the DAC area.

The power and area of the beamforming DSP are minimized through frequency planning and simple and innovative up-sampling and up-conversion strategies. Conventionally, a bandpass ΔΣ modulator runs at 4 times the analog output frequency; however, in our case, this would lead to an excessive clock rate of 4.8 GS/s. Instead, we run the ΔΣ modulator at the reduced rate of 4/3 times the RF center frequency and make use of the image frequency.[2] Furthermore, in our frequency planning, the digital phase shifter runs 8 times slower, leading to an order-of-magnitude reduction in DSP power. Up-sampling is done through simple linear interpolation. Up-conversion is with simple MUX-based processing.
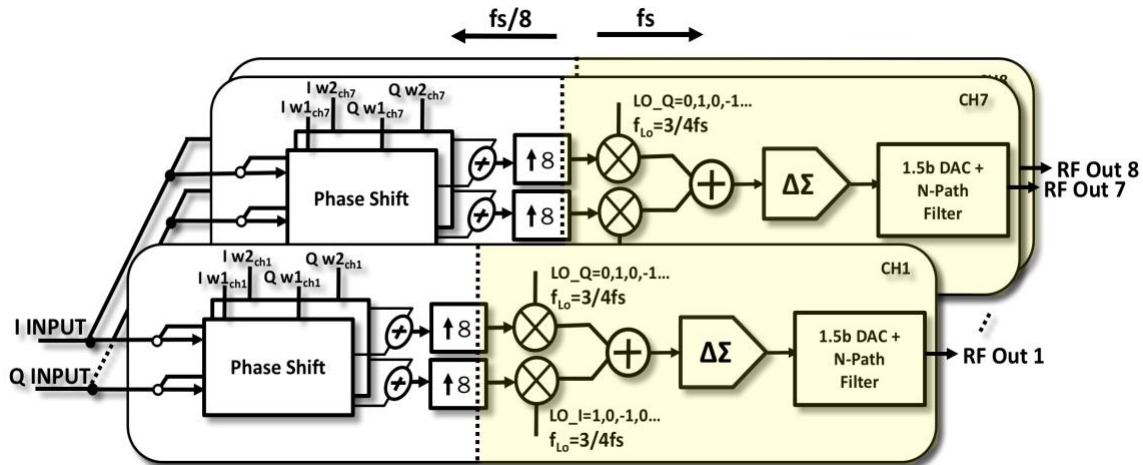
Figure 2.2: System architecture.

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[2] In [18], a similar technique is presented. Unlike our design methodology, which customizes the Noise Transfer Function (NTF) for target sampling frequency and bandwidth, [18] switches to the image frequency when the carrier reaches a certain frequency. Since the NTF of the ΔΣ modulator is fixed, this causes a discontinuity in the bandwidth between various carrier frequencies. In addition, the N-path filter in our design tracks the image frequency as its center frequency.

Figure 2.2 shows our overall system architecture. The eight-element RF modulator is comprised of eight identical stripes. Each stripe phase-shifts, up-samples, up-converts, converts to analog, and finally filters each per-element output RF transmit signal.
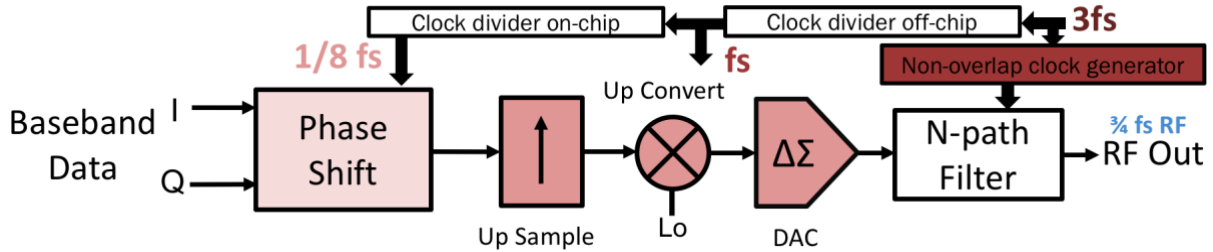
Figure 2.3: Frequency planning and synchronization.

Figure 2.3 illustrates the overall clock-rate distribution in the prototype chip. We use fs to represent the $\Delta\Sigma$ modulator processing rate. The other frequency domains are all represented in terms of fs for clarity. The RF center frequency is chosen as 3fs/4 for the simple representation of the digital LO and to reduce the power consumption of the digital signal processing. This is elaborated later in this section. The N-path filter requires a clock rate of 4 times of the RF center frequency for a 4-path non-overlap clock generation, which yields 3fs. The phase shifter operates at fs/8, which is chosen in consideration of DSP efficiency, simplicity of the implementation of linear interpolator, and reasonable digital I/O speed. This frequency planning greatly eases practical hardware implementation. The simplified processing and the relaxed DSP sampling rate make the digital synthesis of the entire DSP practical in 40-nm CMOS technology.

A single off-chip clock generator ensures that all operations and frequencies are synchronized. The RF center frequency is directly determined by tuning the clock rate, and then the N-path filter inherently tracks the RF center frequency. The RF bandwidth is chosen as fs/40, ensuring an Oversampling Rate (OSR, defined as fs/(2*bandwidth)) of 20 for the $\Delta\Sigma$ modulator. The N-path filter bandwidth, which is also fs/40, complements the NTF of $\Delta\Sigma$ modulator. In the

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rest of this discussion, fs is 1.6 GS/s. The RF bandwidth, the RF carrier, and input sampling frequency are 40 MHz, 1.2 GHz, and 200 MS/s, respectively, derived from fs.

Beginning with phase-shifting, in each stripe, phase shift approximates time-delay the baseband I/Q transmit data. The input baseband I and Q transmit data are multiplied with I and Q coefficients. We form two simultaneous beams by multiplying I/Q data with two sets of complex weights. After multiplication, the phase-shifted I/Q data from the different beams are summed to form single I and Q streams.

After phase shifting, the phase-modulated I/Q streams are up-sampled by 8 to the fs (i.e., 4/3fc) sampling-rate using linear interpolation. Linear interpolation has spectral advantages over interpolation with non-return-to-zero, while the hardware complexity is still low. The up-sampled baseband streams are up-mixed from baseband to RF by multiplication with digital I/Q local oscillator (LO) sequences. The ratio between sampling rate and RF center frequency (f_{LO}=3/4 fs), allows the digital LO signals to be represented by -1,0,1,0..., which greatly simplifies multiplication and summing and makes DSP processing a lot more efficient. We also use the image frequency to reduce the final sampling rate by a factor of 3.

Sampling at four times (4x) the output frequency greatly simplifies digital up-conversion, but the high sampling speed is challenging to implement. When the sampling rate is four times the RF center frequency, we can represent the digital sinewave LO sequence as 0, -1, 0, 1..., making LO multiplication trivial. This digital-domain I/Q mixing eliminates I/Q mismatch problems. However, for the desired 1.2 GHz RF signal frequency, this would lead to a sampling rate of 4.8 GS/s. Such a high DSP speed is a great challenge for digital beamform processing, especially for the digital $\Delta\Sigma$ modulator. In fact, the digital $\Delta\Sigma$ modulator becomes a critical path for DSP because the digital filter within the modulator requires high-resolution multiplications. This 4.8 GS/s speed

is very challenging in 40-nm CMOS and is not practical for Verilog-based design. The power

consumption of the DSP would also be very high – at least 100 mW per channel.

Instead, we operate at one third of the 4x sampling frequency (i.e. fs = 4/3fc) and make use

of the image to produce the RF output. As indicated by sample dots in Figure 2.4, with the reduced

sampling rate, the sampled digital LO sequence can still be represented as 0, 1, 0, -1…. We exploit

the image frequency at 3/4 fs, which is shown overlaid as a sine wave on the same plot. The output

spectrum of the ΔΣ DAC is shown in Figure 2.5. For a sampling rate of 4.8 GS/s, the fundamental

output frequency is 1.2 GHz. Instead, operating at 1.6 GS/s, the fundamental output frequency of

the modulator is at 400 MHz, and its image is at 1.2 GHz. Using the image allows us to run the

up-converter and the modulator at 1.6 GS/s, consuming only 16 mW per element and saving more

than 85% in digital power consumption.
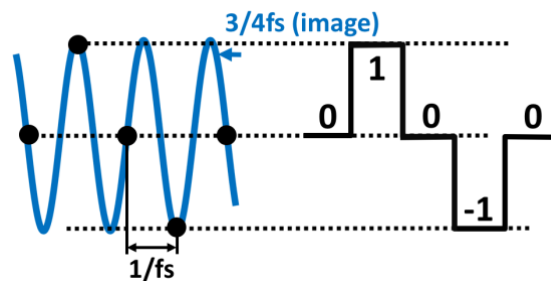
Figure 2.4: Illustration of subsampling of the 3/4fs LO and the resulting state transition sequence of the digital LO (i.e., 1, 0, -1, 0, …).
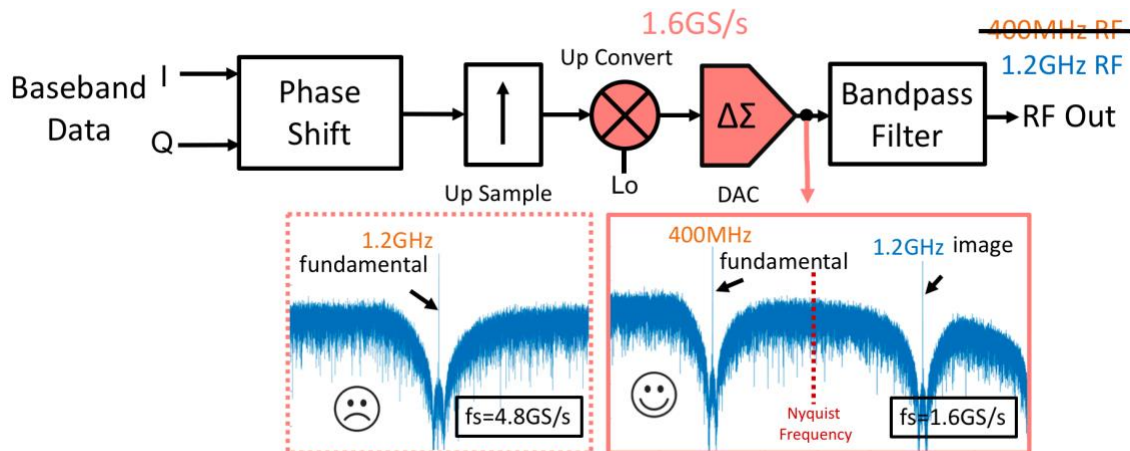
Figure 2.5: Comparison of the output spectrum of the bandpass ΔΣ modulator operating at fs=4.8 GS/s and at fs=1.6 GS/s in a single stripe.

We digitally up-mix the phase-shifted, up-sampled baseband signals to the RF frequency of 1.2 GHz by multiplying the up-sampled I and Q signals with digital I and Q LO sequences. We emphasize that the relationship between the sampling frequency fs and the RF carrier frequency (fc=3/4 fs) allows the digital LO to be represented by the same sequence as when fc=1/4 fs. Then, as shown in Figure 2.6, we sum the up-mixed I and Q sequences to form the digital RF output. In practice, we can further simplify this implementation because the I and Q LO sequences are orthogonal, and only one is non-zero at any time. Ignoring the 0 values, the resulting summed-up digital RF sequence is equivalent to MUXing between the I and Q streams and alternately multiplying by 1 and -1. This process greatly simplifies the up-mixing circuitry and reduces hardware complexity.
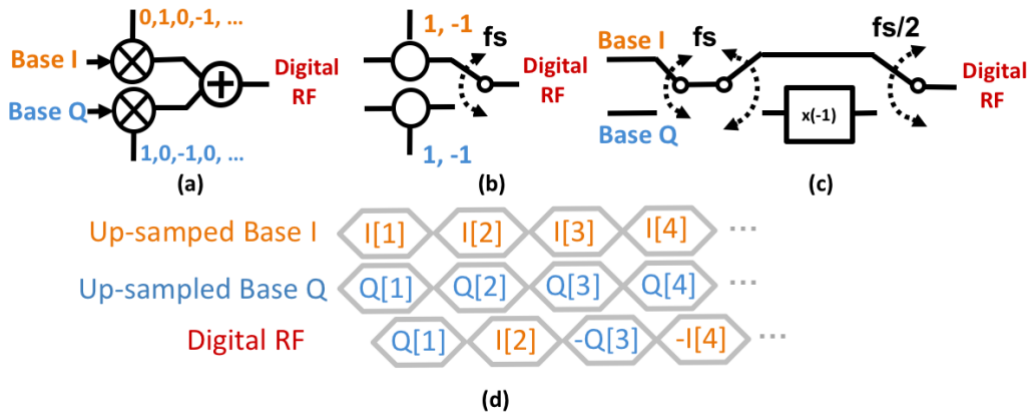
Figure 2.6: (a) Digital up-conversion and summing, (b) simplified with MUXing, (c) final implementation, and (d) timing diagram.

It is worth mentioning that mixing I and Q baseband data with orthogonal I and Q LO sequences, respectively, and then adding them together eliminates the high-frequency image. This single sideband (SSB) modulation reduces power consumption and is bandwidth efficient.

Using the image in the second Nyquist zone enables the DSM to run at 3 times slower but attenuates the signal power by around 12 dB. This is the primary disadvantage of this approach. As an example in [18], a 12 dB in-band power degradation and a 9-dB maximum ACPR degradation are observed in measurement. However, our design is not intended for direct RF power generation and a preamplifier is required.

The up-converted I and Q streams are combined into a single digital stream and then noise-shaped by a digital bandpass $\Delta\Sigma$ modulator to drive a 1.5-bit DAC, which directly generates the analog RF signal. This avoids the need for a high-resolution DAC, which would need a large additional die area and often requires extra calibration circuitry to reduce mismatch. The use of a minimal-resolution DAC, driven by a $\Delta\Sigma$ modulator, relaxes the DAC linearity problem and greatly reduces analog complexity [19]. Noise-shaping and oversampling with the low-resolution DAC deliver the equivalent in-band precision of a high-resolution DAC. The oversampling rate is the ratio between the sampling rate and signal bandwidth.
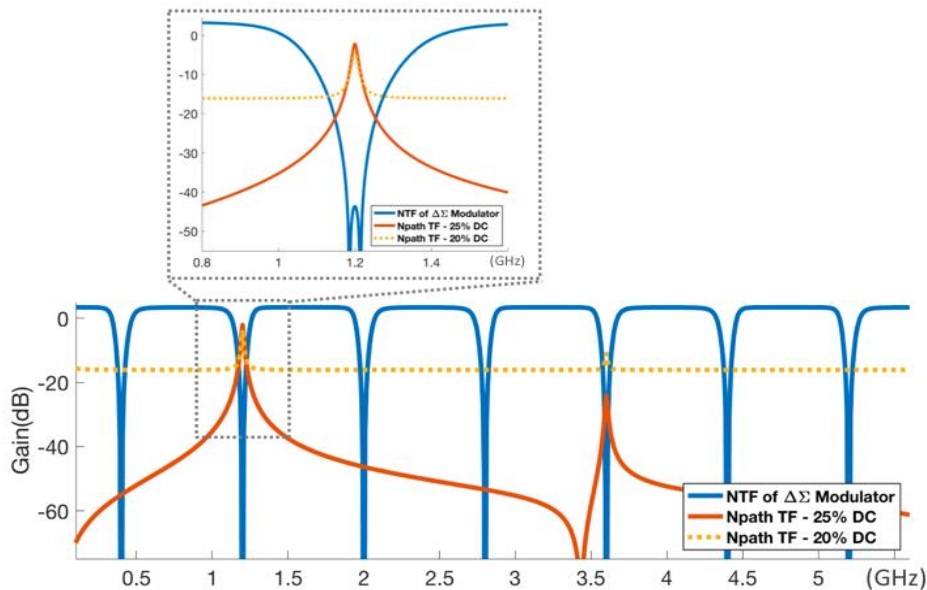
Figure 2.7: 4th order Inverse Chebyshev NTF and N-path filter frequency responses with different N-path duty cycles (DC).

We take advantage of the inherent linearity of a 3-level or 1.5-bit DAC. In Chapter 1.3, we mentioned that DSM can encode a high bit-width digital signal into a low-bit one. Low-bit bitstream output leads to a smaller DAC array and enables easier matching. In our work, we use a l.5-bit DAC, driven by a digital bandpass DSM for its very small area and immunity to mismatch. As in the case with a 1-bit DAC, a 1.5-bit DAC is inherently linear; however, a 3-level quantizer generates less quantization noise than a 2-level one, potentially providing a higher SNR. We also solve the problem of spurs caused by the low resolution (3-level) quantizer in the modulator by efficiently introducing near-Gaussian dither in the modulator. The dither scheme is elaborated in Chapter 3.

Counteracting the shaped quantization noise of DAC with on-chip bandpass filtering is another highlight of our scheme. The $\Delta\Sigma$ modulator translates the 15-bit-wide data stream into a 3-level digital signal to drive the 1.5-bit DAC. The modulator shapes the quantization noise to sides of the RF band, which is centered at fc, thereby providing a high SNR within the RF bandwidth. We add an N-path filter to reduce out-of-band quantization noise. The NTF of the modulator and the transfer function of the N-path filter are complementary. For this reason, an N-path filter is a natural match for the bandpass modulator since it can remove the shaped quantization noise produced at the output of the modulator. The transfer function of the N-path filter is tailored to the NTF. Although the N-path filter generates harmonics at multiples of the center frequency, the $\Delta\Sigma$ modulator also generates NTF notches in the corresponding image bands, as shown in Figure 2.7. A further advantage is that both the modulator and N-path clocking are derived from the same clock and inherently track the center frequency. An N-path filter is also small and efficient and does not require inductors, which are needed in other on-chip RF filters.

2.2.2   Second Prototype: 6 GHz RF center
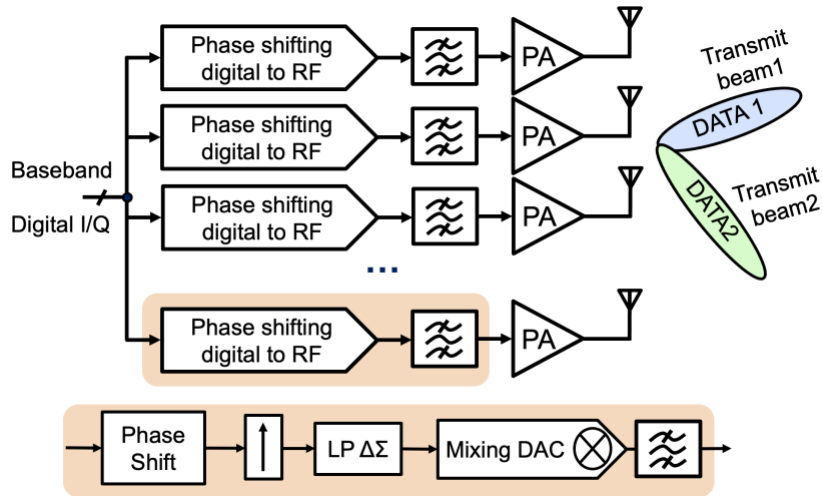
Figure 2.8: System architecture of the multi-input eight-element digital beamforming TX.

This beamforming TX prototype paves the way for digital-phase-shifting DDRF TX for wireless networking and other applications. Figure 2.9 shows the signal chain for a single element of the beamforming TX array. We also show an example of the spectrum at each node of a transmit stripe for a single-tone input. CWM logic operating at 375 MHz phase-shifts and combines multiple, independent baseband 375 MS/s I/Q data streams for true MIMO beamforming. Beamform processing at 8 times slower than the 3 GHz DSM clock rate ensures an efficient implementation. L-fold interpolation up-samples the phase-shifted baseband I/Q data and generate the 3 GS/s I and Q inputs to the lowpass delta-sigma modulators.

Two separate 3 GS/s (i.e., fs), digital, lowpass delta-sigma modulators generate noise-shaped single-bit I and Q bitstreams. The I/Q bitstreams feed an up-converting 1-b DAC to generate the 6 GHz RF (i.e., fc) output. FIR filters of the bitstreams effectively bandpass filters the quantization noise around the 6GHz RF fundamental, as shown in Figure 2.9. A critical advantage is that this bandpass filter is implemented in the digital domain and at baseband.
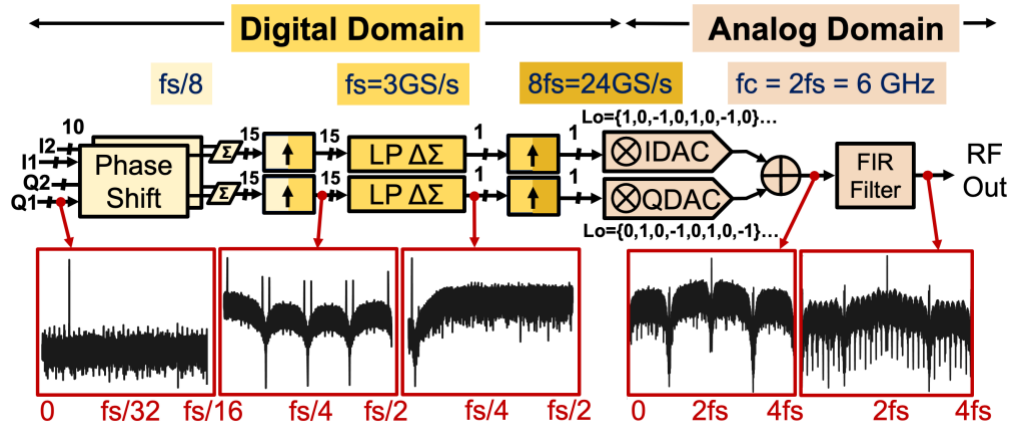
Figure 2.9: Signal model and spectra of a single stripe of the 6 GHz MU-MIMO TX.

Various aspects should be considered in the design of a DDRF TX system. These include strategies for up-mixing and filtering, considering different targeted carrier frequency and bandwidth.

As mentioned earlier in this section, a bandpass filter is usually required to meet the OOB spectral mask requirements in a TX system. In our work, the near-in in-band shaped quantization noise due to DSM must be attenuated. For this reason, our system requires a more aggressive bandpass filter compared to a scenario without noise shaping. In the first prototype, an N-path filter at the end of the transmit chain bandpass filters the quantization noise. For a 1.2 GHz RF frequency, thanks to its high Q, an N-path filter can well handle the shaped quantization noise generated by a DSM. The N-path filter also provides out of band attenuation. However, N-path filtering is not practical for a 6 GHz RF because duty-cycle errors and duty-cycle reduction of the non-overlap clocks limit attenuation.

In this work, we mitigate the challenges of designing a 6 GHz inductor-less bandpass filter using a pair of baseband I/Q digital lowpass filters before the DACs. This filtering is facilitated by summing delayed versions of the I/Q bitstreams to attenuate quantization noise. Chapter 4 elaborates on this scheme.

Figure 2.10 shows the signal model and the implementation of part of a single stripe, from the DSM output to the overall RF output. In the signal model, an effective sampling rate of 24 GHz is needed for quadrature mixing to up-convert the baseband bitstream to the 6 GHz RF center frequency. Extra up-sampling before the mixing DAC provides an effective sampling rate of 24 GS/s needed for quadrature mixing at 6 GHz RF. The implementation shown in Figure 2.10 avoids the 24 GHz clock rate by using four 6 GHz clock phases to sum the I and Q current signals. The I and Q DACs are alternately enabled, and the direction of the nominal DAC current changes each time to realize the mixing operation. Two delay chains in I and Q basebands facilitate equivalent RF bandpass FIR filtering. Moreover, a binary-to-thermal (B2T) decoder further enhances the H-Bridge DAC's power efficiency (Figure 2.10). Chapter 4 provides more details about the B2T decoder and H-bridge DAC.
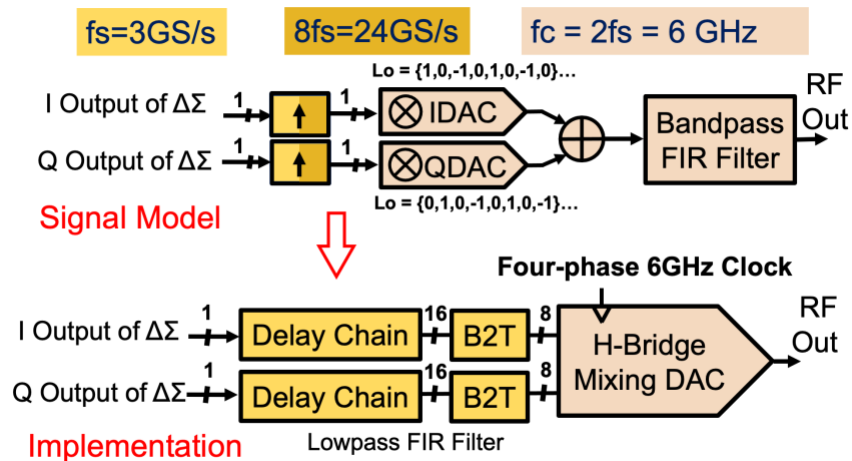
Figure 2.10: Signal model and implementation of the up-sampling and the filtering.

We use careful frequency planning to optimize the power budget allocation throughout the transmit stripe. Furthermore, frequency planning is essential to avoid issues with images and noise folding.

Baseband DSM has a noise folding challenge because the noise shaping precedes the up-mixer. In the up-mixing process from baseband to RF, noise on the opposite side of the targeted RF frequency folds back onto the signal. A bandpass DSM is free of this issue because the noise shaping follows the up-mixing. The quantization noise is shaped directly at RF frequency in this bandpass DSM, so no shaped noise contaminates the fundamental tone.[3] However, we do not use bandpass DSM in this prototype. The bandpass DSM needs to run at 4 times the RF center frequency because of the quadrate mixing. In prototype 1, the 4fc is 4.8 GS/s, which is still doable. In the 6 GHz RF center case, the sampling rate is 24 GS/s, which is not feasible in digital automation.

In our approach, the baseband DSMs precede the quadrature mixing, relocating the shaped quantization noise relocates after the mixing. Figure 2.11 illustrates how mixing affects the shaped noise for three fs scenarios. In the first case (yellow in Figure 2.11), fc is set to fs/2. Up-mixing at the mixing DAC not only up-mixes the signal around DC to fc (which is fs/2) but also folds back energy on the right of the spectrum. The signal around fs moves to fs/2, falling on top of the up-converted baseband fundamental. However, since quantization noise is shaped away from fs by the modulator, the folded quantization noise does not contaminate the fundamental tone; therefore, fc = fs/2 is an acceptable choice. However, for a 6 GHz RF, fc = fs/2 would require a 12 GS/s sampling rate.

The second scenario (red in Figure 2.11) is for fc = 2fs. Similarly, noise at 4fs folds back around 2fs. As the modulator shapes noise away from 4fs, therefore fc=2fs is also a good choice. Finally, we consider the scenario of fc = 1.8fs. Noise at 3.6fs folds back, and as quantization noise

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[3] Besides noise folding, up-sampler image-folding is a potential issue because up-mixing relocates the up-sampler image. L-fold interpolation sufficiently attenuates the images to avoid this issue.

at 3.6fs is not attenuated; therefore, the quantization noise contaminates the fundamental tone. It is easy to conclude that fc should be n*fs/2 because the attenuation of the quantization noise repeats around n*fs. Our final choice is fc=2fs because for a 6 GHz RF, 3 GS/s is a reasonable clock speed for digital automation. As already discussed, for an 80 MHz baseband bandwidth, 3GS/s is large to ensure a high OSR of 18. This constraint (fc = n*fs/2) helps finalize the frequency plan.
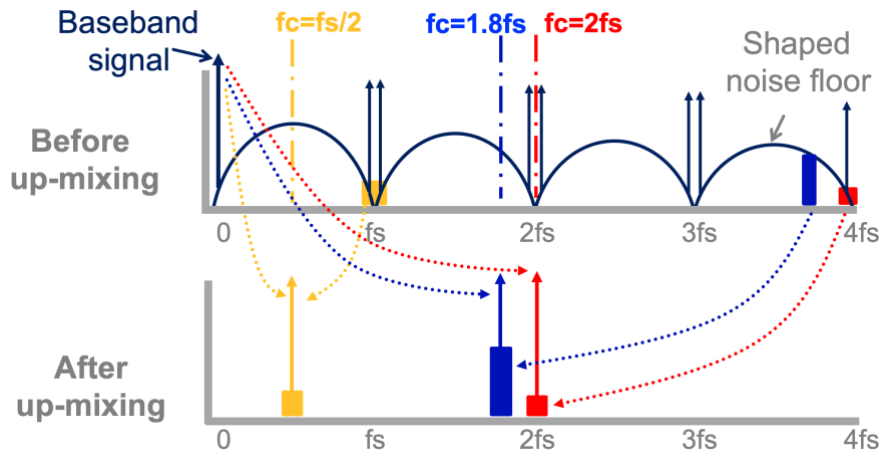
Figure 2.11: Noise folding for different ratios of the modulator sampling frequency, fs and RF carrier, fc. Example with fc=1.8fs shows shaped noise folding back onto the desired signal. We use fc=2fs in this work. The FIR H-bridge up-converts and filtered quantization noise.

Figure 2.12 summarizes the clock rates for a single element of the prototype. The phase shifters run eight times slower than the modulator. An on-chip digital generates the fs/8 clock. The baseband data are re-sampled at fs and processed by the up-sampler before being fed to the delta-sigma modulator. Each transmit stripe has its own PLL, which generates four 6 GHz clock phases from a 750MHz reference. The switch driver logic and the four 6 GHz clock phases control the mixing DAC. The fundamental is up-mixed to RF at 6 GHz.
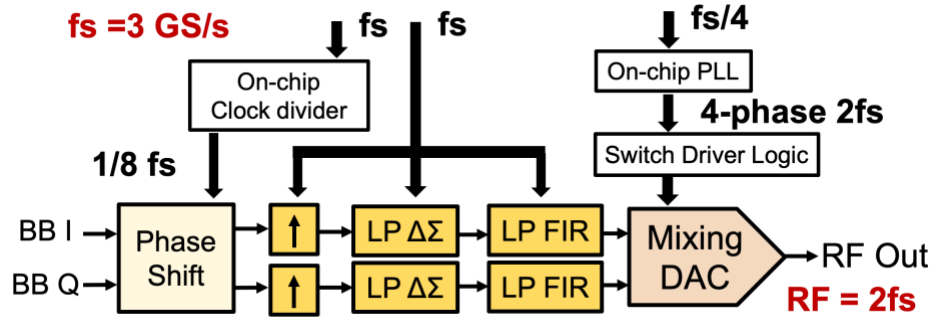
Figure 2.12: Clocking for a single stripe.

2.2.3 Image Attenuation in the Up-sampling Process

The image introduced by up-sampling is a key challenge when processing at different frequencies. We require the frequency plan to be immune to the images.

When the up-sampling process up-samples by n times, it generates (n-1) copies of the fundamental tone. With a zero-order hold up-sampler, the aliases are shaped by a sinc function [22]. Linear interpolation is advantageous over conventional up-sampling using the zero-order hold technique. Linear interpolation can be seen as a convolution of the signal with a triangular pulse, and we can show that the signal is enveloped by a $sinc^2$ function in the frequency domain. Therefore, aliases caused by up-sampling are filtered by the $sinc^2$ transfer function. This significantly improves alias suppression. Figure 2.13 shows the spectra with an 18 MHz input signal applied to the system in the first prototype. The spectra of the output of the interpolator and the output of $\Delta\Sigma$ modulator for a single stripe are shown to illustrate the shaping effect of different types of interpolation and the advantages of linear interpolation in alias suppression. In addition, linear interpolation only leads to a slight in-band attenuation. The total RF bandwidth of our design is 40 MHz, and therefore the 20 MHz I or Q bandwidth is only 1/80 fs, so there is very little attenuation of the desired signal.
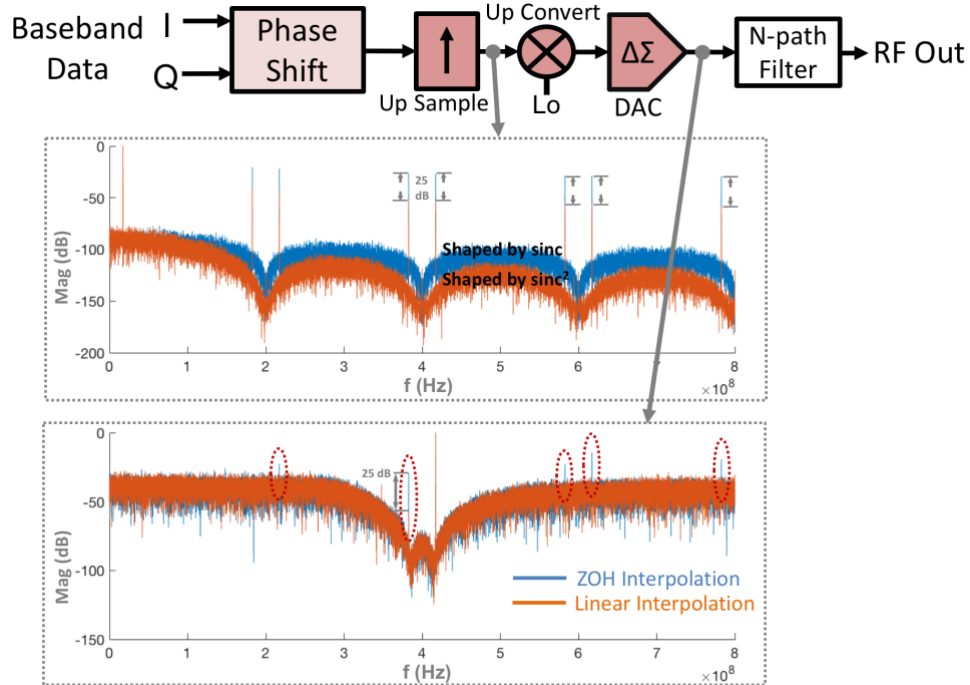
Figure 2.13: The shaping effect and alias suppression of a conventional interpolator (sinc) compared with a linear interpolator (sinc^2).

Applying linear interpolation, we up-sample the 200 MS/s phase-shifted streams by 8 to the fs= 4/3fc frequency. We implement linear interpolation by first calculating the difference between adjacent samples by subtracting the value of the previous sample from the current sample. A single interpolation step is calculated by dividing this difference by 8. This division by 8 is simply implemented by 3-bit binary shifting. The incremental addition of this single interpolation step yields the seven interpolated values.

Similar to linear interpolation, L-fold interpolation is another way to balance between image attenuation and implementation efficiency. In our second prototype, L-fold interpolation up-samples the signal by eight to ensure a sufficient OSR for the sigma-delta modulators. L-fold interpolation is more power-efficient than linear interpolation and has better image-replica suppression compared to zero-hold interpolation. As shown in Figure 2.14, L-fold interpolation

(LFI) has an effective sinc^2 transfer function near DC and an effective sinc transfer function near fs/2. LFI attenuates the critical images that are fs/8 away from RF center frequency by 30 dB.
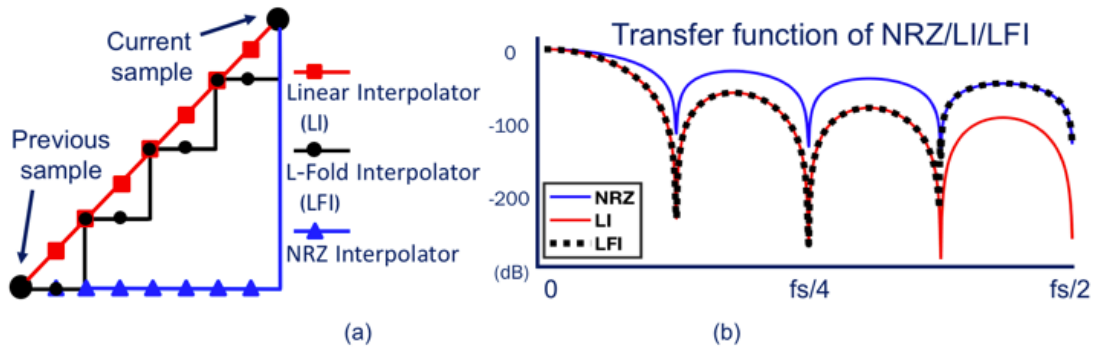
Figure 2.14: (a) L-fold interpolation is used in up-sampling from the 375 MHz phase-shifting frequency to the 3 GS/s rate of the delta-sigma modulators and (b) transfer functions for Linear (LI), L-fold (LFI), and NRZ interpolation.

2.2.4 Energy Efficiency and Synthesizable Logic

Several frequency-planning techniques enhance efficiency. Indeed, energy efficiency is our main target in frequency planning in the prototype. We achieve high efficiency through the management of the block placement and other delicate frequency planning. The block placement strategy is the most straightforward one and is our first-step consideration. The phase shifter performs phase rotation for different transmit channels to determine the overall beam direction. Phase shifting can be very energy-intensive because it requires complex multiplication. For this reason, the phase shifter is placed before the up-sampler and operates at fs/8 to save power. A large OSR is essential in DSM, but this requires a high sampling rate. We place the DSM after an up-sampler to avoid running the phase shifters at the same high speed.

Nevertheless, an essential goal in frequency planning is to ensure that the digital logic throughout the entire DDRF system is synthesizable. In designs based on digital quadrature mixing and digital DSM modulation (both BP and LP), DSM is usually the main bottleneck for digital automation for two reasons. First, the large RF bandwidth and the need for a sufficient OSR for

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noise shaping necessitates a large sampling rate. For an 80 MHz baseband bandwidth and an OSR of 20, the sampling rate should be 3.2GS/s. Second, a complex digital filter in the DSM implementation facilitates an optimized NTF. And DSM itself is usually a feedback system, which is challenging for pipelining. The complexity of filter and the feedback characteristic of DSM both contribute to a long critical path.

Furthermore, quadrature mixing requires the equivalent sampling rate to be four times the RF frequency. In the first prototype, a 1GHz RF requires a 4GS/s sampling rate, but this is not synthesizable in 40 nm CMOS. So we utilize the image frequency and sample three times lower than the original rate. In the second and third prototypes, baseband LP DSM decouples this constraint. Another advantage is that the baseband LP halves the filter order compared with a BP DSM. An LP filter not only simplifies the implementation but also helps shorten the critical path. The lower order filter allows a Verilog-synthesizable 3 GS/s DSM in 28nm CMOS.

It is worth mentioning that technology scaling provides some more flexibility. In our experience, scaling from 40 nm CMOS to 28 nm CMOS allows a 50% faster maximum sampling rate. At the same time, when the sampling rate is pushed to the extreme, some margin is essential to avoid extensive automatic clock tree buffering by the auto place and route tools, especially for long wire routing.

In summary, multiple constraints determine the final sampling rate choice and frequency plan. Our design strategy can be widely applicable to communication systems in general.

Chapter 3 Delta-Sigma Modulator Design in DDRF Systems

In our approach, digital delta-sigma modulation is vital in transforming a high bit-width digital signal into a low-bit one. In this way, the low-bit signal drives a much smaller DAC, and we can get the same in-band Signal-to-Noise (SNR) ratio as with a higher resolution (and larger) conventional DAC. In this chapter, we present the digital DSM design methodology. Several techniques, such as dithering and time-interleaving, are studied to improve the DSM design further. We present the final DSM design for each prototype as well.

3.1 Digital DSM Design Methodology
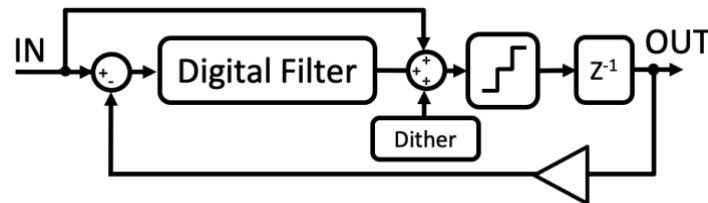
Figure 3.1: Block diagram of a general form of digital $\Delta\Sigma$ modulator.

The general digital $\Delta\Sigma$ modulator is formed as a single loop, with a single feedback path and a feedforward path around a digital filter, as shown in Figure 3.1. The feedback path and the feedforward path decide how the Signal Transfer Function (STF) and Noise Transfer Function (NTF) are related to the digital filter transfer function. If we assume the transfer function of the digital filter is H(z), and the quantization noise added by the quantizer is E(z), we generalize the model in the form in Figure 3.2. The additional feedforward path around the digital filter is designed to ensure that the Signal Transfer Function is 1, as illustrated in Figure 3.2.
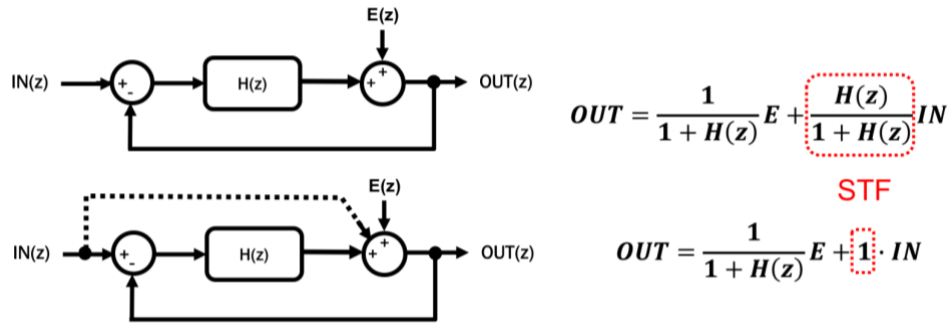
Figure 3.2: Effect of feedforward path on STF.
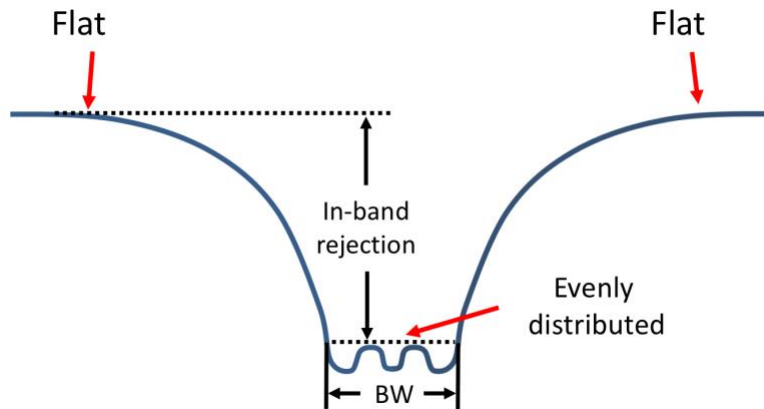
Figure 3.3: General Inverse Chebyshev band-reject NTF.

Since the stability of the modulator is sensitive to the peak out-of-band gain, choosing a filter that is maximally flat out-of-band allows the greatest in-band noise reduction without instability. This, combined with an even distribution of in-band noise, makes the Inverse Chebyshev (aka Chebyshev Type II) the most spectrally efficient choice, as shown in Figure 3.3.

We now describe the design flow for the Inverse Chebyshev digital filter. One can derive the equivalent bandwidth starting with the in-band signal attenuation and the order of the filter. The center frequency (fc) and the sampling frequency are scalable in the DDRF systems. In our first prototype, fc/fs=3/4 is used for the simplest digital up-conversion. In the second and third prototypes, we choose fc =2fs to have a reasonable clock speed for digital automation and avoid noise folding issues during up-mixing.

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We place the poles and zeros of the Inverse Chebyshev NTF based on the above information, as shown in Figure 3.4. The STF without the feedforward path is derived from the NTF using $STF(z) = \left(\frac{1}{NTF} - 1\right) \cdot z$. The matrix values in the Discrete State Space (DSS) are formulated from the STF using the Matlab *ssdata* function. This design process is readily configurable in Matlab and the DSS model of the digital filter can be easily implemented in Verilog, as shown in Figure 3.4.
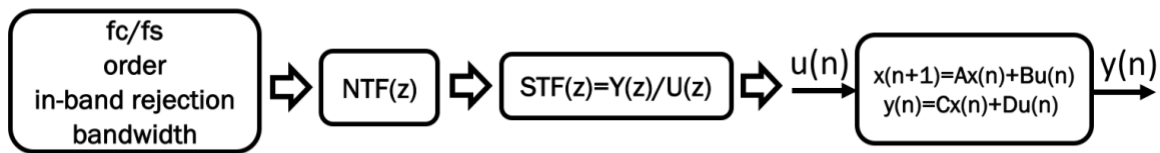
Figure 3.4: Design flow for the digital filter of the digital ΔΣ modulator.

3.2 Dithering

We add dither at the output of the digital filter before the signal is quantized to improve the performance of the bandpass modulator [23]. Generally, in the design of a ΔΣ modulator, the quantizer is modeled as an additive white Gaussian noise that is spread across the entire frequency spectrum. However, this assumption is only true if the quantizer resolution is large. When the resolution of the quantizer is low (in our case, only 1.5 bits), the low quantizer resolution leads to spurious tones at certain frequencies. To eliminate these spurs, we add one LSB wide near-Gaussian dither to the input of the quantizer to enforce the additive white Gaussian noise assumption. Since we have a high effective resolution at the output, the benefit of adding a dither far outweighs the cost of adding random LSB-level noise.

We efficiently generate near-Gaussian random dither on-chip by summing the outputs of four 20b-23b Linear Feedback Shift Registers (LFSRs) as shown in Figure 3.5. Each LFSR

generates uniformly distributed noise. Each LFSR is different in length to ensure that they are not correlated with each other. When four uncorrelated uniformly-distributed noise signals are added, a near-Gaussian noise is derived. The digital near-Gaussian noise is scaled to ensure that the variance of the dither added to the circuit is around $LSB^2/12$, which is equivalent to 1 LSB of quantization noise.
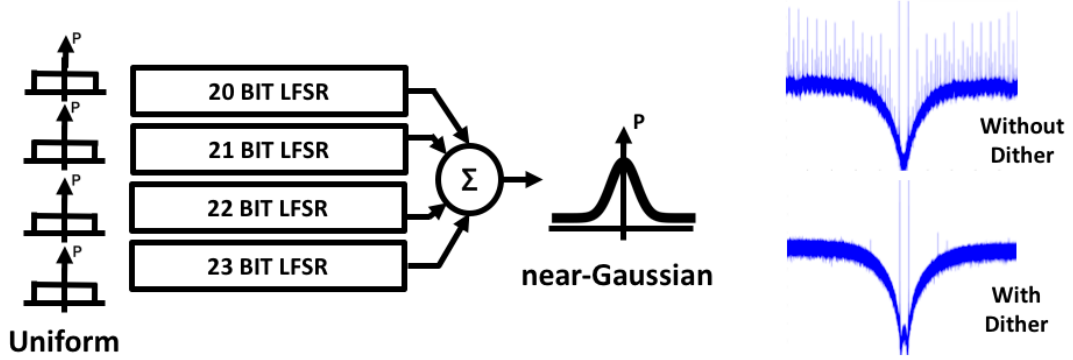
Figure 3.5: Generation of near-Gaussian dither and the improvement in the bandpass modulator spectrum thanks to the introduction of the dither.

3.3 Time-Interleaved (TI) ΔΣ Modulator

DSM is the critical path in the TX chain. We study time-interleaved DSM to pave the way for potential higher sampling rate and ease synthesis requirement. We did not utilize TI technique in the final prototypes and the reason is elaborated in this subsection.

For a general form of s polynomial in z domain (5), it can be expanded in the form in (6). If we group the even and odd terms, respectively, it can be represented in (7).

$$H(z) = \sum_{n=-\infty}^{\infty} h(n)\, z^{-n} \tag{5}$$

$$= \quad \ldots + h(-4)z^4 + h(-3)z^3 + h(-2)z^2 + h(-1)z^1 + h(0)$$

$$+ h(1)z^{-1} + h(2)z^{-2} + h(3)z^{-3} + h(4)z^{-4} + \cdots \tag{6}$$

$$= \quad [\ldots + h(-4)z^4 + h(-2)z^2 + h(0) + h(2)z^{-2} + h(4)z^{-4} + \cdots]$$

$$+ z^{-1}[\ldots + h(-3)z^4 + h(-1)z^2 + h(1) + h(3)z^{-2} + \cdots] \tag{7}$$

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If we use the abbreviations

$$E_0(z) = \sum_{n=-\infty}^{\infty} h(2n) \, z^{-n}, \ E_1(z) = \sum_{n=-\infty}^{\infty} h(2n+1) \, z^{-n} \tag{8}$$

We can re-express $H(z)$ in the form

$$H(z) = E_0(z^2) + z^{-1}E_1(z^2) \tag{9}$$
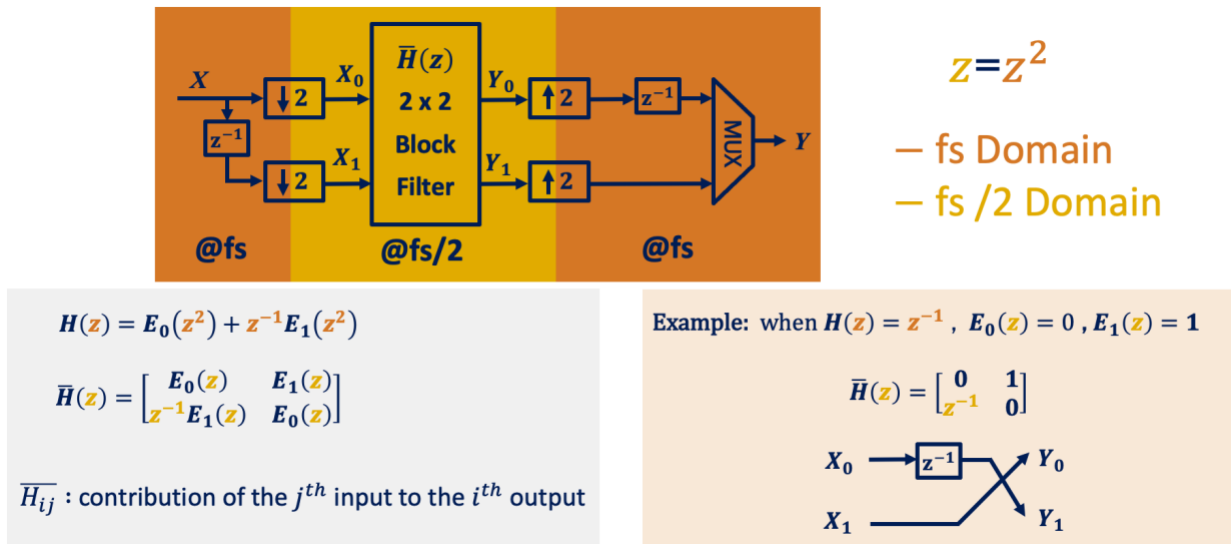
Figure 3.6: Polyphase decomposition: 2-channel interleave.

Here $E_0(z)$ and $E_1(z)$ represents the transfer function in $\overline{H}(z)$, in which $\overline{H_{ij}}$ represents the contribution of X_j to Y_i. We also show an example of a simple system with one delay cell in Figure 3.6. In Figure 3.7, we illustrate a more general case with M-channel interleaving. $\overline{H}(z)$, the block filter can run at M times slower under this strategy.
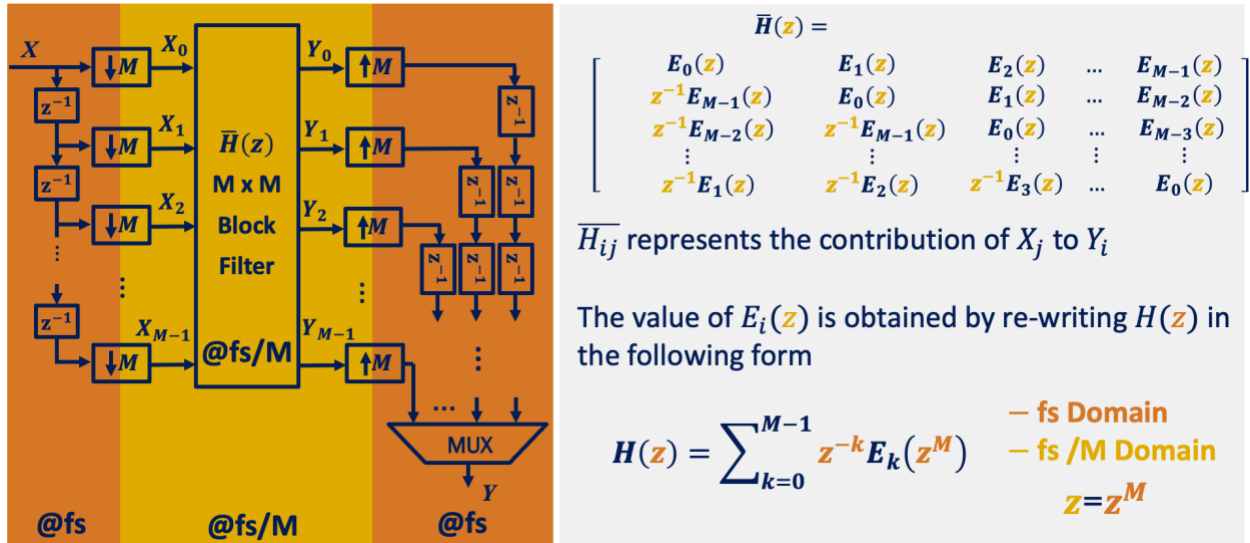
Figure 3.7: Polyphase decomposition: M-channel interleave.
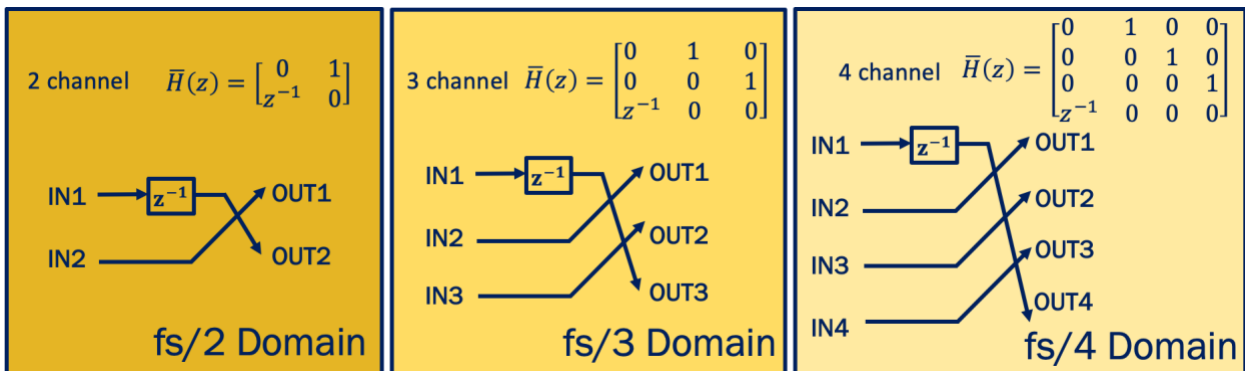
Figure 3.8: Polyphase decomposition of a delay cell with 2,3,4 channel interleaving, respectively.

In Figure 3.8, we show the polyphase decomposition of a delay cell with 2,3,4 channel interleaving respectively, and in Figure 3.9, we apply the 4-channel interleaving strategy to the DSM with a 4-th order IIR digital filter. The resulting topology of the time-interleaved DSM is the version that with four copies of the single-channel and with all the time delays cells replaced by its 4-port version. This resulting topology is shown in Figure 3.10. It is worth mentioning that the critical data path (highlighted in red in Figure 3.10) goes across the channels because of the characteristic of the feedback structure. The total hardware also increases as the channel increases.
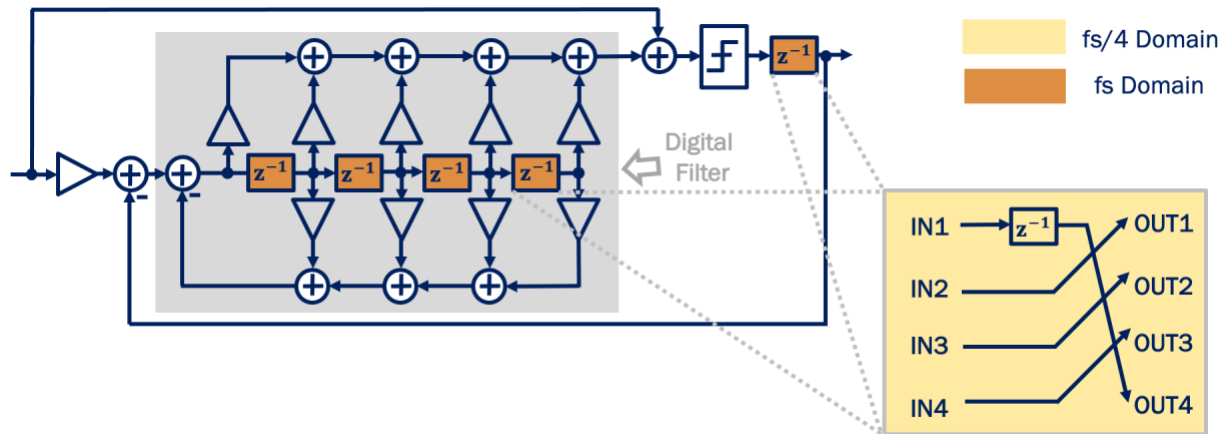
Figure 3.9: Applying time interleaving strategy to DSM.
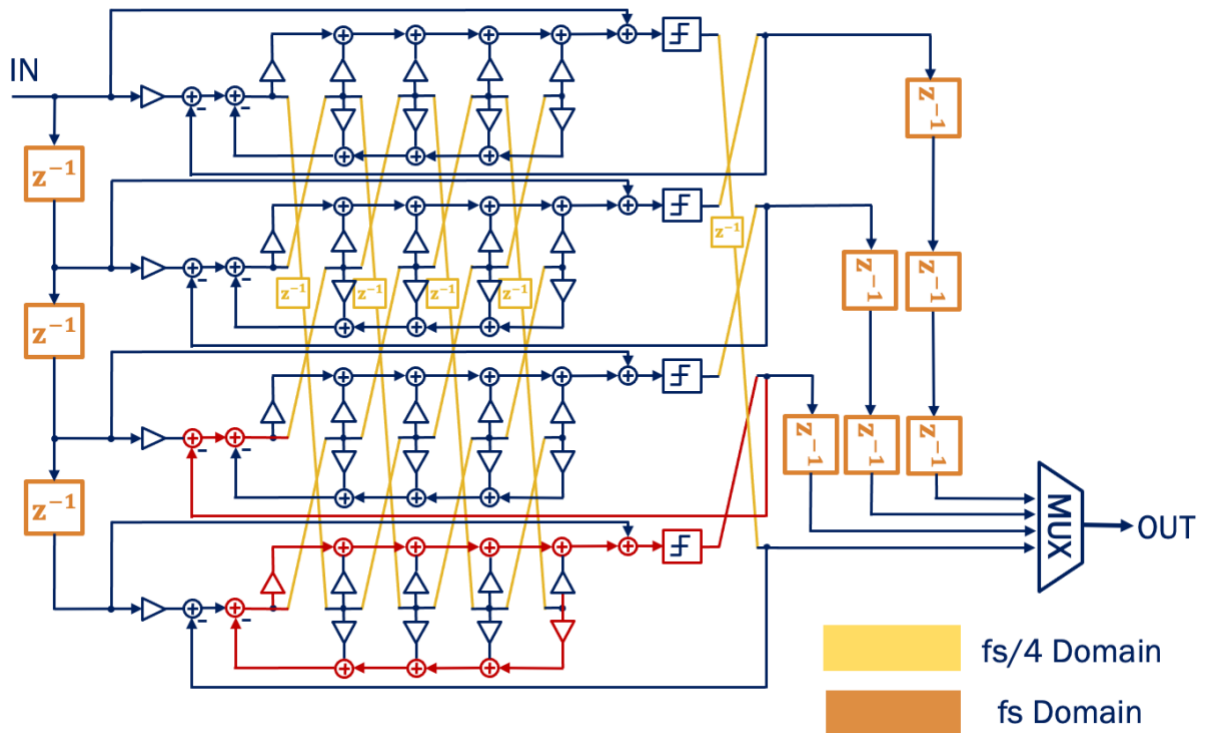
Figure 3.10: A complete 4-channel interleaving DSM with its critical data path highlighted.

In [24], multi-stage noise shaping (MASH) is used in a 1st order error feedback structure.

A look-ahead block is designed to achieve more efficient processing. In [25], bit-level pipelining

combined with time-interleaving, makes the time-interleaving beneficial. The look-ahead block halves the critical path.

To conclude, TI DSM is thoroughly studied, and previous works are investigated. We did not adopt this strategy in our prototypes after analyzing the pros and cons. For a feedback system like DSM, the benefit gained from using TI is limited unless bit-level pipelining is used. Targeting 6 GHz RF and using 3GS/s sampling rate for DSP in 28 nm CMOS, bit-level pipelining is not needed, and single-channel DSM is synthesizable.

3.4 Digital DSM for DDRF System in Our Prototypes

Table 3.1 summarizes the statics of the three prototypes. Each of the prototypes is discussed in three subsections.

	Prototype 1	Prototype 2	Prototype 3
RF frequency	0.8-1.2 GHz	6 GHz	6 GHz
RF Bandwidth	40 MHz	160 MHz	160 MHz
DSM sampling rate	1.6 GS/s	3 GS/s	3 GS/s
DSM filter type (NTF)	4th Order Inverse Chebyshev band-reject filter	2nd Order Inverse Chebyshev high pass filter	TaNS: cascades two 2nd order Type II Chebyshev IIR filters
Technology	40 nm	28 nm	28 nm

Table 3.1: Summary of specifications of the DSMs in the three prototypes.

3.4.1 Bandpass DSM for 1-GHz RF

The bandpass DSM in our first prototype is highlighted in Figure 3.11. Bandpass digital $\Delta\Sigma$ modulation is vital in transforming the 15-bit word-length of up-mixed digital RF signal to the 1.5-bit digital signal needed to drive the 1.5-bit DAC. In this way, we can use a 1.5-bit DAC and get the same in-band Signal-to-Noise (SNR) ratio as with a higher resolution (and larger)

conventional DAC. The digital bandpass modulator provides noise-shaped 3-level copies of the digital signal at 1/4 and 3/4 of the sampling rate, as already shown in Figure 2.4. As discussed in Chapter 2, our choice of sampling frequency greatly simplifies the up-conversion mixer.

The Noise Transfer Function (NTF) is a 4th order Chebyshev band-reject filter. The 4th order digital filter is an integration of four independent feedback loops and four feedforward paths in the canonical form with a single time delay. The center frequency (fc) and the sampling frequency are scalable with fc/fs=3/4 as mentioned for the simplest digital up-conversion. In our case, for a 4th order Chebyshev NTF, an in-band rejection of 47 dB and the sample-to-signal ratio yield a bandwidth of 38 MHz, which meets our specification.
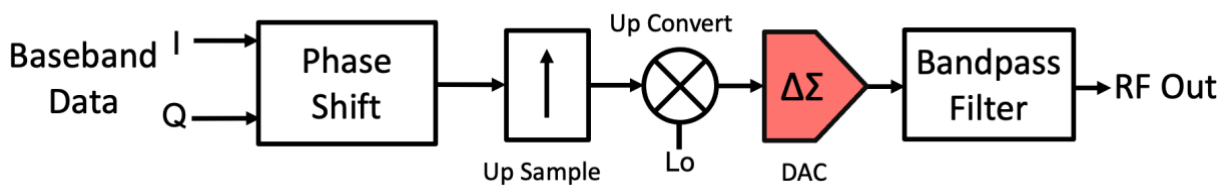
Figure 3.11: DSM highlighted in the single element TX in the first prototype.

3.4.2 Baseband LP-DSM for 6-GHz RF

This subsection discusses the optimal choice of DSM type in the DDRF system for 6 GHz RF. Quadrature mixing is common in DDRF systems because of the simple representation of LO sequence (i.e., 1,0,-1,0…). This LO sequence allows the up-mixer to be implemented with simple mux logic. On the other hand, quadrature mixing requires a bandpass delta-sigma modulator to run at a sampling rate four times the RF frequency, as shown in Figure 3.12. This sampling rate is doable in low-frequency RF systems, but for WiFi-6E targeting a 6 GHz RF, it would require a 24 GHz clock rate. It is not possible to synthesize digital circuity to run at this high clock rate in 28nm CMOS. An alternative is to break the constraint between the sampling rate and center frequency

(i.e., use fs < 4fc). In this prototype, we place the baseband DSM before up-mixing, as shown on the right in Figure 3.12. In our prototype, we use fs = fc/2 where fs still represents the sampling rate of the DSM. It is worth mentioning that there cannot be an arbitrary relationship between fs and fc, and Chapter 2 already elaborates on the choice of fc and fs. We choose a 1-bit DSM output because 1-bit DAC has the crucial advantages of very small size and inherent linearity.
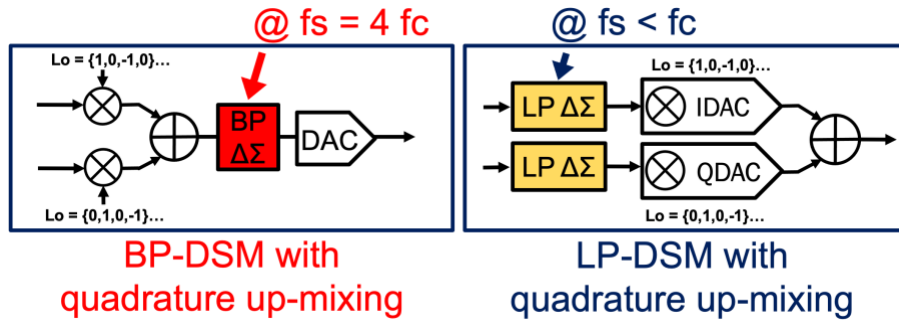
Figure 3.12: Comparison of BP/LP DSM, both with quadrature mixing.

We utilize a high-bandwidth digital delta-sigma modulator and an up-converting 1-b DAC for high efficiency and small area. The digital filter in this prototype is a 2nd-order type II Chebyshev structure. The filter combines two independent feedback loops and two feedforward paths in the canonical form with a single period of delay. A type II Chebyshev type filter ensures a maximally flat out-of-band response, allowing the greatest in-band noise reduction without instability.

Compared to 4th-order bandpass modulation in the first prototype, the lower order of an equivalent pair of 2nd-order lowpass modulators removes a significant digital-speed bottleneck. The shaping effect at the RF band remains the same as with the 4th-order bandpass counterpart. As discussed in Section III, the RF center frequency is chosen as fc=2fs, so that fs is 3 GS/s for a 6 GHz RF frequency. The OSR of the digital DSM is 18. With a 3 GS/s sampling rate, this provides

an effective baseband bandwidth of 80 MHz, and a calculated in-band quantization noise density is -119 dBc/Hz.

3.4.3 Targeted Noise Shaping (TaNS)

As mentioned in Chapter 1.4.3, noise-shaping is essential for DDRF because it enables high in-band SNR with a small, low-resolution DAC. Noise-shaping facilitates excellent in-band modulation accuracy (i.e., EVM) by relocating quantization noise from in-band to out-of-band (OOB) but requires filtering of adjacent-channel and OOB emissions to meet spectral mask requirements. This section presents the design procedure of a filter-free, noise-shaping DDRF architecture that targets noise-shaping (TaNS) to meet spectral mask requirements and avoids the complexity and power/area cost of a bandpass filter.
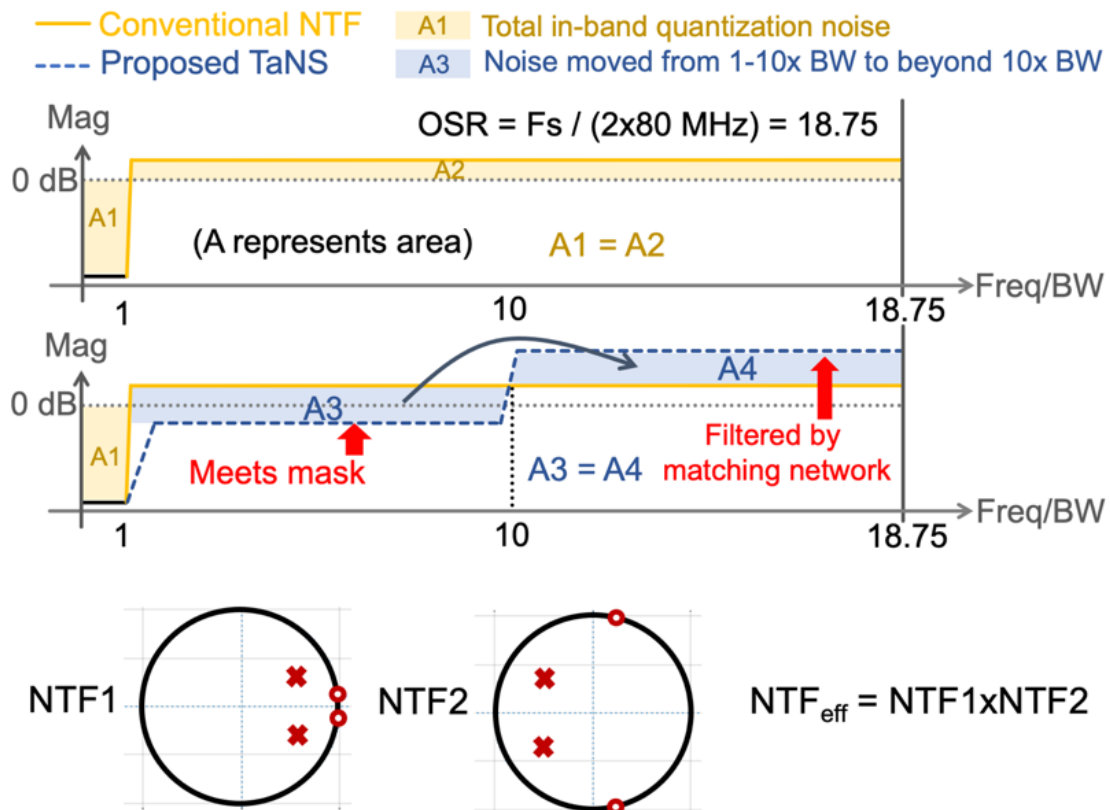
Figure 3.13: (top) Conventional noise shaping, (middle) TaNS meets the spectral mask, (bottom) TaNS NTF pole and zero placement.

Fundamentally, the Bode Sensitivity Integral and Lee's Rule govern the noise-shaping budget. Bode's Sensitivity Integral determines the modulator's noise-shaping budget by requiring that the integral of the noise-transfer function (NTF) magnitude in dB be zero. Lee's Rule sets the maximum allowable NTF magnitude at any frequency (i.e., $\|H\|\infty$). Conventional noise-shaping distributes quantization noise uniformly out-of-band (Figure 3.13, top). For our filter-free DDRF, we engineer the near-in region to directly meet the spectral mask by moving quantization noise far out-of-band, as highlighted in Figure 3.13 (middle). As a result, $\|H\|\infty$ increases so that the noise-shaping budget and stability constraints ultimately limit TaNS.

Technology and architecture limit the maximum sampling rate and the noise-shaping order. We optimize power and performance with a 3GS/s 4th order IIR NTF delta-sigma modulator (DSM) architecture – Furthermore, our design is synthesizable from Verilog in 28nm CMOS. The high 3GS/s sampling rate not only ensures a high OSR but also sets a large OOB region width (i.e., Fs/2 – BW=1420MHz). This OOB region is 17.75x the in-band BW, ensuring a low $\|H\|\infty$ and good stability. The 4th order NTF cascades two 2nd order Type II Chebyshev IIR filters for flexible placement of NTF zeros and a practical Verilog implementation. An important advantage of the Type II Chebyshev response is that its flat out-of-band keeps $\|H\|\infty$ low. For the most effective noise-shaping, we optimize: (i) transitions between regions; (ii) NTF zero locations; and (iii) quantizer (i.e. DAC) resolution.

The transitions between NTF regions should be as sharp as possible to optimize the noise-shaping budget. A rapid transition slope enables better allocation of the quantization-noise budget. As shown in Figure 3.13, we place the NTF poles close to the unit circle for faster transition slopes. We put the second pair of zeros at 635MHz, setting the width of the low-noise OOB region.

Together with zeros at 57MHz, these zeros form a low-NTF region between 1x BW and 10x BW. We want the low-noise OOB region to be as wide as possible, leaving only the far-away OOB noise to be suppressed by the output matching network/antenna. However, considering Bode's Sensitivity Integral, too wide a low-noise OOB region would cause too large $\|H\|\infty$. A low-noise OOB region of 10x BW is a very effective compromise.

As discussed previously, Lee's rule dictates that $\|H\|\infty$ should not exceed a certain value to ensure stability. Increasing the quantizer resolution not only reduces the total quantization noise but also permits a higher $\|H\|\infty$ for stability. After optimizing the transition slope and the zero locations, we use a digital quantizer resolution of 5-bits to ensure a stable modulator.

Our digital DSM uses a classic single-loop architecture (Fig. 3). A cascade of two IIR NTFs achieves comparable performance to a much higher order FIR NTF. The total $NTF_{eff} = NTF1xNTF2$. The 4th order filter is directly implemented by calculating the response from the NTF, $G = (1/NTFeff -1) \times z$ (see Figure 3.14). It is important to use as low order as possible to ensure the feasibility of the digital implementation. This modulator delivers 11-bit SQNR in an 80MHz baseband bandwidth (i.e., 160MHz RF bandwidth), corresponding to an ideal EVM below 0.1% for QAM 64.

$$G = (1/(NTF1 \times NTF2) -1) \times z$$
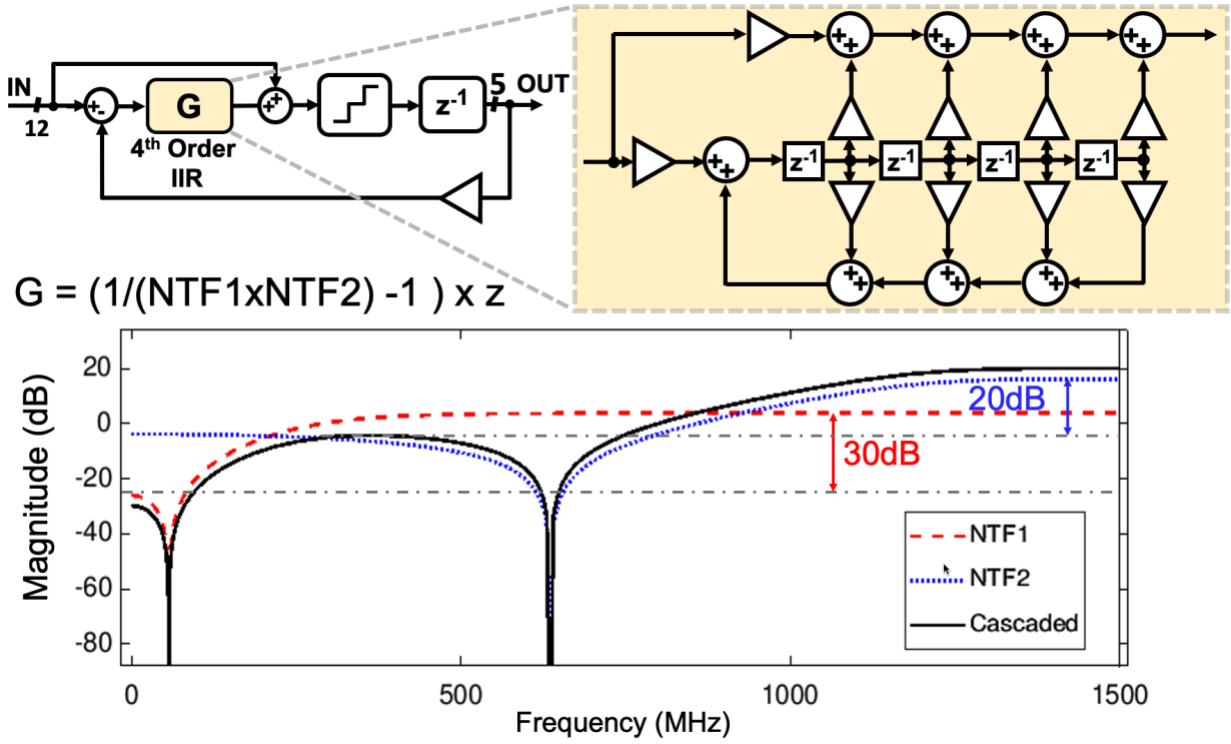
Figure 3.14: DSM block diagram and the cascaded NTF.

Chapter 4 DAC and RF Filter Design

A digital DSM produces a low-bit output and drives a small DAC. This helps with DAC linearity. However, we need a filter to suppress the shaped the out-of-band quantization noise generated by DSM. In the following sections, we present DAC and filter structure of the three prototypes. In prototype 1, an N-path filter is tailored with the bandpass DSM and a 1.5-bit DAC is used for linearity. In prototype 2, the I/Q FIR filters are paired with baseband I/Q DSMs. This avoids analog filtering at a high frequency at 6 GHz. In the third prototype, a filter-free DSM NTF is designed to enable targeted noise function.

4.1 1.5-bit DAC and N-path filter for 1.2 GHz RF
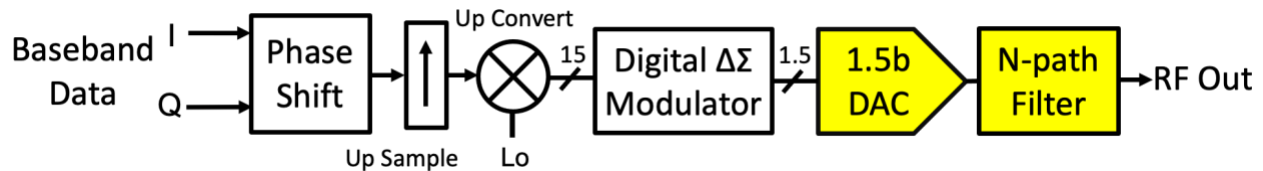
Figure 4.1: Single stripe in prototype 1 with DAC and N-path filter highlighted.

As shown in Figure 4.1, the up-mixed, noise-shaped 1.6 GS/s 1.5-bit digital signal directly drives the 1.5-bit DAC to form the 1.2 GHz RF signal. An N-path filter in each transmit stripe suppresses the shaped quantization noise caused by the digital $\Delta\Sigma$ modulator, as illustrated in Figure 4.2. The N-path filter also suppresses the 400 MHz fundamental tone more than 30 dB with an ideal duty cycle and zero switch resistance. The combination of a 1.5-bit $\Delta\Sigma$ DAC and N-path filtering leads to a small and efficient DAC because of the small size of the 1.5-bit current steering DAC compared with a high-resolution DAC. Compared to a single-bit DAC, a 3-level DAC

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generates less quantization noise, and thanks to its single current source, it still avoids the problem of unit mismatch seen in higher resolution DACs. The digital bandpass modulator and 1.5-bit DAC also ensure flexible center frequency and direct modulation to RF without the need for analog up-conversion.
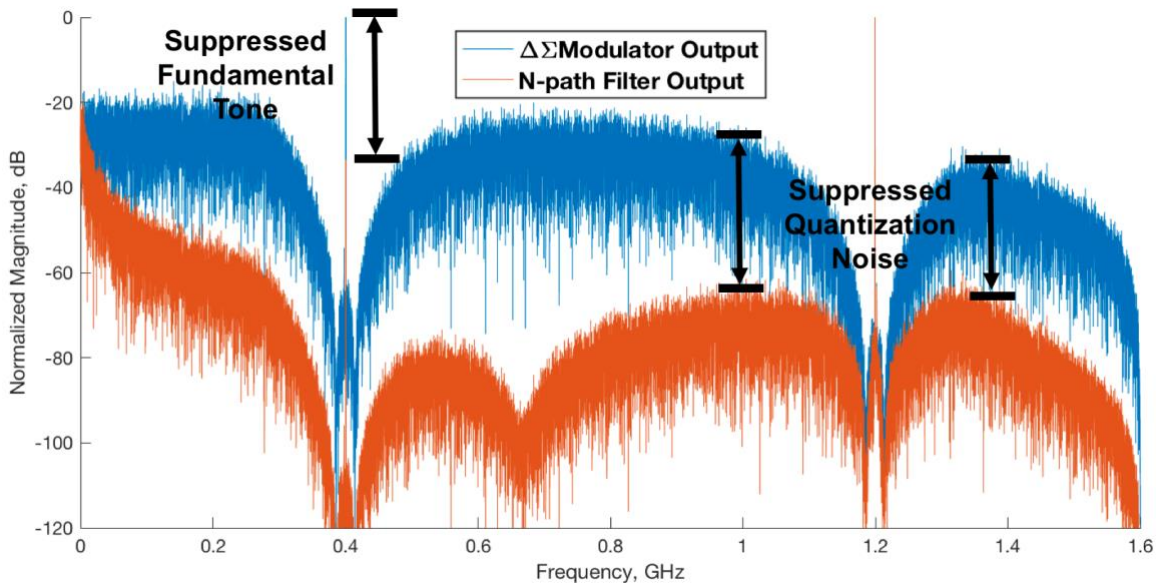
Figure 4.2: Spectra of the output of $\Delta\Sigma$ modulator and the output of the N-path filter.

An N-path filter also contributes to the compactness and efficiency of analog circuitry since an N-path filter does not need inductors as in some RF bandpass filters. An N-path filter requires only switches, resistors, and a capacitor array. An N-path filter is a compact, highly configurable, high-Q bandpass filter that tracks the center frequency of the modulator and effectively suppresses the shaped quantization noise.

Figure 4.3 shows the N-path filter and DAC in detail. The DAC is directly driven by the 3-level 1.6 GS/s digital signal from the bandpass $\Delta\Sigma$ modulator. The switch driver is implemented as cascaded buffers with increasing sizes. The 3-level signal is represented with 2 bits as 01,00, and 10 for the high, middle, low level, respectively. The 3-level DAC has a single current source and three switches connecting to the two differential load resistors and the dummy load. The

dummy branch ensures that there is always a current path from the source. Filter capacitors are connected sequentially to the load resistors to provide a filter passband centered on the 1.2 GHz RF carrier, which is a quarter of the N-path filter clock rate. There are two copies of the filter capacitor array since it is fully differential.
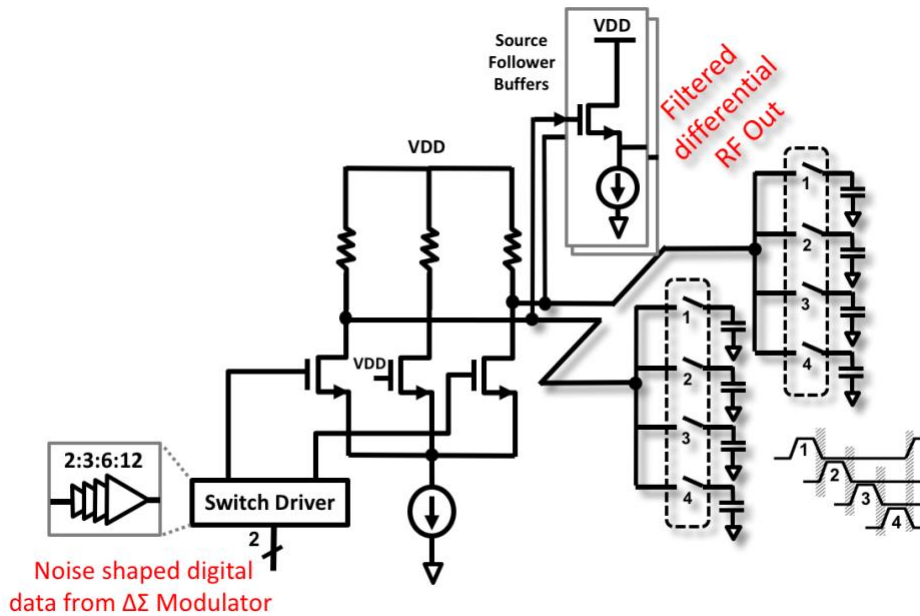
Figure 4.3: Circuit implementation of the 1.5-bit DAC and N-path filter.

The load resistors are shared by the DAC and N-path filter. The load resistance is 1 kΩ, and the filter capacitors are 2 pF MOM caps, both integrated on-chip. Theoretically, this RC value sets the bandwidth $f_{rc}=1/(\pi nRC) = 39.8\ MHz$. Using the more accurate 4-path filter model [26], including other non-idealities, such as the reduction in duty cycle and switch resistance, a periodical AC analysis simulation predicts a 3 dB filter bandwidth of approximately 40 MHz, which matches the bandwidth of digital ΔΣ modulator.
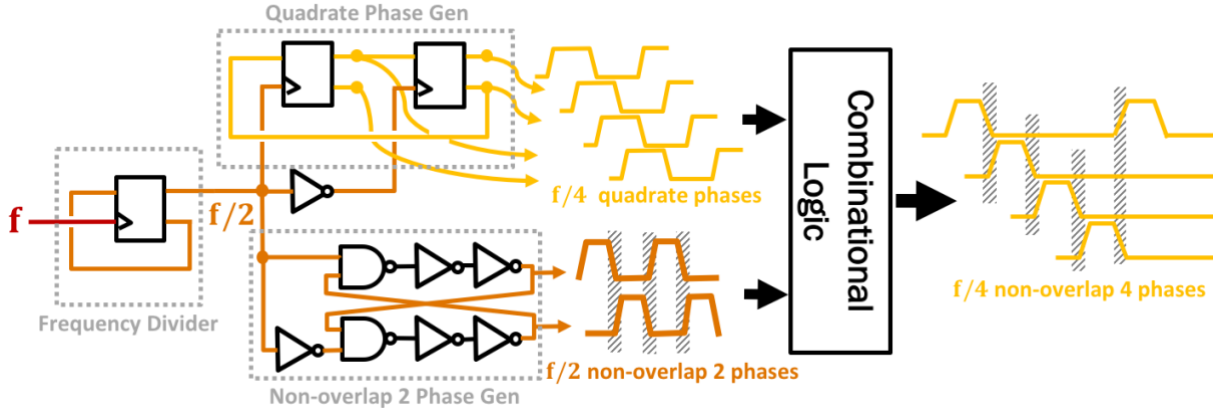
Figure 4.4: Implementation of a 4-phase non-overlap clock generator.

The four-phase 1.2 GHz non-overlapping clocks for the N-path filter are derived from a 4.8 GHz clock using a frequency divider and simple combinational logic, as shown in Figure 4.4. The 4.8 GHz clock is 3 times the modulator sampling rate, and clock is shared across the transmit array since the clock of the N-path filter inherently tracks the modulator sampling frequency. This tracking of the RF center frequency provides better filtering performance and significantly improves the beam accuracy compared with fixed-center-frequency passive filters.

A current-steering DAC does not have a rail-to-rail output swing. However, for a 3-level signal, current steering is still advantageous because it makes use of a third dummy branch and avoids the mismatch inherent in a DAC with multiple cells. As shown in Figure 4.5, the conventional non-return-to-zero type of DAC has a shaping effect on the original signal. By holding the digital sampled value during the whole sampling period, the signal is convolved with a single square pulse of width *1/f$_s$*. In the frequency domain, the signal is shaped by $sinc(\pi f / f_s)$, as is also shown in Fig. 20. At the image center frequency of 3/4 *f$_s$*, the signal is attenuated by 12 dB. This power loss is a drawback of using the image, but it facilitates our mostly-digital approach. As an alternative, the use of a mixing DAC [27] ensures less signal loss by moving the maximum power region to the second Nyquist zone.
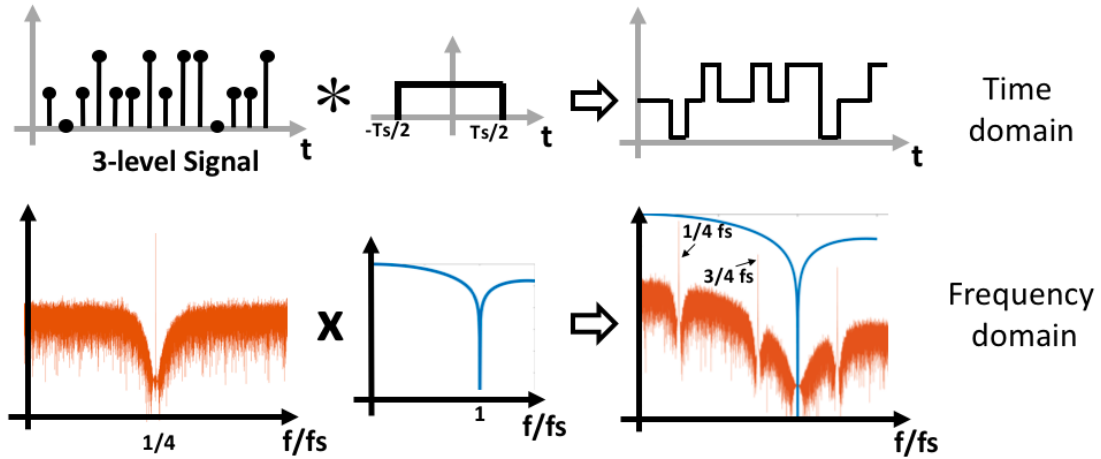
Figure 4.5: The shaping effects of DAC in the frequency domain.

For an N-path filter, the finite number of paths (in our case, four) and reduction in duty cycle all contribute to a loss [28-30]. With four paths, the theoretical loss is about 2 dB. Switch resistance reduces the maximum attenuation of the sideband, limiting suppression of the fundamental tone. We use low-V_T devices to keep the switch on-resistance low. A source-follower at the output of each stripe, also shown in Figure 4.3, ensures 50 Ω output matching.

4.2 Digital lowpass filters and H-bridge DAC

In the 2nd prototype, a digital FIR bandpass filter suppresses the shaped the out-of-band quantization noise generated by DSM. Designing a bandpass filter at 6 GHz is hugely challenging. Sharp, active filters are problematic at 6 GHz. Passive LC filters are too large. N-path filtering is impractical at high speed and suffers from significant insertion loss. In our scheme, we avoid the filter challenge at 6 GHz with equivalent filtering at baseband.

We design the digital I/Q lowpass FIR filter based on a 3 GS/s digital delay chain, as shown in Figure 4.6. The 15-tap FIR filter, which sums the 16 outputs of the 3 GS/s delay chain, facilitates adequate attenuation and, at the same time, keeps the design small and synthesizable. As shown in Figure 4.6, the 16 outputs of the delay chain combine in the current domain in the current steering DAC. Each 1-bit output controls the on/off state of a single current source. The number of taps

and the tap delay are chosen for an effective RF bandwidth of 160 MHz. The baseband counterpart of the filter matches the 80 MHz baseband bandwidth and the delta-sigma modulator noise transfer function. The estimated filtering of out-of-band quantization noise at a 750 MHz offset and beyond is -113 dBc/Hz.
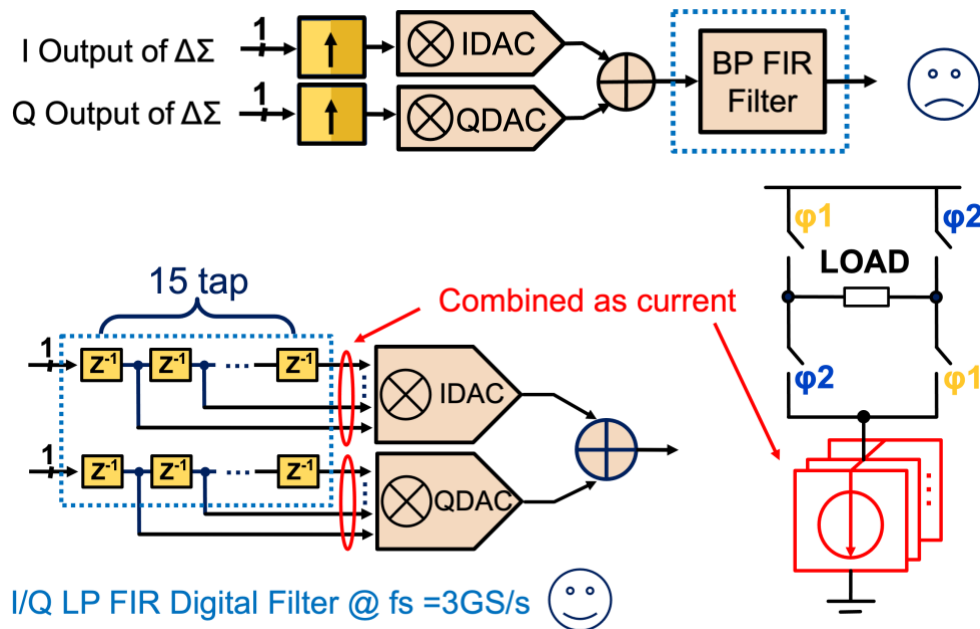
Figure 4.6: FIR filter implementation.

We combine current steering DACs, FIR filtering, and RF up-conversion in a new H-bridge structure for efficiency and compact size. Figure 4.7 shows the complete architecture. The 16 outputs of the delay chain driven by the DSM sum to control the DAC current source amplitude. Compared to a conventional current steering DAC, the H-bridge DAC has the advantage of doubling the effective swing by changing the bridge-current direction. As shown in Figure 4.7, separate H-bridge structures handle the I and Q components. A switch driver, fed with four 6 GHz clock phases and input sign, controls H-bridge switching, effectively up-mixing the DAC output with a 24 GS/s 0,1,0,-1,… sequence. Orthogonal mixing sequences control the I and Q H-bridges. The up-mixed current signals sum together at the H-bridge outputs.
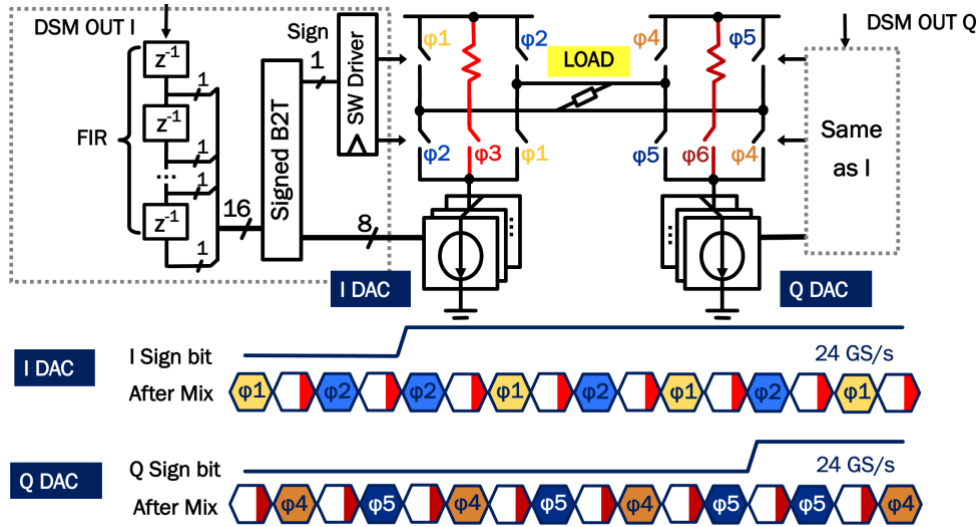
Figure 4.7: FIR H-bridge I/Q current steering DAC with B2T decoder to improve power efficiency. An example of the timing diagram showing the activation of the bridge current switches and the dump current.

The sum of the {1, -1} outputs of the FIR-filter delay chain controls the direction and value of the H-bridge DAC current. Many of the 16 delay tap outputs are opposite in value; therefore, a direct implementation with opposing current directions on the bridge would result in extremely low efficiency. We introduce a binary to thermometer (B2T) coding scheme to reduce DAC current consumption by around 50%, as shown in Figure 4.7.

An essential part of our approach is a binary-to-thermometer (B2T) decoder that produces a sign and an 8-bit thermometer code. The B2T decoder sums the delay-chain outputs and converts the sum to a thermometer code plus sign. The sign bit (combined with the up-conversion sequence) sets the overall bridge-current direction, while the 8-bit thermometer code decides how many current sources turn on. Since all switch drivers and switches are shared, the only components with multiple copies are the current sources. This significantly helps maintain the linearity advantages of a single-bit DAC, especially by avoiding data and clock alignment mismatch between current switches and switch drivers, which is mainly caused by layout wiring. Furthermore, the mismatch

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between the current sources only affects the filter tap weights and does not introduce DAC non-linearity.
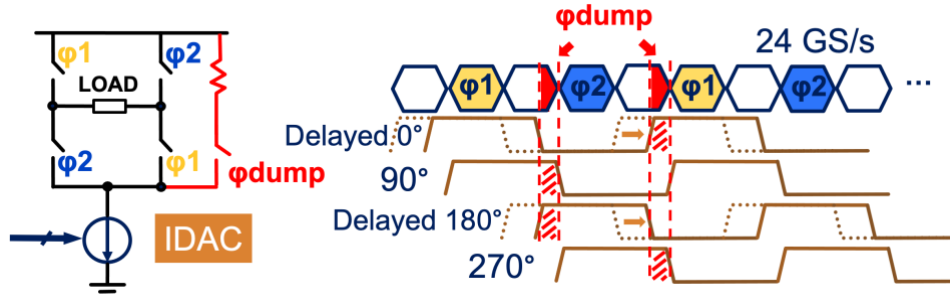
Figure 4.8: Circuit diagram and timing diagram for the dump current branch.

We use a timed dump branch to ensure fast current-settling and reduce the effective DAC current dissipation by about one third. Figure 4.8 shows the timing for the dump procedure and highlights the dump branch. As mentioned, separate I and Q H-bridges generate and combine I and Q currents. In principle, the current sources for each H-bridge (i.e., I or Q) are only required for half of the time, and therefore we can disable these currents sources when not needed to save power. However, to prevent non-linearity due to current settling, we enable current flow to a dump branch before the I/Q switch turns on (shown in the timing sequence and highlighted in red in Figure 4.8). The dump path is enabled for 1/6 of the period. Compared to keeping the dump path always on, this timing scheme reduces DAC current dissipation by one third.

4.3 Moving towards filter-free: TaNS

In chapter 3, we present the design procedure of a filter-free, noise-shaping DDRF architecture that targets noise-shaping (TaNS) to meet spectral mask requirements and avoids the complexity and power/area cost of a bandpass filter. In this section, we simply show the filter-free TX architecture. The H-bridge DAC is similar to the one used in the second prototype.

Figure 4.9 shows a block diagram of the TaNS DDRF and the mixing H-bridge DAC implementation. An H-bridge DAC delivers double the output swing compared with a

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conventional current-steering DAC. The 12-bit I and Q baseband signals are pre-processed off-chip with digital pre-distortion (DPD). The input data is up-sampled by an FIR interpolator and modulated by the TaNS DSM to form I & Q 5-bit noise-shaped signals. A thermometer encoder encodes the 5-bit signal into a 1-bit sign + 16-bit thermometer code. The sign bit, together with a 4-phase 6GHz clock, controls the direction of the H-bridge. The 16-bit thermometer code sets the current source magnitude. An on-chip clock divider generates a four-phase 6GHz clock from an external 12GHz clock.
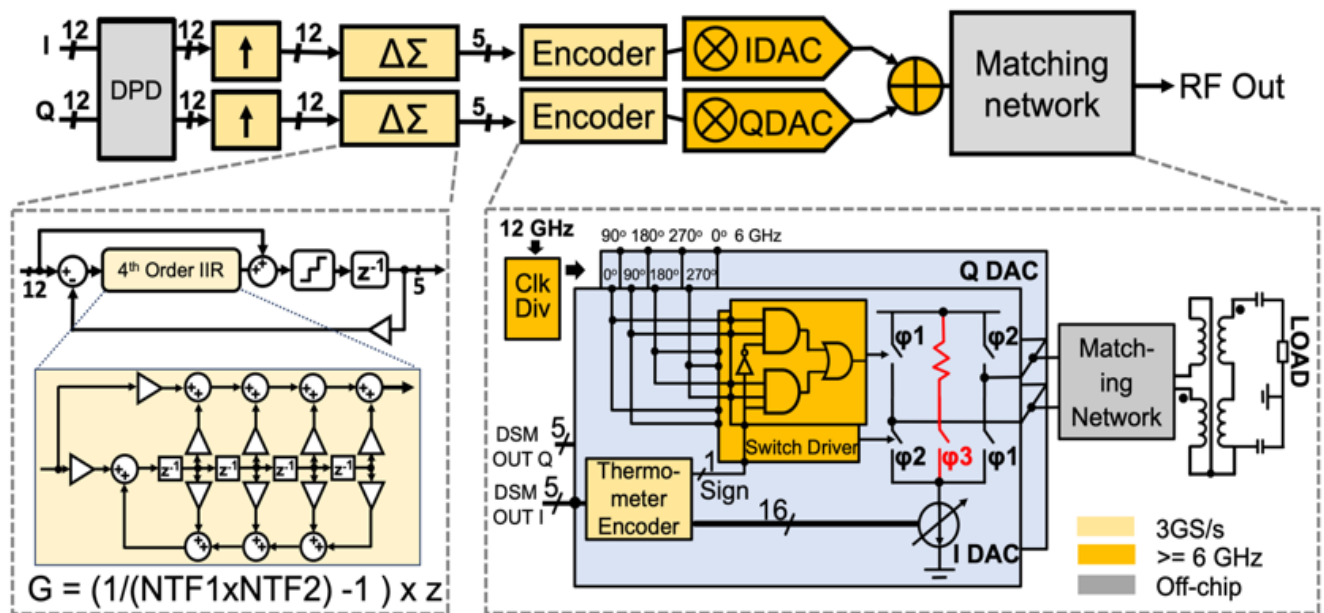
Figure 4.9: (top) System block diagram, (bottom left) $\Delta\Sigma$ block diagram, and (bottom right) mixing DAC implementation.

Chapter 5 Prototypes and Measurements

Three prototype ICs were implemented and tested. Prototype 1 achieves an order of magnitude improvement in the area and power consumption per element by digital phase-shifting combined with bandpass $\Delta\Sigma$ modulation and N-path filtering. Key to the efficiency are the pairing of area-efficient bandpass $\Delta\Sigma$ modulation with N-path filtering to suppress quantization noise and careful frequency management to allow efficient digital phase-shifting and up-conversion. Prototype 2 extends the bandwidth and frequency range of digital phase-shifting direct digital to RF TX, paving the way for use in MU-MIMO wireless networking applications. A sigma-delta modulation chain enables an inherently linear 1b RF DAC. Low-loss FIR filtering suppresses sigma-delta DAC noise. An H-bridge combines current-DAC, FIR-filtering, and RF up-conversion for efficiency. Prototype 3 introduces targeted noise shaping (TaNS) for filter-less fully synthesizable DDRF meeting the WiFi-6E requirements.

5.1 Prototype 1

Prototype 1 is implemented in 40-nm CMOS, and a die photo is shown in Figure 5.1. The active area is 0.19 mm^2, and the digital core size is 0.12 mm^2. The overall power consumption is 128 mW for a 1.2 GHz output, corresponding to 16 mW per channel. The test setup is shown in Figure 5.2.
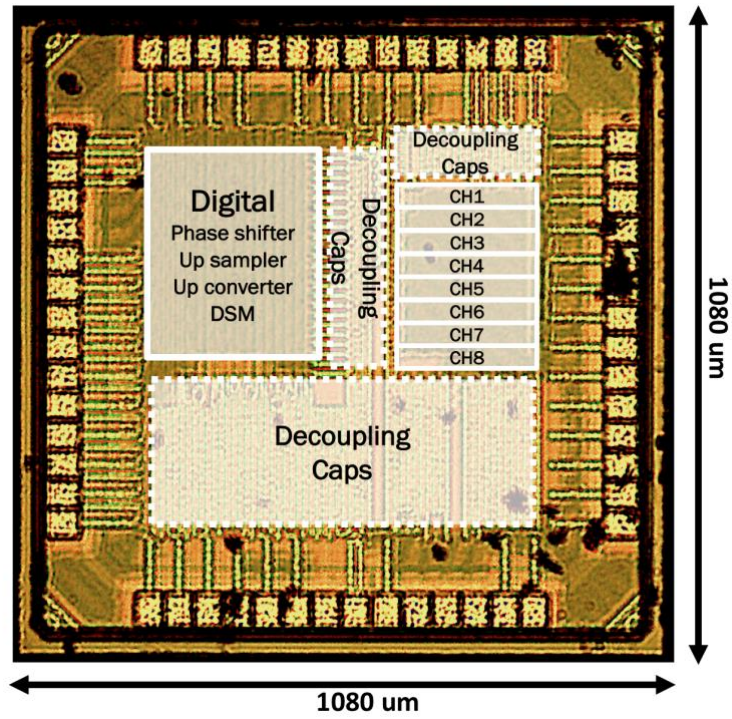
Figure 5.1: Die micrograph of prototype 1.
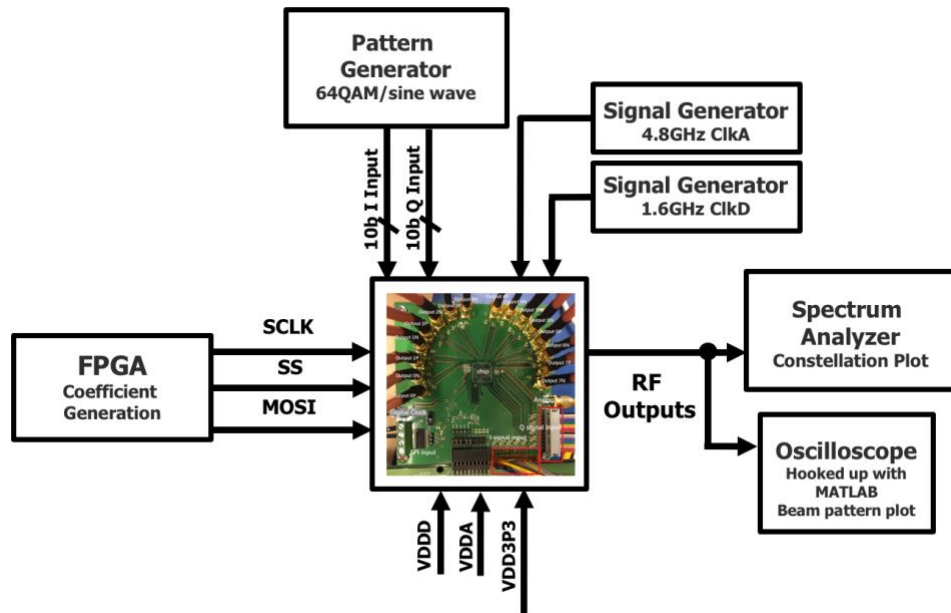
Figure 5.2: Test setup of prototype 1.

Figure 5.3 compares the simulated and measured output spectra. The simulated result is

based on an ideal N-path filter with ideal duty-cycle switching and ideal zero-resistance switches.

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Also, this simulation does not consider the power loss caused by the output matching circuit. From the measured spectrum, we can notice the shaped noise around the fundamental tone, while for the image tone, where we apply the N-path filter, we see that the quantization noise is suppressed. However, it is noteworthy that the noise-shaping around the fundamental is not significant since it is attenuated by the N-path filter. Since the power of the fundamental tone is originally 12 dB higher than the image tone, the suppressed fundamental tone is still significant.[4]
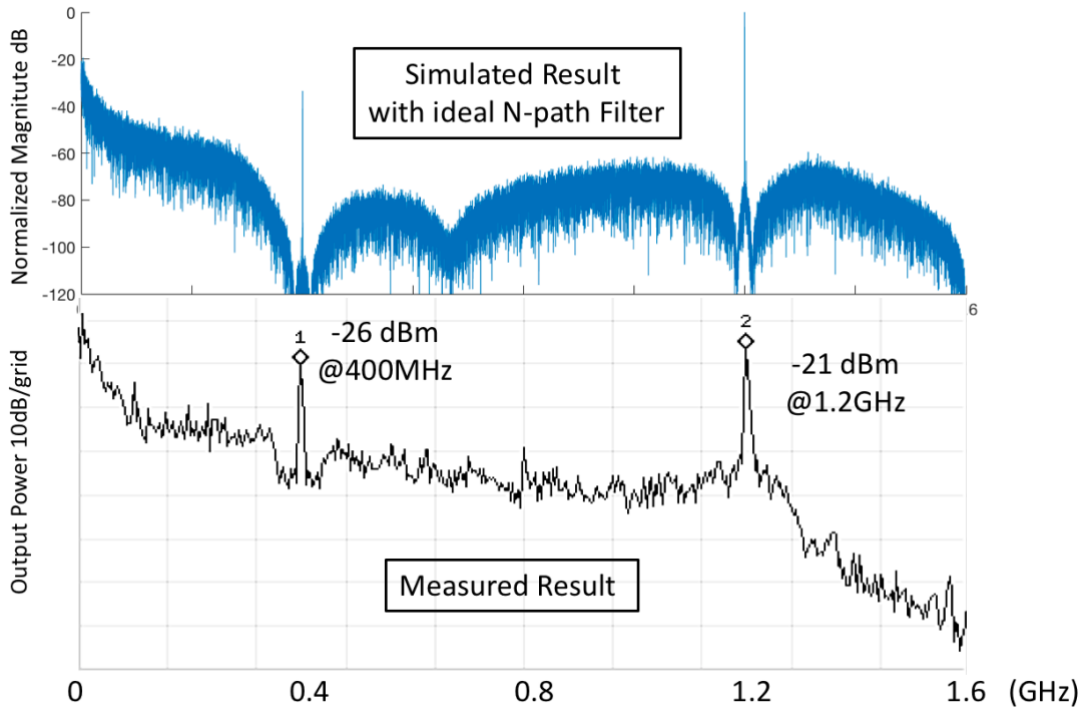
Figure 5.3: Comparison of simulated and measured output spectra.

Figure 5.4 shows a zoomed-in spectrum around the 1.2 GHz carrier frequency. The main tone is at 1.2055 GHz. The LO feedthrough, image, IM3, and IM5 are marked in the figure. The measured IM3 is 32 dBc, which corresponds to an in-band SFDR of 32 dB. The measured image rejection is 36 dBc. The estimated SNR is 24 dB[5].

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[4] The internal digital noise-shaped signals are not available for measurement since the digital signals are not driven off-chip.

[5] For 64 QAM, this is equivalent to a theoretical EVM of 4.1%.
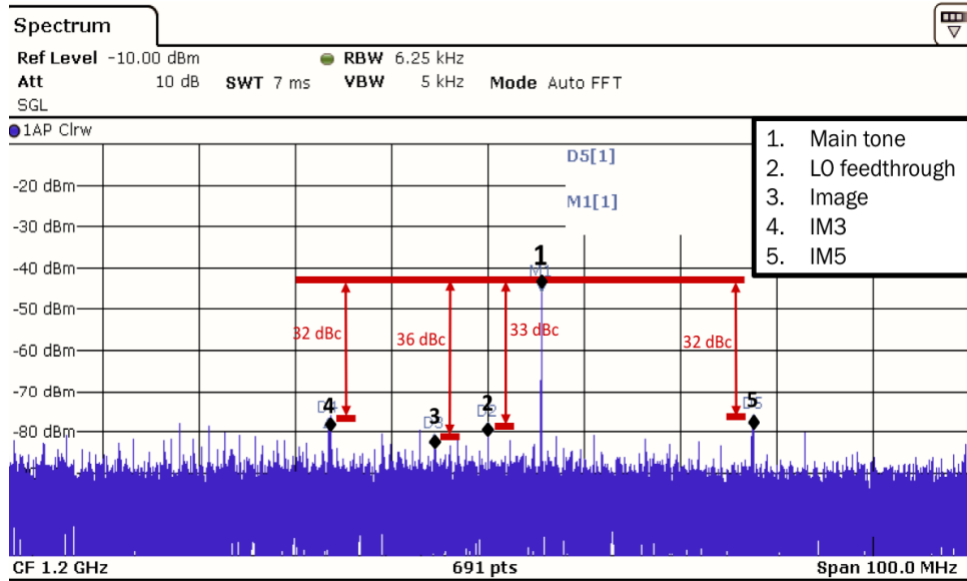
Figure 5.4: Zoomed-in measured output spectrum.

Figure 5.5 shows the measured constellation when a 64 QAM modulated digital baseband signal is applied to the prototype. The constellation plot is generated from the output of a single channel. EVM is further improved when combining the outputs of the 8 channels because uncorrelated noise from different channels is averaged out. The digital transmit data is filtered with a Gaussian filter with a roll-off factor of 0.22. With a 64-QAM signal at 1.205 GHz, an EVM of -23.6 dB is measured for a symbol-rate of 320 kSymbols/s. For the same conditions, the measured EVM is -29.0 dB for a 405 MHz carrier.

The measured beam patterns for 0, 30, and 45 degrees and for two separate beams are shown in Figure 5.6. These measurements assume eight in-line dipolar antennas, spaced at half wavelengths. The measurement step size is 2.5 degrees. These measurements show good beam patterns. The side lobes are around -15 to -12 dB with various steering angles (the ideal is -12 dB). The beam direction is accurate within 2 degrees, as is indicated in Figure 5.6, where the ideal beam direction is marked in red.

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Ref Level -28.00 dBm | Mod 64QAM | SR 320.0 kHz | (a) @400MHz Carrier
Att 0 dB | Freq 405.46875 MHz | Res Len 800
SGL Stat Count 1

A Const I/Q(Meas&Ref) ● 1M Clrw

B Result Summary (see more in full screen)

		Mean	Peak	Unit
EVM	RMS	3.52	3.52	%
	Peak	15.24	15.24	%
Phase Error	RMS	1.58	1.58	deg
	Peak	7.99	7.99	deg
Carrier Freq Error		-44.59	-44.59	Hz
Rho		0.998 764	0.998 764	
I/Q Offset		-54.74	-54.74	dB
Gain Imbalance		0.08	0.08	dB
Quadrature Error		0.04	0.04	deg
Amplitude Droop		-0.000 03	-0.000 03	dB/sym

Ref Level -10.00 dBm | Mod 64QAM | SR 320.0 kHz | (b) @1.2GHz Carrier
Att 10 dB | Freq 1.20546875 GHz | Res Len 800
SGL Stat Count 1

A Const I/Q(Meas&Ref) ● 1M Clrw

B Result Summary (see more in full screen)

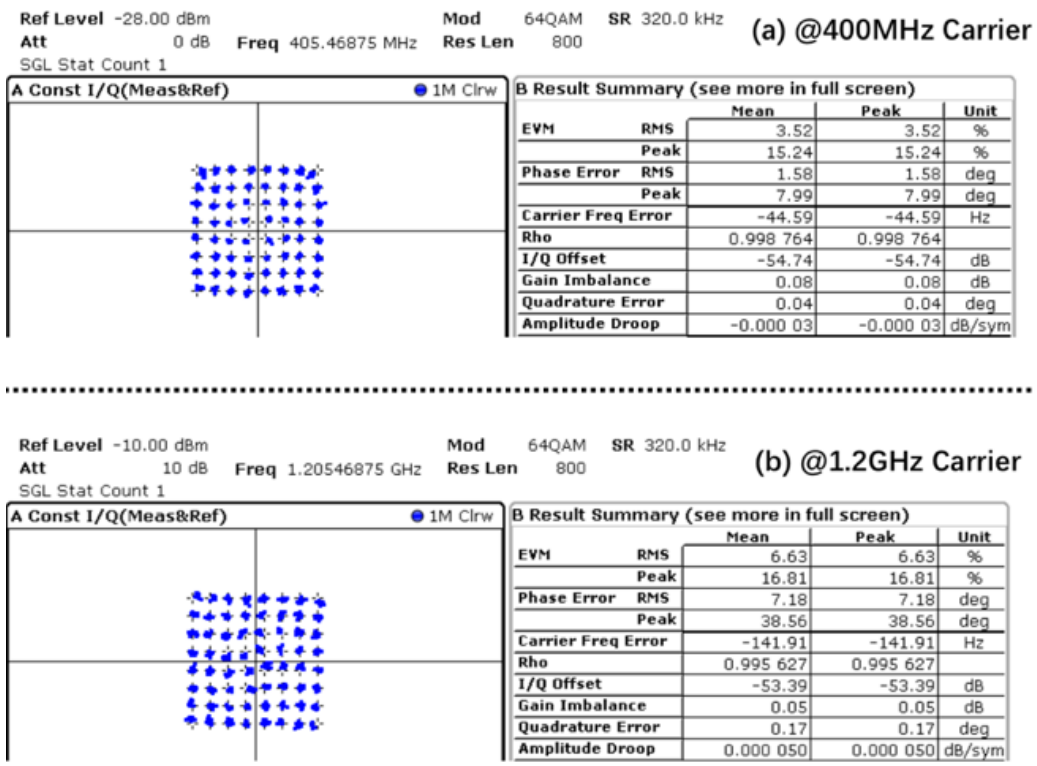|		Mean	Peak	Unit
EVM	RMS	6.63	6.63	%
	Peak	16.81	16.81	%
Phase Error	RMS	7.18	7.18	deg
	Peak	38.56	38.56	deg
Carrier Freq Error		-141.91	-141.91	Hz
Rho		0.995 627	0.995 627	
I/Q Offset		-53.39	-53.39	dB
Gain Imbalance		0.05	0.05	dB
Quadrature Error		0.17	0.17	deg
Amplitude Droop		0.000 050	0.000 050	dB/sym

Figure 5.5: 64 QAM constellation plot with 320k symbol/s rate, EVM=3.52% @400 MHz carrier (top) and EVM=6.63% @1.2 GHz carrier (bottom). [6]

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[6] The output power level primarily limits the measured EVM values. The prototype does not include the PA design.
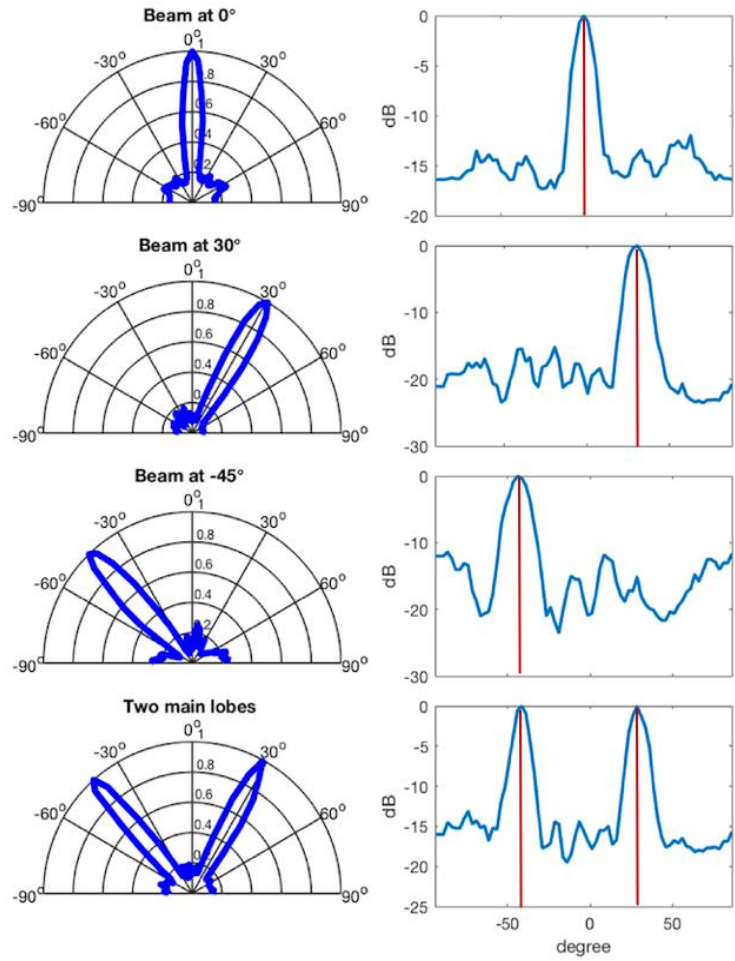
Figure 5.6: Measured transmit beam patterns at 0 degrees, 30 degrees, -45 degrees and with two simultaneous main lobes. The rho axis of the polar plot represents the normalized amplitude.
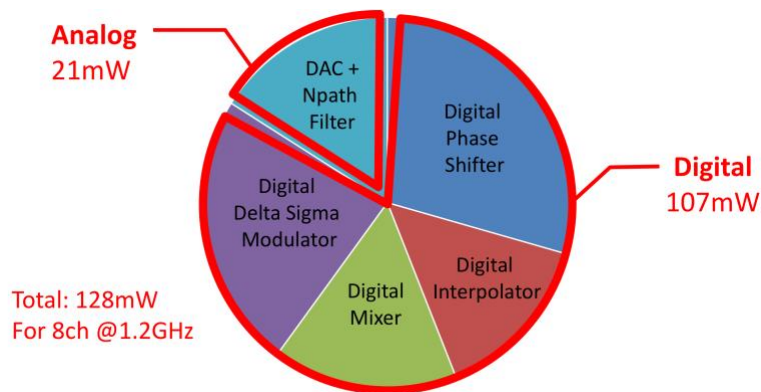

Figure 5.7: Power consumption breakdown of prototype 1.

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A power breakdown is given in Figure 5.7. Except for the DAC and N-path filter, all the other blocks are digital, and these digital blocks consume most of the total power. It is also clear that the digital phase shifting is a significant part of the power consumption, highlighting the advantage of reducing the digital phase-shifting frequency by a factor of eight as well as the benefits of our approach to frequency planning. The simple implementation of the digital up-mixer ensures that it is a minor contributor to the total power consumption.

Architecture	Digital transmit beam forming
Technology	40-nm CMOS
RF bandwidth	40 MHz
Carrier frequency	0.8-1.2 GHz
Input data	200 MS/s 10-bit I/Q baseband
Beamforming	Eight channels
Coefficient resolution	10 bits, 5-bit I and Q
# of simultaneous beams	2
EVM for 64 QAM	3.5% @400 MHz, 6.6% @ 1.2 GHz
Area	0.19 mm^2 (0.02 mm^2 /channel)
Power consumption	83 mW @ 0.8 GHz (**10 mW / channel**) 128 mW @ 1.2 GHz (**16 mW / channel**)

Table 5.1: Design summary for prototype 1.

Table 5.1 summarizes the measured performance. Table 5.2 shows a comparison with previous works. Similar to our RF modulator, [8] and [18] do not include a PA. For [31], the power consumption and area of the digital-RF converter (DRFC), in which the output driver is integrated, are excluded to make the comparison meaningful.

The die area per antenna element of our work is an order of magnitude smaller than the state-of-the-art. Apart from the DAC and the N-path filter, the design is generated with digital synthesis and place and route tools. This work demonstrates the promise of digital techniques for highly compact, flexible, and efficient direct-to-RF digital beamforming.

	[8]	[18]	[31]	This work[a]
$\Delta\Sigma$ **Type**	2nd order BP	3rd order LP	2nd order MASH	4th order BP
Carrier	900 MHz	1.95 GHz	5.25 GHz	1.2 GHz
BW [MHz]	20	50	200	40
EVM/SNR	36 dB	3.42%	30 dB	6.6%
Peak output power	3 dBm	-15.8 dBm	-13.73 dBm	-21 dBm
Power consumption	150 mW	69 mW	120 mW (digital Modulator only)	16 mW
Process	28 nm	90 nm	130 nm	40 nm
Area	0.82 mm^2	0.15 mm^2	0.16 mm^2 (digital Modulator only)	0.02 mm^2
Power amplification	1.5V MS DAC	Output stages	DRFC (2.5V)	No
BPF?	no	no	LC	N-path

[a]The power consumption and area of this work are per element of the transmit beamformer, and include the phase-shifter and N-path filter.

Table 5.2: Comparison with previous work.

5.2 Prototype 2

The second prototype is fabricated in 28 nm CMOS, occupies an active area of 0.08 mm^2. A die photo is shown in Figure 5.8. The use of wire-bond chip-on-board packaging means that the layout is I/O limited. To reduce RF losses, we place each H-bridge DAC close to its respective output pads. Each H-bridge DAC has an individual clock generator. We route a single 750 MHz reference to all eight PLL clock generators. One clock generator can be injection-locked for lower phase noise. The digital core (i.e., phase shifting, interpolation, up-sampling, and sigma-delta modulators) is at the center and occupies 0.06 mm^2. The core also includes SRAM to store transmit patterns. The patterns in SRAM and the beamforming coefficients are loaded through an SPI interface. The test setup is shown in Figure 5.9.

A single tone and a two-tone output spectrum are shown in Figure 5.10. Figure 5.11 shows measured beam patterns for beam directions of 0 degrees, 30 degrees, and -60 degrees, for a 6.048 GHz output. The plots assume a half-wavelength antenna spacing at the 6.048 GHz carrier frequency. The measurement angle step-size (phase resolution) is one degree. Outputs are recorded from all eight channels with the clock generator operating as PLL. We conducted a one-time digital calibration for amplitude and delay mismatch between channels for a zero degree beam angle. Figure 5.11 also shows measured beam patterns for two simultaneous beams. The measured beam patterns are close to the ideal patterns.
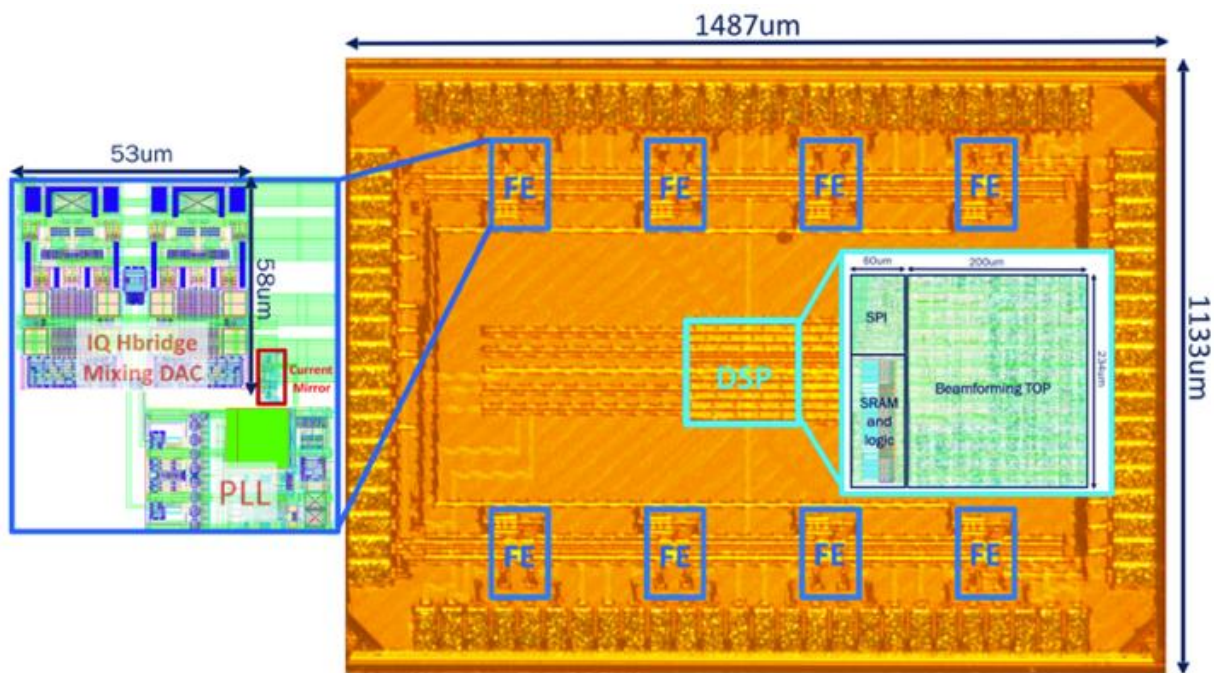

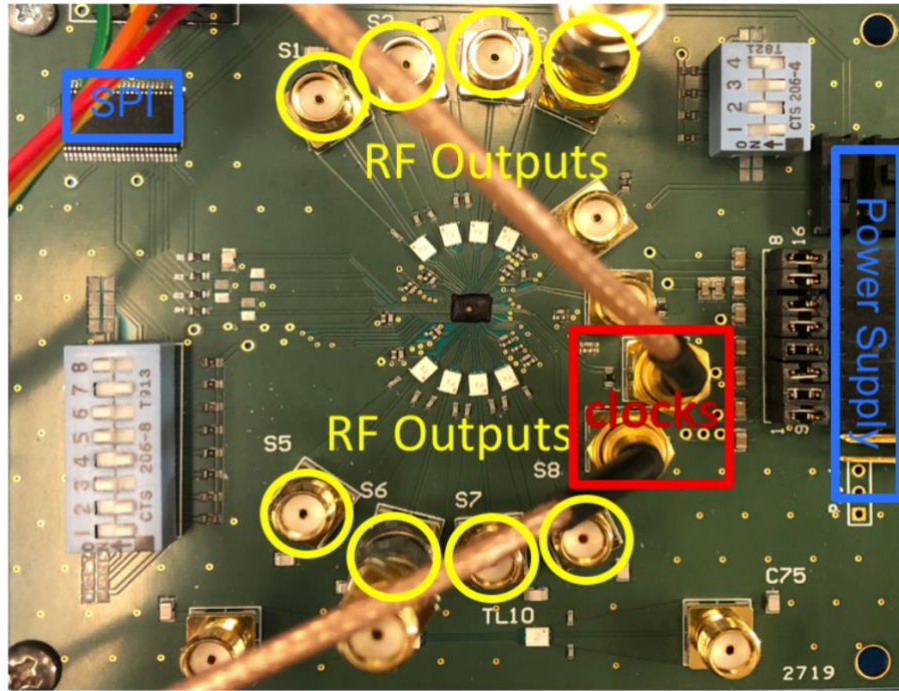Figure 5.8: Die micrograph of Prototype 2.

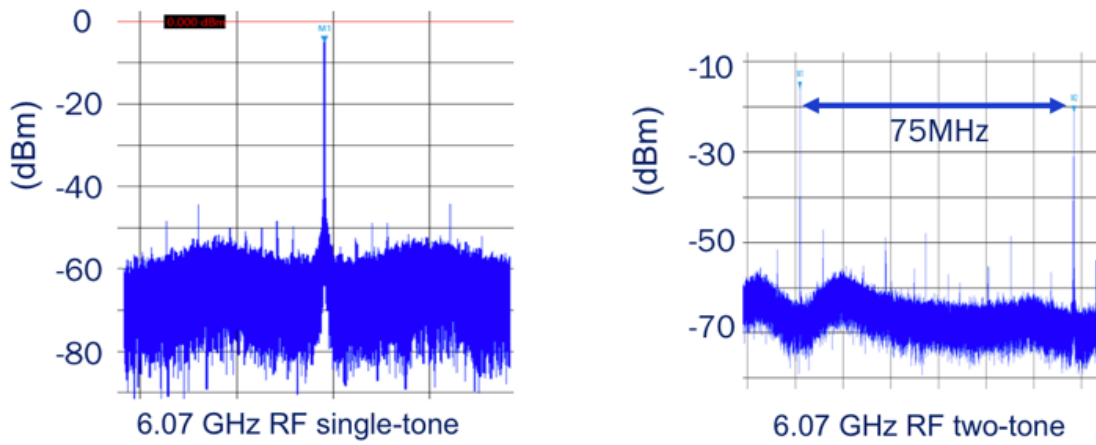Figure 5.9: Test setup of prototype 2.

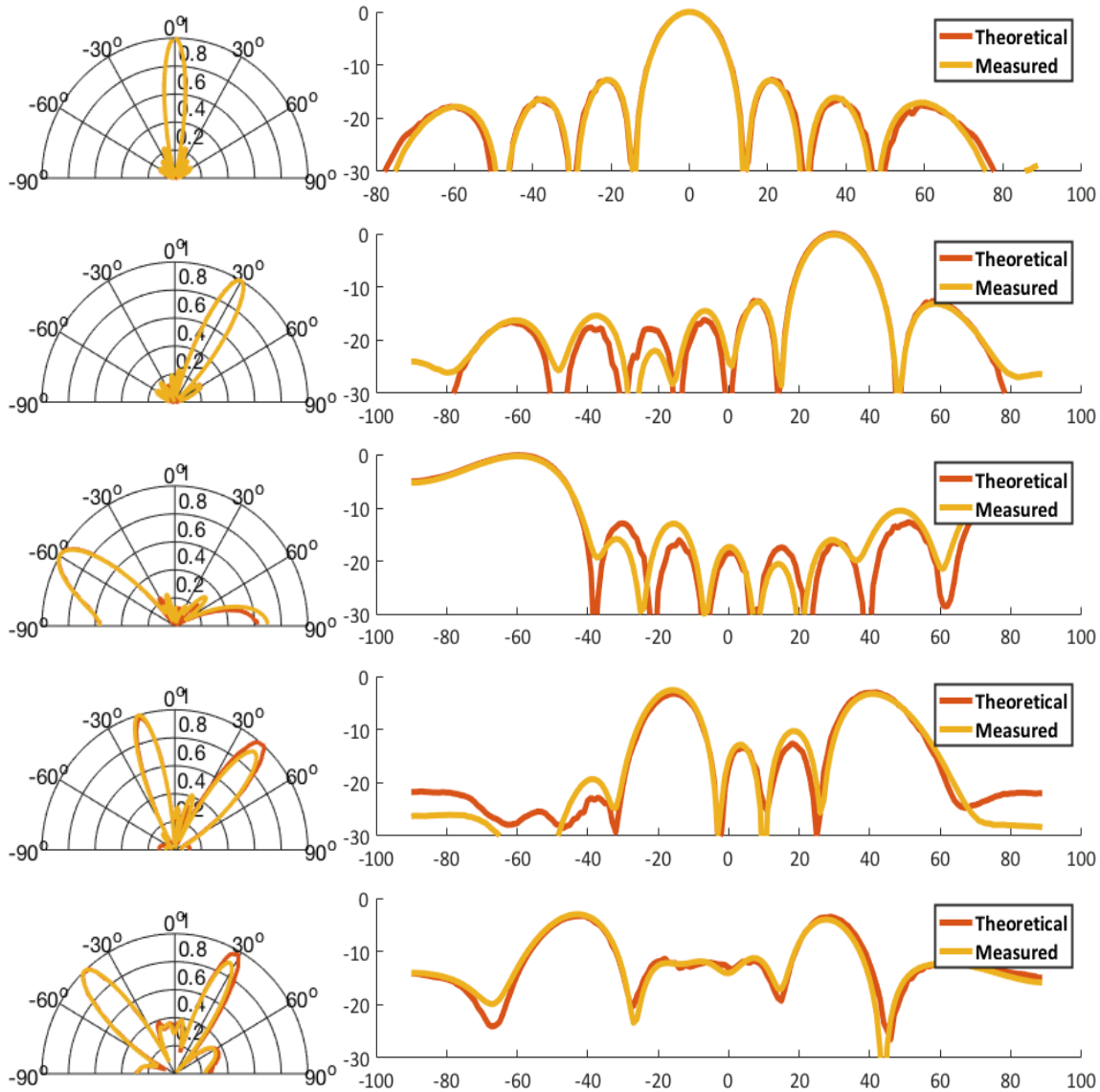Figure 5.10: Measured single-tone and two-tone spectra.

Figure 5.11: Measured beam patterns for 0 degrees, 30 degrees, -60 degrees, simultaneous -15 and 40 degrees, and simultaneous -45 and 30 degrees steered angles compared with ideal beam patterns.

Figure 5.12 shows the measured constellations for a single channel with the clock generator operating in injection lock mode. The measured EVMs for 16 QAM modulation at symbol rates of 20 MHz and 24 MHz are -30.13 dB and -29.6 dB, respectively. Table 5.3 shows the breakdown of power consumption. The total measured power consumption is 380 mW. The measured per-

element power consumption (including PLL) is 47.5 mW, for a measured -1.2 dBm per-element output power. After compensating for the measured cable and board losses, the effective output per-element power is 2 dBm. The DAC consumes 15.9 mW indicating a DAC power efficiency of 10%. The overall output power of the eight-element array is 11 dBm.
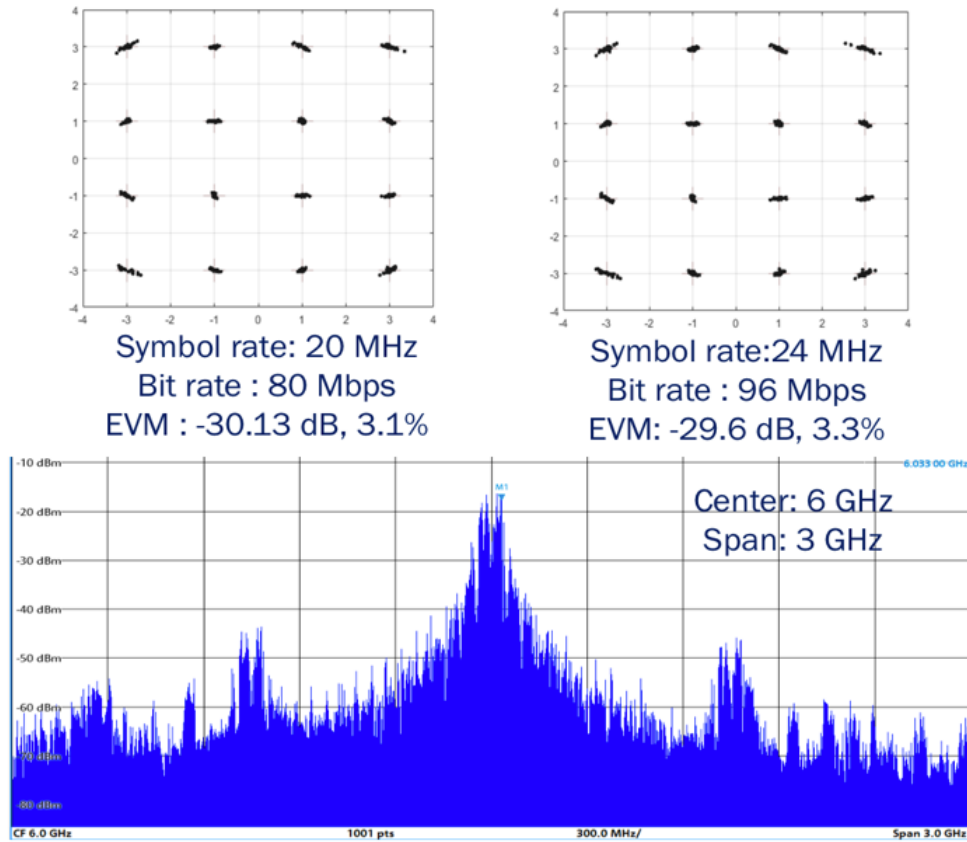

Figure 5.12: Measured 16-QAM constellations for a single output channel and the corresponding wideband spectrum.

Overall (mW)		Per element (mW)	
DAC	127	DAC	15.9
PLL	63	PLL	7.9
DSP	190	DSP	23.7
Total	380	Total	47.5

Table 5.3: Measured power breakdown of Prototype 2.

Table 5.4 compares this work with state-of-the-art beamforming transmitters and some single-element DDRF transmitters. The comparison table also includes some recent single-element

digital-to-RF transmitters. This work shows the potential of mostly-digital TX techniques for emerging beamforming wireless communication schemes.

	[1]	[2]	[20]	This Work		[8]	[11]
Architecture	SCPA #	IDPA #	1-bit DSM + N-path Filter	1-bit DSM + FIR Hbridge CSDAC #		10-bit DSM + CSDAC #	3-bit BP DSM + CSDAC #
# Elements	4	4	8	8		1	1
Technology (nm)	65	40	40	28		28	130 SiGe
Frequency (GHz)	1.45-2.15	3.0-7.0	1.2	6		0.9	1.0-2.25
BW (MHz)	15	12.5	40	160/80/40/20		20	50
EVM (%)	3.7	3.76 @ 68Mbps	6.6	2.6 @92Mbps		-	-
Supply Voltage (V)	1.4/2.8	1.1/1.2	1.1/1.2	1		0.9/1.5	1.5/3.3
Average Pout (dBm)	18.4	14.6	-21	11 in all	2 per element	3	-10.5
Peak Pout (dBm)	24.4	21.8	-15	13.7 in all	4.7 per element	-	-0.6
Power (mW)	-	-	128	380 in all	47.5 per element	150	445 *
Active area (mm²)	3.5 +	2.5 +	0.19	0.08 in all	0.01 per element	0.82	1.1 *

\# SCPA: switched-capacitor PA, IDPA: current digital PA, CSDAC: current steering DAC
* Only includes DAC core, retiming data path and DSM
+ Estimated from die micrograph

Table 5.4: Performance summary of prototype 2 and comparison with prior works.

5.3 Prototype 3

This prototype is fabricated in 28nm CMOS. The digital signal processing block occupies 0.019mm^2. The DAC and encoder together occupy 0.004mm^2. Figure 5.13 shows the die photo. The test setup is shown in Figure 5.14.

Figure 5.15 shows the measured and simulated broadband spectra for an 80 MHz RF bandwidth OFDM-modulated input signal. The transmitter directly meets the mask between 5.2GHz to 6.8GHz. The output matching network (i.e., on-board baluns) attenuates the far-out OOB noise. Figure 5.16 shows measured 64-QAM constellations for different modulation rates. The measurements show the feasibility of 64-QAM modulation up to 281Mbps. Figure 5.17 shows a close-in spectrum with a single carrier at 13 MHz.
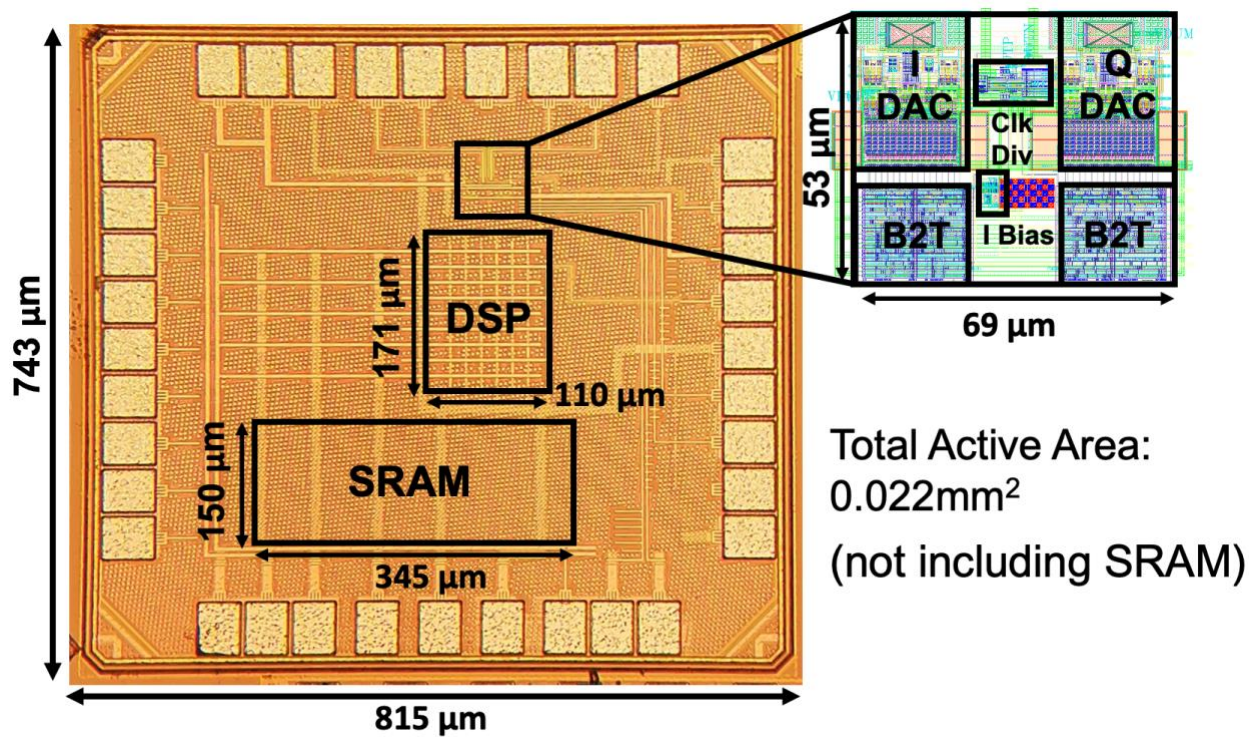

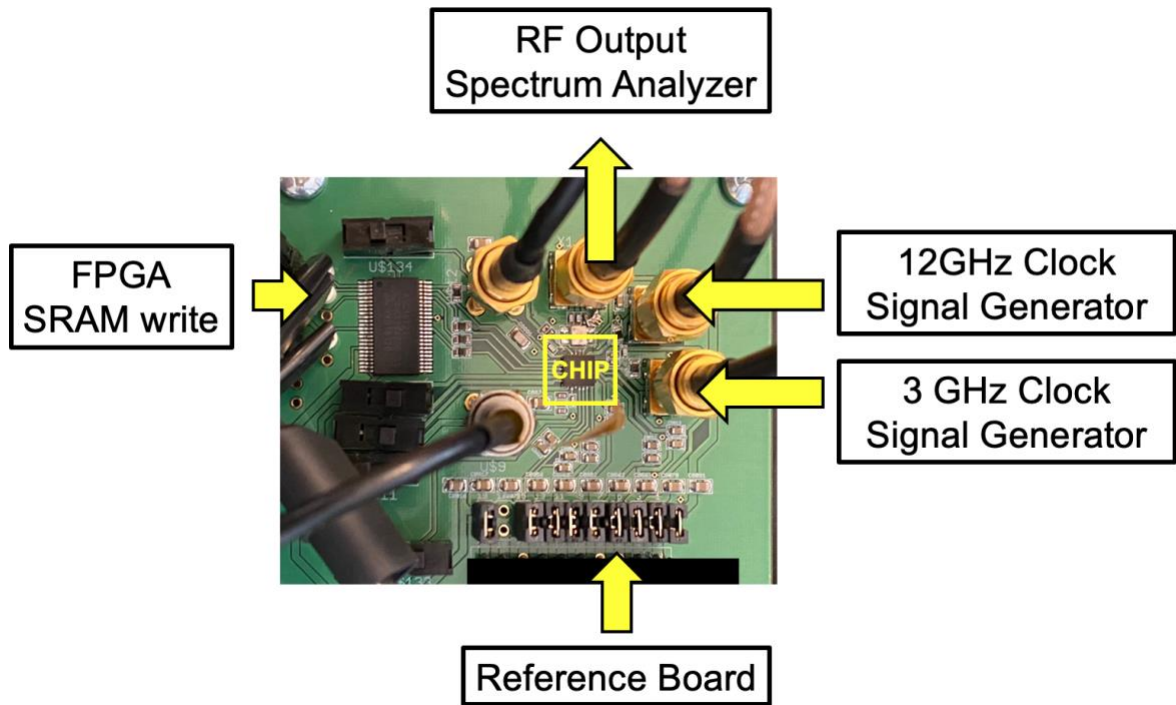Figure 5.13: Die micrograph of prototype 3.

Figure 5.14: Test setup of prototype 3.

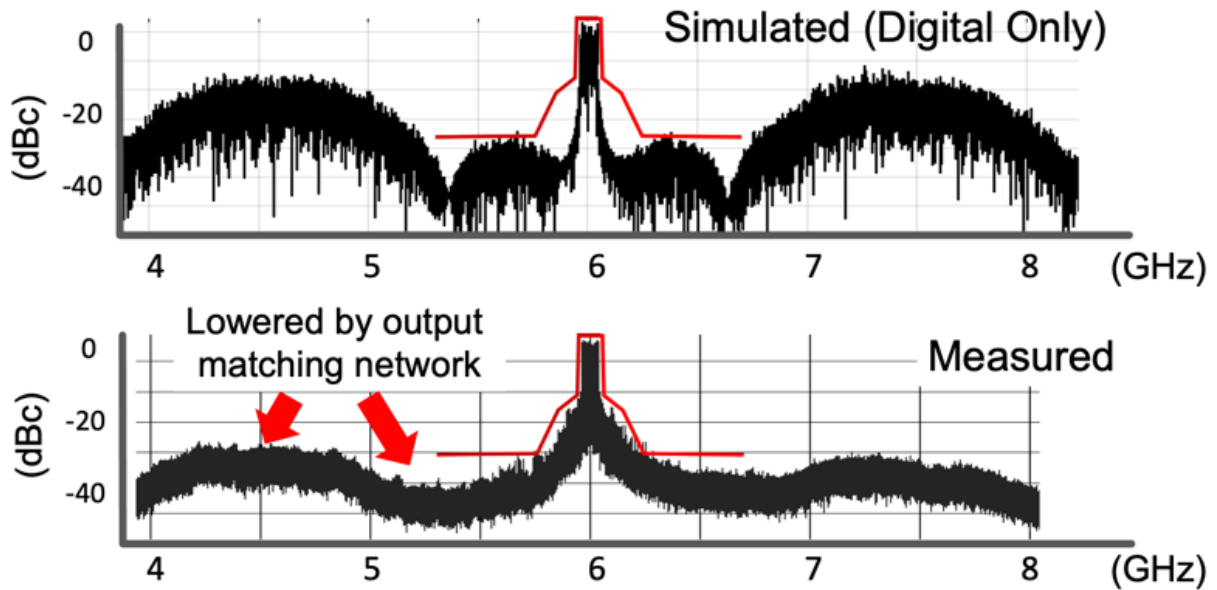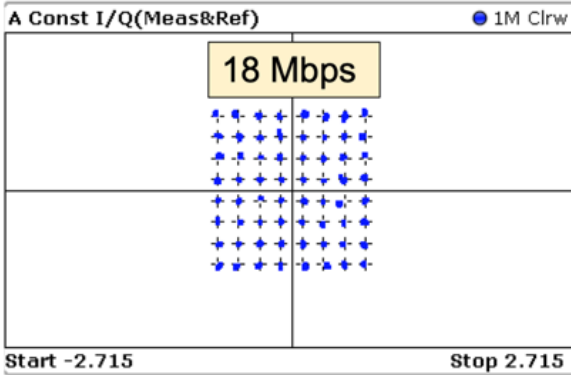Figure 5.15: Simulated and measured spectra for OFDM with 80MHz RF bandwidth. The spectral mask is shown in red.
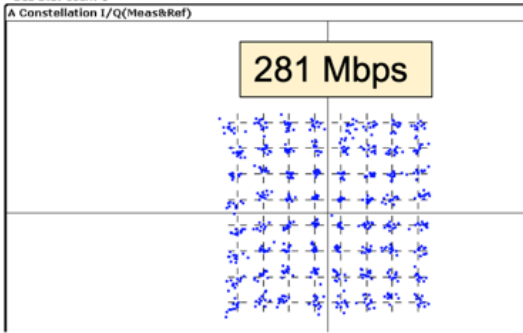
Figure 5.16: Measured constellation plots for 18 Mbps, 141 Mbps and 281 Mbps.
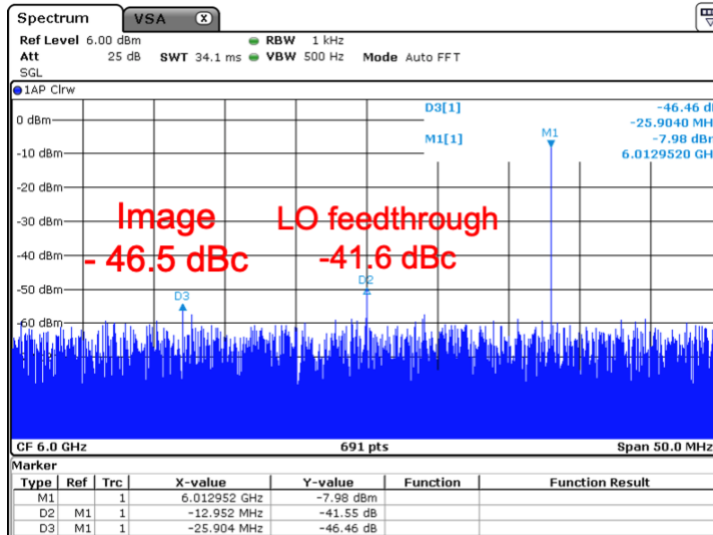
Figure 5.17: A close-in spectrum with a single carrier at 13 MHz.

Table 5.5 summarizes this work and compares it with prior DDRF systems. The table shows the advantage of this prototype in power efficiency. At the same time, it achieves high resolution (i.e., EVM) at 6 GHz RF.

	This work	[8]	[11]	[15]	[14]
Architecture	TaNS DSM + Hbridge CSDAC #	DSM + CSDAC #	BP DSM + CSDAC #	IQ mapping DDRM	TAF DDRM+
DAC resolution	5	10	3	12	12
Technology (nm)	28	28	130 SiGe	40	65
Frequency (GHz)	6	0.9	1.0-2.25	0.5-3	4.4
BW (MHz)	160	20	50	320	20/40
EVM (%)	3.4	-	-	2.5	1.8
Supply Voltage (V)	1	0.9/1.5	1.5/3.3	1.1/2.5	1/2.5
Peak Pout (dBm)	-4	-	-0.6	18.2	5
Power (mW)	64	150	445 *	540	1330 ^
Active area (mm2)	0.022	0.82	1.1 *	1.1	0.57

\# CSDAC: current steering DAC
* Only includes DAC core, retiming data path and DSM
\+ TAF: Time-approximation filter
^ Estimated from P_{out} and efficiency

Table 5.5: Performance summary of Prototype 3 and comparison with prior work.

Chapter 6 Conclusion and Future Work

This thesis explores direct digital processing for beamforming transmitters targeting 1 GHz RF and 6 GHz WiFi-6E. This work is one of the first to attempt direct-digital-to-RF for WiFi-6E.

We develop highly-efficient techniques from careful frequency planning. We investigate use of the image frequency, up-mixing noise folding, image duplication, and attenuation. Utilizing the image frequency allows the digital circuitry to run three times slower. Understanding of noise folding from up-mixing ensures we choose a practical sampling frequency. We develop interpolation filters for sufficient attenuation of the interpolation image. These contributions ensure highly-efficient fully-synthesizable DDRF architectures.

We thoroughly research delta-sigma modulation because noise-shaping is vital for good in-band Signal-to-Noise ratio (SNR) with a much smaller DAC. A smaller DAC also helps with DAC linearity. We develop a generalized flow to decide the DSM NTF starting with the bandwidth requirement, OSR, in-band SNR requirement and then finalize the filter form and coefficients. Time interleaved delta-sigma modulation is studied to potentially enable faster synthesized digital-logic speed.

We design an N-path filer and digital baseband I/Q lowpass filter tailored to the DSM NTF, in two different prototypes. We also propose a filter-free targeted noising-shaping (TaNS) technique. These techniques contribute to the feasibility of filtering at a very high RF frequency. An H-bridge combines current-DAC, filtering, and RF up-conversion for efficiency. A binary-to-thermal (B2T) decoder and dump current path further enhance the H-Bridge DAC's power efficiency.

We achieve a high level of digital automation. The digitally-intensive architecture scales well with technology. We develop a widely-applicable design strategy for digital-intensive communication systems.

Potential improvements and topics for further research include:

1) Digital adaptive pre-distortion to enhance linearity

2) DAC calibration and non-linearity modeling

3) A more thorough study and verification of the output matching network

4) A complete frequency plan to meet the WiFi-6E standard scenarios for different bandwidths (10-160 MHz) and different subcarriers (5.925-7.125 GHz).

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