Advances in Amorphous Oxide Semiconductor Devices, Materials, and Processes for Customizable Scalable Manufacturing of Thin-Film Electronics

by

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To my parents,
for giving me the world.

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Abstract

Electronic circuits comprised of thin-film transistors (TFTs) are essential to nearly every modern display technology. For decades, the TFT industry relied on amorphous silicon, but increasing performance demands required semiconductors with superior electron transport leading to the adoption of amorphous oxide semiconductors (AOS). The superior electron transport and ease of thin-film preparation of AOS has led to a growing interest in developing thin-film electronics for beyond-display technologies. These include monolithic 3D integration on Si complementary metal-oxide-semiconductor integrated circuits (ICs) – to continue Moore's law, add new functionality, and improve performance – and flexible electronics for electronic skins, textiles, solar cells, and displays. In this thesis we facilitate the adoption of thin-film electronics for beyond-display technologies by: 1) developing uniform and conformal AOS deposition processes with record performance; 2) demonstrating expanded AOS capabilities by exploring new device architectures; and 3) developing a new additive manufacturing technique for customizable scalable manufacturing.

First, we meet the performance and thermal budget requirements of AOS for beyond-display applications by using atomic-layer deposition (ALD) – a conformal, uniform, and precise vapor-phase deposition technique – and aggressively optimizing the process conditions. We discovered that improved electrical performance correlated with an increase in film density, which can be achieved by increasing deposition temperature, by post-deposition annealing, and by using plasma enhanced-ALD (PE-ALD). Second, we made innovations in device design to expand the range of circuit applications for AOS TFTs by exploiting the benefit of their wide-bandgap to

fabricate high-voltage TFTs (HVTFTs). While the current handling capabilities of these HVTFTs cannot compete with conventional power electronics, the ability to deposit AOS materials directly on Si ICs may enable monolithic 3D integration of HVTFTs, adding new functionality as an HV interface to aggressively scaled low-voltage Si CMOS. Third, we show that ambient instabilities are caused by interactions between the surface of the AOS film and ambient molecules. We eliminate these instabilities by developing an ALD-based passivation layer. Fourth, we study the temporal and bias stress stability of our ALD AOS thin-film transistors and see excellent stability after the first month of aging and improved positive bias stress stability with passivation. Fifth, we investigate several materials to form a Schottky contact to ALD AOS films to enable future rectifier-based circuits and unipolar logic circuits. Finally, we develop an additive manufacturing approach for customizable manufacturing of AOS devices. Further improvement in device performance and reduction of channel length, enabled by the sub-μm precision of EHD, has the potential to yield fully customizable additive manufacturing of high-frequency circuits.

Chapter 1 Introduction

1.1 Motivation for scalable manufacturing of thin-film electronics

Silicon has been the go-to semiconductor for more than 60 years, allowing for material characterization, device optimization, and enhanced production processes. State of the art silicon complementary metal oxide semiconductor (CMOS) technology has exploited materials and processes to reach commercialized 5 nm node integrated circuits (ICs) with 3 nm node technology in the works.[1] The continual two-dimensional device scaling continues Moore's law, an exponential increase of the performance-to-cost ratio, but as the nodes get smaller, the continuation of Moore's law becomes more challenging and may eventually reach a limit due to process or physical limitations.[2]

While Moore's law will reach a limit, the increase in performance demands will not, as the development of artificial intelligence and neural networks expands. Other technologies are being explored to continue performance improvements past two-dimensional device scaling. The "More-than-Moore" technologies being explored include novel computing methods and novel device structures and integration schemes.[3] Of particular interest to the material and device community are device integration schemes, including 3D scaling.

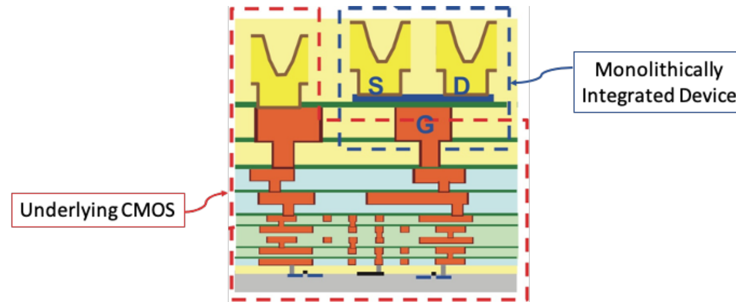


Figure 1.1 Schematic illustration of device-level monolithic 3D integration. Adapted from [4] copyright 2011 The Japan Society of Applied Physics.

Expanding two-dimensional device scaling to include a third dimension can be achieved through three-dimensional integration of integrated circuits at the package-, die-, wafer-, or device-level.[5]–[9] Of these integration techniques, device-level monolithic 3D integration, illustrated in Figure 1.1, offers the least complex method of increasing device density and reducing interconnect delays.[9] The devices used for device-level integration typically use thin-film materials grown on heterogeneous substrates without requiring bulk wafers, Table 1.1. Successful industry adoption of device-level integration requires scalable manufacturing of thin-film electronics for high-throughput and large-area processing as the CMOS wafer size exceeds 8” in diameter. Silicon has been studied as a thin-film material by depositing amorphous silicon and using a laser to induce recrystallization into poly-silicon.[10] This process, however, is not suitable for large-area scalable manufacturing because polysilicon is not uniform across grain boundaries. Therefore, there is a need for other materials and processes for scalable manufacturing.

Table 1.1 Summary of 3D-IC approaches.

Semiconductor	Process	Process Temperature	Large-area Uniformity	Reference
Poly-Ge	Flash-lamp annealing of sputtered *a*-Ge	400ºC	No	[11]
Poly-Si	Laser annealing of *a*-Si	400ºC	No	[10]
CNT	CNT transferred from quartz	200ºC (900ºC growth)	Yes	[12]
MoS_2/WSe_2	Exfoliation of MoS_2 flakes and pick-and-place WSe_2	120ºC	No	[13]
c-IGZO	Sputtering	-	No	[14]
a-IGZO/SnO	Sputtering	-	No	[15]
a-ZTO	Solution process	520ºC	Yes	[16]

Another rapidly growing application area for scalable electronics is flexible electronics. Flexible electronics are being investigated for stretchable electronic skins and textiles and flexible solar cells and displays. While the exploitation of silicon has been extremely successful for CMOS ICs, the substrates are flat and rigid prohibiting flexible applications. Several processes have been investigated to create flexible silicon-based CMOS electronics, but these approaches are often complex and subtractive resulting in a loss of material.[17] Furthermore, many of the flexible applications require large-area electronics and these processes are not compatible with large-area processing. As a result, silicon is not a commercially viable technology for flexible electronics and, again, there is a need for other materials processes for scalable manufacturing for flexible applications.

There are three main areas of development required for scalable manufacturing of thin-film electronics: 1) materials, 2) processes, and 3) devices. These will be introduced in more depth in the following sections.

1.2 Amorphous oxide semiconductors for active layers in scalable manufacturing of thin-film electronics

The two application areas for scalable manufacturing of thin-film electronics discussed in the previous section, device-level monolithic 3D integration and flexible electronics, have their own electrical and material property requirements. For successful device-level monolithic 3D integration, the resulting devices should have a field-effect mobility, μ_{FE}, greater than 20 $cm^2V^{-1}s^{-1}$, behave as normally-off (enhancement-mode) transistors, and be switched between on and off with the limited supply voltages used in 5 nm node Si-ICs with process temperatures below the back-end-of-line thermal budget of approximately 450ºC. While the requirements of monolithic 3D integration are also desired for flexible electronics, flexible applications have the additional material requirement of deposition techniques compatible with flexible substrates.

While crystalline and poly-crystalline silicon meet many of these requirements, the uniformity issues with poly-silicon and limitation to largely flat and rigid substrates make crystalline and poly-crystalline silicon a poor-choice for scalable manufacturing. These same limitations exist for other crystalline and poly-crystalline materials prohibiting their use in scalable manufacturing for these applications. Amorphous silicon, on the other hand, removes the grain boundary uniformity issues and can be processed on a variety of substrates, but suffers from poor electron transport, as discussed later in this section. Another class of materials suitable for large-area application are organic semiconductors, but these too suffer from poor electron transport and environmental instabilities.[18]

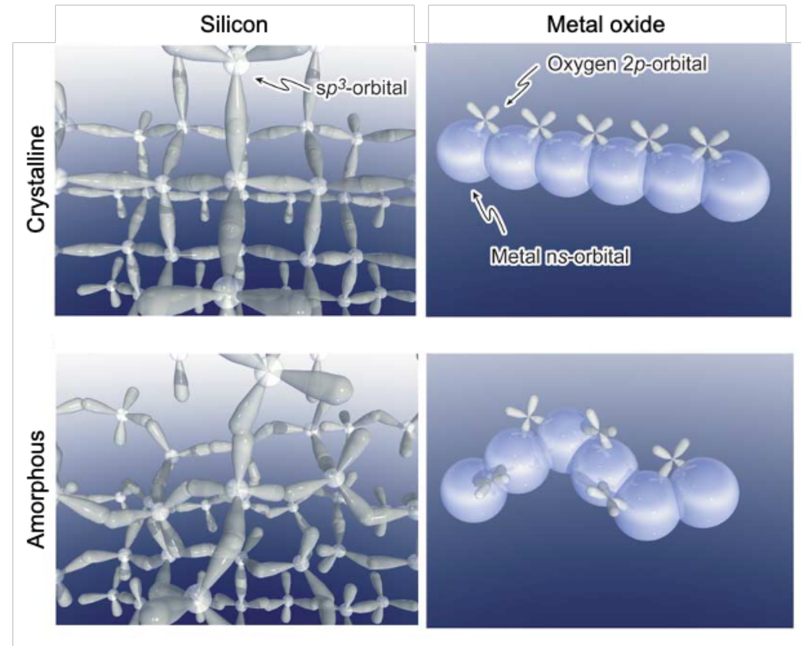


Figure 1.2 Schematic showing the orbitals that form the conduction band minimums in covalently bonded silicon (left) and metal oxide semiconductors (right). The conduction band minimum of Si is comprised of sp^3 orbitals that are severely disrupted in the amorphous phase (bottom left) whereas the large spherical metal *ns* orbitals of metal oxides are insensitive to phase. Adapted by permission from Springer Nature Customer Service Center GmbH: [19].

The a-Si mobility limitation of approximately 1 $cm^2V^{-1}s^{-1}$ is due to the directivity and bond-angle fluctuation of sp^3 orbitals which make up the carrier transport paths, or conduction band minimum, in covalently bonded semiconductors.[19] The disruption of the conduction band minimum is not present in amorphous oxide semiconductors (AOS), containing post-transition-metal cations, because the conduction band minimums are primarily composed of spherical metal *ns* orbitals with a large overlap between neighboring *ns* orbitals. This means that even in the amorphous phase, degenerate band conduction and mobility at least an order of magnitude higher than a-Si is possible in AOS. These orbitals are schematically illustrated in Figure 1.2.

Indium-gallium-zinc-oxide (IGZO) is a widely studied AOS successfully commercialized in scalable manufacturing for the active layer of thin-film transistors in display backplanes.[20] Successful commercialization is due, in part, to the large area uniformity which results from the amorphous structure that also makes AOS an ideal candidate for scalable manufacturing. In

indium-containing AOS, such as IGZO, indium is required to achieve good electrical conduction because the large spherical *5s* orbitals of indium cause conduction band dispersion between neighboring metal ions. Indium has become an expensive metal due to scarcity and an increasing demand for transparent conductor materials that contain indium.[21] Indium is also a by-product of mining for zinc and is difficult to extract because it is naturally found with toxic elements such as cadmium.[22] The environmental impacts and scarcity of indium leads to a desire for indium-free AOS thin-films. In this thesis, we focus on studying zinc-tin-oxide (ZTO) as an indium-free AOS with the *5s* orbital of earth-abundant tin replacing indium in causing the conduction band dispersion mechanism without sacrificing electrical performance. ZTO can be deposited by a variety of different techniques which will be discussed in the following section.

1.3 Atomic layer deposition for scalable manufacturing of thin-film electronics

Deposition techniques compatible with the large-area and low-temperature process requirements of scalable manufacturing must also be able to deposit high-quality films to meet the electrical-performance requirements of scalable manufacturing. ZTO has been deposited using solution processing[23] and vacuum-based processes like pulsed laser deposition (PLD),[24] sputtering,[25]–[27] and atomic layer deposition (ALD).[28], [29] All of these deposition techniques are able to deposit films with typical field effect mobility of ~10-30 $cm^2V^{-1}s^{-1}$, generally meeting the μ_{FE} requirements of device-level monolithic 3D integration. However, each deposition process presents unique opportunities and challenges for scalable manufacturing.

A portion of the work in this thesis uses solution-processing to deposit ZTO because it is a low-cost and low-barrier means of studying AOS.[30], [31] Recent work has also demonstrated the promise of using solution processing for device-level monolithic 3D integration.[16] These works currently require annealing the solution at greater than 450ºC to create high-performance

thin-films making the process incompatible with BEOL processing and flexible substrates, presenting a challenge for industry adoption of solution processing for scalable manufacturing. A low-temperature vacuum-based technique may be a more viable option for deposition of high-quality films for scalable manufacturing.

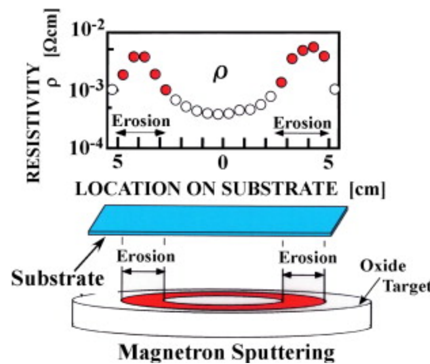


Figure 1.3 An erosion ring appears in sputtering targets as they are used. The erosion ring causes non-uniformities, as illustrated here, for the resistivity of a transparent conducting oxide deposited by DC magnetron sputtering. Reprinted from [32] with permission from Elsevier.

Sputtering, a type of physical vapor deposition, is one of the most widely studied AOS deposition techniques as it allows films to be deposited at room temperature.[33] Sputtered AOS thin-films have been commercialized for large-area thin-film transistor arrays demonstrating an AOS deposition technique in scalable manufacturing.[20] Sputtering of AOS materials does, however, present its own set of challenges. For example, moisture inadvertently introduced into the sputtering chamber during sample loading can lead to poor-quality AOS films, illustrating the importance of the chamber gas composition to device performance.[34] Therefore, precise control of the sputtering environment is required to achieve high-performance films. Additionally, sputtering can lead to compositional gradients across a substrate and changes in film morphology and electrical properties can occur as the target is used and eroded (Figure 1.3).[32], [35] While some research groups have leveraged this compositional gradient to study different film compositions, it is an unwanted characteristic when trying to deposit large-area uniform films for scalable manufacturing.[36], [37]

PLD, on the other hand, typically results in thin-films compositions very similar to that of the source material with minimal changes from the vacuum environment.[38] This is not to say, however, that the films are uniform across a substrate. The films in the center of the PLD plume may differ, in thickness, by up to 50x from the films at the edges of the plume, forming a somewhat Gaussian distribution of films thickness across a substrate.[39] Spatial non-uniformity and low-throughput present challenges in adoption of PLD for scalable manufacturing.

In addition to the unique challenges of each deposition technique outlined above, both PVD techniques are not suitable for non-planar substrates as they are line-of-sight deposition techniques. Some solution-process coating techniques, e.g. dip coating, can deposit on non-planar substrates, but the surface interactions required may prevent uniform coverage. ALD, on the other hand, is an advanced chemical vapor deposition (CVD) technique that can produce uniform films on both planar and non-planar substrates without line-of-sight limitations.[40]

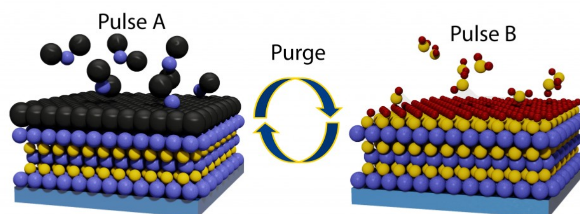


Figure 1.4 A schematic illustration of one ALD cycle. First, precursor A is pulsed into a vacuum chamber. Once the surface is saturated with the precursor, the material is purged out of the vacuum chamber. Next, the same is done for precursor B or the oxidant species. Together, these make up one ALD cycle and ideally leads to one atomic layer of deposition. Courtesy of Prof. Neil Dasgupta's group.

The excellent uniformity and conformality of ALD is due to the process being a vapor-phase deposition technique that exploits self-limiting surface reactions as illustrated in Figure 1.4. Furthermore, ALD is a low-temperature, atomically precise layer-by-layer growth technique allowing for precise control of film interfaces, stoichiometry, and thickness. All of these characteristics make ALD an excellent candidate for scalable manufacturing, Table 1.2.

Furthermore, industry has adopted ALD for deposition of high-*k* gate dielectrics, proving the scalability of the process.[41] The main drawback to ALD is the slow growth rate. Spatial-ALD, where precursors are separated by space instead of time, is being studied as a way to increase deposition speed and therefore throughput.[42]

Table 1.2 Summary of the advantages and challenges of AOS deposition techniques.

	Solution Process	Sputtering	PLD	ALD
Uniform and Conformal	Yes	No	No	Yes
Process Temperature	High	Low	Low	Low
Adopted in Industry	No	Yes	No	Yes

ALD has been used to deposit device active layers for many different quaternary or quinary indium-containing AOS materials with field effect mobility greater than the 20 $cm^2V^{-1}s^{-1}$ minimum required for device-level monolithic integration.[43]–[47] As these processes are quaternary or higher and contain indium, they are more complex and costly than a ternary indium-free ZTO process. Most previous work on ALD ZTO focused strictly on the material science aspects,[48]–[55] with just two studying thin-film devices made using ALD ZTO.[28], [29] These studies report field effect mobility as high as 13.2 $cm^2V^{-1}s^{-1}$, below the device-level monolithic 3D integration minimum. Therefore, new ALD processes are required to achieve high-performance within the scalable manufacturing performance and process requirements.

In addition, the previous work on ALD ZTO thin-film devices use thermal SiO_2, a low-*k* dielectric, as a gate insulator resulting in high switching voltages, the difference between the threshold voltage and turn-on voltage, leading to supply-voltage incompatibility with CMOS ICs. Furthermore, thermal SiO_2 must be grown on Si substrates and at high temperatures, neither of which are compatible with the applications of scalable manufacturing we are investigating. Fortunately, ALD can also be used to deposit high-*k* gate insulators, resulting in reduced switching

voltages and process compatibility with scalable manufacturing applications, but further work is required to integrate an ALD-based gate insulator with ALD ZTO active layers. As ALD can uniquely deposit high-quality dielectrics and semiconductors, *in situ* processes can also be studied to form excellent interfaces for low subthreshold swing TFTs.

1.4 Electrohydrodynamic-jet printing and area-selective ALD for scalable manufacturing of customizable thin-film electronics

Advances in photolithographic patterning have enabled the state-of-the-art 5 nm node ICs patterned using extreme ultraviolet (EUV) technology.[56] The entire process requires tens to hundreds of steps each using a set mask for top-down etching of deposited thin-films or selective ion implantation. While industry has worked for decades to perfect these processes for high-throughput of planar Si ICs, customizing the process to meet unique run requirements or patterning non-planar substrates would be costly and inefficient. As the field of flexible electronics grows to include more personalized and non-planar systems, there is an increased demand for customizable manufacturing in an inexpensive and efficient way. Additive manufacturing, building up layer-by-layer, is being studied as a customizable manufacturing technique.

Direct printing of materials, an additive manufacturing technique, allows for rapid low-cost customizable large-area 3D patterning. Standard inkjet-based direct printing can achieve pattern resolution down to 20 μm.[57] To push the resolution limit, the "coffee ring effect" was exploited to print metal-oxide TFTs with channel lengths as short as approximately 3.5 μm.[58] The challenges with this approach are that the semiconductor is deposited using a solution-process requiring annealing up to 350ºC making the process incompatible with most flexible substrates and only achieves a moderate μ_{FE} of 4.9 $cm^2V^{-1}s^{-1}$.

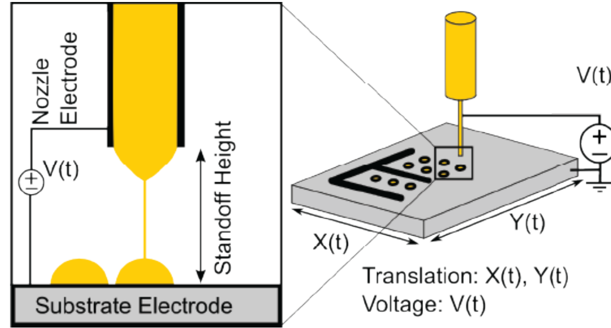


Figure 1.5 Schematic illustration of electrohydrodynamic jet printing. Courtesy of Prof. Kira Barton's group.

Electrohydrodynamic jet (e-jet) printing, illustrated in Figure 1.5, uses an electric field applied between a printing nozzle and substrate to perform direct printing of materials.[59]–[61] Using this process, long channel (> 50 µm) TFTs were directly printed.[62]–[64] As with the inkjet work referenced above, this process is incompatible with flexible substrates because the ink solution requires annealing at 500°C to achieve a μ_{FE} of 9.82 $cm^2V^{-1}s^{-1}$. To meet the thermal budget of flexible substrates and the performance requirements of device-level monolithic 3D integration, the process must transition away from solution-processed active layers in favor of a lower temperature and higher performance deposition technique.

In the previous section, we explained why ALD is a good deposition technique for scalable manufacturing and here we will explain how ALD can be combined with non-photolithographic patterning for customizable manufacturing. Polymers deficient in the surface reaction sites required for ALD can act as inhibitors to ALD growth leading to area-selective ALD (AS-ALD) of oxides, nitrides, and metals.[65] The inhibitor polymers can be patterned by inkjet printing, micro-contact printing, and directed self-assembly of monomers to define features to manufacture thin-film devices.[66] By using inkjet printing of polymer inhibitors, ZnO TFTs have been fabricated with mobility approaching 20 $cm^2V^{-1}s^{-1}$.[67] Without special tricks, like the coffee ring effect introduced above, the resolution on inkjet-printing and AS-ALD is > 20 µm.

E-jet printing has been used to print features with resolution down to ~30 nm.[61] By combining e-jet printing of inhibitor polymers and AS-ALD of thin-films, customizable fabrication of devices with sub-μm channel lengths on non-planar substrates may be possible. To successfully exploit e-jet printing and AS-ALD for high-performance device fabrication, the process must be developed with an understanding of the material's physical and electrical properties, the interfaces between materials, and how the manufacturing process impacts device performance.

1.5 Thesis objectives

The objective of this thesis is to develop advances in amorphous oxide semiconductor materials, processes, and devices to enable customizable scalable manufacturing of thin-film electronics. Initially we develop an AOS ALD process to both increase the performance of indium-free AOS semiconductors, to achieve $\mu_{FE} > 20$ cm^{2}V^{-1}s^{-1} required for device-level monolithic 3D integration, and reduce the process temperature to 200ºC, to enable flexible substrate compatibility. To reduce the power consumption and enable compatibility with low-voltage CMOS, we use an *in situ* gate insulator to achieve TFT subthreshold swing approaching the ~59.7 mV dec^{-1} room temperature Boltzmann limit. While there are many reports of using AOS to create thin-film devices, the majority of them focus on conventional TFTs. To explore the full capabilities of AOS in thin-film devices, we investigate other device architectures including high-voltage TFTs (HVTFTs). While analyzing the HVTFT performance, we discover instabilities and performance degradation caused by exposure to air-ambient. To improve the device stability and limit performance degradation, we develop a passivation layer. Once the ambient stability is solved, we study and improve the temporal and bias stress stability of AOS TFTs required for future adoption for beyond-display technologies. To further expand the range of devices that can

be made using our ALD ZTO semiconductor deposition technology, we then investigate Schottky-based devices which requires the development and characterization of Schottky contacts to ALD-based AOS. Finally, we develop the e-jet and AS-ALD processes required to additively manufacture customizable high-performance devices. Combined, this work represents significant advances in customizable and scalable manufacturing of AOS thin-film electronics.

1.6 Thesis overview

In Chapter 2, we demonstrate three ALD processes to deposit ZTO. First, we study the material properties of the resulting thin-films and find an equation to fit the tin composition to the tin cycle fraction. Then, we tune the tin content, deposition temperature, and post-deposition anneal to achieve the highest μ_{FE} ever reported for an ALD ZTO process. Furthermore, the temperatures are compatible with BEOL. A lower temperature process yielding a slightly lower μ_{FE} can be used for flexible substrate compatibility. Finally, we use an *in situ* gate insulator with a low density of interface defects to achieve an excellent *SS* of 60 mV dec^{-1}. In Chapter 3, we begin with device modeling to study the impact of HVTFT device architecture on breakdown voltage, V_{BD}, and on-resistance, R_{on}. The findings from the device modeling are then used to inform successful fabrication and testing of HVTFTs. Finally, device modeling is used to suggest improvements to the HVTFT architecture. In Chapter 4, we study thinning of solution-processed ZTO and passivation of the back channel. Measuring fabricated devices under vacuum revealed that both active layer thickness and the back surface are important for device stability. Using this information, we developed an O_3-based ALD Al_2O_3 passivation layer leading to ambient insensitive enhancement-mode devices. In Chapter 5, we investigate the temporal and bias stress stability of our high-performance ALD ZTO TFTs. Devices show minimal changes in the first 25 days of aging and then excellent temporal stability. The positive bias stress stability is improved

through application of a passivation layer. In Chapter 6, we investigate several materials as rectifying contacts to ALD ZTO and demonstrate the first Schottky contact. Future work improving Schottky performance will enable rectifier-based circuits and MESFET-based logic circuits. In Chapter 7, we describe our development of an e-jet and AS-ALD process required to additively manufacture high performance devices. This required an understanding of the impact of the manufacturing process on device performance, including interfaces and materials. The thesis concludes with Chapter 8, summarizing the contributions of this thesis and giving recommendations for future research based on scientific questions raised by this work.

Chapter 2 High-Performance Zinc-Tin-Oxide TFTs with Active Layers Deposited by Atomic Layer Deposition

2.1 Introduction

The superior electron transport, high optical transparency, amorphous morphology, and large-area uniformity of transparent amorphous oxide semiconductors (TAOSs) have led to their commercialization as thin-film transistors (TFTs) in display backplanes.[20], [68] To open new functionality opportunities and increase performance of silicon complementary metal oxide semiconductor integrated circuits (CMOS ICs), TAOS are being explored for back end of line (BEOL) 3D monolithic integration.[16] For a TAOS material to be considered for BEOL 3D monolithic integration the thermal budget must be compatible with CMOS, less than approximately 450 ºC, and meet specific performance criteria, e.g. $\mu_{\mathrm{FE}} > 20\ \mathrm{cm^2V^{-1}s^{-1}}$, enhancement-mode behavior, and small switching voltages.[69] Advances in material processes are required to meet the thermal and performance requirements.

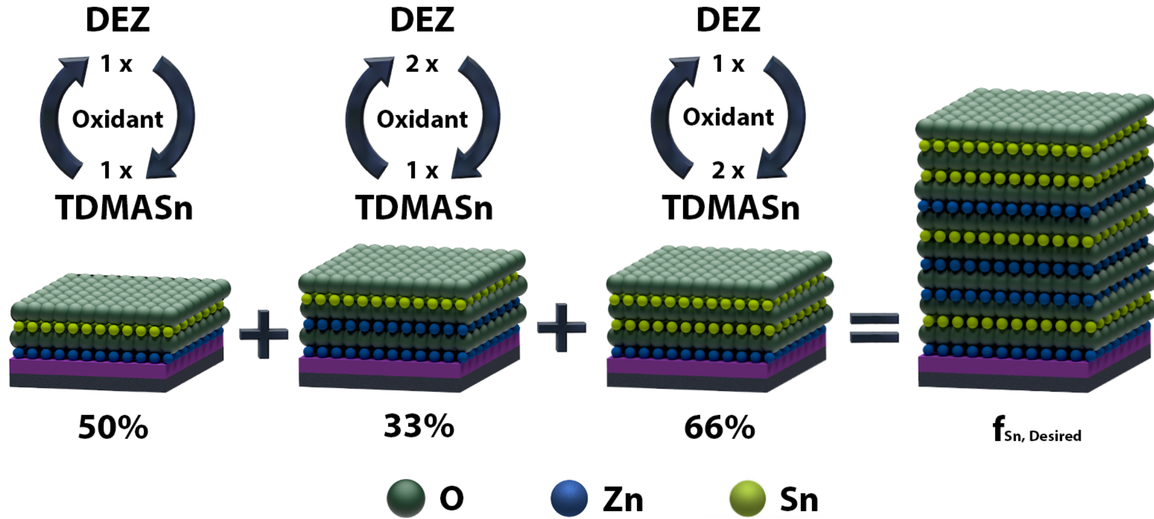


Figure 2.1: Schematic illustration of the ZTO ALD supercycle used in this chapter composed of sub-supercycles with f_{Sn} of 50%, 33%, and/or 66%. The sub-supercycles can be combined and repeated in any order within the supercycle to obtain the desired f_{Sn} of the final ZTO film. Reprinted with permission from reference [70].

Considering the vacuum-based deposition techniques, pulsed laser deposition (PLD),[24] sputtering,[25]–[27] and atomic layer deposition (ALD),[28], [29] the latter two are more promising for BEOL 3D monolithic integration as they are already widely used in industry. In this chapter, we will focus on ALD because it is a low-temperature self-limiting vapor-phase deposition process that allows for precise control of film interfaces, stoichiometry, and thickness.[40], [71] The more widely studied ALD processes are for the deposition of binary metal oxides (e.g., Al_2O_3, HfO_2, ZnO, etc.) grown using two precursors, a metal precursors and an oxidant (e.g. water, hydrogen peroxide, ozone, or oxygen plasma). In these binary processes, the substrate is first exposed to a dose of the metal precursor that reacts with functional groups on the substrate's surface and is then pumped out of the chamber. Next, a dose of the oxidant is injected into the chamber completing one cycle of ALD. One cycle is illustrated in Figure 1.4. The self-limiting nature of this process allows for precise, sub-nm, control of the film thickness. Multiple binary processes can be combined into a supercycle, illustrated in Figure 2.1, to deposit higher order oxides with the desired composition.[42], [72], [73]

ALD has been used previously to deposit a-IGZO,[43], [44] IZTO,[45], [46] or IGZTO[47] as active layers in high-performance TFTs. The processes used for these quaternary or quinary metal oxide alloys are more complex than the ZTO ternary process and contain indium. The majority of previous reports on ALD deposited indium-free ternary ZTO focus on the material properties,[48]–[55] with only two previous reports describing TFTs with ALD deposited active layers.[28], [29] Both of the reports on TFTs only explored using H_2O_2 as the oxidant and the resulting as-deposited devices were highly conductive (always on) requiring anneals at 350ºC, or above, to achieve field-effect mobility greater than 11 $cm^2V^{-1}s^{-1}$ making the process incompatible with most flexible substrates and the μ_{FE} too low for BEOL applications. [28], [29] After annealing, they observed a transition from conducting to semiconducting behavior which they attributed to a measured decrease in oxygen vacancies.[28] They also found a low content of tin was necessary to achieve good device performance.[29]

In this chapter, three ALD processes are investigated to create as-deposited semiconducting ZTO films with low concentrations of oxygen vacancies. The first and third processes take a traditional thermal or plasma-enhanced ALD approach using H_2O or oxygen plasma as the oxidant for both metal precursors, respectively, while the second process combines these two processes to use H_2O as the oxidant for zinc-related steps and oxygen plasma for the tin-related steps within each supercycle. In this thesis, the thermal H_2O, the hybrid H_2O and plasma-enhanced, and the plasma-enhanced processes will be referred to as the "thermal," "hybrid," and "plasma" processes, respectively. In contrast with the previously reported ALD ZTO TFTs, all three deposition processes explored in this chapter result in semiconducting as-deposited behavior. The hybrid process shows an as-deposited field-effect electron mobility, μ_{FE}, as high as 13.8 $cm^2V^{-1}s^{-1}$

increasing to a record high value for an ALD ZTO process of greater than 22 $cm^2V^{-1}s^{-1}$ after annealing.

We will also explore moving beyond thermal SiO_2 as the gate insulator, in order to reduce the power consumption and enable compatibility with low-voltage CMOS and flexible substrates. While previous works have shown *SS* below the Boltzmann limit by tunneling, charge trapping [74], impact-ionization, or negative capacitance [75], these processes are not easily scaled at the BEOL or introduce unwanted instabilities. By using an *in situ* ALD gate insulator with a low density of interface defects (D_{it}), we reach an *SS* of 60 mV dec^{-1} with BEOL-compatible materials and a traditional, scalable, metal-insulator-semiconductor-field-effect-transistor (MISFET) structure. The ALD ZTO processes presented in this chapter have thermal budgets less than 450ºC enabling compatibility with BEOL and other large-area monolithic integration of thin-film electronics.

2.2 Experimental Section

2.2.1 ALD ZTO Process

All ZTO films were deposited using a flow-type ALD tool with the thermal process using a custom-built thermal ALD tool[76] and the hybrid and plasma processes using a Veeco Fiji G2 ALD tool. The binary ZnO and SnO_x used diethylzinc (DEZ; thermal: Sigma Aldrich, St. Louis, MO, ≥52 wt. % Zn Basis; plasma/hybrid: Strem Chemicals, Inc. Newburyport, MA, 95%) and tetrakis(dimethylamino)tin (TDMASn, thermal: Strem Chemical, Inc., Newburyport, MA, 99%; plasma/hybrid: Strem Chemicals, Inc., Newburyport, MA 99%) for the metal precursors, respectively. The oxidants were deionized H_2O for the thermal process and the ZnO cycles of the hybrid process and 300 W O_2 plasma for the plasma process and SnO_x cycles of the hybrid process. The binary cycles were repeated to generate ZTO films with a desired thickness and tin cycle

fraction. The thermal process used ultra-high purity Ar (GGI International, LLC, Washington, PA, 99.999%) set to a flow rate of 10 sccm during pulses for the carrier gas and during purges. The substrate temperature was set to 130ºC, 150ºC, or 200ºC.

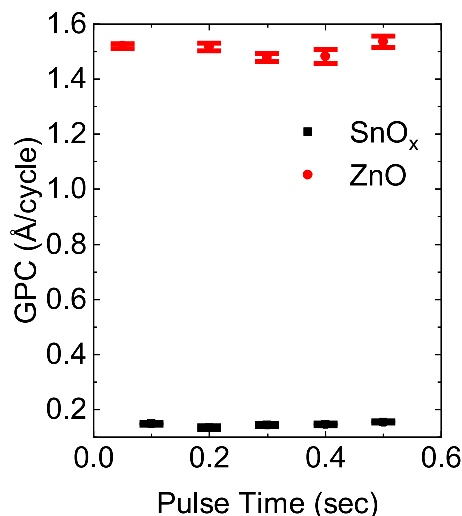


Figure 2.2: Binary saturation curves of ZnO (red) and SnO_x (black) at an ALD deposition temperature of 200ºC. Errors bars indicate uniformity across multiple samples placed in the deposition chamber during the same ALD run. Reprinted with permission reference [70].

Spectroscopic ellipsometry was used to measure the film thickness and generate the pulse length saturation curves for the thermal process DEZ and TDMASn binaries at 200ºC, Figure 2.2. For the pulse times tested, there is no significant change in the growth-per-cycle (GPC), indicating that the films deposited at 200ºC are within the ALD regime. We note that when the deposition temperature is increased from 150ºC to 200ºC, the GPC of the binary SnO_x is significantly reduced while the GPC of the binary ZnO only slightly reduced. This leads to a thinner ZTO film achieved at 200ºC for the same number of ALD cycles. As the deposition temperature increased, the tin composition stayed around 21%, perhaps due to increased suppression of ZnO growth within the ternary oxide under these deposition conditions. The specific details about the growth conditions used for these tests can be found in Table 2.1.

Table 2.1: Growth conditions used for the ZnO and SnO_x steps within the thermal ALD process. The binary GPC were measured by ellipsometry for films deposited at 200ºC. Reprinted with permission from reference [70].

Element	Precursor	Source Temp.	Pulse Time [sec]	Purge Time [sec]	Binary GPC [Å $cycle^{-1}$]
Zn	Diethylzinc (DEZ)	20 ºC	0.05	30	1.59
Sn	tetrakis(dimethylamino)tin (TDMASn)	65 ºC	0.2	30	0.15

2.2.2 Device Fabrication – Common Gate

Heavily doped n^+ silicon was used as the substrate and gate electrode for all common gate TFTs in this chapter. The gate insulator is either 100 nm thermally grown SiO_2 or approximately 30 nm of Al_2O_3 deposited using ALD. The ALD Al_2O_3 process used trimethylaluminum (TMA; Strem Chemical, Inc., Newburyport, MA, 99%) as the metal precursor in an O_2 plasma-based based ALD process at 150ºC in an Oxford OpAL ALD system. ZTO deposited using the processes described above was patterned by wet etching for device isolation. Annealed devices were placed on a hotplate at 300ºC, 400ºC, or 500ºC for one hour in a custom-built moisture-controlled glovebox flowing compressed air with humidity less than 20% RH.[77] Source and drain contacts were made by sputtering approximately 100 nm of molybdenum and patterned by lift-off.[78]

2.2.3 Device Fabrication – Separated Gate

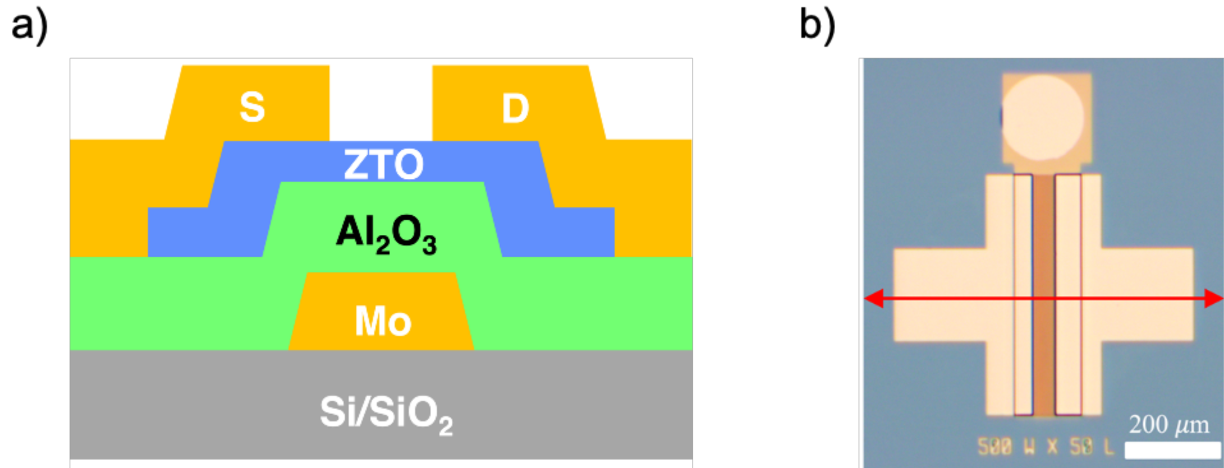


Figure 2.3 a) Schematic cross section of bottom-gate top-contact MISFET. b) Top-down microscope image of fabricated device. Red-line indicates cutline for cross section in a). From [79].

Bottom-gate, top-contact MISFETs with channel width (W) and length (L) of 520 and 50 µm, respectively, were fabricated with a cross-section shown schematically in Figure 2.3a. To create the patterned gate electrode, approximately 100 nm molybdenum was sputtered onto a silicon substrate with 100 nm thermally-grown SiO_2. The Mo was then etched using XeF_2. Then, approximately 35 nm Al_2O_3 was deposited for the gate insulator using an O_3-based ALD process at 200ºC. Without breaking vacuum, approximately 11 nm of ZTO with a Sn content of 21 at. % was deposited by ALD at 200ºC using a hybrid thermal and O_2-plasma based process for the active layer [70]. The ZTO was then wet-etched for device isolation before being annealed for one hour at 400ºC in air with relative humidity $< 20\%$. Next, the gate insulator was wet-etched to allow probing of the gate electrode. Finally, approximately 100 nm of molybdenum was deposited by sputtering and patterned by lift-off to form the source and drain electrodes (Figure 2.3b).

2.2.4 Materials Characterization

The thickness of ALD thin films on Si (100) substrates was measured using ellipsometry (J. A. Woollam M-2000) and a Cauchy model (wavelength range: 400 – 1600 nm).The crystallinity

of ZTO films was analyzed using GIXRD (Rigaku Smartlab X-ray Diffractometer) at a grazing incidence of 1º for 2θ from 20º to 70º. XPS was performed using a Kratos Axis Ultra XPS with settings described in reference [70]. The XPS curves were analyzed using CasaXPS software where each peak was fit using a Gaussian-Lorentzian curve with a full-width half max less than two and a linear background. The ZTO film composition was analyzed by integrating the area under the Zn $2p_{3/2}$ (near 1021.8 eV), Sn $3d_{5/2}$ (near 486.2 eV), and O 1s peaks with relative sensitivity factors of 3.726, 4.725, 0.780, and 0.287, respectively. Ar sputtering was used for depth profiling as described in reference [70]. Film density was measured using XRR (Rigaku Smartlab) as described in reference [70] and analyzed using GlobalFit 2 Rigaku software version 2.0.10.0.

2.2.5 Electrical Measurements

Electrical measurements were taken using 3 PLC integration with continuous voltage sweeps in the dark at room temperature using a Keysight B1505A with a noise floor of several pA. Forward *I*-*V* curves, sweeping V_{GS} negative to positive, were taken first immediately followed by reverse *I*-*V* sweeps, sweeping V_{GS} positive to negative. During I_D-V_{GS} measurements three forward and reverse sweeps were measured consecutively and the third sweep is reported in this chapter. The gate current for devices with 100 nm thermal SiO_2 is less than 100 pA, Figure 2.10. The mobility was extracted using a gate voltage range of 27 V to 30 V with V_{DS} = 1 V and the procedure outlined in reference [70]. Unless otherwise specified, all device parameters and *I*-*V* curves were taken with V_{DS} = 1 V. Only positive I_D is plotted therefore any data points which appear missing or below the co-ordinate axis are due to current flowing out of the drain. Hysteresis is measured as the difference between V_{GS} of the forward and reverse sweep required to achieve 100 nA I_D at 1 V V_{DS}, sub-threshold slope, *SS*, is the inverse of the logarithmic rate of device current turn-on,

and the turn-on voltage, V_{ON}, is defined as the value of V_{GS} where the subthreshold slope is minimum.

2.3 ALD Growth of Zinc Tin Oxide

As described in Section 2.2.1, the ZTO ALD processes used in this chapter use diethylzinc (DEZ) and tetrakis(dimethylamino)tin (TDMASn) as the metal precursors for the ZnO and SnO_x binary cycles, respectively. The ternary ZTO deposition process combines these binary cycles and can be characterized using the tin cycle fraction, f_{Sn}, defined as the total number of metal precursors steps within one supercycle that use the tin precursor. The tin composition, c_{Sn}, is usually lower than f_{Sn} for ALD ZTO because the SnO_x cycles deposit fewer atoms than the ZnO cycles.[48], [50], [51], [53], [55] As reported throughout the literature, the composition and cycle fraction of ALD ZTO are also not linearly related, with the net ternary growth-per-cycle (GPC) reduced compared to what would be expected from the binary constituents. The non-linearity is caused by a recued ZnO GPC when deposited after a SnO_x cycle and is attributed to suppression of ZnO nucleation and growth on SnO_x surfaces.[51], [53], [54]

Suppressed growth of one ALD material on another is seen in other ALD processes and one strategy to overcome this is a nanolaminate approach where discrete binary oxide layers are deposited resulting in f_{Sn} becoming dependent on the relative thickness of each binary oxide. Annealing can be used to drive interdiffusion of the nanolaminate films,[73], [80] but this process can cause the formation of unwanted discrete ZnO and SnO_x inclusions in a ternary ALD ZTO process.[53] A tailored supercycle strategy minimizing the number of sequential binary cycles is used in this chapter as an alternative to the nanolaminate process to create a well-mixed amorphous and homogenous film by minimizing differences caused by the suppression of ZnO growth.[81] Within this supercycle approach, we used sub-supercycles with low f_{Sn} as schematically illustrated

in Figure 2.1 with the goal of achieving a solid solution of amorphous ZTO through atomic-level intermixing.

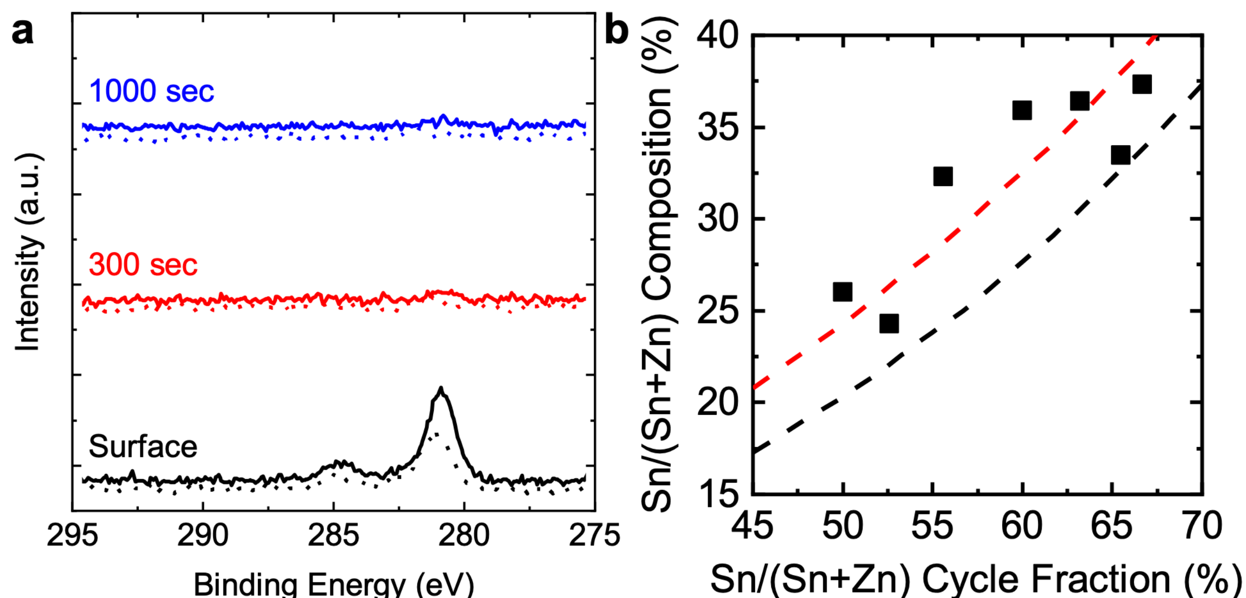


Figure 2.4: a) C 1s XPS core scans of 21% tin composition films deposited at 200ºC using thermal ALD. Scans were taken at the surface and after Ar sputtering of various duration to measure film properties. Both as-deposited (solid lines) and 500ºC annealed films (dotted lines) show carbon at the film surface. After 300 sec of sputtering, the amount of carbon is below the detection limit of XPS, ~0.1 at. %. b) Tin composition, c_{Sn}, obtained from XPS taken after 200 s sputtering, as a function of tin cycle fraction, f_{Sn}, for ZTO films deposited at 150 ºC using the thermal ALD process. Experimental data is shown in symbols. The dashed lines indicate fits using the rule of mixtures (Equation (2.1)) (black dashed line) and with a reduced ZnO growth rate of 1.27 Å/cycle (red dashed line). Adapted with permission from reference [70].

X-ray photoelectron spectroscopy (XPS) was used to analyze purity and composition of resulting ZTO thin films. Adventitious surface carbon was removed using Ar sputtering and then C 1s core scans were taken revealing the bulk films are free of carbon impurities within ~0.1 at. %, the XPS detection limit, Figure 2.4a. Cores scans of the Zn $2p_{3/2}$ and Sn $3d_{5/2}$ levels were used for compositional analysis of the tin composition, c_{Sn}, as a function of f_{Sn} where c_{Sn} was varied from 20% to 40% by varying f_{Sn} from 45% to 67%, as this range results in optimal semiconductor properties for several ZTO deposition techniques.[29], [36], [82] Figure 2.4b compares the results of the compositional analysis (black squares) for the thermal films deposited at 150ºC to the rule of mixtures (black dashed line) given by Equation (2.1):[50]

$$c_{Sn} = \frac{n_{SnO_2}\frac{\rho_{SnO_2} r_{SnO_2}}{M_{SnO_2}}}{n_{SnO_2}\frac{\rho_{SnO_2} r_{SnO_2}}{M_{SnO_2}} + n_{ZnO}\frac{\rho_{ZnO} r_{ZnO}}{M_{ZnO}}} \tag{2.1}$$

where, for SnO_2 and ZnO, the density, ρ_{SnO_2} and ρ_{ZnO}, is 6.85 g cm^{-3} and 5.6 g cm^{-3}, the molar mass, M_{SnO_2} and M_{ZnO}, is 150.7 g mol^{-1} and 81.4 g mol^{-1},[83] and the measured binary GPC of the thermal process at 150ºC, r_{SnO_2} and r_{ZnO}, is 0.6 Å $cycle^{-1}$ and 1.6 Å $cycle^{-1}$, respectively, and n represents the number of binary cycles in one supercycle. The poor fit, in agreement with previous studies,[50], [55] is a result of the reduced ZnO growth after SnO_x cycles where approximately 6 cycles of ZnO is required to achieve the binary GPC.[51] As the supercycle design approach used in this chapter only has one or two ZnO cycles in a row, r_{ZnO} can be reduced to the GPC of ZnO after a SnO_x, found to be approximately 1.26 Å $cycle^{-1}$. Using the reduced r_{ZnO} in Equation (2.1) results in much closer fit to the data, red dashed curve in Figure 2.4b. Previous work with a different supercycle approach required complex equations to fit the ratios.[50] The result is a ternary ALD deposition technique that allows for precise tuning of the film composition with c_{Sn} ranging the values of interest for active electronic devices.

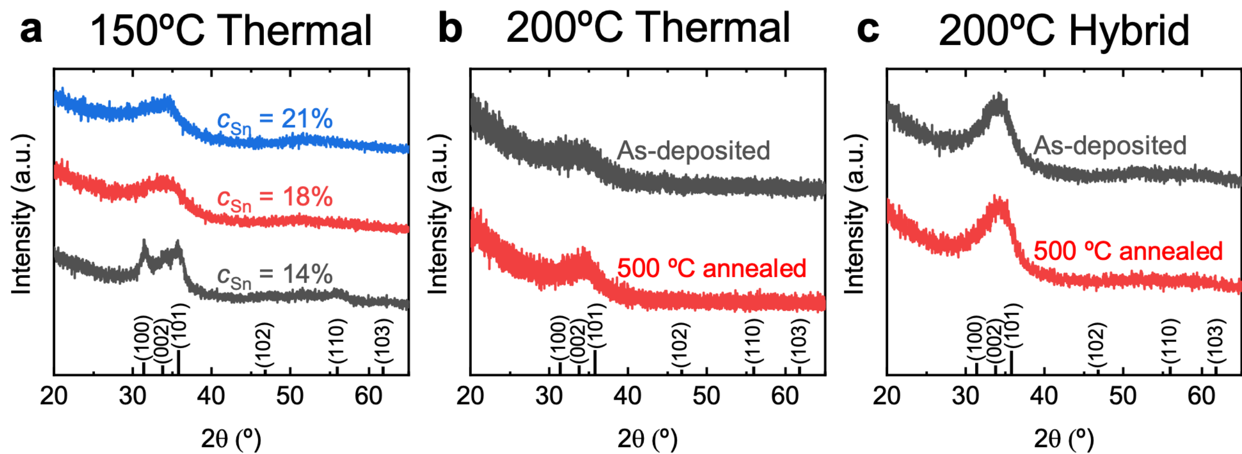


Figure 2.5: GIXRD patterns of ALD ZTO: deposited using a) and b) the thermal or c) the hybrid process at a) 150ºC or b) and c) 200ºC for a) as-deposited films with various tin composition or b) and c) 45% tin cycle fraction as-deposited and annealed at 500ºC. ZnO peak positions (JCPDS No. 36-1451) are shown at the bottom. Adapted with permission from reference [70].

Grazing incidence x-ray diffraction (GIXRD) was used to verify the amorphous phase of the ALD deposited ZTO films. As-deposited films deposited using the thermal process at 150ºC with c_{Sn} of 18% and 21% (f_{Sn} of 33% and 45%, respectively) are x-ray amorphous, Figure 2.5a, showing only a single broad peak centered around 2θ of 35º. The broad peak encompasses the hexagonal wurtzite ZnO peaks at 2θ of 31.8º (100), 34.4º (002), and 36.3º (101)[84] and has been observed previously in other work on amorphous or mostly amorphous ZTO.[52], [85] While these ZTO films appear x-ray amorphous, small (less than 10 nm) crystallites in an amorphous matrix may be present.[52] As zinc content increases (c_{Sn} and f_{Sn} of 14% and 25%, respectively) multiple distinct crystalline peaks are present in the broad peak indicating the formation of larger nanocrystallites. Figure 2.5b and Figure 2.5c show the GIXRD patterns for 45% f_{Sn} films before and after post-deposition annealing for the thermal and hybrid processes, respectively. These films are amorphous as-deposited and remain amorphous after the 500ºC anneal as expected because the crystallization temperature of ZTO is typically greater than 600ºC,[85], [86] much higher than that of the binary components. The GIXRD results indicate the sub-supercycle approach used in this chapter results in successful atomic-level intermixing of zinc and tin within an amorphous metal oxide matrix when c_{Sn} is greater than 14%.

2.4 Electrical Properties of Common Gate ALD ZTO Thin-Film Transistors

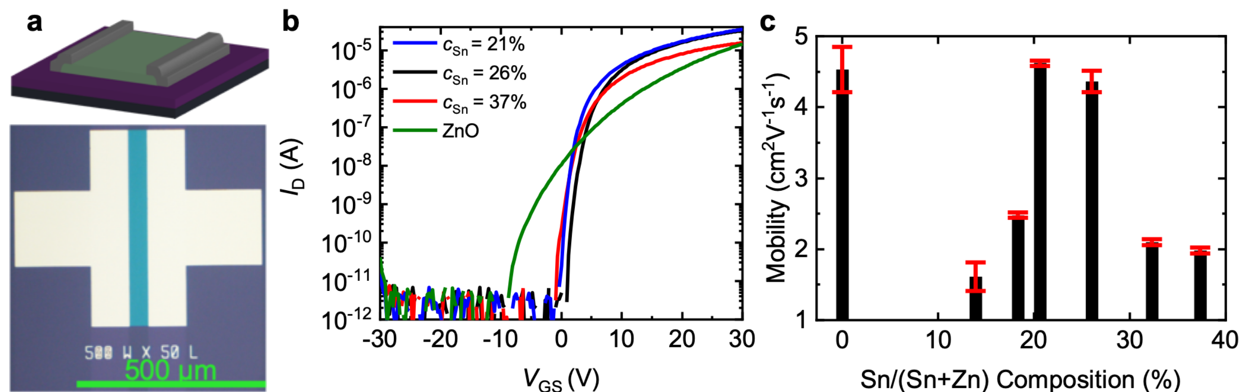


Figure 2.6: a) Top: Schematic illustration of a TFT and bottom: top-down microscope image of a fabricated device. b) Transfer curves of thermal films deposited at 150ºC annealed at 500ºC. All TFTs have W/L of 10 and V_{DS} = 1 V. The legend indicates the tin composition obtained by XPS. c) Field effect mobility as a function of tin composition, extracted from the transfer curves shown in (b) and in reference [70]. Error bars indicate standard deviation based on measurement of at least four different transistors for each composition. Reprinted with permission from reference [70].

To achieve high-mobility semiconducting ALD ZTO films, we first optimized the tin composition by depositing films with various tin cycle fractions using the thermal process at 150ºC with a 500ºC post-deposition anneal in air. We also created ZnO, c_{Sn} = 0%, films for comparison using the binary thermal ALD process. These films were used as the active layer in bottom gate, top contact transistors as shown in Figure 2.6a with corresponding transfer curves found in Figure 2.6b and reference [70] and extracted mobility in Figure 2.6c. For the ZTO films, the highest field-effect mobility, μ_{FE}, was observed for a tin composition of 21% with lower mobility values observed with lower or higher tin composition fractions in agreement with prior results using other ZTO deposition methods.[36], [82] The observed mobility roll off at low tin composition fractions is likely due to the formation of ZnO nanocrystallites, consistent with the XRD observations in Figure 2.5a.[23] At higher c_{sn}, ZTO has been shown to crystallize into a rutile, SnO_2-like structure where Zn may occupy the Sn site and act as an acceptor or electron-trap, reducing electron mobility.[87] While binary ZnO has a reasonably high mobility, the mobility of ZnO TFTs has a

larger device-to-device variation and a larger subthreshold slope, *SS*, of 2.15 V dec^{-1} compared to the ZTO *SS* of 0.57 V dec^{-1} for c_{Sn} = 21%.

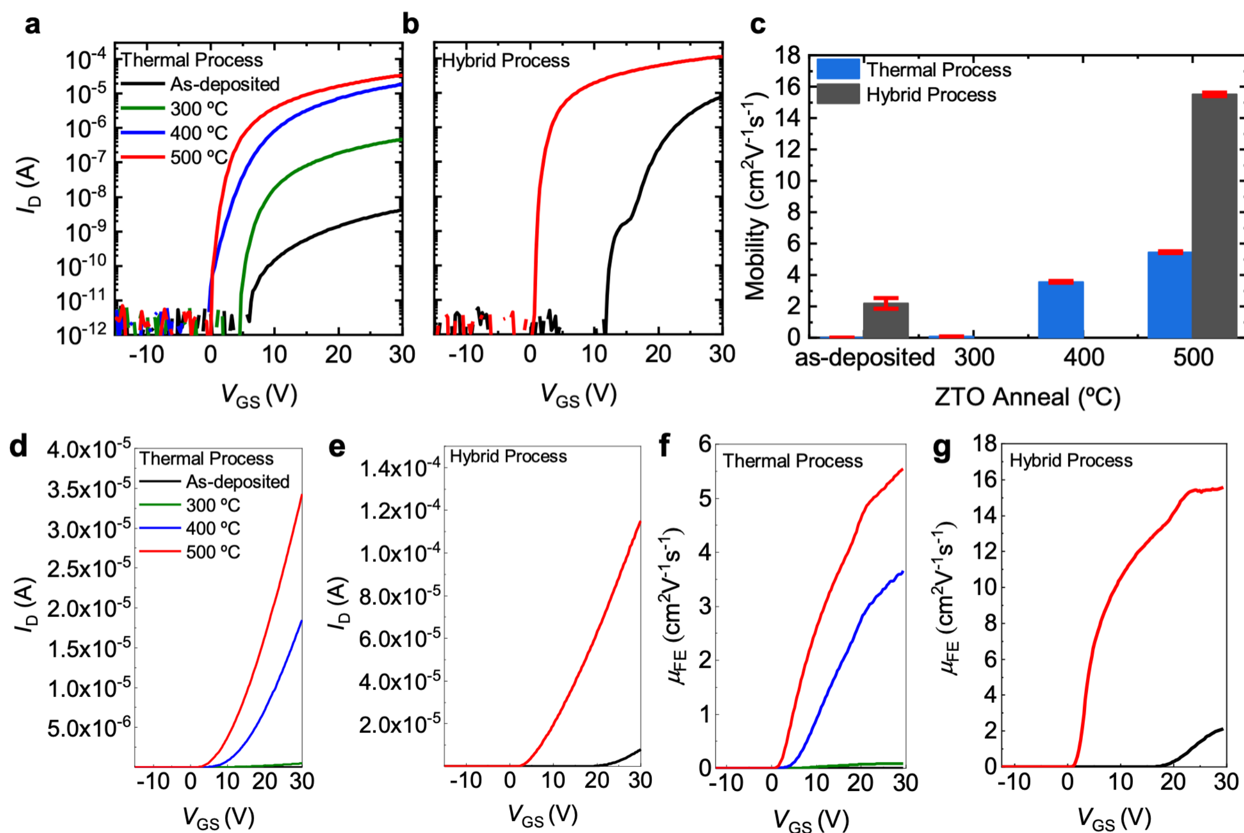


Figure 2.7: Transfer curves of ALD ZTO TFTs deposited at 150ºC with f_{Sn} = 45% versus post-deposition anneal temperature in a,b) semi-log and d,e) linear scale for ZTO deposited using a,d) thermal process; and b,e) the hybrid process. c) Field effect mobility as a function of anneal temperature, extracted from 27 V < V_{GS} < 30 V in (f) and (g). Error bars indicate standard deviation from measurement of at least five different transistors for each condition. f,g) Field-effect mobility extracted from the transfer curves. All TFTs have W/L of 10 and V_{DS} = 1 V. The 500ºC curve in (a) is the same as the 21% c_{Sn} curve in Figure 2.6b. Adapted with permission from reference [70].

Next, the impact of the oxidant used during the ALD process was studied by comparing as-deposited performance of TFTs with ZTO active layers deposited using the thermal and hybrid ALD processes at 150ºC with f_{Sn} = 45%, found to yield c_{Sn} = 21% above. Transfer curves and effective mobility are shown in Figure 2.7 and extracted device parameters are reported in Table 2.2. TFTs fabricated using both ALD processes exhibit as-deposited semiconductor field-effect behavior and operate as enhancement mode devices with turn-on voltages, V_{ON}, above 0 V. In

contrast, a prior report on ALD ZTO TFTs made with H_2O_2 as an oxidant showed conducting behavior,[28] similar to previous results on ALD SnO_x,[88] due to a high concentration of oxygen vacancies. The extracted electron mobility achieved in as-deposited hybrid ALD films is 2.19 $cm^2V^{-1}s^{-1}$, much higher than the thermal process mobility of 9.90×10^{-4} $cm^2V^{-1}s^{-1}$. Nonetheless, ALD ZTO TFTs made with as-deposited hybrid films deposited at 150ºC exhibit a large positive turn-on voltage, a kink in sub-threshold I_D, and a large *SS* all indicative of a large number of defects or trap states in the ZTO active layer.[89] The physical origin of these states, and the reason for the improved mobility of the hybrid process, are discussed below.

Table 2.2: Electrical properties of ALD ZTO TFTs discussed in this chapter. The corresponding *I-V* curves are shown in Figure 2.7 and Figure 2.9. The ZTO layers were deposited with f_{Sn} = 45%. Reprinted with permission from reference [70].

ALD Type (Deposition Temperature)	Post-Deposition Anneal Temperature	μ_{FE} [$cm^2V^{-1}s^{-1}$]	SS [V dec^{-1}]	ΔV_C [V]	V_{ON} [V]
Thermal (150 ºC)	As-deposited	9.90×10^{-4}	2.2	N/A	7.4
Thermal (150 ºC)	300 ºC	8.76×10^{-2}	0.89	4.6	5.4
Thermal (150 ºC)	400 ºC	3.54	1.2	1.3	1.1
Thermal (150 ºC)	500 ºC	5.44	0.57	0.89	0.54
Hybrid (150 ºC)	As-deposited	2.19	0.68	3.1	10
Hybrid (150 ºC)	500 ºC	15.5	0.29	0.87	0.66
Thermal (200 ºC)	As-deposited	9.56×10^{-5}	4.6	N/A	23
Thermal (200 ºC)	400 ºC	16.1	0.37	1.7	3.1
Thermal (200 ºC)	500 ºC	17.5	0.30	1.1	1.8
Hybrid (200 ºC)	As-deposited	13.8	0.43	3.4	4.6
Hybrid (200 ºC)	300 ºC	18.8	0.31	1.4	2.3
Hybrid (200 ºC)	400 ºC	22.1	0.29	0.95	1.1
Hybrid (200 ºC)	500 ºC	22.0	0.28	0.53	-0.78

Post-deposition anneals were performed on the ZTO layer before applying metal contacts to improve the electrical properties of the films. Anneals performed in air at 300ºC, 400ºC, and

500ºC increased the field-effect mobility, decreased the sub-threshold slope, and shifted the V_{ON} value towards zero volts for both thermal and hybrid ALD films. The plot in Figure 2.5c and data in Table 2.2 show that the higher the annealing temperature, the greater the performance improvements. The mobility of the thermal ALD ZTO dramatically increases from 9.90×10^{-4} $cm^2V^{-1}s^{-1}$ for as-deposited films to 5.44 $cm^2V^{-1}s^{-1}$ after a 500ºC anneal and the TFTs made using the hybrid ALD ZTO annealed at 500ºC exhibit a mobility of 15.5 $cm^2V^{-1}s^{-1}$, greater than any previously reported value for ALD ZTO, Table 2.3. Both thermal and hybrid ALD ZTO TFTs show a turn-on voltage and hysteresis less than 1 V, with subthreshold swings of 0.57 and 0.29 V dec^{-1}, respectively, after a 500ºC anneal. The subthreshold swings are above the Boltzmann limit, 60 mV dec^{-1} at room temperature, due to charge traps at or near the dielectric-semiconductor interface.[90] Thus, the more rapid turn-on with increased anneal temperature is due to a reduction of interface charge trap density.

Table 2.3: Comparison of previously published ALD ZTO TFTs with those reported in this chapter. Reprinted with permission from reference [70].

ALD Deposition Temperature	ALD Oxidant	Anneal Temperature	Tin composition	μ_{FE} [$cm^2V^{-1}s^{-1}$]	*SS* [V dec^{-1}]	Ref.
200 ºC	**Hybrid**	**None**	**21%**	**13.8 d)**	**0.43**	**This Work**
170 ºC	Thermal (H_2O_2)	250 ºC	20%	9-10 a)	0.97	[29]
200 ºC	**Hybrid**	**300 ºC**	**21%**	**18.8 d)**	**0.31**	**This Work**
170 ºC	Thermal (H_2O_2)	350 ºC	20%	11-12 a)	0.27	[29]
150 ºC	Thermal (H_2O_2)	400 ºC	50% b)	13.2 c)	0.15	[28]
200 ºC	**Thermal (H_2O)**	**400 ºC**	**21%**	**16.1 d)**	**0.37**	**This Work**
200 ºC	**Hybrid**	**400 ºC**	**21%**	**22.1 d)**	**0.29**	**This Work**
170 ºC	Thermal (H_2O_2)	450 ºC	20%	12-13 a)	0.27	[29]
170 ºC	Thermal (H_2O_2)	450 ºC	18%	12-13 a)	?	[29]
170 ºC	Thermal (H_2O_2)	450 ºC	23%	12-13 a)	?	[29]
170 ºC	Thermal (H_2O_2)	450 ºC	31%	10 a)	?	[29]
170 ºC	Thermal (H_2O_2)	450 ºC	53%	5 a)	?	[29]
120 ºC	Thermal (H_2O_2)	450 ºC	18%	3.4 a)	?	[29]
120 ºC	Thermal (H_2O_2)	450 ºC	23%	2.5 a)	?	[29]
120 ºC	Thermal (H_2O_2)	450 ºC	31%	1.5 a)	?	[29]
120 ºC	Thermal (H_2O_2)	450 ºC	53%	1.75 a)	?	[29]
150 ºC	**Hybrid**	**500 ºC**	**45% b)**	**15.5d)**	**0.29**	**This Work**
150 ºC	Thermal (H_2O_2)	500 ºC	50% b)	4.8 c)	0.27	[28]
200ºC	**Thermal (H_2O)**	**500 ºC**	**21%**	**17.5 d)**	**0.30**	**This Work**
200ºC	**O_2 Plasma**	**500 ºC**	**45% b)**	**22.7 d)**	**0.36**	**This Work**
200 ºC	**Hybrid**	**500 ºC**	**21%**	**22.0 d)**	**0.28**	**This Work**

a) Mobility extracted for V_{DS} = 0.1 V.
b) Tin cycle fraction reported because composition fraction was not available.
c) Mobility extracted for V_{DS} = 10 V.
d) Mobility extracted for V_{DS} = 1 V.

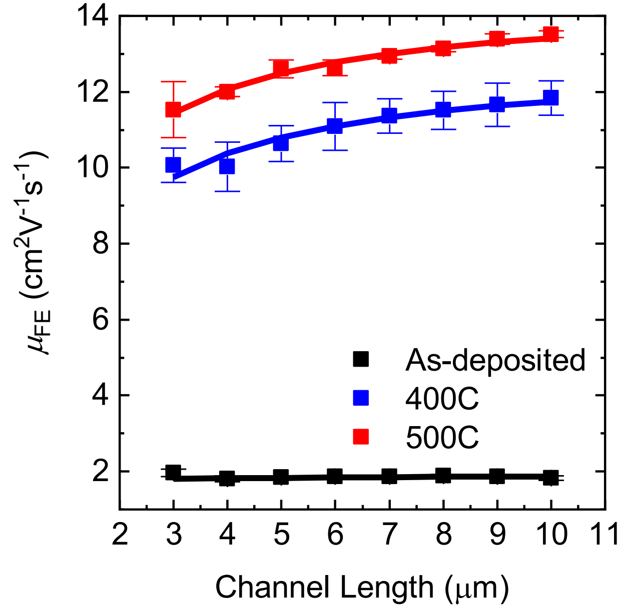


Figure 2.8: The symbols indicate the linear field-effect mobility of TFTs fabricated using the 150ºC hybrid process as a function of anneal temperature with error bars indicating the standard deviation of five measured devices. The lines indicate fits to $\mu_{FE,C}$ using equation (2.2).

The total resistance of a TFT, R_{tot}, is composed of the contact resistance, R_C, and the channel resistance that scales with channel length, $r_{ch}L$. When R_C is a significant portion of R_{tot}, the extracted field-effect mobility, $\mu_{FE,C}$, can be less than the intrinsic field-effect mobility of the channel, $\mu_{FE,0}$. The impact of R_C on μ_{FE} is given by

$$\mu_{FE,C} = \frac{\mu_{FE,0}}{1+\frac{R_C}{r_{ch}L}}.[78] \qquad (2.2)$$

To explore whether contact resistance is changing with post-deposition annealing, the mobility of 150ºC hybrid devices with different channel lengths was extracted at various anneal temperatures and then Equation (2.2) was fitted to extract R_C, Figure 2.8. The fitted width normalized R_C value for all three anneal conditions is approximately 4 Ω cm indicating that improved contact resistance is not the cause for improved performance with increased post-deposition anneal temperature.

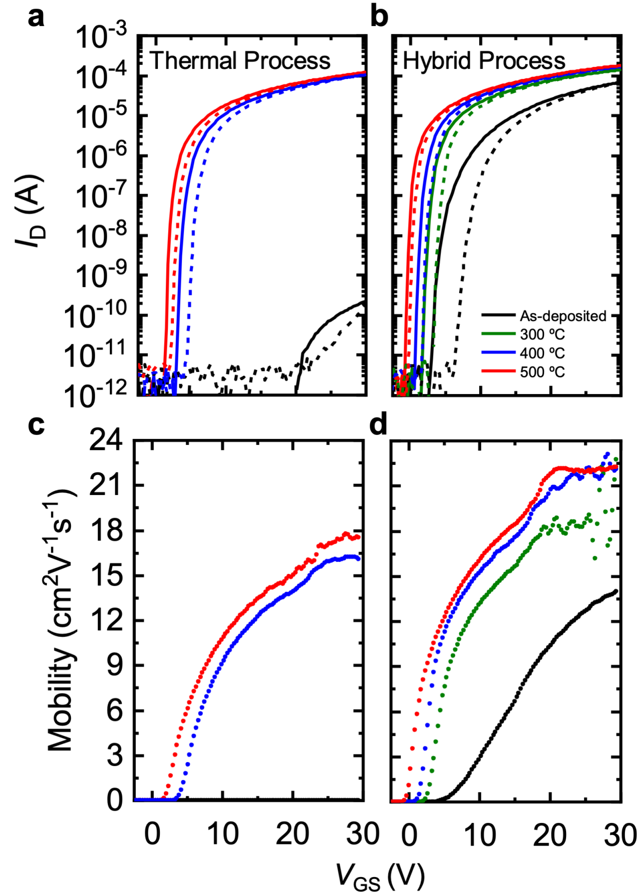


Figure 2.9: a,b) Transfer curves of ALD ZTO TFTs made with 21% tin composition films deposited at 200ºC with various post-deposition anneal temperatures. Forward *I-V* curves are indicated by solid lines and reverse curves are indicated by dashed lines. c,d) Effective mobility extracted from the forward *I-V* curves. TFTs shown in a,c) were made using the thermal ALD ZTO process while those in b,d) used the hybrid ALD process. For all TFTs, W/L = 10 and V_{DS} = 1 V. Reprinted with permission from reference [70].

The performance of the ALD ZTO films was further improved by increasing the deposition temperature to 200ºC. Transfer curves for TFTs fabricated using the thermal and hybrid processes at a deposition temperature of 200ºC are shown in Figure 2.9 with extracted transistor parameters in Table 2.2. The hybrid ALD process at 200ºC results in excellent as-deposited TFT properties: a mobility of 13.8 $cm^2V^{-1}s^{-1}$ and sub-threshold slope of 0.43 V dec^{-1}. In contrast, TFTs measured with ZTO active layers deposited using the thermal process showed a ~10 × decrease in mobility to 9.56×10^{-5} $cm^2V^{-1}s^{-1}$ when the deposition temperature is increased from 150ºC to 200ºC. As with the films deposited at 150ºC, both the thermal and hybrid ALD ZTO deposited at 200ºC show

improvement after post-deposition annealing. The best TFT performance is observed for the hybrid 200ºC process followed by a 500ºC anneal exhibiting a mobility of 20.0 $cm^2V^{-1}s^{-1}$ and a sub-threshold slope of 0.28 V dec^{-1}.

We should note the TFTs made with a ZTO deposition temperature of 200ºC show nearly identical behavior if annealed at 400ºC or 500ºC, Figure 2.9 and Table 2.2. With a thermal budget under 450ºC, technological compatibility of ALD ZTO with monolithic integration on silicon CMOS at the BEOL is shown.[69] For applications requiring an even lower thermal budget, for example, for integration on flexible substrates, as-deposited films made with the hybrid ALD process at 200ºC can be used.

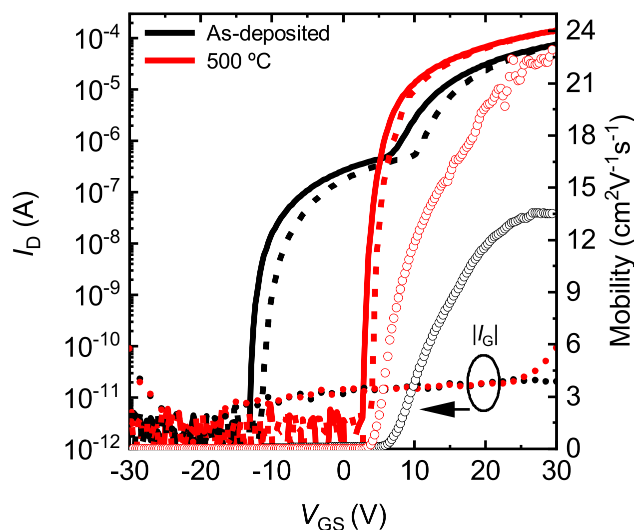


Figure 2.10: Transfer curves of f_{Sn} = 45% films deposited at 200ºC using an all-plasma process, as-deposited and after a 500ºC anneal. The forward *I-V* curves are indicated by the solid lines, the reverse curves are indicated by the dashed lines, and the $|I_G|$ is indicated using solid dots, all plotted on the left y-axis. Mobility is plotted using the open circles on the right y-axis. For both devices, W/L = 10, and V_{DS} = 1 V. Reprinted with permission from reference [70].

ZTO films were made using an all-plasma ALD process at 200ºC with f_{Sn} = 45%, and resulting transfer curves are shown in Figure 2.10, for comparison with the hybrid and thermal processes. The effective mobility of the as-deposited and 500ºC annealed plasma ALD ZTO films are 13.4 $cm^2V^{-1}s^{-1}$ and 22.7 $cm^2V^{-1}s^{-1}$, respectively, and are nearly identical to those of the hybrid

ALD ZTO process, Table 2.2. However, the as-deposited plasma ALD TFT *I-V* curves shows a kink in the sub-threshold $I_{D,}$ indicating the presence of a conduction path with low mobility and a turn-on voltage near -14 V. This second conduction path may be caused be defects created by oxygen plasma damage within the film as similar behavior has been observed following the plasma treatment of AOS films.[91], [92] The increased mobility and shift of the turn-on voltage to near zero volts following post-deposition annealing indicates that this damage is recovered and the defects are reduced during annealing.[91] Nonetheless, even after annealing, the plasma ALD ZTO films have a *SS* of 0.36 V dec^{-1}, between the values obtained for the thermal and hybrid process, and ΔV_C of 1.03 V, larger than the hysteresis of either other process. The larger sub-threshold slope and hysteresis may be caused by traps in the film or at its interfaces that cannot be completely resolved by annealing.[78] The hybrid process clearly offers the best as-deposited and annealed TFT performance.

Thus far, we have observed a dramatic improvement in ZTO electrical properties with 1) post-deposition annealing; 2) an increase of the deposition temperature from 150ºC to 200ºC; and 3) the use of the hybrid process instead of pure thermal or plasma-enhanced ALD processes. To develop a mechanistic understanding of the chemical and structural origins of these improvements, XRD, XPS, and x-ray reflectivity (XRR) measurements were performed.

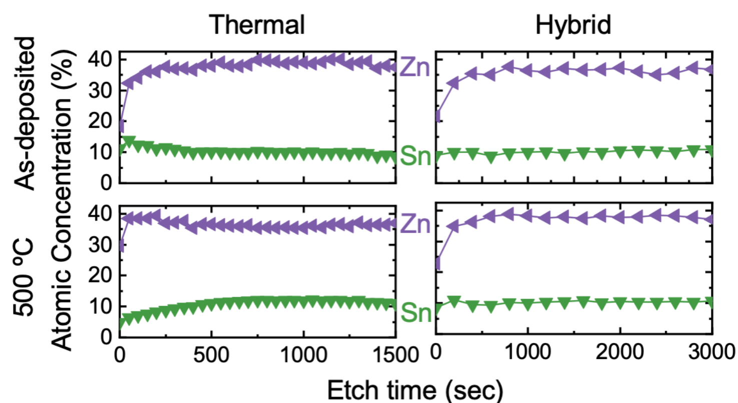


Figure 2.11: Zn and Sn concentrations as a function of sputtering time (depth), obtained by XPS for c_{Sn} = 21% ZTO films: as-deposited (top row), 500ºC annealed (bottom row), deposited at 200ºC using thermal ALD (left) and hybrid ALD (right). Reprinted with permission from reference [70].

In a previous work, improvements resulting from post-deposition annealing of ALD ZTO were attributed to a change in the local atomic arrangement within the channel layer.[29] However, in this chapter, XRD analysis shows both the thermal ALD and hybrid ALD ZTO films remain amorphous after a 500ºC anneal, Figure 2.5b and Figure 2.5c, indicating no phase change is occurring during the post-deposition anneal. Furthermore, XPS depth profiling indicates Zn and Sn concentrations are highly uniform through the bulk of the film, and the c_{Sn} values are comparable for the thermal and hybrid 200ºC processes, both before and after post-deposition annealing, Figure 2.11. Therefore, the observed increases in mobility cannot be attributed to a change in phase or bulk stoichiometry.

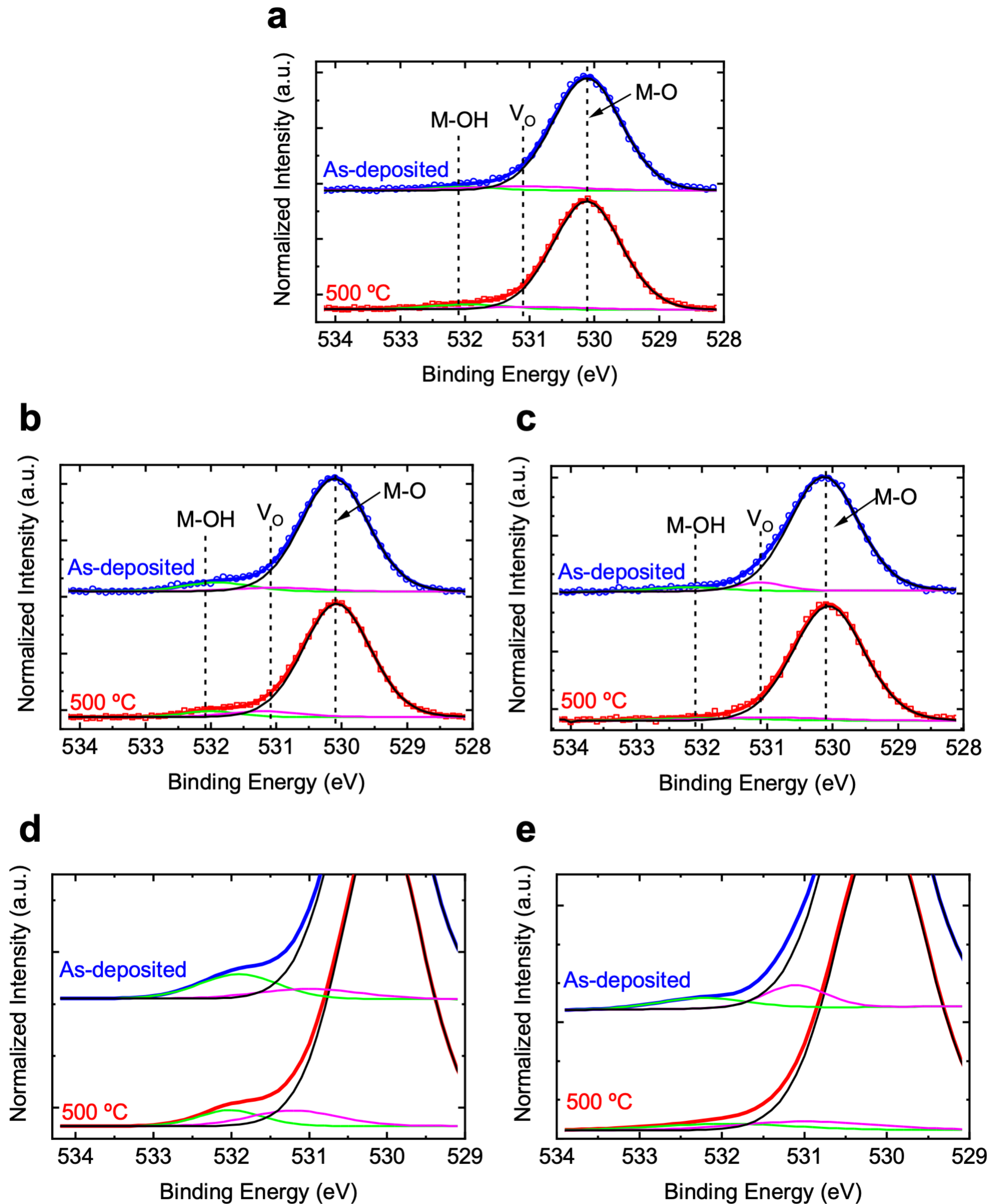


Figure 2.12: O 1s XPS spectra normalized to the M-O peak height of each film acquired after Ar sputtering of ZTO ALD films as-deposited (blue circles) and after 500ºC anneal (red squares). The solid lines indicate fits using the atomic percentages of metal-oxygen bonds (black), M-O, oxygen vacancies (pink), V_O, and metal-hydroxide bonds (green), M-OH, listed in Table 2.4. Spectra for three ZTO films are shown: a) thermal ALD at 200ºC; b) thermal ALD at 150ºC; and c) hybrid ALD at 200ºC. d) and e), zoomed in spectra showing only the Gaussian fits of b) and c), respectively. Adapted with permission from reference [70].

Another previously proposed mechanism for improvements resulting from post-deposition annealing of ALD ZTO is a decrease in oxygen vacancy defects caused by the anneal.[28] Therefore, we quantified the oxygen-related states by analyzing the oxygen O 1s XPS peak measured for several films after Ar sputtering of the surface to remove adventitious carbon. During analysis, the O 1s peak was deconvoluted into three components: (1) metal-oxide bonding (M-O) at 530.1 ± 0.1 eV; (2) oxygen-deficient regions (V_O), at 531.1 ± 0.1 eV; and (3) hydroxyls (M-OH), at 532.1 ± 0.2 eV.[93]–[96] The oxygen component peak locations are indicated by vertical dotted lines and the Gaussian fits are plotted in Figure 2.12 with Table 2.4 listing the atomic percentages of each component. For all films, the oxygen vacancy concentrations are between 3.7% and 5.4%, and do not change significantly after annealing; they remain constant within ±1.2%. Thus, a reduction in oxygen vacancies cannot explain the drastic increase in mobility observed for annealed thermal ALD ZTO films.

Table 2.4: Atomic fractions of oxygen atom components for various ALD ZTO films. The table indicates three oxygen found in three environments: (1) fully oxidized surroundings (M-O); (2) in oxygen-deficient regions (V_O); and (3) in hydroxyls (M-OH). The fractions are obtained by deconvolution of the O 1s XPS spectra shown in Figure 2.12, taken after Ar sputtering to measure bulk properties. The deconvolution procedure is described in the Section 2.2.4. Reprinted with permission from reference [70].

ALD Deposition Temperature	Anneal Temperature	ALD Oxidant	M-O [%]	M-OH [%]	V_O [%]
150ºC	As-deposited	Thermal (H_2O)	89.4	6.9	3.7
150ºC	500ºC	Thermal (H_2O)	91.4	3.7	4.9
200ºC	As-deposited	Thermal (H_2O)	92.1	2.5	5.4
200ºC	500ºC	Thermal (H_2O)	92.9	3.5	4.6
200ºC	As-deposited	Hybrid	91.9	3.3	4.8
200ºC	500ºC	Hybrid	92.9	3.0	4.1

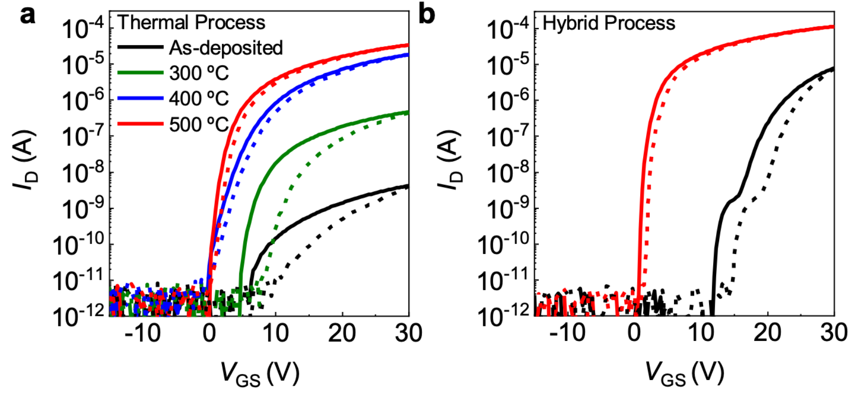


Figure 2.13: Transfer curves of ALD ZTO TFTs with f_{Sn} = 45% at 150ºC as a function of post-deposition anneal temperature for a) ZTO deposited using the thermal ALD process; and b) ZTO deposited using the hybrid ALD process. All TFTs have W/L of 10 and V_{DS} = 1 V. The forward *I-V* curves are indicated by solid lines, and are identical to those shown in Figure 2.7a and Figure 2.7b. The reverse *I-V* curves are indicated by dashed lines. The hysteresis (ΔV_C) between the forward and reverse sweeps, caused by either traps in the bulk ZTO film or by reactions at the back interface of the film,[97] is tabulated in Table 2.2. Reprinted with permission from reference [70].

The as-deposited 150ºC thermal films show a much higher hydroxyl concentration, compared to the 200ºC as-deposited films, Table 2.4. We attribute this difference to a more complete dehydrogenation of surface functional groups during the ligand-exchange reactions at elevated deposition temperatures.[98] Electrically, the as-deposited 150ºC thermal ALD films exhibited large V_{ON}, comparatively low mobility, and large hysteresis, but these undesired features are eliminated or reduced after annealing at 500ºC, Table 2.2 and Figure 2.13. The improved performance after annealing is caused by a decrease in the hydroxyl concentration, which contribute defect states that act as electron traps,[77] in the films and a corresponding increase in the M-O concentration, Table 2.4. By post-deposition annealing, the M-OH concentration in the ALD ZTO films is reduced and TFT behavior improves.

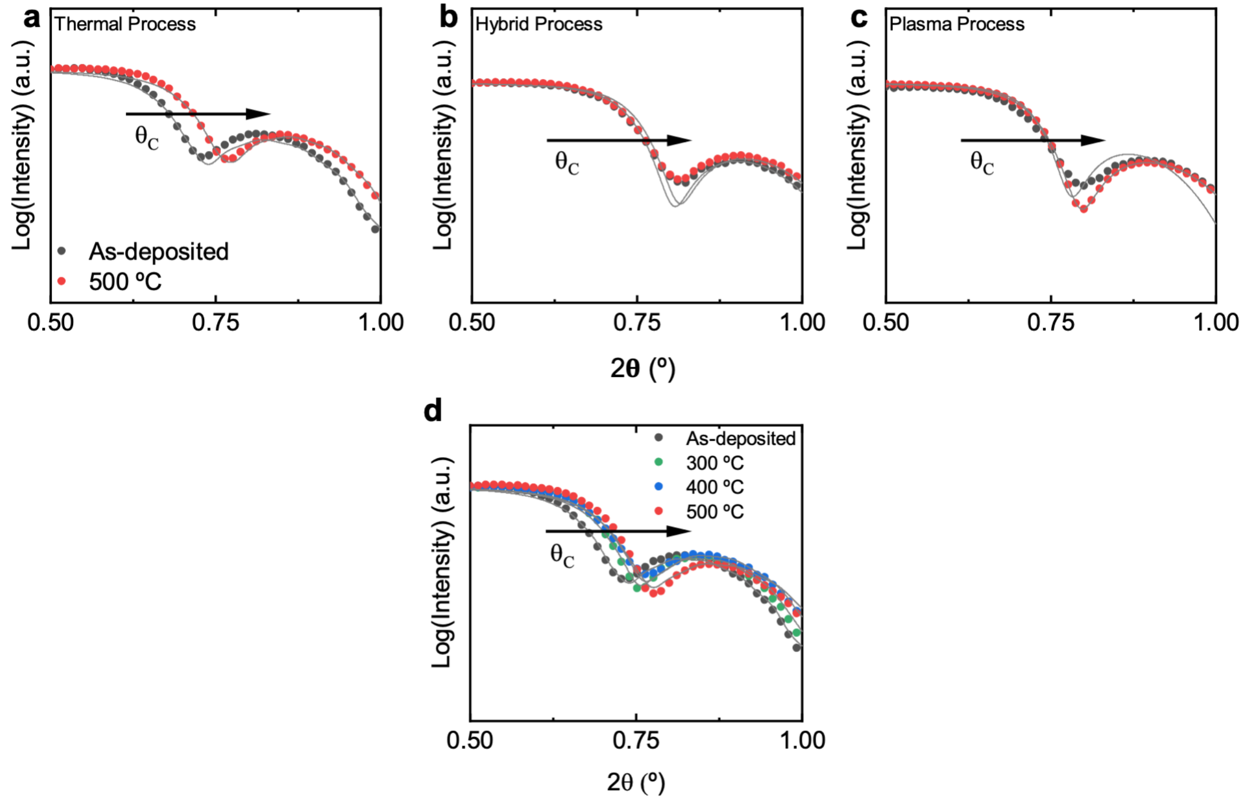


Figure 2.14: Normalized XRR of f_{Sn} = 45% ZTO films deposited: (a,b,c) at 200ºC using the (a) thermal, (b) hybrid, or (c) all-plasma ALD process. XRR spectra are shown for as-deposited films and films annealed at 500ºC; (d) at 150ºC using the thermal ALD process, comparing as-deposited films to those annealed at various temperatures. In all plots, open circles are measured data and lines are simulated fits. The critical angle shifts right as anneal temperature increases, indicating an increase in density. The fit values of ZTO density can be found in Table 2.5. Adapted with permission from reference [70].

A decrease in M-OH concentration (Table 2.4) cannot, however, explain the higher mobility observed for the hybrid 200ºC ALD ZTO films compared to those deposited using a thermal process. Therefore, an additional factor must be contributing to the dependence of mobility on the oxidizing species in the ALD process. Prior work on sputtered ZTO showed the mobility of the ZTO films increased upon densification.[99] XRR was performed on several ALD ZTO samples to assess film density, Table 2.5 and Figure 2.14. The density extracted from the XRR spectra revealed the density of the 200ºC thermal ALD ZTO film increased from 5.1 g cm^{-3}, as-deposited, to 5.9 g cm^{-3}, after annealing at 500ºC. Ellipsometry measurements confirmed the XRR results by showing the thermal ALD ZTO film thickness decreased from 9.9 nm to 8.8 nm upon

500ºC annealing. Similarly, the density of the thermal ALD ZTO film deposited at 150ºC showed an increase in density from 5.0 g cm^{-3}, as-deposited, to 5.7 g cm^{-3}, after annealing at 500ºC. Clearly, both increasing the ALD deposition temperature and/or adding a post-deposition anneal induce an increase in film density correlating with the observed increase in electron mobility.

Table 2.5: ZTO density for films with f_{Sn} = 45% determined by fitting the XRR spectra shown in Figure 2.14. The fitting method is described in the note below. For comparison, note the density of SnO_2 is 6.85 g cm^{-3} and the density of ZnO is 5.6 g cm^{-3},[83] and a previous study on ALD ZTO using H_2O_2 as the oxidant reported ZTO density of 5.3 g cm^{-3}.[29] Reprinted with permission from reference [70].

ALD Deposition Temperature	ALD Process	Anneal Temperature	ZTO Density [g cm^{-3}]	% Change after Annealing
150 ºC	Thermal	As-deposited	5.0	
150 ºC	Thermal	300 ºC	5.4	8.0 %
150 ºC	Thermal	400 ºC	5.6	12.0 %
150 ºC	Thermal	500 ºC	5.7	14.0 %
200 ºC	Thermal	As-deposited	5.1	
200 ºC	Thermal	500 ºC	5.9	15.7 %
200 ºC	Hybrid	As-deposited	6.3	
200 ºC	Hybrid	500 ºC	6.5	3.2 %
200 ºC	Plasma	As-deposited	6.0	
200 ºC	Plasma	500 ºC	6.1	1.7 %

Note: To obtain ZTO density by XRR, we deposited ZTO on top of 100-nm thermally-grown SiO_2. We measured the thickness of SiO_2 by ellipsometry before ZTO deposition and measured the ZTO thickness after ZTO deposition and again after annealing. The thin-film structure was then entered in the GlobalFit XRR software. The density of Si and SiO_2 were held fixed at the default values in the GlobalFit library. The initial density of the ZTO film was calculated based on the XPS atomic composition measurements. The experimental XRR data was then fit to determine the ZTO thickness and density.

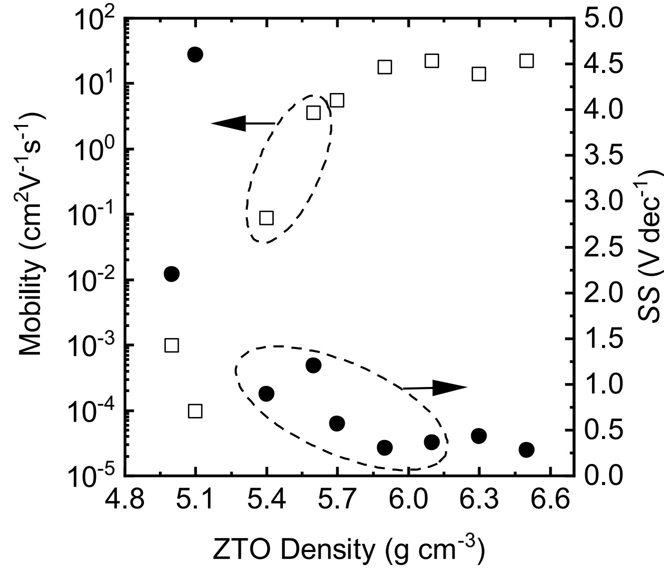


Figure 2.15: ALD ZTO TFT mobility (open squares) and sub-threshold slope (closed circles) plotted against ZTO density as measured by XRR. The numerical data can be found in Table 2.2, Table 2.3, and Table 2.5. The mobility correlates positively with film density, $r(7)=0.894$, $p=0.00116$, while the sub-threshold slope correlates negatively with density, $r(7)=0.745$, $p=0.021$, across all three ALD processes, deposition temperature, and post-deposition anneal temperature. Reprinted with permission from reference [70].

In fact, the ZTO film density correlates positively with mobility, $r(7)=0.894$, $p=0.0016$, while the sub-threshold slope correlates negatively with density, $r(7)=0.747$, $p=0.21$, for all films characterized, Figure 2.15. These correlations indicate that densifying the ZTO film both improves electron transport within the active layer and reduces the density of interfacial states at the gate insulator-semiconductor interface, improving the switching properties of the TFT.

The differences in electrical properties observed between thermal and plasma-enhanced ALD ZTO processes, Table 2.2 and Table 2.3, can also be explained by film densification. The ZTO films deposited at 200ºC have significantly lower density when deposited by a thermal process compared to the plasma enhanced ALD processes, Table 2.5. These results are consistent with previous reports of plasma-enhanced ALD of silicon nitride films, where plasma exposure during growth lead to an increase in film density.[100] Thus the excellent behavior of as-deposited hybrid ALD ZTO TFTs, compared to thermal ALD with the same deposition and anneal

temperatures, can be attributed to the denser amorphous films achieved using the hybrid ALD process.

2.5 ALD ZTO TFTs with *ex situ* ALD Gate Insulator

Previous work on ALD ZTO TFTs has been limited to thermally-grown SiO_2 for the gate insulator material.[28], [29] Not only is thermally-grown SiO_2 incompatible with monolithic integration with Si CMOS and flexible substrates, but devices driven with SiO_2 are limited by low oxide capacitance caused by the low dielectric constant of SiO_2. High-*k* dielectrics deposited by ALD, such as HfO_2,[101] ZrO_2,[102] and TiO_2,[103] can be used to increase the oxide capacitance, resulting in higher on-current, smaller operating voltages, and compatibility with BEOL integration.

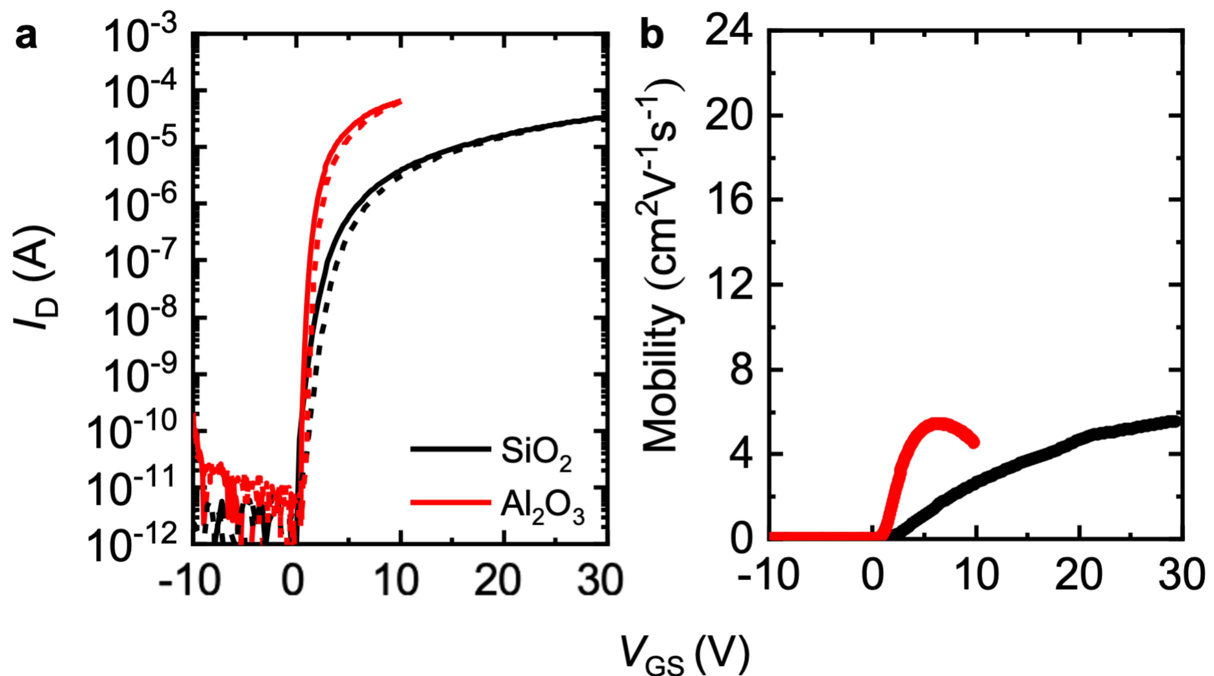


Figure 2.16: a) Transfer curves of TFTs made with c_{Sn} = 21% ALD ZTO films deposited using the thermal process at 150ºC and annealed at 500ºC with two different gate insulators: 100 nm thermal SiO_2 or 30 nm ALD Al_2O_3. Note, the SiO_2 data is the same as that shown for the 500ºC anneal in Figure 2.7a and the V_{GS} range for the Al_2O_3 film was reduced to prevent dielectric breakdown. Forward *I*-*V* curves are indicated by solid lines and reverse curves are indicated by dashed lines. b) Effective mobility extracted from the forward *I*-*V* curves show in part (a). Adapted with permission from reference [70].

To compare the effects of the gate insulator material, SiO_2 and Al_2O_3 were used as gate insulators in TFTs with approximately 22 nm thick c_{Sn} = 21% ZTO active layers deposited using the thermal ALD process at 150ºC and post-deposition annealed at 500ºC. Al_2O_3 was chosen as a gate insulator because it is one of the most widely studied ALD materials and is amorphous as-deposited and after annealing.[104] Transfer curves are shown in Figure 2.16a, and extracted electrical parameters are tabulated in Table 2.6. The increased capacitive coupling of the approximately 30 nm Al_2O_3 yields a peak mobility of 5.39 $cm^2V^{-1}s^{-1}$, very similar to the maximum mobility of 5.44 $cm^2V^{-1}s^{-1}$ for the ZTO on SiO_2 (Table 2.6). The device turn-on is, however, much quicker for devices with Al_2O_3 gate insulator causing the peak mobility to occur at a much lower voltage compared to devices with SiO_2 gate insulator.

Table 2.6: Electrical properties of TFTs made using SiO_2 or Al_2O_3 gate insulator. The ZTO layer is deposited by thermal ALD at 150ºC with c_{Sn} = 21% ALD ZTO annealed at 500ºC. The *I-V* behavior and extracted mobility are shown in Figure 2.16a and Figure 2.16b, respectively. The peak mobility is the maximum value obtained for the V_{GS} range shown in Figure 2.16. Reprinted with permission from reference [70].

Gate Insulator	Peak μ_{FE} [$cm^2V^{-1}s^{-1}$][a)]	SS [V dec^{-1}]	ΔV_C [V]	V_{ON} [V]	V_{switch} [V]
SiO_2	5.44	0.57	0.89	0.54	6.84
Al_2O_3	5.39	0.23	0.55	0.70	2.06

Furthermore, by using Al_2O_3 as the gate insulator, the switching voltage (V_{switch}), defined as the difference between the threshold voltage, extracted for the linear regime, and the turn-on voltage, is reduced from 6.84 V, for devices with SiO_2 gate insulator, to 2.06 V, Table 2.6. The reduction in V_{switch} corresponds to a reduction in SS to 0.23 V dec^{-1} for the Al_2O_3-ZTO TFTs. As predicted, the increased capacitive coupling of a high-k dielectric enables fast turn-on and reduced turn-on voltage, thereby enabling their future electrical integration with BEOL Si CMOS, which runs at supply voltages of a few volts. To further improve switching and turn-on properties the high-k dielectric and ZTO deposition can occur *in situ*, i.e., within the same ALD vacuum

environment and will be investigated in Section 2.6.[105] Optimizing substrate preparation and the insulator deposition process may also improve field-effect mobility to more closely rival quaternary indium-containing ALD TFTs.[67]

2.6 Steep Subthreshold Swing ALD ZTO TFTs with *in situ* Gate Insulator

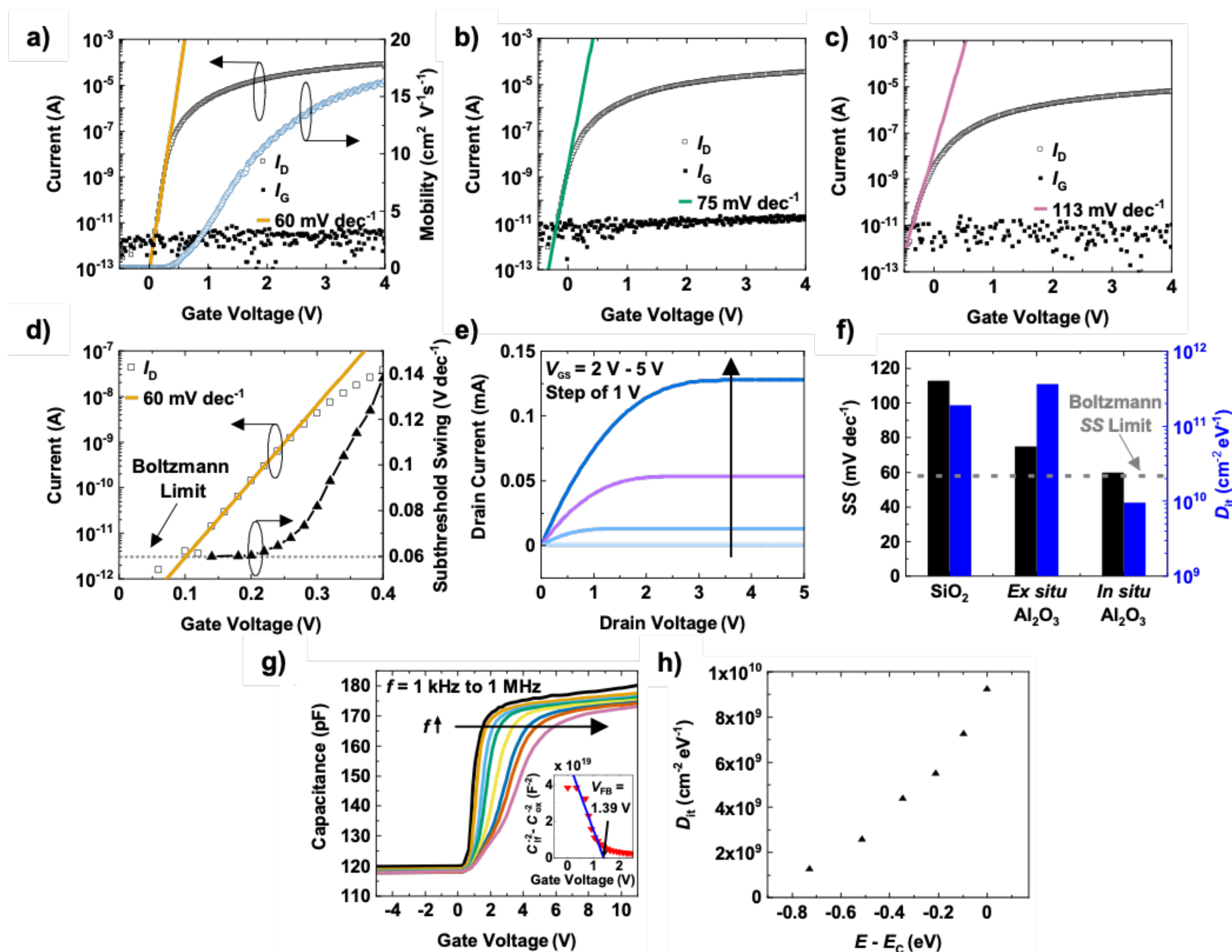


Figure 2.17 Left *y*-axis, transfer characteristics (I_D-V_{GS}) for a) *in situ* Al_2O_3, b) *ex situ* Al_2O_3, and c) SiO_2 gate insulator with V_{DS} = 1 V. The line indicates a fit of 60, 75, and 113 mV dec^{-1}, respectively. The right *y*-axis in a) is the extracted effective mobility. d) Detailed I_D-V_{GS} from a). On the right *y*-axis, *SS* is plotted as a function of V_{GS}. e) Output characteristics (I_D-V_{DS}) with V_{GS} swept from 2 to 5 V with a 1 V step. Note: 0 and 1 V V_{GS} plots overlap with the 2 V V_{GS} plot. g) Measured C_p-V_{GS} as a function of frequency. Inset: V_{FB} extracted by a linear fit of $C_{\mathrm{LF}}^{-2} - C_{\mathrm{ox}}^{-2}$ as a function of V_{GS}. h) Energy distribution of D_{it} extracted using the high-low frequency method. Adapted from [79].

ALD ZTO TFTs made with *in situ* gate insulator exhibit an extremely low *SS* of 60 mV dec^{-1}, a maximum linear mobility of 17.0 cm^{2}V^{-1}s^{-1}, an ON/OFF current ratio > 10^8, and a

threshold voltage of 1.8 V (Figure 2.17a). The minimum *SS* of 60 mV dec^{-1} occurs at the turn-on voltage of 0.18 V (Figure 2.17d). The linear mobility is in good agreement with the saturation mobility of 15.8 cm^{2}V^{-1}s^{-1} (Figure 2.17e). Multi-frequency *C-V* measurements (Figure 2.17g) were used to extract an estimated D_{it} using the high-low frequency method [106]. The measured parallel capacitance, C_p, is shown in Figure 2.17g. First, the equations

$$C_{\mathrm{lf}} = \left(\frac{1}{C_{\mathrm{ox}}} + \frac{1}{C_{\mathrm{s}} + C_{\mathrm{it}}}\right)^{-1} \tag{2.3}$$

and

$$C_{\mathrm{s}} = \frac{C_{\mathrm{ox}} C_{\mathrm{hf}}}{C_{\mathrm{ox}} + C_{\mathrm{hf}}} \tag{2.4}$$

where C_{lf} is the low frequency (1 kHz) C_p, C_{hf} is the high frequency (1 MHz) C_p, and C_{ox} is the oxide capacitance taken as the maximum of C_{lf}, are used to solve for the capacitance, $C_{it,}$ due to D_{it}. Then, D_{it} is calculated using the equation

$$D_{\mathrm{it}} = \frac{C_{\mathrm{ox}}}{q^2}\left(\frac{C_{\mathrm{lf}}/C_{\mathrm{ox}}}{1 - C_{\mathrm{lf}}/C_{\mathrm{ox}}} - \frac{C_{\mathrm{hf}}/C_{\mathrm{ox}}}{1 - C_{\mathrm{hf}}/C_{\mathrm{ox}}}\right) \tag{2.5}$$

where q is the electron charge, and the energy level *E* is calculated by

$$E - E_{\mathrm{C}} = \int_{V_{\mathrm{FB}}}^{V_{\mathrm{GS}}} \left(1 - \frac{C_{\mathrm{lf}}}{C_{\mathrm{ox}}}\right) dV_{\mathrm{GS}} \tag{2.6}$$

where E_C is the conduction band edge and the flat band voltage, V_{FB}, is extracted as the *x*-axis intercept of $C_{\mathrm{lf}}^{-2} - C_{\mathrm{ox}}^{-2}$ as a function of V_{GS} (Figure 2.17g inset). The HF-LF D_{it} energy distribution is shown in Figure 2.17h and agrees with the value of 9.59×10^9 cm^{-2} eV^{-1} calculated directly from *SS* [106]. For comparison, two similar samples having different gate insulators and ZTO deposited at 150ºC were measured (Figure 2.17b and Figure 2.17c). TFTs with a 100 nm thermal SiO_2 gate insulator yields a *SS* of 113 mV dec^{-1} while TFTs with an *ex situ* deposited Al_2O_3 gate insulator,

made using the same O_3-process as the *in situ* Al_2O_3 layer, yields a *SS* of 75 mV dec^{-1}. The extracted D_{it} for these two comparison TFTs are 1.9×10^{11} cm^{-2} eV^{-1} and 3.66×10^{11} cm^{-2} eV^{-1}, respectively. These D_{it} values are factor of 20 to 50 higher than that of the TFT with *in situ* Al_2O_3 gate insulator. As expected, by replacing the low-*k* SiO_2 gate insulator with higher-*k* (~8.38) *ex situ* Al_2O_3, the device *SS* is reduced due to the increased capacitive coupling, however D_{it} increased slightly. In contrast, the *in situ* ALD deposition process, where the surface of Al_2O_3 is kept in vacuum and is not exposed to ambient air before ZTO deposition, dramatically reduces the D_{it}, which leads to an *SS* of 60 mV dec^{-1}, very close to the Boltzmann limit (Figure 2.17f). The *in situ* process may result in a lower D_{it} because the *ex situ* process exposes the surface to air which may cause adsorption of water molecules, or other adventitious species, that act as defects in ZTO [107]. By using an *in situ* O_3-based ALD Al_2O_3 gate insulator with a low concentration of interface defects, we achieve the steepest *SS* reported to date for BEOL-compatible traditional MISFETs (Table 2.7).

Table 2.7 Comparison with other BEOL-compatible MISFETs. Adapted from [79].

Deposition Method & Material	**Gate Insulator**	***SS* [mV dec^{-1}]**	**Ref.**
ALD ZTO	***in situ* O_3-based ALD Al_2O_3**	**60**	**This Work**
	***ex situ* O_3-based ALD Al_2O_3**	**75**	**This Work**
	SiO_2	**113**	**This Work**
	SiO_2	150	[28]
Solution-processed ZTO	AlO_x	96	[108]
	HfO_2	70	[109]
RF Sputtered IGZO	HfO_2	70	[110]
	Al_xO_y	68	[111]
	SiO_2/HfO_2	96	[112]
Exfoliated MoS_2	HfO_2	74	[113]
	Y_2O_3/HfO_2	65	[114]

2.7 Impact of active layer thickness on device performance

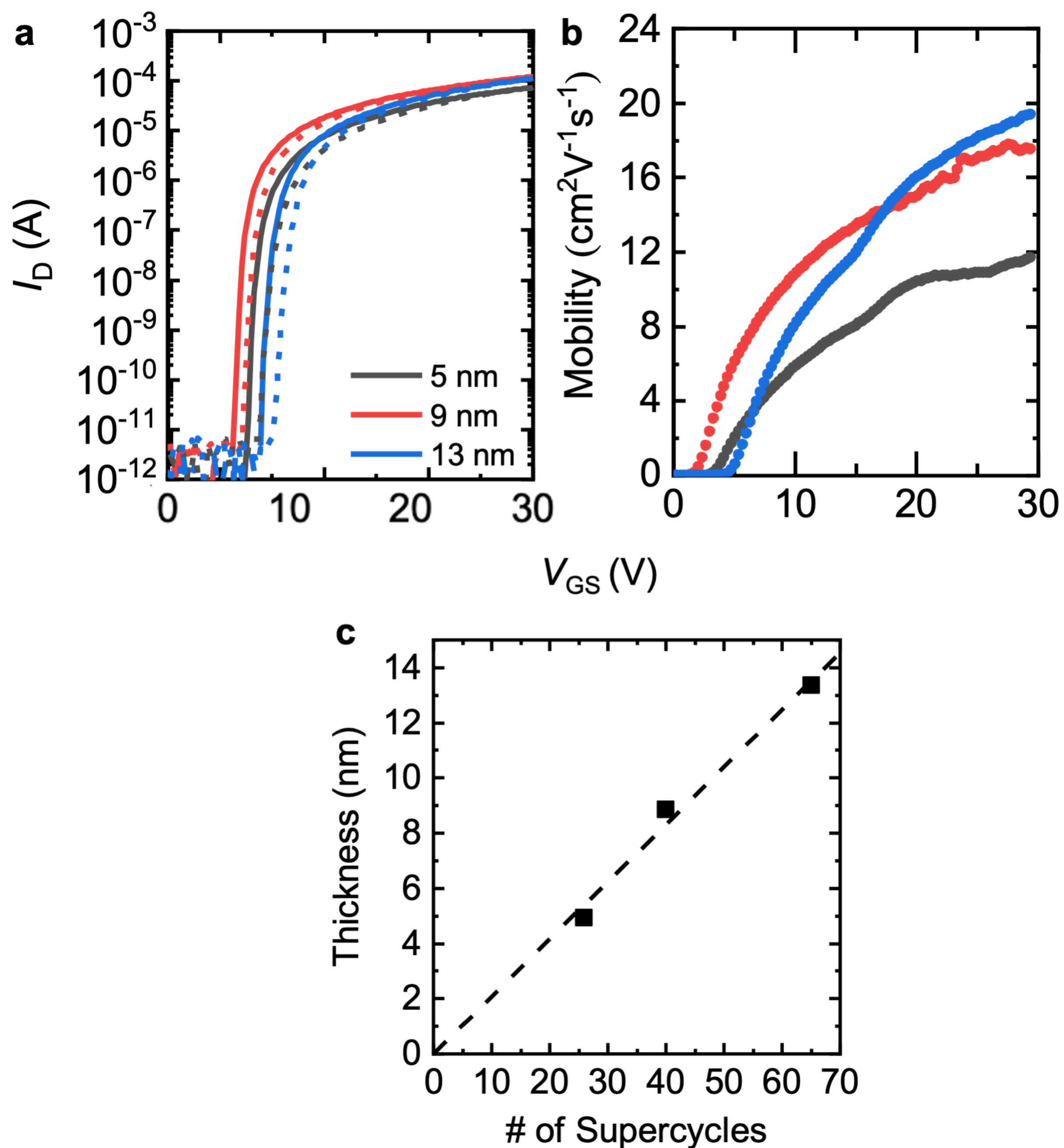


Figure 2.18: a) Transfer curves of TFTs made with c_{Sn} = 21% ALD ZTO films deposited using the thermal process at 200ºC and annealed at 500ºC with various ZTO layer thickness. Note, the trace labeled 9 nm is the same as that shown in Figure 2.9a. Forward *I-V* curves are indicated by solid lines and reverse curves are indicated by dashed lines. b) Effective mobility extracted from the forward *I-V* curves show in part (a). c) The number of supercycles vs. film thickness for the devices in Figure 2.18a and Table 2.8 are plotted in black squares. The linear fit of the points going through the origin is indicated by the black dashed line. Adapted with permission from reference [70].

Optimization of active-layer thickness has been shown to be necessary to obtain good TFT stability[115] and enhancement mode behavior[116] for TFTs made using other deposition techniques or semiconductor oxides. To investigate the effect of thickness on TFT behavior, three identical devices were fabricated with thermal ALD ZTO active layers deposited at 200ºC with thickness of 5, 9, and 13 nm and post-deposition annealed at 500ºC. Transfer curves and plots of effective mobility are shown in Figure 2.18a and Figure 2.18b, respectively, with extracted device parameters tabulated in Table 2.8. The 200ºC thermal process yields enhancement-mode behavior for all three active layer thicknesses. While both the 9 and 13 nm thick films have a mobility greater than 17 $cm^2V^{-1}s^{-1}$, there is a decrease for the 5 nm thick device. In Figure 2.18c, we plot the number of supercycles vs. film thickness for these three films and create a linear fit through the origin. The good linear fit through the origin indicates the films have a similar GPC and there is minimal nucleation delay for the 200ºC thermal process. Additionally, all three films have similar refractive index, Table 2.8, which would not be expected if there as a growth issue as the film thickness was reduced. Therefore, nucleation-limited growth likely does not explain the reduced mobility of the 5 nm thick device. Instead, the reduced mobility could possibly be attributed to the increased influence of carrier scattering at the top surface. Future work could investigate applying a passivation layer to the 5 nm thick device to reduce the influence of carrier scattering at the top surface.

Table 2.8: Electrical properties of TFTs made with different ZTO layer thicknesses. The ZTO layers are deposited by thermal ALD at 200ºC with 21% tin composition and annealed at 500ºC. The *I*-*V* behavior and extracted mobility are shown in Figure 2.18a and Figure 2.18b, respectively. The last column gives the refractive index of the ZTO films measured by ellipsometry. Reprinted with permission from reference [70].

ZTO Thickness [nm]	μ_{FE} [$cm^2V^{-1}s^{-1}$]	*SS* [V dec^{-1}]	ΔV_C [V]	V_{On} [V]	Refractive Index
5	11.3	0.35	1.63	3.54	1.90
9	17.5	0.30	1.06	1.75	1.86
13	18.5	0.37	1.58	3.60	1.85

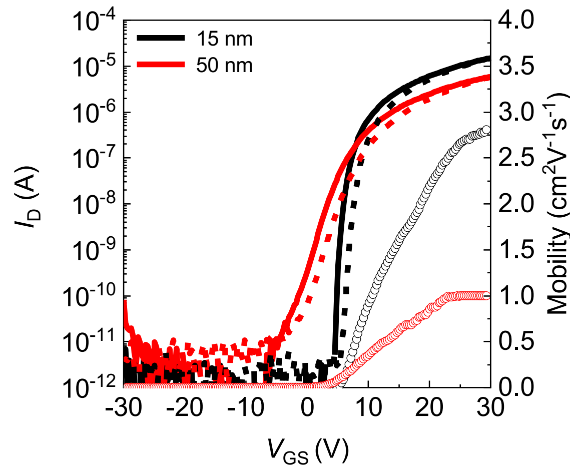


Figure 2.19: Transfer curves of TFTs with two different channel layer thickness. In both cases, the ZTO was deposited by thermal ALD at 130ºC with f_{Sn} = 50%, and annealed at 500ºC. For both devices, W/L is 10 and V_{DS} = 1 V. The forward *I-V* curves are indicated by solid lines while reverse curves are indicated by dashed lines, all plotted on the left y-axis. Mobility is plotted using the open circles on the right y-axis. Reprinted with permission from reference [70].

Interestingly, for some ALD ZTO recipes we tried, device performance degrades for thicker films. TFT behavior for thermal ALD ZTO deposited with f_{Sn} = 50% at 130ºC and annealed at 500ºC is shown in Figure 2.19. As ZTO film thickness increased from 15 to 50 nm, the mobility decreased from 2.7 $cm^2V^{-1}s^{-1}$ to approximately 1 $cm^2V^{-1}s^{-1}$. In addition, the *SS* increases substantially from 0.48 V dec^{-1} for the 15 nm thin film to approximately 1 V dec^{-1} for the 50 nm thick film and the turn-on voltage became more negative with increasing thickness. Similar trends with channel thickness have been reported previously for a-Si, IGZO, and ZnO TFTs, and may be associated with surface depletion layers or other back-channel effects, or, in some cases, with vertical gradients in semiconductor film trap densities.[117] These results indicate that, at least for some ALD ZTO conditions, the channel layer thickness needs to be optimized alongside the gate dielectric process in order to achieve the best TFT behavior.

2.8 Conclusions

In conclusion, we developed an ALD supercycle approach to deposit high quality amorphous zinc tin oxide. Using XPS to extract the tin composition for a given tin cycle fraction resulted in a correction of the ZnO growth rate in the c_{Sn} equation based on the rule of mixtures. This equation can be used for precise tuning of the film composition with c_{Sn} ranging the values of interest for active electronic devices and is less complex than previously proposed equations because the supercycle design approach used in this chapter only has one or two ZnO cycles in a row. The tin composition was then tuned to find 21% yielded the best TFT performance for the processes studied in this chapter.

Three different deposition processes were studied: H_2O-based thermal, hybrid H_2O/O_2 plasma, and all-plasma. All processes yield as-deposited semiconducting films, due to a low concentration of oxygen vacancies, with enhancement-mode behavior and electron mobility as high as 13.8 $cm^2V^{-1}s^{-1}$. For all processes, we found increasing the ALD deposition temperature and the post-deposition annealing temperature improves the ZTO electrical properties, due to film densification studied using XRR. The best performance was seen for hybrid ALD ZTO films with c_{Sn} = 21% deposited at 200ºC and annealed at 500ºC with μ_{FE} = 22.0 $cm^2V^{-1}s^{-1}$ and SS = 0.28 V dec^{-1}. The better behavior of the hybrid thermal/plasma ALD ZTO films compared to those deposited by thermal ALD or all-plasma ALD is attributed to the densification of the film and reduction of hydroxyl states, extracted from XPS data, while avoiding the plasma damage that may come from an all-plasma process.

Moreover, nearly the same performance was observed when the hybrid ALD film was annealed at 400ºC: μ_{FE} = 22.1 $cm^2V^{-1}s^{-1}$ and SS = 0.29 V dec^{-1}. This indicates the compatibility of these ALD processes with the thermal budget at the silicon CMOS back-end-of-line. Finally, by using

an *in situ* ALD Al_2O_3 gate insulator with a low D_{it} and choosing an optimal ZTO film thickness of 9 to 13 nm, we obtained transistors with *SS* approaching the Boltzmann limit leading to rapid turn-on and low switching voltages, enabling supply voltage compatibility with silicon ICs. The results of this chapter pave the way for future monolithic integration of multi-functional ZTO electronics on top of silicon CMOS or onto large-area flexible substrates.

Chapter 3 High voltage ZTO thin film transistor

3.1 Introduction

In Chapter 1, we discussed how over 60 years of silicon research has led to maturity of the silicon industry, but even as a mature material, Si is a poor choice for power devices because of a narrow bandgap and low breakdown electric field. Instead, power semiconductors have a wide bandgap which generally leads to high thermal conductivity, high critical fields (allowing for higher doping and reduced on-resistance), and high barrier heights (reducing the leakage current). Traditional wide bandgap semiconductors, like SiC and GaN, require crystalline substrates with devices fabricated in only a single plane of bulk material leading to a costly and complex process. Thin-film power devices present a low-cost opportunity to act as a low to high voltage interface through large-area 3D monolithic integration of power devices on underlying integrated circuits.

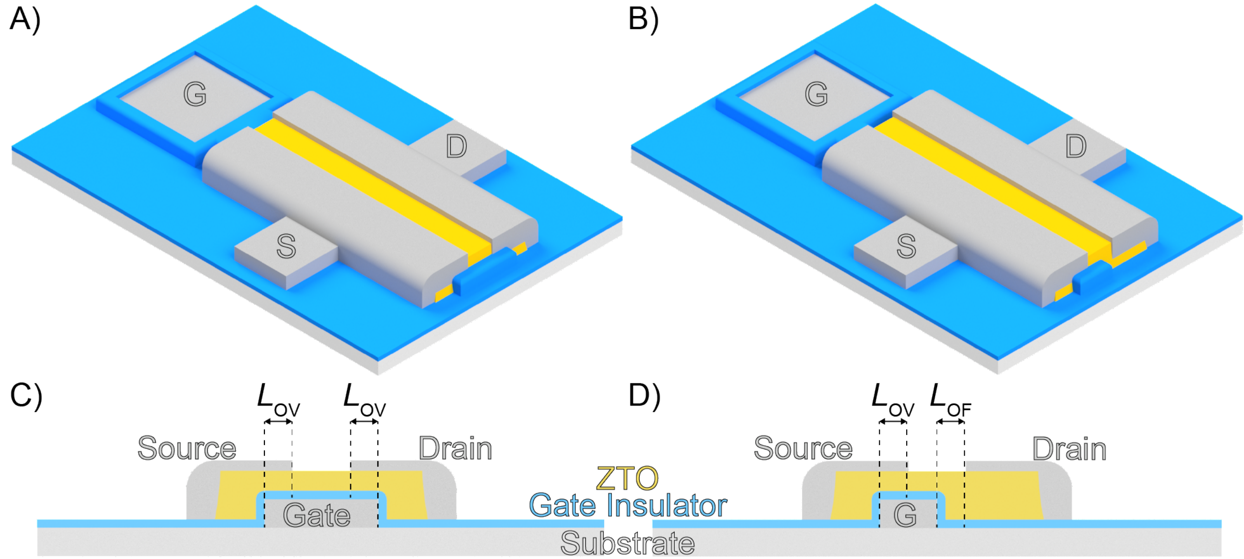


Figure 3.1: A) Schematic and C) cross section diagram of traditional bottom gate top contact TFT with top source/drain metal overlapping the bottom gate metal by length, L_{OV}. C) Schematic and D) cross section diagram of HVTFT with offset between bottom gate metal and top drain metal by length, L_{OF}.

An important characteristic of power devices is the highest sustainable drain voltage before failure, known as the breakdown voltage, V_{BD}. One way to increase V_{BD} is by introducing an offset between the gate and drain electrode edges of length L_{OF}, Figure 3.1. These offsets have been used with bulk crystalline materials, both silicon and wide bandgap semiconductors, and with amorphous silicon TFTs as early as 1993.[118] Even with a gate/drain offset, a-Si is a poor choice for HVTFT applications because of a-Si's narrow bandgap and low field effect mobility.

Amorphous oxide semiconductors, on the other hand, are well posed for HVTFT applications because of their large area uniformity and favorable semiconductor properties, i.e. wide bandgap, large dielectric constant, and higher mobility compared to a-Si and organics, Table 3.1. Vacuum-deposited amorphous-indium gallium zinc oxide and zinc oxide TFTs for high voltage applications have adopted gate/drain offset structure to achieve high-voltage TFTs (HVTFTs) with V_{BD} as high as 82 V.[15], [119]–[122] ZnO is a nano-crystalline material and nano-crystalline morphology may present uniformity issues and cause a buildup of defects along grain boundaries leading to premature breakdown.

Table 3.1 Summary of semiconductor properties for high-voltage applications.

Property (at 300K)	*c*-Si	*a*-Si:H	ZnO	GaN	Ga_2O_3	4H-SiC	AOS
Bandgap (eV)	1.12	1.7-1.9	3.3	3.4	4.6	3.3	~3.0
Relative dielectric constant	11.8	11.8	8.75	10.6	10.2	9.7	11.5-13.8
Electron mobility ($cm^2V^{-1}s^{-1}$)	1400	<1	226	5300	100-300	1000	10-30
Large area scalable	Yes	Yes	Yes	No	No	No	Yes

To achieve an amorphous indium-free HVTFT, we implement the gate/drain offset structure with a-ZTO deposited using a solution-process. The V_{BD} of the HVTFTs increases from 45 V with no-offset to over 100 V with a 3 µm drain offset while maintaining 200 µA on-current. As shown with previous work with gate/drain offset HVTFTs, the on-resistance (R_{on}) increased due to the drain offset region. Large R_{on} values limit current and lead to power loss and reduced power efficiency. To optimize the trade-off between V_{BD} and R_{on} the impact of the gate/drain offset on device characteristics was studied using Silvaco ATLAS simulations.

3.2 Experimental Section

Silvaco Atlas Simulations

To choose the appropriate L_{OF}, 2D TCAD simulations of devices with a cross section as depicted in Figure 3.1D were performed using Silvaco Atlas. When simulating AOS films, the defects of the film define how the devices operate. The parameters used to define the defects in these simulations were selected from previous work.[123] Furthermore, the breakdown of the a-ZTO film was simulated by using an impact ionization rate from a revised lucky drift model.[124] The model calculates the energy an electron gains, E_a, under an applied electric field where the optical photon energy, E_r, and the ionization threshold energy, E_i, were taken as the worst-case prediction of 30 meV and 1.7 eV, respectively.[125] The model is then incorporated

into Silvaco Atlas simulations using a piece-wise linear approximation. Breakdown simulations swept V_{DS} while keeping V_{GS} and V_S grounded. These simulations resulted in approximations of the breakdown field and V_{BD} of the HVTFTs with various L_{OF}. As these results were approximations based on assumptions of breakdown of ZTO, the electric-fields were normalized for comparison. Additional simulations of I_{DS}-V_{DS} were performed to extract a R_{on} approximation from the slope of the I_D-V_{DS} curves in the linear, or ohmic, region before saturation occurs.

3.2.1 Sample fabrication

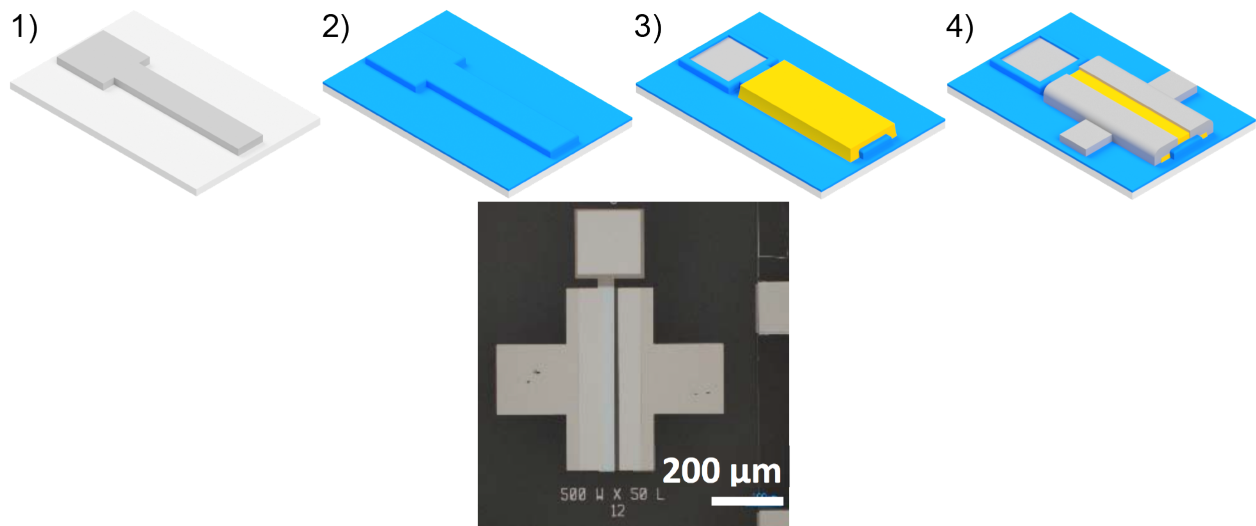


Figure 3.2: Top: Fabrication process of TFT. 1) Bottom gate metal deposited by sputtering Mo and patterned by RIE. 2) 30 nm Al_2O_3 deposited by ALD as gate insulator. 3) ZTO deposited by solution process and etched using a wet etch. Gate insulator etched using a wet etch. 4) Top ohmic contacts made by sputtering Mo and patterning by liftoff. Bottom: Top down microscope image of fabricated device with 500 µm width, 50 µm length, and L_{OF} of 12 µm. Adapted from [31].

Approximately 40 nm of molybdenum was deposited on to Corning Eagle XG glass substrates by sputtering. The molybdenum was then etched to form the bottom gate using standard photolithography and reactive ion etching (RIE). After patterning of the bottom gate metal, approximately 30 nm of Al_2O_3 was deposited by atomic layer deposition (ALD) to form the gate insulator with an oxide capacitance, C_{ox}, of 72.3 nF·cm^{-2}. Then, 3 layers of 0.5 M ZTO solution with a 7:3 Zn:Sn ratio were spin coated onto the samples with a 1 min 520ºC air anneal between

each layer and a final 1 hour 520ºC air anneal after the final layer was spin coated for a film thickness of approximately 80 nm.[77] For device isolation, the ZTO layer was patterned using standard photolithography and etched with a dilute hydrochloric and nitric acid solution. To allow probing of the gate, the insulator was then patterned using standard photolithography and etched in a heated dilute ammonium hydroxide wet etch. Finally, ohmic top source and drain electrodes were deposited by sputtering approximately 40 nm of molybdenum and patterned by liftoff.[78] This fabrication process is illustrated in Figure 3.2.

3.3 Increased Blocking Voltage in ZTO HVTFTs through Drain Offset

3.3.1 Simulations Varying Offset Length

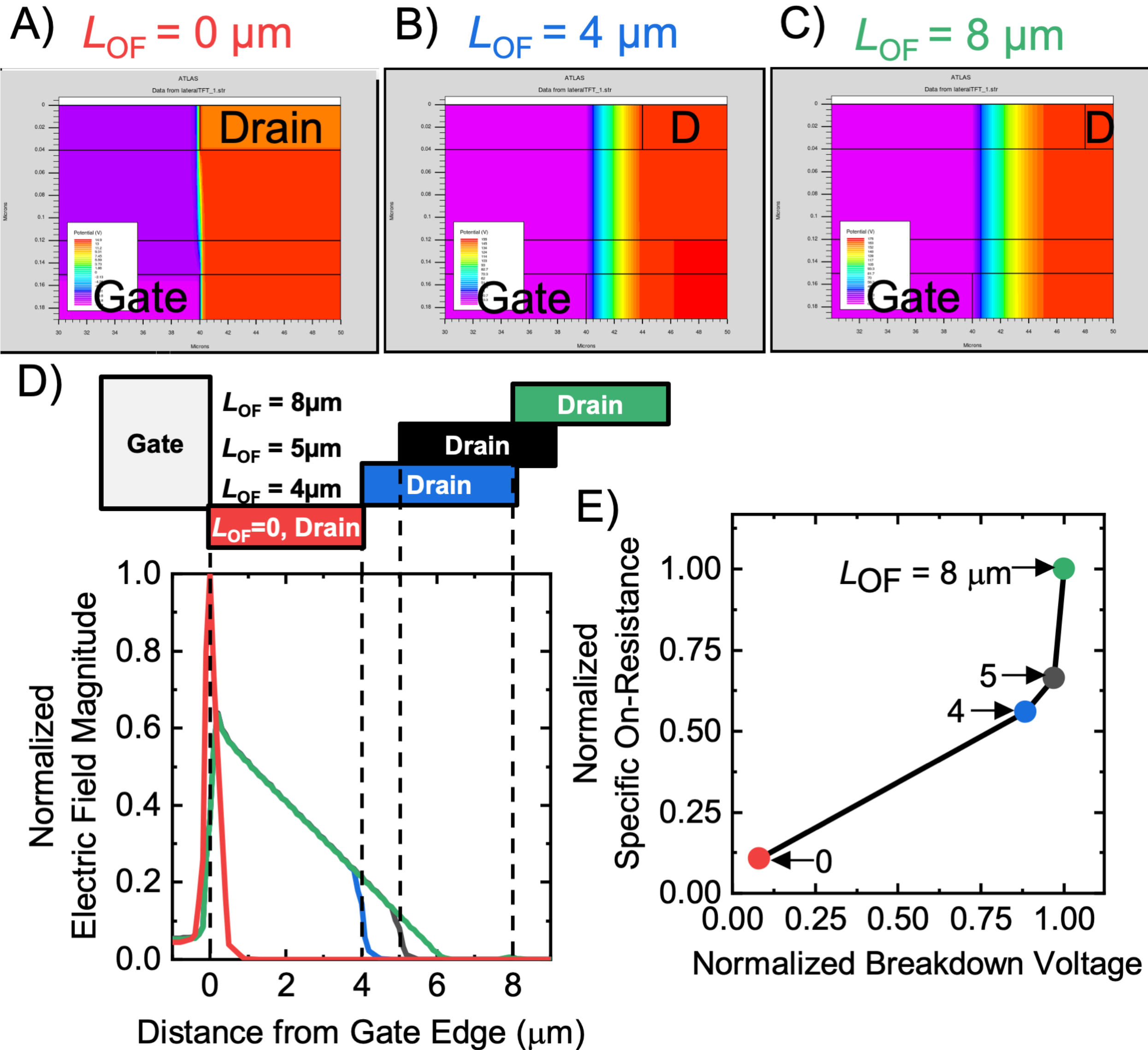


Figure 3.3: A),B) and C) show cross sections views of the electric field magnitude in the offset region for devices with L_{OF} of 0, 4, and 8 µm, respectively. D) Normalized electric field between gate and drain edges at breakdown. E) Plot showing how the breakdown voltage and on-resistance of the devices are correlated. Adapted from [31].

Before fabricating devices, device simulations were performed using Silvaco Atlas to understand the impact of L_{OF} on the electric field distribution and to help define the architecture of the fabricated devices. The electric field magnitude, normalized to the highest peak, at breakdown

for devices with L_{OF} of 0, 4, 5, and 8 μm are shown in Figure 3.3D. In general, there is a peak at the gate and drain edges and the drain offset works to distribute the electric field in the device increasing the voltage at which breakdown occurs.

The electric field is redistributed because the offset acts as a depletion region where the voltage applied to the drain electrode causes depletion of the semiconductor starting at the gate edge. With no offset, the electric potential is only spread vertically leading to a low breakdown voltage (red curve in Figure 3.3D). With an offset, the potential is spread further, laterally, across the depletion region reducing the peak electric field. If L_{OF} is smaller than the depletion width, the depletion layer penetrates just past the drain edge creating a trapezoidal field shape (gray and blue curves in Figure 3.3D) with a non-zero electric field at the drain edge and this electric-field setup is called punch-through type. For these devices, punch-through means that increasing the L_{OF} will increase the breakdown voltage, Figure 3.3E. If the L_{OF} is larger than the depletion width, about 6 μm in these simulations, there is a triangular field shape (green curve in Figure 3.3D) with zero electric field at the drain edge and this is called non-punch-through dimensioning.[126] For these devices this means the maximum breakdown voltage for this architecture has been achieved. When the maximum breakdown voltage is achieved, any further increase in L_{OF} will cause an increase in on-resistance, Figure 3.3E. As discussed earlier, any increase in R_{on} yields increased power loss and therefore, it is important to optimize the offset length.

Simulations show the gate cannot accumulate a channel in the offset region of the HVTFT. For AOS MISFETs, where device operation is dependent on the ability to accumulate a channel, the inability to accumulate more electrons means the offset, with low unintentional doping of about 10^{16} cm^{-3}, will dominate R_{on} . The resistance of the offset region increases as the length of the resistance (L_{OF}) increases while the blocking voltage will reach a maximum value. As there is a

tradeoff between R_{on} and V_{BD}, the minimum L_{OF} to achieve a given V_{BD} should be chosen to minimize R_{on} and therefore power loss.

3.3.2 Reducing Series Resistance of Offset Region

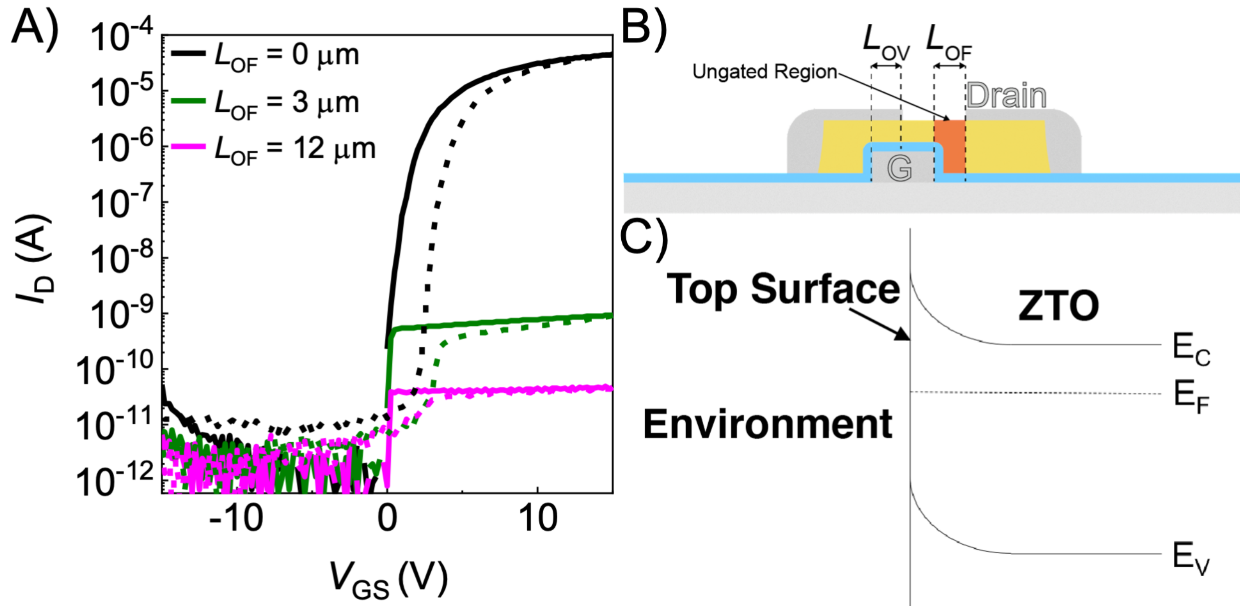


Figure 3.4: A) Transfer curves of HVTFTs with various L_{OF}. All HVTFTs have a W/L of 10 and V_{DS} = 1 V. The forward *I-V* curves are indicated by the solid lines and the reverse *I-V* curves are indicated by the dashed lines. The hysteresis between the forward and reverse sweeps is caused by traps in the bulk ZTO or by reactions at the back interface.[97] B) Schematic diagram of HVTFT highlighting (red shaded area) high-resistance ungated region of the HVTFT. C) Band diagram of the top surface of the ZTO in the ungated region showing depletion caused by adsorbed oxygen in the environment.

Initial measurements of fabricated HVTFTs with non-zero L_{OF}, as short as 3 μm, resulted in unexpectedly low on-current, Figure 3.4. Some decrease in on-current was expected due to introduction of the offset, but this cannot explain the decrease observed. The low on-current is instead attributed to oxygen adsorption on the top surface.[127] The adsorbed oxygen depletes carriers in the offset region, Figure 3.4B and Figure 3.4C, which cannot create an accumulation region without gate control. The resulting low carrier concentration, caused by the depletion of electrons, leads to a large resistance and decreased on-current. The on-current decreases as L_{OF}

increases because as the length of the high-resistance ungated region increases the series resistance also increases.

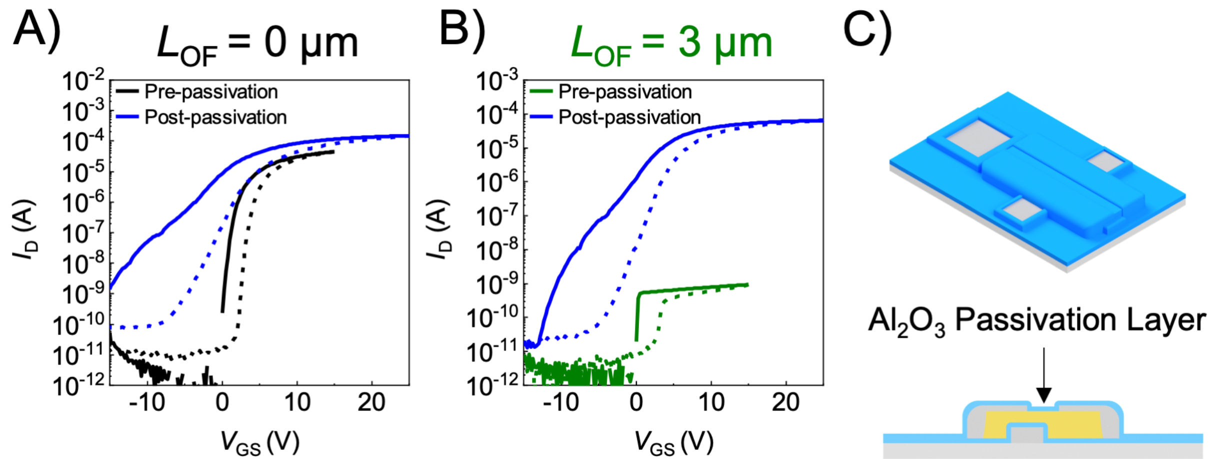


Figure 3.5: Transfer curves of HVTFTs with L_{OF} of A) 0 µm and B) 3 µm both pre- and post-passivation. All HVTFTs have a W/L of 10 and V_{DS} = 1 V. The forward *I-V* curves are indicated by the solid lines and the reverse *I-V* curves are indicated by the dashed lines. Note: The pre-passivation curves are the same as those in Figure 3.4. C) Top: Schematic and bottom: cross section diagram of passivated HVTFT. Adapted from [31].

One way to prevent the adsorption of oxygen molecules is to encapsulate the back surface of the ZTO. This can be accomplished through deposition of a dielectric layer after the devices are fabricated. Here, we use approximately 30 nm of Al_2O_3, deposited by thermal ALD at 150ºC, as the passivation layer as illustrated in Figure 3.5C. Transfer curves for devices pre- and post-passivation with L_{OF} of 0 µm and 3 µm are shown in Figure 3.5A and Figure 3.5B, respectively. Post-passivation there is a clear increase in on-current for both devices indicating successful inhibition of oxygen adsorption causing depletion and possibly even doping from the H_2O during the ALD process.[127] The passivated device with L_{OF} of 0 µm has an electron mobility of 11.8 $cm^2V^{-1}s^{-1}$, threshold voltage of -0.4 V, and $I_{on}/I_{off} > 10^6$. Unfortunately, however, passivation introduced a second parallel channel, either at the back interface or at the semiconductor edges, that turns on at negative V_{GS} and increases the subthreshold slope from 0.33 V dec^{-1} to 1.36 V dec^{-1}.

This issue was resolved by using an O_3-based ALD Al_2O_3 passivation layer and is the topic of Section 4.4.

3.3.3 Electrical and Breakdown Performance of Fabricated HVTFTs

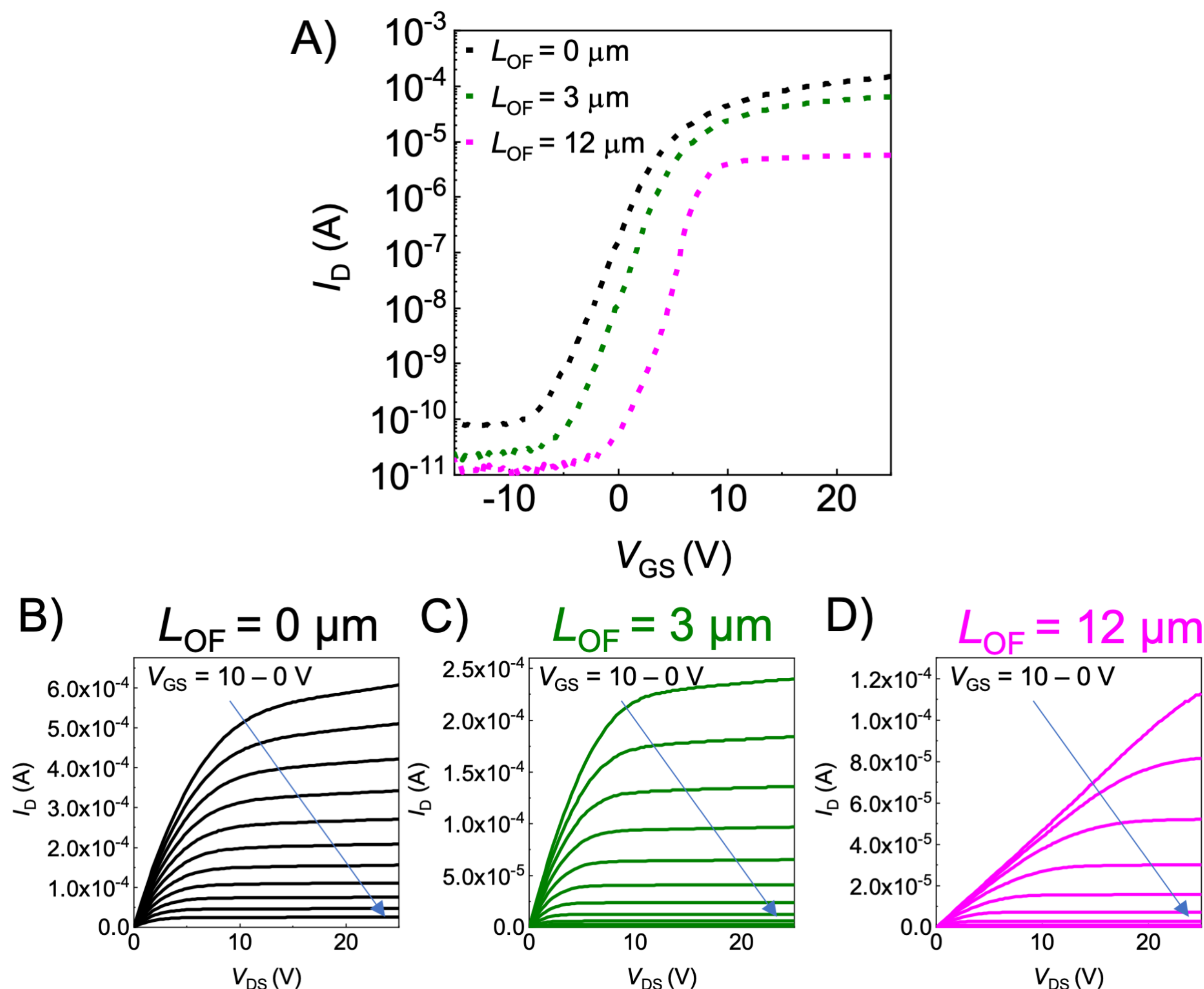


Figure 3.6: A) Reverse transfer curves of passivated HVTFTs with various L_{OF}. All HVTFTs have a W/L of 10 and V_{DS} = 1 V. Note: The L_{OF} = 0 μm and L_{OF} = 3 μm curves are the same as the reverse curves in Figure 3.5. Output curves of passivated HVTFTs with L_{OF} of B) 0 μm, C) 3 μm, and D) 12 μm. The V_{GS} is varied from 0 V to 10 V in 1 V increments. Adapted from [31].

The reverse sweeps (positive V_{GS} to negative V_{GS}) are better representations of how the devices would perform with a higher quality passivation layer and are therefore analyzed in this section. Figure 3.6A shows the reverse I_D-V_{GS} sweeps for devices with L_{OF} of 0 μm, 3 μm, and 12 μm. As expected from simulations, an increase in offset length leads to a decrease in on-current

due to increased resistance. The output characteristics for these devices are shown in Figure 3.6B-D. All devices show good linear and saturation behavior indicating ohmic contacts. Again, as L_{OF} increases the saturation current decreases and the linear region becomes more prominent due to the increased resistance of the offset region.

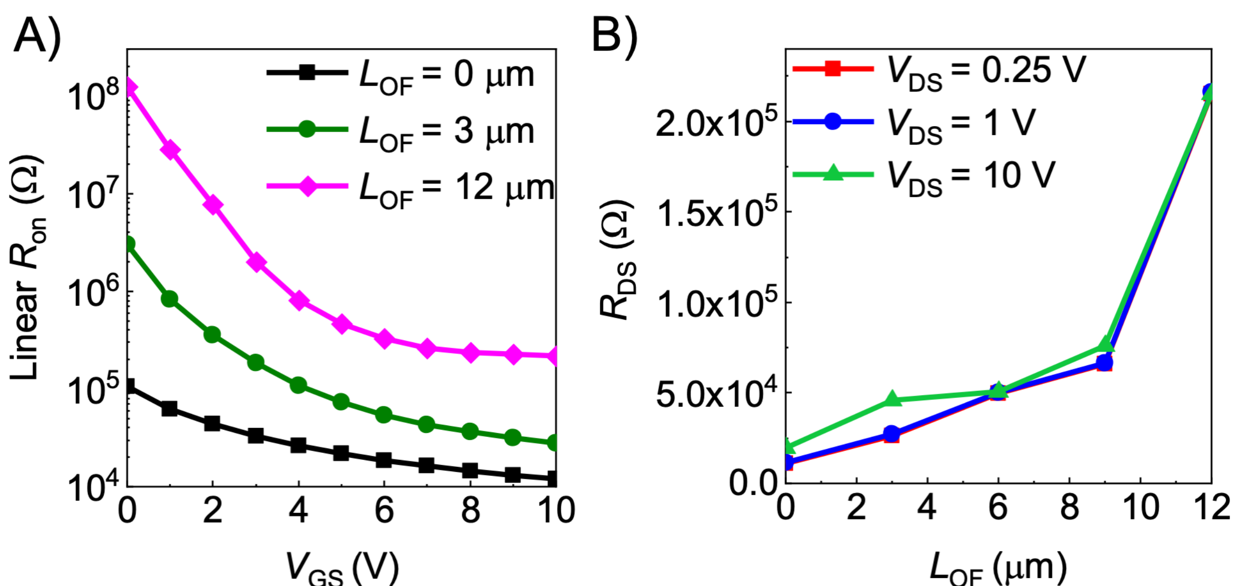


Figure 3.7: A) R_{on} extracted from the inverse slope of the linear region of the output curves in Figure 3.6B-D as a function of gate voltage. B) R_{DS} as a function of L_{OF} for V_{GS} = 10 V. Adapted from [31].

The resistance of the devices can be extracted from the output curves in Figure 3.6B-D by taking the inverse of the slope in the linear region. The extracted R_{on}, Figure 3.7A, confirms the longer L_{OF} is, the higher R_{on} is. At low V_{GS} all devices have a comparatively high R_{on} because in this region, R_{on} is dominated by the channel resistance, $R_{channel}$. As V_{GS} increases, the channel is accumulated and the resistance decreases. Once $R_{channel}$ is less than the offset resistance, R_{OF}, R_{on} as a function of V_{GS} begins to flatten out as R_{OF} dominates R_{on} and cannot be modulated by V_{GS}. Another indication of ohmic contacts is that R_{DS} is independent of V_{DS} down to V_{DS} = 0.25 V for all devices analyzed here, Figure 3.7B.

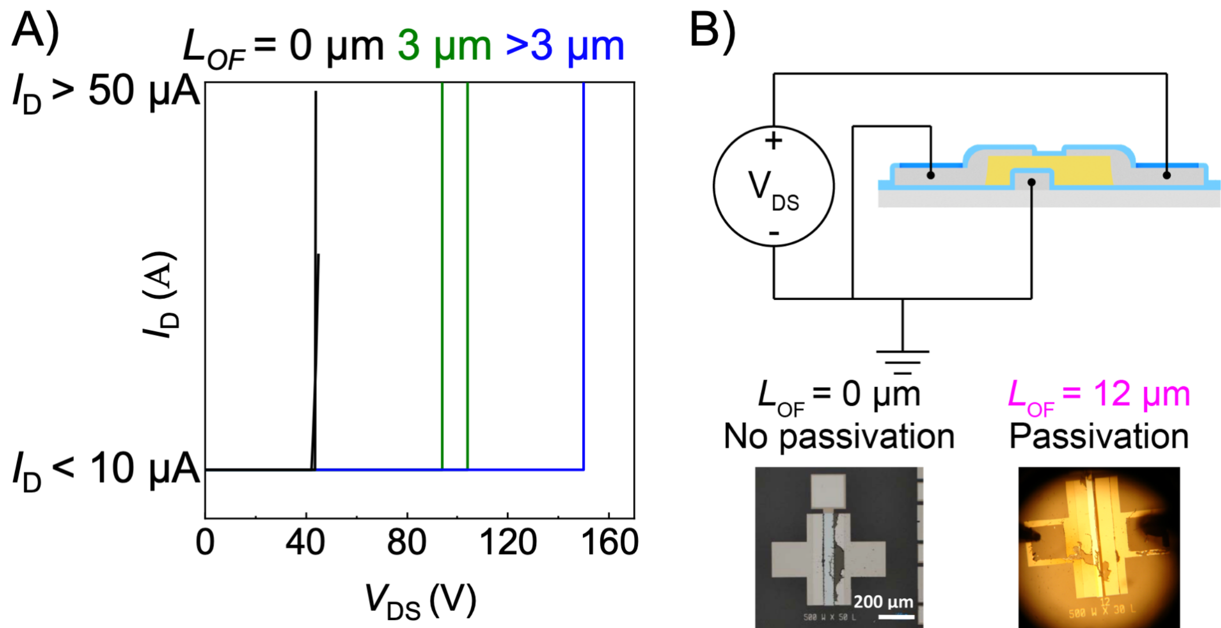


Figure 3.8: A) V_{DS} sweeps to test breakdown of the devices. Note: Current resolution is limited by the test setup. B) Top: Schematic illustration of test setup used in A). Bottom: Photos of devices after breakdown. Adapted from [31].

Breakdown was measured by grounding the source and gate electrodes and sweeping the drain voltage using an SRS PS310, as schematically shown in Figure 3.8B. Without a drain offset, breakdown occurs at about 45 V, Figure 3.8A, regardless of passivation. This breakdown is dielectric breakdown and occurs at the drain-gate edge as shown in Figure 3.8B. With an L_{OF} of 3 µm, the breakdown voltage increases to about 100 V and the breakdown mechanism is still dielectric breakdown. When L_{OF} is greater than 3 µm, the breakdown mechanism changes. The influx of charge at the higher voltages may cause the metallic pads to vaporize or breakdown may occur through the air/surface of the film as shown in Figure 3.8B for a device with a 12 µm offset. As a result, the breakdown voltage becomes less sensitive to offset length and is around 150 V.

3.4 Potential Next Generation HVTFTs

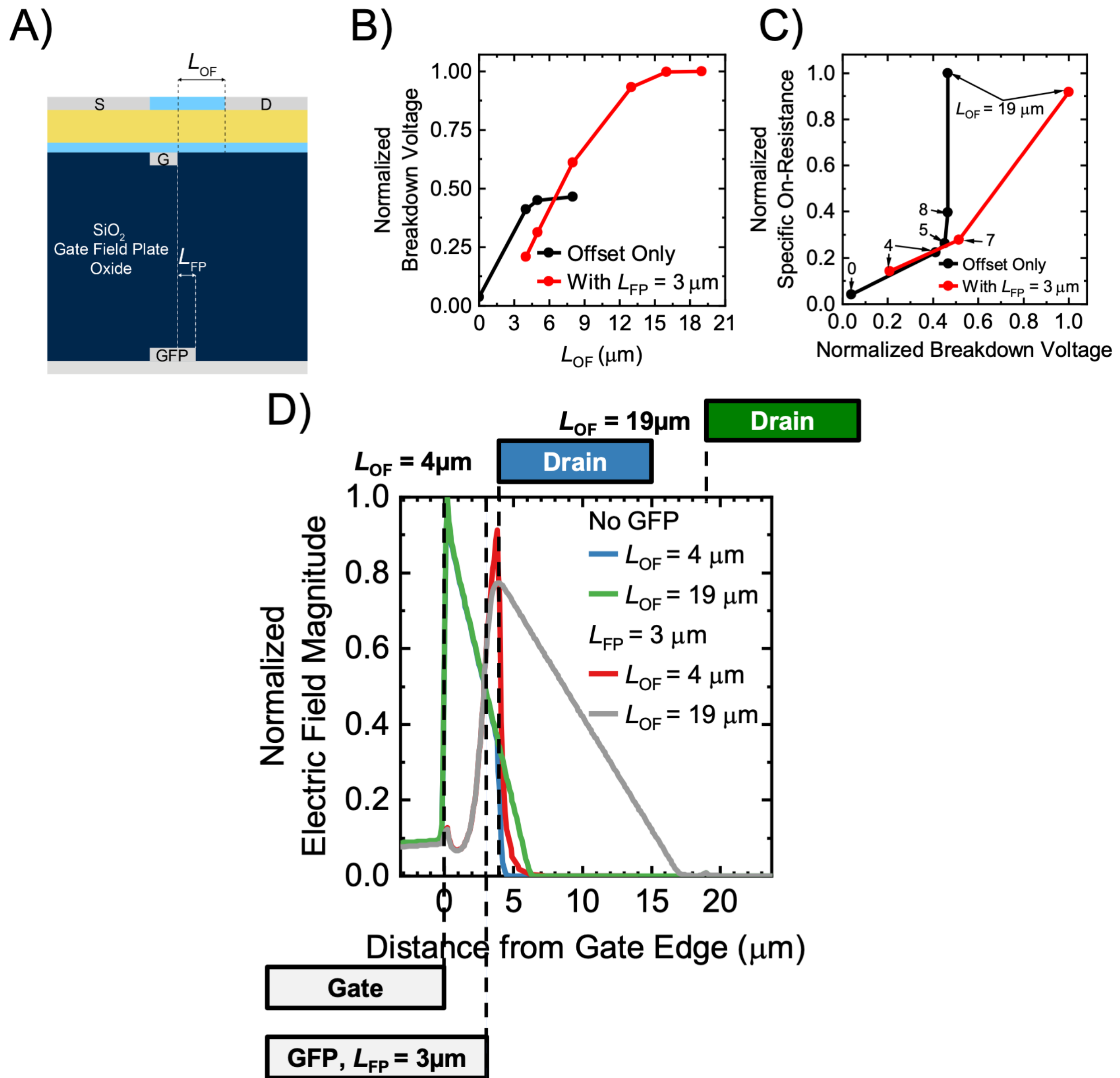


Figure 3.9: A) Diagram of simulated device. Simulation results of devices without a gate field plate and devices with L_{FP} = 3 µm. B) Breakdown voltage as a function of offset. C) Plot showing the breakdown voltage and on-resistance of the devices. D) Normalized electric field between gate and drain edges at breakdown.

As discussed earlier in this chapter, there is a tradeoff between V_{BD} and R_{on} where the highest V_{BD} for a given R_{on} is desired to reduce power loss. When plotting R_{on} versus V_{BD}, as done in Figure 3.3E, devices low on the y-axis and far to the right on the x-axis are desirable. After fabrication of the first-generation HVTFTs, Silvaco Atlas simulations were again used to find design windows

where better devices on the R_{on} versus V_{BD} plot could be found. Devices with cross section as shown in Figure 3.9A were simulated where the gate field plate oxide was 640 nm of SiO_2. As was found earlier in this chapter, V_{BD} saturates for devices without a gate field plate when the non-punch-through field condition is met. Adding the gate field plate with a length past the gate edge, L_{FP}, of 3 μm can spread the electric field, as shown in Figure 3.9D, allowing the devices to achieve higher V_{BD} with extended L_{OF}, Figure 3.9B. Even so, the devices with L_{FP} of 3 μm reach a non-punch-through field condition around L_{OF} = 16 μm, Figure 3.9D, resulting in V_{BD} saturation, Figure 3.9B. Looking at the R_{on} versus V_{BD} plot the only clear advantage of using a gate field plate with an L_{FP} of 3 μm is an increase in V_{BD} capability. The R_{on} still suffers from the large resistance of the offset and is not improved by a gate field plate with L_{FP} of 3 μm.

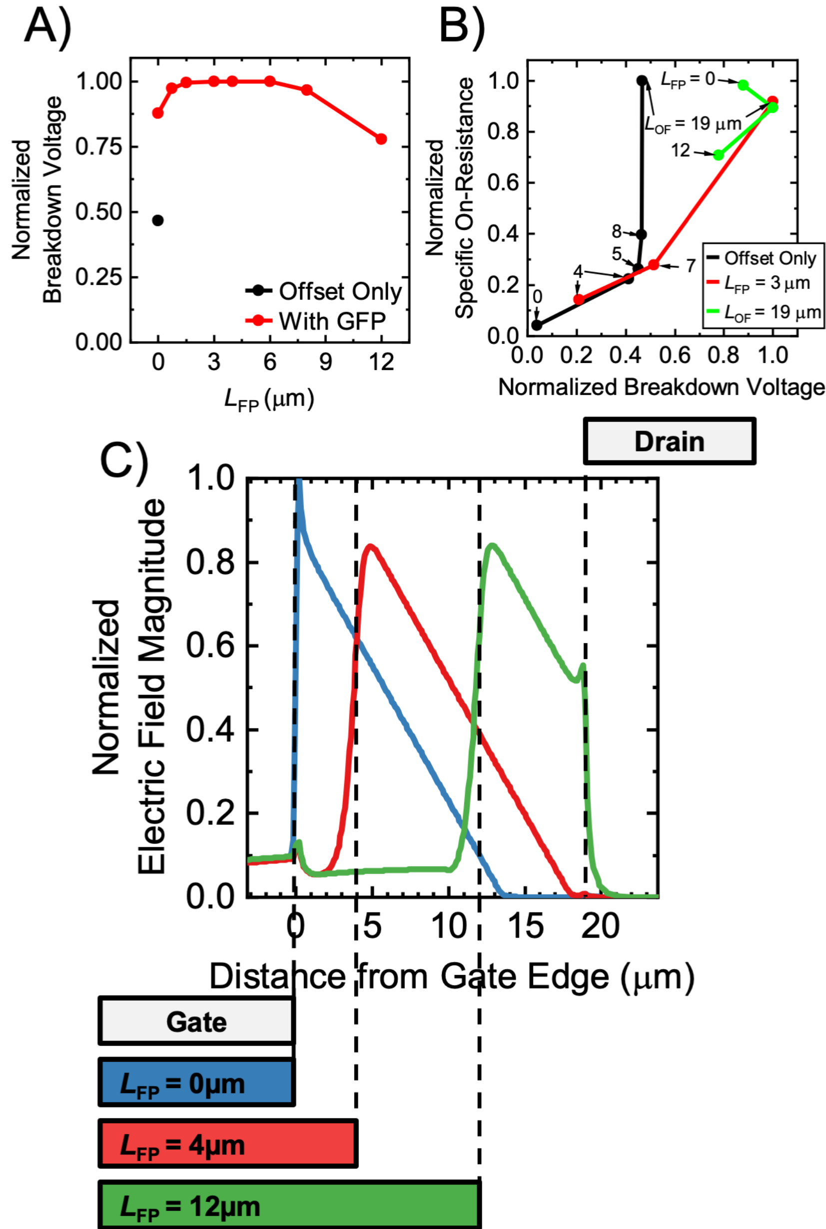


Figure 3.10: A) Breakdown voltage as a function of L_{FP} for devices without the gate field plate structure (black dot) and with various L_{FP} (red symbols). B) Plot showing the breakdown voltage and on-resistance of devices with only an offset (black symbols), with a 3 μm L_{FP} and various L_{OF} (red symbols), and with a 19 μm L_{OF} and various L_{FP} (green symbols). C) Normalized electric field between gate and drain edges at breakdown for simulated devices with a L_{OF} or 19 μm and various L_{FP}.

Further simulations were performed using the structure in Figure 3.9A where L_{OF} was 19 μm, chosen past the non-punch-through condition of a 3 μm L_{FP}, and L_{FP} was varied. Simply by introducing a gate field plate with L_{FP} of 0 μm (aligned with the gate metal), the fringing fields are enough to increase the breakdown voltage by about 1.9 times, Figure 3.10A. The fringing fields

of a gate field plate with L_{FP} of 0 μm spread the electric field an additional approximately 7 μm (blue curve Figure 3.10C) compared to the devices with no gate filed plate (green curve Figure 3.9D). As L_{FP} is extend past the gate edge two distinct separate peaks between the gate edge and the gate field plate edge are observed (red curve Figure 3.10C). Distinct separate peaks result in saturation of V_{BD} (red curve Figure 3.10A). When L_{FP} is long enough to cause punch-through field condition at the drain edge (green curve Figure 3.10C), V_{BD} begins to roll off again (red curve Figure 3.10A). Here, again, we do not see an improvement in R_{on} for a given V_{BD}, Figure 3.10B.

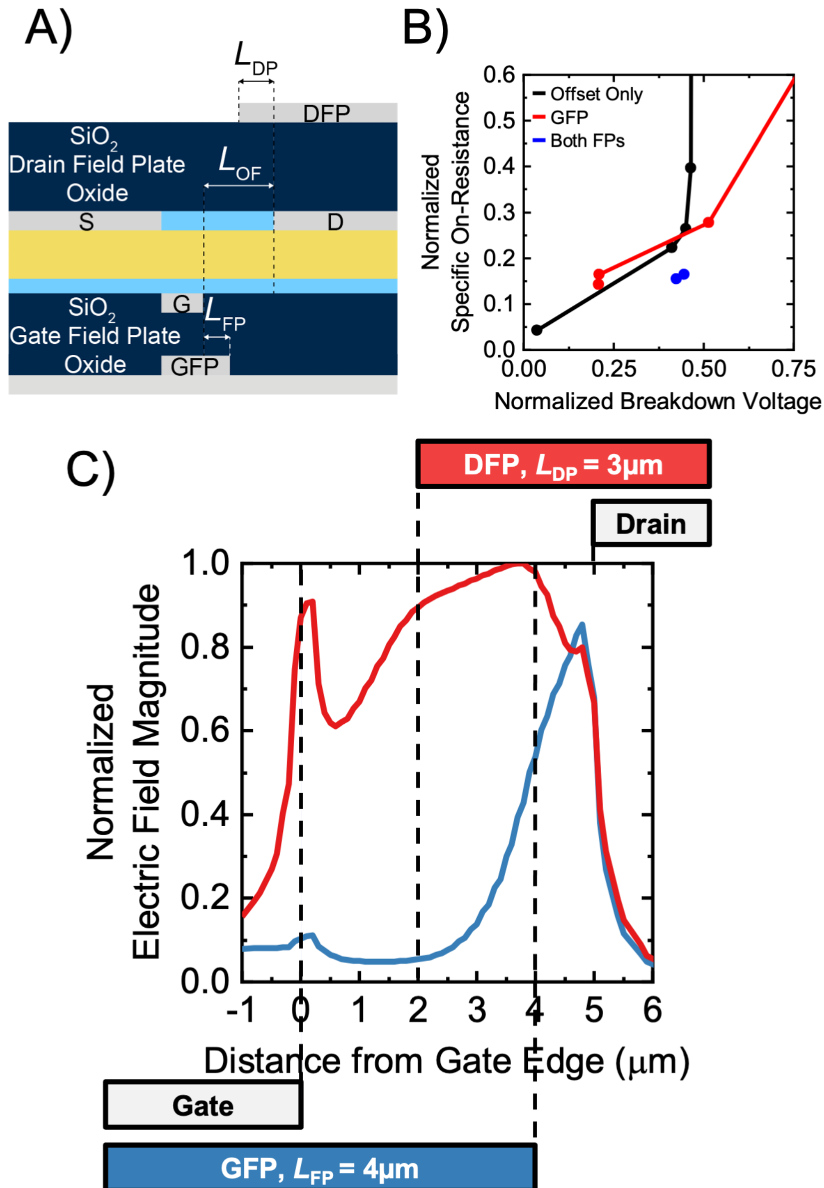


Figure 3.11: A) Diagram of simulated device with both a gate and drain field plate. B) Plot showing the breakdown voltage and on-resistance of various devices. C) Normalized electric field between gate and drain edges at breakdown for simulated devices.

From the previous simulations two things are apparent: a short L_{OF} is required for low on-resistance and a gate field plate is useful for decreasing the on-resistance and increasing the blocking voltage. When combining a short L_{OF} with a gate field plate, the peak electric field shifts to the drain edge (blue curve Figure 3.11C). To more evenly distribute the electric field in the offset region a drain field plate, with length L_{DP} past the drain edge, was added to the simulations in addition to the gate field plate as shown schematically in Figure 3.11A. As shown in Figure

3.11C for a simulated device with L_{OF} of 5 μm and a gate field plate with L_{FP} of 4 μm adding a drain field plate with L_{DP} of 3 μm more evenly distributes the electric field resulting in a V_{BD} increase of about 2.1 times compared to the same structure without the drain field plate. In addition to increasing V_{BD}, this is the first design showing significant improvement in R_{on} (Figure 3.11B). The reduction in R_{on} is due to the drain field plate accumulating a second channel. Further performance improvements may be possible with optimization of all the different dimensions and/or adding more field plates.[128]

3.5 Conclusions

The work in this chapter explored expanding the capabilities of AOS TFTs by using lateral device architectures to create high-voltage TFTs with ZTO active regions deposited by solution-processing. First, Silvaco Atlas simulations were used to model HVTFTs with a gate-to-drain offset. Simulations results show a gate-to-drain offset increased the breakdown voltage by distributing the electric field in the offset region. There is a limit to the highest breakdown achievable by the offset and the on-resistance of the devices suffers. The offset region's conductance cannot be modulated by the gate and therefore its resistance dominates the on-resistance of the ZTO HVTFTs with drain offset.

Fabricated devices based on the simulations showed an unexpectedly low on-current. The low on-current was attributed to depletion of the offset region caused by oxygen adsorbed onto the surface of the semiconductor. Passivation was used to prevent the oxygen adsorption and higher on-current was achieved. Passivated devices with no offset show excellent linear and saturation behavior and have an electron mobility of 11.8 $cm^2V^{-1}s^{-1}$, threshold voltage of -0.4 V, on/off current ratio greater than 10^6, and a breakdown voltage around 45 V. The introduction of a 3 μm

drain offset increased the breakdown voltage to over 100 V. As predicted by the simulation results, the on-resistance increases with increasing offset length.

Finally, Silvaco Atlas was again used to model new HVTFT structures. Gate field plates can be added to the gate-to-drain offset structure to enable higher breakdown voltages by further distributing the electric field in the offset region. There is, however, little improvement in the on-resistance. To reduce the on-resistance a short offset length is required in combination with the gate field plate but under these conditions, the breakdown shifts to the drain edge and there is little improvement in breakdown voltage. Adding a drain field plate to the structure spreads the electric field yielding a higher breakdown voltage and a second electron channel is accumulated by the drain field plate resulting in a significant improvement in on-resistance. Future work could look at co-optimizing all of the dimensions using simulations and then finally device fabrication.

Chapter 4 Enhancement-mode ZTO TFTs with Improved Ambient Stability

4.1 Introduction

While amorphous oxide semiconductors (AOS) are interesting materials for several reasons, e.g. material properties of metal oxide semiconductors plus large-area uniformity,[20], [68] potential applications, as shown in the previous chapter, require high device stability. Changes in humidity during fabrication of AOS TFTs can cause poor electrical performance characterized by large hysteresis, strong depletion-mode behavior, and a kink in the subthreshold region.[34] The degree of moisture sensitivity can be dependent on the active layer thickness.[115] Active layer thickness is also important when a highly conductive back channel is present because as the thickness increases, kinks in the subthreshold region become more pronounced.[129] ZnO TFTs require a thin semiconductor to keep enhancement-mode behavior after passivation using ALD Al_2O_3.[116]

For AOS devices, various passivation layers have been studied to stabilize device characteristics. Devices with sputtered ZTO or IGZO channel layers have shown successful passivation, i.e. minimal changes in device characteristics, with sputtered amorphous zinc-tin-silicon-oxide as the passivation layer.[130] Other work on pulse laser deposition IGZO investigating passivation using Y_2O_3, Al_2O_3, HfO_2, and SiO_2 found Y_2O_3 was the highest performance passivation material when the channel was annealed prior to passivation and the passivation layer went through a post-deposition anneal.[131] These findings lead to the conclusions that the bulk defects should be removed by annealing before passivation and the

passivation layer can remove deep subgap defects from the surface therefore eliminating the subgap photo response during negative bias illumination stress.

There have been many more studies looking at the stability of indium-based AOS deposited using various deposition techniques for TFT applications,[117], [131]–[134] but here, we investigate the back-channel stability of TFTs with various thickness with solution processed zinc-tin-oxide active layers, as an indium-free AOS alternative. Previous work studying film thickness of single-layer solution-processed ZTO has produced films as thin as 20 nm by varying the spin coater speed [23] and down to 5 nm by varying the solution molarity.[115] In this chapter, we vary both the molarity of the solution and number of spin-coated layers to achieve sub-10 nm film thickness.

There are several different solution chemistries that can be used to create ZTO active layers. One popular chemistry uses a chloride-based process but this is undesirable due to the release of harmful byproducts during the process[23], [115] and no solution to device instability for chloride-based processes has been demonstrated.[135] We have chosen a solution chemistry that uses acetate precursors with the ability to be processed over a wide range of conditions while avoiding the creation of harmful byproducts.[77]

In this chapter, we explore depositing sub-10 nm ZTO films using an indium-free acetate-based solution process. The resulting devices were passivated using an alumina passivation layer deposited using an ozone-based atomic layer deposition (ALD) process. The devices passivated using the O_3-based ALD Al_2O_3 layer show enhancement-mode behavior with good bias stress stability, a low hysteresis of 0.85 V, and a field effect mobility, μ_{FE}, of 8.3 cm^{2}V^{-1}s^{-1}.

4.2 Experimental Section

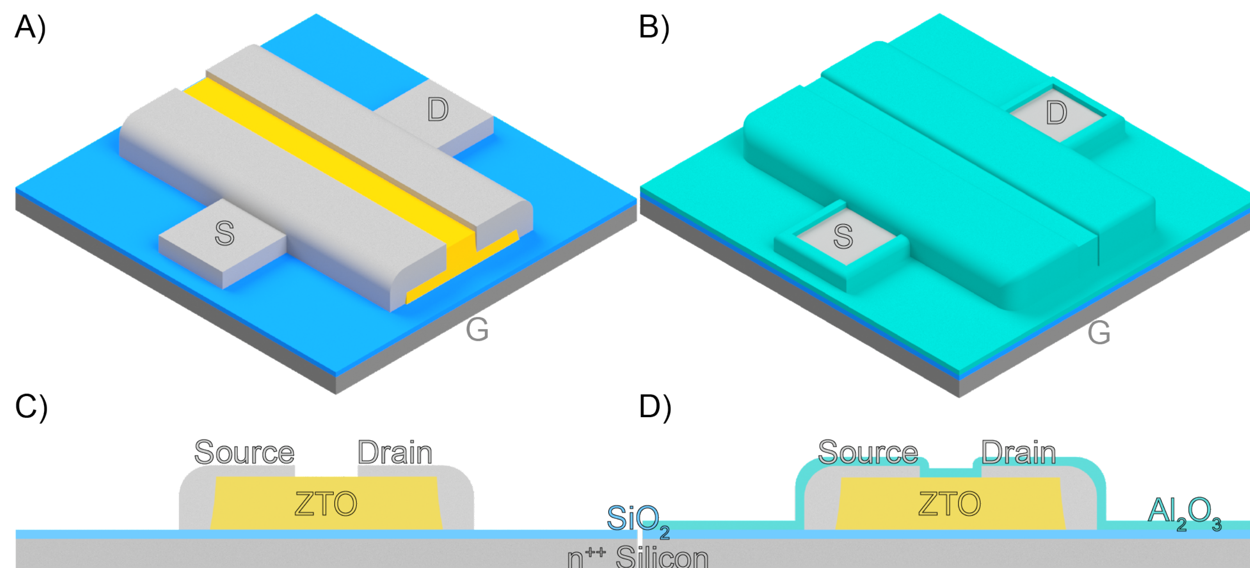


Figure 4.1: A) Schematic and C) cross section diagram of common bottom-gate top-contact TFT. B) Schematic and D) cross section diagram of passivated TFT. The n^{++} silicon substrate and 100 nm of thermally grown SiO_2 act as the gate electrode and insulator, respectively.

Using heavily doped silicon with 100 nm thermally grown SiO_2 layer as the gate and gate insulator, respectively, common bottom-gate, top-contact TFTs with ZTO active layers were fabricated with the structure shown in Figure 4.1A and Figure 4.1C. The deposition of the ZTO active layer followed our previously-reported acetate-based solution with the exception that in this chapter we explore changing the solution molarity and number of spin-coated layers to vary the film thickness.[77] After the 1-hour 520ºC anneal, following the spin-coating of the final layer, the ZTO is patterned using a wet etch process for device isolation. The top source/drain contacts were deposited by sputtering 100 nm of molybdenum and patterned by liftoff. The overlap between the top metal and ZTO layer was chosen to be much greater than the transfer length of Mo to ZTO in order to create low resistance ohmic contacts.[78] Two different deposition techniques were used to explore the use of approximately 30 nm of ALD deposited Al_2O_3 as a passivation layer as illustrated in Figure 4.1B and Figure 4.1D. The first technique is the traditional thermal ALD process where H_2O and trimethylaluminum (TMA) are the ALD precursors used at a process

temperature of 150ºC in an Oxford OpAL ALD system.[133], [136], [137] The second technique, used previously with sputtered ZTO [138] and IGZO [139], is a thermal ALD process that uses ozone as the oxidant, instead of H_2O, at a process temperature of 100ºC in a Veeco Savannah system. A J.A. Woollam M-2000 Ellipsometer was used to measure film thickness. A HP4156A semiconductor parameter analyzer or Keysight B1505A power device analyzer were used to take electrical measurements in the dark at room temperature in an air ambient. Vacuum measurements were taken using a Lake Shore Cryotronics TTPX Probe Station and the HP4156A semiconductor parameter analyzer.

4.3 Thinning of solution-processed ZTO active layer

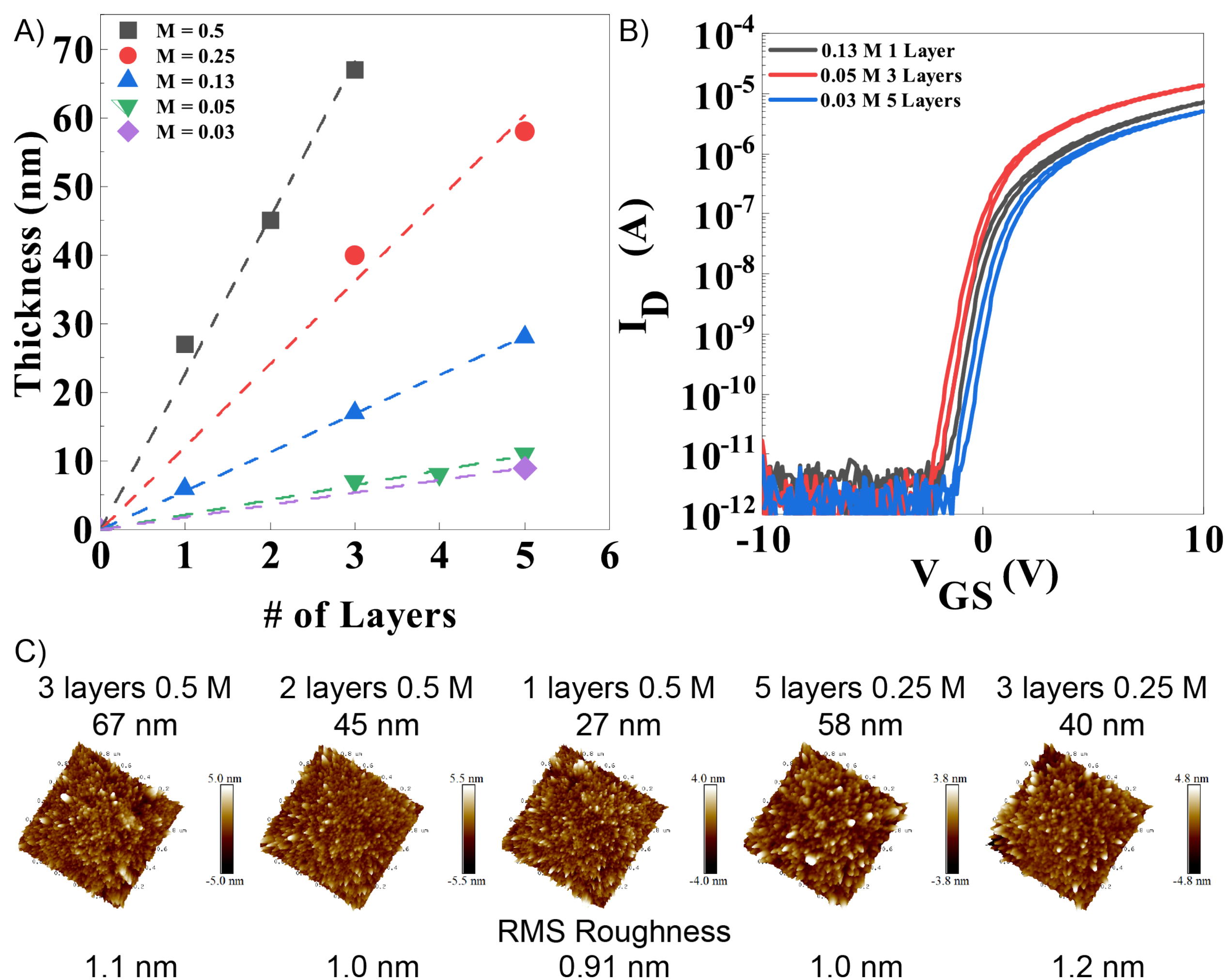


Figure 4.2: A) Measured ZTO film thickness as a function of number of spin-coated layers deposited with solutions with various molarity (M). Symbols indicate experimental data while dashed lines indicate linear fits through the origin. B) Transfer curves of ZTO TFTs with $t_{channel}$ < 10 nm, W/L of 10, and V_{DS} = 1 V. C) AFM measurements of a 1 μm² area indicate a uniform continuous film with RMS surface roughness less than 1.2 nm. Adapted with permission from [30].

Samples were prepared with ZTO deposited using various solution molarity and number of spin-coated layers. The resulting film thickness was measured using ellipsometry and is plotted in Figure 4.2A showing the relationship between the number of spin-coated layers and the final film thickness. For a given molarity, the relationship between thickness and number of spin-coated layers is approximately linear as indicated by the dashed lines in Figure 4.2A. A linear relationship means that, for a given molarity, the thickness of each layer making up the final film is

approximately equal allowing the thickness of the active layer to be easily tuned. The layer thickness is dependent on the molarity of the solution, where a higher molarity results in a thicker layer. To ensure any changes in electrical performance were due to changes in film thickness, rather than a change in the number of layers or solution molarity, devices with similar active layer thickness but various number of layer and solution molarity were measured as shown in Figure 4.2B. The variation seen falls within the device-to-device variation indicating the number of layers and solution molarity does not impact device performance. AFM measurements, Figure 4.2C, on a 1 μm^2 area show a uniform continuous film with RMS roughness less than 1.2 nm, much lower than 3.85 nm measured for a 20 nm thick film previously reported.[23]

4.4 Vacuum measurements and passivation of ZTO TFTs with various active layer thickness

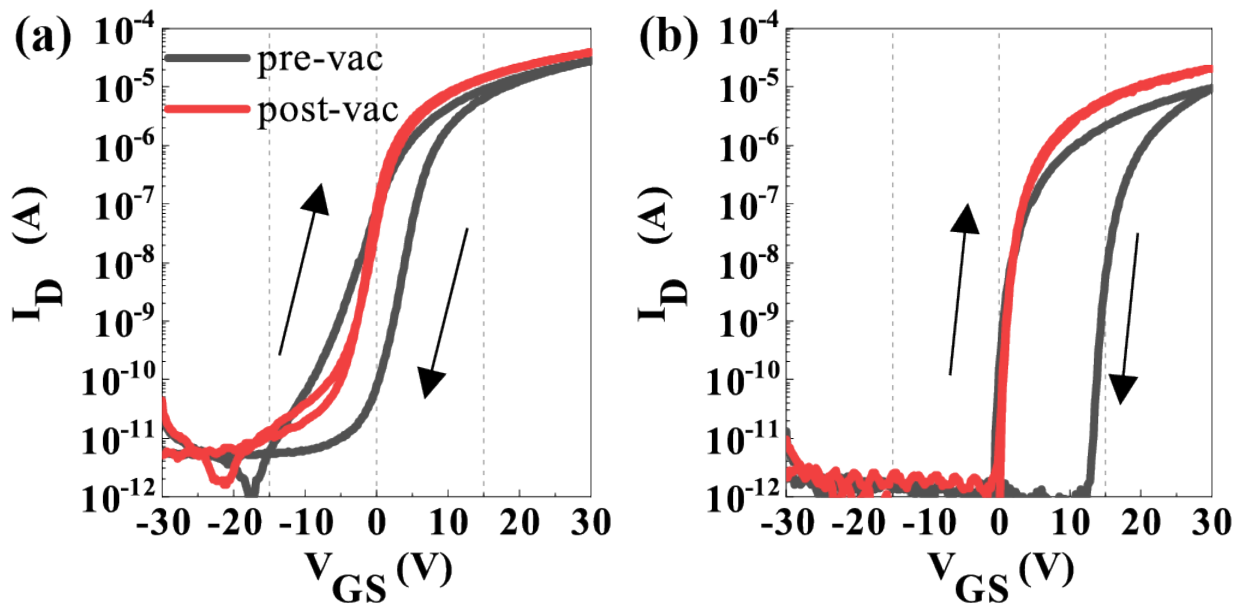


Figure 4.3: Transfer curves of ZTO TFTs as-fabricated in an air environment (pre-vac) and under vacuum after a vacuum treatment (post-vac) with V_{DS} = 1 V. The device in a) has a film thickness of approximately 70 nm and W/L of 10 while b) has a film thickness of approximately 7 nm and W/L of 12.5. From [30] © 2019 IEEE.

To study the impact of environmental oxygen and water on device performance, devices with thick (~70 nm) and thin (~7 nm) active layers were measured both in an air ambient as-fabricated

and under vacuum after a vacuum treatment. The vacuum treatment consisted of keeping the samples under vacuum for approximately 22 hours and, while under vacuum, annealing the samples up to 400 K for approximately 1.75 hours. Transfer curves for as-fabricated devices in an air environment (pre-vac) and vacuum treated samples under vacuum (post-vac) are shown in Figure 4.3. Large hysteresis, measured as the difference between V_{GS} of the forward and reverse sweep required to achieve 100 nA I_D at 1 V V_{DS}, of 5.28 V and 12.65 V is present in the as-fabricated devices under air ambient for the thick and thin films, respectively. When the devices are measured under vacuum after vacuum treatment, the hysteresis is significantly reduced to -0.52 V and -0.05 V for the thick and thin films, respectively, leading to forward and reverse sweeps that are almost completely overlapping. The devices with a thick active layer have an "S" shaped transfer characteristic caused by a kink in the subthreshold region between -15 V and -5 V V_{GS} not apparent for devices with a thin active layer. Kinks in the subthreshold region are caused by traps in the channel that are attributed to remaining adsorbed water.[107]

Hysteresis is expected for as-fabricated AOS devices when measured in an air ambient due to interactions between the back channel and molecules in the environment, such as water and oxygen.[140] When water is adsorbed onto the back channel, it can act as either an electron donor [115] or an acceptor-like trap [97] depending on the active layer thickness [127] and relative humidity of the air.[141] On the other hand, molecular oxygen has only been characterized to act as an electron trap when adsorbed onto the back channel.[97], [115], [127], [141] Under an air environment, these molecules can freely desorb and re-adsorb during V_{GS} sweeps while, when the devices are under vacuum only desorption can happen freely as readsorption is limited by the minimal number of molecules available. During the vacuum treatment, desorption was assisted by

the vacuum annealing process. The reduced hysteresis under vacuum is due to this desorption without readsorption.

The inferior characteristics of the thicker film under vacuum are due, in part, to the remaining adsorbed water that also causes the kink in the subthreshold region as discussed earlier in this chapter. As the thickness of the films decreases, the gate has a greater ability to couple through the bulk of the active layer and control the back channel of the device making thin films less susceptible to these issues and leading to the superior characteristics of the thin film.[142] The devices measured here were the thickest and thinnest films studied and as such we expect films with intermediate thicknesses to perform similarly. The next focus of this chapter is developing a passivation layer to enable the post-vacuum treatment behavior in an air environment without impractical vacuum treatment.

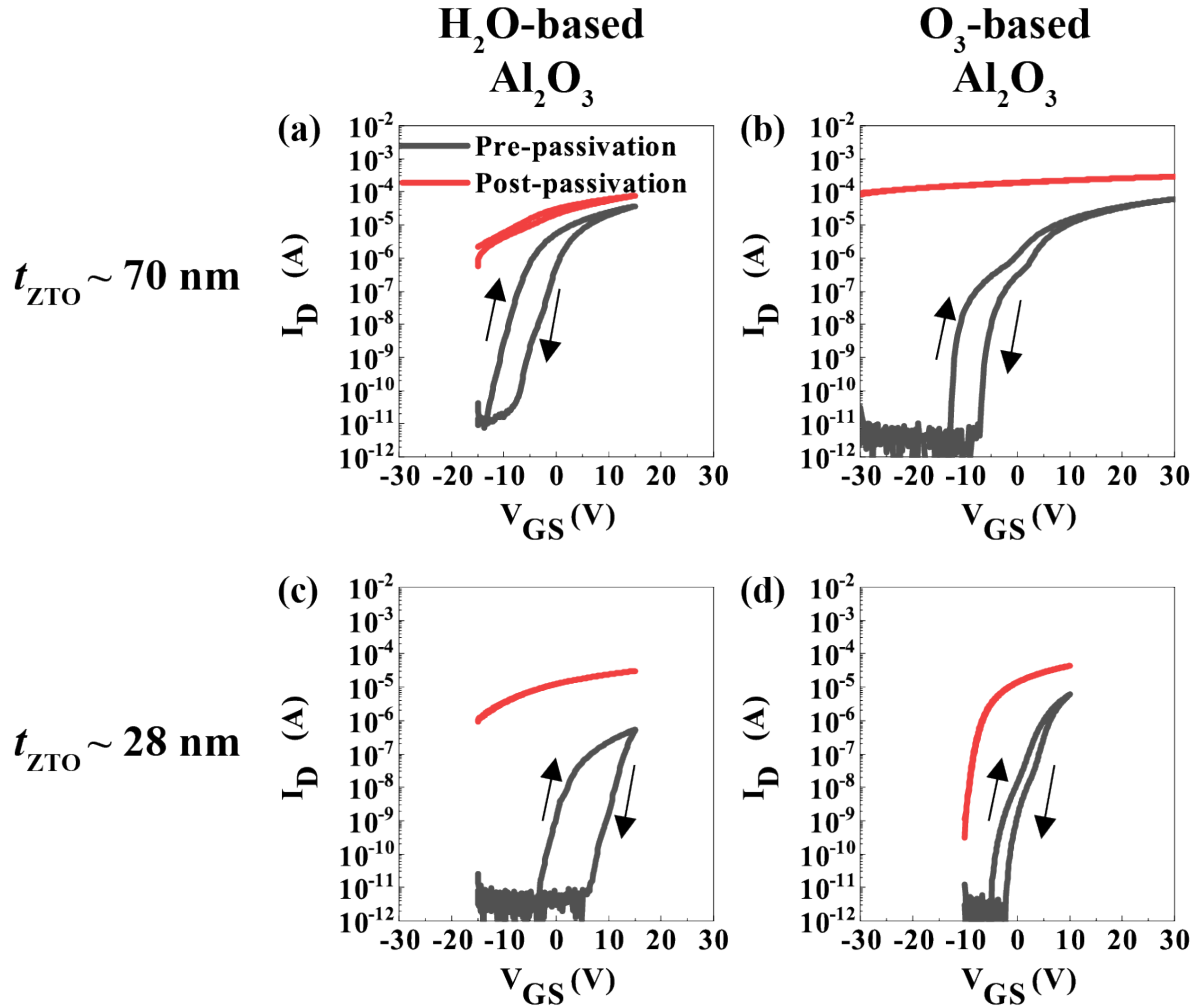


Figure 4.4: Transfer curves of ZTO TFTs in an air environment with V_{DS} = 1 V and W/L of 10 as-fabricated (pre-passivation) and after deposition of approximately 30 nm Al_2O_3 using a) and c) a H_2O-based ALD process and b) and d) an O_3-based ALD process (post-passivation). Devices measured have a film thickness of a) and b) ~ 70 nm and c) and d) ~ 28 nm. The apparent differences in pre-passivation characteristics of devices with the same thickness are caused by device-to-device variation and/or temporal instability of devices without passivation. Adapted from [30].

Samples with a ZTO thickness of approximately 70 nm and 28 nm were passivated using approximately 30 nm of Al_2O_3 deposited using either an H_2O-based or O_3-based ALD process to study which deposition process would lead to device characteristics that are stable and hysteresis-free in an air environment. The samples passivated using the H_2O-based process, Figure 4.4A and Figure 4.4C, are unable to be turned off in the V_{GS} region tested, exhibiting conducting behavior

regardless of film thickness. A more conductive film is caused by an increased number of free carriers, in this case, electrons. The metal precursor used during the ALD process, TMA, is highly reactive and may remove chemisorbed oxygen, or -OH groups, from the ZTO surface that would normally deplete the film and reduce the number of free carriers.[136] Without the chemisorbed molecules causing depletion, the number of free carriers increases and the device becomes more difficult to turn off. Hydrogen generated from the reaction between H_2O and TMA may also be trapped in the ZTO changing the film conductivity.[137] These results make the H_2O-based process an unattractive solution for device passivation.

The O_3-based process, Figure 4.4C and Figure 4.4D, still results in conductive behavior for the passivated device with a 70 nm thick active layer while the passivated 28 nm thick device can be turned off in the V_{GS} range measured. Passivating the 28 nm thick film resulted in a negative V_t shift of 9.9 V, a decrease in hysteresis from 2.03 V to 0.16 V, and a μ_{FE} of 8.6 cm^{2}V^{-1}s^{-1}. The O_3-based process still uses the same highly reactive metal precursor (TMA) that we attributed to the conductive behavior for the H_2O-based passivation, but ozone may reintroduce the -OH groups that are stripped form the ZTO surface by TMA resulting in the better switching ability when the O_3-based process is used.[138], [139] While the 28 nm film results in switchable devices, the device turn-on is near -10 V and must be closer to 0 V for enhancement-mode behavior.

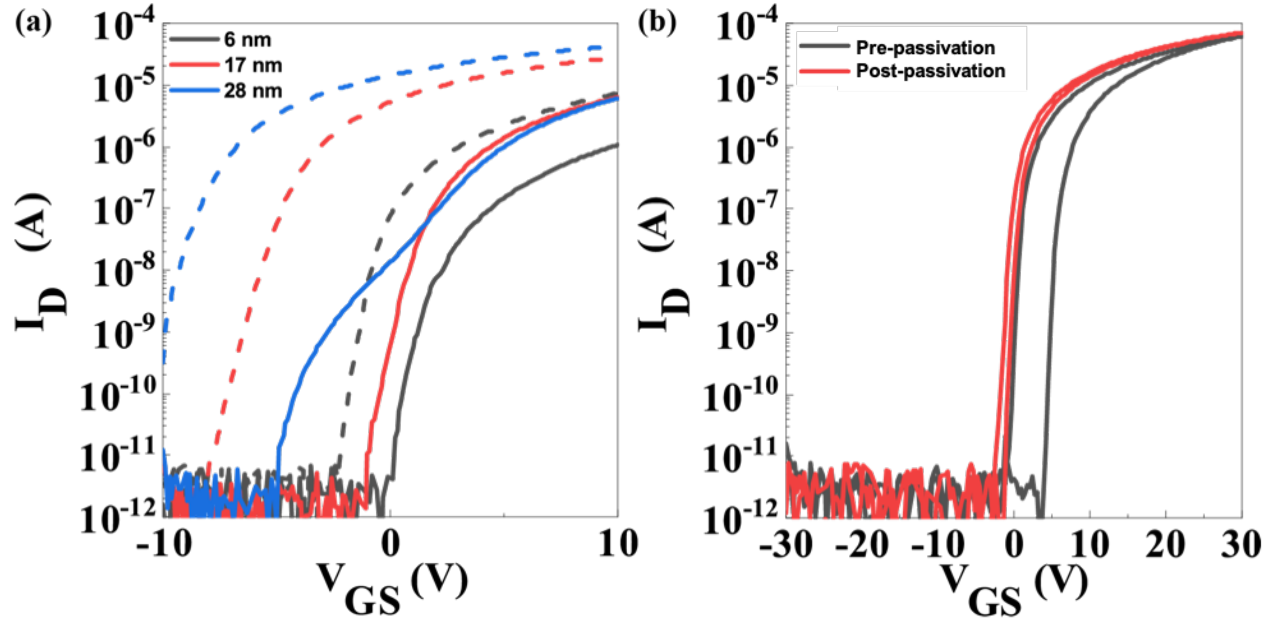


Figure 4.5: Transfer curves with V_{DS} = 1 V of ZTO TFTs with a) various thickness before passivation (solid line) and after passivation (dashed line) using an O_3-based Al_2O_3 ALD process. B) I-V curves showing the hysteresis of the 6 nm thick device in a) before passivation (black lines) and after passivation (red lines). Adapted with permission from [30].

To create passivated devices with enhancement-mode behavior, devices with active layer thickness of 6 nm, 17 nm, and 28 nm were measured before passivation and after passivation using the O_3-based Al_2O_3 ALD process, Figure 4.5. As the thickness of the film increases, the V_t of the as-deposited devices becomes more negative, Figure 4.5A. This relationship between V_t and film thickness is not unusual for AOS devices and has been attributed to a decrease in the number of traps in thicker films [143] resulting in an increased number of free carriers requiring more negative voltage to turn-off the device.[23], [144] As with the thicker films studied previously in this chapter, the as-deposited 28 nm thick film shows a kink in the subthreshold current near 0 V V_{GS} explained by traps caused by water adsorption. The subthreshold slope (*SS*) of the 6 nm and 17 nm devices do not greatly vary with passivation, while the 28 nm device shows a decrease in *SS* from 0.77 V dec^{-1}, before passivation, to 0.38 V dec^{-1}, after passivation. The reduction in *SS* for the 28 nm device can be explained by the removal of the kink in the subthreshold current likely caused by a reduction of trap density in the bulk of the film or at the back interface.[117] The pre-

passivation trend of thicker films causing more negative V_t persists post-passivation with all devices showing a negative shift caused by passivation. The negative shift is explained by an increase in free carriers caused by the desorption of surface species as discussed earlier in this chapter. Forward and reverse sweeps for the pre- and post-passivation 6 nm device are shown in Figure 4.5B. The post-passivation 6 nm device exhibits the best performance with a μ_{FE} of 8.3 $cm^2V^{-1}s^{-1}$, V_t of 5.5 V, and hysteresis of 0.85 V.

4.5 Bias stress stability of solution-processed ZTO TFTs

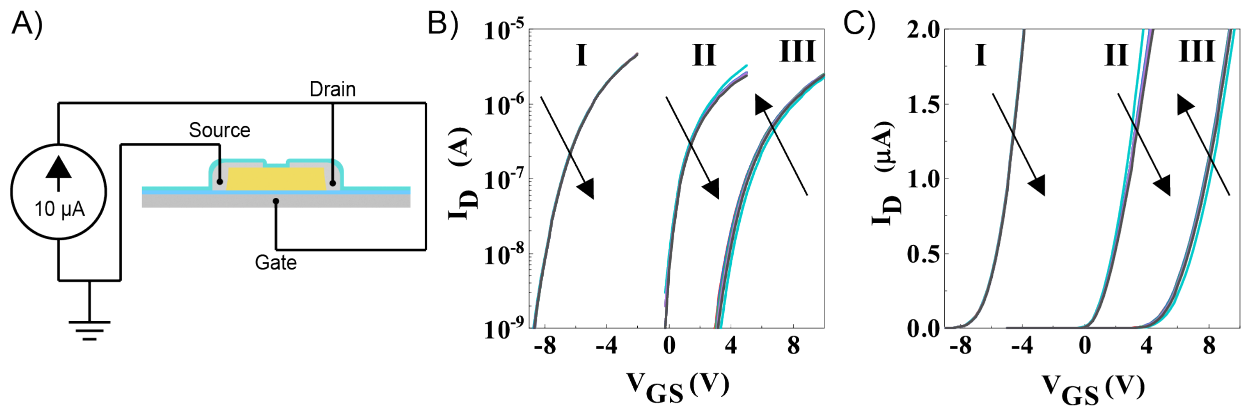


Figure 4.6: A) Schematic illustration of constant current bias test setup used. Transfer curves of ZTO TFTs with V_{DS} = 1 V during constant current stress testing in B) semi-logarithmic and C) linear scale. I and II are 28 nm and 7 nm thick devices, respectively, passivated using the O_3-based process. III is the same 7 nm thick film II but prior to passivation. Adapted from [30].

To test the stability of the fabricated devices, both before passivation and after passivation using the O_3-based process, a constant current stress test was used. The test was performed in the dark at room temperature with the source grounded and a constant current of 10 µA applied to the gate and drain in parallel as illustrated in Figure 4.6A. Transfer curves with a V_{GS} range of approximately $V_t \pm 5$ V, where V_t is defined here as the value of V_{GS} required to produce 10 nA I_D, were taken after every 1000 s of constant current stress for a total of 5000 s, an appropriate time to observe device instability.[115], [132], [134] The resulting transfer curves for passivated devices with a thickness of 28 nm (I) and 7 nm (II) and for a 7 nm device without passivation (III)

are show in Figure 4.6B and Figure 4.6C. The change in threshold voltage, ΔV_t, after 5000 s constant current stress for the thin device improves from -0.18 V to 0.08 V after O_3-based passivation and remains positive while the 28 nm device shows even smaller V_t, 0.03 V, however the device behaves in depletion mode. These results indicate an Al_2O_3 layer deposited using an O_3-based ALD process can be used to passivation thin ZTO TFTs to enable enhancement mode devices with improved V_t stability compared to devices without passivation.

4.6 Conclusions

By varying the solution molarity and number of spin-coated layers, solution processed ZTO TFTs were fabricated with active layer thickness as thin as 6 nm. The resulting device characteristics were independent of the solution molarity and number of layers but were dependent on film thickness where V_t was more negative with increasing film thickness. As-fabricated devices show hysteresis as large as 12.65 V at 100 nA I_D when V_{DS} = 1 V. A vacuum treatment was used to study the impact of the device back channel on transfer characteristics. The hysteresis measured after vacuum treatment was greatly reduced to -0.05 V due to desorption of molecules at the back channel without readsorption. To obtain devices that are stable and hysteresis-free in an air ambient, passivation using ALD deposited Al_2O_3 was studied.

When the Al_2O_3 back channel passivation layer was deposited using an ALD process that used H_2O as the oxidant, the resulting ZTO films were conductive. The conductive behavior was attributed to the highly reactive metal precursor, TMA, stripping the back channel of molecules that would otherwise deplete the ZTO film resulting in an increased number of free carriers. An O_3-based process, on the other hand, resulted in normal TFT behavior with a μ_{FE} of 8.3 $cm^2V^{-1}s^{-1}$, V_t of 5.5 V, and a hysteresis of 0.85 V. As seen with as-deposited devices, the threshold voltage decreased with increasing film thickness and the devices all exhibited a negative V_t shift after

passivation. The O_3-based passivation layer also improved stress stability indicating an Al_2O_3 layer deposited using an O_3-based ALD process can be used to passivate thin ZTO TFTs to enable enhancement mode devices with improved V_t stability. Further work investigating less reactive metal precursors for Al_2O_3, e.g. dimethylaluminum hydride [145] or dimethylaluminum isopropoxide,[146] or for other dielectrics [131] in combination with thin active layers could result in further improvement to air-stable enhancement mode devices. Additionally, materials analysis, e.g. XPS, could be used to verify chemical composition and co-ordination changes at the back channel due to different ALD processes.

Chapter 5 Robustness of Passivated ALD Zinc Tin Oxide TFTs to Aging and Bias Stress

5.1 Introduction

In Chapter 2 we developed high-performance ALD films necessary for beyond-display technologies and in Chapter 4 we used passivation to improve the ambient stability of the devices. To apply these devices to the applications introduced in Chapter 1, devices with excellent temporal and bias stress stability are necessary. Here, by device temporal stability, we mean any changes in threshold voltage, V_t, field-effect mobility, μ_{FE}, and subthreshold swing, *SS*, that occur due solely to aging. In contrast, device bias stress stability is a measure of the change in those same parameters due to bias stress.

Temporal and bias stress stability can vary with ambient atmosphere [34], thickness of the active layer [115], [127], the active layer structure [147], and passivation [130], [131]. Ambient dependency, as discussed in Chapter 4, comes from interactions with water and oxygen molecules where water can act as an electron donor [115] or an acceptor-like trap [97] and oxygen acts as an electron trap [97], [115], [127]. In Chapter 4 we applied passivation layers, as others have, to prevent interactions with ambient molecules [115], [130], [131], [136]. The bias stress stability is dependent on the stress time and magnitude where longer stress times and larger magnitudes generally result in larger changes [115], [127]. These changes can result from creation of defect states near the gate insulator/semiconductor interface [148], charge trapping in the gate insulator [149], or interactions with ambient molecules [150].

As the stability can also vary with deposition technique and postdeposition annealing [151], it is important to study the stability of each promising technique. ALD is one of the most promising

techniques because it is a low-temperature vapor-phase deposition method allowing for conformal and uniform thin-films with precise interfaces, stoichiometries, and thicknesses [40]. Only one previous study examined the stability or reliability of ALD ZTO TFTs and was limited to studying negative bias stability (NBS) [28]. The NBS of ALD ZTO TFTs is of limited interest because it is well known that holes cannot be readily generated without illumination in n-type AOS because of a high density of deep subgap states [152]. Furthermore, no previous study on ALD ZTO TFTs has explored passivation layers. Therefore, a more thorough investigation of ALD ZTO TFT temporal and bias stress stability, including a passivation layer, is required.

In this study, we examine the temporal and bias stress stability of ALD ZTO TFTs prepared under two different sets of process conditions, with and without a passivation layer. Devices without a passivation layer show minor changes in V_t and ΔV_c during the first 25 days of aging in a dark air ambient, after which they stabilize. Passivation greatly improves the temporal stability and robustness to PBS but also results in a one-time decrease in V_t and increase in SS and contact resistance, extracted using the transmission line method. Silvaco Atlas simulations are used to show that these one-time changes in V_t and SS are likely due to back-channel interface states induced during deposition of the passivation layer. NBIS is reduced by using optimal ZTO process conditions, but is not eliminated by passivation. The work presented here demonstrates the excellent temporal and bias stress stability of passivated ALD ZTO TFTs, which paves the way for their adoption in thin-film electronics for beyond-display technologies.

5.2 Experimental Section

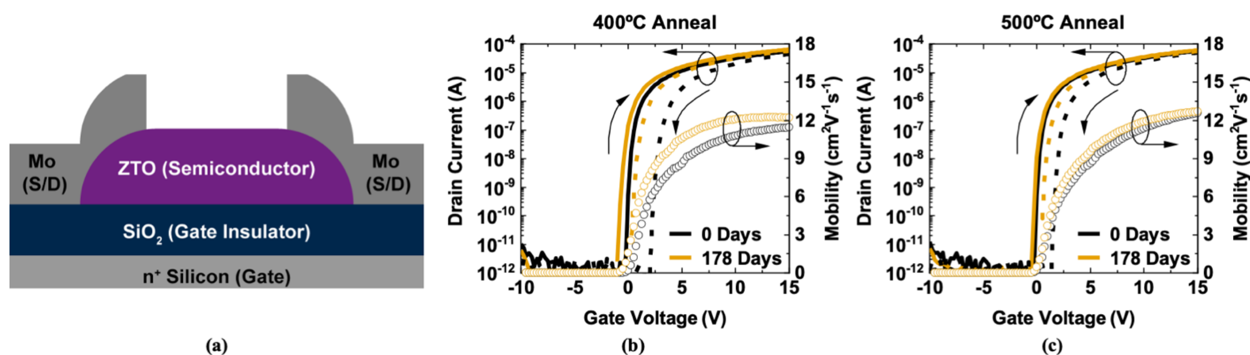


Figure 5.1 (a) Schematic illustration of a ZTO TFT cross section with bottom-gate top-contact structure. Representative transfer characteristics (I_D-V_{GS}) with V_{DS} = 1 V are plotted on the left *y*-axis for devices with ZTO annealed at (b) 400ºC and (c) 500ºC. The forward *I*-*V* curves are indicated by the solid lines and the reverse *I*-*V* curves are indicated by the dashed lines. Linear field effect mobility extracted from these *I*-*V* curves are plotted on the right *y*-axis using open circles. From [153].

TFTs were fabricated on heavily doped n^+ Si where approximately 100 nm of thermal oxide was grown to act as the gate and gate insulator, respectively, in a bottom-gate top-contact structure schematically illustrated in Figure 5.1(a). The active layer, approximately 12 nm of ZTO, was deposited by ALD at a deposition temperature of 150ºC using a hybrid thermal H_2O and O_2-plasma process with a cycle ratio yielding a film with approximately 21 at. % Sn content, as described in Chapter 2. The ZTO films were then wet-etched for device isolation before being annealed at either 400 or 500ºC on a hotplate in air in a custom-built moisture-controlled glovebox with less than 20% relative humidity (Chapter 2). Finally, approximately 100 nm of molybdenum was deposited by sputtering and patterned by lift-off to form source/drain ohmic contacts [78]. Devices have channel lengths, L, and widths, W, of 10 and 120 µm, respectively, unless otherwise stated. Passivated devices were encapsulated with approximately 30 nm of Al_2O_3 deposited by ALD at 100ºC in a Veeco Savannah system using an ozone process [30], chosen in Chapter 4 to reduce the V_t shift introduced by passivation [154]. Samples were stored at room temperature in a dark air ambient between measurements.

Temporal stability and transmission line method (TLM) measurements were taken using a Keysight B1505A power device analyzer while bias stress measurements were taken using an HP4156A semiconductor parameter analyzer. All measurements were taken at room temperature in air using continuous voltage sweeps. When both forward and reverse *I-V* curves are shown, the measurement was first taken in the forward direction, negative to positive V_{GS}, immediately followed by the reverse direction, positive to negative V_{GS}. Positive bias stress (PBS) was applied by biasing the gate at +20 V while the source and drain were kept at 0 V. Negative bias illumination stress (NBIS) was applied by biasing the gate at -20 V while the source and drain were kept at 0 V under illumination of a green LED (520 nm) with an optical power density of 900 μW cm^{-2}. All other measurements were taken in the dark.

The linear field-effect mobility, μ_{FE}, is extracted using the equation $\mu_{FE} = (dI_D/dV_{GS})L(WC_{ox}V_{DS})^{-1}$ where C_{ox} refers to the oxide capacitance per unit area and dI_D/dV_{GS} is the slope of the I_D-V_{GS} curve in the linear region. Reported μ_{FE} values were taken using a gate voltage range of 13 V < V_{GS} < 15 V with V_{DS} = 1 V, unless otherwise stated. Threshold voltage, V_t, is reported as the x-axis intercept of a linear fit to the linear region of an I_D-V_{GS} sweep. Subthreshold swing, *SS*, is taken as the inverse of the logarithmic rate of device current turn-on, in units of volts per decade of current. Hysteresis, ΔV_C, is defined as the difference in the value of V_{GS} at I_D = 100 nA between the reverse and forward sweeps.

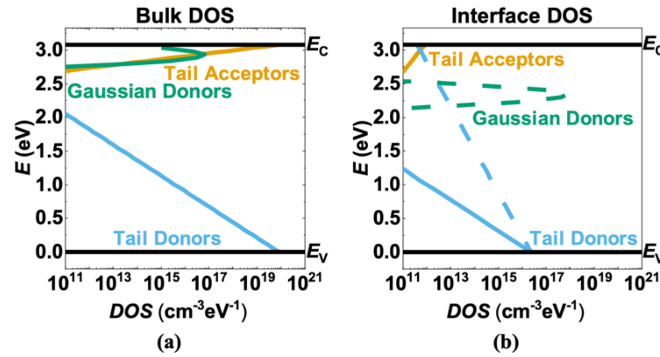


Figure 5.2 (a) Band structure of bulk ZTO and (b) interfaces used in Silvaco ATLAS simulations. For (b), solid lines indicate the semiconductor/gate insulator interface (BG) used in all simulations while the dashed lines indicate the semiconductor/passivation interface (BC) used in simulations including a passivation layer. From [153].

Silvaco ATLAS was used to conduct 2-D numerical simulations of the TFTs to understand the changes in device performance with the addition of a passivation layer. Simulation parameters from [155], [156] were used as a starting point and were then modified to fit the device characteristics presented here. The final band model of the subgap states is shown in Figure 5.2 using the parameters found in Table 5.1 where *BG* refers to the ZTO/gate insulator interface, *BC* refers to the ZTO/passivation interface, and *IT* refers to parameters applied to both *BG* and *BC* where *BC* parameters were only applied to simulations that include a passivation layer.

Table 5.1 Parameters used in Silvaco Atlas simulations. From [153].

Symbol (Unit)	Description	Value
μ_n (cm^{2}V^{-1}s^{-1})	Electron Mobility	13.46
N_C/N_V (cm^{-3})	Conduction/Valance Band Effective DOS	4.14×10^{18}
E_G (eV)	Band Gap	3.08
N_{TA}/N_{TD} (cm^{-3}eV^{-1})	Tail Acceptor/Donor State Peak Density	8.25×10^{19}
W_{TA} (eV)	Tail Acceptor State Width	0.019
W_{TD} (eV)	Tail Donor State Width	0.1
N_{GD} (cm^{-3}eV^{-1})	Gaussian Donor State Peak Density	6.5×10^{16}
E_{GD} (eV)	Gaussian Donor State Peak Position	2.93
W_{GD} (eV)	Gaussian Donor State Peak Width	0.05
$N_{TA,IT}$ (cm^{-3}eV^{-1})	IT Tail Acceptor State Peak Density	8.34×10^{11}
$N_{TD,IT}$ (cm^{-3}eV^{-1})	IT Tail Donor State Peak Density	2.25×10^{16}
$W_{TA,IT}$ (eV)	IT Tail Acceptor State Width	0.19
$Q_{F,BG}$ (cm^{-2})	BG Fixed Charge	-5.20×10^{10}
$W_{TD,BG}$ (eV)	BG Tail Donor State Width	0.1
$Q_{F,BC}$ (cm^{-2})	BC Fixed Charge	2.38×10^{11}
$W_{TD,BC}$ (eV)	BC Tail Donor State Width	0.28
$N_{GD,BC}$ (cm^{-3}eV^{-1})	BC Gaussian Donor State Peak Density	6.5×10^{17}
$E_{GD,BC}$ (eV)	BC Gaussian Donor State Peak Position	2.334
$W_{GD,BC}$ (eV)	BC Gaussian Donor State Peak Width	0.05

5.3 Results and Discussion

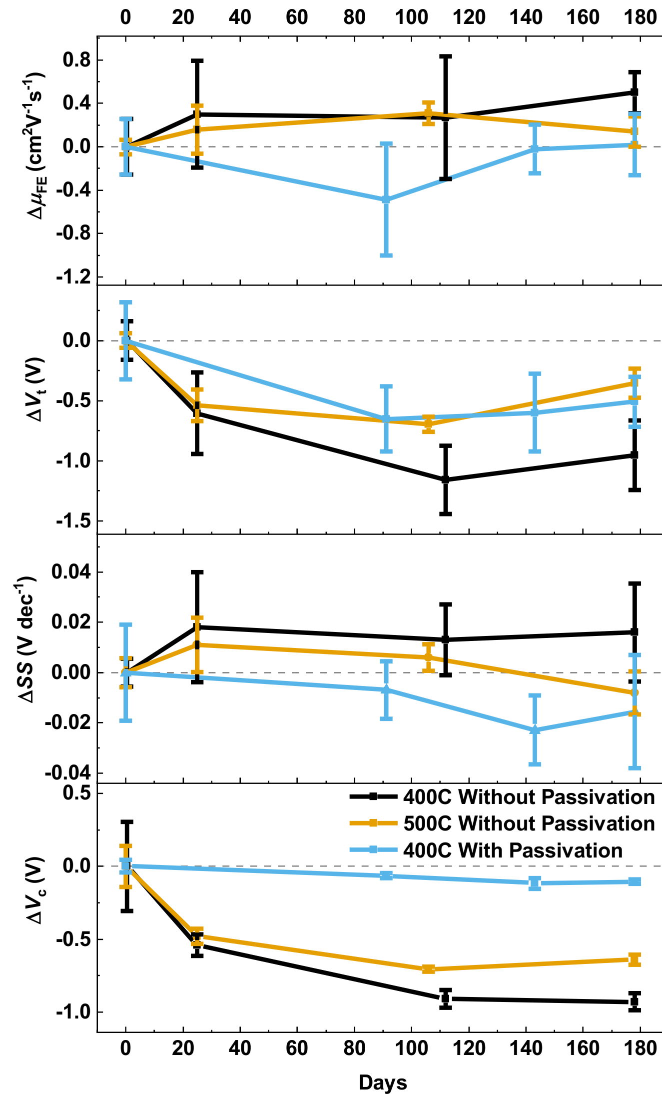


Figure 5.3 Changes in electrical characteristics of TFTs with aging. Symbols indicate the average of 5 measured devices and error bars indicate the standard deviation. From [153].

The transfer characteristics for devices without passivation and annealed at 400 and 500ºC are shown in Figure 5.1(b) and Figure 5.1(c), respectively, and are summarized in Table 5.2 for 0 and 178 days of aging. The excellent performance of unaged devices has been discussed in Chapter 2. For both samples without passivation, the μ_{FE} and *SS* before and after 178 days of aging agree within the measured standard deviation. (Five devices of each type were measured on each date.) The stability of μ_{FE} indicates the bulk tail acceptors at the conduction band edge do not change

with time [157] while the stability of *SS* indicates a stable semiconductor/gate insulator interface [117]. There are, however, statistically significant decreases in V_t and ΔV_c within the first 25 days of aging (Figure 5.3).

Table 5.2 Electrical characteristics of TFTs. From [153].

		μ_{FE} ($cm^2V^{-1}s^{-1}$)	V_t (V)	*SS* ($V\ dec^{-1}$)	ΔV_c (V)
400ºC without passivation	**0-day**	11.8	3.03	0.220	2.18
	178-days	12.2	2.08	0.235	1.25
	Change	0.4	-0.95	0.015	-0.92
500ºC without passivation	**0-day**	12.4	3.73	0.223	1.59
	178-days	12.5	3.37	0.215	0.949
	Change	0.1	-0.36	-0.008	-0.641
400ºC with passivation	**0-day**	10.2	1.32	0.473	1.18
	178-days	10.3	0.815	0.458	1.07
	Change	0.1	-0.505	-0.015	-0.11

There are at least two possible explanations for a decrease in V_t with aging. The first is adsorption of water molecules that would then act as electron donors [127]. This explanation is unlikely to apply here because water has been shown to act as an electron donor only in thicker AOS films [127] and adsorption/desorption of water should also correspond to an increase in hysteresis [97], which is not seen for these devices (Figure 5.3). The other, more likely, explanation is an increase in the oxygen vacancies that are native defect dopants and the main contributor to free electrons in AOS materials [158]. As ΔV_t stabilizes after 25 days of aging (Figure 5.3), the concentration of oxygen vacancies must reach an equilibrium value within the first 25 days due to kinetic constraints or a self-limiting reaction [159]. Hysteresis, however, continues to vary after 25 days of aging (Figure 5.3) because of interactions between ambient molecules and the exposed AOS surface, commonly referred to as the back-channel, requiring passivation to inhibit these interactions [30], [127].

As the 400 and 500ºC annealed devices without passivation show similar trends with aging, studies implementing an Al_2O_3 passivation layer were only performed on devices with a 400ºC

anneal as those are within the 450ºC thermal budget of 3D monolithic integration [69]. The sample with passivation exhibits V_t temporal stability, in addition to the μ_{FE} and *SS* temporal stability also exhibited by the samples without passivation (Figure 5.3). The passivation process may speed up or inhibit the creation of oxygen vacancies that resulted in the V_t instability of the samples without passivation, reaching an equilibrium value without the need for aging. The only parameter that does vary with aging is ΔV_C, which decreases in the first 100 days of aging and then stabilizes. As the passivation layer inhibits interactions with ambient molecules, the source of hysteresis in passivated devices must come from another source, such as trapping and detrapping of electrons into defect states at the BC that may reduce with time [159], [160].

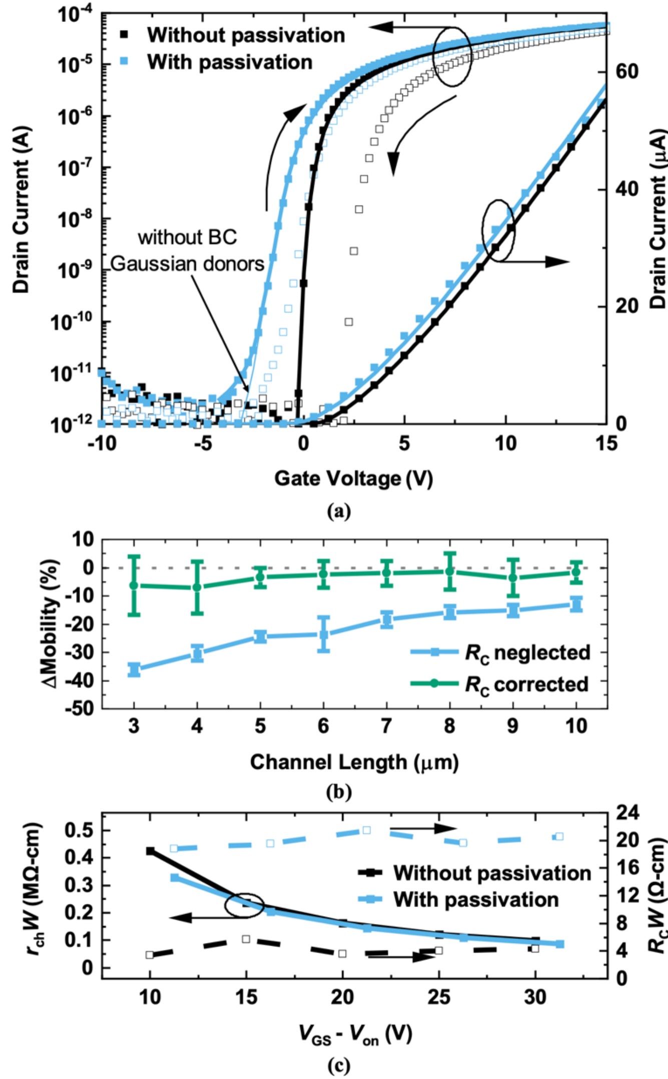


Figure 5.4 (a) Experimental (symbols) and simulated (lines) I_D-V_{GS} curves of 0 day 400ºC annealed ZTO devices. Closed symbols indicate forward sweeps while open symbols indicate reverse sweeps. The without passivation data is the same as the I_D-V_{GS} data in Figure 5.1(b). (b) Percent Change in μ_{FE} with passivation as a function of channel length for 0 day 400ºC annealed ZTO devices. Symbols and error bars indicate averages and standard deviations of five devices, respectively. c) Width normalized channel resistance (left *y*-axis) and contact resistance (right *y*-axis) as a function of V_{GS}-V_{on} as extracted using transmission line method for 0 day 400ºC annealed ZTO devices. From [153].

Transfer characteristics for 400ºC annealed devices with and without passivation are shown in Figure 5.4(a). From these transfer curves, there is a perceptible decrease in V_t and ΔV_c and increase in *SS* with passivation. The reduction of ΔV_c with passivation is an expected result as the main contributor to hysteresis for the devices without passivation, interactions between ambient molecules and the back-channel, is blocked by passivation and is now attributed to BC defect states

[97]. Silvaco ATLAS simulations (Figure 5.4 (a)) with parameters listed in Table 5.1 were used to explain the change in *SS* and V_t with passivation. The simulated Gaussian distribution of donor states at the BC (Figure 5.2(b)) create a second parallel channel resulting in a kink in the subthreshold I_D between -5 and -2 V V_{GS} (Figure 5.4(a)) while the tail donors increase the *SS* of the main channel [161]. The parallel negative shift in V_t was modeled by a positive fixed charge at the BC and may result from reactions with highly reactive trimethylaluminum or ozone [16] or positive fixed charge in the bulk Al_2O_3 [162]. The kink in the subthreshold I_D is no longer present in the aged sample, further indicating the reduction of *BC* states with time. We should note that there was no increase in *SS* with passivation for the solution-processed devices in Chapter 4. This is because the solution-processed devices without passivation already have a large *SS* caused by a large number of defects making the further contribution of back-channel defects negligible.

A statistically relevant reduction in μ_{FE}, unperceivable in Figure 5.4(a), from 11.8 to 10.2 $cm^2V^{-1}s^{-1}$ also occurs with passivation (Figure 5.4 (b)). The change in μ_{FE} with passivation becomes more dominant as L decreases as shown in Figure 5.4 (b). When μ_{FE} decreases with decreasing L, the apparent μ_{FE} degradation is caused by voltage division between the channel resistance, r_{ch}, that scales with L and the contact resistance, R_C. As L decreases, R_C becomes a larger portion of the total resistance, creating a voltage drop effectively reducing the voltage, V_{DS}, across the channel by $I_{DS}R_C$. The μ_{FE} equation neglects R_C but can be corrected for this voltage drop by replacing V_{DS} with V_{DS}-$((R_C V_{DS})R_{Tot}^{-1})$, where $R_{Tot} = R_C + r_{ch}L$ [78]. TLM measurements were used to extract r_{ch} and R_C as shown in Figure 5.4(c). As expected, for an n-type device with ohmic contacts, r_{ch} decreases with increasing V_{GS} while R_C stays constant. While r_{ch} does not change with passivation, indicating the bulk ZTO is unchanged, there is an approximate five times increase in R_C after passivation. Using the extracted R_C values, a corrected μ_{FE} is calculated and

plotted in Figure 5.4 (b). The corrected μ_{FE} is within one standard deviation of 0% change in mobility indicating that the five times increase in R_C may account for the apparent decrease in μ_{FE}.

During the passivation process, the sample is placed in an ALD chamber and exposed to a vacuum environment at 100ºC. These conditions may cause an increase in contact resistance with passivation. To test whether these conditions would increase the contact resistance, a sample with identical ZTO film was prepared and R_C was estimated. The fresh sample has an estimated contact resistance of about 6.89 Ω-cm, similar to the 0 day device with passivation. To test whether a vacuum treatment would impact R_C, the sample was placed in a vacuum chamber for one hour and remeasured in an air ambient. Vacuum treatment caused the estimated R_C to increase to about 13.5 Ω-cm. Then, the sample was annealed for one hour in vacuum at 100ºC to test whether a vacuum anneal would change the contact resistance. After the vacuum anneal, the estimated R_C further increases to about 19.8 Ω-cm, similar to the 0 day device without passivation. Therefore, the increase in contact resistance with passivation may be attributed to the coincidental vacuum anneal of the ALD process. Contact resistance may increase during a vacuum anneal because the oxygen vacancies induced by the top metallization process [78], [163] will readily diffuse from the metal/semiconductor junction increasing the potential barrier and, therefore, the interfacial contact resistance [164]. Further work is required to verify these proposed mechanisms. Nonetheless, from the aging stability of μ_{FE} we can conclude that the contact resistance – after undergoing the one-time change induced during passivation – appears stable under aging.

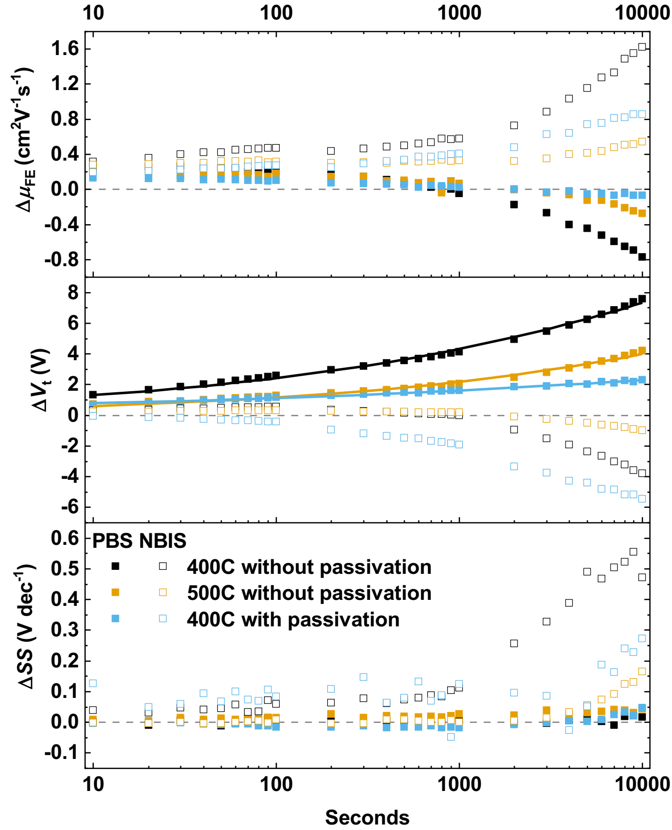


Figure 5.5 Change in μ_{FE}, V_t, and SS with stress time. The filled symbols indicate PBS, the open symbols indicate NBIS, and the lines in the plot of ΔV_t are fits by the stretched-exponential equation for ΔV_t. From [153].

Finally, the reliability of the aged devices was studied by PBS and NBIS and the results are shown in Figure 5.5. Under PBS, there is an increase in V_t with increasing stress time for all samples. The source of the PBS for the 400ºC device without passivation is related to the interaction between the ambient oxygen and the back channel and can be described by the stretched exponential, $\Delta V_t(t)=\Delta V_{t0}[1-\exp(-(t/\tau)^{\beta})]$ where $\Delta V_{t0}=V_{stress}-V_t(t=0\text{ s})$, τ is the stretched exponential, and β is the characteristic trapping time of carriers [150]. In the ΔV_t plot in Figure 5.5, the filled symbols indicate the measured change in V_t with time while the line indicates the $\Delta V_t(t)$ fitted equation. For the devices without passivation, τ is on the order of 10^5 s which is in line with pervious results attributed to oxygen adsorption [165]. After passivation, however, τ increases to the order of 10^9 s indicating an increase in stability [166]. Without passivation, β is approximately

0.28 while after passivation it decreases to 0.16. The change in both τ and β indicate the dominant charge trapping shifts from oxygen adsorption without passivation to interface states, likely the shallow Gaussian donors, with passivation and that an improved passivation layer, with reduced interface states, could further reduce ΔV_t from PBS.

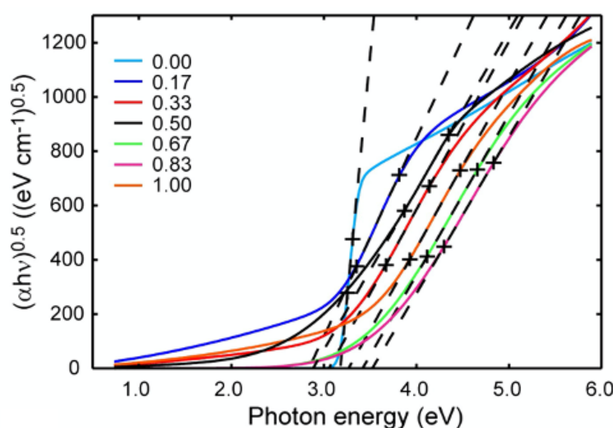


Figure 5.6 Variable angle spectroscopic ellipsometry analysis for ZTO films deposited on Si at 150ºC with various c_{Sn}. The exponent of 0.5 indicates indirect or amorphous type bandgap and the *y*-axis intercept of the fitted lines indicate the bandgap of the film. Sub-bandgap absorption is clearly present. Reprinted from [50] with permission from Elsevier.

Under NBIS, there is a decrease in V_t with increasing stress time for all samples. The source of negative V_t shift in AOS materials with NBIS has been attributed to photo-ionization of oxygen vacancy sites from V_O to V_O^{2+} which occurs under the combination of visible light ~2.3 eV and negative gate bias. These V_O^{2+} states contribute free electrons, causing parallel negative V_T shifts and persistent photoconductivity.[33] The neutral oxygen vacancy sites and/or local under-coordination of oxygen, can be correlated with the simulated valence band tail-states with a density of ~10^{20} cm^{-3} (Figure 5.2), and are experimentally observable in absorption spectra (Figure 5.6) as subgap absorption.[167], [168] The larger negative V_t shift of the 400ºC samples with and without passivation, compared to that of the 500ºC sample, may be due a greater concentration of subgap defects. The passivated sample exhibits the largest negative V_t shift with NBIS, likely due to the presence of donor-like tail states at the back channel/passivation interface (Figure 5.2(b)).[169], [170] In addition to a negative V_t shift, the 400ºC annealed sample without passivation shows a

large increase in *SS* with increased NBIS time. The other two samples also show an increase in *SS* for stress times greater than approximately 4000 s. These *SS* increases may be due to changes in subgap defects states or interface states [148].

The mobility values used to calculate the change in mobility shown in Figure 5.5 were extracted using the same gate over-drive voltage for every measurement of a given sample in order to reduce the impact of ΔV_t on mobility extraction. Two clear trends are observable for samples without passivation: PBS causes a decrease in μ_{FE} and NBIS causes an increase in μ_{FE}. The decrease in μ_{FE} with PBS can be understood from the interaction of carriers with the chemisorbed oxygen that also causes the positive V_t shift. As the passivated sample does not suffer from interaction with ambient molecules, the $\Delta\mu_{FE}$ with PBS is significantly reduced for that sample. The increase in μ_{FE} with NBIS can be understood as the increase in free carriers resulting in more band-like conduction with higher mobility.

5.4 Conclusion

Understanding and improving the temporal and bias stress stability of AOS TFTs fabricated using promising techniques such as ALD is critical for their adoption for beyond-display technologies. Here, we have investigated the temporal and bias stress stability of BEOL compatible zinc-tin-oxide n-TFTs with and without passivation layers. Devices without passivation exhibit slight changes within the first 25 days of aging and then excellent temporal stability. PBS instability, predominately caused by interactions with ambient molecules in samples without passivation, is significantly reduced for samples with passivation. However, passivation also causes an increase in contact resistance, *SS*, and does not completely eliminate NBIS instabilities. Future studies are needed to reduce the interface defect density between the passivation layer and

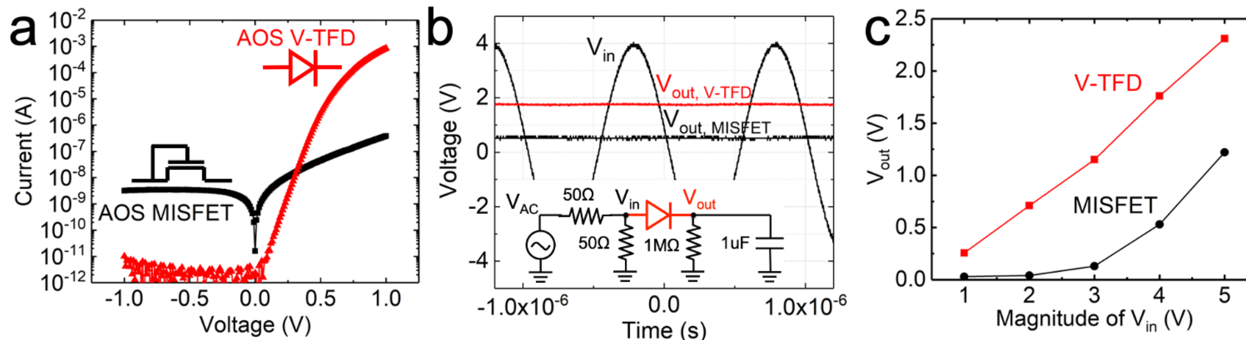
the active channel layer, and to confirm the physical mechanism driving the increased contact resistance following passivation.

Chapter 6 Schottky Contact to ALD ZTO

6.1 Introduction

In Chapter 2, we developed the processes required to deposit high-performance ZTO and low interface defect density gate insulators, achieving μ_{FE} greater than 20 $cm^2V^{-1}s^{-1}$ and *SS* approaching the Boltzmann limit. With high quality films and interfaces, we focused on characterizing and improving the ambient, temporal, and bias stress stability in Chapter 4 and Chapter 5. These chapters have, thus far, only focused on metal insulator semiconductor field effect transistors (MISFETs), as has the majority of existing literature.[29], [82], [86], [171] The thin-film electronics that can be fabricated using only our ZTO MISFETs are limited because of their unipolar, n-type, behavior and, therefore, other types of devices are required to expand to other thin-film ICs. In this chapter, we will focus on developing Schottky contacts to our high-performance ZTO which can be used to fabricate diodes used for rectification and metal semiconductor field effect transistors (MESFETs) for unipolar logic circuits.

Diodes → Rectifiers



MESFETs → Logic Inverters

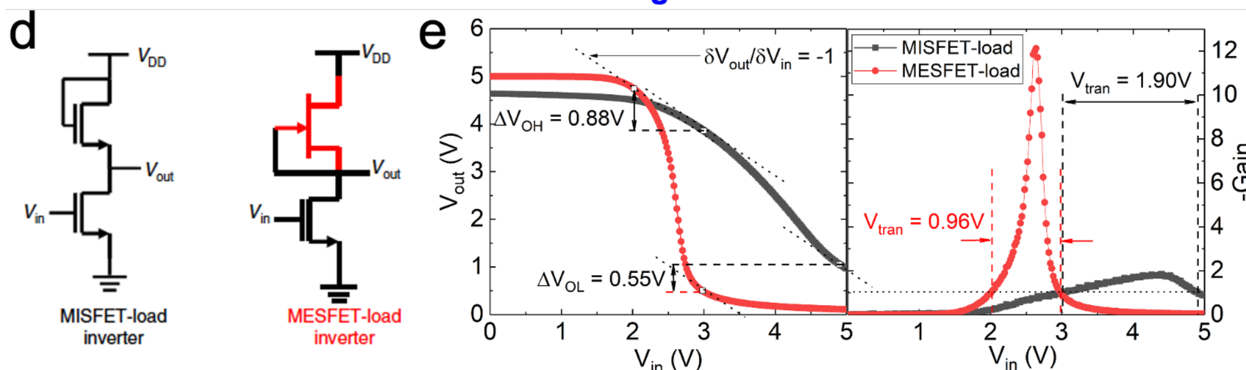


Figure 6.1 a) *I-V* measurements demonstrating diodes can be fabricated using either MISFETs, by tying the gate and drain electrodes as shown in the inset, or through a Schottky contact-based vertical thin film diode (V-TFD). b,c) AC/DC conversion using a half-wave rectifier, schematically shown in the inset. The lower switching voltage of the V-TFD results in a higher V_{out}. d) Circuit diagrams of logic inverters using a bottom drive MISFET and a top load MISFET (left) or MESFET (right). e) Inverter characteristics show a sharper voltage transfer characteristic and higher gain is observed for the MESFET-loaded inverter. Adapted by permission from Springer Nature Customer Service Centre GmbH: [16].

Rectification is critical for applications where wireless energy harvesting and power conversion is required. In wireless energy harvesting, a radio frequency (RF) input is received by an antenna and then fed into a full-wave rectifier, converting AC to DC.[172] This DC output can then be modulated using a DC-DC converter with a rectifier-based architecture.[173] Unipolar rectifiers can be fabricated using MISFETs in a diode-tied configuration, where the drain and gate are shorted together, or by applying a Schottky contact to the AOS material. Previous works on AOS Schottky-based devices have illustrated the superiority of their rectifying behavior and application to MESFETs.[16] In Figure 6.1a, *I-V* curves of diodes fabricated using a diode-tied

MISFET (black) and Schottky-based vertical thin film diode (V-TFD) shows the V-TFD has much lower reverse current and higher forward current leading to a better on/off current ratio and more ideal diode characteristics. When the MISFET is diode-tied, the device is operated in saturation where the current is defined by

$$I = \frac{WC_{\mathrm{ox}}}{2L}\mu_{\mathrm{sat}}(V_{\mathrm{GS}} - V_{\mathrm{t}})^2 \tag{6.1}$$

and increases by the square of V_{GS} (or V_{DS} as they are tied together).[171] Ideal diodes, on the other hand, have current defined by

$$I = I_{\mathrm{s}}\left\{\exp\left[\frac{qV}{nk_{\mathrm{B}}T}\right] - 1\right\} \tag{6.2}$$

that increases exponentially by the applied forward bias, V.[174] The exponential increase results in the lower on-resistance and thus lower forward voltage drops compared to the diode-tied MISFET and the half-wave rectifiers in Figure 6.1b,c show higher output voltages when diodes are used for the rectification.

Without a comparable p-type AOS material, current matching for CMOS-based logic architecture is challenging. An alternative to using CMOS architecture is enhancement/depletion-mode architecture based on unipolar semiconductors. Previous work has demonstrated diode-tied MISFETs (black) or MESFETs (red) can be applied as load transistors in AOS-based unipolar logic inverters, Figure 6.1d. The resulting transfer characteristics and gain profiles illustrate the superiority of the MESFET loaded inverter compared to the MISFET loaded inverter for small switching voltages and high gain, Figure 6.1e.

As Schottky contacts and MESFETs are important to achieve high-performance AOS logic circuits, as shown above, some work on AOS MESFETs has been performed over the last decade, as summarized in Table 6.1. Several of the works use IGZO as the semiconductor but, as we

explained in previous chapters, we are interested in ZTO as a ternary alternative. From the works that do focus on ZTO, annealing at 400ºC, or higher, is necessary for even moderate μ_{FE}, ruling out application to flexible substrates. Furthermore, the deposition techniques used are not suitable with the scalable manufacturing applications we are interested in. As a result, new low-temperature high-performance processes must be developed for ALD ZTO MESFETs, but first Schottky contacts to ALD ZTO are required.

Table 6.1 Brief summary of current AOS MESFETs

Process Temperature	Deposition Technique	AOS Material	μ_{FE} [$cm^2V^{-1}s^{-1}$]	*SS* [V dec^{-1}]	Ref.
200ºC	PLD	IGZO	0.5 (V_{GS} = 0 V)	0.13	[175]
350ºC	Mist-CVD	IGZO	3.2 (V_{DS} = 3 V)	0.35	[176]
RT	Sputter	IGZO	8.8 (V_{DS} = 2 V)	0.42	[177]
400ºC	Mist-CVD	ZTO	12 (V_{DS} = 2 V)	0.18	[178]
RT	Sputter	ZTO	0.9 (V_{DS} = 3 V)	0.12	[179]
520ºC	Solution-process	ZTO	4.5 (V_{GS} = 0 V)	0.11	[16]

At the simpliest level, to form a high quality Schottky interface to an n-type semicondcutor, the metal must have a high-workfunction and the junction between the metal and semiconductor must be clean and abrupt. Even with a high-workfunction metal and a clean junction, neither an abrupt or Schottky junction is guaranteed. Abrupt junctions are not energentically favorable and interactions between the semiconductor and metal, such as interdiffusion or alloy-mixing, can lead to interfacial layers, interface defects, or semiconductor defects that change the characteristics of the junction. For oxide-based based semiconductors, inlcuding ZTO, reduction and oxidation also play a critical role in the charactertics of a metal semiconductor junction. For example, junctions

between high-workfunction Pd, Pt, and Au show little to no retification to ZnO because redox reactions between the metal and ZnO create Zn and O vacancies that cause Fermi-level pinning or trap-assited tunneling.[180], [181] This is further illustrated by earlier work done by PetersonLab, in which O_2 plasma is used to modify the surface of Pd to PdO_x before spin-coating ZTO. During the annealing of the spin-coated ZTO, the PdO_x is reduced to Pd and oxygen vacancies in ZTO are filled resulting in a Schottky contact at that interface.[182]

A previous study on reactively sputtered Au, Ag, Ni, Pd, and Pt Schottky contacts to PLD ZTO showed Ni provides no rectifying behavior while Au, Ag, Pd, and Pt all provide greater than three orders of magnitude of rectification with Au and Pd showing the best performance with over seven orders of magnitude of rectification.[183] Another previous work showed evaporated Ag created a Schottky contact to solution-processed ZTO because the Ag oxidized to AgO_x due the favorable chemical states that existed at the interface.[16] All of this is to say, the formation of a Schottky contact may be highly dependent on the interface, which varies with deposition technique.

Schottky contacts are required to create unipolar thin-film diodes and MESFETS but have not yet been studied with ALD ZTO. Therefore, it is unknown whether metals that provide Schottky contacts to ZTO deposited by other deposition techniques will create Schottky contacts to ALD ZTO because of differences in the metal-semiconductor interface. In this chapter, we study and characterize different contact materials to enable future high-performance Schottky-based devices. First, we will attempt to use bottom Pd and top Ag as a bottom ohmic and top Schottky contact, respectively. Then, we will use reactively sputtered AgO_x as a top Schottky contact in a lateral structure to demonstrate the first Schottky contact to ALD ZTO. Finally, because of the

limitations of a lateral structure, we will investigate several different metals as possible bottom Schottky contacts.

6.2 Experimental Section

6.2.1 Silver and Reactively Sputtered Silver Process

Samples were first prepared following a process similar to that in [16] with bottom Pd and top Ag. First, heavily doped n-type silicon with 100 nm thermally grown oxide was used as the substrate where 10 nm of Ti followed by 100 nm of Pd was deposited by evaporation and patterned by lift-off to form the bottom electrode. Then, ZTO was deposited using 200ºC thermal ALD process described in Chapter 2. The sample was either annealed at 400ºC in an air ambient with relative humidity < 20% first and then wet-etched for device isolation or vice versa. Finally, a top electrode was formed by evaporating 100 nm of Ag followed by 10 nm of Pd and patterned by lift-off.

Another set of samples were fabricated using the same substrate where ZTO was deposited using the same 200ºC thermal ALD process described in Chapter 2. The ZTO was then wet etched for device isolation and annealed at 400ºC in an air ambient with less than 20% RH. Top Schottky contacts were deposited using reactive sputtering of Ag using a Kurt J. Lesker PVD 75 and top ohmic contacts were deposited using sputtering of Mo. Both metals were patterned using liftoff. Fabricated devices were measured in air ambient in the dark using an HP4156A semiconductor parameter analyzer with the substrate floating, the ohmic contact grounded, and the bias applied to the Schottky contact.

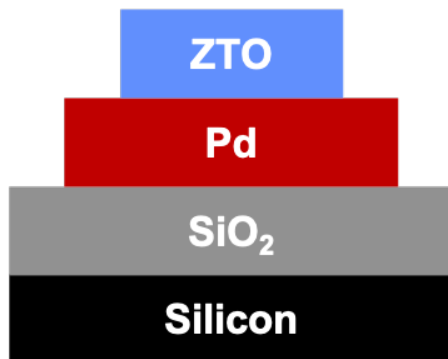
6.2.2 Process to Screen Other Potential Bottom Schottky Contacts

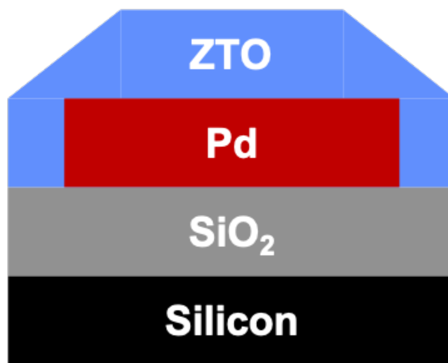
Starting with a glass substrate, two samples each were coated in approximately 100 nm of Ag, Pd, or Pt. The first sample for each metal was used to test the metal as a bottom Schottky contact while the second sample was exposed to 800 W of O_2-plasma for 10 min at 60ºC using a YES-CV200RFS. Previous work has shown this O_2-plasma exposure results in oxidization of the surface of metals such as Ir, Pd, and Pt, improving rectifying performance to metal-oxide semiconductors.[182], [184] We will therefore refer to the O_2-plasma treated metals as oxidized in this chapter. Next, approximately 80 nm of ZTO was deposited using the 200ºC thermal process described in Chapter 2 and was then annealed at 400ºC in a moisture controlled glovebox with relative humidity less than 20%. Then, the ZTO was wet-etched for device isolation. Finally, ohmic contacts were made to the top of the ZTO by sputtering approximately 100 nm of Mo. Passivated samples were encapsulated with 30 nm of Al_2O_3 deposited using the O_3-based ALD process introduced in Chapter 4.

6.2.3 Process to Further Investigate Platinum as a Bottom Schottky Contact

Starting with a silicon substrate with 100 nm of thermally grown oxide on the surface, two samples were prepared. Both samples were coated with approximately 100 nm of Pt. The bottom Pt layer on the second sample, Sample B, was patterned by lift-off while the bottom Pt on the first sample, Sample A, remains as a blanket film. Next, approximately 96 nm of ZTO was deposited on both by the 200ºC O_3-based ZTO process developed in Section 7.4.1. The ZTO was patterned by wet-etching for device isolation for Sample B only. Then, the samples were annealed at 400ºC for one hour in an air ambient with relative humidity less than 20%. Finally, top ohmic contacts were fabricated by depositing approximately 100 nm of Mo that was then patterned by lift-off.

6.3 Demonstration of the First Schottky Contact to ALD ZTO





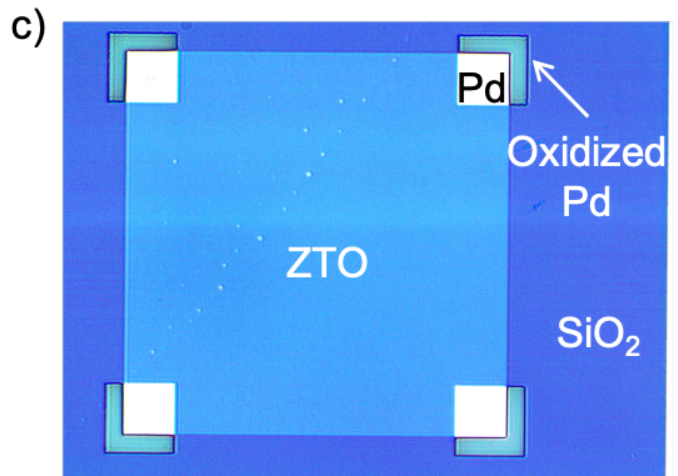


Figure 6.2 a) Schematic cross section of ALD sample with ZTO etched prior to ZTO annealing. b) Schematic cross section of solution-processed sample during ZTO annealing. c) Top down microscope image of a) after annealing.

The Ag process used to create Schottky contacts to solution-processed ZTO was the first process we attempted to create Schottky contacts to ALD ZTO.[16] During the first fabrication run, we discovered an issue with the fabrication process illustrated in Figure 6.2. As-deposited ZTO etches in our wet-etchant more readily than annealed ZTO and because of this, our preferred fabrication process is to etch the ZTO before annealing (Figure 6.2a). This is different than the solution process where annealing is required before wet-etching (Figure 6.2b). As a result of these

differences, the bottom Pd, in some areas, was exposed to air during the ALD ZTO anneal , which would not be exposed during the ZTO solution process. The Pd that was exposed to air readily oxidized and no longer provided a metallic contact. To correct for this issue, we switched the order of process steps to anneal the ALD ZTO before wet-etching.

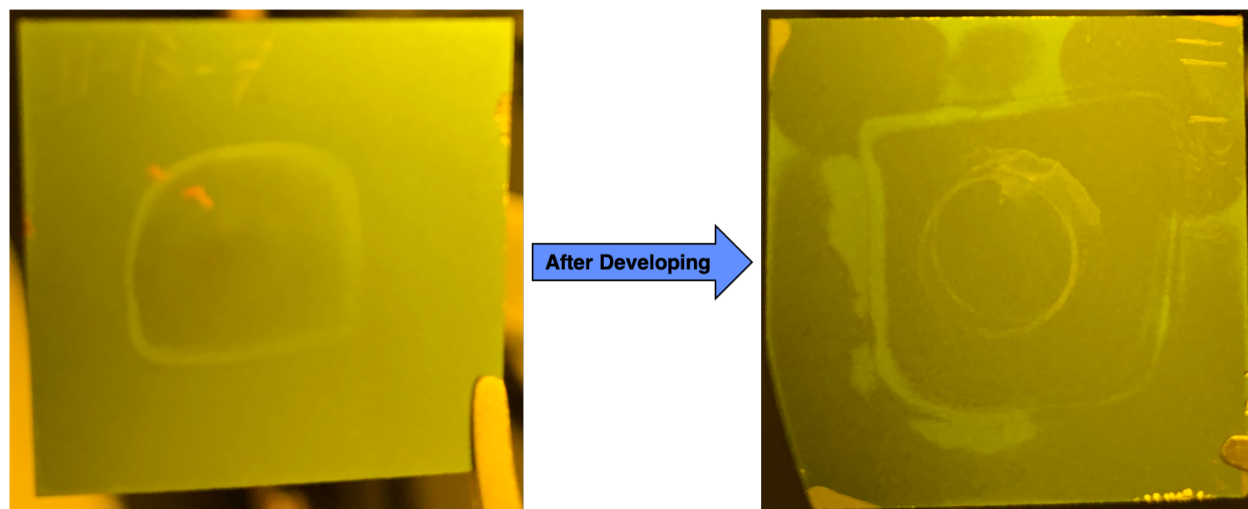


Figure 6.3 On the left, we see the back of a sample with ZTO deposited on the back from the conformal vapor-phase ALD process. On the right, we see the back of a different sample after photoresist developing where the ZTO that was exposed to the developer was etched.

After correcting the issue of oxygen exposure of Pd during the ALD ZTO anneal, a second fabrication issue was discovered. The typical photolithography process we use calls for a 30-second single pass of AZ-726 developer after exposing the photoresist. However, we found that the AZ-726 developer readily etches our ZTO films, as illustrated in Figure 6.3. As a result, the photolithography process used to pattern the top electrode may cause a short between the top and bottom electrodes anywhere the developer etched the ZTO film and the metals overlap vertically. To mitigate this, we found that developing with a 15-second pass was sufficient and did not cause a short the top and bottom metal electrodes.

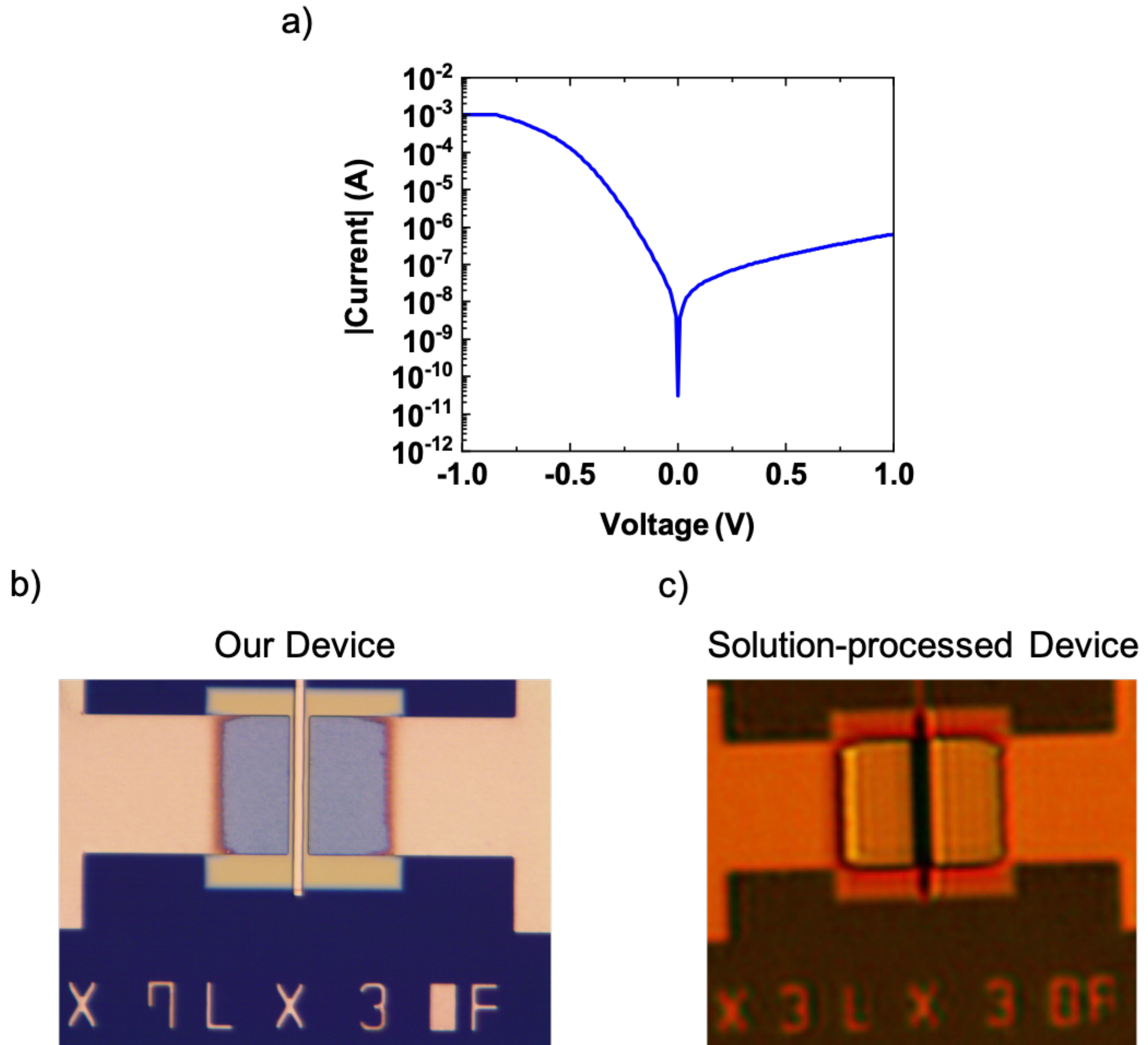


Figure 6.4 a) *I-V* curve of a circular diode with 110 μm diameter. The bias was applied to the top Ag contact. b) Top-down microscope image of MESFET fabricated using ALD ZTO. c) Top-down microscope image of MESFET fabricated using solution-processed ZTO reprinted with permission from [16]. Notice, the Pd overlapping ZTO in b) and c) both show obvious reactions with the ZTO.

Finally, with the fabrication issues resolved, we could fabricate devices with bottom Pd and top Ag contacts. In [16], the bottom Pd acts an ohmic contact to the ZTO while the top Ag acts a Schottky contact. To test these devices, assuming the Ag would form a Schottky contact, we biased the Ag electrode and measured the *I-V* shown in Figure 6.4a. If the Ag was a Schottky contact, we would expect to see low off-current for reverse bias (negative *V*) and higher on-current for forward bias (positive *V*). Instead, we see the opposite where off-current is measured in forward

bias and on-current is measured in reverse bias. With the device operating with rectification in the opposite V direction than we expected for a Ag Schottky contact, this indicates the Ag may have formed an ohmic contact while the bottom Pd formed a Schottky contact.

We hypothesize that the evaporated Ag contact to solution-processed ZTO in [16] formed a Schottky contact because the Ag reacted with the ZTO at the interface to form a AgO_x interfacial layer via out-diffusion of oxygen from the ZTO film. AgO_x has a workfunction of > 5.0 eV, which is higher than the 4.3 eV workfunction of Ag.[185], [186]. We hypothesize the higher workfunction interfacial AgO_x layer is needed to create a Schottky contact to ZTO. If AgO_x was not created at the junction with our ALD ZTO films, the result is an ohmic, rather than Schottky, behavior. Later in this section, we will attempt to directly deposit AgO_x to form a top Schottky contact.

Pd, on the other hand, appears to form a Schottky contact, rather than the expected ohmic contact. Previous work with bottom Pd intentionally oxidized the metal using O_2-plasma before ZTO deposition and then annealed the ZTO showing the oxidized Pd could act as a Schottky contact when the PdO_x reduced to Pd by filling oxygen vacancies in ZTO.[182] Here, our ALD ZTO has a lower concentration of oxygen vacancies than the solution-processed ZTO films, as shown in Chapter 2. As a result of a lower concentration of oxygen vacancies, the Pd may form a Schottky contact to ALD ZTO without the need to first oxidize the Pd to form PdO_x. In Section 6.4, we investigate whether oxidizing Pd before ZTO deposition and annealing will result in a higher rectification magnitude.

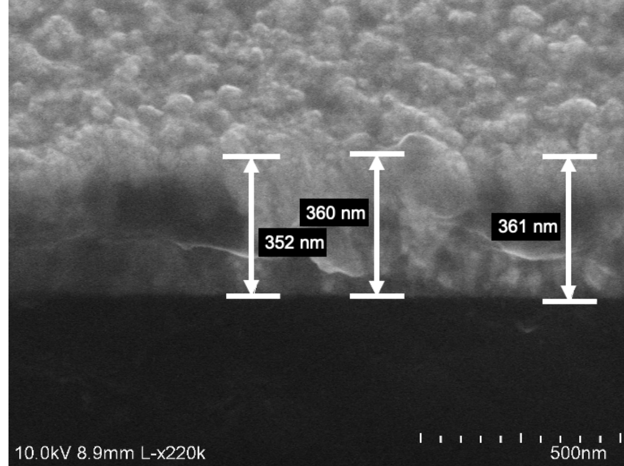


Figure 6.5 SEM image taken at a 45º angle showing the AgO_x film thickness after sputtering a Ag target for 1000 seconds at 100 W DC, 5 mTorr, and 9% O_2.

As the Ag Schottky contact to solution processed ZTO appears to depend on the formation of AgO_x at the interface, and we hypothesize we do not have an AgO_x interfacial layer with our ALD ZTO, we attempted to directly deposit AgO_x at the interface using reactive sputtering. To do this, we first characterized the deposition rate of AgO_x by measuring film thickness after sputtering an Ag target for 1,000 seconds at 100 W DC, 5 mTorr, and 9% O_2 by taking an SEM image at a 45º angle. The SEM image can be seen in Figure 6.5 and the average calculated film thickness is approximately 470 nm, leading to a deposition rate of about 0.47 nm sec^{-1}. For the device contacts, we targeted a 40 nm AgO_x interface layer followed by a 60 nm Ag capping layer. As the deposition rate varies with O_2 partial pressure, we estimated the sputtering times in Table 6.2.

Table 6.2 Summary of sputtering parameters used.

O_2 %	DC Sputtering Power [W]	Pressure [mTorr]	Reactive AgO_x Sputtering Time [sec]	Ag Sputtering Time [sec]
4.75	100	5	80	128
9	100	5	85	128
13	100	5	90	128

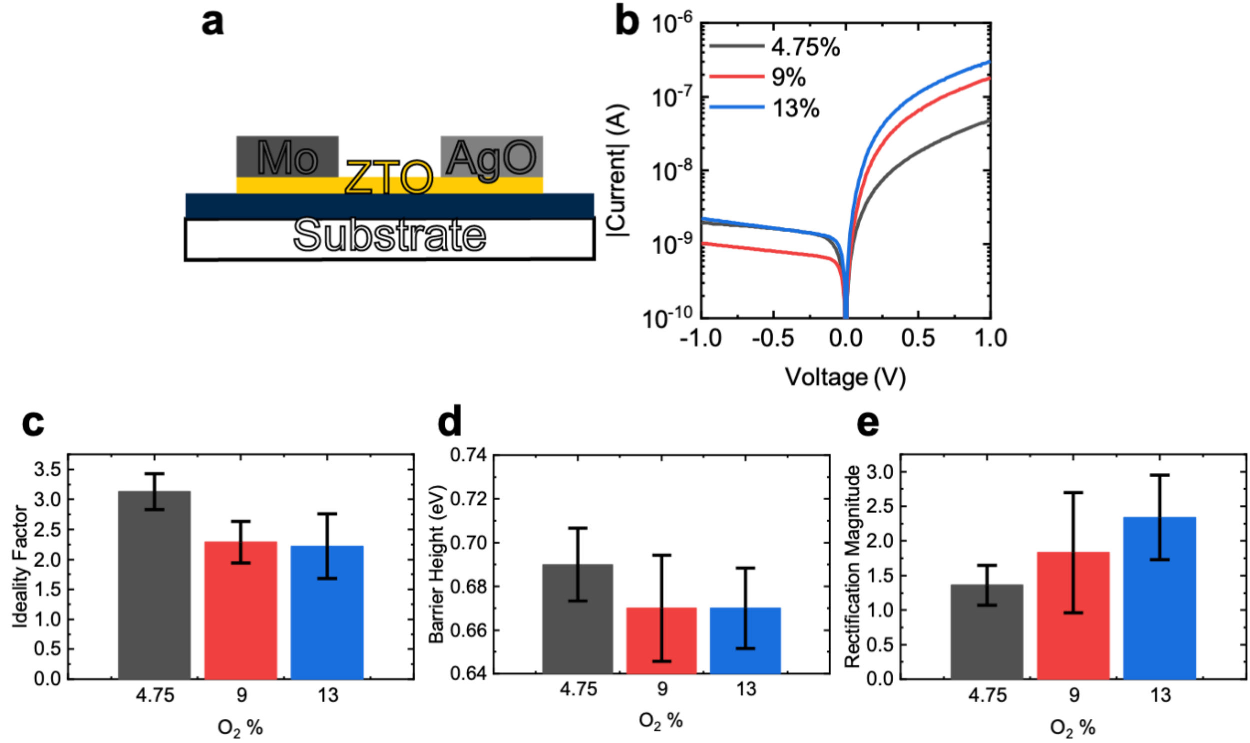


Figure 6.6 a) Schematic cross section of lateral co-planar Schottky diode. b) Representative *I*-*V* curves for diodes created using the sputtering parameters listed in Table 6.2. c) ideality factor, e) barrier height, and f) rectification magnitude extracted from *I*-*V* curves. The black error bars indicate standard deviation based on analysis of five to six measured devices.

The fabricated devices have a cross section as shown schematically in Figure 6.6a, with co-planar Mo ohmic contacts and AgO_x Schottky contacts. By measuring diodes with Schottky contacts formed using the sputtering parameters listed in Table 6.2, we report the first intentional Schottky contact to ALD ZTO, Figure 6.6. We can extract the saturation current density, J_s, ideality factory, n, and series resistance, R_s, by fitting the forward bias current density, J, equation

$$J = J_s \left\{ \exp\left[\frac{q(V - JAR_s)}{nk_B T} \right] - 1 \right\} \tag{6.3}$$

where V is the applied bias, T is the temperature (300 K for all measurements here), k_B is the Boltzmann's constant, A is the area of the device, and q is the charge of an electron. The extracted ideality factor is shown in Figure 6.6c and generally decreases with increased O_2 partial pressure as the Schottky contact improves also leading to an increase in rectification magnitude Figure 6.6e.

This result further illustrates the importance of having AgO_x at the surface, rather than Ag, to achieve a Schottky contact. The effective Schottky barrier height, $\Phi_{B,IV}$, can be extracted by the thermionic emission model given by

$$J_s = A^* \times T^2 \exp\left(\frac{-q\Phi_{B,IV}}{k_B T}\right) \quad (6.4)$$

where A^* is the Richardson constant taken to be 41 A cm^{-2}.[182], [187] The extracted $\Phi_{B,IV}$ is about 0.68 eV which is what is expected from the work function of AgO_x (>5.0 eV) and the electron affinity of ZTO (4.35-4.60 eV). While this is a first step in creating devices based on Schottky contacts, there are issues with these devices.

First, ungated devices that have a lateral channel, as shown in Figure 6.6a, can suffer from a large series-resistance, minimizing the rectification magnitude. The lateral ungated portion acts like the offset region studied in Section 3.3.2. Without accumulation the ungated portion has high resistivity, reducing the forward current. Some groups have reduced this series resistance by minimizing the lateral dimension between contacts to approximately 15 nm using wafer-scale adhesion lithography.[188] Another option is to create a V-TFD where the separation between electrodes becomes the thickness of the semiconducting thin-film. As we already have Mo as an ohmic top contact to our ALD ZTO, we investigate other potential materials for a bottom Schottky contact to ALD ZTO in Section 6.4 to form a V-TFD.

6.4 Screening of Several Metals for Bottom Contact Behavior to ALD ZTO

In Section 6.3 we fabricated and briefly characterized a lateral Schottky diode and discovered the device performance is limited by the lateral distances between the coplanar Schottky and ohmic contacts. One way we to overcome the limitations of the lateral structure is to move to a V-TFD architecture, requiring Schottky and ohmic contacts to be placed on opposite

planes (above and below) the ZTO thin-film. As we already have Mo as a top ohmic contact and Pd, which has acted as an bottom ohmic contact with other ZTO films,[16] did not create an ohmic contact to our ALD ZTO film in Section 6.3, but rather a Schottky contact, we will investigate other potential metals as bottom Schottky contacts to ALD ZTO in this section. Table 6.3 is a brief summary of previous works using bottom metals or metal oxides to create a bottom Schottky contact to AOS thin-films. From this list, we can see that PtO_x, PdO_x, and Pt have all been shown to create a bottom Schottky contact to AOS thin-films with an ideality factor less than 1.36 and a rectification magnitude greater than 6.38. In this section, we will study PtO_x, PdO_x, and Pt as a bottom Schottky contact to ALD ZTO because of their previous success with other AOS thin-films. Additionally, we will study Pd to try to recreate the results in Section 6.3 and Ag and AgO_x because we know from Section 6.3 that AgO_x forms a top Schottky contact to our ALD ZTO.

Table 6.3 A brief summary of the properties of bottom Schottky contacts to AOS thin-films.

Process Temp.	AOS Deposition Process	AOS Material	Schottky Metal	Ideality Factor	Rectification Magnitude	Reference
520ºC	Solution-process	ZTO	MoO_x	>3	3.00	[189]
RT	Sputter	IGZO	Pt	21	3.00	[190]
520ºC	Solution-process	ZTO	PdO_x	1.9	3.70	[182]
300ºC	Sputter	IGZO	Au	1.29	4.00	[191]
RT	Sputter	IGZO	PtO_x	1.36	6.38	[192]
RT	Sputter	IGZO	PdO_x	1.22	6.86	[193]
RT	Sputter	IGZO	PdO_x	1.51	7.00	[194]
200ºC	PLD	IGZO	Pt	1.04	8.00	[195]

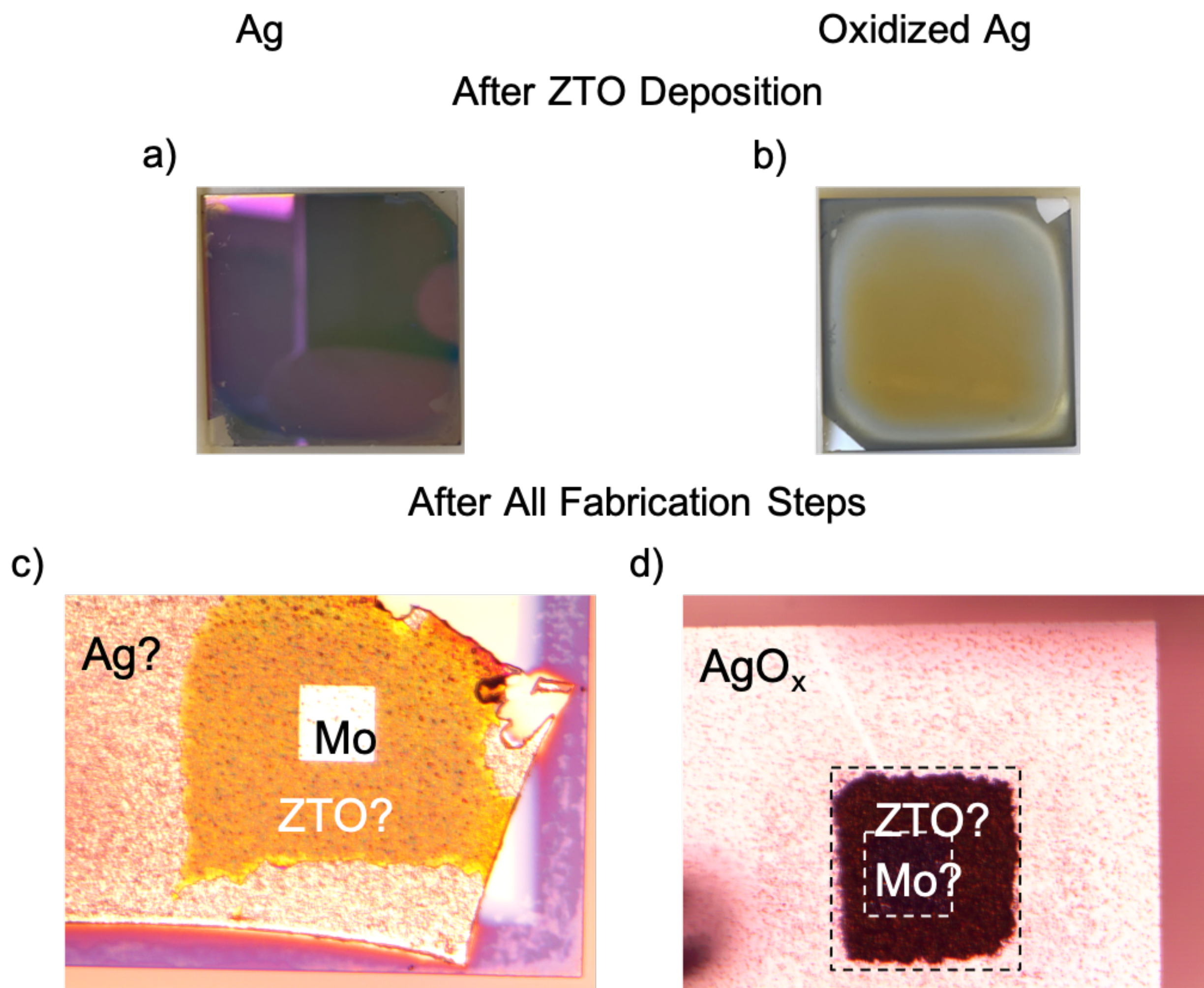


Figure 6.7 Left column: samples where Ag was not intentionally oxidized before further processing. Right column: samples with intentionally oxidized Ag. a) and b) show photographs of 2.5 x 2.5 cm samples after ZTO deposition. c) and d) show top-down microscope images of finished samples.

All of the as-deposited metals looked metallic before further processing, with the Pd and Pt based bottom layers remaining metallic in appearance throughout the entire process. The Ag based bottom layers, on the other hand, do not keep a metallic appearance with further processing. Figure 6.7b, shows the Ag sample that was intentionally oxidized through O_2-plasma exposure is no longer metallic immediately after O_2-plasma exposure, while Figure 6.7a shows the Ag sample that was not exposed to O_2-plasma becomes at least partially oxidized by the ALD ZTO and annealing processes. The resulting devices, Figure 6.7c and Figure 6.7d, show rough surfaces and unexpected ZTO and Mo interactions due to silver's low oxidation potential.[196] From this, we

conclude that using Ag for a bottom contact is unstable, at best, and therefore unsuitable for a bottom contact to ALD ZTO. Other materials with higher oxidation potentials should be investigated.

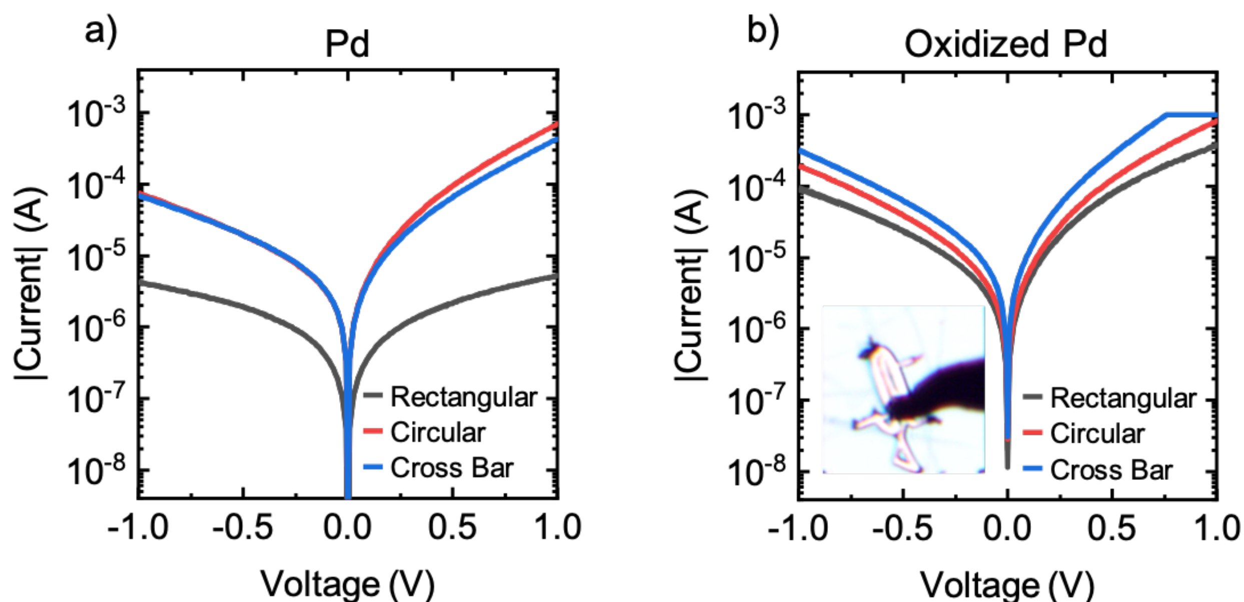


Figure 6.8 Representative *I-V* curves for diodes created with bottom Pd a) without intentional oxidation b) with intentional oxidation. Inset in b) shows layer of PdO_x that had to be scratched off to probe the electrode.

The *I-V* curves for devices fabricated using Pd based contacts are shown in Figure 6.8. As found in Section 6.3, the Pd bottom contact without intentional oxidation forms a Schottky contact to the ALD ZTO (Figure 6.8a). Here, we also test intentionally oxidized Pd on the premise that the oxidized Pd will out-diffuse oxygen to the ZTO and fill oxygen vacancies to form a better Schottky contact.[182] We find, however, that intentional oxidation of the Pd results in an increased reverse current and similar forward current, therefore decreasing the rectification magnitude. Furthermore, there is a possible reaction between the intentionally oxidized Pd and the ZTO during the ZTO processing that results in a surface layer on the PdO_x electrode, also seen in Figure 6.4, that cannot be etched by our ZTO wet-etchant. It had to be scratched through to probe the electrode (Figure

6.8b inset). Ideally, we would use a bottom metal that could withstand the air exposure during the ZTO anneal without oxidation in the probing areas.

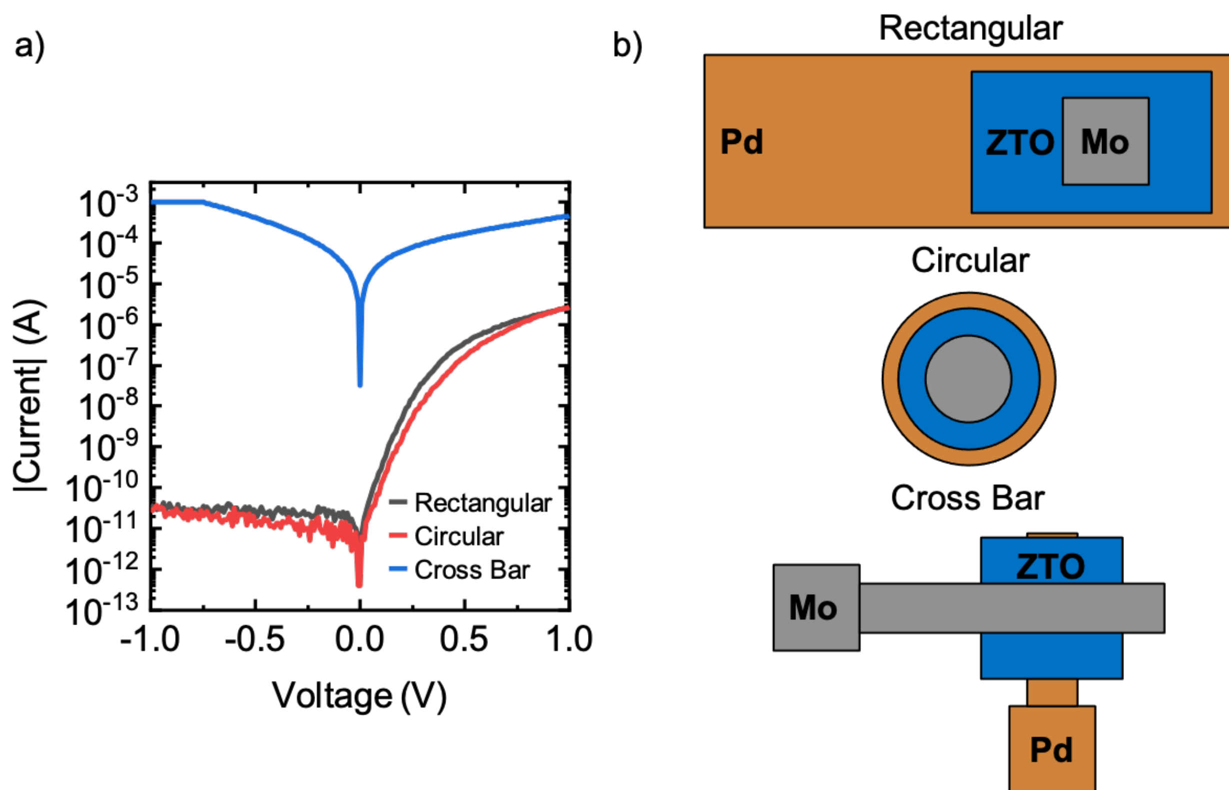


Figure 6.9 a) Representative *I-V* curves for diodes created with bottom Pd without intentional oxidation after passivation. Note: the top Mo is biased for this figure rather than the bottom electrode. b) Top-down schematic showing the different V-TFD architectures.

The edges of our ALD ZTO films often demonstrate different characteristics than the bulk films which may result from defects at the edges caused by damage introduced during the fabrication process.[197] Such defects can result in lower resistivity films, increasing the reverse leakage of our V-TFDs. To passivate these defects and avoid possible surface conduction, the sample without intentional Pd oxidation was encapsulated with 30 nm of Al_2O_3 using the O_3 process from Chapter 4. After passivation, the resulting *I-V* curves (Figure 6.9a) are significantly different than the pre-passivation curves (Figure 6.8a). The main difference is that the Mo contact now acts as a Schottky contact for the rectangular and circular architecture V-TFDs.

In Section 5.3, we saw that passivation increases the interfacial contact resistance between Mo and ALD ZTO. We attributed the changes to diffusion of defects at the interface during the ALD process. While that may also be happening here, resulting in changes in the contacts, there is an additional change resulting in differences between the circular/rectangular and crossbar structures. The top-down schematic illustrations of the three different architectures used here, shown in Figure 6.9b, illustrate that the probing area, where the Al_2O_3 is etched to make contact to the top metal, overlaps with the ZTO only for the circular and rectangular structures and is therefore exposed to both the ALD process and the Al_2O_3 etchant. Whereas for the cross bar structure, the Mo/ZTO contact is only exposed to the ALD process. The combination of passivation and etching Al_2O_3 to contact Mo on-top of ZTO somehow results in a Mo Schottky contact for the circular and rectangular structures. While these devices exhibit the highest rectification magnitude we have seen thus far, the mechanism is not well understood and may be unstable or unrepeatable.

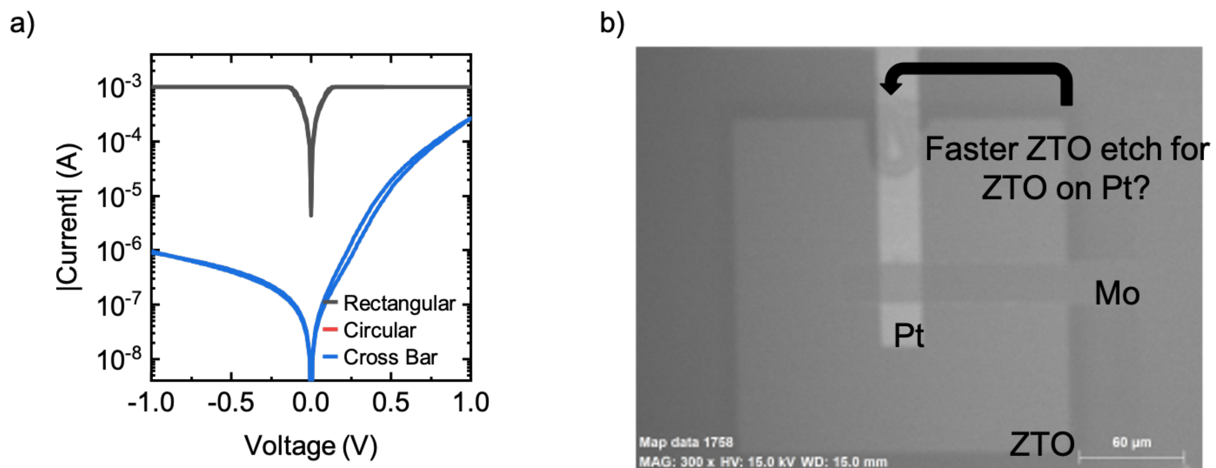


Figure 6.10 a) Representative *I-V* curves for diodes created with bottom Pt without intentional oxidation. b) SEM image of cross-bar diode.

Finally, we look at the devices fabricated with bottom Pt contacts. Representative *I-V* curves for rectangular, circular, and cross bar diodes are shown in Figure 6.10a. The diodes

fabricated using both the rectangular and circular structures result in an apparent short between the bottom and top metals. As these samples were annealed before ZTO wet-etching, the ZTO required long wet-etches for isolation. As seen by the SEM image in Figure 6.10b, it appears that ZTO on Pt etches faster than the ZTO on the glass substrate. As a result, the ZTO on the rectangular and circular architectures, which is completely on top of Pt and may etch isotropically, may have over-etched during these long wet-etches, causing a direct contact between the top and bottom metals. As the ZTO is only over Pt in one small area for the cross bar structure, in an area that is far away from the Mo contact, the two electrodes in the cross bar structures are not shorted together and can be measured. The cross bar devices result in the highest rectification magnitude measured in this section, but still suffer from high reverse current. One of the sources of high reverse current may be from edge conduction that would be minimized with the circular and rectangular architectures. As Pt has a very high oxidation potential, we will investigate etching the ZTO before annealing in Section 6.5 to fabricate the circular and rectangular devices.

6.5 Platinum as a Bottom Schottky Contact to ALD ZTO

In Section 6.4, we successfully fabricated crossbar diodes using Pt as a bottom Schottky contact. There were, however, issues with the circular and rectangular diode architectures because of apparent over-etching of ZTO deposited on Pt. In this section, we reverse the order of the ZTO etching and annealing to etch the ZTO before annealing so the ZTO has a more uniform etch rate, eliminating the over etching of ZTO on Pt. While in Section 6.3, we saw that Pd exposed to air during the annealing process oxidized, the Pt does not have that issue because of the high oxidation potential of Pt.

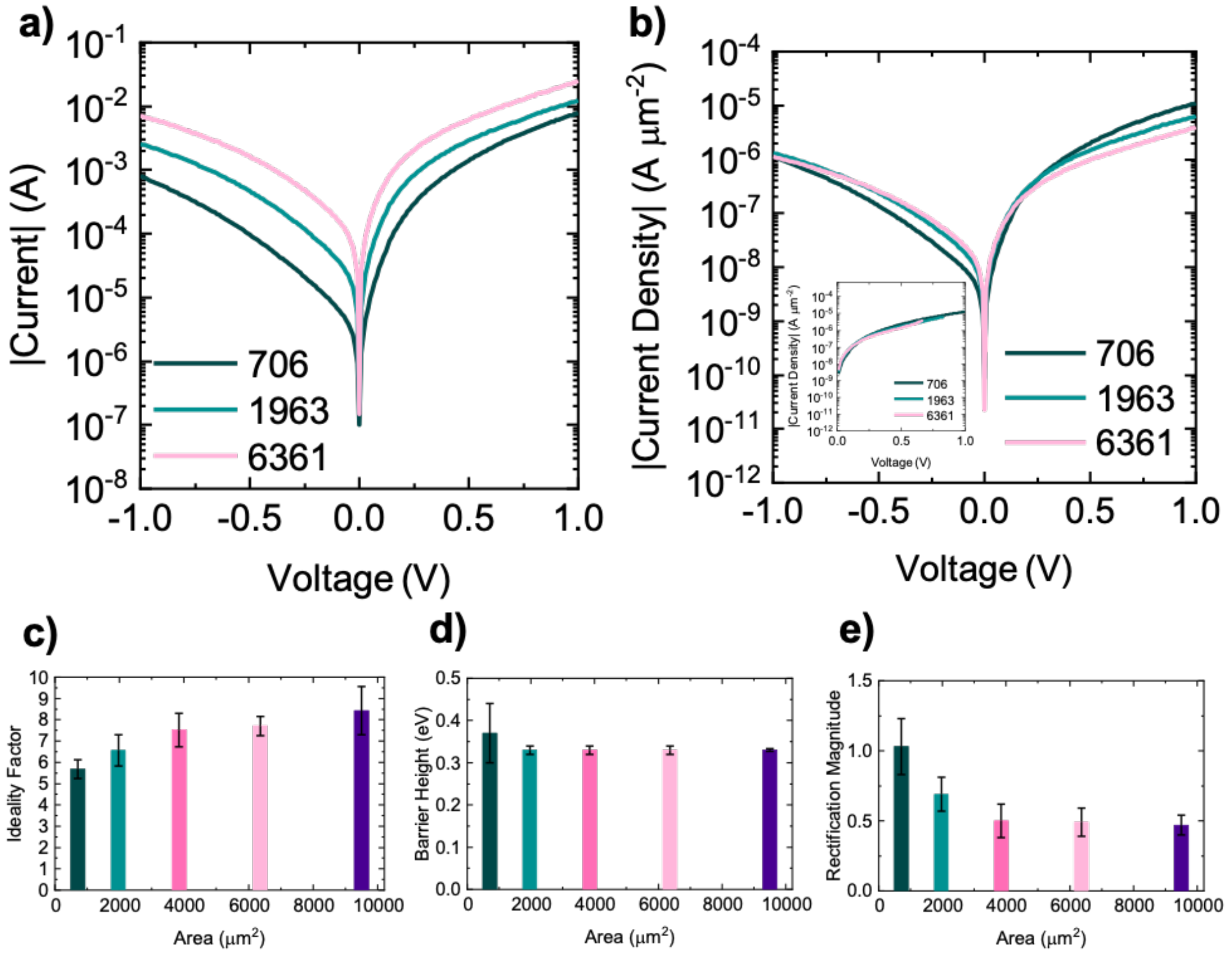


Figure 6.11 Representative a) *I*-*V* and b) *J*-*V* curves for diodes as a function of device area in μm^2. b) inset: *J*-*V* curves corrected for the voltage dropped across the series resistance. c) ideality factor, d) barrier height, and e) rectification magnitude extracted from *I*-*V* curves. The black error bars indicate standard deviation based on analysis of five to six measured devices.

The *I*-*V* and *J*-*V* curves for Sample B, where the bottom Pt and ZTO were etched for device isolation, are shown in Figure 6.11a and Figure 6.11b, respectively. While the forward current increases with device area (Figure 6.11a), the forward current density does not scale properly with area (Figure 6.11b). When current-density does not scale properly with device area, it is usually due to series resistance.[182] The series resistance can be separated into two components. The first component scales with area and is due to the resistivity of the ZTO and any contact resistance while the second component does not scale with area and can be caused from parasitic resistance of the measurement setup or from the resistance of the bottom Pt metal. By assuming the non-

scaling resistance is negligible for the device with an area of 706 μm, it is calculated as 13.6 Ω and is corrected for in the inset of Figure 6.11b which shows good agreement between devices with different areas. The difference in rectification magnitude shown in Figure 6.11e is also attributed to this series resistance. The barrier height shown in Figure 6.11d is lower than expected considering the work function of Pt (5.12-5.93 eV)[196] and the electron affinity of ZTO (4.35-4.6 eV)[198], [199]. The high reverse current that increases with increasing reverse bias and high ideality factor, Figure 6.11c, may be caused by parallel current paths.[200] Possible parallel current paths could be from the semiconductor surface or edges that exhibit different proprieties than the bulk ZTO. To minimize those sources of parallel current, we next study Sample A where blanket ZTO and Pt films are used.

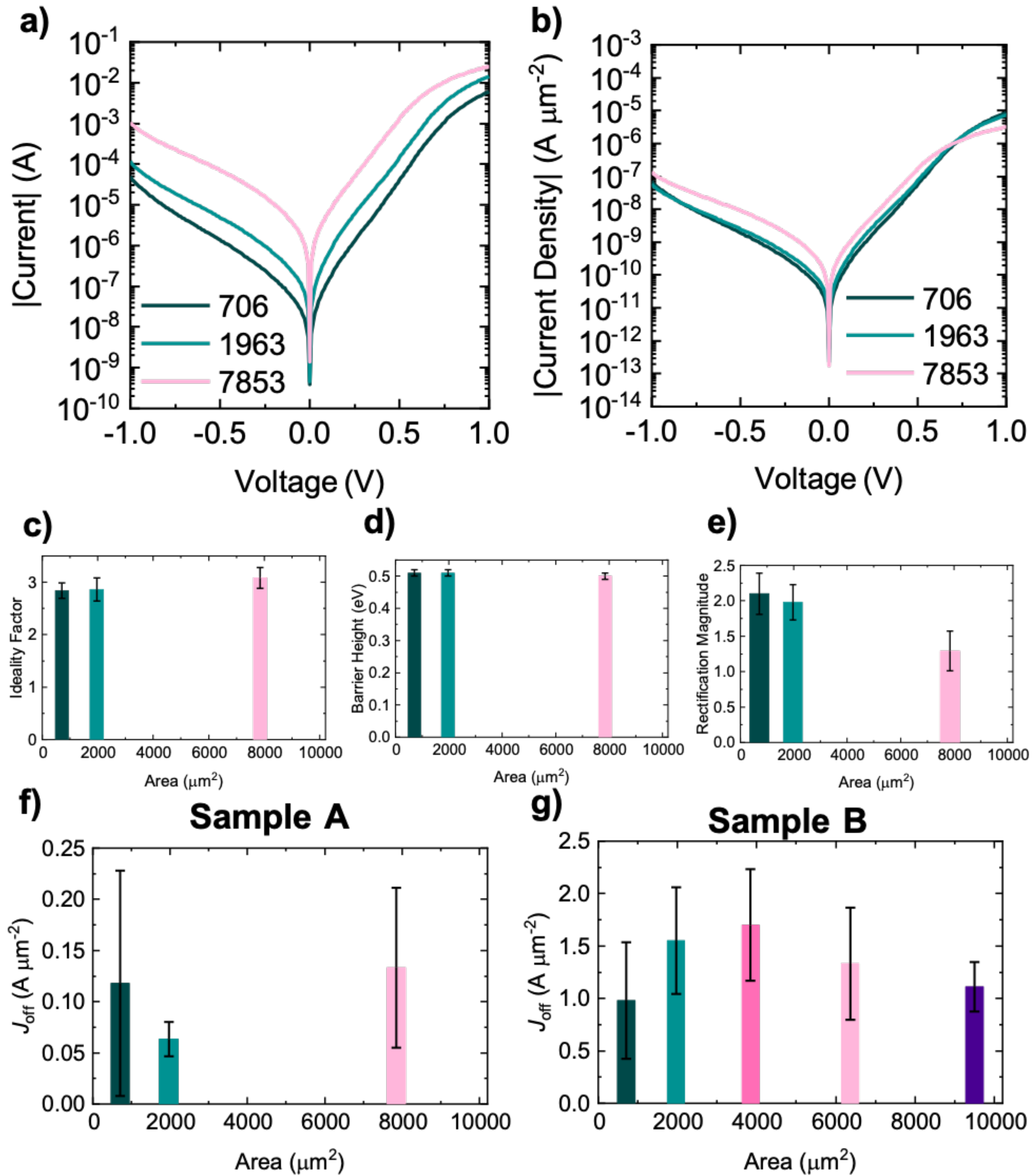


Figure 6.12 Representative a) *I-V* and b) *J-V* curves for diodes as a function of device area in μm^2. c) ideality factor, d) barrier height, and e) rectification magnitude extracted from *I-V* curves. The black error bars indicate standard deviation based on analysis of five to six measured devices. Reverse current densities extracted at V = -1 V for f) Sample A and g) Sample B.

The *I-V* and *J-V* curves for Sample A, where the bottom Pt and ZTO were not patterned, are shown in Figure 6.11a and Figure 6.11b, respectively. By not patterning the bottom Pd or ZTO,

we decreased the reverse current density by about an order of magnitude (Figure 6.12f) compared to Sample B (Figure 6.12g). With the forward current remaining at the same magnitude, the one order of magnitude decrease in reverse current directly yields an order of magnitude increase in the rectification magnitude (Figure 6.12e). The decrease in reverse current is a result of minimizing sources of parallel current, possibly the semiconductor surface and/or edges. The extracted barrier height (Figure 6.12d) is also closer to what we would expect for Pt and ZTO. In addition, the ideality factor (Figure 6.12c) is approximately half of what it was for Sample B.

As there is still a voltage-dependent reverse current and high ideality factor, there may be persistent sources of parasitic parallel current. To further minimize surface conduction, a future study could explore passivating the surface using the process developed in Chapter 4. The photolithography process used could also be impacting the ZTO film as we saw in Section 6.3, where the photoresist developer was found to etch the ZTO film. A future study could use a shadow mask to deposit the top metal contact and rule out photolithography as a source of damage to the ZTO thin-films.

6.6 Conclusions and future work

6.6.1 Conclusions

The goal of this chapter was to characterize the ability of different metals and metal oxides to form a Schottky contact to ALD ZTO to create Schottky diodes and enable MESFETs for integrated circuits using unipolar devices. First, we fabricated devices using bottom Pd and top Ag contacts that were shown to create ohmic and Schottky contacts, respectively, to solution-processed ZTO. For ALD ZTO, however, the Pd acted as a Schottky contact while the Ag acted as ohmic contact. The formation of ohmic contacts using Pd requires a high-density of oxygen vacancies in the ZTO thin-film which, as we showed in Chapter 2, the ALD ZTO films do not

have and therefore a Schottky contact is formed. While the formation of a Schottky contact to solution-processed ZTO using Ag resulted from the oxidation of Ag leading to a higher work function oxide, here, we hypothesize that the surface of the ALD ZTO was not favorable for oxidation of Ag at the interface, leading to an ohmic contact.

Since the formation of AgO_x at the interface between ZTO and the Schottky contact appears to be critical to the formation of a rectifying contact, we directly deposited AgO_x using reactive sputtering. With AgO_x at the interface between Ag and ALD ZTO, intentional rectifying contacts were demonstrated for the first time. The diodes, however, have a low rectification magnitude caused by the lateral device architecture used. To remove the limitations of a lateral structure, we move to a vertical structure which requires the creation of a bottom Schottky contact.

To find a suitable bottom Schottky contact to ALD ZTO, we screened several metals and metal oxides. Silver-based contacts, which we showed can create a Schottky contact to the top of ALD ZTO, are too unstable to be deposited before ZTO processing because of the low oxidation potential of silver. Palladium can be used to create a Schottky contact to ALD ZTO, but further work is needed to decrease the reverse current. Palladium oxide, on the other hand, leads to an undesirable interfacial layer between the PdO_x and ZTO. Finally, platinum was tested and formed a Schottky contact to ALD ZTO.

Of all the materials tested (Ag, AgO_x, Pd, PdO_x, and Pt), we further studied platinum because its high oxidation potential may form a stable Schottky contact. First, we showed that the forward current of large-area devices is limited by non-scaling parasitic series resistance. Then, we minimized the impact of parallel current paths by creating devices with blanket Pt and ZTO films. The devices fabricated using these blanket films show an order of magnitude increase in rectification magnitude caused by an order of magnitude decrease of parasitic parallel current.

These devices still exhibit high reverse current that increase with increasing reverse bias and ideality factors greater than two. More work is required to fabricate high-performance Schottky-based devices.

6.6.2 Outstanding Scientific Questions and Future Work

This work raised several scientific questions:

1) Chemically and structurally, is the ZTO deposited for the thick layers used for V-TFDs identical to the thin layers deposited for MISFETs in previous chapters? The ellipsometry data of the thicker film did not fit our thickness model from our thinner films, possibly indicating changes in film composition or optical absorption. If the film is changing with thickness, this may change the band structure and how contacts are formed to the material. The same material analysis we performed in Chapter 2 could be performed on these thicker films to compare.

2) Chemically and structurally, is the ZTO deposited on different materials the same as the ZTO used for MISFETs in previous chapters? In this chapter, we saw that the ZTO deposited on Pt etches differently the ZTO on other parts of the sample. The same was seen for ZTO deposited on glass compared to ZTO deposited on Si/SiO_2 substrates. The same material analysis we performed in Chapter 2 could be performed on films grown on different substrates for comparison. If differences are found, they could result from differences in the surface[201] or the thermal profile of the substrate.

3) Can a passivation layer be deposited before top metallization to minimize edge and surface conduction? Many of the devices fabricated in this chapter show reverse current that increases with reverse bias and ideality factors greater than two, which are both evidence of parasitic parallel current sources. The surface and the edge of ZTO surfaces are potential sources of parasitic parallel current and can be passivated by depositing an encapsulation layer. While we

tried that in this chapter, there were unwanted changes in the ohmic contact caused by the process. By changing the fabrication process, i.e. depositing the passivation layer before ohmic contact deposition, the ohmic contacts would not be exposed to the passivation process that changes their characteristics.

4) Throughout this chapter we refer to metals that have been treated with O_2 plasma or deposited by reactive sputtering as oxidized because of previous works that have shown these processes oxidize the metals. In the future, chemical analysis, e.g. XPS, TEM, etc., could be performed to confirm the oxidation of the treated and reactively-sputtered metals.

Chapter 7 Scalable Precision Customizable Thin-film Electronics

7.1 Introduction

An increasing demand for customizable manufacturing, driven by increasingly specific end-user requirements, has motivated the development of processes to fabricate scalable, precise, and customizable thin-film electronics.[202], [203] While advances in photolithographic patterning have enabled the state-of-the-art 5 and 7 nm node ICs with ultra-low defect density, the multiple lithographic patterning steps required makes customizing the process to meet unique run requirements costly and inefficient.[1], [56] Additive manufacturing, building up layer-by-layer, can be tuned on-the-fly to allow for scalable, precise, and customizable thin-film electronics.

Not all additive microfabrication processes are created equal and there is often a tradeoff between spatial resolution, throughput, cost, and material compatibility. While there are current printing techniques that can print in the nanoscale, they are limited to certain materials that meet the strict ink requirements. Other patterning techniques, such as scanning-probe-microscopy-based techniques, can pattern with sub 10 nm resolution but are limited by cost and high process times.[204] Another patterning technique, direct laser writing using two-photon polymerization, can pattern polymers with sub-micron precision but requires expensive laser equipment and is limited to photoactive polymers.[205], [206]

Direct printing techniques, such as inkjet printing, are less expensive, are compatible with a wider range of inks, and are faster processes.[207], [208] Traditional direct ink-jet printing is limited to critical device dimensions of greater than 20 μm.[57] Some research groups have studied using other ways to use ink-jet printing, without direct printing of the critical dimension, to achieve

dimensions of about 3.5 μm.[58] Therefore, a challenge with additive microfabrication is that there is no technique that is best for high resolution, low cost, and high process speeds.

Electrohydrodynamic jet (e-jet) printing, an additive printing technique where an electric field is used to pull ink out of a conductive nozzle, is being studied to overcome this challenge because of its low cost, material compatibility, high process speeds, and sub-micron precision.[57] While e-jet printing has demonstrated resolution down to ~30 nm,[61] devices fabricated by e-jet have not broken into sub-μm resolution.[63], [209], [210] In addition to device dimensions greater than 1 μm, direct printing requires semiconductor deposited using a solution-process. As shown in Table 7.1, the direct printing of solution-processed thin-films generally require high temperature annealing for even moderate performance making the process incompatible with most flexible substrates. Therefore, we look to use our ALD-based AOS process to fabricate customizable high-performance devices.

Table 7.1 Summary of TFTs with direct printed semiconductor channel. Adapted with permission from [57].

Material	Printing Technique	Annealing Condition	μ_{FE} [$cm^2V^{-1}s^{-1}$]	Reference
IGO	Inkjet	450ºC	7.5	[211]
IGO	Inkjet	600ºC	5.5	[212]
IGZO	Inkjet	200ºC + Laser 400ºC	1.5 1.6	[213]
IGZO	Inkjet	300ºC	3-4	[214]
IGZO	Inkjet	400ºC	2.45	[215]
IGZO	E-jet	400ºC	1.3	[210]
InO	Inkjet	-	12.5	[216]
InO	Inkjet	150ºC + DUV	1	[217]
InO	Inkjet	225ºC	13.7	[218]
InO	Inkjet	250ºC	10	[219]
InO	Inkjet	300ºC	4.9	[58]
InO	Inkjet	350ºC + UV Ozone	9.9	[220]
InO	Aerosol Jet	400ºC	3.4	[221]
InO	E-jet	250ºC	5-7.7	[222]
IZO	Inkjet	600ºC	7.4	[223]
IZO	E-jet	500ºC	3.7	[209]
IZTO	Inkjet	600ºC	30	[224]
ZnO	Inkjet	150ºC	3	[225]
ZnO	Inkjet	200ºC	15-20	[226]
ZnO	Inkjet	150ºC 300ºC	0.4 4-6	[227]
ZnO	Aerosol Jet	250ºC	1.61	[228]
ZnO	Aerosol Jet	300ºC	1.9	[229]
ZTO	Inkjet	500ºC	0.58	[230]
ZTO	Inkjet	500ºC	5	[231]
ZTO	E-jet	500ºC	9.8	[63]

As we discussed in Chapter 2, ALD is a conformal process that generally results in uniform coverage of a substrate surface and additional steps are required for patterning. Area-selective ALD (AS-ALD) has been studied to selectively grow ALD films resulting in patterned ALD films as-deposited. Growth is selectively inhibited by partially covering the surface with a self-assembled monolayer (SAM) or polymer. The AS-ALD patterns have been formed using a variety of direct printing techniques from electron-beam induced deposition to self-assembly of templates. Previous studies have combined AS-ALD and ink-jet printing to fabricate customizable ZnO devices.[65] After some process optimization, the ZnO devices fabricated using ink-jet printing and AS-ALD exhibit mobility approaching 20 $cm^2V^{-1}s^{-1}$.[67] As we stated above, however, the use of ink-jet printing confines device scaling to ~20 μm without special tricks to push the resolution. Furthermore, there have been no demonstrations of AS-ALD of ZTO for TFTs.

In this chapter, we combine e-jet patterning of inhibitor polymers and ALD of thin-films, including transparent conducting oxides, semiconductors, and insulators, to fabricate a bottom-gate top-contact ZTO TFT. This work required development of the process to fabricate devices using e-jet patterning and AS-ALD with understanding of the physical and electrical properties of ALD deposited materials, the interfaces between the materials, and how the manufacturing process impacts device performance. Once the first device was realized, we then investigate the limitations to device performance and propose improvements. In the future, this process could enable customizable processing on a variety of substrates, including flexible and non-planar substrates.

7.2 Experimental Section

7.2.1 Atomic Layer Deposition and Electrohydrodynamic Jet Patterning

The custom-built ALD tool introduced in Chapter 2 was used to deposit AZO, Al_2O_3, and ZTO thin-films at a temperature range of 100-170ºC. A 130ºC thermal ZTO process was used as

developed in Chapter 2. The Al_2O_3 process used dimethylaluminum isopropoxide (DMAI) and H_2O as the precursors. A 15:1 Zn:Al ratio was used for the AZO film. More information about the ALD processes can be found in [232].

The e-jet system used was custom-made by the Barton Research Group at the University of Michigan.[61] The e-jet printing nozzles of size 5 and 10 μm were formed from pulled-glass and were coated in 5 nm gold to make them conductive. After gold coating, they were coated in a hydrophobic solution to prevent wetting of the nozzle body. The polyvinyl-pyrrolidone (PVP) was additively printed using 10 wt % PVP dissolved in dimethyl sulfoxide (DMSO). For subtractive printing, we start with a poly(methyl methacrylate) (PMMA) coated sample that was coated by spin-coating a 950 MW 2% anisole- PMMA solution at 4000 rpm for 45 s and then baking at 180ºC for 10 s. N-Methyl-2-pyrrolidone (NMP) was e-jet printed as the solvent for PMMA. Before the subtractive e-jet printing processing, the PMMA coated sample was exposed to UV O_3 for 20 min to improve solubility in NMP. Following subtractive printing, a 30 s O_2 plasma exposure at 100 W, 66 sccm O_2, 47 sccm Ar, and 50ºC was performed to remove any residual PMMA in the printed regions. More information about the e-jet process can be found in [232].

7.2.2 Thin-film Transistor Fabrication and Electrical Measurements

ZTO was deposited for the channel layer and was subjected to a 1 hour 500ºC post-deposition anneal before top AZO deposition, in ambient air with relative humidity less than 20%. Electrical measurements were taken in the dark at room temperature in ambient air using an HP4155A semiconductor parameter analyzer. The data were taken with continuous voltage sweeps from negative to positive V_{GS} and short integration.

7.3 Developing the E-jet and AS-ALD Process to Fabricate the First E-jet Patterned AS-ALD Deposited TFT

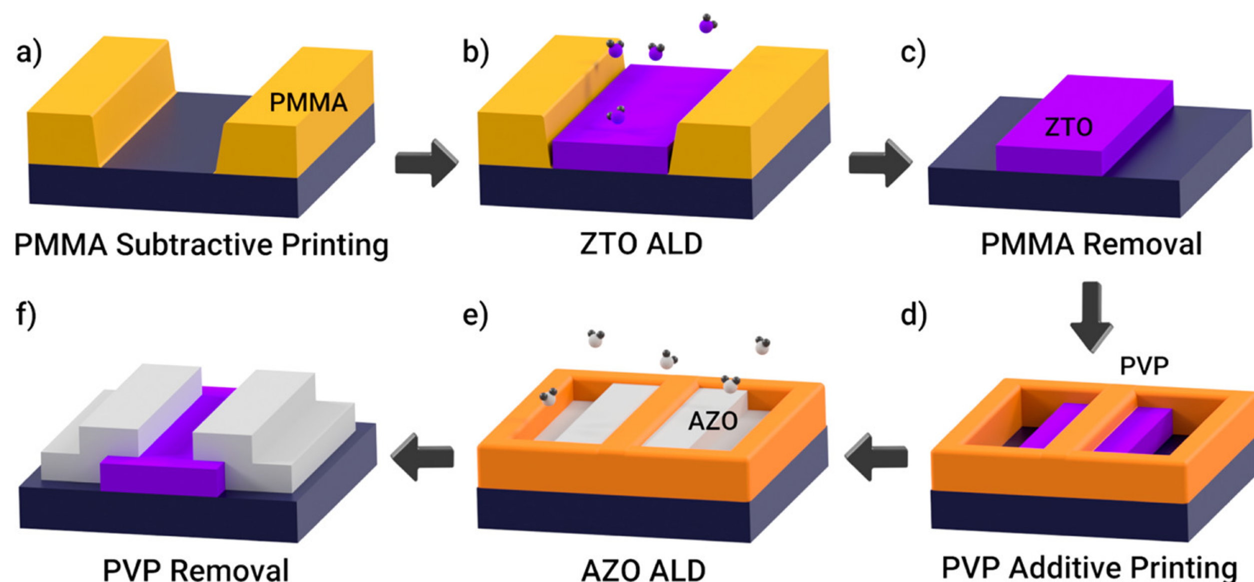


Figure 7.1 Process flow for TFT fabrication with subtractive and additive e-jet printing. Using substrative e-jet printing a), the ZTO pattern was first defined b). After PMMA removal and ZTO annealing, c) PVP was additively printed on top of the gate insulator (SiO_2) and ZTO film to isolate and define the channel between the source and drain using AZO contacts d). After selective deposition of AZO e), PVP was removed. The final device is schematically illustrated in f). Reprinted with permission from [232]. Copyright 2020 American Chemical Society.

The additive and subtractive e-jet/AS-ALD techniques developed in [232] can be combined to enable additive manufacturing of 3D architectures with deterministic control of geometry. To demonstrate fabrication of 3D metal oxide structures by a combination of subtractive and additive techniques, we developed the process shown in Figure 7.1 to fabricate a bottom-gate top-contact ZTO TFT. First, ZTO, the device active layer, was patterned on a n^+ heavily doped Si substrate with 100 nm thermal oxide using subtractive e-jet printing of a solvent on spin-coated PMMA. After removal of the ZTO inhibitor polymer, the ZTO film was annealed at 500ºC to improve its transport properties as discussed in Chapter 2. Finally, AZO, a transparent conducting oxide that will act as the source/drain contact electrode material, was patterned on top of the ZTO film using additive e-jet printing of PVP.

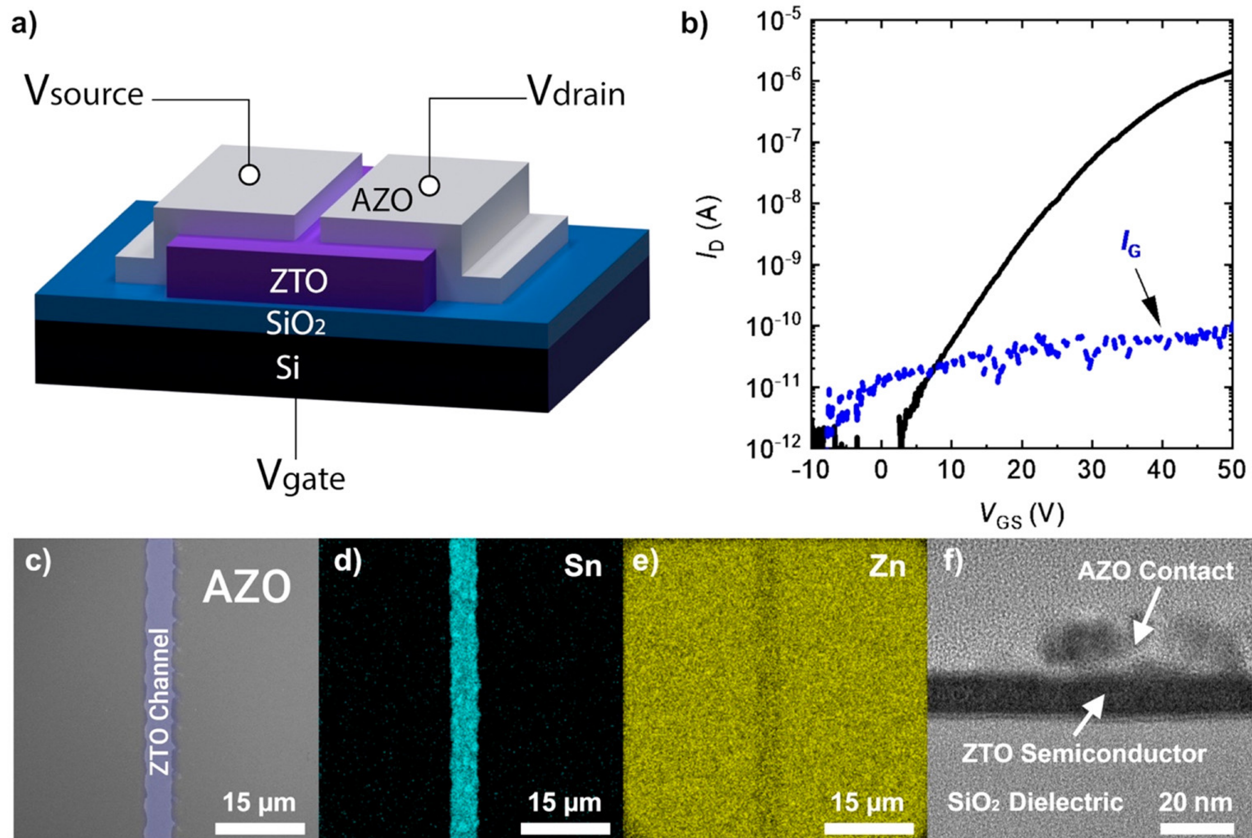


Figure 7.2 a) Illustration of TFT structure. In this first generation of e-jet/AS-ALD printed TFTs, device isolation is achieved by ensuring that the AZO source and drain contacts are separate from other AZO regions on the sample, and are the only AZO feature to contact the ZTO island. b) Transfer characteristics (I_D-V_{GS}) of a 5-μm channel length device with V_{DS} = 1 V. c) Top-down SEM image of a device with a 4-μm long channel with corresponding AES mapping of d) Sn and e) Zn. f) Cross-sectional scanning transmission electron microscopy (STEM) image of a 4-μm channel device after selective AZO deposition using additive PVP printing. Reprinted with permission from [232]. Copyright 2020 American Chemical Society.

The final device structure is illustrated in Figure 7.2a. Electrical measurements of the first TFTs fabricated using e-jet and AS-ALD show that the devices are well-behaved (Figure 7.2b), with 0 V turn-on, on current > 1 μA, and an on/off current ratio > 10^5. The devices have a minimum channel length of approximately 5 μm, 1 order of magnitude smaller than what has been achieved previously for inkjet printed inhibitors for AS-ALD.[67], [233] Thus, these devices demonstrate the ability to leverage the improved resolution of e-jet printing.

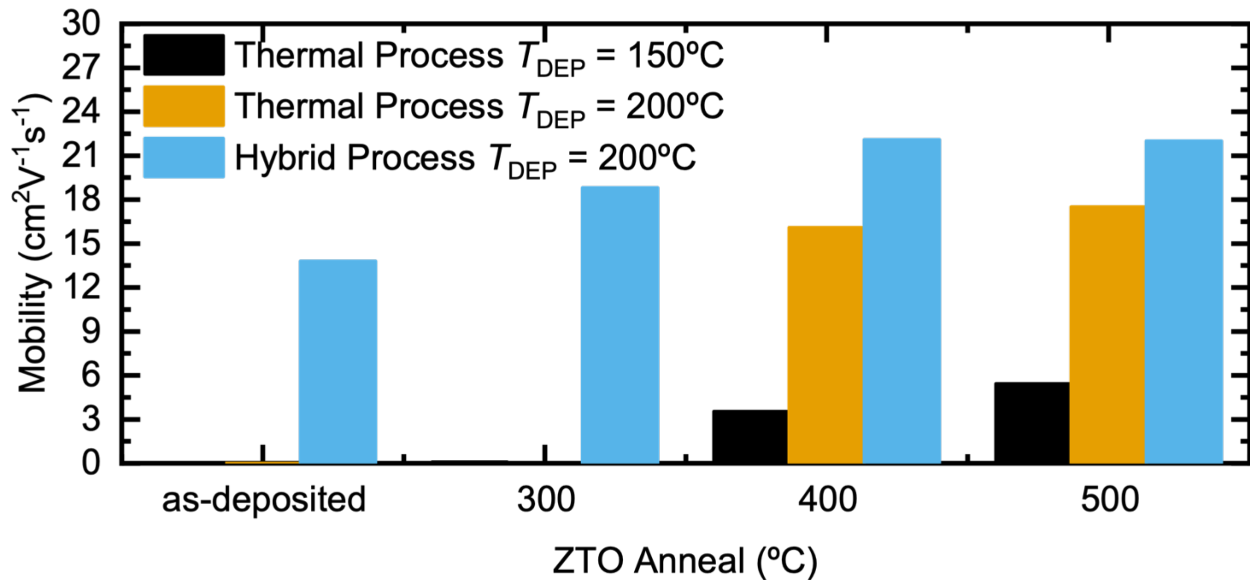


Figure 7.3 Field effect mobility as a function of anneal temperature for several ALD processes and deposition temperatures. From [234].

In Chapter 2, we achieved electron mobility > 22 $cm^2V^{-1}s^{-1}$ for TFTs fabricated with ALD ZTO using traditional photolithography methods. To successfully fabricate the e-jet and AS-ALD device in this initial demonstration, the ZTO ALD deposition temperature was reduced to 130ºC and thermal ALD was used, in order to maintain compatibility with the inhibitor polymers used here. As shown by Figure 7.3, reducing the temperature and using a thermal process results in lower ZTO mobilities which, at least partially, contributes to a reduced mobility of approximately 0.12 $cm^2V^{-1}s^{-1}$ seen here. In the next section, we will explore the limitations of device performance by optimizing the e-jet and AS-ALD processes to increase ZTO mobility and by studying the impact of the contacts on device.

7.4 Exploring Performance Limitations of the First E-jet/AS-ALD Device

7.4.1 The ALD ZTO Film

As discussed at the end of Section 7.3, compatibility with the polymeric inhibitors used for the AS-ALD process we developed required a lower performance ALD ZTO thin-film process. To

be compatible with the polymers, the ALD process must not remove the polymers and selective growth must be observed. Our highest performance films, as seen in Figure 7.3, use a hybrid process at 200ºC. This process, however, is not compatible with the AS-ALD process we developed because the PE-ALD portions of the process can remove the polymeric inhibitors. The next option is to use a high temperature (~200ºC) thermal (H_2O) process, but that process is not compatible either because at high deposition temperatures, the thermal process no longer exhibits selective growth. In this section, we develop and characterize a fourth ALD ZTO process to enable AS-ALD of higher performance ALD ZTO thin-films.

In Chapter 4, we studied ozone as an ALD oxidant for passivation processes because it minimized the change in device performance compared to H_2O and O_2-plasma based processes. Ozone has additional benefits of generally providing higher growth rates, film density, and purity because it has a higher oxidation protentional compared to H_2O.[235]–[237] We found in Chapter 2 that a higher density film corresponded with a higher performance ZTO film and because ozone results in higher density films compared to H_2O, we next develop an O_3-based ZTO process.

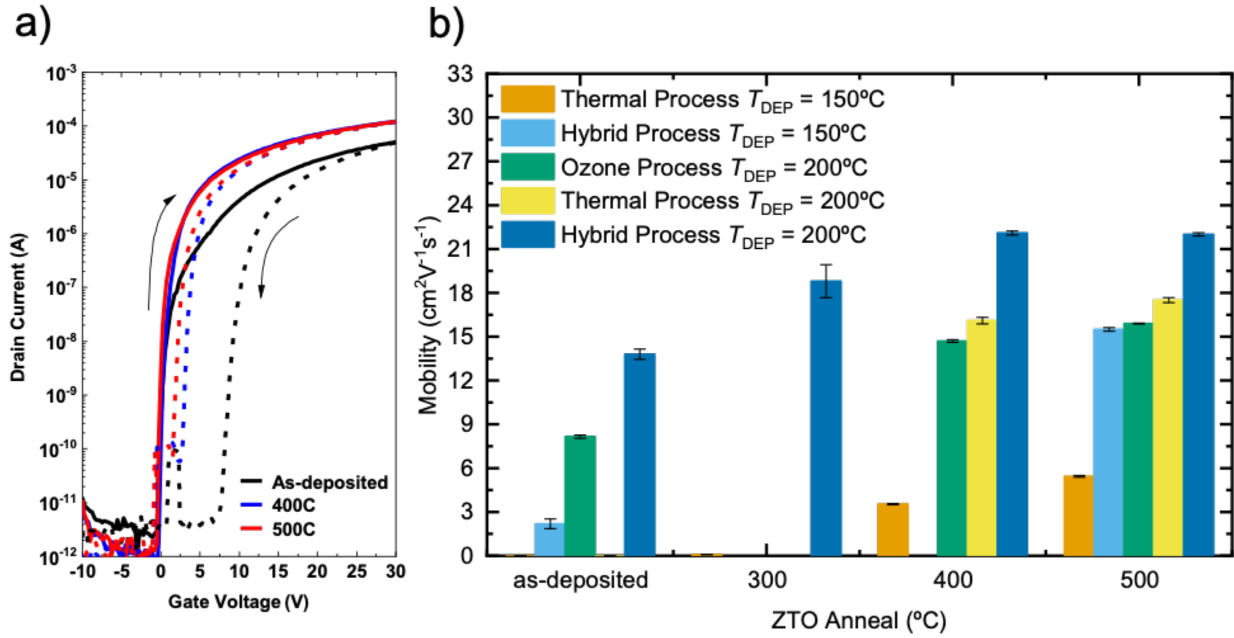


Figure 7.4 a) Transfer characteristics (I_D-V_{GS}) of O_3-based ALD ZTO TFTs deposited at 200ºC with c_{Sn} = 21% as a function of post-deposition anneal temperature. b) Field effect mobility as a function of anneal temperature, extracted from 27 V < V_{GS} < 30 V for several of the ALD ZTO processes we have developed. Error bars indicate standard deviation from measurement of at least five different transistors for each condition.

After tuning in the c_{Sn} to 21%, the TFTs annealed at 500ºC fabricated using the O_3-based ALD process exhibit a μ_{FE} of 15.9 $cm^2V^{-1}s^{-1}$, an *SS* of 0.25 V dec^{-1}, and a turn-on voltage near 0 V (Figure 7.4a and Table 7.2). Comparing this to the other 200ºC processes, Figure 7.4b and Table 7.2, we see that when annealed at 500ºC the O_3-based films underperform the μ_{FE} of the hybrid process, but is comparable with the thermal process. As the O_3-based process is also compatible with our AS-ALD process and the films outperform other compatible films, we have achieved our goal of finding a process compatible with inhibition that also yields good mobility. Furthermore, we beat the previous record μ_{FE}, 13.6 $cm^2V^{-1}s^{-1}$, for O_3-based ALD ZTO while using a lower temperature process.[201] In the next section, we begin to integrate the O_3-based ALD process with the e-jet/AS-ALD process.

Table 7.2 Comparison of O_3-based ALD ZTO performance with some of our other ALD ZTO processes

ALD Type (Deposition Temperature)	Post-Deposition Anneal Temperature	μ_{FE} [$cm^2V^{-1}s^{-1}$]	*SS* [$V\ dec^{-1}$]	V_{ON} [V]
Thermal (150ºC)	As-deposited	9.90×10^{-4}	2.2	7.4
Thermal (150ºC)	500ºC	5.44	0.57	0.54
Ozone (200ºC)	As-deposited	8.16	0.36	0.20
Ozone (200ºC)	500ºC	15.9	0.26	-0.05
Thermal (200ºC)	As-deposited	9.56×10^{-5}	4.6	23
Thermal (200ºC)	500ºC	17.5	0.30	1.8
Hybrid (200ºC)	As-deposited	13.8	0.43	4.6
Hybrid (200ºC)	500ºC	22.0	0.28	-0.78

7.4.2 Ohmic Contacts to ALD ZTO

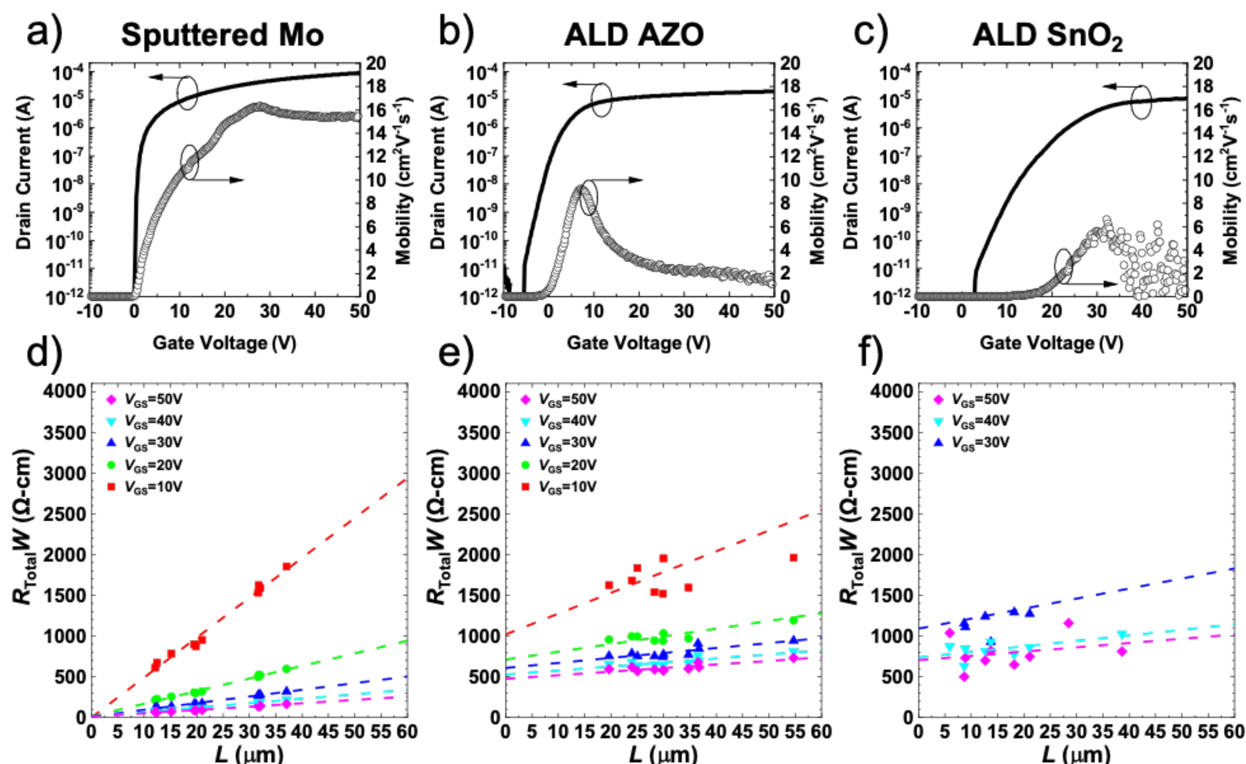


Figure 7.5 Transfer characteristics (I_D-V_{GS}) plotted on the left *y*-axis for devices with 200ºC O_3-based ZTO patterned by photolithography and annealed at 500ºC with a) sputtered Mo, b) ALD AZO, or c) ALD SnO_2 top source and drain contacts patterned by e-jet. Extracted field-effect mobility is plotted using the open circles on the right *y*-axis. Total width-normalized resistance of the same TFTs with d) sputtered Mo, e) ALD AZO, or f) ALD SnO_2 top source and drain contacts patterned by e-jet.

Now that we have developed a high-performance ALD ZTO process that is compatible with our AS-ALD process, we investigate the impact of contact resistance on our devices. To do this, we deposited ZTO using the 200ºC ozone process developed in Section 7.4.1, patterned it using photolithography, annealed it at 500ºC, and then used e-jet to pattern top source and drain contacts using sputtered Mo, ALD AZO, or ALD SnO_2. After the devices were fabricated, we measured transfer characteristics at 1 V V_{DS} and extracted μ_{FE} (Figure 7.5a-c). In Figure 7.5a-c, we can see that initially the extracted μ_{FE} increases with V_{GS} but then peaks and rolls off as V_{GS} increases. To explain these mobility roll-offs, we must consider the impact of contact resistance on our extraction of μ_{FE}.

Typically, we consider ohmic contacts to be perfect with no contact resistance resulting in the applied V_{DS} being identical to the voltage across the channel. In reality, contact resistance is non-zero and will reduce the voltage across the channel by $I_D R_C$. As I_D increases with increasing V_{GS}, the voltage dropped across the contacts, $I_D R_C$, also increases. Once the voltage drop across the contacts becomes a non-negligible percent of V_{DS}, the effective mobility begins to roll-off as seen in Figure 7.5a-c. How much the effective mobility rolls-off, and at what I_D the roll-off occurs, depends on the value of R_C. The worse the contact resistance, the more roll-off and the lower the peak mobility.

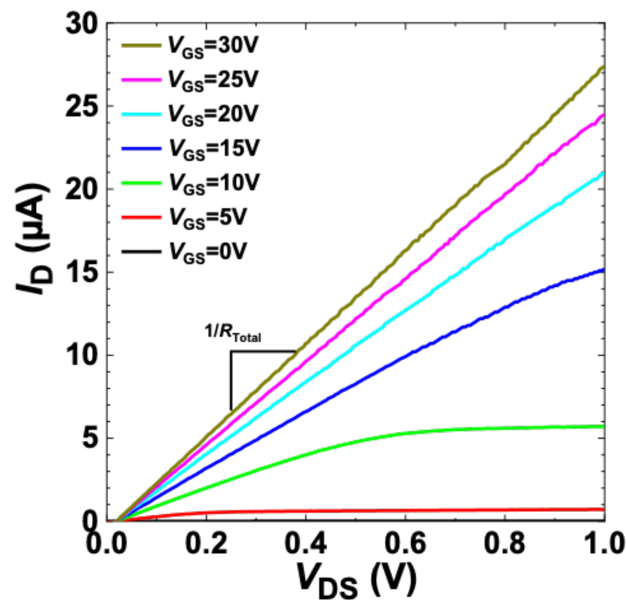


Figure 7.6 Output characteristics (I_D-V_{DS}) of e-jet/AS-ALD AZO contact TFTs.

Now that we know that contact resistance limits our devices because of the observed roll-off in mobility, we quantify it using transmission line method.[106], [238] First we measure output characteristics as shown in Figure 7.6. The inverse slope of the output curve in the linear region gives the total resistance by

$$R_{\mathrm{Tot}} = \frac{V_{\mathrm{DS}}}{I_{\mathrm{D}}} \approx \frac{R_{\mathrm{sh}}}{W}(L + 2L_{\mathrm{T}}) \quad (7.1)$$

where R_{sh} is the sheet resistance of the ZTO and L_T, or the transfer length, is the distance over which most of the current transfers between the semiconductor and metal.[106] By plotting the width normalized total resistance, $R_{Total}W$, as a function of channel length, as shown in Figure 7.5d-f, we can extract the width normalized contact resistance, $R_C W$, as the y-axis intercept when $L = 0$ μm.

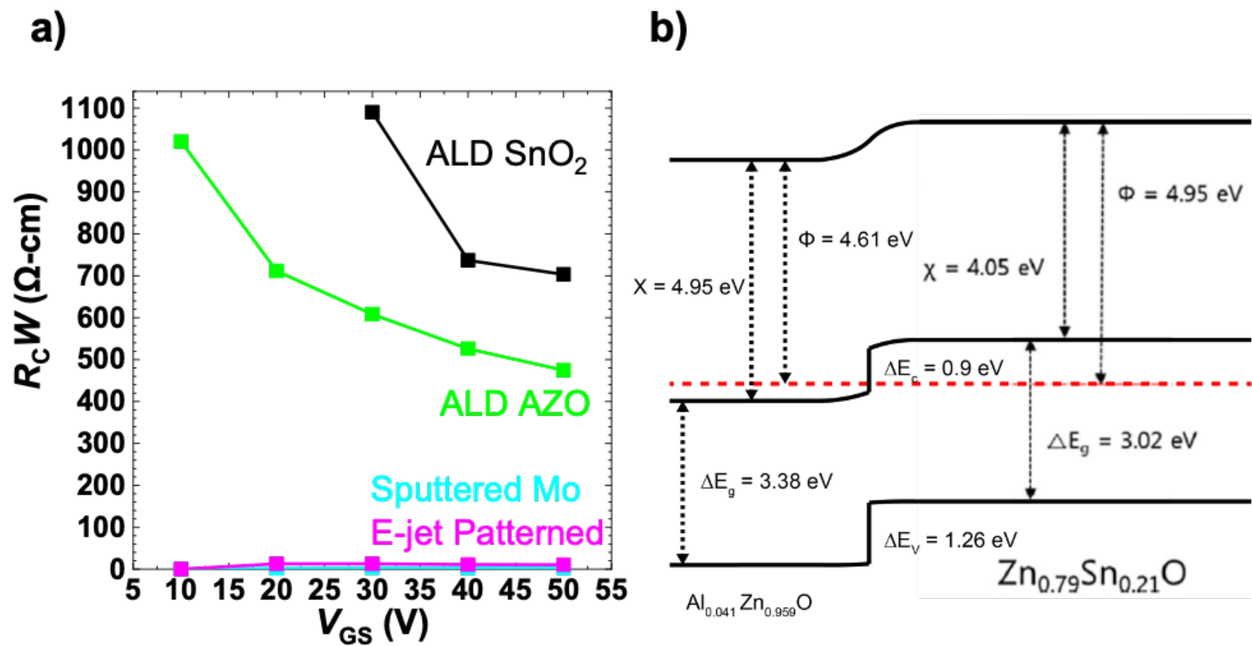


Figure 7.7 a) Width-normalized contact resistance of ZTO TFTs as a function of V_{GS}. The cyan curve shows sputtered Mo patterned by photolithography while the magenta curve shows Mo patterned by e-jet. As there is no significant change between the two patterning techniques, we conclude that the e-jet process is not limiting performance. b) Approximate band diagram of the AZO/ZTO interface, adapted with permission from [55], [239], [240].

By plotting the width-normalized contact resistance versus V_{GS} in Figure 7.7a, we see that the ALD AZO contacts show a dependence on V_{GS} and about a 40x increase in contact resistance value, compared to the sputtered Mo contacts. We sketch the band diagram for the AZO heterojunction with ALD ZTO in Figure 7.7b. The band diagram shows a barrier between the AZO and ZTO of about 0.9 eV which may cause the V_{GS} dependence: as V_{GS} increases, the bands will bend, decreasing the barrier. Finally, we calculate specific contact resistance, ρ_C, of the films to

be approximately 1 Ω cm^2 for AZO and 30 μΩ cm^2 for Mo. The AZO specific contact resistance is five orders of magnitude greater than that of Mo. The transfer length, L_T, is approximately 53 and 0.30 μm for ALD AZO and sputtered Mo, respectively, and represents the minimum effective channel length for each contact material (L must be >> 2 L_T in order for channel resistance to dominate).[106] As channel length scaling is required for high-speed performance, the e-jet/AS-ALD contacts to ZTO must be improved.

There are a several material options to make source and drain contacts to ALD ZTO. First, contacts can be directly printed using e-jet.[241], [242] E-jet patterned materials, as discussed in Section 7.1, are generally lower quality than ALD films and thus do not outperform the AZO process we have developed. The next option is to look at materials that can be deposited and patterned by AS-ALD. One possible metallic choice is copper,[243] but Cu has also been shown to cause significant mobility roll-off with channel length scaling.[244] Another material, SnO_2, has been shown to be suitable as a transparent conducting oxide, but has not been studied as a contact material to ALD ZTO.[245] To see if we can make a high-quality SnO_2 conductor, we deposited SnO_2 using a 200ºC O_3-based ALD process. The deposited film had resistivity of 5.92 ± 1.8 mΩ cm, about an order of magnitude higher than previous results.[246]

We then applied the SnO_2 film as a top contact material and we measured the transfer curves shown in Figure 7.5c. Of the three contacts studied, the SnO_2 performs the worst with the highest SS and lowest μ_{FE}. The low-performance may be caused by the contact resistance that quickly increases below 30 V V_{GS} (Figure 7.7a). The increase in R_C with decreasing V_{GS} may indicate the SnO_2 is semiconducting and the SS captures the turn-on of the SnO_2 rather than the ZTO film. Further studies to improve SnO_2 contacts could investigate increased deposition temperatures or contact anneals.[246]

7.5 Towards an All E-jet/AS-ALD Device

In Section 7.3, the fabricated devices used bottom Si and SiO_2 as common gate and gate insulator, respectively. Common gated devices cannot be switched individually to be used in a circuit. To create separated gate devices, we must first develop a process that uses e-jet and AS-ALD to pattern all layers of the device, or an all e-jet/AS-ALD device. The first step in doing this is designing a process that works for the gate and gate insulator. As we already have an e-jet/AS-ALD process for AZO, we can use that for the gate electrode. The AZO process requires alumina cycles and can be patterned by e-jet/AS-ALD so we will use alumina for the gate insulator.

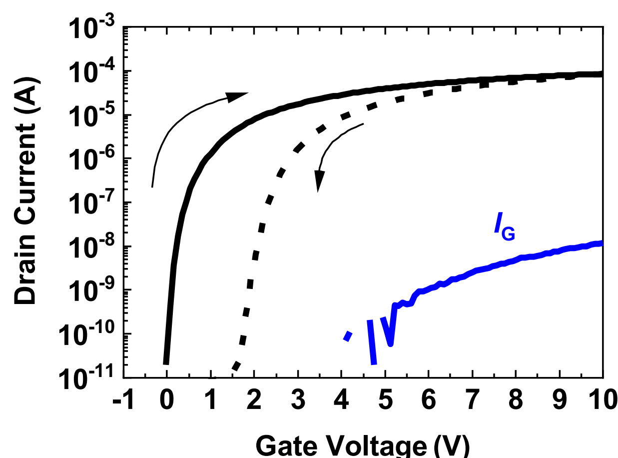


Figure 7.8 Transfer characteristics (I_D-V_{GS}) of devices with ALD AZO gate and Al_2O_3 gate insulator. The forward *I-V* curves are indicated by the solid lines and the reverse curves are indicated by the dashed lines. Gate leakage current is indicated by the blue line.

To check material and process compatibility, we fabricate devices with blanket gate and gate insulator layers. First, we deposit an *in situ* stack of 40 nm AZO, 30 nm Al_2O_3, and 10 nm of ZTO using a 200ºC thermal process. The ZTO is then wet-etched for device isolation and the sample is then annealed at 500ºC. Next, the Al_2O_3 is wet-etched to allow probing of the bottom AZO. Finally, approximately 100 nm of Mo is sputtered and patterned by liftoff to form the source and drain electrodes. Transfer characteristics are shown in Figure 7.8 and the devices have a V_t of 1.44 V, an *SS* of 0.213 V dec^{-1} and a ΔV_C of 0.325 V. While we have demonstrated material and

process compatibility for an all ALD device, future work is needed to pattern each layer by e-jet and AS-ALD.

7.6 Conclusions and Future Work

7.6.1 Conclusions

In this chapter we developed a process to additively manufacture TFTs using electrohydrodynamic jet patterning of inhibitor polymers and area-selective ALD. The first demonstrated device using this process has a channel length of 5 μm, an order of magnitude smaller than what has been achieved with inkjet patterning and AS-ALD, and are well-behaved with a V_{on} of 0 V, I_{on} greater than 1 μA, and an on/off current ratio > 10^5. Effective mobility, on the other hand, was much lower for the e-jet/AS-ALD device than the photolithographically patterned devices in Chapter 2. We identified two sources of performance limitation. The first is the low temperature thermal ALD process required for compatibility with the polymeric inhibitors and the second is high contact resistance between ALD ZTO and the AZO used for source and drain contacts.

To improve the performance of the ZTO layer, we developed a fourth ALD ZTO process using O_3 as the oxidant. TFTs fabricated with the O_3-based ALD ZTO film have good mobility > 15 $cm^2V^{-1}s^{-1}$. With a high-performance ALD ZTO film compatible with our AS-ALD process, we then looked at looked at the material choices for contacts to ALD ZTO. One option we investigated was ALD SnO_2 that shows promising film resistivity but requires future work to improve the performance as a contact material. Finally, to enable a separated gate device with all e-jet/AS-ALD layers, we demonstrated process and material compatibly of using ALD AZO and Al_2O_3 as the bottom gate and gate insulator. This chapter presents significant advancements in achieving customizable manufacturing of thin-film electronics based on ALD ZTO.

7.6.2 Outstanding Scientific Questions and Future Work

This work raised several outstanding scientific questions:

1) Can ALD materials be used to form a high-quality ohmic contact to ALD ZTO? In Section 7.4.2 we deposited SnO_2 with O_3-based ALD that showed promising resistivity, but future work is required to improve performance a contact material to ALD ZTO. Questions remain on the band alignment and interfacial reactions between the ZTO and SnO_2. The high-performance of our sputtered Mo contact is dependent on energetic ion bombardment creating defects that make the region heavily doped. Future work could investigate if the plasma processes of many ALD tools could be used *in situ* to create heavily doped regions in the ZTO, similar to the ion bombardment, before depositing the contact materials.

2) While each process necessary to fabricate a fully e-jet/AS-ALD TFT with separated gate has been demonstrated in this chapter, future work is required to combine all those processes to demonstrate devices.

3) Can a buffer layer between the gate insulator and ZTO be applied to improve the *SS*? In Section 2.6 we demonstrated *SS* approaching the Boltzmann limit using an *in situ* gate insulator. An *in situ* gate insulator may not be possible with our current e-jet/AS-ALD process because each layer is patterned separately during its deposition. Previous work has shown a buffer layer, a thin layer of the gate insulator material, deposited right before the semiconductor can improve device performance.[67] A similar buffer layer could be deposited after the e-jet patterning and *in situ* before the ZTO deposition possibly leading to near Boltzmann *SS*.

4) Can these devices be scaled to the sub-micron precision of e-jet? The goal of using e-jet patterning is to scale device dimensions to increase the cut-off frequency f_T, where f_T is inversely proportional to square of the device length as shown in Equation (7.2).[247]

$$f_T = \frac{\mu V_{DS}}{2\pi}\frac{1}{L^2} \tag{7.2}$$

As the device length approaches sub-micron, there are undesirable short channel effects. In particular, for AOS devices, source and drain contact resistance will impact device performance with decreased channel lengths. The contact resistance, R_C, is controlled by the metal/semiconductor barrier height, ϕ_{MS}, and the semiconductor doping, N_D, as shown in Equation (7.3).

$$R_C = \exp\left[\frac{2\sqrt{\varepsilon_s m^*}}{h}\left(\frac{\phi_{MS}}{\sqrt{N_D}}\right)\right] \tag{7.3}$$

In addition to R_C, the overlap between the gate and source/drain electrodes, L_{OV}, will impact the overlap capacitance, C_{OV}, which also limits f_T. Therefore, in addition to contact resistance, the frequency limit must be studied in terms of both R_C and C_{OV} as well as any other short channel effects while building up the capability to manufacture these devices using e-jet printing and AS-ALD.

Chapter 8 Conclusion and Future Work

8.1 Contributions to date

This thesis enables scalable manufacturing of thin-film electronics for beyond-display applications, in particular for 3D monolithic integration and customizable thin-film electronics, through advancements in AOS devices, materials, and processes. The main contributions of this thesis are summarized as follows:

1. Three ALD ZTO processes were developed and characterized leading to as-deposited semiconducting behavior with μ_{FE} as high as 13.8 cm^{2}V^{-1}s^{-1} and record mobility of greater than 20 cm^{2}V^{-1}s^{-1} when annealed at BEOL compatible temperatures. As demonstrated in Chapter 2, the high-performance films were achieved through aggressive process optimization leading to high-density films with a low concentration of oxygen vacancies. After developing the high-performance semiconductor, we then fabricated devices with an *in situ* gate insulator resulting in a low density of interface defects and an excellent *SS* of 60 mV dec^{-1}, very close to the Boltzmann limit and better than other BEOL compatible TFT demonstrations. Together, this work enables high-performance TFTs compatible with 3D monolithic on low-voltage CMOS.
2. To exploit the advantages of the wide bandgap of AOS thin-films, we developed high-voltage thin-film transistors in Chapter 3. First Silvaco Atlas simulations were used to understand the impact of device architecture on breakdown voltage and on-resistance. Then, to validate the understanding, we fabricated and measured devices with specific gate-drain offset lengths. Encapsulated devices showed normal on/off current ratios and breakdown voltages above 100 V were demonstrated. Using a simple gate/drain offset structure, the breakdown voltage

saturated while the on-resistance continued to increase with increasing offset length. Finally, Silvaco Atlas modeling was used to design a future optimized device architecture using both offsets and field plates to co-optimize breakdown voltage and on-resistance. The ability to deposit AOS materials directly to fabricate HVTFTs on Si ICs adds new functionality as an HV interface to aggressively scaled low-voltage (V_{DD} < 1 V) Si CMOS.

3. The encapsulation layer used in the Chapter 3 degraded the transfer characteristics and shifted the turn-on voltage to negative values. In Chapter 4 we investigated the impact of film thickness and ambient environment on TFT characteristics. Using our ZTO solution-process, we show that varying the solution molarity and number of spin-coated layers can be used to reduce ZTO film thickness to 6 nm with resulting device characteristics only dependent on the final film thickness. Thinner-films show better performance and under vacuum the hysteresis was reduced from 12.65 V to -0.05 V due to desorption of molecules at the back channel without re-adsorption. By implementing an O_3-based ALD Al_2O_3 passivation layer, surface interactions were blocked leading to normal TFT behavior with a hysteresis of 0.85 V and minimal performance degradation.
4. With the ambient instability solved in Chapter 4, we studied the temporal and bias stress stability of devices in Chapter 5. Devices exhibit slight changes within the first 25 days of aging, followed by excellent temporal stability for up to > 178 days. The positive bias stress instability, found to be predominately caused by interactions with ambient molecules in samples without passivation, is significantly reduced for sample with passivation. Passivation, however, causes and increase in contact resistance, *SS*, and NBIS instability which are explained by changes in the molybdenum ohmic contacts and defects at the interface between

the passivation layer and ZTO. By understanding and improving the stability of AOS TFTs, this works move towards adoption of these films for beyond-display technologies.

5. Through reactive sputtering of AgO_x on the top surface of ALD ZTO, we demonstrate the first Schottky contact to ALD ZTO in Chapter 6. With both the Schottky contact and ohmic contact deposited on the same plane, these first devices suffer from the series resistance challenges of a lateral structure. To move towards a vertical thin-film diode, we studied several materials as bottom contacts to ALD ZTO. Silver-based contacts were eliminated because of instabilities caused by its low oxidation potential. Pallidum and platinum may be promising as bottom Schottky contacts, but further work is required to remove surface and edge conduction as possible sources of parallel parasitic current.
6. We fabricated the first TFTs using a novel additive manufacturing technique by developing the design rules for using electrohydrodynamic jet printing and area-selective ALD to fabricate functional devices in Chapter 7. The first devices fabricated with this process have channel lengths of approximately 5 μm, an order of magnitude smaller than what has been achieved through ink-jet and AS-ALD, with reasonable device behavior. The main limiters to device performance were identified as the low-performance ALD ZTO layer and the contact resistance of ALD ohmic contacts. To improve the performance of the ALD ZTO layer, we develop a fourth ALD ZTO process using O_3 as the oxidant that is compatible with our AS-ALD process and has a good μ_{FE} greater than 15 $cm^2V^{-1}s^{-1}$. Finally, we demonstrate process and material compatibility for fabrication of separated gate devices with all layers deposited and patterned by e-jet and AS-ALD. This work demonstrates the ability to approach sub-μm pattering using customizable scalable additive manufacturing.

8.2 Future Work

The development of high-performance ALD ZTO films compatible with the additive manufacturing process developed in this thesis are great advancements in enabling customizable scalable manufacturing of thin-film electronics. Future studies can improve the performance of the additively manufactured devices to enable high-frequency thin-film electronics. The following future work, summarized in Figure 8.2, can improve performance and answer some of the scientific questions raised by this thesis.

1. **Tuning of the Chemical States of Interfaces:** In this thesis, oxygen plasma and ozone were used as oxidants to create high-quality ALD films. There are challenges, however, forming Schottky contacts and ALD-based ohmic contacts to the ALD AOS film. In both cases, the AOS film interface properties are important for the contact performance. For example, a high concentration of oxygen vacancies is necessary for ohmic contacts and a low concentration of oxygen vacancies is necessary for Schottky contacts.[78], [182] By incorporating *in situ* oxidation and/or reduction, through ozone and/or O_2/H_2 plasma treatment, at these interfaces, the chemical states may be tuned to promote formation of high quality ohmic or Schottky contacts (Figure 8.2).[163] This work would require more precise understanding of how these states impact the contact electrical behavior. This knowledge could then be used to tune the states to form high quality contacts to the ALD ZTO film using processes compatible with the nanomanufacturing platform we have developed in this thesis.
2. **Grading of Ternary Materials for Passivation and Stability:** The work performed in this thesis achieved high-quality films with homogenous multi-component alloy films. To realize complex device geometry, it is necessary to create three-dimensional heterogeneity. ALD is uniquely able to deposit layers with graded chemical composition at the atomic-scale. Previous

work using ALD to create a composition gradient channel of aluminum-doped zinc oxide (AZO) by varying the amount of aluminum was performed to create high-performance, stable devices.[248] In that work, when the gradient direction was properly engineered, the energy bands were advantageously bent by the gradient to simultaneously achieve good mobility and back-channel passivation. These devices were limited to mobilities no greater than 4.5 $cm^2V^{-1}s^{-1}$ because aluminum is an impurity in ZnO causing increased electron scattering. The mobility of the ZTO deposited using the processes we have developed in this thesis is much higher than that of AZO, and published work on the material properties of ALD deposited ZTO has shown varying the tin composition fraction varies the bandgap of the film.[49], [50], [55] As such, using a gradient of ZTO, varying the tin composition fraction, may align the bands in a way to create an *in situ* back-channel passivation layer, without sacrificing device performance (Figure 8.1).

3.

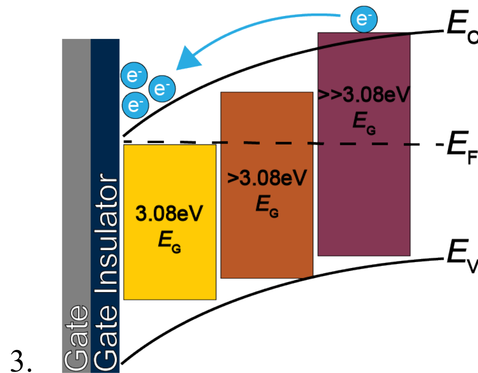


Figure 8.1 Schematic illustration showing advantageous band bending caused by grading tin composition to form *in situ* back channel passivation.

4. **Grading and Alloying of Ternary Materials for Contacts:** A second application of engineered gradients is for minimizing ohmic contact resistance, which enables high-quality, dense interconnects between integrated system components. Our first-generation devices additively manufactured using e-jet and AS-ALD in Chapter 7 showed performance that was not as good as that of our traditionally-fabricated devices (Chapter 2). We identified the reasons

for the performance degradation in Section 7.4. One major reason is the low-quality ohmic contact created between the transparent conducting oxide (AZO) and the semiconductor (ZTO). The electrodes have a high contact resistance, so that voltage is dropped across the contact instead of across the transistor channel, leading to lower on-current. In traditional fabrication processes, graded or alloyed contacts have successfully been used to improve contact quality. [249], [250] Improving ohmic contacts may be possible by exploiting ALD to grade the ZTO and/or AZO near their interface *in situ* without the need for the high temperature processes that are normally required to drive alloying.

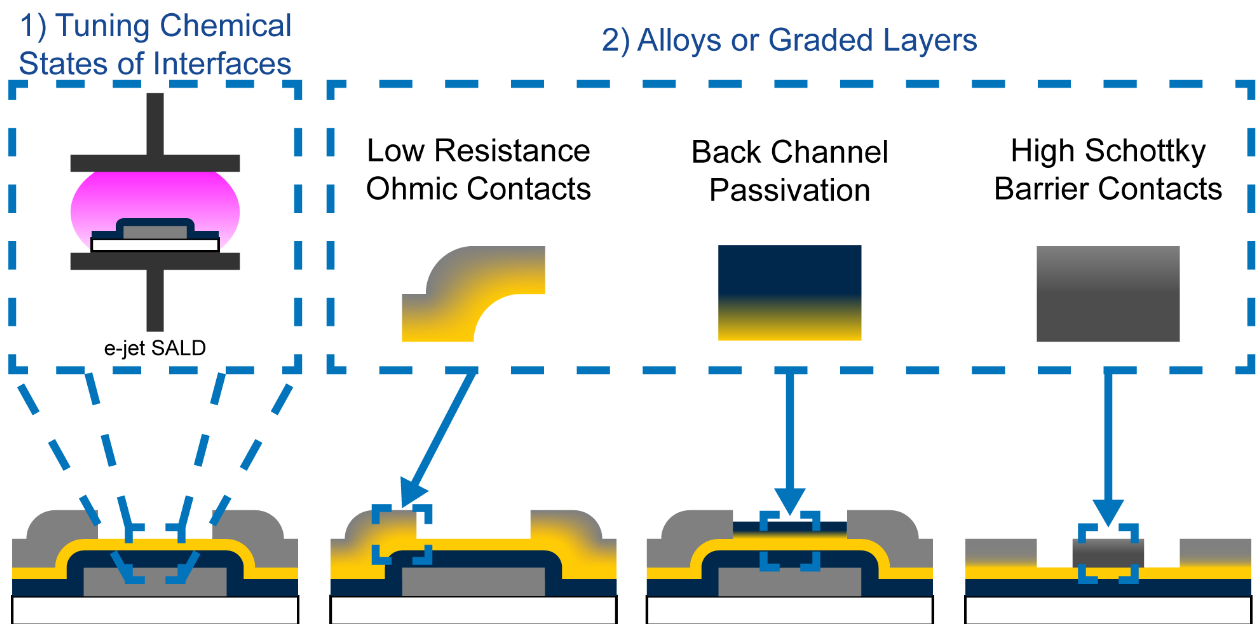


Figure 8.2 Schematic illustration of the proposed future work. 1) Tuning of chemical states or interfaces using oxidation/reduction. 2) More fully exploiting the capabilities of ALD to form alloys and/or graded layers to improve performance past vertically homogenous films by creating low resistance ohmic contacts, back channel passivation, and high Schottky barrier contacts. These key technologies present new challenges that will require further development of processes and control rules to guide selective-area growth.

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