Energy-Efficient Wireless Connectivity and Wireless Charging for Internet-of-Things (IoT) Applications

by

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DEDICATION

To my beloved family, friends, and advisors.

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ABSTRACT

During the recent years, the Internet-of-Things (IoT) has been rapidly evolving. It is indeed the future of communication that has transformed Things of the real world into smarter devices. To date, the world has deployed billions of "smart" connected things. Predictions say there will be 10's of billions of connected devices by 2025 and in our lifetime we will experience life with a trillion-node network. However, battery lifespan exhibits a critical barrier to scaling IoT devices. Replacing batteries on a trillion-sensor scale is a logistically prohibitive feat. Self-powered IoT devices seems to be the right direction to stand up to that challenge. The main objective of this thesis is to develop solutions to achieve energy-efficient wireless-connectivity and wireless-charging for IoT applications.

In the first part of the thesis, I introduce ultra-low power radios that are compatible with the Bluetooth Low-Energy (BLE) standard. BLE is considered as the preeminent protocol for short-range communications that support transmission ranges up to 10's of meters. Number of low power BLE transmitter (TX) and receiver (RX) architectures have been designed, fabricated and tested in different planar CMOS and FinFET technologies. The low power operation is achieved by combining low power techniques in both the network and physical layers, namely: backchannel communication, duty-cycling, open-loop transmission/reception, PLL-less architectures, and mixer-first architectures. Further novel techniques have been proposed to further reduce the power the consumption of the radio design, including: a fast startup time and low startup energy crystal

oscillators, an antenna-chip co-design approach for quadrature generation in the RF path, an ultra-low power discrete-time differentiator-based Gaussian Frequency Shift Keying (GFSK) demodulation scheme, an oversampling GFSK modulation/demodulation scheme for open loop transmission/reception and packet synchronization, and a cell-based design approach that allows automation in the design of BLE digital architectures. The implemented BLE TXs transmit fully-compliant BLE advertising packet that can be received by commercial smartphone.

In the second part of the thesis, I introduce passive nonlinear resonant circuits to achieve wide-band RF energy harvesting and robust wireless power transfer circuits. Nonlinear resonant circuits modeled by the Duffing nonlinear differential equation exhibit interesting hysteresis characteristics in their frequency and amplitude responses that are exploited in designing self-adaptive wireless charging systems. In the magnetic-resonance wireless power transfer scenario, coupled nonlinear resonators are proposed to maintain the power transfer level and efficiency over a range of coupling factors without active feedback control circuitry. Coupling factor depends on the transmission distance, lateral, and angular misalignments between the charging pad and the device. Therefore, nonlinear resonance extends the efficient charging zones of a wireless charger without the requirement for a precise alignment.

Chapter 1

Introduction and Motivation

1.1. Evolution of Internet-of-Things (IoT) devices

The first idea of the Internet of Things (IoT) appeared almost three decades ago, but core technologies behind it, e.g. Internet, RFID, and embedded computer systems, had already existed and have been under development for many years prior that [1]. Sensor nodes were developed in the mid-1990s to sense the data from uniquely identified embedded devices and seamlessly exchange the information to realize the basic idea of IoT [2-4]. In 1999, device-to-device communication was introduced by Bill Joy in his taxonomy of the internet, and the term 'Internet of Things' was used for the first time by Ashton [5, 6]. From 2000 and onwards, IoT connectivity gained momentum for many applications, becoming part of a shared vision for the future of the internet. The roadmap of the Internet of Things from 2000 onwards is shown in Fig. 1.1 [1].

The considerable rise in the number of objects connected to the internet, either by wire or wireless, has caused research growth in this area from both industry and academia [2]. Today, the growth of small and cheap computing devices endowed with sensing and communication capabilities promote the realization of the vision of IoT. Virtually all everyday objects can be connected to the internet, including smart homes, medical equipment, sports equipment, and vehicles. Therefore, IoT is a concept that has the potential to impact our lives and the way we work [7]. It can dramatically improve security, energy efficiency, education, health, and many other

aspects of daily life for consumers [8-13]. IoT is an evolution of mobile, embedded applications and everything that is connected to the internet to integrate greater communication ability and use data analytics to extract meaningful information. Thus, two main components of an "IoT object" are required: (1) the ability to capture data via sensors and (2) transmit data via the Internet [14, 15].

Experts predict that the IoT will have a substantial economic impact with that many possible applications and probably more unimagined ones. As per McKinsey, the growth of the IoT market would be from 4 trillion USD to 11 trillion USD by 2025 [16], whereas Statista predicts it to be 1.6 trillion USD by 2025 [17]. Regarding number of connected IoT devices worldwide, CABA anticipates >70 billion devices on the Internet by 2025 [18] (Fig. 1.2(a)) while Statista forecasts >30 billion connected devices by 2025 [19] as shown in Fig. 1.2(b).

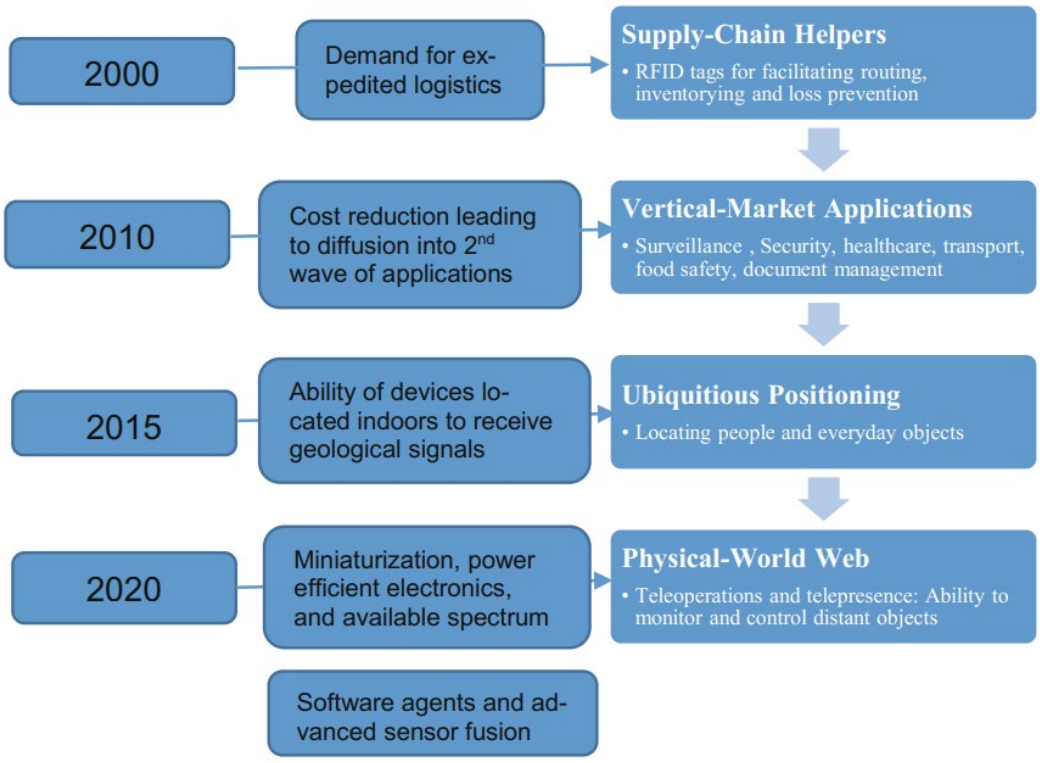
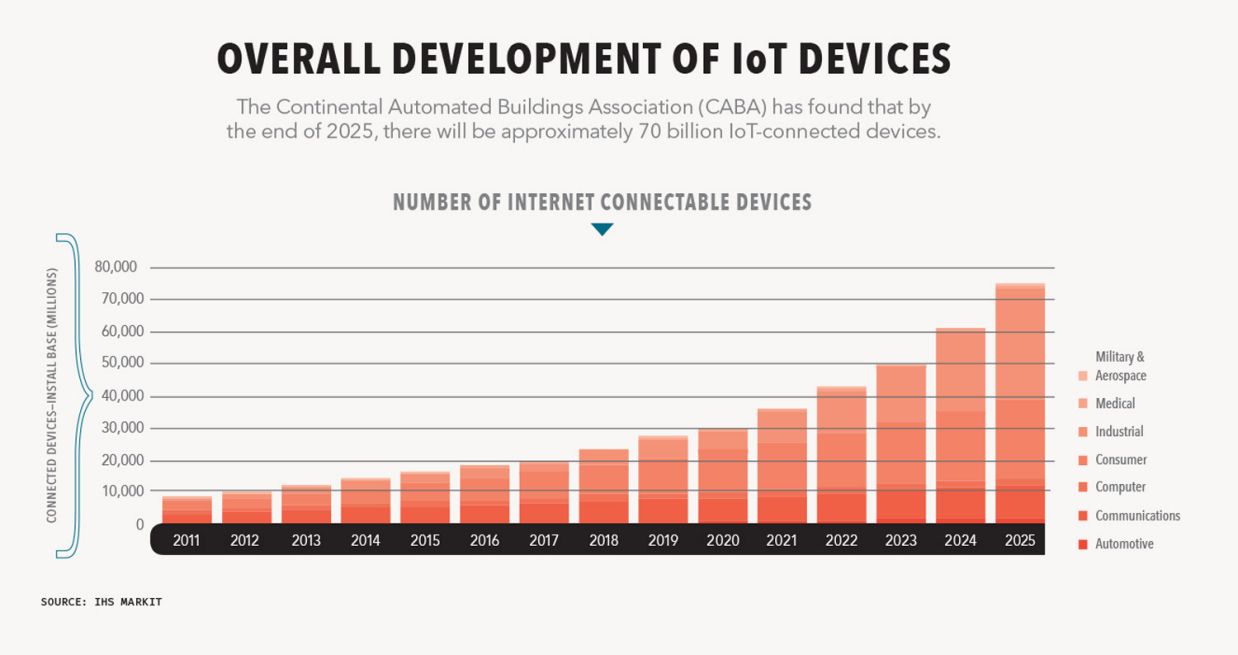
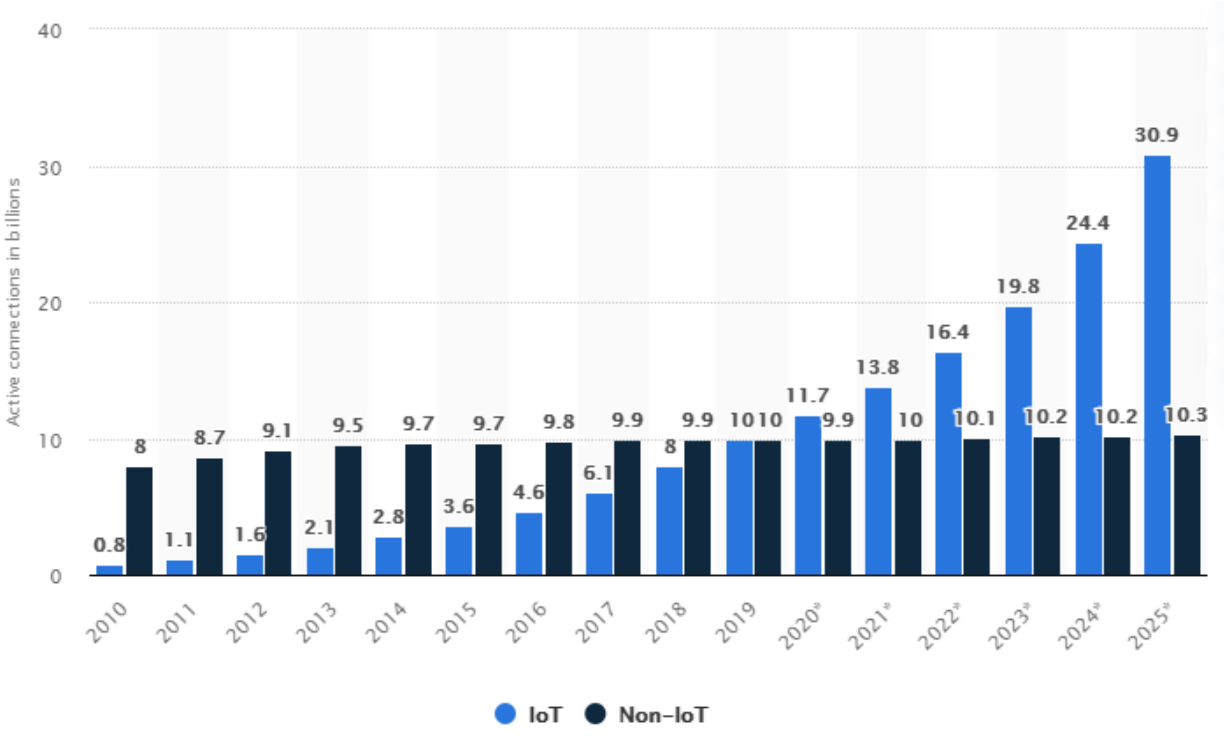


Figure 1.1 The roadmap of the Internet of Things from 2000 onwards [1].



(a)



(b)

Figure 1.2 Predictions for overall connected devices by 2025: (a) Source: CABA [18], (b) Source: Statista [19].

1.2. IoT emerging applications and requirements

Given the recent advances in ubiquitous computing, there are currently many diverse IoT applications for many different environments expected to enhance and improve the quality of everyday life for the end-user community. Major application domains include but are not limited to smart homes, smart cities, intelligent transportation systems, industrial and smart health care [20]. Those various applications have different characteristics and requirements in terms of latency and data rate. It can also be broadly divided into two main categories: consumer IoT (cIoT) and industrial IoT (iIoT) [21]. Consumer IoT aims at improving quality of life of consumers by saving time and money. It also involves the interconnection of consumer electronic devices along with other technology belonging to user environments such as homes, offices, and cities. Conversely, industrial IoT focuses on the integration between Operational Technology (OT) and Information Technology (IT) [22] and on how smart machines, networked sensors, and data analytics can improve business-to-business services. It generally implies machine-to-machine interactions, either for application monitoring (e.g., process monitoring in chemical production plants, vehicle fleet tracking, among others), or as part of a self-organized system, with a distributed control which does not require human intervention (i.e., autonomic industrial plants) [23].

The two service domains share some general communication requirements, such as scalability, the need for lean protocol stack implementations in constrained devices, and friendliness to the IP ecosystem. Nonetheless, the specific communication requirements of iIoT and cIoT can be very different in terms of reliability, QoS (latency, throughput, etc.), and privacy. In cIoT, communications are typically machine-to-user and usually in the form of client-server interactions. Desirable features of IoT are low power consumption, ease of installation, integration, and maintenance. For instance, the advent of fitness and health tracking systems, smartwatches,

and sensor-rich smartphones require a high power efficiency to enable long-term monitoring by small, portable devices as part of a "smart" environment or integrated into our daily wearings [24].

Energy efficiency is perhaps the most crucial aspect of IoT, in particular, because most IoT devices are battery-powered and are expected to be operational for a very long period without human intervention. The time interval between changing batteries for such a smart connected device is a significant cost factor to be considered. Previous research has shown that most energy expended in IoT devices is due to communication [25]. Therefore, energy efficiency has to be considered in the design of both hardware and software. There are several medium access control (MAC) protocols that support duty cycling, allowing the radio to be put to sleep (i.e., low power mode) for periods when it is not expecting to receive data, therefore extending battery life. Energy management techniques also play an essential role in low power operation through lightweight protocols and scheduling optimization, for instance [26] and energy harvesting, where IoT devices can harvest ambient energy from various sources. Moreover, this would also allow the connectivity of new smart device applications that are not currently deployed. A minimum of a ten-year battery life span of operation will be achieved for the daily connectivity of these devices.

1.3. Wireless connectivity landscape for IoT devices

The IoT landscape includes the diverse availability of connectivity solutions as shown in Fig. 1.3. Although there is still no unified solution for IoT at this point, several different communication technologies have been proposed and are currently in operation, having been deployed in a number of devices worldwide. Both long-range and short-range communication standards will be utilized for most connections to achieve both Massive IoT and Critical IoT connectivity through either traditional cellular IoT or Low Power Wide Area Networks (LPWAN).

Common communication technologies use for different application domains include:

- Personal Area Networks → Bluetooth Low Energy
- Home Automation Systems → ZigBee
- iIoT – LoRa, WirelessHART
- Broader coverage → Low Power Wi-Fi, Low Power Wide Area Networks (LPWA), Cellular communications (such as 3GPP - 4G machine-type communications, MTC).

LPWA technologies are designed for IoT applications because of their unique features like wide-area coverage, high energy efficiency, channel bandwidth, data rate, and low power consumption [20]. This technology represents the various technologies currently being used in connecting both sensors and controllers to the internet without the intervention of existing traditional Wi-Fi or cellular networks. Among these promising technologies are SigFox, Ingenu RPMA, and LoRa. Current future demand for internet connectivity of "Things" has motivated the cellular technology to introduce their own IoT devices connectivity landscape solutions such as LTE Cat-M1 (also known as eMTC), EC-GSM-IoT, and NB-IoT (also called LTE Cat-NB1) that will enhance and enable future IoT use cases. LPWA networks are currently being deployed for IoT applications, including smart cities, building management systems, asset monitoring, smart agriculture, etc.

Legacy short-range wireless network technologies are currently being used to support short-range M2M communication applications, including Bluetooth, ZigBee, and low-power Wi-Fi. These technologies are a viable and best fit for consumer use cases of the IoT. Still, they may not support civic, industrial, and other related IoT applications for which the demands are beyond the capacity of their characteristic features.

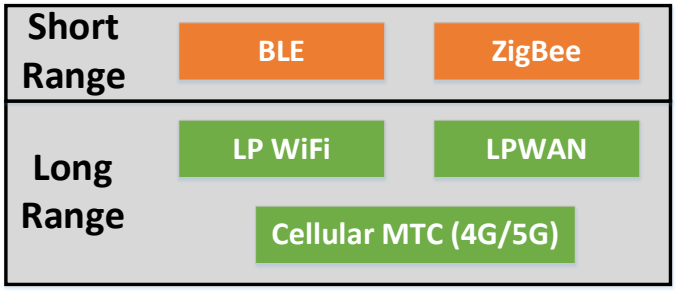


Figure 1.3 IoT connectivity landscape.

1.4. Bluetooth Low Energy (BLE) Standard Overview

Bluetooth was designed based on the IEEE's 802.15.1 wireless personal area communication standard [27] to be used for short-range (up to 50m) ad-hoc communication between devices with achievable data rates in the low Mbps. Bluetooth Low Energy (BLE) was introduced to improve energy consumption suitable for low-power, control, and monitoring applications (e.g., automotive, entertainment, home automation, etc.). BLE operates in the 2.4 GHz ISM band and defines 40 channels with 2MHz channel spacing. The modulation scheme used is Gaussian Frequency Shift Key (GFSK) modulation. To the final aim of achieving low power usage, BLE uses (and thus, scans) only three advertising channels, which are used for device discovery, connection set up, and broadcast transmission. The other 37 data channels are dedicated to the bidirectional exchange of short bursts of data between connected devices. BLE also sets up connections very quickly, which further minimizes the radios on-time. BLE uses an adaptive frequency hopping algorithm on top of the data channels where the signal switches carriers over a predetermined pattern of channels to make it more robust to interference and multi-path fading [28].

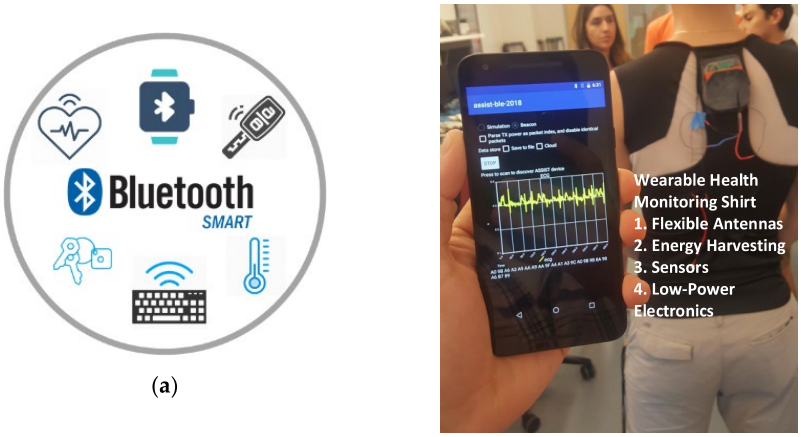
However, one of the drawbacks is the restriction of only one-to-one communication between only two devices at a time. BLE currently only supports a single-hop topology, namely piconet, with one master device communicating with several slave nodes and a broadcast group topology, with an advertiser node broadcasting to several scanners. The Bluetooth Special Interest Group proposed the Bluetooth Smart Mesh working group to define and standardize a new architecture for mesh networking for BLE. This will enable extended communication range and simplify deployments of BLE networks for IoT. BLE is envisaged as a connectivity solution for short-range communication in IoT applications, including smart energy, healthcare, and smart home applications [29].

1.5. Battery-powered IoT devices limitations

The power consumption of IoT devices is widely recognized as the limiting factor to scaling the number of battery-powered IoT devices [30]. Assuming a scenario where a billion devices are deployed with an expected battery life of one year, this would result in replacing 2.7 million batteries each day. In reality, this unacceptable number imposes significant logistical burdens in operational deployments and reduces the utility of IoT devices in different sectors. In addition, batteries represent a logistically prohibitive maintenance problem that requires a large maintenance workforce, presenting a daunting challenge for individual facilities where maintenance resources are already at capacity. Therefore, the battery needs to last as long as the product's life, which can be on the order of 10 years for an embedded device performing signal processing and wireless communication [31].

Unfortunately, current battery lifetimes of BLE sensors are typically <1 year, far short of the 10-year target for other IoT protocols such as cellular narrowband IoT (NB-IoT) and LoRa

devices. However, reducing the power consumption and the operating supply voltages enable the design of self-powered IoT devices in which energy harvesting technologies can be used to power the node from the environment [32]. One growing application in this field is body-powered wearable devices in mobile health technologies that allow remote and continuous health monitoring, as shown in Fig. 1.4 (b) [33]. Another application in the industrial sector is in machine health monitoring (MHM), where self-powered ULP sensors can be deployed to observe specific abnormal patterns in the monitored physical/mechanical signals of a machine for early failure detection. Low-power operation facilitates harvesting of the machine's vibrational energy using piezoelectric materials to charge super-capacitors used to power the sensor [34].



(a)

Figure 1.4 (a) Wide range of consumer IoT applications, (b) self-powered wireless sensor systems used for health monitoring purposes.

Typically, the RF radio accounts for a significant portion of the aggregate power profile of the device. Thus, each data transmission operation performed by a battery-powered node shortens its subsequent lifetime, limiting the amount of data transmittable before needing to recharge/replace the battery. In a typical IoT application, it is reasonable to assume the radio consumes 60–90% of the operating power budget [35]. The active power for a single BLE packet

transmission is usually several mWs, in addition to the startup energy of the frequency synthesizer and the crystal oscillator [35]. To extend the battery's lifetime, aggressive duty-cycling can be implemented [31]. This technique leads to a significant increase in the operational lifetime for battery-powered devices. Using the advertising interval (TI) defined as the time between two successive transmission events, the intended battery lifetime can be estimated (preferably >10 years). A good example application is a tracking device that establishes a Bluetooth connection to a smartphone. Using a common CR2031 coin battery with an energy density of 653 mWh, the required average power consumption for a 20-year lifetime is 3.7 μW. The TI can be calculated as shown in Fig. 1.5. For a more accurate estimation, several additional factors need to be considered, including: (1) the battery self-discharge rate (usually <20 years), (2) the battery capacity degradation by temperature variations, and (3) the startup/shutdown overhead energy which might add extra ~50% to the power budget. All the aforementioned factors will limit the device from achieving the desired lifetime values.

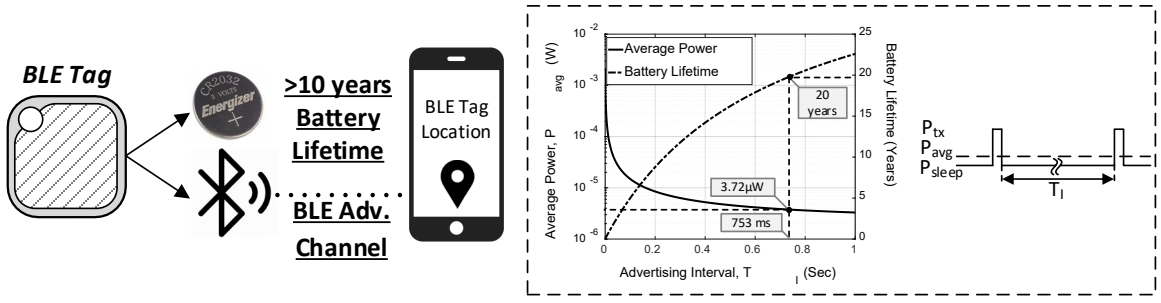


Figure 1.5 A typical IoT BLE application (left), the tradeoff between the required average power consumption and battery lifetime in duty-cycled transmission targeting a specific latency (right).

1.6. Wireless charging for IoT devices

As a fast developing technique, wireless power transmission (WPT) incredibly performs cordless energy migration [37, 38]. This seemingly incredible way can change our traditional

energy utilization patterns in different applications, such as low-power wide-area networks, portable electronic devices, implanted medical devices, integrated circuits, solar-powered satellites, electric vehicles (EVs), unmanned aerial vehicles (UAVs), etc. Through its remarkable characteristics of flexibility, position-free, and mobility, the WPT technique has been taken as an ideal technical solution in the near future, especially for smart home applications, to energize electrical-driven devices within certain specific regions. According to a study by ABI research, despite the economic restraints of COVID-19, the consumer spending on home automation is expected to reach $317 billion by 2026 [39]. ABI research also found that the next generation of smart home customers is looking for low-cost and flexible devices that are easy to set up. Therefore, manufacturers that plan to grow their market share in this emerging space should make their devices convenient to use, with wireless charging for smart homes.

Mostly, IoT devices are powered by batteries. Two basic battery-powered device issues limit their popularization: short battery life and high initial cost. A major limitation of devices powered by battery is finite battery capacity dominated by the power consumption of radios. As IoT devices communicate with each other, a large amount of energy is consumed due to which devices operate for a limited duration only as long as the battery lasts [40]. To prolong the battery life of an IoT device, potential tradeoffs would be low data rate and high latency which lower power by essentially leaving the radio off for more of the time. Furthermore, when the device battery is exhausted, the network may be interrupted. Thus, the lifespan of an IoT device is crucial to the success of an application.

One of the solutions to this problem is to use replaceable batteries. This solution of replacing the battery may be effective for small IoT systems. Still, for large IoT systems, this solution is not practical because the cost of maintaining and replacing billions of batteries is very

high. Therefore, effective charging strategies are needed. Different core wireless charging technologies have been developed and classified into: inductive coupling, magnetic resonant coupling, and energy harvesting of electromagnetic (EM) radiation [41] as shown in Fig. 1.6. Wireless power transfer via an electromagnetic (EM) wave has gained attention thanks to its capability of far-field power transmission [42]. Inductive coupling provides highly efficient charging for a single target at a very close range. It is often applied when charging mobile phones, electric toothbrushes, and other devices.

On the other hand, magnetic resonant coupling provides high-efficiency charging for devices at a distance, making it suitable for wireless sensing networks, mobile devices, and electric vehicles. However, it is susceptible to coupling factor variation. Unlike magnetic wireless power transfer techniques such as inductive coupling and magnetic resonant coupling, the radio frequency (RF) energy harvesting technique uses a radiative EM wave to convey power through free space. Therefore, the RF energy transfer enjoys a relatively longer energy transfer distance compared to magnetic wireless power transfer [43]. However, the wireless power transfer via an EM wave suffers from low end-to-end transfer efficiency because of severe power attenuation. But it can still be used in wireless sensing networks owing to the small size of the receiving power device.

Figure 1.6 (a) near-field versus (b) far-field wireless charging technologies.

Therefore, to achieve energy-efficient operation in wireless sensor networks and maintain network communication, efforts in reducing the energy consumption of the IoT device shall be combined with the efforts to improve the range and efficiency of wireless charging.

1.7. Dissertation Contribution and Organization

The main objective of this thesis is to develop a complete solution to achieve energy-efficient networks for IoT applications. The thesis is divided into two main parts: 1) design of low power BLE radios for energy-efficient wireless connectivity solutions, and 2) design of robust and high efficiency wireless power transfer and wide-bandwidth energy harvesting circuits for energy-efficient wireless charging solutions. The main contributions of this thesis can be summarized as:

1. A novel coherent-based ultra-low power GFSK demodulation architecture is designed and tested for BLE receivers that allows eliminating power-hungry PLLs and utilizing open-loop reception schemes. The demodulator deals independently with the I and Q waveforms in time-domain for proper symbol detection.
2. Antenna-chip co-design approach is introduced for quadrature generation in the RF path with only 3dB NF penalty using lossless power dividers; significantly reducing the power consumption of BLE receivers.
3. A BLE TX with few μWs average power consumption is achieved through duty cycling thanks to the fast-startup time and low startup energy on-chip crystal oscillator; achieving vigilant health wearables with self-powered operation.
4. A cell-based design approach for a digital BLE TX architecture is presented and implemented for the first time in FinFET technology; leveraging the automatic place-and-route capabilities of the FASoC framework.

5. Self-adaptive nonlinear resonant circuits represented by Duffing equations have been proposed to achieve robust wireless power transfer and wideband energy-harvesting circuits with zero overhead power consumption and control/feedback circuitry. This technique is generic and can be applied for wide range of power levels and frequencies.

An overview of the topics discussed in this thesis is portrayed in Fig.1.7. To accomplish the stated goal, different system architectures and circuit techniques have been proposed, designed, fabricated and measured to prove the concept as summarized in Fig 1.7.

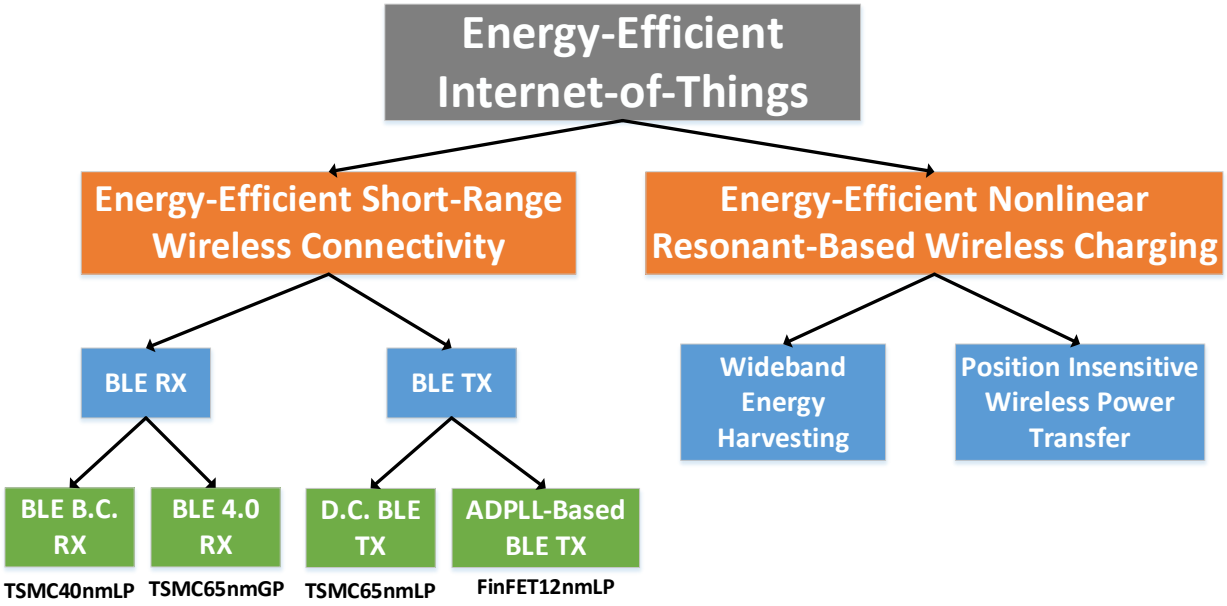


Figure 1.7 Overview of the Dissertation Topics

The rest of the thesis is organized as follows:

Chapter 2 discusses the different strategies that have been proposed to tackle the limited capacity of battery-powered IoT devices both in physical and network layers. The ultimate goal is to lower the power consumption of radios without sacrificing other important metrics like latency, transmission range and robust operation under the presence of interference. Joint efforts in

designing energy-efficient wireless protocols and low-power radio architectures result in achieving sub-100 μW operation. One technique to lower power is back-channel (BC) communication which allows ultra-low power receivers to communicate efficiently with commonly used wireless standards like BLE while utilizing the al-ready-deployed infrastructure. In this chapter, a review of BLE back-channel communication and its forms is introduced. Additionally, a comprehensive survey of ULP radio design trends and techniques in both Bluetooth transmitters and receivers is presented [44].

Chapter 3 presents a 300μW backchannel receiver (RX) compatible with the Bluetooth-Low-Energy (BLE) standard for ultra-low power Internet-of-Things (IoT) applications. A PLL-less, mixer-first zero-IF architecture is proposed to achieve the low power operation featuring an antenna-chip co-design for lossless quadrature (I/Q) generation in the RF path. A novel 10μW switched-capacitor differentiator-based GFSK demodulator is presented. The demodulator exhibits a robust operation under I/Q phase and amplitude imbalances and operates at a 1MHz baseband clock frequency. The proposed backchannel communication within the packet's payload is achieved through 2× data repetition. The chip is designed and fabricated in CMOS 40nm technology. The RX achieves -69dBm sensitivity for 0.1% bit error rate (BER) at 0.5Mbps effective data rate [45].

Chapter 4 present fully-integrated Bluetooth Low-Energy (BLE) transmitter (TX) for Internet-of-Things (IoT) applications. The BLE TX achieves a total energy per bit of 3.5nJ in an open-loop transmission scheme due to the ultra-low startup energy of the system. The overall system architecture of the BLE TX includes an RF front-end, a 16 MHz crystal oscillator (XO), a GFSK modulator, and a digital baseband including a SPI interface. An enhanced capacitively loaded three-stage inverter chain XO is proposed, featuring a 10.2nJ startup-energy, a 150μs

startup time, and a 70μW steady-state power. The steady-state frequency inaccuracy of the XO is 14 ppm with less than 26ps cycle-to-cycle jitter. The BLE TX is fabricated in 65nm CMOS technology and it consumes an average power of 2.17mW to transmit an advertisement packet consisting of 368 bits entirely over 600μs including the startup time. Duty-cycling operation is implemented through power gating achieving an average power consumption of 3.72μW (1.86× sleep power) when transmitting a BLE advertising message every 753ms. In our target application, by using these techniques, we are able to extend a common coin battery's lifetime to more than 20 years [46].

Chapter 5 presents a cell-based digital architecture BLE TX in FinFET GF12nm technology. The FASoC tool has been exploited to automate the design of the ADPLL and perform top level integration. A custom-designed switched-capacitor power amplifier (SCPA) has been designed and used as an auxiliary cell at the top level. The SCPA achieve a desired output power by tuning both the supply voltage and the digital control work to optimize the efficiency. The main challenge in this technology node is the passives' limited quality factor which requires additional consideration when designing the capacitor banks and the on-chip output matching network for the SCPA. The SCPA satisifies class2 BLE power with maximum power of 4dBm with efficiency of 18%.

Chapter 6 discusses the design of robust WPT systems which is challenging due to its position-dependent power transfer efficiency (PTE). In this chapter, a new approach is presented to address WPT's strong sensitivity to the coupling factor variation between the transmit and receive coils. The introduced technique is generic and relies on harnessing the unique properties of a specific class of nonlinear resonant circuits to design position-insensitive WPT systems that maintain a high PTE over large transmission distances and misalignments without tuning the

source's operating frequency or employing tunable matching networks, as well as any active feedback/control circuitry. A nonlinear-resonant-based WPT circuit capable of transmitting 60 W at 2.25 MHz is designed and fabricated. The circuit maintains a high PTE of 86% over a transmission distance variation of 20 cm. Furthermore, transmit power and PTE are maintained over a large lateral misalignment up to ±50% of the coil diameter, and angular misalignment up to ±75°. The new design approach enhances the performance of WPT systems by significantly extending the range of coupling factors over which both load power and high PTE are maintained [47-50].

Chapter 7 concludes the contributions of the thesis and the future work is listed.

Chapter 2

Bluetooth Communication Leveraging Ultra-Low Power Radio Design

2.1 Introduction

Bluetooth Low-Energy (BLE) is the leading protocol for short-range, low power wireless communication networks [51]. Wireless short-range technologies like BLE support tens of meters of maximum distance between devices for a variety of applications including wireless sensor networks and the majority of the low-power devices used in the Internet of Things (IoT). The BLE standard has a competitive advantage over other IoT-compatible wireless technologies because of its ability to communicate directly with smart phones, computers and tablets. Since consumer electronics are ubiquitous, BLE-enabled IoT devices can be seamlessly connected to personal area networks without the need for additional wireless access points. The use cases for BLE have proven to be valuable in different IoT applications including medical health monitoring, automated emergency calls, smart tags, home automation and in-vehicle networks. For environ-mental and industrial monitoring systems, BLE beacon tags can also be used for indoor localization [52, 53], identification and tracking of objects and personnel.

This chapter presents a review of recent efforts devoted to realizing low power connectivity solutions for wireless sensor nodes in BLE networks. The proposed solutions can be classified into two main categories: low-power radio design (physical layer) and energy-efficient wireless access technologies (network layer). Ultimately, combining the efforts in both areas will result in a new

generation of IoT devices that are mobile and self-powered to help propel IoT applications to new paradigms.

The rest of the chapter is organized as follows: in Section 2, we discuss different synchronization schemes adopted in IoT applications with the main focus on BLE networks. Then, we present the concept of asymmetric BLE communication, referred to as back-channel communication. A design example of a BC receiver is also described, demonstrating one possible implementation of the BC communication in BLE-based networks. Section 3 reviews the ULP radio design challenges and trade-offs in both receivers and transmitters. A summary of the state-of-the-art fully compliant and back-channel BLE radios is reported, emphasizing the trade-off between the power consumption and other performance metrics. Finally, conclusions and future directions are presented in Section 4.

2.2 Back-Channel Communication for Energy-Efficient Operation

2.2.1 Synchronization Schemes

The core operation of a wireless sensor node is to sense different physical phenomena from the ambient environment and share the information securely with other nodes within the network. Therefore, the IoT connectivity landscape is structured in the form of hierarchical layers of networking [61]. Local area networks are utilized to facilitate interaction between different nodes in the form of machine-to-machine (M2M) communication as well as establishing connection with the hub or the access point. Eventually, the access point (AP) sends the aggregated information from the endpoint nodes to the backend analytic engines to handle the event through means of wide area networks, mainly the internet. Based on the targeted application, the wireless connectivity capabilities of each sensor node is determined whether to stay online for continuous

data exchange or in a “bursty” nature at scheduled/specific events. Many key performance factors regulate the design of the network like the latency budget, power consumption budget and capacity of the network. For short-range networks, usually a star topology is prevalent as seen with Bluetooth and body area networks. In a star topology, a set of endpoints are allowed to communicate only with a single controller (base station/access point), for example a smart phone.

Reliable network synchronization is needed for wireless sensor networks. It is a prerequisite to establish node-to-node and node-to-AP communication and is commonly performed in a controller-agent manner. However, the synchronization process might dominate power consumption when designing low-power radios for IoT. Two major application-specific synchronization schemes are proposed, resulting in different complexity and power budget requirements as summarized in Fig. 2.1 [62]. In the first scheme, both the node and the AP radios keep transmitting the synchronization sequences (beacons) periodically. This approach offers the shortest network latency at the cost of increased power consumption due to the always-on radios. To achieve energy-efficient operation at the battery-powered node, the radio is placed in a “sleep mode” to preserve the battery’s lifetime. A separate ULP wake-up receiver (WuRx) can be designed to off-load the synchronization task from the main radio. The WuRx continuously searches for a pre-defined wakeup signal or the standard beacon from the AP. Once received, the WuRx will wake-up the main radio to perform on-demand high data-rate communication. Alternatively, in the asynchronous scheme, the node’s radio is woken up only when needed asynchronously. The AP repeats transmitting the synchronization sequences until it acquires the node.

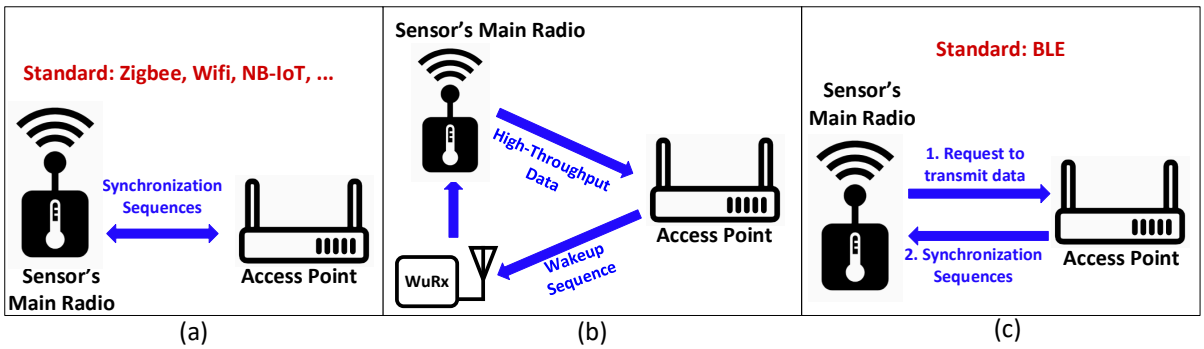


Figure 2.1 Different synchronization schemes resulting in different complexity and power budget requirements: (a) synchronous; (b) wake-up receivers; (c) asynchronous.

The WuRx receiver is an attractive solution to minimize the power consumption of the nodes while not compromising latency or scalability. The average power effectively becomes the active power of the always-on WuRx in addition to the leakage power of the main radio in a deep sleep mode. Since the WuRx and the main radio share the same communication link budget with the AP, both radios need to have similar sensitivity levels in order not to jeopardize the performance of the main radio. The reliability of the WuRx to properly detect the wakeup signaling in the presence of interference in congested bands is also of concern to minimize false alarms. Lastly, it is preferable for the WuRx signal sequence to be compatible with the communication protocol utilized in the network between the main radio and the AP to avoid additional hardware and cost at the AP side.

2.2.2 Back-Channel Communication Concept

Much research has been devoted to realizing energy-efficient wireless connectivity considering both the radio architectures and networking topologies. The motivation is to realize lasting operation for both battery-powered and battery-less wireless sensor nodes. According to

the ULP radio survey [63], low power operation can be achieved when using simpler modulation techniques like on-off keying (OOK) or frequency-shift keying (FSK) at low data rates. Low complexity modulation schemes eliminate the requirement for having high-accuracy frequency synthesizers (PLL) which typically consume more than 50% of the radio power consumption. Moreover, lower data rates result in a lower SNR requirement and higher sensitivity level which can be achieved with basic radio ar-chitectures utilizing passive RF frontends [62]. The majority of previous work in this area utilizes simpler receiver architectures that rely on energy-detection and can achieve sub-10 μW active power consumption. However, it is difficult for these receivers to operate reliably in the presence of interference. Another challenge is that most of the wireless standards commonly used in IoT connectivity do not support such modulation techniques and data rates. For instance, the BLE standard utilizes GFSK modulation with data rates of 1 or 2 Mbps. Although BLE signals are widely used in developed high population density areas, most ULP devices cannot take advantage of BLE connectivity because of their extremely limited power and/or complexity budget. State-of-the-art BLE radios still consume several mWs of active power. One reason behind the high power operation is the interference mitigation techniques to robustly achieve the highest possible sensitivity and adjacent channel rejection (ACR) performance. Efficient techniques such as asymmetric BLE communications, duty-cycling, wakeup techniques, ring-oscillator-based local oscillator (LO) generation and open loop GFSK modulation have been reported to reduce the power consumption of the radio [44]. Although heavy duty-cycling brings the average power down to sub-100 μW, it comes at the expense of long latency.

In this section, we will focus on BLE with back-channel communication. Prior work [4,14–16] have reported the idea of back-channel communication, where signals are embedded in standard compliant wireless packets and generated by a standard-compliant transmitter. The basic

idea is to design ULP radios that are compatible but not ful-ly-complaint with the BLE standard to encode information in an auxiliary low-complexity and low data rate modality as depicted in Fig. 2.2. Two classes of IoT devices are considered: BLE-enabled (e.g., smart watch) devices where the power consumption is in the range of mW and ULP IoT devices (e.g., temperature sensors) with limited power consumptions of tens of μW. In such scenarios, commercial smart phones can be easily configured to transmit BLE back-channel messages in addition to the fully compliant BLE packets based on the targeted device. In back-channel communication, some BLE standard requirements like data rate can be traded off with power consumption while being able to still communicate properly with already deployed hardware infrastructures. Thus, the major advantage of this technique is that it leverages widespread smart phones to send back-channel signals which can be utilized in different applications scenarios. BLE back-channel communication can be seen as a wakeup mechanism that bridges the gap between ULP and standard compliant BLE radios. The BLE receiver stays in sleep mode until it is woken up through an always-on ULP WuRx listening to the back-channel to realize the concept of BLE on-demand. This approach significantly decreases the active power consumption of the receivers without sacrificing the latency in the network.

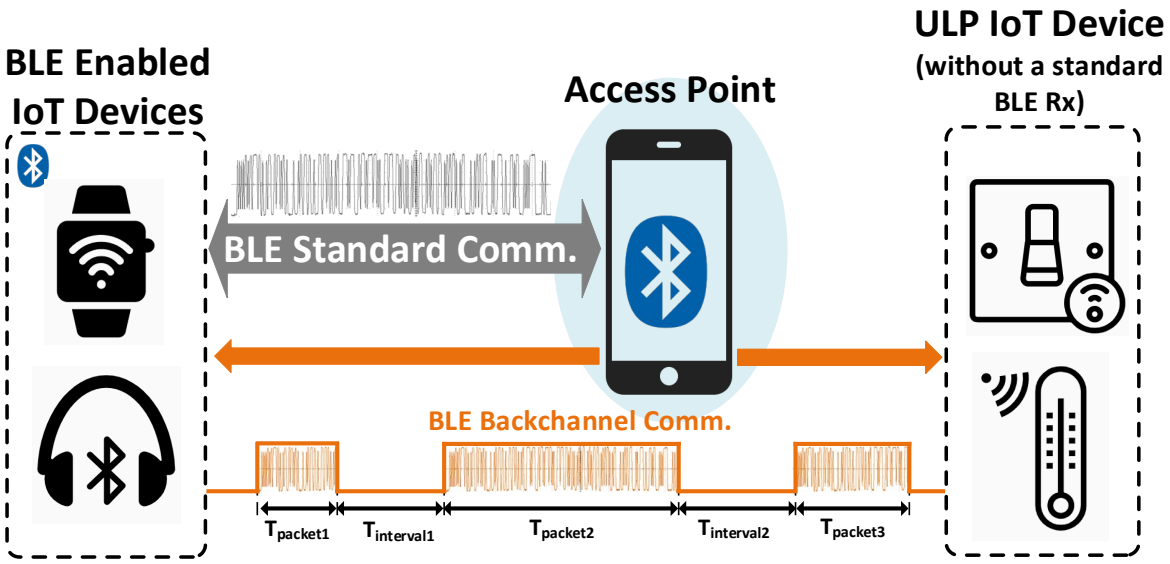


Figure 2.2 Concept of BLE (Bluetooth Low-Energy)-based back-channel communication.

One of the greatest challenges in designing an IoT platform is dealing with the heterogeneity of devices [54, 64]. The proposed back-channel communication technology breaks this barrier to allow heterogeneous ULP IoT devices to interoperate with already existing BLE infrastructure with minimal power consumption [62]. The concept of embedded back-channel communication enables a variety of new applications with inter-connecting heterogeneous devices. For example, the proposed scheme allows ULP devices in deep-sleep states that are not BLE compliant to wake up by back-channel communication embedded in standard BLE compliant packets.

Back-channel modulation is an entirely software-defined process which is accomplished by the MAC layer. It can be realized within a packet by generating a specific sequence of bits in the payload [54] or applying duty cycling at the bit-level [67, 68]. In addition, back-channel communication can be implemented on a packet-level by generating a proper sequence of packets [62, 66]. Prior works [69, 70] demonstrated the back-channel communication concept in the form of packet length modulation or packet interval modulation using multiple consecutive BLE packets

as shown in Fig. 2.2. The packet length or interval modulation utilizes an entire packet (or multiple packets) as an on-off-keying information symbol for an energy-detector based receiver. Its bandwidth efficiency, however, is very poor since the signaling requires many consecutive packets. Moreover, this form of back-channel signaling is particularly vulnerable to interferences as the packet length modulation is susceptible to an interferer packet (or any other high power interference signal) that could appear between multiple back-channel signaling packets. The other related technique is hierarchical modulation. In hierarchical modulation, receivers can selectively demodulate high rate (e.g., 16QAM) or low rate (e.g., 4QAM) information from a single packet depending on the channel quality. However, this hierarchical modulation scheme does not allow communication among heterogeneous devices using very distinct modulation schemes (e.g., coherent vs. non-coherent). Other work demonstrated intra-packet back-channel modulation schemes and the feasibility of the embedded back-channel signal generation without modifying the existing packet structure. Embedded back-channel signals are all generated by a set of carefully crafted bit sequences within the boundary of the standard-compliant packet structure. More specifically, binary FSK modulated back-channel communication embedded in GFSK BLE packets has been reported. A standard compliant data receiver can demodulate the entire bit sequence including the bits to create a back-channel message. Meanwhile, at the ULP back-channel receiver, only the embedded back-channel message is decodable, not the entire bit sequence. The backchannel signaling must be accomplished within strict constraints of the standard compliant packet structure.

2.2.3 ULP Back-Channel BLE RX Prototype

In order to further clarify the concept of back-channel communication and its implementation in the BLE standard, a BC receiver prototype is presented in this subsection. The receiver consumes 150 μW and is based on a ring oscillator (RO) for LO generation. The RO-based LO is designed to operate at 0.5× the BLE frequency band to reduce the active power consumption [66]. A dual-mixer front-end is hence required to enable the lower frequency for the oscillator. In this receiver, interference rejection is enhanced by (1) using a Zero-IF architecture to eliminate the image problem, (2) utilizing a narrowband low-pass filter at baseband with cutoff frequency of 1 MHz and (3) forming a 2-D back-channel message built on the presence and length of packets in all three advertising channels instead of utilizing a single advertising channel. This improves its resilience to interference. The FSK demodulation is performed by sensing the frequency-hopping sequence on the advertising channels. The frequency-hopping sequence can be defined in any order and still be compliant with the BLE standard. Therefore, this BC receiver can receive a wake-up message from a mobile phone that is sending a BLE compatible message.

A BLE advertising event includes three packets separated by less than 10 ms as shown in Fig. 2.3. Each of these packets can be transmitted on any of the three BLE advertising channels which are numbered: CH37, CH38 and CH39. These channels' frequencies are 2402, 2426 and 2480 MHz, respectively. The packet duration can be anywhere between 128 to 376 μs (Fig. 2.3 shows a 300 μs packet for illustration). The BLE standard specifies the time gap between advertising events to be at least 20 ms, but not more than 10.24 s. On top of this time gap, a pseudo-random delay of up to 10 ms is added to reduce the probability of collisions.

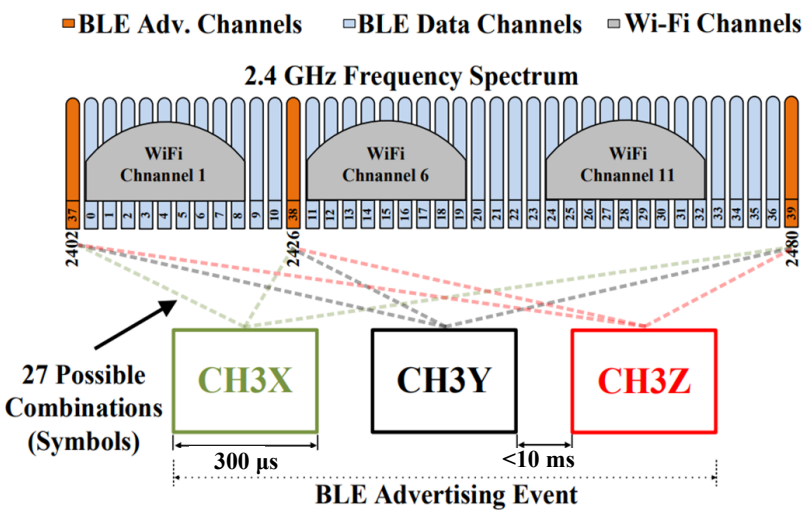


Figure 2.3 Structure of a BLE advertising event.

In the form of back-channel BLE communication used by this receiver, the three BLE advertising channels are scanned for the presence of transmitted energy. This is implemented by scanning the three channels sequentially for energy. To suppress the impact of adjacent channel interference, the bandwidth of the receiver baseband is set to 1 MHz. The receiver's oscillator frequency controller hops the oscillator frequency be-tween all three BLE advertising channels (78 MHz apart).

This BC-BLE receiver was fabricated in a 65 nmLP CMOS process. At a 112.5 kbps data rate, the measured receiver sensitivity was −57.5dBm for a 0.1% bit error rate (BER) requirement. To characterize the interference rejection of the receiver, a GFSK-modulated interferer is utilized in measurements. The signal-to interference ratio (SIR) was measured to be −4, −20 and −30 dB for the 1st, 5th and 10th BLE adjacent channels, respectively which is measured when the received signal amplitude is 3 dB higher the sensitivity level. The entire receiver consumes 150 µW total power from two separate supplies: 0.9 V for digital circuits and 1.1 V for analog blocks. About 120 µW (80%) is consumed by the RO-based LO generation including the LO buffers which

operate at 1.2 GHz, the digital FLL and the LO frequency dividers. The remaining 30 μW is dissipated in the analog baseband.

2.3 BLE Radio Design Trends and Considerations

2.3.1 Receiver Design Trends

In this section, we will present a survey of low power receivers that have been published in top journals and conferences since 2005 [63]. The survey summarizes the state-of-the-art receiver specifications, helps identify the research directions and trends and gives a deep understanding of radio design trade-offs and limitations [71]. Figure 2.4(a) shows the power trend of published receivers over years. It can be seen that the first sub-μW receiver was introduced in 2012 [72] and, since then, a number of sub-μW wakeup receivers have been published for IoT applications.

An important figure of merit (FoM) in receivers design is based on the product of power consumption and the achieved sensitivity. Lower FoM implies an energy-efficient radio design. However, since different radios target different data rate requirements, a normalized sensitivity on data rate is mandatory for a fair comparison and consistent FoM. Figure 2.4(b) shows the well-known tradeoff between sensitivity and active power consumption in radios. With the exception of sub-μW receivers, a Pareto optimal line with a slope of −10×/20 dB can be observed bounding the power-sensitivity design space. The slope indicates that for every 20 dB improvement in sensitivity (or a 10× increase in the transmission range in free-space), you would expect 10× increase in the power. Therefore, in order to achieve a lower power operation, sensitivity shall be sacrificed. Normalizing the sensitivity to data rate for each point, as shown in Fig. 2.4(c), results in a clearer ob-servation for the power-sensitivity trade-off since sub-μW receivers typically operate at fairly low data-rates.

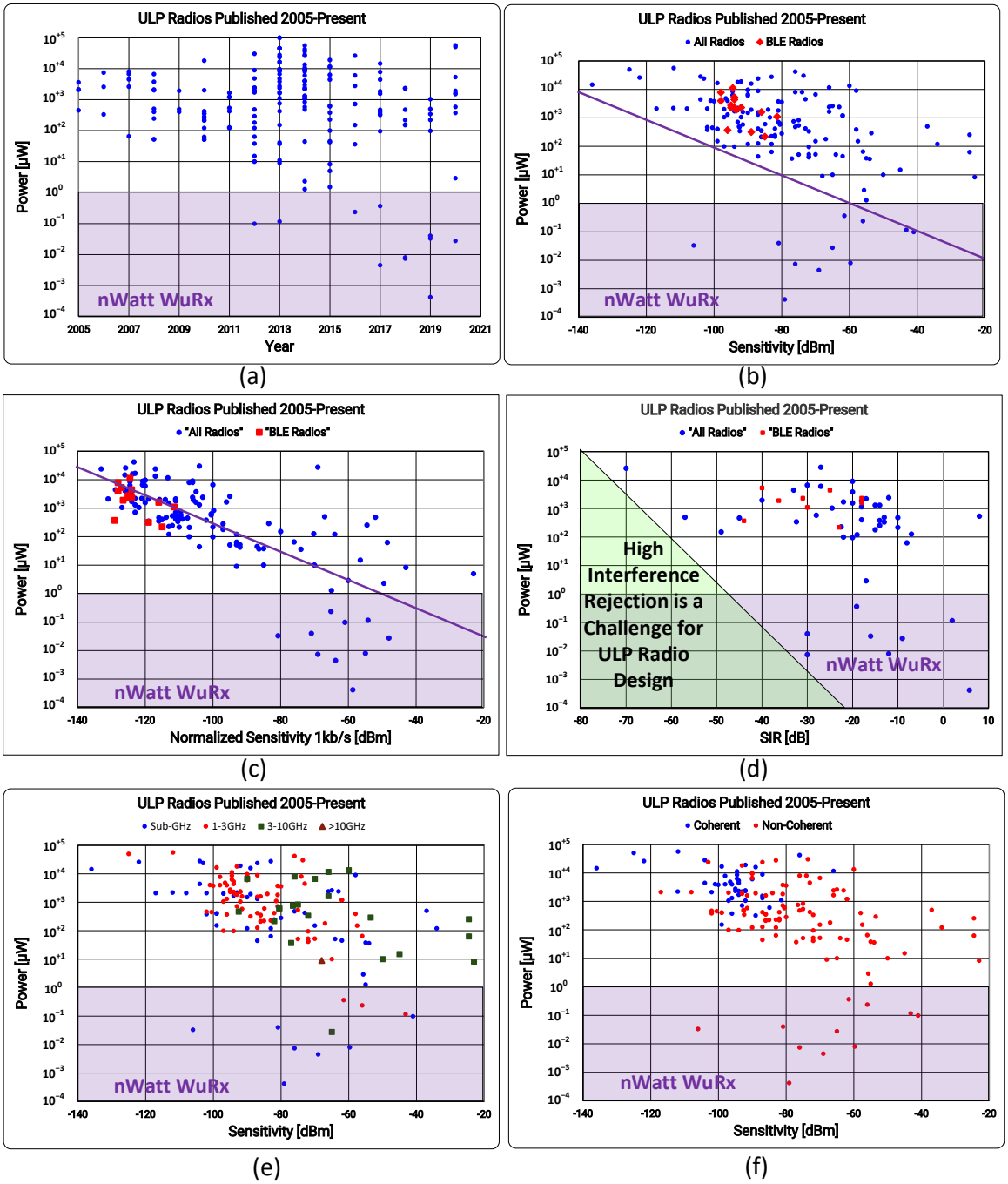


Figure 2.4 ULP (ultra-low power) receivers' survey showing different design trade-offs. (a) Power trend of published receivers over years; (b) power consumption versus sensitivity; (c) power consumption versus normalized sensitivity; (d) power versus signal-to- interference ratio (SIR); (e) power versus sensitivity at different frequency ranges; and (f) power versus sensitivity for different modulation schemes.

The signal-to-interference ratio (SIR) is another performance metric which resembles another challenge to achieve robust operation at a limited power budget. Figure 2.4(d) clearly shows the aforementioned trade-off. Another important observation is that few papers report the SIR performance with a modulated interferer and the majority of these ULP radios have power consumption of 100 s of μWs. The reason is that in order to achieve good rejection at adjacent channels, frequency translation and cascaded signal filter stages are required which translates to higher power consumption. An alternative approach to improve the frequency selectivity of the receiver is based on exploiting high-Q off-chip RF MEMS filters, as in [73, 74]. However, it lowers the system integration level and increases the module's cost. In addition, it requires multiple devices to cover the wide bandwidth required in many standards. Network level solutions such as frequency-hopping can effectively improve interference tolerance as proposed in [66].

The distribution of ULP receivers across different frequency bands is shown in Fig. 2.4(e). As can be seen, sub-10 μW receivers operate at sub-3 GHz frequency range. Lower frequencies provide wider coverage at the expense of data rates which is attractive in numerous IoT applications. Several low power and low voltage techniques can be utilized at low frequencies like subthreshold analog and digital logic to reach <1 μW power budget [70].

Complexity of the modulation is another critical factor which limits the power con-sumption of the receivers [75] as depicted in in Fig. 2.4(f). Coherent modulation schemes (e.g., BPSK, OFDM, QAM) require the phase information of the received signal for proper demodulation and hence high-performance PLLs are used. This results in higher power consumption for demodulation. On the other hand, simple modulation schemes like OOK and FSK are suitable for ultra-low power designs. All sub-μW receivers utilize non-coherent modulation schemes. Additionally, simple modulation combined with low data rate allows the implementation of bit-

level duty-cycling to further reduce the power consumption as reported in [76]. Thus, decent sensitivity levels at low average power consumption can be achieved at the expense of the data rate.

Fully-compliant BLE receivers tend to consume several mWs of power. This is ex-pected due to the stringent requirements on sensitivity at high data rates, adjacent channel interference rejection, GFSK modulation error and center frequency deviation. To achieve these specifications, power-hungry circuit blocks as high-gain LNAs, high-selectivity active filters, high-performance PLLs and accurate and fast-startup ref-erence oscillators are required.

The survey also provides a holistic overview of the common receiver architectures and circuit techniques followed in ULP radio design as summarized in Fig. 2.5. Since the power consumption scales with frequency, RF gain and selectivity consume a large portion of the receiver power profile. Since RF power consumption dominates the power budget, employing passive RF front-ends significantly decreases the overall RX's power consumption. In sub-μW receivers, RF envelope detectors (ED), e.g., diodes, preceded by high-Q transformers are commonly used with moderate sensitivity performance [70]. In such architectures, the interference rejection techniques are mostly focused on continuous wave tones which are not an accurate assumption since wireless communication is packetized, resulting in discontinuous interference. In addition, many modulation for-mats result in amplitude variation making those techniques inefficient in real-world scenarios due to multipath fading. ED-based receivers are adequate mainly at low fre-quency ranges because of their large parasitic capacitors [77].

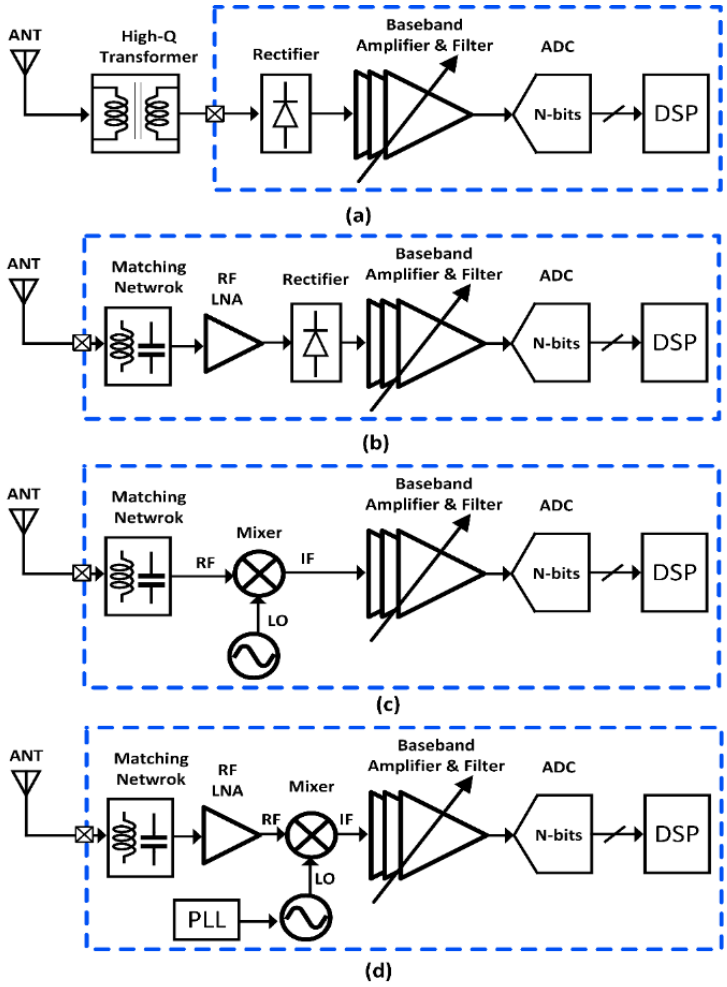


Figure 2.5 Common architectures of low power receivers: (a) energy-detector first; (b) energy-detector + LNA first; (c) mixer-first without PLL; (d) LNA-first architectures.

Mixer-first receivers are another attractive solution to avoid power-hungry active RF gain [78–83]. Passive N-path mixers are utilized as a first stage and are matched to the antenna. However, mixer-first architectures exhibit higher noise figure compared to LNA-first receivers, limiting their sensitivity. Nevertheless, mixer-first architectures can still achieve decent sensitivity levels through passive gain provided by matching networks in sub-mW receivers [84]. In such architectures, the major part of power is consumed by the LO generation and buffers used to drive the mixer switches. Different techniques are proposed to decrease the power of LC-based LO

generation including utilizing high-Q low profile off-chip inductors which can be integrated with the radio in the same package. This solution results in a 75% power saving compared to on-chip LC oscillators at the expense of integration level [85]. Alternatively, ring-oscillators (RO) can be exploited for low-power LO generation especially in advanced CMOS nodes. The main challenge becomes improving the frequency stability and phase noise performance of the RO to avoid the degradation in the sensitivity and/or selectivity of the receiver [66].

Table 2.1 summarizes the trade-off between power and other performance metrics in BLE receivers. The table shows the performance of back-channel BLE receivers in comparison with fully-compliant BLE receivers [86–97]. It can be seen that state-of-the-art fully compliant receivers consume around ~2 mW, while BLE back-channel receivers have power consumption as low as ~200 μW. The receiver data rate, sensitivity at BER of 0.1% and adjacent channel rejection are lower in the case of back-channel BLE receivers which can be acceptable for some targeted applications.

Table 2.1 Comparison table for the state-of-the-art Bluetooth-Low Energy receivers.

	[62] JSSC'21	**[66] JSSC'19**	**[89] RFIC'18**	**[68] CICC'18**	**[96] ISSCC'20**	**[97] ISSCC'20**	**[90] ISSCC'18**
Standard	BLE WuRx	BLE B.C.	BLE B.C.	BLE B.C.	BLE4.0	BLE4.0/5.0	BLE4.0/5.0
Technology	65 nm	40 nm	65 nm	65 nm	40 nm	22 nm	40 nm
Supply Voltage	0.5 V	1.0/0.9 V	1.1/0.9 V	0.75 V	0.9/1.0 V	0.5 V	0.8 V
Modulation	FSK: 3-channel voting + pkt length + pkt interval + RSSI	FSK: 3-channel hopping sequence + BC symbol correlation		GFSK w/ data repetition	GFSK	GFSK	GFSK
Data Rate	N/A	250 kbps	112.5 kbps	333 kbps	1 Mbps	1/2 Mbps	1/2 Mbps
Latency	1 adv. packet ~200 μs	1 adv. event 1.47 ms		1 adv. packet ~200 μs	N/A	N/A	N/A
RX Sensitivity	−85 dBm	−82.2 dBm	−57.5 dBm	−76.6 dBm	−86 dBm	−96.4 dBm	−95 dBm
Power Consumption	220 μW	1200 μW	150 μW	230 μW	2100 μW	1900 μW	3040 μW
SIR [dB] @2MHz	−6 dB	−10 dB	−4 dB	N/A	−18 dB	−36.1 dB	−18 dB
Die Area	2.4 mm^2	1 mm^2	1.1 mm^2	4 mm^2	1.3 mm^2	1.9 mm^2	0.8 mm^2

2.3.2 Transmitter Design Trends

A generic architecture of a BLE transmitter is shown in Fig. 2.6, summarizing the main blocks referred to in this section. The following design trends are observed in recent BLE transmitter publications:

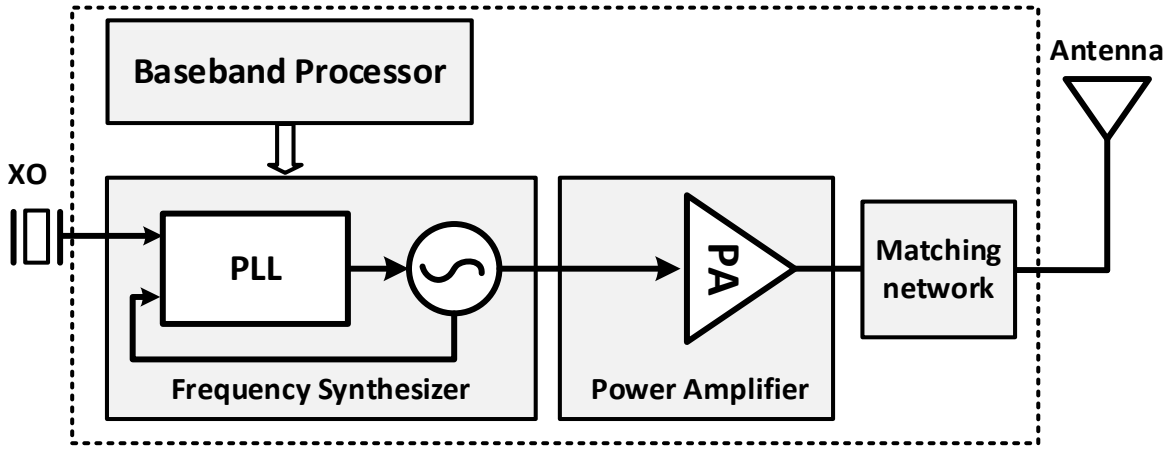


Figure 2.6 Conventional architecture of BLE transmitters.

2.3.2.1 Direct GFSK Modulation for Open-Loop LCVCO

BLE utilizes GFSK as its modulation scheme for data transmission. Traditionally, 2-point injection in the PLL is used to modulate the output frequency while the PLL is locked [60, 87, 98, 99]. The digital baseband of the BLE transmitter generates control signals according to the data packet and injects the corresponding frequency control words to the PLL reference and the VCO at the same time. In this way, by balancing the reference phase and the VCO phase at the same time, the frequency change in the VCO output will not cause a transient signal in the loop for the PLL during transmission. However, this topology requires matched control at both of the injection points, and it is easily affected by the PLL bandwidth, data rate and frequency deviation according to the BLE standards. Recently, it was discovered that typical LC-VCOs can easily satisfy the

phase noise requirement of the BLE standard while running open loop [100]. More and more designs have started to utilize direct frequency modulation on an open-loop VCO [55, 56, 101–103]. This calibration and open loop modulation method has several benefits compared to the traditional modulation method: (1) it simplifies the role of the PLL in the BLE transmitter and reduce its design complexity, (2) it could reduce the average power consumption of the transmitter by duty cycling the PLL and (3) it enables new design methodologies for BLE transmitters such as crystal-less design.

2.3.2.2 Digitization of BLE Transmitters

Another trend of BLE transmitter design is digitization. There are three major building blocks in a BLE transmitter: baseband processor, frequency synthesizer and power amplifier (PA). The baseband processor is a digital block that generates data packets for modulation and transmission. The frequency synthesizer converts the baseband signal into RF frequency at its target channel and applies modulation to the data. In addition, finally, the PA amplifies the signal for transmission. All-digital PLLs have been used more and more in recent designs [87, 101, 102]. Due to CMOS process scaling, digitally controlled capacitor banks can now reach very fine resolution. Thus, the modulation signal, which used to be applied to the varactor in the LC-VCO in the analog charge pump PLL, is now applied to these digitally controlled capacitor banks in the ADPLL [87]. Recently, [104] proposed the first reported ring-oscillator based all-digital BLE transmitter design which has successfully removed the LC-VCO as the last analog circuit block in the frequency synthesizer block. The power amplifier has also gone digital as well. The class-D switched-capacitor digital power amplifier [105] has been adopted more and more in recent publications. Digital architectures benefit more from process scaling and could eventually be

automatically synthesized using digital IC design tools [106]. This will result in significant reduction in production time and overall cost for circuit design.

2.3.2.3 Reduction of On-Chip/Off-Chip Components

In order to reduce the overall cost of the BLE module, a lot of research has been done to reduce the on-chip and off-chip components. In the past decade, a lot of the research focused on reducing the number of passive devices in the matching networks. Ref. [60] proposed a BLE transceiver with embedded RX image-rejection filter and TX harmonic-suppression filter by reusing an on-chip matching network that reduced the number of passive devices. Ref. [103] proposed a BLE transmitter utilizing a co-designed loop antenna and combined enhanced power oscillator which embedded the matching network into the power oscillator while improving both the VCO phase noise and transmitter efficiency. These designs reduced the number of on chip inductors which typically occupy a large portion of the die area. As mentioned above, the all-digital BLE transmitter design proposed in [100, 104] replaced the LC-VCO with an ultra-low power ring oscillator and successfully removed all the inductors from the transmitter, resulting in a 40× core area saving compared to the state-of-the-art.

Recent work focuses on removing the crystal oscillator (XO) in BLE transmitters [107–109]. The XO is one of the most expensive off-chip components in a BLE module. Several XO replacements have been evaluated, such as a real time clock (RTC), FBAR oscillator and recovered RF signal. In [107], the high-frequency XO is replaced with a 32 kHz re-al-time clock (RTC) for frequency calibration and channel selection, while in [108], the XO is replaced with an FBAR resonator. The work in [96, 108] reported an XO-less BLE transmitter with clock recovery from GFSK-modulated BLE packets. These designs show that the BLE transmitter is capable of

working without a typical MHz-range XO and it not only reduces the overall cost of the BLE module but also introduces some new design insights for BLE beacon transmitters.

2.3.2.4 Transmitter-Focused Design Requirement for System Efficiency

The brief survey below summarizes recent design trends in ultra-low power BLE transmitter designs. In order to reduce power consumption as well as the overall cost and improve the system efficiency, a lot of techniques are used for different applications. In order to design the BLE transmitter at its physical limit in terms of power and cost, de-signers have to adjust their design specifications according to application needs. For example, the frequency synthesizer specifications in traditional full function BLE transceivers are set by the receiver adjacent channel rejection requirements which requires exceptional performance of the VCO. However, from the transmitter's point of view, such performance far exceeds its need according to either spectrum emission or frequency modulation requirement [100, 104, 110]. Thus, designing the transmitter frequency synthesizer for a BLE network according to the receiver requirement is wasting power and cost. For power amplifier design in BLE transmitters, it is better to optimize the output power and system efficiency according to application needs as well. For example, if the target communication range is only within 3–4 m, optimizing the PA for its highest efficiency at 10 dBm would not be as efficient as optimizing its highest efficiency at 0 dBm.

Table 2.2 presents a comparison table for state-of-the art BLE transmitters with different architectures. It can be seen that BLE transmitters have an average overall efficiency around 25%. Therefore, in order to achieve longer transmission range, the power consumption is expected to be in mW levels. Aggressive duty-cycling techniques can be implemented for discontinuous transmission events/advertisements to bring the average power consumption to μW levels for ULP applications.

Table 2.2 Comparison table for the state-of-the-art Bluetooth-Low Energy transmitters.

	[109] JSSC'21	**[103] ISSCC'19**	**[56] JSSC'19**	**[103] JSSC'19**	**[91] ISSCC'18**	**[101] JSSC'16**
Technology	40 nm	65 nm	28 nm	40 nm	65 nm	28 nm
Supply Voltage	0.6/1.0 V	1.2 V	0.2 V	0.6/0.9 V	1.0 V	0.5/1.0 V
Transmission Scheme	Closed loop (RO-based)	Open Loop	Closed loop (Type-I)	Closed loop (RO-based)	Closed loop (ADPLL)	Closed loop (PLL)
PLL Locking Time	50 µs	15 µs	N/A	0.4 µs	Not reported	15 µs
Power Consumption	1.1 mW	0.61 mW	4 mW	1.55 mW	3.1 mW	6.3 mW
TX Output Power	Not reported	−8.4 dBm	0 dBm	−3.3 dBm	−3 dBm	3 dBm
Overall efficiency	Not reported	23.6 %	25 %	30.17 %	16.13 %	32 %
Die Area	1.33 mm^2	0.494 mm^2	0.53 mm^2	0.0166 mm^2	1.64 mm^2 *	0.65 mm^2

2.4 Conclusions and Future Work

BLE, as a well-established protocol, is utilized for short-range communications in a wide spectrum of applications, ranging from audio streaming to wireless sensors nodes. It offers a low power solution that can support connectivity between heterogeneous IoT devices and access points in personal area networks. Several efforts have been devoted to reducing the power consumption of the RF radios to empower scaling IoT devices and enable self-powered operation. Efficient and complete solutions can be realized in both the network and physical layers. In the network layer, back-channel communication is presented where the back-channel message is embedded in a standard compliant BLE packets which is an attractive solution to design ULP radios while able to connect with the already-deployed infrastructure. Back-channel communication can be implemented in a packet-level fashion within an advertisement event or within a packet based on the la-tency requirements. This approach allows the main radios to stay in a deep sleep-mode, while the ULP wakeup/BC receivers continuously monitors the spectrum for wakeup/BC signaling from the access points or other fully functioning devices.

We presented a comprehensive survey for fully compliant BLE transceivers as well as back-channel receivers. In receive mode, fully compliant BLE receivers consume mWs of power

to meet the stringent requirements on the data rate, sensitivity level at 0.1% BER and adjacent channel interference rejection. On the other hand, different backchannel receiver architectures were proposed to limit the power consumption to 10 s or 100 s of μWs. Mixer-first architectures, in an open-loop transmission scheme, accompanied with RF passive gain provide a decent performance at low power budget. BLE transmitters utilizing linear/switched power amplifiers suffer from low overall efficiency which led to a power consumption of several mWs to achieve high output power levels. Ring oscillator PLL-based architectures are proven to decrease the power budget to 100 s of μWs while satisfying the BLE requirements in terms of phase noise and frequency stability. Alternatively, open loop transmission utilizing LC-based oscillators can be utilized to eliminate the extra power of PLLs and PAs leading to a significant reduction in power consumption.

Extensive research efforts from industry and academia are still ongoing to create more energy-efficient wireless connectivity and low-power radio design architectures. These efforts extend beyond the BLE standard to cover the entire connectivity landscape of IoT devices.

Chapter 3

A 300μW Bluetooth-Low-Energy Backchannel Receiver Employing a Discrete-Time Differentiator-Based Coherent GFSK Demodulation

3.1 Introduction

Power consumption is widely recognized as the limiting factor of scaling IoT devices. Bluetooth Low-Energy (BLE) is established as the leading standard for short-range, low-power wireless communication. Even so, realized battery lifetimes of BLE sensors is <1 year, far short of the 10-year target for NB-IoT and LoRa devices. Typically, the radio's power consumption dominates the power profile of the sensors. Recent works on fully-compliant BLE receivers (RXs) [111, 112] demonstrate a few milliWatts power consumption. This chapter presents a 300μW backchannel RX compatible with the BLE 4.0/5.0 standard for ultra-low power IoT devices.

In this work, the low power operation is achieved through employing: 1) a PLL-less mixer-first zero-IF architecture; 2) a high-Q, in-package inductor for LO generation; 3) antenna-chip co-design approach for I/Q generation in the RF path; and 4) a novel 10μW coherent GFSK demodulator with high immunity to I/Q amplitude/phase imbalances. The proposed RX demodulates symbols at 1Mbps and uses 2X data repetition in the packet payload to meet the BER requirement (0.1%) at the sensitivity level; demonstrating an effective data rate of 0.5Mbps.

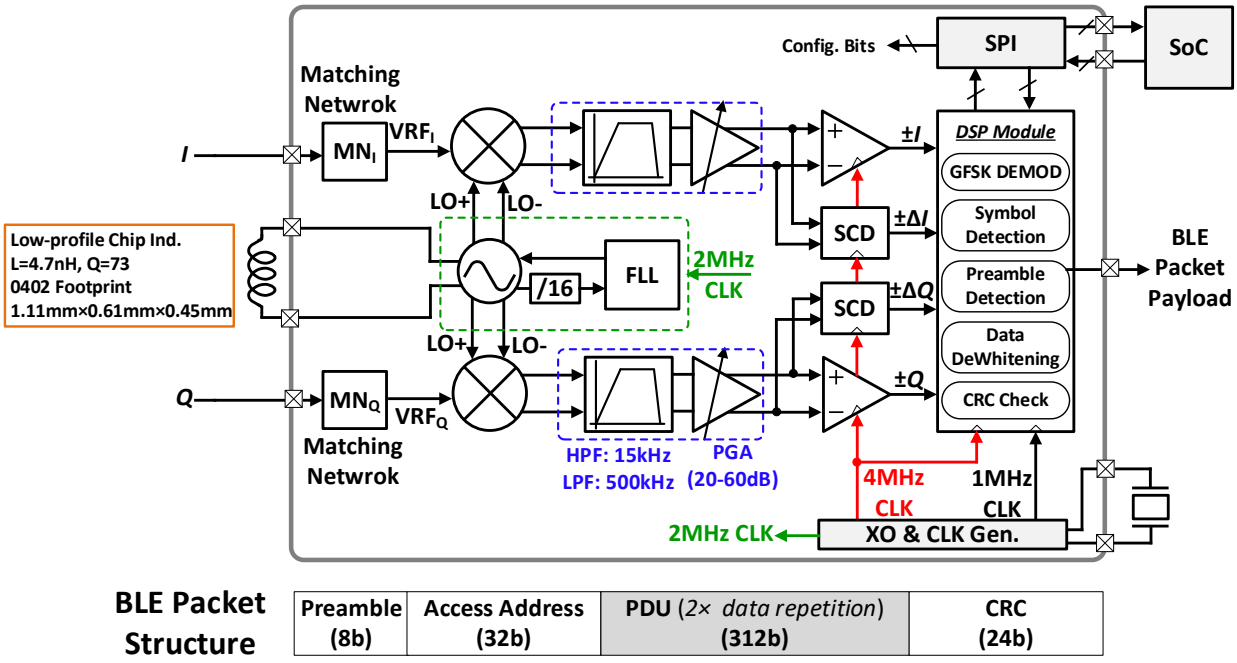
3.2 RF Front End

3.2.1 Passive I/Q Generation Network

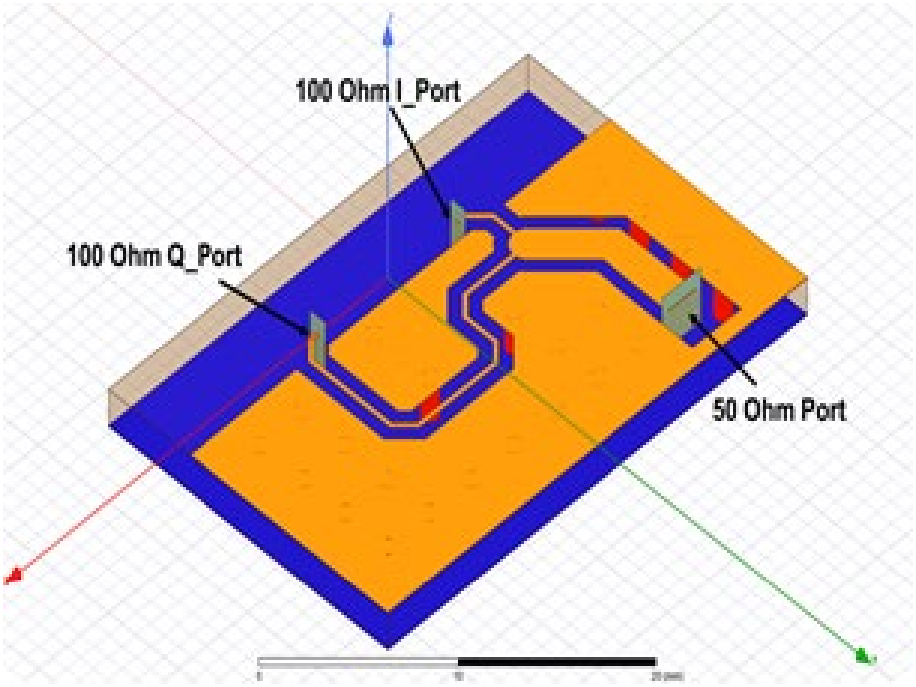
A block diagram of the receiver is shown in Fig. 3.1(a). Quadrature signals with a differential LO are used instead of quadrature LOs to save power. The quadrature LO OSC consumes around 2× the nominal power of a differential LO OSC which cannot be used in low power designs. For RF path quadrature generation, a 1st order RC-CR network is typically adopted for passive I/Q generation [113]. This approach is not adequate for mixer-first architectures because of the high NF degradation due to the lossy network. Another approach is to use off-chip hybrid quadrature couplers but they are bulky and costly.

In this work, we propose an antenna-chip co-design approach for RF quadrature generation. A 50Ω single port antenna followed by a lossless T-junction power divider with a $\pi/2$ relative phase shift can be used instead with only a 3dB NF degradation. The π/2 relative phase shift between the I/Q ports is achieved through adjusting the lengths of the CPW transmission lines routings in the PCB from the antenna to the chip as shown in Fig. 3.1(b).

The I/Q ports on-chip are matched to 100Ω for proper impedance matching seen at the antenna ports. Two on-chip LCC impedance matching networks (Fig. 3.2) match the high input impedances of the I/Q mixers to 100Ω providing ~8dB passive gain and improving the NF. Also, they serve as a bias network for the mixers to be able tune the mixers' input impedance for proper matching.



(a)



(b)

Figure 3.1 (a) Architecture of the proposed backchannel RX with a passive I/Q generation which can be achieved using b) a 50Ω single port antenna employing a lossless T-junction power divider.

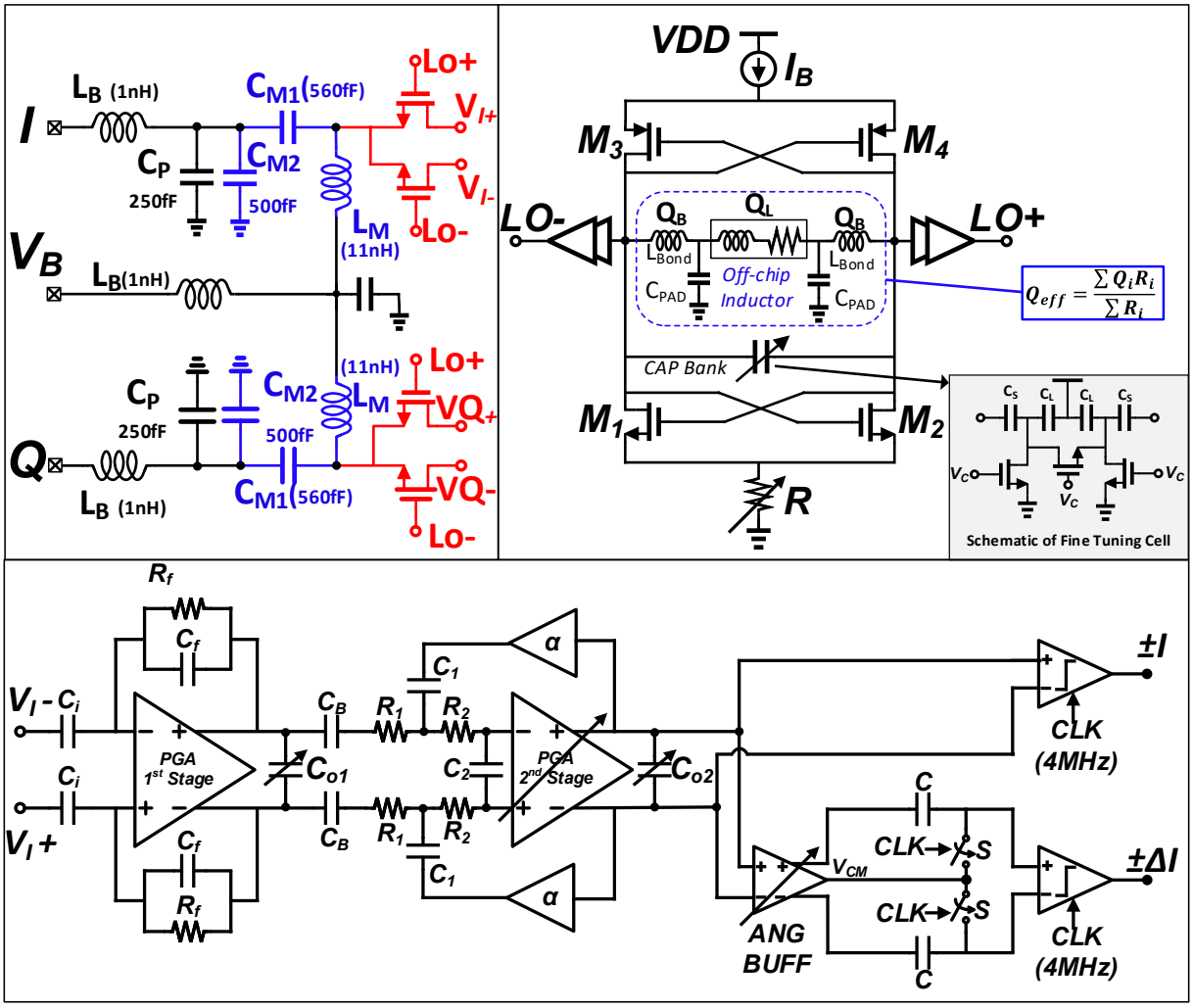


Figure 3.2 RF front-end and analog baseband circuitry showing: input matching network, mixer biasing, LC-DCO, two-stage PGAs and SCD of the I-channel.

3.2.2 LC-DCO

An LC-based digitally-controlled oscillator (LC-DCO), shown in Fig. 3.2, is critical to attain the BLE phase noise requirement derived from the standard specifications. The DCO power reduction is limited by the quality factor (Q) of the LC tank which is dominated by the Q of the On-Chip inductors, typically <15. A low profile off-chip inductor with a Q>70 at 2.4GHz is

integrated with the die in a QFN package achieving a small form factor. The external inductor is placed close to one side of the die to shorten bonding wires in order to avoid degradation of the effective inductor Q presented to the tank. Therefore, the chip layout floorplan is optimized to only include two PADs at that side which connect the off-chip inductor to the LC-tank.

The LC-DCO uses a PMOS current source and a tail resistor to adjust the output common-mode voltage to VDD/2. This is necessary to achieve a 50% duty cycle after the LO buffers to avoid the self-mixing problem might be caused by the 2nd harmonic. Two capacitor banks with course tuning (4b) and fine tuning (8b) are designed to meet the desired frequency resolution (~32KHz) and cover the entire tuning range (110MHz). Each unit capacitor consists of MOM capacitors and NMOS switches. To reduce the equivalent series resistance (ESR), large W/L LVT transistors are used. The LC-DCO and LO buffers consume 170μW and achieves -110dBc/Hz phase noise at 1MHz offset.

A 25μW counter-based frequency locked loop (FLL) is implemented to locks the LO frequency to the desired BLE channel (Fig. 3.3). A TSPC div-by-16 circuit is used to divide the LO frequency (2.4-2.48GHz) to a lower frequency which is used for frequency locking to further decrease the power consumption. The logic of the FLL block runs at 2MHz clock provided by the on-chip crystal oscillator.

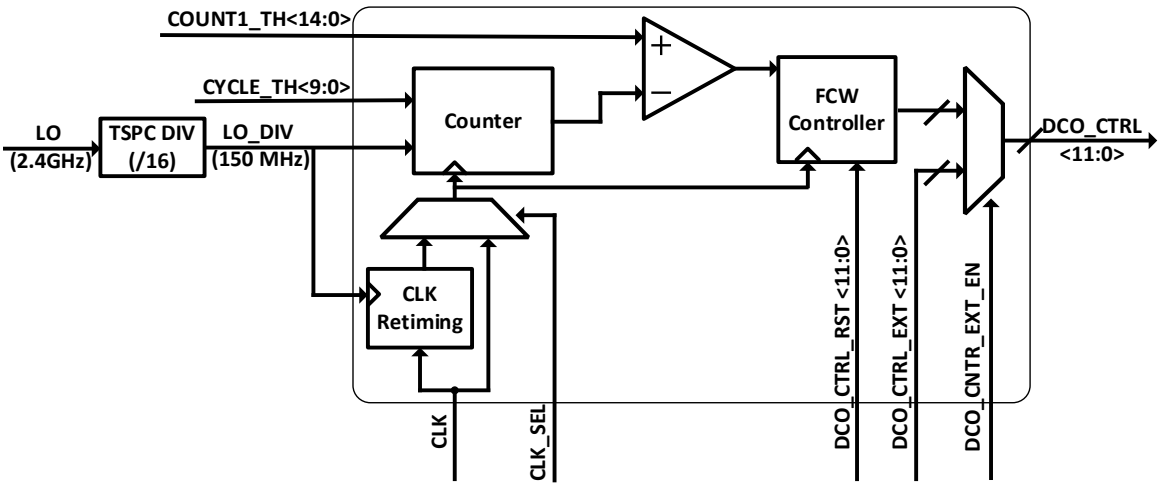


Figure 3.3 Block diagram of the counter-based FLL.

3.2.3 Baseband PGA

The receiver comprises a programmable two-stage PGA adopted from [114] as shown in Fig. 3.2. The first stage implements a first-order CR HPF with cutoff frequency at 18 kHz to remove the DC offset and flicker noise without degrading the BER for GFSK modulation index of 0.5. The second stage PGA is a 2nd order Sallen-Key low pass filter. The overall PGA performs a 3rd order LPF with a cutoff frequency of 470 KHz which is sufficient to suppress interferers at adjacent channels.

3.3 Proposed GFSK Demodulation

The demodulation of GFSK is a design challenge for its strict requirements on power and robustness. The baseband GFSK modulated signal is represented in the complex phasor domain as a rotating vector with amplitude proportional to the strength of the received signal. Clock-wise and anti-clock-wise phasor rotations denote symbols ‘0’ and ‘1’, respectively as shown in Fig. 3.4. The overall angle of phasor rotation over one bit duration is a function of the modulation index and

data rate; resulting in a rotation angle of less than π/2 at 1Mbps. Hence, simple zero-detection algorithms cannot be applied in I/Q waveforms for demodulation. High resolution phase analog-to-digital converters (Ph-ADCs) were introduced for demodulation based on the phasor rotation's direction [114]. N-ary Phase ADCs split up the I/Q plane by defining N/2 thresholds with an angle of 2π/N. This approach requires signal conversion and linear combination circuits, applying accurate pre-calculated weights to both I and Q to obtain demodulation based on zero-crossing detection. This technique leads to high power consumption while being prone to the inevitable I/Q imbalances.

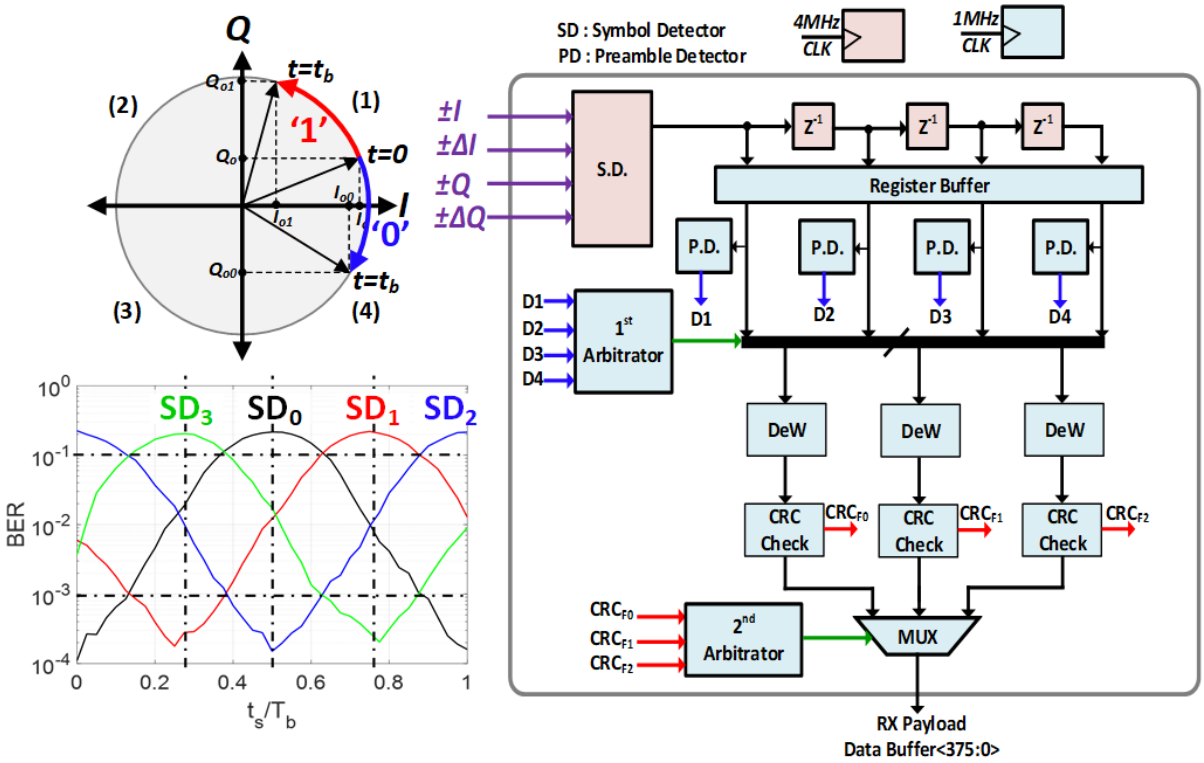


Figure 3.4 Proposed GFSK demodulation, symbol detection, packet synchronization, and CRC check.

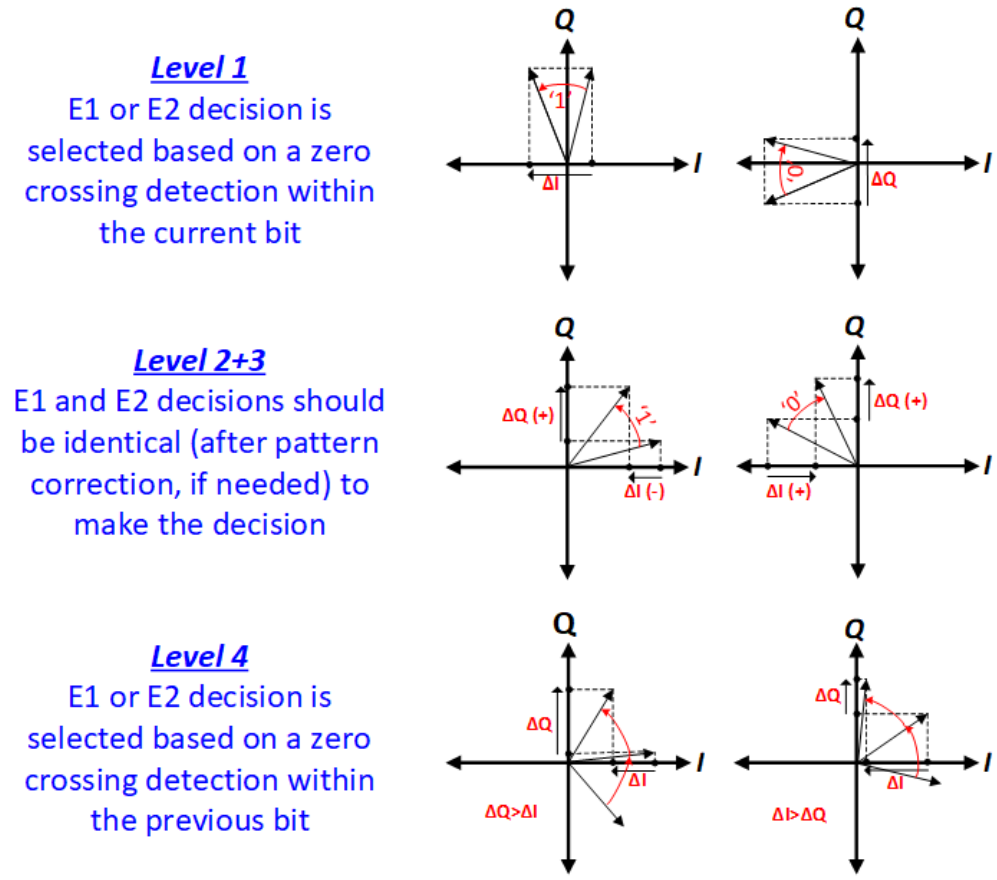


Figure 3.5 Proposed 4-level symbol detection algorithm implemented in DBB. The SD is independent on the random input phase of the received signal.

This work proposes a time-domain GFSK demodulation by examining the waveforms of the real I/Q signals separately without dealing with them in the complex phasor domain. A 10μW coherent GFSK demodulation is presented which consists of two discrete-time differentiators and four dynamic comparators. Two dynamic comparators are connected directly to the outputs of the PGAs generating ±I and ±Q signals. The other two comparators are connected to the outputs of the differentiators generating ±ΔI and ±ΔQ where +/- represent increasing and decreasing slopes, respectively. The received vector's rotation direction can be identified accurately by determining its quadrant number (±I, ±Q) and the rate of change of either I (±ΔI) or Q (±ΔQ) (Fig. 3.4) over a

1bit duration. This redundancy in information is exploited to improve the accuracy of the symbol detection algorithm. The proposed demodulator is highly immune to the phase and amplitude imbalances of the quadrature signals. Switched capacitor differentiators (SCDs) are utilized for their power-efficient operation and high-frequency noise filtering at the expense of gain. The SCD's input resolution for a given SNR sets the required voltage gain of the preceding stages. Fig. 3.2 shows the circuit schematic of the SCD which consumes only a 3μW.

Since the PLL is eliminated to save power, over-sampling is used for packet synchronization. Higher over-sampling factor (OSF) improves the performance; however, the OSF is limited by the SCD's input resolution. OSF of 4 is found to be an optimum choice in terms of power budget, SCD's resolution, and SNR requirement for the sensitivity spec. The digital symbol detection algorithm operates at 4× the baseband clock frequency and employs two independent engines running in parallel; E1:{±I, ±Q, and ±ΔI} and E2: {±I, ±Q, and ±ΔQ}. A sequential four-level decision algorithm built on the confidence level is followed as described in Fig. 3.5. In level (1), the output of E1 or E2 is prioritized based on zero-crossing detection in either I or Q signals. A zero-crossing in I significantly minimizes ΔQ and vice versa. Hence, a zero-crossing in I prioritizes E1's decision while a zero-crossing in Q prioritizes E2's decision. In the case of no zero-crossing, the outputs of both engines are compared to reliably make a decision in level (2) examining each engine's decision independently. If the outputs of both engines don't agree, level (3) performs sequence correction to the invalid samples' patterns using a predefined LUT and hence re-evaluates E1 and E2 decisions. If they still don't agree, level (4) will prioritize either the E1 or E2 decision based on zero-crossing detection in the previous symbol similar to level (1) criteria. In case of symbol detection failure over the aforementioned levels, symbol '0' will be assumed.

The block diagram of the entire DSP block is shown in Fig. 3.4. The packet synchronization is achieved through phase arbitration, accomplished in two steps. A pipelined symbol detector generates symbols at the rate of 4MHz (4x the data rate) corresponding to four phases of the input symbols. The four phases of the symbols are then synchronized to a 1MHz clock edge and applied to four parallel preamble detectors (PDs). The first phase arbitration criterion is based on the preamble detection. Since the preamble length is only 8b (BER of <12.5%), three or less PDs will be able to detect the preamble as shown in the bottom left corner of Fig. 3.4. However, only one SD will meet the BER requirement of 0.1% for the properly aligned packet. Since it is difficult to identify at this point which is the correct phase shift and corresponding PD output, three parallel data de-whitening (DeW) and cyclic redundancy check (CRC) branches were implemented. The first arbitrator multiplexes the outputs of the four SDs to one of the three idle branches based on the PD outputs using a predefined mapping scheme. The second arbitrator picks the packet with correct CRC and stores it in the data buffer. Simulations show that this approach improves the packet drop rate to be less than 2% assuming no interference. Adjacent channel interference tolerance is accomplished by providing enough PGA filtering to achieve -17dB SIR at 2MHz offset.

The BLE access address is fixed for the non-connectable advertising mode, a programmable preamble length of up to 16b is implemented to improve the packet drop rate. This considerably mitigates the shadowing effect due to false preamble detections. Additionally, increasing the preamble length reduces the number of PDs that can detect the start of the packet to two or one; leading to an extra power saving.

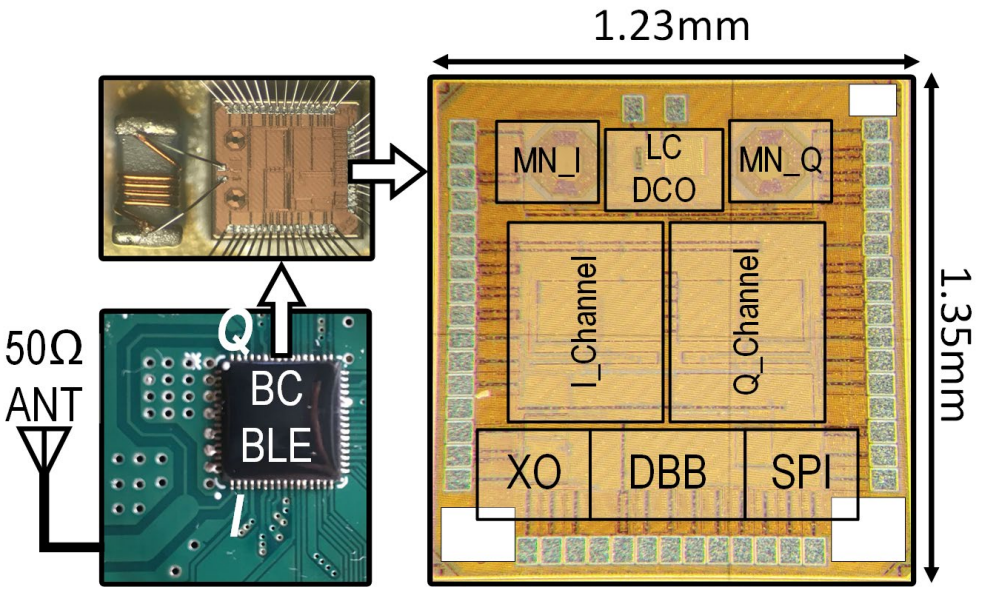


Figure 3.6 On-board I/Q generation, in-package inductor, and Die micrograph.

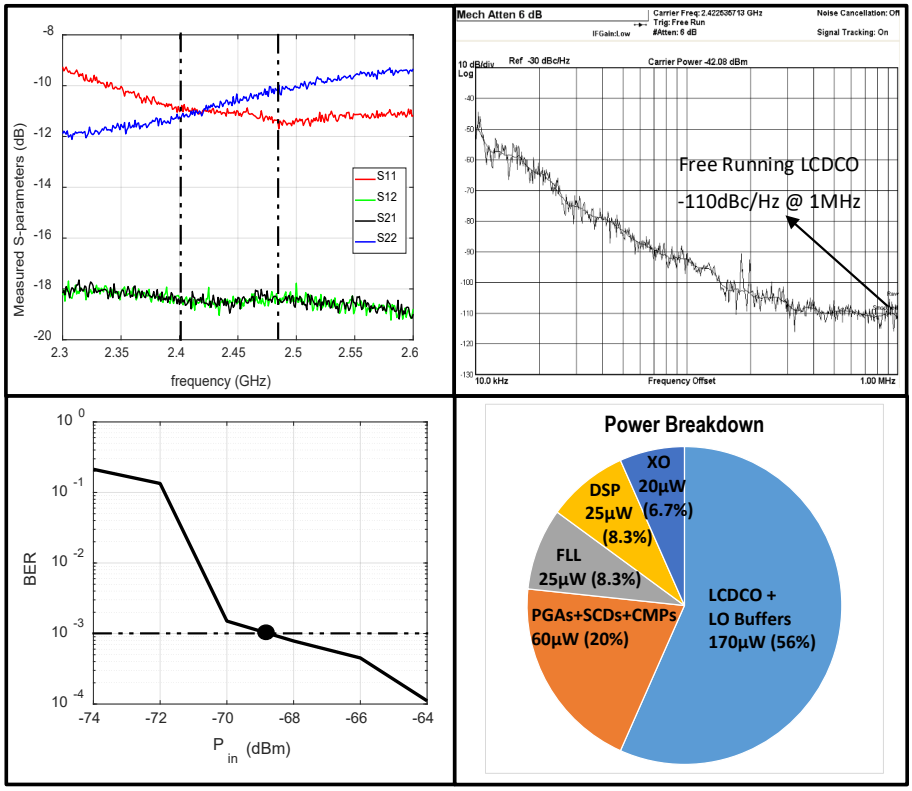


Figure 3.7 Measured performance of BLE receiver (S-parameters, LCDCO phase noise, sensitivity) and the power breakdown of the receiver.

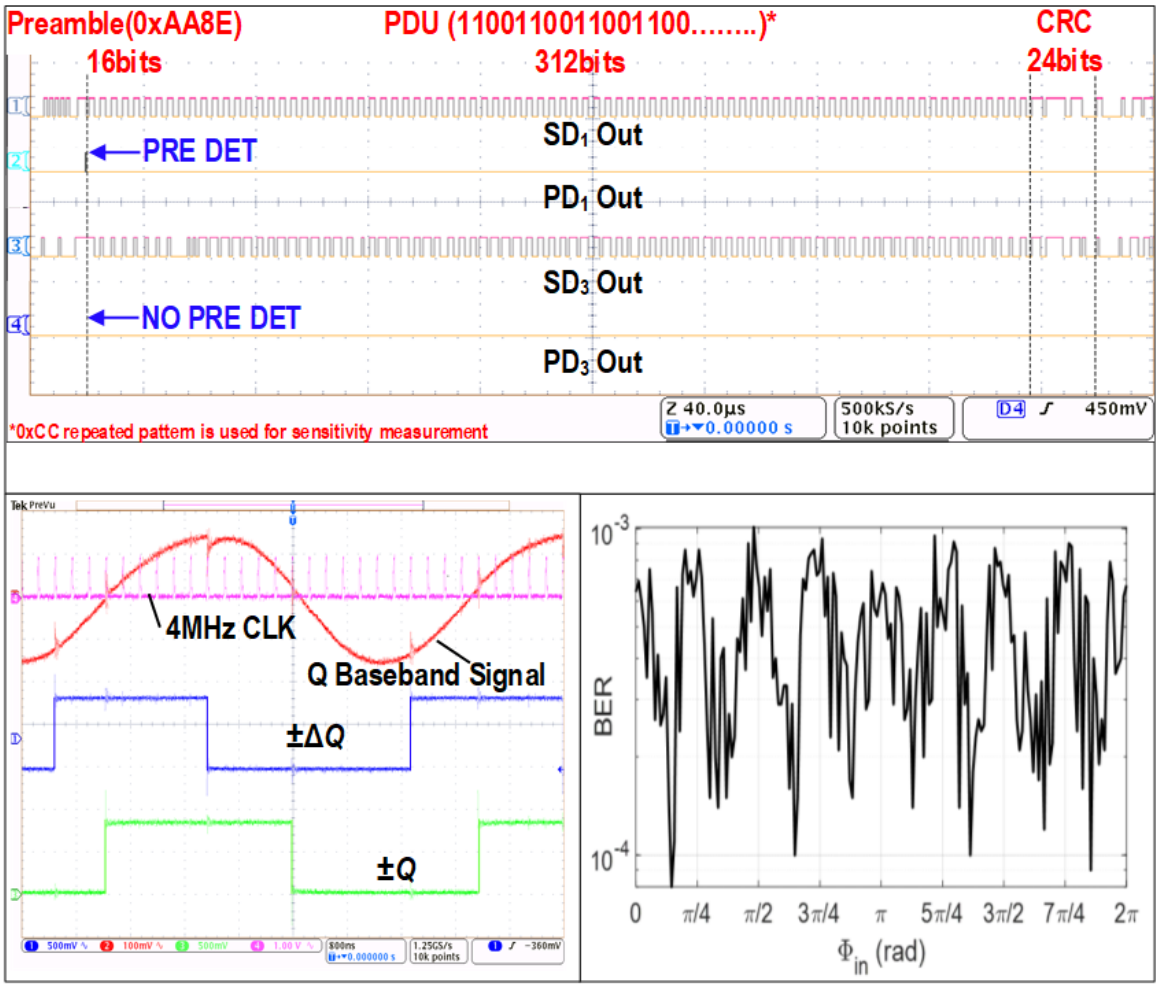


Figure 3.8 Timing diagram of: 1) a received packet, 2) baseband signal. The simulated effect of the random input phase on the BER showing the robustness of the proposed symbol detection algorithm.

3.4 Measurements

The chip was fabricated in 40nm CMOS process and occupies an area of 1.66mm2 including the on-chip matching (Fig. 3.6). The inductor is integrated with the chip in a QFN package. The entire B.C. BLE RX consumes a 300µW active power and Fig. 3.7 shows the power breakdown. Figure 3.7 also shows the measured RX performance achieving -69dBm sensitivity for 0.1% BER. The NF of the mixer-first RX, including the passive I/Q generation, is 20dB. The

measured s-parameters show good matching at the I/Q RF ports and a coupling of less than -18dB between both ports. Figure 3.8 shows an example of a received packet and the baseband waveforms after the comparators showing the monitored outputs of 2 PDs and 2 SDs. The proposed GFSK demodulator maintains the BER independent on the initial phase while tolerating up to ±6dB I/Q amplitude imbalance and ±10o phase imbalance. The performance of the B.C. BLE RX is summarized and compared with recent works in Table 3.1. The proposed RX achieves 0.5Mbps effective data rate making it a good candidate for low power IoT applications.

Table 3.1 Comparison with recent fully-compliant and backchannel BLE receivers.

	This Work	[1]	[2]	[3]	[4]	[5]	[6]
		ISSCC'20	ISSCC'20	ISSCC'17	T-MTT'13	RFIC'18	CICC'18
Standard	BC - BLE	BC - BLE	BLE	BLE	BLE	BC-BLE	BC-BLE
Data Rate	0.5 Mbps	1Mbps	1/2Mbps	1Mbps	1Mbps	0.1125Mbps	0.333Mbps
Supply Voltage	0.9V	0.9V/1V	0.5V	0.18V	1V	0.9/1.1V	0.75V
Technology	40nm	40nm	22nm	28nm	130nm	65nm	65nm
Integration Level	RF/DBB/XO /External Inductor	TX/RX/DBB	RF/ADPLL /DBB	RF only	TRX: RF/ABB	RF/DBB	RF/DBB
RX Architecture	Zero-IF	Low-IF	Low-IF	Zero-IF	Zero-IF	Zero-IF	Low-IF
Image Rejection	No image	-	-	No image	No image	No image	-
Noise figure	20 dB	12dB	-	11.3dB	16dB	-	-
RX Sensitivity	-69dBm	-86dBm	-96dBm	-	-81.4dBm	-57.5dBm	-76.6dBm
Active Power	300µW	2100µW	1900µW	382µW	1100µW	150µW	230µW
Radio Area	1.5mm2	1.3mm2*	1.9mm2	1.65mm2	2.1mm2	1.1mm2	4mm2
On-chip Matching	Yes	No	Yes	Yes	Yes	No	No

3.5 Conclusion

This chapter presents a 300µW BLE backchannel RX for ultra-low power IoT applications. A mixer-first zero-IF architecture is employing I/Q generation in the RF path is presented. A switched-capacitor differentiator-based GFSK demodulator is designed consuming only a 10µW. The RX achieves -69dBm sensitivity for 0.1% BER at 0.5Mbps.

Chapter 4

A Low Power Bluetooth Low-Energy Transmitter with a 10.5nJ Startup-Energy Crystal Oscillator

4.1 Introduction

For wireless sensor nodes and the majority of the low-power devices used in the Internet of Things (IoT), Bluetooth Low-Energy (BLE) is becoming the preeminent protocol for short-range wireless communications [117]. In such applications, the battery is expected to last as long as the life of the product, which can be in the order of 10 years for an embedded device performing signal processing and wireless communication. Often, the RF radio accounts for a significant portion of the aggregate power profile of the device.

Many works have been devoted to design low-power BLE radios to extend the battery's lifetime and to enable their adoption in energy-harvesting applications. However, state-of-the-art BLE radios still consume several milliwatts of power due to the strict phase noise requirement and the complexity of local oscillator (LO) generation [118]. For instance, a typical BLE radio transmitter (TX) consisting of a phase locked loop (PLL) and voltage control oscillator (VCO) followed by a power amplifier (PA) consumes more than 3mW [119, 120]. Efficient techniques such as asymmetric communications, duty-cycling (Fig. 4.1) and wakeup techniques, and open loop GFSK modulation have been reported to reduce the power consumption of the radio [44].

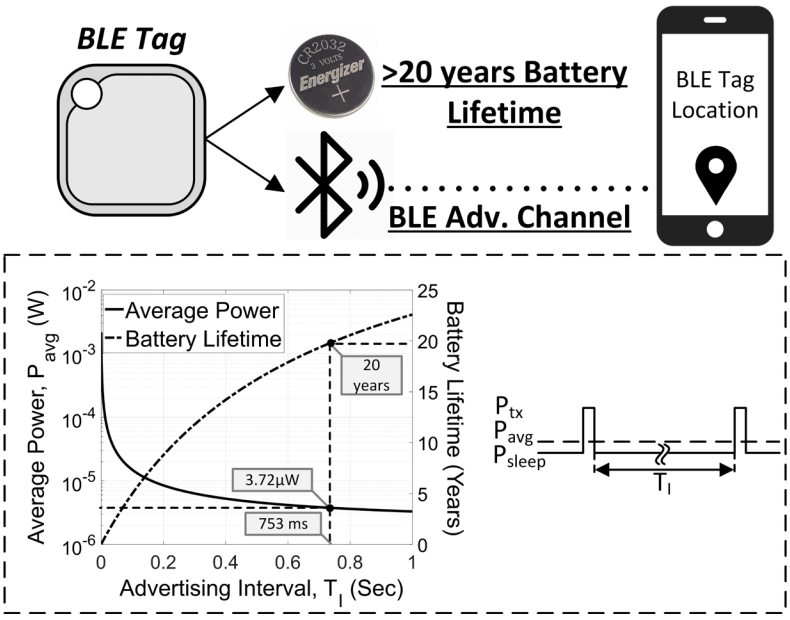


Figure 4.1 System level application for the proposed low power BLE TX.

In this paper, we propose a fully-integrated, low power BLE TX that demonstrates BLE standard-compliant communication to a mobile phone at a distance >8m. By combining open loop transmission and low power crystal oscillator, we can achieve a 3.5nJ/b total energy per bit including the startup energy.

The rest of the chapter is organized as follows: Section II describes the BLE TX overall architecture of the. Then, the fast startup crystal oscillator is presented in Section III. Section IV discusses the measurement results and the comparison to the state-of-the-art. Finally, Section V draws the conclusion.

4.2 Transmitter Architecture

Energy per bit, E_b, is considered the most important figure of merit (FoM) in BLE radios. Traditionally, E_b is calculated as:

$$E_b = P_{avg}/R_b \qquad (1)$$

where P_{avg} is the average power consumption per transmission and R_b is the data rate. However, this definition doesn't entirely reflect the actual E_b for the BLE TX since it doesn't account for the startup energy of both XO and PLL, which might be significant. Thus, we define the total E_b in this chapter as:

$$E_{b,tot} = E_{tx}/N_b \qquad (2)$$

where E_{tx} is the overall energy consumption to transmit one packet including the startup energy, and N_b is the number of bits in the packet. The total E_b in this work is 3.5nJ/b when transmitting an advertisement packet of 368 bits. To the best of the authors' knowledge, this is the first reported total E_b.

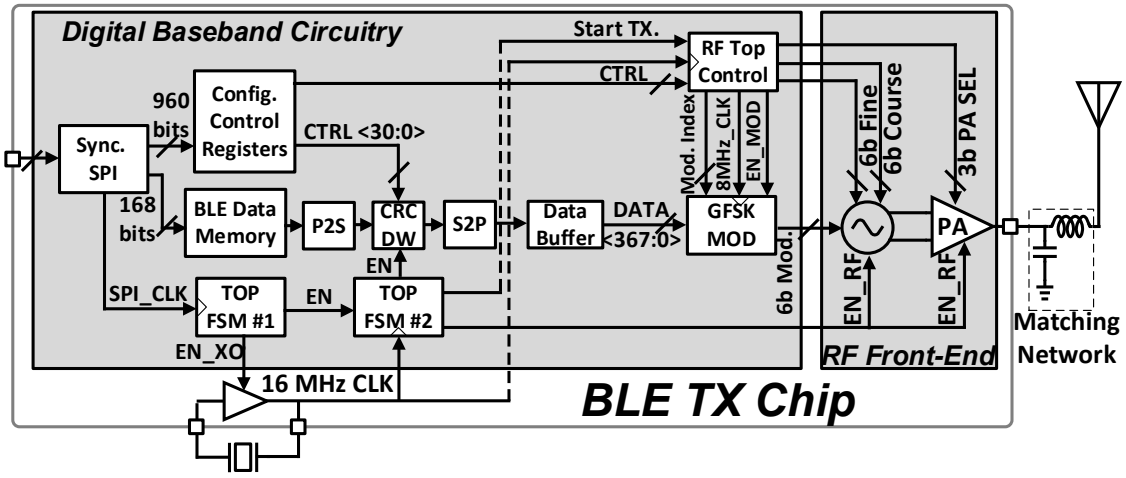


Figure 4.2 Simplified block diagram showing the architecture of the proposed low power complete BLE TX.

The average active power for a single packet transmission, P_{tx}, is 2.17mW over a 600µs transmission period. In order to extend the battery lifetime, a duty-cycling technique is

implemented between successive transmission events. This leads to a significant increase in operational lifetime for battery-powered devices. In this paper, the advertising interval, T_I, is defined such that the battery lifetime is more than 20 years. Using a common CR2031 coin battery with an energy density of 653mWhr, the required average power consumption is $3.72\mu W$, which is 1.86× of the sleep power, $P_{sleep} = 2\mu W$, as shown in Fig. 4.1. Hence, T_I can be calculated to be $753ms$. A good example application is a Tile key finder that establishes a Bluetooth connection to a smartphone as demonstrated in Fig. 4.1.

In order to achieve a low power operation, open-loop transmission of the GFSK modulated advertising packets is proposed to eliminate the Phase Locked Loop (PLL) block from the TX. The free running oscillator must comply with the requirements of the BLE standard in terms of the center frequency deviation (<150kHz), FSK modulation accuracy and frequency drift during the packet transmission (<50 kHz) which is 368 bits long. The simplified top-level block diagram of the BLE TX is shown in Fig. 4.2. The overall system architecture consists of three major blocks: a digital baseband (DBB), a 16MHz XO, and RF front-end. In this section, a description of the DBB and the RF front-end will be discussed while a detailed discussion about the XO is presented in the following section.

The BLE TX communicates with external systems through a Serial Peripheral Interface (SPI) to receive the advertisement messages and the configuration bits for the control units. A two-stage digital FSM packetizes BLE data and coordinates XO and TX behavior during transmission. After receiving a transmit-ready flag, the first FSM stage enables the XO with enough start-up time to achieve steady state operation before the second FSM, clocked by the XO, is enabled. The second stage takes the packet data from SPI and performs a BLE standard CRC check on the data. Then the packet, with post-pended CRC result, is fed through a data whitening block and directly

to the GFSK modulator. Transmission is initialized when the packet has been fully processed. Once the current packet is fully sent, the first stage resets itself in preparation for the next transmission event.

The GFSK modulator is implemented as an oversampled (8×) interpolative digital filter where the output frequency during the current bit is determined considering both preceding and following bits. The look-up table of the modulator array control word is pre-calibrated for open-loop modulation.

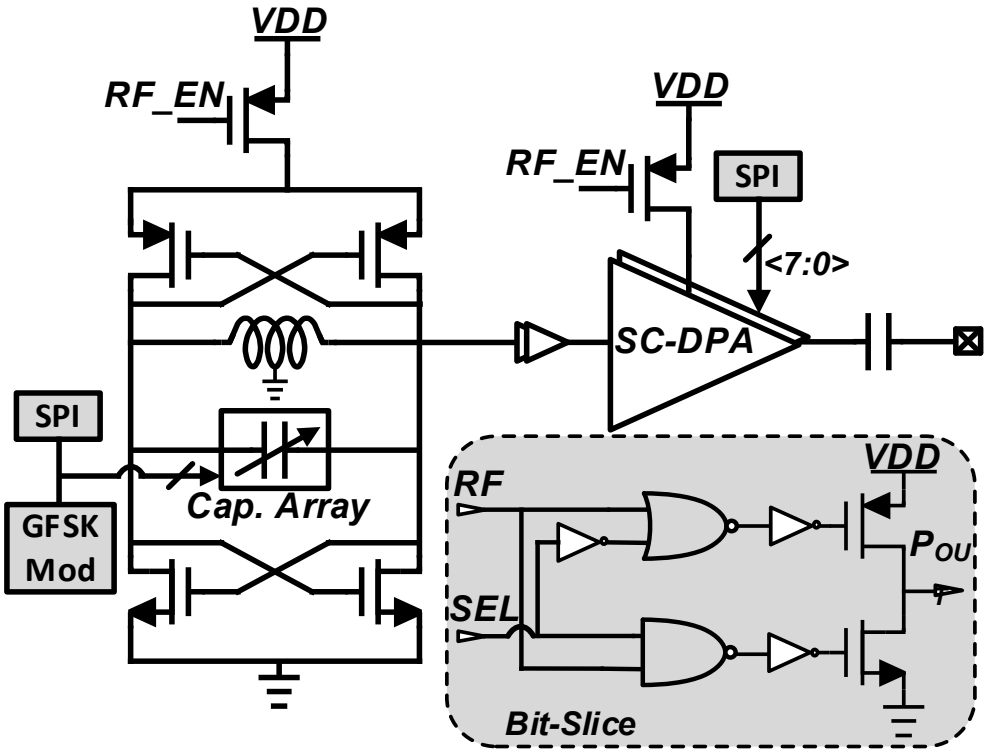


Figure 4.3 Circuit schematic of RF front-end.

The RF front-end is shown in Fig. 4.3 and consists of a digitally controlled oscillator (DCO) followed by a switched-capacitor digital power amplifier (SC-DPA). The DCO center frequency is determined based on the targeted BLE advertisement channel using a digitally switched MOM

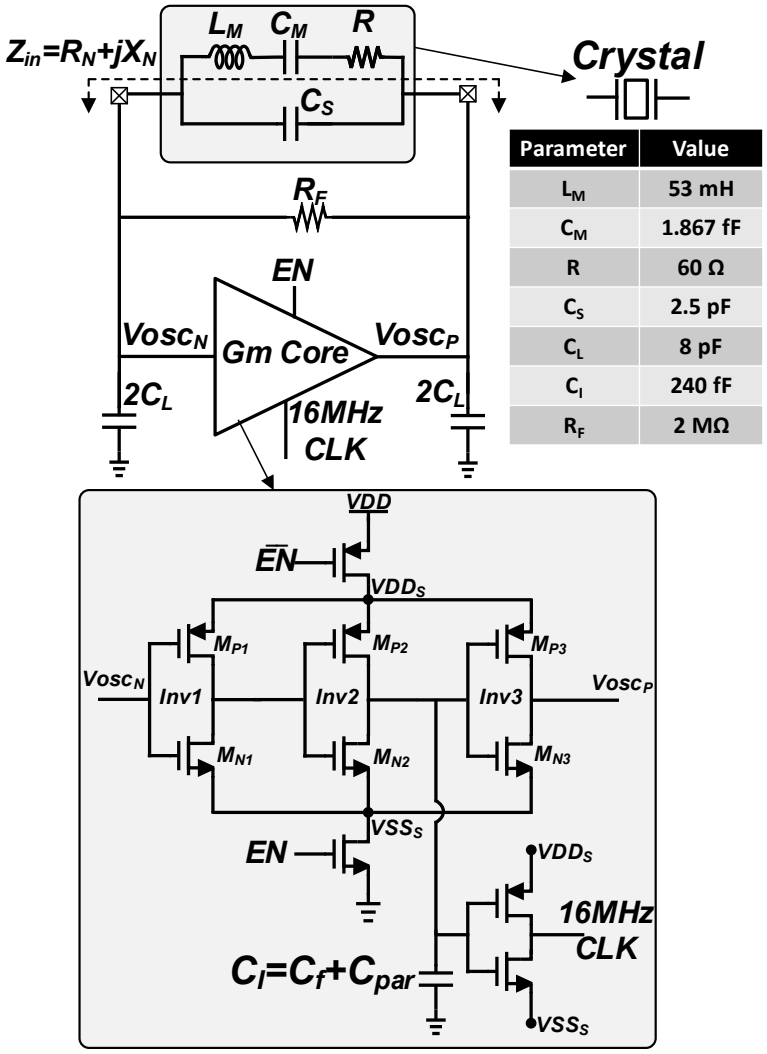
capacitor array resonating with the tank's inductor. The capacitor bank incorporates a coarse capacitor array obtaining ~110MHz frequency range to cover the BLE bandwidth in conjunction with a fine capacitor array. The DCO achieves a 32.2kHz frequency resolution and a phase noise of -118 dBc/Hz at 1 MHz required for BLE standard compliance. Furthermore, a 6b modulator capacitor array which has a resolution of 22.6kHz is designed for GFSK modulation. LVT NMOS switches with large W/L ratios are used to reduce the ESR and increase the capacitor bank's quality factor. The low power class-D SCDPA is thermometer coded with 8-bit cells to achieve various output power levels from -30 to -10dBm based on the targeted transmission distance. The SCDPA with partial on-chip impedance matching is optimized for the highest efficiency for -10dBm operation. The entire RF front-end consumes 2.75mW when transmitting a 368μs packet.

4.3 On-Chip Fast-Startup Crystal Oscillator

The XO is designed to minimize power consumption and achieve the goal of the low energy possible per BLE advertisement packet. The steady-state power consumption of the XO is critical since it is active during the packet transmission. In addition, given that the packet length is 368μs, the startup time/energy must be minimal in order to have an efficient BLE TX power profile. Also, it is important for the XO to have low phase noise to meet the BLE standard specification. Given the above requirements, the specifications of the XO are determined to be: 1) steady state power of sub 0.1mW, 2) startup time of less than 50% of the packet length, 3) startup energy of less than 1% of the overall energy per advertisement packet, and 4) integrated clock jitter of less than 25ps.

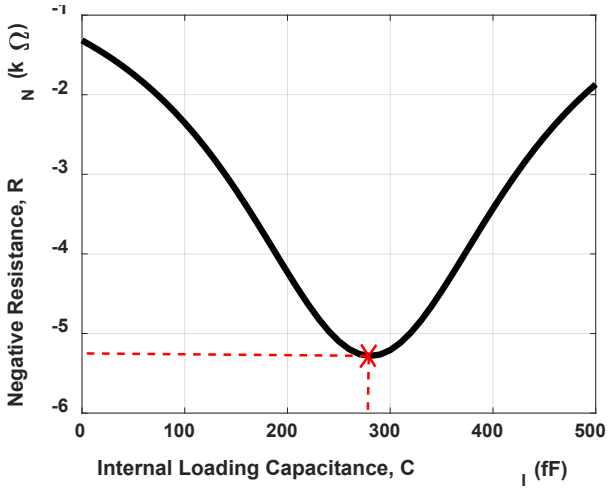
In this design, an enhanced capacitively loaded three-stage inverter chain is utilized to meet the aforementioned specifications. Fig. 4.4(a) shows the circuit schematic of the proposed XO as well as the equivalent circuit parameters of the crystal. In order to satisfy the startup oscillation

condition, the crystal losses must be compensated by an active Gm core resembling a large negative resistance [121]. The Gm core consists of a three-stage CMOS inverter chain with a scaling factor in the transistors' sizes, n. The inverter chain is preferable in low power applications to reduce the short-circuit current in the conventional inverter-based Pierce oscillator and hence the steady-state power consumption of the XO [122]. The size of *Inv1* is chosen to be twice the minimum transistor size to reduce its power consumption as its gate is connected to the crystal terminal that has a sinusoidal signal, $Vosc_N$.



Parameter	Value
L_M	53 mH
C_M	1.867 fF
R	60 Ω
C_S	2.5 pF
C_L	8 pF
C_I	240 fF
R_F	2 MΩ

(a)



(b)

Figure 4.4 (a) Circuit schematic of the fast-startup low-power crystal oscillator using three-stage capacitively loaded inverters and the crystal's equivalent circuit, and (b) simulation results of the series equivalent negative resistance versus the internal loading capacitance showing the optimum value of CI.

Based on [121], the negative resistance value of the three-stage Gm core can be boosted by loading each stage with a carefully designed capacitor. In this design, only the second inverter is loaded with a capacitor since the first inverter is restricted to have a smaller size and it cannot drive a large load capacitance. Fig. 4.4(b) shows the simulation results of the negative resistance, $R_N = Re\{Z_{in}\}$, versus the internal loading capacitor, C_I. It can be seen that the negative resistance is increased five times at $C_I = 280fF$ in comparison with the conventional Pierce oscillator having the same power consumption.

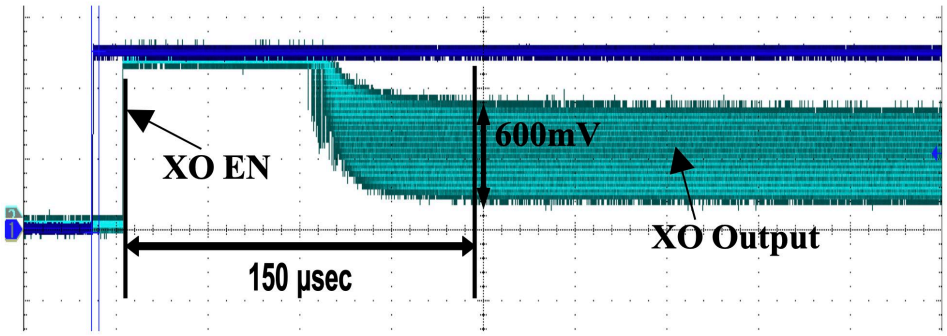


Figure 4.5 Measured startup time of the crystal oscillator.

Table 4.1 Measured Performance Summary and Comparison to The State-Of-Art

	ISSCC'16 [122]	ISSCC'17 [123]	ISSCC'18 [121]	This Work
Technology (nm)	65	90	65	65
Active area (mm^2)	0.08	0.072	0.023	0.00625
Supply voltage (V)	1.68	1	0.35	1.2
Frequency (MHz)	24	24	16	16
Load capacitance (pF)	9	10	6	8
S.S. power (µW)	693	95	31.6	70
Startup time (µS)	435	200	460	150
Startup energy (nJ)	N/A	36.7	15.8	10.5

4.4 Measurement Results

The BLE TX chip was fabricated in 65nm LP CMOS technology. The core area of the XO is 0.00625 mm^2 with an on-chip load capacitor of 8pF. The performance of the XO is shown in Fig. 4.5 and is compared with a conventional Pierce XO having the same power consumption. The startup time is reduced from 1.5ms to 150µs resulting in a 10X improvement. The proposed XO also has a steady-state frequency inaccuracy of less than 14ppm. The startup energy and the steady-state power are 10.5nJ and 70µW, respectively. The measured rms integrated jitter is 26ps which is adequate for BLE requirements. Table 4.1 summarizes a comparison with the state-of-art XOs.

The XO in this work exhibits the lowest startup energy, shortest startup time, and lowest steady-state power among published XOs.

The BLE TX chip consumes an average power of 2.17mW from a 1.2 V supply. The power consumption is dominated by the RF front-end power with packet-level duty cycling. A power breakdown as well as a timing diagram of the power versus time are shown in Fig. 4.6. The transmission event requires only 900µs including the startup time of the XO and the settling time of the DCO's center frequency. The only necessary off-chip components are for the antenna's impedance matching. Figure 4.7 summarizes the measured BLE TX performance. The modulated spectrum measurement of the BLE TX while transmitting a BLE packet is shown in Fig. 4.7(a), confirming that the BLE spectral mask is met. The measured transient response of the DCO frequency during a packet transmission is shown in Fig. 4.7(b) demonstrating that the frequency drift is below the BLE specification of 50kHz. The eye-diagram is calculated from the captured transient frequency domain signal and is shown in Fig. 4.7(c). It can be seen that the symbol period and frequency drift meet the BLE communication limit. Figure 4.8(a) shows the chip micrograph with 1.56mm^2 area. The wireless test setup shown Fig. 4.8(b) is configured to transmit a BLE iBeacon message as per our target application which is captured properly by a mobile phone. The BLE radio board was configured through a Pattern Generator Logic Analyzer (PGLA) kit. Finally, a comparison with recent low-power BLE transmitters is summarized in Table 4.2 showing the reported total E_b of the presented work. While [117, 118] have better reported E_b, they utilize an external crystal oscillator which its startup energy is not inlcuded in the E_b calculation.

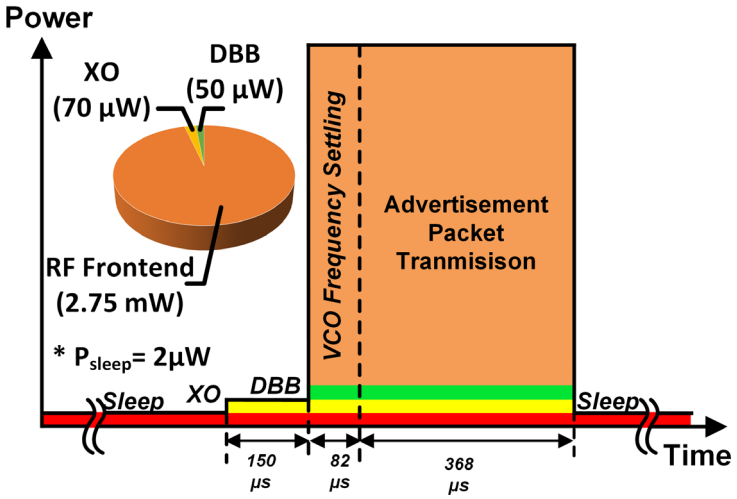
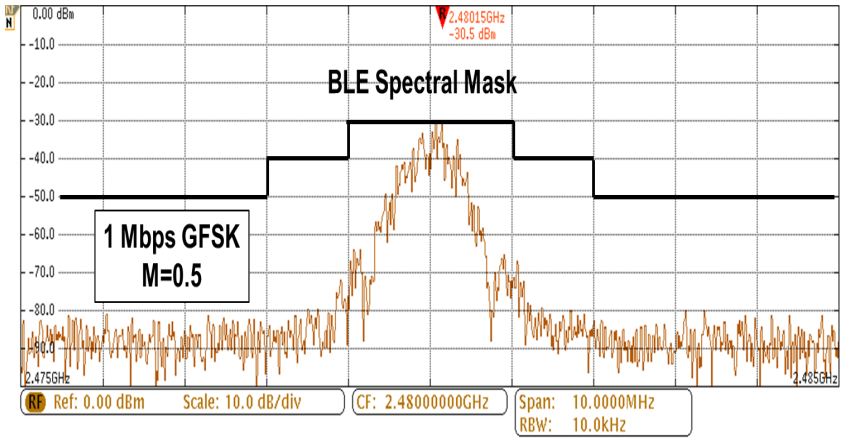
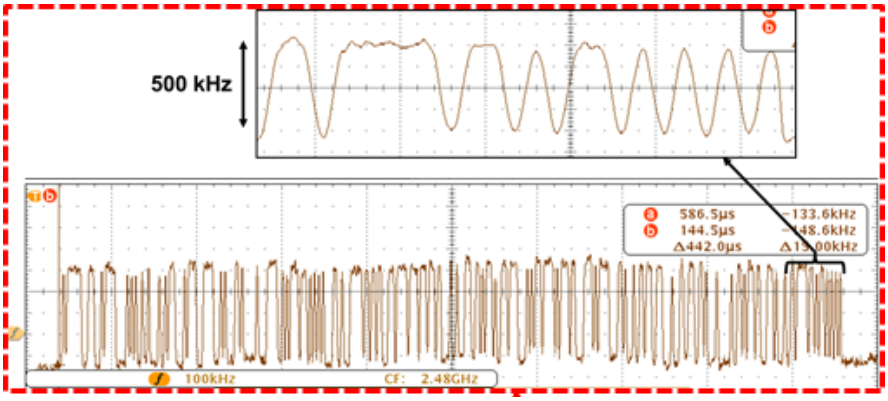


Figure 4.6 Timing diagram of the proposed BLE TX showing the duty-cycling operation and the power break down.



(a)



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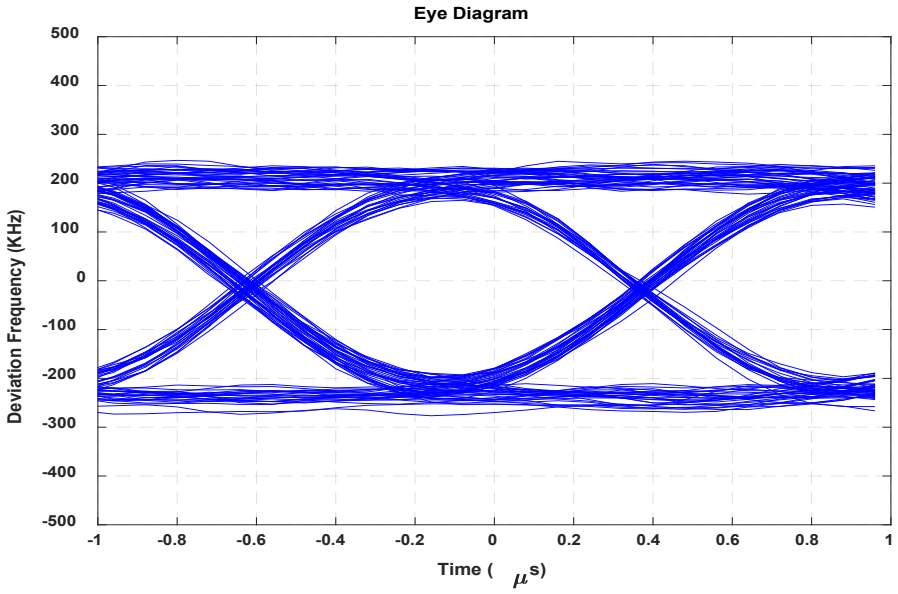


(c)

Figure 4.7 a) Continuous mode spectrum, b) transient of oscillator frequency, and c) eye diagram across two UIs.

Table 4.2 Measured Performance Summary and Comparison to The State-Of-Art

	ISSCC'15 [120]	JSSC'16 [119]	RFIC'18 [118]	ISSCC'19 [117]	This Work
Technology (nm)	40	28	40	65	65
Standard	BLE	BLE	BLE	BLE	BLE
Supply Voltage (V)	1	0.5/1	0.6	1.2	1.2
Power Consumption (mW)	4.2	3.6	0.49	0.61	2.87
Energy Per Bit (nJ/b)	4.2	3.6	0.49*	0.45*	2.87
Total Energy Per Bit (nJ/b)	N/A	N/A	N/A	N/A	3.5
Max TX Output Power (dBm)	-2	0	-19	-8.4	-10
Osc. Phase Noise @ 1MHz (dBc/Hz)	-110	-116	-85	-118.5	-118

* Doesn't include the startup energy of the external crystal oscillator

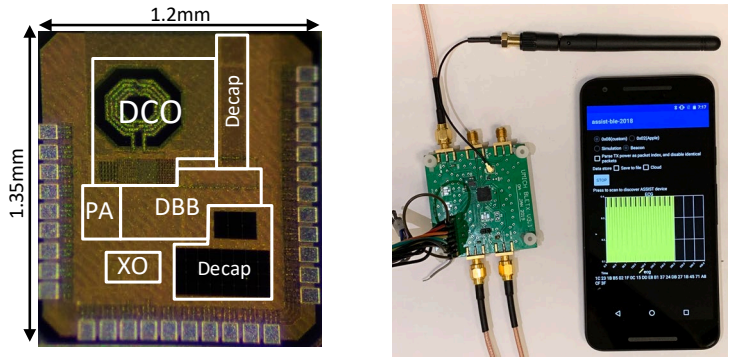


Figure 4.8 a) Die micrograph, and (b) wireless test setup showing a continuous reception of the BLE packet on a phone.

4.5 Conclusion

This chapter introduced a fully-integrated, low power BLE TX with the lowest reported energy per advertisement. The BLE TX consumes 2.17mW average power to transmit a 368bits advertisement packet entirely in 600µs resulting in a 3.5nJ/b total energy per bit. The top level architecture is based on the open loop transmission and duty-cycling techniques. The BLE TX also incorporates a fast startup time crystal oscillator with startup energy of 10.5nJ and steady-state power of 70µW.

Chapter 5

A Cell-Based Bluetooth Low-Energy Transmitter Employing RO-Based ADPLL in FinFET12nm Technology

5.1 Introduction

Automation in analog circuit design and integration has been steadily growing to meet the modern-day system-on-chip (SoC) requirements. Fast time-to-market demands quicker design cycles, where extensive use of standard digital cells, auxiliary analog cells, and even automated place-and-route tools for layout is preferred. Furthermore, the design complexity has increased significantly and more functional blocks are being integrated into SoCs. These challenges often translate to increased manual engineering efforts and non-recurring engineering (NRE) costs [106].

The objective of this project is to explore the design of fully-synthesizable wireless transceivers to meet a standard/user specifications. In this work, we presented a cell-based design approach for BLE transmitters which is amenable to be fully-synthesizable as a second step in the future. The BLE TX chip compromises a digital power amplifier, an all-digital PLL (ADPLL), a GFSK modulator and a top controller. A custom-design, cell-based switched capacitor power amplifier (SCPA) has been designed and optimized for high efficiency at low transmit power levels. The SCPA is hence used as an auxiliary cell at higher integration levels in the chip hierarchy. The open-source framework for Fully-Autonomous SoC design (FASoC) tool [124] has been exploited to design the ADPLL and to perform the top level integration of the entire BLE TX

including the auxiliary SCPA cell. The BLE TX architecture utilizes Ring-Oscillator (RO) based ADPLL for power and cost savings and was fabricated in FinFET12nm technology. To the best of the authors' knowledge, this work introduces the first RO-based BLE TX in FinFET technology.

The FASoC tool can generate complete mixed-signal SoC designs from user specifications based on a suite of analog generators [106]. The framework leverages differentiating techniques to automatically synthesize correct-by-construction RTL descriptions for both analog and digital circuits, enabling a technology-agnostic, no-human-in-the-loop implementation flow. In the FASoC tool, analog blocks like PLLs, LDOs, ADCs, and sensor interfaces are recast as structures composed largely of digital components while maintaining analog performance. They are then expressed as synthesizable Verilog blocks composed of digital standard cells and auxiliary cells (aux-cells). Novel techniques are employed to automatically characterize aux-cells and develop models required for generating bespoke analog blocks. The framework is portable across processes, EDA tools and scalable in terms of analog performance, layout, and other figures of merit. The SoC generation tool translates user intent to low-level specifications required by the analog generators. The fully composed SoC design is finally realized by running the Verilog through synthesis and automatic place-and-route (APR) tools to realize full design automation.

A new trend of BLE transmitter design is digitization. There are three major building blocks in a BLE transmitter: baseband processor, frequency synthesizer and power amplifier (PA). The baseband processor is a digital block that generates data packets for modulation and transmission. The frequency synthesizer converts the baseband signal into RF frequency at its target channel and applies modulation to the data. In addition, finally, the PA amplifies the signal for transmission. All-digital PLLs have been used more and more in recent designs [87, 101, 102]. Due to CMOS process scaling, digitally controlled capacitor banks can now reach very fine

resolution. Thus, the modulation signal, which used to be applied to the varactor in the LC-VCO in the analog charge pump PLL, is now applied to these digitally controlled capacitor banks in the ADPLL [87]. Recently, [104] proposed the first reported ring-oscillator based all-digital BLE transmitter design which has successfully removed the LC-VCO as the last analog circuit block in the frequency synthesizer block. The power amplifier has also gone digital as well. The class-D switched-capacitor digital power amplifier [105] has been adopted more and more in recent publications. Digital architectures benefit more from process scaling and could eventually be automatically synthesized using digital IC design tools [106]. This will result in significant reduction in production time and overall cost for circuit design.

The choice of the CMOS technology is critical in designing fully-autonomous wireless transceivers. Since the BLE transmitter is a part of an entire digital-rich SoC chip, FinFET 12nm technology is used as it benefits from Moore's law. FinFET devices display superior short-channel behavior, achieve higher computational capacity, have considerably lower switching times, and higher current density than conventional MOSFET technology. Additionally, they exhibit much lower leakage current compared to short-channel planar MOSFETs. However, traditional radio architectures require extensive use of high-quality passives, which might use large silicon area or not be available due to process limitations. Since FinFET technology is customized for digital design, the quality factor of passives in this technology is lower than conventional planar CMOS technology with RF flavors. For instance, the inductors' quality factor is limited to (7-10) in FinFET technology which requires extra design consideration for the power amplifier's output matching network. If the transceiver is integrated in a different technology node, multi-chip solutions are required, increasing system cost and form-factor.

5.2 BLE Transmitter Architecture

The complete BLE transmitter architecture is shown in Fig. 5.1 while the functional block diagram is shown in Fig. 5.2. The working principle of the BLE TX can be summarized as follows:

1. The BLE packet data is used to determine the frequency command word (FCW) required for the PLL.

2. The PLL locks the ring oscillator frequency to the desired BLE advertising channel and generates the desired modulated RF clock.

3. The PLL output drives a switched-capacitor power amplifier (SCPA) which is matched to the antenna port.

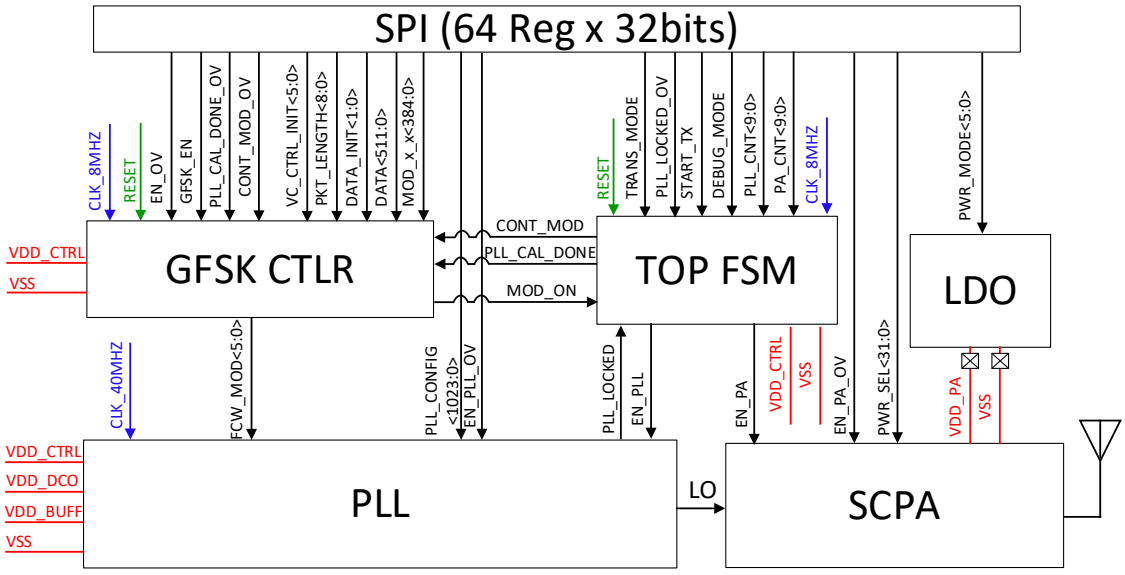


Figure 5.1 BLE TX block diagram.

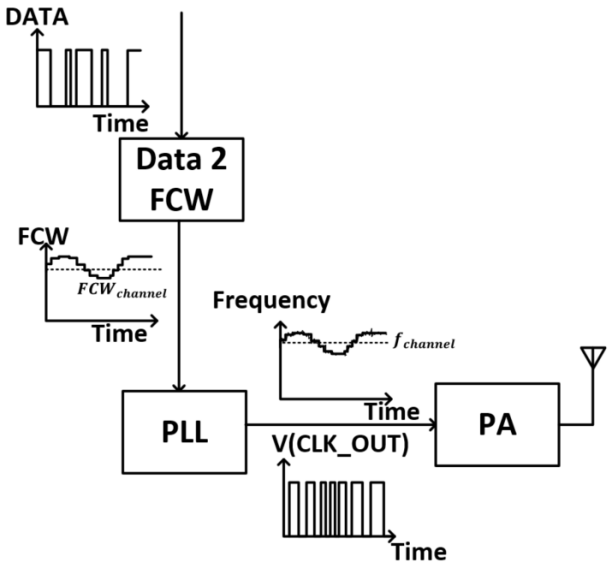


Figure 5.2 BLE TX functional diagram.

An 8X oversampled interpolative digital filter-based GFSK modulator is used to generate the desired frequency control word (FCW) for the PLL based on the packet's data. The FCW is 6bits width to modulate the modulation bank in the PLL based on the characteristics of the GFSK modulation index defined by the standard. The output frequency during the current bit is determined considering both preceding and following bits. The look-up table of the modulator array control word is pre-calibrated.

A fully-synthesizable, RO-based fractional-N all-digital PLL (ADPLL) is designed to satisfy the BLE standard requirements. The RO-based digitally-controlled oscillator achieves a 30 kHz frequency resolution to be able to generate the required GFSK modulation index. A hybrid time-to-delay converter (TDC) architecture is presented in order to achieve a fine time resolution with reduced spurious tones. The PLL uses a 40MHz reference clock frequency and consumes a 4.2mW covering a tuning range from 1.4-2.9GHz.

The output of the PLL is buffered to drive a 32-slice switched-capacitor power amplifier (SCPA) which is implemented to fulfil the class-2 power requirement with +4dBm maximum output power and -20dBm minimum output power. The output power can be controlled digitally through the SPI interface to determine the number of switching slices or by tuning the supply voltage through the on-chip LDO. An on-chip output matching network is designed to match the output impedance of the SCPA to the 50Ohms antenna. The inductance of the wire bonding and the parasitic capacitors of the PAD and the package are absorbed in the output matching network.

A top digital controller implemented as a finite state machine (FSM) enables both the PLL and the SCPA when needed to allow duty-cycling operation. It also monitors the locking state of the PLL before the starting transmitting the BLE packet through a hand-shaking scheme. Different modes of operation were designed for both debugging and transmission use cases. Details will be discussed later in this chapter. A SPI interface is integrated in the BLE TX to configure different blocks and serves as data buffers for the transmitted packets.

In the following subsection, we will focus on the design, implementation and measurements results of the building blocks.

5.3 Switched-Capacitor Power Amplifier

The switched capacitor power amplifier (SCPA) is a digital-PA architecture that achieves output amplitude tuning by controlling charge transfer in a capacitor array [125]. The SCPA comprises an array of capacitors that are either switched at the RF center frequency between the supply voltage (VDD) and ground (GND) or held at a signal ground, depending on a digital code word [126]. SCPA circuits exploit capacitors, which are area-efficient, native devices in CMOS technologies, precision capacitor ratios realized using well-known design and layout techniques,

and switches. Benefiting from CMOS technology scaling, the SCPA was employed in the BLE transmitter due to the advantageous high switching speed of MOSFET transistors in FinFET 12nm technology. Additionally, cell-based design approach can be utilized in designing SCPAs, allowing automation and scalability.

An SCPA comprises a capacitors array and is matched to the 50Ohm antenna through a band-pass impedance matching network as shown in Fig. 5.3. To achieve a specific output power, a certain number of the bottom plates of the capacitors array are switched at the RF center frequency between GND and VDD according to the digital control word. The un-switched bottom plates of the capacitors array remain connected to a signal ground (i.e., GND or VDD). In such a technique, the total capacitance seen by the output impedance matching network remains constant versus the digital code because no top-plate is ever switched [126]. Hence, the frequency response is fixed and the band-pass matching network does not require tuning at different output power levels.

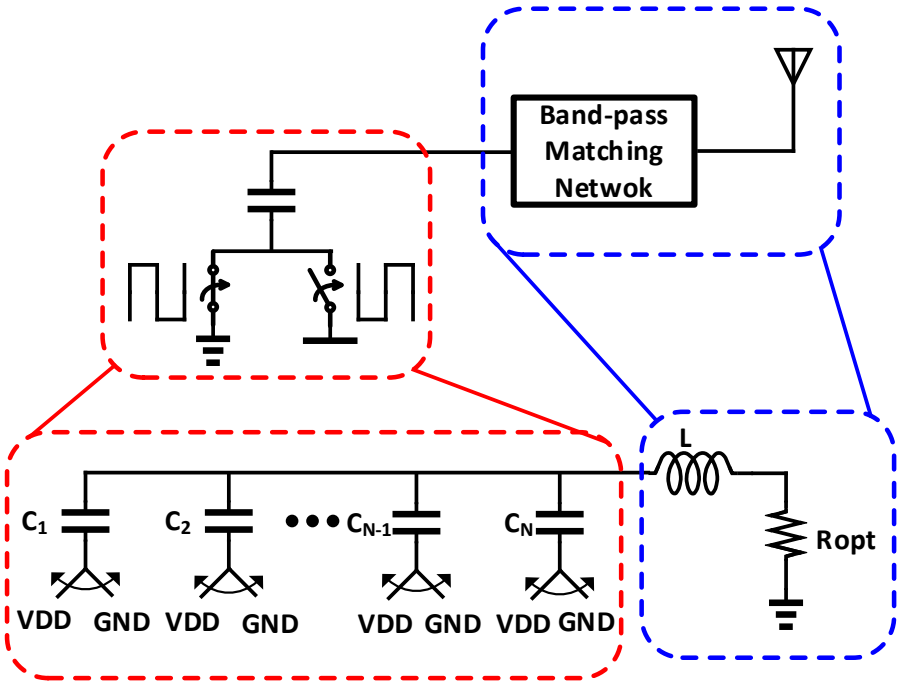


Figure 5.3 Block diagram of an ideal single-ended SCPA.

Based on the digital control word, a square-wave at the RF carrier frequency is generated at the capacitors' top-plate node with an amplitude proportional to the ratio of n/N, where n is number of switched capacitors and N is the total number of capacitors as follows[126]:

$$V_{OUT} = \frac{n}{N} \times VDD$$

The output impedance matching network filters the capacitors' top-plate square-wave voltage and transforms the impedance of the antenna from 50Ohm to the optimum load value presented to the SCPA to achieve the target output power (max of +4dBm in BLE class2 power). Because of the band-pass response of the matching network, only the fundamental component at the RF carrier frequency flows to the output. The output power can be calculated as follows [126]:

$$P_{out} = \frac{2}{\pi^2} \left(\frac{n}{N}\right)^2 \frac{VDD^2}{R_{opt}}$$

The peak output power when n=N is hence function of VDD and Ropt. Given a supply voltage of 0.8V for the FinFET12nm technology, the Ropt is estimated to be 20Ohms. An important observation from the above equation is that, output power can be tuned by tuning the number of switched capacitors (n<=N) or the supply voltage (VDD). In this design, we employed both tuning mechanisms to achieve fine/course tuning of the output power level while optimizing for higher power-added efficiency (PAE) as will be explained later.

The ideal PAE can be defined as [126]:

$$PAE_{ideal} = \frac{Pout}{P_{out} + P_{SC}}$$

where P_{SC} is the switching dynamic power and can be calculated as [126]:

$$P_{SC} = C_{in}\, VDD^2\, f$$

where C_{in} is the input capacitance driven through the selected switches, and f is the RF carrier frequency. C_{in} can be derived as [126]:

$$C_{in} = \frac{n(N-n)}{N^2} \times C$$

It can be seen that C_{in} is minimum at n=0 and n=N. Consequently, the switching dynamic power is minimum at both ends and increases in between. At peak output power, the dynamic loss is dominated by parasitic cap of clock drivers. Therefore, to achieve higher PAE at power backoff levels, reducing the supply voltage (VDD) helps with the PAE better than decreasing the number of switched capacitors. However, tuning the supply voltage is limited due to the constraints of the devices required headroom voltages and the devices maximum rating voltages.

Fundamentally, the PAE of the SCPA increases with CMOS technology scaling because of the reduced capacitive parasitics. For higher RF carrier frequencies, however, the requirement for wider switches increases dynamic power consumption in the driver chain which reduces PAE. Optimization is recommended in order to finalize the switch sizes.

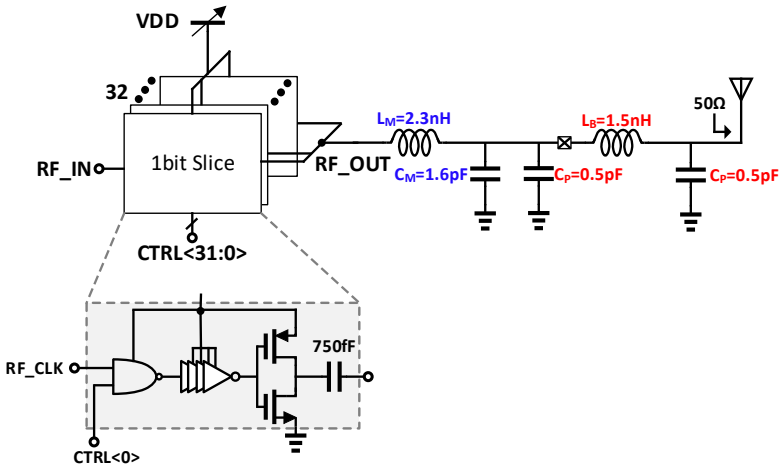
Since the output impedance matching compromises a series resonance circuit, the choice of the L and C values are critical to determine the loaded quality factor of the network as follows:

$$Q_{loaded} = \frac{2\pi fL}{R_{opt}} = \frac{1}{2\pi fCR_{opt}}$$

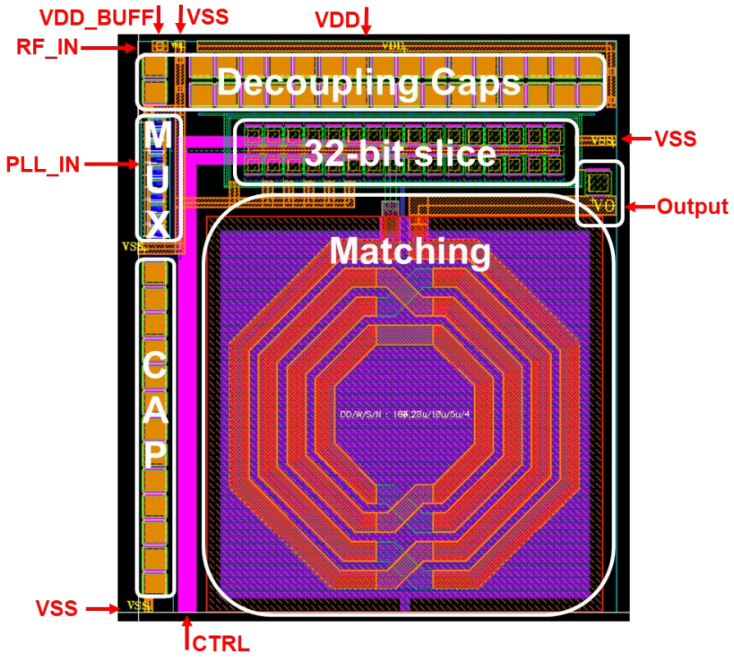
Although higher Q_{loaded} means less capacitance and dynamic power loss, its maximum value is limited by the Q of the inductor (7–10 in FinFET12nm technology) which limits the Q_{loaded} in fully integrated CMOS implementations. Design iterations are required to optimize the PAE at the peak output power.

A top-level schematic and layout of the single-ended SCPA is shown in Fig. 5.4(a) and 5.4(b), respectively. A 32-bit slices array (thermometer coded) is chosen to achieve the required tuning range for the output power level. The 32 slices are placed around the output common node which connects the top plates of all capacitors to the output matching network. For each clock

driver path, a cascaded chain of inverters with increased sizing is utilized preceded by a NAND gate for the digital control word selection. The parasitic capacitances and the wire-bonding inductance have been absorbed in the design of the output matching network. A multiplexer is used at the input of the clock driver circuit to enables an external RF input signal for debugging purposes. An overall 64pF decoupling MIM caps are used to reduce the supply noise.



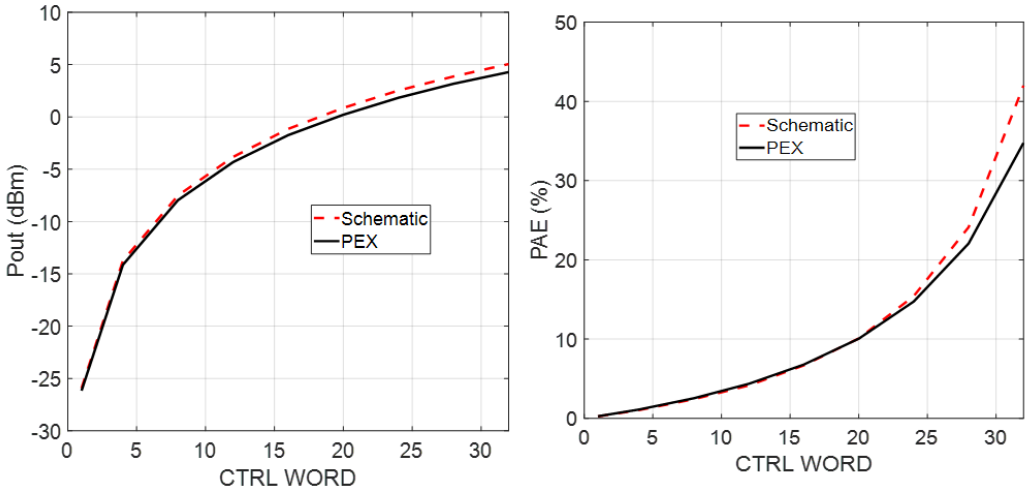
(a)



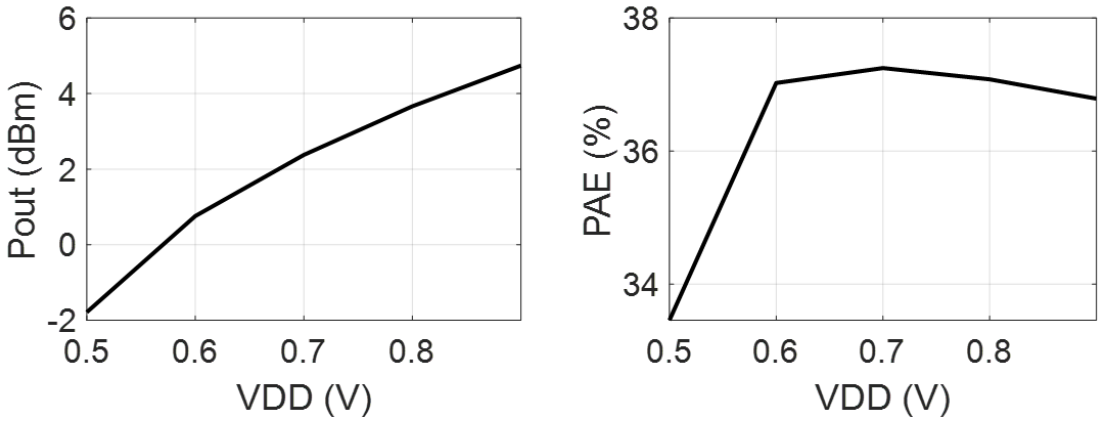
(b)

Figure 5.4 (a) schematic and (b) layout of the complete SCPA.

The post-layout output power and PAE versus digital control word of the implemented SCPA is shown in Fig. 5.5(a) while the output power and PAE versus supply tuning at n=32 is shown in Fig. 5.5(b). It can be shown that tuning the supply voltage from 0.5-0.8V results in 5dB variation of the output power level when n=N=32. From both figures, it can be seen that there are different supply and digital control combinations that result at output power level of 0dBm for example. Tuning the digital control word would result in PAE of approximately 10% while tuning the supply voltage would result in a much better PAE of 34%.



(a)

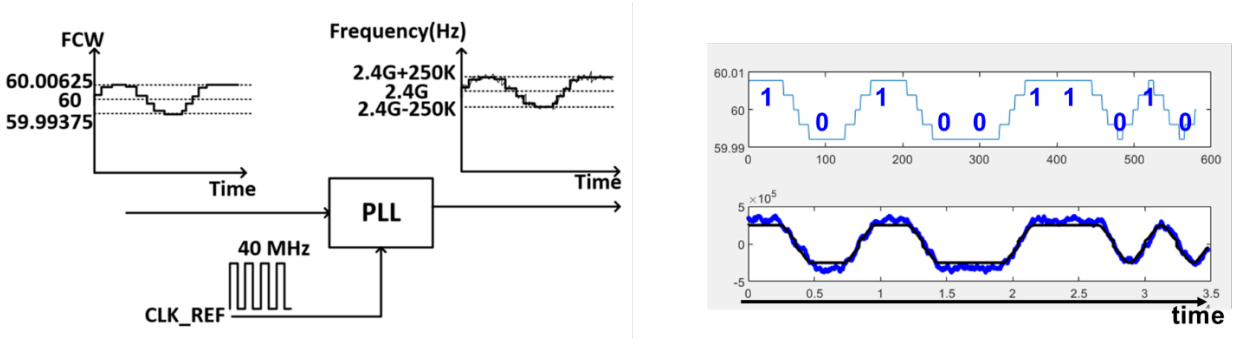


(b)

Figure 5.5 Pout and PAE of the SCPA while tuning (a) digital control word and (b) supply voltage.

5.4 RO-Based ADPLL

This part is designed by another student, Kyumin Kwon. A fully-synthesizable RO-based all-digital PLL (ADPLL) is designed to satisfy the BLE standard requirements. The BLE transmission utilizes GFSK modulation with $\Delta f = 500\,KHz$, $fcenter = 2.4 - 2.4835GHz$. Fractional-N operation is required to achieve $f_{data=1} - f_{data=0} = 500KHz$. Assuming a reference clock of 40MHz, the frequency control word range will be $FCW = 60.00625$ $(data = 1)$ and 59.99375 $(data = 0)$ as explained in Fig. 5.6. The PLL bandwidth is designed based on the 8X over sampled BLE symbol duration of 1Mbps (125nsec).



(a) (b)

Figure 5.6 (a) PLL functional block diagram and (b) Matlab behavioral simulation results.

Two major challenges are represented in achieving the fine time resolution for the time-to-delay converter (TDC, captures the phase/frequency error) circuit as well as the fine frequency resolution of the digitally-controlled oscillator (DCO) to generate the small frequency deviation without excess spurious tones. To compensate the large quantization error coming from the embedded-TDC, a delay-line TDC ($\Delta t_{TDC} = 6ps$, equivalent to 60stg embedded TDC) is added as a fine TDC while using the embedded-TDC ($\Delta t_{TDC} = \frac{T_{DCO}}{2N_{stg}}$) as a coarse one as shown in the architecture in Fig. 5.7. This topology can achieve both small quantization noise and wide input

time range without using a large number of stages for the delay-line TDC. For instance, if a delay-line TDC with time resolution of 10ps was designed to achieve the time range of a single period of the DCO (410ps), a delay line of 41 stages is required, which not only consumes significant area and power, but is also more vulnerable to non-linearity. When embedded-TDC is used alone, deterministic jitter due to large quantization error will cause a degradation of the performance. Using python scripts, placements of TDC cells are automatically generated to follow a certain pattern to minimize delay mismatches.

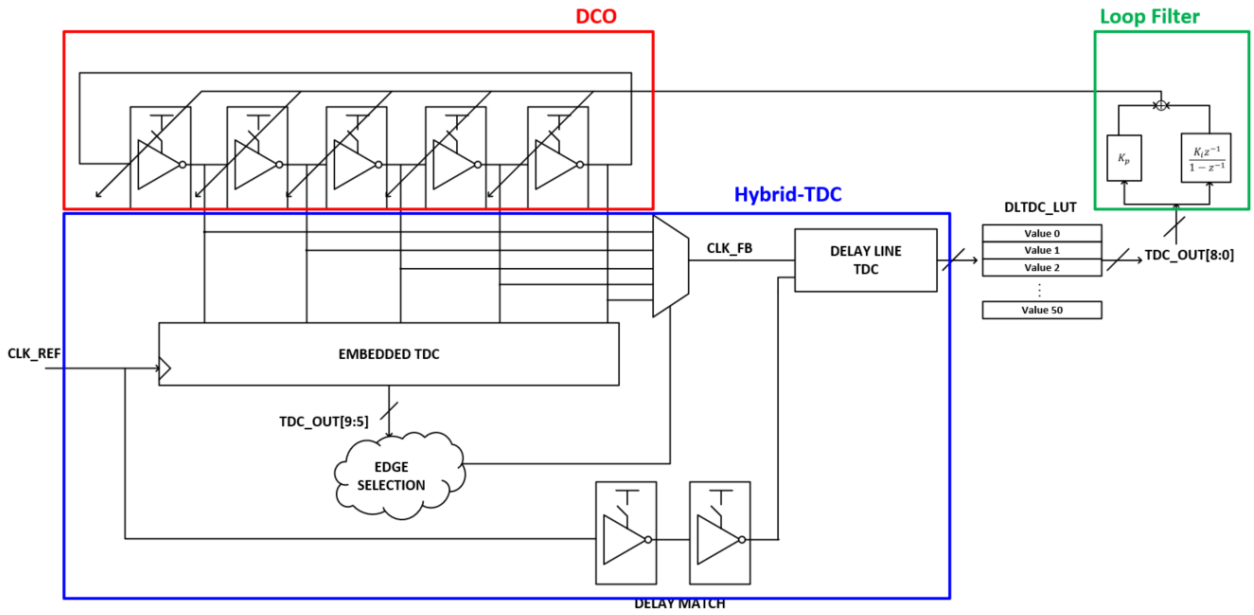


Figure 5.7 Schematic of the proposed ADPLL.

Figure 5.8 shows the Matlab behavioral simulation results, comparing the BLE performance between embedded-TDC and hybrid-TDC. Spurious tones are significantly reduced, and the eye-diagram is much clearer; satisfying the BLE specifications.

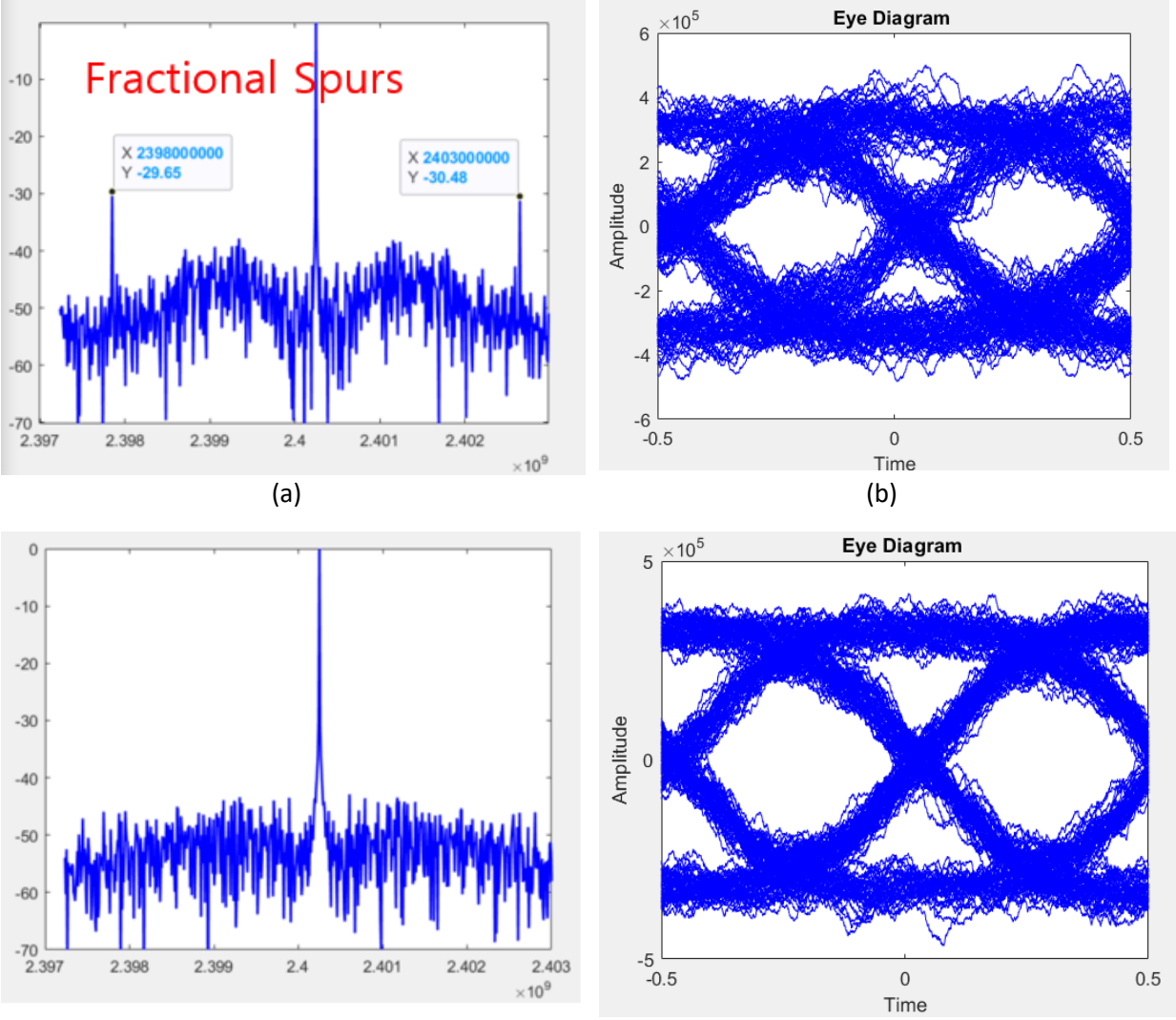


Figure 5.8 Matlab behavioral simulation results. (a) and (b) are the results with only embedded TDC. (c) and (d) are the results with the hybrid-TDC.

The fractional-N (FCW = 60.025) performance of the PLL calculated from Matlab behavior model with post-layout extracted analog blocks (TDC, DCO) characteristics is shown in table 5.1. Phase noise plot is shown in Fig. 5.9.

Table 5.1 Summary of the Fully-Synthesizable ADPLL Specifications

Specification	Value
Reference Frequency (MHz)	40
Output Frequency (GHz)	1.4 ~ 2.9
Rms Jitter when FCW = 60.025 (ps)	5.7
Power (mW)	4.2
FoM when FCW = 60+1/40 (dB)	-218

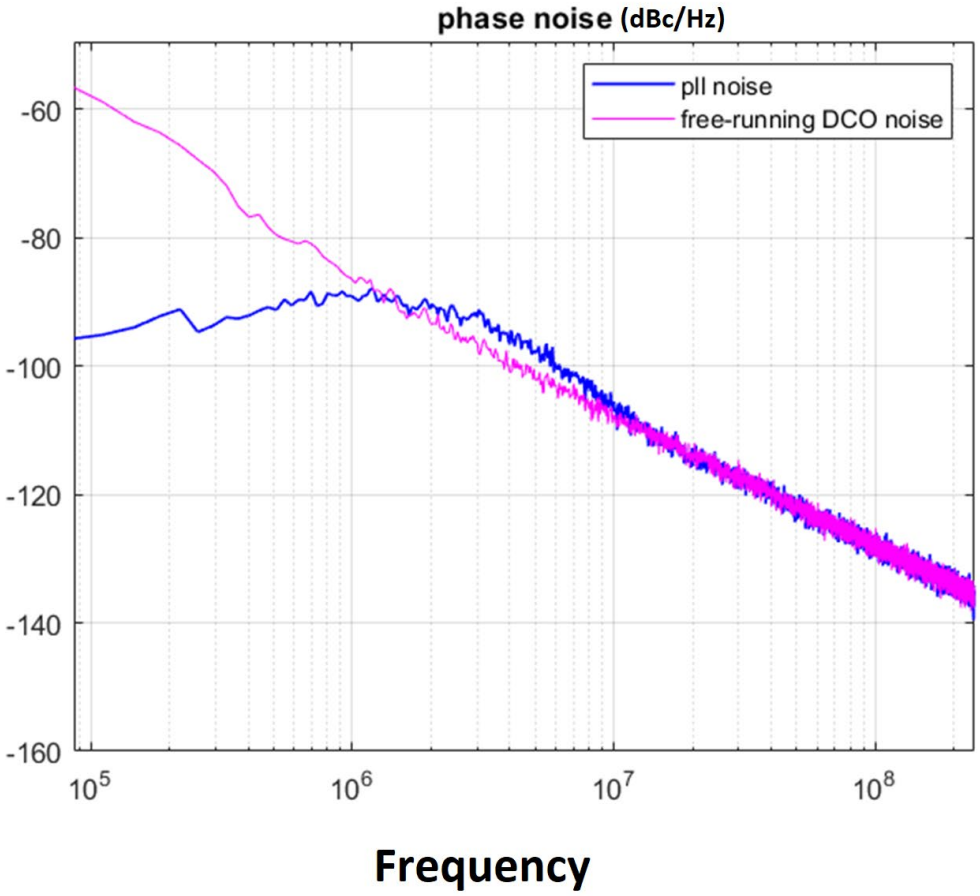


Figure 5.9 Phase noise plot of PLL with FCW = 60.025

5.5 Top Digital Controller

The finite state machine for the top digital controller is shown in Fig. 5.10. Different states are designed to allow both debugging and transmission modes. The FSM also supports single transmission mode or continuous transmission mode based on the application. The single transmission mode is important to allow duty-cycling for the BLE TX in order to reduce the average power consumption and energy-per-bit FOM; enabling its utilization in low-power IoT applications. The FSM is running at 8MHz frequency divided from the reference clock frequency (40MHz). A divide-by-5 block is implemented as 5-stage secondary FSM which generates a 8MHz clock with 40% duty cycle.

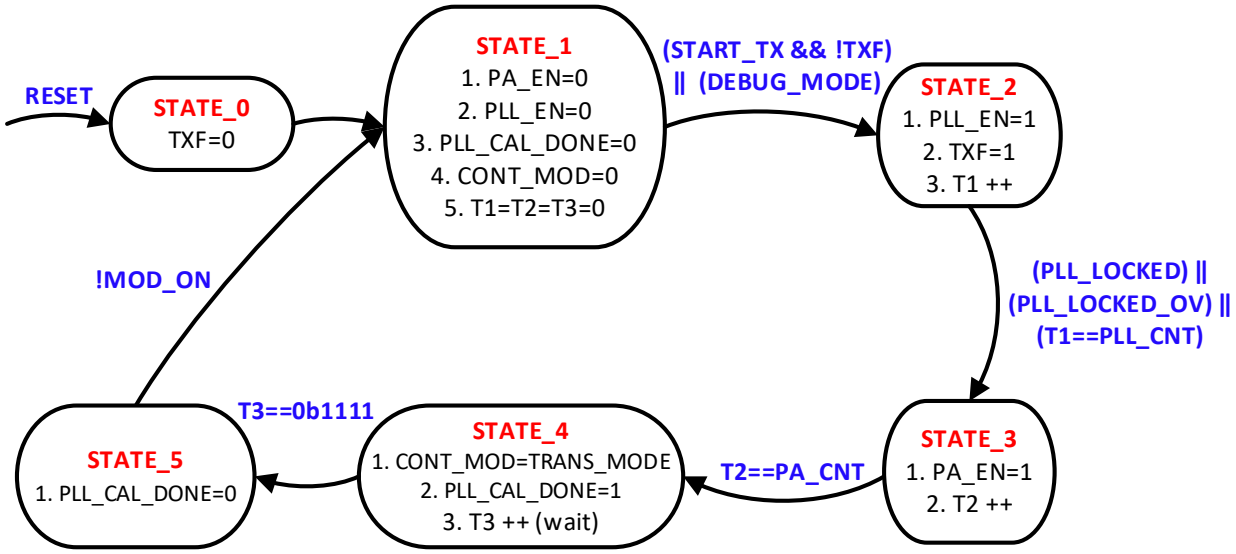


Figure 5.10 Implemented FSM for the top level controller.

The detailed description of the FSM is discussed below:

1. Once global reset is triggered, the FSM goes to STATE_0 and assigns the transmission flag in the SPI to low (TXF=0).

2. Then it forwards to STATE_1 where the PLL and SCPA are disabled along with other internal timers/counters (T1, T2 and T3) as well as PLL_CAL_DONE signal.

3. If either the start transmission (START_TX && !TXF) or debug mode (DEBUG_MODE) signals goes high, the FSM proceed to STATE_2 where it enables the PLL to start locking to the desired frequency, assign high to the TXF flag, and start the timer T1. The timer T1 is implemented to avoid the situation when the PLL is not able to lock to the desired frequency. If the PLL successfully locks to the desired frequency (PLL_LOCKED) or the timer T1 expires (T1=PLL_CNT), the FSM moves to STATE_3. An override PLL locking signal (PLL_LOCKED_OV) can be directly assigned through SPI for debugging purposes.

4. In STATE_3, the SCPA is enabled and timer 2 (T2) start counts to stall the FSM for a predefined number of cycles. The threshold count (PA_CNT) for time 2 (T2) is chosen long enough to stabilizes the PLL output frequency after the disturbance due to the loading effect of the SCPA when enabled.

5. When timer 2 (T2) expires, the FSM goes to STATE_4 where it passes the transmission mode (single or continuous) to the GFSK modulator. It also assign high to the PLL_CAL_DONE which is connected to the GFSK modulator block to start the transmission. The FSM then moves to STATE_5 after some delay (T3).

6. In STATE_5, the PLL_CAL_DONE is set to zero and the GFSK modulator start updating the FCW based on the data. After completing the packet transmission/s based on the transmission mode (MOD_ON signal), the FSM goes finally to the STATE_1 to disable the PLL and SCPA blocks and reset the internal timers.

The following waveforms (Fig. 5.11, 5.12, and 5.13) present the timing diagrams of the FSM control signals at different modes of operations:

I. Single Transmission:

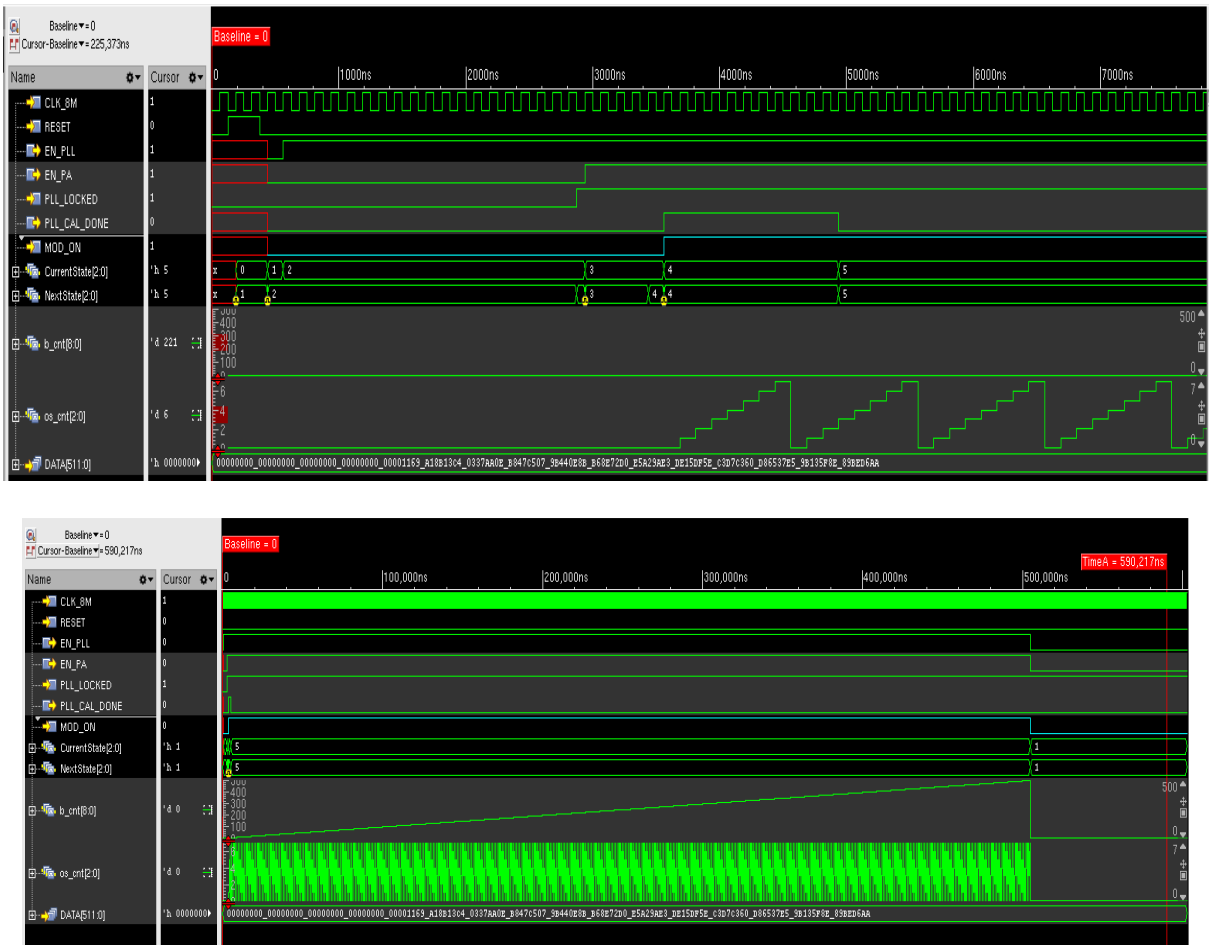


Figure 5.11 FSM timing diagram for single transmission mode.

II. Continuous Transmission

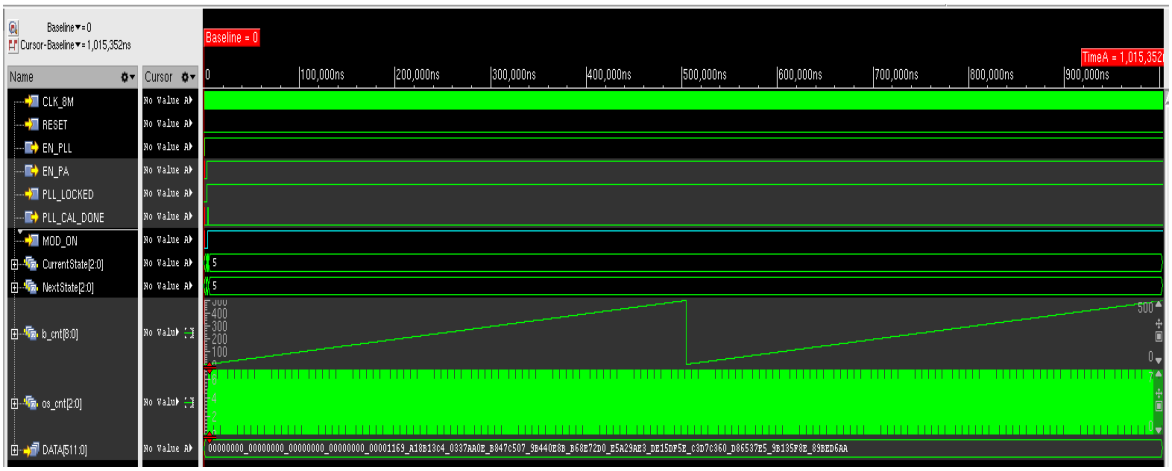


Figure 5.12 FSM timing diagram for continuous transmission mode.

III. Debugging Mode

Figure 5.13 FSM timing diagram for debugging mode.

5.6 Preliminarily Measurement Results

The die micrograph for the 2mm×2mm SoC chip is shown in Fig. 5.14. The BLE TX occupies an area of 0.4mm×0.6mm. The BLE TX top level integration is performed using the FASoC tool where the SCPA block is used as an auxiliary cell in the flow.

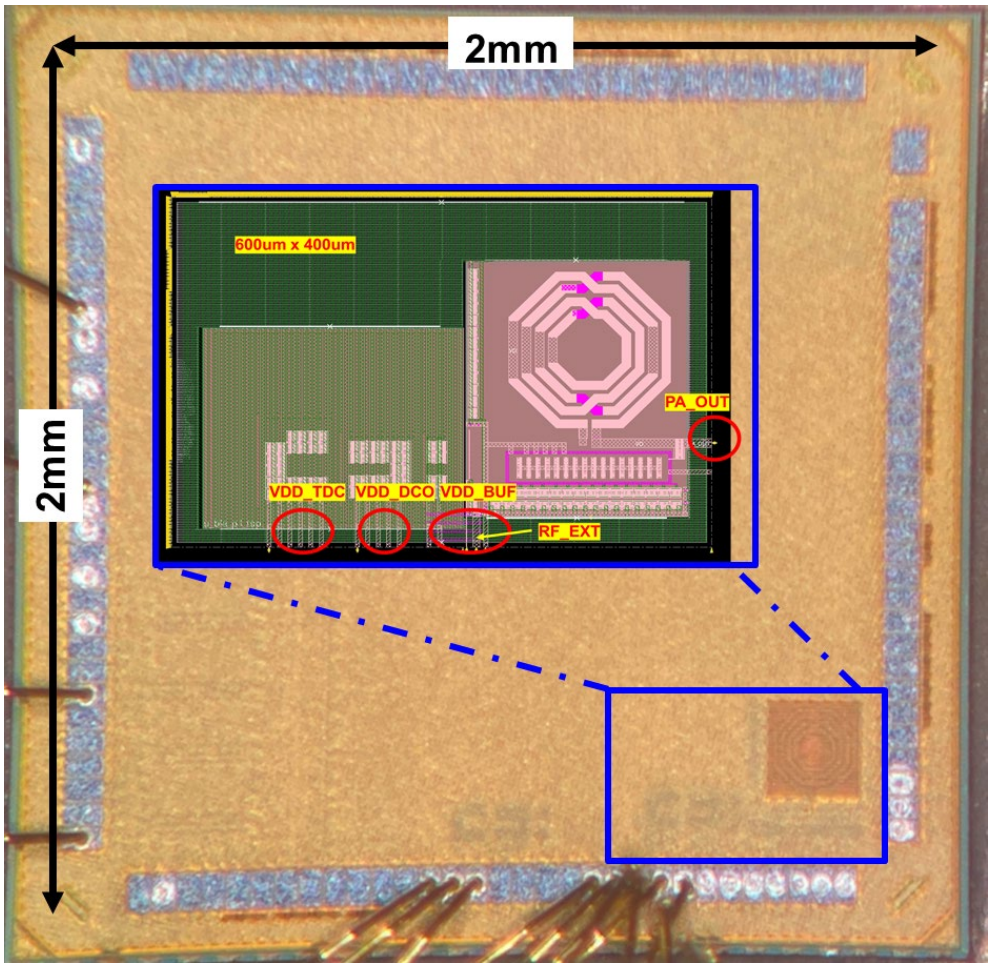
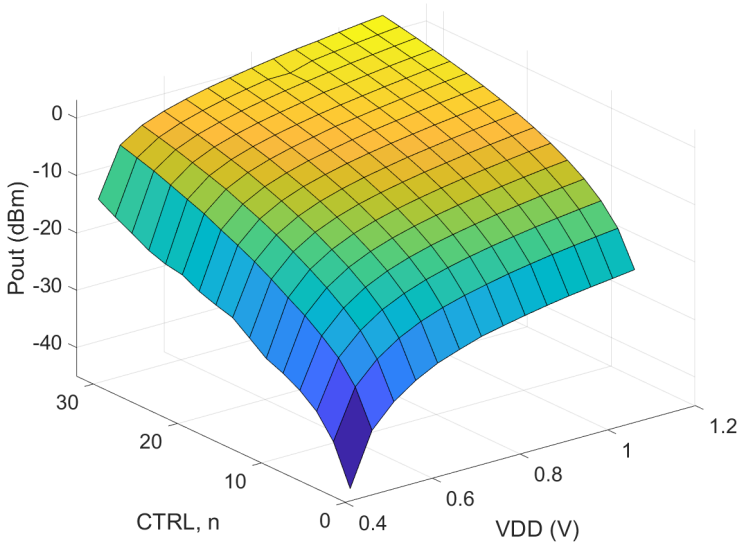


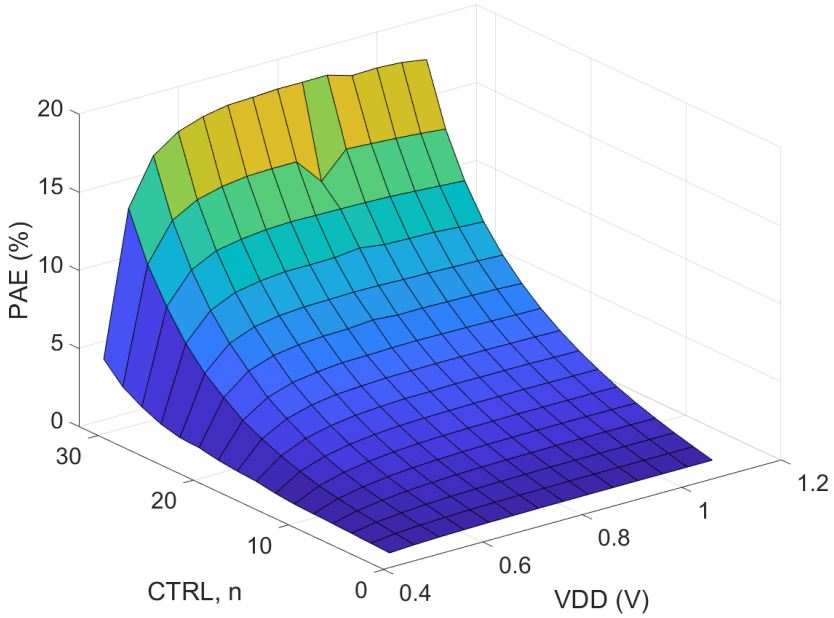
Figure 5.14 Die micrograph of the entire SoC chip.

The SCPA has been fully characterized in terms of output power and efficiency across the different digital control words and supply voltages as shown in Fig. 5.15. At nominal supply voltage (VDD=0.8V) and maximum CTRL (n=32), the output power is measured to be 0.8dBm instead of 4dBm in post-layout simulations. We refer that to the excess passive losses associated with the on-chip matching network as well as the capacitors bank. High output power levels can still be achieved by increasing the supply voltage but with lower PAE compared to the simulations. Figure 5.16(a) shows the Pout and PAE of the SCPA at the nominal supply voltage when sweeping the CTRL word while Fig. 5.16(b) shows the Pout and the PAE at the maximum CTRL word when

sweeping the supply voltage. It can be seen that sweeping the supply voltage has less impact on the PAE but with limited Pout's tuning range as discussed previously.

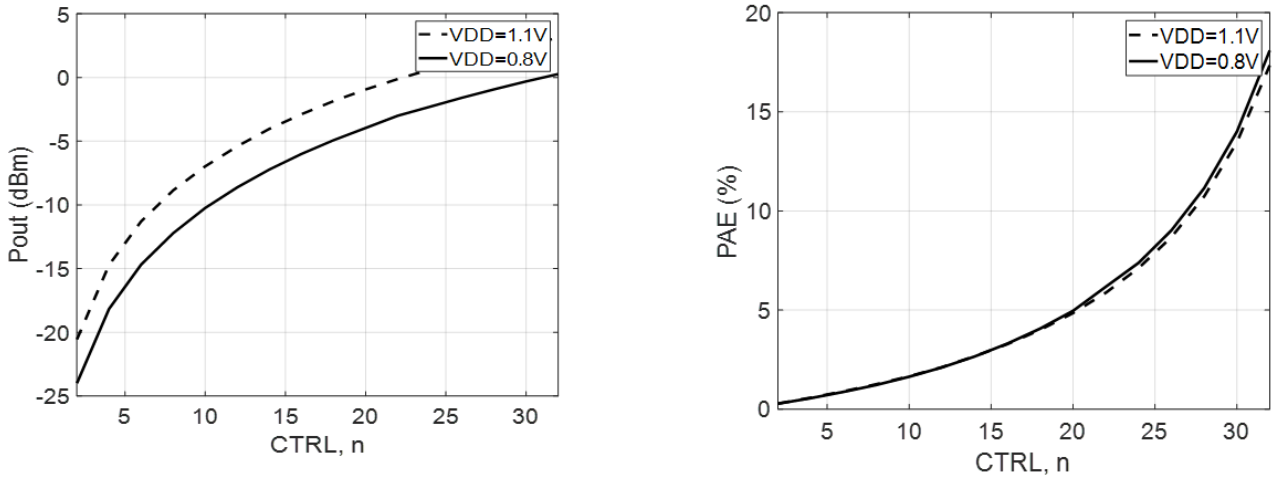


(a)

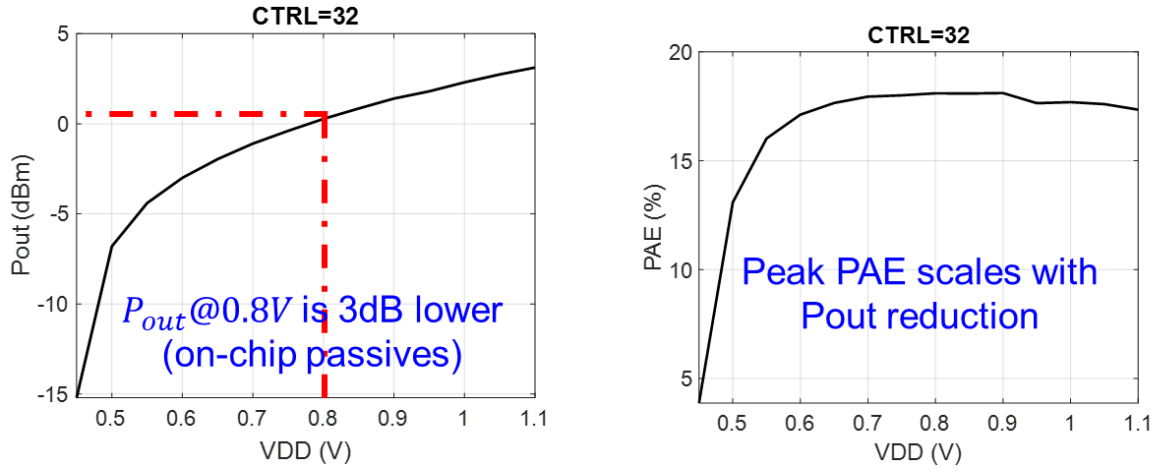


(b)

Figure 5.15 Measured (a) Pout and (b) PAE of the SCPA versus CTRL and VDD tuning schemes.



(a)



(b)

Figure 5.16 Measured Pout and PAE of the SCPA at (a) nominal supply voltage when sweeping the CTRL word, (b) the maximum CTRL word when sweeping the supply voltage.

The integer-N PLL operation has also been verified and the phase noise plot is shown in Fig. 5.17. The phase noise plot shows a PN of -87.5dBc/Hz at 1MHz offset which matches the post-layout simulations.

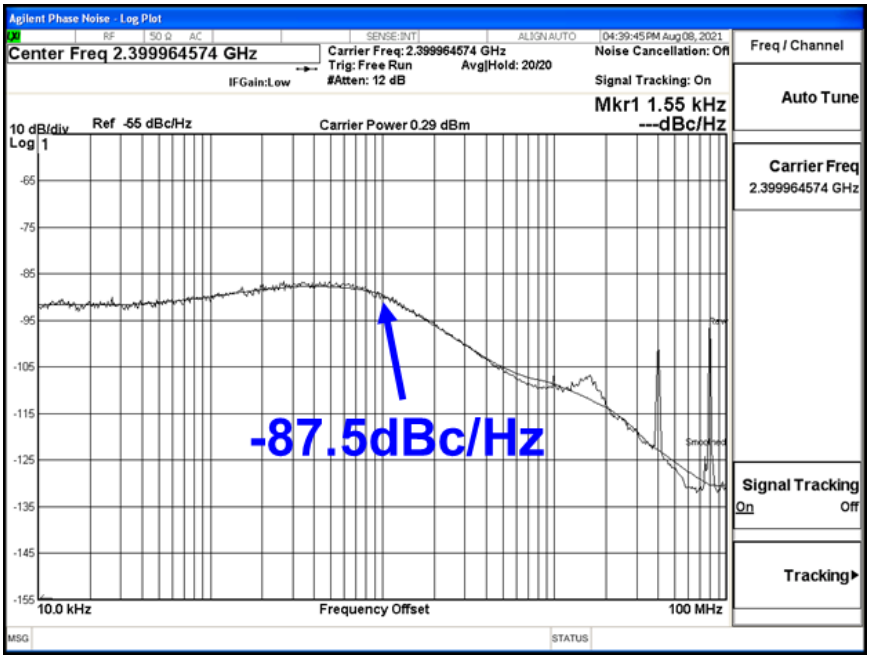


Figure 5.17 Measured phase noise of integer-N PLL.

5.7 Conclusion

In this chapter, a cell-based approach to design digital BLE-TX architectures is presented and fabricated in the GF12nm FinFET technology. The design approach is amenable to be fully-synthesized in the future work. The BLE TX compromises of three major building blocks: RO-based ADPLL, SCPA, and top FSM. The ADPLL design and the top level integration were fully-synthesized utilizing the FASoC framework. The custom designed SCPA achieves +1dBm maximum output power at the nominal supply voltage with PAE of 18%. The discrepancy between the measured and post-layout simulations are due to the excess losses in the on-chip passives which require extra careful consideration when designing and lay-outing the output matching network as well as the capacitors array.

Chapter 6

Position-Insensitive Wireless Power Transfer Based on Nonlinear Resonant Circuits

6.1 Introduction

NEAR-FIELD wireless power transfer (WPT) is an emerging technology that enables seamless, contactless electrical power transmission from microwatts to kilowatts power levels [128–130]. Near-field WPT technology utilizes time-varying electromagnetic (EM) fields to transfer energy between a charging pad (the transmitter) and a pick-up pad (the receiver) attached to an electronic device or a battery, either through magnetic field coupling (inductive WPT) [131–133] or electric field coupling (capacitive WPT) [134–136]. WPT technology has attracted much interest as it can deliver power conveniently without using power cords while maintaining the same performance as plug-in charging. Some applications that significantly benefit from wireless power transfer include the powering of biomedical implants, consumer electronics, robots, drones, and electric vehicles (EVs) [137]. Furthermore, WPT technology is expected to play an important role in the area of autonomous electric vehicles.

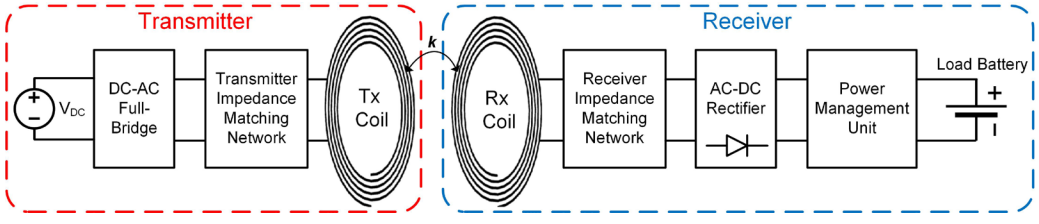


Figure 6.1 Typical block diagram of an inductively coupled WPT system.

The block diagram of a typical magnetic resonance WPT system is shown in Fig. 6.1. In such a system, the power source drives the transmit coil, while the secondary coil in the receiver captures the transmitted magnetic fields. Subsequently, the received RF energy is converted to direct current (dc) via a rectifier and regulated using a power management unit before it is delivered to a load, often a rechargeable battery.

In order to achieve high power transfer efficiency (PTE) at considerable transmission range in an inductively coupled WPT system, resonance based WPT circuits have been proposed since non-resonant inductive WPT is highly inefficient [138]. In such circuits, resonators with high loaded quality factors (Q) are utilized. An important figure of merit in such systems, namely PTE which is defined as

$$PTE = P_L/P_{av,S} \qquad (1)$$

where P_L is the power delivered to the load, and $P_{av,S}$ is the power available from the source. This definition for PTE considers both the source and the load matching, where $P_{av,S}$ is the maximum power that the source can provide under matched condition. Therefore, if the PTE is maintained as a function of the coupling factor, the output power delivered to the load also remains constant.

The strong dependence of the PTE in resonant-based WPT systems to the coupling factor between the transmit and receive coils is depicted in Fig. 6.2. The coupling factor is inversely proportional to the distance between the transmit and receive coils and the lateral/angular misalignment too [139]. At the optimum transmission distance, the transmit and receive coils are critically coupled and the load impedance is matched to the source impedance in order to satisfy the maximum power transfer condition. Hence, PTE is maximized when the resonant coils are critically coupled at the desired operating frequency. If the distance between the two coils is

increased, the coupling factor decreases below the critical coupling value (the under-coupled region). In this region, the optimum frequency of operation remains the same, yet the PTE drops exponentially, as shown in Fig. 6.2. Conversely, at shorter distances, as the coupling factor increases above the critical coupling factor (the over-coupled region), a phenomenon known as frequency split occurs [140]. In this case, a high PTE can still be achieved but at two different frequencies away from the original operating frequency. Therefore, resonant-based inductively coupled WPT systems are prone to a significant PTE degradation as coupling factor varies.

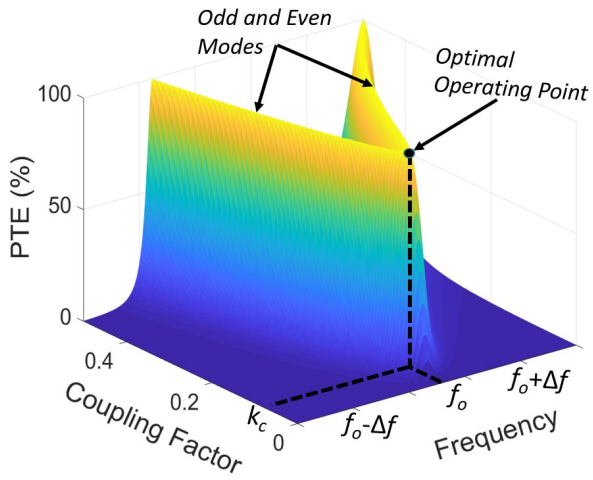


Figure 6.2 PTE vs. operating frequency and coupling factor presenting the frequency splitting phenomenon for the conventional linear WPT systems.

In the real world, it is difficult to accurately control the distance and alignment between the transmitter and receiver in most WPT applications. For example, in electric vehicle charging, the driver has to park directly over the charging pad at an exact position due to the intolerance of WPT systems to misalignment. Although ground-viewing cameras and other parking assist systems have been proposed to help the driver to accurately park over the charging pad (e.g. the BMW 530e iPerformance wireless charging system, 2018), such systems are complex, costly, and not infallible. Moreover, different classes of EVs require customized charging pad design due to

varying tire sizes and ground clearance. In dynamic charging scenarios, power is transferred to EV while driving over an array of transmitters, it is essential to maintain high PTE as the vehicle travels over the charging pads. Another example is the biomedical applications, where a high degree of reliability is important and the WPT performance must be maintained regardless of any misalignment between the transmit and receive coils. Additionally, in practical systems, the resonance frequencies of the resonators are affected due to environmental conditions, coupling to the nearby objects and component aging, hence degrading WPT power transmission efficiency. Therefore, practical WPT systems must be tolerant to coupling factor variation.

Several methods have been reported to improve the performance of near-field WPT systems [141–155]. It has been proposed in [143] to track one of the bifurcated modes (even and odd modes) in the over-coupled region by adjusting the source frequency in order to maintain high PTE. However, the frequency tracking range of this method is limited by the regulations of the Federal Communications Commission (FCC) regarding the allowable bands allocated for the WPT, mainly the Industrial, Scientific, and Medical (ISM) bands [144]. Therefore, this method cannot fully track the coupling factor variation within the entire over-coupled region. In addition, tunable matching circuits and switchable capacitor arrays [145–148] are proposed. However, the optimum impedance for maximum PTE varies drastically over distance, potentially making the impedance matching range unreasonable (high impedance matching range results in higher losses) and limiting the effective transmission distance [142]. Techniques of adjusting the coupling between multiple resonant loops [149–151], utilizing non-identical resonant coils [152], and using antiparallel resonant loops [153] are also introduced. Nevertheless, the extension of the transmission range provided by those techniques is limited due to the weak coupling factor. Thus-far, most of the approaches reported in the literature require sensing circuits and employ active

feedback/control circuitry to adjust the circuit optimum operating point at each coupling factor. Therefore, these approaches are generally complex, increase systems' cost and size, and consume some overhead power for their operation. In [154], an alternative method is proposed where the RF power source is replaced by a parity–time symmetric circuit incorporating a nonlinear gain saturation element. However, the circuit's operating frequency varies as a function of the coupling factor, resembling the same drawback of the frequency tuning method. On the other hand, [155] proposes the combination between the electric and magnetic coupling to suppress the frequency splitting phenomenon. However, the variation in the power delivered to the load is significant and the structure of the proposed resonators is complex.

In this paper, a novel, self-adaptive nonlinear resonant based WPT circuits are introduced to maintain high PTE as the coupling factor varies within the over-coupled region by suppressing the frequency splitting phenomenon. The presented technique automatically adjusts the resonance frequencies of the coupled nonlinear resonators at each coupling factor between the transmit and receive coils without the need to adjust the source frequency, utilize active feedback/control circuits, or employ tunable impedance matching networks. The presented self-adaptive mechanism is accomplished by utilizing off-the-shelf passive nonlinear devices in the design of the WPT and energy harvesting circuits [156–160]. This work is distinguishable from [160] by presenting a general discussion of the duffing-type resonant circuits' properties, the working principle of the proposed position-insensitive WPT circuit, the nonlinear WPT circuit's modeling and analysis as well as the measurement setup and the experimental results of a 60 W WPT circuit prototype. The circuit employs a nonlinear resonant circuit at the receiver and exhibits a near-constant PTE of approximately 86% over a ±10 cm transmission distance variation from the desired transmission range.

The chapter is organized as follows: the theoretical background and properties of the Duffing-type nonlinear resonant circuits are discussed in Section II. The principle of operation and analysis for the position-insensitive nonlinear resonant-based WPT circuits are described in Section III. The implementation and measurement results are presented in Section IV.

6.2 Theory and properties of electrical nonlinear resonant circuits

The principle of operation for the position- insensitive WPT circuits relies on the behavior of a specific class of nonlinear resonant circuits known as Duffing resonators. In this section the unique characteristics of the forced harmonic oscillation of a nonlinear resonator described by a nonlinear differential equation referred to as Duffing Equation are discussed. The Duffing equation is used to characterize the mechanical resonances/oscillations with a nonlinear restoring force [161]. The basic form of the Duffing equation is given by,

$$\ddot{x} + 2\gamma\dot{x} + \omega_o^2\, x + \epsilon x^3 = Fcos(\omega t) \qquad (2)$$

where x is the displacement, γ is the damping coefficient, ω_o is the oscillation frequency, ϵ is the third order nonlinearity coefficient, and $Fcos(\omega t)$ is the excitation force. The steady state solution of (2) can be approximated as $x(\omega, t) = X\, cos(\omega t - \theta)$, where X represents the amplitude, and θ represents the phase shift relative to the excitation signal [162]. The nonlinear resonators described by the Duffing equation demonstrate several important and unique properties that have been investigated in a number of fields including mathematics, physics, and mechanical engineering. The electrical representation of the Duffing-type nonlinear electrical resonator has been developed for the first time in [159] for wireless power harvesting applications to enhance the bandwidth of High-Q resonant circuits.

The basic schematic of a magnetically coupled nonlinear resonant-based WPT circuit described in this chapter is shown in Fig. 6.3(a). The resonant circuit in the transmitter (primary circuit) is linear and driven by a sinusoidal voltage source $v_s(t) = V_s\, cos(\omega_s t)$, while the secondary resonator at the receiver side is nonlinear. In order to study the overall circuit behavior, an equivalent nonlinear RLC series resonant circuit with the same characteristics can be developed by referring the transmitter circuit to the receiver side as shown in Fig. 6.3(b). The basic series nonlinear electrical resonator is comprised of an inductor, a resistor, and a nonlinear capacitor, $C(v)$. The resonant circuit is driven by a sinusoidal voltage source $v_s\ (t) = V_s\ cos(\omega_s t)$. The C-V relationship of the nonlinear capacitor is symmetric (even function of voltage), i.e. $C(v_C) = C(-v_C)$, which can be either bell-shaped (Fig. 6.3(c)) or well-shaped (Fig. 6.3(d)). In general, a nonlinear inductor can also be used to provide the required nonlinearity. In this case, the nonlinear inductor's inductance must be an even function of the current.

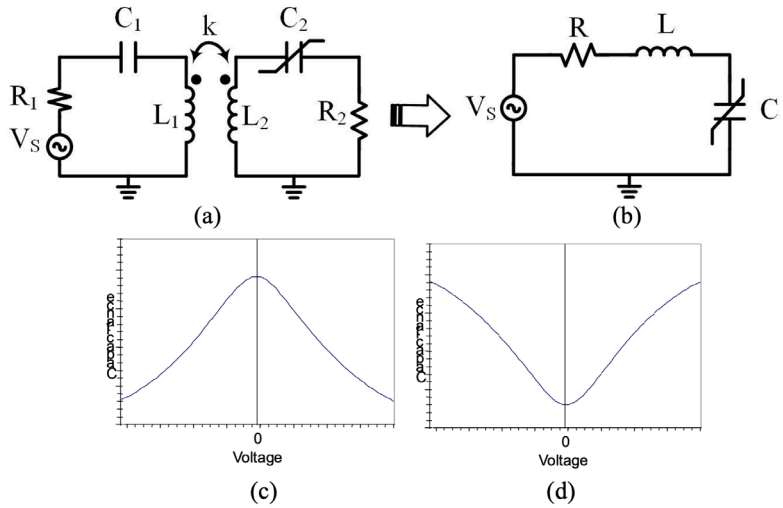


Figure 6.3 (a) Nonlinear resonant-based inductively coupled WPT circuit, (b) equivalent single nonlinear series resonance circuit, (c) symmetrical bell-shaped C-V curve, and (d) symmetrical well-shaped C-V curve.

The time domain dynamic equation describing the behavior of the nonlinear series RLC resonant circuit can be obtained by applying the Kirchhoff voltage law (KVL) and with the use of $i = dq\ /\ dt$:

$$v_c(t) + R\frac{dq_c}{dt} + L\frac{d^2\ q_c}{dt^2} = v_s(t) \qquad (3)$$

where $v_s(t) = V_S cos(\omega_S t)$ is the excitation voltage, $v_c(t)$ is the voltage across the nonlinear capacitor, and $q_c(t)$ is the amount of charge stored in the nonlinear capacitor. In order to express the voltage across the nonlinear capacitor in terms of charge q_c, the fundamental relationship between the voltage, current, and charge of the for a nonlinear capacitor is applied as follows,

$$dq_c = C\ dv_c + v_c\ dC \qquad (4)$$

Thus, the total amount of stored charge during one cycle can be calculated by:

$$q_c = \int C\ dv_c + \int v_c\ dC = \int \left(C + v_c\frac{dC}{dv_c}\right) dv_c \qquad (5)$$

The symmetric bell-shape C-V response of the nonlinear capacitor is approximately expressed by a polynomial of order n with even order terms assuming weak nonlinearity,

$$C = c_o + c_2 v_c^2 + c_4 v_c^4 + c_6 v_c^6 + \cdots + c_n v_c^n \qquad (6)$$

The odd order coefficients can be negligible since the device is bilateral symmetric. This assumption was motivated by desire to express the differential equation governing the WPT circuit in the form of Duffing equation.

The voltage across the capacitor can be approximated with a truncated Taylor series, and by substituting (6) into (5), q_c can be written as:

$$q_c = \int \sum_{i=0}^{n(even)} (i+1) c_i v_c^i\ \ dv_c = \sum_{i=0}^{n(even)} c_i v_c^{i+1} \qquad (7)$$

Since q_c is an odd function of v_c, the even order terms in the Taylor expansion of (7) vanish. Consequently, v_c can be expressed in terms of q_c, while neglecting terms higher than the third order for simplicity, using the inverse Taylor expansion,

$$v_c = \frac{1}{a_1} q_c + \frac{1}{a_3} q_c^3 \qquad (8)$$

where $a_1 = c_o$ is the inverse of the linear coefficient and has a unit of C/V, and $a_3 = -c_o^4 c_2^{-1}$ is the inverse of the nonlinear coefficient with a unit of C^3/V. In general, a_1 and a_3 can be calculated from the capacitance-voltage relationship for any nonlinear capacitor. Substituting (8) into (3) results in:

$$\ddot{q_c} + \frac{R}{L}\dot{q_c} + \frac{1}{La_1} q_c + \frac{1}{La_3} q_c^3 = \frac{V_s}{L} cos(\omega t) \qquad (9)$$

Equation (9) has the same form as the Duffing equation described in (2). The equation can be solved using the method of multiple scales, and the steady-state frequency response can be written as a sinusoidal function as follows:

$$q_c(t) = Q_c \, cos(\omega t - \theta) \qquad (10)$$

where Q_c represents the amplitude of the stored charge in the nonlinear capacitor, and θ represents the phase difference relative to the excitation signal. Both the linear term, $(1/La_1)q_c$, and the nonlinear term, $(1/La_3)q_c^3$, contribute to the restoring force. Therefore, an equivalent linear capacitance C_{eff} can be defined to quantify the restoring force contributed by the 3rd order nonlinear term,

$$\int_0^{T/2} \frac{1}{La_3} q_c^3 \, dq_c = \int_0^{T/2} \frac{1}{LC_{eff}} q_c \, dq_c \qquad (11)$$

From (11), C_{eff} can be derived as:

$$c_{eff} = \frac{a_3}{\frac{3}{4}Q_c^2} \qquad (12)$$

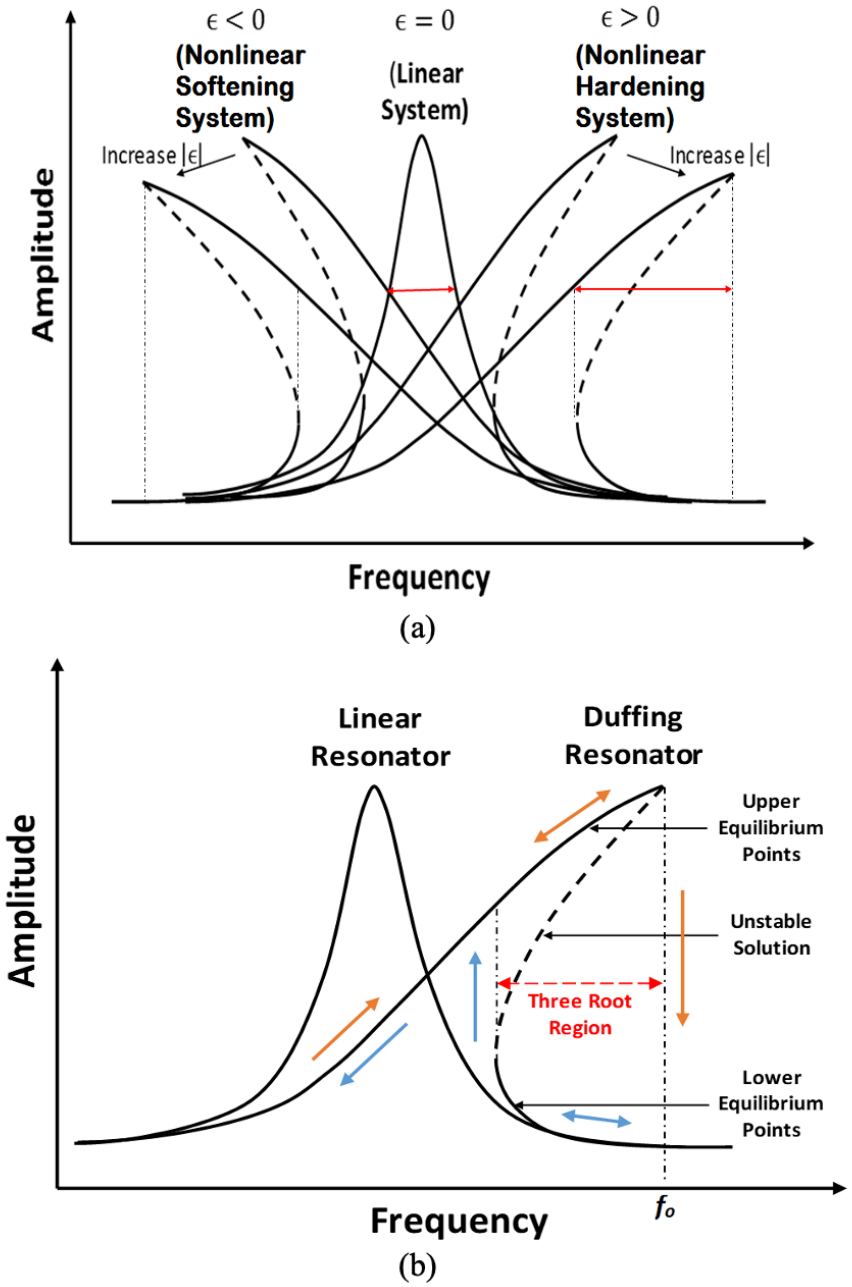


Figure 6.4 The amplitude-frequency response of: (a) a single resonator with different nonlinearity coefficient (ϵ), (b) Duffing resonator (red and blue arrows show the hysteresis loop and jump phenomenon).

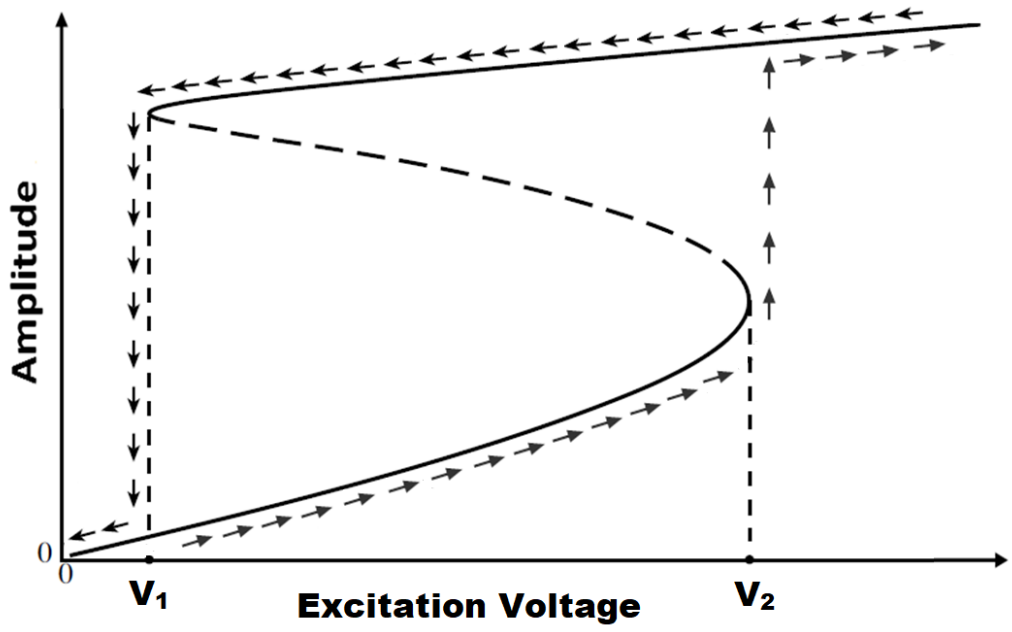


Figure 6.5 The resonance amplitude versus excitation amplitude response.

Hence, the resonance frequency of the resonator, ω_o, in the presence of nonlinear restoring term can be written as:

$$\omega_o = \sqrt{\frac{1}{L}\left(\frac{1}{a_1} + \frac{1}{C_{eff}}\right)} = \sqrt{\frac{1}{L}\left(\frac{1}{a_1} + \frac{\frac{3}{4}Q_c^2}{a_3}\right)} \qquad (13)$$

Equation (13) implies that the resonance frequency, ω_o, depends on the nonlinear capacitor charge amount (Q_c), which is function of the voltage (v_c). The circuit's amplitude-frequency relationship of (9) can be expressed in the frequency domain as,

$$(j\omega)^2 Q_C + \frac{R}{L}(j\omega)Q_C + \left(\frac{1}{La_1} + \frac{1}{LC_{eff}}\right)Q_C = \frac{V_s}{L} \qquad (14)$$

where

$$Q_C = Q_c e^{-j\theta} \qquad (15)$$

is the phasor form of $q_c(t)$. Substituting (12) and (15) into (14) yields,

$$Q_c^2\left(\frac{1}{La_1}+\frac{\frac{3}{4}Q_c^2}{La_3}-\omega^2\right)^2+\left(\frac{R}{L}Q_c^2\omega\right)^2=\left(\frac{V_s}{L}\right)^2 \quad (16)$$

After determining the amplitude of Q_c, the magnitude of current flowing in the nonlinear resonator is determined by,

$$I = j\omega Q_C \quad (17)$$

Hence, the average power delivered to the resistive load can be calculated as follows,

$$P_{avg} = \frac{1}{2}|I|^2R \quad (18)$$

Based on (16), the resonance amplitude (Q_c) as a function of the excitation frequency (frequency response) and the excitation magnitude (force response) can be determined. The multiple solutions of the resonance amplitude that satisfy (16) either at different frequencies (Fig. 6.4) or excitation amplitudes (Fig. 6.5) are calculated numerically and plotted using Matlab for an arbitrary nonlinear resonant circuit parameters, assuming weak nonlinearity. The goal of this section is to briefly discuss the behavior of the Duffing-type resonant circuits. This behavior is exploited in explaining the working principle of the proposed nonlinear-resonant-based WPT circuits. Therefore, the analytical details are not provided while referring to [161] for more details.

Fig. 6.4(a) shows the typical frequency response of a nonlinear duffing resonator. The peak of the resonator's frequency response is tilted to the right or left, resulting in an increased bandwidth as compared to a linear resonator having a similar quality factor. The tilt direction of the amplitude-frequency response is dependent on ϵ. Positive ϵ causes the curve to tilt to the right (hardening systems), and a negative ϵ causes the curve to tilt to the left (softening systems). Since the nonlinear capacitor with a bell-shaped C-V curve shown in Fig. 6.3(a) has a positive nonlinear term, a_3, resonators utilizing such a nonlinear capacitors will have a frequency response that is tilted to the right (higher frequency). The tilting characteristic results in a three-root region as

shown in Fig. 6.4(b). The region where there are three different solutions is called the bistable interval. The coexisting solutions forms the hysteresis where the trajectories initiated from different initial conditions can be attracted to different solutions. The stability of each solution can also be examined as illustrated in [161]. It can be proven that the medium solution points (represented by the dashed line) in this region are unstable, while the upper and lower points are stable and called equilibrium points [161]. As a result, the steady state solution of such a system converges to one of the two equilibrium solutions depending on the initial conditions. Moreover, the peak of the amplitude-frequency response can be predicted analytically [161]. In forced excitation of such resonators, like in WPT circuit described here, the source frequency is chosen to be at the same frequency of the highest resonance amplitude (denoted as f_o in Fig. 6.4(b)) allowing the maximum power to be delivered to the load.

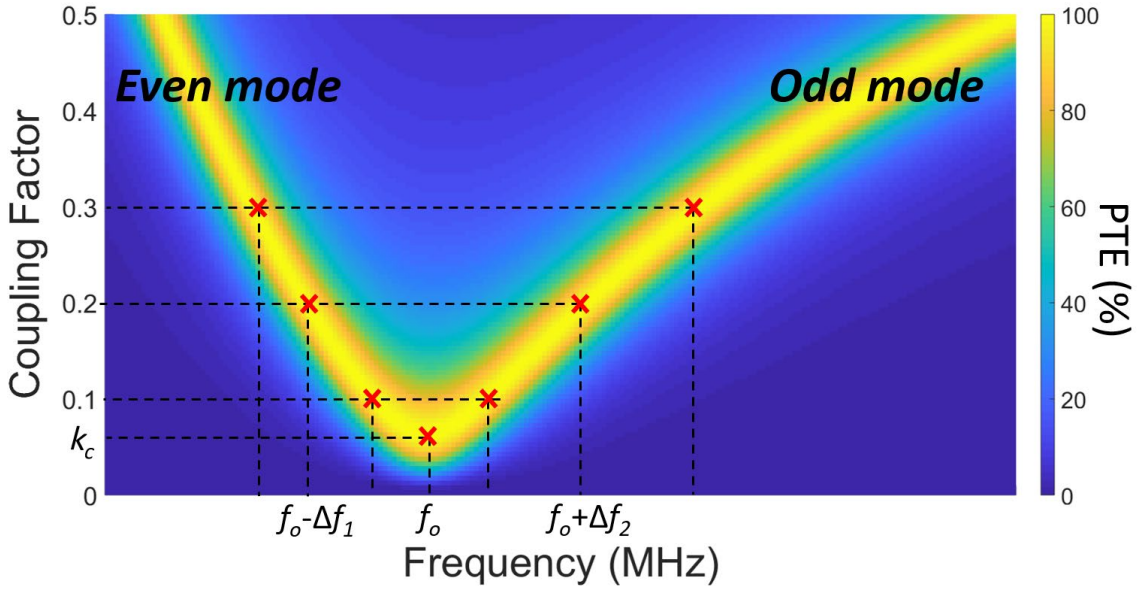


Figure 6.6 PTE vs. frequency and coupling factor (k), showing the optimum operating frequency at different coupling factors.

The resonance response amplitude as a function of the excitation amplitude (V_s) at the desired source frequency is depicted in Fig. 6.5. As can be seen, when V_s increases quasi-statically from $V_s = 0$, the resonance amplitude increases gradually and moves on the lower equilibrium branch. When V_s reaches V_2, a jump-up in the response to the upper equilibrium branch is occurred. If V_s is decreased, a jump-down occurs at $V_s = V_1$. In particular, there are three coexisting solutions for $V_1 < V_s < V_2$ (the solid and dashed lines correspond to stable and unstable branches, respectively). The unique force-response characteristic of Duffing nonlinear resonators is very important in understanding the working principle of the proposed position-insensitive WPT circuits described in this paper. Generally, two resonators are coupled in a WPT system to transfer the power from the source to the load. As the coupling factor between the transmit and receive coils is varied, the amount of energy coupled to the receiver varies correspondingly. This can be modeled by an equivalent excitation source at the receiver side having a variable excitation amplitude ($V_s'(k)$) which is a function of the coupling between the transmitter and receiver. By employing a nonlinear resonator at the receiver side, the resonance amplitude can be maintained at its peak value regardless of the variation in the amplitude of the equivalent excitation source at the receiver due to the hysteretic response shown in Fig. 6.5. Hence, high PTE values can be maintained as the coupling factor varies without tuning the operating frequency.

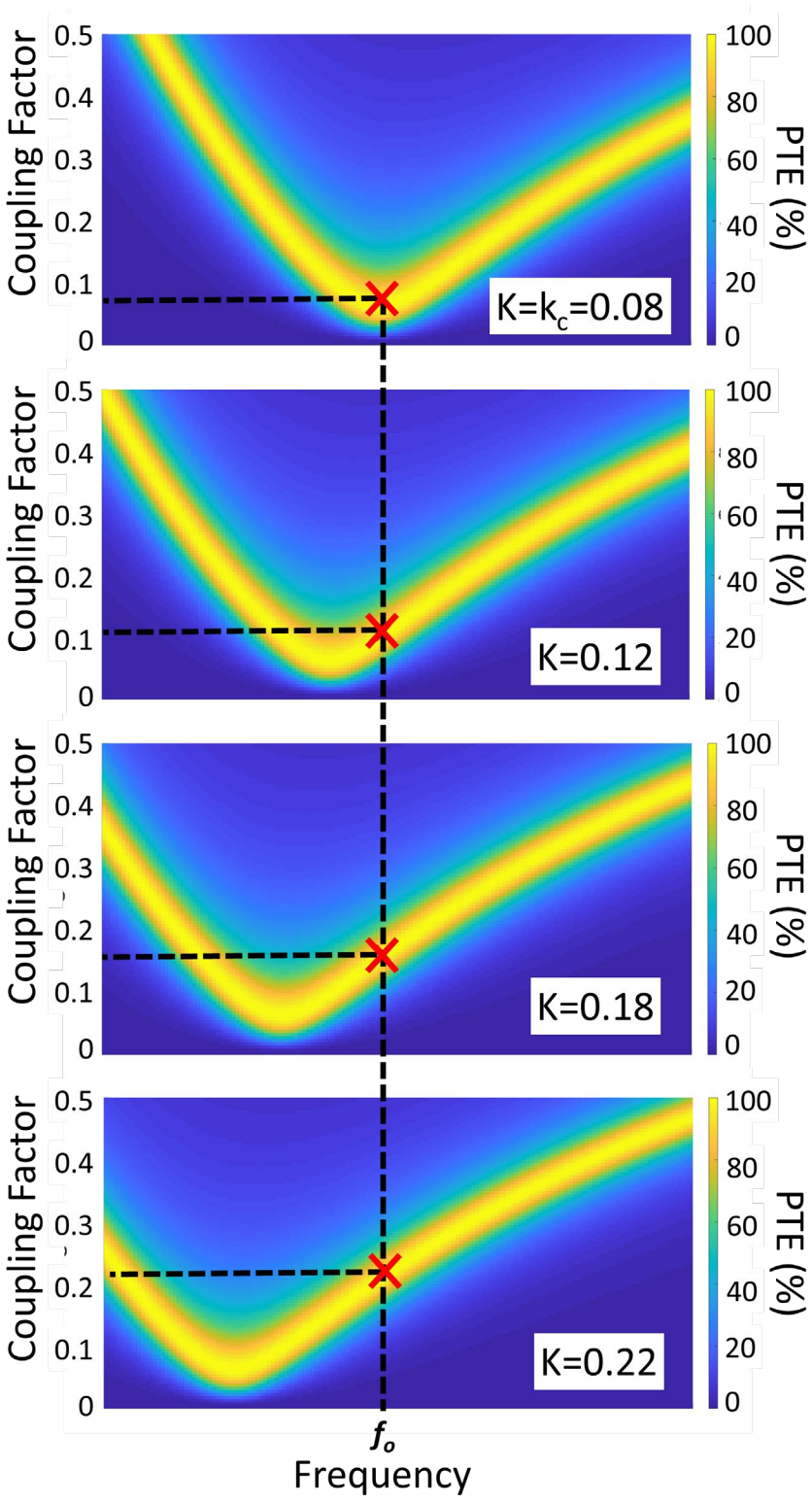


Figure 6.7 Multiple plots of the PTE vs. frequency and coupling factor (k), associated with the adjusted resonance frequencies at different coupling factors.

6.3 Principle of operation, analysis, and design of nonlinear resonant-based WPT circuits

The self-adaptive behavior of the nonlinear circuits described provide a novel solution to extend the transmission range of WPT systems over which the maximum PTE is maintained without varying the source frequency or employing any active feedback and control circuits. They provide a simple technique that allows a significant reduction in the sensitivity of WPT circuits to the variation of the coupling factor in real world operating conditions. In this section, the analysis, mathematical modeling, dynamical behavior, and the design methodology of the proposed nonlinear resonant-based WPT circuits are discussed.

Nonlinear resonant circuits are capable of adjusting their resonance frequencies based on the voltage amplitude across the nonlinear capacitors as can be seen from (13). Since the voltage amplitudes across the nonlinear capacitors in coupled nonlinear resonant circuits depend on the coupling factor, the resonance frequencies of the nonlinear resonators will be adjusted automatically based on the coupling factor. This self-adjustment characteristic is exploited to design the position-insensitive WPT circuit.

In this section, an arbitrary series-series WPT circuit, shown in Fig. 6.3, has been designed and simulated using the Advanced Design System (ADS) | Keysight simulator to generate the results shown in Fig. 6.6, 6.7, and 6.8. The scale of the frequency axis is normalized to the natural resonance frequency of the resonators, f_o, to generalize the discussion. The same simulation results and performance can be obtained for all different WPT circuit topologies at any operating frequency or power level based on the WPT application.

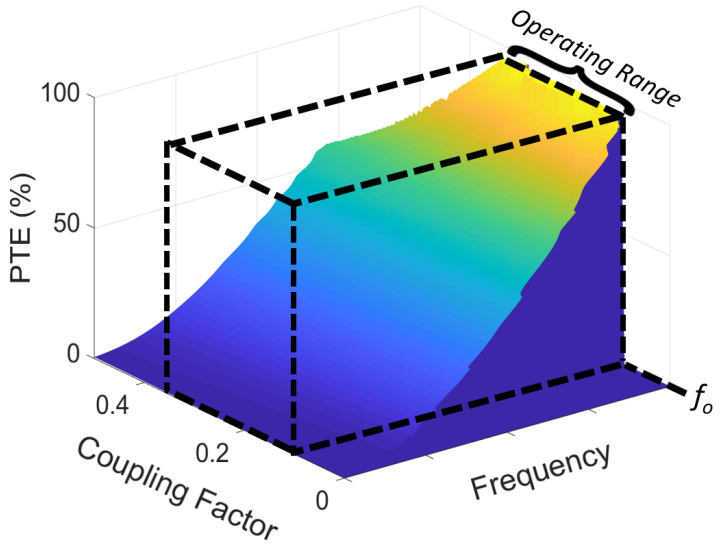


Figure 6.8 PTE vs. operating frequency and coupling factor for the presented nonlinear resonant-based WPT circuits.

6.3.1 Principle of Operation

In order to visualize the operation of the proposed nonlinear resonant-based WPT circuit, the 3D plot of the PTE versus the frequency and the coupling factor (k), shown in Fig. 6.2, is plotted in 2D as shown in Fig. 6.6 (represented by the V-shaped curves). This figure shows the behavior of a conventional WPT circuit designed to operate at a critical coupling factor (k_c) operating at an arbitrary operating frequency, f_o. The principle of operation of conventional frequency tracking approach that relies on adjusting the operating frequency at each coupling factor is also shown in Fig. 6.6. The operating frequency is adjusted to track the optimum frequency (either odd or even modes) within the over-coupled region in order to maintain the maximum power transfer efficiency as the coupling factor varies.

On the contrary, the nonlinear resonant WPT circuits presented in this chapter allow the circuit to maintain both the maximum power transfer and transfer efficiency at a fixed operating

frequency as the coupling factor between the transmitter and the receiver is varied. The principle of operation for the position-insensitive WPT circuit is shown in Fig. 6.7.

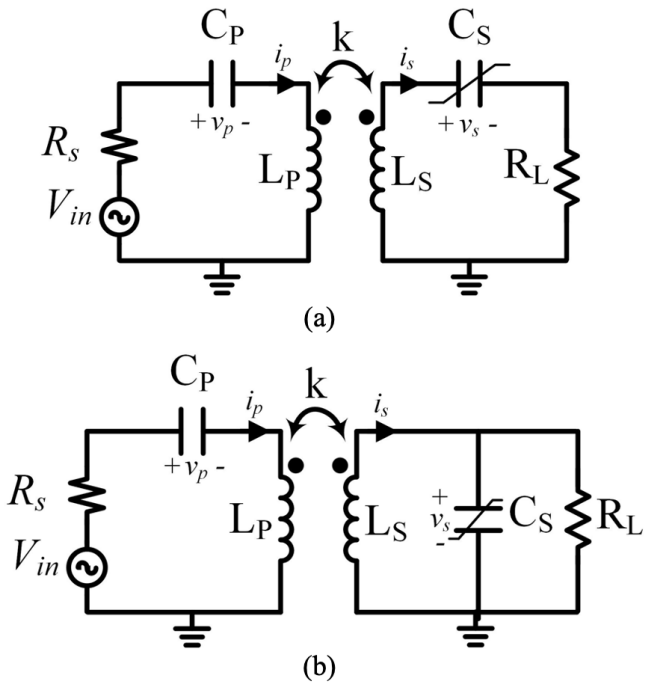


Figure 6.9 Circuit schematics of the nonlinear resonant-based WPT (a) Series-Series topology, and (b) Series-Parallel topology.

Multiple snapshots for shifted versions of the original V-shaped curve (shown in Fig. 6.6) at different coupling factors are plotted to demonstrate the operation of the nonlinear WPT circuits. The nonlinear WPT circuit's operation is visualized by sliding the position of the original V-shaped curve to lower or higher frequencies at each coupling factor such that a solution for maximum PTE exists at the same operating frequency. This can be achieved by tuning the values of the capacitors at each coupling factor.

This is achieved by utilizing a nonlinear resonant circuit which is capable of adjusting its resonance frequency automatically at each coupling factor since the voltage level across the

nonlinear capacitor is a function of the coupling factor. A capacitor with a bell-shaped nonlinearity is utilized in this example, resulting in shifting the V-shaped curves to lower frequencies. Therefore, the WPT circuit effectively "tracks" the odd mode frequency response of the original linear WPT circuit. This self-adaptation mechanism is general as both the even and odd modes can be tracked based on the type of the device nonlinearity. Furthermore, PTE of the nonlinear resonant-based WPT circuit is simulated versus the frequency and coupling factor as shown in Fig. 6.8. The linear capacitors in the conventional WPT circuit are replaced with anti-series connected varactors to demonstrate the performance of the proposed nonlinear-resonant-based WPT circuit. As can be seen, the frequency splitting phenomena due to non-optimal matching is suppressed. At the desired operating frequency (f_o), the simulated WPT system provides a constant PTE over a wide range of coupling factors, as represented by the region inside dashed box.

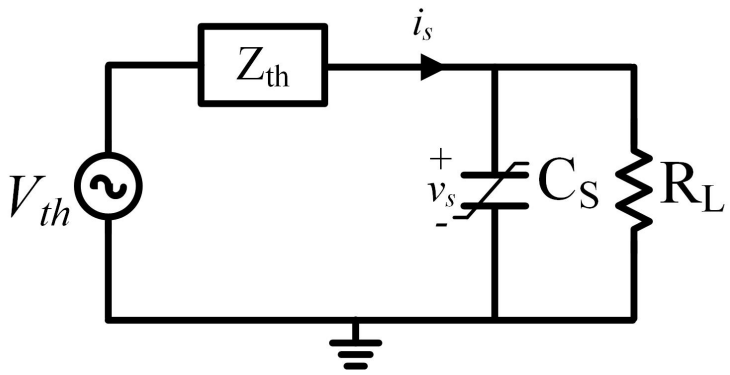


Figure 6.10 The equivalent single nonlinear resonator at the receiver side of the series-parallel topology.

The enhancement of the nonlinear resonance WPT circuit's tolerance to coupling factor variation can also be understood by representing the nonlinear resonator's operation as a negative feedback. When the distance between the two coils is reduced, the coupling factor increases and the voltages across the nonlinear capacitors decreases due to the non-optimal matching. Therefore,

the equivalent average capacitance (C_{eff}) increases. According to (13), the resonance frequency, ω_0, decreases which results in shifting of the V-shaped curve (Fig. 6.7) to a lower frequency allowing the maximum efficiency point to be tracked at the same desired frequency.

6.3.2 System Description and State-Space Modeling

The circuit schematics for series-series (SS) and series-parallel (SP) topologies of a resonant-based WPT circuit are shown in Fig. 6.9(a) and Fig. 6.9(b), respectively. The circuits' parameters are designed in order to provide resonant periodic waveforms of state variables namely, inductors' currents and capacitors' voltages. Application of the Kirchhoff's voltage law to the SS circuit topology shown in Fig. 6.9(a) results in:

$$i_p R_s + v_p + L_p\, di_p/dt - M\, di_s/dt = v_{in} \qquad (19)$$

$$i_s R_l + v_s + L_s\, di_s/dt - M\, di_p/dt = 0 \qquad (20)$$

where i_p, i_s, v_s and v_p are the state variables of the resonant-based WPT circuit that stand for the inductor currents and the capacitors' voltages in the primary and secondary sides, respectively. L_p, L_s, C_p, and C_s are respectively the inductances and capacitances in the primary and secondary sides. R_s and R_l are the source and load resistances, respectively.

Thus, the system state equations which describe the instantaneous nonlinear dynamics can be obtained from (19), (20), and using the time domain voltage-current relationship for capacitors [163]. The state equations are given by:

$$\dot{v_p} = i_p/C_p \qquad (21)$$

$$\dot{v_s} = i_s/C_s \qquad (22)$$

$$\dot{i_p} = \left[L_s v_{in} - L_s v_p - M v_s - L_s R_s i_p - M R_l i_s\right]/\Delta \qquad (23)$$

$$\dot{i_s} = \left[M v_{in} - M v_p - L_p v_s - M R_s i_p - L_p R_l i_s\right]/\Delta \qquad (24)$$

where $\Delta = L_s L_P - M^2 = L_s L_P (1 - k^2)$.

Similarly, the system state equations for SP topology can be expressed by:

$$\dot{v_p} = i_p / C_p \tag{25}$$

$$\dot{v_s} = i_s / C_s - v_s / C_s R_l \tag{26}$$

$$\dot{\imath_p} = \left[L_s v_{in} - L_s v_p - M v_s - L_s R_s i_p \right] / \Delta \tag{27}$$

$$\dot{\imath_s} = \left[M v_{in} - M v_p - L_p v_s - M R_s i_p \right] / \Delta \tag{28}$$

Both topologies can be expressed by an equation of the form $\dot{x}(t) = Ax(t) + u(t)$, where

$$x(t) = \left[v_p(t) \quad v_s(t) \quad i_p(t) \quad i_s(t) \right]^T \tag{29}$$

$$u(t) = [0 \quad 0 \quad L_S/\Delta \quad M/\Delta]^T . v_{in}(t) \tag{30}$$

$$A_{SS} = \begin{bmatrix} 0 & 0 & \frac{1}{C_p} & 0 \\ 0 & 0 & 0 & \frac{1}{C_s} \\ \frac{-L_s}{\Delta} & \frac{-M}{\Delta} & \frac{-L_s R_s}{\Delta} & \frac{-M R_l}{\Delta} \\ \frac{-M}{\Delta} & \frac{-L_p}{\Delta} & \frac{-M R_s}{\Delta} & \frac{-L_p R_l}{\Delta} \end{bmatrix} \tag{31}$$

$$A_{SP} = \begin{bmatrix} 0 & 0 & \frac{1}{C_p} & 0 \\ 0 & \frac{-1}{C_s R_l} & 0 & \frac{1}{C_s} \\ \frac{-L_s}{\Delta} & \frac{-M}{\Delta} & \frac{-L_s R_s}{\Delta} & 0 \\ \frac{-M}{\Delta} & \frac{-L_p}{\Delta} & \frac{-M R_s}{\Delta} & 0 \end{bmatrix} \tag{32}$$

The parameters of the matrix A for both SS and SP circuit topologies are functions of the primary and secondary components. Thus, the equations that describe the dependence of the nonlinear devices (either capacitive or inductive) on the system's states can be evaluated and substituted into the matrix A. The solution for $x(t)$ starting from an initial time instant and an

initial state, x_0, can be expressed by using Euler's method to approximate the differential equations by discrete difference equations is given:

$$x(t+1) = (I + A.\Delta t)x(t) + u(t).\Delta t \qquad (33)$$

where I is the identity matrix. In this paper, we study the effect of employing a nonlinear capacitor at the secondary side, $C_s(v_s)$, upon the circuit's performance of the series-parallel topology.

6.3.3 Synthesizing the C-V Relationship for the Secondary Nonlinear Capacitor

Since the nonlinear device is employed at the receiver side, an equivalent single nonlinear resonant circuit is realized at the receiver circuit in order to simplify the determination of the required nonlinearity while reducing the simulation time. The primary and secondary inductors are assumed to be equal, $L_p = L_s = L$. The linear series resonant circuit at the primary side is reflected to the receiver side after the secondary inductor as shown in Fig. 6.10 by calculating the Thevenin Equivalent circuit as follows:

$$V_{th} = \frac{-\omega^2 C_p L k}{(1-\omega^2 L C_p)+j\omega C_p R_s} \times V_{in} \qquad (34)$$

$$Z_{th} = \frac{-\omega^2 C_p L R_s + j\omega L\left(1-\omega^2 L C_p(1-k^2)\right)}{(1-\omega^2 L C_p)+j\omega C_p R_s} \qquad (35)$$

Therefore, the real and imaginary parts of the Thevenin impedance can be expressed as:

$$Re\{Z_{th}\} = \frac{\omega^4 C_p^2 M^2 R_s}{(1-\omega^2 L C_p)^2+\omega^2 C_p^2 R_s^2} \qquad (36)$$

$$Im\{Z_{th}\} = \omega L - \frac{\omega^3 C_p M^2(\omega^2 L C_p - 1)}{(1-\omega^2 L C_p)^2+\omega^2 C_p^2 R_s^2} \qquad (37)$$

The resonance frequency of the primary resonator is designed to be the same as operating frequency, $\omega_{o,p} = 1/\sqrt{LC_p} = \omega$. Accordingly, (34), (36), and (37) expressions can be reduced to:

$$V_{th}(\omega = \omega_o) = jkQ_{l1}V_{in} \tag{38}$$

$$Re\{Z_{th}(\omega = \omega_o)\} = \frac{\omega^2 k^2 L^2}{R_s} = Q_{lp}^2 k^2 R_s \tag{39}$$

$$Im\{Z_{th}(\omega = \omega_o)\} = \omega L \tag{40}$$

where $Q_{lp} = \omega L_p/R_s$ is the loaded quality factor of the primary resonator. It can be seen that V_{th} is function of the coupling factor. The state-space modeling of the single equivalent resonant circuit hence can be evaluated as:

$$\begin{bmatrix} \dot{v_s} \\ \dot{i_s} \end{bmatrix} = \begin{bmatrix} -1/C_s(v_s)R_l & 1/C_s(v_s) \\ -1/L & -Q_{lp}^2 k^2 R_s/L \end{bmatrix} \begin{bmatrix} v_s \\ i_s \end{bmatrix} + \frac{k}{L} \begin{bmatrix} 0 \\ Q_{lp} \end{bmatrix} v_{in} \tag{41}$$

Finally, the power delivered to the load and the corresponding overall PTE can be calculated as

$$P_{out} = V_s^2/2R_l \tag{42}$$

$$PTE = P_{out}/P_{av} = \frac{V_s^2/2R_l}{V_{in}^2/8R_s} \tag{43}$$

Using (41) and (43), the C-V relationship of the nonlinear capacitor ($C_s(v_s)$) can be synthesized such that high PTE is maintained across the required coupling factor range. A search algorithm is utilized to optimize the design parameters for different types of nonlinear capacitors. For example, the anti-series varactor diodes' C-V equation can be given by:

$$C = \frac{C_{j0}}{\left(1-\frac{V_{j1}}{V_{bi}}\right)^{\gamma}} || \frac{C_{j0}}{\left(1-\frac{V_{j2}}{V_{bi}}\right)^{\gamma}} \tag{44}$$

where C_{j0} is the zero-bias junction capacitance, V_{j1} is the junction voltage across first diode, V_{j2} is the junction voltage across the second diode where $v_{j1} + v_{j2} = v_s$, V_{bi} is the built-in

potential, and γ is the grading coefficient. Thus, the design parameters are C_{j0} , V_j and γ. Alternatively, the nonlinear capacitor can be expressed by the following polynomial form:

$$C = C_0 + C_1 V + C_2 V^2 + C_3 V^3 \qquad (45)$$

where C_0, C_1, C_2, and C_3 are the optimization parameters. Using the aforementioned system analysis, the time domain transient and steady-state waveforms and the FFT spectra of the output power delivered to the load can be numerically simulated using Matlab. Fig. 6.11(a) shows the simulated transient response of the nonlinear WPT circuit, using the aforementioned analysis. A very small amount of overshooting is observed in the transient response which does not affect the operation of the circuit.

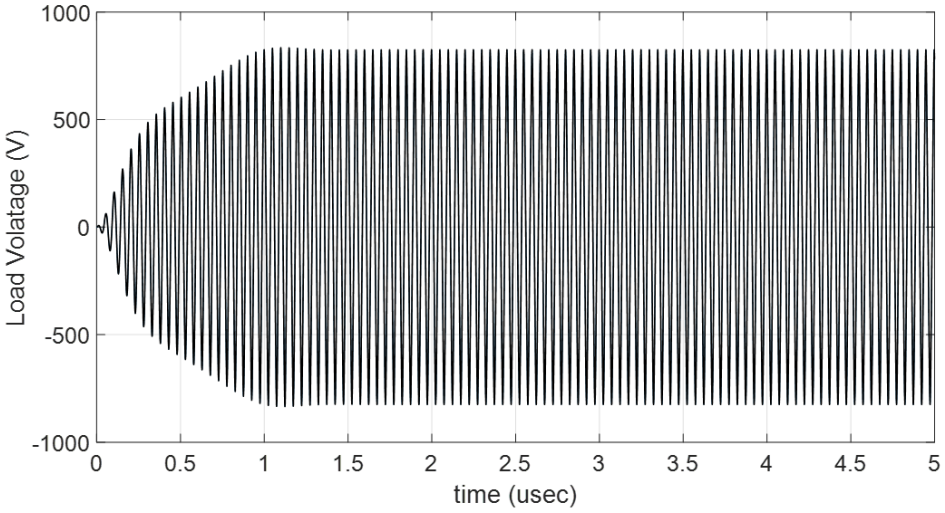


Figure 6.11 Simulated transient response of the voltage across a 5kΩ load resistance in the proposed nonlinear resonant-based WPT circuit at k=0.22. (The source available power is 60 W)

Based on the analysis provided in this section, the design methodology can be summarized in three steps. The first step is to design a linear WPT circuit to fulfil the required WPT circuit specifications in terms of operating frequency, targeted power level, desired transmission range, and load value. The second step is to determine the optimum nonlinearity required to maintain the

PTE over the desired range of coupling factor values. This is achieved through optimization tools in circuit simulators. Finally, the third step is to synthesize the required nonlinearity using through different combination of the available commercial nonlinear devices that can provide the proper nonlinearity while handling the targeted power levels. In the following section, the implementation and measurement results for the position-insensitive WPT circuit prototype is discussed in details".

6.4 Nonlinear WPT Circuit Implementation and experimental results

As a proof of concept, a WPT circuit employing a nonlinear resonator in the receiver side has been designed and implemented. The WPT primary circuit is capable of transmitting 60 W to a resistive load of 2.5 kΩ in the secondary circuit at 2.25 MHz. Initially, a 60 W conventional linear WPT reference circuit has been designed. The value of the load resistance was chosen based on the targeted critical coupling factor ($k_c = 0.14$) corresponding to a 25 cm transmission distance between the two coils used in this setup. Recalling that, $k_c = 1/\sqrt{Q_p Q_s}$ [131], where $Q_p = \omega_o L_p / R_{source}$ is the loaded quality factor of the primary series resonant circuit and $Q_s = R_{load}/\omega_o L_s$ is the loaded quality factor of the secondary parallel resonance circuit. Knowing the values of $k_c, Q_p, Q_s, L_p, L_s, R_{source}, and\ \omega_o$, the load value has been determined to be 2.5 kΩ. A real RF load resistor was used during the measurements while the light bulb with equivalent resistance, shown in Fig. 6.12(b), was used for the performance's demonstration purposes only [165]. While the load resistance value might seem very large, the proposed technique is generic and can be applied to design any WPT circuit with particular specifications including the load value. The circuit topology (i.e. the type of resonance, series or parallel) is decided based on the equivalent load impedance of the rechargeable battery.

The prototype was mounted on ball bearing sliders to allow for a smooth movement of the receiving coil with respect to the transmitting coil. It is noteworthy to point out that the circuit's power level and frequency can be scaled up and down to address the required specifications for different applications or to comply with a standard. In this experiment, series-parallel topology is utilized and the circuit schematic as well as the experiment setup employing a 2.5 kΩ load, are shown in Fig. 6.12(a) and 6.12(b), respectively. A signal generator is used to feed the transmitter's linear power amplifier (PA) and the output of the PA is then connected to the transmit circuit through a 1:1 balun. The available power from the power amplifier is 60 W (the maximum power level that PA can provide to a perfectly matched load at that frequency). A typical class-A RF power amplifier with an efficiency of ~30% is utilized in the experiment. The efficiency of the PA is not included in the reported PTE of the proposed WPT circuit. On the receiver side, the receive coil is connected in parallel with the passive nonlinear capacitor and the load resistor. The load resistor value is determined based on the loaded quality factor of the resonators required to satisfy the critical coupling factor. Both the transmit and receive coils have 5 turns with inner diameter of 25 cm, outer diameter of 40 cm, a pitch of 1 cm. Table 6.1 summarizes the component specifications for the implemented WPT circuit.

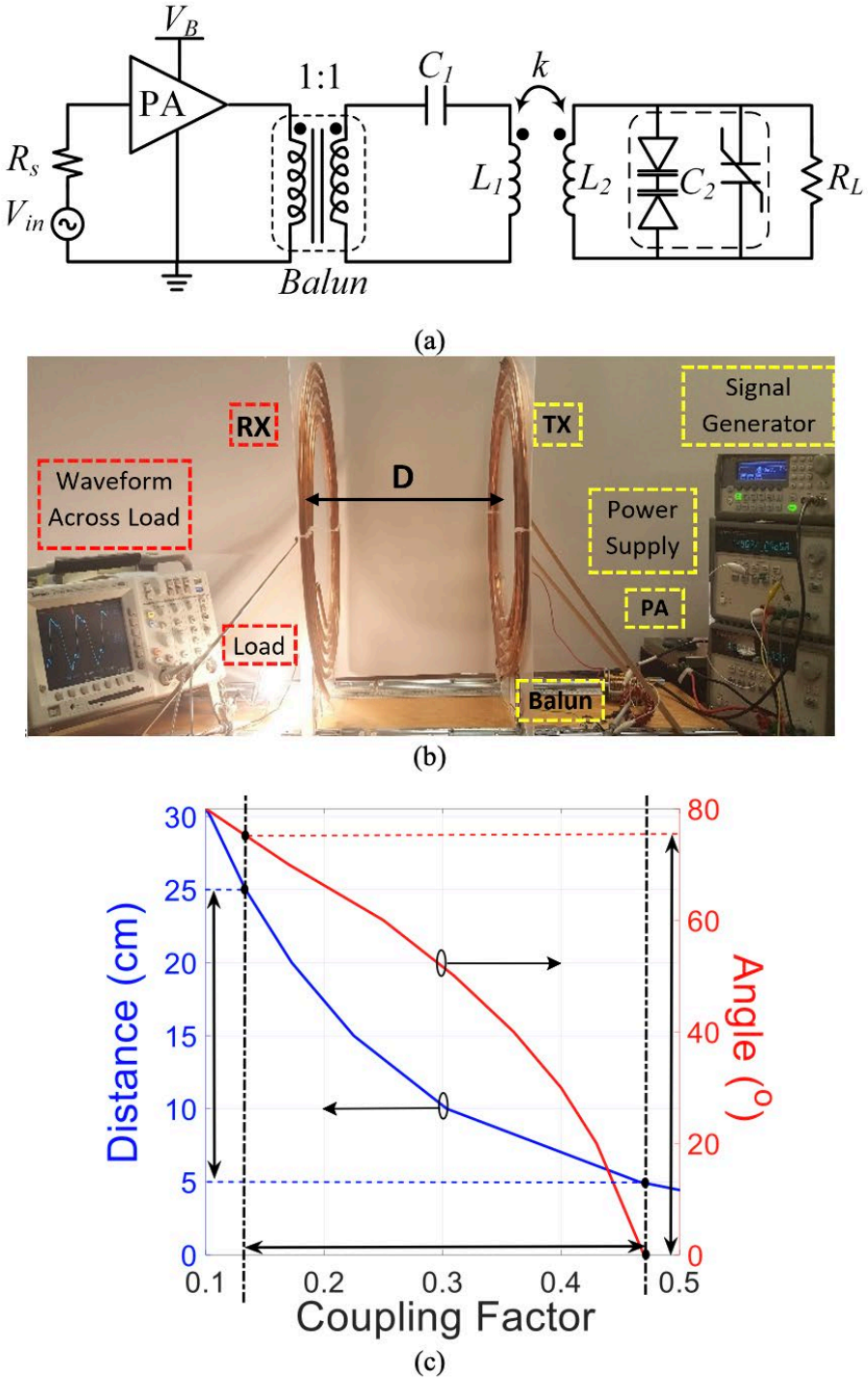


Figure 6.12 Implemented series-parallel topology of the position-insensitive WPT circuit: (a) circuit schematic, (b) experiment setup, and (c) measured coupling factor between the transmit and receive coils versus the transmission distance and the angular misalignment.

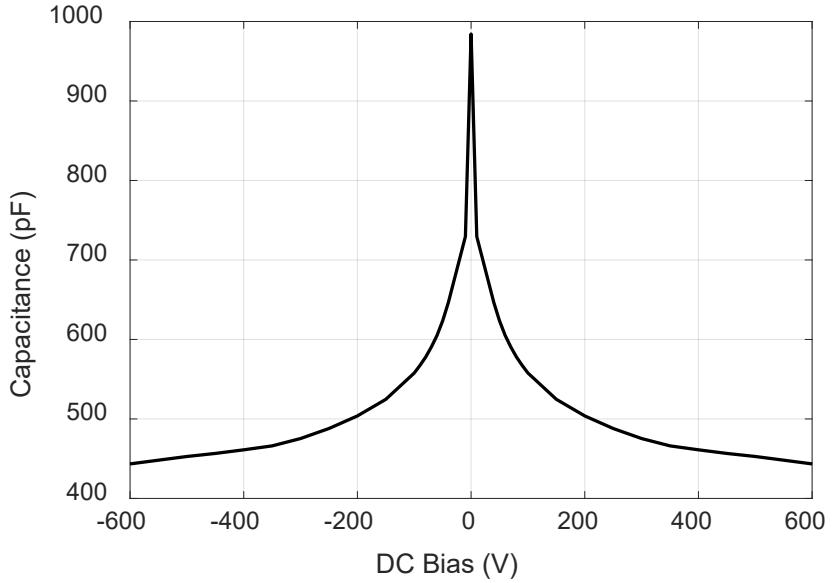


Figure 6.13 Measured C-V response of the optimized combination of the nonlinear capacitors.

Table 6.1 Component Specifications for the Implemented WPT Circuit.

Component	Specification
Transmit and Receive Coils	
Inductance	15 μH
Outer Diameter	40 cm
Inner Diameter	25 cm
Pitch	1 cm
Number of turns	5
Primary Capacitor	350 pF
Secondary Capacitor	Shunt combination of: 1. Anti-series connection of SiC STPSC20H12-Y 1.2kV Schottky diodes 2. Series & parallel combinations of high-voltage nonlinear X7R ceramic capacitors (equivalent DC capacitance = 200 pF)
Load Resistor	2.5 kΩ

The measured coupling factor values as function of: (1) the transmission distance and (2) the angle between the transmit and receive coils at 20 cm transmission distance, are shown in Fig. 6.12(c). Based on [164], the coupling factor is proportional to $\cos(\alpha)$, where α is the angle between the normal vectors to the coils' planes. Afterwards, the design procedure discussed in Section III is followed to synthesize the required nonlinearity at the receiver side such that a high PTE is maintained within the operating range. The C-V curve of the optimized nonlinear device is measured and shown in Fig. 6.13. This nonlinearity is realized using a combination of an anti-series connected SiC STPSC20H12-Y 1.2kV Schottky diodes in shunt with a combination of several high-voltage, low-loss nonlinear ceramic capacitors of Class II (X7R) which exhibit strong voltage dependent capacitance behavior when driven with high voltage swings [166].

The output power delivered to a real 2.5 kΩ resistive load is measured as a function of the transmission distance (D) and lateral misalignment. The PTE is defined as the ratio of the load power to the PA output available power. Therefore, the impedance mismatch at the PA output port is taken into account when calculating PTE. However, the power efficiency of the PA itself is not included in the measured PTE values. The measured received power is approximately 51 W with max variation of 3 W over a distance variation from 5 cm to 25 cm. The simulation results (dashed lines) in comparison with the measurement results (solid lines) of the PTE versus transmission distance for both the nonlinear WPT circuit (black lines) and the corresponding linear WPT circuit, using the same experimental setup, (red lines) are shown in Fig. 6.14(a). The measured results show a good agreement with the simulation results especially at low coupling factor values. However, there is a slight discrepancy between them at high coupling factor values (transmission distance range between 5 cm and 10 cm). This is expected to be due to the discrepancy between the measured and modeled C-V curves of the nonlinear devices in addition to the inaccurate

modeling of the circuit losses as a function of the temperature and the large signal across the nonlinear devices. These effects can be mitigated by careful optimization for the circuit setup in the simulation environment. More careful modeling optimization would result in a better agreement between the simulation and measurement results.

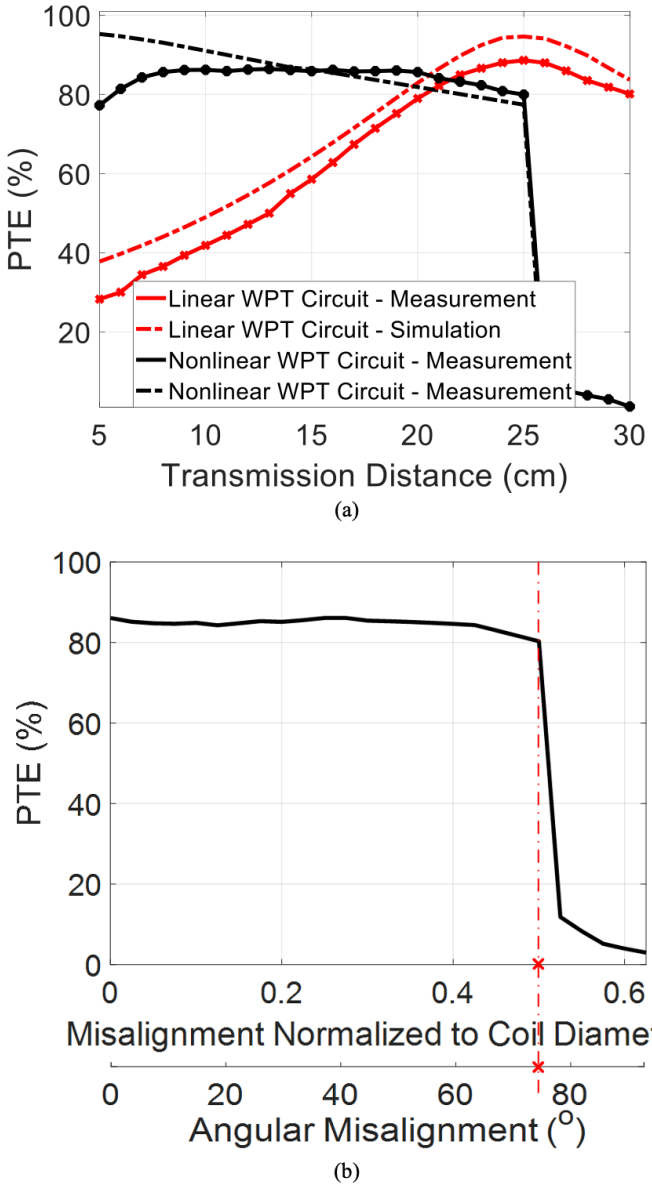


Figure 6.14 Measured PTE versus (a) distance variation, and (b) lateral misalignment offset and angular misalignment between the transmit and receive coils.

As depicted in Fig. 6.14(a), a maximum PTE of 86% in the conventional linear WPT circuit is measured at transfer distance of 25 cm (corresponding to the critical coupling factor for this setup) and decreases as distance varies in both directions (towards and away from the source). At the same time, not only the nonlinear WPT circuit achieves the same peak PTE of 86%, it maintains the high PTE over distance variation of $\Delta D = \pm 10$ measured from the center operating transfer distance ($D = 15\ cm$). Compared to a conventional WPT circuit using the same experimental setup, the high-efficient operating transmission range, defined with a PTE higher than 80%, extends by 200%, and the efficiency at the shortest transmission distance (5 cm) improves by about 2.6 times.

The proposed position-insensitive WPT circuit compensates for the effect of the coupling factor variation on the PTE within a specific range based on the circuit nonlinearity. The value of the coupling factor is highly dependent on the relative position between the transmit and receive coils in terms of the vertical transmission distance, lateral misalignment, and angular misalignment. Therefore, the tolerable range of coupling factor translates into an efficient 3D charging zone for a wireless charger where the high PTE and the targeted power level are maintained independent on the position and orientation of the device. In this paper, the implemented WPT circuit tolerates a variation in the coupling factor value between 0.14 and 0.47, as shown in Fig. 6.12(c).

Motivated by that, the robustness of the nonlinear WPT circuit as a function of the lateral and angular misalignments between the transmit and receive coils are tested. Fig 6.14(b) shows the measured PTE as a function the lateral misalignment, normalized to the diameter of the coil measured at the center operating distance ($D = 15\ cm$), and the angular misalignment in degrees measured at a transmission distance of 20 cm. The peak PTE is maintained when lateral

misalignment is increased up to +/- 20 cm (±50% of the coil diameter). Moreover, the circuit maintains the same peak PTE when varying the angle between the transmit and receive coils up to $\pm 75^{o}$. The tolerable ranges of the lateral and angular misalignments map to the same coupling factor range that can be tolerated by the circuit's nonlinearity. Furthermore, both ranges are function of the transmission distance between the centers of the coils since it affects the overall value of the coupling factor as well.

The jump-down that appears in the PTE curve at the critical coupling distance is imposed by the hysteresis characteristic of the nonlinear resonators. It can be proved that there is no valid solution for high PTE to exist at the operating frequency within the under-coupled region. For nonlinear WPT circuits, the critical coupling distance defines the upper boundary of the efficient transmission range which is designed based on the required system specifications.

The robust nonlinear resonant-based WPT circuit introduced in this chapter promises the 3-dimentional positioning freedom in WPT systems allowing efficient wireless power transfer, without requiring precision positioning or alignment over the charging pad. The presented technique is applicable to a broad range of operating conditions including operating distances, frequencies, or power ranges. Therefore, WPT circuits based on nonlinear resonance can have a significant impact on the performance of WPT systems operating in real world environments.

6.5 Conclusion

This chapter presents a novel technique using nonlinear passive devices to design position insensitive WPT circuits which maintain their performance independent of the coupling factor between the transmit and receive coils. The position insensitive WPT circuit introduced here is entirely passive, simple and highly reliable as it does not require any active feedback control

circuits, source frequency tuning, tunable matching networks, and controllers. A 60 W WPT circuit prototype designed based on such technique is implemented and its performance is measured. The circuit exhibits a near-constant efficiency of approximately 80% operating at 2.25 MHz over: (1) distance variation, ΔD, of up to +/- 10 cm from the center operating transfer distance ($D_o = 15\ cm$), (2) lateral misalignment of up to ±50% of the coils' diameter at the center operating distance, and (3) angular misalignment of up to ±75°.

Chapter 7

Conclusion and Future Work

7.1. Summary

During the recent years, the Internet-of-Things (IoT) is rapidly evolving. It is indeed the future of communication that has transformed Things of the real world into smarter devices. To date, the world has deployed billions of "smart" connected things. Predictions say there will be 10's of billions of connected devices by 2025 and in our lifetime we will experience life with a trillion-node network. However, battery lifespan exhibits a critical barrier to scaling IoT devices. Replacing batteries on a trillion-sensor scale is a logistically prohibitive feat. Consequently, companies continue to revise those predications to reflect this issue. Self-powered IoT devices are considered as the right solution to this challenge. The main objective of this thesis is to develop solutions to achieve energy-efficient wireless-connectivity and wireless-charging for IoT applications.

In the first part of the thesis, I introduce ultra-low power radios that are compatible with the Bluetooth Low-Energy (BLE) standard. BLE is considered as the preeminent protocol for short-range communications that support transmission ranges up to 10's of meters. Two BLE transmitters (TX) has been presented. The first BLE TX is a PLL-less architecture that utilizes open-loop transmission scheme. The BLE TX is duty-cycled over which the TX goes to a sleep mode between advertisement events to reduce the average power consumption. The duty-cycling

requires fast startup time for the crystal oscillator and RF front-end circuits. The second BLE TX is an all-digital architecture implemented in FinFET technology. An all-digital PLL driving a switched-capacitor power amplifier is designed to generate the modulated BLE packets. On the receive side, two BLE receivers (RX) has been presented. The first BLE RX is a backchannel receiver that achieves low power operation through data repetition in the payload of the BLE packet and still be able to communicate with a fully-compliant BLE transmitters. The other BLE receiver is a fully-compliant BLE4.0 receiver including the CRC and Data De-whitening blocks. Both BLE RXs are PLL-less, mixer-first architecture. An antenna-chip co-design approach is introduced for passive quadrature generation in the RF path. Additionally, a novel low-power discrete-time, differentiator-based GFSK demodulator has been presented. The packet synchronization was achieved by means of oversampling in the DSP block.

In the second part of the thesis, I introduce passive nonlinear resonant circuits to achieve wide-band RF energy harvesting and robust wireless power transfer circuits. Nonlinear resonant circuits modeled by the Duffing nonlinear differential equation exhibit interesting hysteresis characteristics in their frequency and amplitude responses that are exploited in designing self-adaptive wireless charging systems. In the wireless power transfer scenario, coupled nonlinear resonators are used to maintain the power transfer level and efficiency over a range of coupling factors without active feedback control circuitry. Coupling factor depends on the transmission distance, lateral, and angular misalignments between the charging pad and the device. Therefore, nonlinear resonance extends the efficient charging zones of a wireless charger without the requirement for a precise alignment.

7.2. Future Work

The space of energy-efficient wireless communications and wireless charging for IoT applications is significantly wide. There are several directions that can be explored as an extended future work for the current thesis.

I. BLE Wireless Transceivers:

   a. BLE Receivers: Improve the current design of the presented BLE RX architecture to achieve a fully-compliant BLE5.0 receiver that can support both 1.0 and 2.0 Mbps. One possible direction is to utilize N-path mixer first architecture to improve NF, low-voltage LNA-first architecture, and extended version for the coherent-based GFSK demodulator to support higher data rates.

   b. BLE Transmitters: develop a complete fully-synthesizable approach for digital BLE transmitters based on proper modeling and variety of auxiliary cells' library.

   c. BLE Transceivers: integrate the presented BLE TX and BLE RX chips to achieve a full-duplex BLE transceiver that can transmit and receive packets from a commercial smart phone with self-powered operation for health monitoring applications.

   d. Other standards: ULP radio architectures for wakeup cellular IoT radios, mainly NB-IoT.

II. Robust wireless charging

   a. WPT circuits: study the utilization of nonlinear inductors and nonlinear dielectric resonators in WPT circuits, explore the behavior of coupled higher-order nonlinear resonance circuits, and design nonlinear-based

capacitive/hybrid (inductive and capacitive) WPT circuits. Additional potential direction is scaling the problem to achieve simultaneous robust power transmission between multiple transmitters and multiple receivers. Another interesting direction is the integration of those circuits on silicon using conventional CMOS technologies to operate at ISM GHz frequency bands.

b. Wireless harvesting circuits: build a complete nonlinear-resonant based circuit including the power management unit, utilize the proposed techniques to achieve simultaneous wireless information and power transmission (SWIPT), and explore the integration of RF WEH circuits on silicon using conventional CMOS technologies.

Appendix 1

Bluetooth Low Energy Standard Requirements for Transmitters

The BLE standard operates in the 2.4 GHz ISM band at 2400-2483.5 MHz and it uses 40 RF channels. These RF channels have center frequencies 2402 + k * 2 MHz, where k = 0, ..., 39. The output power of the transmitter may be informatively classified into power classes based on the highest output power the BLE PHY supports, as defined in table 8.1.

Table 8.1 BLE Standard Transmission Power Classes

Power Class	Maximum Output Power (P_{max})	Minimum Output Power[1]
1	100 mW (+20 dBm)	10 mW (+10 dBm)
1.5	10 mW (+10 dBm)	0.01 mW (-20 dBm)
2	2.5 mW (+4 dBm)	0.01 mW (-20 dBm)
3	1 mW (0 dBm)	0.01 mW (-20 dBm)

The BLE standard utilizes Gaussian Frequency Shift Keying (GFSK) modulation with a bandwidth-bit period product BT=0.5 (Fig. 8.1). The modulation index shall be between 0.45 and 0.55. A binary one shall be represented by a positive frequency deviation, and a binary zero shall be represented by a negative frequency deviation. The standard indicates the minimum frequency deviation shall never be less than 185 kHz when transmitting at 1Mbps. The symbol timing accuracy shall be better than ±50 ppm. The zero crossing error is the time difference between the ideal symbol period and the measured crossing time. This shall be less than ±1/8 of a symbol period.

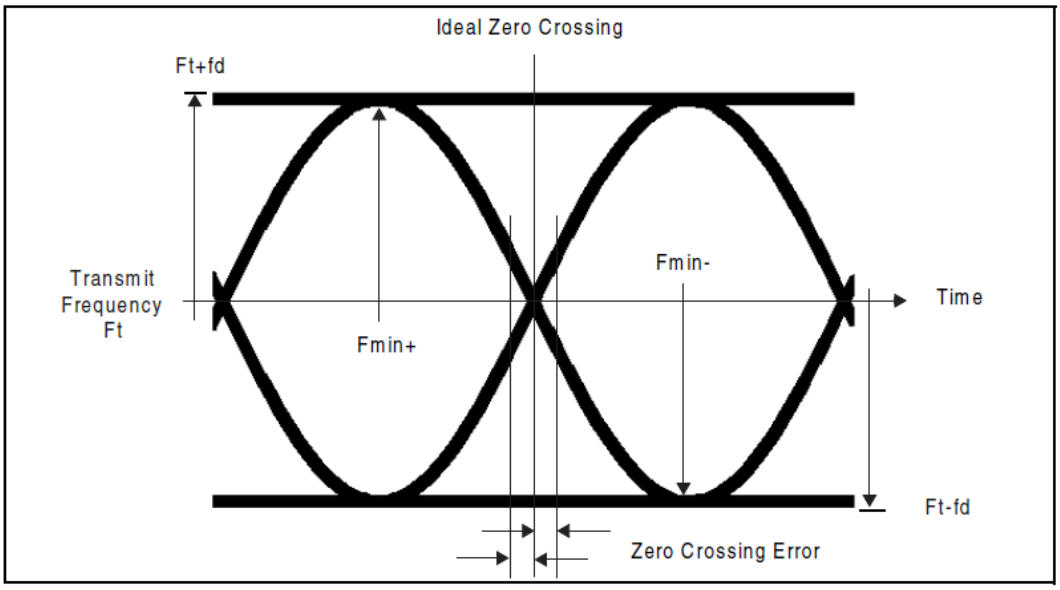


Figure 8.1 BLE Standard GFSK Parameters Definition.

An adjacent channel power is specified for channels at least 2 MHz from the carrier when transmitting with 1Mbps modulation. This adjacent channel power is defined as the sum of the measured power in a 1 MHz bandwidth. The spectrum measurement shall be performed with a 100 kHz resolution bandwidth and an average detector. The device shall transmit on an RF channel with the center frequency M and the adjacent channel power shall be measured on a 1 MHz RF frequency N. The transmitter shall transmit a pseudo random data pattern in the payload throughout the test. The transmit spectrum mask when transmitting with 1Mbps modulation is shown in table 8.2.

Table 8.2 BLE Standard Transmit Spectrum Mask

Frequency offset	Spurious Power
2 MHz (|M-N| = 2)	-20 dBm
3 MHz or greater (|M-N| ≥ 3)	-30 dBm

The deviation of the center frequency during the packet shall not exceed ±150 kHz, including both the initial frequency offset and drift. The frequency drift during any packet shall be less than 50 kHz. The drift rate shall be less than 400 Hz/μs. The limits on the transmitter center frequency drift within a packet is shown in table 8.3.

Table 8.3 BLE Standard Maximum Allowable Frequency Drifts in a Packet

Parameter	Frequency Drift
Maximum drift	±50 kHz
Maximum drift rate[1]	400 Hz/μs

Based on the standard requirements, the PLL specifications can be determined as summarized in table 8.4.

Table 8.4 PLL Specifications Based on the BLE Standard Requirements

Specification	Value
Frequency Band	2.4 – 2.48 GHz (80MHz)
Number of Channels	40
Channel B.W.	2 MHz
Fref	40MHz
GFSK Modulation B.W.	+/-250KHz
PLL Architecture	ADPLL
Settling Time	<15μS
Power	<2 mW
Frequency Fine Tuning	16-24kHz
Frequency Course Tuning	100MHz
Maximum Frequency Deviation (500μS)	+/- 50KHz
Phase Noise @ 1 MHz offset	< -90 dBc/Hz

Appendix 2

List of Acronyms

ABB	Analog Baseband
ACR	Adjacent Channel Rejection
ADPLL	All-Digital Phase Locked Loop
APR	Automatic Place and Route
BC	Back-Channel
BER	Bit Error Rate
BLE	Bluetooth Low Energy
C	Capacitor
CRC	Cyclic Redundancy Check
DBB	Digital Baseband
D.C.	Duty Cycling
DCO	Digitally-Controlled Oscillator
DeW	De-Whitening
DSP	Digital Signal Processing
ED	Energy Detection
EM	Electro-Magnetic

ESR	Equivalent Series Resistance
FASoC	Fully-Automated System on Chip
FCW	Frequency Command Word
FLL	Frequency Locked Loop
FoM	Figure of Merit
FSK	Frequency Shift Keying
FSM	Finite State Machine
GFSK	Gaussian Frequency Shift Keying
GP	General Purpose
I/Q	In-phase/Quadrature
IF	Intermediate Frequency
IoT	Internet of Things
L	Inductor
LNA	Low-Noise Amplifier
LO	Local Oscillator
LP	Low Power
LPWAN	Low Power Wide Area Network
MAC	Medium Access Control
NB-IoT	Narrow-Band Internet of Things
NF	Noise Figure
OOK	On-OFF Keying
OSC	Oscillator
OSF	Over-Sampling Factor

PA	Power Amplifier
PAE	Power Added Efficiency
PD	Preamble Detector
PGLA	Pattern Generator Logic Analyzer
Ph-ADC	Phase Analog-to-Digital Converter
PLL	Phase Locked Loop
PN	Phase Noise
Pout	Output Power
PTE	Power Transfer Efficiency
Q	Quality Factor
QAM	Quadrature Amplitude Modulation
R	Resistor
RF	Radio Frequency
RO	Ring Oscillator
RX	Receiver
SCD	Switched-Capacitor Differentiator
SC-DPA	Switched-Capacitor Class-D Power Amplifier
SCPA	Switched Capacitor Power Amplifier
SD	Symbol Detector
SIR	Signal to Interference Ratio
SoC	System on Chip
SPI	Serial Peripheral Interface
TDC	Time to Digital Converter

TI	Time Interval
TRX	Transceiver
TSPC	True Single Phase Clock
TX	Transmitter
ULP	Ultra Low Power
VCO	Voltage Controlled Oscillator
WEH	Wireless Energy Harvesting
WPT	Wireless Power Transfer
WuRX	Wakeup Receiver
XO	Crystal Oscillator

BIBLIOGRAPHY

[1] V. Balas, K. Solanki, R. Kumar, M. Khari. The history, present and future with IoT. Internet of Things and Big Data Analytics for Smart Generation, Springer, Cham (2019), pp. 27-51.

[2] Khan, R., Khan, S.U., Zaheer, R., Khan, S.: Future internet: the internet of things architecture, possible applications and key challenges. In: Proceedings of Frontiers of Information Technology (FIT), pp. 257–260 (2012).

[3] Ibarra-Esquer, J.E., González-Navarro, F.F., Flores-Rios, B.L., Burtseva, L., Astorga-Vargas, M.A.: Tracking the evolution of the internet of things concept across different application Domains, Sensors 17, 1379 (2017).

[4] Akyildiz, I.F., Su, W., Sankarasubramaniam, Y., Cayirci, E.: Wireless sensor networks: a survey. Comput. Netw. 38, 393–422 (2002).

[5] Jason, P.: Bill joy's six webs. MIT Technology Review, 29 September 2005.

[6] Ashton, K.: That 'Internet of Things' Thing, RFID J. 22 June 2009.

[7] Shen, G., Liu, B.: The visions, technologies, applications and security issues of internet of things. E-Business and E -Government (ICEE), pp. 1–4.

[8] Pal, A., Mukherjee, A., Dey, S.: Future of Healthcare-Sensor Data-Driven Prognosis. International Publishing Switzerland, Springer Series in Wireless Technology (2016).

[9] International Telecommunication Union—Telecommunication Standardization Sector (ITU-T). Recommendation ITU-T Y. 2060—Overview of the Internet of Things; ITU-T: Geneva, Switzerland (2012).

[10] Hwang, J., Choe, Y.: Smart Cities—Seoul: A Case Study. ITU-T Technology Watch Report; International Telecommunication Union—Telecommunication Standardization Sector (ITU-T): Geneva, Switzerland (2013)

[11] Cisco: The Internet of Things Reference Model; Cisco and/or its Affiliates: San Jose, CA, USA (2014).

[12] OECD Committee for Digital Economy Policy: OECD Technology Foresight Forum 2014—The Internet of Things.

[13] Dutta, S., Geiger, T., Lanvin, B.: The Global Information Technology Report 2015—ICTs for Inclusive Growth. Geneva, Switzerland, World Economic Forum and INSEAD (2015).

[14] Atzori, L., Iera, A., Morabito, G.: The internet of things: a survey. Comput. Netw.—SciDirect 54(15), 2787–2805 (2010).

[15] Zeng, L.: A security framework for internet of things based on 4G Communication. In: Computer Science and Network Technology (ICCSNT), pp. 1715–1718 (2012).

[16] https://www.mckinsey.com/featured-insights/internet-of-things/how-we-help-clients#

[17] https://www.statista.com/statistics/976313/global-iot-market-size/

[18] http://greenhvacrmag.com/2018/iot-enabled-systems/

[19] https://www.statista.com/statistics/1101442/iot-number-of-connected-devices-worldwide/

[20] G. A. Akpakwu, B. J. Silva, G. P. Hancke and A. M. Abu-Mahfouz, "A Survey on 5G Networks for the Internet of Things: Communication Technologies and Challenges," in IEEE Access, vol. 6, pp. 3619-3647, 2018, doi: 10.1109/ACCESS.2017.2779844.

[21] D. Bandyopadhyay and J. Sen, “Internet of things: Applications and challenges in technology and standardization,” Wireless Pers. Commun., vol. 58, no. 1, pp. 49–69, 2011.

[22] M. R. Palattella et al., "Internet of Things in the 5G Era: Enablers, Architecture, and Business Models," in IEEE Journal on Selected Areas in Communications, vol. 34, no. 3, pp. 510-527, March 2016, doi: 10.1109/JSAC.2016.2525418.

[23] L. Da Xu, W. He, and S. Li, “Internet of things in industries: A survey,” IEEE Trans. Ind. Informat., vol. 10, no. 4, pp. 2233–2243, Nov. 2014.

[24] M. Swan, “The quantified self: Fundamental disruption in big data science and biological discovery,” Big Data, vol. 1, no. 2, pp. 85–99, 2013.

[25] H. Karl and A. Willig, Protocols and Architectures for Wireless Sensor Networks. Hoboken, NJ, USA: Wiley, 2007.

[26] W. Ejaz, M. Naeem, A. Shahid, A. Anpalagan, and M. Jo, ``Efficient energy management for the Internet of Things in smart cities," IEEE Commun. Mag., vol. 55, no. 1, pp. 8491, Jan. 2017.

[27] IEEE Standard 802.15.1, Bluetooth.

[28] C. Gomez, J. Oller, and J. Paradells, ``Overview and evaluation of Bluetooth lowenergy: An emerging low-power wireless technology," Sensors, vol. 12, no. 9, pp. 11734-11753, 2012.

[29] M. Siekkinen, M. Hiienkari, J. K. Nurminen, and J. Nieminen, ``How low energy is Bluetooth low energy? Comparative measurements with ZigBee/802.15.4," in Proc. IEEE Wireless Commun. Netw. Conf. Work- shops (WCNCW), Apr. 2012, pp. 232-237.

[30] Zhang, H.; Wentzloff, D.; Kim, H. Software-Defined, WiFi and BLE Compliant Back-Channel for Ultra-Low Power Wireless Communication. In Proceedings of the IEEE Global Communications Conference (GLOBECOM), Washington, DC, USA, 4–8 December 2016; pp. 1–6.

[31] Abdelatty, O.; Bishop, H.; Shi, Y.; Chen, X.; Alghaihab, A.; Calhoun, B.; Wentzloff, D. A Low Power Bluetooth Low-Energy Transmitter with a 10.5nJ Startup-Energy Crystal Oscillator. In Proceedings of the IEEE 45th European Solid State Circuits Conference (ESSCIRC), Cracow, Poland, 23–26 September 2019; pp. 377–380.

[32] Yang, S.; Yin, J.; Yi, H.; Yu, W.; Mak, P.; Martins, R. A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS. IEEE J. Solid-State Circuits 2019, 54, 1351–1362, doi:10.1109/JSSC.2018.2888874.

[33] Ruiz, L.; Ridder, M.; Fan, D.; Gong, J.; Li, B.; Mills, A.; Cobarrubias, E.; Strohmaier, J.; Jur, J.; Lach, J. Self-Powered Cardiac Monitoring: Maintaining Vigilance With Multi-Modal Harvesting and E-Textiles. IEEE Sens. J. 2021, 21, 2263–2276, doi:10.1109/JSEN.2020.3017706.

[34] Li, S.; Breiholz, J.; Kamineni, S.; Im, J.; Wentzloff, D.; Calhoun, B. An 85 nW IoT Node-Controlling SoC for MELs Power-Mode Management and Phantom Energy Reduction. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 6–9 Setember 2020; pp. 1–5.

[35] Chen, G.; Ghaed, H.; Haque, R.; Wieckowski, M.; Kim, Y.; Kim, G.; Fick, D.; Kim, D.; Seok, M.; Wise, K.; et al. A cubic-millimeter energy-autonomous wireless intraocular pressure monitor. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 20–24 February 2011; pp. 310–312.

[36] Sano, T.; Mizokami, M.; Matsui, H.; Ueda, K.; Shibata, K.; Toyota, K.; Saitou, T.; Sato, H.; Yahagi, K.; Hayashi, Y. 13.4 A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.

[37] Rim, Chun T., and Chris Mi. Wireless power transfer for electric vehicles and mobile devices. John Wiley & Sons, 2017.

[38] S. Y. R. file:///Users/molefisMac/Desktop/Sel.-R. C. with C. C. for W. P. T. pd. Hui, W. Zhong, and C. K. Lee, “A critical review of recent progress in mid-range wireless power transfer,” IEEE Trans. Power Electron., vol. 29, no. 9, pp. 4500–4511, 2014.

[39] https://www.prnewswire.com/news-releases/covid-19-cuts-smart-home-growth-by-us14-billion-in-2020-but-drives-future-change-301109561.html

[40] M. Molefi, E. D. Markus and A. Abu-Mahfouz, "Wireless Power Transfer for IoT Devices - A Review," 2019 International Multidisciplinary Information Technology and Engineering Conference (IMITEC), 2019, pp. 1-8, doi: 10.1109/IMITEC45504.2019.9015869.

[41] W.-Y. Lai, T.-R. Hsiang Wireless charging deployment in sensor networks Sensors, 19 (1) (2019), pp. 1-19

[42] Y. Zeng, B. Clerckx, and R. Zhang, “Communications and signals design for wireless power transmission,” IEEE Trans. Commun., vol. 65, no. 5, pp. 2264–2290, May 2017.

[43] K. W. Choi, A. A. Aziz, D. Setiawan, N. M. Tran, L. Ginting and D. I. Kim, "Distributed Wireless Power Transfer System for Internet of Things Devices," in IEEE Internet of Things Journal, vol. 5, no. 4, pp. 2657-2671, Aug. 2018, doi: 10.1109/JIOT.2018.2790578.

[44] Abdelatty, O.; Chen, X.; Alghaihab, A.;Wentzloff, D. Bluetooth Communication Leveraging Ultra-Low Power Radio Design. J. Sens. Actuator Netw. 2021, 10, 31. https://doi.org/10.3390/ jsan10020031

[45] O. Abdelatty, A. Alghaihab, Y. Cherivirala, S. Kamineni, B. Calhoun, and D. Wentzloff, "A 300μW Bluetooth-Low-Energy Backchannel Receiver Employing a Discrete-Time Differentiator-Based Coherent GFSK Demodulation", Accepted, RFIC 2021.

[46] O. Abdelatty et al., "A Low Power Bluetooth Low-Energy Transmitter with a 10.5nJ Startup-Energy Crystal Oscillator," ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC), 2019, pp. 377-380, doi: 10.1109/ESSCIRC.2019.8902902.

[47] O. Abdelatty, X. Wang and A. Mortazawi, "Position-Insensitive Wireless Power Transfer Based on Nonlinear Resonant Circuits," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 9, pp. 3844-3855, Sept. 2019, doi: 10.1109/TMTT.2019.2904233.

[48] O. Abdelatty, X. Wang and A. Mortazawi, "Nonlinear Resonant Circuits for Coupling-Insensitive Wireless Power Transfer Circuits," 2018 IEEE/MTT-S International Microwave Symposium - IMS, 2018, pp. 976-979, doi: 10.1109/MWSYM.2018.8439690.

[49] O. Abdelatty, X. Wang and A. Mortazawi, "Exploiting Nonlinearity to Design Robust Wireless Power Transfer and Wideband RF Energy Harvesting," 2018 IEEE Wireless Power Transfer Conference (WPTC), 2018, pp. 1-4, doi: 10.1109/WPT.2018.8639148.

[50] X. Wang, O. Abdelatty and A. Mortazawi, "A novel coupling factor independent highly efficient resonant based wireless power transfer," 2017 47th European Microwave Conference (EuMC), 2017, pp. 200-203, doi: 10.23919/EuMC.2017.8230834.

[51] Jeon, K.; She, J.; Soonsawad, P.; Ng, P. BLE Beacons for Internet of Things Applications: Survey, Challenges, and Opportunities. IEEE Internet Things J. 2018, 5, 811–828, doi:10.1109/JIOT.2017.2788449.

[52] Bechthum, E.; Dijkhuis, J.; Ding, M.; He, Y.; Van Den Heuvel, J.; Mateman, P.; Van Schaik, G.; Shibata, K.; Song, M.; Tiurin, E.; et al. 30.6 A Low-Power BLE Transceiver with Support for Phase-Based Ranging, Featuring 5µs PLL Locking Time and 5.3ms Ranging Time, Enabled by Staircase-Chirp PLL with Sticky-Lock Channel-Switching. In Proceedings of the IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 2–6 February 2020, pp. 470–472.

[53] Moosavifar, M.; Wentzloff, D. Analysis of Design Trade-Offs in Ultra Low Power FSK Receivers for Phase-Based Ranging. In Proceedings of the IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNeT), San Diego, CA, USA, 23 January 2021.

[54] Zhang, H.; Wentzloff, D.; Kim, H. Software-Defined, WiFi and BLE Compliant Back-Channel for Ultra-Low Power Wireless Communication. In Proceedings of the IEEE Global Communications Conference (GLOBECOM), Washington, DC, USA, 4–8 December 2016; pp. 1–6.

[55] Abdelatty, O.; Bishop, H.; Shi, Y.; Chen, X.; Alghaihab, A.; Calhoun, B.; Wentzloff, D. A Low Power Bluetooth Low-Energy Transmitter with a 10.5nJ Startup-Energy Crystal Oscillator. In Proceedings of the IEEE 45th European Solid State Circuits Conference (ESSCIRC), Cracow, Poland, 23–26 September 2019; pp. 377–380.

[56] Yang, S.; Yin, J.; Yi, H.; Yu, W.; Mak, P.; Martins, R. A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS. IEEE J. Solid-State Circuits 2019, 54, 1351–1362, doi:10.1109/JSSC.2018.2888874.

[57] Ruiz, L.; Ridder, M.; Fan, D.; Gong, J.; Li, B.; Mills, A.; Cobarrubias, E.; Strohmaier, J.; Jur, J.; Lach, J. Self-Powered Cardiac Monitoring: Maintaining Vigilance With Multi-Modal Harvesting and E-Textiles. IEEE Sens. J. 2021, 21, 2263–2276, doi:10.1109/JSEN.2020.3017706.

[58] Li, S.; Breiholz, J.; Kamineni, S.; Im, J.; Wentzloff, D.; Calhoun, B. An 85 nW IoT Node-Controlling SoC for MELs Power-Mode Management and Phantom Energy Reduction. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 6–9 Setember 2020; pp. 1–5.

[59] Chen, G.; Ghaed, H.; Haque, R.; Wieckowski, M.; Kim, Y.; Kim, G.; Fick, D.; Kim, D.; Seok, M.; Wise, K.; et al. A cubic-millimeter energy-autonomous wireless intraocular pressure monitor. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 20–24 February 2011; pp. 310–312.

[60] Sano, T.; Mizokami, M.; Matsui, H.; Ueda, K.; Shibata, K.; Toyota, K.; Saitou, T.; Sato, H.; Yahagi, K.; Hayashi, Y. 13.4 A 6.3 mW BLE transceiver embedded RX image-rejection filter and TX harmonic-suppression filter reusing on-chip matching network. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.

[61] Hanes, D.; Salgueiro, G.; Grossetete, P.; Barton, R.; Henry, J. IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things; Cisco Press: Indianapolis, IN, USA, 2017; ISBN: 9780134307091.

[62] Wang, P.; Mercier, P. An Interference-Resilient BLE-Compatible Wake-Up Receiver Employing Single-Die Multi-Channel FBAR-Based Filtering and a 4-D Wake-Up Signature. IEEE J. Solid-State Circuits 2021, 56, 416–426, doi:10.1109/JSSC.2020.3012892.

[63] Wentzloff, D. Low Power Radio Survey. Available online: www.eecs.umich.edu/wics/low_power_radio_survey.html (accessed on 30 March 2021).

[64] Kim, H.; Wentzloff, D. Back-Channel Wireless Communication Embedded in WiFi-Compliant OFDM Packets. IEEE J. Sel. Areas Commun. 2016, 34, 3181–3194, doi:10.1109/JSAC.2016.2612078.

[65] Im, J.; Kim, H.; Wentzloff, D. A 335μW −72dBm receiver for FSK back-channel embedded in 5.8GHz Wi-Fi OFDM packets. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, USA, 4–6 June 2017; pp. 176–179.

[66] Alghaihab, A.; Shi, Y.; Breiholz, J.; Kim, H.; Calhoun, B.; Wentzloff, D. Enhanced Interference Rejection Bluetooth Low-Energy Back-Channel Receiver With LO Frequency Hopping. IEEE J. Solid-State Circuits 2019, 54, 2019–2027, doi:10.1109/JSSC.2019.2907160.

[67] Brown, J.; Huang, K.; Ansari, E.; Rogel, R.; Lee, Y.; Wentzloff, D. An ultra-low-power 9.8GHz crystal-less UWB transceiver with digital baseband integrated in 0.18um BiCMOS. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 17–21 February 2013, pp. 442-443.

[68] Abdelhamid, M.; Paidimarri, A.; Chandrakasan, A. A −80dBm BLE-compliant, FSK wake-up receiver with system and within-bit dutycycling for scalable power and latency. In Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, USA, 8–11 April 2018; pp. 1–4.

[69] Tang, S.; Yomo, H.; Takeuchi, Y. Optimization of Frame Length Modulation-Based Wake-Up Control for Green WLANs. IEEE Trans. Veh. Technol. 2015, 64, 768–780.

[70] Roberts, N.; Craig, K.; Shrivastava, A.; Wooters, S.; Shakhsheer, Y.; Calhoun, B.; Wentzloff, D. 26.8 A 236nW −56.5dBm-sensitivity Bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 31 January–4 February 2016; pp. 450–451.

[71] Roberts, N.; Wentzloff, D. A 98nW wake-up radio for wireless body area networks. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium, Montreal, QC, Canada, 17–19 June 2012; pp. 373–376.

[72] Wentzloff, D.; Alghaihab, A.; Im, J. Ultra-Low Power Receivers for IoT Applications: A Review. In Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, 22–25 March 2020; pp. 1–8.

[73] Moody, J.; Dissanayake, A.; Bishop, H.; Lu, R.; Liu, N.; Duvvuri, D.; Gao, A.; Truesdell, D.; Barker, N.; Gong, S.; et al. A -106dBm 33nW Bit-Level Duty-Cycled Tuned RF Wake-up Receiver. In Proceedings of the Symposium on VLSI Circuits, Kyoto, Japan, 9–14 June 2019; pp. C86–C87.

[74] Wang, P.; Mercier, P. 28.2 A 220μW -85dBm Sensitivity BLE-Compliant Wake-up Receiver Achieving −60dB SIR via Single-Die Multi- Channel FBAR-Based Filtering and

a 4-Dimentional Wake-Up Signature. In Proceedings of the IEEE International Solid- State Circuits Conference—(ISSCC), 17–21 February 2019; pp. 440–442.

[75] Alghaihab, A.; Kim, H.; Wentzloff, D. Analysis of Circuit Noise and Non-Ideal Filtering Impact on Energy Detection Based Ultra-Low-Power Radios Performance. IEEE Trans. Circuits Syst. Ii Express Briefs 2018, 65, 1924–1928, doi:10.1109/TCSII.2018.2807764.

[76] Dissanayake, A.; Bishop, H.; Moody, J.; Muhlbauer, H.; Calhoun, B.; Bowers, S. A Multichannel, MEMS-Less −99dBm 260nW Bit-Level Duty Cycled Wakeup Receiver. In Proceedings of the IEEE Symposium on VLSI Circuits 2020, Honolulu, HI, USA, 13–19 June 2020; pp. 1–2.

[77] Moody, J.; Bowers, S. Triode-mode Envelope Detectors for Near Zero Power Wake-up Receivers. In Proceedings of the IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 4–6 June 2019; pp. 1499–1502.

[78] Kosari, A.; Moosavifar, M.; Wentzloff, D. A 152μW −99dBm BPSK/16-QAM OFDM Receiver for LPWAN Applications. In Proceedings of the IEEE Asian Solid-State Circuits Conference (A-SSCC), Tainan, Taiwan, 5–7 November 2018, pp. 303-306.

[79] Bryant, C.; Sjoland, H. A 0.55 mW SAW-Less Receiver Front-End for Bluetooth Low Energy Applications. IEEE J. Emerg. Sel. Top. Circuits Syst. 2014, 4, 262–272, doi:10.1109/JETCAS.2014.2337153.

[80] Lee, S.; Choi, I.; Kim, H.; Kim, B. A Sub-mW Fully Integrated Wide-Band Receiver for Wireless Sensor Network. IEEE Microw. Wirel. Compon. Lett. 2015, 25, 319–321, doi:10.1109/LMWC.2015.2409808.

[81] Im, J.; Kim, H.; Wentzloff, D. A 217μW −82dBm IEEE 802.11 Wi-Fi LP-WUR using a 3rd-Harmonic Passive Mixer. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 10–12 June 2018; pp. 172–175.

[82] Rahman, M.; Harjani, R. A Sub-1-V 194- 31-dB FOM 2.3–2.5-GHz Mixer-First Receiver Frontend for WBAN with Mutual Noise Cancellation. IEEE Trans. Microw. Theory Tech. 2016, 64, 1102–1109, doi:10.1109/TMTT.2016.2536603.

[83] Abe, T.; Morie, T.; Satou, K.; Nomasaki, D.; Nakamura, S.; Horiuchi, Y.; Imamura, K. An ultra-low-power 2-step wake-up receiver for IEEE 802.15.4g wireless sensor networks. In Proceedings of the Symposium on VLSI Circuits, Honolulu, HI, USA, 2014; pp. 1–2.

[84] Im, J.; Kim, H.; Wentzloff, D. A 470μW −92.5dBm OOK/FSK Receiver for IEEE 802.11 WiFi LP-WUR. In Proceedings of the IEEE 44th European Solid State Circuits Conference (ESSCIRC), Dresden, Germany, 2018; pp. 302–305.

[85] Salazar, C.; Cathelin, A.; Kaiser, A.; Rabaey, J. A 2.4 GHz Interferer-Resilient Wake-Up Receiver Using A Dual-IF Multi-Stage N-Path Architecture. IEEE J. Solid-State Circuits 2016, 51, 2091–2105, doi:10.1109/JSSC.2016.2582509.

[86] Masuch, J.; Delgado-Restituto, M. A 1.1-mW-RX -81.4-dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy. IEEE Trans. Microw. Theory Tech. 2013, 61, 1660–1673, doi:10.1109/TMTT.2013.2247621.

[87] Liu, Y.; Bachmann, C.; Wang, X.; Zhang, Y.; Ba, A.; Busze, B.; Ding, M.; Harpe, P.; van Schaik, G.; Selimis, G.; et al. 13.2 A 3.7mW-RX 4.4mW-TX fully integrated Bluetooth Low-Energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40nm CMOS. In Proceedings of the IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.

[88] Kuo, F.; Ferreira, S.; Babaie, M.; Chen, R.; Cho, L.; Jou, C.; Hsueh, F.; Huang, G.; Madadi, I.; Tohidian, M.; et al. A Bluetooth low-energy (BLE) transceiver with TX/RX switchable on-chip matching network, 2.75mW high-IF discrete-time receiver, and 3.6mW all-digital transmitter. In Proceedings of the IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2.

[89] Alghaihab, A.; Breiholz, J.; Kim, H.; Calhoun, B.; Wentzloff, D. A 150 μW −57.5 dBm-Sensitivity Bluetooth Low-Energy Back-Channel Receiver with LO Frequency Hopping. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 10–12 June 2018; pp. 324–327.

[90] Ding, M.; Wang, X.; Zhang, P.; He, Y.; Traferro, S.; Shibata, K.; Song, M.; Korpela, H.; Ueda, K.; Liu, Y.; et al. A 0.8V 0.8mm2 bluetooth 5/BLE digital-intensive transceiver with

a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS. In Proceedings of the IEEE International Solid—State Circuits Conference—(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 446–448.

[91] Liu, H.; Sun, Z.; Tang, D.; Huang, H.; Kaneko, T.; Deng, W.; Wu, R.; Okada, K.; Matsuzawa, A. An ADPLL-centric bluetooth low-energy transceiver with 2.3mW interference-tolerant hybrid-loop receiver and 2.9mW single-point polar transmitter in 65nm CMOS. In Proceedings of the IEEE International Solid—State Circuits Conference—(ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 444–446.

[92] Sun, Z.; Liu, H.; Tang, D.; Huang, H.; Kaneko, T.; Wu, R.; Deng, W.; Okada, K. A 0.85mm2 BLE Transceiver with Embedded T/R Switch, 2.6mW Fully-Passive Harmonic Suppressed Transmitter and 2.3mW Hybrid-Loop Receiver. In Proceedings of the IEEE 44th European Solid State Circuits Conference (ESSCIRC), Dresden, Germany, 2018; pp. 310–313.

[93] Yu, W.; Yi, H.; Mak, P.; Yin, J.; Martins, R. 24.4 A 0.18V 382μW bluetooth low-energy (BLE) receiver with 1.33nW sleep power for energy-harvesting applications in 28nm CMOS. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 414–415.

[94] Thijssen, B.; Klumperink, E.; Quinlan, P.; Nauta, B. 30.4 A 370μW 5.5dB-NF BLE/BT5.0/IEEE 802.15.4-Compliant Receiver with >63dB Adjacent Channel Rejection at >2 Channels Offset in 22nm FDSOI. In Proceedings of the IEEE International Solid- State Circuits Conference—(ISSCC), San Francisco, CA, USA, 2–6 February 2020; pp. 466–468.

[95] Park, B.; Kwon, K. 2.4-GHz Bluetooth Low Energy Receiver Employing New Quadrature Low-Noise Amplifier for Low-Power Low-Voltage IoT Applications. IEEE Trans. Microw. Theory Tech. 2021, 69, 1887–1895, doi:10.1109/TMTT.2020.3041010.

[96] Alghaihab, A.; Chen, X.; Shi, Y.; Truesdell, D.; Calhoun, B.; Wentzloff, D. 30.7 A Crystal-Less BLE Transmitter with −86dBm Freq μ ency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet. In Proceedings of the IEEE International Solid- State Circuits Conference—(ISSCC), San Francisco, CA, USA, 11–15 February 2020; pp. 472–474.

[97] Tamura, M.; Takano, H.; Shinke, S.; Fujita, H.; Nakahara, H.; Suzuki, N.; Nakada, Y.; Shinohe, Y.; Etou, S.; Fujiwara, T.; et al. 30.5 A 0.5V BLE Transceiver with a 1.9mW RX Achieving −96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI. In Proceedings of the IEEE International Solid- State Circuits Conference—(ISSCC), San Francisco, CA, USA, 2–6 February 2020; pp. 468-470.

[98] Staszewski, R.; Wallberg, J.; Rezeq, S.; Chih-Ming Hung; Eliezer, O.; Vemulapalli, S.; Fernando, C.; Maggio, K.; Staszewski, R.; Barton, N.; Meng-Chang Lee; Cruise, P.; et al. All-digital PLL and transmitter for mobile phones. IEEE J. Solid-State Circuits 2005, 40, 2469–2482, doi:10.1109/JSSC.2005.857417.

[99] Prummel, J.; Papamichail, M.; Willms, J.; Todi, R.; Aartsen, W.; Kruiskamp, W.; Haanstra, J.; Opbroek, E.; Rievers, S.; Seesink, P.; et al. A 10 mW Bluetooth Low-Energy Transceiver with On-Chip Matching. IEEE J. Solid-State Circuits 2015, 50, 3077–3088, doi:10.1109/JSSC.2015.2469674.

[100] Chen, X.; Breiholz, J.; Yahya, F.; Lukas, C.; Kim, H.; Calhoun, B.; Wentzloff, D. Analysis and Design of an Ultra-Low-Power Bluetooth Low-Energy Transmitter With Ring Oscillator-Based ADPLL and 4× Frequency Edge Combiner. IEEE J. Solid-State Circuits 2019, 54, 1339–1350, doi:10.1109/JSSC.2019.2896404.

[101] Babaie, M.; Kuo, F.; Chen, H.; Cho, L.; Jou, C.; Hsueh, F.; Shahmohammadi, M.; Staszewski, R. A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm. IEEE J. Solid-State Circuits 2016, 51, 1547–1565, doi:10.1109/JSSC.2016.2551738.

[102] Kuo, F.; Binsfeld Ferreira, S.; Chen, H.; Cho, L.; Jou, C.; Hsueh, F.; Madadi, I.; Tohidian, M.; Shahmohammadi, M.; Babaie, M.; et al. A Bluetooth Low-Energy Transceiver With 3.7-mW All-Digital Transmitter, 2.75-mW High-IF Discrete-Time Receiver, and TX/RX Switchable On-Chip Matching Network. IEEE J. Solid-State Circuits 2017, 52, 1144–1162, doi:10.1109/JSSC.2017.2654322.

[103] Shi, Y.; Chen, X.; Kim, H.; Blaauw, D.; Wentzloff, D. 28.3 A 606μW mm-Scale Bluetooth Low-Energy Transmitter Using Co-Designed 3.5×3.5mm2 Loop Antenna and Transformer-

Boost Power Oscillator. In Proceedings of the IEEE International Solid- State Circuits Conference—(ISSCC), San Francisco, CA, USA, 17–21 February 2019; pp. 442–444.

[104] Chen, X.; Breiholz, J.; Yahya, F.; Lukas, C.; Kim, H.; Calhoun, B.; Wentzloff, D. A 486 μW All-Digital Bluetooth Low Energy Transmitter with Ring Oscillator Based ADPLL for IoT applications. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, USA, 2018; pp. 168–171.

[105] Yoo, S.; Walling, J.; Woo, E.; Jann, B.; Allstot, D. A Switched-Capacitor RF Power Amplifier. IEEE J. Solid-State Circuits 2011, 46, 2977–2987, doi:10.1109/JSSC.2011.2163469.

[106] Ajayi, T.; Kamineni, S.; Cherivirala, Y.; Fayazi, M.; Kwon, K.; Saligane, M.; Gupta, S.; Chen, C.; Sylvester, D.; Blaauw, D.; et al. An Open-source Framework for Autonomous SoC Design with Analog Block Generation. In Proceedings of the IFIP/IEEE 28th International Conference on Very Large Scale Integration (VLSI-SOC), Salt Lake City, UT, USA, 2020; pp. 141–146.

[107] Li, C.; Yuan, M.; Liao, C.; Lin, Y.; Chang, C.; Staszewski, R. All-Digital PLL for Bluetooth Low Energy Using 32.768-kHz Reference Clock and ≤0.45-V Supply. IEEE J. Solid-State Circuits 2018, 53, 3660–3671, doi:10.1109/JSSC.2018.2871632.

[108] Wiser, B.; Sankaragomathi, K.; Schauer, J.; Korhummel, S.; Kavousian, P.; Yeager, D.; Arumugam, N.; Pletcher, N.; Barkin, D.; Parker, R.; et al. A 1.53 mm3 crystal-less standards-compliant Bluetooth Low Energy module for volume constrained wireless sensors. In Proceedings of the Symposium on VLSI Circuits, Kyoto, Japan, 2019; pp. C84–C85.

[109] Chen, X.; Alghaihab, A.; Shi, Y.; Truesdell, D.; Calhoun, B.; Wentzloff, D. A Crystal-Less BLE Transmitter With Clock Recovery From GFSK-Modulated BLE Packets. IEEE J. Solid-State Circuits 2021, 1–1, doi:10.1109/JSSC.2020.3046610.

[110] Chen, X.; Kim, H.; Wentzloff, D. An analysis of phase noise requirements for ultra-low-power FSK radios. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, USA, 4–6 June 2017; pp. 37–40.

[111] A. Alghaihab, X. Chen, Y. Shi, D. S. Truesdell, B. H. Calhoun and D. D. Wentzloff, "30.7 A Crystal-Less BLE Transmitter with −86dBm Freq μ ency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 472-474, doi: 10.1109/ISSCC19947.2020.9062935.

[112] M. Tamura et al., "30.5 A 0.5V BLE Transceiver with a 1.9mW RX Achieving −96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 468-470, doi: 10.1109/ISSCC19947.2020.9063021.

[113] W. Yu, H. Yi, P. Mak, J. Yin and R. P. Martins, "24.4 A 0.18V 382μW bluetooth low-energy (BLE) receiver with 1.33nW sleep power for energy-harvesting applications in 28nm CMOS," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 414-415, doi: 10.1109/ISSCC.2017.7870437.

[114] J. Masuch and M. Delgado-Restituto, "A 1.1-mW-RX -81.4-dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 4, pp. 1660-1673, April 2013, doi: 10.1109/TMTT.2013.2247621.

[115] A. Alghaihab et al. "A 150 μW −57.5 dBm-Sensitivity Bluetooth Low-Energy Back-Channel Receiver with LO Frequency Hopping," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, 2018, pp. 324-327.

[116] M. R. Abdelhamid, A. Paidimarri and A. P. Chandrakasan, "A −80dBm BLE-compliant, FSK wake-up receiver with system and within-bit dutycycling for scalable power and latency," 2018 IEEE Custom Integrated Circuits Conference (CICC), San Diego, CA, 2018, pp. 1-4.

[117] Y. Shi, X. Chen, H. Kim, D. Blaauw and D. Wentzloff, "28.3 A 606μW mm-Scale Bluetooth Low-Energy Transmitter Using Co-Designed 3.5×3.5mm2 Loop Antenna and Transformer-Boost Power Oscillator," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 442-444.

[118] X. Chen et al., "A 486 μW All-Digital Bluetooth Low Energy Transmitter with Ring Oscillator Based ADPLL for IoT applications," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, 2018, pp. 168-171.

[119] M. Babaie et al., "A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm," in IEEE Journal of Solid-State Circuits, vol. 51, no. 7, pp. 1547-1565, July 2016.

[120] Y. Liu et al., "13.2 A 3.7mW-RX 4.4mW-TX fully integrated Bluetooth Low-Energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40nm CMOS," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3.

[121] K. Lei, P. Mak, M. Law and R. P. Martins, "A regulation-free sub-0.5V 16/24MHz crystal oscillator for energy-harvesting BLE radios with 14.2nJ startup energy and 31.8pW steady-state power," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 52-54.

[122] S. Iguchi, A. Saito, Y. Zheng, K. Watanabe, T. Sakurai and M. Takamiya, "93% power reduction by automatic self power gating (ASPG) and multistage inverter for negative resistance (MINR) in 0.7V, 9.2μW, 39MHz crystal oscillator," 2013 Symposium on VLSI Circuits, Kyoto, 2013, pp. C142-C143.

[123] D. Griffith, J. Murdock and P. T. Røine, "5.9 A 24MHz crystal oscillator with robust fast start-up using dithered injection," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 104-105.

[124] https://fasoc.engin.umich.edu/

[125] J. S. Walling, S. Yoo and D. J. Allstot, "Digital power amplifier: A new way to exploit the switched-capacitor circuit," in IEEE Communications Magazine, vol. 50, no. 4, pp. 145-151, April 2012, doi: 10.1109/MCOM.2012.6178848.

[126] S. Yoo, J. S. Walling, E. C. Woo, B. Jann and D. J. Allstot, "A Switched-Capacitor RF Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 46, no. 12, pp. 2977-2987, Dec. 2011, doi: 10.1109/JSSC.2011.2163469.

[127] M. Babaie et al., "A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm," in IEEE Journal of Solid-State Circuits, vol. 51, no. 7, pp. 1547-1565, July 2016, doi: 10.1109/JSSC.2016.2551738.

[128] X.Z. Wei, Z. Wang, H. Dai, "A critical Review of Wireless Power Transfer via Strong Coupled Magnetic Resonances", Energies 2014, vol. 7, pp. 4316-4341, July 2014.

[129] K. Wu, D. Choudhury and H. Matsumoto, "Wireless Power Transmission, Technology, and Applications [Scanning the Issue]," in Proceedings of the IEEE, vol. 101, no. 6, pp. 1271-1275, June 2013.

[130] S. Y. R. Hui, W. Zhong and C. K. Lee, "A Critical Review of Recent Progress in Mid-Range Wireless Power Transfer," in IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4500-4511, Sept. 2014.

[131] A. P. Sample, D. T. Meyer and J. R. Smith, "Analysis, Experimental Results, and Range Adaptation of Magnetically Coupled Resonators for Wireless Power Transfer," in IEEE Transactions on Industrial Electronics, vol. 58, no. 2, pp. 544-554, Feb. 2011.

[132] P. S. Riehl et al., "Wireless Power Systems for Mobile Devices Supporting Inductive and Resonant Operating Modes," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 3, pp. 780-790, March 2015.

[133] S. Lee and R. D. Lorenz, "Development and Validation of Model for 95%-Efficiency 220-W Wireless Power Transfer Over a 30-cm Air Gap," in IEEE Transactions on Industry Applications, vol. 47, no. 6, pp. 2495-2504, Nov.-Dec. 2011.

[134] J. Dai and D. C. Ludois, "Capacitive Power Transfer Through a Conformal Bumper for Electric Vehicle Charging," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 1015-1025, Sept. 2016.

[135] C. Liu, A. P. Hu and N. K. C. Nair, "Modelling and analysis of a capacitively coupled contactless power transfer system," in IET Power Electronics, vol. 4, no. 7, pp. 808-815, Aug. 2011.

[136] R. Dias Fernandes, J. N. Matos and N. Borges Carvalho, "Resonant Electrical Coupling: Circuit Model and First Experimental Results," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 9, pp. 2983-2990, Sept. 2015.

[137] S. Li and C. C. Mi, "Wireless Power Transfer for Electric Vehicle Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 1, pp. 4-17, March 2015.

[138] Kurs, A., Karalis, A., Moffatt, R., Joannopoulos, J. D., Fisher, P., & Soljačić, M. (2007). Wireless power transfer via strongly coupled magnetic resonances. Science, 317(5834), 83-86.

[139] S. I. Babic and C. Akyel, "Calculating Mutual Inductance Between Circular Coils With Inclined Axes in Air," in IEEE Transactions on Magnetics, vol. 44, no. 7, pp. 1743-1750, July 2008.

[140] R. Huang, B. Zhang, D. Qiu and Y. Zhang, "Frequency Splitting Phenomena of Magnetic Resonant Coupling Wireless Power Transfer," in IEEE Transactions on Magnetics, vol. 50, no. 11, pp. 1-4, Nov. 2014, Art no. 8600204.

[141] J. D. Heebl, E. M. Thomas, R. P. Penno and A. Grbic, "Comprehensive Analysis and Measurement of Frequency-Tuned and Impedance-Tuned Wireless Non-Radiative Power-Transfer Systems," in IEEE Antennas and Propagation Magazine, vol. 56, no. 5, pp. 131-148, Oct. 2014.

[142] J. Park, Y. Tak, Y. Kim, Y. Kim, and S. Nam, “Investigation of adaptive matching methods for near-field wireless power transfer,” in IEEE Trans. Antennas Propag., vol. 59, no. 5, pp. 1769–1773, May 2011.

[143] Wenzhen Fu, Bo Zhang and Dongyuan Qiu, "Study on frequency-tracking wireless power transfer system by resonant coupling," 2009 IEEE 6th International Power Electronics and Motion Control Conference, Wuhan, 2009, pp. 2658-2663.

[144] B.-J. Jang, S. Lee, and H. Yoon, "HF-Band Wireless Power Transfer System: Concept, Issues, and Design," Progress In Electromagnetics Research, Vol. 124, 211-231, 2012.

[145] T. C. Beh, M. Kato, T. Imura, S. Oh and Y. Hori, "Automated Impedance Matching System for Robust Wireless Power Transfer via Magnetic Resonance Coupling," in IEEE Transactions on Industrial Electronics, vol. 60, no. 9, pp. 3689-3698, Sept. 2013.

[146] Benjamin H. Waters and Joshua R. Smith, "Adaptive impedance matching for magnetically coupled resonators." PIERS Proceedings. 2012.

[147] J. Lee, Y. Lim, W. Yang and S. Lim, "Wireless Power Transfer System Adaptive to Change in Coil Separation," in IEEE Transactions on Antennas and Propagation, vol. 62, no. 2, pp. 889-897, Feb. 2014.

[148] Y. Lim, H. Tang, S. Lim and J. Park, "An Adaptive Impedance-Matching Network Based on a Novel Capacitor Matrix for Wireless Power Transfer," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 4403-4413, Aug. 2014.

[149] J. Kim and J. Jeong, "Range-Adaptive Wireless Power Transfer Using Multiloop and Tunable Matching Techniques," in IEEE Transactions on Industrial Electronics, vol. 62, no. 10, pp. 6233-6241, Oct. 2015.

[150] G. Lee, B. H. Waters, Y. G. Shin, J. R. Smith and W. S. Park, "A Reconfigurable Resonant Coil for Range Adaptation Wireless Power Transfer," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 2, pp. 624-632, Feb. 2016.

[151] T. P. Duong and J. Lee, "Experimental Results of High-Efficiency Resonant Coupling Wireless Power Transfer Using a Variable Coupling Method," in IEEE Microwave and Wireless Components Letters, vol. 21, no. 8, pp. 442-444, Aug. 2011.

[152] Y. Lyu et al., "A Method of Using Nonidentical Resonant Coils for Frequency Splitting Elimination in Wireless Power Transfer," in IEEE Transactions on Power Electronics, vol. 30, no. 11, pp. 6097-6107, Nov. 2015.

[153] W. Lee, W. Son, K. Oh and J. Yu, "Contactless Energy Transfer Systems Using Antiparallel Resonant Loops," in IEEE Transactions on Industrial Electronics, vol. 60, no. 1, pp. 350-359, Jan. 2013.

[154] S. Assawaworrarit, X. Yu, S. Fan." Robust wireless power transfer using a nonlinear parity-time symmetric circuit" Nature 546 (2017), 387-390.

[155] X. Y. Zhang, C. D. Xue and J. K. Lin, "Distance-Insensitive Wireless Power Transfer Using Mixed Electric and Magnetic Coupling for Frequency Splitting Suppression," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 11, pp. 4307-4316, Nov. 2017.

[156] X. Wang and A. Mortazawi, "Duffing resonator circuits for performance enhancement of wireless power harvesters," 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, 2015, pp. 1-4.

[157] X. Wang, “High Efficiency and High Sensitivity Wireless Power Transfer and Wireless Power Harvesting Systems,” Ph.D. dissertation, Radiation Lab., Univ. of Michigan, Ann Arbor, 2016.

[158] A. Mortazawi, and X. Wang. “Nonlinear Resonance Circuit for Wireless Power Transmission and Wireless Power Harvesting.” U.S Patent publication 20160336810, application date: May 12, 2015.

[159] X. Wang and A. Mortazawi, "Bandwidth Enhancement of RF Resonators Using Duffing Nonlinear Resonance for Wireless Power Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 11, pp. 3695-3702, Nov. 2016.

[160] X. Wang, O. Abdelatty and A. Mortazawi, "A novel coupling factor independent highly efficient resonant based wireless power transfer," 2017 47th European Microwave Conference (EuMC), Nuremberg, 2017, pp. 200-203.

[161] Kovacic, I., & Brennan, M. J. (2011). The Duffing equation: Nonlinear oscillators and their behaviour. Wiley.com.

[162] Clary Jr William, T. "Nonlinear resonant circuit devices." U.S. Patent 2,838,687, June 10, 1958.

[163] E. Bou-Balust, A. El Aroudi, P. Fisher and E. Alarcon, "Unveiling nonlinear dynamics in resonant inductively coupled wireless power transfer," 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne VIC, 2014, pp. 2612-2615.

[164] E. R. Joy, A. Dalal and P. Kumar, "Accurate Computation of Mutual Inductance of Two Air Core Square Coils with Lateral and Angular Misalignments in a Flat Planar Surface," in IEEE Transactions on Magnetics, vol. 50, no. 1, pp. 1-9, Jan. 2014, Art no. 7000209

[165] https://www.youtube.com/watch?v=paIcyBurQLs&feature=youtu.be

[166] H. P. Jeon, Y. K. Choi, S. W. Kim, D. K. Choi, "Simulation and Characterization for the Non-Linearity of Multilayer Ceramic Capacitors with New Equivalent Circuits under Ac-Field", Solid State Phenomena, Vols. 124-126, pp. 827-830, Jun. 2007