Supporting Information

Low-Voltage Electrochemical Li_xWO_3 Synapses with Temporal Dynamics for Spiking Neural Networks

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1. Repeatability of conductance change and control sample during the Li intercalation/de-intercalation

We prepared a new LiWES device (200 × 50 μm^2) for exploring the repeatability of the conductance modulation during the Li intercalation/de-intercalation. During the test, a small DC reading voltage (0.1 V) was applied between the Source and Drain to continuously monitor the current/conductance level, while a gate dual-sweeping voltage ranging from 1.95 V to 2.75 V (*V* vs. Li/Li$^+$) was applied to the LFP for Li intercalation/de-intercalation. Up to 4 cycles of test were performed (**Figure S1**a) and we observed a fairly consistent dynamic range, which demonstrates the good repeatability of the conductance modulation of our LiWES during the Li intercalation/de-intercalation.

We fabricated a control sample without depositing WO_3 film and only deposited the Au (100 nm)/Ti (5 nm) metal contacts for Source and Drain. The reference gate LFP was placed about 2 mm away from the Source/Drain contacts and was manually coated with LFP slurry. PEO electrolyte was prepared[1] and drop-casted to cover both the Source/Drain contacts and LFP reference gate. The sample was heated at 80 °C on a hot plate to remove the residual solvent in Ar-gas glovebox. During the test, the sample was transferred into the vacuum probe station (JANIS ST-500-UHT) and annealed at 350 K for ~2 hours to eliminate the residual moisture before the electrical measurements. During the test, a small DC reading voltage (0.1 V) was applied between the Source and Drain to continuously monitor the current/conductance level, while a gate dual-sweeping voltage ranging from 1.95 V to 2.82 V (*V* vs. Li/Li$^+$) was applied to the LFP for Li intercalation/de-intercalation. As shown in Figure S1b, there is negligible current/conductance change during the gate dual-sweeping processes, which confirms that the 4 orders of magnitudes of conductance changes are due to the Li intercalation into WO_3 films, rather than electrical conductance changes of the PEO electrolyte.

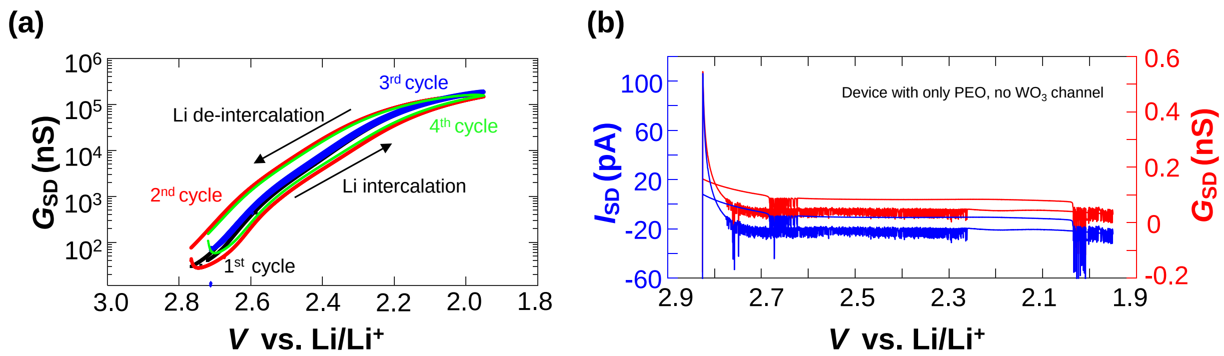

Figure S1. a) The electrical channel conductance change as a function of the electrochemical potential of Li_xWO_3 change during 4 consecutive cycles of Li intercalation/de-intercalation, demonstrating good repeatability. b) I_{SD} and G_{SD} response as a function of the gate sweeping voltage (V vs. Li/Li^+) when no WO_3 film is deposited as the channel and only PEO electrolyte is coated to cover the LFP reference electrode and channel area.

2. Endurance performance

For long-time endurance, we adopted a similar test method as reported in previous work.[2] We cycled our LiWES using 1000 cycles of 50 potentiation (0.5 V, 10 ms) and 50 depression (-0.5 V, 10 ms) pulses with a dynamic range ~ 500 %, shown in **Figure S2**. After the 10^5 pulses, our LiWES device is still working and shows no obvious degradation.

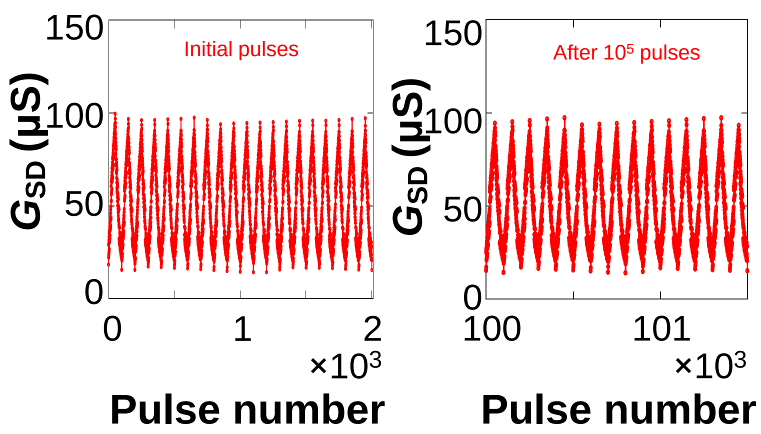

Figure S2. Long-time endurance performance of our LiWES. Endurance test for 10^5 pulses on our LiWES using 1000 cycles of 50 potentiation (0.5 V, 10 ms) and 50 depression (-0.5 V, 10 ms). No degradation of the device is found even after the 10^5 pulses.

3. Variation

Pulse-to-pulse variation and device-to-device variation are very important parameters for evaluating the synaptic device performance for DNNs application.[3] We leveraged the data from Figure 3e and statistically analyzed the conductance change ΔG_{SD} per pulse over the whole dynamic range window. As shown in **Figure S3**a, we find a relatively small variation ~11% of ΔG_{SD} per pulse for potentiation pulses (red) and ~13% for depression pulses (blue). For device-to-device variation (Figure S3b), we fabricated four different devices of the same dimensions (400 × 200 μm^2) in one single batch and applied a single potentiation pulse (0.5 V, 10 ms) to the Li_xWO_3 gate while monitoring the channel conductance change using a small reading voltage (0.1 V) between Li_xWO_3 Source/Drain. We find a small variation of 6.5 %, which demonstrates the good repeatability of our devices.

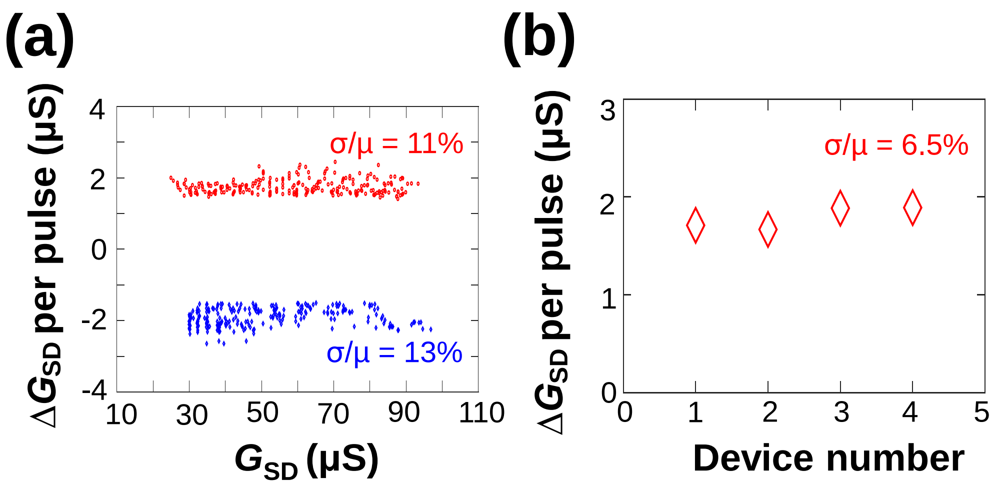

Figure S3. Variation test**.** a) Cycle-to-cycle (pulse-to-pulse) variation, plotted using data from Figure 3e. Small variation ~11% of ΔG_{SD} per pulse is found for potentiation pulses (red) and ~13% variation of ΔG_{SD} per pulse is found for depression pulses (blue). b) Small device-to-device variation ~6.5% of ΔG_{SD} per pulse using single potentiation pulse (0.5 V, 10 ms).

4. Long-term potentiation and depression via LFP gate

We further explored the long-term potentiation and depression by switching to use the LFP gate. For synaptic weight modulation via multiple pulses, we applied 50 potentiation pulses (3 V, 10 ms) and 50 depression pulses (- 1 V, 10 ms) applied at LFP gate as shown in **Figure S4**a. A dynamic range (~ 200 %) was achieved. During the test, a small DC reading voltage (0.1 V) was applied between the Source and Drain to continuously monitor the current/conductance level, while programming pulses were applied at LFP gate. Since the electrochemical OCV between LFP gate and $Li_{0.4}WO_3$ channel is ~ 1.1 V, we need to use potentiation pulses (3 V) and depression pulses (-1 V) at LFP gate to achieve a base voltage level (1 V) that can offset the OCV difference in order to obtain a more linear and symmetric conductance response.

For confirming the intermediate conductance level stability in Figure S4a, we applied 5 potentiona pulses (3 V, 10 ms) at LFP gate (Figure S4b) and then used a small DC reading voltage (0.1 V) at 80 °C to monitor the channel conductance and observed small gradual stability degradation that is likely due to to the slow self-extraction of the pulse-injected Li ions under high temperature at 80 °C. We also studied the long-time stability of the device after applying 5 depression pulses (-1 V, 10 ms) (Figure S4c) and no obvious stability degradation was observed.

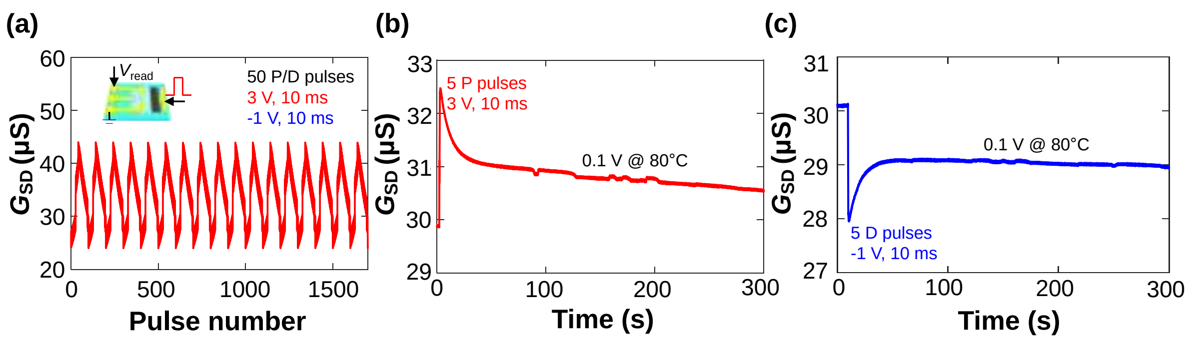

Figure S4. a) Synaptic weight modulation via multiple cycles of 50 potentiation pulses (3 V, 10 ms) and 50 depression pulses (- 1 V, 10 ms) applied at LFP gate. b) Long-time stability test of the LiWES device after 5 potentiation pulses (3 V, 10 ms) were applied. There is small gradual stability degradation, likely due to the slow self-extraction of the pulse-injected Li ions under high temperature at 80 °C. c) Long-time stability test of the LiWES device after 5 depression pulses (- 1 V, 10 ms) were applied. No obvious stability degradation was observed.

5. Scaling performance

We fabricated devices of different channel areas (from 1000 × 200 μm^2 to 200 × 50 μm^2) and applied single potentiation pulse at Li_xWO_3 gate while monitoring the channel conductance change. We define the programming energy as $E = I \times V \times$ t, which is enough to induce 10% increase of conductance change ($\Delta G_{SD}/ G_0$). Since there is near-zero open-circuit voltage (OCV) between our Li_xWO_3 gate and channel, V and t denote the programming voltage pulse amplitude[4] and programming voltage pulse width, respectively, while we define the current I as the average current between our Li_xWO_3 gate and channel. As shown in **Figure S5**, our smallest device (200 × 50 μm^2) demonstrates a very small programming energy (~ 2 pJ) and it shows a pseudo-linear scalability trend as previously reported.[5]

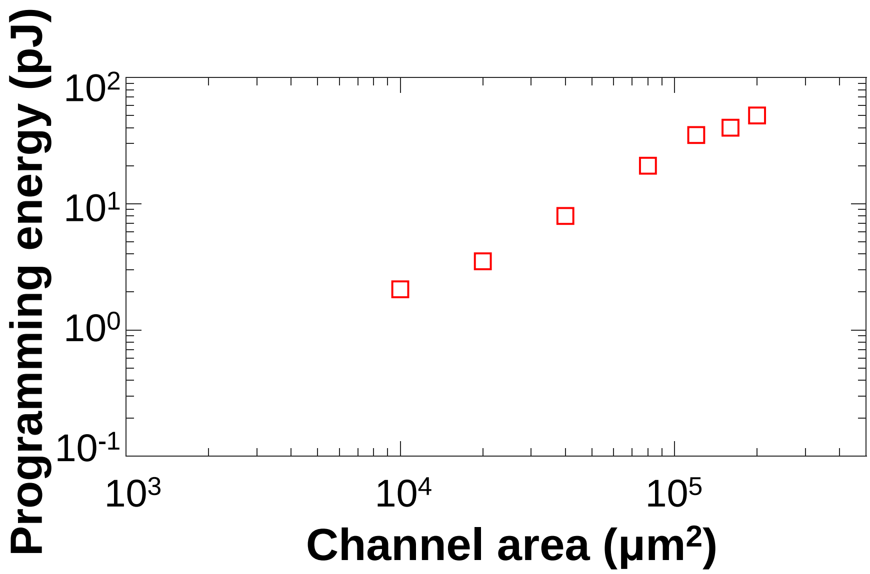

Figure S5. Scaling performance of programming energy as a function of channel area.

Reference

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