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Spice modeling of a tri-state memristor and analysis of its series and parallel characteristics

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Abstract: Memristors are passive nonlinear circuit components with memory characteristics, and have been recognized as the fourth basic circuit component, along with resistors, capacitors, and inductors. It has been nearly half a century since the conceptualization of the memristor, and related research has mainly focused on the two aspects of binary and continuous memristors. However, compared with these two types of memristors, tri-state and multi-state memristors have greater data density per device, with rich dynamics and great potential in logic and chaotic circuit applications. Moreover, prior researches show that the series-parallel connection of memristor generates more diverse circuit behaviors and increased capacity over a single memristor. However, most of this research is based on mathematical analysis, and lack behavioral circuit simulations or experimental validation. In this paper, the tri-state memristor is proposed and the mathematic and equivalent Spice models of the tri-state memristor is shown. Furthermore, the circuit characteristics are studied with a complete characterization of its series-parallel behaviors of the tri-state memristor. Simulations are performed with LTSpice, and the results verify the theoretical analysis, which provides a strong experimental basis for the study of combinational memristive circuits.

1. Introduction

The memristor was postulated by Chua in 1971 as the fourth fundamental circuit element, in addition to the resistor, inductor and capacitor [1]. In 2008, HP Laboratories realized the physical device model of memristor, which has set off a research upsurge of the memristor [2]. However, the barrier to access reliable devices remains high due to the high cost of highly specialized processes. Accordingly, it is important for design verification to model the memristor and design an equivalent circuit emulator to accurately describe the internal characteristics and port characteristics of the components. These studies will provide a theoretical basis and technical foundation for the circuit design and application of new memory devices in the future.

In 2009, Biolek designed a Spice memristor model with parameterizable nonlinear boundary [3]. In 2010, Mohammad and Parker implemented a low-pass filter based on the Spice model of the memristor [4]. In 2011, Batas constructed a Spice model of a memristor, and used this model to simulate the memristor in series and parallel [5]. In 2012, Adzmi devised a Spice model of a memristor based on the

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mathematical model of HP memristor with a window function and built a simple analog circuit to verify the accuracy of the Spice memristor model [6]. In the same year, Eshraghian[7] introduced a modeling approach based on tunneling, which includes the concept of programming threshold and SPICE-friendly adaptation, and the approach significantly improves simulation robustness in terms of convergence and overflows for current. In 2015, Takahashi proposed the Spice model of a memristor with a Tukey window function [8]. In 2016, Biolek established two Spice models of complex memristive networks, namely the improved S model (simple and reliable) and the improved Pickett model (accurate enough to reduce complexity). The improved models can operate without convergence issues in a circuit network containing multiple memristors [9]. In 2017, Mbarek created a simple Spice model suitable for memory cell design, tested the circuit characteristics of the model under different parameter conditions and different input signals. The advantages and disadvantages of the proposed model and the other four types of memristor Spice models are compared [10].

Recently, the research on memristors in mathematical models, circuit models, and physical device models has been carried out successively [6,11-14], and the application of memristors in chaotic circuits and other fields has also deepened [15,16]. However, a single memristor is insufficient for practical applications. Some scholars have researched on the series-parallel characteristics of compositely connected memristor circuits. It is demonstrated that the memristor series-parallel circuits allow for high data density, better performance, and dynamic characteristics. In 2017, He and Huang used a third-order smooth flux-controlled memristor model to theoretically analyze the equivalent resistance of series-parallel and reverse series-parallel circuits, and conducted numerical simulations [17]. In 2018, Zheng studied the memristor series-parallel circuit with coupling effect and applied it to the classic Chua's circuit to generate a chaotic attractor [18]. In 2019, Guo established a combined circuit based on fractional memristor and analyzed the equivalent memconductance of the combined circuit under different parameters and different connection methods. The analysis method and research results provided a reference for the subsequent cascade study of memcapacitors, meminductors and other high-order components [19].

During the in-depth study of the memristor theory, our team found that there is an increasingly important need for tri-state memristors when comparing existing binary with continuous memristor models. For example, in digital logic circuits, a tri-state memristor has greater data density, which is useful for constructing multi-state logic circuits. In nonlinear circuits, building a chaotic system based on a tri-state memristor can expand the type of chaos and broaden the design space of chaotic systems. In 2021, the authors of this paper realized a chaotic system based on a voltage-controlled ternary memristor, which lays the foundation for the application of tri-valued and multi-valued memristors in nonlinear systems[20]. Nevertheless, reports on tri-state memristors are sparse in the literature, and there is a lack of in-depth and systematic analysis on tri-state memristors. Therefore, it is of great importance to propose a mathematical model of tri-state memristor, establish a Spice circuit model of tri-valued memristor, and study the characteristics of the series-parallel circuit of the tri-state memristor.

The content of this article is as follows: Section 2 presents the Mathematical model and LTSpice circuit model of the tri-state memristor. In section 3, series-parallel circuit characteristics of tri-state memristor are analyzed in detail. LTSpice simulations are provided in Section 4 to validate the correction of the theatrical analysis in Section 3. Conclusions are drawn in Section 5.

2. Modeling of a tri-state memristor

2.1 Mathematical model of a voltage-controlled tri-state memristor

In contrast to binary and continuous memristors, this paper shows the series and parallel circuit characteristics of the tri-state memristors, aiming to reveal a simple and feasible method for building a multi-valued memristor by ternary memristors through cascade connection, actually this study provides a way for building a ternary memristor by binary memristors too.

In this study, we take the voltage-controlled tri-state memristor as the research subject, because the current-controlled memristor research is similar to that of the voltage-controlled memristor. We present a mathematical model of voltage-controlled tri-state memristor based on the way of building a multi-valued memristor mathematic model first proposed in [21]. The specific q-φ relation of the tri-state memristor model is described by an asymmetrical piecewise linear function as follows:

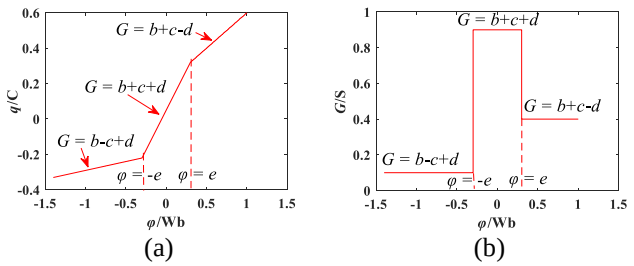
$$q = a + b\varphi + c|\varphi + e| - d|\varphi - e| \quad \varphi(0) < -e \tag{1}$$

where q and φ are the charge and the flux of the memristor, $\varphi(0)$ is the initial state of flux, a, b, c, d, e are constant parameters, here e and $-e$ are the turning points of the tri-valued memristor. Only and only if $\varphi(0)<-e$, Eq.(1) expresses a tri-valued memristor model with threshold characteristics, that is when the flux across the memristor greater or less than the threshold values, the memristor will change to three different values. In the cases not match the condition $\varphi(0)<-e$, this model expresses a binary memristor ($-e<\varphi(0)<e$) and a constant resistor ($\varphi(0)>e$).

According to the mathematical definition of the memristor, by taking the derivative on both sides of Eq.(1), the relationship between the memconductance and the flux of the voltage-controlled tri-state memristor can be obtained as:

$$\frac{dq}{d\varphi} = G(\varphi) = \left[b + c\,\mathrm{sgn}(\varphi + e) - d\,\mathrm{sgn}(\varphi - e)\right] \quad \varphi(0) < -e \tag{2}$$

where $G(\varphi)$ is the memconductance in unit Siemens (S), sgn(•) represents the signum. To show the specific characteristics of the tri-state memristor model, we set [a, b, c, d, e]=[0.0045, 0.25, 0.4, 0.25, 0.3], then we can obtain the flux-charge relationship in Fig.1(a) and the flux-memconductance relationship in Fig.1(b).



(a) (b)

Fig. 1. *Characteristic curves of voltage-controlled tri-state memristor model* (a=0.0045, b=0.25, c=0.4, d=0.25, e=0.3) **(a)** φ-q curve, **(b)** φ-G curve

Applying the sinusoidal excitation voltage $v(t)=1.2\sin(2\pi ft)$ to the above tri-state memristor model, with a frequency f=0.159Hz and initial state $\varphi(0)$=-0.4, the characteristic curves of the voltage-controlled tri-state memristor model are shown in Fig.2.

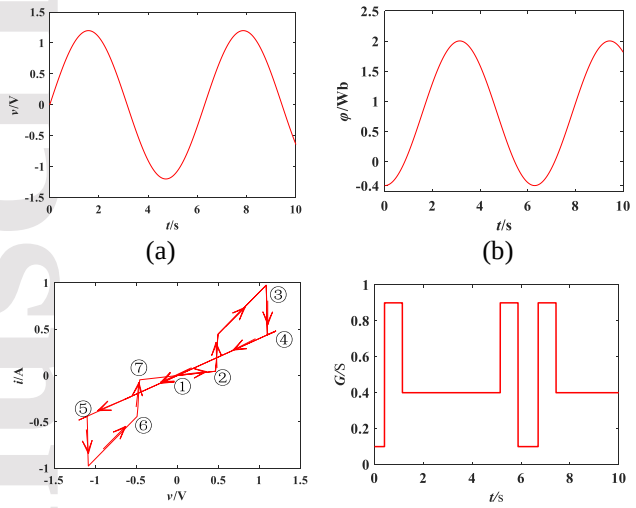


Fig. 2. *Applied voltage curves and characteristic curves of voltage-controlled tri-valued memristor model*
(a) v-t curve, **(b)** φ-t curve, **(c)** v-i curve, **(d)** t-G curve

In Fig.2(c), the v-i curve which is demonstrated as a pinched hysteresis loop passing the origin with current direction for the voltage up and down is shown, along with the three different slopes represents the memconductance that verifies the effectiveness of this model. Concretely, corresponding to the applied signal shown in Fig.2(a), the v-i curve starts from point ①, at this point the memristor is in its initial state ($\varphi(0)$=-0.4Wb, G=0.1S, as shown in Fig.2(b) and Fig.2(d)). Before reaching point ②, the flux accumulated in the memristor is less than -0.3Wb, so the memconductance value remains unchanged. Once the flux reaches -0.3Wb at point ②, the memconductance changes to 0.9S. With the flux increasing over time, when the flux reaches +0.3Wb at point ③, the memconductance changes to 0.4S. The point of inflexion in this case happens at the point ④, where the applied voltage direction is changed, and the flux accumulated in the memristor starts decreasing. at point ⑤, where the flux is less than +0.3Wb, the memconductance changes to 0.9S. When then flux is less than -0.3Wb at point ⑥, the memconductance becomes 0.1S. With the flux decreasing continuously, returning from point ⑦ to the origin point ①, the magnetic flux of the memristor also returns to the initial value -0.4Wb. Fig.2(d) is the time-varying curve of the memconductance, it can be seen that over one cycle, the memconductance changes among 0.1S, 0.9S, and 0.4S.

2.2 Spice modeling of a voltage-controlled tri-state memristor

With the tri-state memristor model having been proposed, it is necessary to use analog circuit simulation software to establish the corresponding tri-state memristor circuit model for further studying on it. As we known, the proposed tri-state memristor is an ideal memristor, to build a Spice model, it is necessary to introduce a 'sibling' of the ideal memristor, namely, the ideal-generic memristor. In fact, every ideal memristor has countless siblings. When the same input signal is applied to an ideal memristor and its siblings, and the initial conditions correspond to each other, and then the hysteresis curves of the two types of memristors in the voltage-current plane are completely consistent. The ideal-generic voltage-controlled memristor form is:

$$\begin{cases} i = G(x)v \\ \dfrac{dx}{dt} = g(x)v \end{cases} \tag{3}$$

where x is the internal state variable of the ideal voltage-controlled generic memristor model, $G(x)$ is the memconductance, and the function $g(x)$ is multiplied by the input voltage v to describe the internal state variable x of the voltage-controlled memristor.

According to the algorithms to calculate the siblings of ideal memristors in [22], the siblings of the voltage-controlled tri-valued memristor model we built can be established.

Firstly, according to the constitutive relationship of the memristor defined by Eq. (1), a linear differentiable 1:1 function $x(\varphi)$ with respect to flux φ is chosen as:

$$x = x(\varphi) = 2.125\varphi - 1.875|\varphi| \tag{4}$$

Secondly, the inverse function $x^{-1}(x)$ of the function $x(\varphi)$ is found as bellow:

$$\varphi = x^{-1}(x) = 2.125x + 1.875|x| \tag{5}$$

Then, by substituting Eq.(5) into Eq.(2), the memconductance related to the internal state variable x can be calculated:

$$\begin{aligned} G(x) = {} & 0.25 + 0.4\,\mathrm{sgn}\left(2.125x + 1.875|x| + 0.3\right) \\ & - 0.25\,\mathrm{sgn}\left(2.125x + 1.875|x| - 0.3\right) \end{aligned} \tag{6}$$

And the expression of $g(x)$ can be obtained as:

$$\begin{aligned} g(x) = \left.\frac{dx(\varphi)}{d\varphi}\right|_{\varphi=x^{-1}(x)} &= 2.125 - 1.875\,\mathrm{sgn}(\varphi)\Big|_{\varphi=x^{-1}(x)} \\ &= 2.125 - 1.875\,\mathrm{sgn}\left(2.125x + 1.875|x|\right) \end{aligned} \tag{7}$$

Finally, referring to Eq.(3), the expression of a sibling created by the ideal voltage-controlled tri-state memristor can be expressed as:

$$\begin{cases} i = G(x)v = \begin{bmatrix} 0.25 + 0.4\,\mathrm{sgn}\left(2.125x + 1.875|x| + 0.3\right) \\ -0.25\,\mathrm{sgn}\left(2.125x + 1.875|x| - 0.3\right) \end{bmatrix} v \\ \dfrac{dx}{dt} = g(x)v = \left[2.125 - 1.875\,\mathrm{sgn}\left(2.125x + 1.875|x|\right)\right] v \end{cases} \tag{8}$$

When the initial flux of the memristor is set to $\varphi(0)$=-0.4, the initial state $x(0)$ of the memristor can be obtained by the following calculation:

$$x(0) = x(\varphi(0)) = 2.125\varphi(0) - 1.875|\varphi(0)| = 2.125\times(-0.4) - 1.875\times|-0.4| = -1.6 \tag{9}$$

Table 1 Spice subcircuit description of ideal voltage-controlled generic tri-state memristor

*Tri-state Memristor Model
* TE - top electrode
* BE - bottom electrode
* XSV - External connection to plot state variable
* that is not used otherwise
.subckt Tri-valued Memristor TE BE XSV

```
* Fitting parameters to model different devices
*a,b,c,d:        Parameters for G(V)
* xo:            Initial value of SV
.params  a=0.25 b=0. 4 c=0. 25 d=0.3 x0=-1.6
.func abs(V) =IF(V <= 0, -V, V)
.func sgn(V) =IF(V <= 0, -1, 1)
* Memristor G(V)
.func G(V) =a+b*sgn(2.125*V+1.875*abs(V)+d)-
c*sgn(2.125*V+1.875*abs(V)-d)
*IV Response
.func IVRel(V1,V2) = V1*G(V2)
Cx XSV 0 {1}
.ic V(XSV) = x0
*Circuit to determine state variable
*dx/dt=g(x)*V
Gx 0 XSV value={(2.125-
1.875*sgn(2.125*V(XSV,0)+1.875*abs(V(XSV,0))))*
V(TE,BE)}
*Current source for memristor IV response
Gm TE BE value = {IVRel(V(TE,BE),V(XSV,0))}
.ends Tri-valued Memristor
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According to Eq.(8), the Spice model can be designed as shown in Fig.3, and the corresponding program statements can be written as shown in Table 1[23]. Then a packaged equivalent circuit model of the proposed memristor can be obtained as shown in Fig.4.

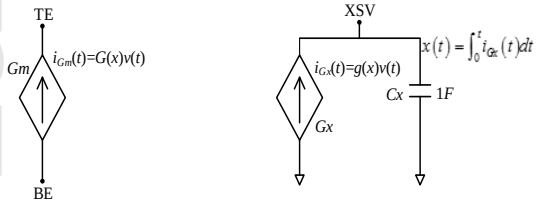


Fig. 3. *Spice model of the proposed tri-state memristor*

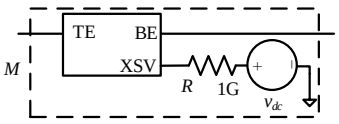
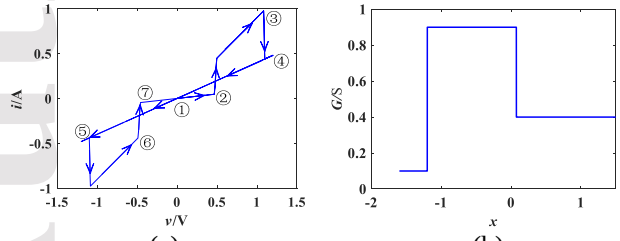


Fig.4. *LTspice equivalent model of the tri-state memristor*

For the sake of verifying the validity of the Spice model established, by applying a sinusoidal excitation voltage $v(t)$=1.2sin(2πft) to this circuit model, the circuit simulation results are obtained as shown in Fig.5, which illustrates the established circuit model conforms to the experimental definition of memristors, the circuit model is effective.



(a) (b)

Fig. 5. *Characteristic curves of voltage-controlled tri-state memristor model*(f=0.159Hz, x(0)=-1.6)
(a) *v-i* curve, **(b)** *x-G* curve

3 Characteristic analysis of series-parallel circuit of the tri-state memristors

For simplicity, the series and parallel circuits composed of two tri-state memristors M_1 and M_2 are analyzed in detail. Considering that the internal parameters of the memristor affects the series and parallel results, both circuits are divided into two sub-cases for analysis. In the first case, two identical memristors are connected in series and parallel, and in the second case, the two memristors are mismatched due to parameter variation. Here, M_1 is as shown in Eq.(10), and M_2 is a memristor with internal variable parameters b_2, c_2, d_2, e_2 as shown in Eq. (11), where b_2, c_2 and d_2 control the size of the memconductance, e_2 determines the switching point of the memconductance. $\varphi_1(t)$ and $\varphi_2(t)$ are the flux through the tri-state memristors M_1 and M_2, respectively.

$$G_1(t)=0.25+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)-0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right) \tag{10}$$

$$G_2(t)=b_2+c_2\,\mathrm{sgn}\left(\varphi_2(t)+e_2\right)-d_2\,\mathrm{sgn}\left(\varphi_2(t)-e_2\right) \tag{11}$$

Table 2 Parameter values of the tri-valued memristor M_2

Parameters of M_2	(b_2	c_2	d_2)	e_2
Case1	0.25	0.4	0.25	0.3
Case2	0.35	0.5	0.35	0.3
Case3	0.25	0.4	0.25	0.1
Case4	0.35	0.5	0.35	0.1

The internal parameters of M_2 are divided into two groups: (b_2, c_2, d_2) and e_2. According to the control variate method, the internal parameters of M_2 have four cases, as shown in Table 2. Case 1 indicates that the two internal parameters of memristor M_2 are the same as those of M_1, Case 2 and Case 3 represent that there is only one group of parameters of memristor M_2 and M_1 is same, and Case 4 shows that both parameter groups of M_2 are different from those of M_1. It is noteworthy that all the initial values, input voltage amplitudes and frequencies are needed to satisfy the conditions for the tri-state memristor to obtain three distinguishable resistance states in the simulations.

Next, the series-parallel connection rules of a pair of tri-state memristors in the aforementioned four cases will be analyzed in detail.

3.1 Analysis of the characteristics of the tri-state memristor series circuit

The charges that go through M_1 and M_2 are assumed to be $q_1(t)$ and $q_2(t)$, respectively. When the two memristors are connected in series, the equivalent memconductance, charge, and flux are expressed by $G(t)$, $Q(t)$ and $\Phi(t)$. Then the following relationship can be met:

$$Q(t)=q_1(t)=q_2(t)\quad \Phi(t)=\varphi_1(t)+\varphi_2(t) \tag{12}$$

According to the definition of memristor and combined with Eq. (12), the equivalent memconductance $G(t)$ of the series circuit in the same direction can be given as:

$$G(t)=\frac{1}{\frac{1}{G_1(t)}+\frac{1}{G_2(t)}}=\frac{G_1(t)G_2(t)}{G_1(t)+G_2(t)} \tag{13}$$

It can be manifested from formula (10), (11) and (13) that when the parameters of the two memristors are identical, that

is, when the value of M_2 corresponds to Case 1 in Table 2, the flux through the two memristors in the series circuit is the same, namely, $\varphi_1(t)=\varphi_2(t)$. At this time, the series circuit is equivalent to a tri-state memristor, and the expression of its equivalent memconductance $G(t)$ is as follows:

$$\begin{aligned} G(t) &= \frac{G_1(t)}{2} \\ &= \frac{0.25+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)-0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right)}{2} \\ &= \begin{cases} 0.05, & \varphi_1(t)<-0.3 \\ 0.45, & -0.3\le\varphi_1(t)\le 0.3 \\ 0.20, & \varphi_1(t)>0.3 \end{cases} \end{aligned} \tag{14}$$

When the parameters of the two tri-state memristors are not completely the same, that is, the value of M_2 corresponds to the three cases of Case 2, Case 3 and Case 4, the flux flowing through the two memristors is different, in other words, $\varphi_1(t) \neq \varphi_2(t)$. At this time, the circuit is equivalent to a penta-state (five-valued) memristor, and the equivalent memconductance is determined by the internal parameters of the two memristors. Taking Case 4 in Table 2 as an example, the equivalent memconductance $G(t)$ can be calculated:

$$G(t)=\frac{G_1(t)G_2(t)}{G_1(t)+G_2(t)}=\begin{cases} 0.067, & \varphi_1(t)<-0.3,\varphi_2(t)<-0.1 \\ 0.163, & -0.3\le\varphi_1(t)\le 0.3,\varphi_2(t)<-0.1 \\ 0.514, & -0.3\le\varphi_1(t)\le 0.3,-0.1\le\varphi_2(t)\le 0.1 \\ 0.321, & -0.3\le\varphi_1(t)\le 0.3,\varphi_2(t)>0.1 \\ 0.222, & \varphi_1(t)>0.3,\varphi_2(t)>0.1 \end{cases} \tag{15}$$

For the series connection of two tri-state memristors with opposing polarities, as the direction of the tri-state memristor M_1 is the same as the reference direction, and memristor M_2 is opposite to the reference direction, the conductance of M_2 will always appear as the maximum resistance among the three resistances, that is, the minimum memconductance value b_2-c_2+d_2 according to Eq.(11). Therefore, the value of M_2 in Table 2 can be summed up as two cases, one case includes Case 1 and Case 3 with a memconductance of 0.1S, and the other case include Case 2 and Case 4 with a memconductance of 0.2S. Hence, when M_1 and M_2 are connected in reverse series, the circuit can still be equivalent to a tri-state memristor. For example, when M_2 is 0.1S, the equivalent memconductance $G(t)$ of the circuit is described as follows:

$$\begin{aligned} G(t) &= \frac{G_1(t)G_2(t)}{G_1(t)+G_2(t)} \\ &= \frac{0.1\times\left[0.25+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)-0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right)\right]}{0.35+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)-0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right)} \\ &= \begin{cases} 0.05, & \varphi_1(t)<-0.3 \\ 0.09, & -0.3\le\varphi_1(t)\le 0.3 \\ 0.08, & \varphi_1(t)>0.3 \end{cases} \end{aligned} \tag{16}$$

3.2 Analysis of the characteristics of the tri-state memristor parallel circuit

In the parallel circuit, the flux flowing through each memristor is identical. According to the parallel circuit law, we can derive the following constituent expressions:

$$\Phi(t)=\varphi_1(t)=\varphi_2(t) \quad Q(t)=q_1(t)+q_2(t) \tag{17}$$

Then the equivalent memconductance $G(t)$ of parallel circuit can be expressed as:

$$G(t)=G_1(t)+G_2(t) \tag{18}$$

From the Eqs. (17) and (18), it can be seen that the two memristors M_1 and M_2 in the parallel circuit under the same direction are with the same flux, when e_2=0.3(corresponding to the case1 and case 2 in Table 2), M_1 and M_2 are with the same turning point in the q-φ curve, so that the memcondutance of them will change at the same time, so in this case the parallel equivalent circuit appears as a tri-state memristor. When $e_2\neq$0.3, corresponding to Case 3 and Case 4 in Table 2, the two memristors will with different turning points, then the crossover change of M_1 and M_2 makes the parallel equivalent circuit behave as a penta-state memristor. Here we express the specific calculation of the equivalent memconductances of the parallel circuit with the same direction when M_2 in Case 1 and Case 4 in Eq.(19) and (20):

$$\begin{aligned} G(t)_{case1} &= G_1(t)+G_2(t) \\ &= 2\times\left[0.25+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)-0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right)\right] \\ &= \begin{cases} 0.2, & \varphi_1(t)<-0.3 \\ 1.8, & -0.3\le\varphi_1(t)\le 0.3 \\ 0.8, & \varphi_1(t)>0.3 \end{cases} \end{aligned} \tag{19}$$

$$\begin{aligned} G(t)_{case4} &= G_1(t)+G_2(t) \\ &= 0.6+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)+0.5\,\mathrm{sgn}\left(\varphi_1(t)+0.1\right) \\ &\quad -0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right)-0.35\,\mathrm{sgn}\left(\varphi_1(t)-0.1\right) \\ &= \begin{cases} 0.3, & \varphi_1(t)<-0.3 \\ 1.2, & -0.3\le\varphi_1(t)<-0.1 \\ 2.1, & -0.1\le\varphi_1(t)\le 0.1 \\ 1.4, & 0.1<\varphi_1(t)\le 0.3 \\ 0.9, & \varphi_1(t)>0.3 \end{cases} \end{aligned} \tag{20}$$

Similar to the analysis of the reverse series circuit, in the reverse parallel circuit, it is assumed that M_1 is connected to the circuit in the forward direction, and M_2 is connected in the reverse direction. At this moment, the circuit can be regarded as a tri-state memristor and a single-valued memristor in parallel, and the parallel result is equivalent to a tri-state memristor too. Take M_2 =0.1S (Case 1 and Case 3 in Table 2) as an example, the equivalent memconductance $G(t)$ of the circuit can be calculated as:

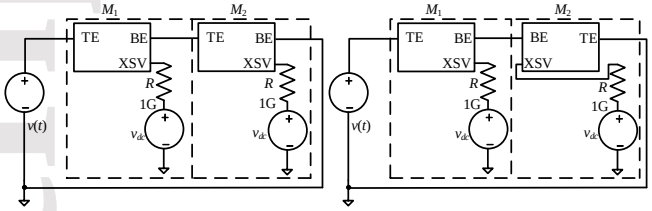
$$\begin{aligned} G(t) &= G_1(t)+G_2(t) \\ &= 0.35+0.4\,\mathrm{sgn}\left(\varphi_1(t)+0.3\right)-0.25\,\mathrm{sgn}\left(\varphi_1(t)-0.3\right) \\ &= \begin{cases} 0.2, & \varphi_1(t)<-0.3 \\ 1.0, & -0.3\le\varphi_1(t)\le 0.3 \\ 0.5, & \varphi_1(t)>0.3 \end{cases} \end{aligned} \tag{21}$$

4 LTSpice simulation analysis of series-parallel circuits of tri-state memristor

In order to verify the correctness of the aforementioned theoretical analysis results, the LTspice circuit simulations are performed in the following parts.

4.1 Simulation analysis of LTspice circuit of tri-state memristor series circuit

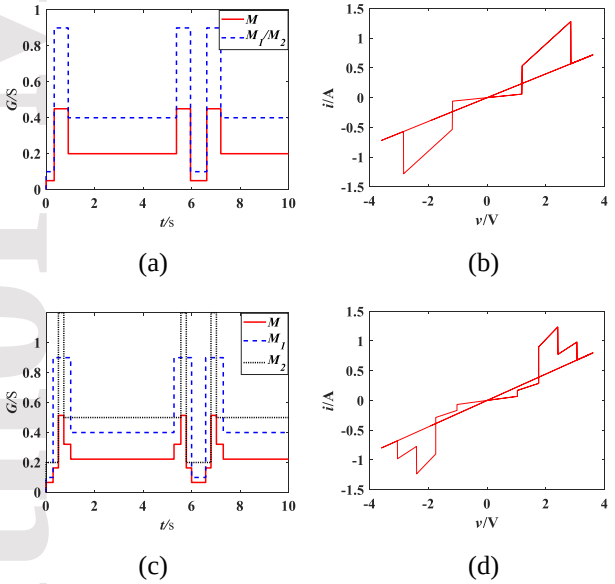
Consider the series circuit composed of two tri-state memristors. The specific circuits are shown in Fig.6, and all the simulations are done by applying a sinusoidal voltage $v(t)=3.6\sin(2\pi ft)$, f =0.159Hz as the driving voltage.



(a) (b)

Fig. 6. *Tri-state memristor series circuit*
(a) Series with same direction,
(b) Series with reverse direction

4.1.1 Simulation analysis of LTspice circuit of the tri-state memristor in series with same direction: The series circuit with the same direction as shown in Fig.6(a) in LTspice. Under the given excitation voltage, the *t-G* and *v-i* curves of a single tri-valued memristor and two tri-valued memristors in series in the same direction can be obtained as shown in Fig.7. Fig.7(a) and (c) demonstrate the G-t relations when M_2 in both case 1 and case 4 in Table 2, from which we can see that the memconductance values of the series equivalent circuit are consistent with the calculation results of Eqs. (14) and (15). Fig.7(b) and (d) are the *v-i* relation of each equivalent circuit when M_2 in case1 and case 4 .



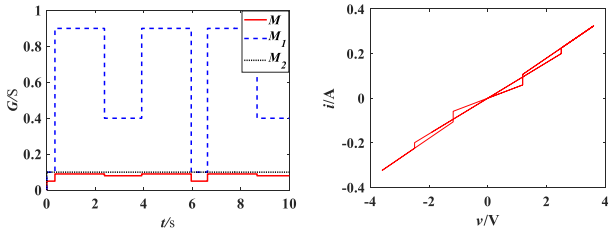
(a) (b)

(c) (d)

Fig. 7. *Characteristic curves of two tri-state memristors in series with same direction*
(a) *t-G* curves of Case 1, **(b)** *v-i* curve of Case 1, **(c)** *t-G* curves of Case 4, **(d)** *v-i* curve of Case 4

In Fig.7(a) and (c), the abscissa represents time and the ordinate denotes the memconductance of a single tri-state memristor(blue and black colour) and equivalent memconductance in a series circuit(red colour).The experimental results verified that under the above parameters, when two same tri-state memristors are connected in series in the same direction, the equivalent circuit will be taken as a new tri-state memristor. At any time t, the equivalent memconductance of the circuit is 1/2 times that of a single tri-valued memristor. When two different tri-state memristors are connected in series in the same direction, the circuit can be equivalent to a penta-state memristor, whose equivalent memconductance satisfies Eq.(15) as shown in Fig.7(c).

4.1.2 Simulation analysis of LTspice circuit of tri-state memristor in series with reverse direction: The corresponding circuit is as shown in Fig.6(b), by simulation the *t-G* and *v-i* characteristic curves can be shown in Fig.8, where M_2=0.1S, corresponding to Case 1 and Case 3 in Table 2, and the memconductance value of the equivalent circuit is consistent with Eq. (16).



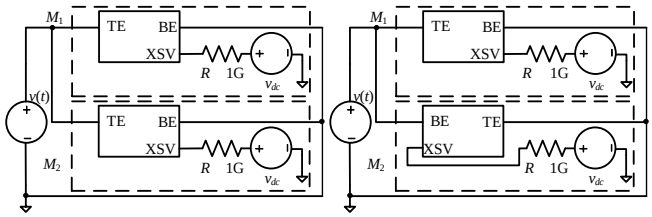
(a) (b)

Fig. 8. *Characteristic curves of two tri-state memristors in series with reverse direction*
(a) *t-G* curves, **(b)** *v-i* curve

In Fig.8 (a), the red line denotes the *t-G* curve after the two tri-state memristors are connected in reverse, and the blue and black lines express the *t-G* curves of the ternary memristors M_1 and M_2, respectively. Fig.8 (b) shows the *v-i* characteristic curve of the equivalent circuit. The simulation results in Fig. 8 indicate that two tri-state memristors connected in reverse series is equivalent to a tri-state memristor.

4.2 Simulation analysis of LTspice circuit of the tri-state memristor parallel circuit

Similar to the tri-state memristor series circuits, the parallel circuits composed of two tri-state memristors are shown in Fig.9.



(a) (b)

Fig. 9. *Tri-state memristor parallel circuit*
(a) Parallel with same direction,
(b) Parallel with reverse direction

4.2.1 Simulation analysis of LTspice circuit of tri-state memristor in parallel with same direction: In order to verify the characteristics of the tri-valued memristor parallel circuit in the same direction, the LTSpice circuit as shown in Fig.9(a) is constructed, and the sinusoidal excitation voltage $v(t)=3.6\sin(2\pi ft)$ with frequency f=0.159Hz is applied to the circuit. The experimental results in two cases can be obtained

as shown in Fig.10, where Fig.10(a) and (b) correspond to Case 1, Fig.10(c) and (d) correspond to Case 4 in Table 2. The memconductance values of the parallel equivalent circuit are consistent with Eq.s (19) and (20).

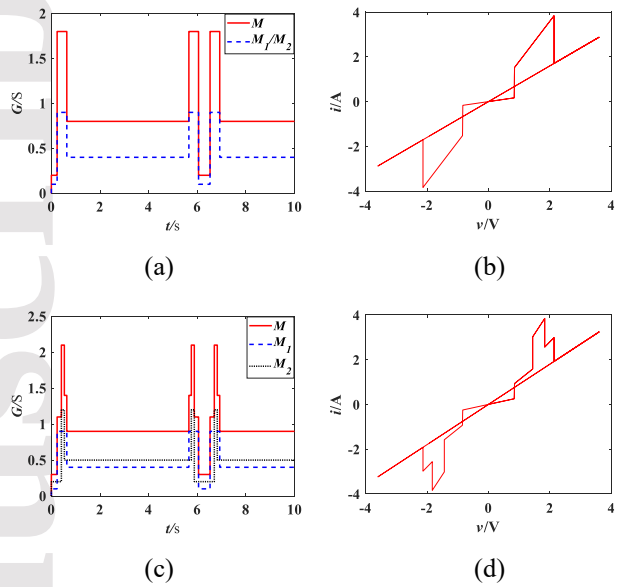


Fig. 10. *Characteristic curves of two tri-valued memristors in parallel with same direction*
(a) *t-G* curves of Case 1, **(b)** *v-i* curve of Case 1, **(c)** *t-G* curves of Case 4, **(d)** *v-i* curve of Case 4

The results in Fig.10 demonstrate that after two tri-state memristors with the same parameters are connected in parallel in the same direction, the circuit is equivalent to a new tri-state memristor, and the memconductance of its equivalent circuit is equal to 2 times the corresponding memconductance of a single tri-state memristor. In a parallel circuit composed of two tri-state memristors with different parameters, when parameters e_2 are the same in these two memristors, the circuit is equivalent to a new tri-state memristor. When parameters e_2 are different, the circuit will be equivalent to a penta-state memristor, and its equivalent memconductance is equal to the sum of the memconductances of the two memristors.

4.2.2 Simulation analysis of LTspice circuit of the tri-state memristor in parallel with reverse direction: The parallel circuit with reverse direction is as shown in Fig.9(b). And Fig.11 shows the memconductance of the equivalent circuit in Eq. (21) and the *t-G* and corresponding *v-i* characteristic curves of the parallel circuit in Case 1. It can be seen that when two same tri-state memristors are connected in parallel in a reverse direction, the circuit is equivalent to a tri-state memristor.

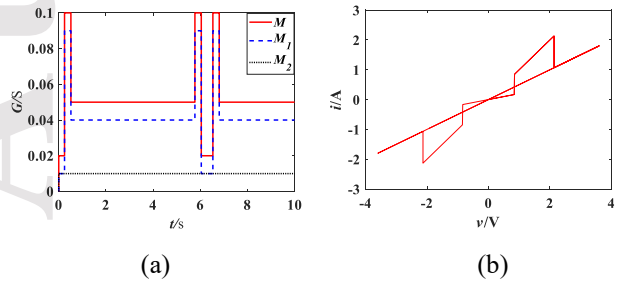


Fig. 11. *Characteristic curves of two tri-state memristors in parallel with reverse direction*
(a) *t-G* curves, **(b)** *v-i* curve

5 Conclusion

In this paper, a Spice circuit model of the proposed tri-state memristor is constructed, and the composite characteristics of tri-state memristor series and parallel circuits are analyzed. Specifically, the equivalent memconductance expressions of two tri-state memristor series-parallel circuits are theoretically derived, and the effect of the parameter consistency of the tri-state memristors on the equivalent memconductance of the series-parallel circuit is analyzed. It is found that the equivalent memristance of the series circuit of the memristor is equal to the algebraic sum of the memristance of each memristor. The equivalent memconductance of a parallel circuit composed by two memristor is equal to the algebraic sum of the memconductance of the two memristors, and the internal parameters of the tri-valued memristor determine the values and state number of equivalent resistances of the series-parallel circuit.

In addition, the series-parallel circuits consisting of two tri-state memristors were verified through circuit simulation. And all the simulation results are consistent with the theoretical analysis, confirming the validity of the theoretical derivation. Distinct from previous research, this paper uses the tri-state memristor model with significant application potential to carry out systematic theoretical research and circuit verification on series-parallel circuits, which provides a theoretical basis and experimental reference for subsequent research of compositely connected memristor circuits.

6. Acknowledgments

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