Upgrades of the ATLAS Muon Spectrometer Front-end Electronics for the High-Luminosity LHC

by

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ASD Amplifier Shaper Discriminator

BCR Bunch Counter Reset

BC Bunch Crossing

BER Bit Error Rate

BGA Ball Grid Array

BSM Beyond Standard Model

BW Big Wheel

CSC Cathode Strip Chamber

CSM Chamber Service Module

DNL Differential Non-Linearity

FELIX Front-End Link Exchange

FPGA Field Programmable Gate Array

GUI Graphical User Interface

HL-LHC High-Luminosity LHC

IBERT Integrated Bit Error Ratio Tester

INL Integral Non-Linearity

L0A L0 Accept

L1A L1 Accept

L1DDC Level-1 Data Driver Card

L1 Level-1

LDO Low-DropOut

LHC Large Hadron Collider

LUT Lookup Table

LVCMOS Low-Voltage Complementary Metal Oxide Semiconductors

LVDS Low-Voltage Differential Signaling

LV Low voltage

MC Monte Carlo

MDT Monitored Drift Tube

mini-DAQ mini data acquisition

MIP Minimum Ionizing Particle

MM MicroMegas

MO Monitored Output

MPV Most Probable Value

MS Muon Spectrometer

NIM Nuclear Instrumentation Module

NSW New Small Wheel

I/O Input and Output

pFEB pad Front-End Board

PLL Phase Locked Loop

PRBS Psuedo-Random Binary Sequence

RMS Root-Mean-Square

ROC Readout Controller

ROI Region of Interest

RPC Resistive Plate Chamber

sFEB strip Front-End Board

SLVS Scalable Low-Voltage Signaling

SM Standard Model

SNR Signal-to-Noise Ratio

sTGC small-strip Thin Gap Chamber

TDAQ trigger and data acquisition

TDC Time-to-Digital Converter

TDS Trigger Data Serializer

TGC Thin Gap Chamber

TMR Triple Module Redundancy

ToT Time-over-Threshold

TP Test Pulse

TTC Time, Trigger, and Control

DAC Digital-to-Analog Converter

ADC Analog-to-Digital Converter

ABSTRACT

The Large Hadron Collider (LHC) is the world's largest and most powerful particle accelerator. The High-Luminosity LHC (HL-LHC) is an upgraded version of the LHC that will further increase the instantaneous luminosity by a factor of $5-7.5$ and the integrated luminosity by a factor of 10. The ATLAS detector is one of the two general-purpose detectors at the LHC. It offers unique opportunities to study properties of fundamental particles and explore physics beyond the Standard Model. The current detector needs to be upgraded to maintain or improve its performance to profit from the HL-LHC operation. Two major upgrades, the Phase-I upgrade and the Phase-II upgrade, have been planned and they are both 10-year-long projects.

The integration and commissioning of the Phase-I upgrade happened during the period between 2019 and 2021. The innermost endcap station of the ATLAS Muon Spectrometer was replaced by a New Small Wheel (NSW) detector to reduce fake muon triggers and to improve offline muon track measurements for future HL-LHC runs. The small-strip Thin Gap Chamber (sTGC) is the primary trigger detector for the NSW. It utilizes the sTGC pad detector to form a coarse region of interest (ROI) and read out the charge information from the sTGC strip detector underneath the ROI. The charge information is further used to generate trigger primitives for the first-level trigger. This dissertation presents the design of a mobile data acquisition system and its application to the sTGC trigger chain integration and commissioning. This dissertation also presents cosmic ray studies with an sTGC chamber, which provides first insights into the performance of the sTGC detector in the trigger chain with final front-end electronics. For the first time, the sTGC strip charges from the detector were read out through the trigger chain data path.

The integration and commissioning of the Phase-II upgrade will happen during the period between 2025 and 2027. The primary muon tracking detector, Monitored Drift Tube (MDT), will also be used as a trigger device at the first trigger level to improve the trigger muon momentum resolution. The present MDT electronic system can not offer enough bandwidth for the increased event rate (by about an order of magnitude) at the HL-LHC. As a result, all MDT front-end and back-end electronics need to be replaced. This dissertation presents the development of a Time-to-Digital Converter (TDC) Application-Specific Integrated Circuit (ASIC) for the new MDT front-end elec-

tronics. The TDC provides digitization of the rising and falling edges of the earliest arrival signal, which is the basis for all subsequent trigger and readout processing. Detailed performance studies have been performed on the produced prototype chips.

CHAPTER 1

Introduction

Particle physics, a branch of physics, studies fundamental constituents of matter and their interactions (forces) [1]. Figure 1.1 presents the summary of all elementary particles we observed so far. These particles are divided into two categories: matter particles and force carriers. Matter particles are the most basic building blocks of all matter in nature, and force carriers mediate forces between matter particles. There are four fundamental forces at work in the Universe: the electromagnetic force, the weak force, the strong force, and the gravitational force. All the known forces of nature can be traced to these four fundamental forces.

All matter particles are fermions carrying half-integer spins. They cannot occupy the same state at once and thus obey the Fermi-Dirac statistics. They can be further be divided into quarks and leptons. There are six flavors of quarks grouped into three generations (also called families) of doublets: up quark (u) and down quark (d) for the first generation, charm quark (c) and strange quark (s) for the second generation, and top quark (t) and bottom quark (b) for the third generation. The up, charm and top quarks carry an electrical charge of $\frac{2}{3}e$ and the other three quarks carry an electrical charge of $-\frac{1}{3}e$. Leptons also have six flavors and are also grouped in three generations: electron (e) and electron neutrino (ν_e) for the first generation, muon (μ) and muon neutrino (ν_μ) for the second generation, and tau(τ) and tau neutrino (ν_τ) for the third generation. Electron, muon and tau have an electrical charge of $-e$ while the three neutrinos are charge neutral. Quarks carry color charges while leptons are colorless. Each of the 12 fermions has its corresponding anti-particle, which has the same mass but opposite electric charge.

All force carriers are bosons carrying integer spins. They can occupy the same state at once and thus obey the Bose-Einstein statistics. Electromagnetic forces are transferred between charged particles through the exchange of massless bosons called photons (γ). Weak forces are responsible for the radiative decay of atoms and can change one type of subatomic particle into another. In the weak interaction, fermions can exchange three types of force carriers, namely W^+, W^- and Z bosons. These bosons are massive with the $W^\pm$ boson mass around 80 GeV and the Z boson mass around 91 GeV. Strong forces bind quarks together in cluster to make other subatomic particles,

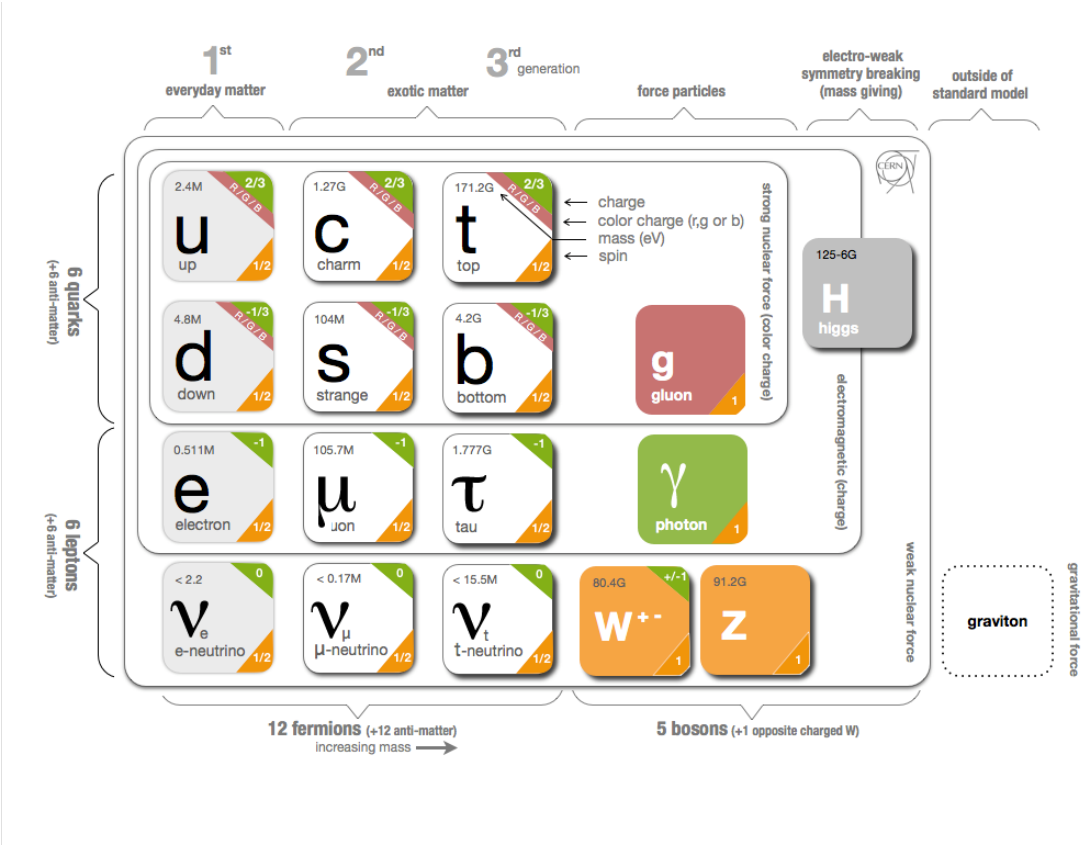


Figure 1.1: Summary of all elementary particles [2].

such as protons and neutrons. Massless gluons (g) are the mediators for strong forces. There is a hypothesized mediator, the graviton (G), for gravity, but it has not been observed experimentally.

The Higgs boson is a scalar boson with zero spin, no electric charge, and no color charge. It is the only elementary scalar particle we observed so far. The Higgs boson is the excitation of the Higgs field that permits the Universe. Matter particles acquire their masses through their interactions with the Higgs field [3–5]. The Higgs boson was first observed by the ATLAS and CMS experiments at CERN's Large Hadron Collider (LHC) in 2012 [6, 7].

Our best understanding of matter particles and the electromagnetic, weak and strong forces is encapsulated in the Standard Model (SM) [8–11] of particle physics . Developed in the early 1970s, it has successfully explained almost all experimental results and precisely predicted a wide variety of phenomena. However, it is an incomplete theory. It does not describe gravity which is one of the four fundamental forces. It does not include dark matter and dark energy indicated by astrophysical measurements. It does not explain the origin of non-zero neutrino masses. All of those questions drive us to explore physics Beyond Standard Model (BSM).

Particle physicists use high energy accelerators to study properties of fundamental particles and

to search for BSM physics. The LHC is currently the world's highest energy proton-proton (pp) collider. It has run successfully over the last ten years with the discovery of the Higgs boson being the highlight. The High-Luminosity LHC (HL-LHC) is an upgrade of the LHC to increase the pp collision data sample by an order of magnitude to reach $3000-4000$ fb^{-1} (about 150 fb^{-1} of data collected during the past ten years) [12]. The peak instantaneous luminosity will be increased to $5-7.5\times10^{34}$ cm^{-2}s^{-1}, compared to the nominal value of 1.0×10^{34} cm^{-2}s^{-1} for the LHC. The large dataset delivered by the HL-LHC will substantially boost the accelerator's potential for new physics discoveries and greatly improve the precision to study the properties of the Higgs boson.

The HL-LHC era offers exciting physics possibilities, albeit with substantial experimental challenges. The increases in both the integrated and instantaneous luminosities have significant impacts on the detectors. Performance of the ATLAS detector in terms of acceptance, efficiency, and resolution for all physics objects needs to be maintained and in many systems, improved. The increase of particles produced in the collisions implies an increased radiation dose. The higher instantaneous luminosity means many more collisions occur in the same Bunch Crossing (BC). At the HL-LHC, the average number of interactions in a single crossing will increase from 25 to 200. As a consequence, the detectors at the HL-LHC will have to handle higher particle densities leading to higher detector channel occupancies and higher radiation levels.

ATLAS has programs ongoing to upgrade sub-detectors, front-end and back-end electronics, and the trigger and data acquisition (TDAQ) system to handle harsh conditions expected at the HL-LHC. ATLAS plans to have two phases of upgrade for the muon spectrometer. For the Phase-I upgrade, the endcap innermost station will be replaced by a New Small Wheel (NSW) detector to reduce fake muons found at the first trigger level and to improve offline muon track measurements. Two detector technologies will be used for the NSW detector: MicroMegas (MM) and small-strip Thin Gap Chamber (sTGC). For the Phase-II upgrade, Monitored Drift Tube (MDT) chambers will also be used as a trigger device at the first trigger level to improve the trigger-level momentum resolution for real muons. The present MDT electronic system can not offer enough bandwidth for the increased event rate (by about an order of magnitude) at the HL-LHC. As a result, both front-end and back-end electronics need to be redesigned and replaced.

The organization of this dissertation is as follows: Chapter 2 describes the LHC machine and the ATLAS detector. Chapter 3 gives a brief overview of ATLAS Phase-I and Phase-II upgrades. In Chapter 4, the sTGC front-end electronics are introduced. Chapter 5 presents the sTGC mini-DAQ system. Chapter 6 discusses the sTGC trigger chain front-end electronics commissioning task. Chapter 7 presents the study of the performance of sTGC with final front-end electronics using cosmic rays. Chapter 8 introduces the MDT front-end electronics for the Phase-II upgrade. In Chapter 9, the development of the MDT TDC is presented.

CHAPTER 2

Large Hadron Collider and the ATLAS Detector

2.1 The Large Hadron Collider

The LHC [13] is the world's most powerful particle collider. It has a circumstance of 26.7 kilometers and is located about 100 meters underground on the France-Swiss border near Geneva, Switzerland. CERN, the European Organization for Nuclear Research, operates the LHC. The LHC accelerates two beams of hadrons (protons or lead ions) to a speed faster than 99% of the speed of the light in the opposite direction [14]. The two beams collide every 25 ns, known as BC, at four Interaction Points (IPs). Each IP is equipped with a detector, and they are ATLAS [15] (A Toroidal Lhc ApparatuS), CMS [16] (Compact Muon Solenoid), ALICE [17] (A Large Ion Collider Experiment), and LHCb [18] (Large Hadron Collider beauty). ATLAS and CMS are two general-purpose detectors for exploring SM and BSM physics. ALICE is designed for heavy-ion collisions, and LHCb is primarily for b-physics studies. The layout of the LHC is presented in Figure 2.1.

The LHC aims to accelerate each proton beam to an energy of 7 TeV to reach a enter-of-mass energy ($\sqrt{s}$) of 14 TeV and an instantaneous luminosity of 1.0×10^{34} cm^{-2}s^{-1}. To achieve such high energy, a series of accelerators are used. Protons are initially produced by stripping electrons away from hydrogen atoms in a duoplasmatron source. These protons are first accelerated to 50 MeV through the LINAC linear accelerator and then to 1.4 GeV in the Proton Synchrotron Booster (PSB). Next, they are pushed to 25 GeV by the Proton Synchrotron (PS) and 450 GeV by the Super Proton Synchrotron (SPS) before injected into the LHC tunnel.

The LHC has about 10,000 superconducting dipole and quadrupole magnets operating at a temperature of -271.3°C. Each proton beam has 2,808 bunches and each bunch has about 1.2×10^{11} protons at start. The two beams collide at a rate of 40 MHz. The total number of proton collisions per second is thus about 1 billion. Since the total inelastic pp cross section is about 100 mb at $\sqrt{s} = 14$ TeV (1 b = 10^{-24} cm^{-2}), the average number of inelastic pp interactions per BC (25 ns) is about 25 for an instantaneous luminosity of 1.0×10^{34} cm^{-2}s^{-1} [20].

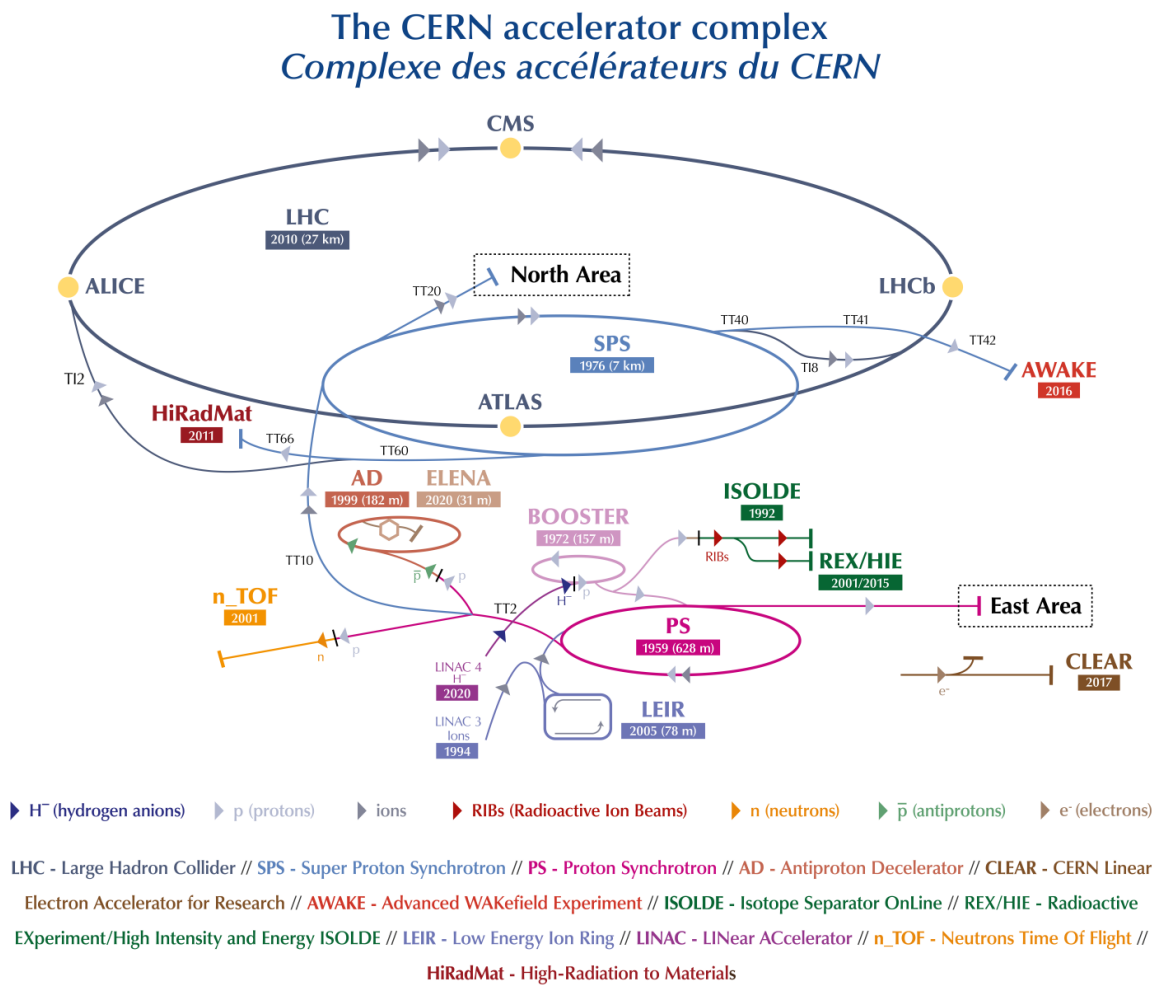


Figure 2.1: The CERN accelerator complex [19].

2.2 The ATLAS detector

The ATLAS detector, one of the two general-purpose detectors at the LHC, is the largest particle detector ever built in terms of volume. It has a cylindrical shape with a diameter of 25 m and a length of 44 m, and weighs approximately 7000 tons [15].

The two beams collide near the center of the ATLAS detector. As shown in Figure 2.2, the ATLAS detector consists of several sub-detectors surrounding the collision point. The sub-detectors, the Inner Detector [21–23], the Calorimeters [24–26], the Muon Spectrometer [27], and the magnetic systems [28], are optimized for detecting different types of particles.

The Inner Detector (ID) is in the innermost part of the ATLAS detector. It consists of a Pixel detector [29, 30], a Semi-Conductor Tracker (SCT) [31], and a Transition Radiation Tracker

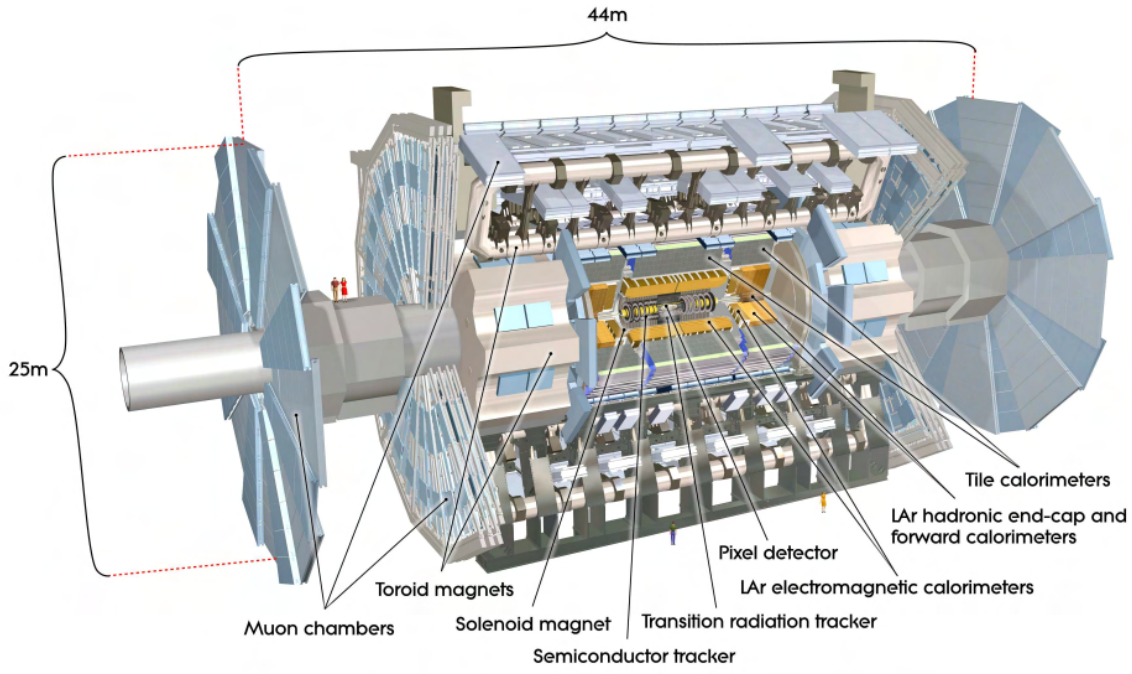


Figure 2.2: A view of the ATLAS detector [15].

(TRT) [32, 33]. The ID is immersed in a 2 Tesla solenoid magnet field [34, 35], providing precise measurements of charged particles.

Calorimeters, sitting outside of the ID, provide excellent measurements of electrons, photons, hadronic jets, and missing transverse energy. The ATLAS detector has two calorimeters: the inner electromagnetic calorimeter [36, 37] that measure electrons and photons, and the outer hadronic calorimeter [38–40] that provide measurements for hadronic jets.

The Muon Spectrometer (MS) [41–43] locates at the outmost of the ATLAS detector, and is mainly used for muon triggering, identification and momentum measurement. This is the focus of this dissertation, and more details are shown in Section 2.3.

Figure 2.3 presents simulated detector signatures for different types of particles in the ATLAS detector. Electrons and photons are both detected by the electromagnetic calorimeter. Electrons also have corresponding tracks found by the ID, while photons do not. Protons are measured by the hadronic calorimeter with matching tracks found by the ID, while neutrons are measured by the hadronic calorimeter without matching tracks in the ID. Muons do not deposit much energies in the calorimeters but will be detected by the MS. Neutrinos will not interact with the detector, leaving unbalanced momentum measurement of the calorimeters in the transverse plane.

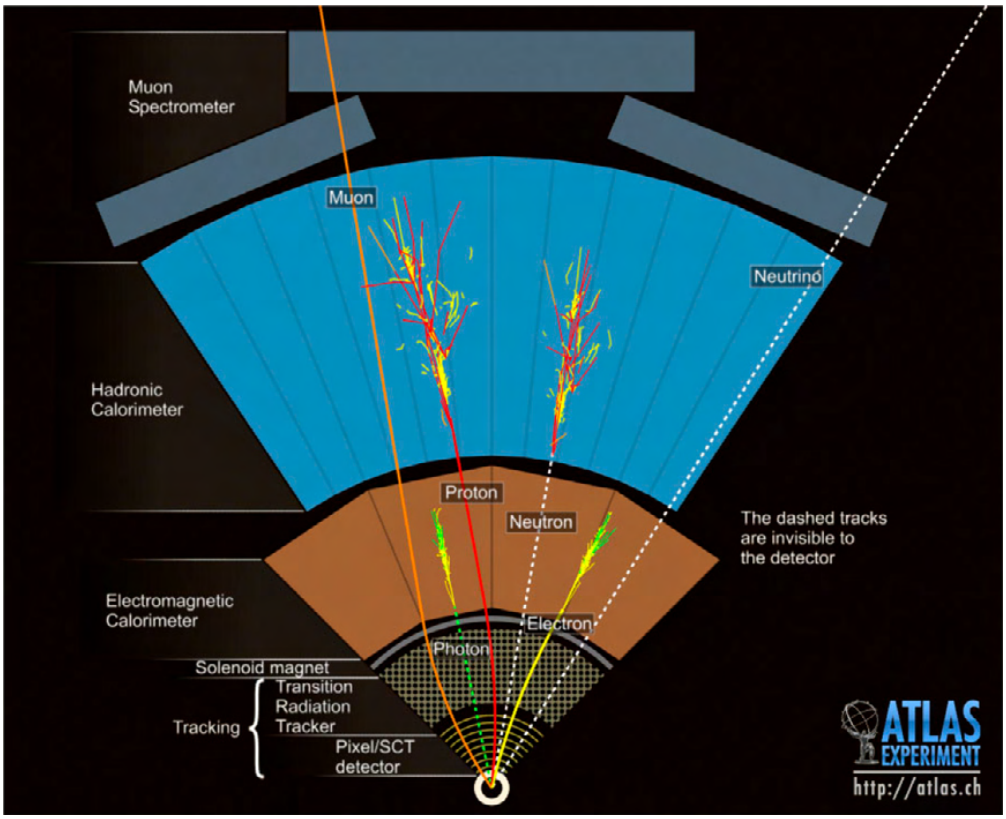


Figure 2.3: Simulated detector responses for different types of particles in the ATLAS detector [44].

2.2.1 The ATLAS coordinate system

The ATLAS collaboration uses a right-handed Cartesian coordinate system (x, y, z) with the z-axis lying along the direction of one proton beam and the origin locating at the center of the detector, as shown in Figure 2.4. The x-y (transverse) plane is perpendicular to the beam line. The positive x-direction points from the collision point to the center of the LHC, and the positive y-direction is upwards. The two sides of the detector, side-A and side-C, are defined as the positive z-direction and negative z-direction, respectively.

ATLAS also utilizes spherical coordinates (r, θ, ϕ) with the azimuthal angle (ϕ) measured around the beam line and the polar angle θ measured from the beam line. The pseudorapidity (η), a common nomenclature used in particle physics, is defined as $\eta = -\ln(\tan(\frac{\theta}{2}))$. The transverse momentum (p_T) is defined as the momentum component in the x-y plane, so do the transverse energy (E_T) and missing transverse energy (E_T^{miss}).

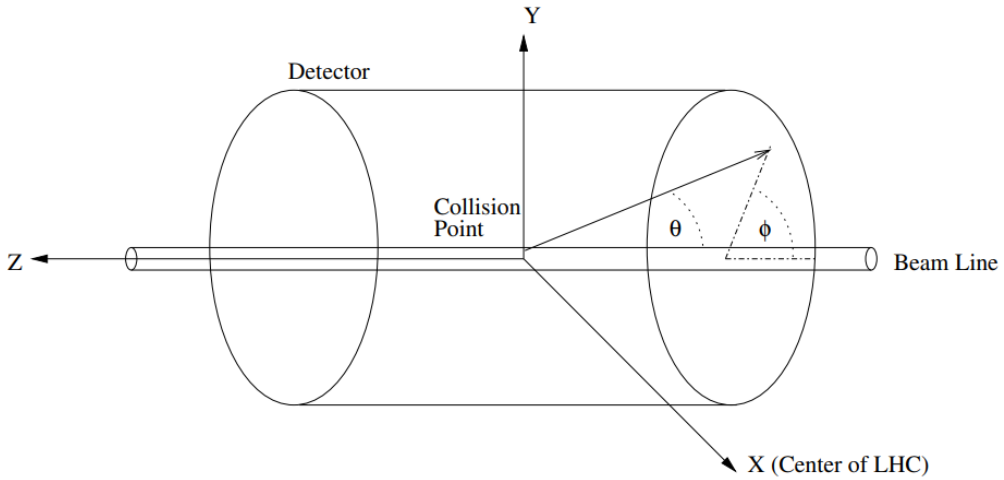


Figure 2.4: The right-handed coordinate system used by the ATLAS collaboration [45].

2.2.2 The ATLAS trigger and data acquisition system

The ATLAS detector has in total about 100 million channels. For each collision, the raw data size is ~ 1.4 MB, which means the raw data rate is ~ 60 TB/s [46]. It is unfeasible to transmit and store all of these raw data in terms of transmission bandwidth, writing speed, and storage capacity. Furthermore, only a small fraction of collision events may have interesting physics processes happened. A trigger system is needed to select potential interesting candidates for the offline storage.

The ATLAS Trigger and Data Acquisition (TDAQ) [47, 48] system is a two-stage trigger system that consists of a hardware-based Level-1 (L1) trigger and a software-based High-Level Trigger (HLT), as shown in Figure 2.5. The L1 trigger uses the information from the calorimeters and the MS to trigger on interesting events. It reduces the data rate from 40 MHz down to 100 kHz and provides a Region of Interest (ROI) to the next stage. The HLT uses a computing farm executing fast trigger and object reconstruction algorithms. It utilizes all sub-detector information within the ROIs and further reduces the data rate down to 1 kHz.

2.3 The Muon spectrometer

While most particles produced from the collisions are stopped by the calorimeters, muons and neutrinos can pass through the entire ATLAS detector. The MS is used for detecting muons. The design of the MS was driven by the need of having a standalone muon momentum measurement at a precision of 10% for 1 TeV muons [49], and having large detector acceptance for precision tracking and triggering. Precision tracking is achieved with Monitored Drift Tube (MDT) chambers and Cathode Strip Chamber (CSC). Muon triggering is accomplished using dedicated fast detectors:

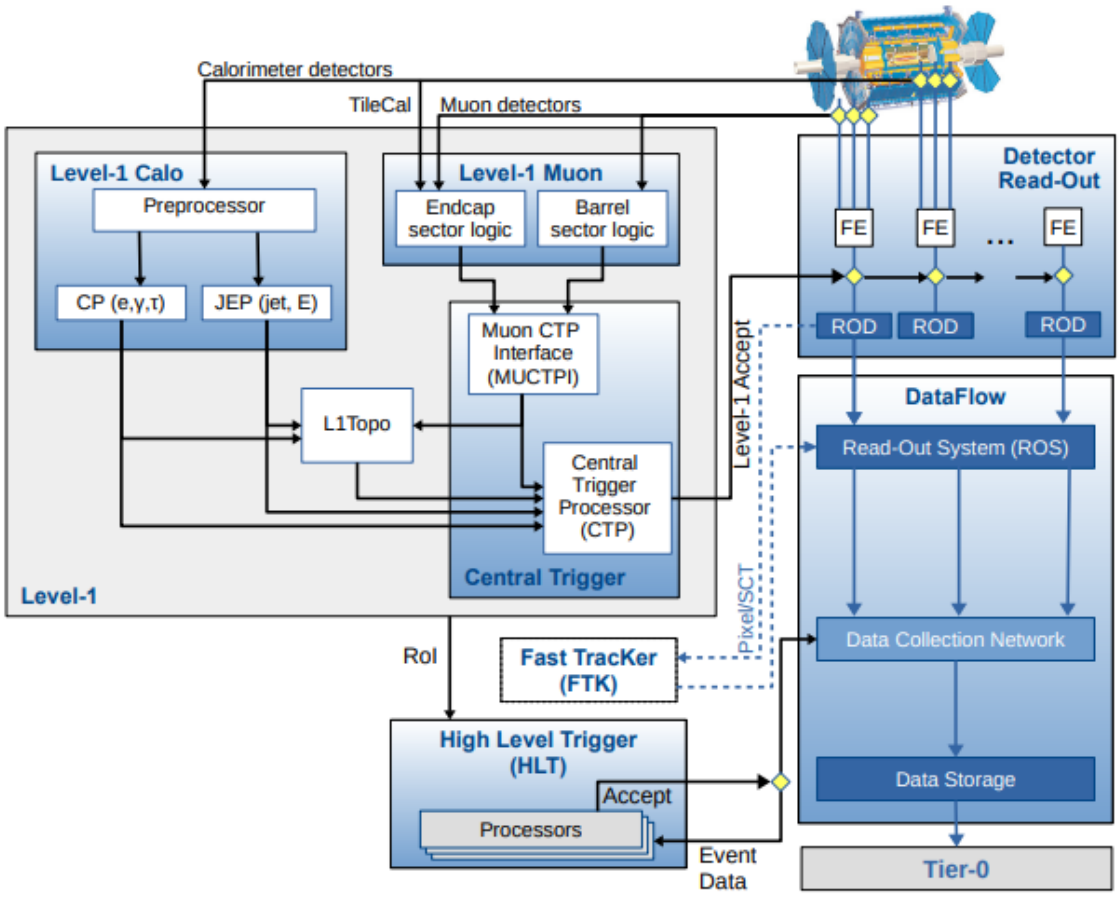


Figure 2.5: The ATLAS Trigger and Data Acquisition (TDAQ) system used during the Run II. [47].

Thin Gap Chamber (TGC) and Resistive Plate Chamber (RPC). The trigger detectors also provide the coordinate measurement in the non-bending plane. Figure 2.6 presents two different views of the MS.

The MS is split into the barrel region and the end-cap region. In each region, there are three detector stations. In the barrel region, the three stations are Barrel Inner station(BI), Barrel Middle station (BM), and Barrel Outer station (BO). The three stations in the end-cap are End-cap Inner station (EI) or SM, End-cap Middle station (EM) or Big Wheel (BW), and End-cap Outer station (EO) or Outer Wheel (OW). The MS provides precision tracking in the range of $|\eta| < 2.7$. The MDT detector provides majority of the tracking measurement except in the region of $2.0 < |\eta| < 2.7$ in the EI station where the CSC detector is used. This arrangement is due to the consideration of high particle rates expected in the EI region. The magnetic field is provided by three air core toroids (one barrel and two end-caps), each made of 8 coils [51, 52]. The field integral varies between 2 and 5 Tm in the barrel region. The field integral in the end-cap regions has larger variations, and the maximum field integral is around 9 Tm. However, the magnetic field changes its direction

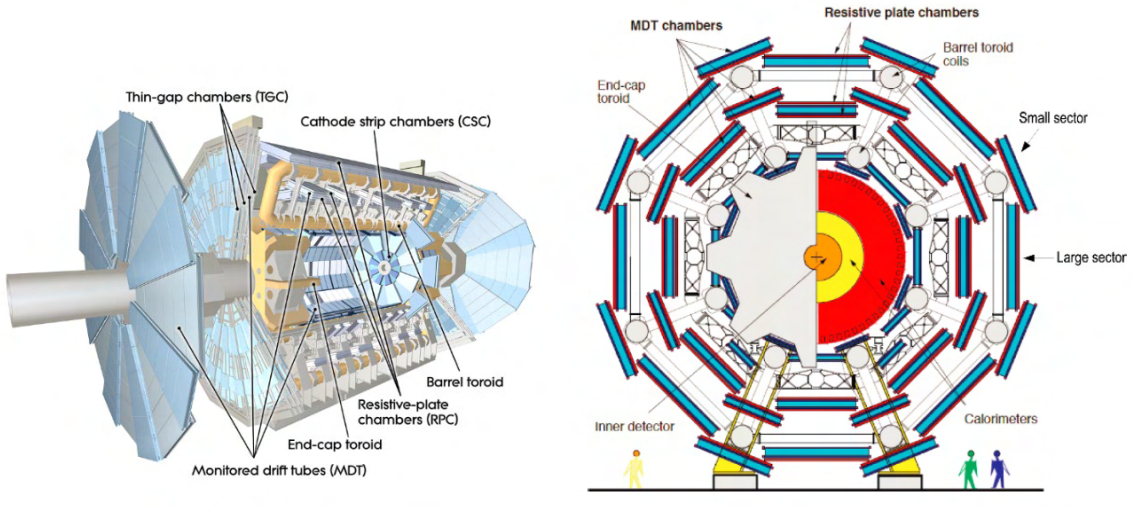


Figure 2.6: ATLAS Muon spectrometer cutaway diagram [15] and the view perpendicular to the beam line [50].

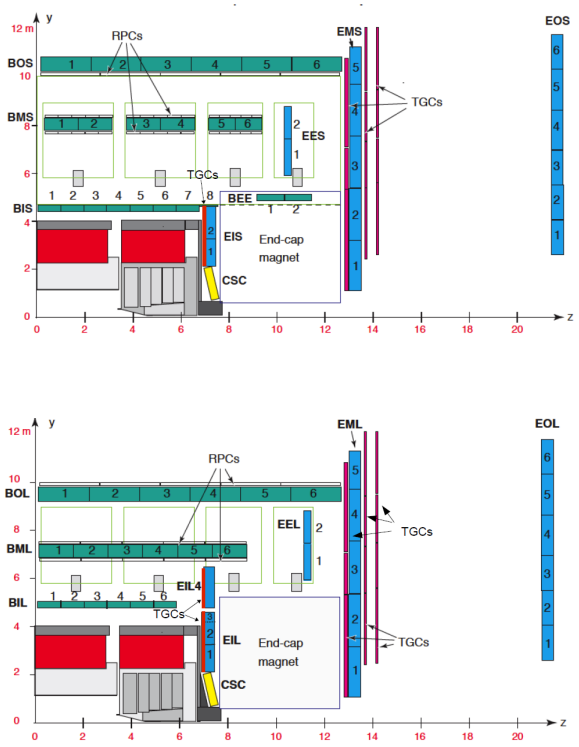


Figure 2.7: ATLAS Muon Spectrometer quadrant in the $r-z$ direction. The top figure is the layout for larger sectors and the bottom figure is the layout for small sectors [50].

around $|\eta| = 2.7$

The MS play an important role in the L1 trigger and the trigger coverage is $|\eta| < 2.4$. In the

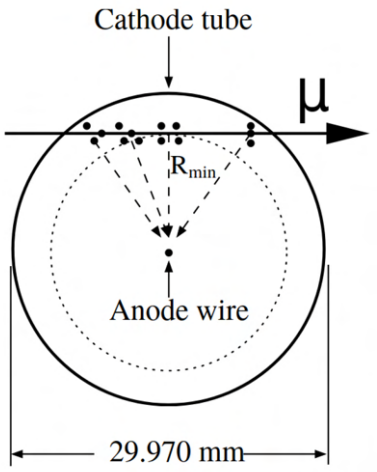


Figure 2.8: Diagram of a MDT tube with ionisation along a muon track [53].

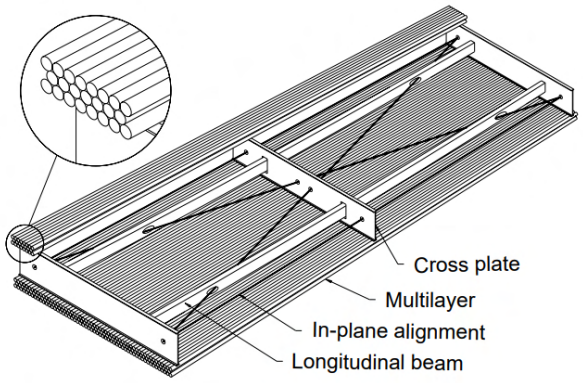


Figure 2.9: Structure of a MDT chamber [41]

end-cap region with $1.05 < |\eta| < 2.4$, the trigger information is provided by the TGC in the EM station. In the barrel region with $|\eta| < 1.05$, RPCs at the BI, BM and BO stations offer trigger primitives.

2.3.1 Monitored Drift Tube chamber

The MDT detector is the primary precision tracking detector for the ATLAS MS. As its name states, it consists of aluminum tubes with a diameter of 29.979 mm and a length range from 1 m to 6 m. It is a gaseous detector filled with a mixture of Ar(97%)-CO_2(3%) under a pressure of 3 bars. A tungsten wire with a radius of 50 μm is the anode node holding a high voltage of 3080 V. The wall of the tube is the cathode node and has a thickness of 0.4 mm. When a muon passes through a tube, ionized electrons in the gas drift to the central wire due to the electric field and generate a pulse signal that the front-end electronics could detect. An MDT chamber consists of 6 (or 8) layers of drift tubes, arranged such that 3 (or 4) layers of closely-packed tubes are mounted on each side of a support structure. Figure 2.8 shows the cross section of a drift tube with ionization clusters distributed along a muon track and Figure 2.9 presents the structure of a MDT chamber.

Figure 2.10 presents the drift time spectrum in the MDT tubes. The electron drift velocity shows a strong dependence on the radius due to the non-linear gas mixture used. The drift speed is about 10 μm/ns close to the wall, 26 μm/ns in the middle, and 52 μm/ns close to the wire. The average drift velocity is 20 μm/ns and the maximum drift time is 720 ns. The MDT front-end electronics measures the time of the first arrival electron. Based on the radius-to-drift time relation

($r-t$ relation) shown in Figure 2.10, the minimum radius from the muon track to the central wire can be determined. The $r-t$ relation depends on parameters like temperature, pressure, magnetic field and total hit rate in the tube. This relation needs to be known with high accuracy, which is achieved by continuous calibration with tracks in the ATLAS experiment.

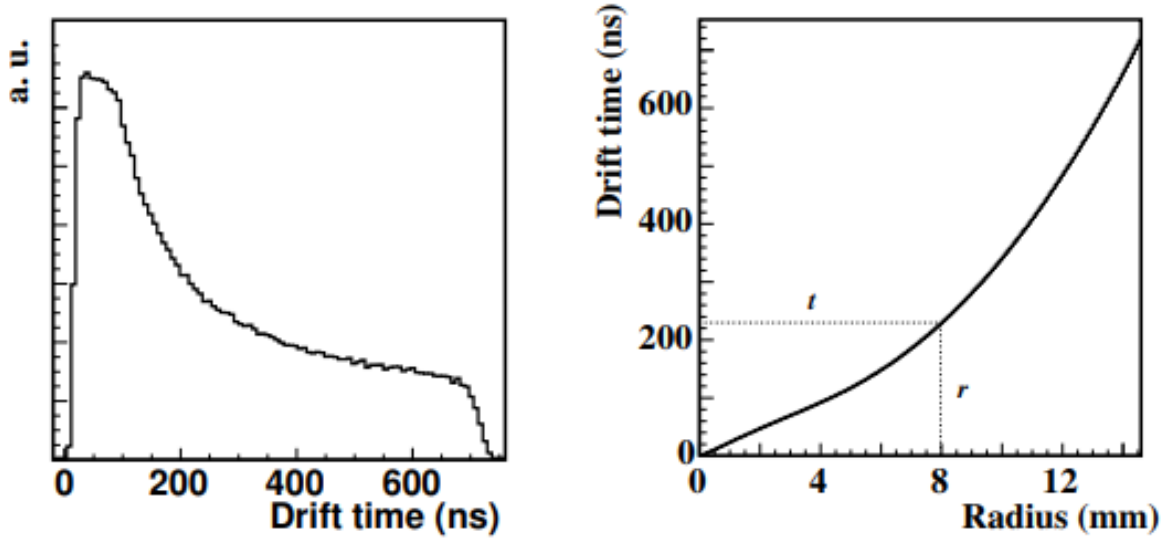


Figure 2.10: Typical MDT electron drift time spectrum and $r-t$ relation [15].

The muon momentum measurement is accomplished using three MDT stations (except CSC is used in the EI station with $2.0 < |\eta| < 2.7$) in both barrel and end-cap regions. Figure 2.11 presents the example of a track reconstruction. A track normally leaves 6 (or 8) hits in a MDT chamber. A single MDT tube has a spatial resolution of $\sim$100 μm, and each chamber has a spatial resolution of $\sim$35 μm.

2.3.2 Cathode Strip Chamber

The CSC detector is a multiwire proportional chamber. The pitch of the anode wires s is 2.5 mm, which is equal to the anode-cathode spacing d, as shown in Figure 2.12. A gas mixture of Ar(80%)-CO_2(20%) is used. When a muon passes through the chamber, it ionizes the gas atoms in the chamber. The ionized electrons drift to the anode wire and form a charge avalanche, which induces charges on the cathode strips. Presented in Figure 2.13, the cathode stripes are perpendicular to the anode wire, and adjacent strips share the induced charges. By collecting charges on multiple cathode strips and using the centroid of the charges, the position of the muon track can be determined.

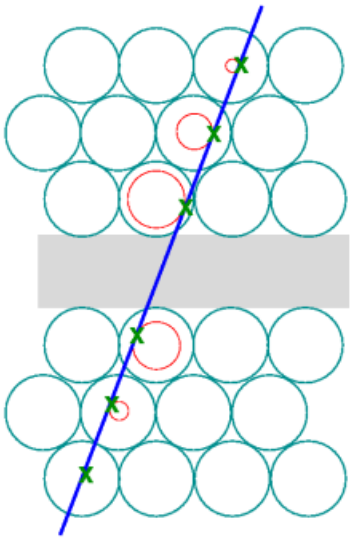


Figure 2.11: MDT track reconstruction with a MDT chamber [54].

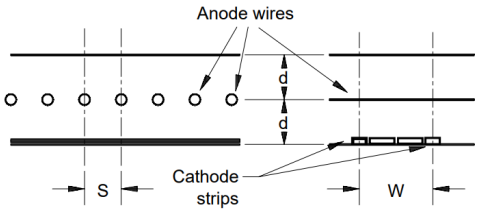


Figure 2.12: Structure of the Cathode Strip Chamber [55].

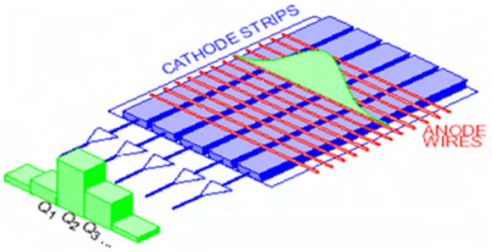


Figure 2.13: Charge distribution on CSC strips [15].

2.3.3 Resistive Plate Chamber

The RPC detector is a gaseous detector with a gas mixture of $C_2H_2F_4$ (94.7%)–C_4H_{10} (5%)–SF_6 (0.3%). The structure is shown in Figure 2.14. It consists of two resistive plates (electrodes) separated by 2 mm, and a high voltage of 9.6 kV is applied between two electrodes. The RPC is working in avalanche mode. Once a muon passes through the detector, the strong electric field creates avalanche ionization. Through capacitive coupling, drifting electrons and ions induce a current on the readout copper strips, and the front-end electronics further measure the current. The RPC detector can provide a spatial resolution of ~1 cm and a timing resolution of ~1 ns.

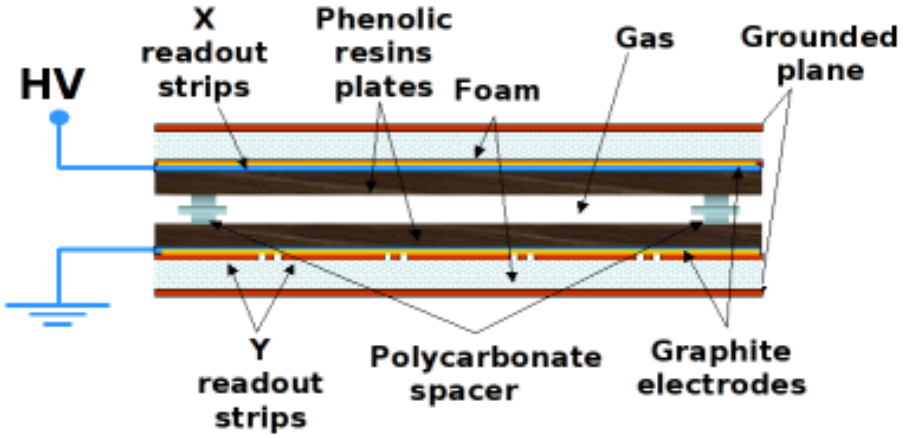


Figure 2.14: Structure of the Resistive Plate Chamber [56].

2.3.4 Thin Gap Chambers

The TGC detector is also a multiwire proportional chamber. It provides L1 trigger information in the end-cap region and performs position measurement in the radial direction to complement the MDT measurement. The structure is shown in Figure 2.15. It is similar to the CSC but with the anode-to-cathode distance (1.4 mm) smaller than the wire pitch of 1.8 mm. The width of the pick-up strip varies in different chambers and ranges from 1.46 cm to 4.91 cm. The working gas mixture is a highly quenching gas mixture of CO_2(55%) and n-pentane (45%). The TGC has a timing resolution of ~4 ns and a spatial resolution of ~1 cm.

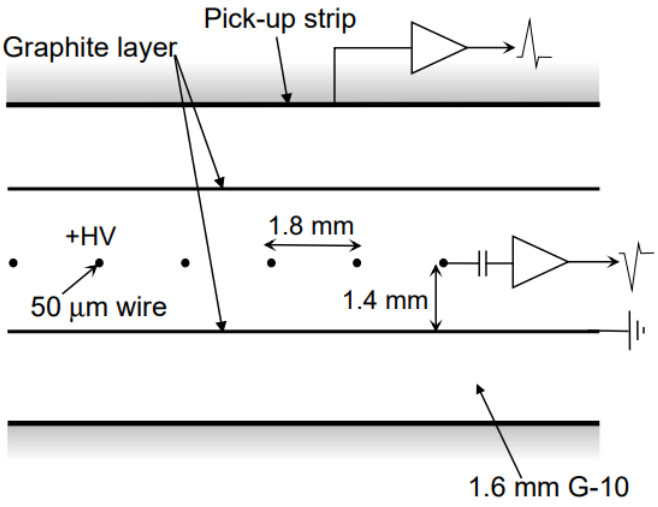


Figure 2.15: Structure of the Thin Gap Chamber [15].

CHAPTER 3

Upgrades of the ATLAS Muon Spectrometer

3.1 Introduction

To maximize the physics reach, the LHC plans to upgrade to the High-Luminosity LHC (HL-LHC) and increases its w to $5-7.5\times10^{34}$ cm^{-2}s^{-1} and delivers $3000-4000$ fb^{-1} of data at a center-of-mass energy of 14 TeV. The schedule of the HL-LHC is shown in Figure 3.1. In the most recent data-taking period between 2015 and 2018, Run 2, the LHC has reached a center-of-mass energy of 13 TeV and a peak instantaneous luminosity of 2.13×10^{34} cm^{-2}s^{-1}. The total integrated luminosity is about 150 fb^{-1} [12].

Figure 3.1: The overall LHC/HL-LHC schedule [57].

With the increased instantaneous luminosity, the number of pp collisions per crossing will

increase from 25 to 200 by a factor of 8. The event rate passing the first-level trigger and the event rate recorded offline will increase by a factor of 10. Table 3.1 lists the main ATLAS operation parameter comparisons between nominal LHC and HL-LHC.

	Nominal LHC	HL-LHC	Ratio
Bunch Crossing rate	40 MHz	40 MHz	1
Number of pp collisions per crossing	25	200	8
Event rate passing the first-level trigger	100 kHz	1 MHz	10
Event rate recorded offline	1 kHz	10 kHz	10
Number of detector channels	~90 M	>5000 M	>50
Average event size	~1.4 MB	~5.2 MB	~4
TID for the innermost pixel layer	790 kGy	14.4 MGy	~20

Table 3.1: ATLAS operation comparisons between nominal LHC and HL-LHC [58].

To profit from the HL-LHC operation, performance of the ATLAS detector needs to be maintained and in many systems, improved. ATLAS has two major upgrade plans: Phase-I [59, 60] and Phase-II [50, 58, 61–65]. The integration and commissioning of the Phase-I upgrade happened during the LS2 (the second Long Shutdown period from 2019 to 2022), and the integration and commissioning of the Phase-II upgrade will happen during the LS3 (the third Long Shutdown period from 2025 to 2027). These upgrades are 10-year-long projects and will improve the capability of the ATLAS detector to handle large data rates and large data volumes expected at HL-LHC runs. The muon spectrometer also has a series of upgrades. The Phase-I upgrade is discussed in Section 3.2 and the Phase-II upgrade is discussed in Section 3.3.

3.2 The Phase-I upgrade

The main focus of the Phase-I MS upgrade is the replacement of the current Small Wheel detector with the New Small Wheel (NSW) [59, 66] detector. In addition to the NSW upgrade, there is also a BIS78 project [50, 67], which replaces the current MDT chambers in the BIS7 and BIS8 stations with integrated small-diameter MDT (sMDT) and RPC chambers. The BIS78 project is a pilot Research and Development project for the Phase-II upgrade of the BI station. This section will focus on the NSW upgrade.

3.2.1 Motivation of the New Small Wheel detector

To cope with the increased luminosity and hit rate expected at HL-HLC runs, the NSW will replace the current SW to resolve the following two issues:

The first issue is the degradation of precision tracking performance, efficiency, and resolution. The current SW is based on the MDT system. Figure 3.2 presents the efficiency of a single MDT tube and the efficiency of an MDT chamber with 8 layers of tubes. With a hit rate of more than 300 kHz per tube, the single tube efficiency reduces to about 70%, and the efficiency to find track segments in an 8-layer chamber also drops to about 90%. Figure 3.3 shows the expected hit rate as a function of the radius at the SW region with an instantaneous luminosity of 3.0×10^{34} cm^{-2}s^{-1}. For an instantaneous luminosity of $5 - 7.5 \times 10^{34}$ cm^{-2}s^{-1}, the maximum hit rate can be up to 15 kHz/cm^2. It is thus critical to have a new detector that can work efficiently at HL-LHC runs.

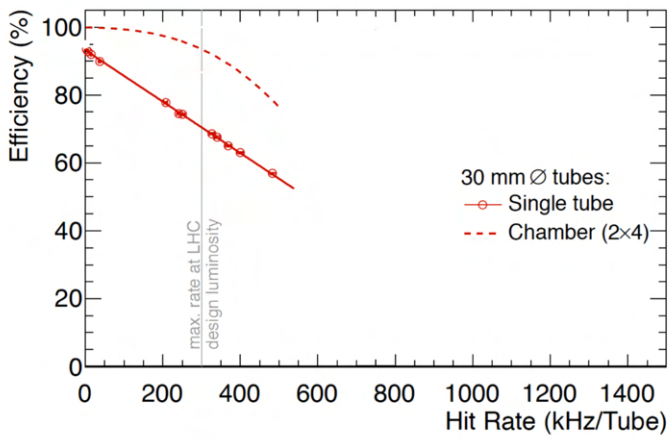


Figure 3.2: The MDT efficiency as a function of the tube hit rate. The solid line is the efficiency for a single tube and the dashed line is the efficiency for a 8-layer MDT chamber [59].

The increased background rates also degrade the MDT spatial resolution due to the space charge effects. The space charge, generated by the ionization avalanche, reduces the electric field and decreases the amplification gain. The variation of the space charge brings fluctuations to the electric field, which causes an unstable drift velocity and modify the $r-t$ relation. Figure 3.4 shows how the background hit rate impacts the MDT spatial resolution.

The second issue is the muon trigger selection in the end-cap region. The current L1 trigger in the end-cap region relies on the TGC detector in the BW. The data taken in 2012 indicated that about 90% of muon trigger candidates found at L1 are not real but fake muons. Figure 3.5 shows the η distribution of all muons triggered by the L1_MU20 trigger using data taken in 2017 at $\sqrt{s}$ = 13 TeV. The yellow histogram indicates all muons, the red histogram indicates these muons with an offline-reconstructed muon nearby, and the green histogram indicates these muons with an offline-reconstructed $p_T > 20$ GeV muon nearby.

The reason that about 90% of muons triggered by L1_MU20 are not real muons is due to low energy particles generated in the end-cap toroid region and low p_T muons deflected by the

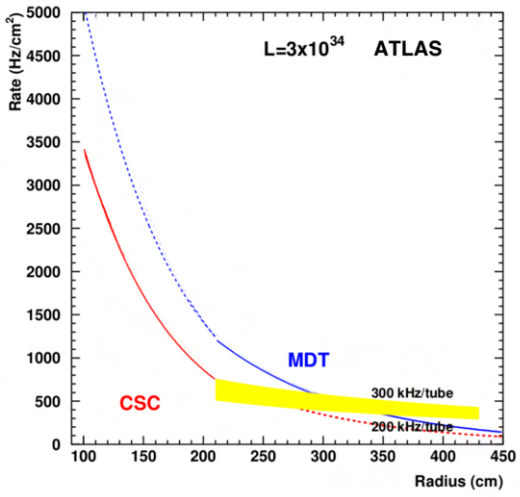


Figure 3.3: Expected hit rate as a function of the radius for the inner end-cap station at an instantaneous luminosity of 3.0×10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and $\sqrt{s} = 14$ TeV [59].

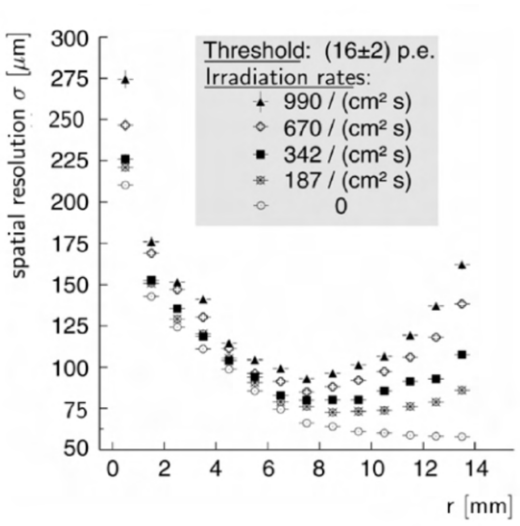


Figure 3.4: MDT spatial resolution as a function of the radius under different background rates [68].

calorimeters. These particles do not originate from the collision point but hit the BW with large angles. They are likely to be identified as high p_T muons by the TGC detector. Figure 3.6 shows three hypothetical high p_T muon tracks detected by the BW. Track B only hits the BW while track C does not point back to the IP. Only track A should be triggered since it comes from the collision point. The NSW detector will provide a measurement of the muon segment in the EI station at L1, by matching the NSW segment with the BW TGC segment and requiring the NSW segment pointing back to the origin, tracks B and C will be removed and only track A will be triggered.

3.2.2 Structure of the New Small Wheel detector

The NSW uses two novel technologies, small-strip Thin Gap Chamber (sTGC) [59, 70, 71] and Micro-Mech Gaseous Structure detector (Micromegas or MM) [59, 72–75]. It can measure the muon segment direction with an angular resolution of ~1 mrad at L1 within a latency of 1 μs. The NSW detector also provides precise measurement of muon hits with a position resolution of $100-200\,\mu$m per detector layer. Both sTGC and MM have the capability of tracking and triggering, with the sTGC being the primary trigger detector and the Micromegas being the primary tracking detector.

The NSW has two wheels, NSW-A and NSW-C, which are designed for side-A and side-C EI stations, respectively. Each wheel, with a diameter of around 10 m, is composed of 16 sectors with the combination of 8 large sectors and 8 small sectors as shown in Figure 3.7. The

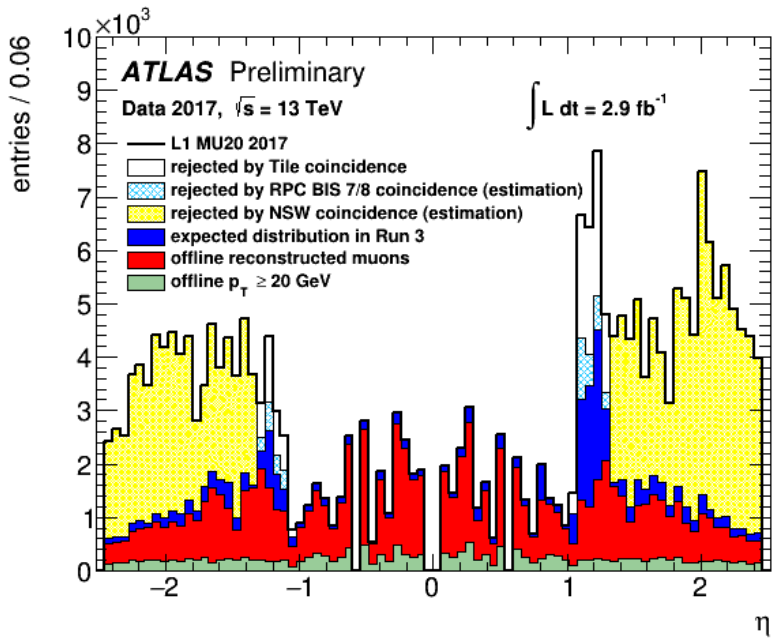


Figure 3.5: The η distribution of the $L1\_MU20$ with different matching conditions considered [69].

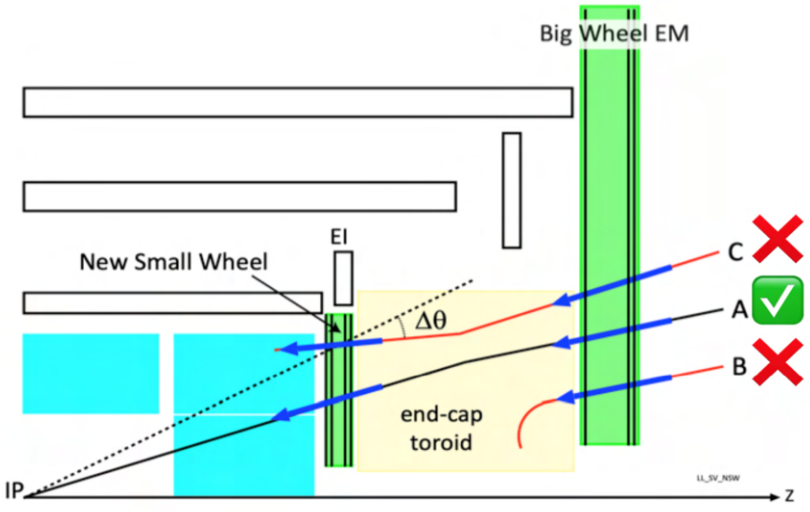


Figure 3.6: Trigger selection with the NSW detector. Track B only hits the BW while track C does not point back to the IP. Only track A should be triggered. [59].

middle sub-figure shows the structure of a single sector. It has one MM double wedges in the middle sandwiched by two sTGC wedges. Each sTGC wedge consists of three quadruplets. These quadruplets are called QS1, QS2, and QS3 for the small wedge and QL1, QL2, and QL3 for the large wedge (they are also named as Q1, Q2, Q3 despite the large or small wedges). Along the z-direction, the two sTGC wedges are called "Pivot" and "Confirm" quadruplets. An abbreviation

of “P” or “C” might added to the end of the name of a quadruplet to indicate if it belongs to a ”Pivot” wedge or a ”Confirm” wedge. In total there are 16 detector layers (8 for the MM and 8 for the sTGC), as shown in the right sub-figure.

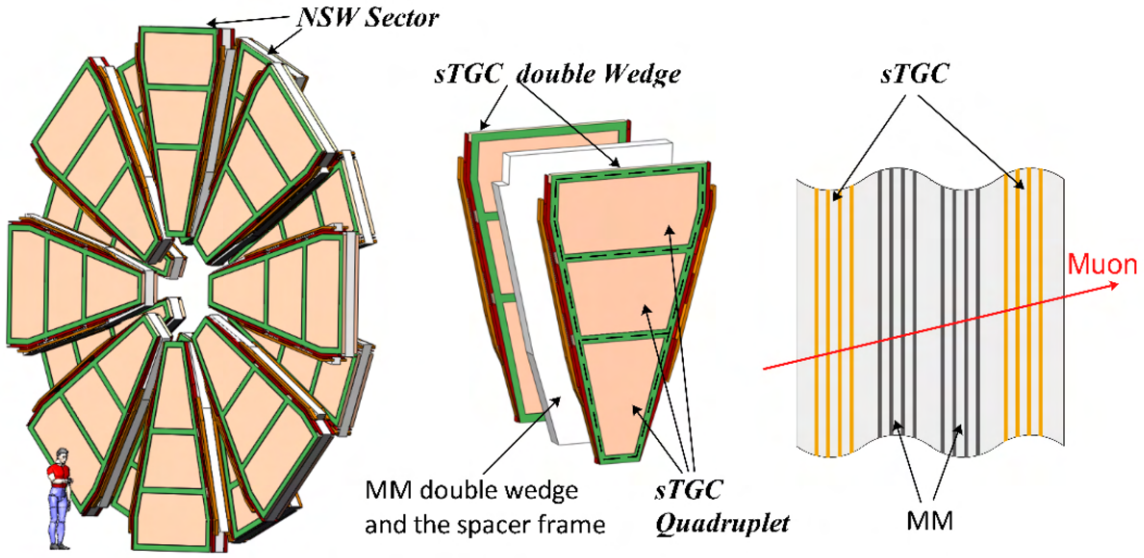


Figure 3.7: The mechanical structure of the NSW detector [76]. There are eight large sectors and eight small sectors. Each sector has two sTGC wedges and two MM wedges. Each sTGC wedge is composed of three sTGC quadruplets. In total there are 16 detector layers for each sector.

Figure 3.8 shows the internal structure of the sTGC detector. Similar to the TGC detector mentioned in Section 2.3, it is also a multi-wire proportional chamber with 50 μm tungsten wires separated by 1.8 mm apart. The detector is filled with a gas mixture of CO_2(55%) and n-pentane (45%). The high voltage applied is around 2.8 kV. The cathode planes, made by the graphite-epoxy mixture, cover the wires with a distance of 1.4 mm. Outside the two cathode planes, there are two pick-up electrodes capacitively coupled to the cathode planes. Unlike the TGC detector with a cathode strip with a width of $1.46-4.91$ cm, the pith of the sTGC strip is only 3.2 mm. That is why it is called “small-strip” TGC. This dense strip structure gives sTGC a position resolution of $\sim$100 μm depending on the incident angle. Another change compared to the TGC detector is that the other side of the cathode plane is placed with pick-up pads. The pads have a large pitch of 80 mm, and their length varies at different locations. The sTGC pads provide a coarse Region Of Interest (ROI) indicating the muon’s path.

The MM is also a gaseous detector and a gas mixture of Ar(93%)-CO_2(7%) is used. The structure is shown in Figure 3.9. A thin metallic mesh, called micro-mesh, splits the gas gap into two asymmetric regions: the amplification region and the conversion (or drift) region. The drift region usually has a thickness of a few millimeters with an electric field of a few hundred

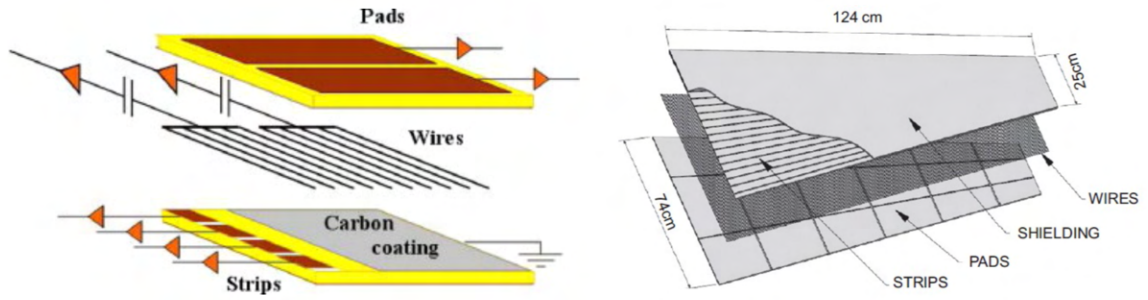


Figure 3.8: The internal structure of the sTGC detector [59].

V/cm. The amplification region is 128 μm thick and its electric field is $40-50$ kV/cm. When charged particles traverse the detector, they ionize the gas in the drift region. The ionized electrons drift to the micro-mesh and 95% of the electrons pass through the mesh entering the amplification region where avalanches happen. The newly generated ions and electrons drift to the mesh and the cathode, respectively. The motion of the electrons induces a current on the readout strips and the front-end electronics will read out this current. The MM strips have a pitch of $0.4-0.45$ mm.

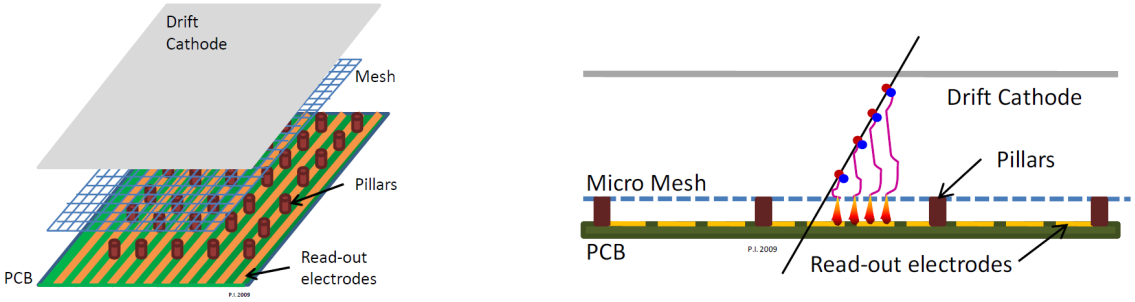


Figure 3.9: Structure of the MM detector and its operation principle [59].

Figure 3.10 shows a picture of the NSW-A and NSW-C in the Building 191 at CERN. At the time when the picture was taken (July 2021), the NSW-A was ready for the transport and installation inside the ATLAS collision hall.

3.2.3 Electronics of the New Small Wheel detector

Figure 3.11 shows an overview of the NSW frontend and backend electronics [78]. To provide both precision tracking and fast triggering with millions of detector channels in a harsh radiation environment, the NSW electronic system is based on a set of Application-Specific Integrated Circuits (ASICs) integrated on Front-End Boards (FEBs). Both sTGC and MM have two distinct data

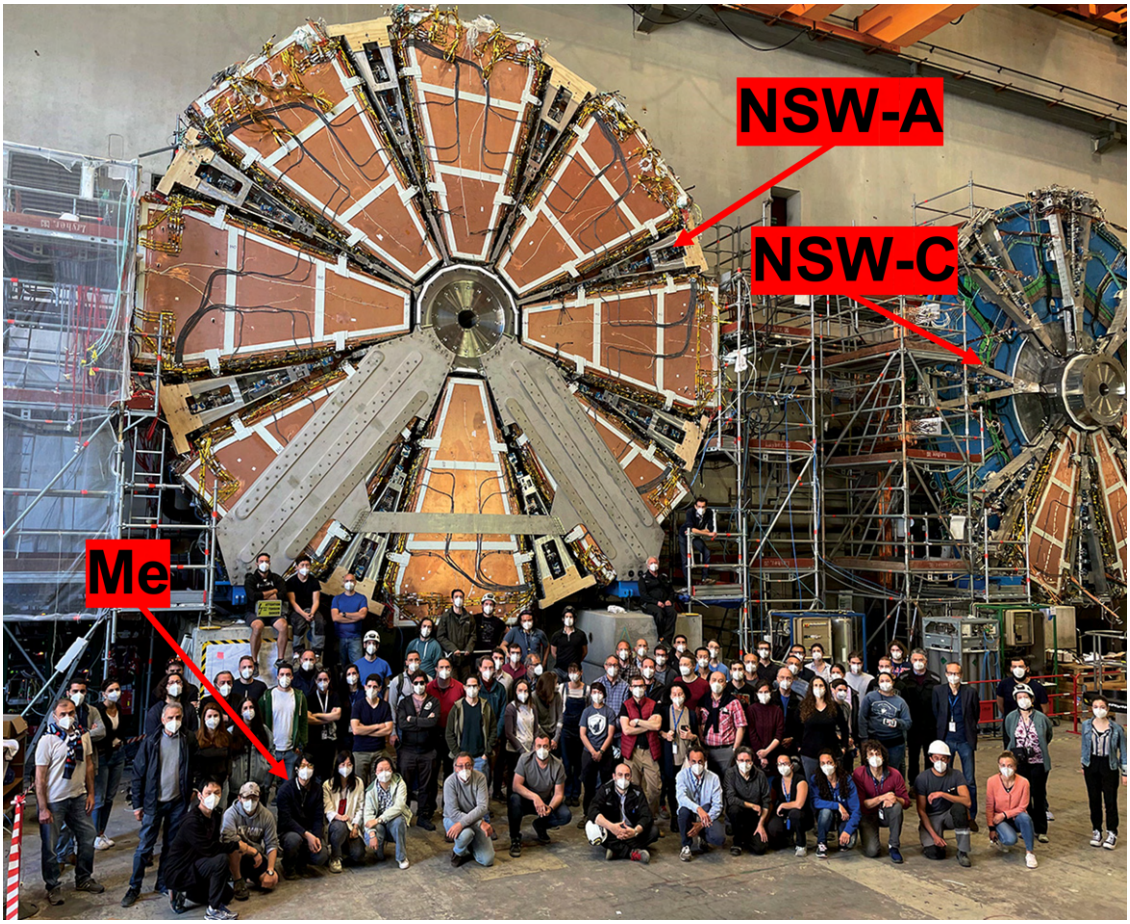


Figure 3.10: The picture of the NSW-A (left) and NSW-C (right) when NSW-A was ready for the transport and installation to the ATLAS collision hall in July 2021[77].

paths: the trigger chain and the readout chain, presented by black lines and blue lines in the diagram, respectively. The trigger chain provides the L1 muon trigger at the end-cap region for the ATLAS detector, and the readout chain offers data for offline muon track reconstruction.

The FEBs serve as a platform integrating several ASICs designed for the NSW. There are three types of FEBs in the NSW, depending on the data flow. They are strip Front-End Board (sFEB) [76, 79] for sTGC strips, pad Front-End Board (pFEB) [76, 80] for sTGC pads and wires, and MicroMegas Front-End (MMFE8) [81, 82] (number 8 named as there are 8 front-end readout ASICs on each board). In the rest of this section, I will introduce the NSW electronics for different data paths.

3.2.3.1 Readout Chain for the sTGC and the MM

The Venetios MicroMegas (VMM) [84–86] front-end ASIC provides multi-channel charge and timing measurement for MM and sTGC detector signals with its integrated amplifier, shaper, dis-

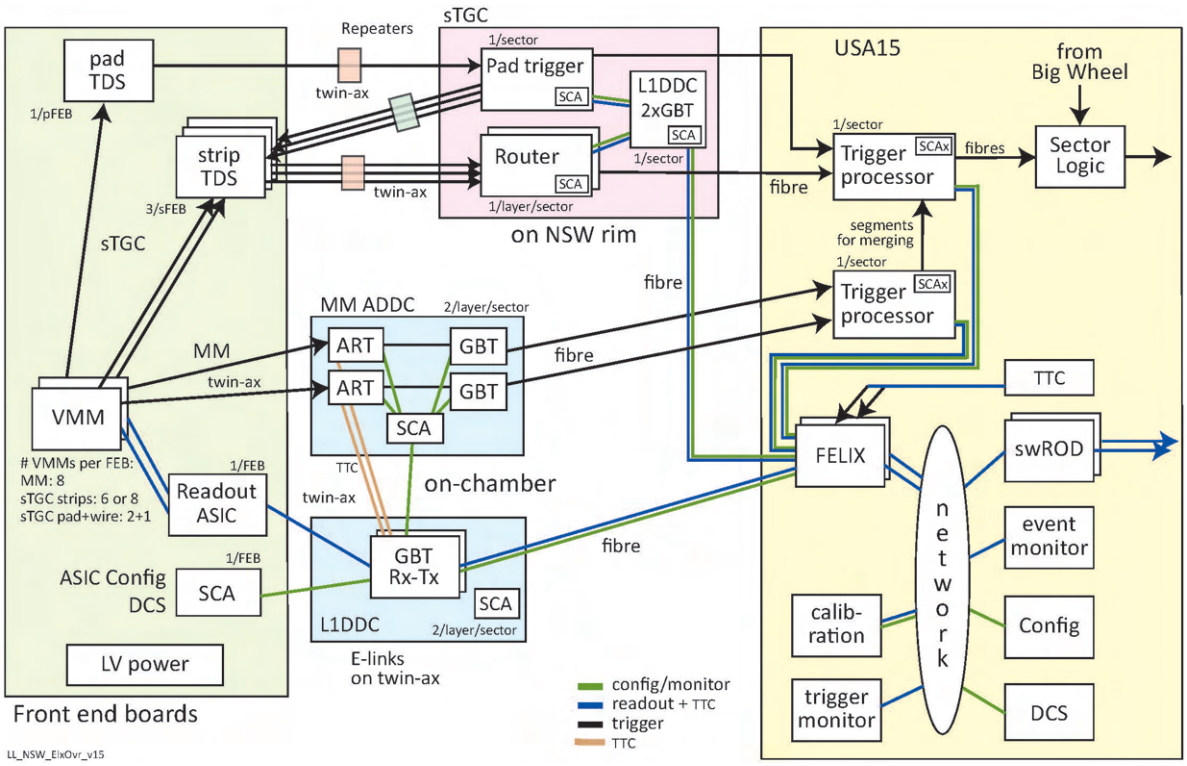


Figure 3.11: Overview of the NSW trigger and readout electronics [83].

criminator, and several analog-digital converters (ADCs). It is the first-stage front-end electronics measuring the detector signal and offering Level-0 (L0) data buffering and triggering. The L0 data will be collected by the Readout Controller (ROC) [87, 88] ASIC with the L0 Accept (L0A) trigger matching in VMM. The ROC holds the L1 data until it receives the L1 Accept (L1A) trigger signal. In the meantime, the ROC distributes the Time, Trigger, and Control (TTC) signals for triggering and electronics synchronization.

The Level-1 Data Driver Card (L1DDC) [89] is an intermediate node that connects multiple FEBs to the Front-End Link Exchange (FELIX) [90, 91] system. The GigaBit Transceiver (GBTx) [92] ASIC on the L1DDC, works as a serializer and deserializer, communicates between the FEBs (serial links up to 320 MHz) and the FELIX system (a bi-direction 4.8 Gpbs serial link). The FELIX system sends TTC signals to FEBs through the L1DDC, including the L0A trigger signal, the L1A trigger signal, and synchronization signals. The matched L1 data from the ROC is also transmitted through these links.

The FEBs-L1DDC-FELIX links are also used for slow control signals handled by the Slow Control Adapter (SCA) [93] ASIC on FEBs. The SCA configures all ASICs on FEBs and monitors the status of all on-board sensors.

3.2.3.2 Trigger Chain for the sTGC detector

The sTGC uses two sets of 3-out-of-4 coincidence from sTGC pads, which provides a coarse ROI, to read out the sTGC strips underneath. Only data for the selected strips will be transmitted to form trigger primitives. The sTGC trigger data flow is presented in Figure 3.12.

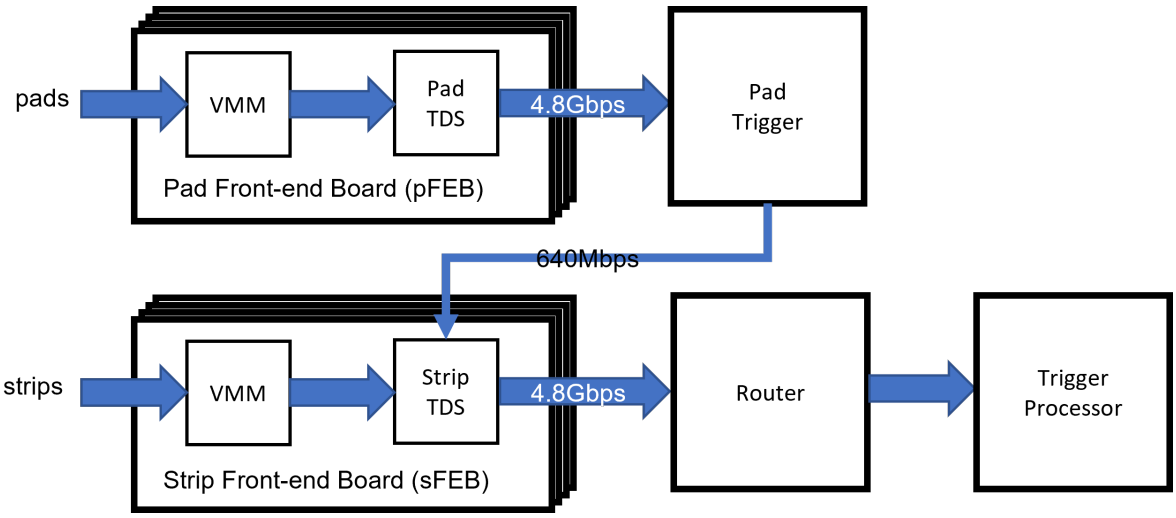


Figure 3.12: The sTGC trigger chain data flow.

In addition to the measurement and buffering of the L0 data, the VMM also provides direct outputs to the Trigger Data Serializer (TDS) [94, 95] ASIC for triggering purposes. The TDS ASIC can be configured in the pad mode or the strip mode depending on which FEB it serves.

On the pFEB, the VMMs send Time-over-Threshold (ToT) direct outputs (more discussions about direct output options will be shown in Section 4.1) to the pad TDS. The ToT direct output for each channel is a real-time one-bit flag signal that changes in every BC, with "1" indicating the sTGC pad is fired and "0" indicating the sTGC pad is not fired. Each pad TDS can handle up to 104 channels from two VMMs connected. It transmits a 12-bit BCID with 104 ToT status bits to the Pad Trigger board [59] through a 4.8 Gpbs serial data link in every BC.

The Pad Trigger board is mounted on the rim of the NSW detector and is a commercial FPGA-based board that collects high-speed serial data from 24 pad TDS chips (24 pFEBs from an entire sector). It receives the real-time hit status for all sTGC pads in the entire sTGC sector in every BC. An algorithm is then used to determine a coarse ROI using two sets of 3-out-of-4 coincidence. The logical pad concept is introduced in the coincidence process and will be discussed in Section 7.4. Based on the coarse ROI, the Pad Trigger board sends a pre-L1 trigger to the strip TDS via the 640 Mbps trigger interface. This pre-L1 trigger contains the timing information in terms of BCID and the location information in terms of Band-ID and Phi-ID.

In the meantime, when the sTGC pad signals are processed by the pFEB and the Pad Trigger

board, the sTGC strip electrodes also send analog signals to the VMM on the sFEB. After amplification and shaping, the VMM sends a 6-bit ADC fast charge data for every fired strip directly to the strip TDS. The strip TDS samples the 6-bit ADC data from 2 VMMs (up to 128 detector channels) along with a BCID timing stamp from its internal BC counter. The data will stored in strip TDS buffers waiting for the pre-L1 trigger signal from the Pad Trigger board.

Once the strip-TDS receives the pre-L1 trigger, it will perform a matching based on timing and location for all strips. The timing match is based on the BCID information from the pre-L1 trigger and the BCID stamp inside the strip data. The location information is based on a Band-ID to strip mapping. Each Band-ID from the pre-L1 trigger will be mapped to a range of strip-TDS channels using the pre-configured Lookup Tables (LUTs). The strip TDS outputs a 120-bits data packet containing 14 channels of 6-bit ADC data for every pre-L1 trigger it receives.

The Router board [59], which is also based on a commercial FPGA and mounted on the NSW rim, collects the strip-TDS outputs and acts as a switch to pass four active TDS links out of twelve from one sTGC layer to the Trigger Processor board. This is based on the assumption that only one quadruplet will be hit in each BC. Each sTGC sector is equipped with 8 Router boards, with each board receiving data from three sFEBs on one sTGC layer.

The sTGC trigger path requires a latency of less than 1 μs so that it can be combined with the segment found by the BW TGC station to generate the L1 trigger decision.

3.2.3.3 Trigger Chain for the MM detector

The trigger chain for the MM detector is simpler compared to the one for the sTGC detector. When a VMM measures and buffers the L0 data, it also outputs an Address in Real Time (ART) signal, the address of the first fired strip in every BC. This design is equivalent to re-segment the MM channels and combine 64 channels to one.

Each MMFE8 transmits 8 ART signals to the ART Data Drive Card (ADDC) [96], and each ADDC handles up to 64 ART signals. There are two dedicated ART ASICs [97] on the ADDC card that receives and deserializes the ART signals. Each ART ASIC will forward the selected data together with a 5-bit VMM geographical address and a 12-bit BCID timing stamp to the MM Trigger Processor (MMTP). This information will be further used for L1 triggering.

3.3 The Phase-II upgrade

The Phase-II upgrade for the ATLAS MS consists of upgrades of other muon sub-detectors and electronics during the LS3 period. Figure 3.13 presents the layout of the MS after the Phase-II upgrade. In the BIS region, followed by the BIS78 pilot project, current MDT chambers will be

replaced by sMDT and RPC chambers. The diameter of the sMDT tube is 15 mm, only half of the diameter of a normal MDT tube, which allows extra room for a new RPC detector to be installed.

In the EIL4 region, the old TGC doublet chambers will be replaced by new TGC triplets, which allows a more robust 2-out-of-3 majority coincidence. It covers the region of $1.05 < |\eta| < 1.3$ in the EIL station to compensate with the NSW detector. ATLAS also plans to install a high-η detector to tag muons in the region of $2.7 < |\eta| < 4.0$.

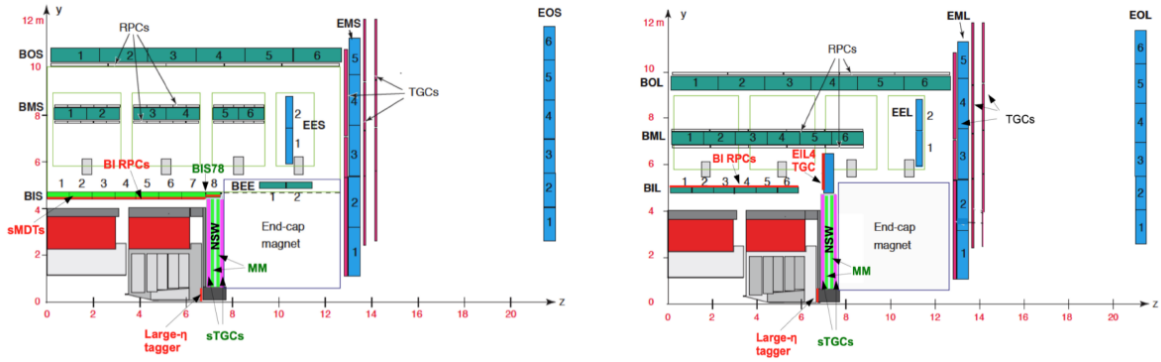


Figure 3.13: The new MS layout in the $r-z$ direction (the left plot is for the small sector and the right plot is for the large sector). Detectors marked by green text were installed during the Phase-I upgrade, those marked with red text are the detectors that will be installed during the Phase-II upgrade [58].

A main change in the MS electronic system is the MDT will also be used as a trigger device and join the first level muon trigger. Details will be discussed in the next section.

3.3.1 First-Level Muon Trigger with MDT chambers

In the Phase-II upgrade, the ATLAS TDAQ system will be upgraded to a single-level hardware-based trigger system with a maximum rate of 1 MHz and a latency of 10 μs [58]. The current L1 muon trigger will be replaced by a Level-0 Muon (L0Muon) trigger system. The L0Muon uses RPC information in the barrel region, and TGC and NSW information in the end-cap region. In addition, the MDT will be used at L0 to improve the trigger muon momentum resolution and to reduce the overall trigger rate. Figure 3.14 presents the ATLAS L0 trigger architecture with the calorimeters and Muon system after Phase-II upgrade.

Figure 3.15 shows the trigger efficiency at the three stages of L1 (L1MU15), Level-2 (L2), and Event Filter (EF) (L2 and EF are contained in the HLT) using data collected at $\sqrt{s} = 8$ TeV. L1MU15 means the L1 muon trigger with a p_T threshold of 15 GeV. However, from the red line in Figure 3.15, the L1MU15 efficiency raises at 10 GeV and reaches the plateau around 13 GeV (ideally, it should raise sharply at 15 GeV). This is due to the poor spatial resolution (only around

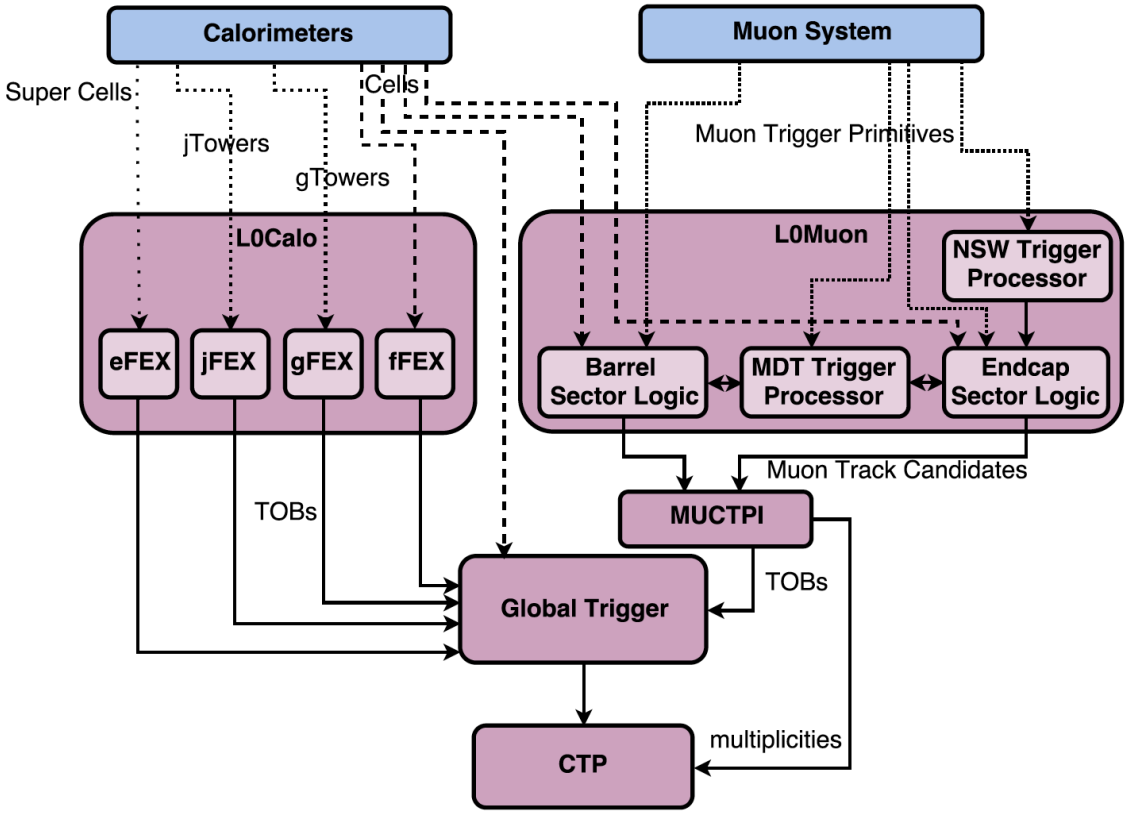


Figure 3.14: Diagram of the Level-0 trigger of ATLAS detector after Phase-II upgrade. The muon trigger primitives from the RPC (barrel region) and TGC (end-cap region) are used in coincidence with the information from the outermost layer of the tile calorimeter. The NSW and MDT prove hit information to their corresponding trigger processors. The Barrel Sector Logic and Endcap Sector Logic determines muon candidates with the refinements of momentum measurement from MDT Trigger Procesor [58].

1 cm) of the current RPC and TGC trigger detectors. Consequently, muons with p_T lower than the L1 threshold still have a high chance to pass the L1 trigger threshold.

Figure 3.16 shows the single muon production cross-section as a function of the muon p_T. The cross-section describes the probability for a process to occur during the pp collision. A larger cross-section means a larger chance for this process to happen. As shown in Figure 3.16, high p_T muons are only a small portion of the total muons produced during collisions. The cross-section raises quickly for muons with p_T below 20 GeV. Therefore, bringing the MDT to the L0 trigger system to improve the p_T resolution is vital to suppress fake trigger muon candidates with low p_T thresholds, especially at the HL-LHC. The study [98] using data collected at $\sqrt{s}$ = 8 TeV shows that a MDT-based L0 trigger with a threshold of 18 GeV is efficient for muons with p_T larger than 24 GeV in the barrel region and p_T larger than 20 GeV in the end-cap region.

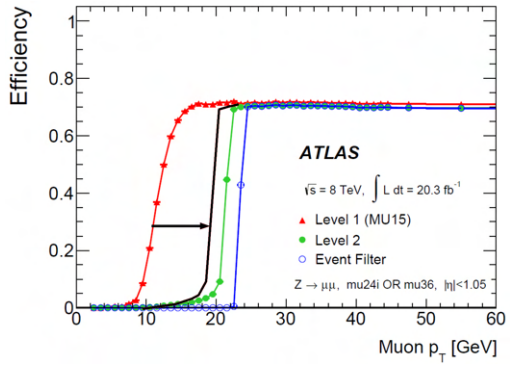


Figure 3.15: Trigger efficiency in terms of p_T at L1, L2, and EF stages. The black line is the expected L0 trigger performance with the MDT detector used [98].

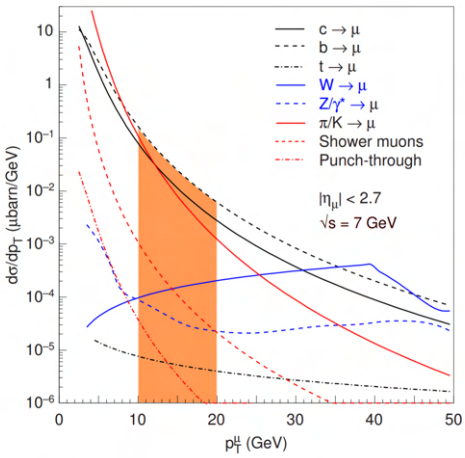


Figure 3.16: The production cross-section of single muons as a function of the muon p_T. The momentum range marked by the orange area is vital to be assisted by the MDT in the muon triggering [98].

3.3.2 The Phase-II MDT Electronics

The present MDT electronic system was only designed to provide precision tracking, not for triggering. The bandwidth of the system of the present is not enough to handle the increased rate, presented in Table 3.1, in the trigger-less mode. Those demands require a new MDT electronics system capable of triggering and tracking and offering high bandwidth. Figure 3.17 presents the new architecture of the MDT electronics system for the Phase-II upgrade. The main design focus is to send the MDT hit information off the detector as soon as possible. The Mezzanine card on the MDT detector collects the analog signals from 24 MDT tubes. After Amplification/Shaping/Discrimination of raw detector signals by the Amplifier Shaper Discriminator (ASD) [99] chip, the Time-to-Digital Converter (TDC) [100] ASIC samples the rising and falling edges of the discriminated signal and provides digitized timing stamps. In the current design, the TDC will hold the data inside its L1 buffer and wait for the L1A trigger signal. In the new architecture, the TDC will directly send out the data to the Chamber Service Module (CSM). The CSM collects data from up to 18 Mezzanine cards and transmits the data to the back-end MDT Data Processor Board, located inside the USA15 area (the main electronics cavern that is several meters away from the ATLAS detector).

The Hit Extractor uses the timing information from the RPC and TGC trigger detectors as references to extract relevant hits. Followed by the segment finder and the track fitter algorithms, muon tracks are reconstructed and momenta are determined. The reconstructed muon track information

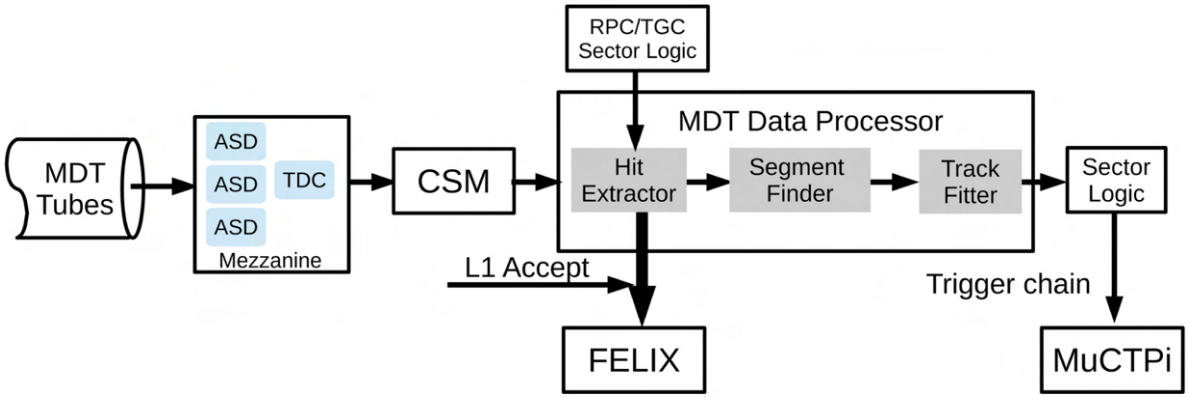


Figure 3.17: The new architecture of the MDT electronic system in the Phase-II upgrades.

is further transferred to the Sector Logic and the Muon Cental Track Processor (MuCTPI). In the meantime, the Hit Extractor also sends the hits that match the L1 trigger window to the FELIX system (the same system is used for the NSW readout). Details of the MDT front-end electronics will be discussed in Chapter 8.

CHAPTER 4

The Phase-I Upgrade: sTGC Front-end Electronics

This chapter introduces the sTGC front-end electronics. The Overview of the NSW trigger and readout electronics was already presented in Figure 3.11, and Figure 4.1 shows a simplified diagram of the trigger and readout system for the sTGC only. The sTGC pFEB and sFEB, marked by the green block, host a set of front-end ASICs customized for the NSW. Details of those ASICs will be discussed here.

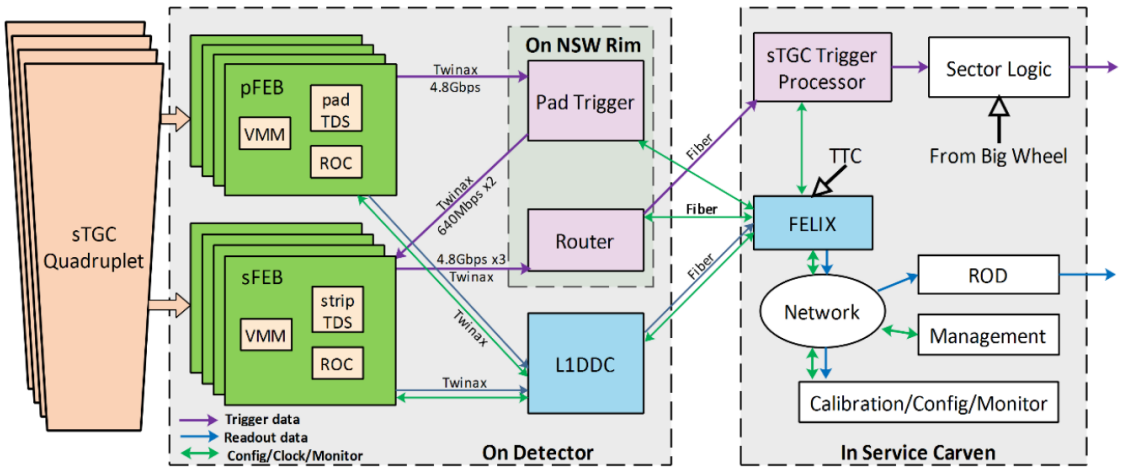


Figure 4.1: Simplified diagram of the sTGC trigger and readout system [76].

4.1 VMM

The VMM, abbreviation for Venetios MicroMegas, is developed for the MM and sTGC charge and timing measurements. It was manufactured with the 130 nm Global Foundries 8RF-DM process and packaged in a Ball Grid Array (BGA). Each chip has a silicon area of 21×21 mm^2.

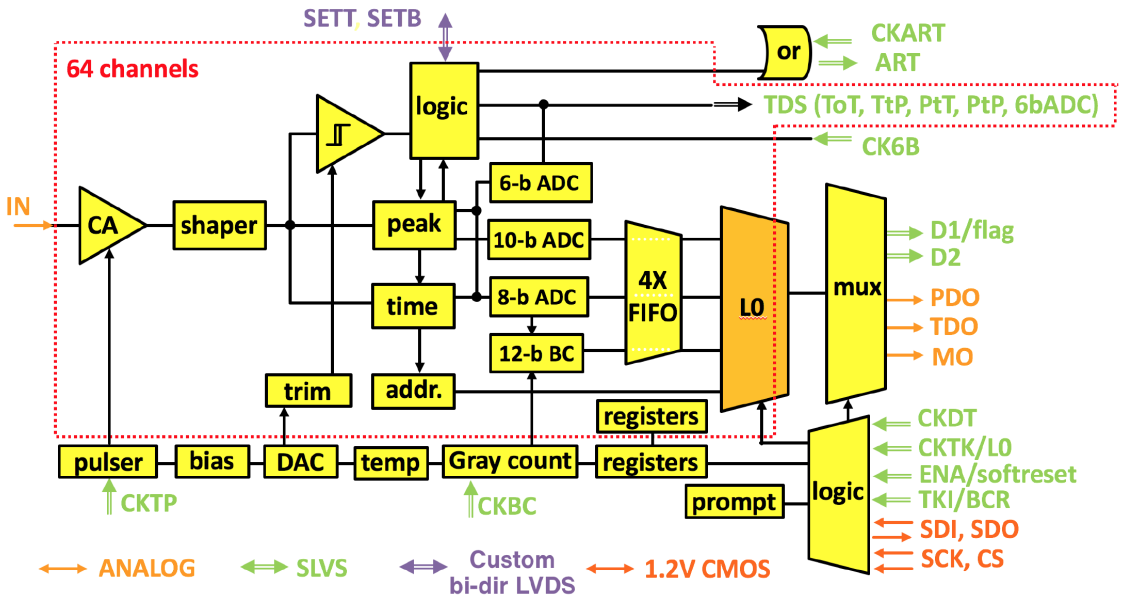


Figure 4.2: Architecture of the VMM ASIC [101].

Figure 4.2 shows the block diagram of the VMM architecture. Each VMM ASIC has 64 channels, and each channel has a low-noise charge amplifier (CA) that receives the analog signal from the connected detector electrode. The CA has adjustable polarity so that it can handle different polarities on sTGC electrodes: pad (positive), strip (positive), and wire (negative). The shaper, or the filter, maximizes the Signal-to-Noise Ratio (SNR) by limiting the signal bandwidth. It has an adjustable peaking time with the choice of 25 ns, 50 ns, 100 ns, and 200 ns. After the shaping, the signal is routed to the discriminator, peak detector, and time detector.

The threshold of the discriminator is controlled by a global 10-bit Digital-to-Analog Converter (DAC), with an individual 5-bit trimming DAC in each channel. The peak detector measures the amplitude of the signal, and the time detector measures the timing using a time-to-amplitude converter (TAC). Both measured values are stored in analog memories.

After the peak and time detectors, there are three low-power Analog-to-Digital Converter (ADC): a 6-bit ADC, an 8-bit ADC, and a 10-bit ADC. Those ADCs digitize the stored analog signals. The 6-bit ADC provides the direct output for sTGC strips as fast charge measurement in the trigger chain. The 8-bit ADC and the 10-bit ADC give an 8-bit timing ADC measurement and a 10-bit charge ADC measurement that will be buffered as L0 data. The L0 data waits for the L0A trigger signal to be read out through the readout chain.

In the sTGC trigger chain for pFEB, the VMM provides a direct output with the following four options:

- Time-over-threshold (ToT);

- Threshold-to-peak (TtP);
- Peak-to-threshold (PtT);
- A 10 ns pulse occurring at peak (PtP).

The direct output pulses will be captured by the pad TDS together with a BCID time stamp. It provides a real-time hit status for each sTGC pad every BC. By default, the VMM will be configured to use the ToT mode. Section 7.2.4 presents a detailed study of the timing performance of the ToT mode and the PtP mode.

In the sTGC trigger chain for sFEB, the VMM provides a 6-bit ADC direct output. The VMM peak detector converts the voltage into a current. This current is fed into the 6-bit ADC for a fast but low-resolution analog-to-digital conversion. The strip TDS samples the 6-bit ADC data and store them in its buffer. Those data will be used to for the sTGC trigger primitives at L1.

The VMM also provides a test pulse function. It uses the Pulser to inject a pulse to the CA with a 10-bit DAC. This function provides an emulated detector signal to the system, which serves as an important calibration tool for the VMM operation and verification.

4.2 ROC

The ROC ASIC was fabricated in the same wafer as the VMM using the IBM 130 nm CMOS technology. Figure 4.3 presents the ROC structure diagram. It collects the L0 data from up to 8 VMMs through two 160 MHz Double Data Rate (DDR) serial links on each VMM. The bandwidth for a single VMM is 640 Mb/s, and the effective data rate is 512 Mb/s after the 8b/10b encoding. The ROC uses 8 VMM capture modules to receive L0 data from those links and store them in the channel FIFO. Four independent sub-ROCs inside the ROC perform the L1 matching from the channel FIFO. A crossbar structure provides a flexible switch scheme that routes 8 VMM capture modules to 4 sub-ROCs. Each sub-ROC can handle up to 4 VMMs and has configurable E-links with a speed of 80, 160, 320, or 640 Mb/s (two E-link lines use 640 Mb/s). This design suits different data rates at different detector regions.

The ROC also receives the TTC signal and distributes the L0A trigger signal to the VMM. It forwards the BC clock and BCR to the TDS and VMM.

4.3 TDS

The TDS ASIC was also fabricated using the IBM 130 nm CMOS technology. It prepares the trigger data for both pads and strips, performs pad-strip matching, and serializes the trigger data

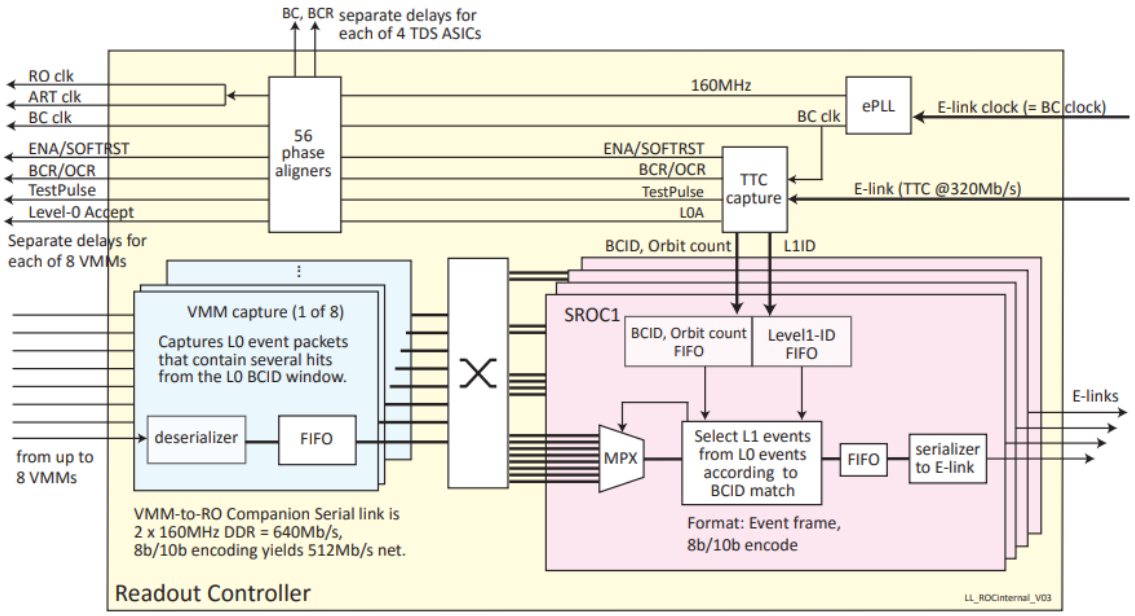


Figure 4.3: Structure diagram of the ROC ASIC [102].

with high-speed and low-latency. It can be configured to two different working modes: the pad mode for sTGC pads and the strip mode for sTGC strips, denoted by pad TDS and strip TDS, respectively.

4.3.1 Pad TDS

Figure 4.4 is the block diagram of the pad TDS. The pad TDS can handle direct outputs from up to 104 pads. It sends a one-bit fire status flag for each pad channel in every BC to the Pad Trigger board.

Starting with the pulse detection of each channel, it creates a BCID time stamp for the rising edge of the VMM direct output. Every channel has its own local BC clock and the phase can be adjusted independently. This scheme is designed to compensate for delay differences caused by different pad trace lengths. The adjustable phase function is achieved by a phase shifter circuit shifting the local BC clock with a step of 3.125 ns and a range of 25 ns.

The sampled BCID is stored in the 2-depth buffer waiting for the global BCID counter to synchronize. The frame builder combines the synchronized 104-bit channel fire status and the 12-bit global BCID to form a data packet. After scrambling, the GBT serializer (GBT-SER) sends out the data packet to the Pad Trigger board using a 4.8 Gbps data link.

The TDS can also be configured in the Psuedo-Random Binary Sequence (PRBS) mode, which outputs the PRBS-31 data sequence. This function can be used to verify the connectivity and

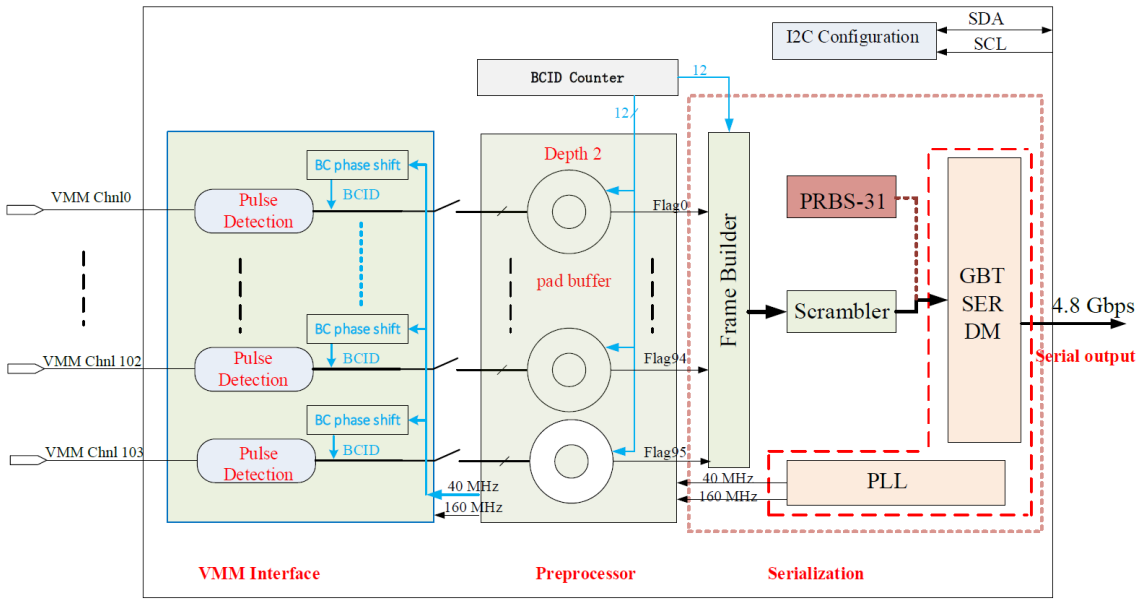


Figure 4.4: Architecture of the pad TDS ASIC [103].

stability of the data link.

4.3.2 Strip TDS

Figure 4.5 shows the architecture of the strip TDS. The strip TDS samples the 6-bit ADC direct output data from 128 VMM channels (two VMMs) using dual edges of its own 160 MHz clock. After deserializing the 6-bit ADC data, the values will be stored in each channel's 4-depth ring buffer along with the BCID time stamp. The TDS assigns the BCID to the 6-bit ADC data based on the leading edge of the VMM direct output flag. The data stays in the buffer and waits for the pre-L1 trigger signal from the Pad Trigger board.

Limited by the output bandwidth, each strip TDS data packet is 120-bit and only contains 6-bit ADC data for 14 VMM channels. Those 14 channels are chosen based on the Band-ID information inside the pre-L1 trigger signals and the Band-ID mapping LUT. Each LUT maps a Band-ID to a 17-strip group, and only 14 of them will be selected. How those channels are selected will be discussed in Section 5.1.1.6. The matched data will be sent out through the 4.8 Gbps link after descrambling.

The strip TDS provides two 160 MHz clocks to the two VMMs it connects. The phases of those two clocks can be programmed separately to avoid timing violations of the 6-bit ADC data sampling. The phase of the TDS-VMM 160 MHz clock is one of the important clock phases that need to be tuned.

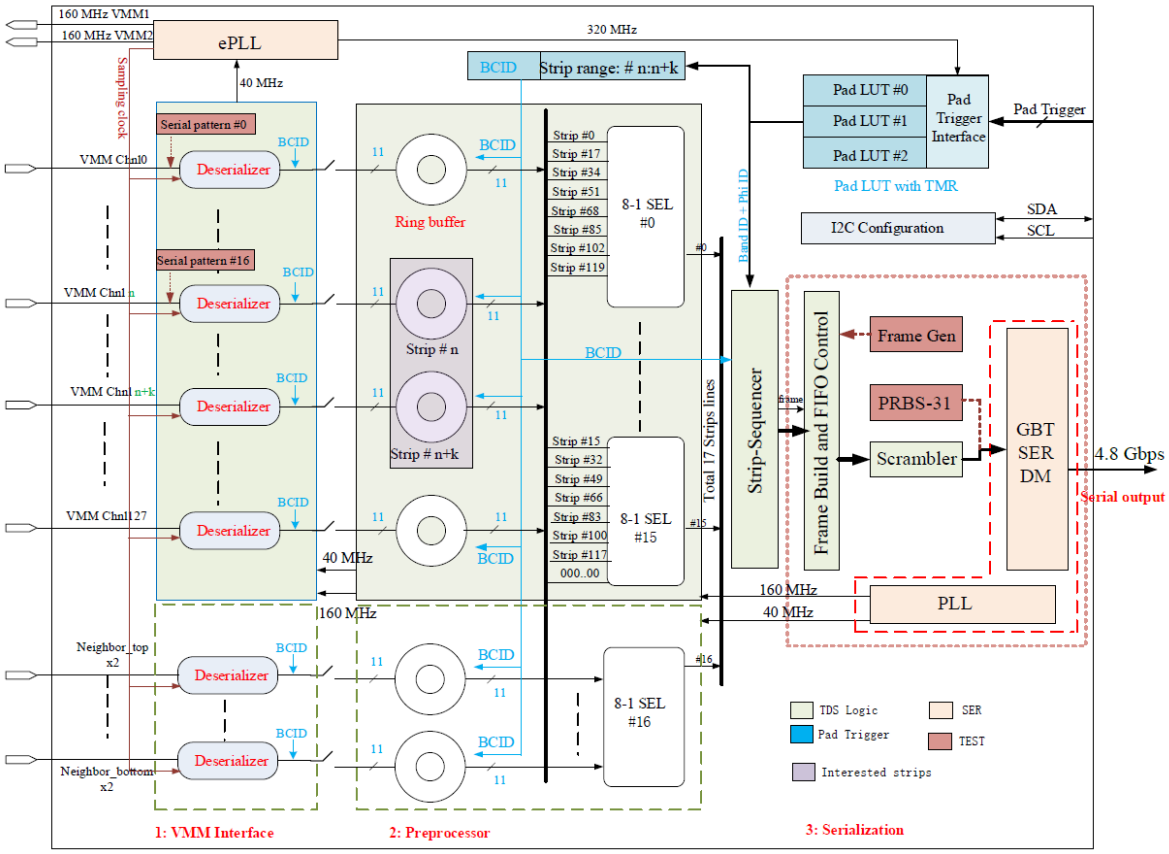


Figure 4.5: Architecture of the strip TDS ASIC [103].

4.4 sTGC FEBs

The sTGC Front-End Boards (FEBs) host the main three front-end ASICs: VMM, ROC, and TDS. To deal with the three types of electrodes of the sTGC (wire, strip, pad), two types of FEB have been designed. The pad-FEB (pFEB) handles sTGC pads and wires, while the strip-FEB (sFEB) handles sTGC strips.

Figure 4.6 shows the structure of the pFEB. It connects to the sTGC detector adapter board through a spring-loaded 300-pin connector called the GFZ connector. There is a special analog input protection circuit, presented in Figure 4.7, for each channel that protects the VMM CA from potential electrostatic discharge (ESD) damage during operation in the high-rate radiation environment. The first stage of the ESD protection is a Transient Voltage Suppressing (TVS) diode which connects to the input line in parallel. It quickly dissipates the electrostatic discharge by absorbing the instant current of both polarities. The second stage of ESD protection consists of a 10 Ω resistor and a pair of back-to-back diodes, located next to the VMM input, which further protects the discharge current.

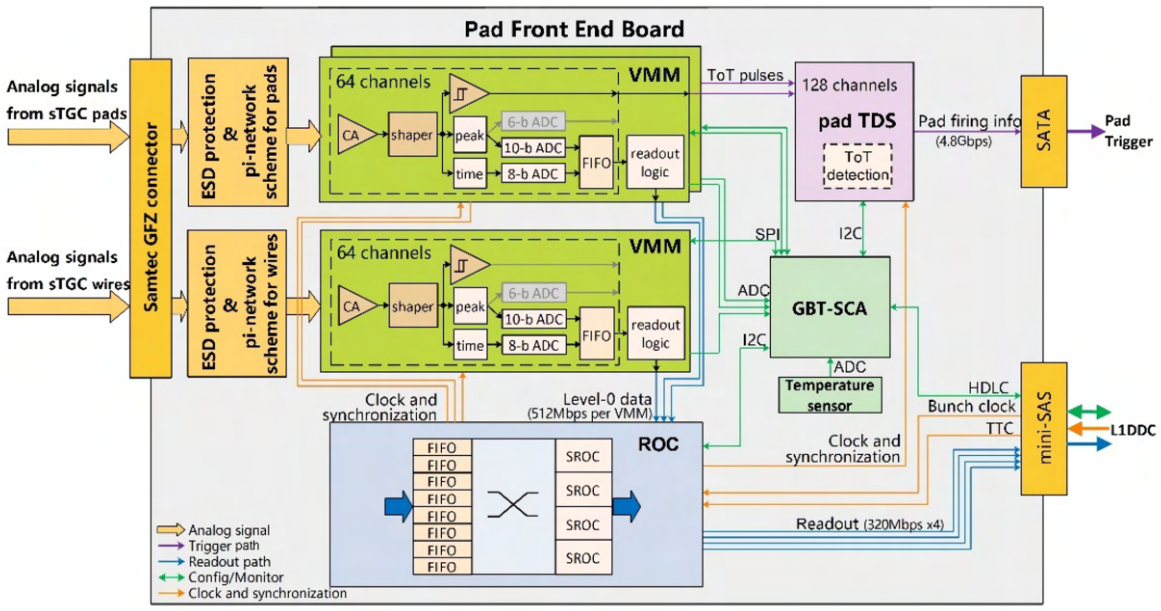


Figure 4.6: Block diagram of the pFEB [76].

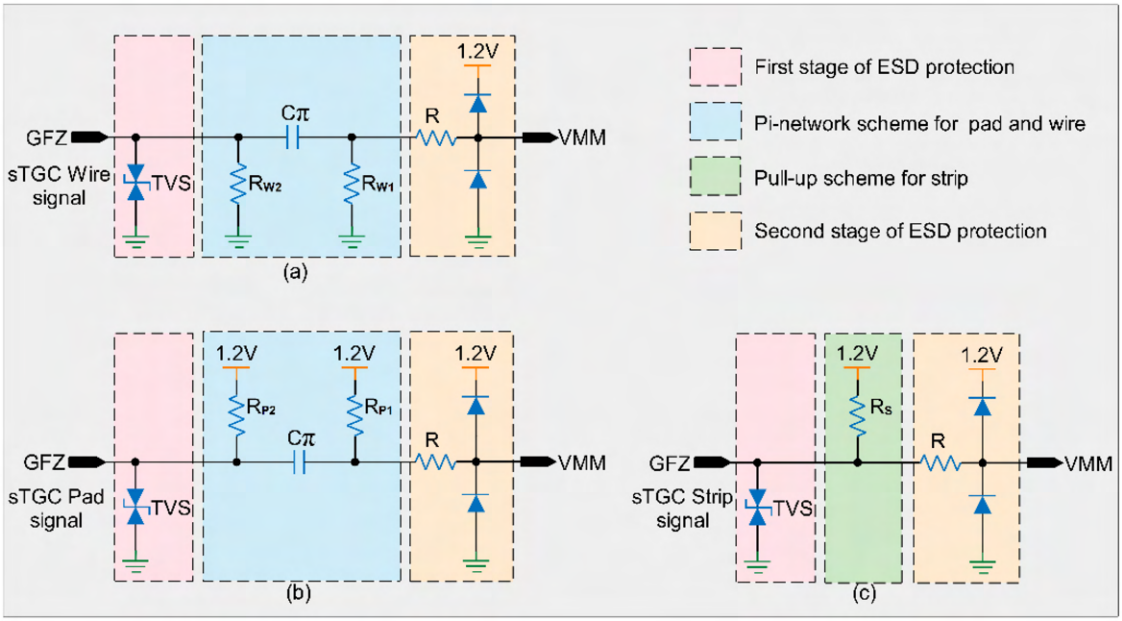


Figure 4.7: The sTGC FEB analog input protection circuit [76].

In the middle stage, a compensation circuit, composed of a π-network, attenuates the sTGC pad and wire signals. Considering the high gas gain of the sTGC detector and large photon background rate at the NSW location, the π-network is necessary to keep the VMM amplifier in its safe linear region (with an input charge up to 2 pC). It also helps to reduce the dead time caused by saturation.

The capacitor C_π is connected to the sTGC pad in parallel, which is equivalent to attenuate

the charge current by $C_\pi/(C_{pad}+C_\pi)$. The size of the sTGC pad determines the value of the capacitance C_{pad}, and it varies in different locations. Ideally, C_π values should be optimized to have a similar attenuation factor for each sTGC pad. However, it is impractical to customize C_π for every channel. Consider the fact that the majority of pads from the same quadruplet have a similar size, only three C_π values are chosen for three types of quadruplets. They are 200 pF, 330 pF, and 470 pF for Q1, Q2, and Q3.

The two VMMs that are connected to sTGC pads send ToT direct outputs to the pad TDS. The pad TDS transmits 104 sTGC pad fire status together with a 12-bit BCID on a 4.8 Gbps serial link through a Serial AT Attachment (SATA) connector to the Pad Trigger board. This is the trigger chain data flow.

All three VMMs (including the one that connects to sTGC wires) are connected to the ROC and provides L0 data. The ROC L1 data is transmitted to the L1DDC card through a mini-SAS (mini Serial Attached Small Computer System) connector with four data links. This is the readout chain data flow.

The L1DDC also sends BC clock and TTC signals to the ROC, which will be further distributed to on-board ASICs. The slow control of the FEBs is handled by the SCA chip. It communicates with the back-end electronics with the High-Level Data Link Control (HDLC) protocol. It offers various interfaces for different ASICs (TDS and ROC with I2C and VMM with SPI). Moreover, its internal ADC monitors the temperature measured by temperature sensors,VMM peak detector multiplexed analog output (PDO), and VMM time detector multiplexed analog output TDO.

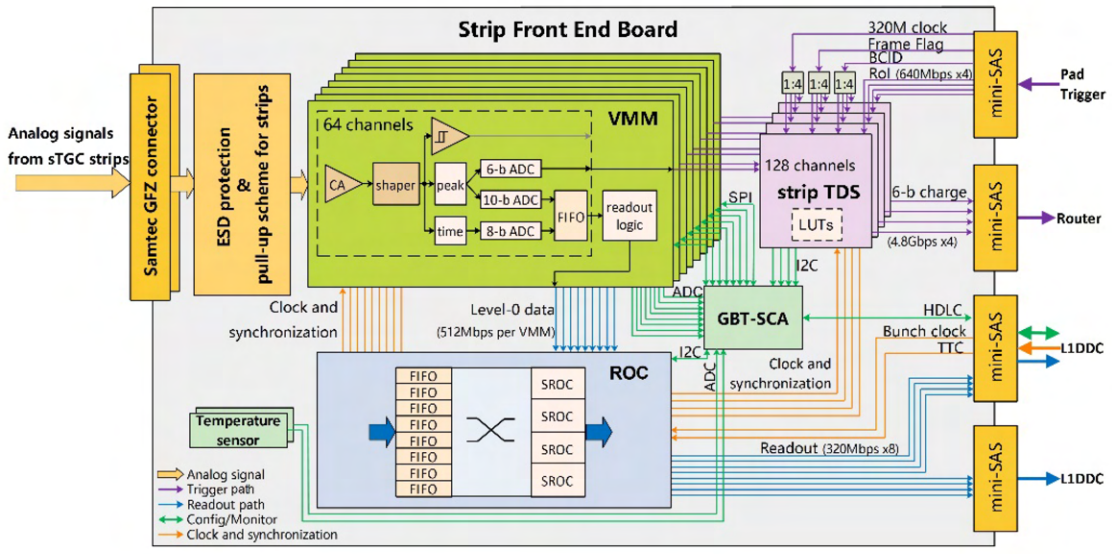


Figure 4.8: Block diagram of the sFEB [76].

Figure 4.8 shows the block diagram of the sFEB. The overall scheme is similar to the pFEB.

But it has more components since it needs to handle up to 400 sTGC strips per board. It uses two GFZ connectors to connect the detector adapter board. The analog input protection circuit is similar to the pFEB as well. It consists of two stages of ESD protection and a compensation circuit with a 400 kΩ pull-up resistor, as shown in Figure 4.7. The pull-up resistors help to correct the bias current and working node of the VMM.

Four mini-SAS connectors are used on each sFEB. One mini-SAS connector is used to transmit the ROC data, BC clock, TTC, and HDLC signals. A second connector is used as a supplement port to provide another four data links for the ROC to handle higher data rates expected at the HL-LHC. A third mini-SAS connector is connected to the Pad Trigger board that receives the pre-L1 trigger for the strip TDS. The fourth connector is used to transmit data to the Router using four TDS 4.8 Gbps data links.

There are 8 VMM and 4 TDS ASICs on each sFEB and are named sFEB8. In some sTGC regions, 6 VMM and 3 TDS ASICs are enough to handle all detector channels. Those boards are called sFEB6. Figure 4.9 shows the picture of the fully assembled pFEB and sFEB8. The power consumption is 9 W and 21 W, respectively. Water cooling is needed to keep these ASICs under 50 Fahrenheit. In total, 768 (12×64) sFEB and 768 pFEB are needed for the two NSW wheels.

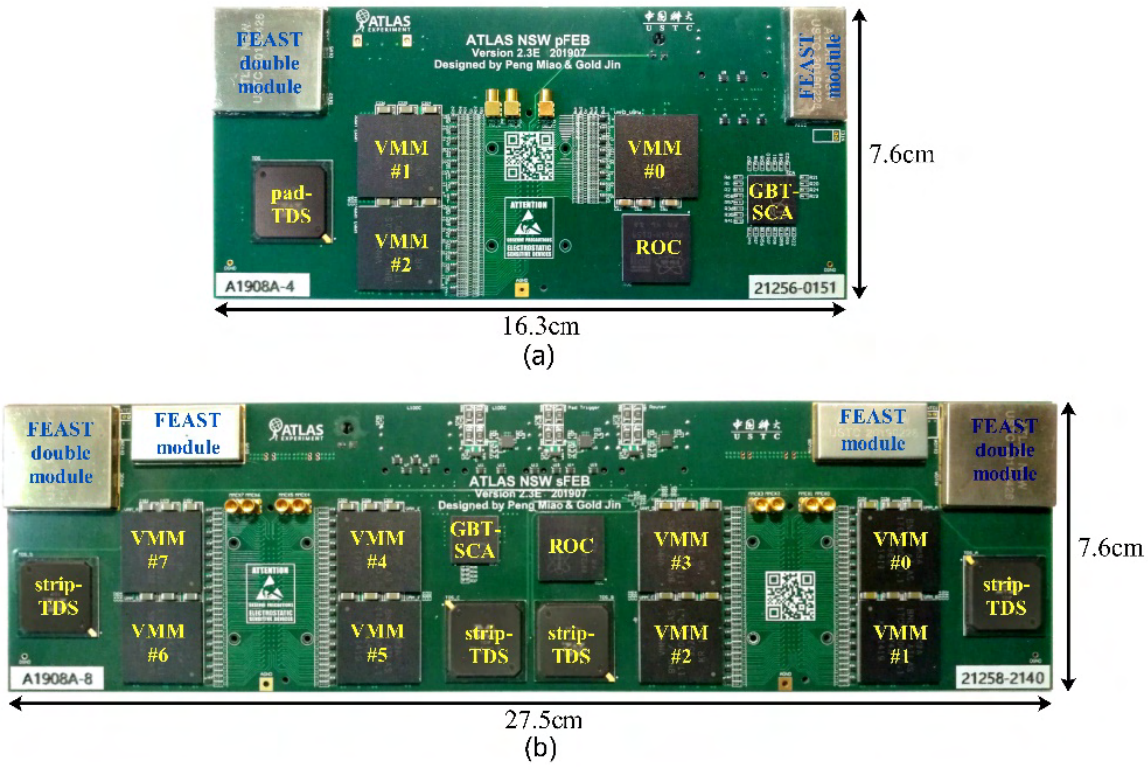


Figure 4.9: Assembled sTGC pFEB (a) and sFEB8 (b) boards [76].

CHAPTER 5

The Phase-I Upgrade: sTGC Mini-DAQ System

The Michigan ATLAS group was in charge of the sTGC Front-End (FE) electronics integration and commissioning during the LS2 period. The sTGC FE electronics system includes 1,536 FE boards, 11,776 ASICs and in total 354,000 detector channels. In addition, there are 32 pad trigger boards, 256 Router boards, and 288 L1DDCs mounted on the edge of the NSW. All trigger and readout channels have to be fully calibrated including gain, timing, and noise thresholds to establish proper operating parameters during the commissioning phase.

To verify the functionality of the front-end electronics, a system is needed to control the electronics and read out data from all FEBs. Several FELIX stations are used for the configuration and readout. However, the Pad Trigger board and the Router board, which are critical components in the sTGC trigger chain, don't offer special firmware dedicated for our commissioning task. A robust system to receive the sTGC trigger chain high-speed 4.8 Gbps TDS data and to provide the 640 MHz pre-L1 trigger signal to the strip TDS is needed. I was the person responsible for developing a mini data acquisition (mini-DAQ) system to handle those requirements. The developed system consists of an FPGA-based board, an adapter board, and relevant firmware and software. It aims to provide support for the sTGC front-end trigger chain commissioning (discussed in Chapter 6) and the sTGC trigger chain performance study (discussed in Chapter 7). The detail of the mini-DAQ system will be presented in this Chapter.

5.1 Mini-DAQ FPGA Firmware

The mini-DAQ Field Programmable Gate Array (FPGA) firmware is developed on the Xilinx Kintex-7 FPGA (on the Xilinx KC705 evaluation board) and the Xilinx UltraScale FPGA (on the mini-DAQ motherboard, a customized FPGA-based motherboard using the Xilinx XCKU035 FPGA). Figure 5.1 and Figure 5.2 show the pictures of these two boards.

The firmware can receive up to sixteen 4.8 Gbps high-speed TDS data links from either pFEBs or sFEBs. After deserialization and decoding, the TDS data is fed into different computational

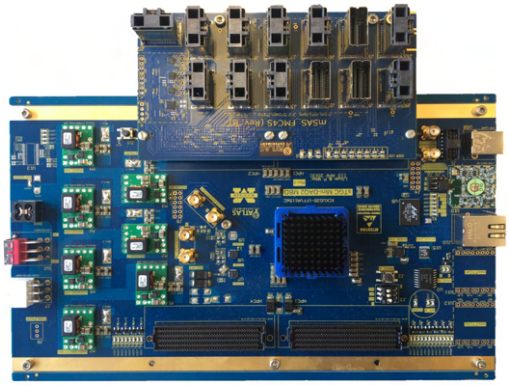


Figure 5.1: The custom-designed mini-DAQ motherboard with a XCKU035 FPGA. A mini-SAS to FMC adapter board is mounted on it.

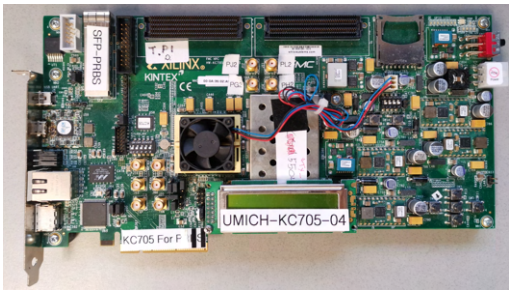


Figure 5.2: The Xilinx KC705 evaluation board.

modules for different tasks, as presented in Figure 5.3.

The Trigger chain checker module performs various test tasks during the commissioning. The Rate monitor module monitors the sTGC pad hit rate in the trigger chain covering the maximum 40 MHz hit rate. The Active data readout module reads out raw data from active TDS chips. The Online trigger module works as an emulated Pad Trigger board that generates pre-L1 triggers for the strip TDS readout. Each module is designed to cope with the TDS features and the details will be discussed in the rest of this section.

The firmware communicates with the control server through a 1-Gbps Ethernet link using the Xilinx Tri-Mode Ethernet Media Access Controller IP. The mini-DAQ software running on the server sends commands to the mini-DAQ firmware and receives test results, rate monitoring information, and active data.

The primary clock used is a 40 MHz BC clock from the FELIX system. This ensures the firmware uses the same clock source as the FEBs. The Xilinx Clocking Wizard LogiCORE IP is used to generate a 160 MHz clock as the primary logic clock for the firmware. Another 160 MHz external reference clock, also from the FELEX system, is used to receive the 4.8 Gbps TDS data.

5.1.1 Trigger Chain Checker

The Trigger chain checker is used for sTGC front-end electronics integration and commissioning. Several computational units inside this module perform different test tasks. Table 5.1 presents the functions that are integrated in the trigger chain checker.

The trigger chain checker can only perform one test task at a given time. A configuration register controls which unit to use. To start a test task, the control server needs to send a start

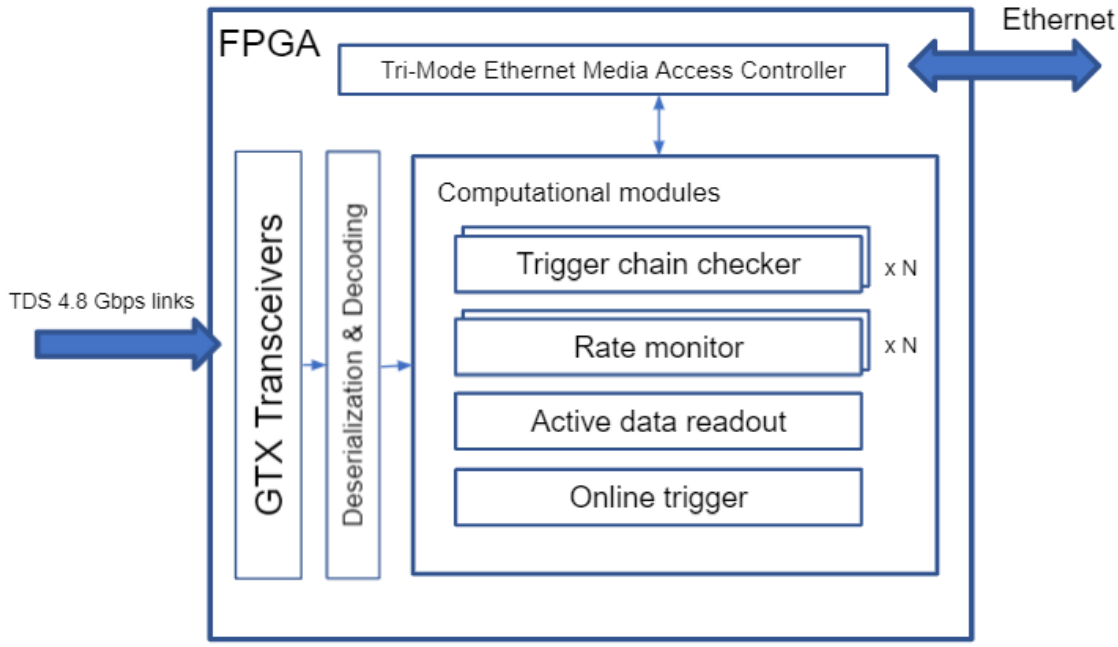


Figure 5.3: Architecture of the mini-DAQ firmware.

signal to the firmware. The test result will be sent back to the server once the task is finished.

Function Name	Description
PRBS Error Check	Check the PRBS error count for the TDS PRBS data
PAD BCID Rollover Value Check	Check and record the BCID rollover values
Pad Dead Channel Check	Check the dead channel of 104 pad TDS channels
Strip TDS Idle Mode Check	Check if the strip TDS is outputting idle packets
Strip TDS Trigger Receiving Check	Check if the strip TDS can receive and decode trigger signals correctly
Strip 6-bit ADC Readout	Read out the 6-bit ADC data from 128 strip TDS channels
Strip 6-bit ADC BCID Inquiry	Check and record BCIDs containing active 6-bit ADC data

Table 5.1: Trigger chain checker functions.

5.1.1.1 PRBS Error Check

To verify the connection and quality of the 4.8 Gbps link from the FEB TDS to the mini-DAQ system, the PRBS is used. The TDS can be configured to output the PRBS-31 pattern and a PRBS pattern checker is implemented in this unit to check the bit error count.

This test task is often the first step of any automatic test flow. It ensures the FEB TDS to mini-DAQ link is built, the configuration of the FEB is successful, and the transceiver on the mini-DAQ system is working correctly. Once the task unit receives the start request, it will count number of bit errors of the PRBS-31 pattern from the TDS for a certain period. The total number of errors will be sent back to the server.

5.1.1.2 Pad BCID Rollover Value Check

In this test task, the unit records the pad TDS BCID rollover values. There could be multiple rollover values in the data flow. The BCID is a 12-bit value and it can range from 0 to 4,095.

Table 5.2 shows the data format for the pad-TDS output. In every BC, it has 116 bits of effective data, consisting of 12-bit BCID and 104-bit channel ToT data. The 12-bit BCID is a timing ID, increased by one after each BC and reset to zero once the rollover value is met or the Bunch Counter Reset (BCR) signal is received. Two factors impact the rollover value. The first one is the configured rollover value inside the TDS. This configuration register tells TDS which value to roll over. The other factor is the BCR signal. Once the TDS receives the BCR, the BCID counter will be reset to zero. To ensure the TDS BC counter work properly, the BCR has to be sent to the TDS periodically, and the period should match the configured TDS rollover period.

Bit location	Content
115:104	12-bit BCID
103:0	104-bit channel ToT data

Table 5.2: Pad TDS data format.

Once the start signal is given, it will check the rollover values in the pad data. The rollover values are the BCIDs with their succeeding BCID equals to 0. The unit can record up to 90 rollover values. Ideally, there should be only one rollover value, and it should equal to the configured TDS rollover value or the period of the BCR signal. Common factors that will cause problems are:

- The period of the BCR signal is not the same as the configured TDS rollover period;
- Lack of the BCR signal;
- TDS configuration failure.

This test is useful to check if the TDS is configured correctly and the system is receiving the BCR signal.

5.1.1.3 Pad Dead Channel Check

The pad TDS receives ToT pulses from the VMM and generates one-bit hit information for each pad channel. To check if the pad TDS can receive the ToT pulse or if there are any dead channels, this task records the hit status of all 104 channels when an emulated signal is fed to each channel.

The Test Pulse (TP) function in VMM is used to provide emulated detector signals. Controlled by the TTC signal, the ROC sends a TP signal to the VMM. It triggers the VMM internal TP function, which generates an emulated pulse and then injects the signal to the VMM amplifier. Consequently, an ToT pulse will be sent to the TDS. If the TP functions are enabled for all VMM channels, each channel will send a ToT pulse to the TDS. Therefore, each bit of the 104-bit TDS data should have a non-zero value unless there are dead channels.

Once the start signal is given, it will monitor the hit information of each channel from the pad TDS data. In the meantime, the TP signal is given periodically to the system. After a certain amount of time, it will report the condition of each channel - whether or not it sees hits for each channel. The amount of time this task lasts is set to have at least one TP signal sent to the FEB.

By checking the 104-bit TDS hit information, this test can determine number of dead channels in the trigger chain. It could be due to dead VMM channels or dead TDS channels. Alternatively, a rare case is that the malfunction of the VMM TP. This could be mitigated by checking the Monitored Output (MO) of the VMM using an oscilloscope.

5.1.1.4 Strip TDS Idle Mode Check

The raw output data format of the strip TDS is listed in Table 5.3. Every strip packet contains four groups of 30-bit data. The first 4 bits of each 30-bit data are the header indicating whether the packet is a data packet or the null packet. For the idle packet, the header is 4'b1010, while it is 4'b1100 for the null packet. If there is no trigger signal provided to the strip TDS, it will only output idle packets so that the data header should constantly be 4'b1100.

	4-bit Header	26-bit Data
Data Packet	4'b 1010	Data 3
	4'b 1010	Data 2
	4'b 1010	Data 1
	4'b 1010	Data 0
NULL Packet	4'b 1100	NULL
	4'b 1100	NULL
	4'b 1100	NULL
	4'b 1100	NULL

Table 5.3: The strip TDS 30-bit raw data format.

Once the start signal is given to the task, it will monitor 65,536 (2^{16}) of the 30-bit data packets and record if all of those packets have the idle packet header 4'b1100. This test ensures that the TDS is running in the normal mode.

5.1.1.5 Strip TDS Trigger Receiving Check

This test checks whether the strip TDS can receive and decode pre-L1 trigger signals correctly. Besides receiving the TDS data, the mini-DAQ system can send emulated pre-L1 trigger signals to the strip TDS. Therefore, the unit will send a pre-L1 trigger signal to the strip TDS and check if the out strip TDS data contains the right pre-L1 trigger information.

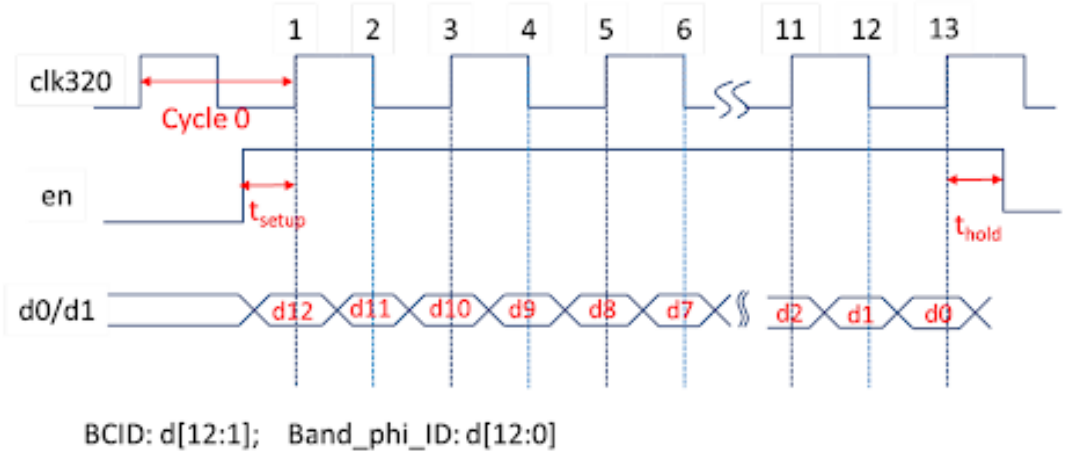


Figure 5.4: The trigger signals sent by the Pad Trigger board to the strip TDS [103].

Figure 5.4 shows the trigger signal sent by the Pad Trigger board to the strip TDS. It has a 320 MHz reference clock, an enable frame line, and two data lines. The trigger information contains a 12-bit BCID, an 8-bit Band-ID, and a 5-bit Phi-ID.

Table 5.4 shows the output data format for the strip TDS. One strip TDS data packet contains 104 bits of data. Bits 103 to 85 are the Phi-ID, Band-ID, and BCID from the pre-L1 trigger. Due to the limitation of the bandwidth, only the lower 6 bits of BCID are contained in the data packet. Since the firmware is in charge of both sending the pre-L1 trigger signal and receiving the data, matching between the two information can indicate whether the strip TDS can correctly receive and decode the pre-L1 trigger signal.

Once the unit receives the start signal, it will send emulated trigger signals to the strip TDS every 50 ns (2 BC). The values of the pre-L1 trigger are sampled from a 13-bit counter. The counter counts how many triggers have been sent out. The 12-bit BCID trigger information is the lower 12 bits of the counter. The Phi-ID is the highest 5 bits of the counter, and the Band-ID is the lowest

Bit location	Content
103:99	5-bit Phi-ID
98:91	8-bit Band-ID
90:85	Lower 6-bit BCID
84:84	High/Low Band
83:0	$14 \times$ 6-bit ADC

Table 5.4: The strip TDS output data format.

8 bits. The strip TDS will decode the pre-L1 trigger information, perform pad-strip matching, and send out data back to the mini-DAQ. The relevant pre-L1 trigger information included in the strip TDS data is:

- A "13-bit value" combined from Phi-ID and Band-ID;
- A "6-bit value" that comes from the BCID.

The unit will perform the following two comparisons to ensure the trigger information matches:

- The lowest 6 bits of the "13-bit value" should equal to the "6-bit value";
- Both the "13-bit value" and the "6-bit value" are increased by one compared to the last received values (except the rollover).

The unit will send and check 65,535 (2^{16}) times if the above two standards meet. An error counter will record how many times it fails, and this value will be sent back to the server as part of the test results. Any non-zero error counts will be considered failures of this test.

5.1.1.6 Strip 6-bit ADC Readout

This test aims to check if each channel could correctly receive and decode the 6-bit ADC data from the VMM. It is a challenging task since the strip TDS data will only be triggered with matched pre-L1 trigger information. This section presents how this unit achieves this difficult function.

Unlike the pad ToT data that only has one-bit hit information for each channel, the strip TDS will have 6 bits of the ADC data. Limited by the bandwidth, each strip TDS data packet will only contain data from 14 channels. Those 14 channels are chosen based on the Band-ID using the strip Lookup Table (LUT).

A strip TDS has 16 mapping LUTs. Each LUT maps one Band-ID to one Leading strip. According to the TDS design, one Band-ID or one Leading strip covers 17 strips. Figure 5.5 shows the location of the Leading strip inside the 17-strip group (The leading strip is the #2 strip

of the group). Based on whether or not the #1 strip, the Checking strip, is fired, the TDS sends out data for either #0 – #13 strips or #3 – #15 strips. The High/Low band bit inside the packet tells which group it is.

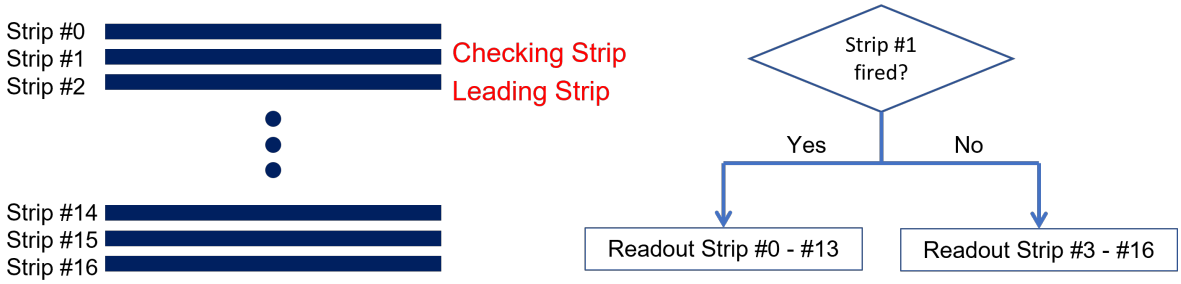


Figure 5.5: The Band-ID to the strip channel grouping.

Under this circumstance, only #3 – #13 strips are guaranteed to be read out. To have the data from all 128 channels, multiple pre-L1 triggers are needed to be sent to the strip TDS. Table 5.5 shows how the strip TDS LUT is designed to cover all channels.

In total 13 LUTs are used. For a typical case such as LUT #5, the Band-ID is set to 6, and the leading strip is mapped to strip #46. Once a trigger with a Band-ID of 6 is sent to the strip TDS, the strip TDS will first check whether the Checking strip, #45, is fired. If the #45 strip is fired, the strip TDS will send strip #44 to #57. Otherwise, the strip TDS will send strip #47 to #60. The complete cover range is strip #47 to #56.

A corner case of this design is how to check whether strip #0 and strip #1 are fired. In Table 5.5, the last column shows the absolute cover range. It only ranges from #2 – #127. To specifically check strip #0, LUT #0 is set to Band-ID 1 with the leading strip as #1. Once the strip TDS receives a trigger with a Band-ID of 1, the triggered data will directly tell if strip #1 is fired or not. For the same reason, LUT#1 with the leading strip #2 has the status of strip #1.

Once the start signal is given, it will send 13 pre-L1 trigger signals with the Band-ID increasing from 1 to 13. In the meantime, the TTC TP signal will be sent periodically to the FEB. This is the same method used for the pad TDS dead channel check. The BCID of the pre-L1 trigger is set to match the time difference between the TTC BCR signal and the TTC TP signal. Section 5.1.1.7 describes another test used to find which BCID to send. Once the BCID value is found, all settings are fixed and no further tuning is needed.

After the unit sends 13 pre-L1 trigger signals to the strip TDS, the strip TDS will send out 13 data packets containing 6-bit ADC data for all 128 channels. Inside the unit, it has 128 6-bit data buffers to record data from all channels. Those buffers will be reset to zero at the beginning of the task. Once a packet is received, it will decode which 14 channels arrived and then fill the buffer accordingly. After all 13 packets are received, the unit will pack data from all 128 channels and

LUT #	Band-ID	Leading Strip	Checking strip	Readout Strip (Checking strip fired)	Readout Strip (Checking strip not fired)	Abosulte strip coverage
0	1	#1	#0	#0 - #13	#2 - #15	#2 - #13
1	2	#2	#1	#0 - #13	#3 - #16	#3 - #13
2	3	#13	#12	#11 - #24	#14 - #27	#14 - #24
3	4	#24	#23	#22 - #35	#25 - #38	#25 - #35
4	5	#35	#34	#33 - #46	#36 - #49	#36 - #46
5	6	#46	#45	#44 - #57	#47 - #60	#47 - #57
6	7	#57	#56	#55 - #68	#58 - #71	#58 - #68
7	8	#68	#67	#66 - #79	#69 - #82	#69 - #79
8	9	#79	#78	#77 - #90	#80 - #93	#80 - #90
9	10	#90	#89	#88 - #101	#91 - #104	#91 - #101
10	11	#101	#100	#99 - #112	#102 - #115	#102 - #112
11	12	#112	#111	#110 - #123	#113 - #126	#113 - #123
12	13	#123	#122	#121 - #127	#124 - #127	#124 - #127
13	-	-	-	-	-	-
14	-	-	-	-	-	-
15	-	-	-	-	-	-

Table 5.5: LUTs used for the strip TDS.

send them back to the server. In total, there will be 768 (6×128) bits of effective data.

The unit also checks if the pre-L1 trigger information received match with the designed pattern. The Band-ID of those 13 packets will start at 1, increase by one each time, and end at 13. The BCID and Phi-ID values are fixed. If the trigger information does not match, this test will be considered a failure.

This unit can be used to check the dead channel of the strip TDS. It can also be used to check the 6-bit ADC linearity. A different configuration of the VMM can change the amplitude of the VMM TP. The 6-bit ADC linearity scan is a standard test step in the on-bench FEB check, which will be discussed later.

5.1.1.7 Strip 6-bit ADC BCID inquiry

This test records the BCIDs that contain active 6-bit ADC data. The biggest puzzle in the trigger chain strip 6-bit ADC readout is what BCID to send. The strip TDS uses both BCID and Band-ID to perform the trigger matching. The BCID matching window can be configured to either one BC or two BCs.

In this test, the TTC is configured in the same way as used in the 6-bit ADC Readout test. The BCR and TP signals will be sent to the FEB periodically, and the time interval is fixed. As a result, only one BCID contains the 6-bit ADC data. However, the BCID has 4,096 possible values, and a random value can rarely trigger the 6-bit ADC value. This test sends the trigger signal to scan all 4,096 BCIDs with all 13 LUT Band-IDs. In total 53,248 ($4,096 \times 13$) pre-L1 triggers are sent. The unit monitors which BCID contains active 6-bit ADC data and records those BCIDs in the buffer. It has 90 BCID data buffers to store.

This task accelerates the debugging process of finding whether the strip TDS has 6-bit ADC data and which BCIDs contain the data. It serves as a useful debugging tool.

5.2 Pad TDS Rate Monitor

This module records the hit rate of each channel for the pad TDS. The pad TDS outputs a one-bit hit status for its 104 channels every BC. The maximum hit rate of a channel is thus 40 MHz. As presented in Figure 5.6, it uses an individual channel counter to count the hit rate. In every second (the time interval is adjustable), it reports the result to the server using the Ethernet link. To cover the 40 MHz range, the counter is set to 26 bits which means it can record up to 67 MHz (2^{26}). For a single TDS, the effective data are 2,704 (26×104) bits.

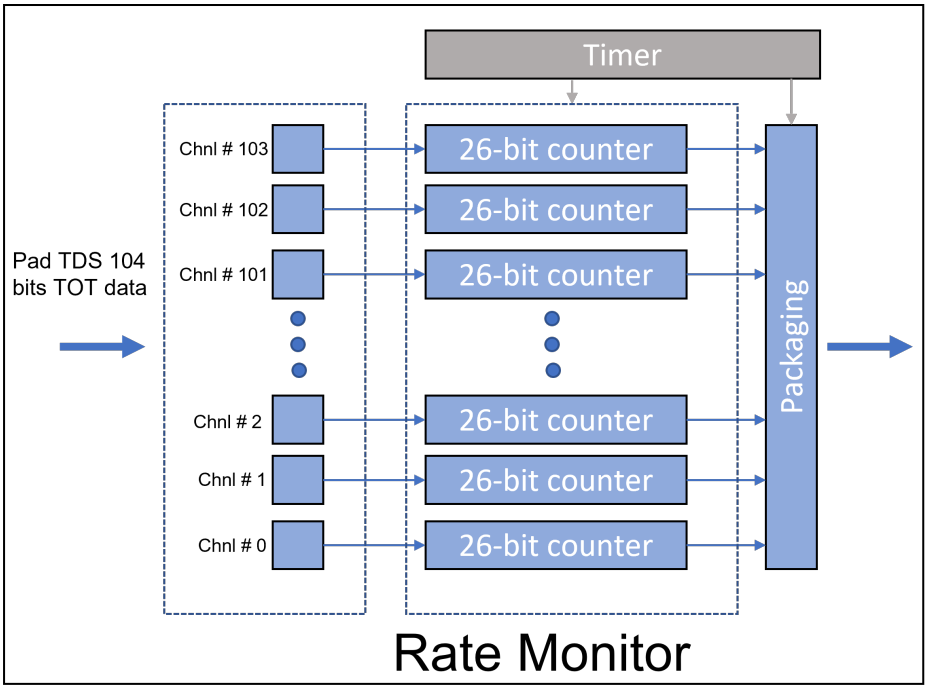


Figure 5.6: Architecture of the Rate Monitor module.

This function could be used to monitor the pad TDS noise rate during the electronics integration and commissioning. At this stage, no working gas and high voltage are applied, and everything that the pad TDS outputs are due to electronics noise (except VMM TP). By changing the threshold of the VMM, the module can be used to monitor the noise rate as a function of the threshold. This is useful to get the S-Curve in the trigger chain.

It could also be used to monitor the hit rate during the cosmic ray study. The cosmic ray hit rate is usually constant at a specific sea level. However, common ground noises are sometimes injected into the system that fire VMM channels. This monitoring module can indicate the presence of a sudden noise burst or increased background noise.

5.3 Online Trigger

This module uses the pad TDS data from four layers of an sTGC quadruplet to generate the online trigger. The pad TDS data from a quadruplet is fed into this module. Those are the real-time sTGC pad hit status of the entire quadruplet. The data will be first buffered in a shift register with a depth of 8 and a size of 120×8 (a TDS packet has 120 bits). It allows the module to synchronize the TDS data among different layers. It also gives the possibility to perform a multi-BCID-window coincidence match.

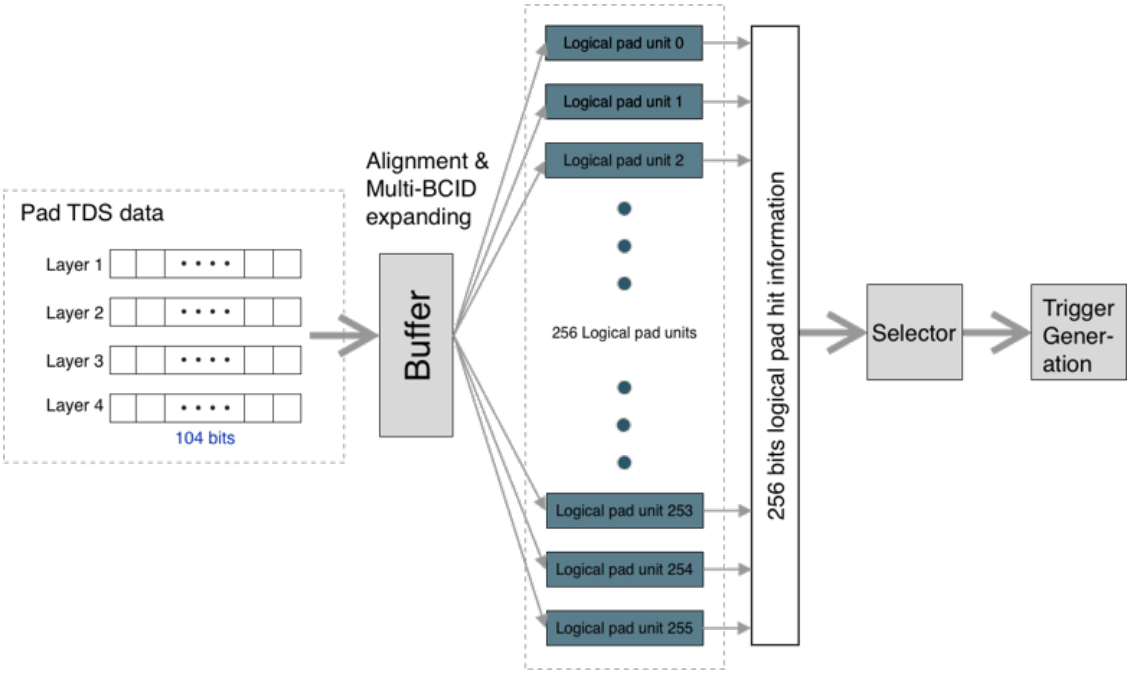


Figure 5.7: The online trigger scheme.

Once the pad TDS data from four layers is synchronized and extended (for the multi-BCID-

window match), it will be routed to 256 logical pad units. Each logical pad unit contains four configurable 104-to-1 multiplexers and one configurable coincidence module. The architecture of the logical pad unit is presented in Figure 5.8.

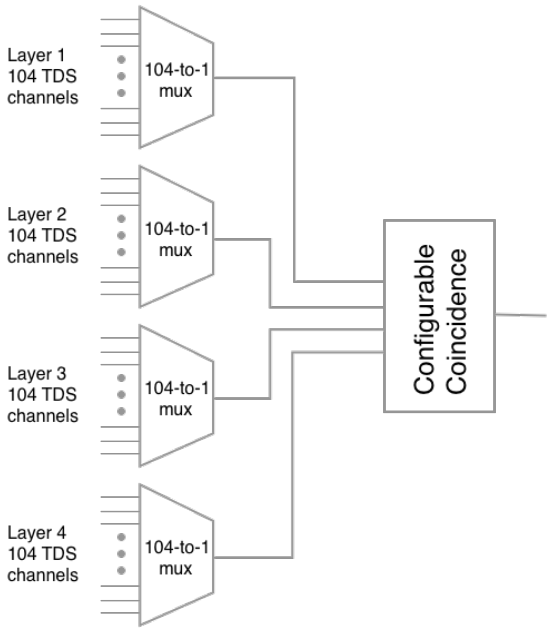


Figure 5.8: Architecture of the logical pad unit.

Each multiplexer selects one of the 104 TDS channels. A 7-bit configuration register (2^7 = 128 > 104) tells the multiplexer which channel to choose. The four multiplexers in the logical pad unit select four pads from each layer. The combination of four pads from four different layers is called a logical pad. In this online trigger module, there are in total 256 logical pads. How the logical pad combination is generated will be discussed in Section 7.4.1.

For each logical pad, the coincidence module monitors the status of the four pads. There are 16 possible hit statuses of these four pads. The coincidence is made based on a 16-bit configuration register, which servers as the truth table value for those 16 possible status combinations. The value "1" means this status is considered as fired.

Table 5.6 presents the 16-bit register for the 3 out of 4 coincidences. It is set as 16'b 1110_1000_1000_0000 (binary) or 16'he880 (hex). The index order of this 16-bit register is directly correlated to the hit status of these four pads. For example, the 7th bit of the 16-bit register is 1, while the binary form of 7 is 4'b0111. It tells the coincidence module that if layer 4 is idle while layer 3, layer 2, and layer 1 are fired, this logical pad should be considered as fired.

This configuration provides highly flexible usage. For 4 out of 4 coincidences, simply set the 16-bit configuration bit to 16'h8000. If a layer is dead, it can also be switched to 2 out of 3 coincidences.

Bit #	16-bit configuration in binary	16-bit configuration in hexadecimal	Hit status combination of four layers
15	1	e	1111
14	1		1110
13	1		1101
12	0		1100
11	1	8	1011
10	0		1010
9	0		1001
8	0		1000
7	1	8	0111
6	0		0110
5	0		0101
4	0		0100
3	0	0	0011
2	0		0010
1	0		0001
0	0		0000

Table 5.6: The 3-out-of-4 coincidence configuration table.

Each logical pad will give one-bit hit information, thus there are 256 bits for every BC. Since it is possible that more than one logical pad being hit in one BC, a priority selector is used, which prefers to select the logical pad with a lower index number.

After the logical pad is selected, its related Band-ID and Phi-ID will be extracted from the stored configuration registers. A trigger signal will be sent out with the BCID, Band-ID, and Phi-ID information.

5.4 Active Data Readout

This module collects, filters, and packages the raw TDS data. The KC705 evaluation board can receive 4.8 Gbps output from four TDS chips, and the mini-DAQ motherboard can receive sixteen links with 4.8 Gpbs TDS data each. The total input data rate is thus 19.2 Gbps (4×4.8 Gpbs) or 76.8 Gbps (16×4.8 Gbps). However, the bandwidth of the Ethernet used is limited to 1 Gbps. Luckily, with cosmic rays, the majority of the TDS packet data are idle packets that do not contain effective data. This module will filter out idle packets and only read out active data packets.

Figure 5.9 shows the structure of this module. It has 12 channel FIFO (First In, First Out) with a depth of 512 and a width of 116 bits. Each channel FIFO can handle one TDS data link, and only the active data will be written to the channel FIFO. For the pad TDS, active data means the

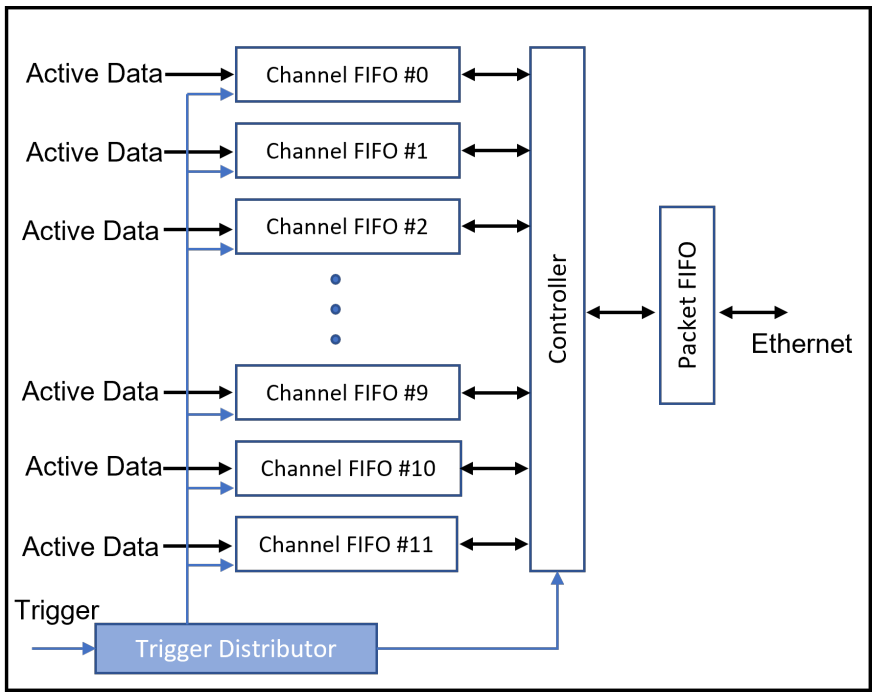


Figure 5.9: Architecture of the Active Data Readout module.

104-bit ToT data are non-zero. For the strip TDS, active data means the lower 84-bit 6-bit ADC data are non-zero. Besides receiving the TDS data, the channel FIFO can also be used to receive other useful information. As discussed in the previous section, the hit status of the logical pad can also be fed into the channel FIFO.

This module can be operated in the trigger mode or the triggerless mode. For the triggerless mode, any active data will be fed into the channel FIFO. For the trigger mode, a trigger signal is required to be fed into the trigger distributor. The trigger distributor will open a trigger time window, which will work as an enable signal for the channel FIFO. Only active data within this time window will be written into the channel FIFO. The size of the trigger time window is configurable. The trigger signal could be an external trigger signal from an external scintillator, or an internal trigger signal.

The controller is in charge of reading out data from the channel FIFO and writing them into the data FIFO. It has an internal timer. Under a configurable interval, the timer will trigger the controller to begin its readout process. Each of the processes sends out one data packet. Figure 5.10 shows the data format. The data packet is fixed in length, 2040 bits (17×120 bits), consists of sixteen 120-bit data slots and one 120-bit channel FIFO status. Every 120-bit data contains 4-bit channel-ID number and 116-bit channel FIFO data. The 120-bit channel FIFO status combines the 10-bit remaining data count value from the 12 FIFO channels.

Here is the detailed readout process:

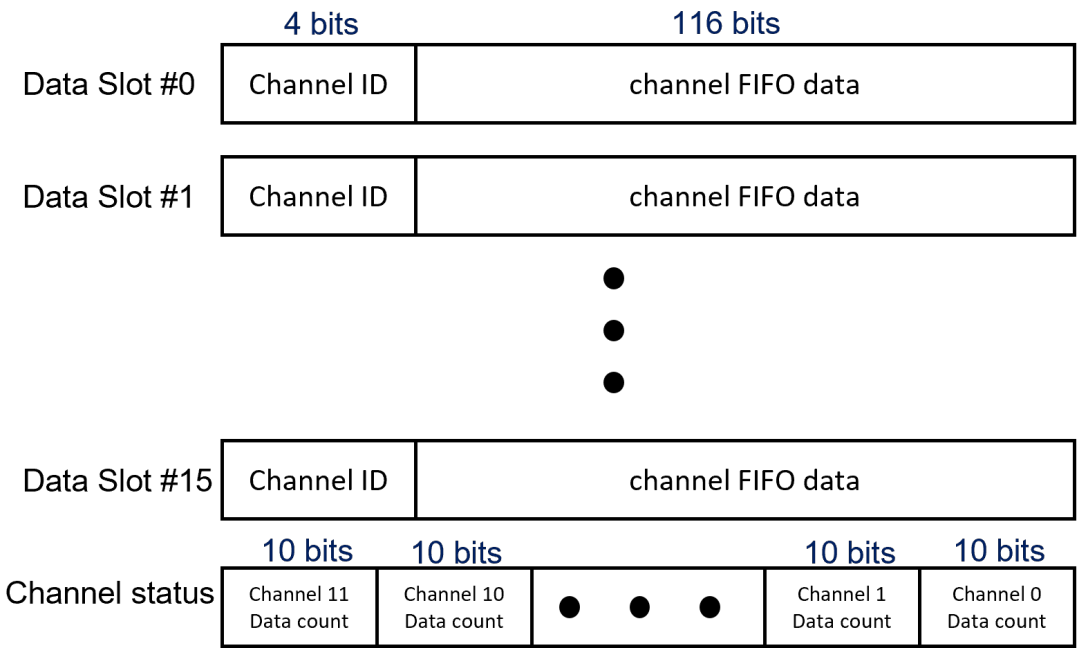


Figure 5.10: Data format of the active data readout packet.

- Step 1: The controller samples the empty signal of the 12 channel FIFO;
- Step 2: The controller read one packet from any non-empty channel FIFO in the order of channel FIFO #0 to channel FIFO #11. The 116-bit channel data will be padded with a 4-bit channel number in the front and written to the packet FIFO;
- Step 3: If all the 16 data slots are filled or there is no non-empty channel FIFO, go to Step 4. Otherwise, repeat Step 1 to Step 3;
- Step 4: Write the 120-bit channel FIFO status to the packet FIFO;
- Step 5: End of one readout process.

Since the length of every packet is fixed, the maximum data rate depends on the configured packet interval, but no more than 1 Gbps. If the active TDS data rate is low, all packets will be sent out. If the active TDS data rate is high, all 16 data slots will be used, and the packet also tells how many TDS data packets are still left in the channel FIFO. The module could be configured to either drop those remaining TDS data or wait till the next readout process.

This module serves an essential role for cosmic ray study. It is used to read out the raw pad TDS and strip TDS data to the server. Further data analysis is performed and will be discussed in Chapter 7.

5.5 Mini-DAQ Software

The mini-DAQ software is developed using Python with PyQt. Figure 5.11 shows the main Graphical User Interface (GUI). The software communicates with the mini-DAQ firmware using the Ethernet cable from the FPGA board to the server. It can send commands to control all mini-DAQ firmware configuration registers. It can also send a start signal to the firmware to initiate a test task. The test result, TDS raw data, and rate monitor information are captured using the second thread to monitor the Ethernet traffic. Those data are stored in the server disk for further analysis. Moreover, it can configure the FEBs by SSH (Secure Shell) to the FELIX system.

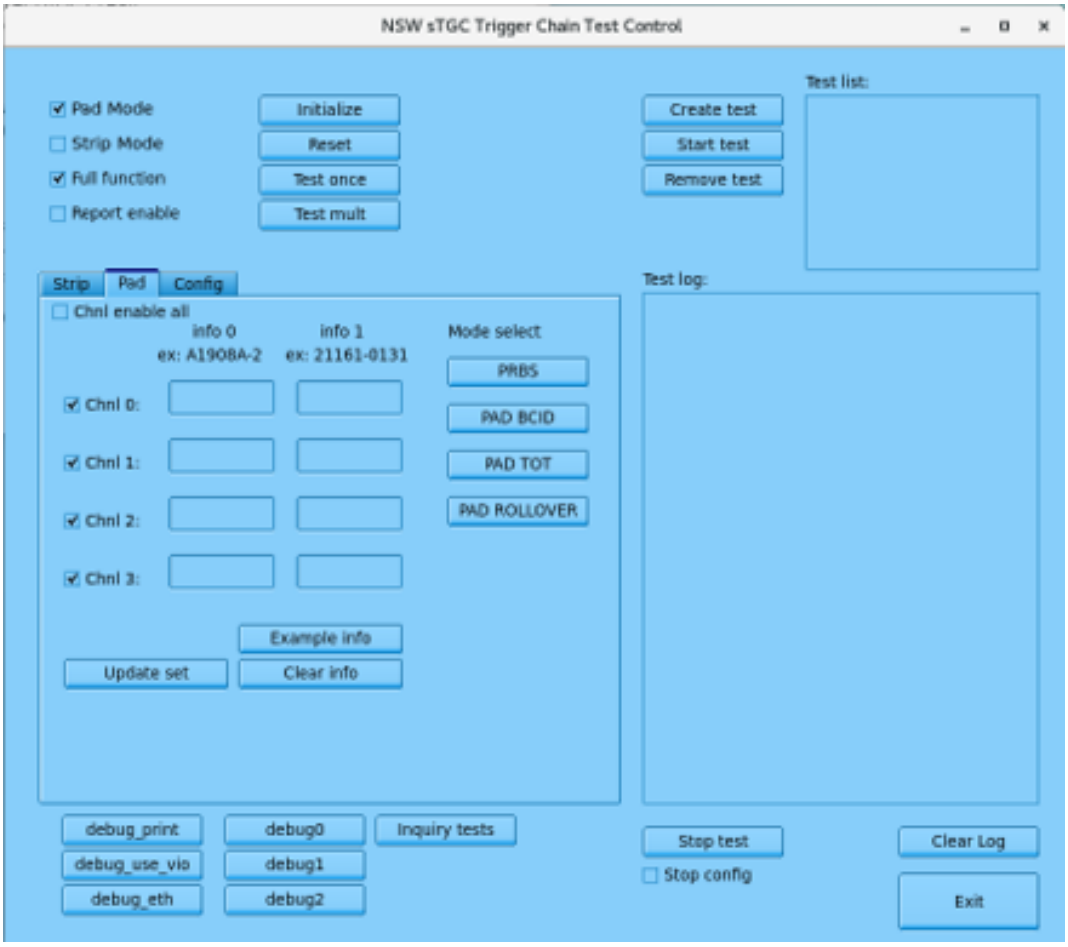


Figure 5.11: The mini-DAQ software GUI.

This software also handles the FEB trigger automatic test flow. It configures the FEBs, requests different test tasks on the mini-DAQ system, read the replied results, and follows the designed test flow. Detailed automatic test flow will be presented in Chapter 6.

CHAPTER 6

The Phase-I Upgrade: sTGC Trigger Chain Front-end Electronics Commissioning

Figure 6.1 shows the sTGC front-end electronics integration and commissioning flow. The preparatory tasks, electronics mechanical integration, and electronics testing and validation are the three major parts. In this chapter, I will go through the workflow and focus on the on-bench FEB trigger chain reception test and on-wedge trigger chain interface connectivity test.

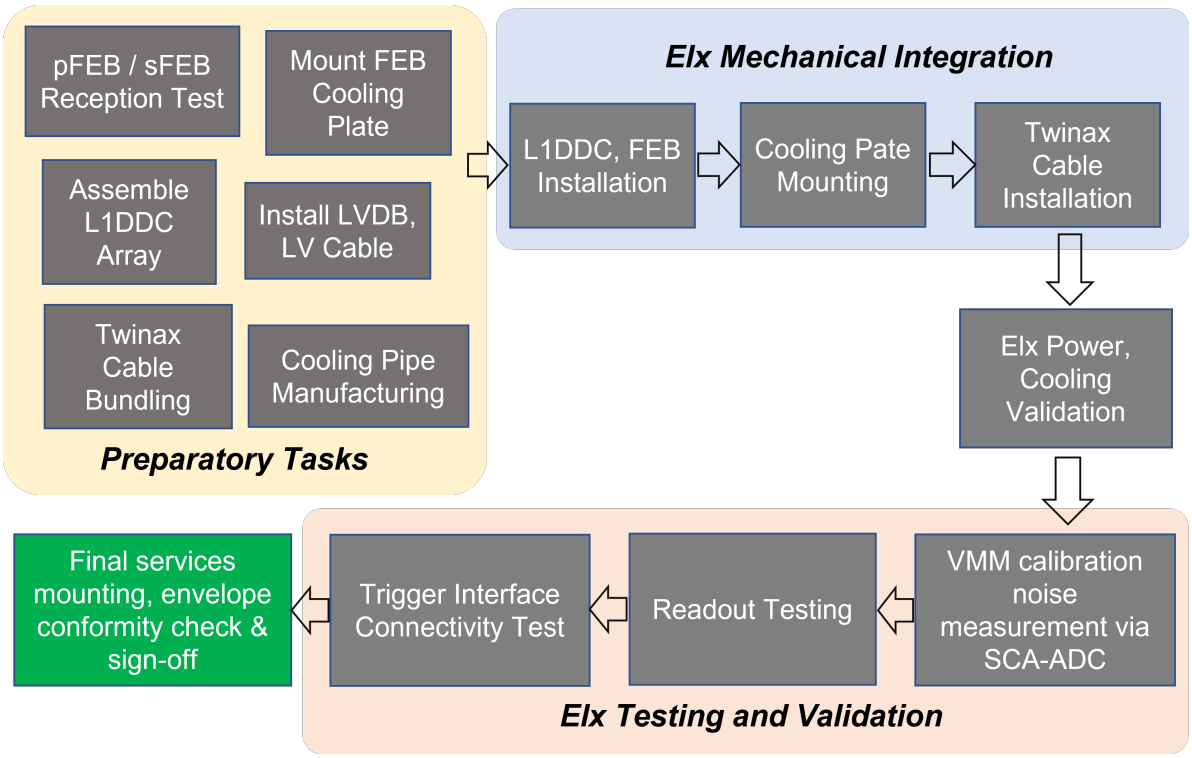


Figure 6.1: Procedure of the sTGC front-end electronics integration and commissioning.

6.1 sTGC Front-end Electronics Integration and Commissioning procedure

The integration and commissioning procedure for front-end electronics on sTGC chambers is listed below:

- Preparatory Tasks
  - Once the FEBs arrive at CERN, they will go through an on-bench test on the readout and trigger chains. Only boards that pass both tests will be mounted with cooling plates. Problematic boards will require further investigation and repairs;
  - Each sTGC wedge is equipped with two 4-L1DDC arrays. The assembly of the L1DDC arrays will be prepared in advance. Two LVDBs (Low Voltage Distribution Boards) will also be mounted on the wedge with the Low voltage (LV) cables routed to the designated area beforehand;
  - Two bundles of Twinax cables are prepared for each wedge, which is important for neat cabling. Cooling pipes are also manufactured in advance.
- Electronics Mechanical Integration
  - Install twelve sFEBs, twelve pFEBs, and two 4-L1DDC arrays on the wedge once they passed all checks mentioned above;
  - Mount the cooling pipes with the FEB cooling plates;
  - Install the Twinax cable bundle;
  - Connect the L1DDC arrays to the fiber panel of the testing FELIX station.
- Electronics Testing
  Before starting the electronic test on wedges, the cooling system needs to be checked for leakage. The power system will also be checked to confirm the current is within the normal range. Here are the steps for the testing:
  - Measure the channel noise level using the VMM analog output or using the ADC output from the SCA. Compare new measurements with previous measurements done before the integration;
  - Step 2: Electronics Readout chain test;
  - Step 3: Electronics Trigger chain connectivity test.

Once all tests are passed, the fibers and cooling pipes will be disconnected. Final server parts will be mounted on the wedge. An envelope conformity check will be performed before signing off and delivering the wedge for the wheel integration.

6.2 On-bench FEB Trigger Chain Reception Test

Once our group receives the FEBs (produced by the ATLAS group at the University of Science and Technology of China), we will perform a reception test on the trigger chain and the readout chain. This section focuses on the trigger chain reception test.

The mini-DAQ system with the KC705 evaluation board is used during this on-bench test. It can simultaneously handle four pFEBs or one sFEB. Figure 6.2 shows the on-bench test station with one sFEB connected. An automatic test flow was developed for pFEB and sFEB tests, and the details will be presented in this section.

For convenience, we prepared and attached a small sheet containing the SCA ID on each board. The SCA ID, which is unique to each SCA, is used to identify the FEB. The sheet also contains a QR code that holds the same information. This allows us to start the automatic test flow by scanning the QR code on each FEB. The SCA ID will be automatically captured and written to the test report.

6.2.1 On-bench pFEB Trigger Chain Automatic Test Flow

The two main things that need to be verified for pFEBs are the TDS link (checked by PRBS) and dead channels. Figure 6.3 shows the automatic test flow for the pFEB.

Starting with scanning the QR code on each board, the mini-DAQ software stores the SCA ID and uses it to identify the test report. Followed by powering the system, opening the FELIX core and the OPC-server, and inquiring about the SCA ID from the FELIX system, the mini-DAQ software will compare the two SCA IDs. If they don't match, the software will fail the test at this stage. If the two SCA IDs match, the software will configure the TDS to the PRBS mode. While waiting for the configuration process to finish, it reads the log message from the OPC-server on whether the configuration is succeeded. If the configuration is failed, the software will try five more times until it ends the automatic test flow and marks it as failed.

If the configuration is successful, the software will check the PRBS error count using the mini-DAQ PRBS Error Check test task mentioned in Section 5.1.1.1. The PRBS test will only be considered as a pass only if the error count value is zero. Otherwise, the software will end the automatic test and report it as a failure. An unstable cable connection usually causes a PRBS check failure.

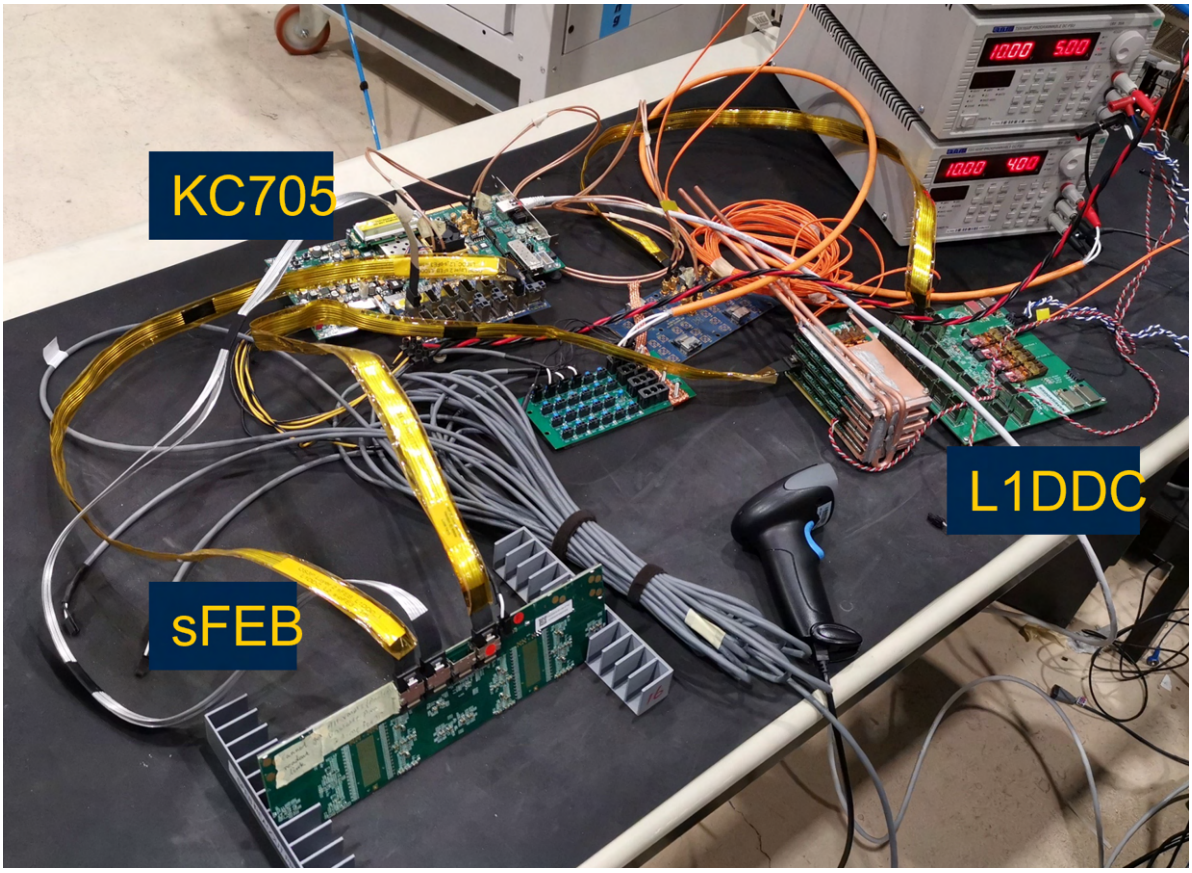


Figure 6.2: The on-bench trigger chain test station with the KC705 board and one sFEB.

Next, the software will check dead channels using the Pad Dead Channel Check test task described in Section 5.1.1.3. It will configure the pad TDS to the normal working mode and enable the TP function on all VMM channels. Once the configuration is succeeded, the software will request and start the Pad Dead Channel Check task 1,000 times. It will check if there are 1,000 hits received by each channel. A dead channel is marked if it sees zero hit count. The standard for the pad TDS to pass the test is that the two connected VMMs have no more than one dead channel.

The software will generate a test report at the end using the SCA ID as the identifier. It summaries the test results and reports dead channels observed.

6.2.2 Clock phases

Before jumping to the sFEB automatic test flow, an important fact needs to be brought up - the clock phase setting. Figure 6.4 is a simplified diagram that shows the clock and data flows in the trigger chain. The FELIX system configures the sFEB and sends the BC clock and TTC signal through the L1DDC. The FELIX system also distributes a 40 MHz clock signal and a 160 MHz

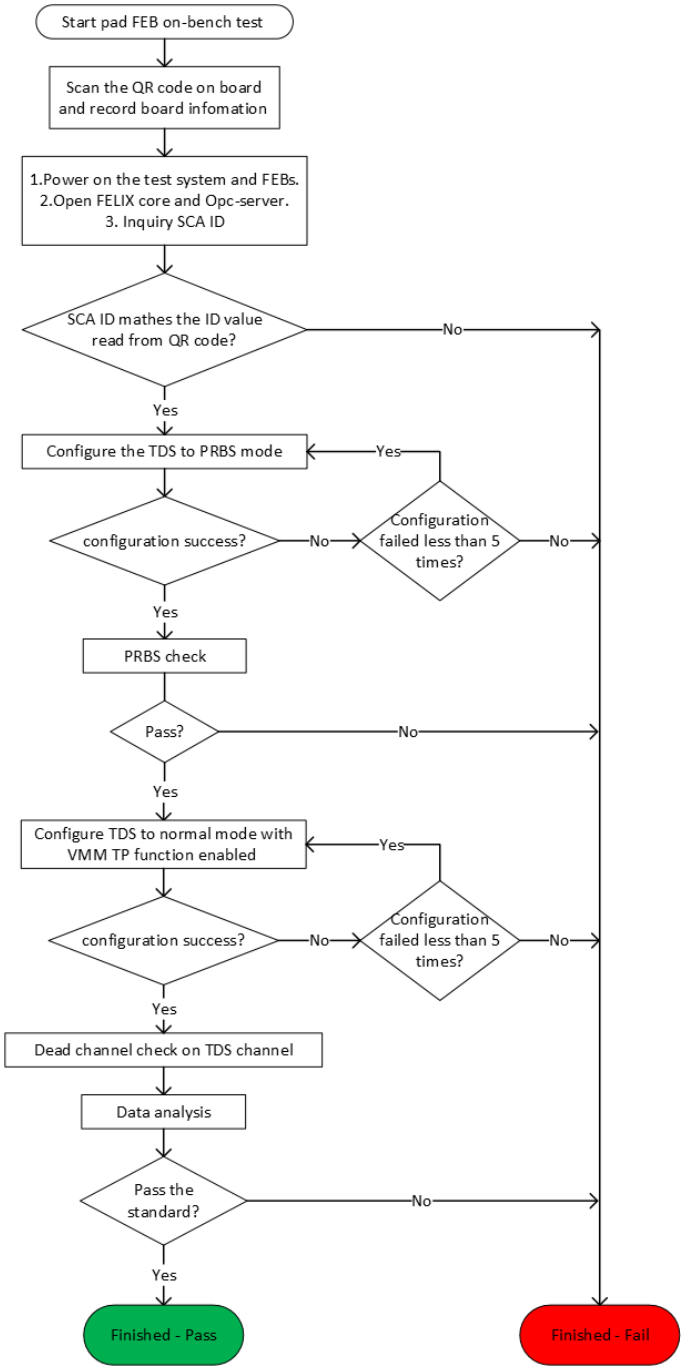


Figure 6.3: The pFEB on-bench automatic test test flow.

clock signal to the mini-DAQ system, ensuring that both the FEB and the mini-DAQ system use a clock from the same source.

Inside the sFEB, the ROC receives the BC Clock (40 MHz) from the L1DDC Elink. The ePLL (extended Phase Locked Loop) Core of the ROC distributes the BC clocks to all TDS and VMM

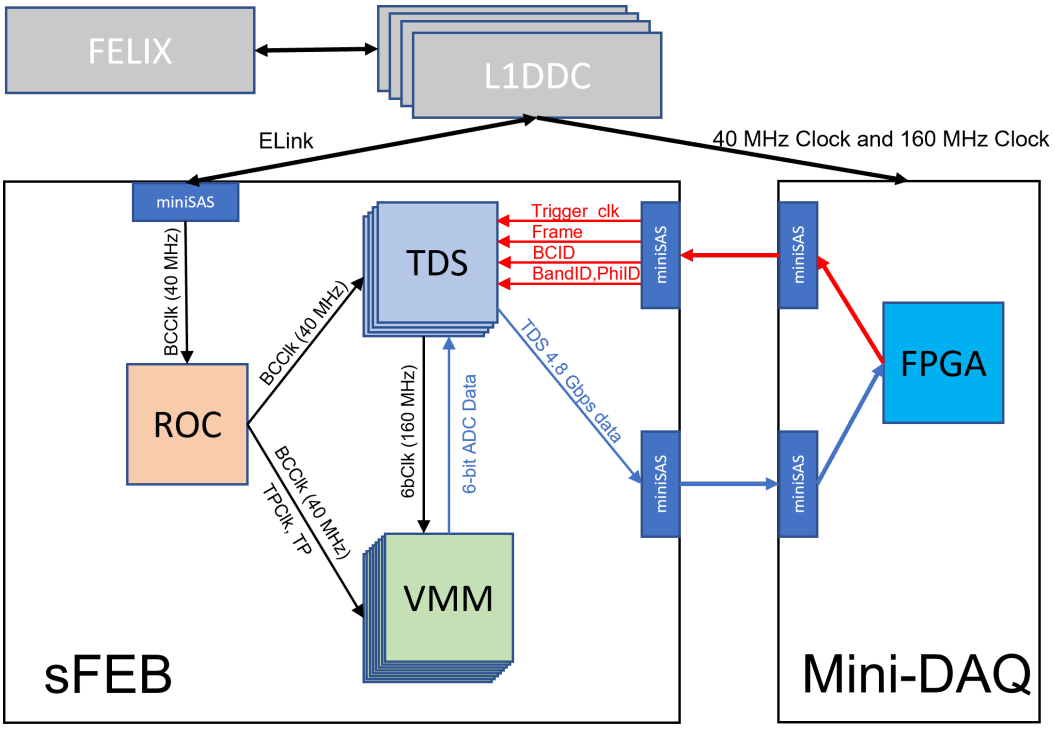


Figure 6.4: sFEB trigger chain data and clock connection.

ASICs. Every TDS sends two "6b" Clocks (160 MHz) to two VMMs, that the VMM used for 6-bit ADC direct output. The mini-DAQ system emulates both the Pad Trigger board and the Router board in the system. It sends trigger signals to the TDS on the FEB and receives the TDS 4.8 Gbps output data. There are four lines for the trigger signals sent by the Pad Trigger board and they are the Trigger clock line, Frame line, d0 (BCID) line, and d1 (Band-ID and Phi-ID) line.

When a clock is distributed from one chip to the other, it goes through the internal ePLL of the chip, which usually offers many phases to choose from. Hence, the phase of each clock is vital for avoiding timing violation. The two major clocks directly related to the trigger chain data flow are the ROC-TDS 40 MHz BC Clock and the TDS-VMM 160 MHz "6b" clock.

6.2.2.1 ROC-TDS 40 MHz Clock Phase

Since the main external 40 MHz clocks for the FEB and the mini-DAQ system are both from the FELIX system, there is a fixed clock phase difference between the TDS BC clock and the 320 MHz trigger clock to the TDS. This clock phase difference is directly correlated to the TDS trigger receiving correctness. The difference is determined by the phase of the ROC-TDS 40 MHz clock, as well as the Twinax cable lengths between the L1DDC to sFEB, L1DDC to mini-DAQ, and the mini-DAQ to sFEB.

The ROC-TDS 40 MHz clock is provided by the ROC internal ePLL, which offers 128 steps of phase tuning possibility. The mini-DAQ firmware can check if the TDS receives the trigger signal correctly by the Strip TDS Trigger Receiving Check test task presented in Section 5.1.1.5. The mini-DAQ software also has a built-in automatic ROC-TDS clock phase scan process. It scans the phase from 0 to 124 with a step size of 4 (by different FEB configurations), and checks the TDS trigger receiving correctness with the mini-DAQ firmware. A study was performed scanning the ROC-TDS clock phases with different L1DDC-to-sFEB cable lengths.

Figure 6.5 shows the phase scan results. The four sub-figures are the results for the four TDSs on one sFEB. The *x*-axis is the phase setting of the ROC-TDS 40 MHz clock, and the *y*-axis is the length of the Twinax cable from the L1DDC to the sFEB. Only the white areas are the good phases that the TDS receives the trigger signal correctly. As the cable length changes, the good phases shift. This is expected as the cable length changes the signal transmission delay.

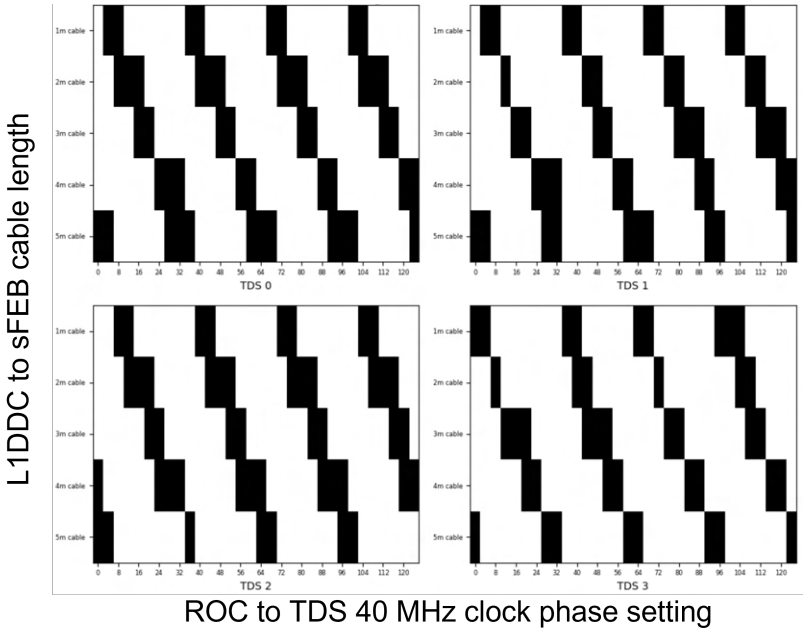


Figure 6.5: Working ROC-TDS clock phase (white areas) for different L1DDC-to-sFEB cable lengths. The four sub-figures are the results of four TDS chips on the same sFEB.

Only part of the ROC-TDS 40 MHz clock allows the trigger system to work correctly. Once the cable length is fixed for the on-bench setup, this automatic scan is performed once to choose the operational phase. A good ROC-TDS clock phase also works for other sFEBs as long as the cable lengths are fixed.

6.2.2.2 TDS-VMM 160 MHz Clock Phase

The TDS sends a programmable 160 MHz clock (TDS-VMM clock) to VMM, and VMM uses this clock to generate the 6-bit ADC direct charge output to TDS. TDS uses its internal 160 MHz clock to sample this 6-bit data. The TDS-VMM clock can be programmed with 32 different phases. A proper phase helps to avoid timing violations.

Another automatic test procedure is integrated into the mini-DAQ software for this TDS-VMM clock phase scanning. It configures the TDS-VMM clock to different phases sweeping from 0 to 31 and uses the mini-DAQ firmware Strip 6-bit ADC Readout task (presented in Section 5.1.1.6) to read out the 6-bit ADC value. The amplitude of the VMM TP is set to a constant value. If The TDS can decode the 6-bit ADC value correctly, the result should be a constant value.

Figure 6.6 shows the result of the scan. The software requests the 6-bit ADC value 100 times for each point, and the median value is used as the measured result. In the figure, there are two spots in which the 6-bit value changes dramatically. Those correspond to the bad phase areas where the TDS can not sample the 6-bit ADC data correctly. Those areas need to be avoided.

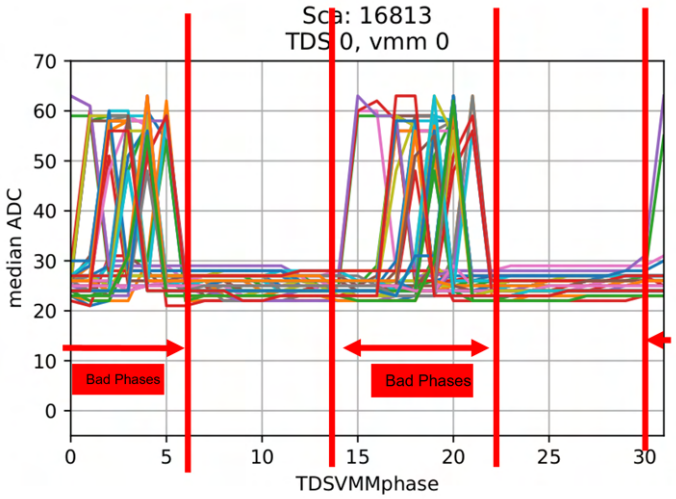


Figure 6.6: sFEB 6-bit ADC scan with different TDS-VMM clock phases. Each line presents one channel. The amplitude of the VMM TP is fixed during the scan.

We performed the TDS-VMM phase scan over the 48 sFEBs in the first batch and Figure 6.7 presents the results obtained. The eight sub-figures are the results of 8 VMMs from each sFEB. The x-axis is the TDS-VMM 160 MHz clock phase, and the y-axis is the SCA ID of each FEB. The black areas correspond to the phases where the TDS has wrong samplings of the 6-bit ADC value, while the white areas correspond to the working phases. As shown in this plot, every sFEB behaves differently. Consequently, this TDS-VMM 160 MHz clock phase scan is needed in the on-bench sFEB test to guarantee the correctness of the 6-bit ADC data sampling.

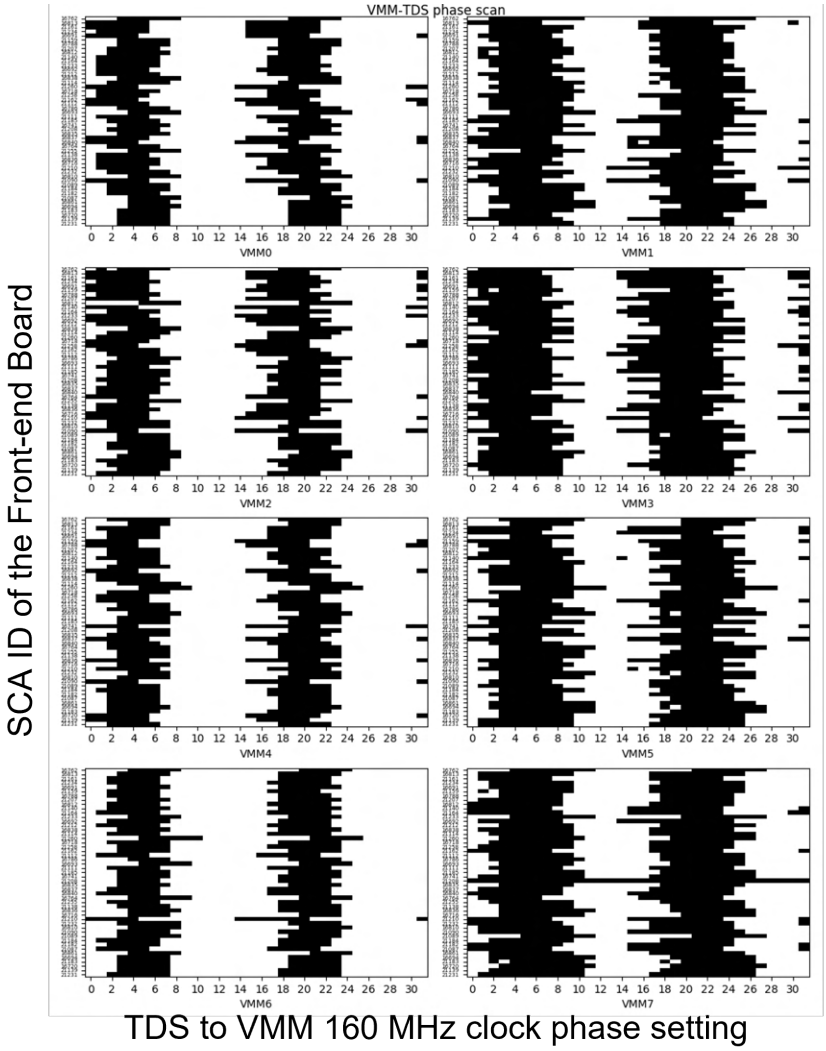


Figure 6.7: Working TDS-VMM clock phases (presented by the white areas) for the first batch of 48 sFEBs. The eight sub-figures are the results of 8 VMMs from the same sFEB. The x-axis is the TDS-VMM 160 MHz clock phase, and the y-axis is the SCA ID of each FEB.

6.2.2.3 On-bench sFEB Trigger Chain Automatic Test Flow

The mini-DAQ software was developed to cope with these test tasks offered with the mini-DAQ firmware. Table 6.1 lists the functions that the software can provide for the sFEB. All functions can be selected as parts of the automatic test flow. Five of the functions are chosen for the sFEB on-bench automatic test flow, and they are:

- Check PRBS Error;
- Check Stripe Idle;
- Check Strip Trigger;

- TDS-VMM Clock Phase Scan;
- Strip 6-bit ADC Linearity Scan.

Those functions check the TDS link, the correctness of TDS trigger receiving, and the VMM 6-bit ADC linearity.

Function Name	Description
Check PRBS Error	Check the error count of the PRBS stream.
Check Stripe Idle	Check if the strip data are the idle packets.
Check Strip Trigger	Check if the strip TDS can receive and decode trigger signals correctly.
TDS-VMM Clock Phase Scan	Scan the TDS-VMM clock phase and find a working phase for correct TDS 6-bit ADC sampling.
ROC-TDS Clock Phase Scan	Scan the ROC-TDS clock phase and list all good phases that TDS can decode the trigger signals correctly.
Strip 6-bit ADC Linearity Scan	Read the 6-bit ADC value for all TDS 128 channels.
Inquiry 6-bit ADC BCID	Inquiry the BCIDs that contain 6-bit ADC value.

Table 6.1: The Test functions available for the sFEB in the mini-DAQ software.

Figure 6.8 shows the sFEB automatic test flow. The first few steps are the same as what we have in the pFEB test flow. Start with scanning the QR code and matching the SCA ID through FELIX inquiry, and followed by the PRBS error check. Those two steps ensure the software records the SCA ID correctly, the FEB can be configured successfully, and the TDS to mini-DAQ link is built.

Next, the software configures the TDS to the normal working mode and checks if the output data from the TDS are idle packets. This ensures the TDS is configured successfully. After that, the software uses the Strip TDS Trigger Receiving Check task to confirm if the strip TDS can receive the trigger signal correctly.

As mentioned in Section 6.2.2.2, each FEB has different working VMM-TDS clock phases. Accordingly, the software uses the TDS-VMM Clock Phase Scan function to find a proper phase. The VMM-TDS clock has 32 possible phases, however, only half of the phases (from phase 5 to phase 20) is scanned to save time. By selecting such a range, working phases will be sandwiched by two bad phase areas. The software will choose the median value of the good phases as a sweet point for later use. Figure 6.9 presents one example of the phase scan result. The eight sub-figures are the results for 8 VMMs on the sFEB. The red dots are the sweet points.

Finally, the software scans the strip 6-bit ADC linearity. The VMM TP amplitude is controlled by the TP DAC setting value. The value can range from 0 to 1,023. The mini-DAQ software configures the VMM TP DAC setting from 200 to 1,000 with a step size of 100. In the meantime,

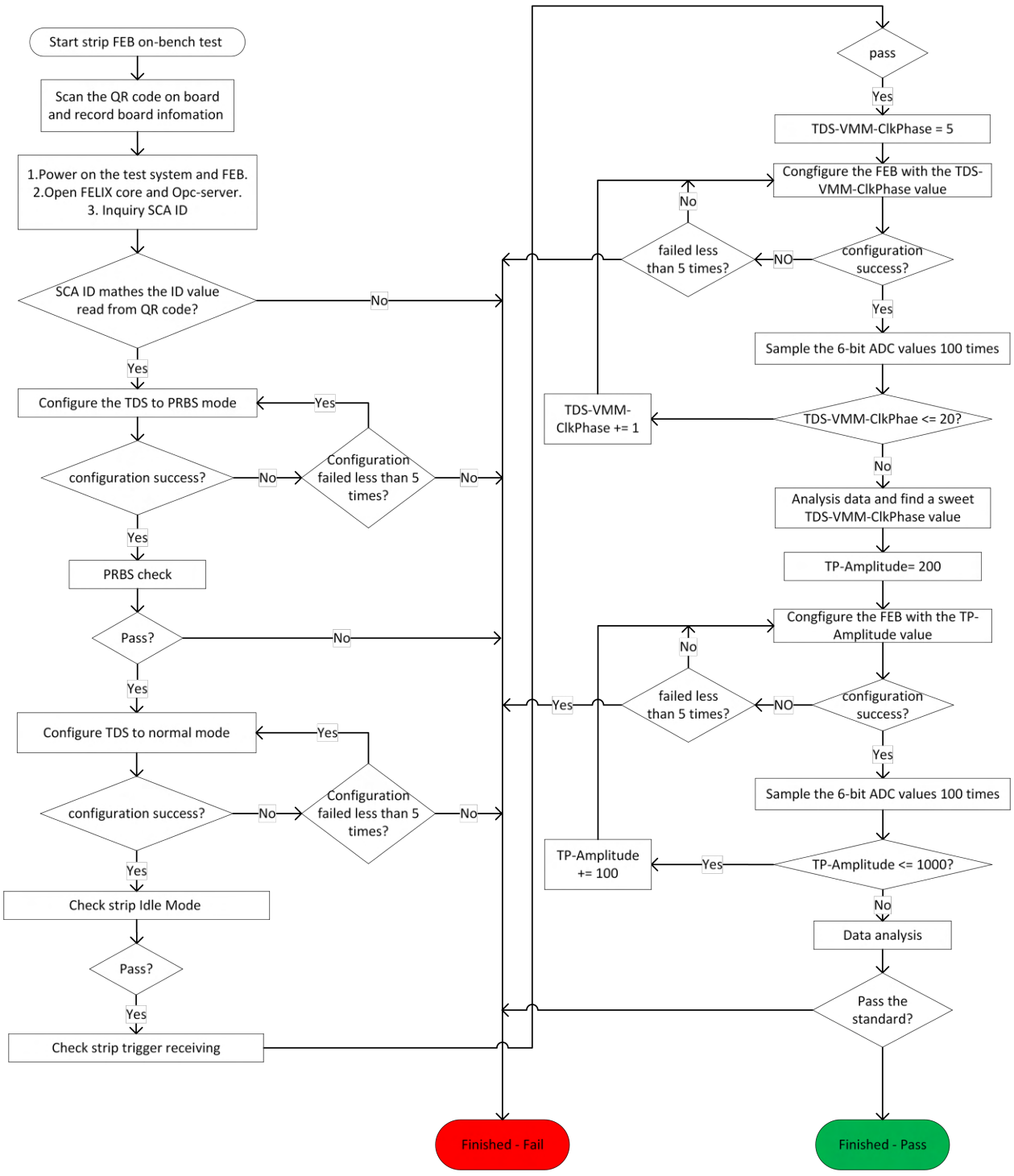


Figure 6.8: sFEB on-bench automatic test flow.

it reads the 6-bit ADC value from the TDS. Figure 6.10 presents one example of this 6-bit ADC linearity scan.

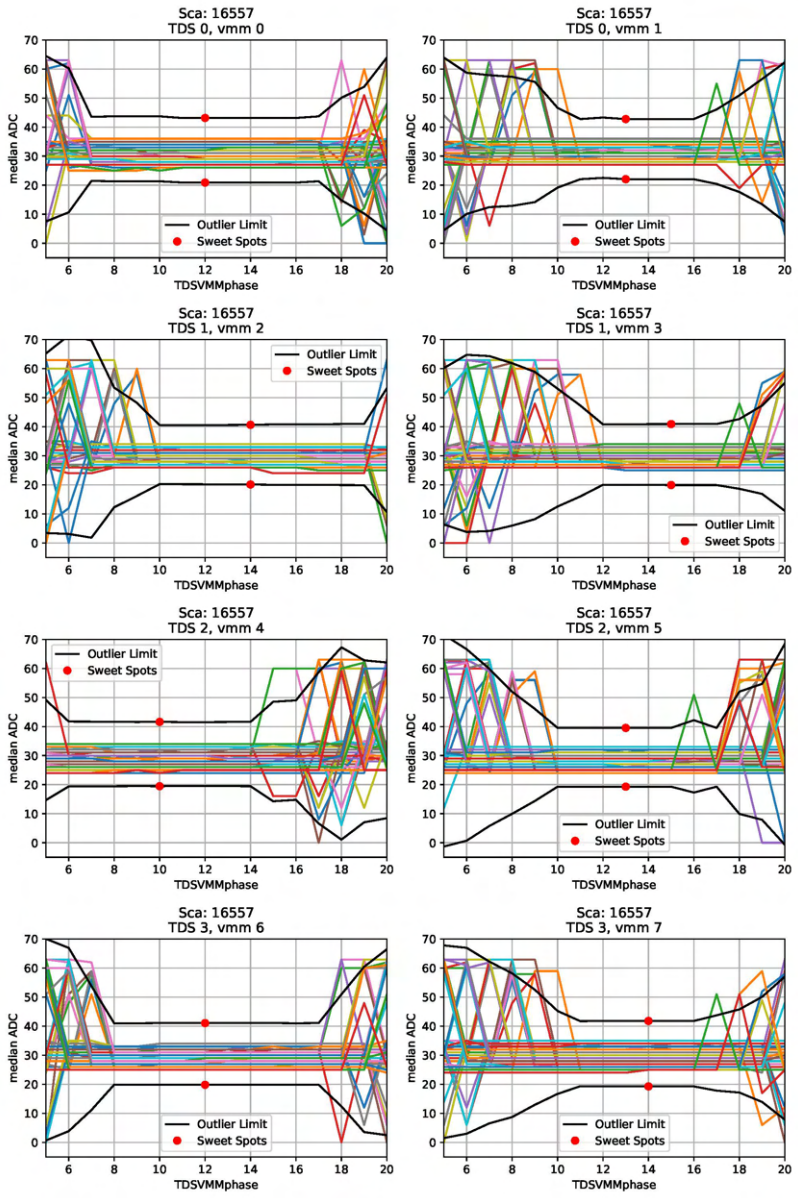


Figure 6.9: TDS-VMM clock phase scan results. The eight sub-figures are the results for 8 VMMs on the sFEB. Each color line presents one VMM channel (64 channels per VMM). The red dots are the sweet points.

Using the 6-bit ADC linearity scan result, the software summarizes dead channels and outlier channels. Dead channels are defined as channels with zero 6-bit ADC value all time. Figure 6.11 shows a dead channel example. The two outlier channels are defined using a linear relationship with the median value and the standard deviation of the measured 6-bit ADC data, as shown in the following equation:

$$\text{Outlier} = a \times \text{Median\_Value} + b \times \text{Standard\_Deviation} + c$$

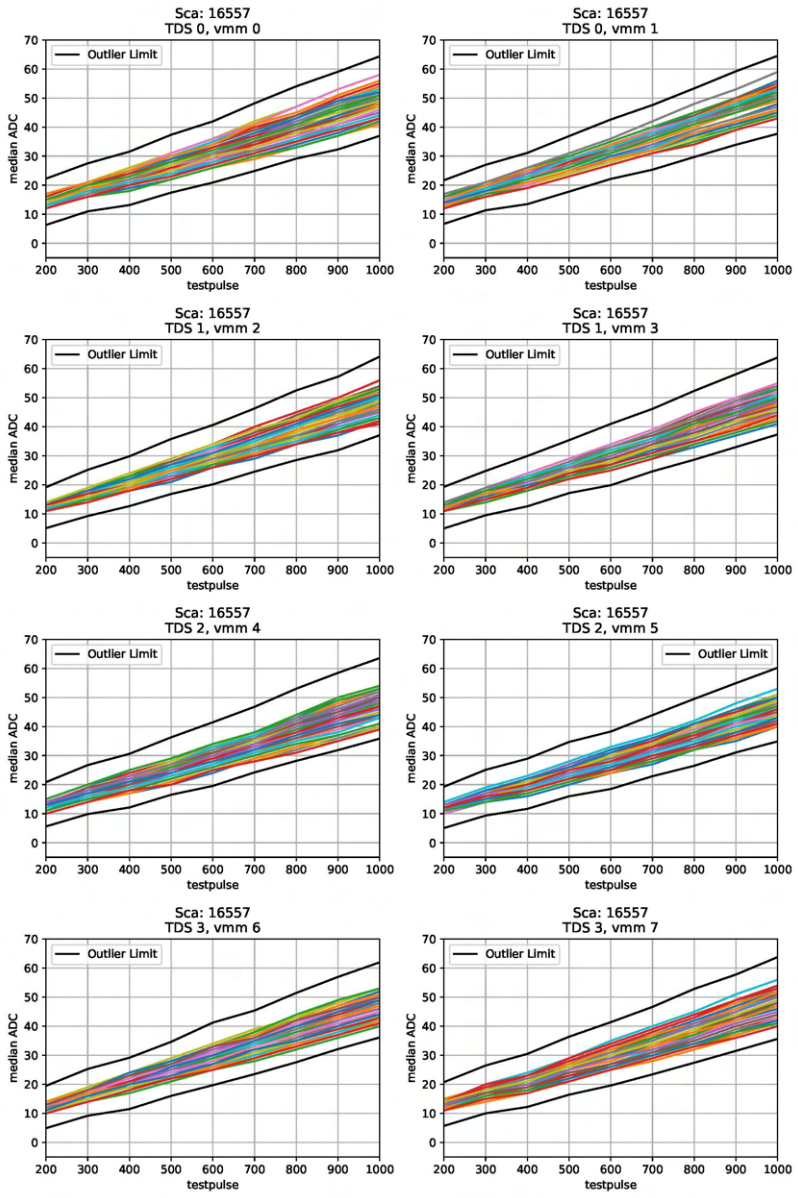


Figure 6.10: sFEB 6-bit ADC linearity scan. The eight sub-figures are the results for 8 VMMs on the sFEB. Each color line presents one VMM channel(64 channels per VMM).

When we had the first batch sFEBs, we manually tuned these parameters. The next two equations are used to define the Upper bound and the Lower bound:

$$\text{Upper\_outlier} = 1.4 \times \text{Median\_Value} + 2 \times \text{Standard\_Deviation} + 5$$

$$\text{Lower\_outlier} = 0.95 \times \text{Median\_Value} + 1.5 \times \text{Standard\_Deviation} - 5$$

The channel is marked as an outlier if its linearity scan line exceeds the upper or lower bounds, as the example presented in Figure 6.12.

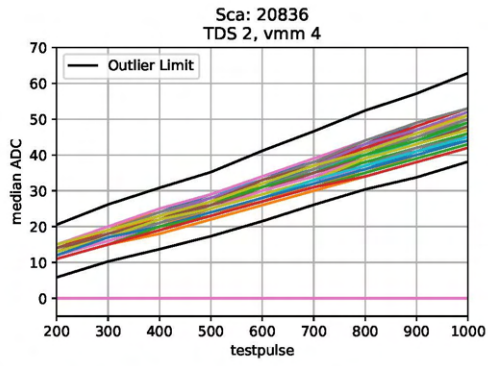


Figure 6.11: Dead channel example in the 6-bit ADC linearity scan. Each color line presents one VMM channel. The pink line shows the dead channel.

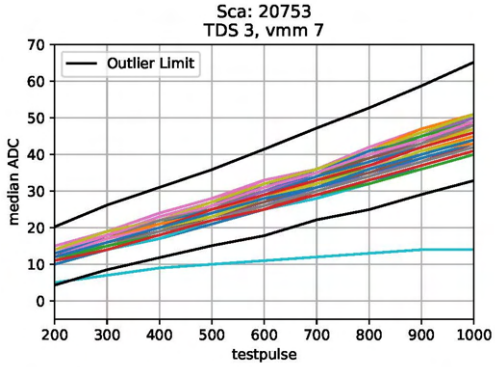


Figure 6.12: Outlier channel example in the 6-bit ADC linearity scan. Each color line presents one VMM channel. The blue line shows the outlier channel.

6.3 On-wedge Trigger Chain Connectivity Test

Once the FEBs are mounted on the sTGC wedge and the Twinax cables are installed, it is essential to verify the connectivity. This section describes the tests performed to confirm the on-wedge trigger chain connectivity.

Figure 6.13 presents the on-wedge trigger chain front-end electronics connections. There are three connections (marked with a number in the figure) that need to be verified. They are pFEB to Pad Trigger board, Pad Trigger board to sFEB, and sFEB to Router. Moreover, due to the long connection length (larger than 5 m), some connections are broken into two lines connected by a repeater to enhance the signal. The pFEB to Pad Trigger board and the sFEB to Router connections have a serial repeater for the 4.8 Gbps signal. The Pad Trigger board to sFEB has an LVD6R (“LVD” shorts for LVDS. “6” means it has six repeaters on the board. “R” presents repeater) board for the 320 MHz DDR signals. This connectivity test also verifies the functionality of repeaters.

Figure 6.14 presents the setup for the on-wedge trigger chain connectivity test. Once the wedge finishes electronics integration, it will be connected to a FELIX test station inside the CERN Building 180. A cooling pump provides cold water flow to the wedge cooling pipes. A trigger chain test cart with the mini-DAQ system, the Router board, and the Pad Trigger board are used to test the trigger interface. Detailed test procedures are discussed in the rest of the section.

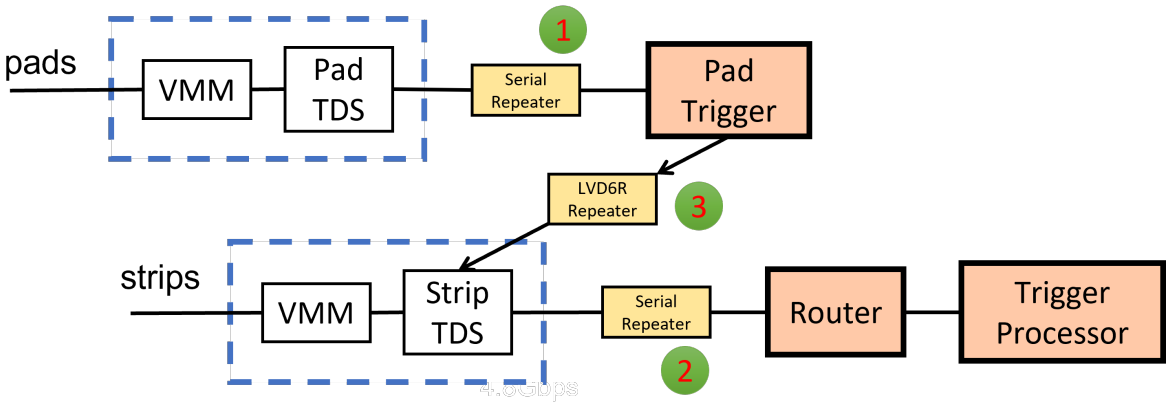


Figure 6.13: On-wedge trigger chain front-end electronics connections

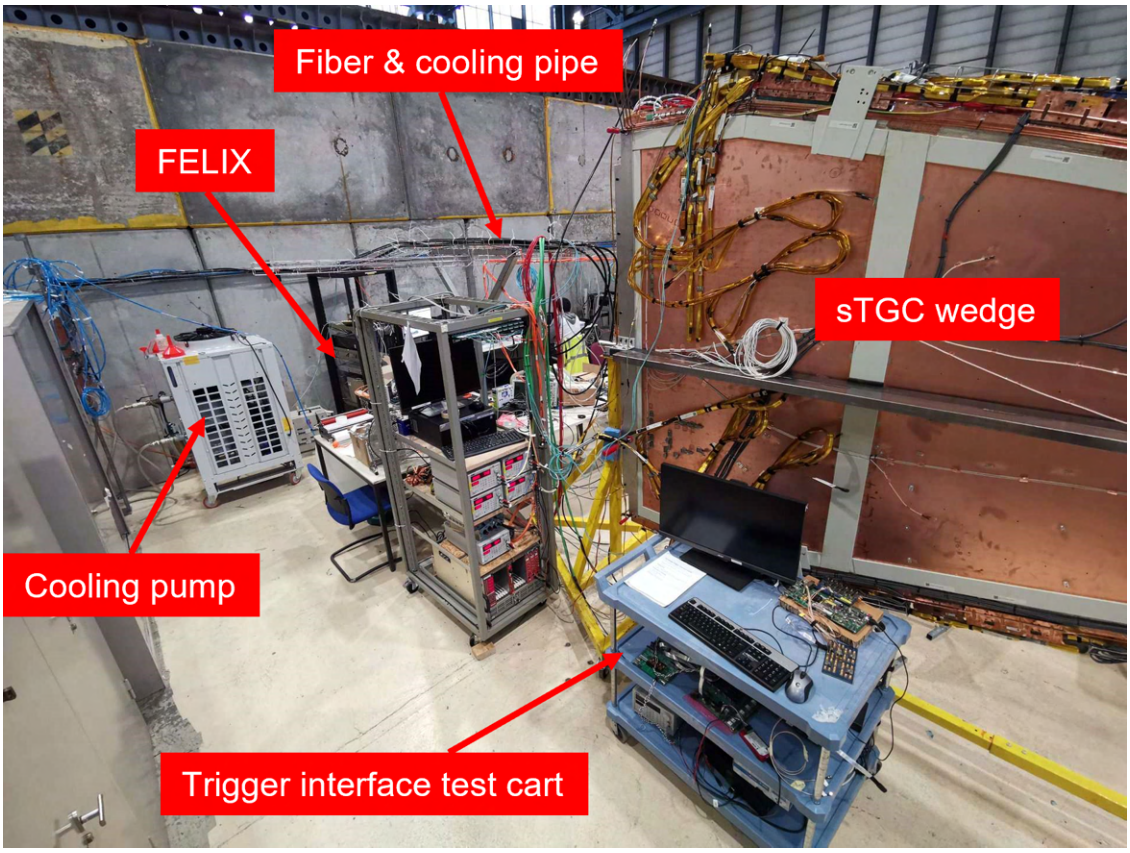


Figure 6.14: The on-wedge trigger chain connectivity test setup.

6.3.1 pFEB to Pad trigger board

A pad trigger board is used as a receiver to verify the pFEB 4.8 Gbps TDS link. The most efficient way is to check the PRBS error rate of the TDS link. Figure 6.15 presents the connection scheme.

The customizable Xilinx Integrated Bit Error Ratio Tester (IBERT) core is used on the Pad

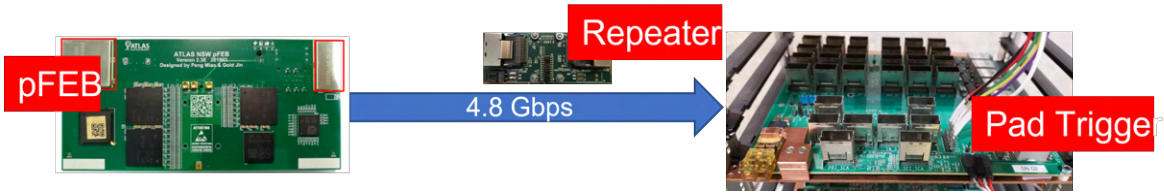


Figure 6.15: On-wedge connection for pFEB to Pad Trigger board.

	A	B	C	D	E	F
1	Name	RX	Bits	Errors	BER	RX Pattern
2	Ungrouped Links (					
3	Link Group 0 (12)					PRBS 31-bit
4	Link 0	MGT_X0Y0/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
5	Link 1	MGT_X0Y1/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
6	Link 2	MGT_X0Y2/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
7	Link 3	MGT_X0Y3/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
8	Link 4	MGT_X0Y4/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
9	Link 5	MGT_X0Y5/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
10	Link 6	MGT_X0Y6/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
11	Link 7	MGT_X0Y7/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
12	Link 8	MGT_X0Y8/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
13	Link 9	MGT_X0Y9/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
14	Link 10	MGT_X0Y10/RX	1.91E+12	0	5.23E-13	PRBS 31-bit
15	Link 11	MGT_X0Y11/RX	1.91E+12	0	5.22E-13	PRBS 31-bit

12 pFEBs

Figure 6.16: On-wedge pFEB PRBS error rate results.Link 0 to link 11 are 12 pFEB links and it shows zero error during the time of test. The BERs are also recorded.

Trigger board to check the error rate of the TDS PRBS data stream. One Pad Trigger board can handle 24 pFEBs at the same time, and thus all 12 pFEBs from a wedge are tested simultaneously. The results are saved in an excel file as shown in Figure 6.16. Link 0 to link 11 are the 12 pFEB links. The standard used in this test is the Bit Error Rate (BER) should be less than 10^{-12}.

6.3.2 sFEB to Router board

In this test, the Router board is used to check the error rate of the sFEB PRBS output. Again, the IBERT IP core from Xilinx is utilized on the Router board. The connection is shown in Figure 6.17. The Router board receives 3 or 4 TDS PRBS data links from one sFEB. The Q1 quadruplet is equipped with an sFEB8, which has 4 TDS ASICs. The Q2 and Q3 quadruplets are equipped with an sFEB6, which has 3 TDS ASICs.

Figure 6.16 shows the saved results for the three sFEBs, one sFEB8 and two sFEB6 boards from the same layer. The test uses the same standard for the TDS on pFEB (BER should be less

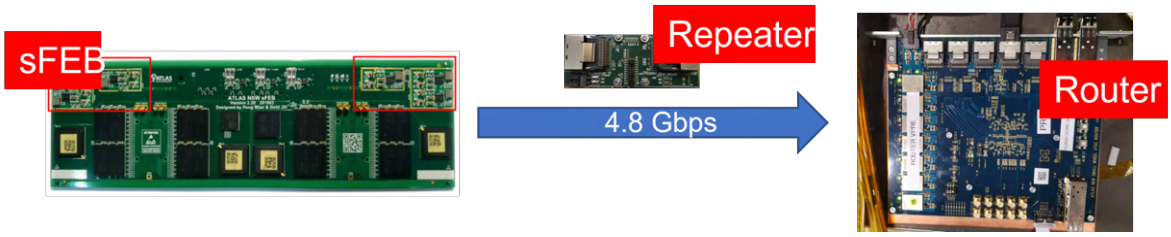


Figure 6.17: On-wedge connection for sFEB to Router board

	A	B	C	D	E	F
1	Name	RX	Bits	Errors	BER	RX Pattern
2	Ungrouped Links (					
3	Link Group 0 (16)					PRBS 31-bit
4	Link 0	MGT_X0Y0/RX	1.33E+12	-442843986	4.97E-01	PRBS 31-bit
5	Link 1	MGT_X0Y1/RX	1.34E+12	-248690179	4.77E-01	PRBS 31-bit
6	Link 2	MGT_X0Y2/RX	1.34E+12	-1082793419	5.82E-01	PRBS 31-bit
7	Link 3	MGT_X0Y3/RX	1.33E+12	2146525694	5.02E-01	sFEB8
8	Link 4	MGT_X0Y4/RX	1.34E+12	0	7.48E-13	PRBS 31-bit
9	Link 5	MGT_X0Y5/RX	1.34E+12	0	7.48E-13	PRBS 31-bit
10	Link 6	MGT_X0Y6/RX	1.34E+12	0	7.48E-13	PRBS 31-bit
11	Link 7	MGT_X0Y7/RX	1.34E+12	0	7.48E-13	PRBS 31-bit
12	Link 8	MGT_X1Y0/RX	1.34E+12	0	7.48E-13	sFEB6
13	Link 9	MGT_X1Y1/RX	1.34E+12	0	7.48E-13	PRBS 31-bit
14	Link 10	MGT_X1Y2/RX	1.33E+12	0	7.51E-13	PRBS 31-bit
15	Link 11	MGT_X1Y3/RX	1.33E+12	713785291	6.39E-01	sFEB6
16	Link 12	MGT_X1Y4/RX	1.33E+12	0	7.51E-13	PRBS 31-bit
17	Link 13	MGT_X1Y5/RX	1.33E+12	0	7.51E-13	PRBS 31-bit
18	Link 14	MGT_X1Y6/RX	1.33E+12	0	7.51E-13	PRBS 31-bit
19	Link 15	MGT_X1Y7/RX	1.33E+12	857459328	5.81E-01	PRBS 31-bit
20						

Figure 6.18: On-wedge sFEB PRBS error test results. There are one sFEB8 and two sFEB6 from the same layer of the sTGC quadruplet.

than 10^{-12}). Four such tests are needed for the 12 sFEBs from all 4 layers.

6.3.3 Pad Trigger Board to sFEB

In this test, the trigger interface of the sFEB will be tested. Ideally, the Pad Trigger board should send pre-L1 trigger signals to the sFEB, and the Router board should check the trigger data. However, people working on the Pad Trigger board and the Router board did not offer us such special firmware. As a result, the mini-DAQ system is used to substitute the two boards.

Like the on-bench sFEB trigger chain test, the mini-DAQ system is in charge of sending trigger signals to the sFEB and receiving the TDS data. The test uses the automatic test flow developed for

the on-bench sFEB trigger chain test (presented in Section 6.2.2.3). Only two functions are used and they are:

- Check PRBS Error;
- Check Strip Trigger.

The Check PRBS Error function ensures that the link from sFEB to mini-DAQ is secured. The Check Strip Trigger function verifies the sFEB trigger interface. Figure 6.20 shows an example of the report.

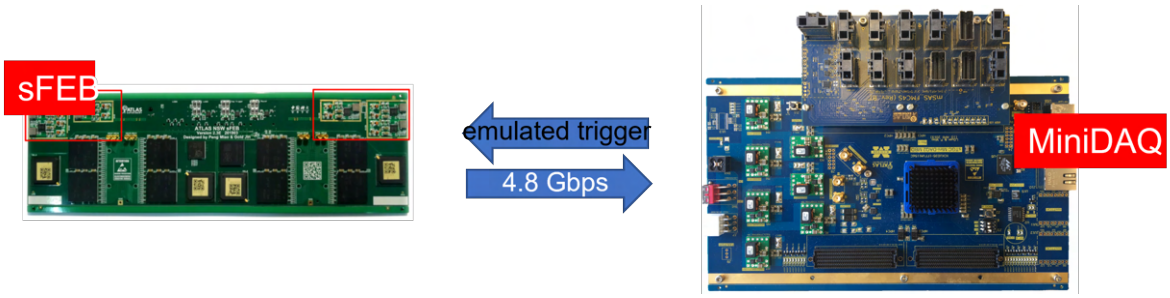


Figure 6.19: On-wedge connection for sFEB trigger receiving test.

6.3.4 Cosmic ray hit map with the CO_2 gas

If time allows, we flush the detector with the CO_2 gas for an additional cosmic ray hit map test on sTGC pads using the mini-DAQ Active Data Readout module (described in Section 5.4). We did not use the working gas due to safety considerations since the working gas has n-pentane and is flammable.

When the HV is applied, the detector will respond to cosmic ray muons. Even though the CO_2 gas is not efficient to detect charged particles, it is good enough for us to look at the hit map and search for dead and high resistance channels.

Figure 6.21 shows an example of the hit map of Layer 3 from the QS3C quadruplet. The measurement was taken in 30 minutes with a threshold setting of 50 mV and 2,800 V HV. There are two channels on the right bottom corner that receive zero hits during the entire measurement. Those two channels are marked as dead channels in the report.

6.4 Result Summary

The sTGC is the primary trigger detector for the NSW detector. Verifying the functionality and connectivity of the trigger chain front-end electronics is absolutely necessary to ensure the opera-

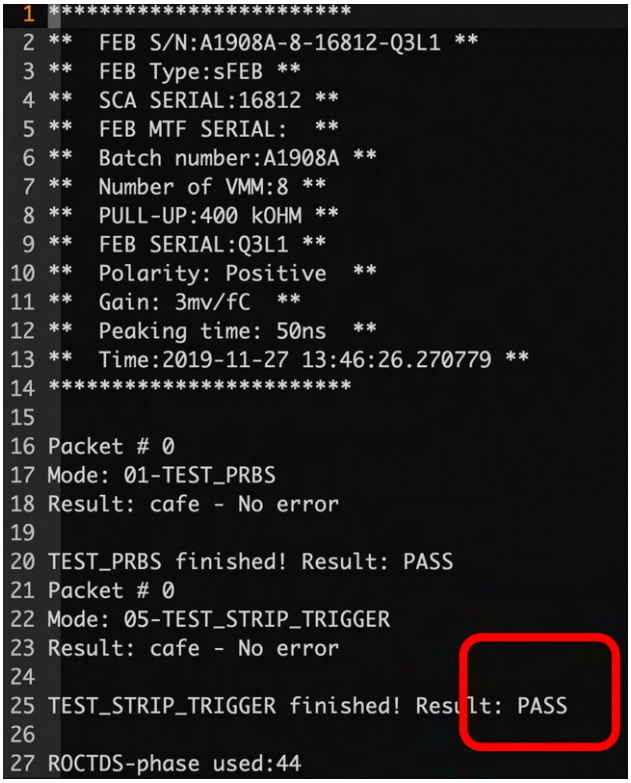


Figure 6.20: On-wedge stip FEB trigger test results log. The test contains PRBS error rate check and the strip trigger receiving test.

tion of the NSW detector for Run-3 and HL-LHC. The mini-DAQ system I developed played an irreplaceable role in the integration and commissioning work during the LS2 at CERN. Our group has successfully integrated and commissioned all 64 sTGC wedges.

Here is the summary for the on-bench trigger chain reception test. We received in total 850 pFEBs and 850 sFEBs (768 pFEBs and 768 sFEBs are needed). In the trigger chain, 3 pFEBs and 17 sFEBs have a major failure, and they are directly rejected for further repair work. The common failure issues are:

- Short circuit;
- On-board SCA does not respond;
- Some ASICs cannot be configured;
- One VMM does not give direct output;
- TDS cannot decode triggers correctly;
- Unstable connections.

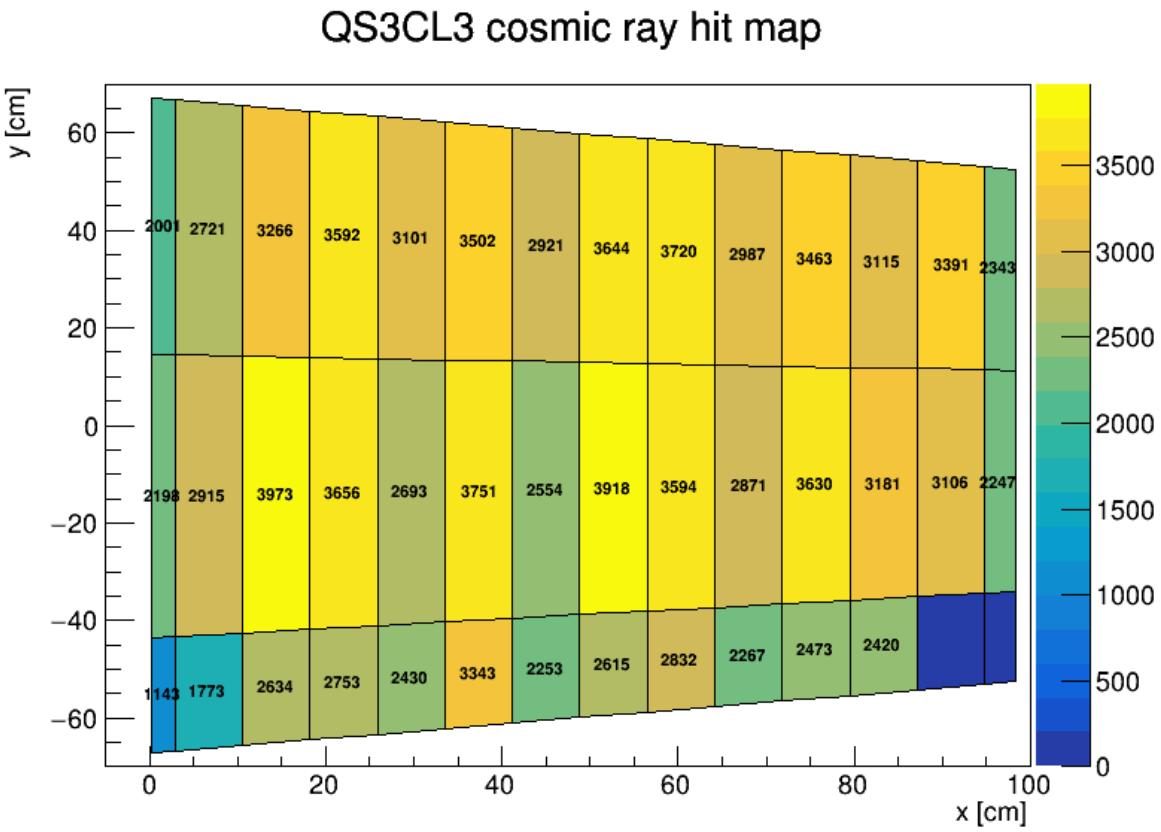


Figure 6.21: Cosmic ray hit map of Layer 3 of the Q3C measured for 30 minutes with a 50 mV threshold setting and 2800 V HV. The two channels at the right bottom corner are dead.

Those failure boards would be a killer if installed in the sTGC detector as one FEB is in charge of an entire sTGC quadruplet layer. The rest 847 pFEBs and 833 sFEBs are functional. Figure 6.22 shows the dead channel summary of all pFEBs. Figure 6.23 and Figure 6.24 show a summary of outlier channels and dead channels for all sFEBs.

Among all 847 functional pFEBs, 830 have zero dead channels and 17 have only one dead channel. For all 833 functional sFEBs, 653 of them have zero outlier channels and 646 have zero dead channels. The dead and outlier channels are registered in the ATLAS database as a reference for operational use. Whether a FEB is accepted depends on both the trigger chain result and readout chain result. It turned out that the readout chain is the bottleneck. We managed to equip all sTGC detectors.

In the on-wedge trigger chain connectivity test, all the trigger chain links have been confirmed. We would fix a link problem before delivering if there were a problem. We did find a handful of unstable cable installation and mis-routing cables, and fixed these problems.

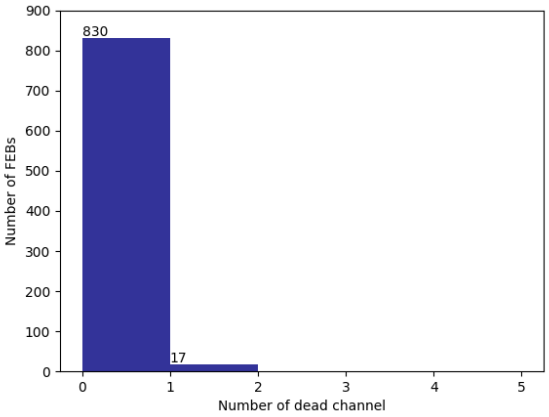


Figure 6.22: Dead channel summary of all 847 functional pFEBs. 830 of them have zero dead channels and 17 of them have one dead channel.

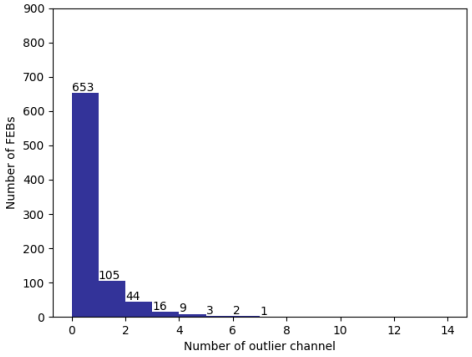


Figure 6.23: Outlier channel summary of all 833 functional sFEBs. 653 of them have zero outlier channels.

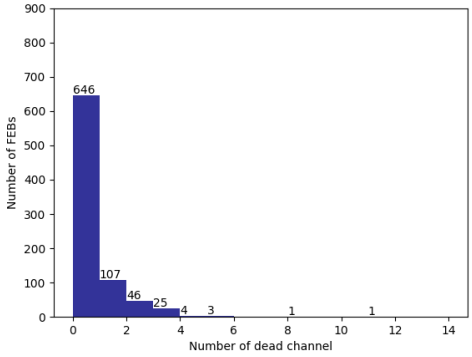


Figure 6.24: Dead channel summary of all 833 functional sFEBs. 646 of them have zero dead channels.

CHAPTER 7

The Phase-I Upgrade: sTGC Cosmic Ray Study

The primary cosmic rays, mostly composed of high-energy protons, originate from outer space. They enter the atmosphere and interact with the air generating secondary particles, mostly pions and some kaons. The charged pions then decay to muons and neutrinos through the weak interaction. Muons have a rest frame lifetime of about 2.2 μs, and most of them can penetrate the atmosphere and reach the ground due to relativistic time dilation and the fact that cosmic muon is the Minimum Ionizing Particle (MIP) (with an average energy loss close to the minimum). Muons at the sea level are the dominant component of cosmic rays, and they have an average energy of 4 GeV [104].

At the sea level, the flux of the muon is approximately followed by

$$I(\theta) = I_0 \cos^2\theta, \tag{7.1}$$

where θ is the zenith angle in the spherical coordinate. I_0 is the flux at $\theta = 0$ and is about 70 $m^{-2}sr^{-1}s^{-1}$ [105].

In this chapter, I present the sTGC performance study with cosmic rays (mostly cosmic muons). We started to look at the cosmic muon signals from the VMM MO analog output and then checked the trigger chain data.

A Monte Carlo (MC) simulation was also carried out for a better understanding of the data taken. The MC simulation uses Eq. 7.1 as the basis for sampling. Furthermore, the flux $I(\theta)$ can be written as

$$I(\theta) = \frac{dN(\theta)}{(d\vec{A}\cdot d\vec{\mathbf{n}})d\Omega dt}$$

where Ω is the solid angle and $d\Omega = \sin\theta d\theta d\phi$. The $d\vec{A}\cdot d\vec{\mathbf{n}}$ is the projected area element which is $\cos\theta dA$. Bringing all of them back to Eq. 7.1 gives

$$\frac{dN(\theta,\phi)}{\cos\theta dA \sin\theta d\theta d\phi dt} = I_0 \cos^2\theta$$

.

Rearrange the above equation and we have

$$\frac{dN(\theta,\phi)}{dAdt} = I_0 \sin\theta \cos^3\theta d\theta d\phi. \tag{7.2}$$

Eq. 7.2 is the probability distribution function that our MC simulation used for sampling cosmic muon (θ, ϕ) angles.

7.1 Setup

Figure 7.1 presents the experimental setup for the sTGC cosmic ray study. We used a production confirm wedge that was rejected due to bad quality of the QS1 quadruplet. However, QS2 and QS3 can still be used for our cosmic ray study. The two quadruplets were equipped with production FEBs and L1DDC. A FELIX station was used to configure all FEBs and to deliver clock and TTC signals.

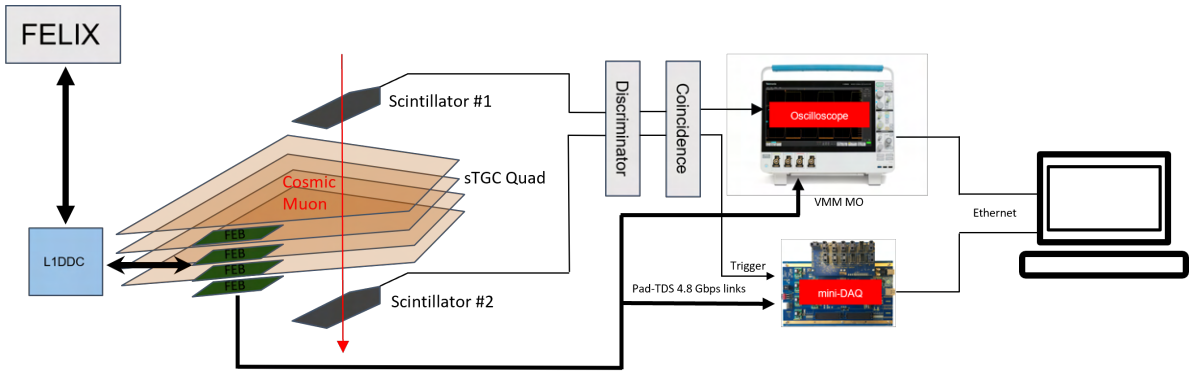


Figure 7.1: Block diagram of the test setup for the sTGC cosmic ray study.

The measurement took place in the CERN Building 180 gas room. The wedge was flushed with the working gas mixture - 45% of n-pentane and 55% of CO_2. Figure 7.2 is a photograph of the experimental setup.

The external triggers were provided by scintillators with Nuclear Instrumentation Module (NIM) devices. Two trigger schemes were used and will be introduced later in this section. Two types of data were collected in two different data paths. The first one is the analog signals output by the VMM MO. Analog signals provide first-hand signal information before they are fed into the VMM's discriminator/ADC. An oscilloscope with a bandwidth of 350 MHz and a sampling rate of 6.25 GS/s is used to measure and record analog signals. The second data path is the sTGC trigger chain. The mini-DAQ system was used with the Active Data Readout (mentioned in Section 5.4) to read out the TDS output data.

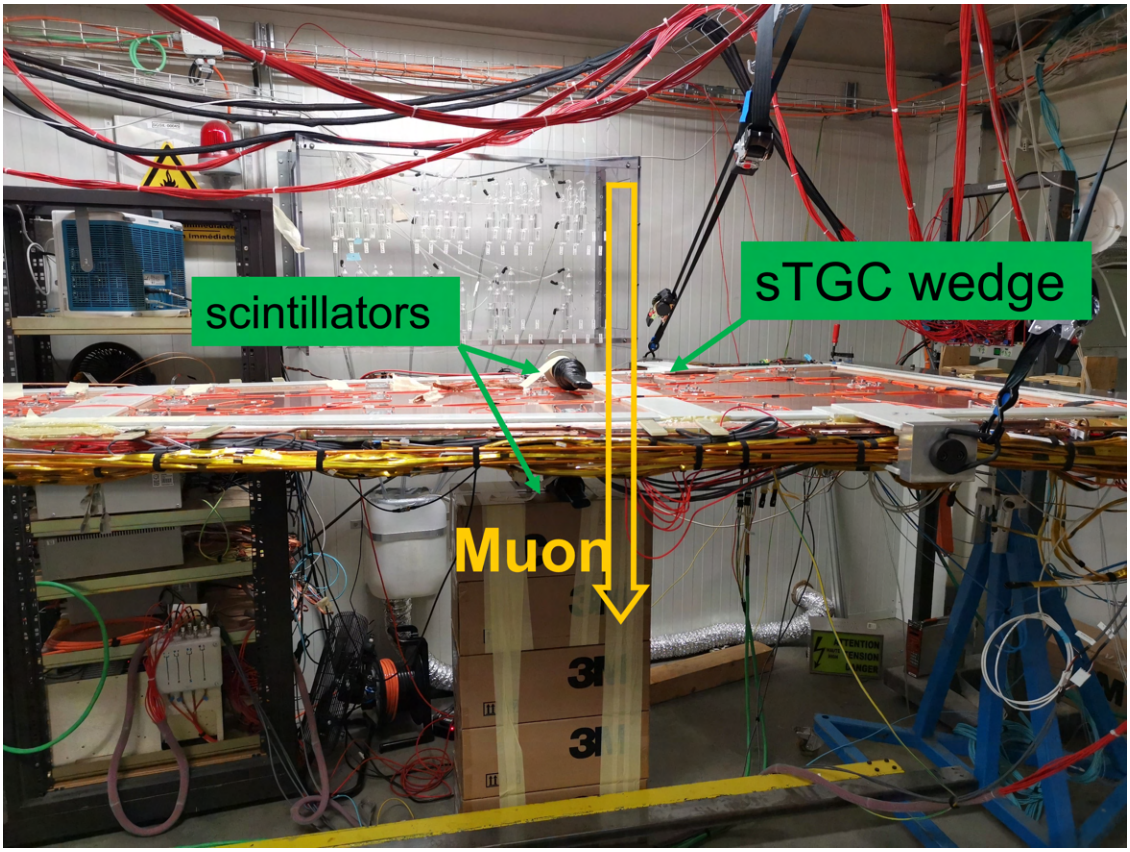


Figure 7.2: A photograph of the test setup in the CERN Building 180 gas room.

7.1.1 Horizontal Trigger Scheme

The horizontal trigger scheme is used when the wedge is fixed in a horizontal position, as presented in Figure 7.1. This is the main trigger scheme used for the cosmic ray study. Two small scintillators, one placed above the detector and the other placed underneath, are used to generate external trigger signals. Both scintillators have the same dimension, 1.5 inches $\times$ 6 inches (or 3.81 cm $\times$ 15.24 cm), and are separated by 30 cm. Their size is smaller than a nominal sTGC pad so that it can be used to control which sTGC pad cosmic muons pass through.

The MC simulation is used to find the muon angular distribution under this scheme. Figure 7.3 shows the simulated angular distribution. From the simulation result, 90% of muons have an incident angle from 1° to 18°, and the mean value is 9.4 °. Therefore, in this trigger scheme, we trigger on muons with small incident angles. The average trigger rate is around 0.05 Hz. Limited by this rate, we could only select a few representative pads for study.

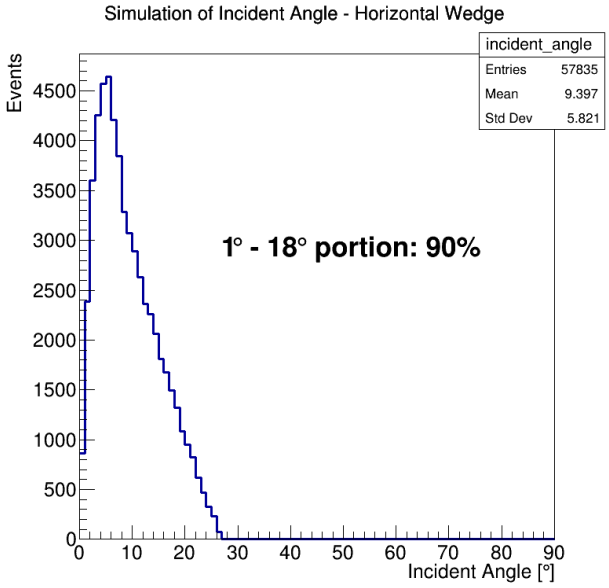


Figure 7.3: Simulated muon angular distribution in the horizontal trigger scheme. 90% of muons triggered have an incident angle from 1° to 18°, and the mean value is 9.4 °.

7.1.2 Vertical Trigger Scheme

Another trigger scheme is used when the sTGC wedge is in a vertical position. Figure 7.4 presents a simplified diagram of this scheme. A large scintillator, sized by 68 cm × 200 cm, is located beside the sTGC detector to provide an external reference. The trigger signal is the coincidence of signals from the scintillator and two sTGC pads in the other two layers.

Due to the geometrical acceptance, the pad we plan to study is not guaranteed to be hit in every triggered event. We only used this scheme to measure the charge distribution. When there was not enough room to set the wedge in the horizontal position, this trigger scheme was also used for debugging and preparation work.

Figure 7.5 shows the angular distribution from the MC simulation. 90% of muons have an incident angle range from $43° - 71°$, and the mean value is 55.5°. So in this trigger scheme, triggered muons have a larger incident angle.

7.2 sTGC Pad Performance

In this section, the sTGC pad performance was measured by looking at the analog signals using the VMM MO.

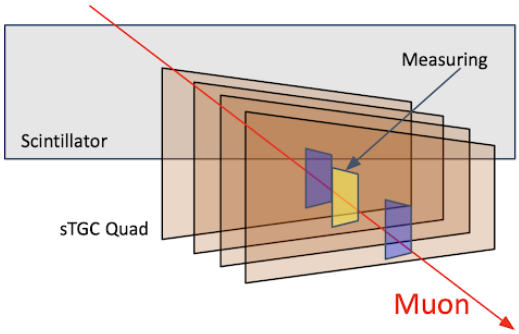


Figure 7.4: Simplified diagram for the vertical trigger scheme. The trigger is the coincidence of the scintillator and two sTGC pads from the other two layers.

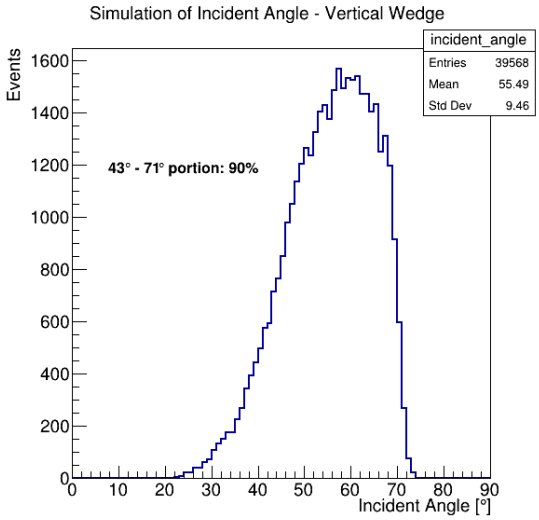


Figure 7.5: Simulated muon angular distribution in the vertical trigger scheme. 90% of the muons have an incident angle from 43° to 71°, and the mean value is 55.5 °.

7.2.1 Data collection

The signals from scintillators and the VMM MO are connected to the oscilloscope. Figure 7.6 presents an example event captured by the oscilloscope in the horizontal trigger scheme. The trigger is the signal coincidence of the two scintillators. The yellow line and the green line are the analog signals from the VMM MO. The oscilloscope saves the waveform of the analog signals with a sampling step of 800 ps.

Figure 7.7 shows the collected signals from one run. The signals are split into three main categories: ringing noise, negative pulse, and candidate muon signal. The top row shows an example of each category, and the bottom row presents the accumulated waveforms.

The ringing noises come from the common ground noise. This type of noise happens when the crane of building was operating or other powerful machines were working. The offline analysis will mark those ringing signals as noises.

The negative pulses are the cross talks from other fired pads. As the charge was induced on the fired sTGC pad, it will also affect the neighbor pads and generate this negative charge pulse. During offline analysis, this type of signal will be separated into its category.

The signals left are the candidate cosmic muon signals. Since the entire waveform of each event has been saved, the amplitude of the signal and timing information can be extracted for later studies.

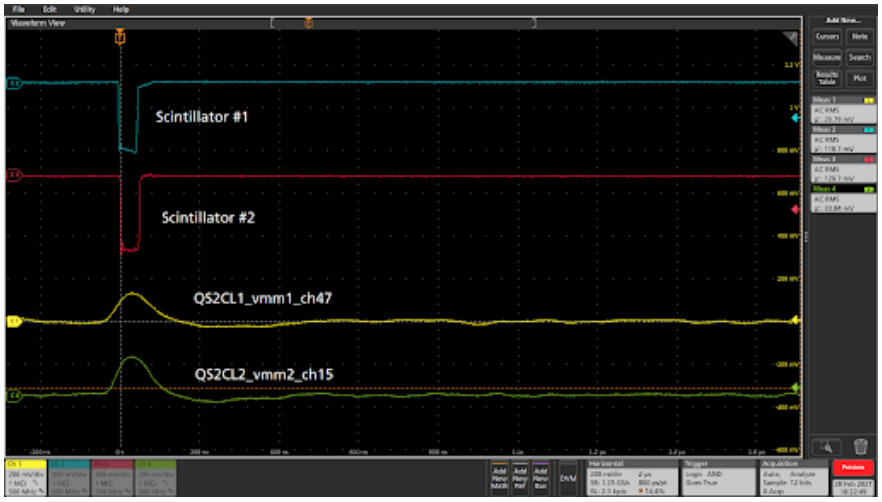


Figure 7.6: An event saved by the oscilloscope. The trigger signal is the coincidence of signals from the two scintillators. The yellow line and the green line are the analog outputs from the VMM MO.

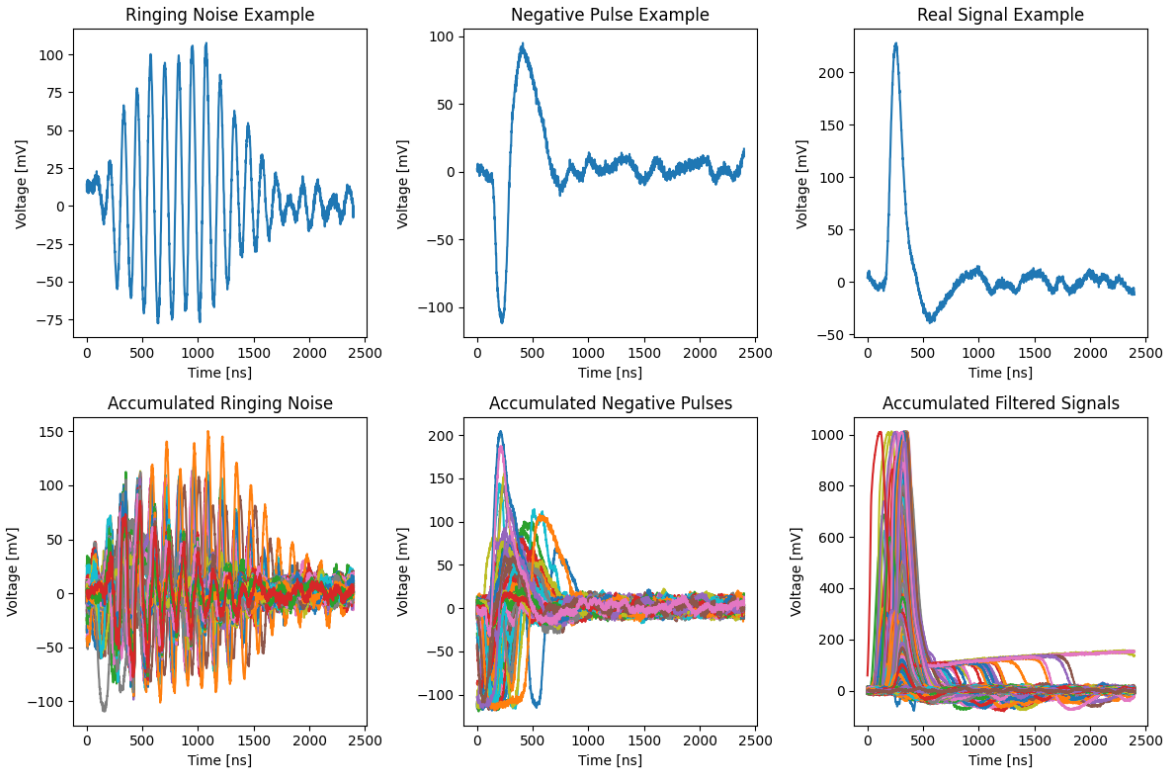


Figure 7.7: sTGC pad analog signal waveforms from the collected events. Three columns represent ringing noise, negative pulse, and candidate muon signal. The top row shows an example of each category, and the bottom row presents the accumulated waveforms.

7.2.2 Charge Distribution and Signal-to-Noise Ratio

As mentioned in Figure 4.7, a π-network was added to the pFEB to attenuate the charge with a factor of $C_\pi/(C_{pad}+C_\pi)$. The C_π values were chosen based on some preliminary studies so that we need to know how they finally perform. The study aims to find the overall signal amplitude (using the Landau distribution [106] Most Probable Value (MPV) to describe) and the SNR.

Figure 7.8 and Figure 7.9 show the charge distributions for a selected pad on layer 2 of the QS3C quadruplet under both trigger schemes. The test was carried out by measuring the distribution under different high voltages: 2,700 V, 2,800 V, and 2,900 V. A fit using a Landau distribution is applied to each measurement, and the MPVs are listed with the figure labels.

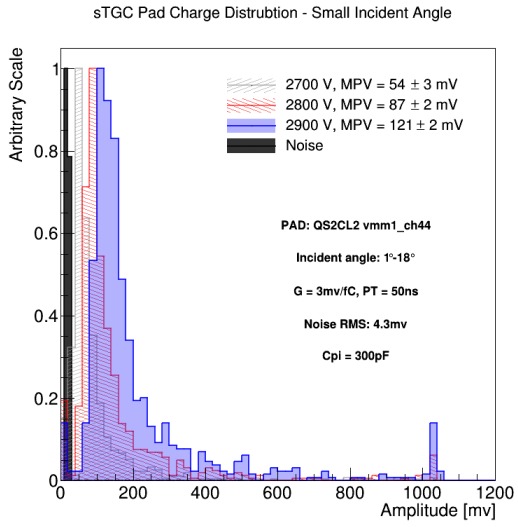


Figure 7.8: sTGC pad charge distribution in the horizontal trigger scheme. The maximum value of each distribution is normalized to one.

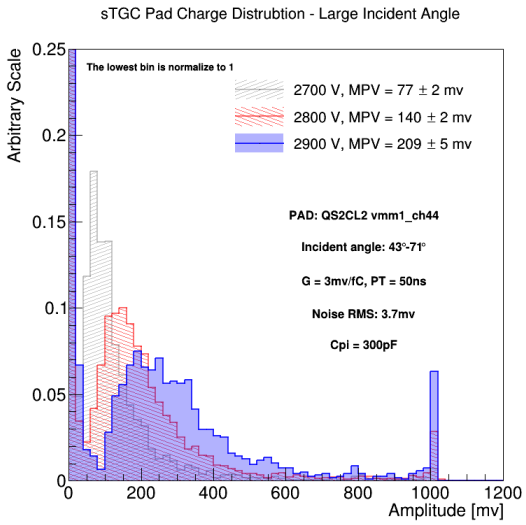


Figure 7.9: sTGC pad charge distribution in the vertical trigger scheme. Noise is normalized to one.

In Figure 7.8, the maximum value of the distribution is normalized to one. In addition to the signal distribution, the noise distribution is also plotted. In this horizontal trigger scheme, muons pass through the detector with relatively small angles, resulting in short tracks in the sTGC gas gap. Less ionization would happen and thus it leads to smaller signals (compared to the vertical trigger scheme). With a high voltage of 2,800 V, the MPV is 87±2 mV, and there is a clear separation between the noise and the signal. When the high voltage increases (before the saturation), the MPV also increases, due to the fact that there would be more electron avalanches.

In Figure 7.9, the lowest bin (noise) is normalized to one. As mentioned in Section 7.1.2, in this vertical trigger scheme, it is not guaranteed that a muon would pass the measured sTGC pad in each event. Consequently, a fixed portion (depends on the geometric acceptance) of the events

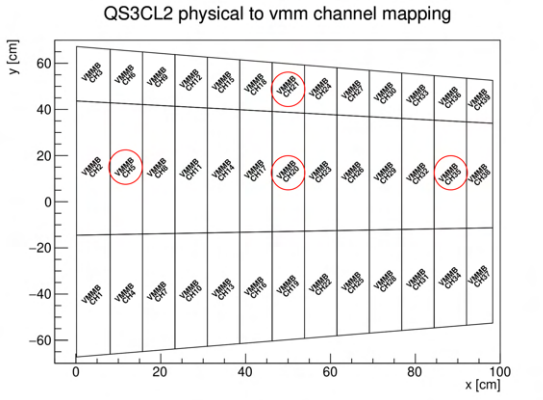


Figure 7.10: Selected sTGC pads for MPV measurements. Marked by the red circles in the mapping figure.The three pads in the middle row are chosen as nominal size pads, while a tiny pad in the top row is chosen to present the extreme case.

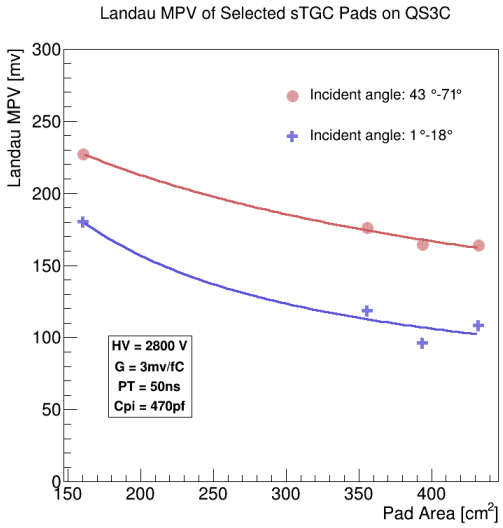


Figure 7.11: MPV of selected sTGC pads with a high voltage of 2,800 V. The red dots are the results from the vertical trigger scheme, and the blue dots are the results from the horizontal trigger scheme.

are noises. Luckily, the signals are large enough to be separated from the noise. The MPV value of the signals can be found by setting a proper Landau distribution fitting range. When the high voltage increases, the overall distribution shifts to the right with a lower and wider shape. This is due to different normalization strategies compare to Figure 7.8. With a high voltage of 2,800 V, the MPV is 140 ±2 mV.

In each measurement, the distribution has a peak around 1 V, which is caused by the saturation of the VMM amplifier. The VMM is supplied with a voltage of 1.2 V, and the baseline of the signal is usually around 170 mV.

Due to the low data rate with cosmic rays, we can only study some representative sTGC pads. Figure 7.10 shows the locations of four pads selected. The three pads in the middle row are chosen as nominal size pads, while the one in the top row represents a tiny pad. Figure 7.11 shows the MPV as a function of the pad size for these four pads. Since the sTGC pad is similar to a parallel plate capacitor, the larger the pad size is, the larger the C_{pad} is. Since the attenuation factor is $C_\pi/(C_{pad}+C_\pi)$, a larger pad will have a smaller signal. The trend observed in Figure 7.11 agrees with this prediction (The trend line is fitted by $a/(1+b\times x)+c$).

The red dots in Figure 7.11 are the results from the vertical trigger scheme (43° to 71° incident angle), and the blue dots are the results from the horizontal trigger scheme (1° to 18° incident angle). The incident angle for the sTGC at the ATLAS detector is between 10° to 30°. The foreseen MPV of those selected pads would be larger than 100 mV from the measured results.

The SNR is defined as

$$\text{SNR} = \frac{\text{MPV}}{\text{Noise RMS}}. \tag{7.3}$$

The oscilloscope measures the Noise Root-Mean-Square (RMS). Table 7.1 shows the measured noise RMS together with the area for these four pads.

Pad #	Location	Area (cm^2)	Noise RMS (mV)
1	QS3CL2_vmm1_ch21	161	4.2
2	QS3CL2_vmm1_ch35	356	5.5
3	QS3CL2_vmm1_ch20	394	4.8
4	QS3CL2_vmm1_ch5	432	5.4

Table 7.1: Noise RMS and the area for the four sTGC pads studied.

Using the MPV from Figure 7.11, the SNR results with a high voltage of 2,800 V are presented in Figure 7.12. The noise RMS of each channel is found to be close to each other and is around 5 mV. It indicates that the major factor impacting the SNR is the MPV. Based on these results, all pads are required to have an SNR larger than 20.

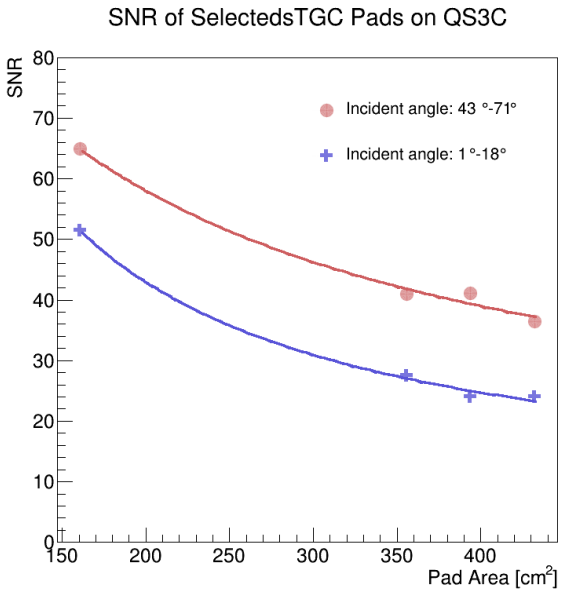


Figure 7.12: SNR of selected sTGC pads. The red dots are the results from the vertical trigger scheme, and the blue dots are the results from the horizontal trigger scheme.

7.2.3 Efficiency

The vertical trigger scheme is used in the pad efficiency measurement. The pad efficiency is defined as:

$$\text{Efficiency} = \frac{N_{\text{pad signal crosses a certain threshold}}}{N_{\text{external triggers}}} \tag{7.4}$$

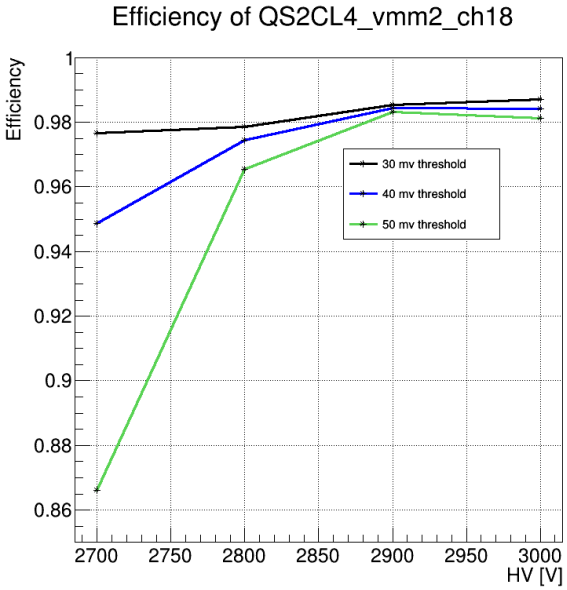


Figure 7.13: The sTGC pad efficiency for a selected pad on the QS2C quadruplet with 30 mV, 40 mV and 50 mV Threshold settings.

Figure 7.13 shows the efficiency of a selected pad on the QS2C quadruplet. The measured pad has an efficiency of 98% with a threshold of 30 mV under the high voltage of 2,800 V. When the threshold rises to 50 mV, the efficiency drops, especially for 2,700 V. To keep the efficiency higher than 90% with a threshold of 50 mV, it is recommended to set the high voltage higher than 2,800 V.

7.2.4 Timing Performance

The sTGC pad timing performance can be measured using the saved waveforms. The scintillator time is used as the reference. Figure 7.14 presents the concept for the timing measurement, where t_s is the falling edge of the scintillator trigger signal, t_{tot} is the time when the sTGC signal crosses the threshold, and t_{peak} is the time when the signal reaches its peak.

We are interested in $t_{\text{tot}} - t_s$ and $t_{\text{peak}} - t_s$ distributions. The sTGC pads will be used to provide a fast but coarse timing measurement (in 25 ns) in the trigger chain, and we are curious about their timing performance with the final front-end electronics. The study here measures the analog

signal performance, which is the signal before processed by VMM's discriminator and subsequent electronics (which could potentially degrade the timing performance). The two quantities, $t_{\text{tot}} - t_s$ and $t_{\text{peak}} - t_s$, are related to the two VMM direct output modes: ToT and PtP (mentioned in Section 4.1). The study provides a reference for the performance of those two modes.

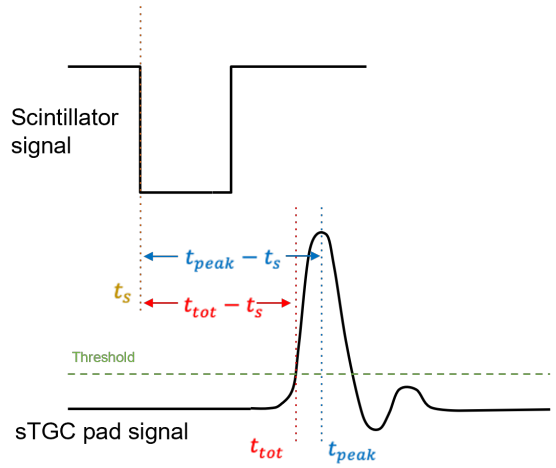


Figure 7.14: Diagram of the timing concepts in the measurement. t_s is the falling edge of the scintillator signal. t_{tot} is defined as the time when the sTGC signal crosses the threshold. t_{peak} is defined as the time when the signal reaches its peak.

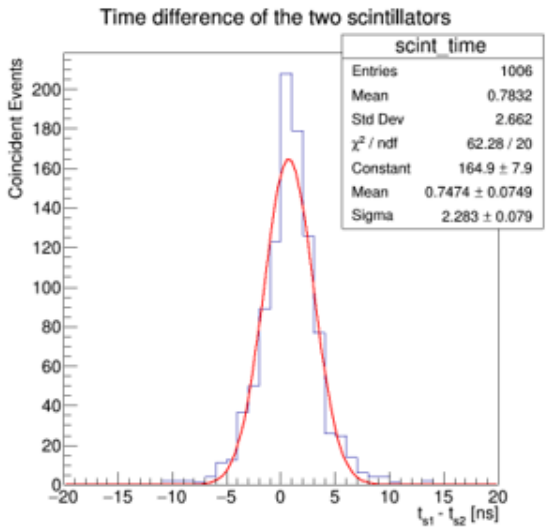


Figure 7.15: Distribution of the timing difference of the two scintillators ($t_{s1} - t_{s2}$). The Gaussian fit sigma is 2.28 ns.

Since the scintillators are used to provide a timing reference, it is vital to know how they perform. Figure 7.15 shows the timing difference of the two scintillators' response to the same cosmic muon. The sigma from the Gaussian fit is 2.28 ns. Assuming that both scintillators have the same timing performance, the timing resolution of a single scintillator is $2.28/\sqrt{2} = 1.61$ ns. This is negligible compared to the sTGC pad timing.

Figure 7.16 and Figure 7.17 show the time difference measurements for a selected sTGC pad from the QS2C quadruplet with a high voltage of 2,800 V. The Gaussian fit results show that $t_{\text{tot}} - t_s$ has a sigma of 7.56 ns, and $t_{\text{peak}} - t_s$ has a sigma of 6.36 ns. The timing performance of t_{peak} is slightly better than t_{tot}.

Since the timing performance is correlated to the high voltage applied and the threshold setting, A high voltage scan was also performed. Figure 7.18 shows the Gaussian fit sigma results under different circumstances. The t_{tot} performs better with higher high voltage and lower threshold settings. This is due to the time walk effect, which will be discussed in Section 7.2.5. The t_{peak} has relatively stable performance and outperforms t_{tot} when the high voltage is lower than 2,900 V.

Another metric used to describe the timing performance is the fraction of events with the time

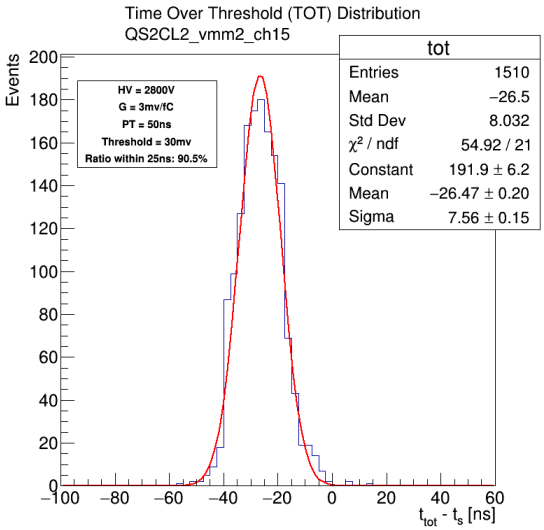


Figure 7.16: Distribution of the $t_{\text{tot}} - t_s$ for a selected pad on the QS2C quadruplet. The Gaussian fit sigma is 7.56 ns.

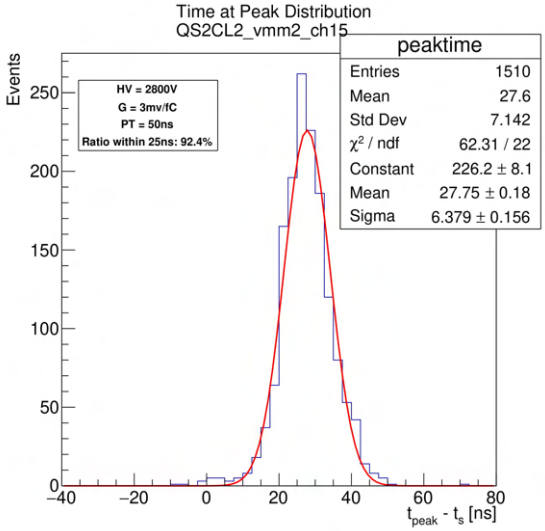


Figure 7.17: Distribution of the $t_{\text{peak}} - t_s$ of a selected pad on the QS2C quadruplet. The Gaussian fit sigma is 6.38 ns.

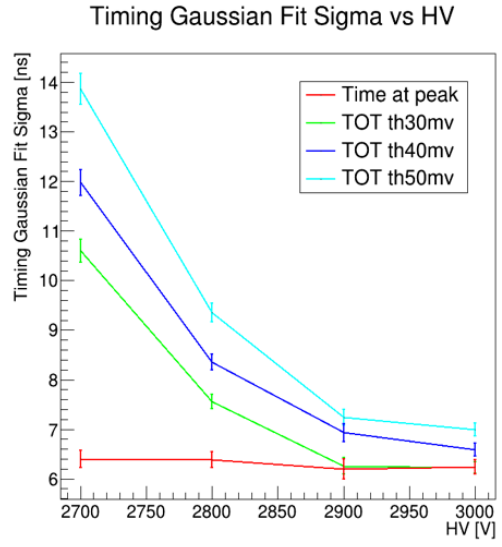


Figure 7.18: Gaussian fit sigma of the timing distribution as a function of the high voltage applied.

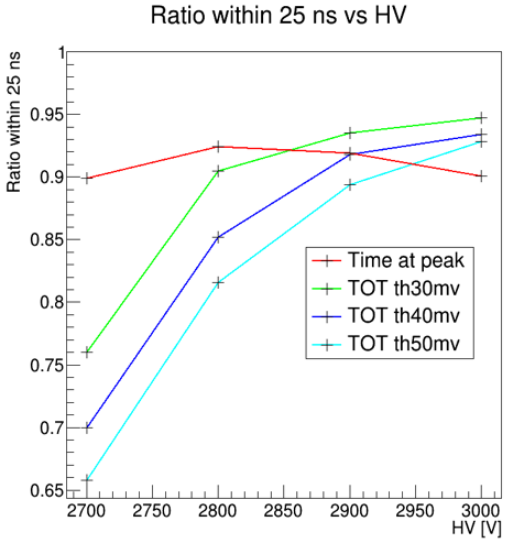


Figure 7.19: The fraction of events contained within 25 ns.

difference smaller than 25 ns (one BC). This is essential to know since the hit status information of the pad TDS is in one BC frame. Figure 7.19 presents the fraction as a function of the high voltage applied. The performance of t_{peak} reaches the highest point at 2,800 V and drops if the high voltage keeps increasing. This is due to the saturation of the VMM. About 90% of events have the time difference smaller than 25 ns. For the t_{tot} performance, higher high voltage and lower threshold

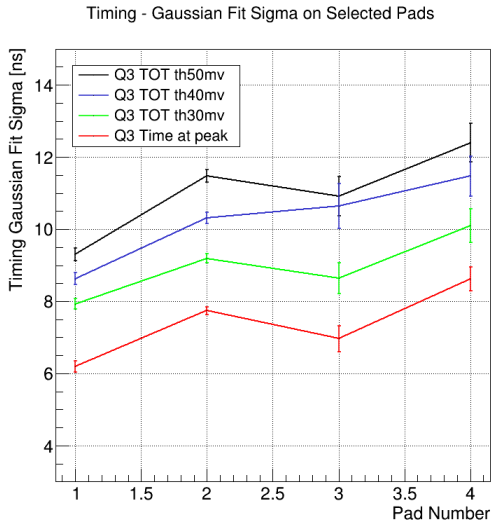


Figure 7.20: Timing Gaussian fit sigma of the selected pads with 2,800 V. The x-axis is the pad number. Each line represents the performance of the four pads under a particular case.

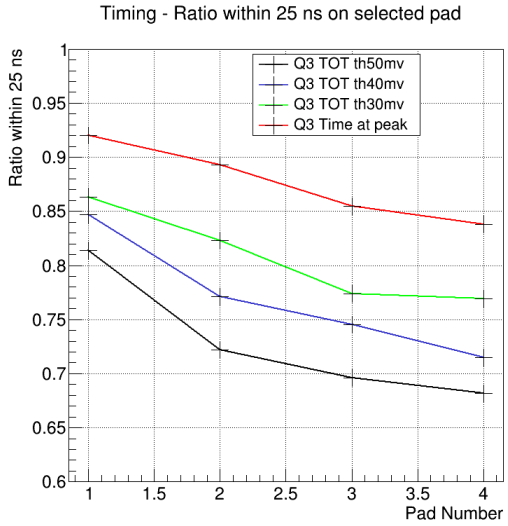


Figure 7.21: The ratio (events contained within 25 ns) of the selected pads with 2,800 V. The x-axis is the pad number. Each line represents the performance of the four pads under a particular case.

result in better performance. To reach the ratio of 90%, the high voltage needs to be set at 2,800 V for 30 mV threshold, 2,900 V for 40 mV, and 3,000 V for 50 mV.

The timing performance of the other three selected pads (mentioned in Table 7.1) are also measured. Figure 7.20 and Figure 7.21 show the results of the Gaussian fit sigma and the fraction of events within one BC. As shown in these two figures, t_{peak} consistently outperforms t_{tot} when the threshold is set to be higher than 30 mV.

It is good to set the threshold higher than five times the noise RMS (around 30 mV for our setup). The current default high voltage setting for the sTGC detector is 2,800 V. With all of that in consideration, the VMM PtP mode is a better choice than the VMM ToT mode in terms of timing performance. The timing performance in the trigger will be discussed in Section 7.3.4.

7.2.5 Time Walk Effect

The performance of the t_{tot} is highly sensitive to the high voltage and the threshold setting. This is due to the time walk effect. In this section, let us take a detailed look at this effect.

Figure 7.22 and Figure 7.23 show the two-dimensional distribution of the $t_{\text{tot}} - t_s$ in terms of the signal amplitude at 2,700 V and 3,000 V. With 2,700 V, the majority of the signals have an amplitude around 100 mV. For a typical muon signal, it raises quickly from the baseline and becomes flat when it reaches the peak. When the amplitude is comparable to the threshold, it takes

longer for the signal to cross the threshold with the flat shape at the top. Signals with different amplitudes thus will cross the same threshold at different times. With 3,000 V, the signal amplitude is usually larger than 200 mV as shown in Figure 7.23. The signals thus will pass the threshold quickly, and the amplitude of the signal does not affect the crossing time that much.

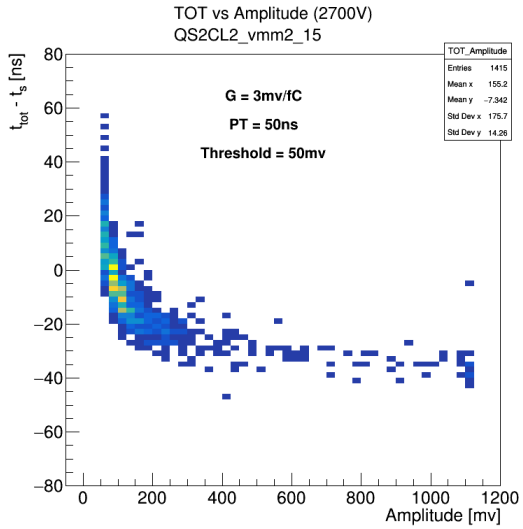


Figure 7.22: $t_{\text{tot}} - t_s$ vs the signal amplitude at 2,700 V.

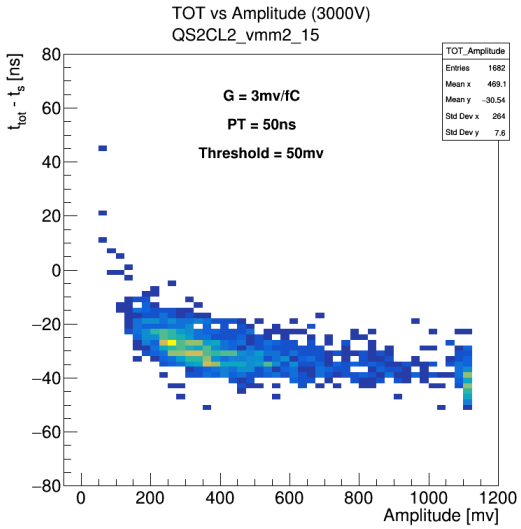


Figure 7.23: $t_{\text{tot}} - t_s$ vs the signal amplitude at 3,000 V.

Figure 7.24 shows the two-dimensional distribution of $t_{\text{peak}} - t_{\text{tot}}$ vs the signal amplitude at 2,700 V. Since t_{peak} is mainly determined by the time when the VMM stops to integrate the charges, it has smaller dependence on the signal amplitude compared to t_{tot}.

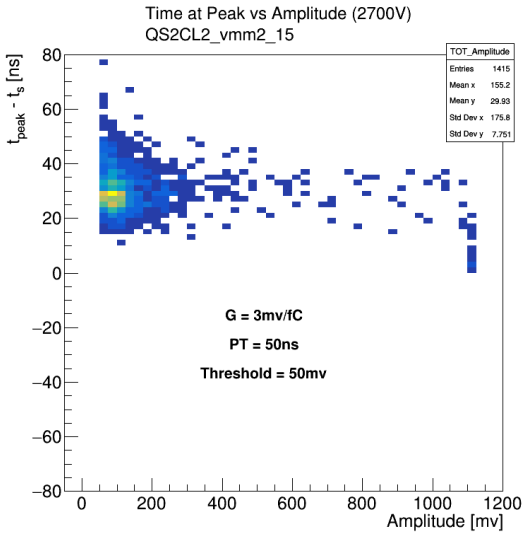


Figure 7.24: $t_{\text{peak}} - t_s$ vs the signal amplitude at 2,700 V.

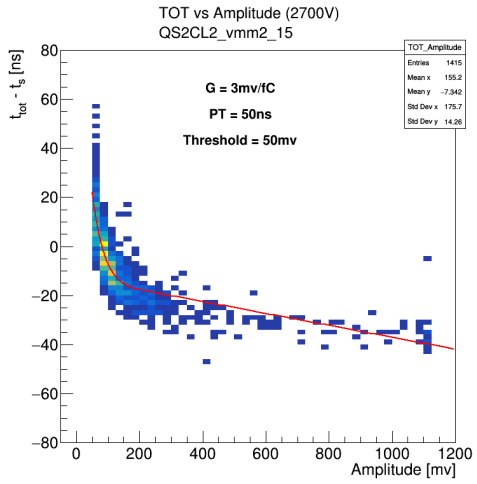


Figure 7.25: $t_{\text{tot}} - t_s$ vs the signal amplitude at 2,700 V. The red line fits the trend.

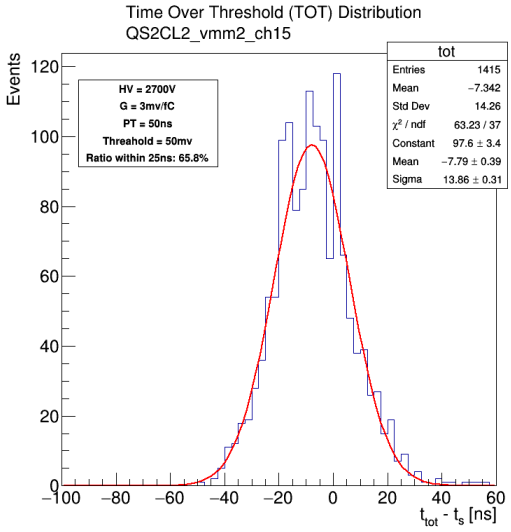


Figure 7.26: Distribution of the $t_{\text{tot}} - t_s$ at 2,700 V. The Gaussian fit sigma is 13.9 ns.

A common way to fix the time walk effect is using the amplitude correction (by adding a time offset to the measured time based on its signal amplitude). We already have both amplitude and timing information on hand, it is interesting to know how much the performance can be improved if the correction is applied.

Figure 7.25 and Figure 7.22 have the same $t_{\text{tot}} - t_s$ distribution but Figure 7.25 has a red curve that is a fit to the $t_{\text{tot}} - t_s$ distribution as a function of the signal amplitude. Figure 7.26 shows the original $t_{\text{tot}} - t_s$ distribution and has an Gaussian fit sigma of 13.9 ns. Time walk corrections can be made by using the red curve as a reference to offset the original signal timing. For each event, the timing is corrected by subtracting the value of the red curve.

Figure 7.27 shows $t_{\text{tot}} - t_s$ vs the signal amplitude after the time walk corrections applied and Figure 7.28 shows the new $t_{\text{tot}} - t_s$ distribution after the corrections applied. The sigma is improved to 5.4 mV. However, this correction is only a preliminary study and it uses the fitting curve to correct for itself, which is biased. The actual performance would be worse than 5.4 mV if more general correction functions are derived.

Nevertheless, the sTGC pad is designed to provide a quick coarse measurement, and online corrections in the trigger chain are not possible. Without corrections applied, t_{peak} is a better option than t_{tot} to avoid time walk effects. The drawback of using t_{peak} is that it adds additional delays to the signal processing time in the trigger chain.

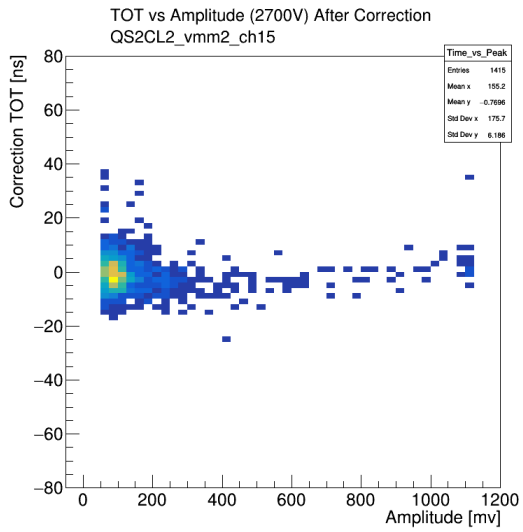


Figure 7.27: $t_{\text{tot}} - t_s$ vs the signal amplitude at 2,700 V after the time walk corrections applied.

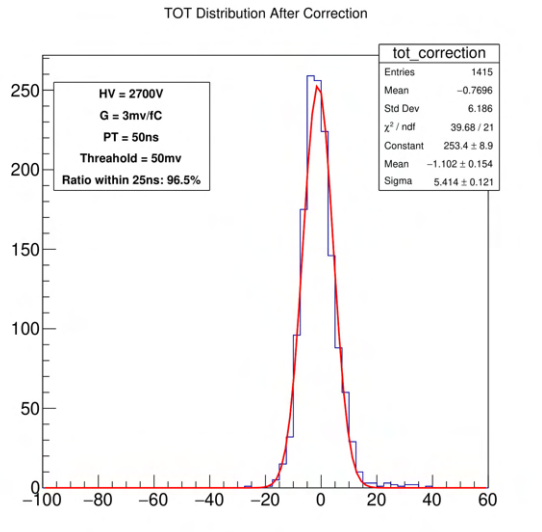


Figure 7.28: Distribution of the $t_{\text{tot}} - t_s$ at 2,700 V after the time walk corrections applied. The Gaussian fit sigma is 5.4 ns.

7.3 sTGC Pad in the Trigger Chain

In the previous section, performances of sTGC pads are studied using analog signals. However, sTGC pads will be used in the trigger chain with the front-end electronics. In this section, I will present the performance study of the sTGC pad in the trigger chain. If not explicitly mentioned, the pad TDS trigger chain data is collected using the mini-DAQ Active Data Readout module (see Section 5.4) with the horizontal trigger scheme.

7.3.1 Mapping Verification

To study the sTGC pad in the trigger chain, we need to map electronics channels to actual pads. We extract the mapping from the sTGC adaptor board, and this mapping needs to be further verified.

The first method is looking at the sTGC pad hit map with external triggers from the scintillators. The scintillators were placed to trigger a hypothetical sTGC pad. The pad TDS data was collected by the mini-DAQ system with external trigger signals from the scintillators. Offline analysis mapped the TDS channel to the sTGC pad and filled in the hit map plot. Multiple locations have been chosen, and Figure 7.29 presents one of the hit maps. The locations of the pads after the mapping match where the scintillators are placed.

The second method is looking at the column hit correlation between different layers. The sTGC pad has many columns (more than 10). When a muon passes through the detector, it will likely hit the same column in the next layer since the layers are closely placed (less than 10 mm). The mini-

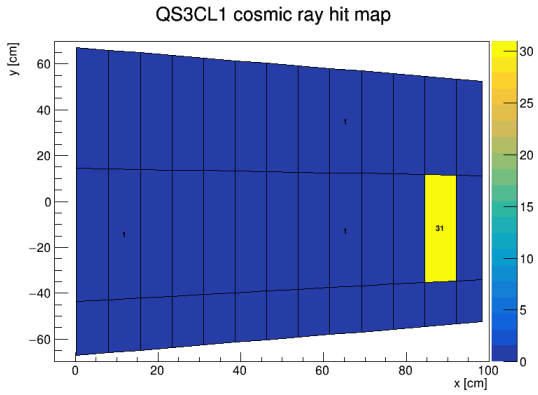


Figure 7.29: An example hit map for the mapping verification. The location of the fired pad matches the location where the scintillators were placed.

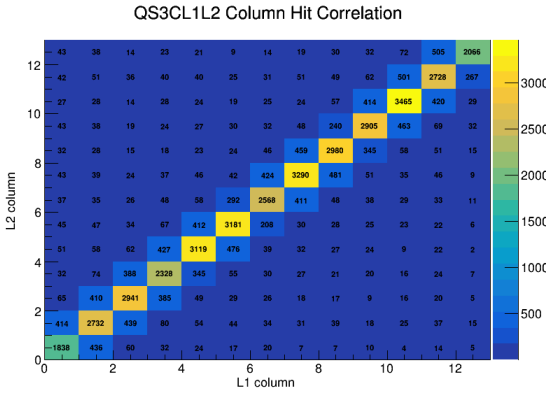


Figure 7.30: The column hit correlation plot between layer 1 and layer 2 on QS3C. A clear diagonal line confirms the mapping.

DAQ system collects the pad TDS data in the triggerless mode. In each event, off-line analysis filled the column correlation plot after channel mapping. Figure 7.30 is one example showing the column correlation between layer 1 and layer 2. We observed large corrections along the diagonal line, which further confirms the mapping.

7.3.2 S-curve

The S-curve study aims to measure the sTGC pad noise performance in the trigger chain. The S-curve is named since the curve has an "S"-shape. The sTGC detector is supplied with 2000 V in the study and thus signals obtained are mainly due to noises. The noise rate is monitored by the mini-DAQ Rate Monitor module (presented in Section 5.2). Figure 7.31 shows the S-curve for the pads on layer 1 of the QS3C quadruplet. The x-axis is the threshold setting (above the baseline), and the y-axis shows the noise rate on a logarithmic scale. Once the threshold is below 30 mV, the noise rate rises quickly and reaches around 2 MHz (reach the VMM dead time) when the threshold is close to the baseline. The S-curve provides a reference for the noise rate under different threshold settings. In our later study, we will not use a threshold lower than 30 mV to avoid noises.

7.3.3 Efficiency

Using the same efficiency measurement as presented in Section 7.2.3 for analog signals, the sTGC trigger chain pad efficiency is defined as

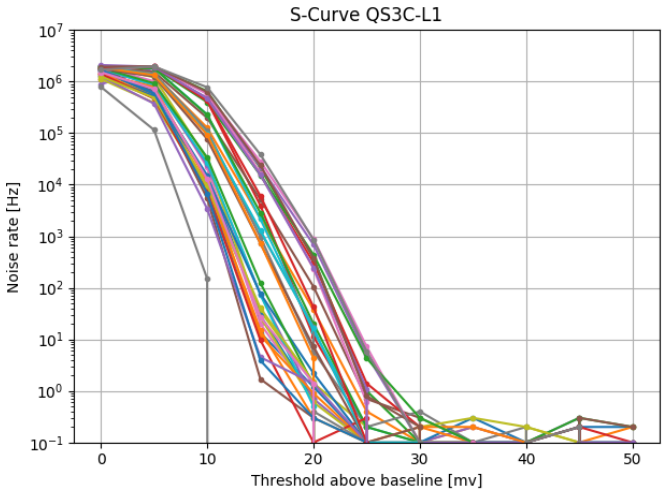


Figure 7.31: The S-curve for pads on layer 1 of the QS3C quadruplet. Each line presents one sTGC pad channel.

$$\text{Efficiency} = \frac{N_{\text{sTGC pad responses}}}{N_{\text{external triggers}}}. \tag{7.5}$$

In addition to collect the pad TDS data using the mini-DAQ system, we also use the oscilloscope to sample analog signals to determine the fraction of signals lost due to the trigger chain electronics process.

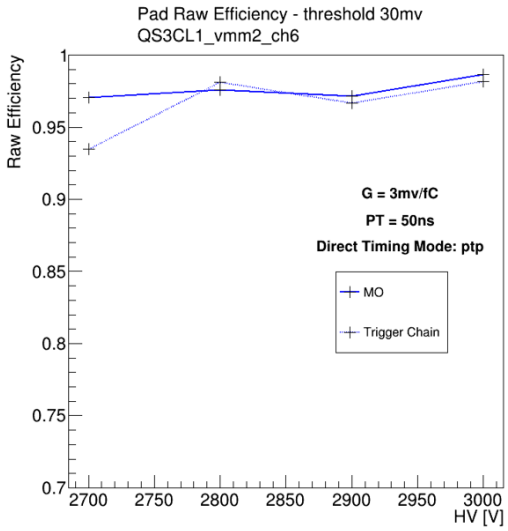


Figure 7.32: The sTGC pad efficiency with a threshold of 30 mV.

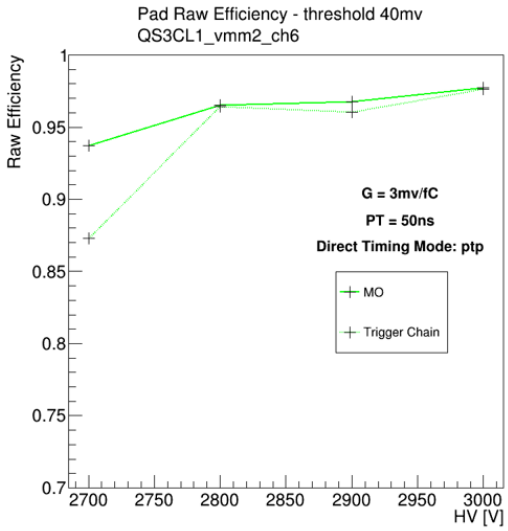


Figure 7.33: The sTGC pad efficiency with a threshold of 40 mV.

Figure 7.32, Figure 7.33, and Figure 7.34 show the measured efficiency of a selected pad with

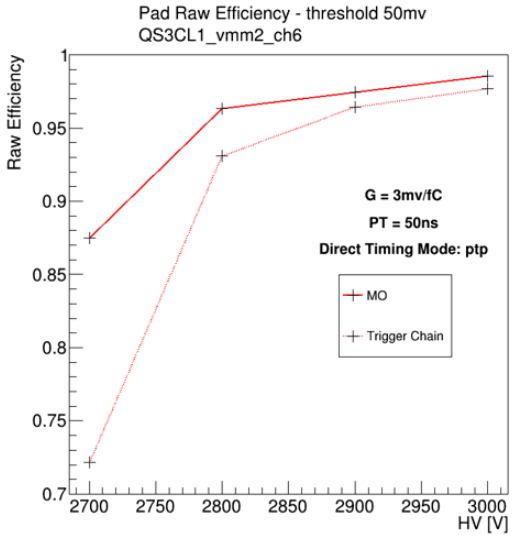


Figure 7.34: The sTGC pad efficiency with a threshold of 50 mV.

different VMM threshold settings. The solid lines show the results from the VMM MO analog signal measurement, and the dashed lines show the results from the digitized data. We scan the high voltage from 2,700 V to 3,000 V. Except for 2,700 V, the two efficiencies are very close, with the analog signal efficiency slightly higher than the trigger chain efficiency.

The discrepancies might be caused by the fact that the threshold used in the VMM is not as accurate as that of the oscilloscope. When the signal is smaller or the threshold is higher, the discrepancies will be enlarged. In overall, the trigger chain efficiency agrees with the efficiency measured by analog signals. At 2,800 V and 30 mV thresholds, this sTGC pad efficiency reaches 97% in the trigger chain.

7.3.4 Timing Performance

Similar to the timing performance measurement mentioned in Section 7.2.4, we use the external trigger provided by the scintillators to represent the arrival time of the cosmic muon (digitized by the mini-DAQ system) to obtain the TDS sampling BCID distribution. However, the pad TDS only has a timing LSB of 25 ns, which is difficult to measure the actual timing performance due to the binning effect.

Ideally, after a fixed delay of the trigger signal, the pad TDS will see the arrival of the ToT signal (for convenience, I will use the term ToT to represent the VMM direct output). However, the sTGC detector has its intrinsic timing resolution and VMM processing also brings some time jitters, the actual arrival time of the ToT signal will have some spreads (compare to the idal arrvial time).

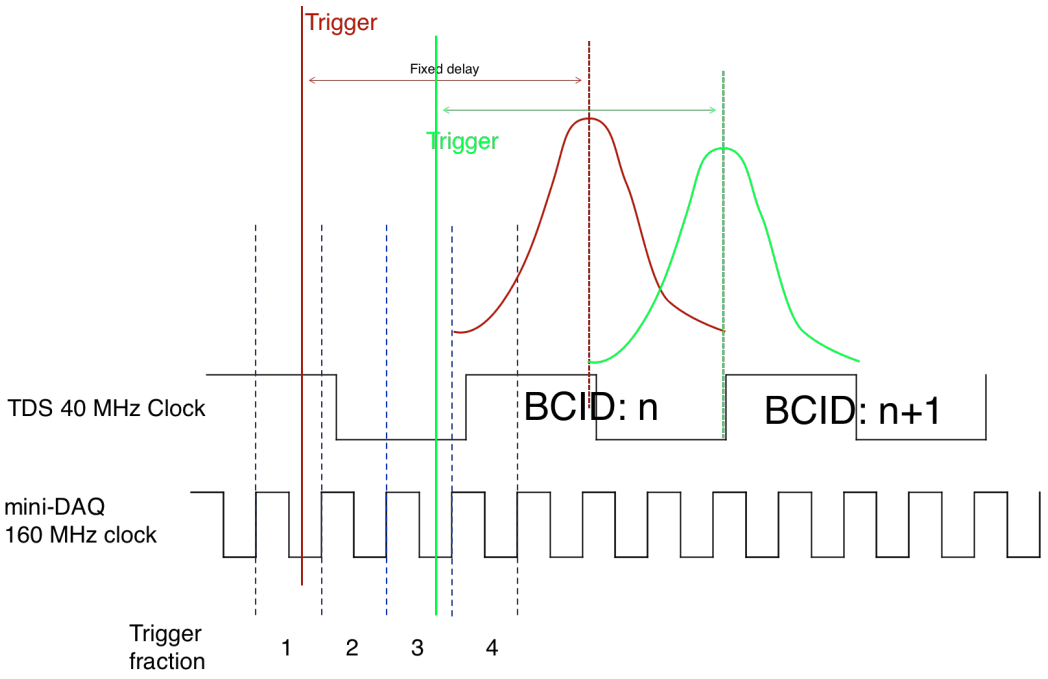


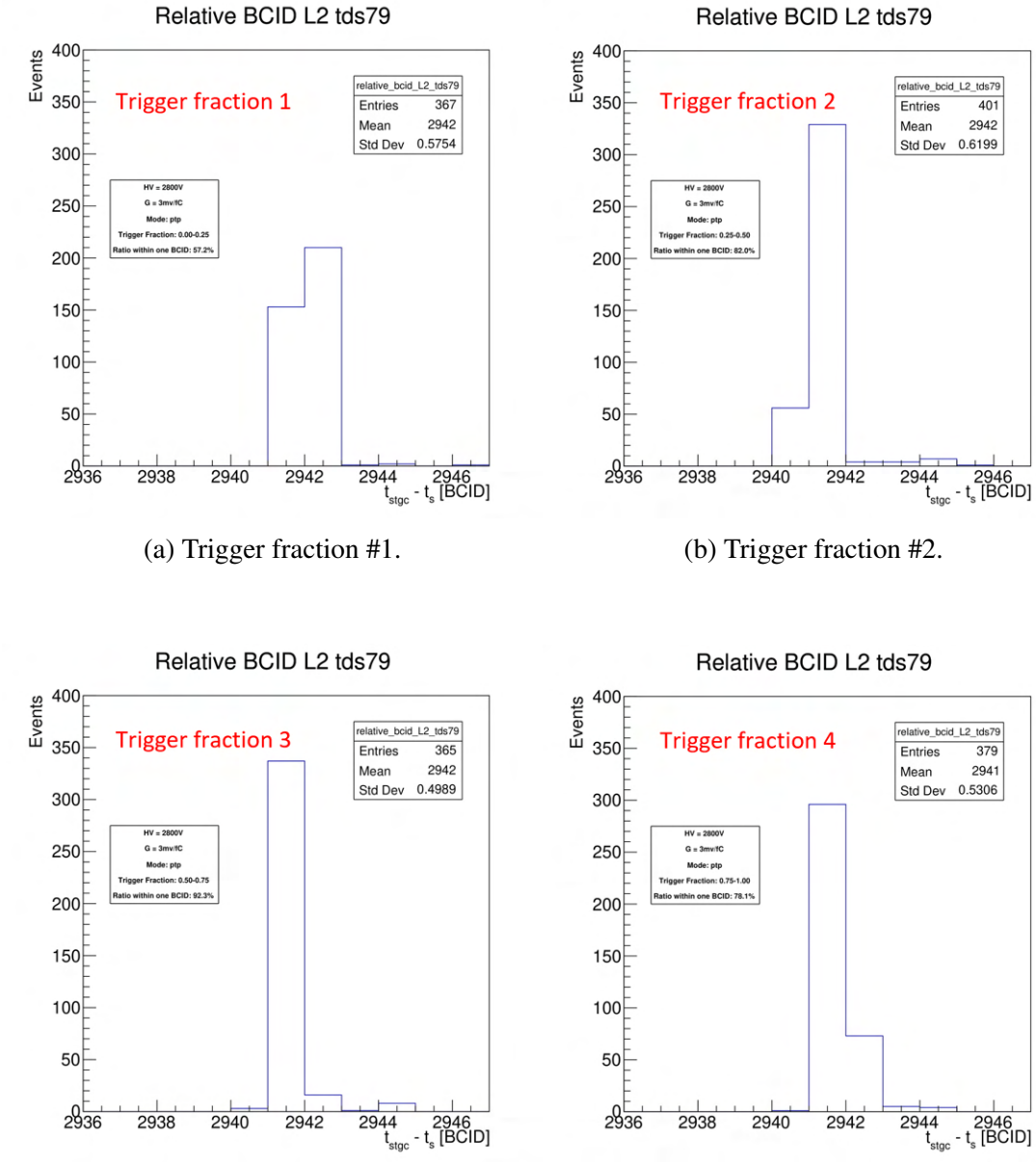
Figure 7.35: Demonstration of the binning effect. In the green line example, the ideal arrival time of the ToT pulse is close to the edge of the TDS 40 MHz clock. The TDS will have a 50% chance to sample the BCID as n and another 50% chance for BCID to be identified as $n+1$.

If the ideal ToT arrival time sits in the middle of the TDS 40 MHz BC clock, the TDS would give consistent timing measure results. The red line in Figure 7.35 shows the ideal case. However, if the ToT signal arrives at the edge of the BC clock, presented by the green line in Figure 7.35, the TDS will have a 50% chance to sample the BCID as n and another 50% chance for BCID to be identified as $n+1$. This is the binning effect.

In the ATLAS operation scheme, the distance from the IP to the sTGC detector is fixed. Muons will hit the sTGC detector in a certain amount of time after the pp collision. Since the LHC collision period and the TDS BC clock are synchronized, the arrival time of a muon is fixed to the TDS BC clock. Tuning the BC clock phase can avoid the binning effect. Nevertheless, We cannot ask cosmic muons to arrive at a specific time, a workaround is used to select events when muons show up at a particular time range.

Inside the mini-DAQ firmware, a 160 MHz clock will be used to sample the trigger signal. With an LSB of 6.25 ns (four times finer than one BC), we can divide the collected events into four fractions based on when the trigger signal arrives in the four 90° phases of a 40 MHz clock frame. Only the fraction with the best timing performance is chosen for the timing measurement. The binning effect is not totally avoided in this way, but we will have a result closer to the real performance.

As presented in Figure 7.35, the 160 MHz clock divides the trigger arrival time into four trigger fractions. The red line falls into trigger fraction #1, and the green line falls into trigger fraction #3. In this example, using results from trigger fraction #1 is a better choice than trigger fraction #3.



(a) Trigger fraction #1.

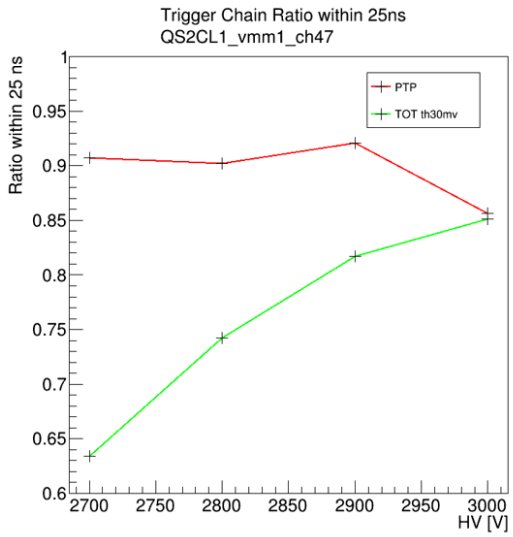
(b) Trigger fraction #2.

(c) Trigger fraction #3.

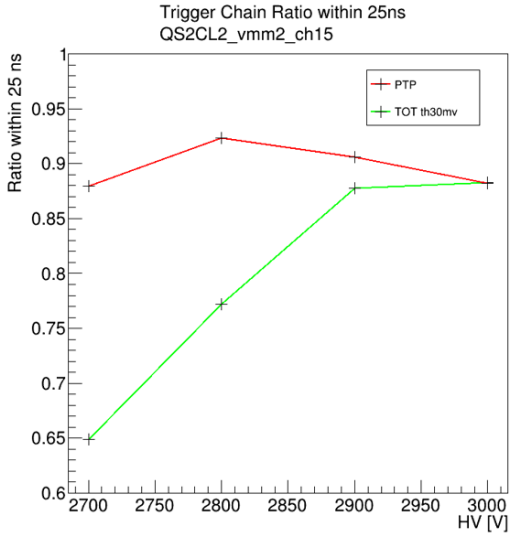
(d) Trigger fraction #4.

Figure 7.36: The distribution of the BCID difference with the four trigger fractions.

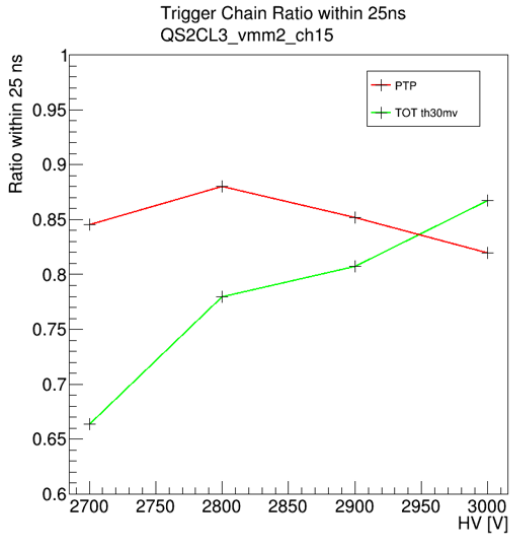
Figure 7.36 presents the trigger chain timing distribution of a selected pad with the trigger fraction dividing. The x-axis is the timing difference, calculated by subtracting the trigger signal BCID (digitized by the mini-DAQ system) from the BCID in the pad TDS data.



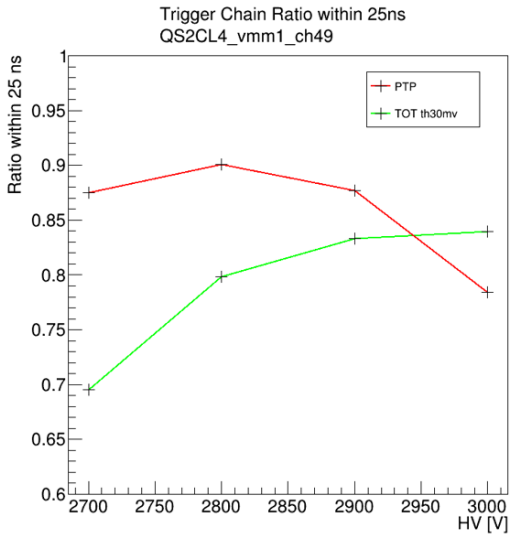
(a) Selected pad from layer 1.



(b) Selected pad from layer 2.



(c) Selected pad from layer 3.



(d) Selected pad from layer 4.

Figure 7.37: The percentage of the events contained within 25 ns on the four sTGC pads selected from a logical pad. The red lines are the results using VMM PtP mode, and the green lines are the results from VMM ToT mode with a 30 mV threshold setting.

In trigger fraction #1, most events are split into two BCs. When switching to trigger fraction #2, more events fall into the right bin. This is equivalent to shifting the distribution to the right. For trigger fraction #3, one bin has most of the events. When using trigger fraction #4, the bin at the right side of the majority bin shows more events. The percentages of events in one BC are 57.2%,

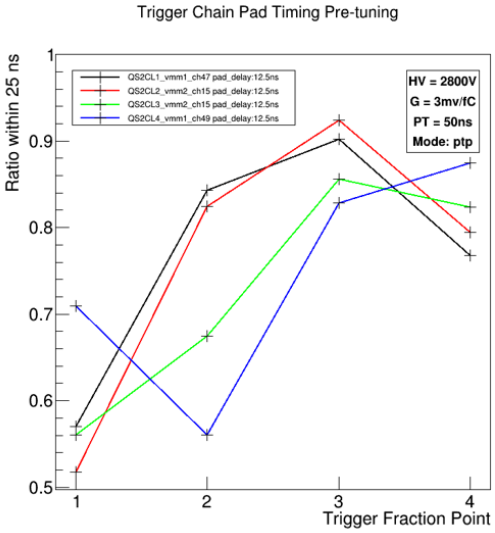


Figure 7.38: Timing performance vs. trigger fraction before tuning. All four pads have a pad dealy setting of 12.5 ns.

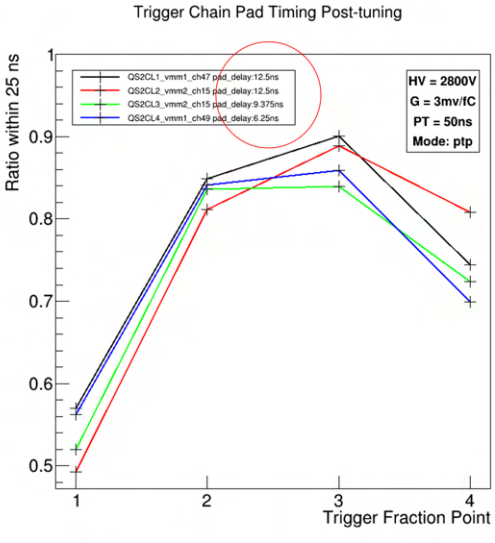


Figure 7.39: Timing performance vs. trigger fraction after tuning. Layer 1 pad delay: 12.5 ns; layer 2 pad delay: 12.5 ns; Layer 3 pad delay: 9.375 ns; layer 4 pad delay: 6.25 ns.

82.0%, 92.3%, and 78.1%, respectively. Therefore, the result of trigger fraction #3 will be used. This result is comparable with the measurement using analog signals (in Section 7.2.4). Dividing the events by four is good enough to look at the sTGC trigger chain timing performance, and the rest of the measurements are based on this method.

Four pads from a logical pad are selected for the timing performance measurement, and Figure 7.37 shows the measured results. The red lines are the results using the VMM PtP mode, and the green lines are the results from the VMM ToT mode with a 30 mV threshold (the lowest threshold we used). The performance agrees with the measurements presented in Figure 7.19 with the analog signal. At 2,800 V, the PtP mode reaches its best performance, and it outperforms the ToT mode. For those four selected pads, they have around 90% of events in one BC.

In Figure 7.36, the result of each pad is chosen from the trigger fraction with the best performance. But the chosen fractions are not necessarily the same due to differences in the sTGC pad trace length. Eventually, the four pads will be used simultaneously to form the 3-out-of-4 coincidence. Figure 7.38 presents their performance in terms of the trigger fractions. The pad from layer 1, layer 2, and layer 3 have their best performance at trigger fraction #3, but not for the pad from layer 4. The pad TDS channel delay function is designed to compensate this. In Figure 7.38, all delays are set to 12.5 ns. By shifting the layer 3 pad delay to 9.375 ns and the layer 4 pad delay to 6.25 ns, four pads reach their best performance at trigger fraction #3, as shown in Figure 7.39.

Figure 7.40 shows the related BCID hit distribution of the four pads using trigger fraction

3. The x-axis shows number of pads with the same BCID. For 3-out-of-4 coincidence using one BCID trigger window, the trigger efficiency is found to be 94.2%. One thing to note here is that this study only looks at events with all four pads fired. Thus the trigger efficiency measured here ignores individual pad raw efficiency.

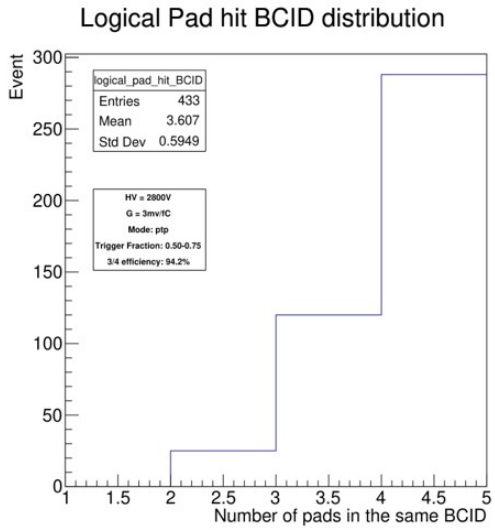


Figure 7.40: Logical pad BCID distribution. For 3-out-of-4 coincidence using one BCID trigger window, the trigger efficiency is found to be 94.2%.

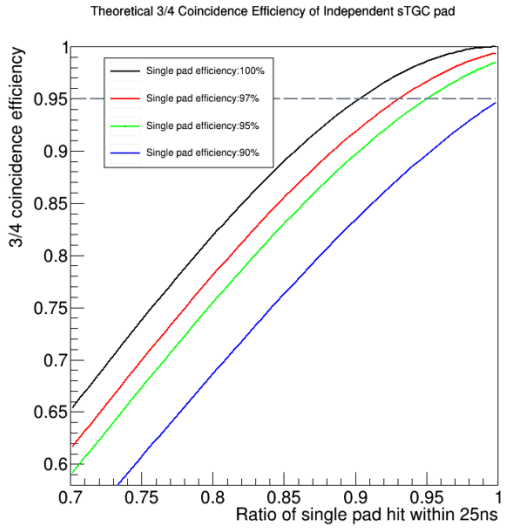


Figure 7.41: The simulation result of 3-out-of-4 coincidence efficiency.

A simulation, which assumes each pad is independent and a binomial distribution is used, provides a reference for the 3-out-of-4 coincidence efficiency using one BCID window, and the

result is shown in Figure 7.41. To reach an efficiency of 95%, if the individual pad raw efficiency is 97%, at least 90% of the hit for a single pad must be contained within the same BCID. The performance we observed barely meets such a requirement, even under our single wedge setup with a 30 mV threshold setting and a noise RMS less than 6 mV. For the final operation, to reach 95% of the 3-out-of-4 coincidence efficiency, it is recommended to use two BCID windows. This also loses the tuning effort for the BC clock phase and individual pad delay.

7.4 Logical pad and sTGC strip in the Trigger Chain

When a muon passes through an sTGC quadruplet, it hits one pad in each layer. The combination of the four pads is called a logical pad, and it defines the region of interest for this muon track. The logical pad is used to map the fired pads to an interesting area smaller than the size of the sTGC pad, as shown in Figure 7.42.

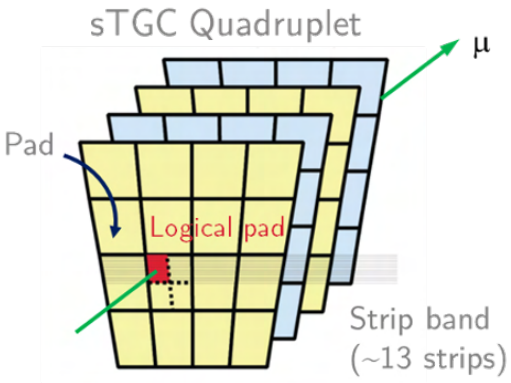


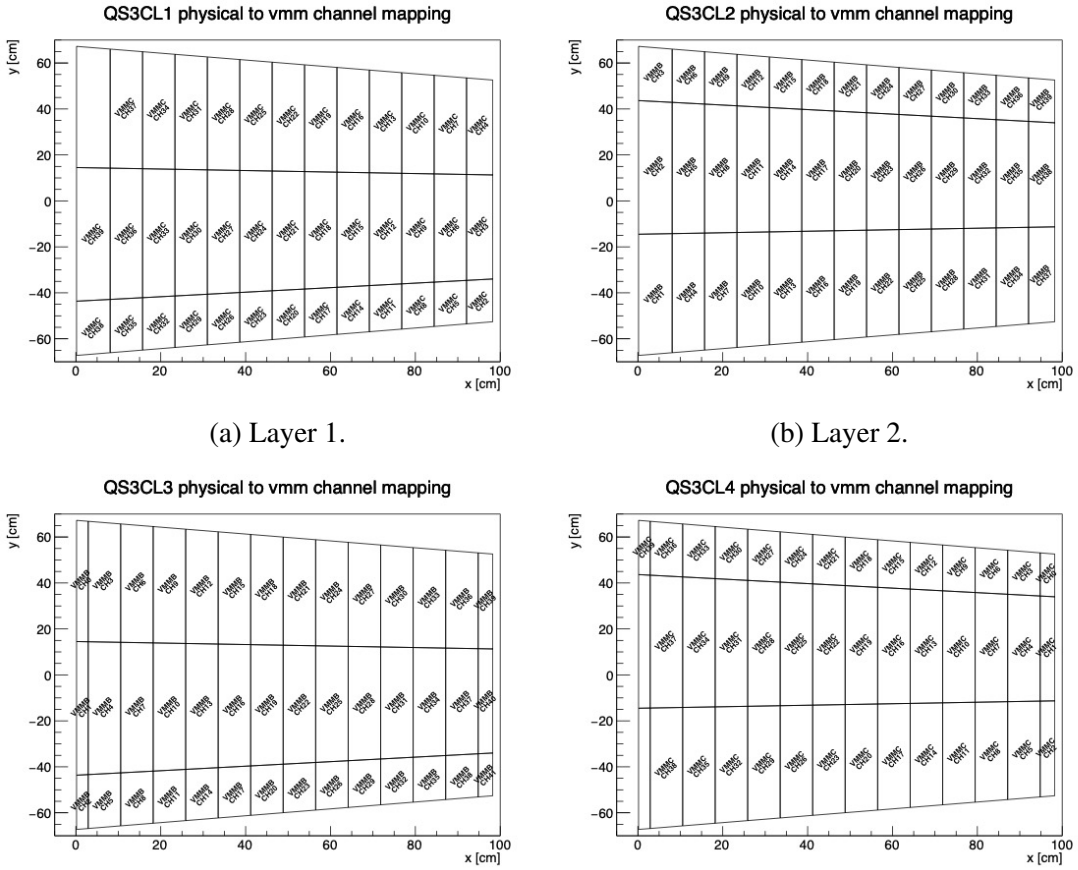
Figure 7.42: Demonstration of the logical pad [59].

Different quadruplets have different pad divisions in each layer. This section will focus on the QS3C quadruplet study on selecting the logical pad combinations, implementing the mini-DAQ firmware for online-trigger generation, and read out strip 6-bit ADC data.

7.4.1 Logical Pad Generation

Figure 7.43 shows the sTGC pad divisions on the QS3C quadruplet. Each layer has three rows of pads. Layer 1 and layer 2 have 13 rows, while layer 3 and layer 4 have 14 rows. The pad division on layer 1 and layer 2 are the same but mirrored by the y-axis, so are layer 3 and layer 4.

Figure 7.44 shows the projection of pad divisions from four layers. The new division splits the detector plane into 130 pieces with 60 large pieces and 70 small pieces. If muons pass through the detector vertically, those 130 pieces are all logical pads for all possible muon tracks. In terms of



(a) Layer 1.

(b) Layer 2.

(c) Layer 3.

(d) Layer 4.

Figure 7.43: sTGC pad divisions on the QS3C quadruplet.

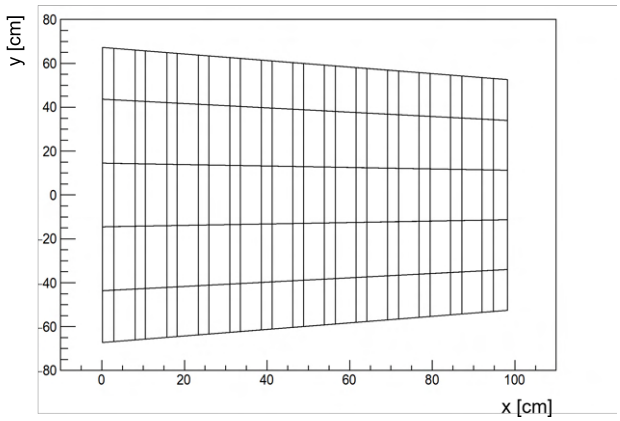


Figure 7.44: Projection of the pad divisions from the four layers on the QS3C quadruplet. The new division splits the detector plane into 130 pieces with 60 large pieces and 70 small pieces.

cosmic muons in the vertical trigger scheme, those 130 logical pads have the large chance to be fired. However, there are still other logical pads that muons could hit with large incident angles. We need to figure out how many logical pads and what are the logical pads needed to reach a reasonable geometric acceptance.

The MC simulation is used to find all possible logical pads. The simulation samples the muon incident angle (θ, ϕ) based on Eq. 7.2, and then inject it into the sTGC detector. It records the four pads (a logical pad) fired in each event. We will have a list of logical pads at the end.

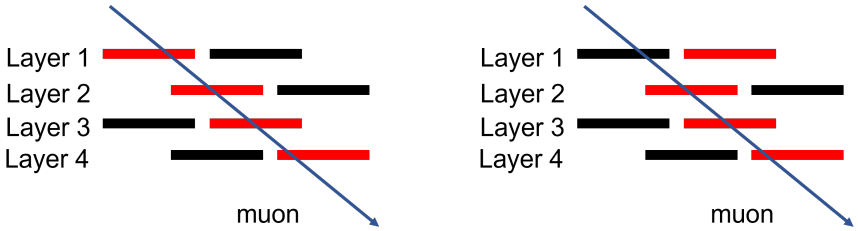


Figure 7.45: Demonstration of multiple logical pads firing under the 3-out-of-4 coincidence.

The 3-out-of-4 coincidence needs to be taken into consideration in the logical pads selection. Figure 7.45 shows a case that two logical pads, marked by red pads, will be fired by the same muon under the 3-out-of-4 coincidence. However, only one trigger could be sent out in every BC. Consequently, we sort the logical pads based on their event numbers and prioritized the logical pads that have a larger chance of being fired.

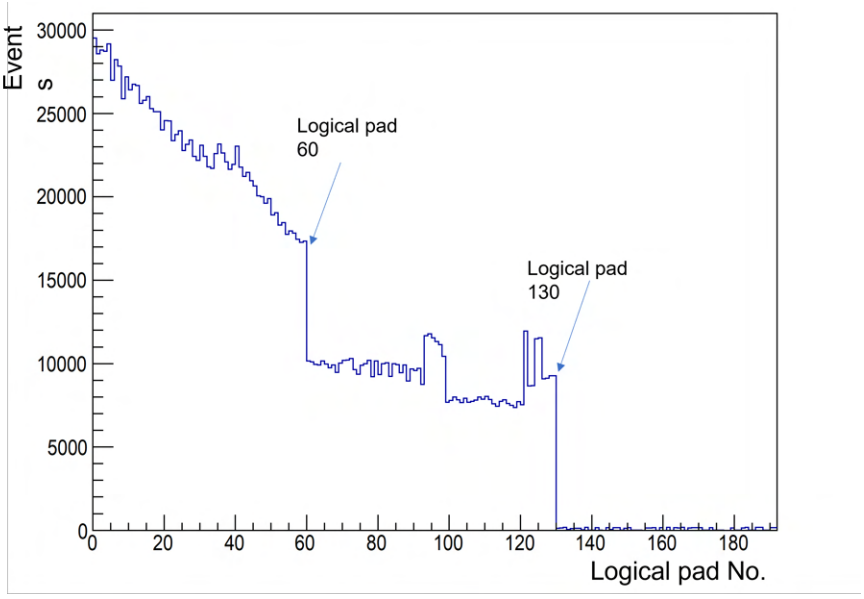


Figure 7.46: Logical pad event distribution.

Once we have the logical pads sorted, we import those logical pads back to the simulation.

We will emulate the 3-out-of-4 coincidence procedure in the simulation this time. The simulation samples muons and injects them into the detector, and only records the logical pads fired based on the coincidence and priority order. Figure 7.46 shows the logical pad event distribution. Most events pass through 130 logical pads defined earlier. There is a sudden event rate drop at the logical pad 60. This is because the first 60 logical pads have an area larger than the rest 70. After the logical pad 130, there are still some events contributed by muons with large incident angles.

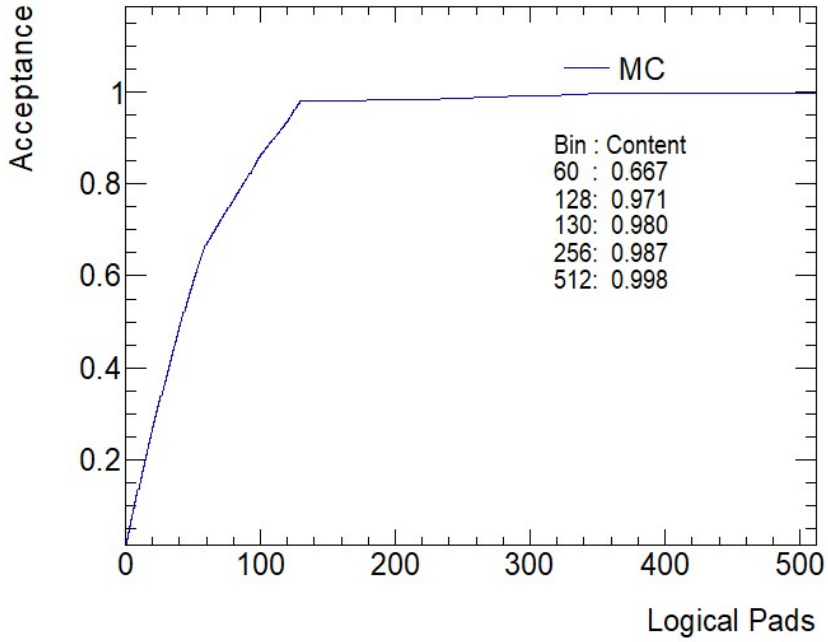


Figure 7.47: Logical pad geometric acceptance.

Figure 7.47 shows the geometric acceptance as a function of the number of logical pads used. The geometric acceptance is defined as the ratio of the number of events accepted and the total event number. If only a few logical pads were used, events would be lost since the tracks will not be recognized by the logical pads. If too many logical pads are used, they will consume unnecessary hardware resources. As shown in Figure 7.47, when 130 logical pads are used, it has an acceptance of 97% and reaches the plateau. Further increase of the number of logical pads will only slightly improve the acceptance. Therefore, 130 logical pads are the sweet point. The mini-DAQ firmware can incorporate 256 logical pads, and thus this firmware is enough for the cosmic study on the QS3C quadruplet.

7.4.2 Logical Pad Hit Distribution

The selected logical pads are imported into the mini-DAQ Online Trigger module (see Section 5.3). The module is configured to perform 3-out-of-4 coincidence with a two-BCID matching window, which eliminates the phase tuning process.

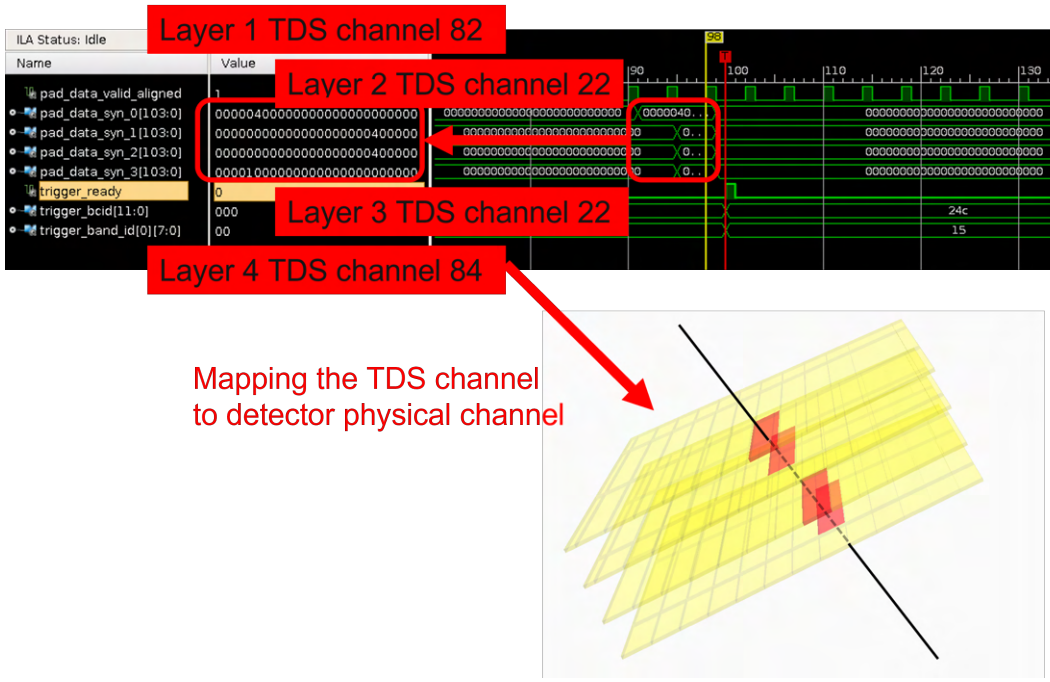
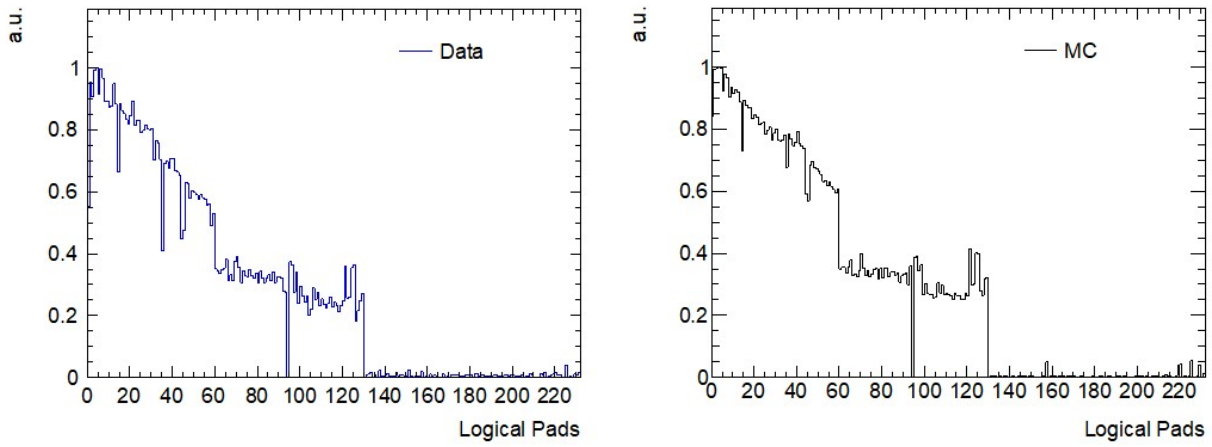


Figure 7.48: An online trigger captured by the ILA core. Each layer has one pad fired, and the bottom 3D model shows all fired pads.

A Xilinx Integrated Logic Analyzer (ILA) debugging core is used to monitor the trigger status. An example is presented in Figure 7.48. Each layer has one pad fired, and the bottom 3D model shows all pads fired. An online trigger signal is generated afterward.

The mini-DAQ system will also upload fired logical pads using the Active Data Readout module. Figure 7.49a shows the hit distribution of all logical pads. An MC simulation is also performed and the results are presented in Figure 7.49b. The MC simulation also considers that there are three dead channels on the quadruplet, and this is why there are few dips in the distribution plot compared to the ideal case shown in Figure 7.46. The overall shape of the hit distribution measured agrees with the simulation. The percentage of each bin differs a little bit, and that is because the MC simulation does not taken into account different timing performance and raw efficiency of each individual pad.



(a) Data.

(b) MC simulation.

Figure 7.49: Hit distribution of the logical pads on the QS3C quadruplet.

7.4.3 Strip TDS Band-ID LUT

To read out the 6-bit ADC data from the strip TDS, a proper strip TDS Band-ID LUT needs to be designed. Each TDS has 16 Band-ID LUT slots and 128 input channels, and each Band-ID covers 17 strip channels (before the selection) as described in Section 5.1.1.6. Therefore, 16 Band-ID LUTs should be enough to cover all 128 channels. An intuitive idea is to assign the leading strip evenly distributed with an interval of 8 (128/16 = 8). Each layer of the QS3C quadruplet has 307 strips, and 3 TDS chips are thus used. Table 7.2 shows the evenly distributed LUT design for all TDS chips on layer 1. In total, 37 Band-IDs are used. Only 7 LUT slots are configured for TDS1 since not all TDS channels are connected to physical channels. At the edge of two TDSs, the same Band-ID is given to the adjacent groups. This is because a muon may hit both TDSs on the edge.

We need to assign a Band-ID to each logical pad. The MC simulation is used. In the simulation, we only look at muons that pass through a logical pad and record strips that each logical pad covers. We then select a Band-ID (with a coverage of 17 strips) with the highest event coverage for each logical pad.

Figure 7.50 shows number of strips that each logical pad covers in the MC simulation without charge sharing. The first 60 logical pads cover 22-24 strips each, which exceeds the 17-strip coverage by one Band-ID. Since there are a small number of muons injected with larger angles, if we lower the acceptance coverage from 100% to 95%, the number of strips per logical pad will be reduced to 17-19 for the first 60 logical pads. However, this number would be larger with the strip charge sharing. Using only one Band-ID is thus not enough to cover the strips during the cosmic muon study, and more discussions will be shown in the next section. This is not a problem for the

TDS #	Band-ID #	Leading strip #	Physical Channel #
1	1	77	307
	2	85	299
	3	93	291
	4	101	283
	5	109	275
	6	117	267
	7	125	259
2	7	0	256
	8	8	248
	9	16	240
	10	24	232
	11	32	224
	12	40	216
	13	48	208
	14	56	200
	15	64	192
	16	72	184
	17	80	176
	18	88	168
	19	96	160
	20	104	152
	21	112	144
	22	120	136
3	22	0	128
	23	8	120
	24	16	112
	25	24	104
	26	32	96
	27	40	88
	28	48	80
	29	56	72
	30	64	64
	31	72	56
	32	80	48
	33	88	40
	34	96	32
	35	104	24
	36	112	16
	37	120	8

Table 7.2: The strip TDS Band-ID LUT for the three TDSs on layer 1.

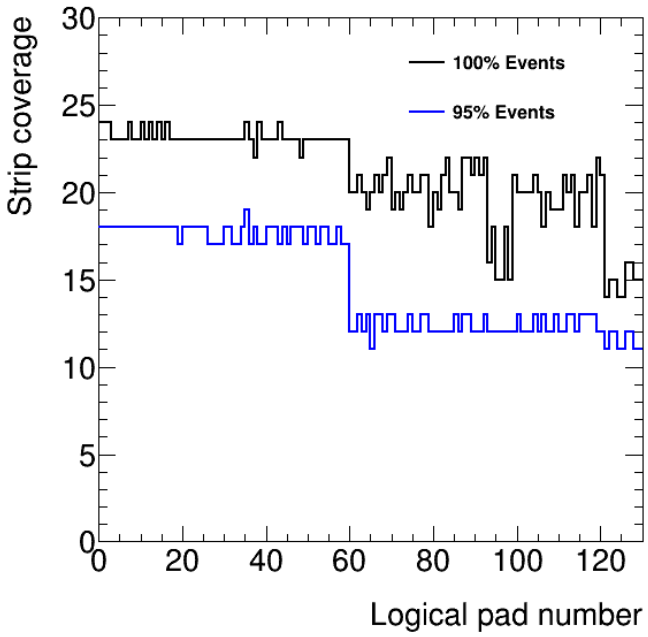


Figure 7.50: Number of strips that each logical pad covers in the MC simulation without charge sharing.

final operation scheme at ATLAS since muon incident angles are relatively fixed.

7.4.4 sTGC Strip 6-bit ADC Readout

Finally, we have everything to read out the strip TDS 6-bit ADC data. The logical pads with assigned Band-ID will be implemented in the mini-DAQ firmware, and the Band-ID LUTs will be stored inside the strip TDS.

Start with the ILA debugging waveform, Figure 7.51 shows the two ILAs used to monitor the online trigger generation and the strip TDS data. The top ILA monitored the data from the four pad TDSs and the online trigger. Circled by red lines, a logical pad is fired and a trigger with Band-ID "0C" is generated. The mini-DAQ system sends six triggers to the strip TDS with six consecutive BCIDs to match the BCID window. The bottom ILA shows that the strips TDS received the six triggers with the Band-ID "0C". It also shows that five strip channels have 6-bit ADC data sent out, marked by the blue box.

Next, we will use the mini-DAQ Active Readout Module to read out strip TDS data. Figure 7.52a shows the hit map on layer 4 from the data collected. The hits are distributed unevenly in the hit map with a few darker bands. There are two factors that caused this:

- One Band-ID per logical pad is insufficient to cover all fired strips, as mentioned in the previous section. Figure 7.52b shows the MC simulation with the strip charge sharing and strip

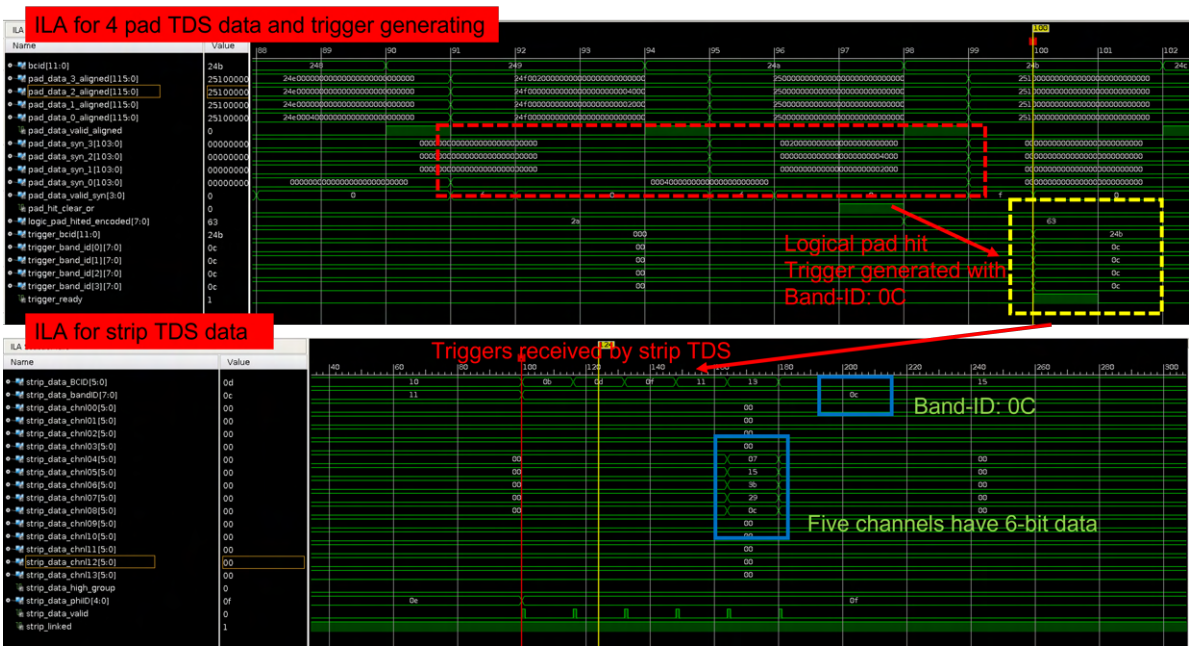
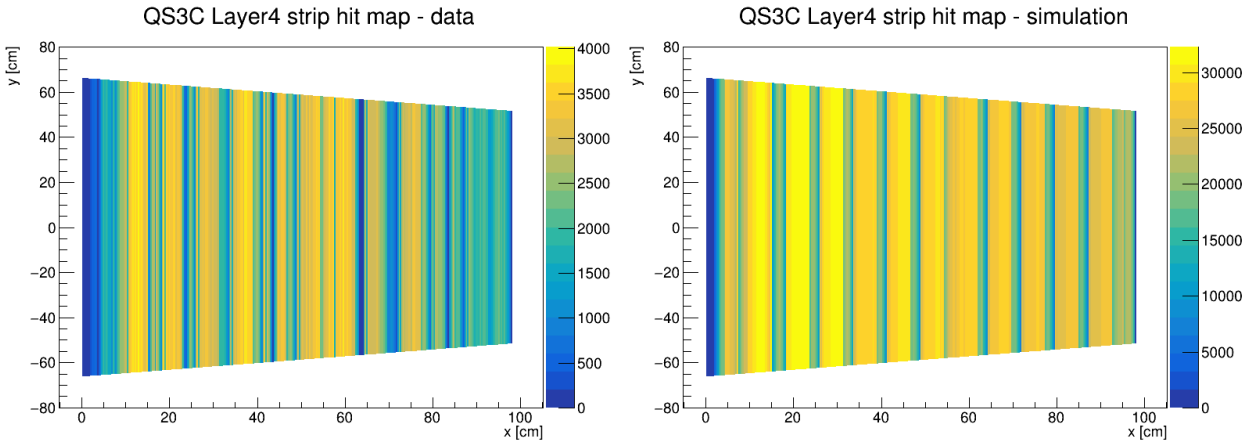


Figure 7.51: Online trigger generating and strip TDS data receiving in ILA.



(a) Data.

(b) MC simulation.

Figure 7.52: The sTGC strip hit map on layer 4.

TDS readout mechanism implemented. The simulation assumes that if the muon fires one strip, the two neighbor strips have a certain chance to be fired. Once a sampled muon passes through the detector, the simulation will look at which logical pad the muon hit. Using the same logical pad to Band-ID relationship and the Band-ID LUT, the simulation will decide which 14 strips to accept using the exact strip TDS triggering mechanism. The simulated hit map further confirms the uneven distribution (If the strip readout is not constraint by the

strip TDS triggering mechanism, the simulation will show an even distribution).

- The sTGC detector has spacers in the gas gap with an interval of around 20 cm apart. If the muon hits those areas, the sTGC detector will have no response.

To overcome the insufficiency of one Band-ID, we decided to send multiple Band-IDs for each triggered event. The mini-DAQ system will dispatch 15 trigger signals, 3 BCIDs $\times$ 5 Band-IDs, to the strip TDS every time a logical pad is fired.

Figure 7.53 is an ILA screenshot that shows the strip TDS data under the revised trigger scheme. At the time marked by the yellow line, three channels had 6-bit ADC data, which would be the result if only one Band-ID was used. In the next Band-ID, four channels had 6-bit ADC data, and this is the complete strip firing information in the event. The channel number shifts by 8 in the next Band-ID because the Band-ID LUT was designed with an interval of 8 strips. The offline analysis will look at the data packets and filter out redundant channels.

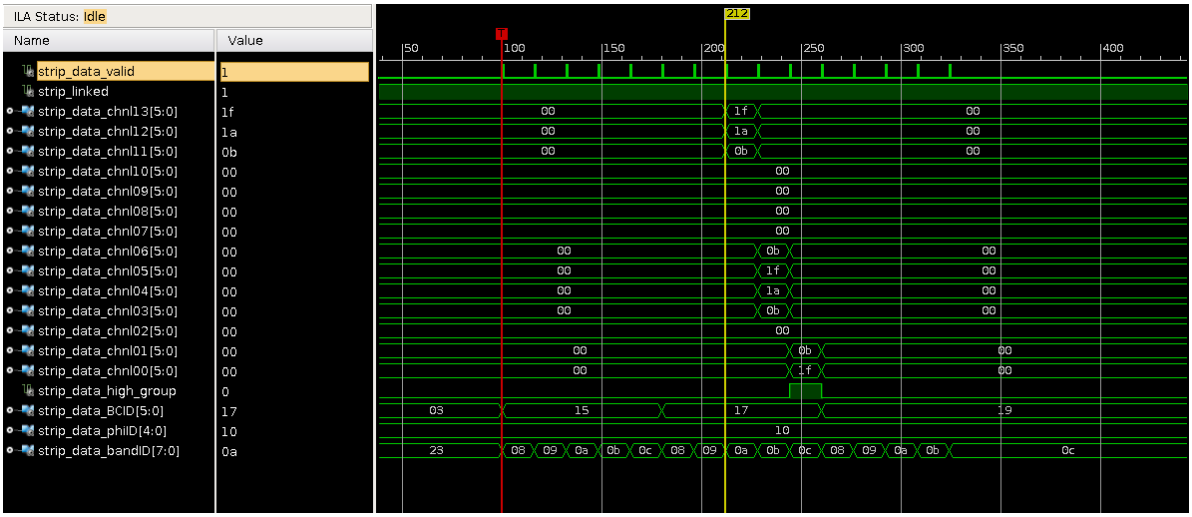


Figure 7.53: Strip TDS data captured by ILA with the multiple Band-IDs triggering.

Figure 7.54 shows the strip hit map with the multiple Band-ID trigger scheme. The hit map is smoother than the measurement using only one Band-ID, with darker bands for the spacers. Figure 7.55 shows the charge-centroid hit map from the strip 6-bit ADC data. This map clearly shows the locations of the spacers.

Figure 7.56 shows the strip cluster charge distribution. The cluster charge is the sum of the ADC numbers of all 6-bit ADC data in an event, and the peak value is around 70 ADC count. Figure 7.57 shows the cluster strip multiplicity distribution. The median number of fired strips per cluster is 4.

Limited by the compatibility of adaptor boards, we could only look at two sFEBs (two layers) at the same time. One more study we performed is the measurement of the 1D projected angular

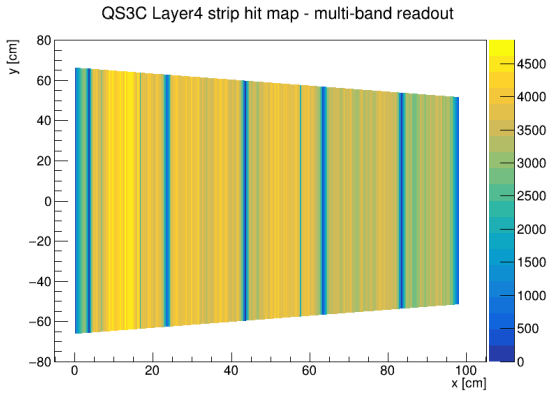


Figure 7.54: Strip hit map with the multiple Band-ID trigger scheme.

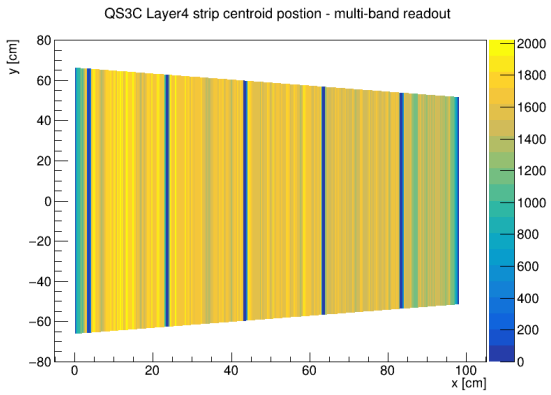


Figure 7.55: Strip charge-centroid hit map with the multiple Band-ID trigger scheme.

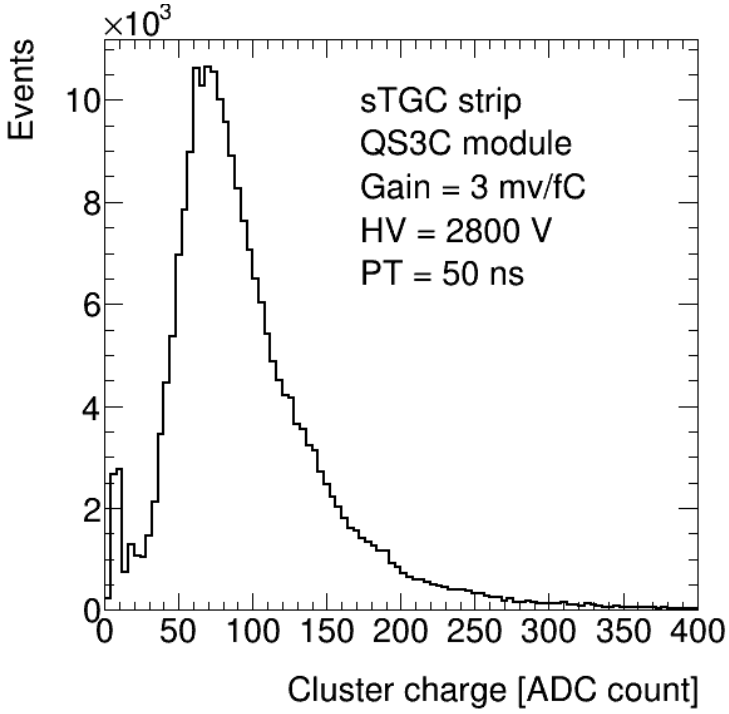


Figure 7.56: Distribution of the strip cluster charge.

distribution of cosmic muons. This measurement uses one KC705 board as the Pad Trigger board to receive data from four pad TDSs, generates and transmits online trigger signals to strip FEBs on layer 1 and layer 4. The mini-DAQ motherboard is used as the Router board that receives the data from strip TDSs from layer 1 and layer 4.

Using the charge-centroid positions along the x-direction on layer 1 and layer 4, the projected

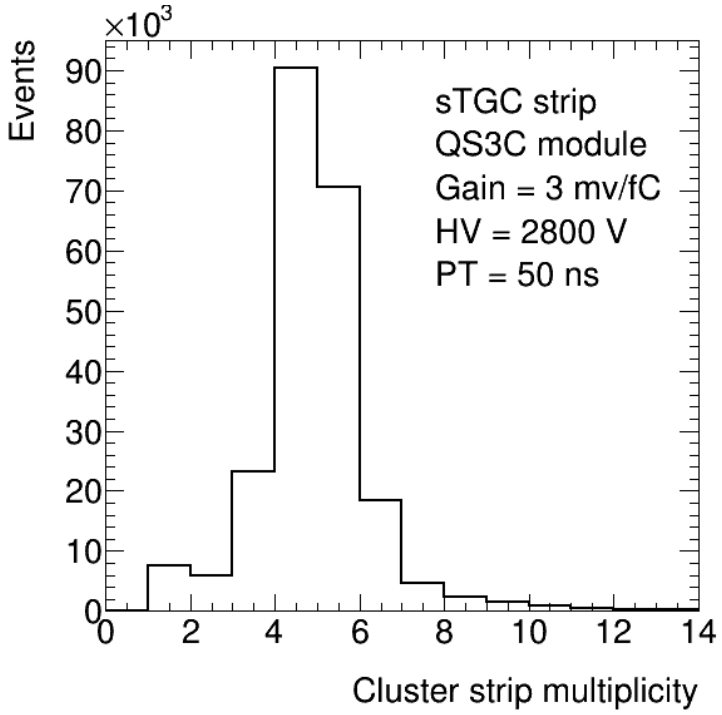


Figure 7.57: Distribution of the cluster strip multiplicity.

incident angle of the muon is calculated as

$$\theta_{\text{1D projected}} = \arctan\left(\frac{x_{\text{L1}} - x_{\text{L4}}}{\text{distance between layer 1 and layer 4}}\right). \tag{7.6}$$

The MC simulation is used with the strip TDS triggering mechanism to provide a reference. Figure 7.58 shows the 1D projected angular distribution between data and the simulation. The data is found to be consistent with the simulation.

This is the first time that the sTGC strip 6-bit ADC data from the detector has been read out. It also verifies the data flow of the sTGC pad - Pad Trigger (FPGA based) - sTGC strip, which is crucial for the future sTGC trigger chain operation.

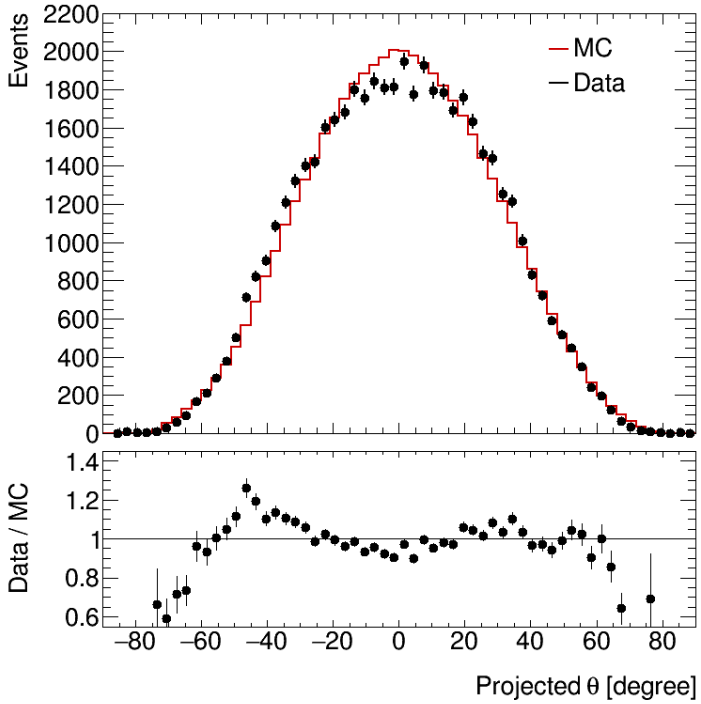


Figure 7.58: The 1D projected angular distribution of cosmic muons measured by sTGC strips in the trigger chain.

CHAPTER 8

The Phase-II Upgrade: MDT Front-end Electronics

This Chapter introduces the current MDT electronics system and the new front-end electronics for the Phase-II upgrade. The new electronics are close to the final stage of R&D.

8.1 Current MDT Electronics

Figure 8.1 presents the electrical services of the MDT tube. The anode wire of the MDT tube is connected to two hedgehog boards in the two ends with capacitors and resistors. On the right side, the high-voltage hedgehog board provides high voltage to the MDT tube with a 383 Ω termination resistor to match the tube impedance. It also has a low-pass filter circuit, comprised of a 470 pF capacitor and a 1 MΩ resistor, that filter the noise with a frequency larger than 500 Hz. On the other side, the signal hedgehog board couples the wire to the mezzanine card with a 470 pf capacitor.

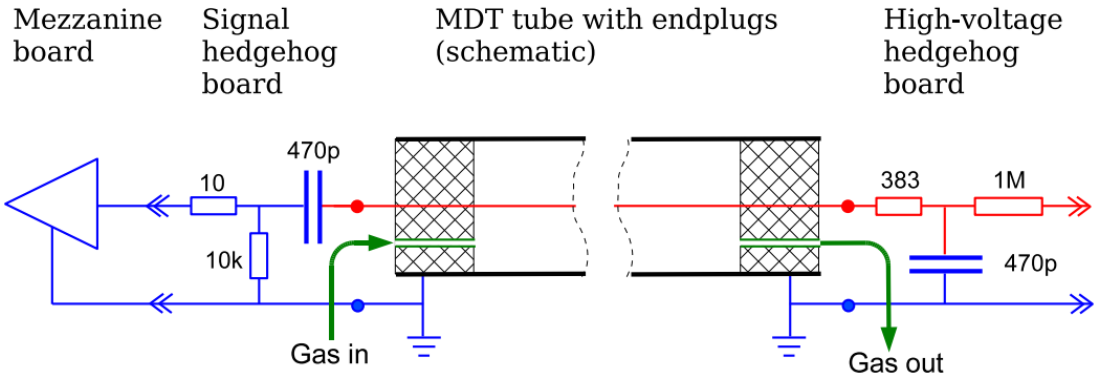


Figure 8.1: Illustration of the electrical services of the MDT tube [53].

Figure 8.2 shows the current MDT readout electronics. The Mezzanine card connects to up to 24 MDT tubes from the signal hedgehog boards. The signals are amplified, shaped, and discriminated by 3 ASD chips. The discriminated signals from these three ASDs are connected to one

TDC chip that digitizes the arrival time of the rising and falling edge of the signals. TDC stores the digitized data in its 256-depth L1 buffer and waits for the L1A trigger signal. Once the trigger signal arrives, the data within the matching window will be transmitted to the Chamber Service Module (CSM) through a 40-pin twisted-pair cable.

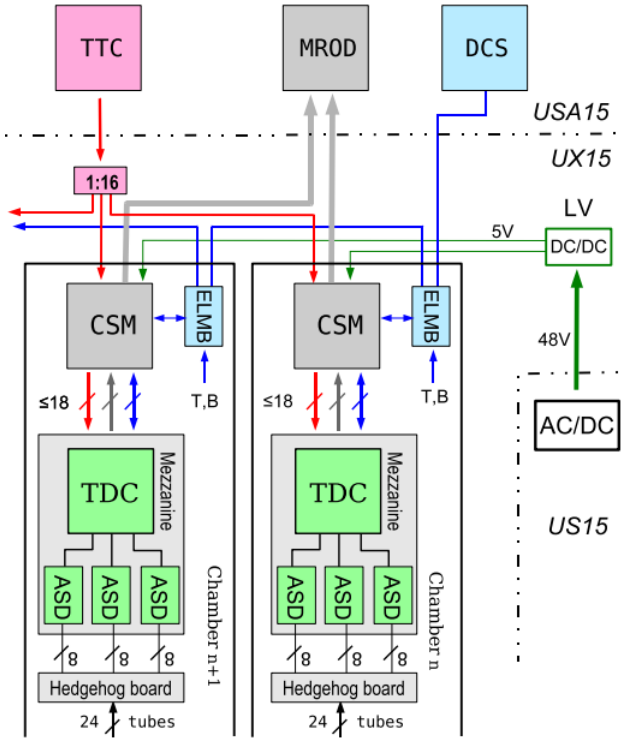


Figure 8.2: The current MDT readout electronics [53].

The CSM collects data from up to 18 Mezzanine cards and forwards it to the back-end MDT Readout Driver (MROD) via a 1.6 Gbps optical fiber link, as presented by the grey line in Figure 8.2. Besides the data path, CSM also distributes TTC control signals (red line), forwards the JTAG signals, and monitors signals (blue line). The Detector Control System (DCS) controls the JTAG information with a serial bus system, CANbus, using the CANprotocal. The Embedded Local Monitor Board (ELMB) is the CANbus node on the chamber that executes the JTAG operations and monitors the temperatures, supply voltage, and magnetic field through various sensors. Figure 8.3 is a photo of the MDT front-end electronics system mounted on an MDT chamber.

8.2 The Phase-II MDT Front-end Electronics

The upgraded MDT front-end electronics will consist of three main parts: hedgehog card, Mezzanine card, and CSM, as shown in Figure 8.4. Since the MDT chamber itself won't be replaced,

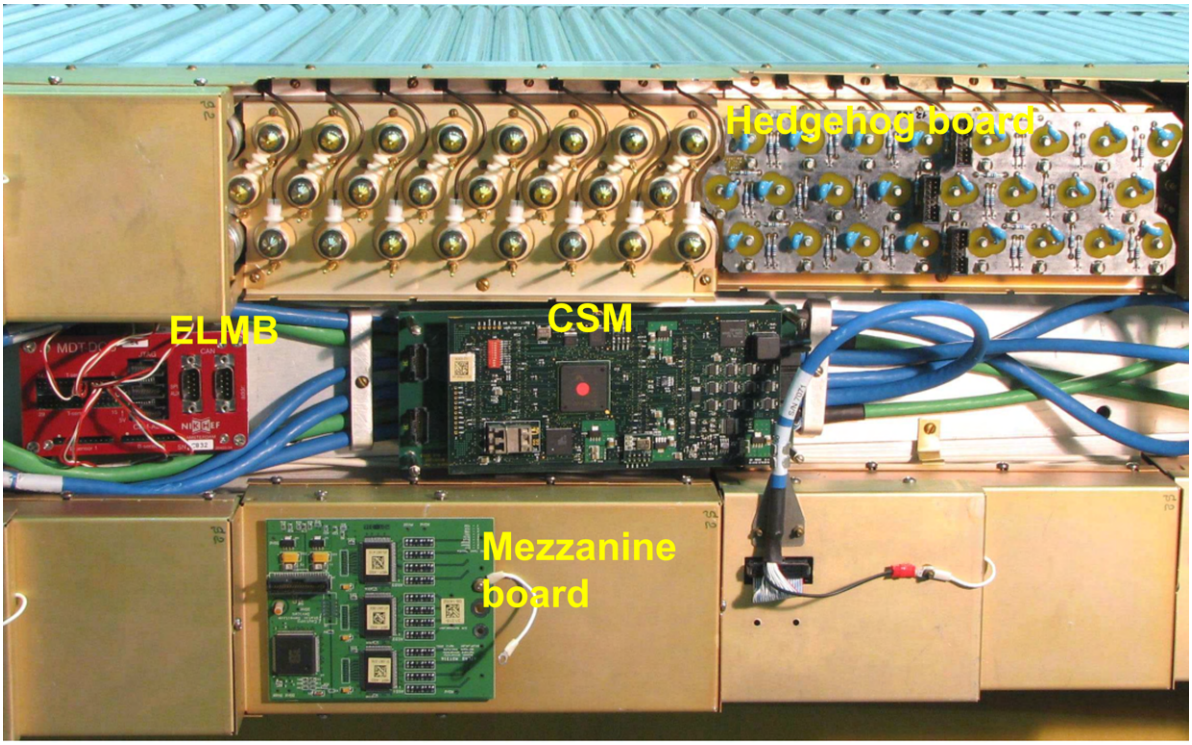


Figure 8.3: Picture of the current MDT front-end electronics mounted on an MDT chamber [53].

the hedgehog cards will be re-used in the Phase-II upgrade. The new Mezzanine card (shown in Section 8.2.2) has a similar structure as the legacy Mezzanine card. It integrates the new ASD (introduced in Section 8.2.1) and new MDT-TDC (presented in Chapter 9) and connects to the new CSM (discussed in Section 8.2.3) with the old 40-pin twisted-pair cable. The new CSM handles up to 18 new Mezzaninces cards with the triggerless TDC data. It also distributes the clocks, JTag configuration signals, TTC signals to the Mezzanine card, and monitors the on-board temperature and voltage information.

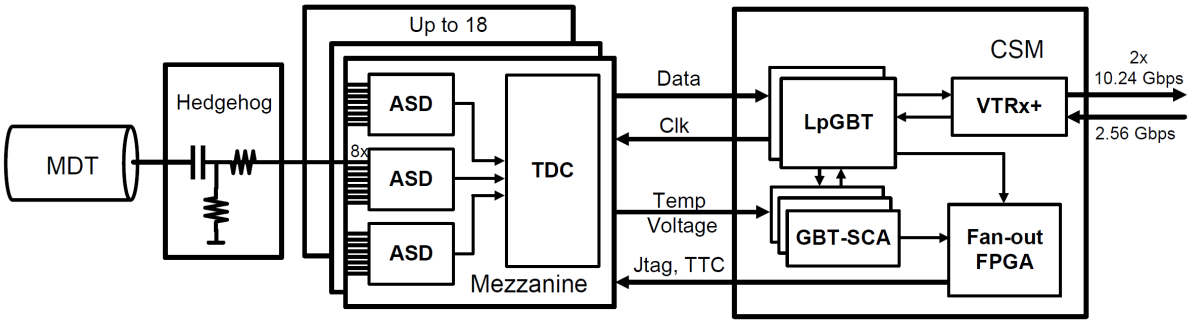


Figure 8.4: MDT front-end electronics for the Phase-II upgrade [107].

8.2.1 ASD

The ASD ASIC, Amplifier–Shaper–Discriminator, is the first stage that processes the MDT analog signals. It was fabricated with the IBM 130 nm CMOS 8RF-DM [108] technology that replaces the old ASD, which used the 0.5 μm Hewlett Packard AMOS14TB process. The new ASD (or ASD2) keeps the same structure as the old ASD but with special efforts to optimize the performance parameters, including gain, peaking time, SNR, and channel uniformity. The structure of the ASD and ASD2 is shown in Figure 8.5.

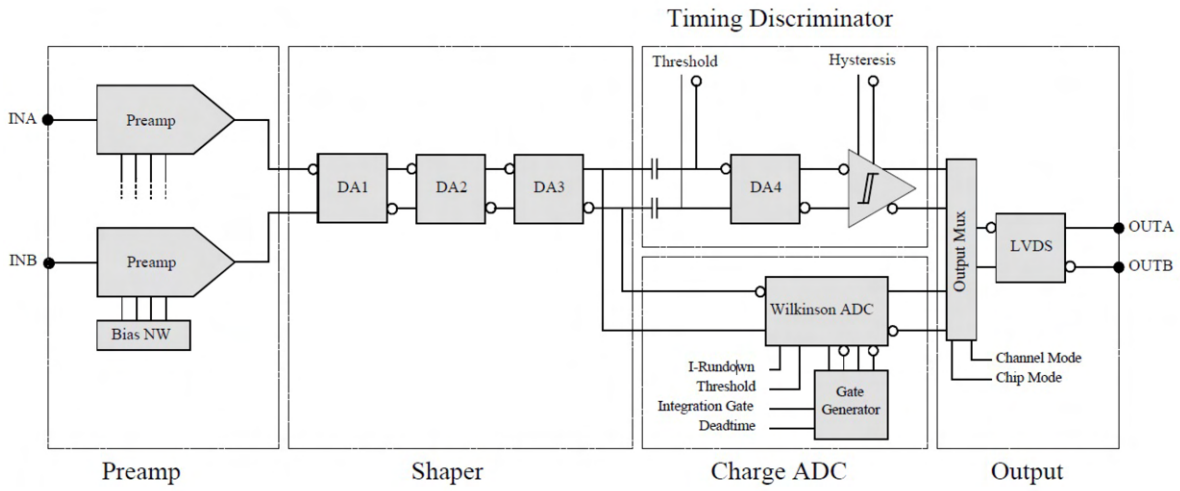


Figure 8.5: Block diagram of the ASD/ASD2 ASIC [99].

The ASD2 consists of five main components in four-stage: the pre-amplifier, the shaper, the timing discriminator, the Wilkinson ADC, and the Low-Voltage Differential Signaling (LVDS) output circuit.

The Charge-Sensing Pre-amplifiers (CSPs) convert the input charge to a pseudo-differential voltage signal by connecting the "dumpy" CSP to the ground. It provides DC balance and common noise rejection. The shaper is composed of three Differential Amplifier (DA), DA1-DA2-DA3. In addition to the gain, the DA1 turns the pseudo-differential signal input to a fully differential signal, and the DA2 and the DA3 implement bipolar shaping, which prevents baseline shift with high background rates.

In the next stage, the discriminator and the Wilkinson ADC provide measurements for the two working modes, the ToT mode and the ADC mode. The discriminator compares the shaped signal with the programmed threshold and outputs the ToT signal. This mode is used to measure the time of the first arrival ionization charge. In the ADC mode, the Wilkinson ADC provides a signal charge measurement by integrating the shaped signal in a given gate window, storing the charge in a capacitor, and discharging the capacitor with a rundown current. Those processes convert the

charge of the signal after crossing the threshold to a digital pulse with the pulse width correlates to the charge amplitude. This ADC mode is mainly used for time slew correction.

At the last stage, The LVDS ouput unit, based on the configuration, outputs the ToT signal or the ADC mode pulse signal with the LVDS standard.

The ASD2 shows a good uniformity with a 3-6 mV channel threshold variation on a chip and a variation of 8 mV among chips [108]. The peaking time is 2 ns shorter than the ASD, which slightly boosts the spatial resolution. A total of 80,000 ASD2 chips (taken into account failure rates and spares) are required for the Phase-II upgrade.

8.2.2 The Mezzanine card

The Mezzanine card is the front-end board that reads 24 MDT tube signals using three ASDs and one TDC. There are four types of Mezzanine cards designed for three kinds of MDT chambers. They are:

- MDT316: Card for the 6-layer MDT chambers with blocks of 3×8 tubes
- MDT436: Card for the first multi-layer of an 8-layer MDT chamber with blocks of 4×6 tubes.
- MDT446: Card for the second multi-layer of an 8-layer MDT chamber with blocks of 4×6 tubes.
- Stack: Card for sMDT chambers with blocks of 4×6 sMDT tubes.

Figure 8.6 presents the overall structure of the Mezzanine card. The new ASD2 and TDC will replace the old ASD and TDC. The MDT tube signals from the hedgehog card are fed into the ASD2 after the high-voltage protection network. The protection network consists of two stages of 20 Ω series resistors with the back-to-back diodes to the ground. The 20 Ω value was chosen to balance the pulse current reduction and series noise [53].

Each ASD2 processes signals from 8 tubes and provides eight LVDS outputs to the TDC. The TDC digitizes the arrival time of ASD2 signals and outputs the timing information to the CSM through two serial links with a data rate up to 640 MHz (two links combined). The configuration of the chips is based on the JTAG protocol. The TDC receives JTAG signals from the CSM and manages the JTAG configuration for the three ASD2, which are connected in a daisy chain.

The Mezzanine card connects to the CSM through the legacy 40-pin twisted-pair cable. The cable's length typically ranges from 0.33 m to 1.33 m and can go up to 5 m if the CSM is installed outside. Those cables will be re-used in the Phase-II upgrade.

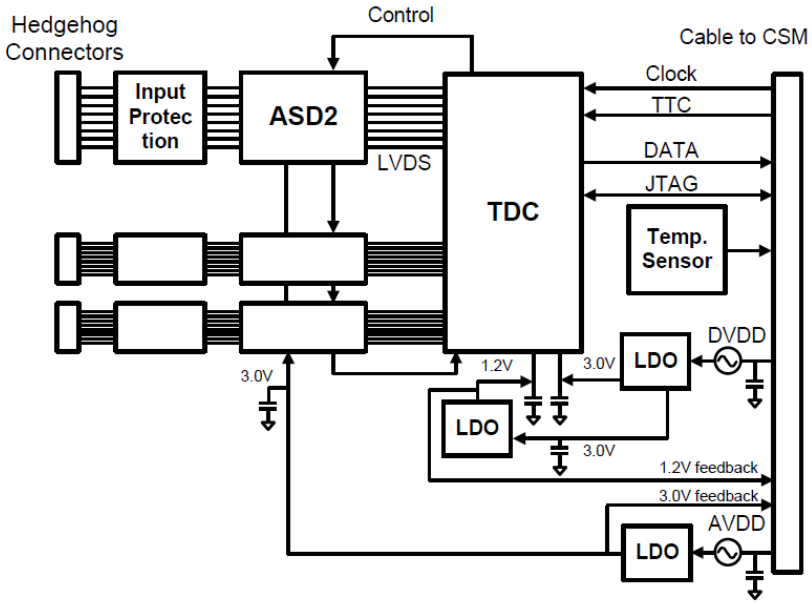


Figure 8.6: Structure of the Mezzanine card for the Phase-II upgrade [107]..

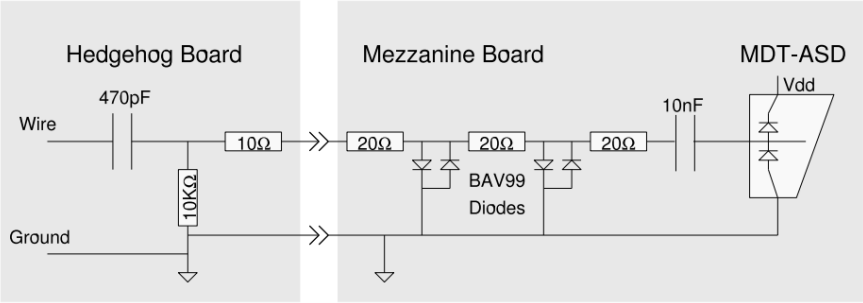


Figure 8.7: The protection network on the hedgehog board and the Mezzanine card that limits the pulse current into the ASD amplifier [53].

The twisted-pair cable transmits the Clock signal, TTC signal, TDC data, JTAG, as well as provides analog and digital power supply (AVDD and DVDD). To reduce noises, digital grounds and analog grounds are separated. One Low-DropOut (LDO) regulator regulates the AVDD at 3.0 V for powering ASD2 (the default power supply for ASD2 is 3.3 V, and the 3.0 V value was chosen to reduce the power consumption). The other two LDOs regulate DVDD at 1.2 V and 3.0 V for the TDC logical and the TDC Input and Output (I/O) power supply. The analog and digital power supply voltages, as wells as the temperature, are monitored by the on-board sensors. Those monitored information are also transmitted to the CSM through the twisted-pair cable.

Figure 8.8 shows the photographs of the legacy MDT316 Mezzanine card and the Stack Mezzanine card for sMDT.

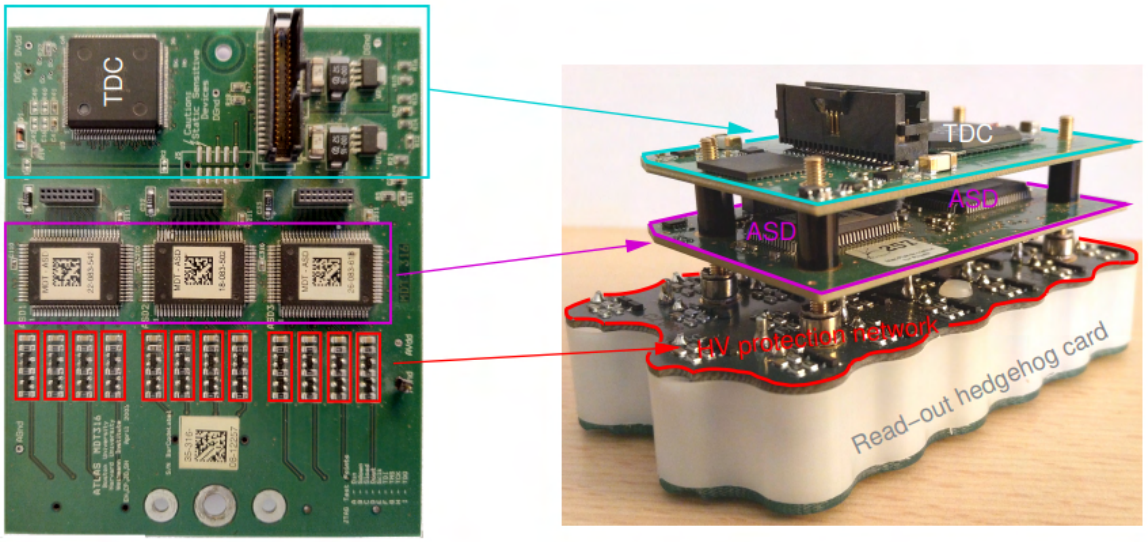


Figure 8.8: Photographs of the legacy MDT316 Mezzanine card (left) and the Stack Mezzanine card (right) for sMDT[109].

8.2.3 CSM

The current CSM, based on Time-Division Multiplexing (TDM), collects the L1 data from up to 18 Mezzanine cards and forwards them to the back-end electronics in the service cavern. It also distributes the control signals and monitors the Mezzanine board status.

In the Phase-II upgrade, this scheme will stay the same, but the data from the TDC on the Mezzanine card will be sent out in a triggerless mode at a much higher data rate. To handle the MDT tube hit rate of up to 400 kHz, the TDS transmission lines will be upgraded to two 320 MHz serial links (the current data rate is 80 MHz with a single line). The new CSM thus needs to handle up to 36 (18×2) links with a 320 MHz line rate.

Another fact to consider for the new CSM is that the current 40-pin twisted-pair cables and CSM motherboards (adaptor board for the twisted-pair to CSM) will be re-used. Some cables are too long to handle the 320 MHz links, which will be configured with a downgraded data rate of 160 MHz. A few Mezzanine cards are not accessible and thus can not be replaced, these Mezzanine card will still be re-used and will provide the data with the legacy 80 MHz link. As a consequence, the CSM needs to be able to handle both 160 MHz and 80 MHz links.

Figure 8.9 presents the architecture of the latest prototype CSM. It is developed on the Low-power GigaBit Transceiver (LpGBT), a data transmission chipset designed for the Phase-II upgrade featuring low-power and radiation-tolerant. Each LpGBT can handle up to 28 of the Elinks with a data rate of 320 MHz. Since there are in total 36 320-MHz TDC links (a total data rate of 11.52 Gbps), the CSM uses two LpGBT chips on-board in the structure of a master LpGBT and a slave

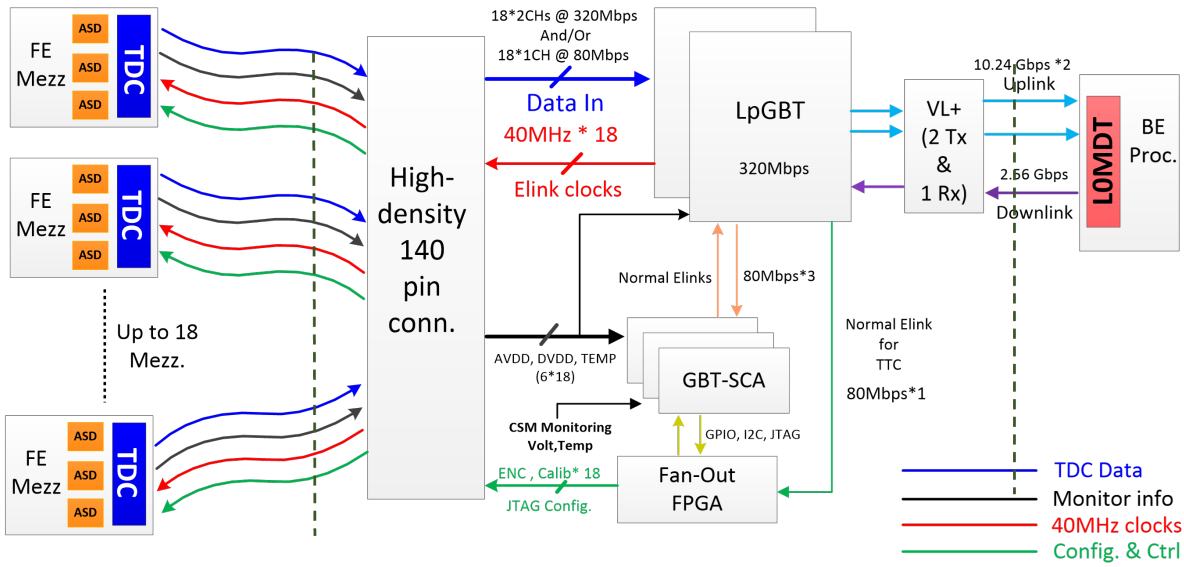


Figure 8.9: The architecture of the prototype CSM [110].

LpGBT to guarantee clock synchronization. The Versatile Link Plus Transceiver (VTRx+) paired with the LpGBTs forms radiation-tolerant optical links to the back-end electronics. The system offers two 10.24 Gbps Uplink and one 2.56 Gbps Downlink.

In addition to forwarding the Mezzanine card output data, the CSM is also responsible for sending control signals to the Mezzanine cards. It uses three SCAs, the same slow control chip used in the Phase-I NSW upgrade, that provides JTAG configuration signals. These configuration signals will be further fan-put by an FPGA, as well as the TTC control signal. The SCA also monitors the Mezzanine card status, such as analog and digital power voltage, temperature sense information, and magnetic field sensor information. Figure 8.10 is the picture of the prototype CSM.

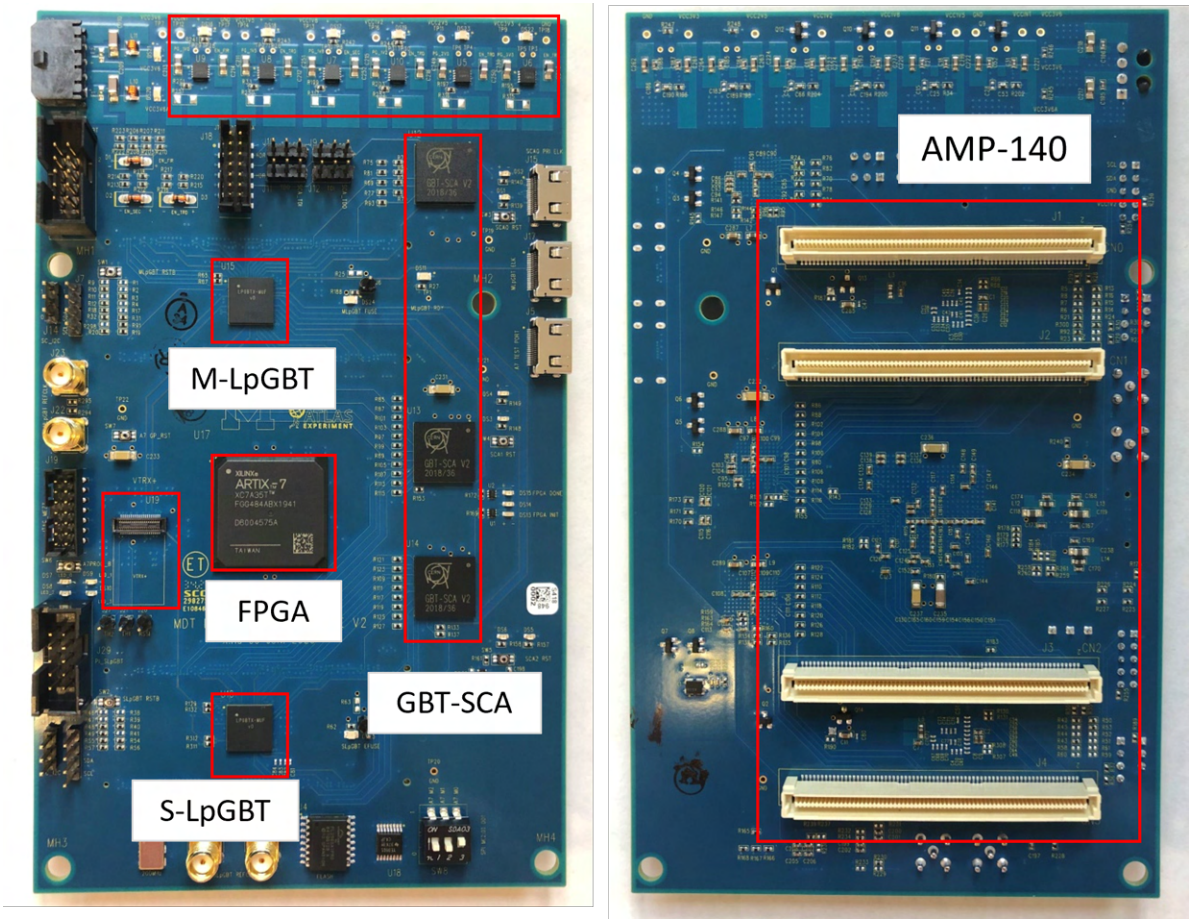


Figure 8.10: Picture of the top side (left) and bottom side (right) of the LpGBT-CSM prototype [110].

CHAPTER 9

The Phase-II Upgrade: Development of the MDT TDC ASIC

The MDT TDC ASIC is a time-to-digital converter ASIC that replaces the current AMT-3 (Atlas MDT TDC) for the MDT system during the Phase-II upgrade. It is responsible for the digitization of the rising and falling edges of the earliest arrival signal after being processed by ASD. This time digitization is the basis for all subsequent trigger and readout processing.

The AMT-3 was fabricated in Toshiba 0.3 μm TC220G CMOS process. It has an LSB of 0.78 ns by dividing the 80 MHz clock into 16 intervals. The 80 MHz clock is produced by an internal Phase Locked Loop (PLL) that doubles the frequency of the 40 MHz LHC BC clock. It determines the arrival time of a detector signal using a fine-time and coarse-time combined method.

The AMT-3 runs in the trigger mode by default, and a trigger signal is required to read out the aggregated data. After the Phase-II upgrade, to reduce unwanted low-momentum muon trigger rate, the MDT system will be added to the first level muon trigger system by providing accurate measurement of the MDT coordinates. The new MDT TDC ASIC will be run in the triggerless mode by default and a low-latency triggerless mode is needed. The legacy trigger mode will be useful for chamber test and commissioning. To handle the increased data rate, the MDT TDC outputs data using two serial links with up to 320 Mbps each instead of the AMT-3 single line of 80 Mbps.

In this chapter, the design of the prototype MDT TDC ASIC will be presented. I was responsible for the design of the time digitization unit and integration of the entire chip. The results from our first prototype run (TDCV1) have been published [111].

9.1 Specifications for the MDT TDC ASIC

Table 9.1 shows the specifications of the MDT TDC ASIC. Following are the requirements listed in detail:

- Each MDT TDC handles 24 channels with dual-edge samplings from three 8-channel ASDs on one Mezzanine card.
- A 781.25 ps bin size, corresponding to a time resolution of $781.25/\sqrt{12} = 230$ ps, is required to maintain a position resolution of ~ 100 μm per tube. The front-end electronic is required to contribute less than 20 μm position resolution, and the average drift velocity is 20.7 μm/ns.
- It has a dynamic range of 102.4 μs to cover the LHC orbit period 89.1 μs (3564×25 ns).
- To maintain uniformity among all channels, the bin size variation is required to be less than 40 ps, and the DNL and the INL should be less than 80 ps (10% LSB).
- The power consumption is required to be less than 350 mW to reduce heat dissipation due to the lack of active cooling for the final MDT system.
- It can be operated under the edge mode, which records the timing of both rising and falling edges, or the pair mode, which records the timing of the rising edge and the pulse width.
- It needs to have both trigger or triggerless working modes.
- The output data rate should be configurable with two lines of 160 or 320 Mbps or one line of 80 Mbps (to be compatible with the AMT-3).

Name	Requirement
No. of channels	24 (dual edges)
Dynamic range	17 bits (102.4 μs)
Bin size	781.25 ps
Integral Non-Linearity (INL)	±80 ps
Differential Non-Linearity (DNL)	±80 ps
Input clock frequency	40 MHz
Max. recommended hit rate	400 kHz per channel
Edge/pair time measurements	Configurable
Output data rate	Configurable: 80 Mbps one line (legacy), 160/320 Mbps two lines
Working mode	Trigger or triggerless
Radiation tolerance	>20 kRad
Power consumption	<350 mW
Fabrication process	TSMC 130 nm CMOS process
Signal level	SLVS

Table 9.1: Specifications of the MDT TDC ASIC.

9.2 The Architecture of the MDT TDC

Figure 9.1 shows the architecture of the MDT TDC. It comprises three main components: ePLL, time digitization units, and the TDC logic unit.

The ePLL receives the LHC 40 MHz BC clock and outputs one 160 MHz clock and two 320 MHz clocks. Twenty-four identical time digitization units digitize the risng and falling edges of the incoming signals. To meet the timing measuerement requirement, the time digitization is broken down into fine-time and coarse-time measurements. The dynamical range is covered by the coarse-time measurement (15 bits with a bin size of 3.125 ns), and the resolution is achieved from the fine-time measurement (2 bits with a bin size of 0.78 ns). The TDC logic reads the digitized data from the time digitization units, packages and buffers the data. It sends out the data either in the triggerless or trigger mode.

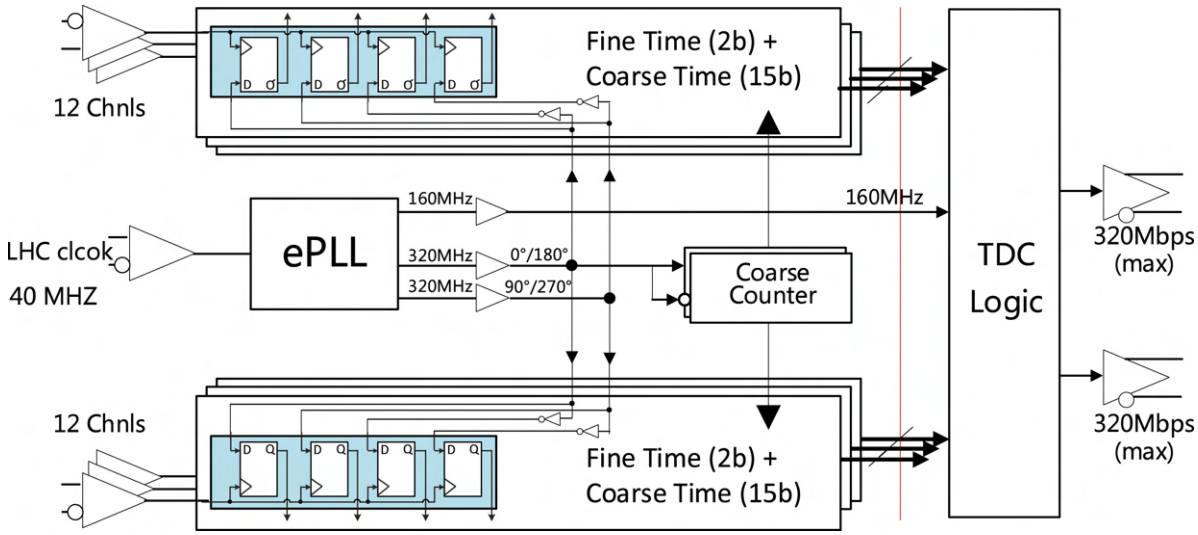


Figure 9.1: Architecture of the MDT-TDC ASIC [111].

A demonstrator TDC prototype (TDCV0) [112] was designed using the Global Foundries 130 nm CMOS process to verify this architecture. The results demonstrated that it satisfies the requirement of the timing measurement. We migrated the design to the TSMC 130 nm CMOS technology and enhanced its performance. Additional features, such as the trigger/triggerless mode, were added to meet the specifications.

9.2.1 ePLL

The ePLL provides clocks for the time digitization units and the logical unit. The quality of the 320 MHz clock directly impacts the timing measurement. The fine-time bin size is correlated to the clock duty cycle and the phase linearity. The ePLL used in the MDT TDC is provided by the

Max-Planck-Institute for Physics and the University of Milan-Biocca group. Figure 9.2 shows the structure of the ePLL.

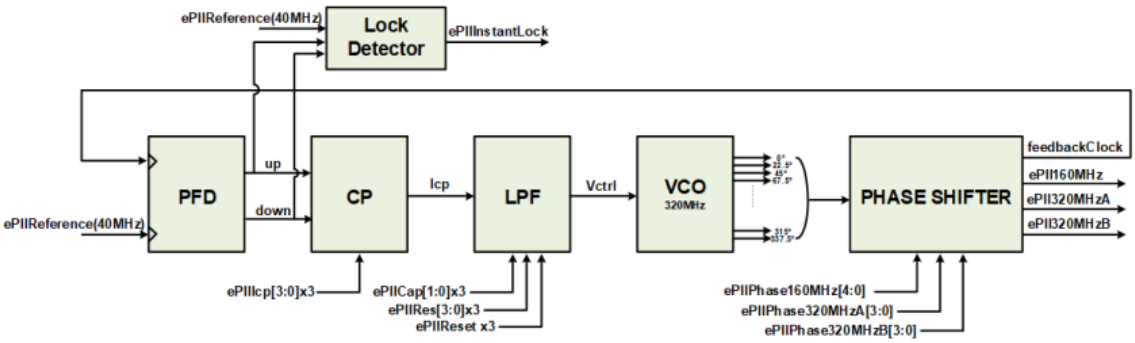


Figure 9.2: The structure of the ePLL [113].

The Phase Frequency Detector (PFD) compares the phase of the 40 MHz BC clock with the feedback clock from the Phase Shifter to generate the up and down signals. Those two pairs of signals control the Charge Pump (CP) to flow or retract a current to the Low Pass Filter (LPF). Therefore, the control voltage to the Voltage-Controlled Oscillator (VCO) is adjusted accordingly.

The VCO cascades eight differential delay cells and provides 16 phases of its oscillating frequency to the Phase Shifter. The Phase Shifter acts as a frequency divider providing a feedback line to the PFD with a divider ratio of 8. Consequently, the desired frequency for the VCO is 320 MHz (40 MHz $\times$ 8). The Phase Shifter also outputs one 160 MHz clock and two 320 MHz clocks with a 195.3125 ps adjustable phase step. Figure 9.3 shows the layout of the ePLL.

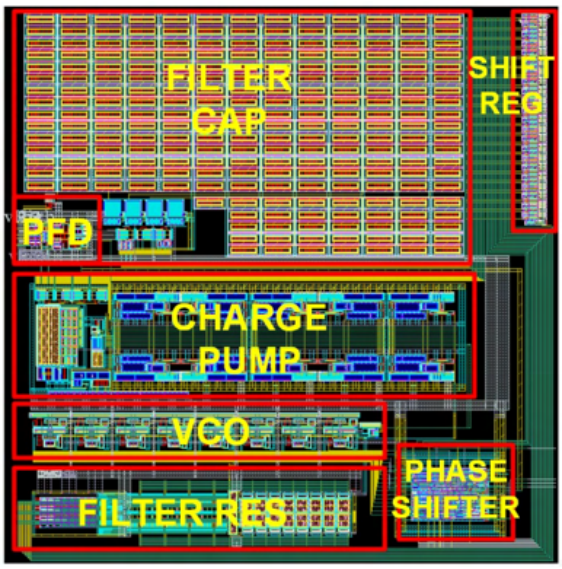


Figure 9.3: Layout of the ePLL [113].

9.2.2 Time Digitization Unit

9.2.2.1 Fine-time and coarse-time sampling

The TDC is required to have a dynamic range of 102.4 μs and an LSB of 781.25 ns, which leads to a 17-bit timing measurement ($\log_2 \frac{102.4\mu s}{781.25ns} = 17$). A naive idea to reach an LSB of 781.25 ns is using a counter running at a rate of 1280 MHz ($\frac{1}{781.25ns}$) to sample the signal. However, a 17-bit counter running with a clock frequency of 1,280 MHz with the 130 nm technology has a tight timing and is not power efficient. Another barrier is that the ePLL is not designed to optimize and output a clock frequency for 1280 MHz. Hence the MDT TDC uses the fine-time and coarse-time combined sampling method similar to the AMT-3.

The 17-bit timing measurement breaks into the fine-time and coarse-time samplings. A digital synthesized counter provides the coarse-time sampling. The fine-time measurement is sampled by a hand-layout multiple clock phases circuit. The more bits the fine-time measurement contains, the more clock phases, routing wires, and circuit complexity the hand-layout sampling circuit will have. The 130 nm technology can handle a 15-bit 320 MHz counter. In the end, a 2-bit fine-time and a 15-bit coarse-time sampling method are chosen.

9.2.2.2 Fine-time Sampling Circuit

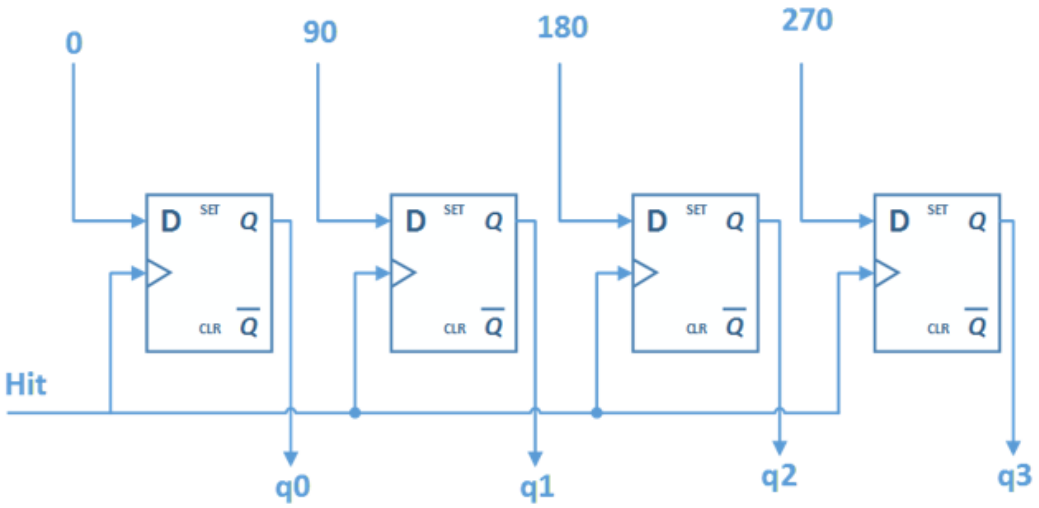


Figure 9.4: Structure of the fine-time sampling circuit.

Instead of sampling the hit signal using multiple phases of clocks, the fine-time sampling circuit use hit signals to sample the clocks. Such scheme avoids clock domain crossing and simplifies the sampling circuit. Figure 9.4 shows the structure of the fine-time sampling circuit. It is composed

of 4 sampling registers. The hit signal is fed into the clock ports of the registers to sample the four 320 MHz clocks with 0°, 90°, 180°, and 270° phases.

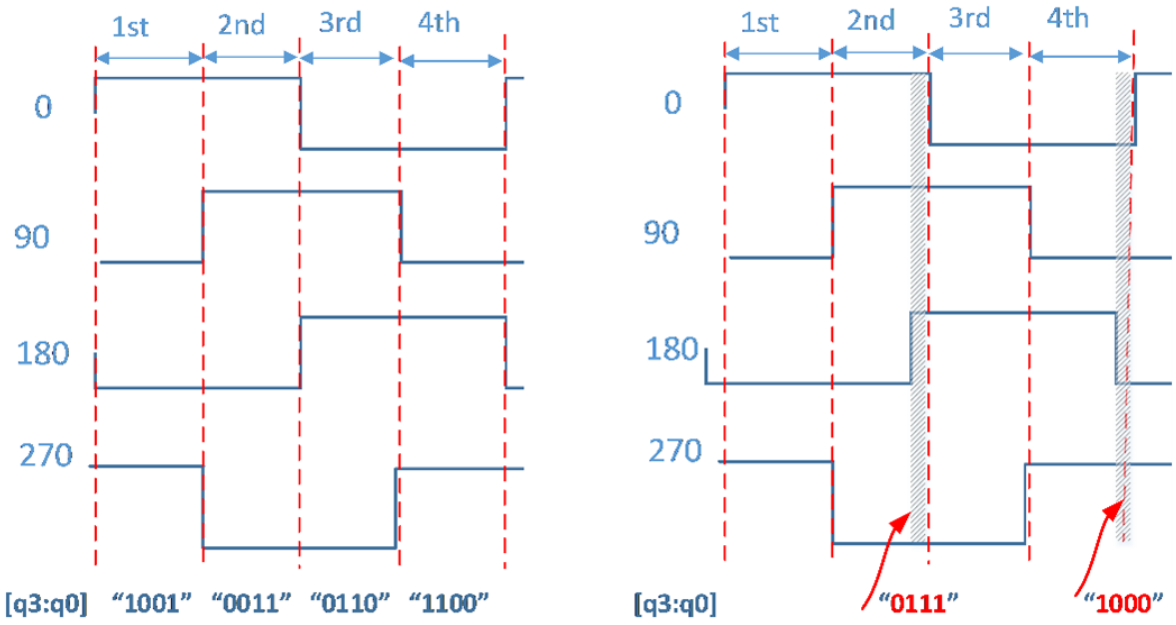


Figure 9.5: The timing diagram presents the fine-time raw coding. Left sub-figure is the ideal case and the right sub-figure is a practical case with unaligned clocks.

Triggered by the rising edge of the hit signal, the sampling registers will sample the status of the four 320 MHz clocks. As presented on the left sub-figure of Figure 9.5, depending on where the hit signal arrives refers to the phase of the 320 MHz clock, the sampled raw coding, $q_3q_2q_1q_0$, are "1001", "0011", "0110", and "1100". They will be decoded to the four fine-time bins (in binary), "00", "01", "10", and "11", respectively.

However, this is an ideal case. In a real circuit, the phase of the four 320 MHz clocks won't align perfectly, and the duty cycle of each clock is not exactly 50%. When the hit arrives around the edge of the clocks, meta-stability happens and unwanted raw coding will occur. Marked by the grey area on the right sub-figure of Figure 9.5, an unwanted raw coding "0111" occurs at the edge of the 2nd bin and 3rd bin. This raw coding could be either categorized into the 2nd bin or 3rd bin.

Table 9.2 is a correction table that corrects the meta-stability raw codings. At the first edge (left side of the first bin), the 90° and 270° phase clocks are stable while the 0° and 180° phase clocks are transiting. Therefore, the raw bins q_0 and q_2 are unstable. Table 9.2 also presents all four possible cases in this edge. The first three raw codings, "1001", "1101", and "1000" are encoded to fin-time bin "00". The last raw coding, "1100", is naturally the raw coding for the previous fine-time bin "11". This is equivalent to both 90° and 270° phase clocks being delayed. The same coding strategies are applied to other edges.

		q_3	q_2	q_1	q_0	Correction	Encoded fine-time (binary)
1st edge	raw	1	0	0	1	1001	00
	meta	1	1	0	1	1001	00
	meta	1	0	0	0	1001	00
		1	1	0	0	1100	11
2nd edge	raw	0	0	1	1	0011	01
	meta	1	0	1	1	0011	01
	meta	0	0	0	1	0011	01
		1	0	0	1	1001	00
3rd edge	raw	0	1	1	0	0110	10
	meta	0	0	1	0	0110	10
	meta	0	1	1	1	0110	10
		0	0	1	1	0011	10
4th edge	raw	1	1	0	0	1100	11
	meta	0	1	0	0	1100	11
	meta	1	1	1	0	1100	11
		0	1	1	0	0110	10

Table 9.2: Default fine-time correction table.

The performance of the sampling register is crucial for the fine-time sampling circuit. With a short setup and hold time, a fast register can reduce the meta-stability region to minimize the variation of the bin size. The True Single Clocked Latches (TSPC), presented in Figure 9.6 (a), was used in the demonstrator prototype design. It consists of two dynamic latches and provides fast sampling. Its performance met the requirement from the test result. However, the bias of internal nodes will drift over time, especially if the states of the latches stay too long. With the millisecond-level hit interval, the sub-threshold leakage plays a non-negligible role.

In the new design, we further optimized the register by replacing the slave dynamic latch with a static latch, using the Pulse-Triggered Register (PTR) structure as shown in Figure 9.6 (b), to reduce the power consumption. The state of the static slave latch will be locked until the next hit signal to avoid bias drifting, whereas the master dynamic latch still offers fast sampling.

A post-layout simulation was carried under different technology process corners to evaluate the performance of the fine-time sampling circuit. Figure 9.7 presents the result under the typical corner. As expected, there are few meta-stability bins in the raw fine-time coding. After corrections applied, presented in the green bar, the four fine-time bins are close to the designed 781.25 ps. The bin size variation among all tested corners is within 20 ps.

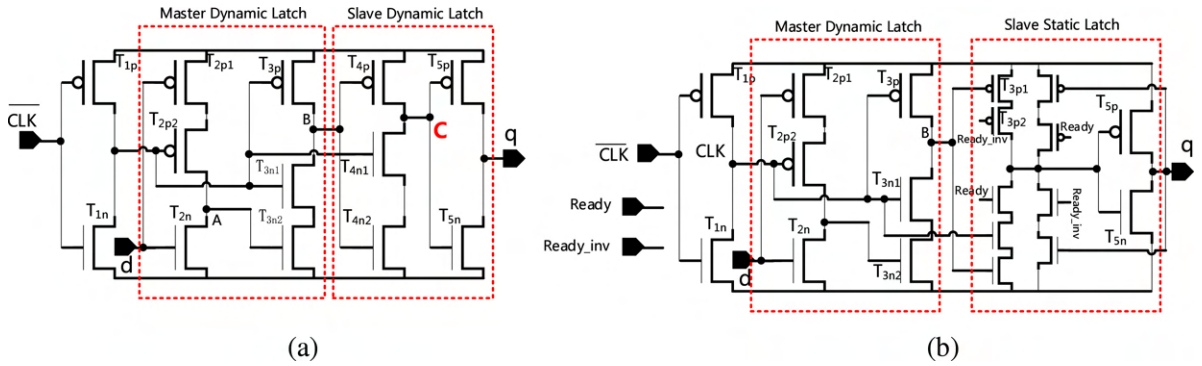


Figure 9.6: Schematic diagram of the sampling register: (a) the True single Clocked Latches (TSPC) used for the demonstrator prototype and (b) the Pulse-Triggered Register (PTR) used for the MDT TDC [111].

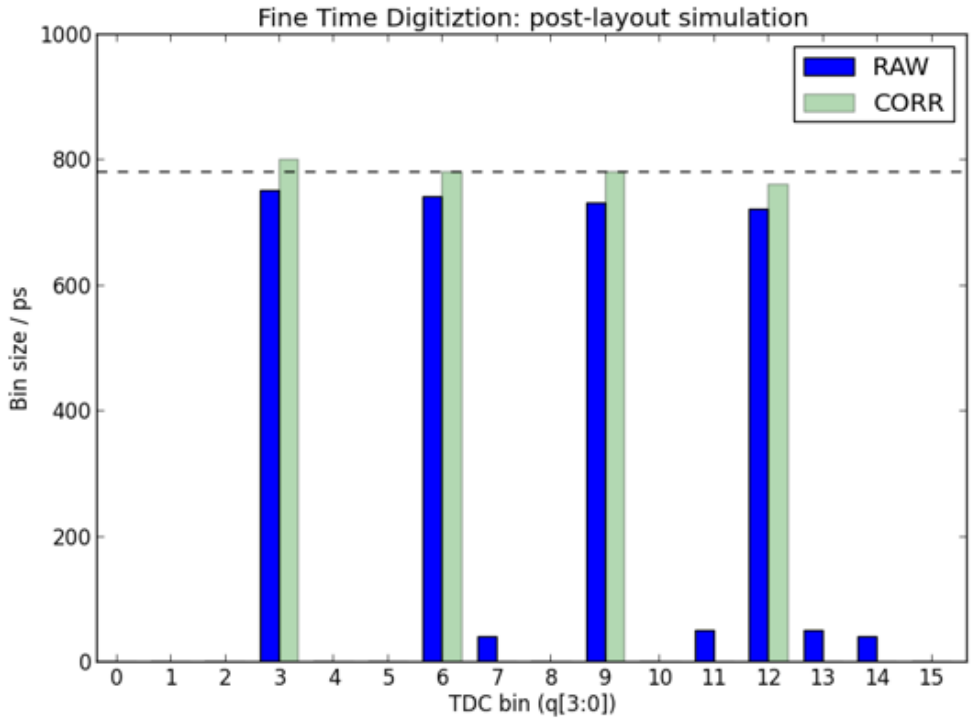


Figure 9.7: Simulation of the fine-time sampling circuit with corrections applied. Correction is applied to the raw codings.

9.2.2.3 Coarse-time Sampling

The 15-bit coarse-time is measured by two 15-bit digital synthesized counters under the 0° 320 MHz clock. As presented in Figure 9.8, the two counters, CNT 1 and CNT 2, are driven by the rising and falling edges of the clock. When a hit arrives, both counters sample the counter values. Only one value is chosen as the coarse-time measurement based on the fine-time result to avoid

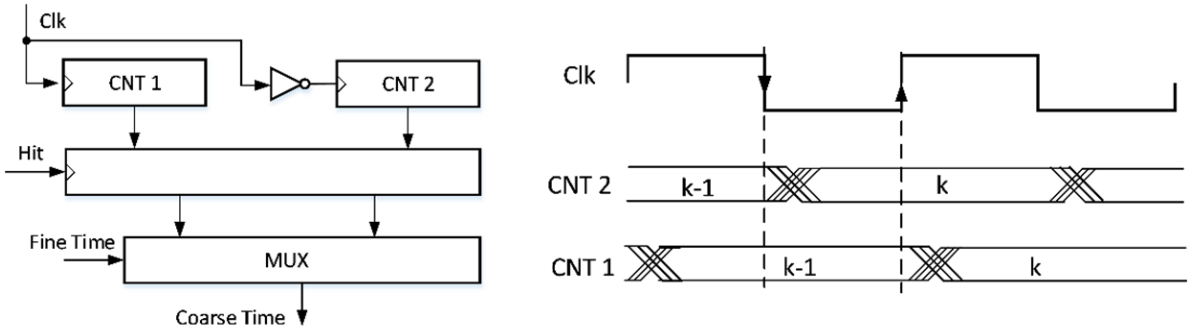


Figure 9.8: Coarse-time Sampling Circuit. The CNT 1 is driven by the rising edge of the clock and the CNT 2 is driven by the falling edge of the clock

meta-stability during the counter transitions.

The counter value of CNT 1 is stable at the falling edge of the clock, while the value of CNT 2 is stable a the rising edge. The CNT 2 is configured to start counting before CNT1. Consequently, if the fine-time bin is “00” or “01”, it means the hit arrives at the first half of the clock period so that the CNT 2 value is chosen. Otherwise, the CNT 1 value will be selected. It is worthwhile to mention that this method requires the counter value to be stable within a half-clock period.

9.2.2.4 Time Digitization of Channels

Each TDC has 24 channels of time digitization circuit, and each channel uses the fine-time and coarse-time combined digitization method. Figure 9.9 is the block diagram of a single channel. It consists of two identical sub-channels that sample the rising and falling edges of the hit signal. The falling edge is measured by inverting the hit signal.

The BCR signal, the 320 MHz clock signal with a 0° phase, and the 320 MHz clock signal with a 90° phase come from the previous channel (or directly from the ePLL) and are cascaded to the next channel. Each channel has its own hit signal injected from external I/O.

The sub-channel is made of coarse-time counters and fine-time digitization circuit. In addition to those main sampling circuits, a supplementary clock tree unit converts the 0° and 90° 320 MHz clock input to 0°, 90°, 180° (inverted from the 0° clock input), and 270° (inverted from the 90° clock input) 320 MHz clock . The clock tree unit is tuned to match the duty cycle and delay among the four 320 MHz clocks. A ready signal generator unit provides a ready signal that informs the TDC logic unit that there is a timing measurement. Figure 9.10 shows the layout of a single channel.

Figure 9.11 presents the simulation result for a single channel that measures an input with a period of 25.01 ns. The measured mean is 25.01002 ns and agrees with the input frequency.

The 24 channels are split into two symmetrical parts, as shown in Figure 9.12. Channel 0 to 11

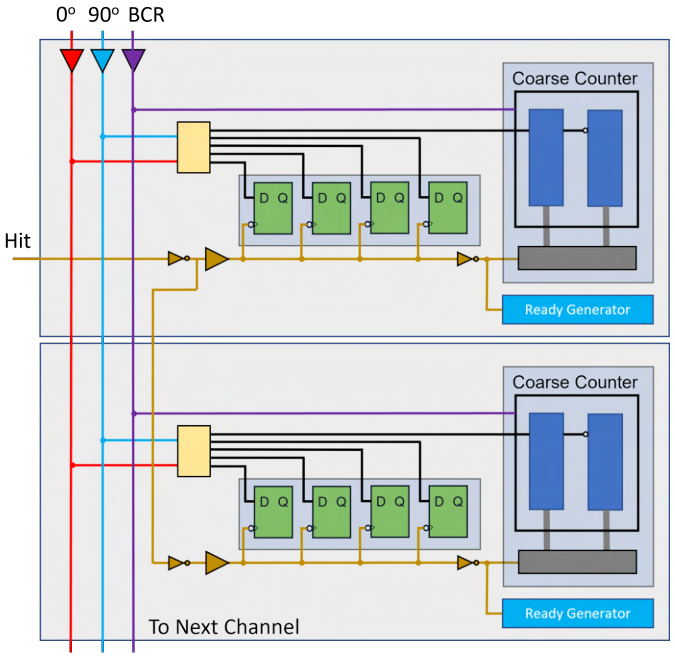


Figure 9.9: Block diagram of the time digitization circuit of a single channel. Two identical sub-channels sample the rising and falling edges of the hit signal, respectively.

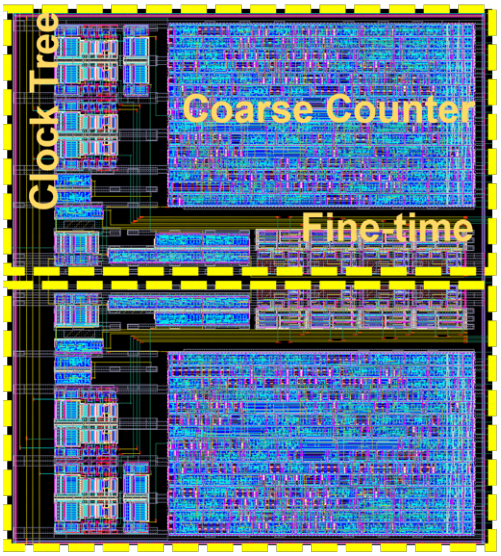


Figure 9.10: The layout of a single channel.

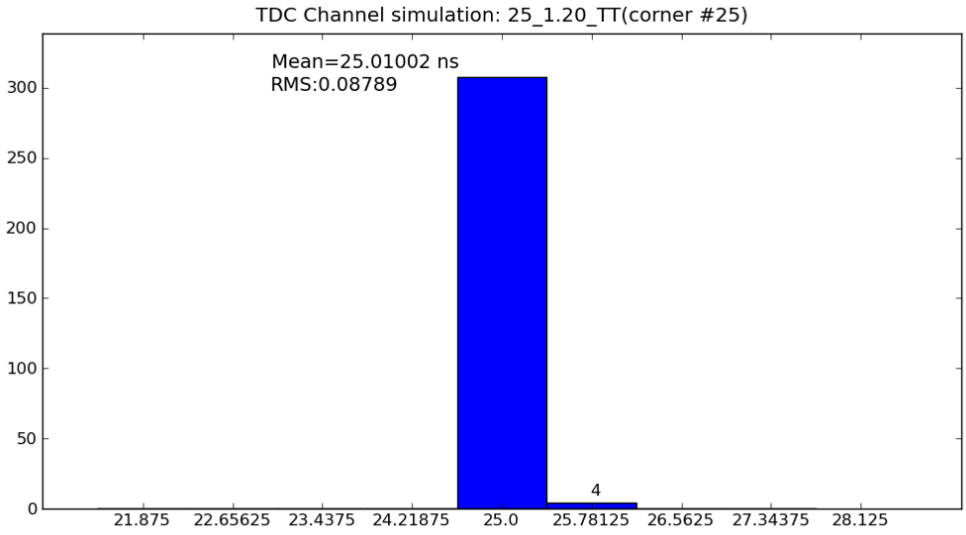


Figure 9.11: Simulation of the timing digitization of a single channel. The input is a clock with period of 25.01 ns. The measured mean value is 25.01002 ns.

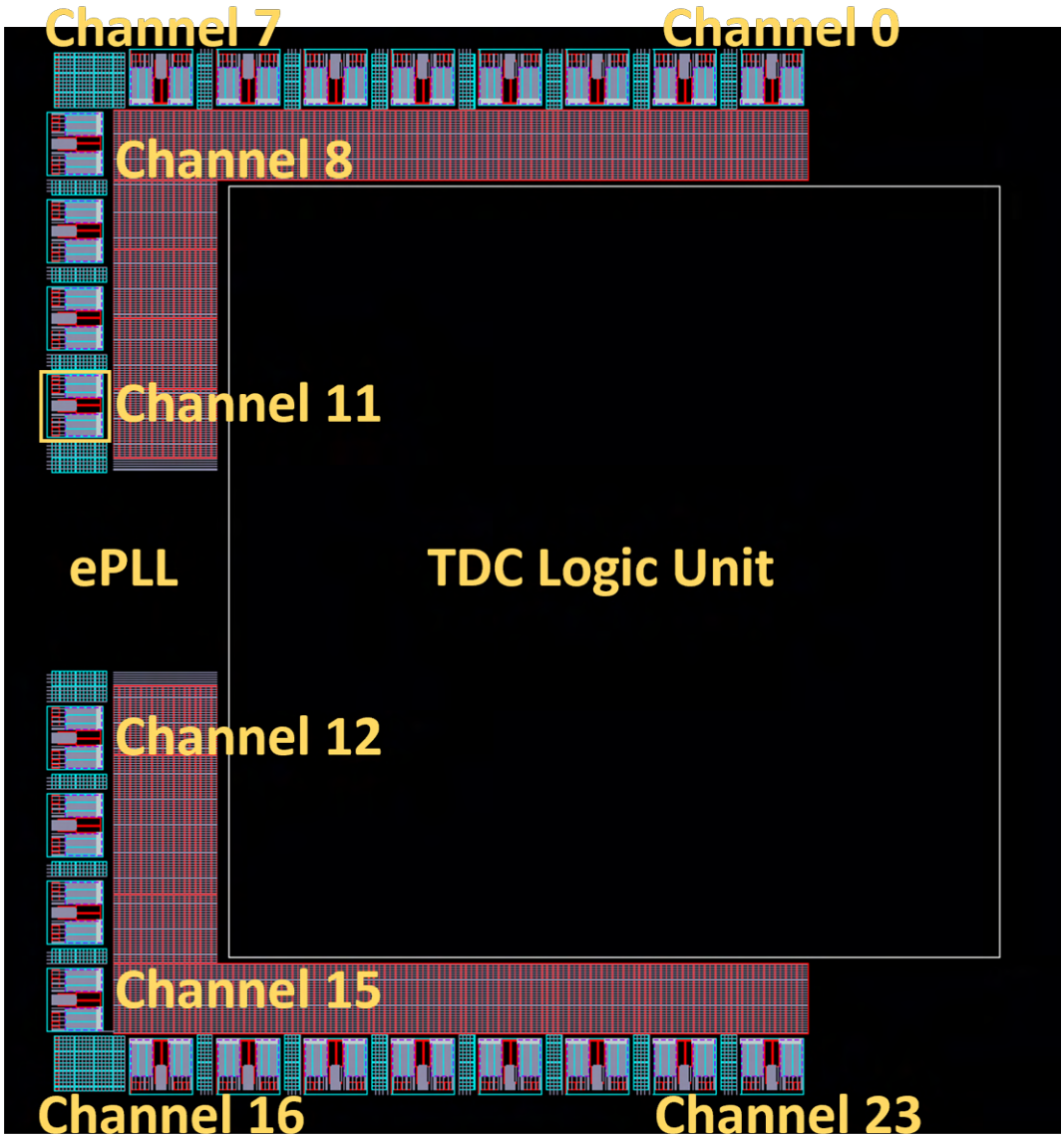


Figure 9.12: Layout of 24 digitization channels

are at the top half of the chip, and channel 12 to 23 are at the bottom half. The ePLL distributes the two 320 MHz clocks to channel 11 and channel 12.

A simulation is performed to check the duty cycle of the clocks in each channel as they are in the daisy chain structure. Table 9.3 shows the duty cycles for the first 12 channels under the typical technology corner. The first channel has a duty cycle of 50.4% while the last channel has a duty cycle of 51%. The net change is (51% − 50.4%) × 3125 ps = 18.8 ps. This is the variation of the bin size compared the channel 11 with channel 0.

	Duty cycle (%)
Input	50.37
Channel 11	50.40
Channel 10	50.46
Channel 9	50.51
Channel 8	50.56
Channel 7	50.62
Channel 6	50.67
Channel 5	50.72
Channel 4	50.78
Channel 3	50.83
Channel 2	50.88
Channel 1	50.94
Channel 0	51.00

Table 9.3: Simulation of the clock duty cycles for 12 channels located on the top half of the chip.

9.2.3 TDC Logic Unit

The TDC logic unit has 24 copies of the channel process module, as shown in Figure 9.13. Starting with the Hit builder, it collects the rising and falling edge measurements from the time digitization unit. Based on the correction table, it corrects the raw fine-time coding and selects which coarse counter to use. In the pair mode, it packages the time of the rising edge with the pulse width. The width is calculated by subtracting the time measurement of the rising edge from the time measurement of the falling edge. In the edge mode, it assembles the measurements from two edges.

Afterward, there are two data paths: the trigger mode data path (solid red lines) and the triggerless data mode path (blue dashed lines). In the triggerless mode, data from the Hit builder are directly fed into the 4-depth Channel FIFO. The Channel Multiplexer writes data from 24 channel FIFOs to the Readout FIFO. The selection is based on the empty and full signals of the Channel FIFOs.

In the trigger mode, data from the Hit builder sits in the 16-depth Hit buffer. Once the trigger signal arrives, the Trigger Matching module performs a timing matching algorithm and writes hits within the trigger timing window to the Channel FIFIOs. The Event building Block reads the Channel FIFO along with the trigger information and builds the event packet to the Readout FIFO.

The data are transmitted out through the Serial interface with two lines of 160/320 Mbps or one line of 80 Mbps (the legacy mode). The configuration of the chip is controlled by the JTAG protocol, and is also capable of configuring three ASDs through the JTGA protocol.

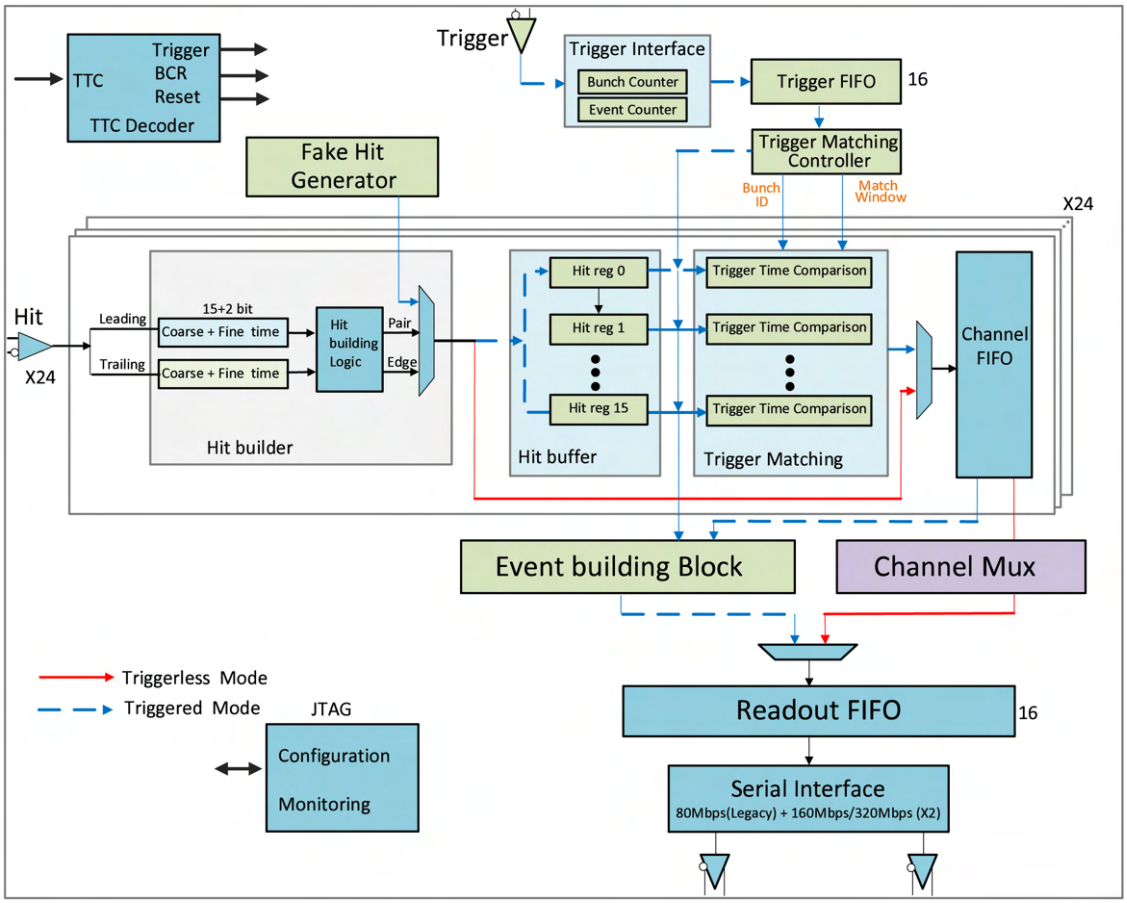


Figure 9.13: Block diagram of the TDC logic unit.

9.2.4 Integration of the TDC chip

Figure 9.14 presents the final layout of the MDT TDC with the time digitization units, the ePLL, and the TDC unit logic integrated. It has a silicon area of 3.7 mm × 3.7 mm and has 136 I/O Pads. At the top right corner, an M logo is made of a few layers of metal, and they are grounded.

The power of the analog circuits (1.2 V), digit logic unit (1.2 V), configuration I/O for TDC (1.2 V - 3.3 V), and configuration I/O for ASD (1.2 V - 3.3 V) are independent. The majority of the signals are differential pairs using the Scalable Low-Voltage Signaling (SLVS) level standard. The JTAG and reset signals are single lines using the Low-Voltage Complementary Metal Oxide Semiconductors (LVCMOS) standard. Details for the I/O Pads are listed below:

- 54 SLVS receiver Pads (24 channel inputs + 1 clock + 1 TTC + 1 BCR);
- 4 SLVS transceiver Pads (2 data lines);
- 7 LVCMOS receiver Pads;

- 4 LVCMOS transceiver Pads;
- 25 Power Pads;
- 30 Ground Pads;
- 7 I/O power Pads;
- 5 I/O ground Pads.

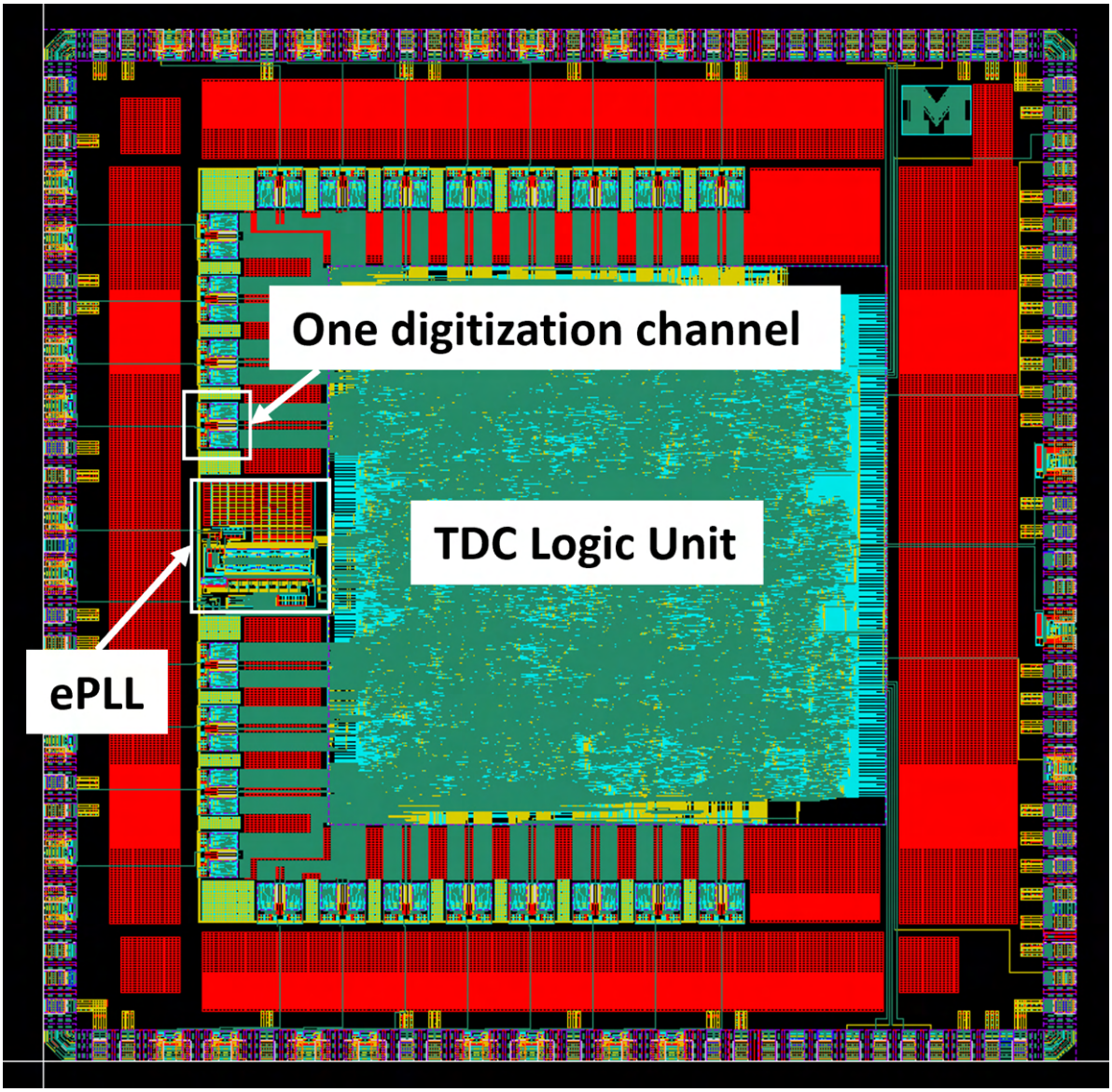


Figure 9.14: Layout of the MDT TDC ASIC (the silicon area is 3.7 mm × 3.7 mm).

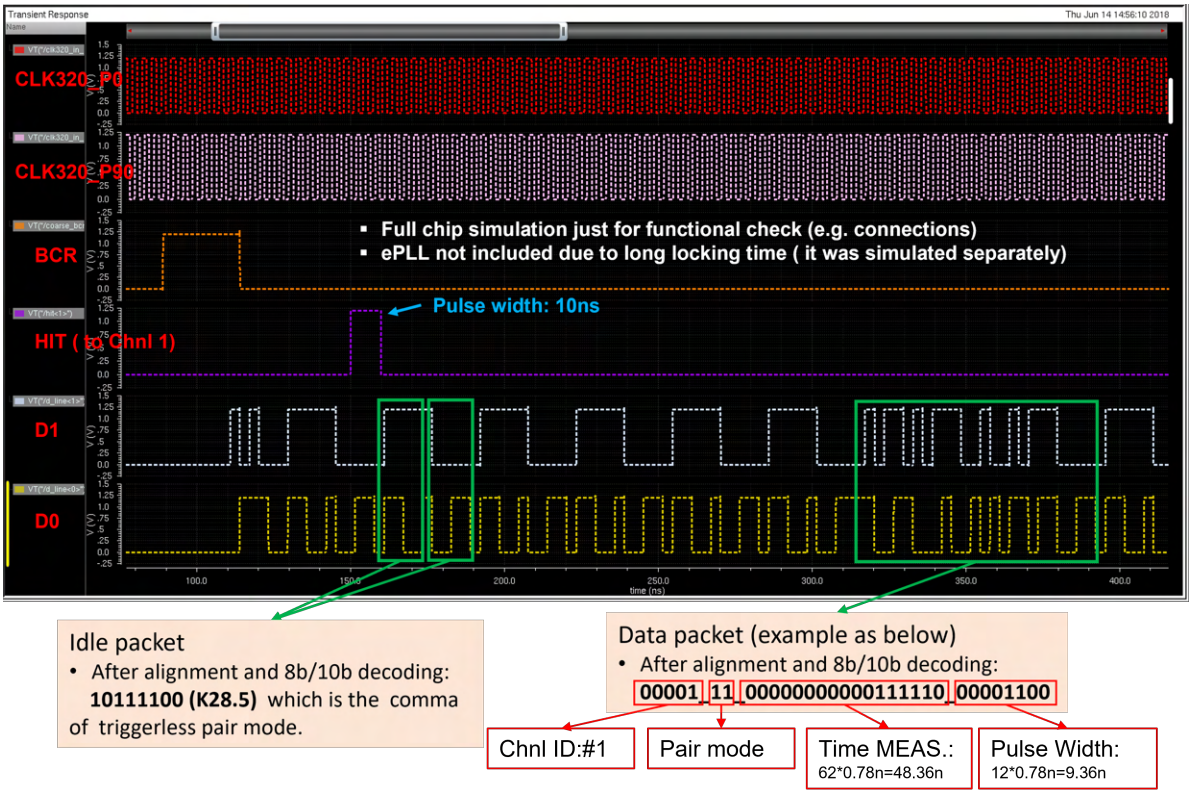


Figure 9.15: Full chip function simulation (time digitization units and logic unit).

A simulation was performed to check the functionality of the time digitization unit and the TDC logic unit. With the complex level of the circuit, the simulation took days to have a waveform result of 2 μs. Hence the ePLL is excluded in this simulation, and ideal clocks are used instead.

Presented in Figure 9.15, after the BCR signal, a hit is injected into channel 1 with a pulse width of 10 ns. Figure 9.15 also shows the output from the two serial data lines with the explanation of the packets after the alignment and 8b/10b decoding. After the BCR signal, the TDC outputs idle packets for the triggerless pair mode (the default running mode). At the time around 310 ns, a data packet is found; at the time aound 48.36 ns, there is a pulse received in channel 1, and the width is 9.36 ns. The result matches with the input.

9.3 Fabrication and Package

The TSMC 130 nm CMOS technology was chosen for the fabrication of the chip. The MDT TDCV1 design (presented in this thesis) was submitted on September 05, 2018, and 100 dies were delivered on November 30, 2018. The 100-pin Quad Flat No-lead (QFN) package, sized by 12 mm $\times$ 12 mm, was chosen and Figure 9.16 presents the die with the QFN package.

The followings are the detail of the 100 pins:

- 1 SLVS clock signal (2 pins);
- 24 SLVS channel inputs (48 pins);
- 2 SLVS data outputs (4 pins);
- 1 SLVS TTC control signal (2 pins);
- 1 SLVS BCR signal (2 pins);
- 5 LVCMOS TDC JTAG configuration signals;
- 1 LVCMOS reset signal;
- 5 LVCMOS ASD configuration signals;
- Others are GND and VDD.

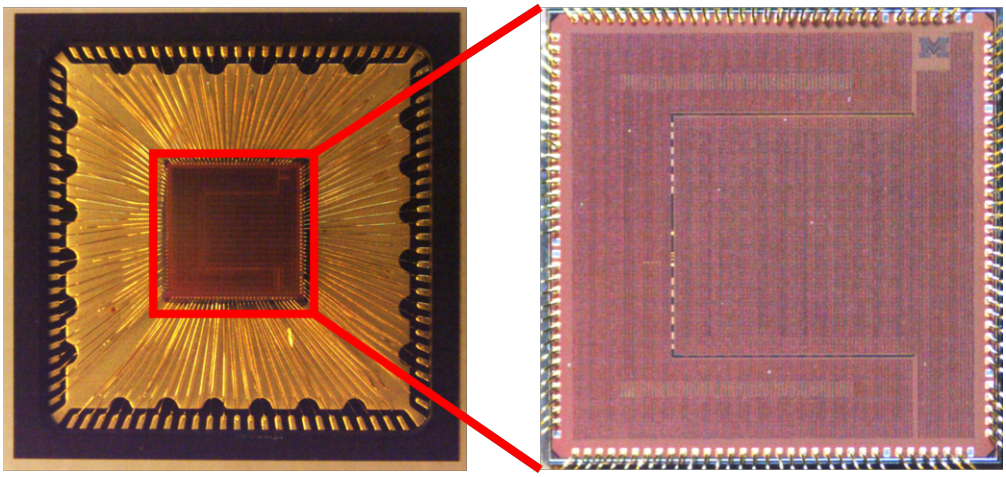


Figure 9.16: MDT TDC die with the QFN100 package [114].

9.4 Design of the Test Board

I designed a test board to study the performance of the MDT TDC. The test board provides flexible input and output options to the TDC, as presented in Figure 9.17. The 40 MHz clock input to the TDC is from an on-board oscillator or an external source through SMA connectors. An FMC (FPGA Mezzanine Card) connector is used to connect to a KC705 FPGA evaluation board. Hence,

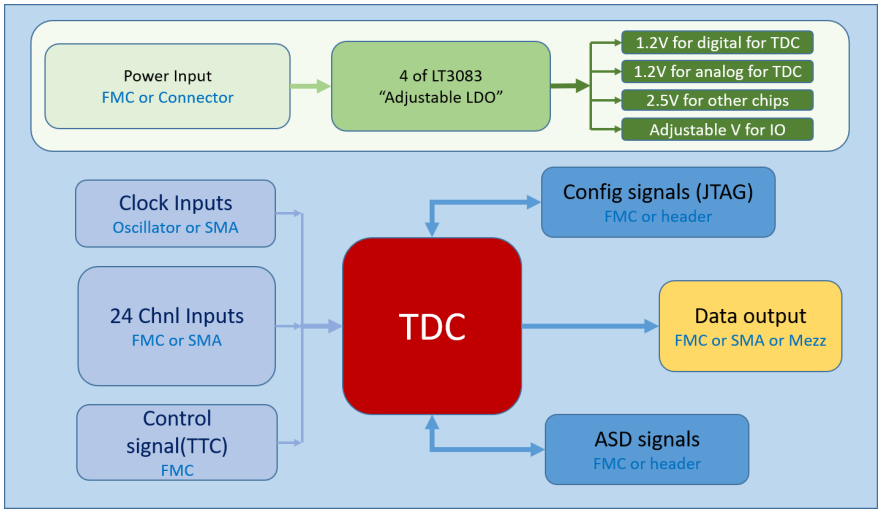


Figure 9.17: Block diagram of the MDT TDC test board [114].

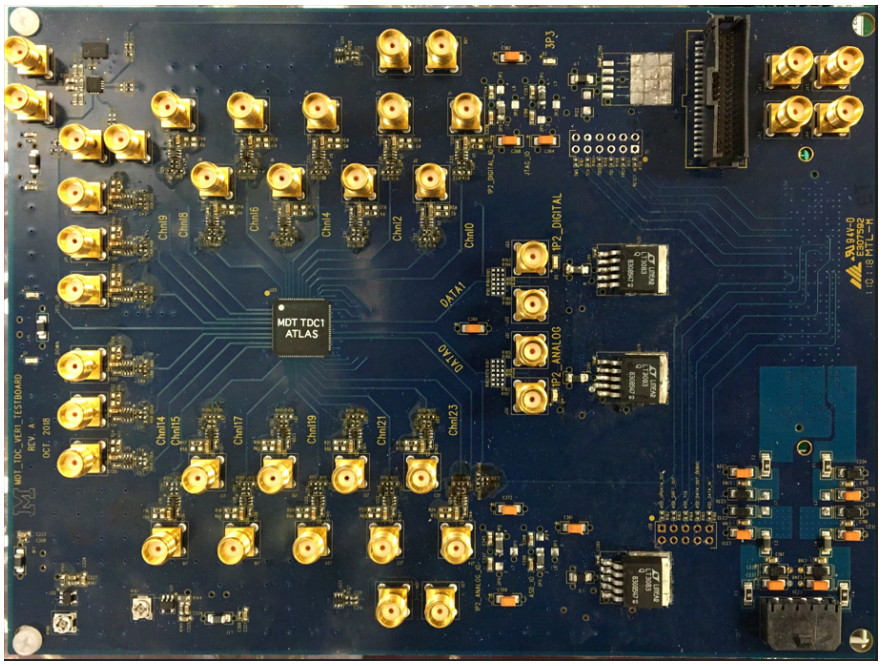


Figure 9.18: A photograph of the MDT TDC test board [114].

the inputs to the 24 channels could be provided either by the FPGA or through SMA (SubMiniature version A) connectors. The FMC connector also distributes other control signals to the TDC.

The JTAG configuration signals to the TDC and the outgoing ASD configuration signals are connected to the FMC connector or header pins. The FMC connector, SMA connectors, or the 40-pin Merzzinane connector can be selected as the output for the two serial data links.

The FPGA evaluation board or the external power supply provides the power to the board. Four

adjustable LDOs (mode LT3083) provide four different voltages to different parts of the boards. They are:

- 1.2 V power supply for TDC logic;
- 1.2 V power supply for TDC analog;
- 2.5 V for on-board chips;
- Adjustable voltage for the TDC I/O.

This board is used to verify the functionality and check the performance of the TDC. It also checks if the TDC is compatible with different I/O voltages. The FMC connector connects to the KC705 FPGA evaluation board during the test. A test firmware was also developed and it can send JTAG configuration signals and emulated hits to the TDC. It can also receive and decode the serial data outputs from the TDC. In addition, the firmware handles the latency test and communicates to a PC server through an Ethernet port. Figure 9.18 is the manufactured test board with the TDC soldered on the centre of the board.

9.5 Performance Results

Figure 9.19 presents the TDC test platform. The test board with the MDT TDC soldered is connected to the KC705 evaluation board.

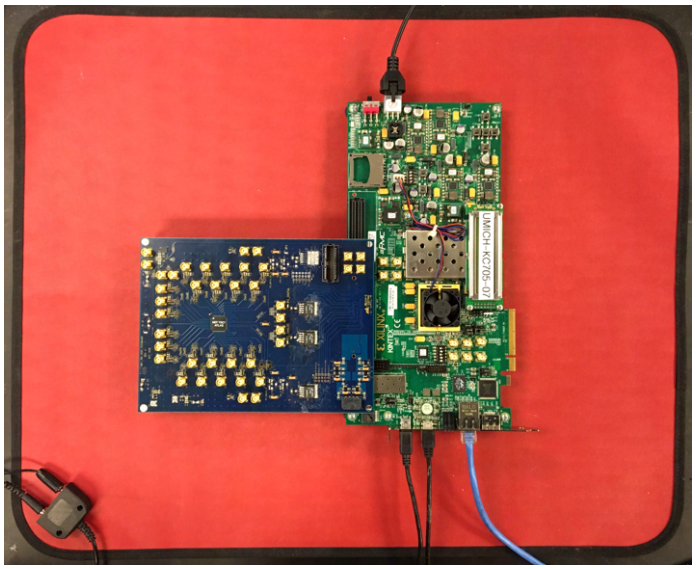


Figure 9.19: TDC test platform [114].

- Fine-time Bin Size

The fine-time bin size is one of the majority performance parameters of the TDC and it is measured by the code density test [115]. The channel inputs to the TDC are provided by the pulsed generated by an oscillator on the FPGA. The frequency of the oscillator is different than the clock of the TDC, hence the density of the fine-time bins in the measurement is linear to the bin size.

Using the triggerless mode, the TDC samples random hits and sends back the measurements to the FPGA. The FPGA then sends the non-idle packets to the PC through the Ethernet port. Further data analysis can extract the density (bin size) of the four fine-time bins. The results are presented in Figure 9.20. Since the TDC has 24 channels and each channel has two sub-channels, so there are in total 48 sub-channels. Among all the 48 sub-channels, the bin variations are within 40 ps (compared to 781.25 ps). The corresponding DNL and INL are less than 6% which meets the requirement of less than 10%.

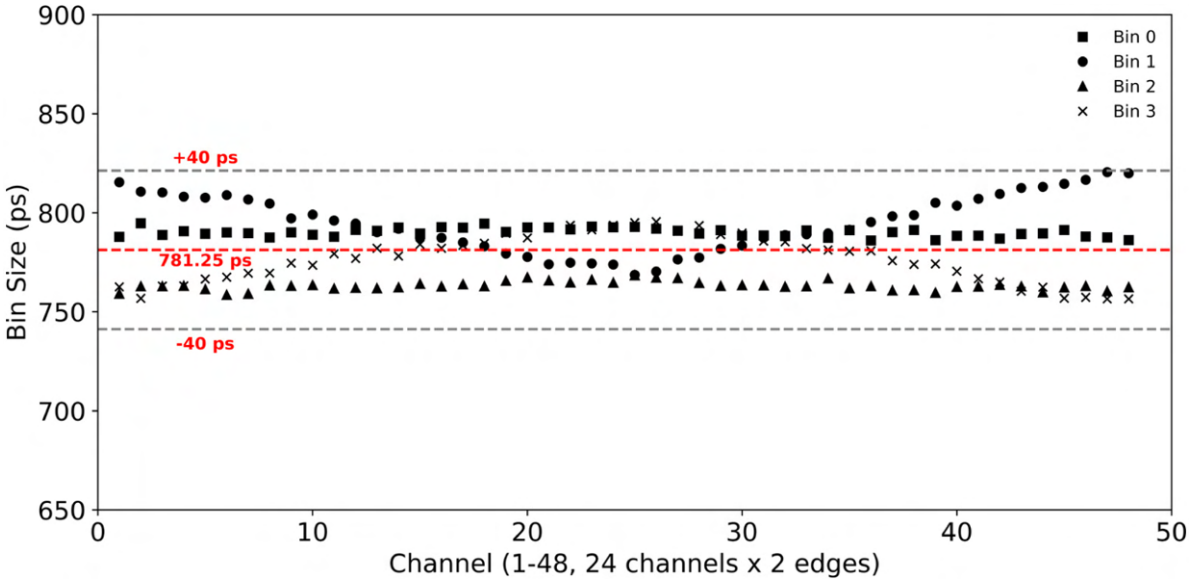


Figure 9.20: Fine-time bin size of the 48 sub-channels.

Bin 0 and Bin 2 have a good uniformity while Bin 1 and Bin 3 are less uniform. The reason is that the 180° and 270° 320 MHz clocks are inverted from the 0° and 90° 320 MHz clocks. The clock buffer used in the clock tree has a slightly shorter delay on the rising edge than the falling edge. The duty cycle would slightly increase after a series of buffering, which is presented in the simulation result in Table 9.3.

- Timing Precision

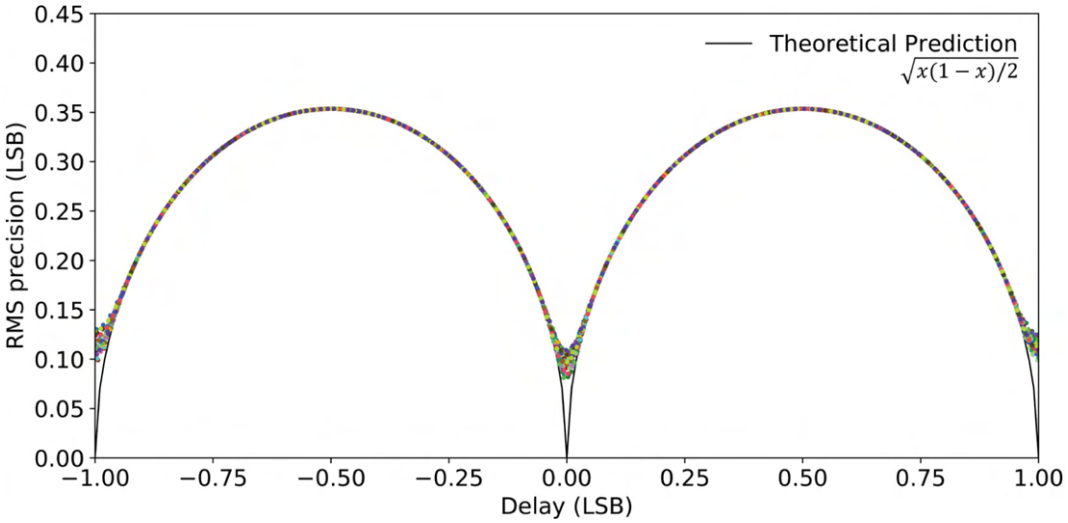


Figure 9.21: The RMS timing precision of the 48 sub-channels.

Another main performance parameter is the timing precision and it is measured by the delay line method [116]. The Mixed-Mode Clock Management (MMCM) IP inside the FPGA is used to provide two signals with different delays to two TDC channels. The RMS precision is the RMS of the interval measurement by the two channels. The theoretical prediction of the precision is $\sqrt{x(1-x)}$ (introduced solely due to quantization), whereas x is the delay in the unit of LSB. Since the two channels have the same structure and are independent of each other, the measured RMS needs to be divided by $\sqrt{2}$ to obtain the resolution for a single channel. The prediction to a signal channel is thus $\sqrt{x(1-x)/2}$. Figure 9.21 presents the RMS timing precision results for 48 sub-channels, and the results agree with the theoretical prediction.

- Triggerless Readout Latency

Since the TDC will be used for the triggerless readout after the Phase-II upgrade, it is important to test the readout latency in the triggerless mode. The latency is defined as the time between when the TDC receives the full hit signal and when the TDC outputs the first data packet. The FPGA generates pseudo-random hits to all 24 channels with a rate of 200/400 kHz. Figure 9.22 presents the latency distribution. With a 400 kHz hit rate (maximum rate expected for future HL-LHC runs), 99 % of the data can be transmitted out after 350 ns. Packet loss test shows that there is no package loss (at least less than 10^{-12}) for 400 kHz/channel with an output rate of 320 Mbps.

- Power Consumption

A 0.1 Ω resistor is connected to the power supply in series with the TDC to measure the TDC power consumption. The voltage of the resistor can be measured, and thus the current to the TDC

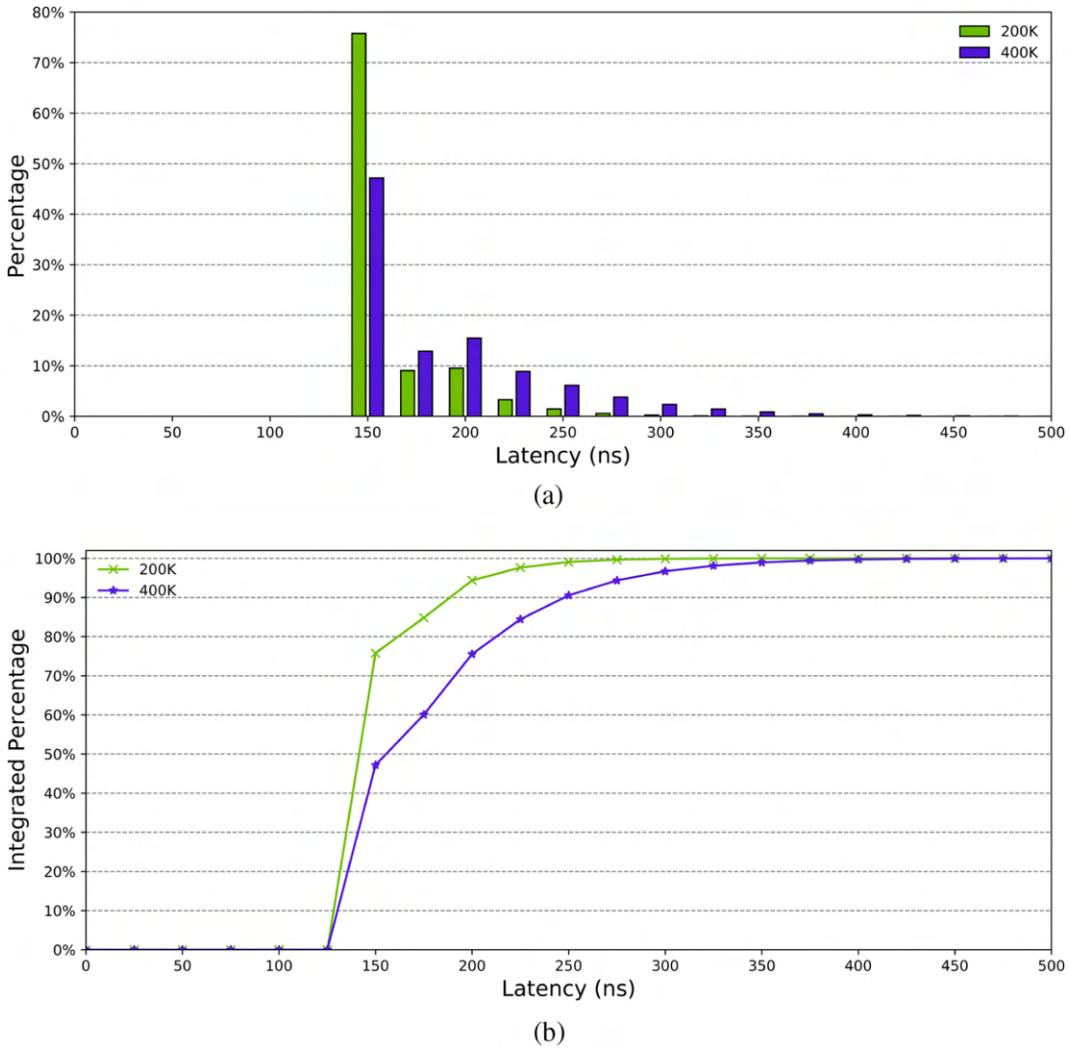


Figure 9.22: (a) Latency distribution with a hit rate of 200/400 kHz per channel. (b) Integrated latency distribution. At 350 ns, 99 % of the data can be transmitted with a hit rate of 400 kHz per channel.

chip can be calculated. The measurement shows that the TDC has a power comsumption of 250 mW regardless of the operating mode. This includes 103.2 mW from the analog circuits and 146.8 mW from the digit unit.

- Summary

The test results indicate the MDT TDCV1 meets the timing performance requirement for future HL-LHC runs. A second version prototype [117], TDCV2, was designed using the same time digitization units and the ePLL but with Triple Module Redundancy (TMR) implemented in the logic unit for radiation tolerance. The MDT TDS is under the final review before mass production.

CHAPTER 10

Conclusion

The LHC will be upgraded to the HL-LHC after the Long Shutdown 3. The instantaneous luminosity will be increased by a factor of ~ 5 and the integrated luminosity will be increased by an order of magnitude. The large dataset will substantially boost the accelerator's potential for new physics discoveries and greatly improve the precision to study the properties of the Higgs boson.

ATLAS plans to have two phases of upgrade for the muon spectrometer for future HL-LHC runs. The Phase-I upgrade will introduce a NSW detector to reduce fake muons found at the first trigger level. The Phase-II upgrade will use the MDT detector also as a trigger device to improve the muon momentum resolution at the first trigger level.

This dissertation presents the design of a mini-DAQ system and its application to the sTGC trigger chain front-end electronics integration and commissioning during the Phase-I upgrade. The mini-DAQ system is composed of FPGA-based hardware and control software. The firmware developed on the FPGA works closely with the front-end electronics featured with multiple (up to 16) 4.8 Gpbs TDS links receiving, Trigger Chain Checker functions, Active Data Readout function, sTGC pad TDS Rate Monitor, and Online Tigger generation. The mini-DAQ software provides control, data collection, automatic test flow handle with the mini-DAQ firmware. The entire system plays an irreplaceable role in the sTGC integration and commissioning task. Our group has successfully integrated and commissioned all 64 sTGC wedges. At the time of writing this dissertation, the NSW detector has been installed inside the collision hall. Extensive work is ongoing to integrate it with the rest of the ATLAS detector.

The dissertation also presents the sTGC cosmic ray study with the mini-DAQ system. As the primary trigger detector for the NSW detector, the sTGC trigger chain is the key to the NSW trigger performance. This is the first time the performance of the sTGC detector has been measured with final versions of front-end electronics. The sTGC pad gives consistent results in the trigger chain with the analog signal measurements. Some measured sTGC pads can reach an efficiency of 97% with an high voltage of 2800 V and a threshold of 30 mV. Regarding the timing performance, 90% of events can be contained within 25 ns under the same condition. For the first time ever, the

sTGC strip charge from the detector has been read out through the trigger chain. The measured angular distribution (projected) of cosmic muons agrees with the simulation. This is the first-ever verification of the sTGC pad - Pad Trigger (FPGA based) - sTGC strip data flow with real detector signals. This dissertation provides a valuable reference for the operation of the sTGC trigger chain such as phase tuning and parameter setting.

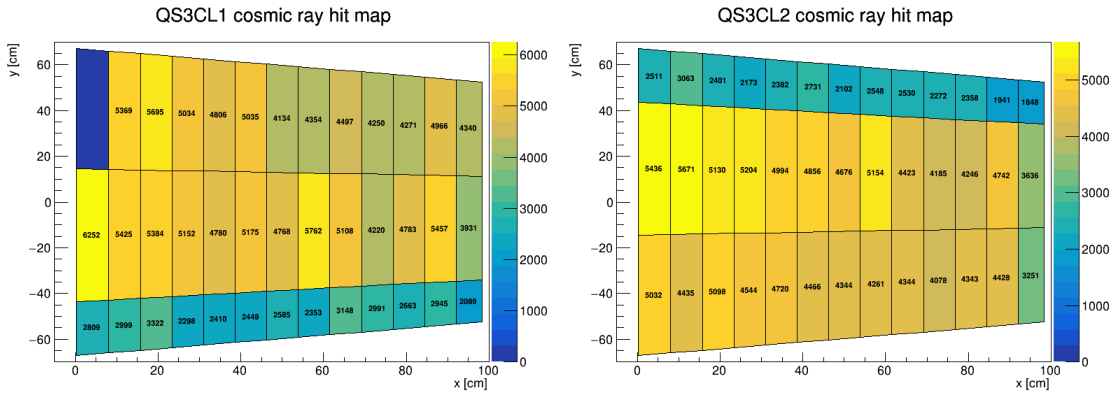
The dissertation also presents the development of the MDT TDC for the Phase-II upgrade. I am the person responsible for the design of the time digitization unit, which determines the timing performance of the TDC. The TDC has 24 channels with an LSB of 781.25 ps. The bin variations are within ± 40 ps, and the DNL and INL are less than 6%. The RMS timing resolution agrees with the theoretical prediction solely induced by bin quantization. The performance meets the specifications for future HL-LHC runs. At the time of writing this dissertation, the MDT TDC is at the final design review stage before mass production.

Some strategies are still left for improvement of the next generation TDC chip. Using more clock phases for fine-time digitization can further divide the fine-time bin size hence improving timing resolution. Using power gating can reduce power consumption by shutting off the current for the logic units that are not used. Using more advanced CMOS technology, such as 65 nm technology, can help to improve the overall performance of the TDC chip.

APPENDIX A

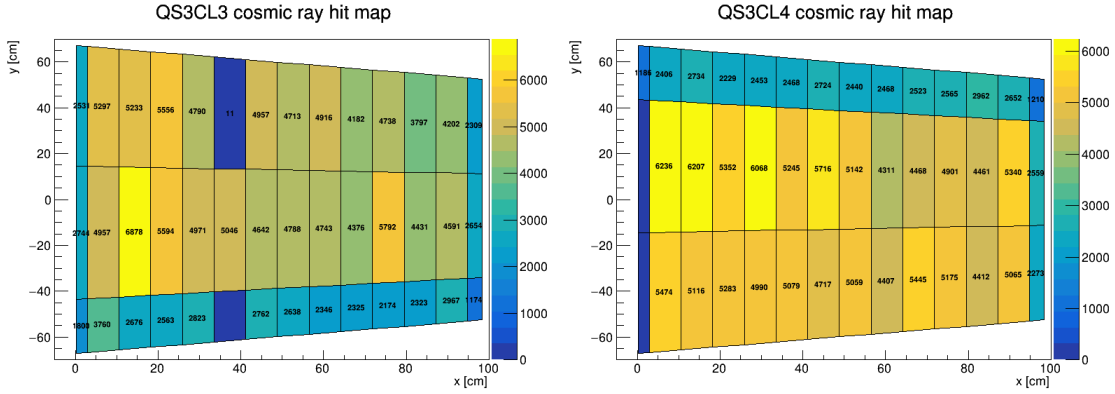
Supplementary Figures

A.1 Unconnected and dead channels on the QS3C quadruplet used for cosmic ray study.



(a) Layer 1.

(b) Layer 2.



(c) Layer 3.

(d) Layer 4.

Figure A.1: Hit map of the four layers of the QS3C quadruplet used for cosmic ray study under 2800 V HV and 50 mV threshold. The number on each pad is the hit count during the test period. The pads with zero or close to zero hit numbers are the unconnected or dead channels.

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