Wide Bandgap Semiconductor-Based Power Converters for Electric Vehicle Applications

by

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Abstract

Wide bandgap (WBG) semiconductor materials allow higher power and voltage, faster and more reliable power electronic devices. These characteristics lead to a massive improvement in power converters, especially for electric vehicles (EV) applications. As a result, new opportunities for high efficiency and power density is coming with the development of WBG power semiconductor. This paper introduces the application of WBG devices in power converters of EV. The EV development trend and the related circuit diagram of an EV system have been introduced. Serval typical power converters' topologies have been discussed. Meanwhile, WBG devices also bring challenges to a high voltage and frequency design. High current and voltage levels need a more powerful heating system. A higher switching speed requires lower loop parasitic inductance. This paper discusses how to apply WBG devices in the power converter design and address these challenges. Finally, The reliability test method of power converters has been discussed. The lifetime of all components in a power converter has been tested under different voltage and temperature levels. The failure reasons and influences parameters are analyzed.

Introduction

Due to an increasing environmental awareness and oil shortage, the EV industry had a huge growth in the past ten years due to a lower CO_2 emission[1-6]. As the International energy agency(IEA) predicted, EVs will contribute to reducing CO_2 emissions by around 30% by 2050. To achieve the proposed target, Industry and academia were keeping trying to improve the performance and efficiency of EVs. An EVs system is mainly composed of three power converters. There are on-board chargers, boost converters, and traction inverters[7-16]. The main power loss of an EV comes from semiconductors in power converters.WBG material semiconductors, especially gallium nitride(GaN) and silicon carbide(SiC), are thought as the most promising alternative to traditional Silicon(SI) devices[17-25].comapred to WBG devices, have higher power and current rate, power density, heating performance and reliability [26-34]. However, WBG devices also bring more critical design challenges. Due to a higher switching speed, lower loop parasitic parameters in both gate drive and power loop are needed in the PCB design. A higher power rate requires a more powerful cooling system A higher working frequency also could cause more critical EMI problems. Meanwhile, how to evaluate the lifetime and reliability of a power converter is also another essential research topic[35-42].In this paper, my research contributes to these challenges will be presented

Chapter 1 Introduction to EV and Power Converters

1.1 EV Development

The EV had a decade of rapid growth in the past ten years. In 2020 the global EV stock had hit 10 million marks. Battery electric vehicles accounted for 66% of EV sales, as shown in figure.1. European and China shows faster growth than other areas, as shown in the figure.2

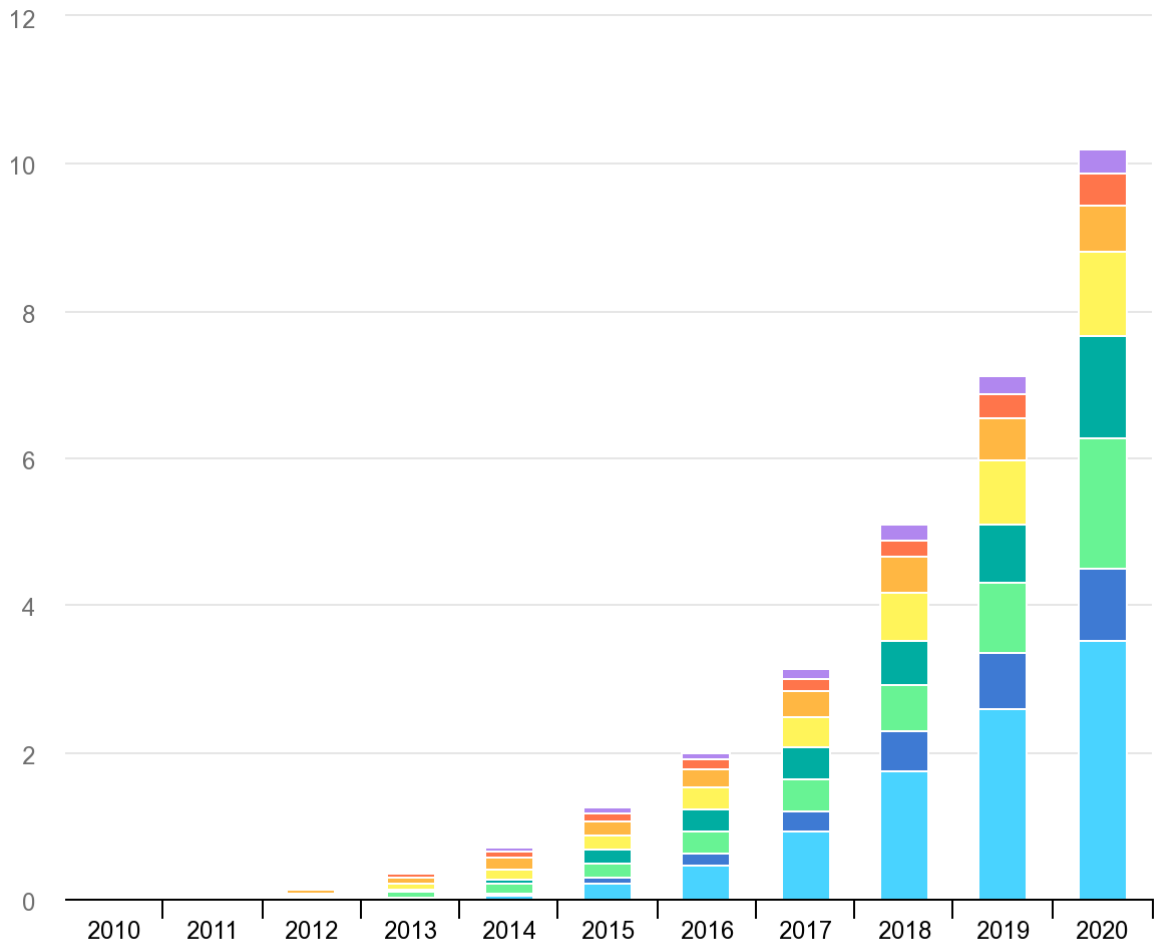


Figure 1 Global EV car sales

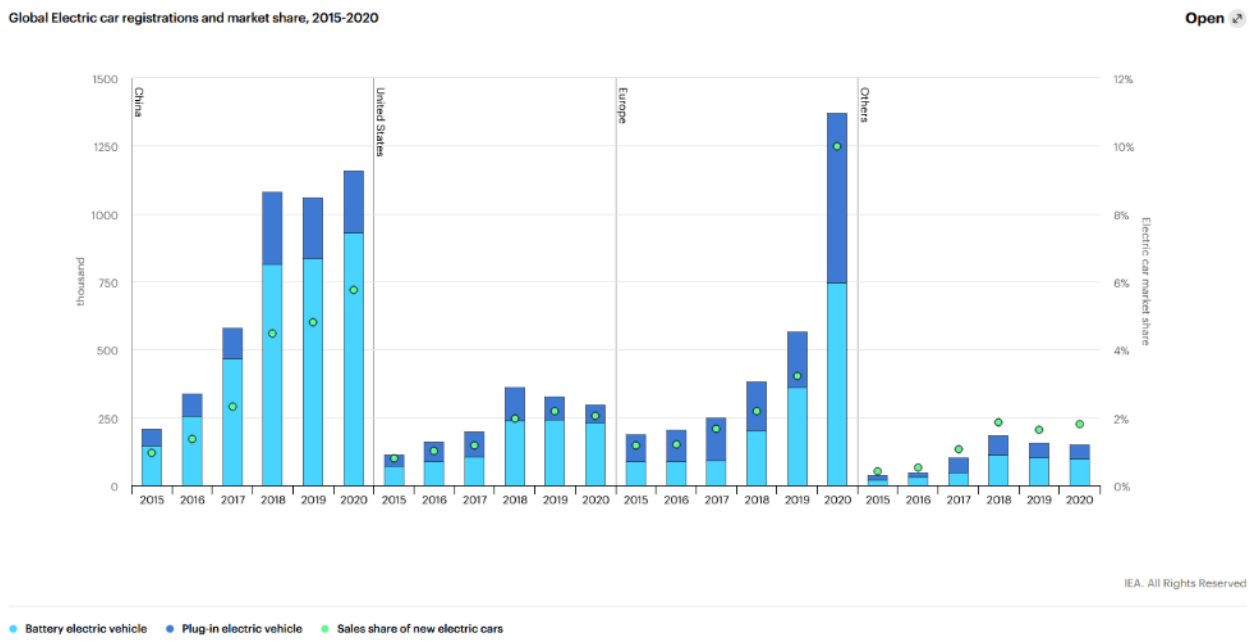


Figure 2 Global EV sales distribution

Original equipment manufacturer	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
BMW Group			25		15-25%					10
BAIC Group	2				1.3					50%
Changan Automobile (Group)					33					
Daimler		10			25%					50%
Dongfeng Motor Co	1	30%	1		1				1	1
FAW					40%					60%
Ford		40				100%*				
GM Group			22		30	1				1
Honda										40%†
Hyundai-Kia					1					
					29					
Mazda		1								5%
Renault-Nissan		20								
		20%								
Maruti Suzuki	1									1.5
SAIC					30%					30
Stellantis					38%*					70%*
					31%**					35%**
Toyota Group	1				15					>1
Volkswagen					20%					70%*
			1		3				26	50%**
					75					
Volvo (Geely Group)	1	1	1	1	50%					100%*

% of sales electric
Annual sales (million)
New EV models (number)
Cumulative sales (million)
* European market only
** Chinese and US markets only
† Includes both EVs and FCEVs

Figure 3 OEM EV development plan

Nowadays, OEMs plan to explore their electric vehicles product line in the next ten years, as shown in figure.3. Most OEMs set that EVs will account for around 50% of their total sale in

2030. Furthermore, some OEMs plan to change their product lines to produce EV only; Volvo will only sell electric cars from 2030; Ford will make only electric car sales in Europe from 2030; General Motors plans to offer only electric LDVs by 2035; Volkswagen aims for 70% electric car sales in Europe, and 50% in China and the United States by 2030; and Stellantis aims for 70% electric cars sales in Europe and 35% in the United States

1.2 Power Converters in EV

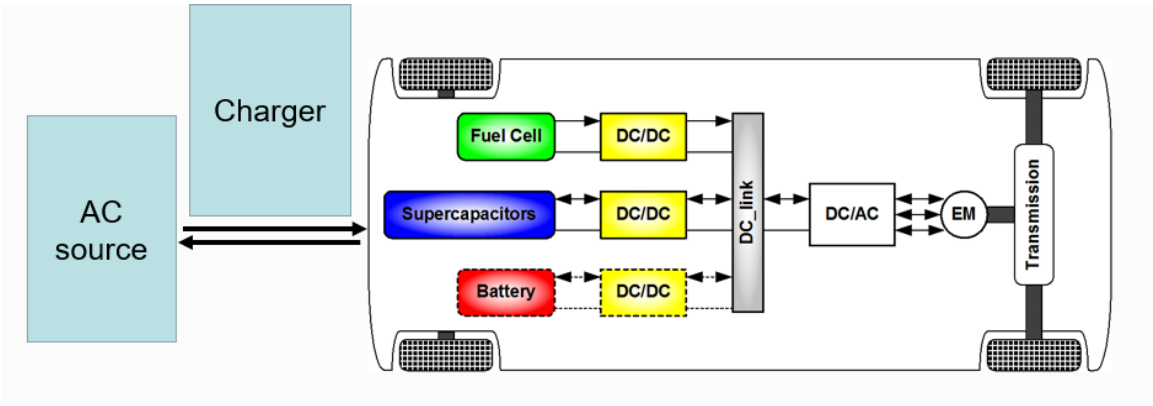


Figure 4 EV circuit diagram

A circuit diagram of EV is shown in figure 4. An electric vehicle could use different power sources: fuel cell, supercapacitor, battery, etc. The battery is usually a Lithium-ion rechargeable battery, which has a higher energy density than a traditional nickel-cadmium or lead-acid material battery. An on-board charger is set between the AC power source and battery. Fuel cell and battery Fuel cells generate energy by fuel chemical conversion. H2 is the current most used chemical fuel for the fuel cell. A Supercapacitor also called an ultracapacitor, is an extremely high capacitance value capacitor. Capacitors can store energy in a static state rather than in the form of chemicals. Which makes the charging and discharging speed much higher than the traditional battery source. A DC-DC boost/buck converter will be applied between the

power sources and DC-link to adjust the DC-link voltage to 200V~800V. A traction inverter will be used to transform DC voltage into multiple phase AC voltage as the drive power for the electric motor.

1.3 On-Board Charger Topologies

An on-board charger is a battery charger for the EV's batteries. The primary function is to realize the power factor correction function and transform the AC voltage into a steady DC voltage. The most common topologies are shown in Figure-Figure The classic boost PFC topology is the simplest on-board charger topology. This topology is a unidirectional hard switching topology. By controlling the duty cycle of the bottom power switch, the circuit can control the output voltage at a set voltage. However, hard switching makes it hard to reach a high efficiency, which increases the cooling system's requirement. Meanwhile, a high-power current increases the power loop inductor value and volume.

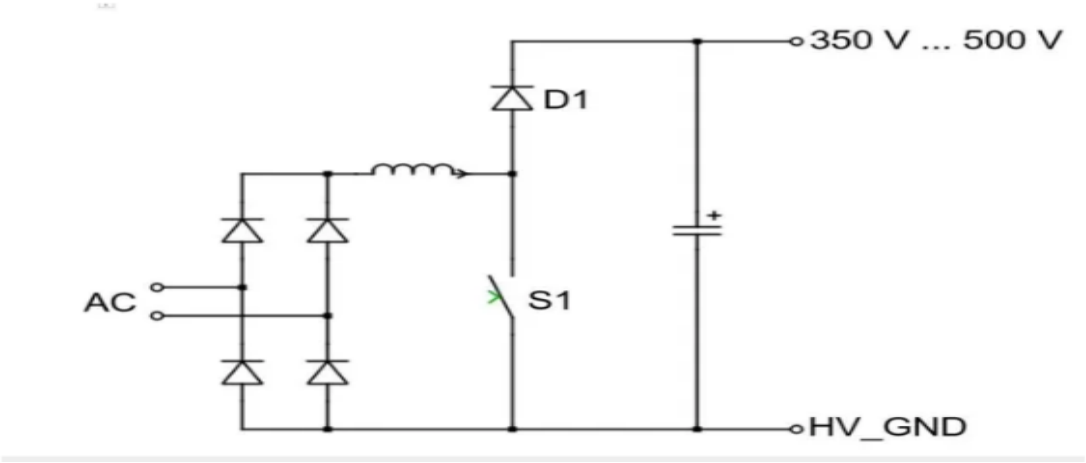


Figure 5 Classic boost PFC circuit

LLC topology is a single directional soft-switching topology, as shown in figure.6. A capacitor and inductor reason tank is put at the primary side to realize ZVS soft switching. ZVS Soft switching can reduce hearing loss and cooling system volume to realize higher efficiency

and power density. One drawback of the LLC topology is that the power is controlled by a variable frequency rather than the PWM duty cycle. A comprehensive working frequency range could challenge the EMI filers design.

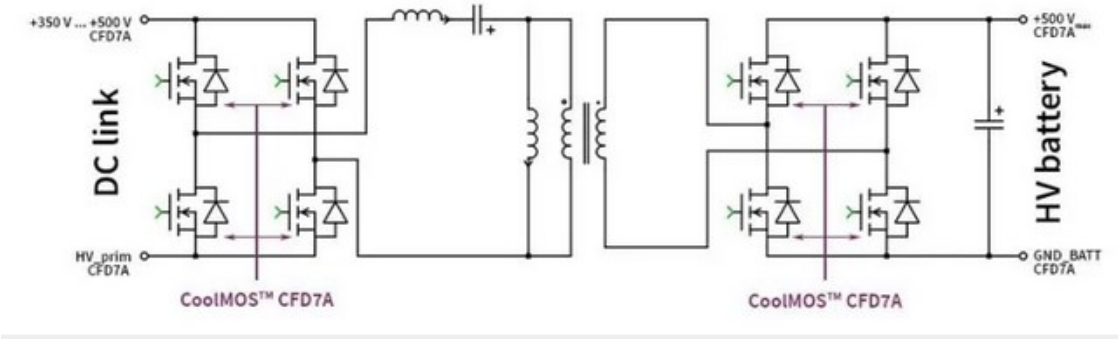


Figure 6 Full bridge LLC topology

DAB topology is a bi-directional ZVS soft-switching topology for the on-board charger. The leakage inductor on the primary or secondary side can realize ZVS soft switching on both the primary and secondary sides. Compared to LLC topology, the power level is controlled by the phase shift angle between the primary side and secondary side rather than a variable frequency. So, the software control could be easier in the DAB topology. Meanwhile, ZVS soft switching on both sides can also reduce heating loss and cooling system volume to realize higher efficiency and power density.

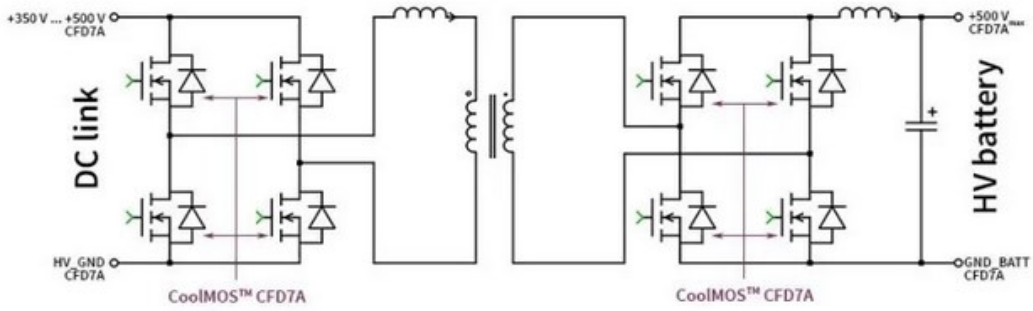


Figure 7 DAB topology

1.4 DC-DC Converter Topology

A boost converter is usually between the power source output and the traction inverter input sides. A traditional boost converter topology is shown in fig 8. In EV application, due to the high power application, traditional boost converter topology goanna has a large DC current in the power loop, which results in a high requirement on power switches. So an interleaved boost converter could improve the above issue. The interleaved boost converter topology is shown in figure.9. Compared to the traditional interleaved boost converter, it has more phase leg to undertake high current. Meanwhile, a coupled inductor can also avoid magnetic saturation.

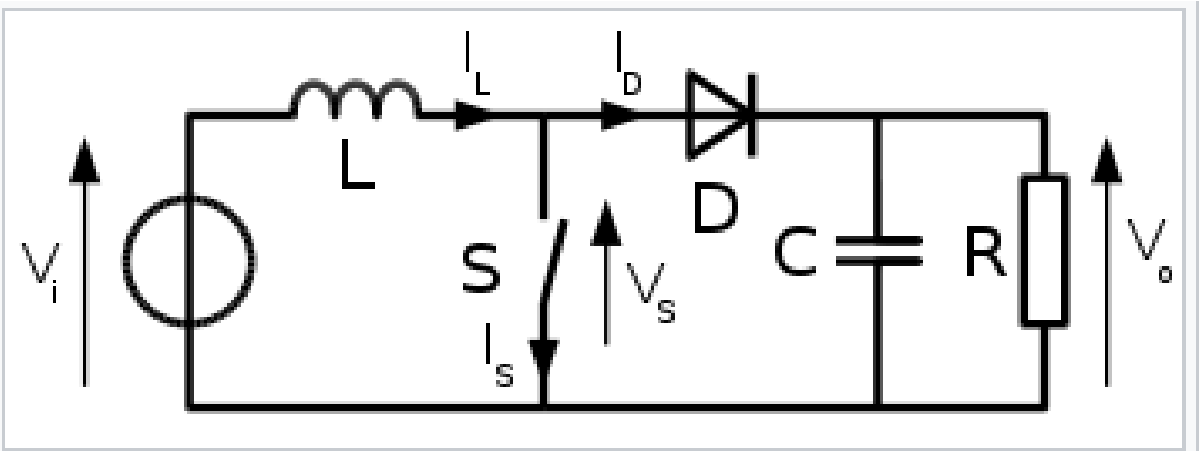


Figure 8 Typical boos converter topology

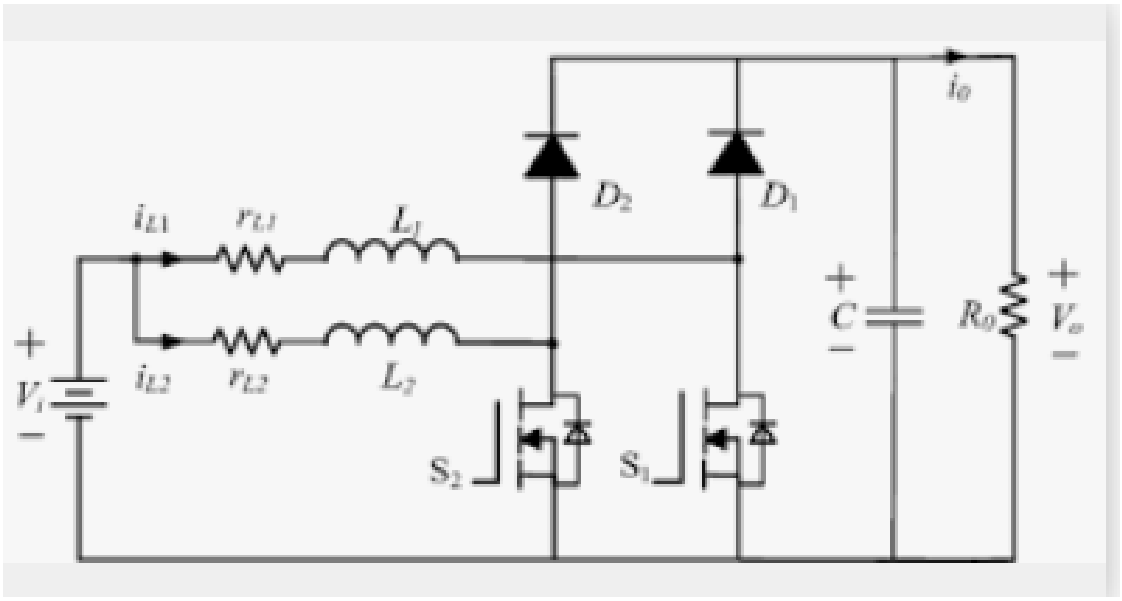


Figure 9 Interleaved boost converter topology

1.5 Traction Inverter Topology

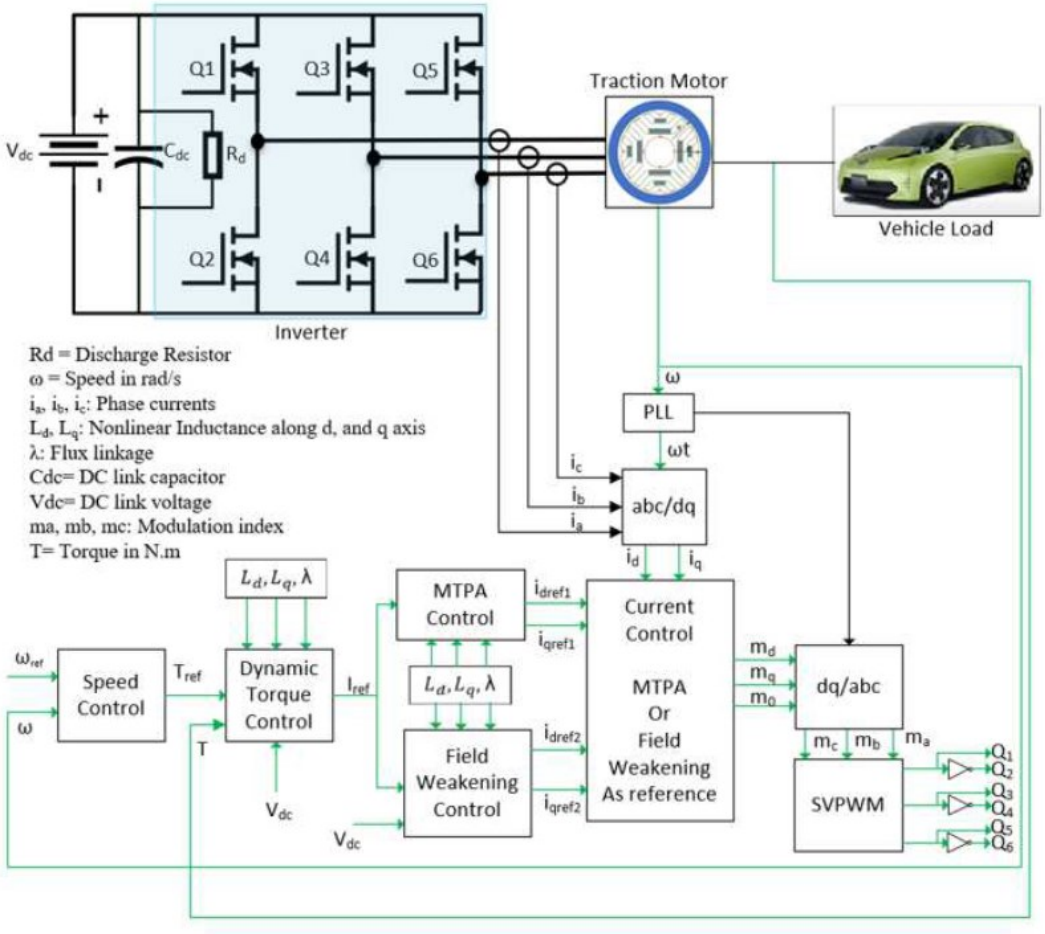


Figure 10 Traction inverter topology

A traction inverter is a high-power level inverter to provide drive power for the traction motor in an EV. The most common three-phase inverter topology is shown in fig.10. Three power MOSFETs consist of the main power loop of an inverter. The output is a three-phase AC voltage with a 120-degree phase shift. Usually, an SPWM or SVPWM control method will be used to control the output AC voltage and frequency. The closed-loop control system is made of a speed loop and a current loop. However, a typical traction inverter will work under hard switching mode. It brings higher power loss and cooling requirements. In order to improve the above issues, a T-type inverter topology is proposed to realize soft-switching, as shown in

figure.11. Meanwhile, a T-type inverter could also reduce the output three-phase AC voltage THD.

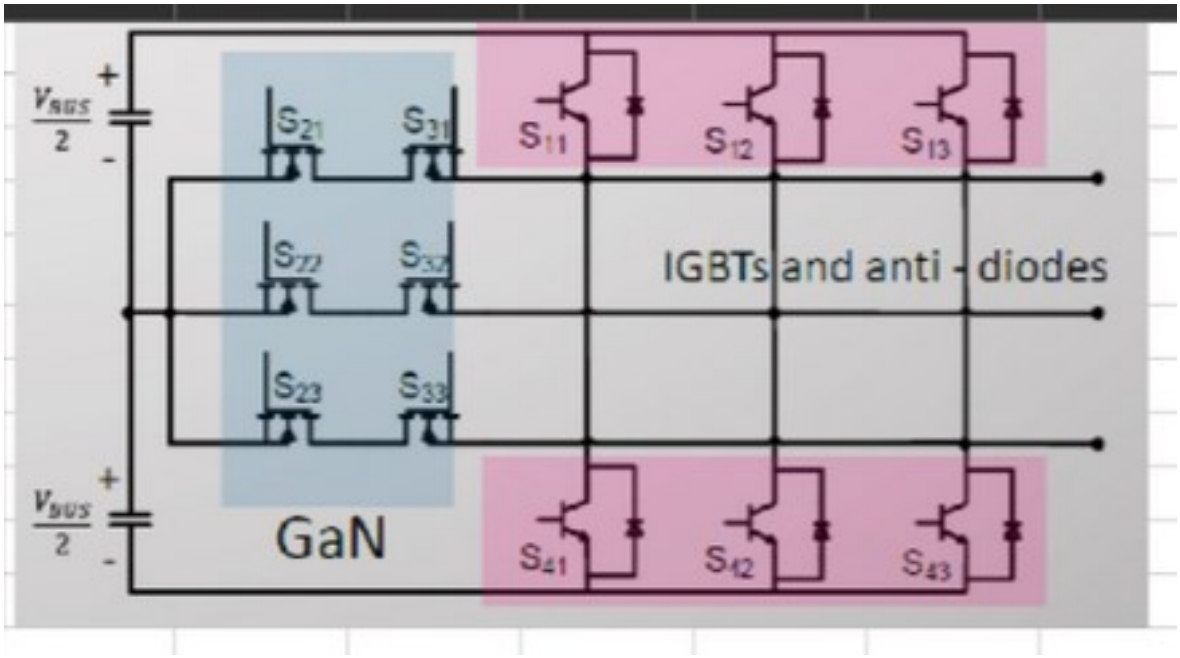


Figure 11 T-type inverter topology

Chapter 2 Benefits of WBG in EV Power Converters

2.1 Wide Band Gap Devices Material Characteristic

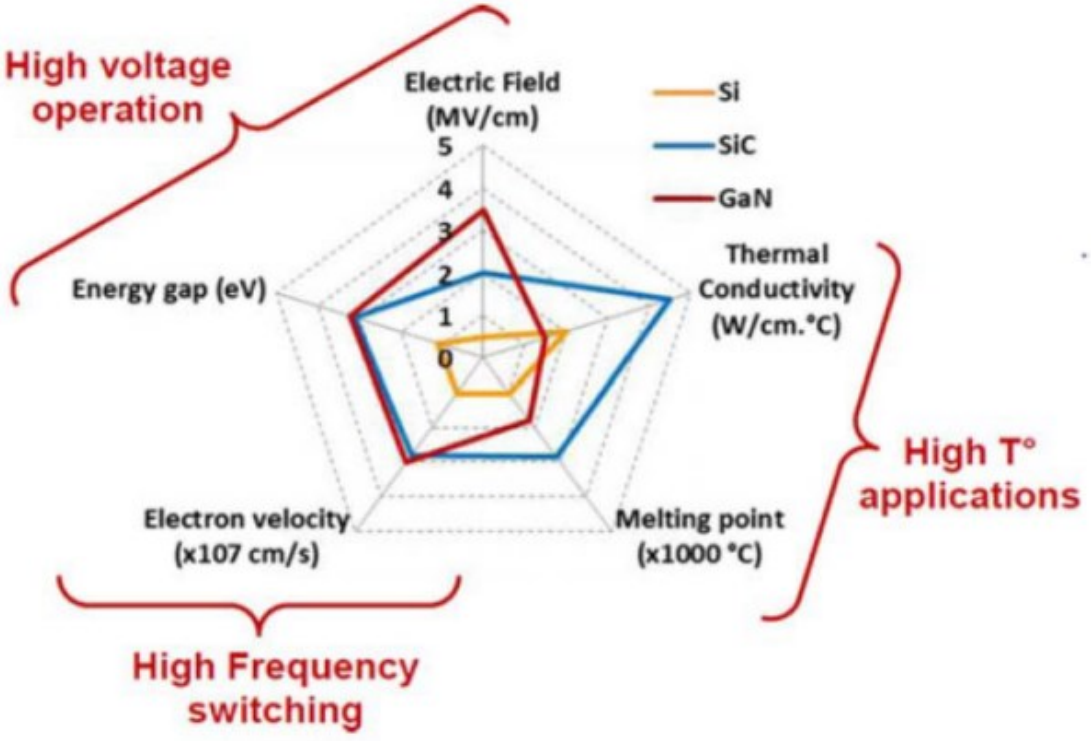


Figure 12 WBG material characterize

Wide-bandgap semiconductors are semiconductors that have a larger bandgap than traditional Si semiconductors, as shown in figure.11. Usually, Si devices' bandgap falls in the range of 1~1.5 electronvolt. However, the WBG devices could have above 2 eV bandgap (2.86ev for SiC,3.4 for GaN). Bandgap means the minimum energy gap between the conduction band and dielectric band. As for semiconductors, a small amount of energy could push more electrons into the conduction band, making devices work in a conduction state. Meanwhile, due to the material charsets, WBG materials also have a high electronic moving speed which makes WBG

devices could have a higher switching speed than traditional Si devices. Two Main Band Gap Devices: Sic and Gan.

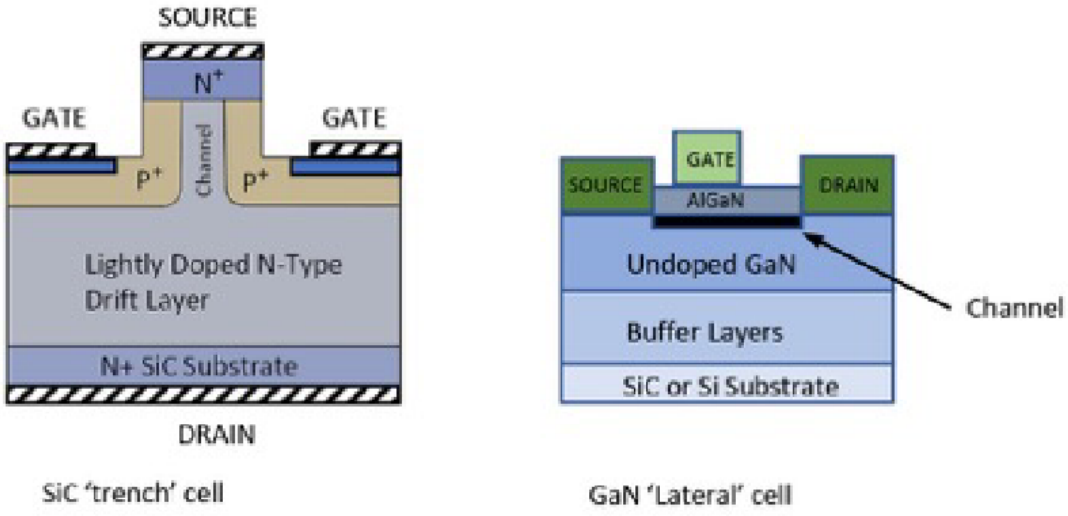


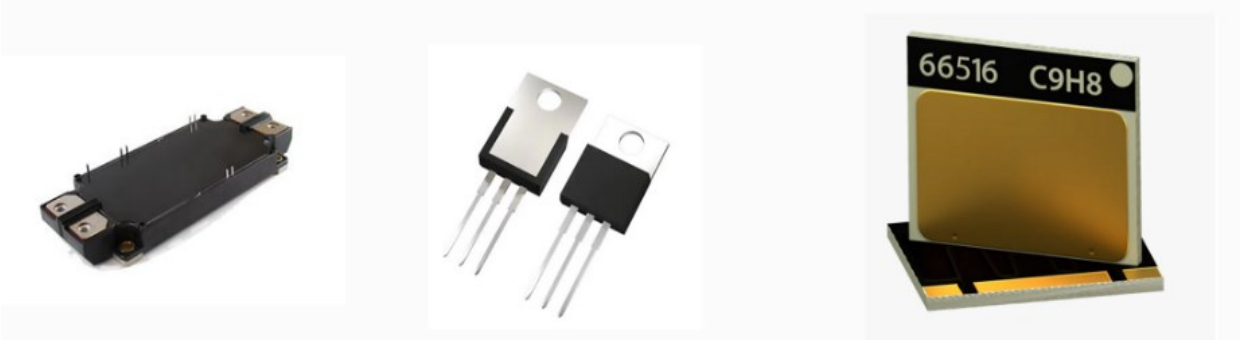
Figure 13 SiC and GaN structure

SiC and GaN both have a similar structure to Si Devices as shown in figure.12. Due to Pure GaN being hard to yield, there is always a SiC/Si substrate in GaN. Substrate mismatch makes GaN breakdown voltage drop around 1000VSo GaN is applied in a low voltage and high switching frequency application (power supply, adaptor). SiC is applied in high voltage and power applications.

2.2 WBG Device Packages

Most of the wideband gap MOSFET packages are shown in figure.13. There are three main package types. The power module package is used for the highest power and current application(up to 500 hundred amperes or even higher), as shown in (a). The TO-247 package, as shown in figure 14(b) is used for the lower current application. Usually, the highest current rate for one To-247 package is around 100A. Surface-mount package, as shown in Figure14.(C),

has the lower parasitic parameters. It is usually applied in a high switching frequency (over 500k) application with a lower current rate(smaller than 100A).



(a) (b) (c)

Figure 14 SiC and GaN device packages (a) Power module (b) through-hole package(c) Surface mount package.

Chapter 3 On-Board Charger Design Case with GaN

3.1 GaN Gate and Power Loop Design

3.1.1 Introduction

Wide-bandgap (WBG) devices attract more and more attention in recent days as the promising alternative of Si devices. It is witnessed that in the past several years high-current GaN devices have been emerging quickly and applied in various power electronics applications, e.g., travel adapters, wireless chargers, smart home appliances, high efficiency AC-DC data-center power supplies, industrial motor drives and on-board EV battery chargers. Different from Si/SiC MOSFETs, GaN HEMTs are essentially hetero-junction devices, relying on the two-dimensional electron gas (2DEG) formed between GaN and AlGaN to conduct the current, shown as Fig.15. When imposing zero or negative voltage on the gate, the 2DEG will diminish thereby turning off the switch. Since electrons are travelling laterally between the drain and the source, the GaN HEMT is a typical lateral switch.

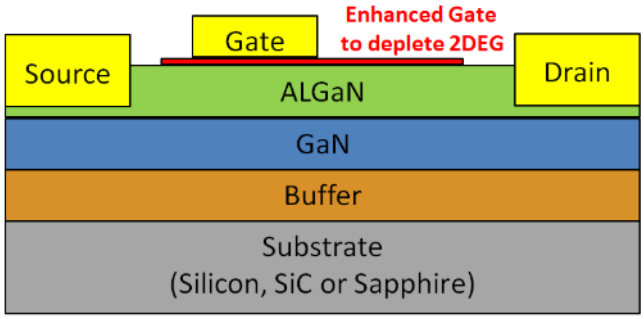


Figure 15 Structure of E-mode GaN HEMTs.

Presently available GaN HEMTs are shown as Table. I. Among which, Transphorm and ON Semiconductor use the cascode design, i.e., employing a Si MOSFET to control of gate of the GaN JFET thereby forming a normally off device. EPC, Panasonic and GaN Systems use theenhancement-mode (E-mode) devices without any extra silicon gate. GaN Systems provides so-far the highest current rating of all GaN HEMTs, which is the study object of this paper.

Table 1 Possible candidates of GaN HEMTs

PartNumber	Manufacturer	V_{DS} /V	Ids /A	Rdson/ mΩ	Package
GS66516T	GaN Systems	650	60	27	GaN *PX* 9x7.6x0.45
TPH3205WS	Transphorm	600	36	52	TO247
EPC2034	EPC	200	31	7	Passivated Die
PGA26E08BA	Panasonic	600	15	56	DFN 8x8 (BV-Typ)
NTP8G206N	ON Semiconductor	600	17	150	TO 220 Style 10
QFN8-HB2-1D	Sanken Electric	600	20	50	QFN 8x8x0.85 (mm)
AVJ199R06060A	Avogy	650		200	TO 220
MGG1T0617D	MicroGaN GmbH	600	30	170	Die

The impact of parasitics on a single device has been thoroughly discussed [43-46], however, there is very little work focusing on the dynamic performance of paralleled GaN HEMTs [47-48], no mention paralleling more than 2 GaN HEMTs, which is thought to be extremely difficult [49]. Previous work is mainly focused on the inductance reduction [50-52] and loss modeling [53]. In addition, it is still recommended to adopt zero-voltage-switching (ZVS) technology to eliminate its switching-on loss to further enhance the efficiency. Such attempt has been implemented in [54], where a 7.2 kW on-board charger has been developed with >97% efficiency and ~4kW/L power density. Four GaN(GS66516T) have been paralleled to undertake 400V/92A hard switching-off reliably. Based on previous literatures, this paper aims to 1) further extend GaN application from the soft-switching to the hard-switching applications, given in some applications such as DC/AC inverters the hard switching is inevitable, and 2)

realize more switch paralleling (>2) given that 60A is not enough for some high-power applications. An analytical model to facilitate the understanding of switching process especially for paralleled GaN HEMTs is built in following section.

There is a growing interest in high-power-density and high-efficiency battery chargers for electric vehicles (EVs)[55-56], most of which adopt three stages [57-59], i.e., an AC/DC stage to convert the grid voltage to a DC voltage and realize the power factor correction (PFC), a DC/AC stage to transform the DC to a high-frequency AC (hundreds of kHz) on the primary side of the transformer, and an AC/DC stage to rectify the induced high-frequency AC to a DC voltage to charge the battery. Shown in Fig. 1a is a typical single-phase charger using resonance technology. The grid-side AC/DC employs the totem-pole boost-type PFC. Lr and Cr form a resonance circuit to realize the zero voltage switching (ZVS)[60]. Shown in Fig.1b is a typical three-phase charger using the full-bridge LLC resonance [61]. When using MOSFETs, all switches have body diodes.

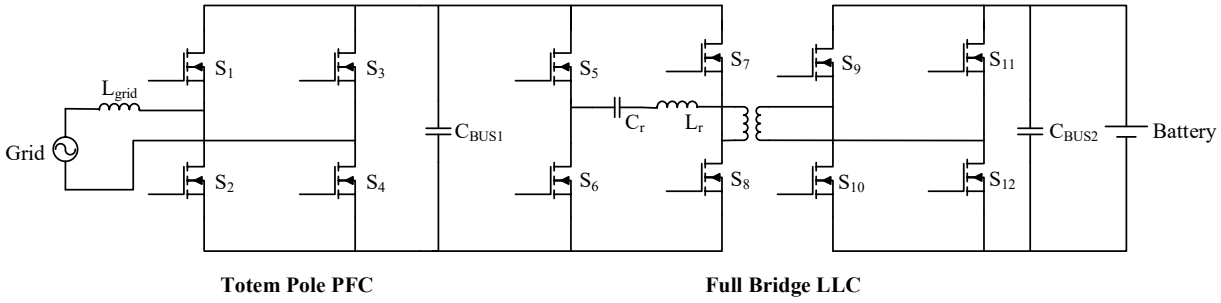


Figure 16 A conventional single-phase isolated charger

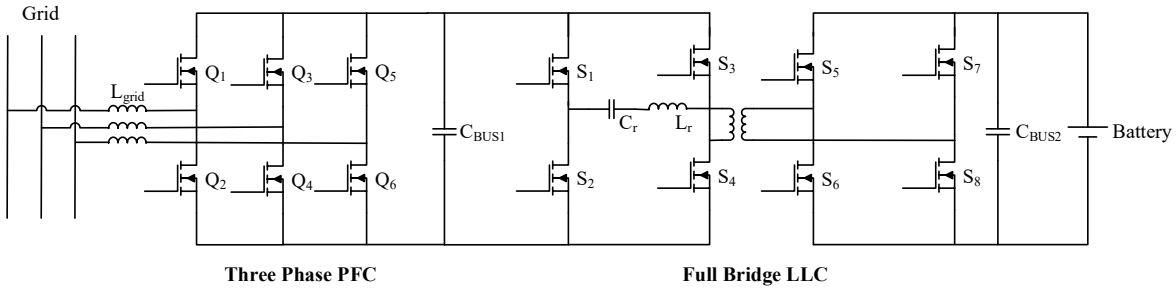


Figure 17 A conventional three-phase isolated charger

All chargers above need bulky DC-bus capacitors and have a relatively high power loss. Assume each stage (AC/DC, high-frequency DC/AC, transformer and AC/DC) has 1~2% power loss. This yields ~94% efficiency and ~2kW/L power density, such as Brusa 22kW charger (NLG664) based on Si devices. Various bidirectional isolated AC/DC converters were investigated in previous literatures [62-64]. In [62], a single-phase bidirectional isolated ZVS AC-DC converter was proposed, as shown in Fig.16. Such topology decreases the stage numbers and eliminates the massive DC-bus capacitor. By using back-to-back switches, the transformer primary voltage follows the envelope of the grid input. It needs vary the phase-shift and switching frequency to secure the power delivery and the power factor simultaneously. Instead of using the back-to-back switches, a circuit in [65-66] is a better candidate. As shown in Fig. 17, the front-end rectifier stage (R1~R4, here R stands for "rectifier") is operated at the line frequency, simply converting the sinusoidal waveform to a double-line-frequency DC voltage. Therefore for the grid-side H-bridge, using conventional Si MOSFET is enough. It meanwhile saves back-to-back switches, eliminates the switching loss, and shrinks the DC-bus capacitance to ~μF level, given there is no need to keep the DC-bus voltage constant. The DAB stage needs realize both PFC and battery charging. To build a three-phase charger, e.g., 380VAC/20kW for European and Asian markets, three such single-phase modules could be connected as Fig.18. The overall charger follows the exact power density and efficiency of each single-phase charging module and offers high tolerance, i.e., providing the power even when two phases fail.

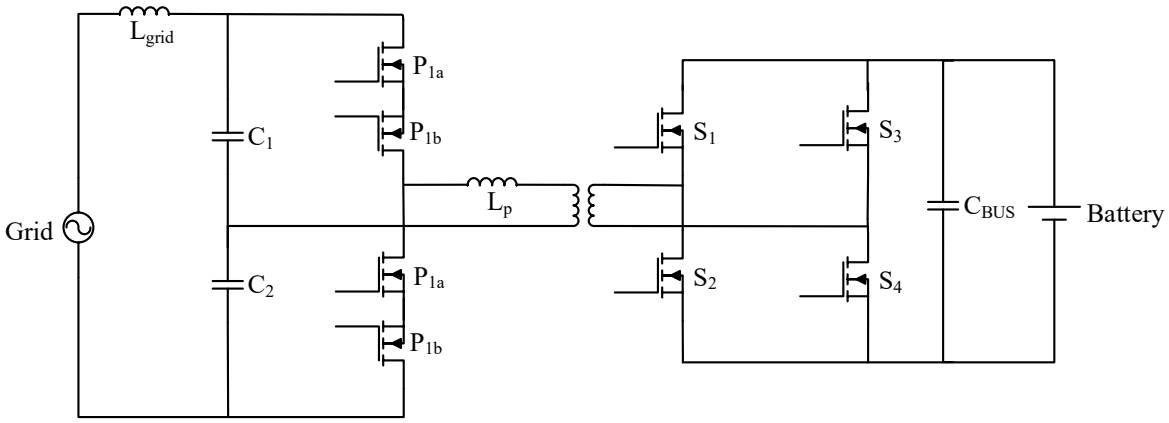


Figure 18 Single-phase single-stage bidirectional isolated ZVS AC-DC converter

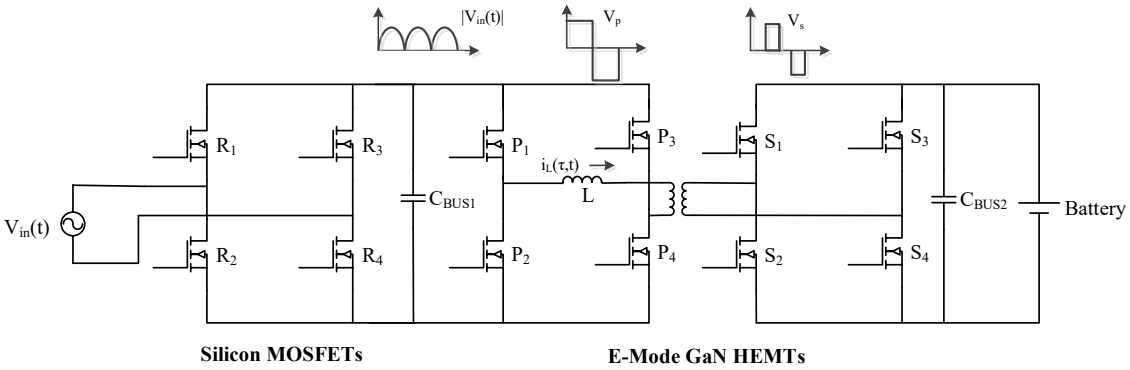
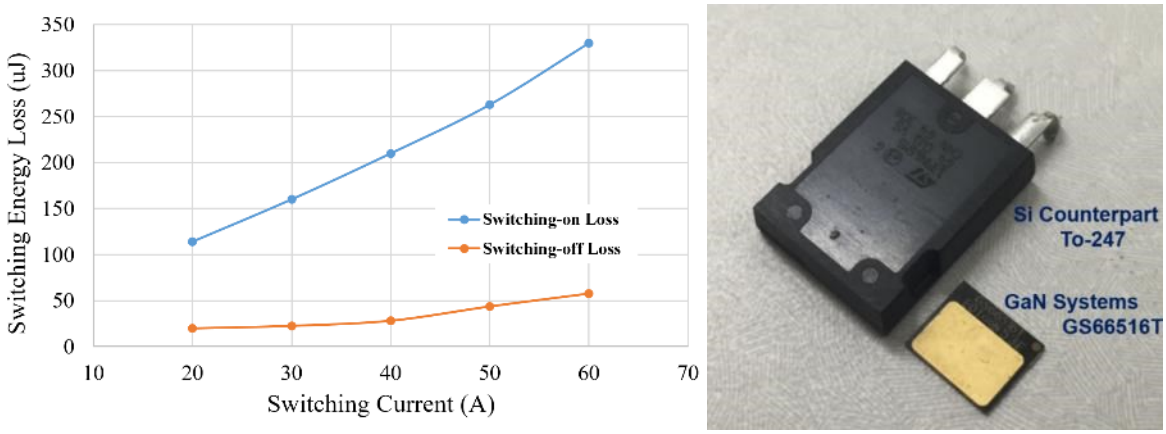


Figure 19 Charger topology adopted in this on-board charger

For the DAB stage (P1~P4, S1~S4), wide-bandgap (WBG) devices such as GaN HEMTs and SiC MOSFETs are excellent candidates to enhance the efficiency and power density, due to their ultra-fast switching transitions and ultra-low gate-drive power [67]. Some attempts have been carried on for EV chargers using GaN for high-switching-frequency applications [68-70]., showing superior efficiency or power density. Different from the previous literature mostly using cascode GaN devices, this paper adopt Enhancement mode (E-mode) GaN HEMTs, GS66516T from GaN Systems Inc, as shown in Fig.3(a). Its no-lead, top-cooled package significantly facilitates the parasitcs reduction. Compared with silicon and other GaN counterparts, its much smaller size

makes it more appealing. Along with the topology shown in Fig.2b



(a) (b)

Figure 20 (a) Switching Energy of GS66516T (b)Leadless Top-Cooled Packaging of GaN HEMTs (GS66516T)

It is also possible to use SiC devices [71-72], which represents another type of WBG devices. Whatever devices preferred, the following issues need be resolved, i.e., 1) ZVS turn-on has to be true within all output-voltage range (200~450VDC), given that both SiC and GaN have much higher switching-on loss than switching-off loss, as shown in Fig.20(b), and a systematic integration of the three single-phase charging modules, not only at the package level but also at the control level, e.g., a closed-loop control to balance each-phase power even when the grid voltage is imbalanced.

3.1.2 Modelling Dynamic Behavior of Paralleled Gan Hemts with Parasitics

Take GS66516T(650V/60A) as an example. Its I-V curve at different temperature is shown in Fig.21, indicating an obvious positive correlation between the channel resistance and the temperature. Such characteristics guarantee the current balancing among paralleled switches in the steady state.

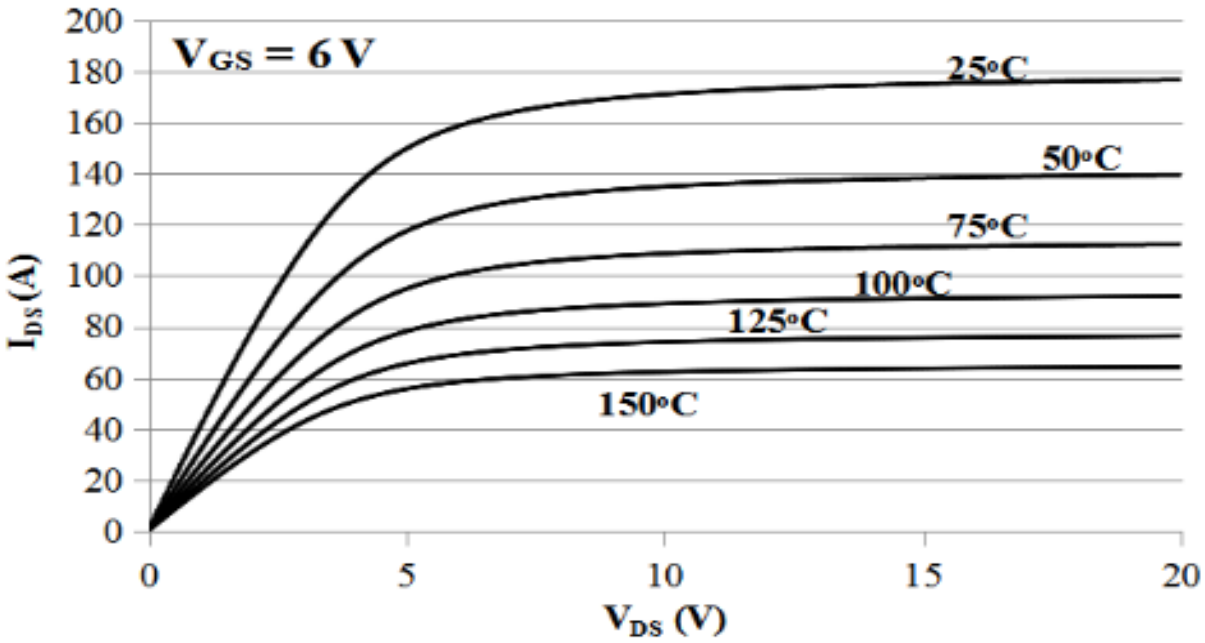


Figure 21 V-I Curve of GS66516T vs. Temperature

The main challenge for the parallel operation, however, lies in the switching process, during which parasitic parameters and gate driver circuits play critical roles. Different from most of Si MOSFET, E-mode GaN has relatively low turn-on gate-voltage threshold, e.g., ~2V, making it very sensitive to the high di/dt and dv/dt during the dynamic process. When VGS exceeds 10V, such device will be destroyed. Therefore the electrical stress caused by parasitics need more attention than conventional Si devices. Any attempt of swapping Si with GaN without optimizing the circuit layout will result in the system failure.

In this section, we will first study two GaN HEMTs in parallel, locate potential influential factors and model their dynamic behaviors, which provides effective guidance for paralleling more GaN HEMTs in Section III. A half bridge consisting of two high-side and two low-side GaN HEMTs in parallel is shown as Fig.22, in which all parasitics are considered, and C2~C4 is the gate driver capacitors, CDC is the decoupling capacitor, and RG1~RG4 and RS1~RS4 are the gate driver resistors.

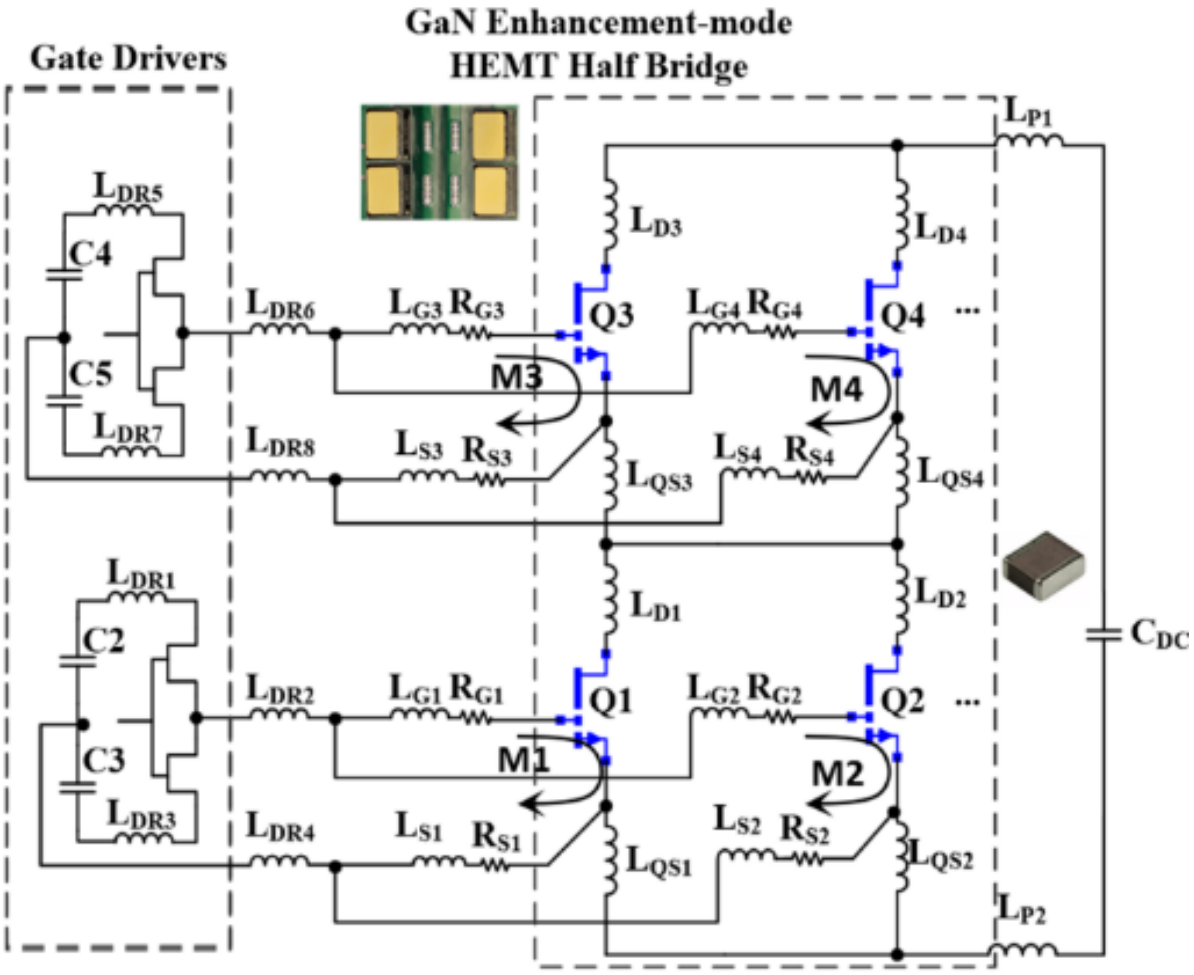


Figure 22 A Half Bridge with 2x GaN HEMTs in Parallel

Fig.23 shows the switching-on process of paralleled GaN HEMTs. Here we divide the whole process into four intervals, i.e., P1-delay period, P2-di/dt period, P3-dv/dt period and P4-remaining switching period. Particular attention needs be paid to P2 and P3 since such periods bring the majority of current and voltage stresses to GaN HEMTs. Fig.24 shows the state trajectory of the switch during the turn-on process.

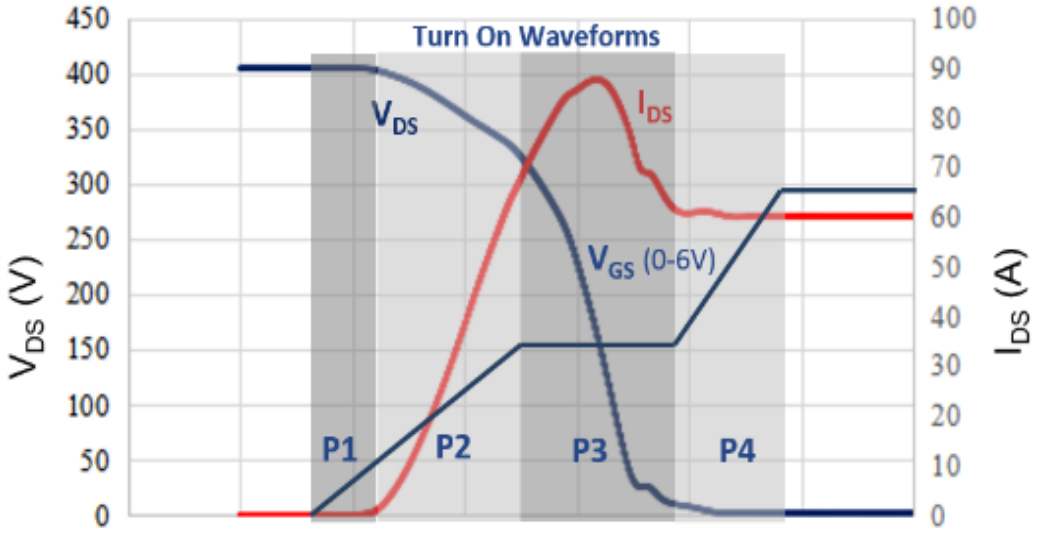


Figure 23 V_{DS}, I_{DS} Waveform During Switching on

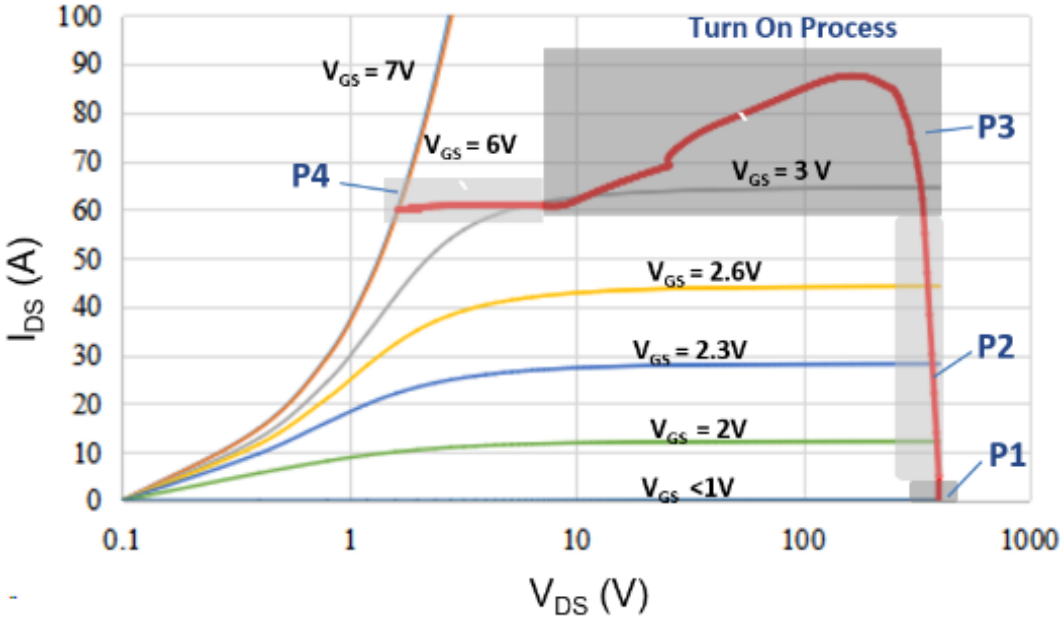


Figure 24 State Transition of GaN HEMT During Switching on

As for the P2:di/dt period ,after the gate-source voltage of any of paralleled HEMTs reaches the threshold, the impedance of 2DEG begins to decrease. In this mode, the HEMT is operated in the saturation region, drain current ($i_{D(t)}$) is controlled by gate-source voltage ($v_{GS(t)}$) i.e.,

$$i_{D(t)} = g \cdot (v_{GS(t)} - V_{th}) \quad (1)$$

Here g is trans-conductance, and V_{th} is threshold voltage. As $v_{GS(t)}$ increases, $\frac{di_{D(t)}}{dt}$ starts to affect the gate voltage through the common-source inductance between gate-drive loops and power loops. To mitigate such cross talking, the Kelvin terminal is usually employed to bypass the common source inductance, as shown in Fig.25. Even so, such interaction between the gate and power loop has not fully resolved yet due to the existence of the quasi-common-source inductance (L_{QS_1} and L_{QS_2}as shown in Fig.19). The imbalanced quasi-common source inductance and high di/dt together will eventually cause a feedback voltage across gate source voltage as shown in (2). Such feedback voltage is regarded as the disturbance on gates of paralleled switches, which will be minimized if the layout is optimized ($L_{QS_1} \approx L_{QS_2}$) and current is evenly distributed among switches ($i_{D_1(t)} \approx i_{D_2(t)}$).

$$v_{QS_1(t)} = \left(L_{QS_1} \cdot \frac{di_{D_1(t)}}{dt} - L_{QS_2} \cdot \frac{di_{D_2(t)}}{dt}\right) \cdot \frac{Z_{s_1}}{Z_{s_1} + Z_{s_2}} \quad (2)$$

Here, $v_{QS_1(t)}$ is the voltage across $L_{S_1}$and R_{S_1}, Z_{s_1} and Z_{s_2} are the impedance of L_{S_1}, $R_{S_1}$and L_{S_2}, R_{S_2} respectively.

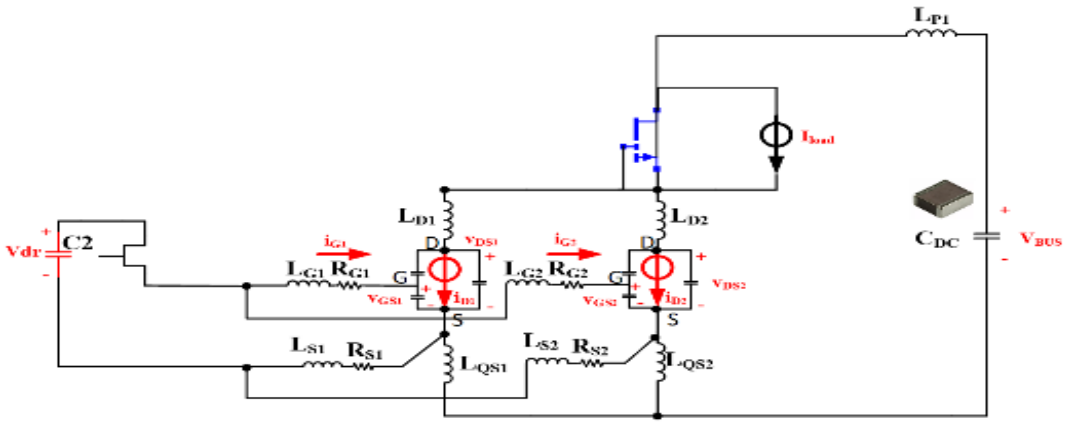


Figure 25 Equivalent Circuit during di/dt Period of Switching on Process

Based on KCL and KVL,

$$C_{GD_1}\cdot\frac{dv_{GS_1(t)}}{dt}+C_{GS_1}\cdot\frac{dv_{GS_1(t)}}{dt}=\frac{1}{R_{G_1}+R_{S_1}}(V_{dr}-v_{GS_1(t)}-v_{QS_1(t)}-M_1\cdot\frac{di_{D_1(t)}}{dt}-(L_{G_1}+L_{S_1})\cdot\frac{di_{G_1(t)}}{dt} \quad (3)$$

$$v_{DS_1(t)}=V_{BUS}-L_P\cdot\left(\frac{di_{D_1(t)}}{dt}+\frac{di_{D_2(t)}}{dt}\right)-M_1\cdot\frac{di_{G_1(t)}}{dt}-(\mathrm{L_{D\,1}}+\mathrm{L_{QS_1}})\cdot\frac{di_{D_1(t)}}{dt} \quad (4)$$

$$\mathrm{i_{G_1(t)}}=C_{ISS_1}\cdot\frac{dv_{GS_1(t)}}{dt}+C_{RSS_1}\cdot\frac{dv_{GD_1(t)}}{dt} \quad (5)$$

Here V_{dr} is the gate-drive voltage generated by the gate-drive ICs, M_1 is the mutual inductance between the gate-drive loop and power commutation loop.

When P2 period ends when $i_{D_1(t)}$ *or* $i_{D_2(t)}$ reaches I_{load}. Assuming $\frac{di_{D_1(t)}}{dt}=\frac{di_{D_2(t)}}{dt}$, v_{GS_1} is derived as (6).

$$v_{GS_1(t)}=V_{dr}+(V_{dr}-V_{th\,1})\cdot\left(\frac{s_2\cdot e^{s_1t}-s_1\cdot e^{s_2t}}{s_1-s_2}\right) \quad (6)$$

Here $s_{1,2}=\frac{\pm\sqrt{b^2-4a}-b}{2a}$,

$a=(R_{G_1}+R_{S_1})\cdot C_{GD_1}\cdot\left(L_{D_1}+\frac{L_{P_1}}{2}+M_1+\mathrm{L_{QS_1}}-\mathrm{L_{QS_2}}\right)+(C_{GS_1}+C_{GD_1})\cdot(M_1+\mathrm{L_{QS_1}}-\mathrm{L_{QS_2}}+L_{G_1}+L_{S_1})$

$,b=1+\left(\mathrm{L_{QS_1}}-\mathrm{L_{QS_2}}+M_1\right)g+(R_{G_1}+R_{S_1})\cdot(C_{GS_1}+C_{GD_1})$.

A higher gate driver voltage (V_{dr}) or smaller gate resistance (R_G+R_S) will lead to a faster switching transition, resulting in a lower loss.

Also, in this period, the quasi-common-source inductance ($\mathrm{L_{QS_1}}$, $\mathrm{L_{QS_2}}$) has a similar effect as the mutual inductance (M1), which might potentially cause overshoot or undamped ringing on v_{GS}. an unsynchronized gate-drive circuit is proposed, using one switch to fully turn on first before other switches. Its problem is that one switch undertakes majority of the turn-on current, which potentially lowers the system reliability. A symmetric power loop and gate driver loop

layout is a better solution, as proposed and discussed in Section III to achieve the reliable switching.

P3:dv/dt Period

During this process, the impedance of 2DEG is controlled by gate-source voltage as shown in (7).

$$R_{2DEG} = \frac{v_{DS(t)}}{g \cdot (v_{GS(t)} - V_{th})} \tag{7}$$

This period ends when $v_{ds(t)}$ reaches zero. The circuit behavior could be modelled as (8) & (9). Miller plateau is observed in this period during which $v_{GS_1(t)} = v_{GS_1\_miller}$.

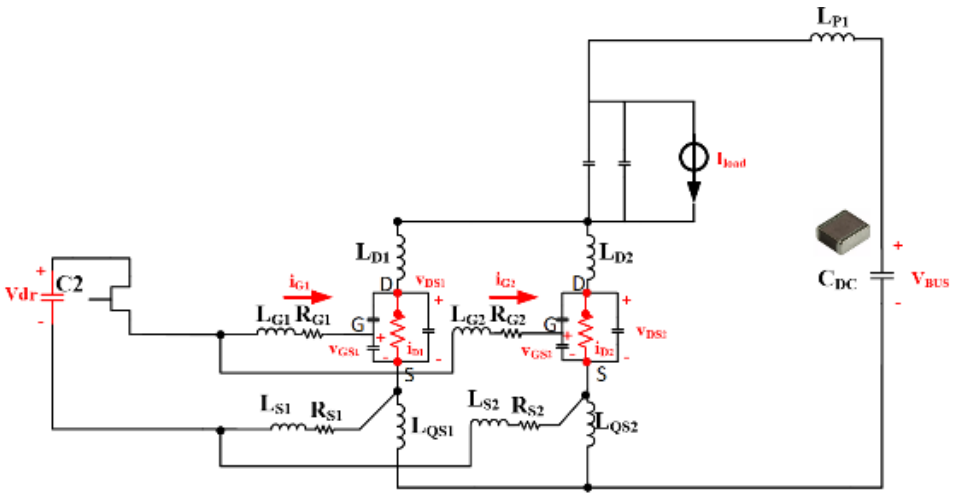


Figure 26 Equivalent Circuit during dv/dt Period of Switching on Process

$$C_{GD_1} \cdot \frac{d v_{DS_1(t)}}{dt} = \frac{1}{R_{G_1}+R_{S_1}} \left(V_{dr} - v_{GS_1\_miller} - v_{QS_1(t)} - M_1 \cdot \frac{di_{D_1(t)}}{dt} - (L_{G_1} + L_{S_1}) \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2}\right) \tag{8}$$

$$\left(I_{load} + C_{OSS_{total}} \cdot \frac{dv_{DS_1(t)}}{dt}\right) \cdot R_{2DEG} + L_{LOOP} \cdot C_{OSS_{total}} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2} = V_{BUS} \; R_{2DEG} = \frac{v_{DS(t)}}{g \cdot (v_{GS(t)} - V_{th})} \tag{9}$$

Here $L_{LOOP} = L_{P1} + (L_{D1} + L_{QS_1}) // (L_{D2} + L_{QS_2})$, $C_{oss_{total}}$ is the total output capacitance of both high-side and low-side transistors and R_{2DEG} is the 2DEG resistance of low-side transistors. So, $v_{DS_1(t)}$ and $v_{GS_1(t)}$ of low-side HEMTs could be derived as (10) and (11).

$$v_{DS_1(t)} = V_{BUS} \cdot \left(1 - \frac{S_2}{S_2 - S_1} \cdot e^{S_1 \cdot t} + \frac{S_1}{S_2 - S_1} \cdot e^{S_2 \cdot t}\right) \mathrm{R_{2DEG}} = \frac{\mathrm{v_{DS(t)}}}{\mathrm{g} \cdot (\mathrm{v_{GS(t)}} - \mathrm{V_{th}})} \quad (10)$$

$$v_{GS_{1\_miller}} = \frac{1}{R_1}\left(V_{dr} - (R_{G_1} + R_{S_1}) \cdot C_{GD_1} \cdot \frac{dv_{DS_1(t)}}{dt} - v_{QS_1(t)} - M_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2} - (L_{G_1} + L_{S_1}) \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2}\right) \quad (11)$$

Here $v_{QS_1(t)}$ follows eqn (2), $s_{1,2} = \frac{\pm\sqrt{R_{2DEG}^2 - 4\frac{L_{LOOP}}{C_{OSS_{total}}}} - R_{2DEG}}{2 \cdot L_{LOOP}}$.

According to (7), the miller plateau voltage ($v_{GS_{1\_miller}}$) determines R_{2DEG} so as to control the slew rate of the drain-to-source voltage. From (7) to (10), the lower the miller plateau, the higher the channel resistance, therefore the longer time for VDS to reach the steady state, representing the higher the switching-on loss. Meanwhile, according to (11), the larger the gate resistance, the lower $v_{GS_{1\_miller}}$, which results in a higher switching-on loss. Overall, (11) indicates that increasing the turn-on voltage or reducing the turn-on gate resistance is an effective solution to reduce the switching-on loss.

The turn-off process is shown in Fig.21. Three intervals are included, i.e., P1-delay period, P2-dv/dt period, P3-di/dt period.

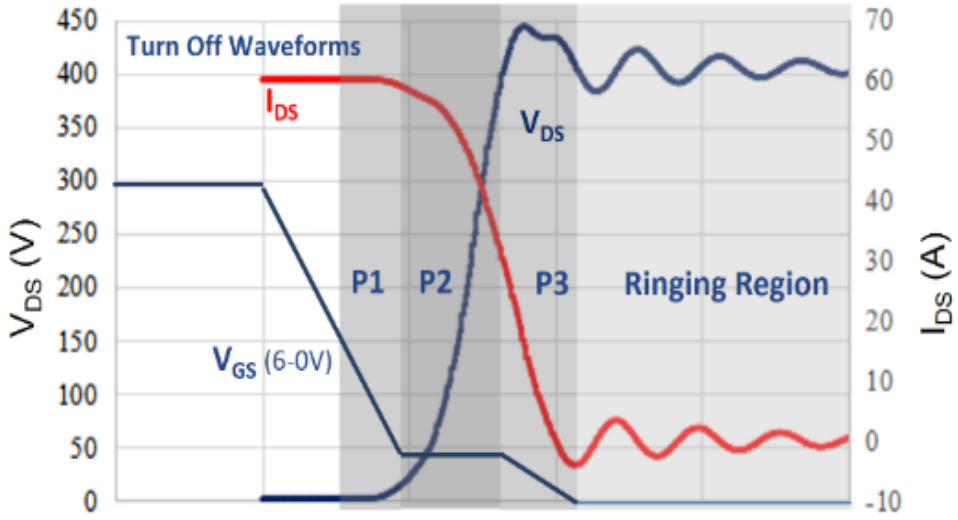


Figure 27 Waveform During the Switching-off

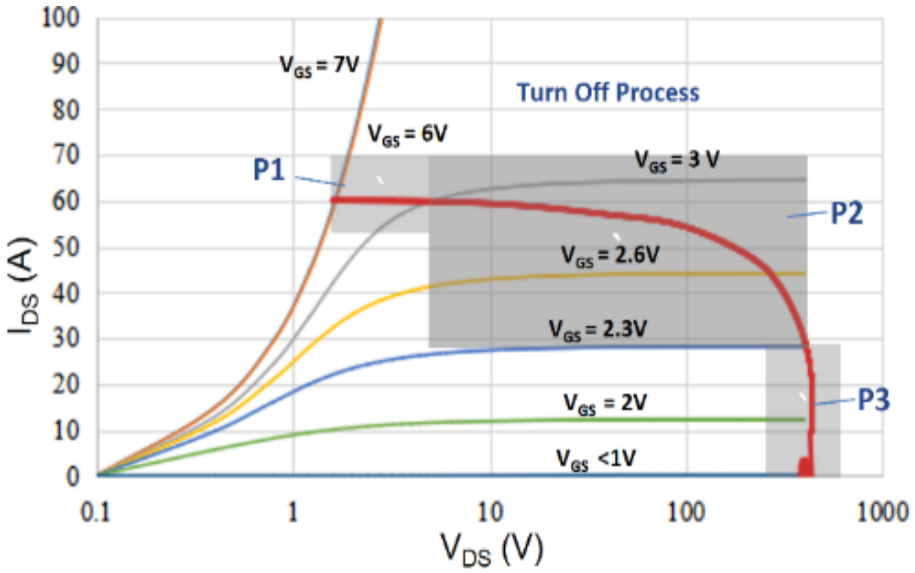


Figure 28 State Trajectory of GaN HEMT During the Switching-off

P2:dv/dt Period is similar to dv/dt Period of switching on process, miller plateau will also be observed during this period. With the 2DEG impedance increasing, the load current (I_{load}) begins to discharge and charge high-side and low-side output capacitance, respectively. Here $C_{OSS_{total}}$ represents the overall output capacitance of the whole leg. $v_{DS_1(t)}$and $v_{GS_1(t)}$of the low-side HEMT are derived as

$$v_{DS_1(t)} = V_{BUS} \cdot \left(1 - e^{\frac{-t}{R_{2DEG} \cdot C_{OSS_{total}}}}\right) \mathrm{R_{2DEG}} = \frac{\mathrm{v_{DS(t)}}}{\mathrm{g} \cdot (\mathrm{v_{GS(t)}} - \mathrm{V_{th}})} \tag{12}$$

$$v_{GS_{1\_miller}} = \frac{1}{R_1}(V_{dr\_off} + R_1 \cdot C_{GD_1} \cdot \frac{d\,v_{DS_1(t)}}{dt} + v_{QS_1(t)} + M_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2} + L_1 \cdot C_{GD_1} \cdot \frac{d^2 v_{DS_1(t)}}{dt^2}) \quad (13)$$

According to (7), (12) and (13), the gate resistance determines the miller plateau voltage ($v_{GS_{1\_miller}}$) then further impacts the slew rate of the drain-to-source voltage. The larger the gate turn-off resistance, the lower $v_{GS_{1\_miller}}$. When the miller plateau voltage is lower than the threshold voltage, the 2DEG is pinched off. Adding a negative switching-off voltage, e.g., Vdr_off=-5V, expedites such switching process thereby reducing the switching loss. This period ends when the drain-source voltage reaches the bus voltage.

P3:di/dt Period

In this mode, the high-side transistors begin to freewheel the current. The low-side GaN HEMTs are shutting down. The $v_{GS_1(t)}$, $i_{D_1(t)}$,and $v_{DS_1(t)}$is derived as (14), (15) and (16) assuming $\frac{di_{D_1(t)}}{dt} = \frac{di_{D_2(t)}}{dt}$.

$$v_{GS_1(t)} = V_{dr\_off} - (V_{dr\_off} - v_{GS_{1_{miller}}}) \cdot (\frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}) \mathrm{R_{2DEG}} = \frac{\mathrm{v_{DS(t)}}}{\mathrm{g} \cdot (\mathrm{v_{GS(t)}} - \mathrm{V_{th}})} \quad (14)$$

$$i_{D_1(t)} = \mathrm{g} \cdot (V_{dr\_off} - (V_{dr\_off} - v_{GS_{1_{miller}}}) \cdot (\frac{s_2 \cdot e^{s_1 t} - s_1 \cdot e^{s_2 t}}{s_1 - s_2}) - V_{th_1}) \quad (15)$$

$$v_{DS_1(t)} = V_{BUS} - L_{P_1} \cdot \left(\frac{di_{D_1(t)}}{dt} + \frac{di_{D_2(t)}}{dt}\right) - M_1 \cdot \frac{di_{G_1(t)}}{dt} - (\mathrm{L_{D_1}} + \mathrm{L_{QS_1}}) \cdot \frac{di_{D_1(t)}}{dt} \quad (16)$$

Here $s_{1,2} = \frac{\pm\sqrt{b^2-4a}-b}{2a}$,

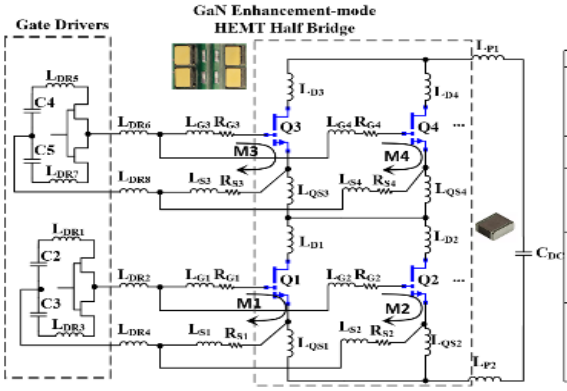
$$a = (R_{G_1} + R_{S_1}) \cdot C_{GD_1} \cdot \left(L_{D_1} + \frac{L_{P_1}}{2} + M_1 + \mathrm{L_{QS_1}} - \mathrm{L_{QS_2}}\right) + (C_{GS_1} + C_{GD_1}) \cdot (M_1 + \mathrm{L_{QS_1}} - \mathrm{L_{QS_2}} + L_{G_1} + L_{S_1})$$

$$,b = 1 + \left(\mathrm{L_{QS_1}} - \mathrm{L_{QS_2}} + M_1\right) g + (R_{G_1} + R_{S_1}) \cdot (C_{GS_1} + C_{GD_1}).$$

Very similar to the di/dt period of switching on process, a higher gate driver voltage (V_{dr}) or smaller gate resistance ($R_G + R_S$) will lead to a faster switching transition, and the quasi-

common-source inductance (L_{QS_1}, L_{QS_2}) has a similar effect as the mutual inductance (M1). If 2DEG is shut off in P2, P3 does not exist.

3.1.3 Parasitic Optimization of GaN Power Modules



Effects of Parasitics

Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} L_{D1-4}	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{S1}-L_{S4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
L_{QS1-6}	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	

Figure 29 Effects and Design Rules of Parasitic Parameters

The fast switching transition of GaN HEMTs results in a high di/dt, which further causes a voltage spike when coupled with the stray inductance in the power loop. Because of the extremely small input capacitance (C_{ISS}) of GaN HEMTs, a large gate-resistor sometimes is applied to slow down the switching transition thereby eliminating the voltage spike across the switch, which however increases the switching loss. To maximize GaN's advantage, minimizing the parasitic inductance is the ultimate solution.

The parasitic inductance is a function of the magnetic flux generated by current, as shown in (17).

$$L = \frac{\Psi}{I} = \frac{\int \vec{B} \cdot d\vec{S}}{I} \tag{17}$$

A multi-layer PCB could significantly reduce parasitics of both the gate-drive loop and power loop by the magnetic-flux-canceling technique, i.e., the direction of the commutation

current on two adjacent layers are opposite so that the generated flux outside the loop gets cancelled. Compared to the direct-bonded-copper (DBC) substrate, the PCB design could easily adopt the multi-layer structure with smaller loop area to achieve an excellent magnetic flux canceling effect.

A half-bridge power module consisting of four high-side and four low-side GaN HEMTs in parallel is shown in Fig.30. Such model is rated at 650V/240A@25oC. The decoupling cap in located under the top and bottom switches to minimize the loop area, which in return reduces the loop inductance. On the other hand, the GaN package of such GaN Systems' devices with no leads or bonding wires, as shown in Fig.25, also tremendously facilitates the parallel connections. Compared with traditional TO-247 package, the stray inductance is reduced by >80%.

Such a half bridge with four GaN HEMTs in parallel is modeled in ANSYS Q3D, and the power-loop and gate-drive-loop inductance are evaluated by Finite Element Analysis (FEA). The power-loop inductance of the proposed design is only 0.7 nH. For each paralleled GaN HEMT, its quasi-common source inductance is <0.2 nH, and the gate-drive-loop inductance is 4.2 nH. Effectiveness of such parasitics reduction will be verified later on the double-pulse tester (DPT).

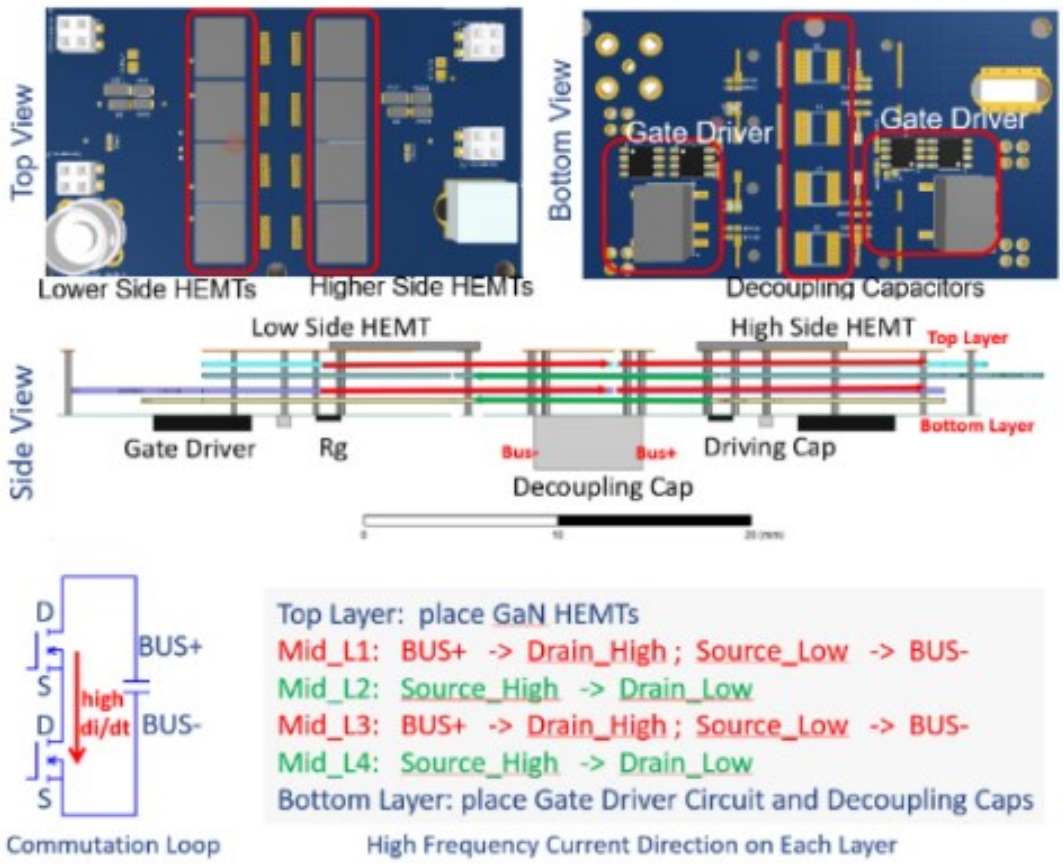


Figure 30 Layout of 650V/240A GaN HEMTs based Half Bridge

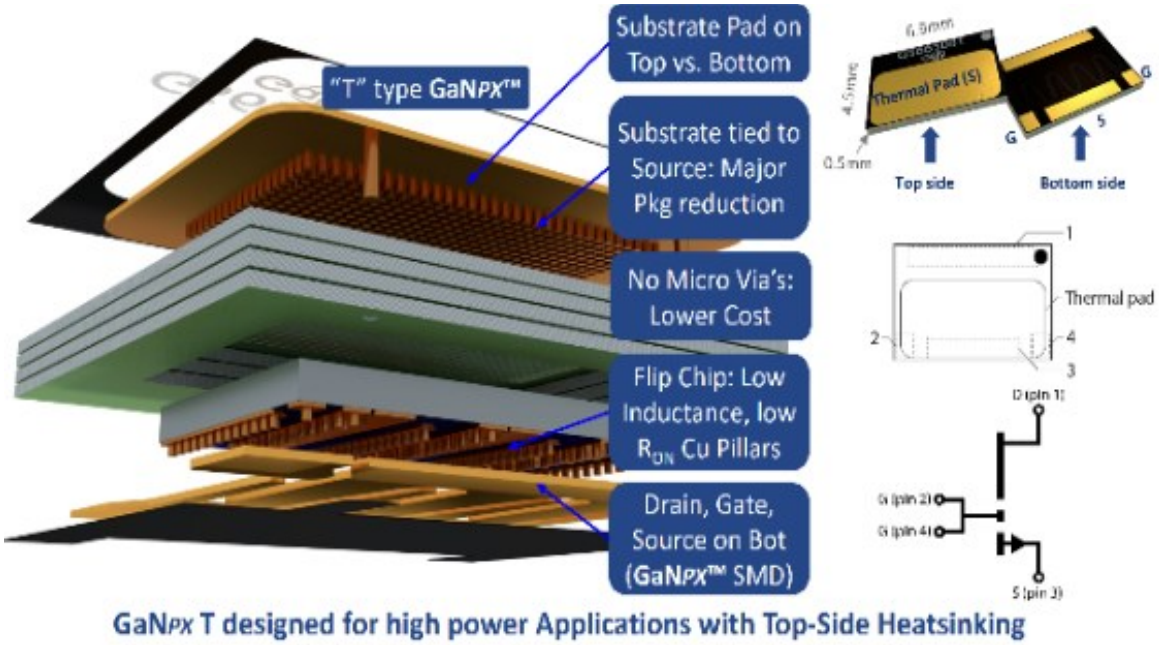


Figure 31 GaNpxTM Packaging

3.1.4 Gate Driver Design

Candidates of the gate-drive circuit are shown in Fig.32. To mitigate the miller affect, a miller clamp circuit is proposed as Fig.32. When the device is fully switched off, the miller clamping transistor is on to bypass the miller charge. Fig.33 is using different gate parameters to vary the switching-on/off speed. It requires two separate output terminals though. The gate-drive circuit in our system is shown in Fig.34. Changing Ron and Roff will alter the switching on and off speed.

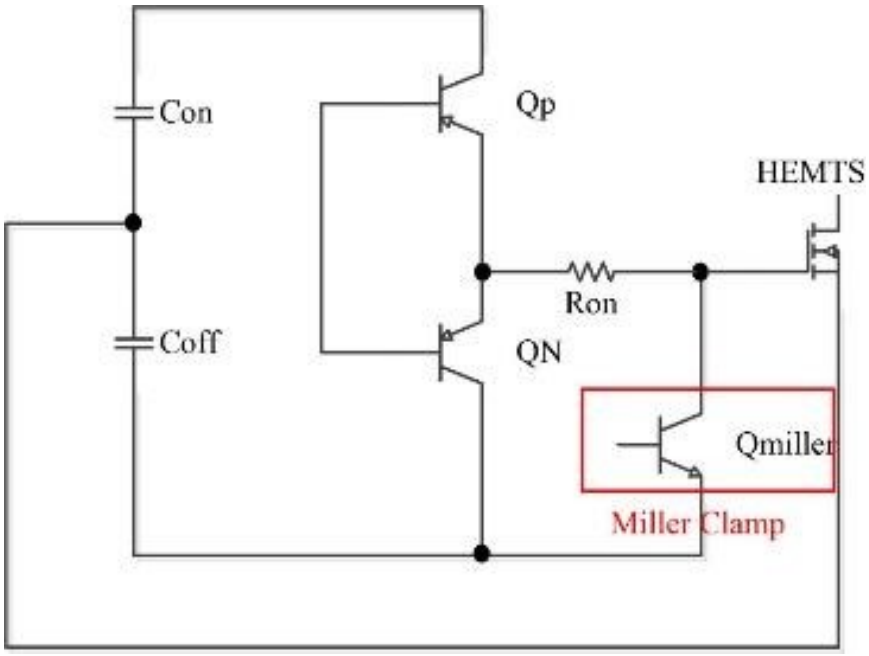


Figure 32 Miller Clamp Circuit

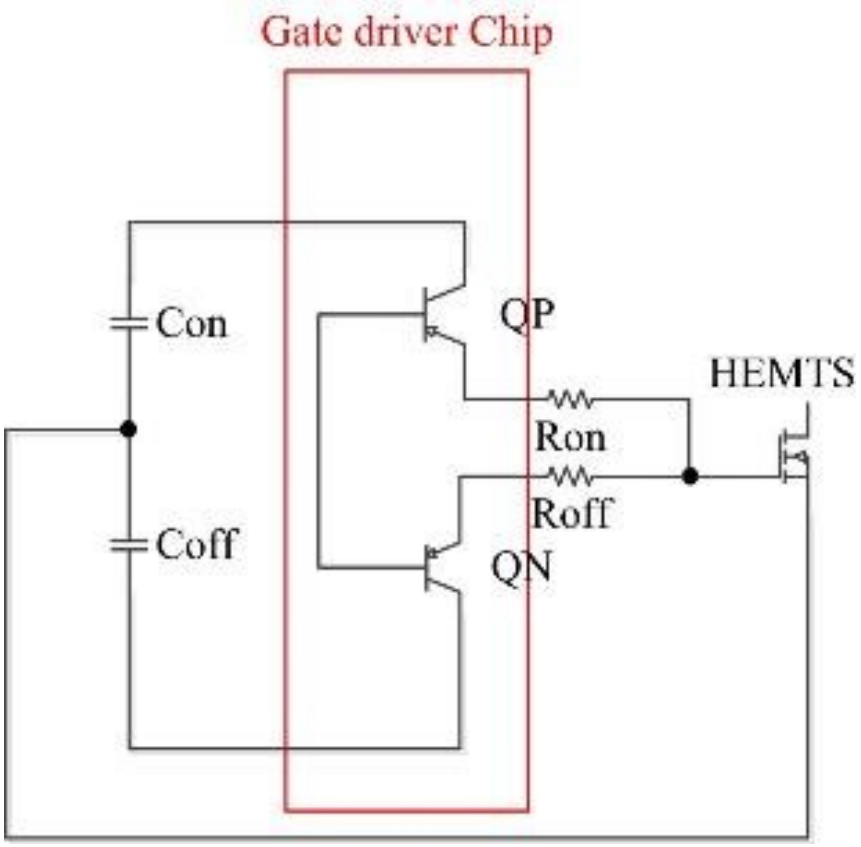


Figure 33 Two-gate-terminal Circuit

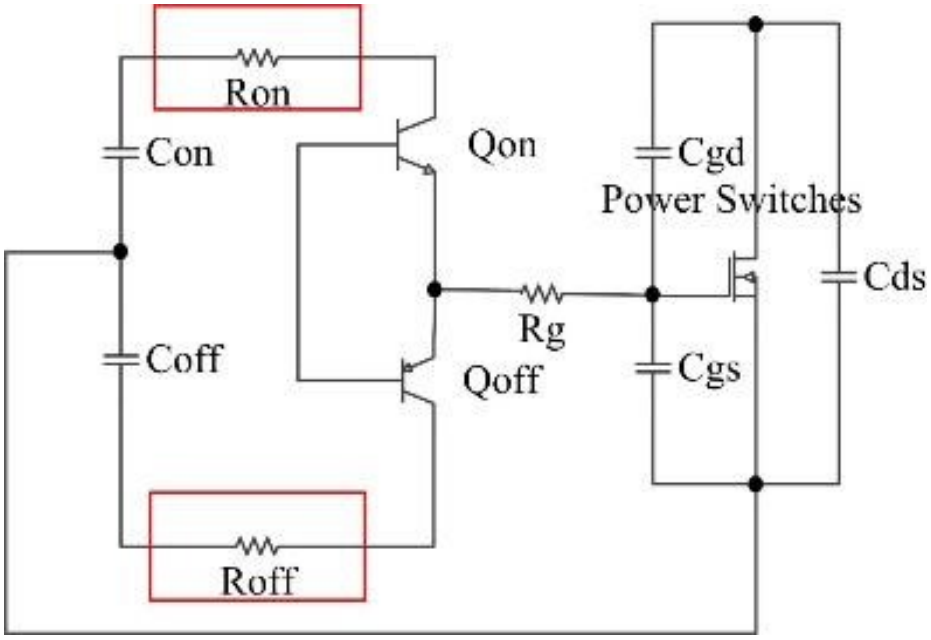


Figure 34 Gate-Drive Circuit used for GaN HEMTs

Compared to other approaches, the gate-drive circuit shown in Fig.10c has the potential to integrate the gate-drive chip (Qon, Qoff and Rg) with GaN devices on the same substrate, further reducing the gate-loop inductance. To vary the switching speed, only changing the two external resistors (Ron and Roff) is required, providing a very high flexibility.

3.1.5 Experimental Verification

A half bridge power module using four GaN HEMTs in parallel is shown in Fig.35. Test carried out on the DPT at ~60A shows the perfect balancing between GaN HEMTs in both steady state and switching process, as shown in Fig.30. This verifies the effectiveness of the gate-loop circuit design. We further pushed the turn-off current up to 240A, as shown in Fig.31. The observed voltage spike is only 52V, validating the effectiveness of reducing the power-loop inductance.

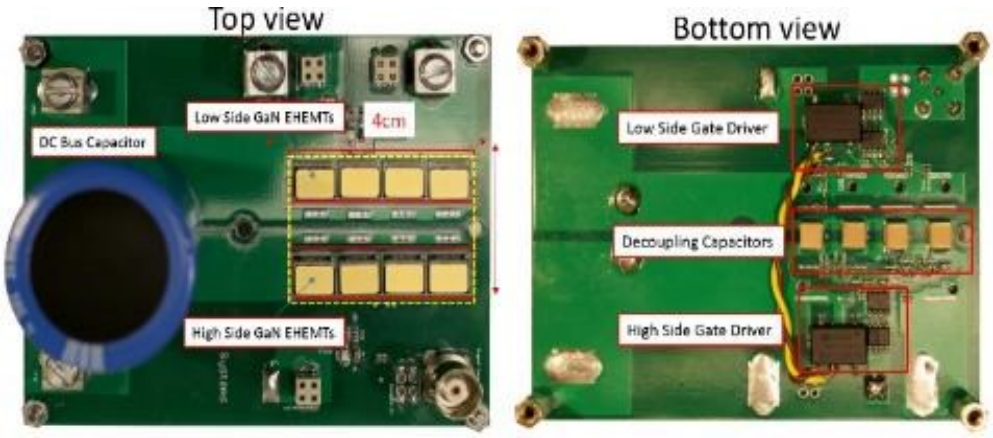


Figure 35 Prototype of 650V/240A GaN HEMTs based Half Bridge

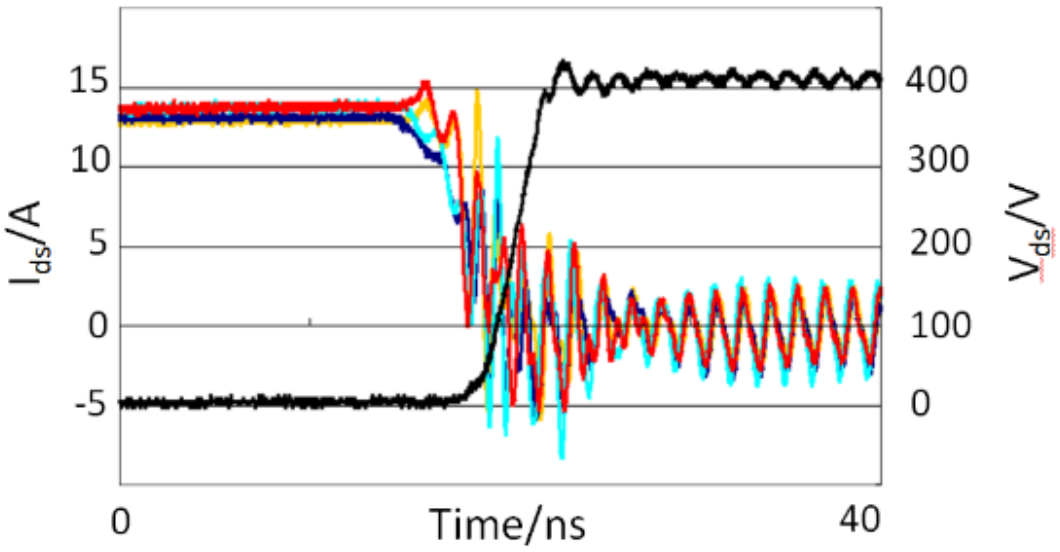


Figure 36 Current Balancing Among Four Paralelled Switches.

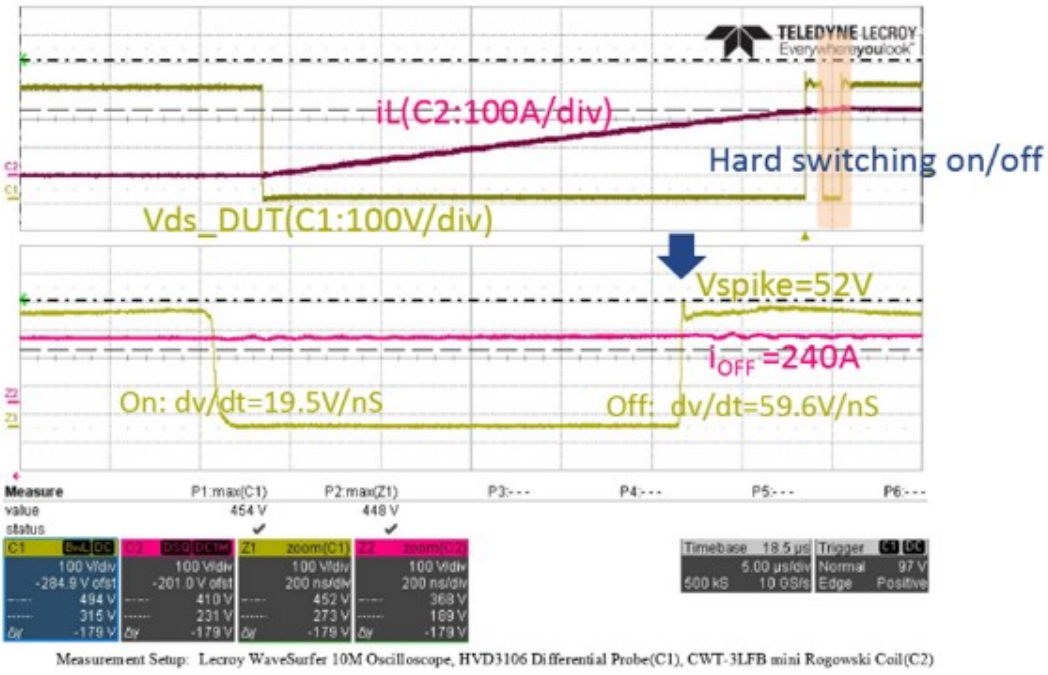


Figure 37 Double Pulse Test Waveform @400V/240 A

3.1.6 Applying Gan-HEMTs Power Modules in High-efficiency Systems

The above effort is to minimize the harmful effect of parasitics. In this section, focus will be shifted to increasing the system efficiency. GaN HEMTs will be applied to two DC/DC converters, one is using the ZVS turn-on technique, the other is using the hard switching-on. Both

converters adopt paralleled GaN HEMTs. The goal is to further investigate the interaction between GaN and peripheral circuits during the transient processes in the actual system.

3.1.7 Soft-switched DC/DC Converter

Even though GaN HEMTs have superior performance over Si devices, it still has much more switching-on loss than switching-off loss. When possible, ZVS turn-on is still preferred even when using GaN.

As shown in Fig.38, when switches in the same leg are both off, the energy stored in the external inductor begins to discharge C1 and charge C2. Here C1 and C2 are the switch output capacitance. Once C1 is fully discharged, Switch_1 is ZVS on, resulting in no switching-on loss.

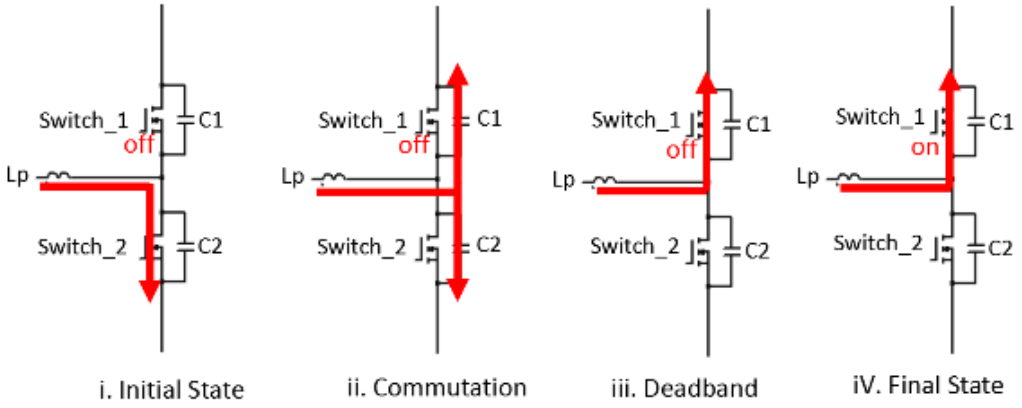
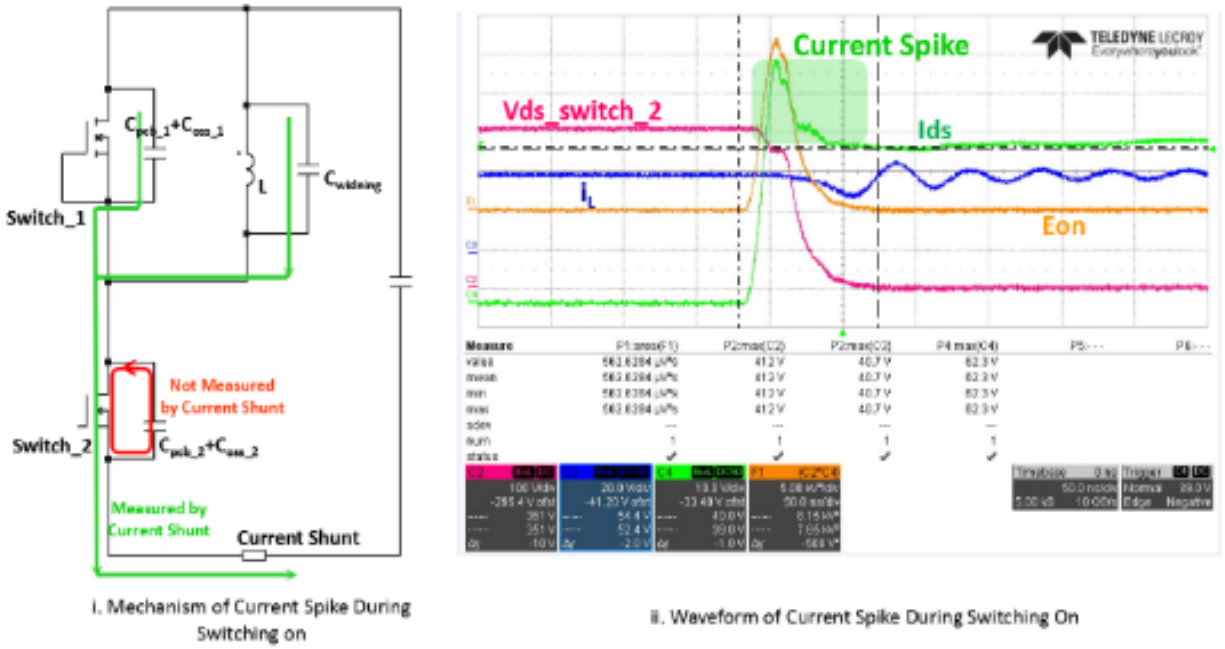


Figure 38 Impact of Coss on Zero Voltage Switching Process

To secure ZVS, the inductor current must be high enough to deplete the overall output capacitance (GaN HEMTs + PCB board) within the dead time. Determination of the dead time and minimum required load current requires an accurate extraction of parasitic capacitance. Note when placed on the PCB, parasitic capacitance introduced by the PCB and other components is not negligible, given that Coss of the GaN HEMT is ultra-small. Such parasitic capacitance could be extracted after modelling the whole PCB in ANSYS Q3D. More accurately, an experimental method using the DPT is preferred, shown as Fig.39. The current spike measured during hard

switching on lower switches is contributed by charging the output capacitance of top switches. The integral of such a spike current divided by the DC-bus voltage indicates that equivalent capacitance is about 2nF for top switches. Therefore, the overall capacitance of the whole H-bridge is 4nF. Note such method is only effective to GaN instead of Si/SiC. Since no body diode exists inside GaN HEMTs, such current spike is solely introduced by charging the Coss without including the diode reverse-recovery current.



i. Mechanism of Current Spike During Switching on

ii. Waveform of Current Spike During Switching On

Figure 39 Current Spike Measurement with Double Pulse Test Platform

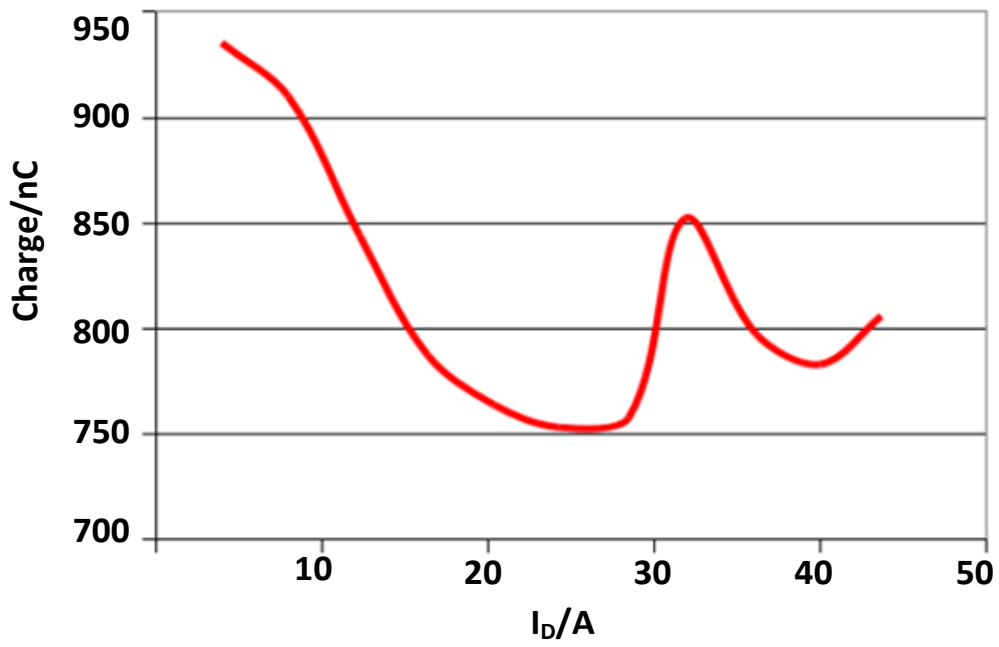


Figure 40 Coss Charge @ Different Load Current

In the reverse conduction mode, the drain will behave as the source and the source will act as the drain. When VGD is higher than Vth_GS, the switch turns on. The voltage drop across the switch is

$$V_{SD} = V_{th\_GD} - V_{GS\_off} + I_D * R_{DSon} \tag{18}$$

Since the gate threshold of GaN HEMTs is ~2V while a negative VGS_off = -5.2V is added to reduce the switching loss, (18) indicates a voltage drop of ~7V in the reverse conducting mode, much larger than Si devices. A large dead time for GaN HEMTs will certainly result in the increment of the dead-band loss. On the other hand, if the dead time is too small, the switch will lose ZVS since no enough time is given to deplete the top-switch Coss, as shown in Fig.40, which results in the increment of the switching-on loss.

One argument is the possibility to drop the dead-band loss by anti-paralleling a SiC Schottky diode to the GaN HEMT. Firstly, such an external diode will bring additional junction capacitance and introduces the reverse-recovery current in hard switching applications. An

experimental comparison between w/n anti-parallel diode C3D10065A to GaN HEMTs is shown as Fig.41. Obviously adding an anti-paralleled diode will result in the significant increment of the switching-on loss, unless the ZVS turn-on is adopted.

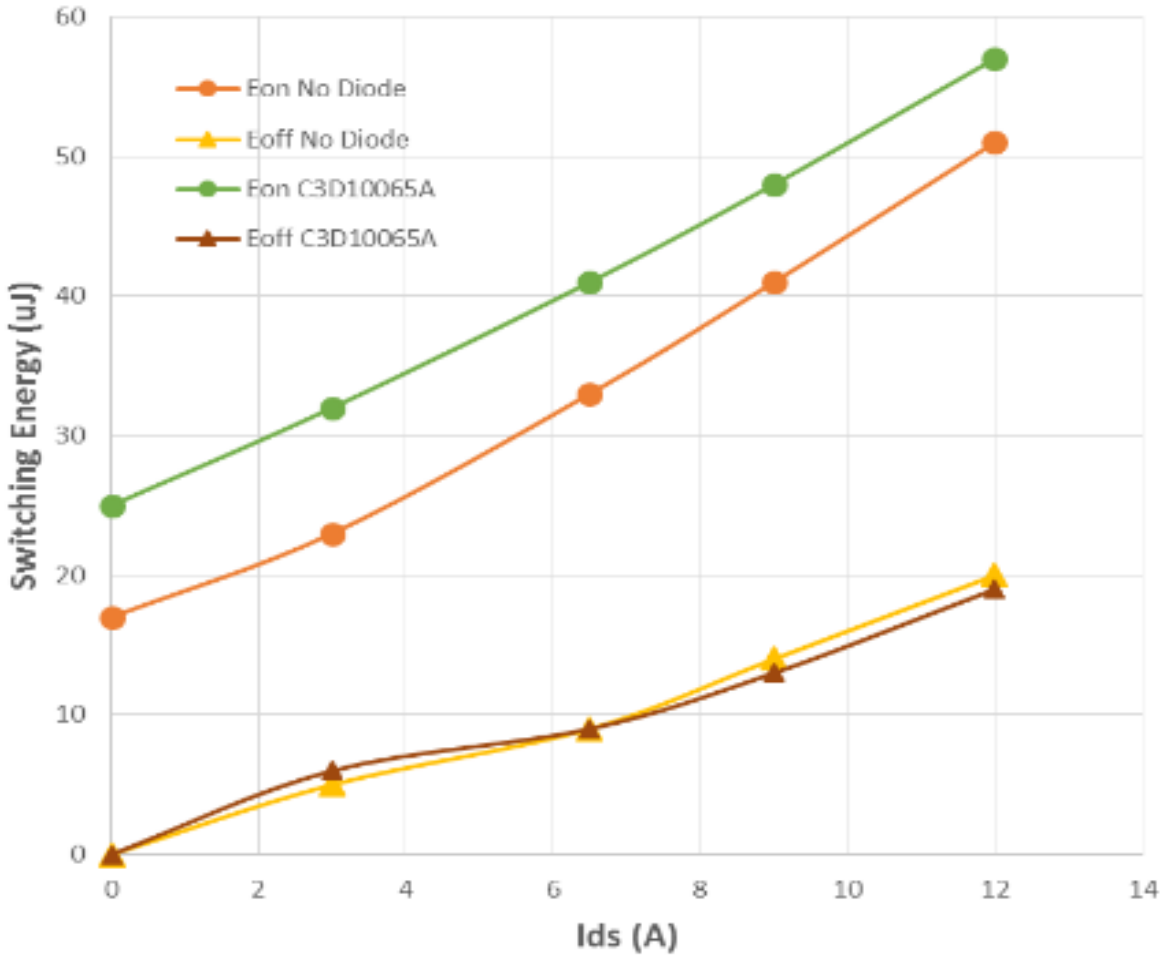


Figure 41 Switching-loss Comparison w/n Anti-Parallel Diodes

Secondly, even with ZVS turn-on, the TO-247/220 packaged diodes are much bulkier than HEMTs, which will complicate the heat sink design and obstruct the reduction of the loop inductance.

3.1.8 Hard-switched DC/DC Converter

To apply 650V GaN HEMTs to an 800V/400V DC-DC converter, a multi-level topology is an excellent candidate, as shown in Fig.42. When S1 and S4 are turned on, the power is flowing from Vin to Vo. When S1 and S4 are off, the inductor current will freewheel through S2 and S3. Essentially this circuit acts as a hard-switched bidirectional buck/boost converter. Two 30A switches are paralleled.

In addition, a conventional buck converter using 1200V SiC MOSFETs is the backup candidate, as shown in Fig.43. Assume all converters are running at 500kHz. The system loss breakdown of two different systems is shown as in following figure, indicating that the 650V GaN HEMT has great advantages on both the conduction and switching performance.

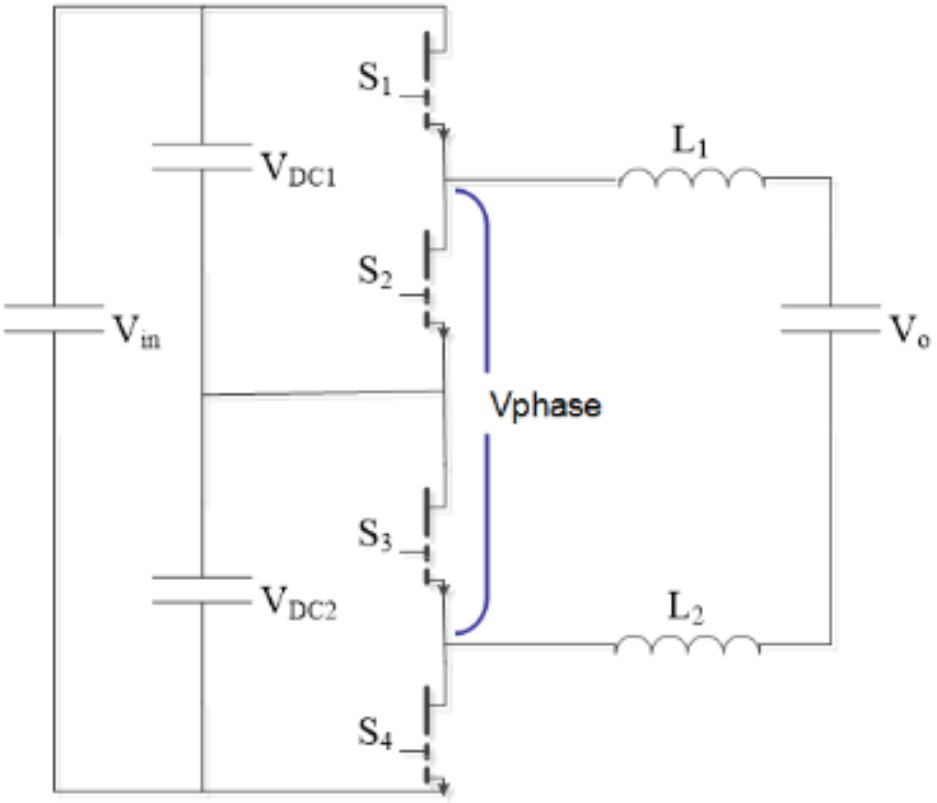


Figure 42 The Three-level Topology with 650V GaN HEMTs

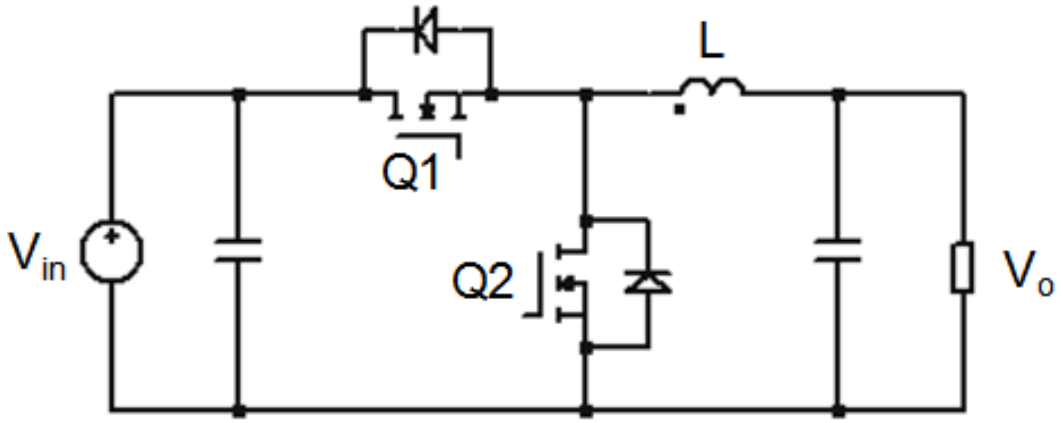


Figure 43 The Conventional Buck Converter with 1200V SiC MOSFETs

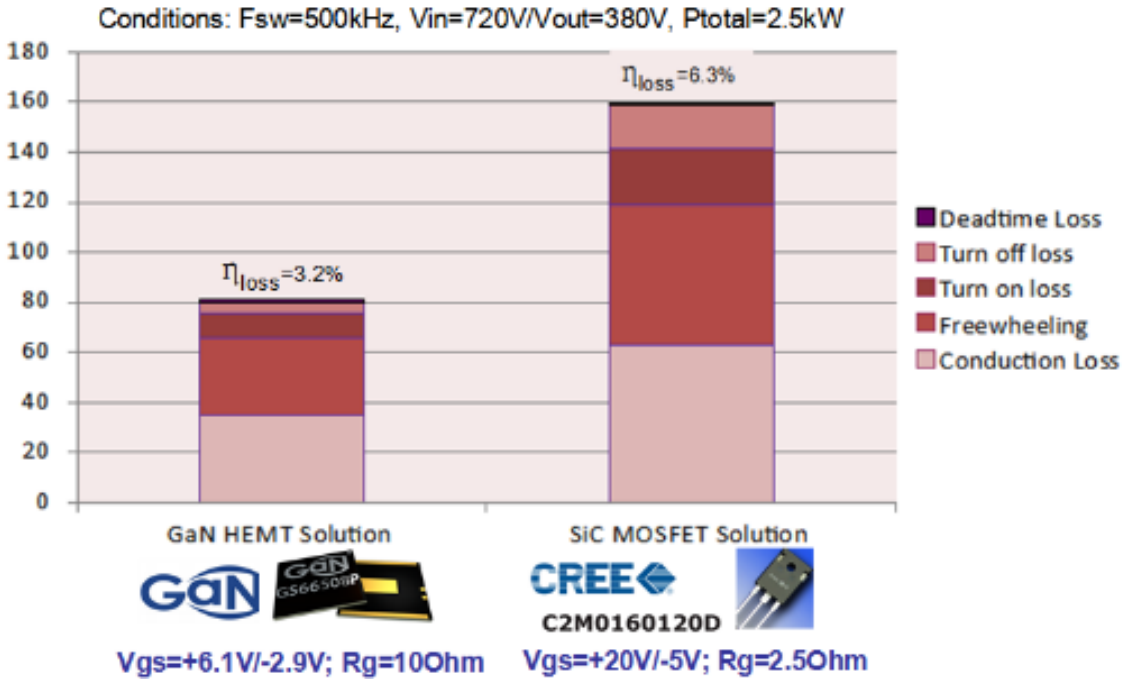


Figure 44 System Loss Breakdown Comparison between Two Solutions

Such comparison of these two hard-switching converters is not aiming to compare these two types of WBG devices, given 1200V devices usually have much worse conducting and switching performance than low-voltage switches. This case validated that 1) GaN HEMTs could be used in hard switching, 2) external diode will increase the switching loss. Shown in Fig.44, the

increment of the switching-on loss is due to the reverse recovery current of Q2 being added to the Q1 turn-on current.

3.1.9 GaN Design Prototype and Experiments

Table 2 Values of key parameters

Symbol	Definition	Values
	Switch equivalent capacitance	2nF
	DC-bus capacitance	10μF
L	Transformer leakage inductance reflected to the primary	11.5μH
n	Transformer turn ration	1:1
f_{sa}	Ceiling switching frequency	500kHz
V_{in}	Nominal input voltage	208VAC
V_{out}	Output voltage	200~450VDC
P	power	0~7.2kW
I_o	Nominal output current of each module	20A

A. Switch Test. As shown in Fig.45, a DPT system with four GaN HEMTs in parallel was built with exactly the same parasitics as the final charger. Additional current shunt resistors are applied to measure the switching off current. The experimental waveform with Ioff=56A @VDC=400V is shown as Fig.46, indicating the currents are balanced well with a small voltage spike.

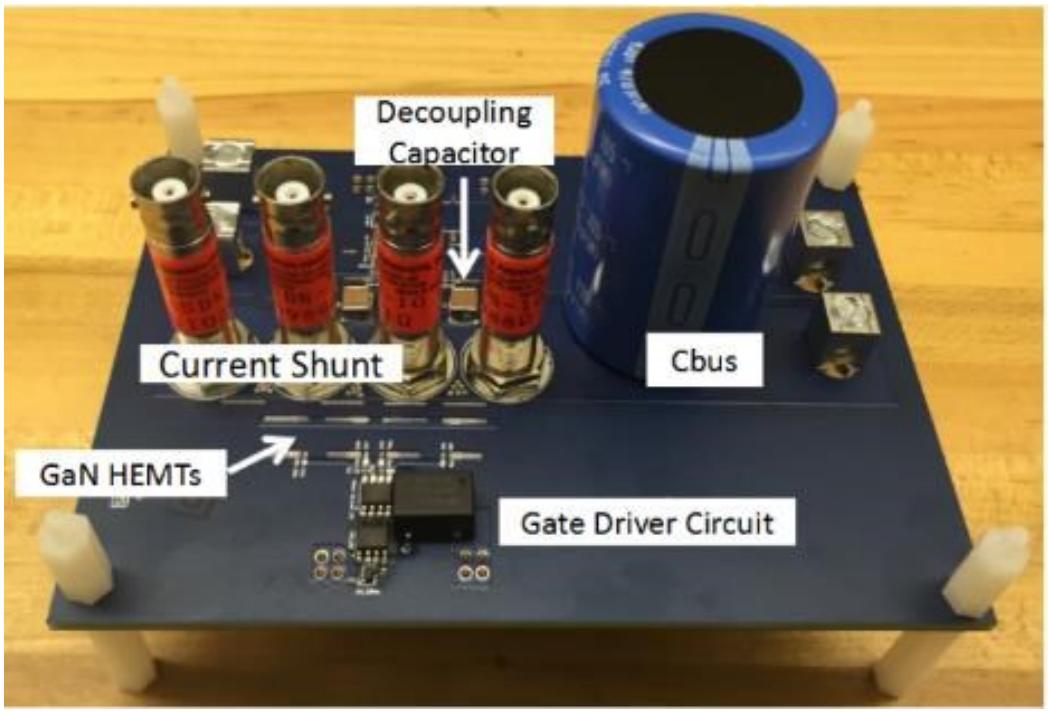


Figure 45 DPT with four GaN HEMTs in parallel

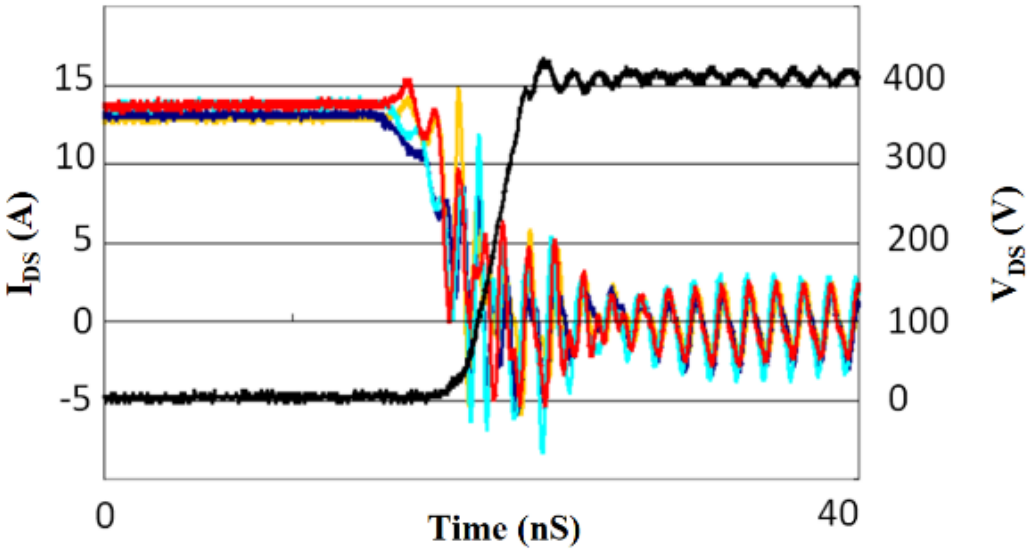


Figure 46 Current Sharing among Paralleled HEMTs @ 400V/56A During the Turn-off Process

B. Single-phase Module Test. A single-phase on-board charger is prototyped as Fig.47. The red block in Fig.48 is the DC-bus capacitor, much smaller than DC links in other chargers. All three PCBs are stacked up together to form a compact package. The overall module includes

the input EMC choke and output capacitor as well. The charger has the dimension of 22*15*6.5cm3, yielding a power density of 3.3kW/L with the enclosure and heatsink. The system input and output waveform at 7.2kW is shown as Fig.49. The measured power factor =0.997. The waveform of the DAB stage at battery voltage of 400V and 200V is shown as Fig.50, respectively. Each bottom plot shows the zoomed-in highlighted area. At the high output voltage, the secondary-side voltage becomes three-level, while at the low output voltage the primary-side voltage is three-level, which is aligned with the SDPS and PDPS design Fig.51.shows the TPS control at the light-load condition, where the grid-voltage distortion disappears, validating its effectiveness. Fig.52 shows the distribution of the grid-side current harmonics. The overall THD is ~6%, slightly higher than the requested 5%, which should be the focus of the future optimization.

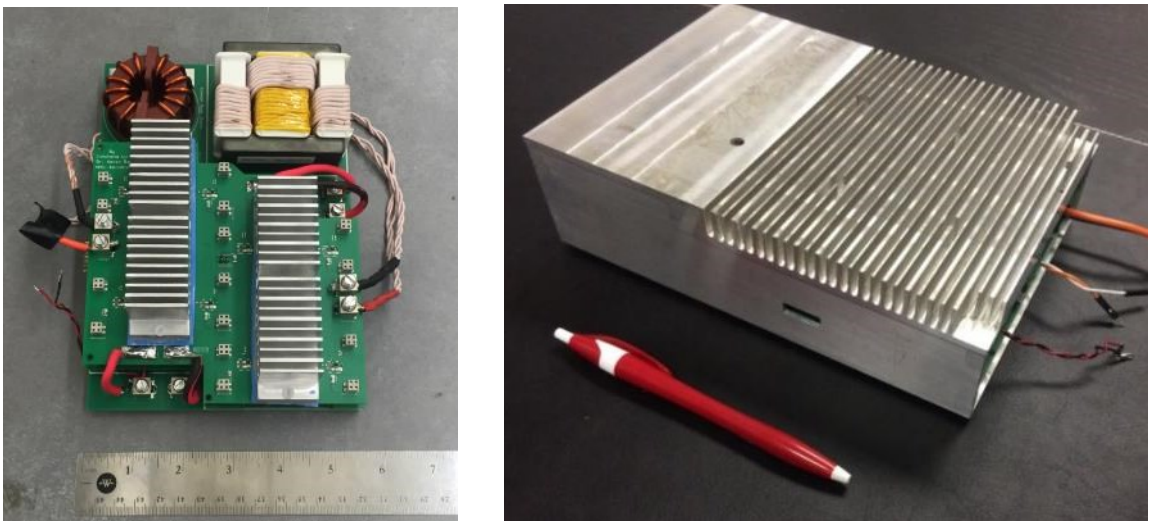


Figure 47 Prototype of the Single-phase Charger (left- the charger, right-charger with the enclosure)

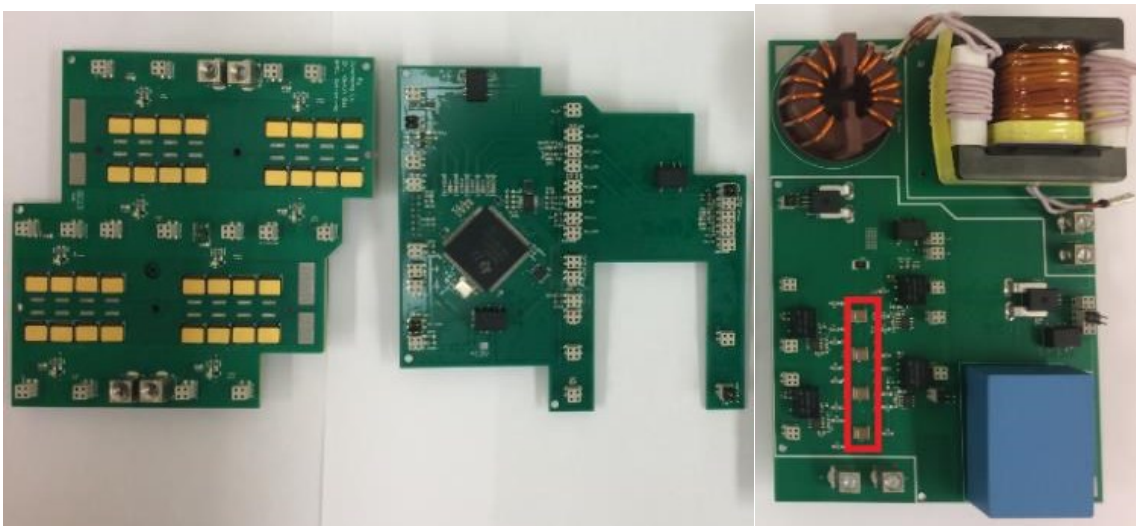


Figure 48 PCBs of the Whole Charger (from left to right: GaN HEMT PCB, control PCB and rectifier PCB)

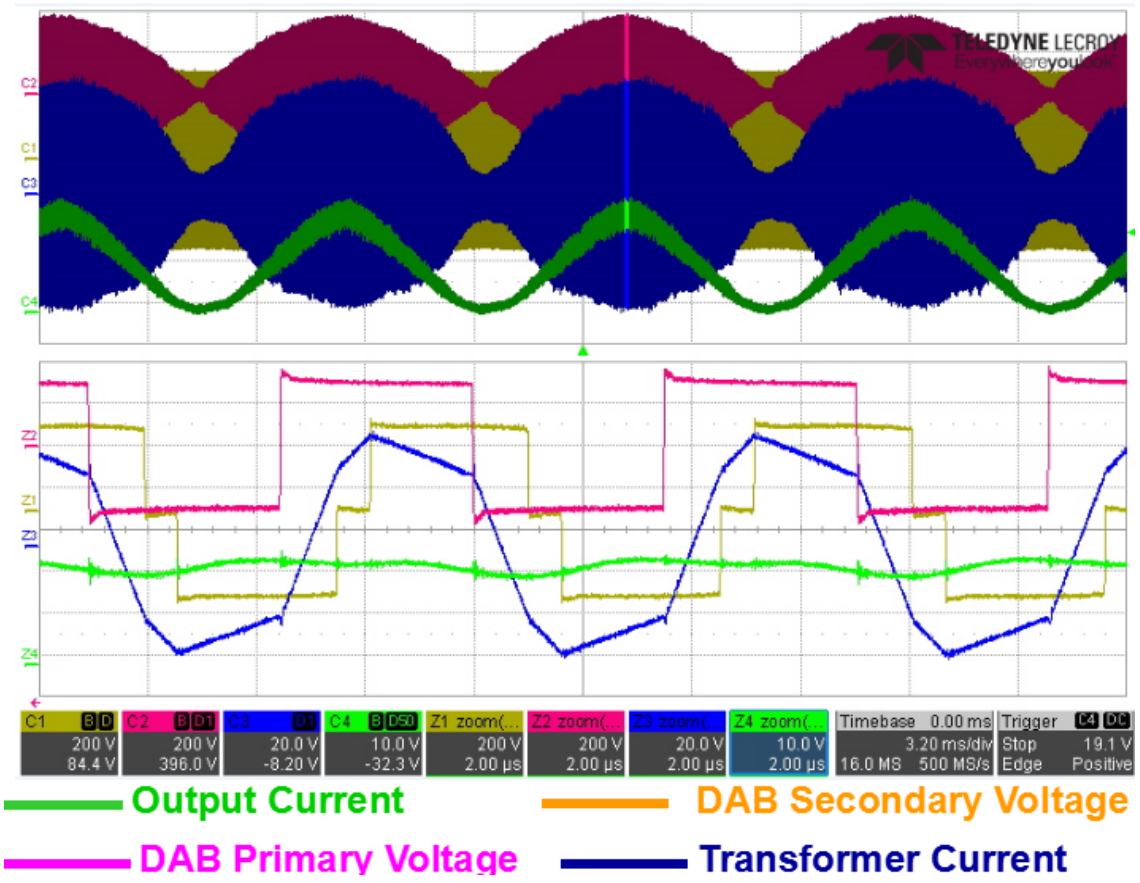


Figure 49 DAB Stage Waveform of the Charger @Vo=400V, P=7.2kW

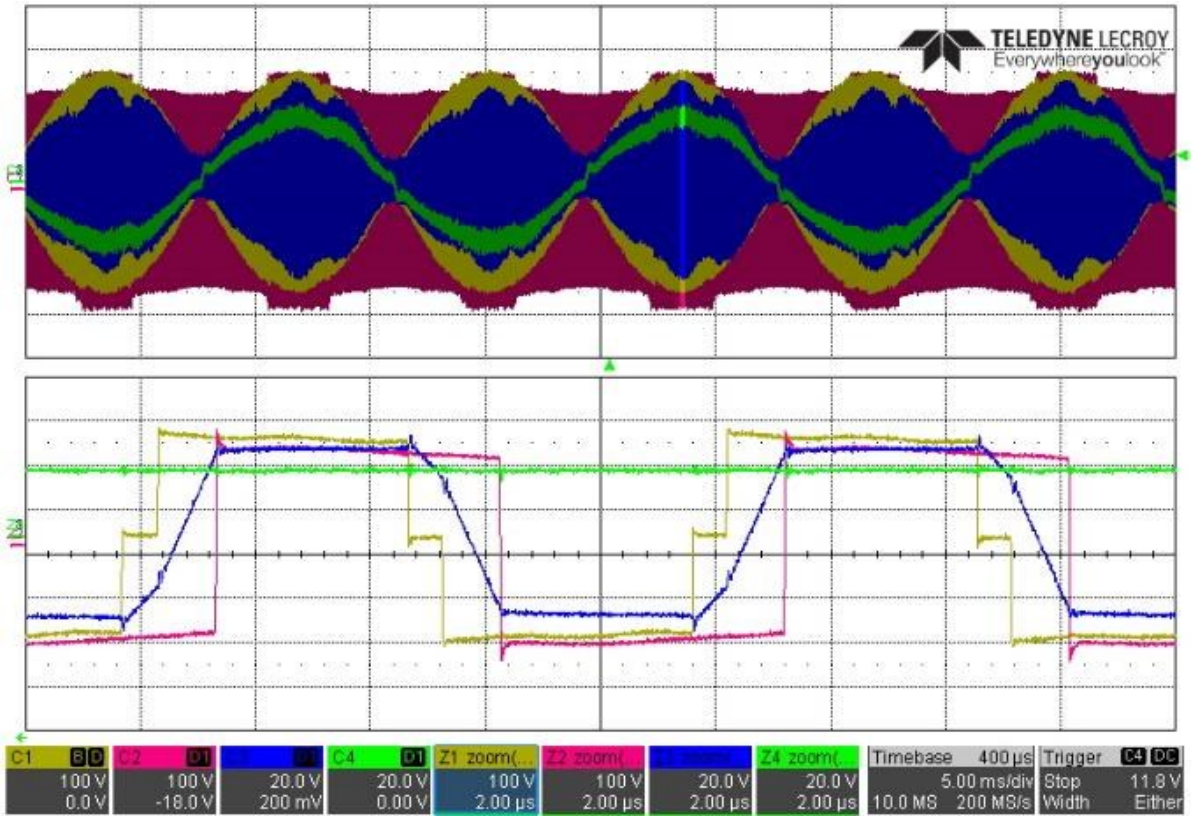


Figure 50 DAB Stage Waveform of the Charger @Vo=200V, P=4kW (yellow-DAB primary voltage, 100V/div; purple-DAB secondary voltage, 100V/div;

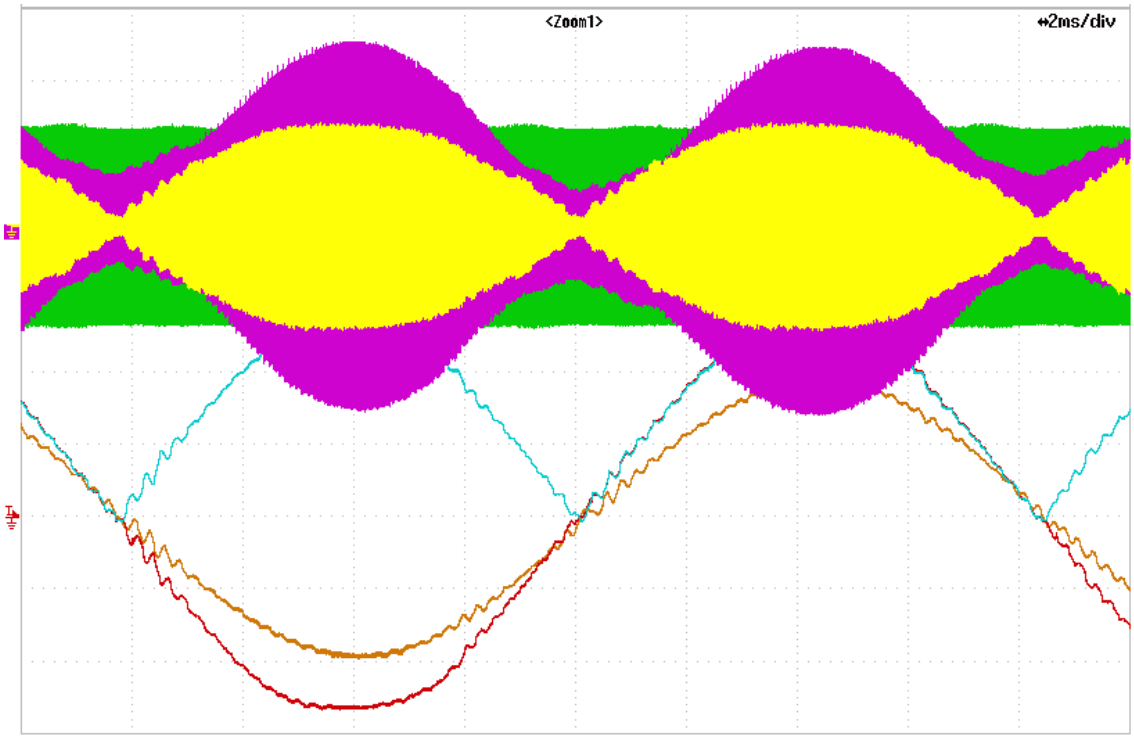


Figure 51 TPS control at the 100W (yellow-transformer primary voltage, 100V/div; purple-transformer current, 1A/div; green-transformer secondary voltage, 100V/div; red-grid voltage 100V/div; brown-grid current 1A/div)

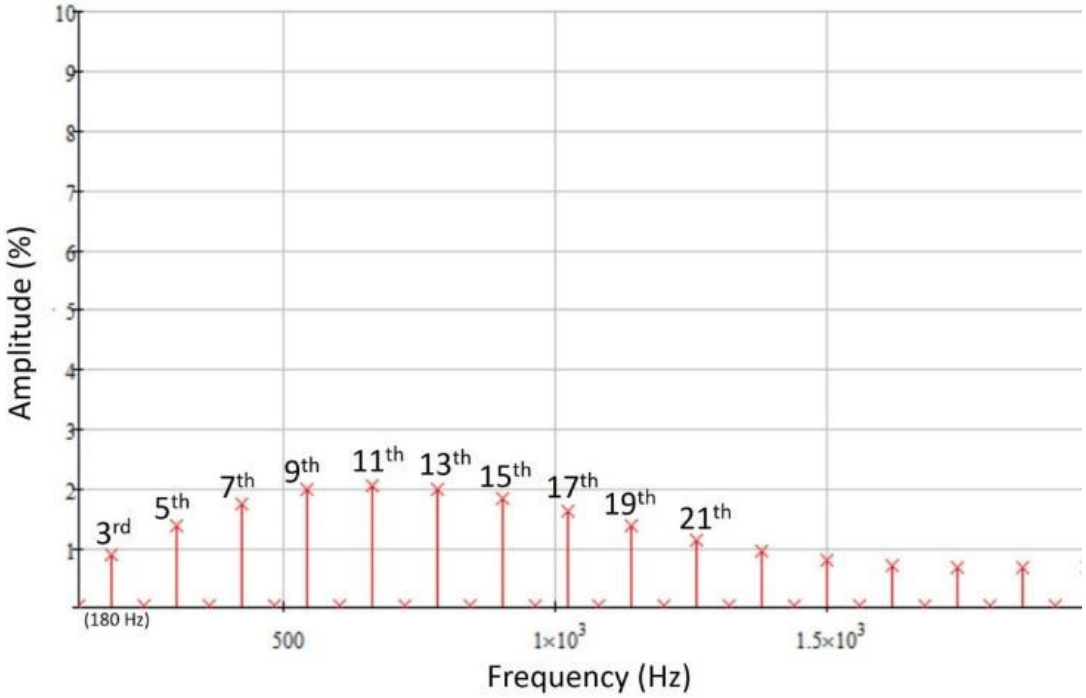


Figure 52 grid-current-harmonics distribution

Three-phase Charger Test. The overall three-phase charger was prototyped, as shown in Fig.53. The overall efficiency, power factor and power density are the same as the single-phase charger. A 5kW test shown in Fig.54 indicates the overall current ripple is small (yellow line), even though the output current Ioa, Iob and Ioc have 120Hz ripples. Such result validated the design of the charger. Fig.55 is the comparison of experimental efficiency between the proposed charger and Brusa Si-version charger. Fig.56 is the loss breakdown, indicating the transformer and switch conduction loss is more dominant. Given the grid-side AC/DC part has a low switching frequency and low channel resistance, the rectifier loss is negligible. Fig.57 is the head-to-head comparison of the power density.

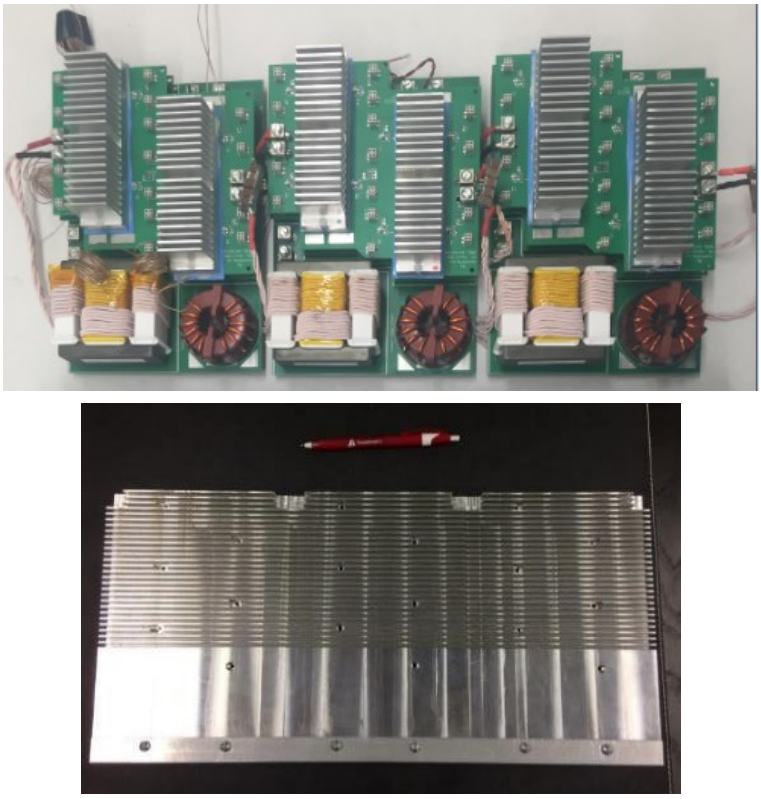


Figure 53 The Three-phase Charger Using Three Single-phase Modules (left) and Its Enclosure (right)

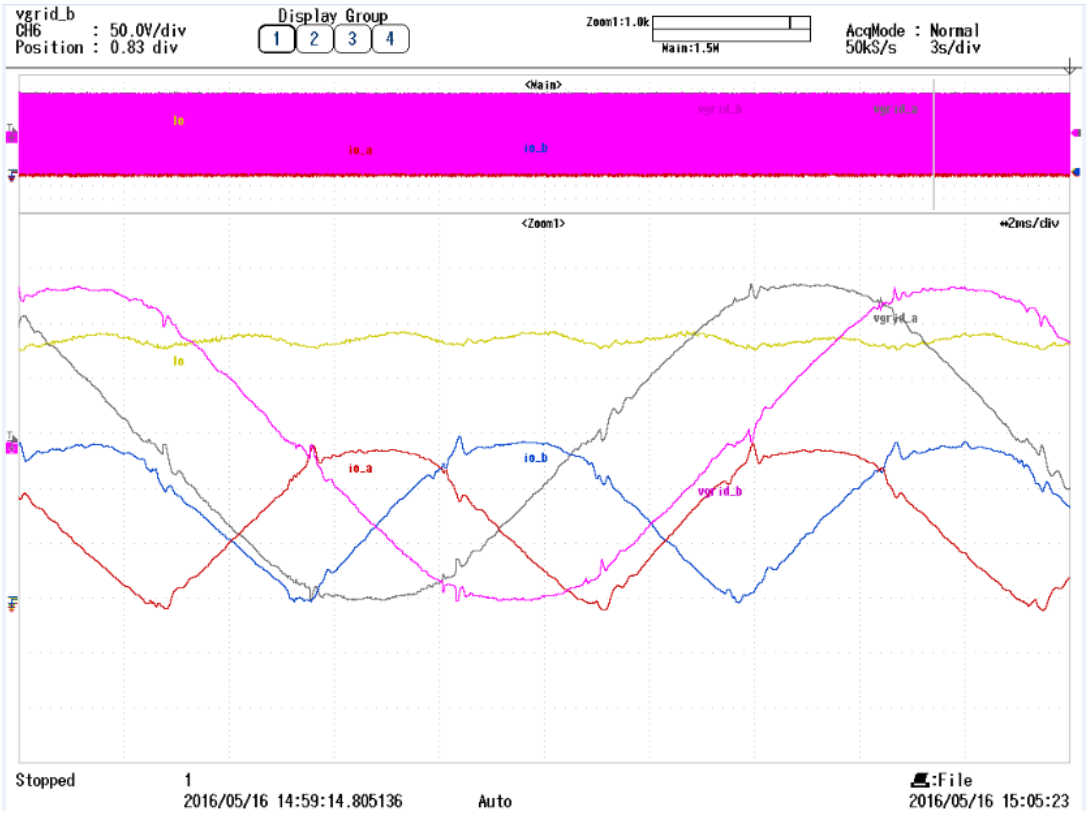


Figure 54 Three-phase-charger Test Result @5kW (yellow-Io: 3A/div; Ioa, Iob, Ioc: 3A/div; grey&purple-grid phase voltage Vgrid_a&b: 100V/div)

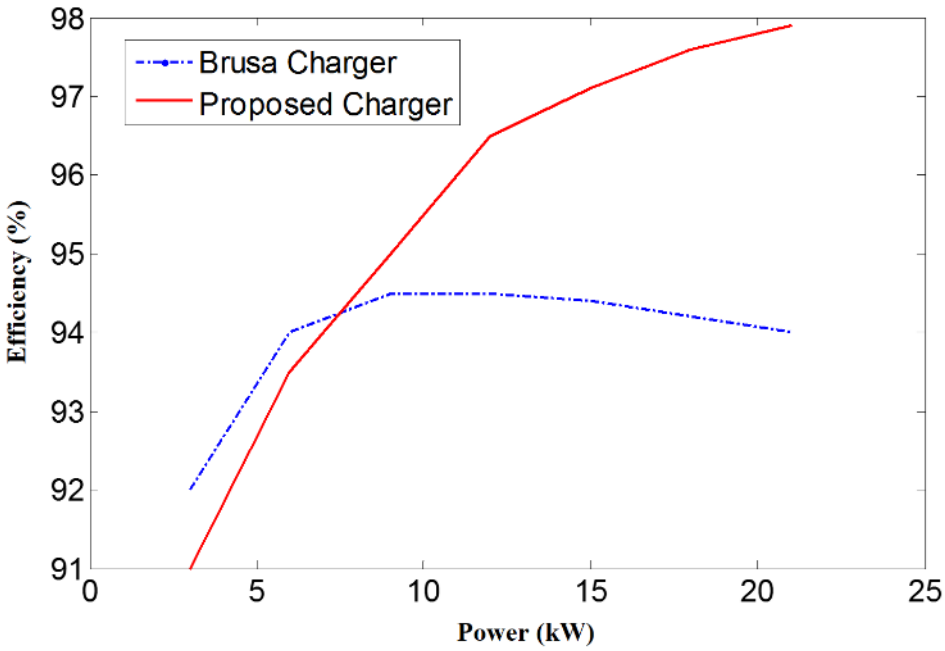


Figure 55 Efficiency Comparison (GaN vs Si)

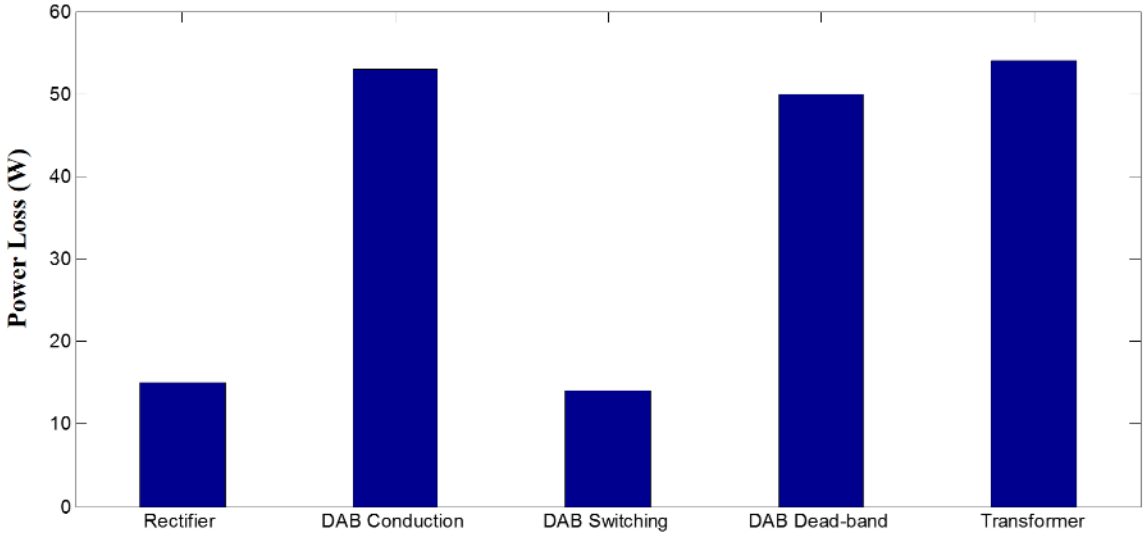


Figure 56 Power loss breakdown (per phase)

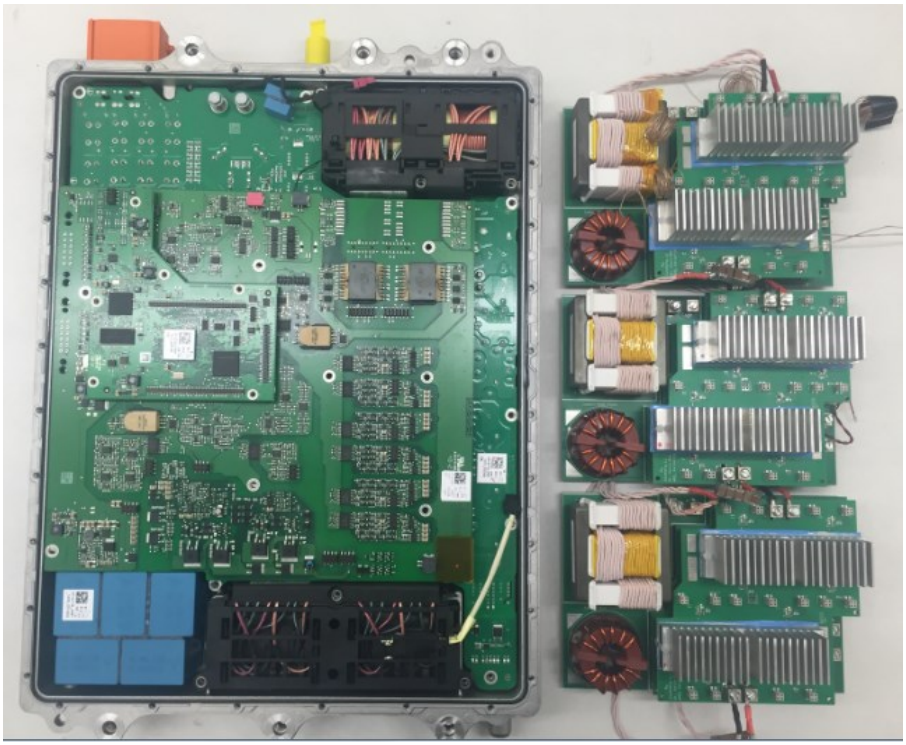


Figure 57 Power Density Comparison (left- Si Charger of 2kW/L, right- GaN charger of 3.3kW/L)

3.2 Control Strategies Optimization of DAB

3.2.1 Introduction

It is believed that wide-bandgap (WBG) devices, such as SiC MOSFETs and GaN HEMTs, are excellent candidates for high-efficiency and high-power-density applications, e.g., on-board chargers (OBCs) for electric vehicles (EVs) due to their ultra-fast switching transitions and low thermal impedance. Even so, to maximize their advantages over conventional Si devices, soft switching strategies, e.g. zero-voltage-switching (ZVS) turn-on are still highly rewarding, given that these WBG device's switching-on losses are still dominant over their switching-off loss. The obstacles for EV OBCs to realize ZVS turn-on remain as:

1) complex circuitry topologies. The safety requirements of on-board vehicle charging call for isolation between the grid and vehicle. An AC/DC + isolated DC/DC circuit topology is a

common candidate [73-74], as shown in Fig.58. Such a battery charger consists of a rectifier stage and a dual-active-bridge (DAB) stage. Constantly securing ZVS for all 12 semiconductor switches is challenging. The majority of the EV chargers employ the grid-side AC/DC converter (M_1~M_4) to handle the control of the power factor [75-76], which potentially yields a large grid-side inductor, a bulky DC-bus capacitor, and a high switching losses. Another control option is to run the grid-side H-bridge at the line frequency, e.g., M_1~M_4 running at 60Hz as synchronous rectifiers to flip the negative grid voltage into positive. In this way, expensive semiconductors are saved while only regular Si MOSFETs with small R_{DSon} are needed. Not only the switching loss but also the passive components are minimized. Both the power factor (PF) and power transfer would then be controlled by the DAB stage solely through varying the phase shift and switching frequency of P_1~P_4 and S_1~S_4 [77-80]. Such an approach was reported to realize a GaN based OBC with >97% efficiency and 4 kW/L power density [81], while majority of the EV chargers have efficiency of ~94~95%[82]. It is reported in [83] that a 96%-efficiency charger was built, but the power density is lower (2.3kW/L).

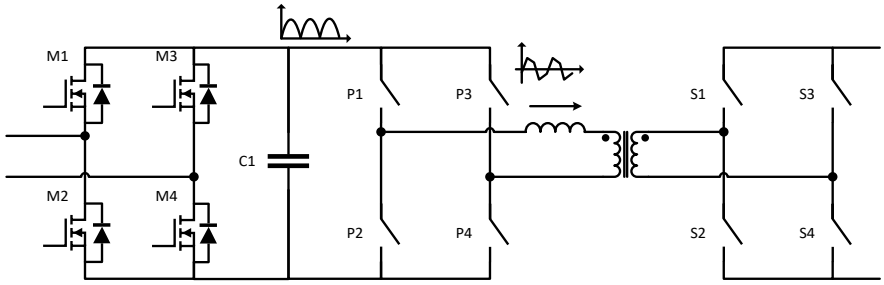


Figure 58 Topology of the on-board level-2 battery charger used in this paper

2) wide input and output voltage range. By using the modulation strategy shown in [84], the OBC faces a wide-input range (0 to grid peak value) and a wide-output range (200~450 VDC, battery voltage) at the DAB stage. The conventional single-phase shift (SPS) control and dual-phase-shift (DPS) will lose the ZVS at the light load. [77-81] utilized a variable switching-

frequency (VSF) DPS algorithm to secure ZVS. [85] further utilized the semiconductor switch output capacitance and charge to determine the ZVS boundary. However the light-load performance of the DPS algorithm is still subject to further improvements. When the power is low, distortion of the grid-current appears, especially at the zero-crossing points. Furthermore, the VSF DPS algorithm needs to vary the switching frequency and switch between primary phase-shift and secondary phase-shift methods at all times. Despite various effort of securing the ZVS for SPS or DPS [86-88], it can be rather complicated to implement in practice.

Based upon [82], this paper proposes a multiple-phase-shift (MPS) modulation strategy, which solves the light-load grid-current distortion by evolving the DPS control to a subset of a triple-phase-shift (TPS) control. Section II compares such newly proposed control with DPS, illustrating its simplicity and effectiveness of securing ZVS turn-on and realizing unity power factor at light load. In Section III, the proposed MPS was verified in a SiC-based 7.2 kW charger from light-load to heavy-load operation. To further enhance the light-load efficiency, i.e., reducing the power loss caused by the circulating current and minimizing the current stress, previous work in [88-91] could be references, however, mostly focusing on the switch current without considering the actual switch characteristics. Therefore, only the conduction loss was considered in previous literatures. In this part we adopted a multi-objective optimization [92] to seek the optimal switching frequency. The double-pulse-test (DPT) results of the switch are incorporated to determine the optimal switching frequency at different power levels.

3.2.2 VSF DPS, TPS & MPS

In this section, we will first summarize two similar modulation strategies used with the DAB, namely, the DPS and TPS, based upon which we propose MPS by combining the TPS and DPS together. VSF DPS was first proposed in [76], which can secure the ZVS turn-on of all

switching events when the grid input voltage is less than the reflected battery voltage. Based upon the work presented there, the authors further enhanced the control to fully cover the wide-input and wide-output range of the battery charger. This was done through dividing the modulation strategy into SDPS (secondary DPS) and PDPS (primary DPS).

SDPS Control when |vi(t)| < nVo

Here $v_i(t)$ is the instantaneous value of the grid voltage, V_o is the battery voltage, and n is the transformer turn-ratio. Switching period T and phase shift times t_r and t_w are shown in Fig.59.

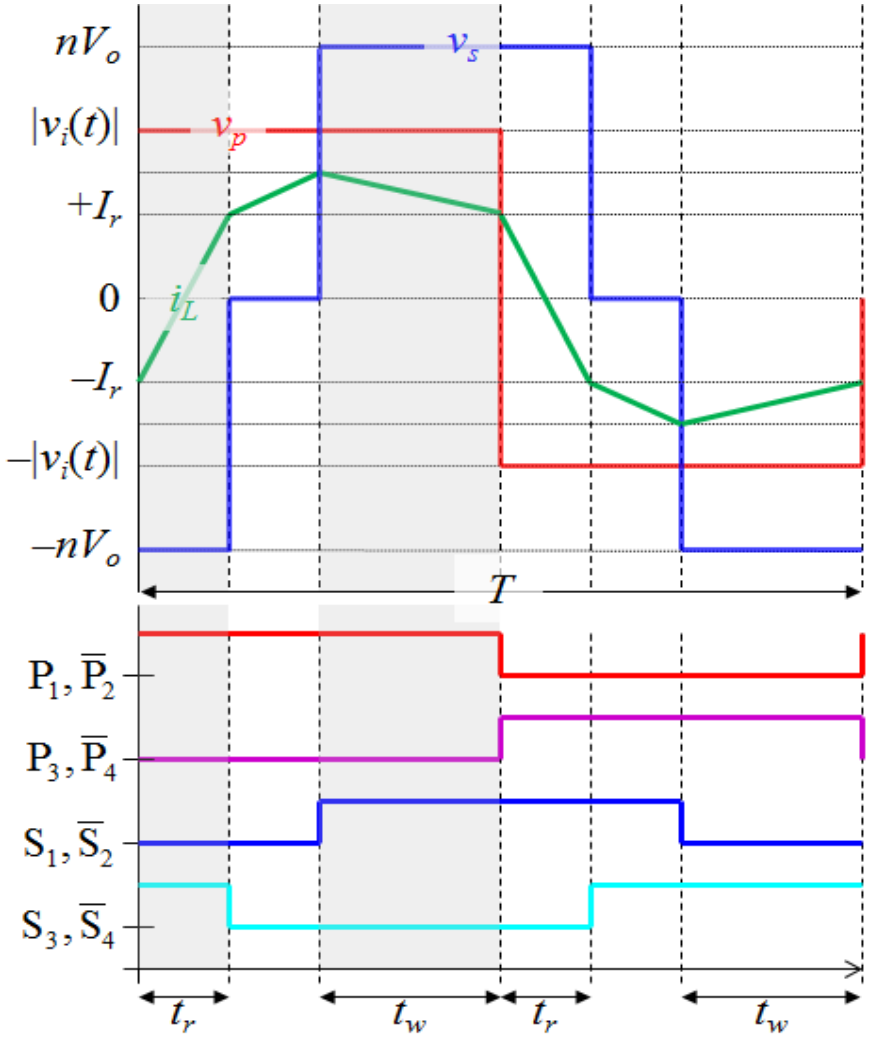


Figure 59 Output voltage of the DAB primary side and secondary side, current of the primary inductor, and gate signals of all switches during SDPS.

The transformer primary-side voltage, v_p, is a two-level square wave, while the secondary-side voltage, v_s, is three-level. These two voltages are responsible for shaping the current of the transformer leakage inductance, i_L. To maintain symmetry with near-zero switching-current magnitudes of I_r, we need:

$$t_w = \frac{T - 2t_r}{2} \frac{|v_i|}{nV_o} \tag{19}$$

$$p(t) = \frac{nV_o f_s}{L} \left[\left(|v_i| - nV_o \right) {t_w}^2 + \left(|v_i| + nV_o \right) t_w t_r \right] \tag{20}$$

The transferred power in one switching period is shown as above. To secure ZVS turn-on, the value of Ir must be kept above a minimum value. This imposes a lower-limit on t_r, which is:

$$t_{r,\min} = \frac{2I_{r,\min} L}{|v_i| + nV_o} \tag{21}$$

Here, $I_{r,\min}$ is the minimum leakage inductor current to charge/discharge the parasitic capacitance of switches during the dead-time.

Examining (19) and (21) together implies that t_w also has a minimum value required to maintain a balanced leakage inductor current. While it is possible to reduce t_w to zero (by setting $T = 2t_r$), this would require a very high switching frequency. Thus, if t_r and t_w cannot be zero, (20) shows that there is a minimum power transfer required for operation. Increasing frequency can reduce the value of t_w, but this will be at the expense of increased semiconductor switching losses and transformer magnetic losses. Thus, operation at light-load is limited by the maximum switching frequency of the system.

When |vi(t)| > nVo, PDPS

To secure a balanced current with near-zero switching points of I_r when $|v_i(t)| > nV_o$, a different phase shift t_v is added on the primary-side voltage (making it three-level) while reducing the secondary-side voltage to a square wave, shown in Fig.60 Here, the phase shift, t_v, can be written as:

$$t_v = \left(\frac{|v_i| - nV_o}{|v_i|} \right) \left(\frac{T - 2t_r}{2} \right) \tag{22}$$

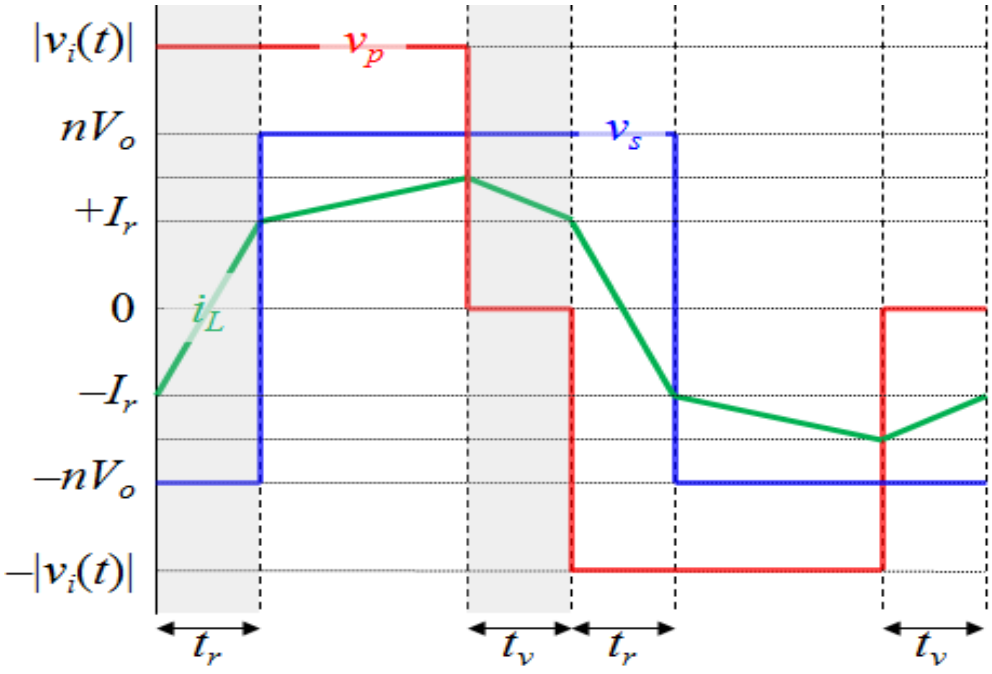


Figure 60 Output voltage of the DAB primary side (red) and secondary side (blue) and current of the primary side (green) during PDPS.

Once t_r is found, t_w or t_v and f_s will be determined. The expression for power in PDPS is similar to (2). Note that the control software will have to switch between PDPS and SDPS frequently (four times per fundamental AC input period) when the battery voltage is less than the peak AC voltage. Meanwhile, f_s and the phase shifts are tightly coupled and need vary at all times. More importantly, our analysis of (2) shows that when the required power is low, f_s must be quite

high, which is usually not a possibility due to switching limitations. Since f_s has an upper-limit, a lower-limit is imposed on the power transfer, thereby distorting the grid current. In Fig.60, the grid voltage is 208VAC and the output (battery) voltage is 400V. When the grid voltage is close to zero, the switching frequency is clamped to a pre-set limit (300kHz), resulting in a bumpy/distorted input current. Such current distortion becomes worse at light load.

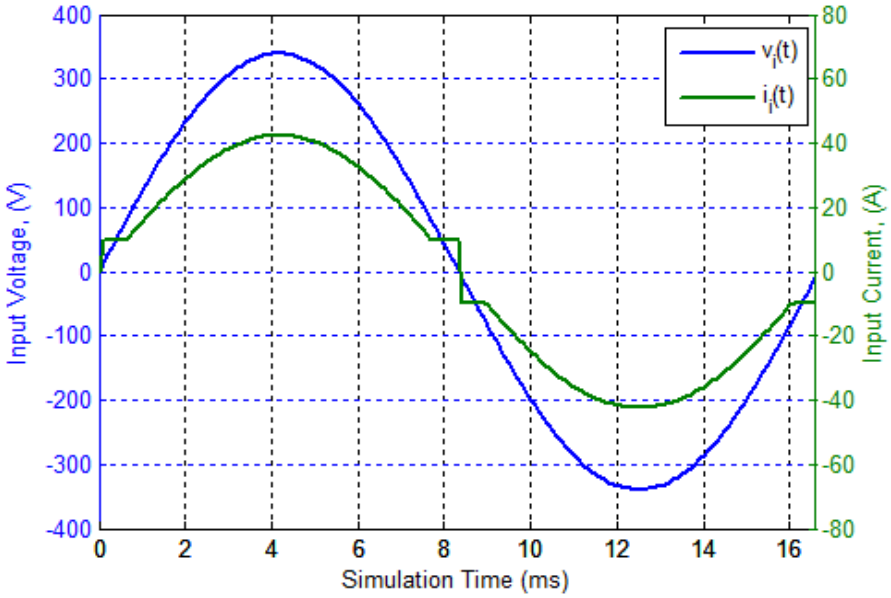


Figure 61 Simulated converter input voltage & current using DPS @ 7.2 kW.

3.2.3 TPS for Light-load Operation

To enhance the light-load control capability and thus resolve the grid-current distortion, a triple-phase-shift (TPS) algorithm has been introduced, which theoretically maintains ZVS down to zero power.

In TPS, the rising edge of P_1 and S_3 in Fig.61 maintain a phase shift of ϕ_r. Meanwhile, a second phase-shift, ϕ_p, is placed between P_1 & P_3 and a third phase-shift, ϕ_s, is placed between P_1 & S_1. This makes both, the primary and secondary voltages of the transformer, three-level waveforms. Both ϕ_r and ϕ_p work to regulate the near-zero switching current, I_r, which is

responsible for maintaining ZVS during 4 of the 8 switching-on cycles within a period. The switching waveforms and the transformer voltages and current are shown in Fig.62.

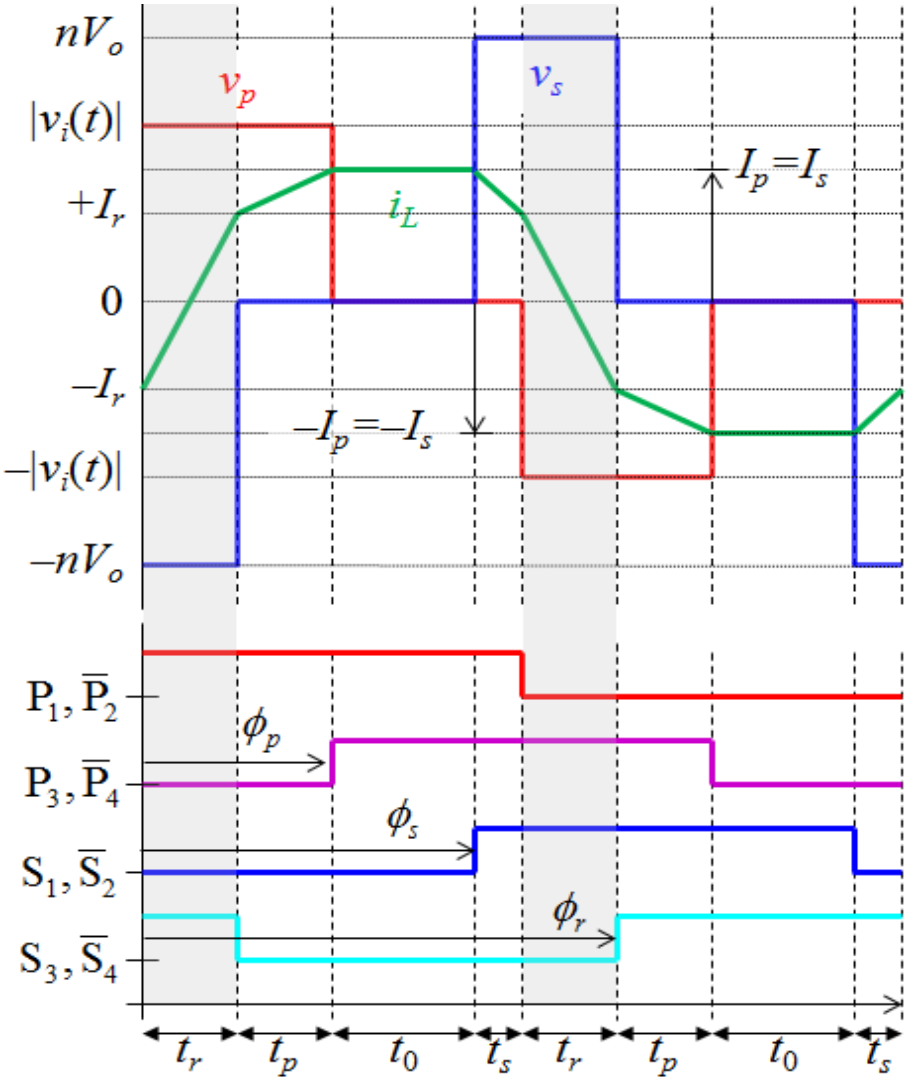


Figure 62 Voltage, current, & switching waveforms of non-overlap TPS.

The power is regulated by ϕ_p and ϕ_s. Note that, since the three phase shifts are independent of each other, it is possible that $\phi_p < \phi_s$ or $\phi_p > \phi_s$; the former case is denoted as the "non-overlap condition" as shown in Fig.56 and the latter is denoted as the "overlap condition", shown in Fig.63.

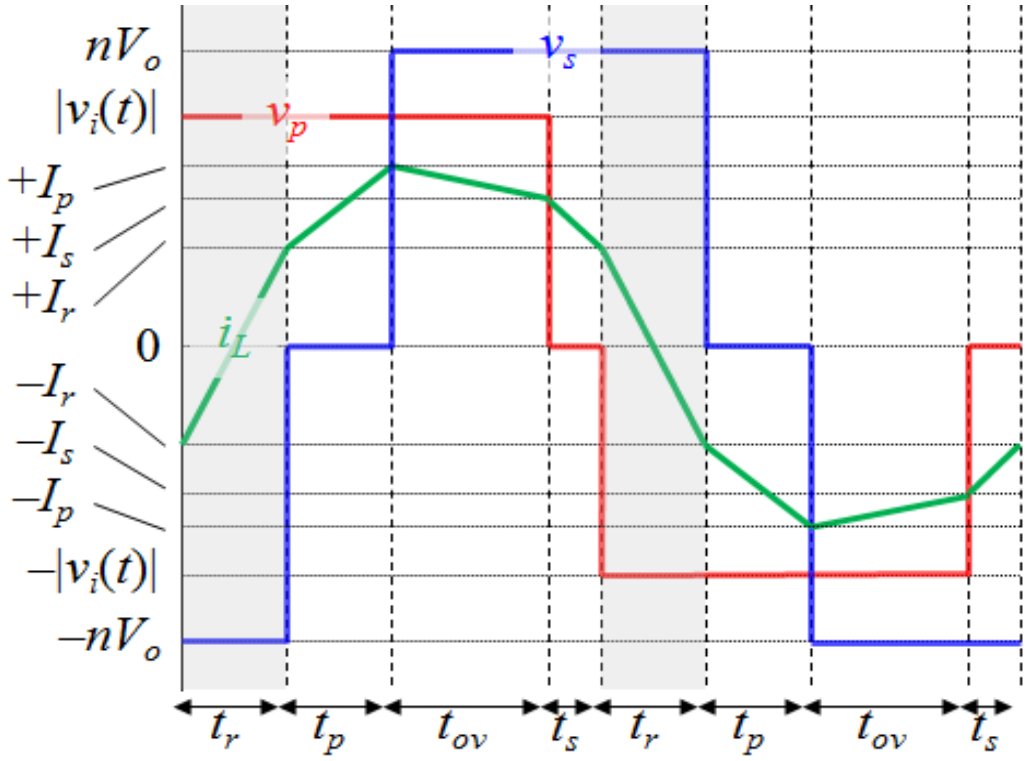


Figure 63 Voltage & current waveforms of TPS during the overlap case.

The variables, t_p, t_s, t_r, t_0 and t_{ov} are denoted as the primary-active, secondary-active, reactive, inactive, and overlap time intervals, where: and the value T is the switching period.

$$\varphi_p = \begin{cases} \left(t_r + t_p\right)/T, \text{non-overlap} \\ \left(t_r + t_p + t_{ov}\right)/T, \text{overlap} \end{cases} \tag{23}$$

$$\varphi_s = \begin{cases} \left(0.5T - t_s\right)/T, \text{non-overlap} \\ \left(0.5T - t_s - t_{ov}\right)/T, \text{overlap} \end{cases} \tag{24}$$

$$\varphi_r = \left(0.5T + t_r\right)/T \tag{25}$$

The value I_r is the magnitude of the current during the reactive power transfer interval when P_1, S_4, P_2, and S_3 turn on. We can describe this value as:

$$I_r = \frac{t_r\left(\left|v_i\right| + nV_o\right)}{2L} \tag{26}$$

To realize ZVS turn-on, the magnitude of I_r must be enough to completely discharge the drain-source capacitances of the upper and lower switching devices during dead-time:

$$I_r \geq \sqrt{2\left(0.5C_{DS}V^2\right)/L} \tag{27}$$

where the voltage, V, could be the primary-side voltage or the secondary-side voltage; whichever side is larger. ZVS turn-on of the other four switching events (P_3, P_4, S_1, and S_2) is guaranteed since the transformer current will be larger than I_r.

The value I_p is the peak transformer current magnitude during the primary active-power-transfer interval when $v_p \neq 0$ & $v_s = 0$. Similarly, I_s is the peak current magnitude of the secondary active-power-transfer interval when $v_s \neq 0$ and $v_p = 0$, where:

$$I_p = I_r + \frac{\left|v_i\right| t_p}{L} \tag{28}$$

$$I_s = I_r + \frac{nV_o t_s}{L} \tag{29}$$

To guarantee that the value of I_r remains constant at the P_1, S_4, P_2, and S_3 turn-on points (and that the i_L waveform is balanced), the two active-time intervals must be proportional to the primary and secondary-side voltages:

$$\frac{\left|v_i\right|}{nV_o} = \frac{t_s}{t_p} \tag{30}$$

The power transfer of the DAB operating under TPS control in the non-overlap case can be described as:

$$p(t) = nV_o\left(I_r + I_s\right)t_s f_s \tag{31}$$

which, after substituting in (11) and rearranging, gives us:

$$p(t) = \left(2nV_o I_r f_s\right)t_s + \left(\frac{n^2 {V_o}^2 f_s}{L}\right){t_s}^2 \tag{32}$$

Note that this expression for power is a quadratic function of the secondary active-time interval, t_s. We could also rewrite this power expression in terms of t_p and $|v_i|$ through use of.

It is important to note here that, while the output power depends on I_r, f_s, t_p, and t_s, the value of I_r is independently controlled by only t_r, the voltage magnitudes, and leakage inductance, L. Thus, I_r could be set to a constant desired value, determined by the switching device's output capacitance and maximum voltage while the power can be set by varying either f_s and/or the time intervals. Here, the ZVS condition is totally decoupled from the power delivery, unlike DPS shown above. Thus, from a control-standpoint, there is no need to vary f_s; this will only vary the width of the t_0 inactive region of the switching waveform. This resolves the PF distortion problem of VSF DPS control at light loads.

One main limitation of non-overlap TPS is the maximum power transfer can be quite low for practical system parameter and voltage values. Additionally, the efficiency of non-overlap TPS will be quite low, since a majority of the transformer current is simply circulating during the inactive period, t_0, leading to excessive conduction losses. For larger power transfer under TPS, both time intervals t_p and t_s must become larger, such that $\phi_p > \phi_s$. In this condition, both voltages

are non-zero for three time intervals: the overlap, active, and reactive intervals. The first two intervals will contribute to power transfer, described as:

$$p(t) = nV_o f_s \left[(I_r + I_s) t_s + (I_p + I_s) t_{ov} \right] \tag{33}$$

$$\frac{|v_i|}{nV_o} = \frac{t_s + t_{ov}}{t_p + t_{ov}} \tag{34}$$

to maintain the balance of the transformer current. Using above equations and noting that

$$0.5T = t_r + t_p + t_s + t_{ov} \tag{35}$$

We can rewrite the output power expression (after much manipulation) as a function of only the primary (or secondary) phase shift time-value:

$$p(t) = \frac{|v_i| f_s}{L} \begin{bmatrix} -nV_o (0.5T - t_r)^2 \\ +2\left[I_r L + (0.5T - t_r)(nV_o - |v_i|) \right](t_p + t_{ov}) \\ -\left({v_i}^2 + nV_o |v_i| + n^2 {V_o}^2 \right) / (nV_o)(t_p + t_{ov})^2 \end{bmatrix} \tag{36}$$

Note that this power expression is also a quadratic function of the total active time interval ($t_p + t_{ov}$ in this case). Also, note that the sign on the 2nd-order term is negative, indicating that there exists a maximum-power-point achievable with this modulation strategy.

If we lower the switching frequency under TPS control, it is possible to increase the maximum power point, P_{max}, to any arbitrary value (within reasonable system limitations). The maximum power point value is given as:

$$P_{\max} = \frac{|v_i| nV_o f_s}{L} \begin{bmatrix} \dfrac{\left(I_r L + (|v_i| + nV_o)(0.5T - t_r) \right)^2}{{v_i}^2 + n|v_i|V_o + n^2 {V_o}^2} \\ -(0.5T - t_r)^2 \end{bmatrix} \tag{37}$$

Thus, it is possible to utilize a VSF TPS control to cover the entire power range. However, the disadvantage with such a scheme is that the circulating current and peak switching currents can become quite large with lower frequencies. Lowering the frequency in the non-overlap region will simply increase the t_0 time interval in Fig.64, which does not contribute any active power transfer and adds conduction loss. Furthermore, the highest peak current occurs at the boundary of non-overlap TPS and overlap TPS, and is given by:

$$I_{pk} = \frac{1}{2Lf_s}\left(\frac{|v_i|nV_o}{|v_i|+nV_o}\right)+I_z\frac{|v_i|^2+n^2V_o{}^2}{\left(|v_i|+nV_o\right)^2} \tag{38}$$

Lowering the frequency will directly increase this value. Therefore, to reduce excessive conduction losses and switching losses, it is advantageous to maintain a high TPS switching frequency, which will consequently result in a low peak-power point.

3.2.4 MPS for All Operating Conditions

To resolve the complexity and PF distortion of the PDPS + SDPS and the low efficiency of low-frequency TPS, we propose here a multiple-phase-shift (MPS) modulation strategy, which essentially is a combination of high-frequency TPS control and VSF DPS.

If we plot the TPS output power vs. one of the active phase shift values (ϕ_p or ϕ_s) at constant switching frequency, we can see the two TPS quadratic waveforms of (14) and (18). In Fig.64, the TPS power expressions are plotted against the primary active phase shift, ϕ_p, assuming that $|v_i| < nV_o$. Note that the far right-hand side of Fig.58 is a boundary condition where ϕ_p has reached 180 degrees.

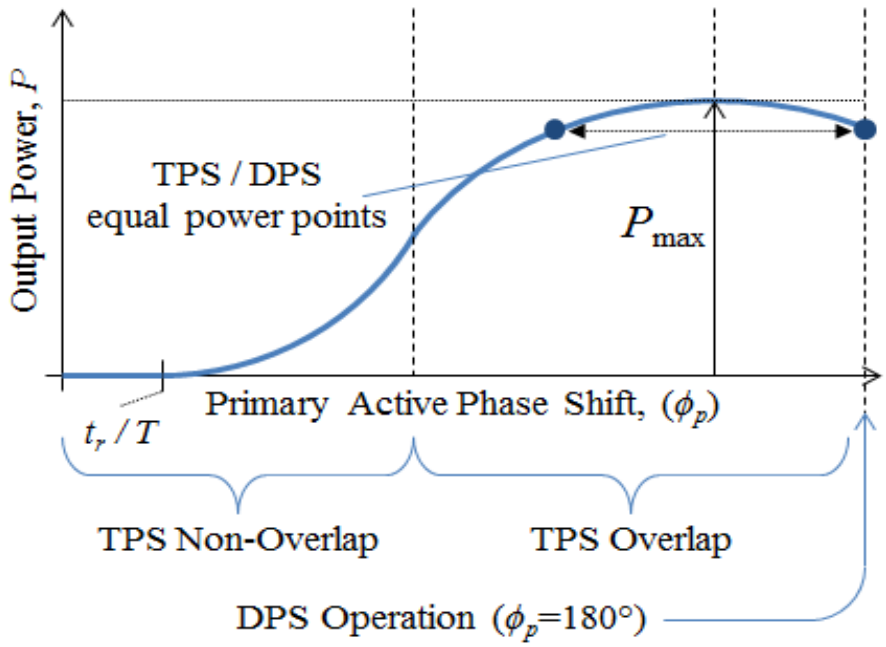


Figure 64 Output power vs. primary active phase shift when |vi| < Vo.

Note that a similar condition could occur where ϕ_s reaches 180 degrees before ϕ_p (in the case of $|v_i| > nV_o$). The phase shift which maximizes depends on the larger of the two transformer voltage magnitudes. If one of the two phase shifts reaches 180 degrees, the control effectively reduces to DPS. Thus, we could regard DPS as a subset of TPS control.

In MPS, the TPS non-overlap and some of the TPS overlap control ranges are used during low instantaneous power output intervals. When the instantaneous power demand is equal to the TPS/DPS equal-power-point and is increasing, the control algorithm will phase-jump from the left-side power point to the right-side power point in Fig.64. This phase jump is a transition from TPS to DPS. Higher powers are achieved by maintaining DPS operation while lowering the switching frequency. When the power is decreasing, a reverse phase-jump from DPS back to TPS is used. Note the switching frequency in TPS is always constant (e.g. 100 kHz); changes in instantaneous power are controlled by adjusting phase shifts. Meanwhile, DPS varies the switching frequency at all times to control the load (e.g., 100k~300kHz).

The benefits of such control are easier to visualize with a simulation waveform. Fig.65 shows a simulation of transformer peak current and transformer RMS current over half of a fundamental cycle of the grid while operating at 7.2 kW output. Fig.66 is a flow chart showing the selection of modulation strategies based on the instantaneous power. When the AC input voltage is sampled by the controller, the controller will compute the needed instantaneous output power required to deliver the demanded average output power and compare the calculated instantaneous power to the MPS equal-power point. If lower, the controller runs the TPS algorithm, otherwise, the DPS algorithm is selected. Directly calculating/controlling the desired instantaneous power (based on the desired average power) is how the shape of the grid current and the power factor are controlled.

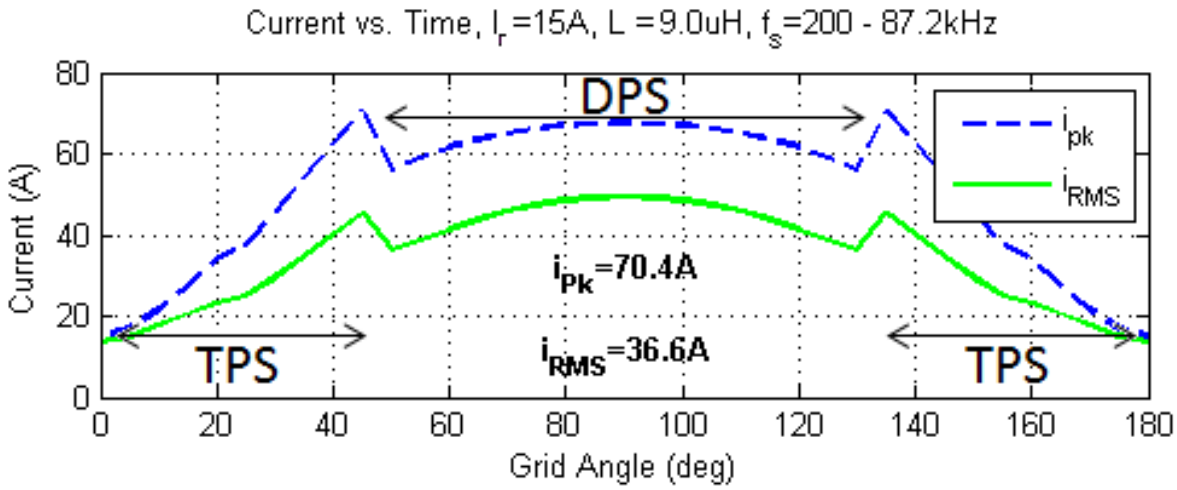


Figure 65 Simulation of transformer currents under MPS control at 7.2 kW.

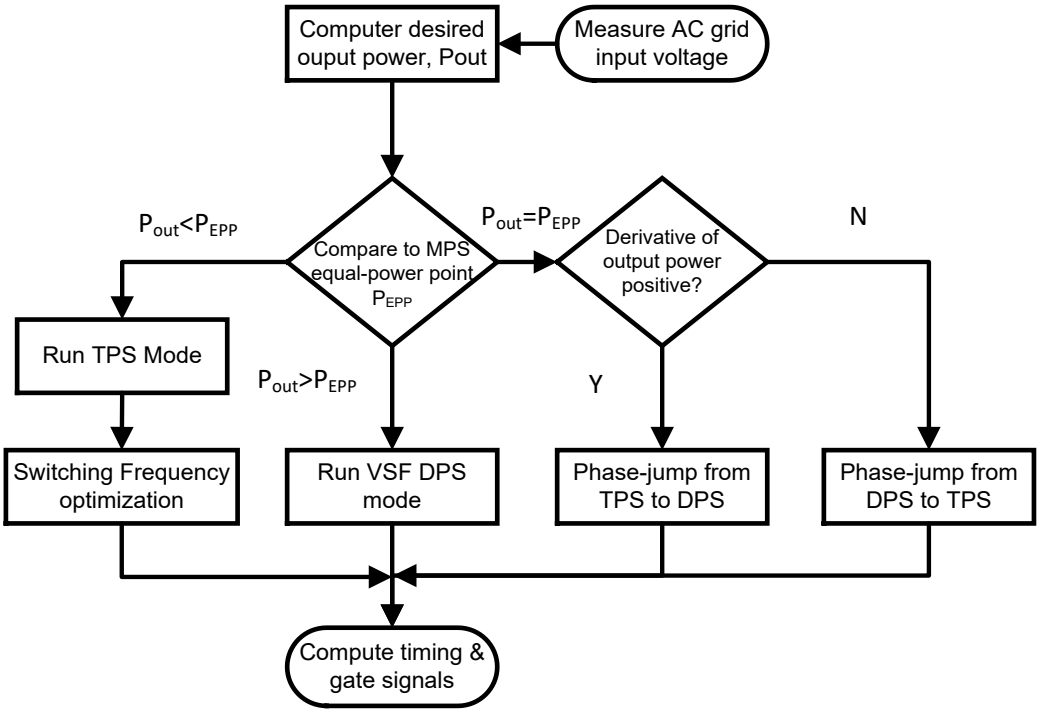


Figure 66 Flowchart of modulation strategies in a grid side period

In Fig.65, from 0° to ~45° and from ~135° to 180°, the instantaneous power demand is low and so TPS is used. The switching frequency selection for the TPS algorithm will be discussed in a later section. For grid angles between 45° and 135°, the instantaneous power is higher than the TPS/DPS equal power point, and so the control phase-jumps to use DPS in this range. The benefit here is obvious – the transformer peak and RMS currents sharply reduce while under DPS. Meanwhile, unity power factor can be achieved by using TPS in the light-load regions. Table 1 shows the comparison between the three control strategies. To summarize, the superior MPS strategy is outlined below:

(1)With low instantaneous power, the DAB operates using TPS on the left-side of the power curve in Fig.60

(2)When the instantaneous power exceeds the TPS/DPS equal-power-point, the DAB control will immediately jump to the right-side of the power curve in Fig.7, and will operate under VSF DPS;

(3)When the instantaneous power reduces, the control will jump back to TPS to control the power down to zero.

This entire process occurs twice for every fundamental period of the AC grid input voltage.

Table 3 Comparison of dual, triple, and multiple phase shift strategies

Control Strategy	PF / Distortion (Light-load@2kW)	Efficiency (7.2kW)	Current Stress (7.2kW)
MPS	Good (27%)	Best (>97%)	Low (85A)
TPS	Good (27%)	Poor (94%)	High (120A)
DPS	Poor (33%)	Good (>97%)	Low (85A)

3.2.5 Experimental Validation of MPS

To verify the effectiveness of such modulation strategy, a SiC-based 7.2kW charger was developed as shown in Fig.67, with the internal component placement shown as Fig.68 and the overall test bench shown as Fig.69. Three single-phase chargers were displayed so that we can test the single-phase charging and three-phase charging. In each single-phase charger, two 650V/93A SiC MOSFETs were paralleled to form one switching module. The entire DAB and transformer were developed and packaged together to yield a power density > 3 kW/L. Some of the system parameters and testing conditions are given below in Table.4.

Table 4 SiC-based DAB system parameters & test conditions.

Parameters	Values	Note
Primary DC-bus cap	10μF	Ceramic + Film capacitors
Transformer turn-ratio	1:1	High-frequency Litz wire used
Leakage inductance	8uH	Integrated inside the transformer
Secondary DC-bus cap	20μF	Ceramic + Film capacitors
Input voltage	240 VAC	60 Hz
Output voltage	360 VDC	Battery simulated w/ 10mF cap

Figure 67 SiC-based DAB + transformer prototype test bench.

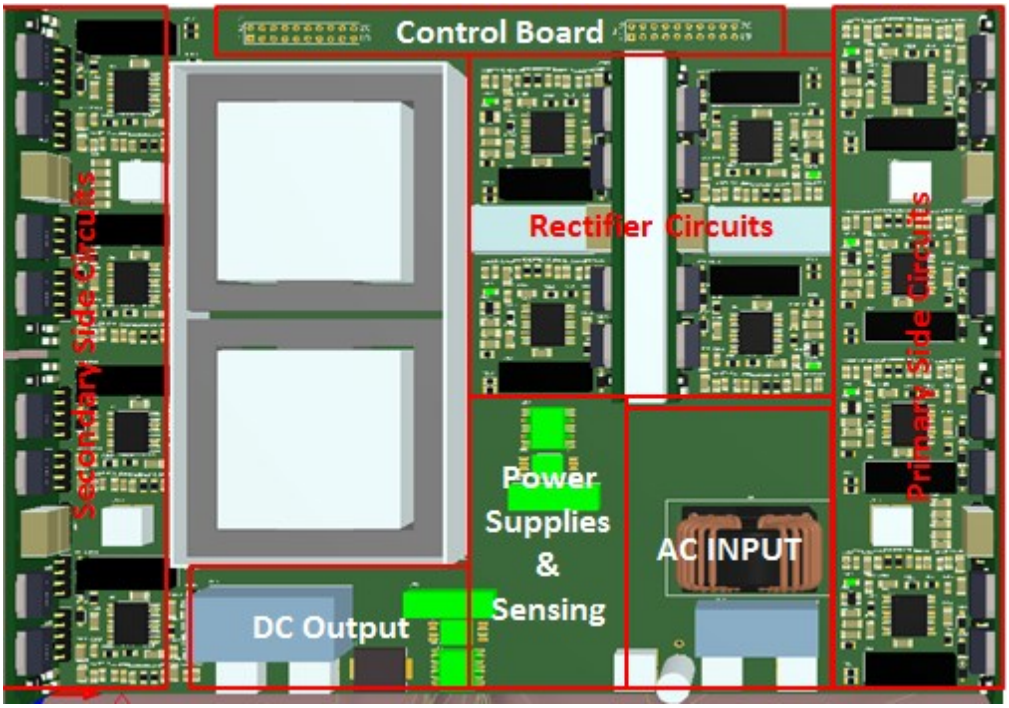


Figure 68 internal layout of the charger

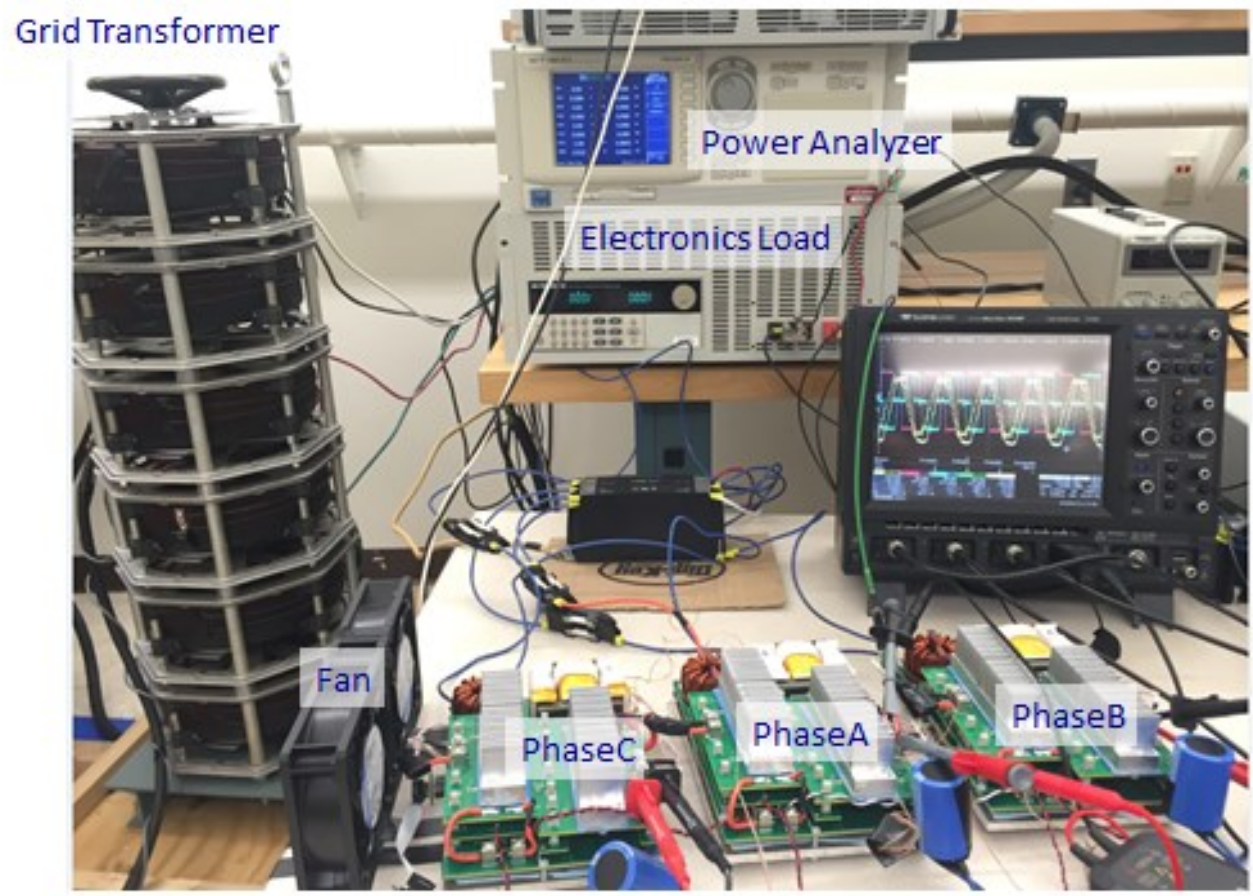


Figure 69 overall test bench

The experimental waveforms of v_p, v_s, i_L, v_i, V_o, and the grid current are shown in Fig.70 using the proposed MPS strategy to charge a 360V battery. Fig.64 and 65 show the waveform at 100W and 5.1kW, respectively. In Fig 71, the red line (grid voltage) and the brown line (grid current) are fully aligned, indicating the grid-side PF is close to 1. More importantly there is no current distortion around zero-crossing points like the DPS control. This validated the effectiveness of the proposed MPS control. Fig.71 shows the waveform when charging at 5.1kW. The sudden change of the transformer current (i_L, green line) represents the transition between TPS and MPS. Fig.72 zooms in the phase-shift-jump area of Fig.66. Here the microcontroller TMS320F28069 controls the phase jump to occur within one switching period. As the instantaneous power reaches the DPS-TPS equal-power point, the microcontroller will

automatically switch between TPS and DPS. During the transition, there is an obvious current change, making the TPS and DPS regions clearly visible. During testing, the transformer peak currents never exceeded a value of 80A, securing the system reliability. Note that the envelope of the transformer current i_L in Fig.64 matches quite well with the simulated peak-current envelope generated in Fig.72.

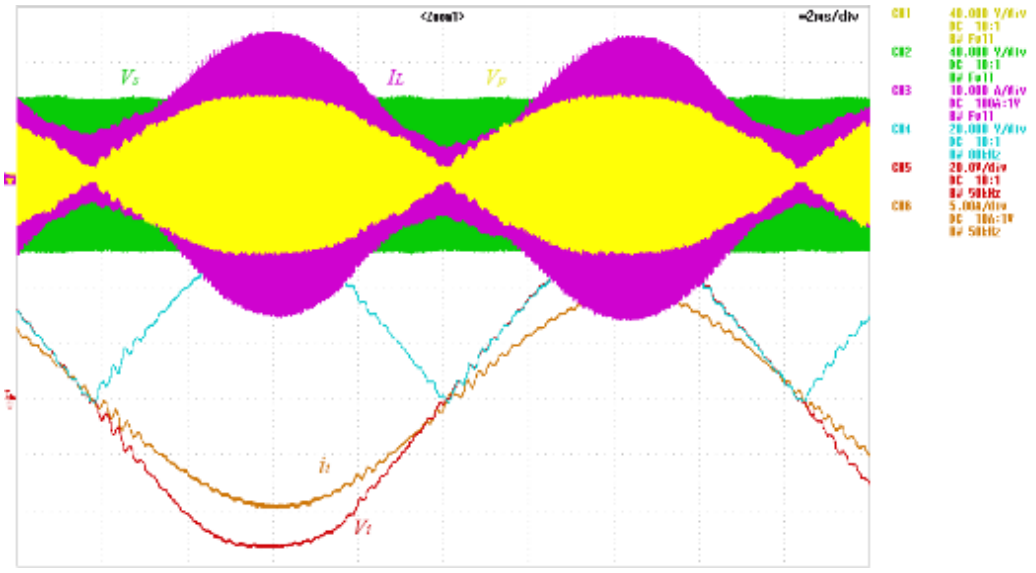


Figure 70 Experimental DAB waveforms at 100W (yellow-transformer primary voltage, 100V/div; purple-transformer current, 1A/div; green-transformer secondary voltage, 100V/div; red-grid voltage 100V/div, brown-grid current 1A/div).

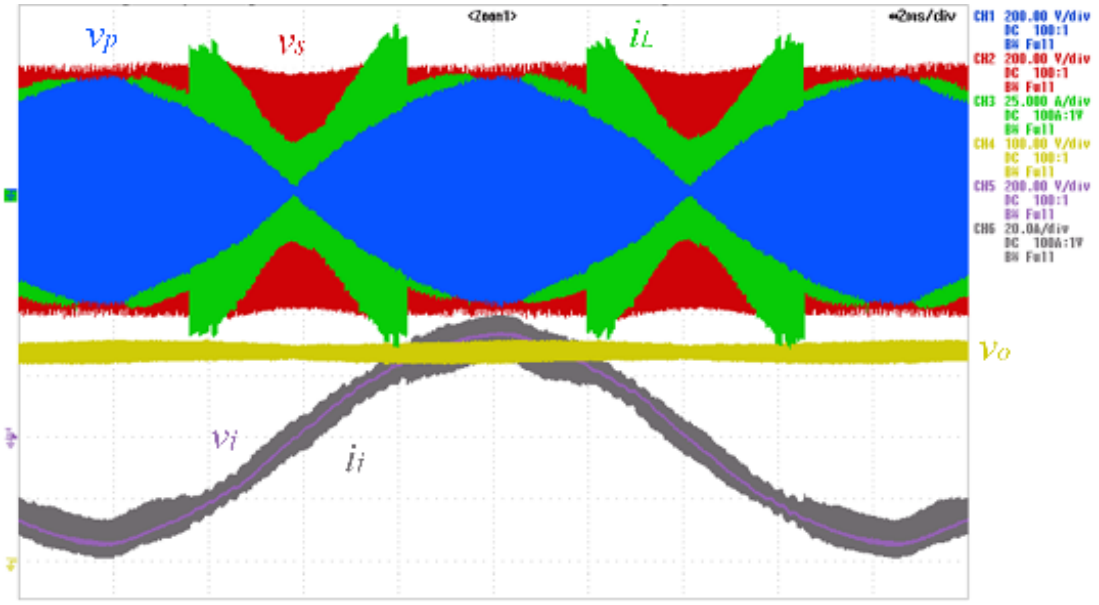


Figure 71 Experimental DAB waveforms at 5.1 kW (blue-transformer primary voltage; green-transformer current; red-transformer secondary voltage; brown-output voltage, gray-grid side voltage, purple-grid side current)

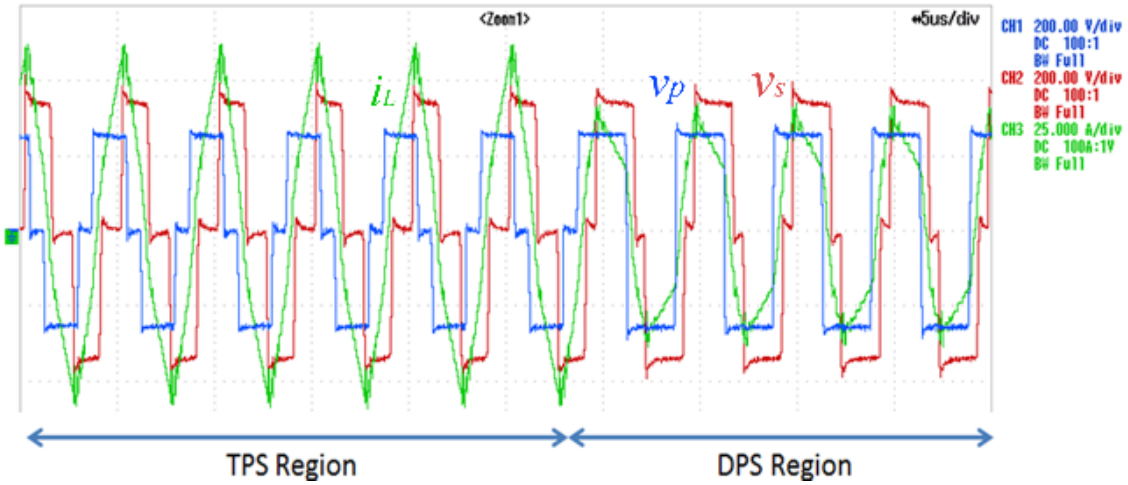


Figure 72 Phase-shift jumping region of Fig.65 (blue- primary voltage, red- secondary voltage, green- transformer current).

In the context of an EV charger, it is important to monitor the input power factor and THD of AC grid input. Fig.73 shows the input voltage and current, where the green line is the instant power. Note that the peak instantaneous power must reach 14.4kW for an average charging power of 7.2kW. The purple line is the grid-side voltage the grey line is the grid-side current. The total

harmonic distortion (THD) of the grid current is given in Fig.74 The THD at the rated power is 6%, slightly higher than requested 5%, which is subject to the future improvement.

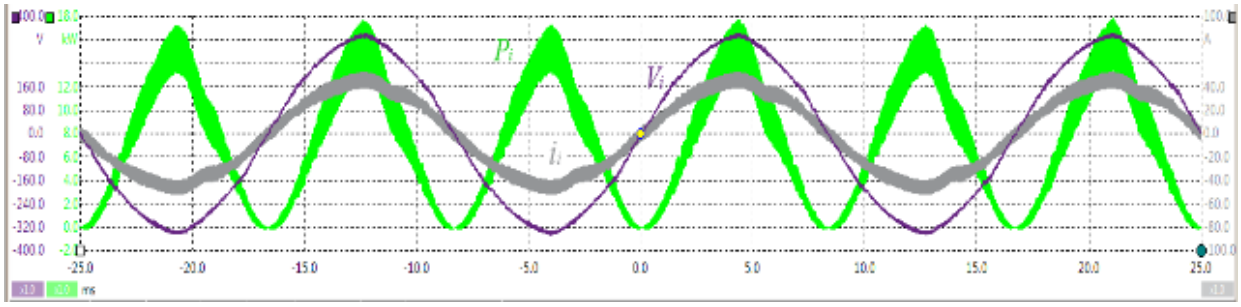


Figure 73 input voltage and current of EV charger

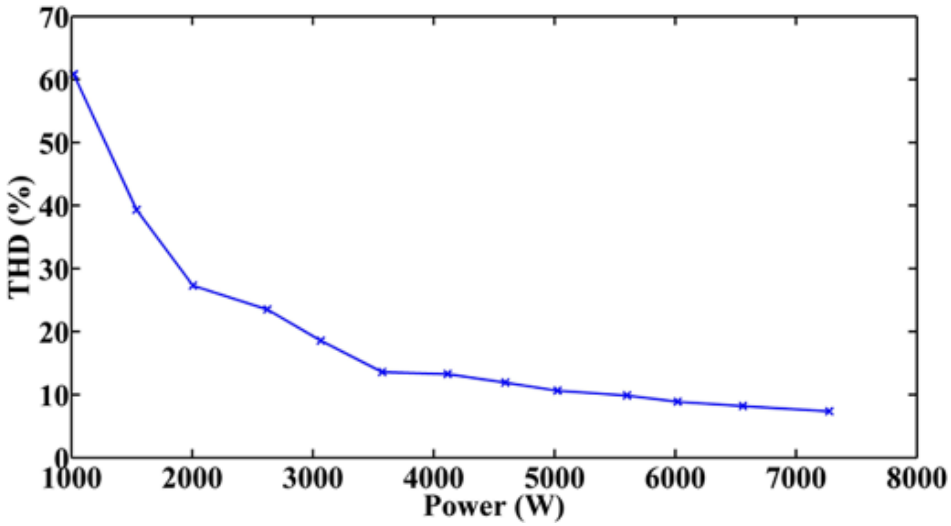


Figure 74 THD of the grid current at different power

In Fig.75, the experimental efficiency of the charger is plotted over the entire load range. The maximum efficiency at full power is ~97.9 %, thanks to having ZVS turn-on at all instantaneous power regions, given by MPS. Note the 2% efficiency loss includes the transformer loss and the semiconductor switch loss (conduction loss, switching loss and the dead-band loss).

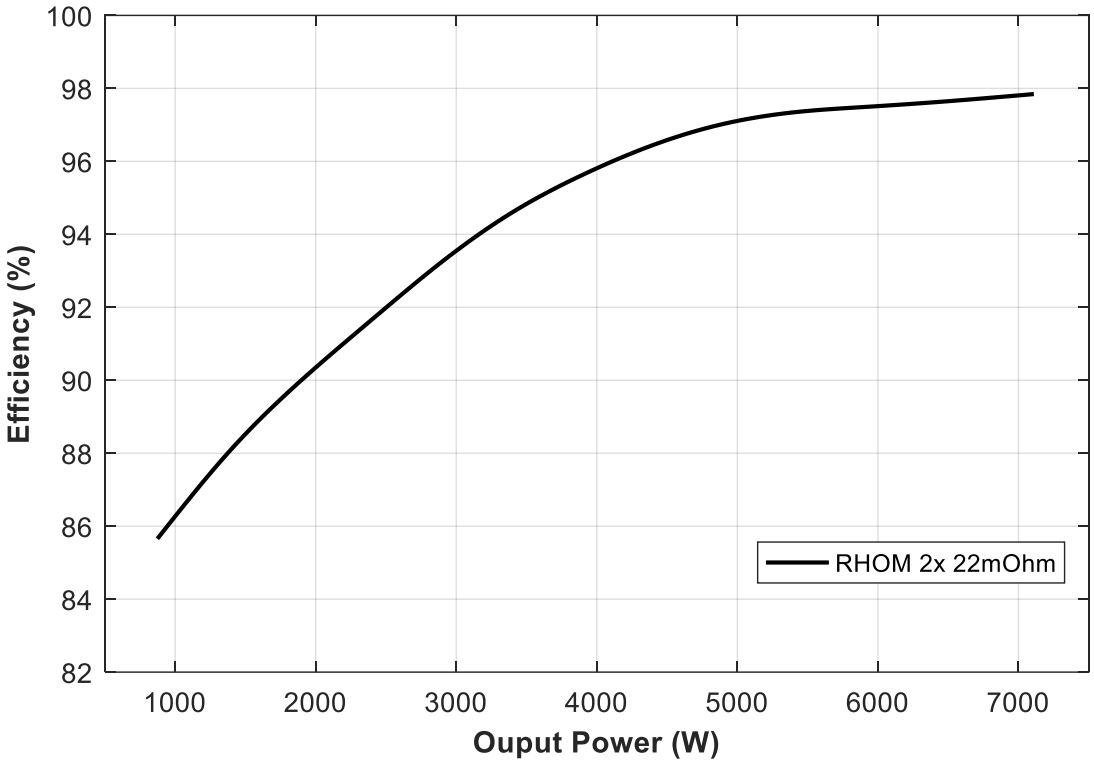


Figure 75 Experimental efficiency of DAB under MPS from 0.5-7.2 kW

3.2.6 Optimization at Light-load Efficiency

As shown in Fig.75, the high-power efficiency beats the expectation of ~97%, while most of the other EV battery charger efficiencies are 94%~95%. This means the loss reduction through use of the proposed control method is roughly 50%. Meanwhile, the power density is >3.3kW/L, in contrast to the 1~2kW/L of the state-of-the-art chargers. However, within the majority of the operational time, the charger works in the medium or low-power regions, making the enhancement of the power efficiency at light load is critical as well.

At light-load operation, where the non-overlap TPS method is employed, the circulating transformer current causes extra power loss and current stress, even though the average output power is low. Without careful control of the light-load TPS operation, it is possible that the light-

load power losses are even higher than the heavy-load losses, causing overheating at light-load operation.

For the non-overlap TPS method, the power loss and current stress are both heavily influenced by the switching frequency. Therefore, the optimization goal for light-load operation under non-overlap TPS is to find a switching frequency which provides the lowest power loss and current stress for the DAB stage, a typical multi-objective optimization. Here, the authors consider the switching loss, conduction loss and the dead-band loss.

The conduction loss can be easily calculated as $I_{\text{rms}}^2 * R_{DS}$. Here I_{rms} is the rms value of the semiconductor switches. R_{DS} is the semiconductor switch's equivalent on-state resistance, which can be obtained through the datasheet. Calculations of the switching loss and dead-band loss are related to the switching currents I_r, I_p and I_s, as shown in Section II. Such switching current values could be obtained through simulation/calculation. For the dead-band loss, it is given below:

$$P_{db} = \frac{V_f I_D T_{db} f_s}{f_{grid}} \tag{39}$$

Here, V_f is the forward voltage across the intrinsic body diode of the SiC MOSFET, which is ~3.2V, I_D is the drain current through the MOSFET at each of the switching moments, which for TPS control is $2(2I_r + I_p + I_s)$, T_{db} is the dead band time interval, which was set to 200ns for the experimental results shown, f_s is the switching frequency, and f_{grid} is the grid frequency, 60 Hz in this case.

To accurately model the switching-off energy (note, no switching-on losses occur due to ZVS turn-on), a detailed double-pulse test (DPT) needs be carried out. The DPT bench is shown in Fig.76 and the tested data were obtained at 300 VDC with the switching current varying from 10 A to 70 A, as shown in Fig.77 A cubic polynomial curve fit is adopted as (40).

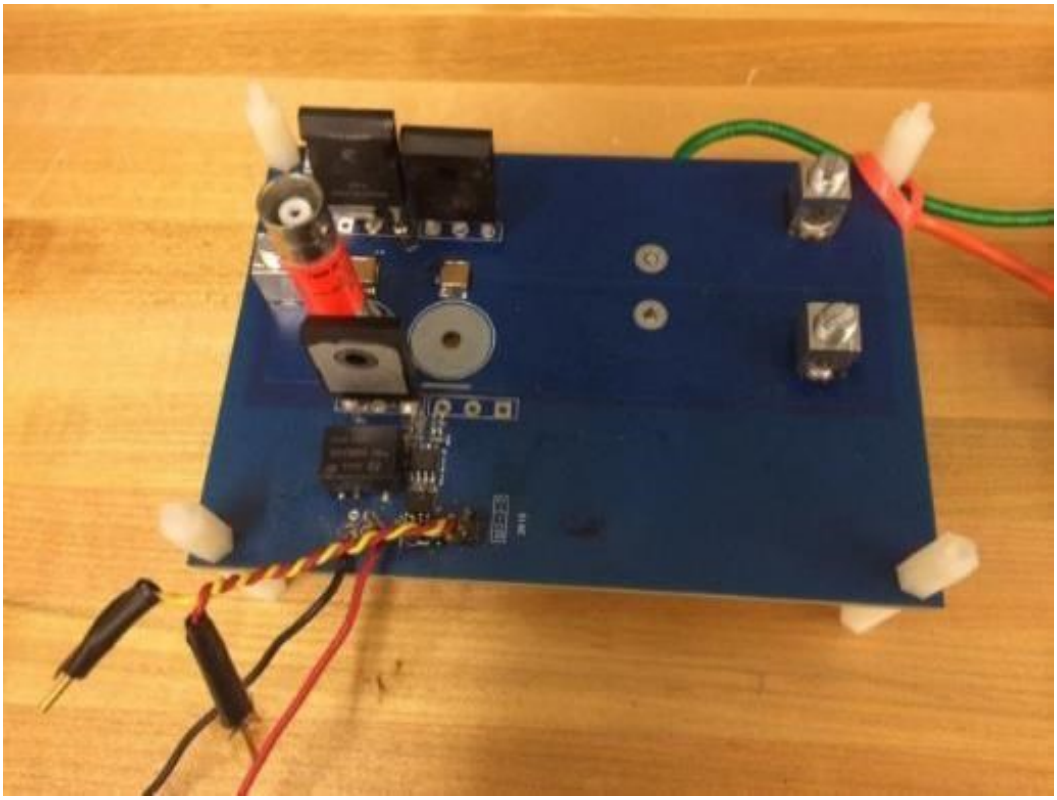


Figure 76 SiC DPT board

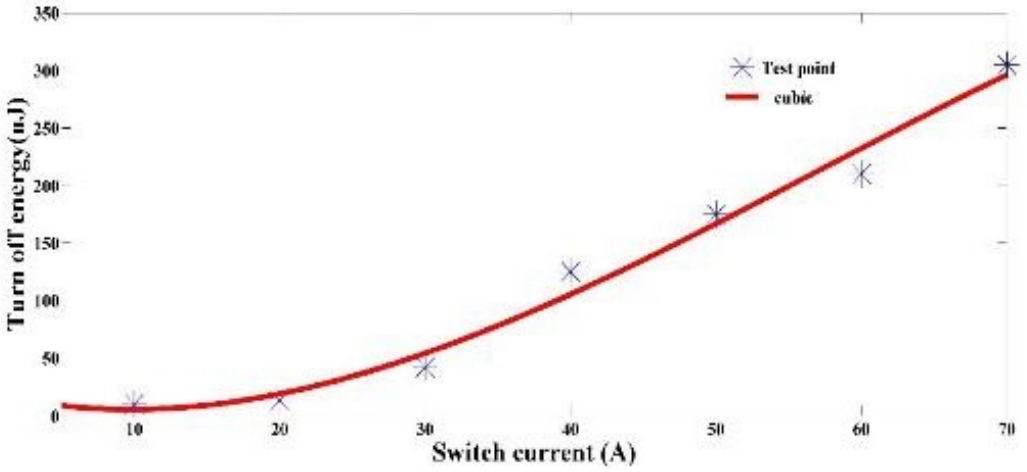


Figure 77 switching-off loss vs the switching current

$$E_{off}(I) = \frac{U}{300}(0.03I^3 + 51I^2 - 900I + 10) \tag{40}$$

In our system, one switching module consists of two SiC MOSFETs in parallel. The currents through each of two devices are assumed to be equal. Within one switching period, the overall switching loss of the DAB stage is

$$P_{off} = (8E_{off}(I_r/2) + 4E_{off}(I_p/2) + 4E_{off}(I_s/2))f_s \tag{41}$$

Therefore, the total DAB loss is:

$$P_{DAB} = P_{Conduction} + P_{deadband} + P_{switch-off} \tag{42}$$

As the TPS light-load (non-overlap) waveform shows, the maximum switching current value is I_s or I_p. The optimization goal is to find the best combination of f_s and I_r, where both the power loss and the current stress are minimized. The optimization restraints are maintaining ZVS turn-on for all switches at all times and limiting the transformer peak current to always be less than 80A. The search range for the switching frequency, f_s, is from 50kHz to 300kHz, and for the minimal ZVS current, I_r, is from 10A to 20A, though 10A is sufficient to turn-on two paralleled SiC MOSFETs in some cases without any switching loss, as calculated above

The multi-objective optimization problem can be mathematically described as

$$\begin{aligned} &Min\ \{P_{DAB}(X), I_{\max imum}(X)\} \\ &X = (f_s, I_r) \end{aligned} \tag{43}$$

To obtain the solution, the non-dominated sorting genetic algorithm 2 (NSGA2) is adopted here, which is the enhanced version of the non-dominating sorting genetic algorithm, first proposed by Deb in 2001. After many years of application, the NSGA2 algorithm has been proven to be a very useful method in many multi-objective optimization problems. Below is an outline of the NSGA2 algorithm:

Step 1. Randomly initialize the initial population P_1 and each parameter's value (switching frequency and ZVS current) in the NSGA2 algorithm, set the iteration number as 1, and start the algorithm's iteration calculation.

$$x(i,:) = (x_{\max} - x_{\min}) \times rand(1, N) + x_{\min} \tag{44}$$

Here $X(i,:)$ is the initialization individual of the population. For the switching frequency from 50kHz to 300 kHz and the ZVS current from 10A to 20A, the upper limit for x of the population is [300, 25], while the lower limit of population is [50, 10] and N is the dimension of optimization variables.

Step 2. Check if the iteration number has reached the limit. If it has reached the maximum iteration, end iteration calculations and output the Pareto optimal set. If not, continue the iteration calculation.

Step 3. Use the fast-non-dominated sorting to evaluate population, carry out the genetic operation including selection, crossover, and mutation to the evolutionary population to form the new generation Q.

Step 4. Combine the population P_i and the population Q as the mixture population R, using the fast-non-dominated sorting strategy and crowding distance function to sort R.

Step 5. Retain the elite individuals as the new generation of the evolutionary population P_{i+1}.

Step 6. Add 1 to the iteration number i once one iteration calculation is done. Go to Step 2 and continue the rest of the iteration calculation

Based on above, the optimization process for TPS during light-load operation (1 kW and 2 kW) is shown below in Fig.72.

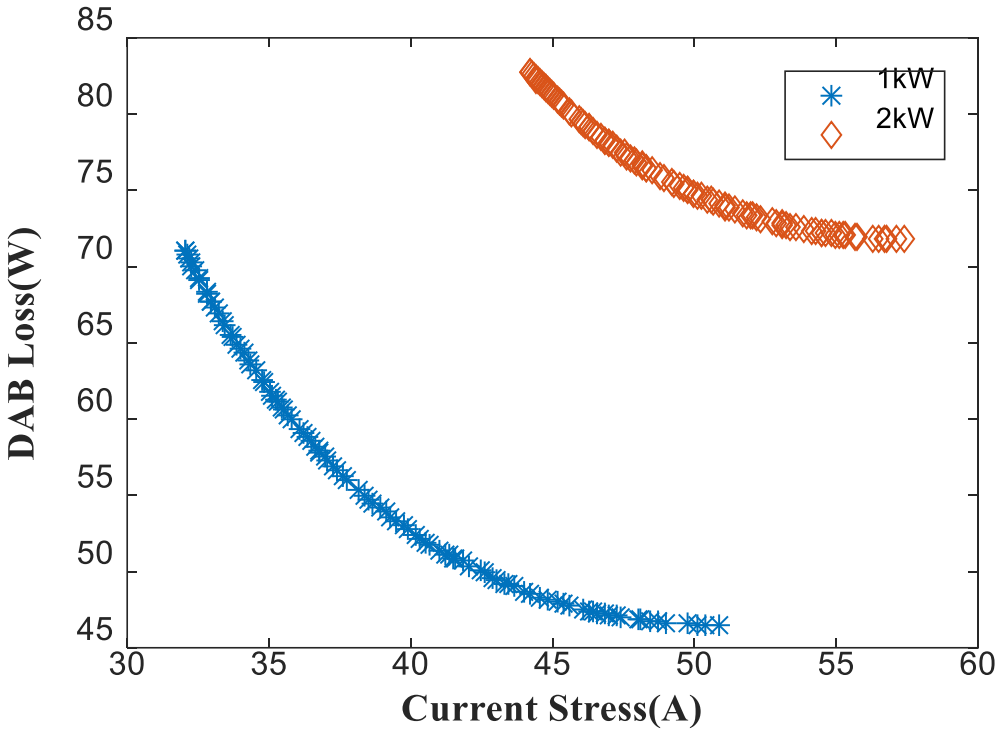


Figure 78 Optimization process at 1kW and 2kW

Figure 78 above shows that initially, when the current stress is ~40A, the switching loss is high. This is because in this region in order to realize very low current, the switching frequency must be high, causing the transformer leakage inductance to have high impedance. After further optimization, the losses reduce. With increasing current stress, the DAB loss will decrease. This is because a higher current stress translates to a lower switching frequency, which in return reduces the switching loss and the dead-band loss, though the conduction loss might increase. The optimal point for 1kW is 113.6kHz and that for 2kW is 171kHz. Both operations require ~17A ZVS current. The loss breakdown for these two power levels is shown in Fig.73 and 74 At different power levels, a similar loss-changing tendency is revealed, i.e., as the switching frequency goes up, the conduction loss reduces while the switching loss and dead-band loss increase. It is worthwhile to point out that, around the optimal point neither the power loss nor the current stress shows much difference. For instance, even though 171kHz is the optimal point for the 2kW operation, we can

technically select any value within 150kHz~220kHz. Some freedoms are provided to select any switching frequency in between. Fig.75 shows that DPS has the highest loss at the light load, given its high switching frequency. The optimized TPS can slightly reduce the loss compared to the non-optimized TPS control.

Note that all loss analysis is based upon the actual DPT results instead of datasheet values. It can be seen through Fig.79 that

1) when the average power increases, the conduction loss does not vary much. This is due to the fact that, as the power increases, the optimal switching frequency increases as well, which, in return reduces the current stress.

2) both the dead-band loss and the switching-off loss increase due to a higher switching frequency.

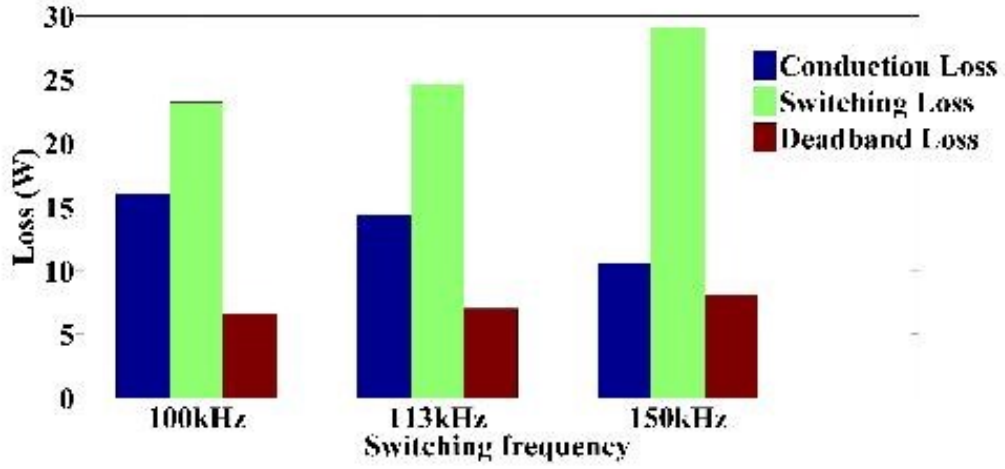


Figure 79 1kW DAB loss breakdown at (100kHz, 113.6kHz, and 150kHz)

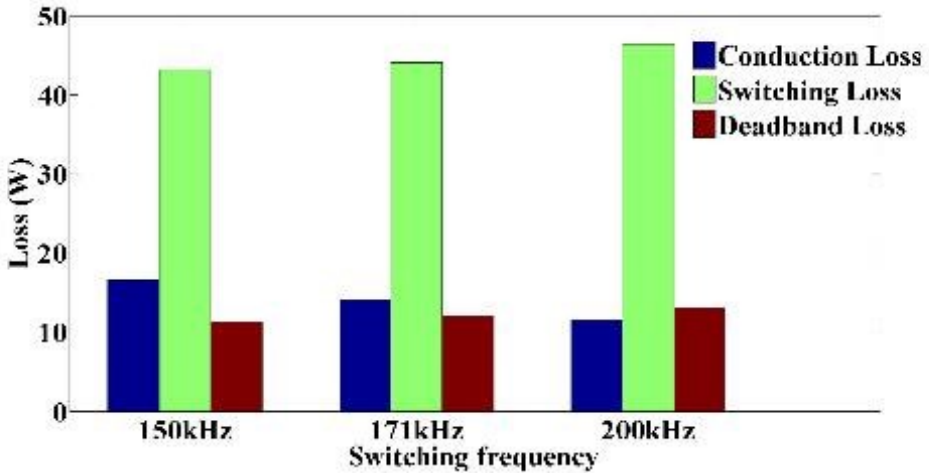


Figure 80 2kW DAB loss breakdown at (150kHz, 171kHz, and 200kHz)

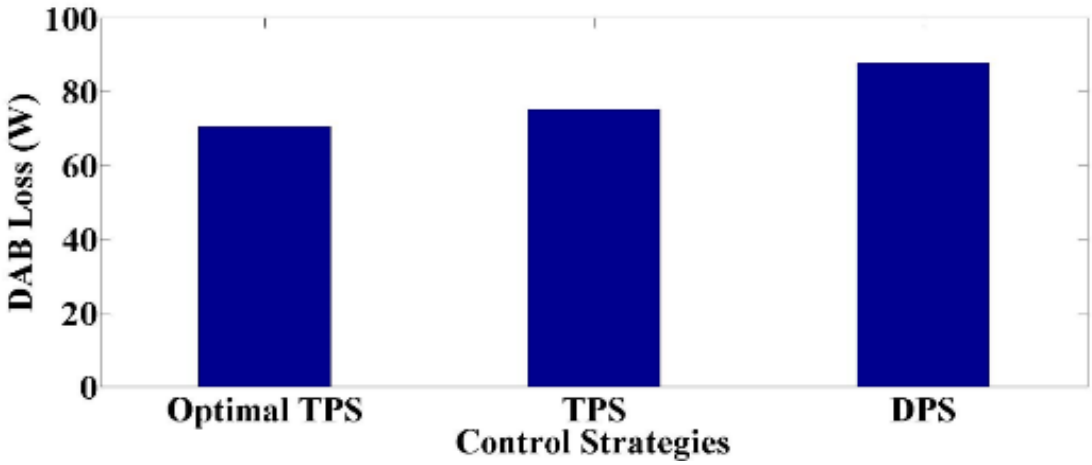


Figure 81 2kW DAB loss breakdown at different control algorithm

3.2.7 Conclusion

A novel MPS modulation strategy (which is a combination of TPS and DPS) was proposed in this paper to secure ZVS on for all switches and enhance the light-load efficiency. The full-load efficiency is >97%, due to the superior performance of SiC operating under ZVS turn-on. To further overcome the demerits of the high switching-off current and high circulating current present in TPS, a phase-shift jump to DPS is added to enhance the heavy-load performance. The proposed modulation strategy at light-load could run constant switching frequency TPS,

simplifying the control compared to the conventional DPS and eliminating the grid current distortion at the light load.

With the high-power efficiency quite adequate, more effort was given to enhance the light-load performance. By using a multi-objective optimization technique, the optimal switching frequency was obtained for multiple power levels, particularly for those occurring in the non-overlapping TPS method's range. The optimization is based upon the actual DPT data, which makes such an optimization strategy more convincing than relying on datasheet values. With such efforts, the system efficiency at light load is optimized with the transformer current stress maintained below the threshold. Such optimization is suitable for other power electronics systems.

3.3 GaN and Si Hybrid Switch

3.3.1 Introduction

GaN HEMT and SiC MOSFET are two exemplified wide-bandgap (WBG) devices. Due to its ultra-fast switching transition and outstanding thermal capability, WBG devices are excellent candidates for high-efficiency and high-power-density power electronics converters [93-95]. Their demerits, however, are also obvious compared to the conventional Si MOSFET. Take E-mode GaN HEMTs as an example. Such GaN device has a high reverse conducting voltage, which exhibits a higher dead-band loss than Si when reverse conducting. In [96], it reported a 7V reverse voltage drop when using -5V to turn off GaN HEMTs. Secondly, the devices so far have few varieties. 650V/60A is the highest power rating found on the market. Even though paralleling GaN HEMTs has been technically validated, its high cost becomes the major hurdle for industries, given that GaN still exhibit 3~5 times cost of Si MOSFETs.

Instead of using pure GaN HEMTs, a hybrid switching module is poised to maximize merits of both GaN HEMTs (low switching loss) and Si MOSFETs (low conduction loss and cost). A similar approach was found when paralleling Si to SiC [97-98], however not widely reported for GaN+Si yet. Once successful, Si paralleled with GaN expects to significantly reduce the reverse-conducting voltage drop, shrink the conduction loss and lower the overall cost.

The major challenges include: 1) impact of parasitics. Except Transphorm's devices, all other GaN vendors adopt much smaller footprints than TO-247 to reduce the stray inductance. When paralleling GaN to a TO-247 package Si, the impact of the large Si parasitics during switching transitions remains unclear. Such study is rewarding to evaluate the feasibility of such hybrid approach, given the switching speed of GaN is much faster than Si and even SiC. 2) difference on gate-drive signals. GaN and Si usually require different gate-voltage, e.g., E-mode GaN from GaN Systems Inc uses 7V/-5V while Si MOSFETs usually require >8V to effectively turn on. Meanwhile, a gate signal delay in between has to be implemented to make sure Si is fully turned on/off before switching actions of GaN HEMTs. Otherwise the high switching loss of Si becomes unendurable.

Given GaN HEMTs still have much higher switching-on loss than switching off [96], zero-voltage-switching (ZVS) turn-on is still highly recommended, which is the focus of this paper. Section II proposes the hybrid-switching solution particularly used in ZVS applications. Design challenges especially the short-timescale transient processes caused by parasitics are detailed. Section III evaluated the system loss and impact on the control strategy by using the proposed approach. A head-to-head comparison of the power loss between the pure-GaN design and the hybrid-switch solution is given. Section IV is the conclusion.

3.3.2 Design and Challenges

The proposed GaN+Si hybrid approach is shown as Fig.82. Two sets of drive circuits were given, sharing the same ground. +7V/-5V is used for GaN and +10V/-5V is for Si. Such design is easy to implement, however makes the Si suffer the hard-switching-on loss and reverse-recovery loss given the poor performance of its body diode. Therefore ZVS turn-on is a must for this particular design. Theoretically adopting a low-resistance Si MOSFETs results in that Si undertakes most of the current at the on-state and within the dead-time, thus ultimately results in a lower conduction loss and dead-band loss. In the switching transition, assigned with a sufficient time delay, Si MOSFETs will be off earlier than GaN HEMTs, i.e., ZVS off without any switching-off loss either. All the current will be switched off by the GaN HEMT, which tends to minimize the low-switching-loss due to its ultra-fast switching transition.

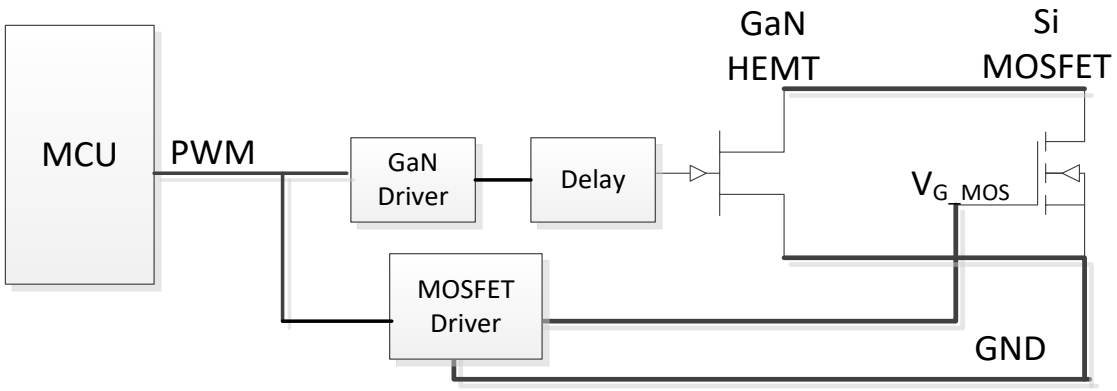


Figure 82 Schematics of the Hybrid Switching Module

To prove the above assumption, detailed switching behaviors of such hybrid module need be analyzed. When paralleling GaN with Si, due to their drastic footprint difference shown as Fig.83, parasitics brought by their own packages are different. In this paper we try to parallel two 650V/60A devices from GaN Systems to one IXYS 650V/150A MOSFET. The equivalent circuit is shown as Fig.83.

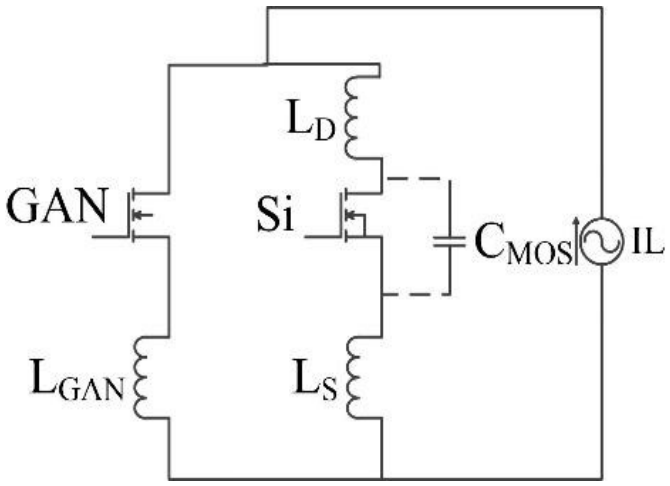


Figure 83 Leadless Top-Cooled Packaging of GaN HEMTs (GS66516T) and The equivalent circuit of the GaN+Si hybrid module

MOSFET switching off. When the Si MOSFET is switched off, its stray inductance LMOS=LD+LS will form the resonant circuit with its output capacitance CMoss. During this interval, GaN is still on. Such resonant energy will be dissipated in the GaN 2-dimensional-electron-gas (2DEG) channel. Specifically, by using KCL and KVL, we have

$$\begin{cases} L_{MOS}\dfrac{di_{MOS}}{dt}+\dfrac{1}{C_{MOS}}\int i_{MOS}dt = L_{GAN}\dfrac{di_{GAN}}{dt}+R_{GAN}i_{GAN} \\ i_{MOS}+i_{GAN}=I_L \end{cases} \tag{45}$$

Assume the load current IL is a constant value, we have

$$(L_{GAN}+L_{MOS})\frac{d^2 i_{GAN}}{dt^2}+R_{GAN}\frac{di_{GAN}}{dt}+\frac{1}{C_{MOS}}i_{GAN}=\frac{1}{C_{MOS}}I_L \tag{46}$$

Such a characteristic equation has two eigen values as below

$$\lambda_{1,2}=\frac{-R_{GAN}\pm\sqrt{R_{GAN}^2-4(L_{GAN}+L_{MOS})/C_{MOS}}}{2(L_{GAN}+L_{MOS})} \tag{47}$$

Existence of the GaN resistance (RGAN) damps the potential current oscillation. However, the introduction of the TO-247 MOSFET results in large LMOS, usually >10nH.

$$I_{GAN}(t) = e^{\alpha t}(A\cos\beta t + B\sin\beta t) + I_L \tag{48}$$

Here A and B are coefficients to be determined, and

$$\alpha = \frac{-R_{GAN}}{2(L_{GAN}+L_{MOS})}, \quad \beta = \frac{\sqrt{-R_{GAN}^2 + 4(L_{GAN}+L_{MOS})/C_{MOS}}}{2(L_{GAN}+L_{MOS})} \tag{49}$$

With the boundary conditions as

$$\begin{cases} I_{GaN}(0) = \dfrac{R_{MOS}}{R_{GAN}+R_{MOS}} I_L \\ L_{MOS}\dfrac{d(I_L - I_{GaN})}{dt}\Big|_{t=0} = R_{GaN} I_{GaN}(0) + L_{GaN}\dfrac{dI_{GaN}}{dt}\Big|_{t=0} \end{cases} \tag{50}$$

We have

$$\begin{aligned} I_{GAN}(t) &= \frac{-R_{GAN} I_L}{R_{GAN}+R_{MOS}} e^{\alpha t} \times \\ &\left(\cos\beta t + \frac{(2R_{MOS}+R_{GAN})}{\sqrt{-R_{GAN}^2 + 4(L_{GAN}+L_{MOS})/C_{MOS}}}\sin\beta t\right) + I_L \end{aligned} \tag{51}$$

Devices in this paper have parameters shown in Table.5.

Table 5 Definition of parameters

Symbol	Definition
GaN	GS66516T
MOSFET	IXFB150N65X2
L_{MOS}	25nH
L_{GaN}	~1nH
C_{MOS}@~10V	53nF
I_L	20~80A
R_{GAN}	25mΩ

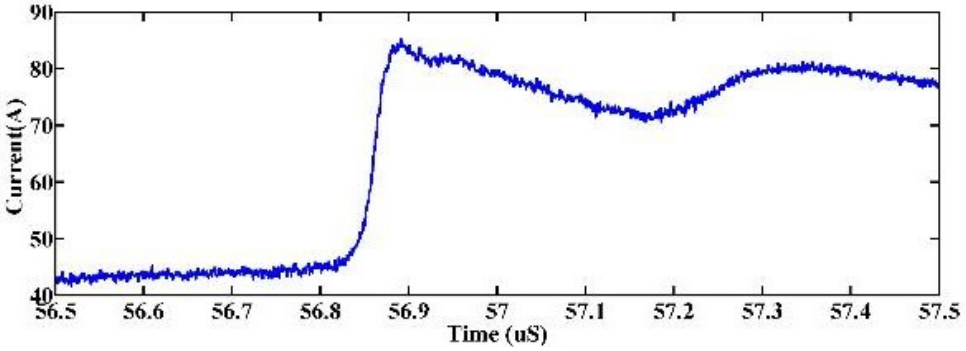


Figure 84 Current changing in switching process

Eqn(51) indicates a potential current oscillation with a overshoot for GaN when Si is turned off. To verify this possible current over shoot and states the parameters that may have influence on the over shoot value, PSpice model was built as well to support such analysis, the simulation model we adopted is given in fig.85.

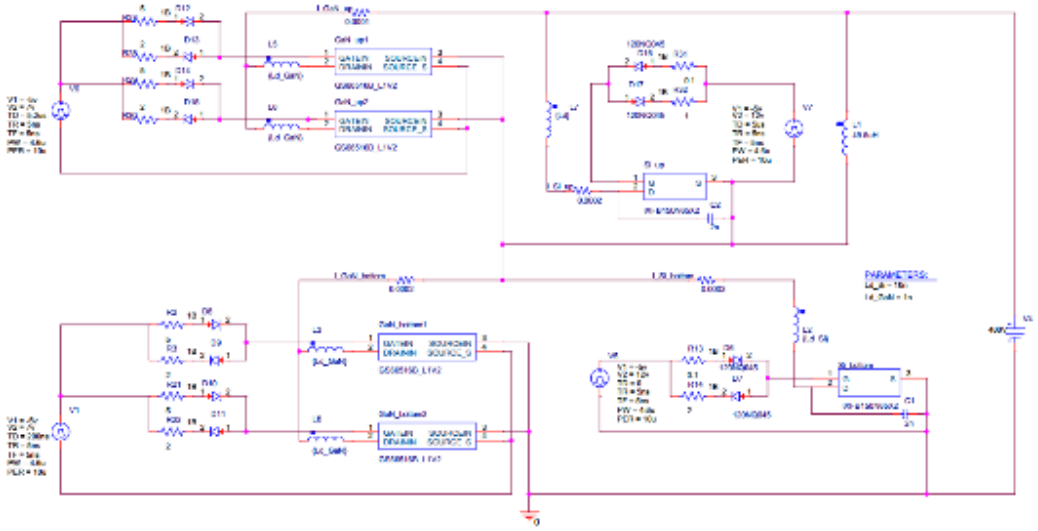


Figure 85 pspice simulation model

Two GaN+Si module with driver were set up, an inductor was parallel with upper module to provides an increasing current through modules in order to investigate the module's performance in different load situations. To allow GaN devices undertake turn off current, a delay of 200ns is insert between driving signal for Si and GaN. The Signal for Si is leaded by signal for GaN.

As shown in Fig.86. Here we use the peak current to subtract the load current IL. For instance, when switching off 70A, at the moment when Si is off, it is observed ~100A peak current in GaN. Both simulation and calculation show similar current overshoot. As shown in fig.81, we can observe a certain overshoot current when Si turns of, Such phenomenon is also observed in experiments, shown as Fig.87.

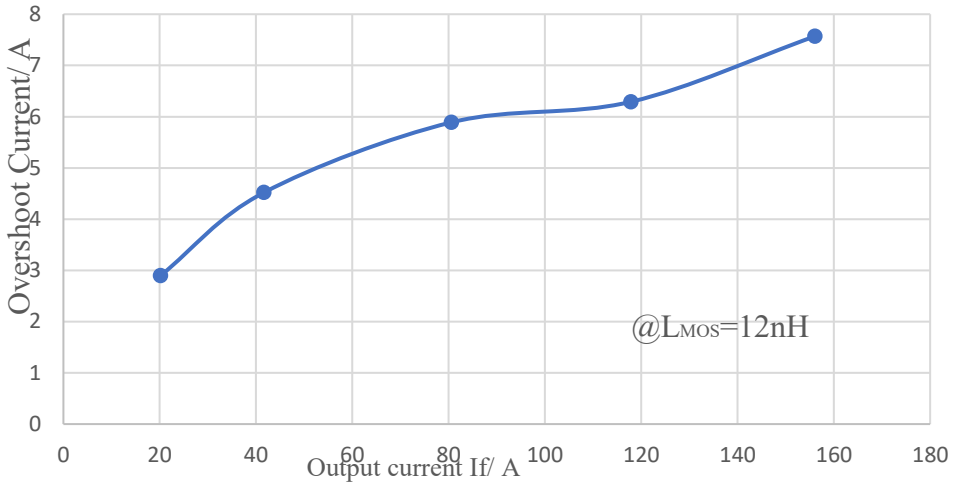


Figure 86 GaN overshoot current during Si switching off

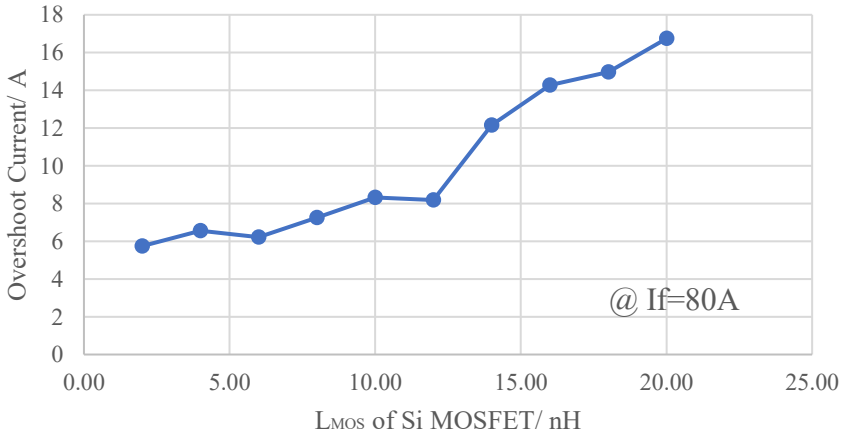


Figure 87 GaN current during Si switching off (experiments @IL=70A)

No obvious harm is done to the switch by such current overshoot, even though it tends to slightly increase the conduction loss. Si parasitics are the main reasons.

The parasitic inductance of Si MOSFET is the main factor that induced this kind of current overshoot. When Si turn off in a short time scale, the energy stored in lead inductance has to find a way to release. The two possible way for current to go is the parallel GaN devices and the series upper module. For upper module, the voltage drop of body diode constrains the current.For different package of the MOSFET, the Ld of a certain device may vary dramatically, thus, it is necessary to investigate the relationship between the Ld and overshoot current for future practical design.

To investigate the relationship between the Ld and overshoot current, Pspice was adopted to perform parametric sweep simulation.

The parametric Ld and overshoot current presents a linear relationship, that can be adopted as a design reference when selecting switch devices.

GaN Switching off. Assume Fig.88 are the bottom switching module of one leg. At the moment when GaN is switched off, the current will freewheel through the top complementary switch, either through the top GaN 2DEG or the intrinsic diode of the top Si MOSFET. When reverse conducting, the MOSFET body diode has ~1V voltage drop while the GaN reverse-conducting voltage drop is different. Given the GaN has no body diode, when reverse conducting, GaN's voltage drop is shown as below.

$$V_{\mathrm{SD}} = V_{th\_GD} - V_{GS\_off} + i_D R_{DSon} \tag{52}$$

Due to the low turn-on VGS threshold of GaN HEMTs (~2V), a negative VGS is recommended to enhance the system reliability and reduce the switching-off loss. However a

VGS=-5V to turn off the GaN yields a VSD= ~7V. Theoretically its paralleled Si MOSFET provides a much lower reverse voltage drop to freewheel all the current.

Both simulation and experimental results shown in Fig.88 and Fig.89 indicate when reverse conducting, even though most of the current goes through the MOSFET body diode, due to Si's large stray inductance, part of current still goes through GaN, which tends to increase the dead-band loss. Such transient, however, reverse conducts the its paralleled GaN once the induced voltage spike by LMOS is high, thereby effectively suppressing VDS spikes of the bottom switch.

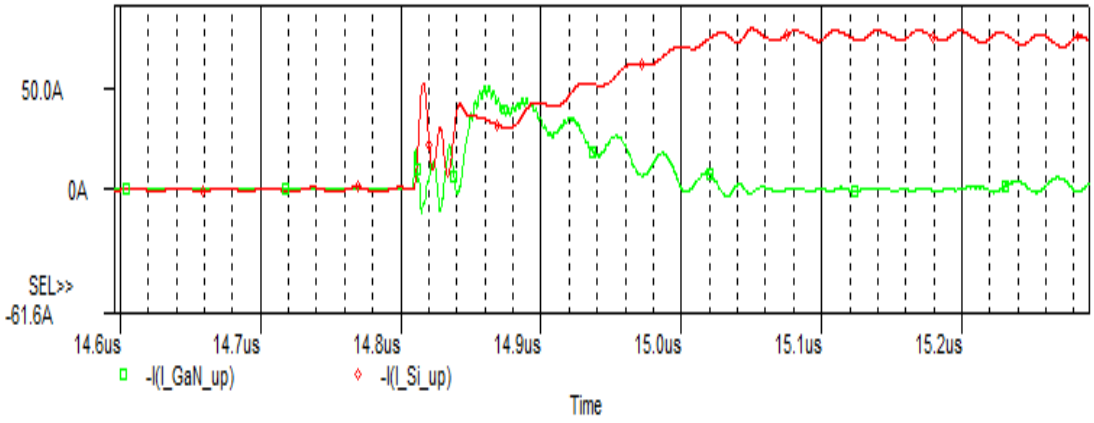


Figure 88 Top GaN+Si Current Distribution when Bottom GaN is Switched Off – simulation result

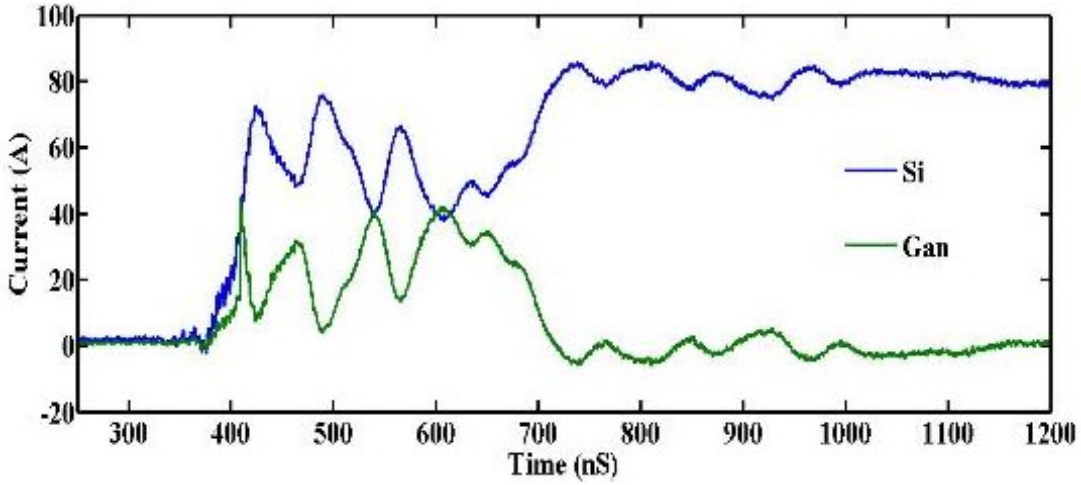


Figure 89 Top GaN+Si Current Distribution when Bottom GaN is Switched Off – experimental result

3.3.3 Design Solution and Layout

The influence of the PCB layout. As what has been mentioned in previous parts, the overshot current and voltage are mainly caused by the parasitic parameters in the power circuit. The parasitic is made of two parts: device and PCB layout. The device parasitic parameters are decided by the package types of devices, so this part of parasitic parameters couldn't be changed. In order to reduce the parasitic parameters' value, the optimization of PCB layout is a practical method. Each module is consist of one si device and two GAN devices. The package of Si Mosfet is TO-247, the to-247 bring in a large value of parasites parameters including loop inductance, which influences the overshoot current and voltage. For sake of research the influence of PCB layout on parasites, several layout plans have been simulated in Q3D model, the fig. shows the several layout plns. In plan A the top GAN faces to bottom GAN, and top Si faces to bottom Si, shown in fig.90. In plan B the top GAN faces to the bottom Si, and top Si faces to bottom GAN, shown in fig.91. Plan C devices facing is same with plan B, but the direction of devices is different, shown in fig.92.

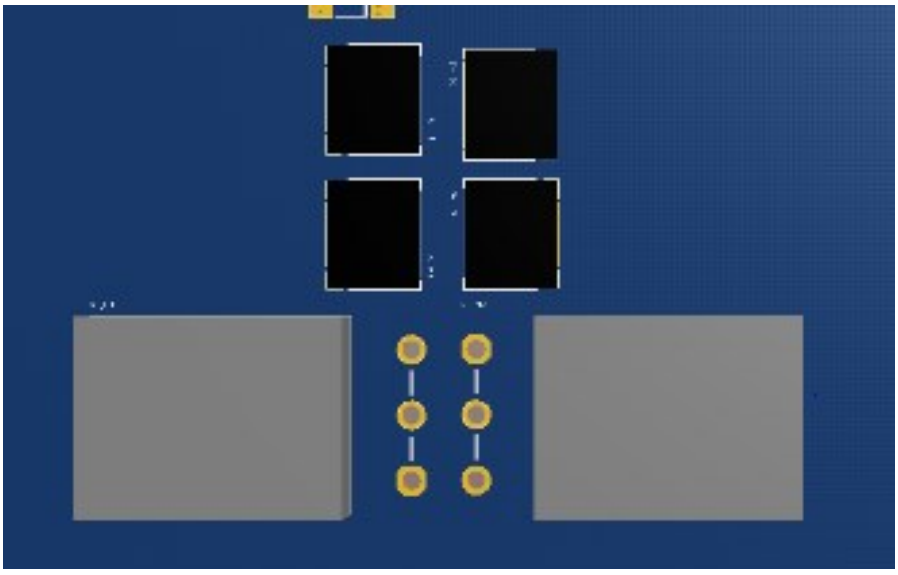


Figure 90 Hybrid layout plan A

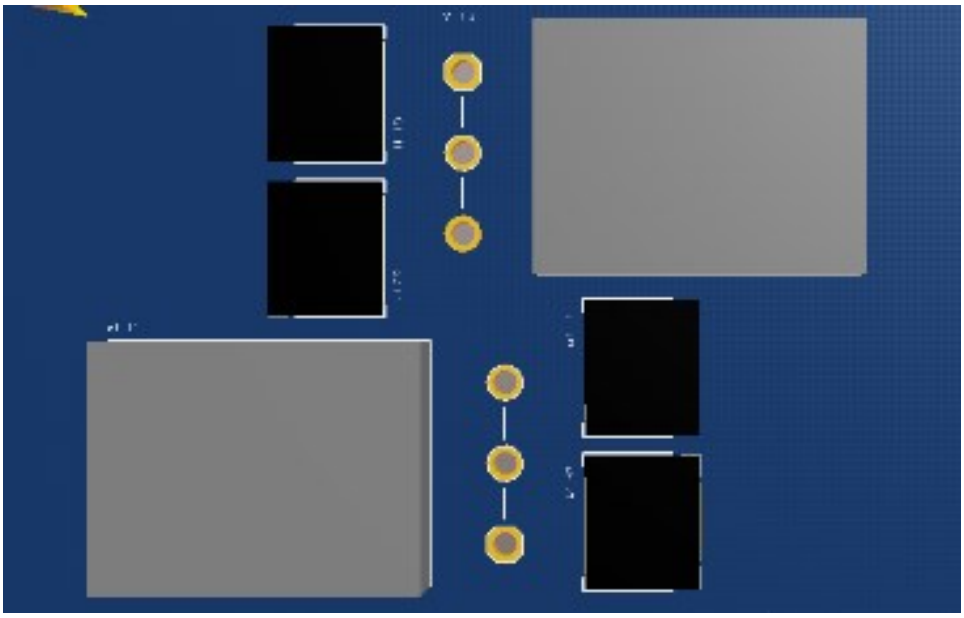


Figure 91 Hybrid layout plan B

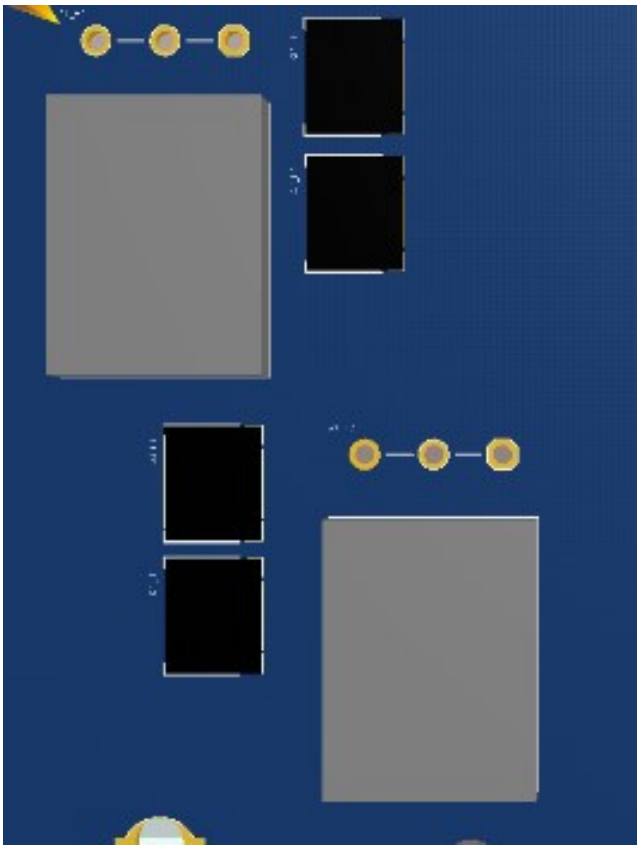


Figure 92 Hybrid layout plan B

According the Q3d result, it shows that in one half bridge, when top Si is closer to bottom GAN, the loop inductance is smaller, which can be explained by the switching progress of two paralleled devices. When bottom GAN is turned off, the current will go through top model. Due the Si body diode reverse voltage is much smaller than GAN body diode reverse voltage So most of current will flow in Si body diode. So the main loop is consist of top Si and bottom GAN. Closer two devices are, the smaller current transform loop is. The loop inductance will be smaller.

Table 6 400V 80A switching simulation table

PLAN	Overshoot current/A	Over voltage/V
A	100%	100%
B	124%	102%
C	97.5%	106%

However due the much large value of TO-247 package, which about 18 nH for package, the value of pcb layout is much smaller. All the Q3d layout values have been used in psipice to simulate the difference on overshoot current and voltage at 400V 80A switching condition. But there is not too much difference as shown in table. So we can come to the conclusion that the Si-GAN hybrid switch module is not sensitive to the parasitic design In porotypes-design, for sake of the size the of board, the Plan C is used as shown in fig.93

Figure 93 PCB layout

3.3.4 Performance Evaluation

A. Power-loss Reduction. The proposed hybrid-switch solution is suitable for the ZVS turn-on applications. Shown in Fig.5a, after Switch_2 is turned off, the inductor current begins to discharge C1 and charge C2. Here C1 and C2 are the output capacitance of the switch, including the switch junction capacitance and other peripheral capacitance, for instance, caused by adjacent PCBs. Once C1 is fully discharged, Switch_1 is ZVS switched on, resulting in no switching-on loss. Such C1 and C2 determine the minimum required current to realize ZVS. A high current to fully charge/discharge C1,2 secures the ZVS, however, it tends to increase the on-state loss and dead-time loss. To fully evaluate its conduction-loss reduction compared to GaN HEMTs at the same current level, we need extract Coss of both pure-GaN design and GaN+Si design.

Figure 87 GaN HEMTs in parallel as one switching module, an experimental method was adopted to extract the parasitic capacitance, as shown in Fig.88. The bottom switch is hard turned on. A current spike is detected to purely charge the capacitance of the top switch given there is no

reverse recovery process. Integral of such current spike (green part in Fig.94. reveals the total charge in the parasitic capacitance, 800nC@ 400VDC. Therefore, equivalently the top-switch Coss is ~2nF, among which 1.3nF is contributed by four paralleled GaN while 0.6 nF results from PCB polygons.

Such method does not work for the hybrid-switch solution, since a hard-turn-on process yields a reverse-recovery current of the complementary body diode. Instead, we could leave both switches off, let the inductor current IL freewheel through the top switch and detect how long it takes for the top switch to fully conduct the current through its body diode (Δt). Therefore, the equivalent leg Coss is shown as (53) and the experimental waveform is shown in Fig.95.

$$C_{\text{oss}} = \frac{I_L \Delta t}{V_{DC}} \tag{53}$$

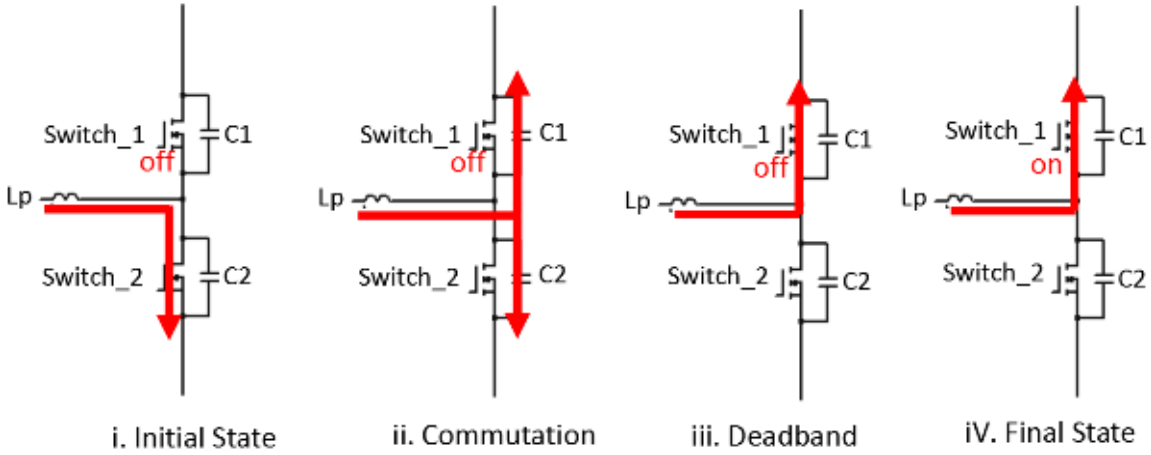


Figure 94 Zero-Voltage Switching-on Process

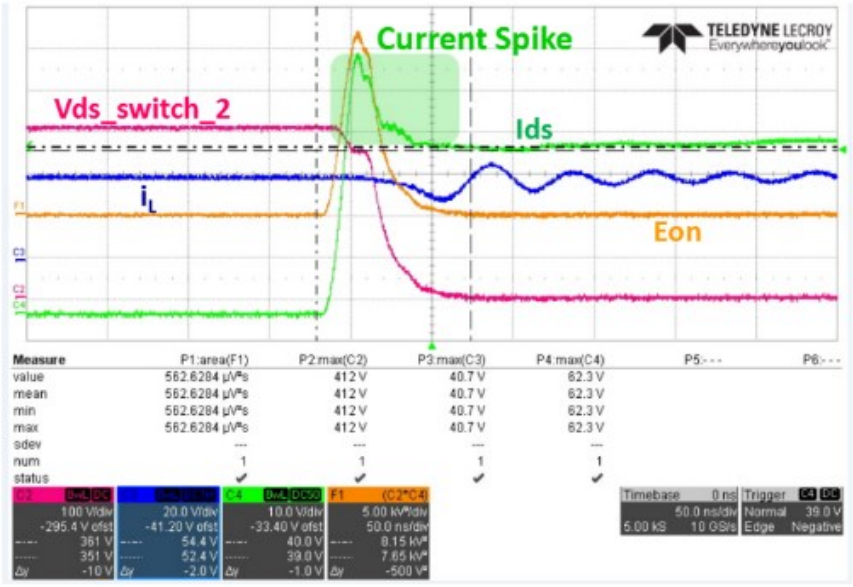


Figure 95 Current Spike Measurement During a Hard-turn-on Process in DPT

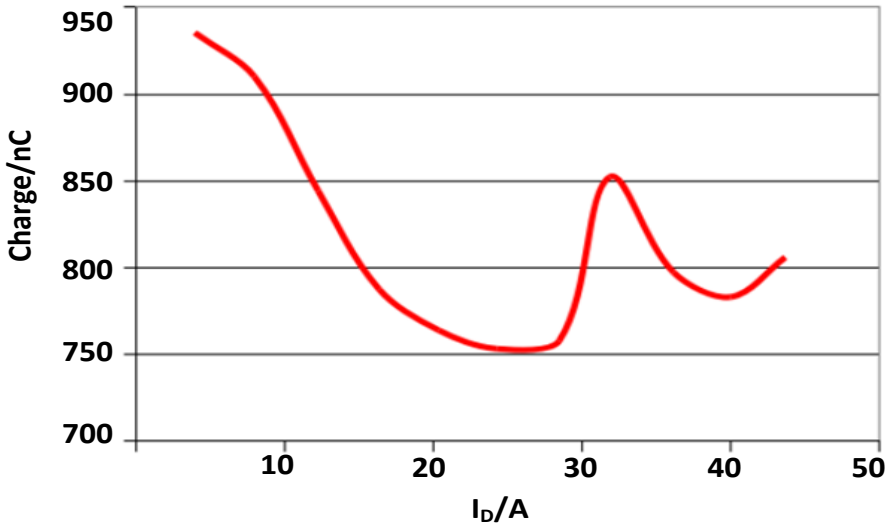


Figure 96 Charge Estimation during a Hard-switching-on Process

Here IL=80A, Δt=21.5ns, VDC=454V. Therefore, the equivalent Coss for the leg is 3.8nF. Assume such Coss is evenly distributed among the top and bottom switch, each top/bottom switching module have the output capacitance as 1.9nF.

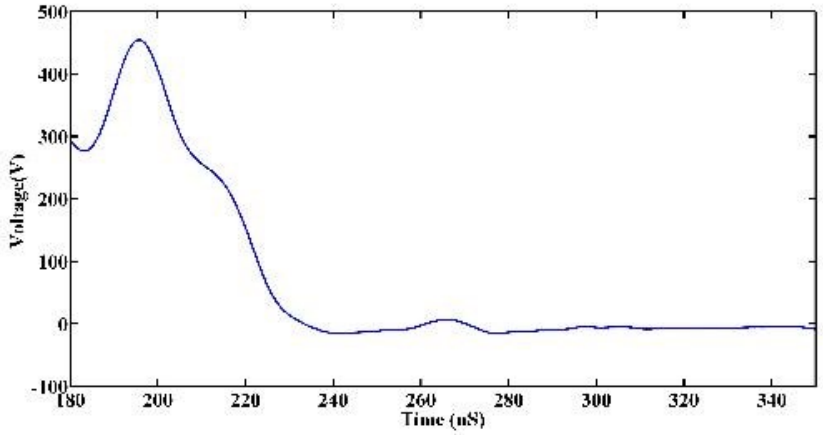


Figure 97 Extraction of the hybrid-switch Coss

The calculated Coss of the hybrid-switch solution is quite close to 4 GaN in parallel. Such similar Coss results in that pure-GaN system and hybrid-switch system could adopt the similar minimum turn-on current, i.e., same ZVS current requirement. Therefore the system based upon the hybrid solution expects to have the same conduction loss as pure-GaN system. With the load current as 80A, a detailed loss breakdown is carried out as Fig.97 based upon the DPT results. Both top and bottom switches are operated with 50% duty cycle at 100kHz. The dead time is 300ns. The hybrid-switch solution has a slightly higher conduction loss (4 GaN has 10.5mΩ while the hybrid solution has 12.45mΩ), cuts deeply the dead-band loss, and maintains switching-off loss nearly unchanged. The switching-on loss is ignored due to the ZVS turn-on. It is validated that such an approach does not only reduce the usage of WBG devices but also shrinks the system loss.

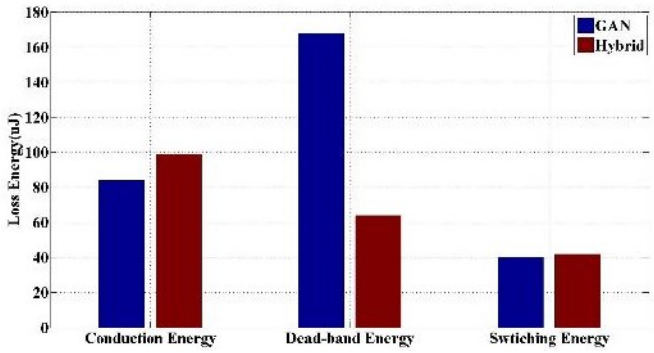


Figure 98 loss breakdown of 4 GaN vs Si+GaN

B. Control Fidelity. Consider a leg made of two complementary switching modules. ZVS turn-on results in a very little output-voltage distortion, if the charging/discharging of the switch output capacitance is ignored in the dead time, seen as Fig.92 for the pure-GaN version. The grey area represents the dead time between two complementary switches. With the proposed hybrid-switch solution shown as Fig.93, both the dead time (grey+brown) and the signal delay (brown) were added, indicating the output voltage of the leg is shifted with one delay. For instance, if the time delay is set as td=300ns, the dead time (between the top Si and bottom Si) setting is tdb*=500ns, the actual dead band between the top Si and bottom GaN is tdb=tdb*-td=200ns. Compared to the original PWM signal, the leg output voltage is shifted one delay td=300ns. The impact of such a time shift is minor, except the micro-controller needs set the dead-band between the complementary PWMs large enough to include the actual dead-time and the time delay.

The figure comparison between pure Si version and Hybrid version at same duty cycle. The fig show the wave form of pure Si version. The fig shows the wave form the hybrid version. These two figures show that the hybrid and Si version have the same waveform at same duty control. The result verify the above control fidelity. The green line is the transformer side voltage, the blue line is the transformer current as shown Fig.101.

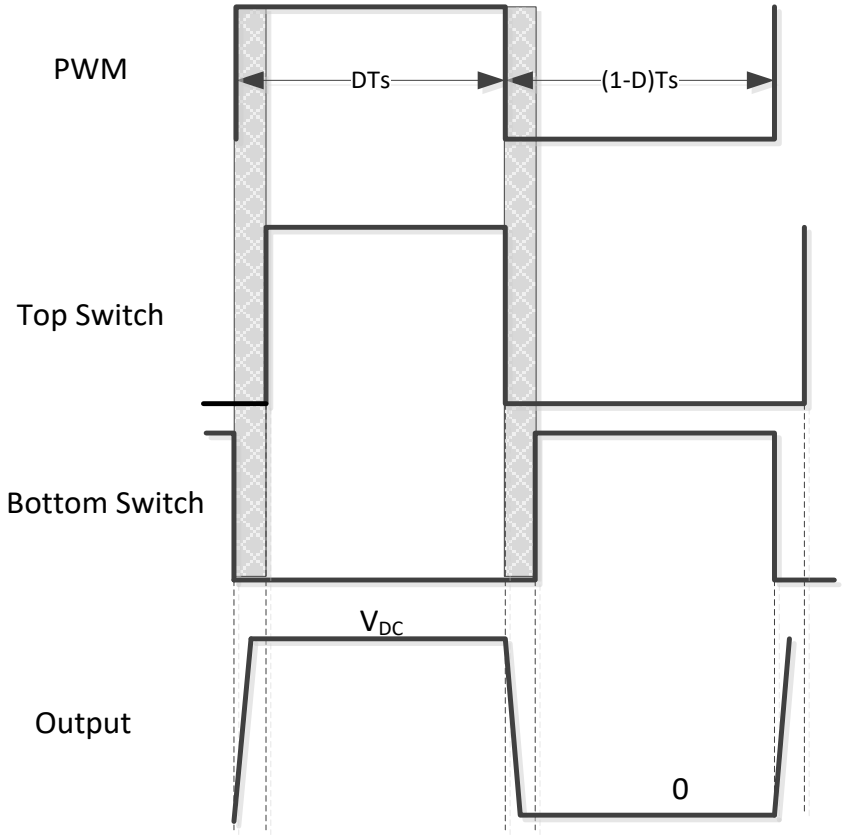


Figure 99 Conventional design

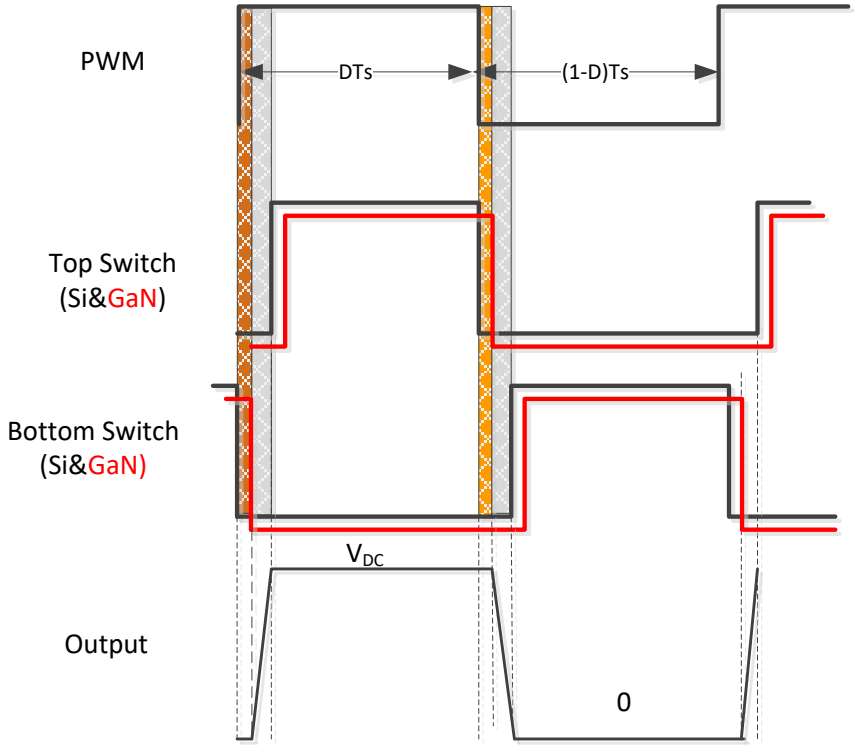


Figure 100 Hybrid-switch solution

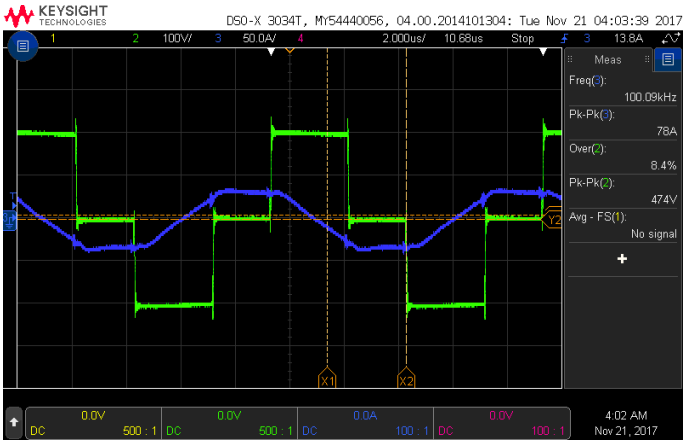


Figure 101 test waveforms

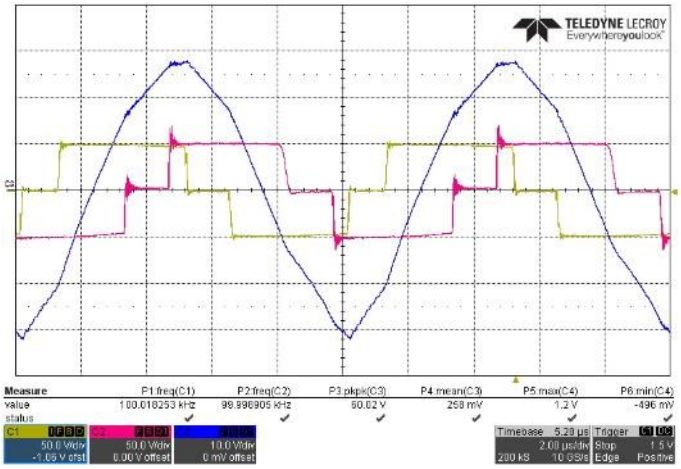


Figure 102 Primary side and secondary side's test waveforms

The yellow line is the primary side voltage, the purple line is the secondary side voltage. The blue line is the transformer current. It is hybrid 50V DC input, 50V DC output 450W figure

3.3.5 Conclusion

A GaN+Si hybrid-switch solution was fully evaluated in this paper from the switching transient process to the steady-state performance, particularly useful for the ZVS turn-on applications. Si MOSFET is off before paralleled GaN HEMTs, resulting in that the stray inductance inside the TO-247 package generates a current overshoot inside GaN. The dead-band

loss is minimized by the Si body diode, however due to the Si parasitics, not all current goes through the Si body diode during the dead band.

The proposed approach was validated on the DPT bench, especially its success of maintaining the switching-off and conduction loss while deeply cutting off the dead-band loss brought by GaN. It is expected that such approach will result in an even higher efficiency when used with ZVS turn on. A brief analysis of its impact on the control strategy shows no obvious distortion on the control waveforms except a time shift. Future work will be applying such design to an actual prototype, e.g., an EV battery charger to validate its effectiveness in real applications.

Chapter 4 Interleaved Boost Converter Design Case with Sic Power Module

4.1 Interleaved Boost Converter Hardware and Software Overall Optimization Design

4.1.1 Introduction

The interleaved boost converter has been widely used as a power converter in the electric vehicle field and other similar fields [99–104]. The interleaved technology connects the multiphase boost converter through a coupled inductor, as shown in Fig.103.

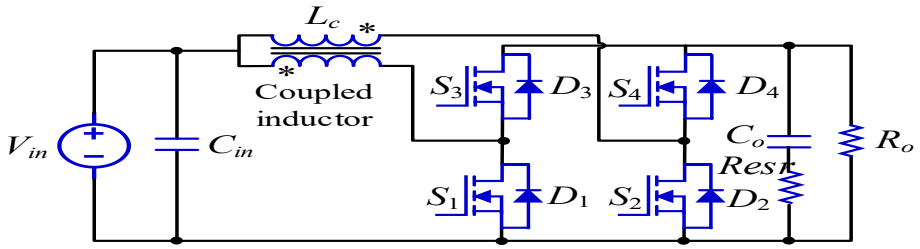


Figure 103 Two-phase interleaved boost converter circuit topology

Compared to other boost converters, the interleaved boost converter, with its interleaved technique, can reduce switching losses, output voltage ripple, and input current ripple [105–106]. What remains the main research hotspot, however, is how to improve system performance, including how to increase the efficiency and power density while reducing current ripple. Although many soft switching circuits have been proposed to reduce power MOSFET loss [107–109], this method is not helpful in reducing the hardware cost and circuit complexity. Some higher-performance inductor design methods [110–111] have also been proposed to reduce the

inductor volume and increase inductor efficiency, but these methods do not consider the power MOSFET's working conditions, and while some new control methods have been proposed as well to improve current ripple [112–113], these methods ignore the influence of the closed-coupled inductor and increase the software complexity. Another main research point for the interleaved boost converter is the coupled inductor design. The coupled inductor is applied in converter designs such as the DC-DC converter [114-117] and the DC-AC inverter [118-119]. Compared to the traditional inductor, the coupled inductor can increase the power density, prevent magnetic saturation, and decrease ripple current.

Optimization control and design have been widely applied in converter design and control [120–123] to improve efficiency, power density, and output performance. In paper [124], a sliding control mode was proposed to realize the MOSFET conduction mode and diode conduction mode shift to realize near-optimal control. In [125–126], simplified optimal trajectory control has been proposed for the LLC circuit. In order to meet increasing optimization target requirements, a multiple-objective optimization algorithm has been applied to the electrical power field [127–131]. In [131–132], the multiple-objective optimization algorithm is used to optimize the motor design to achieve better performance.

This part combines the inductor design and the software-controlled switching frequency into a simple mathematical model. The inductor design parameters and switching frequency are the optimization variables, and the overall system efficiency, inductor volume, and input current ripple are the optimization objectives. The widely used multiple objective optimization algorithm NSGA-II has been applied to solve the interleaved boost converter design problem. Firstly, the overall system mathematical model is introduced. Then the paper introduces the optimization

flow of the NSGA-II. Finally, the optimization results are presented. In addition, a test bench has been set up to verify the effectiveness of the optimization results.

4.1.2 Overall System Mathematical Model

The overall system can be divided into the inductor design and the power MOSFET stage. The inductor design starts with the selection of the inductor type. The inductor type is selected from several different types of inductors, as shown in Fig. 104. The loosely coupled inductor (LCI) converter has the minimum inductor volume that falls within our selected duty ratio range, so in this paper, the LCI inductor has been selected as our optimization inductor type.

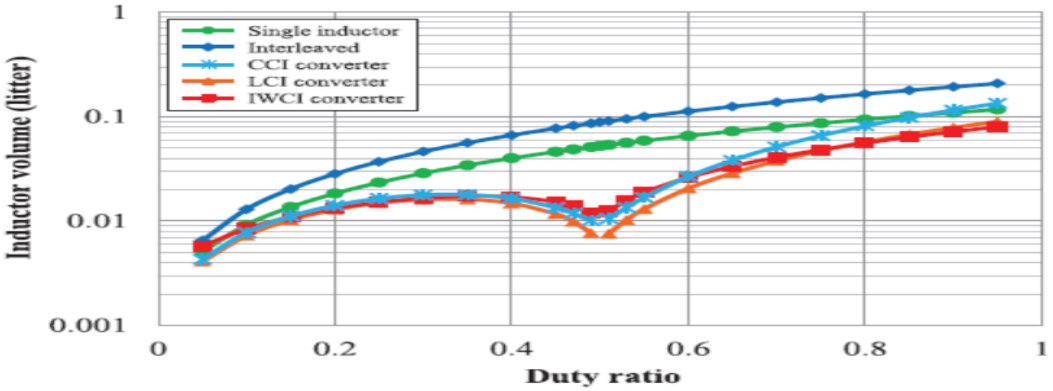
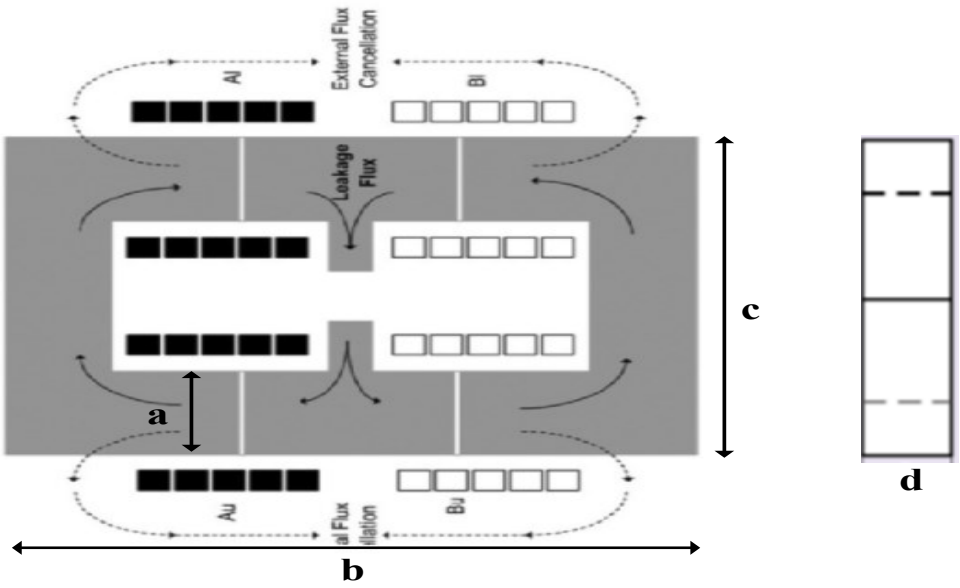
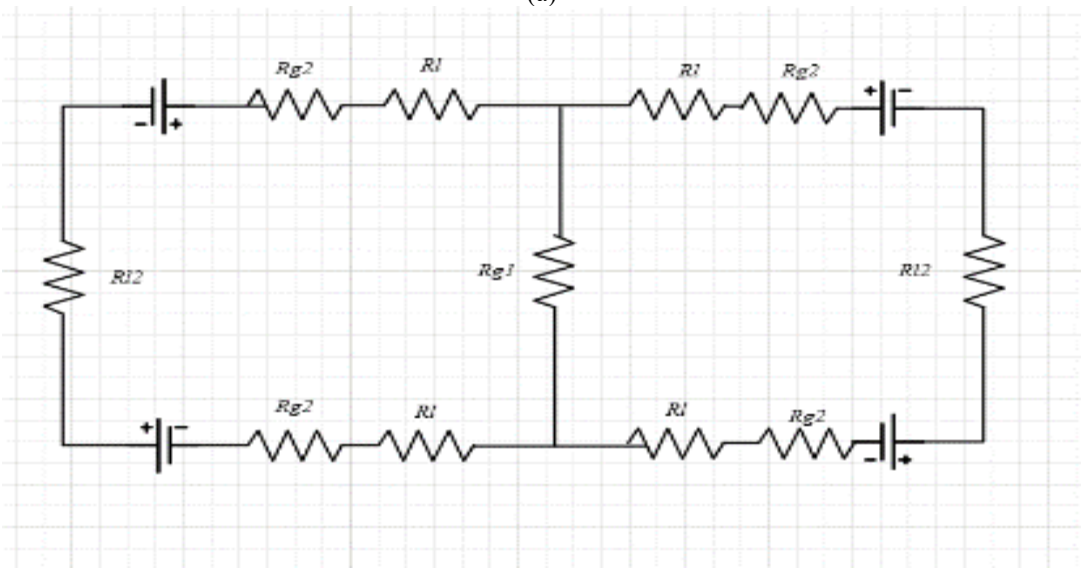


Figure 104 Different inductor converters' volume comparison

Our LCI inductor core is composed of two U-type cores and two convex-type cores, as shown in Fig.105 (a). a is the inductor core section length, b is the inductor length, and c is the inductor width. d is the inductor thickness. After applying the magnetic method to the inductor, the inductor magnetic loop can be converted into the circuit diagram shown in Fig. 105 (b).



(a)



(b)

Figure 105 (a) Inductor magnetic flux diagram; (b) Magnetic resistance inductor circuit

(b) magnetic circuit could be simplified into:

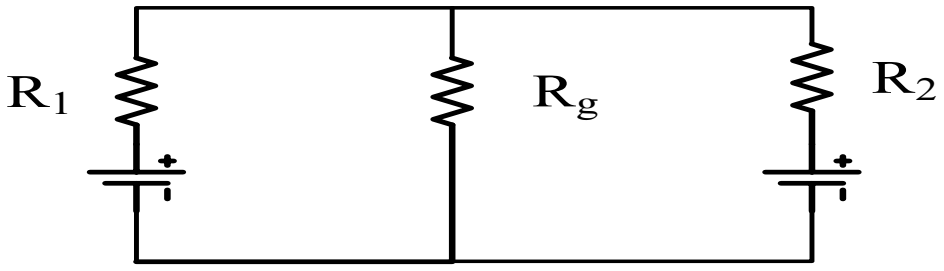


Figure 106 Simplified magnetic circuit

According to the magnetic resistance circuit, we can attain the values of self-inductance L and mutual inductance M through equations as below:

$$R_1 = R_{l2} + R_{g2} + R_l \tag{54}$$

$$R_1 = R_2 = R \tag{55}$$

$$\mathrm{L} = \frac{\mathrm{N_p}^2 (Rg + \mathrm{R})}{R^2 + 2R_g R} \tag{56}$$

$$M = \frac{N_p{}^2 Rg}{R^2 + 2R_g R} \tag{57}$$

The magnetic flux flowing through the phase leg is:

$$\psi = \frac{N_p IR}{R + \dfrac{RgR}{Rg + R}} + \frac{N_p I \dfrac{RgR}{Rg + R}}{Rg + \dfrac{RgR}{Rg + R}} \tag{58}$$

$$\mathrm{B} = \frac{\psi}{a^2} \tag{59}$$

Here, N_p is the winding number. R_g and R_{g2} are the air gap magnetic resistance. R_l and R_{l2} are the inductor core phase leg magnetic resistance.

The inductor loss calculation equations are:

$$B = \frac{0.4\pi N_p I_{ripple}}{L-M} \tag{60}$$

$$P_{core} = 6.5Wfs^{1.51}B^{1.74} \tag{61}$$

$$I_{ripple} = \frac{(1-\alpha)(\alpha - 2)V_{in}}{2\alpha(L-M)f_s}(\alpha < 2)$$
$$I_{ripple} = \frac{(\alpha - 2)V_{in}}{2\alpha(L-M)f_s}(\alpha > 2) \tag{62}$$

$$\mathrm{V}_L = bcd \tag{63}$$

W is the weight of the inductor core. f_s is the switch frequency. B is the magnetic flux of the inductor. V_{in} is the input voltage. α is the boost ratio. V_L is the inductor volume. I_{ripple} is the input ripple current.

The power stage of the interleaved boost converter is composed of four power MOSFETs, The power loss of the power stage can be classified as conduction loss, switching loss, or deadband loss.

The conduction loss equation is:

$$P_{cond} = I^2_{rms}R_{\mathrm{dson}} \tag{64}$$

Here, I_{rms} is the RMS value of the MOSFET current. R_{dson} is the conduction resistance of the MOSFET.

The switching loss equation is:

$$P_{Switch} = f_s(E_{on} + E_{off})\frac{U}{U_{ref}}\frac{I}{I_{ref}} \tag{65}$$

Here, E_{on} and E_{off} are the energy MOSFET turn on and turn off energy. U_{ref} is the reference voltage. I_{ref} is the reference current. U and I are the operation current and voltage of the MOSFET, respectively.

The dead band loss equation is:

$$P_{\text{dead}band} = V_{diobe} I f_s t_{deadband} \tag{66}$$

So the total overall system loss is:

$$P_{Total} = P_{core} + P_{conduction} + P_{switch} + P_{deadband} \tag{67}$$

Furthermore, the system mathematical model still has 2 limitation conditions. The main limitation conditions of our system model are: (1) the inductor saturation status, as shown in Eq. (15), and (2) the window coefficient. The saturation limitation is to avoid saturation status. Saturation is normally caused by a high winding current. The large current generates too much magnetic flux, which could be higher than the maximum value of the core material. The window coefficient is the value used to evaluate the heat distribution ability of the inductor design. Usually, it should be larger than 0.5.

$$B < B_{\max} \tag{68}$$

$$K_w = \frac{HWN_p}{A_w} \tag{69}$$

$$\mathrm{A_w} = \frac{(b-2a)(c-2a)}{2} \tag{70}$$

H is the thickness of the winding copper wire. W is the wildness of the winding copper wire. Aw is the window area space.

4.1.3 Multiple Objective Optimization

The main loss of the interleaved boost converter system has been classified into two parts: inductor loss and MOSFET loss. Both losses are influenced by the selected switching frequency. At a given power condition, the higher frequency will increase the MOSFET switch operation times and then increase the switching loss and deadband loss. The calculated MOSFET power losses at 50kW, 25kW, and 15kw are shown in Fig. 107–Fig. 109. However, a higher switching frequency could lower the current ripple in the coupled inductor and then decrease the inductor loss. The Maxwell inductor simulation results are shown in Fig. 109. The MOSFET and inductor loss change curves are shown in Fig. 110, and the inductor loss calculated curve is shown in Fig. 111 The simulation results verified the accuracy of the calculated inductor loss mathematical model.

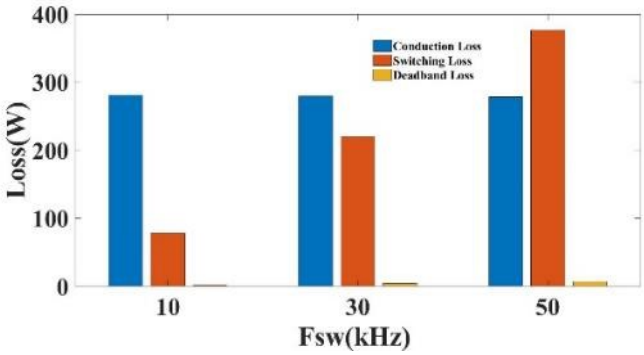


Figure 107 MOSFET loss at 50kW

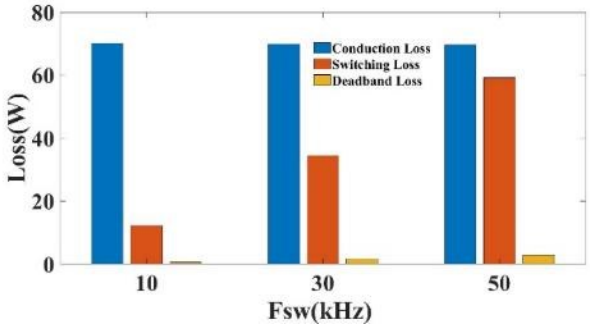


Figure 108 MOSFET loss at 25kW

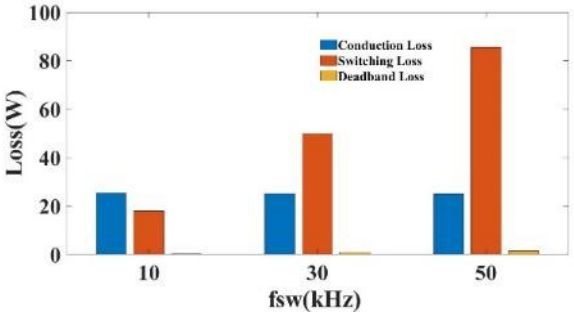


Figure 109 MOSFET loss at 15kW

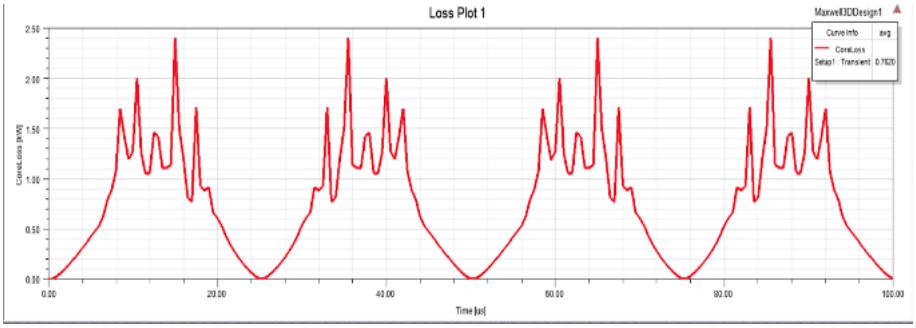


Figure 110 Inductor loss simulation loss result at 50kW

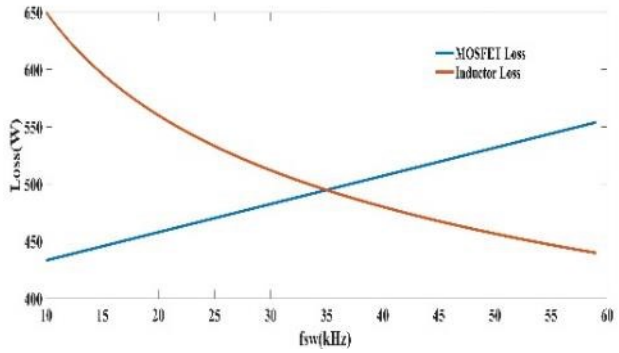


Figure 111 MOSFET and inductor loss change with the switching frequency at 50kW

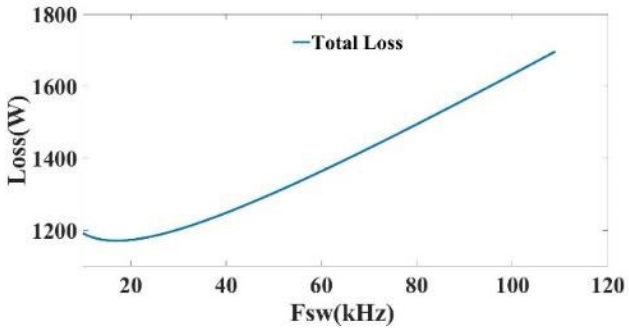


Figure 112 Total loss change with the switching frequency at 50kW.

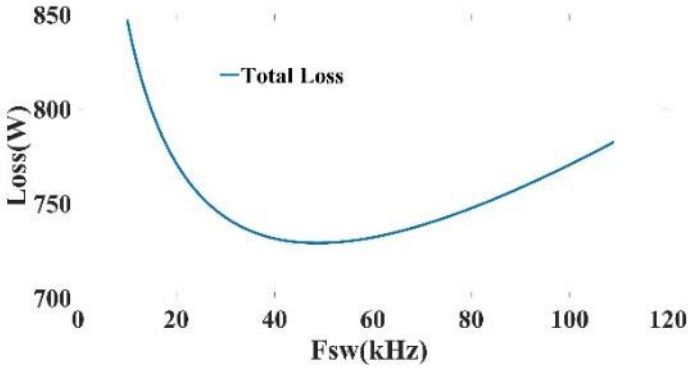


Figure 113 Total loss change with the switching frequency at 25kW

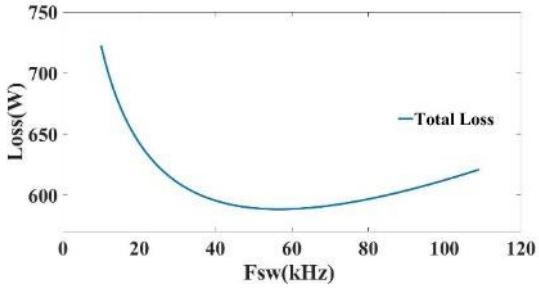


Figure 114 Total loss change with the switching frequency at 15kW

From the above analysis we can see that when the switching frequency goes higher, the power loss will increase but the inductor loss will decrease. Therefore, from the point of view of the overall system, the most efficient switching frequencies are different under different power levels and current conditions. As the power rate grows, the optimization working frequency changes from 90kHz to 30kHz when the power changes from 15kW to 50kW. Based on the previous loss condition, the best switching frequency point may be calculated at different power levels. The best switching points curve is shown in Fig. 115. The overall system control loop is shown in Fig. 116. The control loop will use ADC to get the output power voltage information first. Then the system will compare the output information and set reference power information. Then the DSP will adjust duty cycle for the power MOSFET.

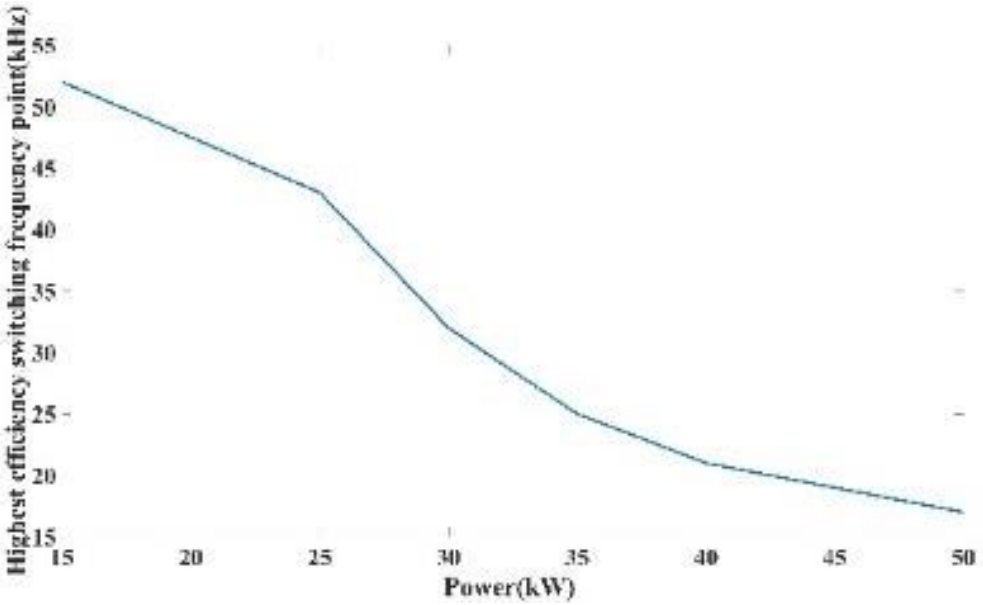


Figure 115 The highest efficiency switching frequency point curve

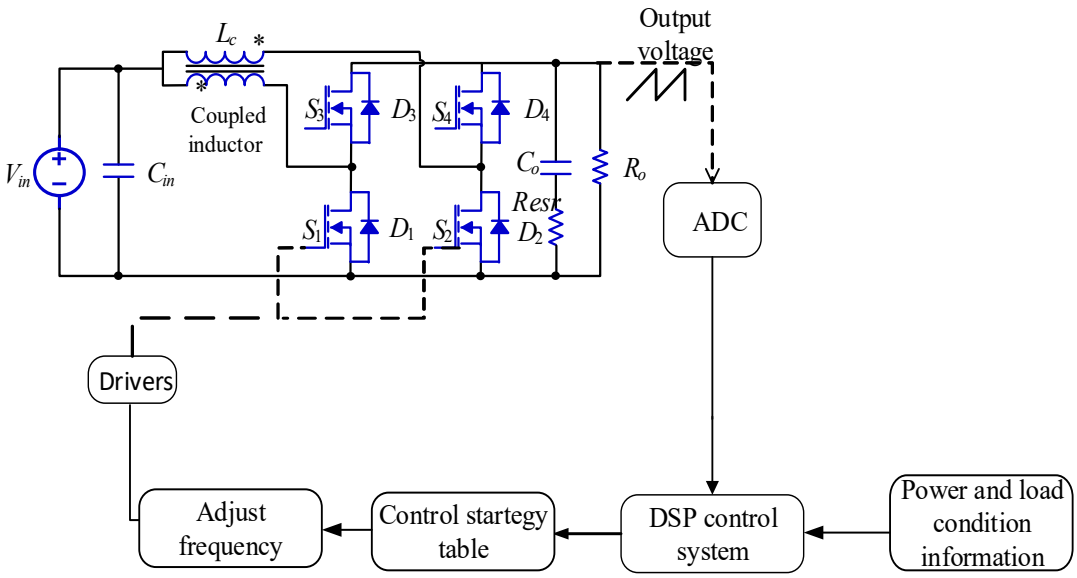


Figure 116 The control system loop

4.1.4 Hardware Component's Design

In order to decrease the physical size of the overall system to achieve a higher power density, the hardware components' selection is processed before the multiple-objective optimization. The main hardware components in the overall system are mainly composed of two parts: power MOSFETs and capacitors. Based on the system's rated power application (50kW), the related power-rate MOSFETs are compared in Table 9. In order to meet the design requirements, multiple single To-247 package MOSFETs need to be paralleled, with at least four together. This will increase the device volume and current-balancing difficulty. Thus, the power MOSFET module is selected as the solution to our design.

Based on the overall system power level, the input capacitor power level is selected at 600V and the output capacitor power level is selected at 800V. Multi-layer ceramic capacitors (MLCC) have higher power density compared to film capacitors. However, because ceramics tend to be weak in tension, a crack is relatively easily formed when excessive board flex is put on the soldered MLCC. Hence, an electrical conduction between the two electrodes would occur,

which would further progress the capacitor toward a short circuit. Therefore, due to these reliability concerns, MLCCs are not preferred for automotive power electronic applications. As a result, film capacitors with good current capability are considered. The related power film capacitors are compared in Table.7 and Table 8. The TDK company capacitors have a higher current rating and lower volume at the same power and capacitance level, so TDK capacitors are selected in our design.

Table 7 600V film capacitors comparison

Manufacturer	Capacitor/uF	Current /A	Dimension/mm
Panasonic	25uF	13.8	22 x 36 x 41
TDK	25uF	17	28.0×37.0×42
Vishay	25uf	13	21.5 x 38.5 x 43
KEMT	20uF	11	20 x 40 x 42

Table 8 800V film capacitors comparison

Part number	Capacitor	Current	Dimension
Panasonic	20uF	15.8A	26.5 x 40.5 x 41
TDK	20uF	19A	30 x 45 x 42
Vishay	20uF	12A	21.5 x 38.5 x 43
KEMT	20uF	15A	30 x 45 x 42

The overall power loop is also important in a high-power application. A longer power loop will increase the loop inductance significantly in a higher-power application. Compared to the Si MOSFET, the SiC MOSFET has a higher switch frequency and speed. In the overall system design, the flux canceling method is applied to reduce the power loop parasitic inductance. The power loop current-flow path is shown in Fig. 117. Based on the designed power loop, a double-pulse test has been performed to verify the designed power loop's effectiveness, and the test waveforms are shown in Fig. 118. It can be seen that at the 600V power-switching

point, when the current is 60A, the overshoot voltage is around 30V in 200ns, so the power loop parasitic inductor value is 100nH, which can meet the system working requirements.

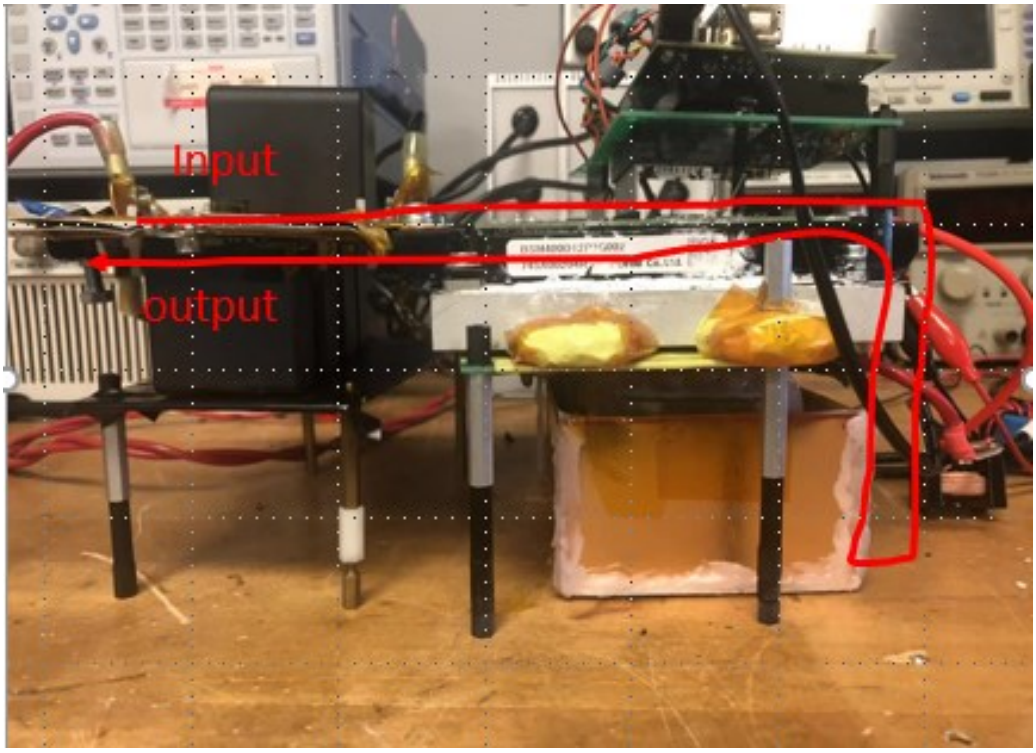
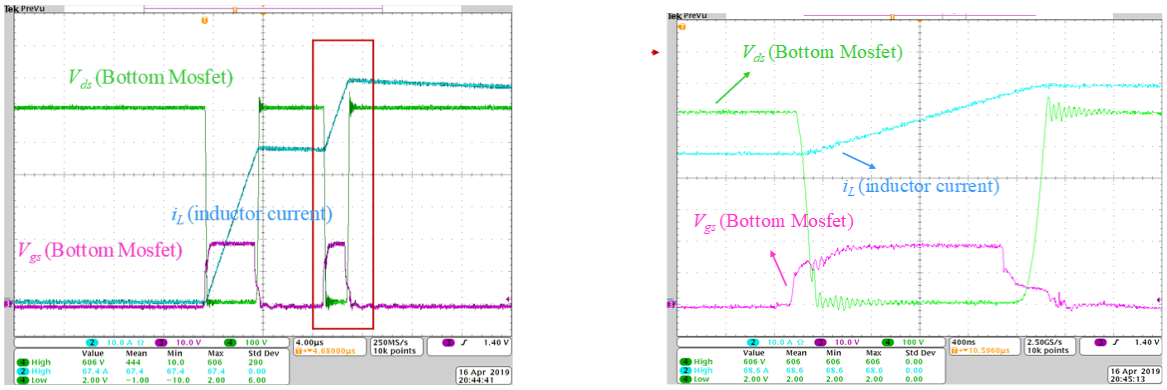


Figure 117 System power-flow path

Table 9 The MOSFETs' parameters

MOSFET	R_{dson}/ohom	package	Current /A	Dimension/mm	Qg/nc	Eon/Eoff(mJ)	VSD/V	Coss/pf
C3M0016120K	16	To-247	115	40 x 14 x 5	211	1.1/0.8	4.2	230
CAB400M12XM3	3.2	XM-3	400	80 x 53 x 19	908	7.5/3	5	1000
BSM400D12P3G002	4	Half-Bridge	358	152 x 62 x 17	1125	18/9	2.1	2000
UF3SC120009K4S	11	To-247	120	40 x 14 x 5	234	3.5/0.7	4.1	755
NTHL020N120SC1	20	To-247	103	40 x 14 x 5	203	2.7/0.3	3.7	260



(a) (b)

Figure 118 Double-pulse test waveforms: (a) two pulses test waveform, (b) the second pulse zoom

4.1.5 Multiple Optimization Algorithm NSGA-II Application

The optimization problem can be summarized as a multiple-objective optimization problem. The optimization variables are the inductor dimension parameters and the switching frequency. The optimization objective is to increase the overall system efficiency, increase system power density, and reduce the current ripple. In order to solve this multiple-objective optimization problem, the NSGA-II has been applied to the proposed problem. The algorithm flow is as follows:

Step 1: Generate the individual vectors that contain optimization variables in a given search range.

Step 2: Sort all the individual vectors based on non-domination.

Step 3: Use selection, mutation, and crossover to generate the temporary general individual vectors.

Step 4: Use the crowding distance sorting principle to find the next-generation vectors.

Step 5: Repeat steps 2–4 until evolution is complete.

The boost converter design problem results are shown in Fig. 119. All the optimization points constitute a Pareto front surface.

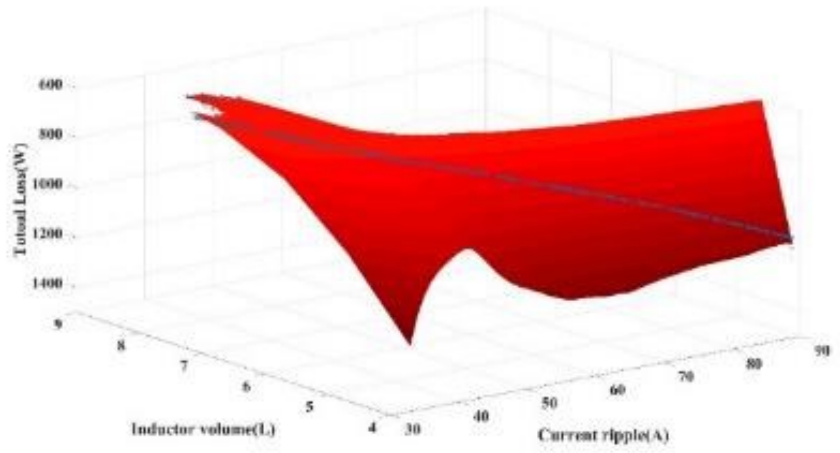
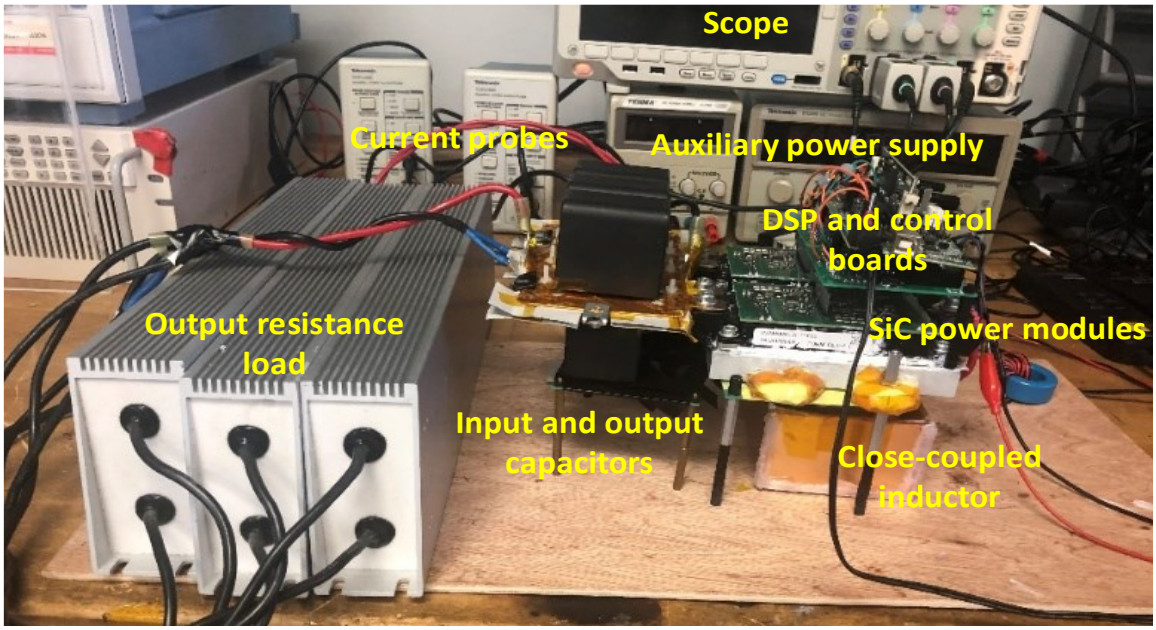
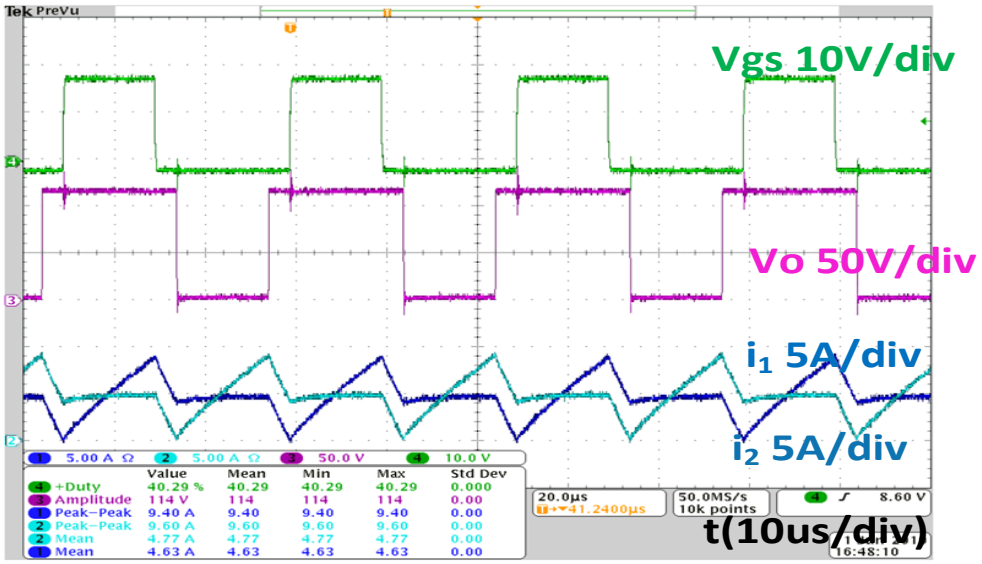


Figure 119 Optimization result: Pareto front surface

One point on the Pareto front surface presented in Fig. 16 has been selected as our interleaved boost converter design solution to build a test bench, as shown in Fig. 120 (a). The 70V input voltage test waveform is shown in Fig. 120 (b).



(a)



(b)

Figure 120 (a) The two-phase interleaved boost converter test bench; (b) 70V input voltage test waveform

4.1.6 Conclusions

In this part, an overall system mathematical model has been built. Through this model, the complex boost converter design problem has been converted into a multiple-objective optimization problem. The inductor dimension parameters and switching frequency are the optimization variables, and the system efficiency, inductor volume, and current ripple have been

selected as the optimization objectives. The NSGA-II algorithm has been applied in the model to solve the summarized optimization problem, obtaining a Pareto front. An experiment test bench was set up to verify the optimal results.

4.2 Current Senseless Control for Multiple Phase Interleaved Boost Converter

4.2.1 Introduction

Interleaved topology has been widely applied to electric vehicles due to its advantages of high power density, high efficiency, and low input current ripple. Interleaved technology has been applied in PFC converters [133-136], photovoltaic applications [137-138], and automotive applications [139-142]. Compared to other traditional set-up converter setups [143-146], the interleaved boost converter can reduce the input current ripple through the magnetic coupled inductor. Meanwhile, the magnetic coupled inductor can reduce the inductance volume. The smaller ripple current also could lower the capacitor value requirement. Compared to the double dual boost [147-149] or switched capacitor [150-151] converter, the interleaved boost converter requires less capacitor and inductor components. The hardware design will be simplified. Also, the coupled inductor could share the current stress in each phase to reduce phase current stress. Compared to cascade and quadratic converter [152-155], interleaved boost converter could simplify the hardware design and reduce the input current ripple. Generally, due to fabrication errors, the parameters of coupled two-phase inductors cannot be identical, which consequently leads to an imbalanced phase current. In addition, some occasional control errors will cause the different phases' MOSFET drive signal values to be unequal, which in turn leads to an imbalanced phase current. The imbalanced current will cause one phase to undertake more

current stress and therefore generate more heat loss, eventually leading to a reduced one-phase power MOSFET lifetime. Moreover, a higher single-phase inductance current can cause one phase inductor to become saturated, ultimately leading to components being damaged.

The conventional phase current balance method [156–158] monitors each phase current by inserting a current sensor into each phase. The current loop is treated as the inner loop, and the voltage loop is treated as the outer loop. The outer loop voltage is used as the inner current loop reference.

Some other research works [159–164] have proposed other technology to reduce the number of current sensors to one. A summary of phase current balancing methods is shown in Table 1. [159–160] proposed measuring the one-phase current rather than the two-phase current. By using the output voltage information, the other phase current value could be obtained. [161–162] proposed a current balance method based on the DC link current. Each phase current could be calculated by decoupling the DC link current. [163–164] used one current sensor to measure the power switches' total current. Based on the switching operation model, each phase current value could be acquired.

In recent years, the sensorless control method has been widely applied in different types of power converters. Eliminating current sensors can reduce system complexity as well as eliminating the current loop, which can simplify the software design. In [165–168], the sensorless current control method is applied to a dual active bridge converter, from which they use the input and output voltage to calculate the current. In [169–173], the sensorless control method is applied in a buck converter. They also use the input and output voltage to estimate the current balance status. [174–176] apply sensorless current control technology in a PFC converter,

using the input voltage, output voltage, and control parameters to estimate the current distribution status.

However, sensorless control methods in an interleaved boost converter have not been fully discussed. Traditional interleaved boost converters [176-178] need current sensors to balance the different phases' currents and putting a current sensor on each phase inductor is the most common current-balancing method. This method is easy to realize but requires a higher quantity of current sensors and introduces parasitic parameters. Using one current sensor [177-179] on the bus lane is another method for current balancing, which reduces the number of current sensors but requires complex calculations to decouple the bus current from the phase current.

We propose a sensorless current control method for a multiphase interleaved boost converter. Instead of sampling the phase current value, the output voltage is used to adjust the phase current. The circuit topology operation principle, the imbalanced phase current diagnosis method, and balance adjustment are discussed. The rest of the paper is summarized as follows: First, the basic interleaved boost converter topology and operation principle are introduced. Then the relationship equations between the phase current and other system parameters are derived. After that, the paper describes a two-phase interleaved boost converter model set up to simulate the output voltage in the imbalanced phase current condition. We also present imbalanced current simulation waveforms, and the relationship between the phase current status and the output voltage ripple is analyzed. Finally, experimental results under different voltage, switching frequency, and resistance load conditions are used to verify the effectiveness of the proposed sensorless control method.

Table 10 A comparison between different current balancing methods

Reference	[166–168]	[169–170]	[171–172]	[173–174]	Proposed
Current sensor amount	2	1	1	1	0
Voltage sensor amount	1	1	1	1	2
Sensor location	Inductor current	Inductor current, and output voltage	DC link current	Switches total current	Output voltage
External calculation loop	No	Yes	Yes	Yes	no
Series/ parallel	series	Series and parallel	series	parallel	parallel

Fig.121 shows the circuit of a two-phase interleaved boost converter with an input coupled inductor, in which the two phases of the SiC MOSFET (S1~S2) gate the drive signal shift 180 degrees between each other. The two phases' currents alternatingly flow into the output side. This converter can operate in two modes, D>0.5 or D⩽0.5, where D is the duty cycle of S1 and S2. Herein, the condition of D>0.5 and D⩽0.5 is discussed, and each condition is further divided into three modes. The D>0.5 condition is composed of Modes 1, 2, and 3. The D⩽0.5 condition is composed of Modes 1, 3, and 4. Fig. 122 illustrates the equivalent circuit of each mode

Mode 1: As shown in Fig. 122 (a), S1 is on and S2 is off.

Mode 2: As shown in Fig. 122 (b), both S1 and S2 are turned on at the same time.

Mode 3: As shown in Fig. 122 (c), S1 is off and S2 is on. This stage is similar to Mode 1.

Mode 4: As shown in Fig. 122 (d), Both S1 and S2 are off.

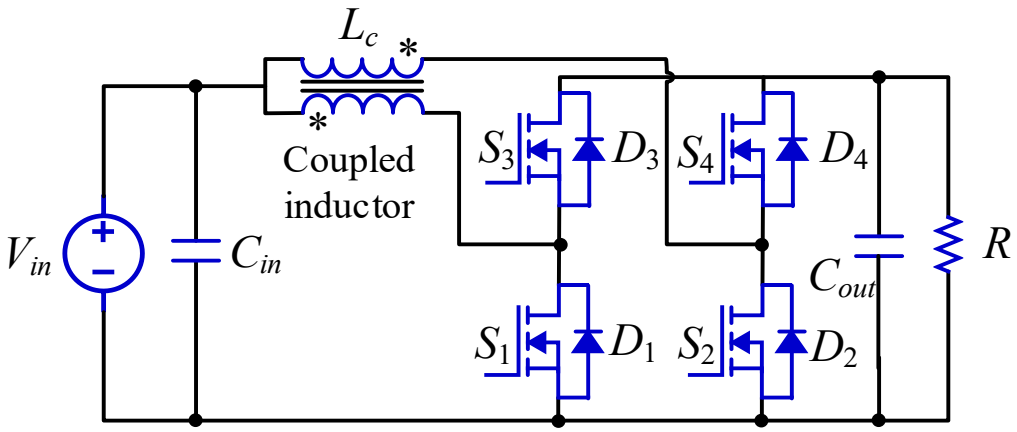
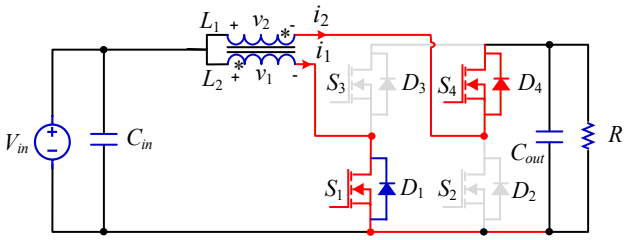
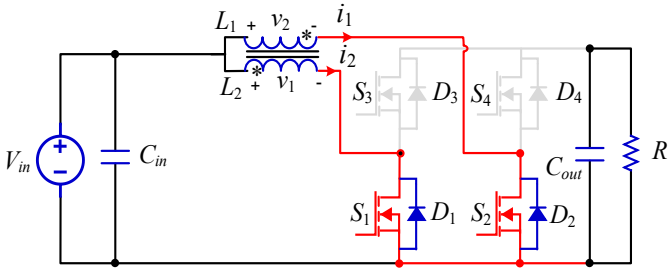


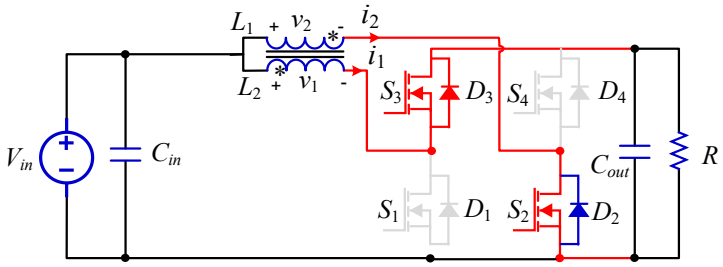
Figure 121 The topology of the two-phase interleaved converter



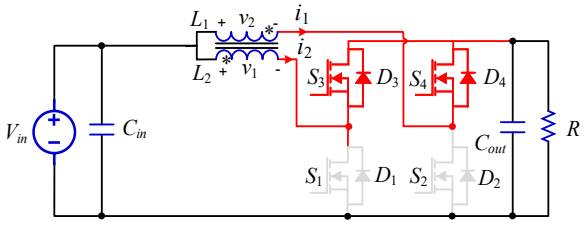
(a) Mode 1



(b) Mode 2



(c) Mode 3



(d) Mode 4

Figure 122 interleaved boost topology work mode

4.2.2 Sensorless Current Control Theory and Calculation Formulas

The interleaved boost converter works under a two-phase alternating conduction status. When the duty cycle is larger than 50%, the waveforms are as shown in Fig. 123. The system works following the Mode 1-2-3-2 path.

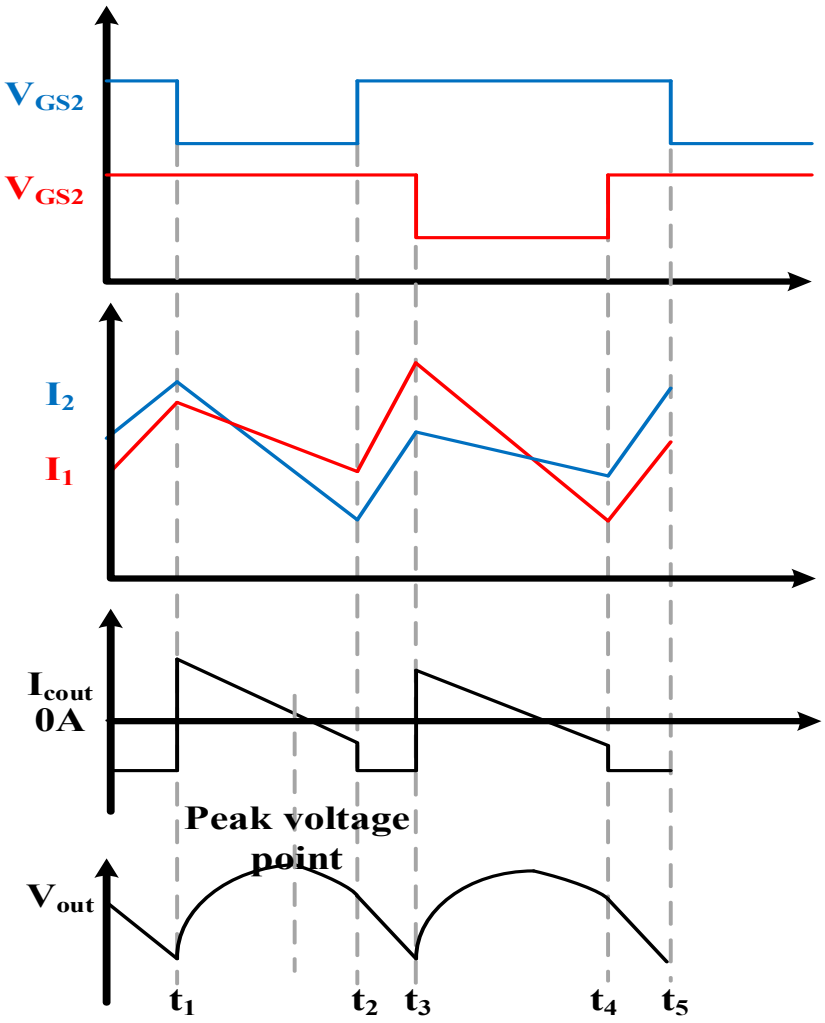


Figure 123 Imbalanced phase current caused by imbalanced phase inductance when cycle >0.5

[t1~t2] period: S1 is on and S2 is off. The circuit works under Mode 1 status.

Using Kirchhoff's voltage law (KVL) in the circuit, we attain equations 71 and 72.

$$t \in [t_1 \sim t_2]$$

$$V_{in} - L_1 \frac{d_{i1}}{dt} + M_{12} \frac{d_{i2}}{dt} = 0 \tag{71}$$

$$V_{in} + M_{21} \frac{d_{i1}}{dt} - L_2 \frac{d_{i2}}{dt} = V_{out} \tag{72}$$

$$M_{12} = kL_2 \tag{73}$$

$$M_{21} = kL_1 \tag{74}$$

Here, M is the mutual inductance, L is the self-inductance, I is the phase current, and K is the coupling coefficient of the coupled inductance.

After solving equations (71-74), we can determine the slope of the phase current as follows:

$$\frac{di_1}{dt} = \frac{V_{in} + (V_{in} - V_{out})k}{(k^2 - 1)L_1} \tag{75}$$

$$\frac{di_2}{dt} = -\frac{V_{in}k + (V_{in} - V_{out})}{(k^2 - 1)L_2} \tag{76}$$

Then we can construct the phase current equation as follows:

$$I_1(t) = I_1(t_1) + \frac{di_1}{dt} t \tag{77}$$

$$I_2(t) = I_2(t_1) + \frac{di_2}{dt}t \tag{78}$$

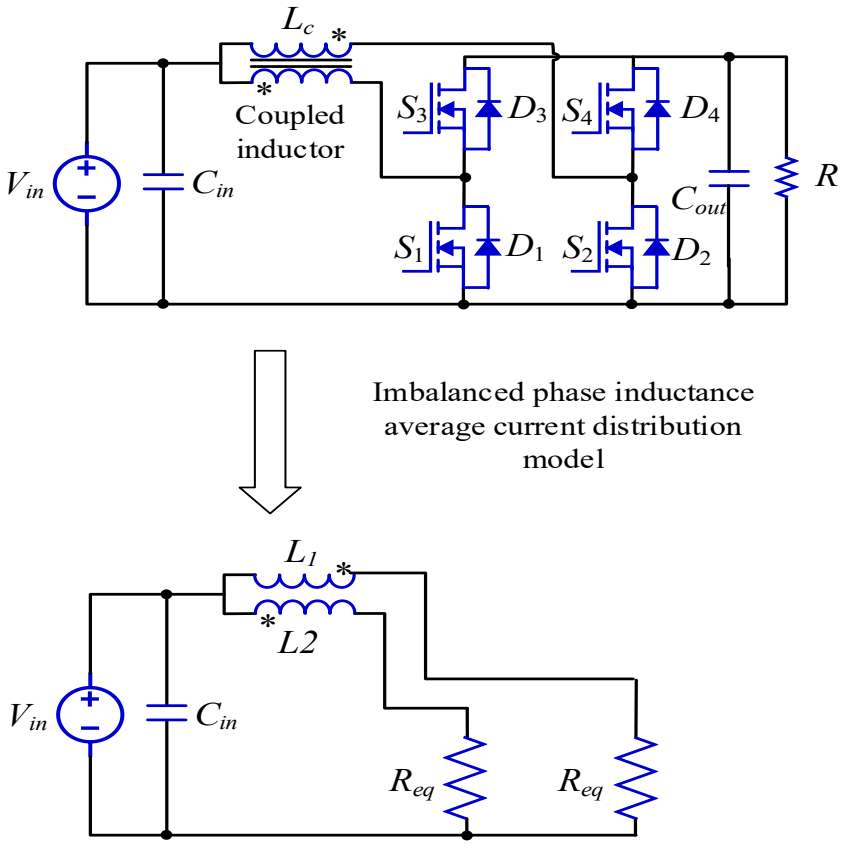


Figure 124 Imbalanced phase current distribution model circuit

The initial current (I_{t1}) is equal to the average current plus the ripple current. In the imbalanced phase inductance, the phase current distribution is in an inverse ratio to the circuit impedance, as shown in equation (79):

$$\frac{i_{1average}}{i_{2average}} = \frac{R_{eq} + 2\pi fL_2}{R_{eq} + 2\pi fL_1} \tag{79}$$

The total input current can be calculated based on the relations of the input and output power. Then the input current will be distributed based on equation (80), and we can get the initial current value in equations (80-82).

$$I_{in} = i_{1average} + i_{1average} = \frac{V_{out}^{\ 2}}{R\eta V_{in}} \tag{80}$$

$$I_1(t_1) = i_{1average} + \frac{di_2}{dt}\frac{D_2T}{2} \tag{81}$$

$$I_2(t_1) = i_{2average} + \frac{di_2}{dt}\frac{D_2T}{2} \tag{82}$$

where η is the converter efficiency.

By using Kirchhoff's current law (KCL) theory, we can find the output capacitor current value:

$$I_R = \frac{V_{out}}{R} \tag{83}$$

$$I_{cout} = I_2 - I_R \tag{84}$$

The current charge of the output capacitor will cause the output voltage to change:

$$\frac{i_{1average}}{i_{2average}} = \frac{R_{eq} + 2\pi fL_2}{R_{eq} + 2\pi fL_1} \tag{85}$$

$$U_{cout(t)} = U_{cout(t1)} + \frac{\int_0^t i_{Cout} dt}{C_{out}} \tag{86}$$

Furthermore, as the output capacitor current is a decreasing current, when the current value is zero, the output voltage reaches its peak value.

$$t_{peak} = \frac{I_2(t_1) - I_R}{d(i_2)/dt} \tag{87}$$

$$U_{outpeak} = \int_0^{t_{peak}} I_2(t_1) - I_R + \frac{di_1}{dt} t \cdot dt \tag{88}$$

$$U_{outpeak2} = \frac{2(I_2(t_1) - I_R) + (I_2(t_1) - I_R)^2}{2C_{out}[V_{in}k + (V_{in} - V_{out})]} \cdot (k^2 - 1)L_2 \tag{89}$$

[t2~t3] period: Both S1 and S2 are on. The circuit works under Mode 2. During this state, the output capacitor will provide the output current.

$$t \in [t_2 \sim t_3]$$

$$I_1(t) = I_1(t_2) + \frac{V_{in}}{L_1 - M \cdot L_2} \cdot D_1 \cdot T \tag{90}$$

$$I_2(t) = I_2(t_2) + \frac{V_{in}}{L_1 - M \cdot L_2} \cdot D_1 \cdot T \tag{91}$$

$$I_{Cout} = I_R = \frac{V_{out}}{R} \tag{92}$$

[t3~t4] period: S2 is on and S1 is off. The circuit works under Mode 3, which is similar to Mode 1 in that both work with one switch on and the other one off. Consequently, the formulas are also similar. The final equations are:

$$t \in [t_3 \sim t_4]$$

$$U_{outpeak1} = \frac{2(I_1(t_3) - I_R) + (I_1(t_3) - I_R)^2}{2C_{out}[V_{in}k + (V_{in} - V_{out})]} \cdot (k^2 - 1)L_1 \tag{93}$$

By comparing Uoutpeak1 and Uoutpeak2, we can determine the phase current balance status.

[t4~t5] period: Both S1 and S2 are on. The circuit works under Mode 2. During this state, the output capacitor will provide the current. This period is the same as the [t2~t3] period.

When the duty cycle is smaller than 50%, the circuit will follow another path, Mode 1-4-3-4. The relevant waveforms are shown in Fig. 124.

[t1~t2] and [t3~t4] period: S1 is on and S2 is off. The circuit works under Mode 1 and Mode 3, respectively.

[t2~t3] and [t4~t5] period: Both S1 and S2 are on. The circuit works under Mode 2. During this state, the output capacitor will provide the output current. The voltage ripple calculation is the same as with equations above

$$t \in [t_2 \sim t_3]$$

$$I_1(t) = I_1(t_2) + \frac{V_{in} - V_{out}}{L_1 - M \cdot L_2} \cdot D_1 \cdot T \tag{94}$$

$$I_2(t) = I_2(t_2) + \frac{V_{in} - V_{out}}{L_1 - M \cdot L_2} \cdot D_1 \cdot T \tag{95}$$

$$I_{Cout} = I_R = \frac{V_{out}}{R} \tag{96}$$

Based on the above calculation equations, when one phase inductance is smaller than another phase, both the phase average current and the ripple current will be different due to imbalanced phase inductance. A lower inductance will result in a higher current ripple value. The higher current ripple value will increase the initial capacitor current in the circuit. It can be seen in Fig. 126 when the phase one inductance is smaller than phase two. The phase one current ripple and average current are larger than phase current I2. The two-phase current flows into the output capacitor alternatingly. The imbalanced phase current will result in an output voltage ripple difference.

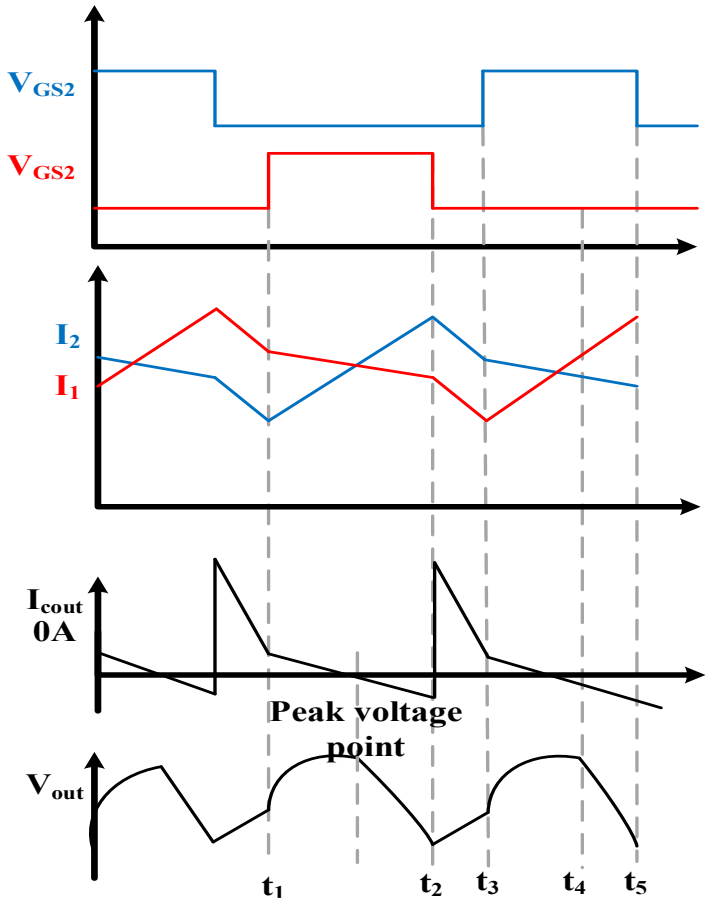


Figure 125 Imbalanced phase current caused by imbalanced phase

The causes of imbalanced phase current are imbalanced phase and imbalanced phase duty cycles. In imbalanced phase duty cycle conditions, the two phases' inductance is set to equivalent; therefore, the current ripple in each phase is the same but the imbalanced phase duty cycles will bring the phase average current into imbalance. The current distribution will be decided by the phase duty cycle, as shown in equations (97–98):

$$\frac{i_{1average}}{i_{2average}} = \frac{1 - D_2}{1 - D_1} \tag{97}$$

$$I_{in} = i_{1average} + i_{1average} = \frac{V_{out}^{\ 2}}{R\eta V_{in}} \tag{98}$$

In the figure, the phase 1 gate drive signal is smaller than the phase 2 gate drive signal. The lower duty cycle will result in a lower average current value. The lower average value will also result in a lower initial current value of the output capacitor. This will also result in a lower output voltage ripple peak value. The current and voltage waveforms in a period are shown in Figs. 126–127. Figure 126 shows the imbalanced current caused by an imbalanced duty cycle when the duty cycle is larger than 50%. Figure 127 is the waveform for the duty cycle smaller than 50% condition. The voltage ripple peak value calculation equations are shown in equations (99–100).

$$U_{outpeak1} = \frac{2(I_1(t_3) - I_R) + (I_1(t_3) - I_R)^2}{2C_{out}[V_{in}k + (V_{in} - V_{out})]} \cdot (k^2 - 1)L_1 \tag{99}$$

$$U_{outpeak2} = \frac{2(I_2(t_1) - I_R) + (I_2(t_1) - I_R)^2}{2C_{out}[V_{in}k + (V_{in} - V_{out})]} \cdot (k^2 - 1)L_2 \tag{100}$$

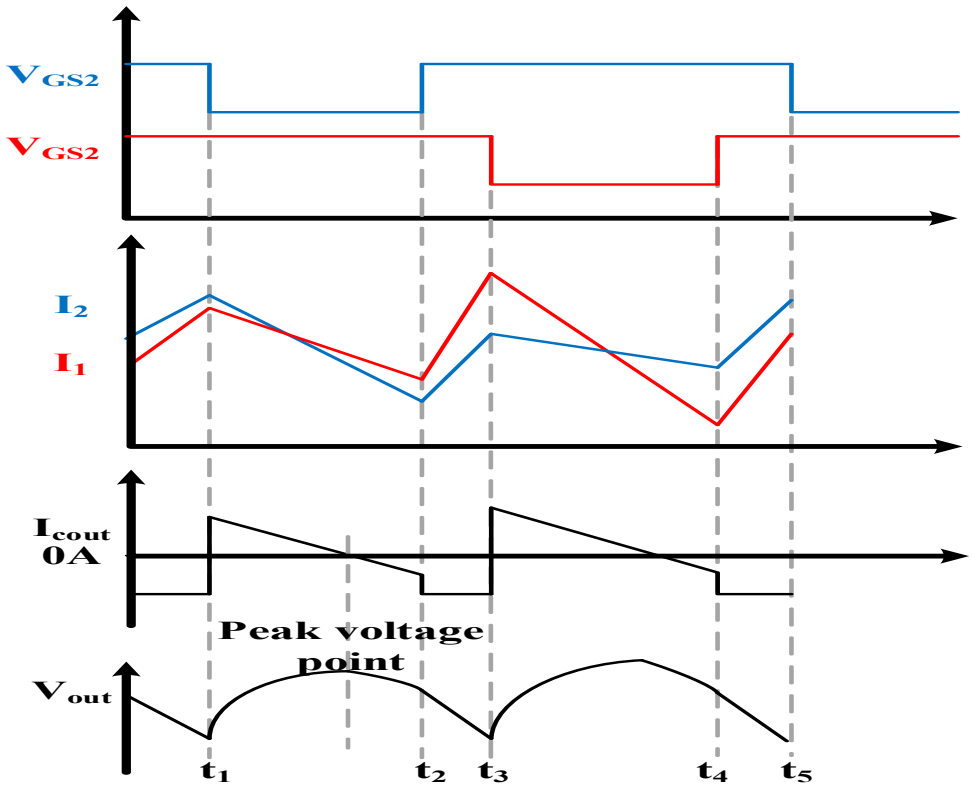


Figure 126 Imbalanced phase current caused by imbalanced phase duty

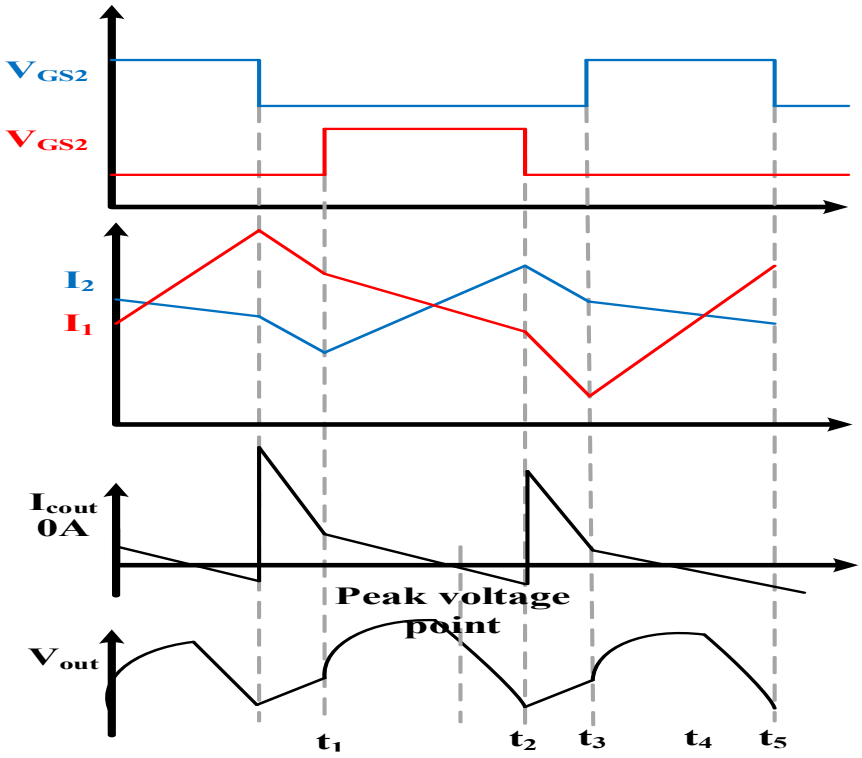


Figure 127 Imbalanced phase current caused by imbalanced phase when duty cycle <0.5

Based on the imbalanced current calculation equation, a MATLAB coding program has been created to verify the voltage ripple difference in the 5–30V input voltage range, as shown in Figs. 128–129.

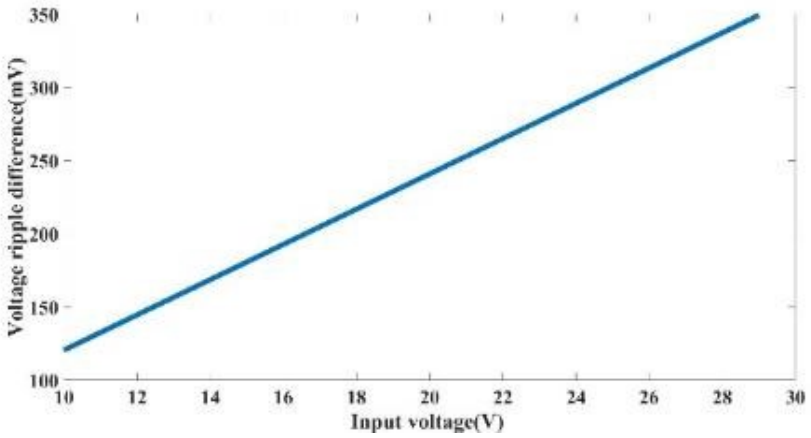


Figure 128 Voltage ripple difference caused by imbalanced phase

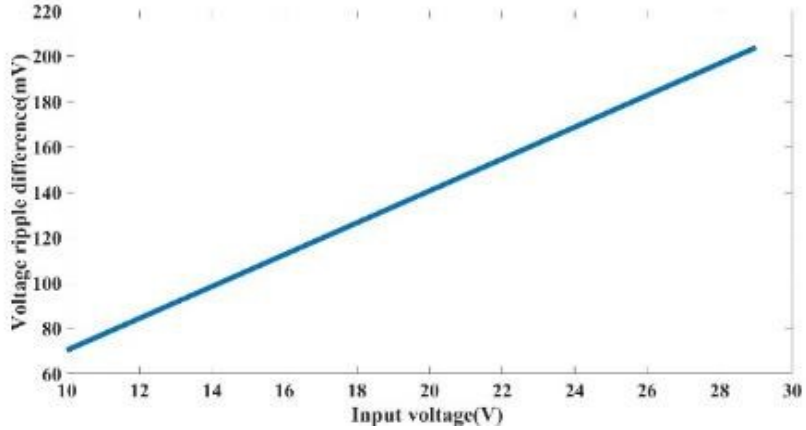


Figure 129 Voltage ripple difference caused by imbalanced phase duty

4.2.3 The Proposed Sensorless Control Method

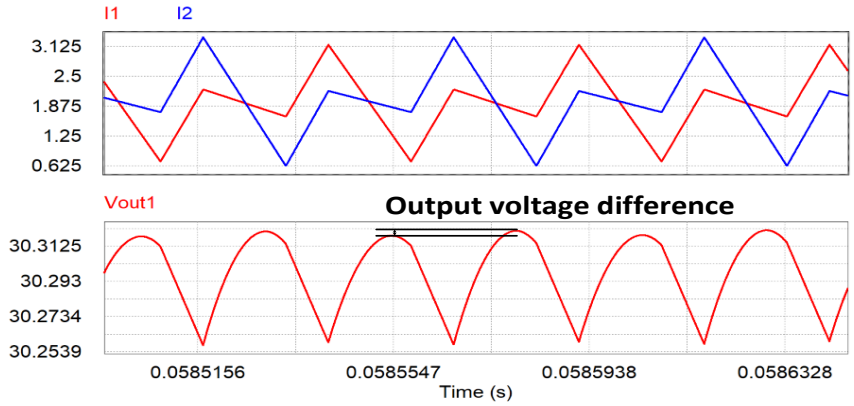
Based on the above interleaved boost converter topology and operation principle, a two-phase interleaved boost converter model has been built in PSIM to investigate the relationship between the phase current status and the output voltage ripple. The imbalanced current mainly

stems from two points: (1) unequal phase inductance values and (2) unequal driver signal duty cycles. The imbalanced current then leads to a difference in the output voltage ripple value.

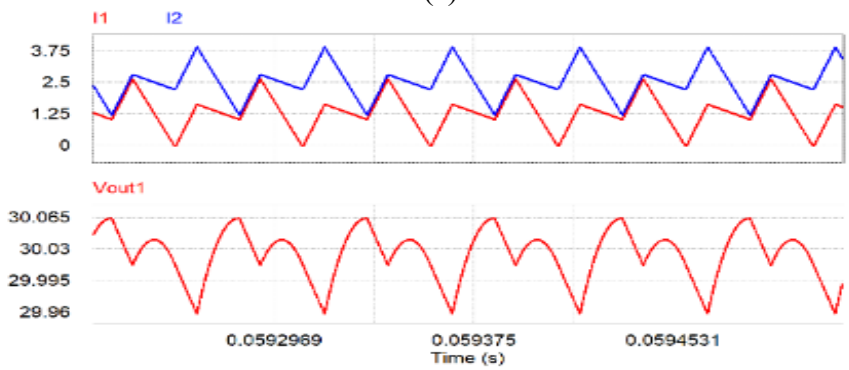
As for the duty cycle >0.5 condition, the output voltages given an imbalanced phase inductor, unequal duty cycle, or balanced phase current status are shown in Fig. 130 (a), (b), and (c), respectively. According to the output voltage ripple waveform, the output voltage is composed of a periodic sinusoidal ripple. When the phase current is balanced, each voltage ripple waveform is almost the same; however, when the phase current is imbalanced, there is a voltage value difference in the periodic voltage ripple. As for the duty cycle <0.5 condition, the output voltages given an imbalanced phase inductor, unequal duty cycle, or balanced phase current status are shown in Figs. 130 (a), (b), and (c), respectively. According to the three statuses' waveforms, the difference is the number of minimum points in a time period. Under the balanced status, there are two minimum points in a time period, as shown in Fig. 130 (c). Under the imbalanced status, there is only one minimum point in a time period, as shown in Figs. 131 (a) and (b).

From Fig. 130 (a), there is a difference in the periodic voltage peak value when the two-phase current is imbalanced. This difference is because two-phase current alternatingly flows into the output side. The equation for calculating the output voltage according to the phase current is derived from above equations The overall system control diagram is shown in Fig. 130. The output voltage is sampled by an analog to digital converter (ADC) to convert the output voltage into digital data. Then a voltage spike filter is applied to block any voltage spikes or noise. At this point, the system compares the voltage ripple peak value to diagnose the phase current status. If the phase current is imbalanced, the system will adjust the duty cycle of the

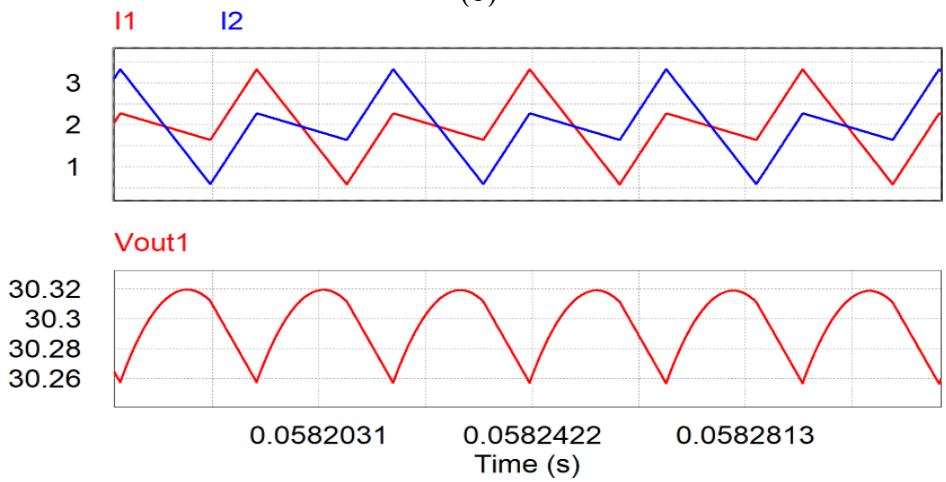
driver signal until the phase current reaches a balanced status. The current adjustment process simulation waveform is shown in Fig. 131



(a)

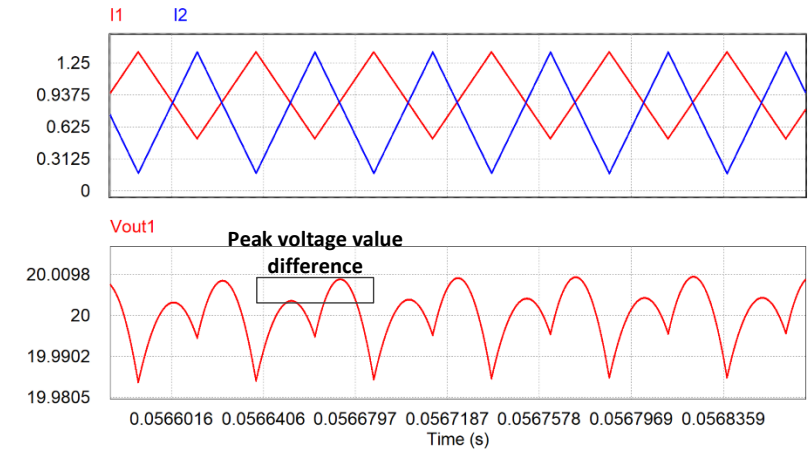


(b)

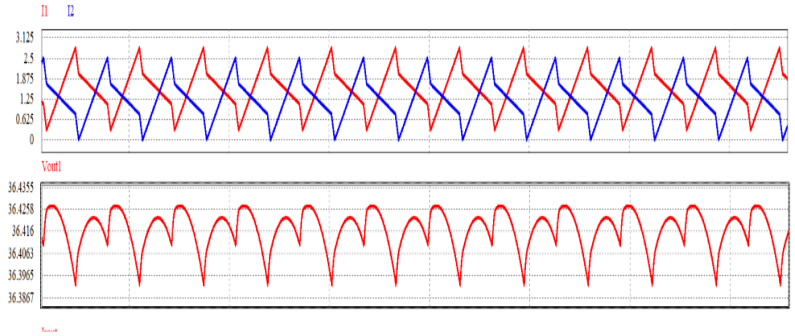


(c)

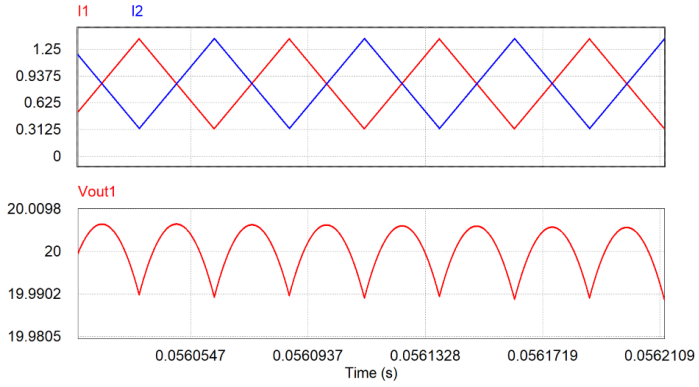
Figure 130 Phase current and output voltage waveforms when D>0.5 under the conditions of: (a) imbalanced phase inductor, (b) imbalanced duty cycle, (c) balanced phase current



(a)



(b)



(c)

Figure 131 Phase current and output voltage waveforms when D ≤0.5 under the conditions of: (a) imbalanced phase inductor, (b) imbalanced duty cycle, (c) balanced phase current

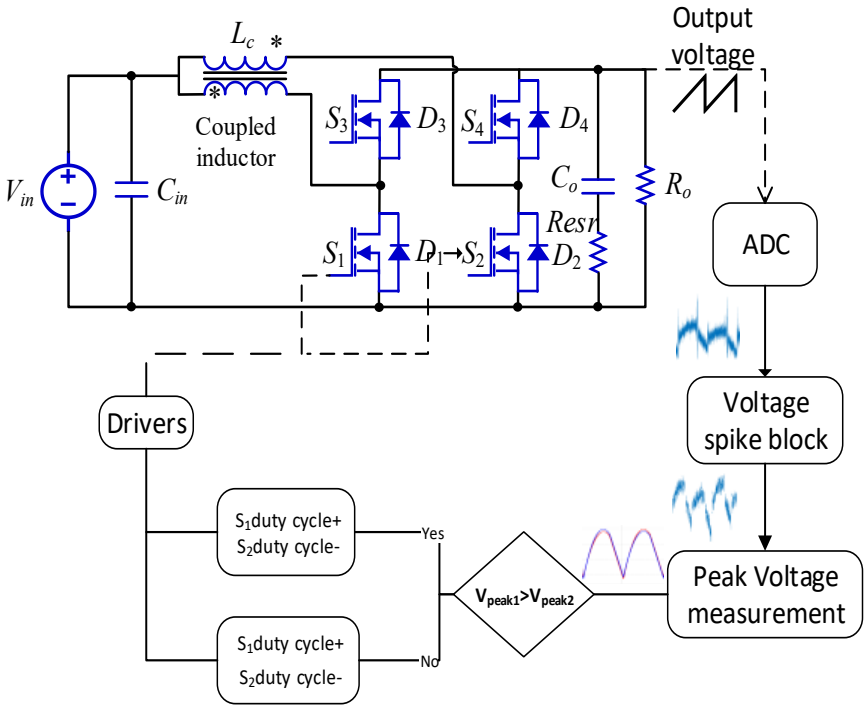


Figure 132 Overall sensorless current balanced closed-loop control diagram

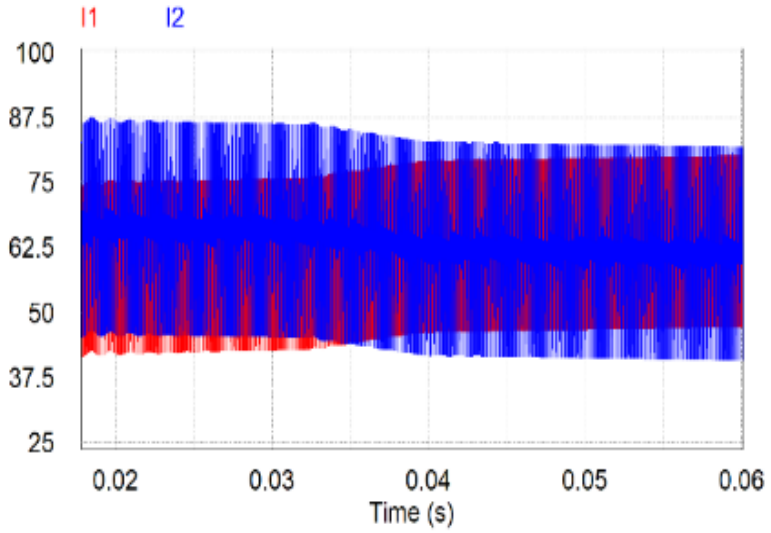


Figure 133 Current balance adjustment process simulation result

4.2.4 Experiment Test Bench and Results

Based on the above principle, a two-phase interleaved boost converter test bench has been set up, as shown in Fig. 134. Table 11 shows the key parameters of the components implemented in our prototype.

Table 11 The test bench components' parameters

Components	Parameter values
Inductor self-value	144 uH
Inductor mutual-value	96.4 uH
Input capacitor	100 uF
Output capacitor	75 uF
SiC MOSFET	BSM400D12P3G002

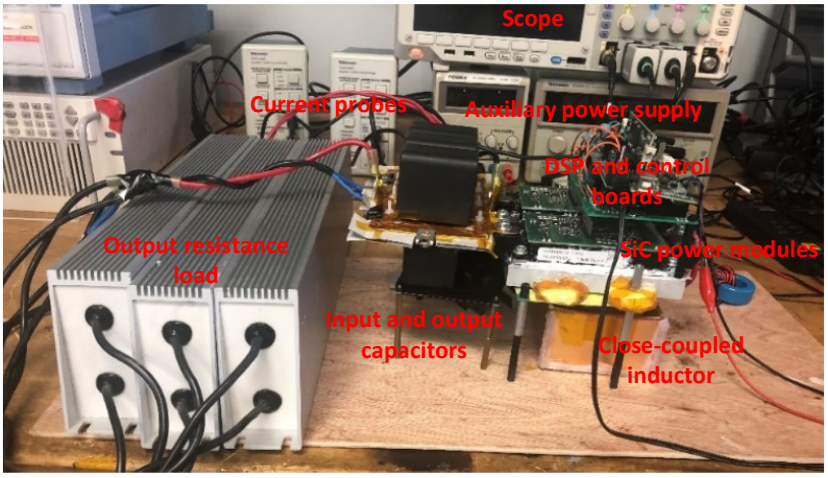


Figure 134 The experiment test bench

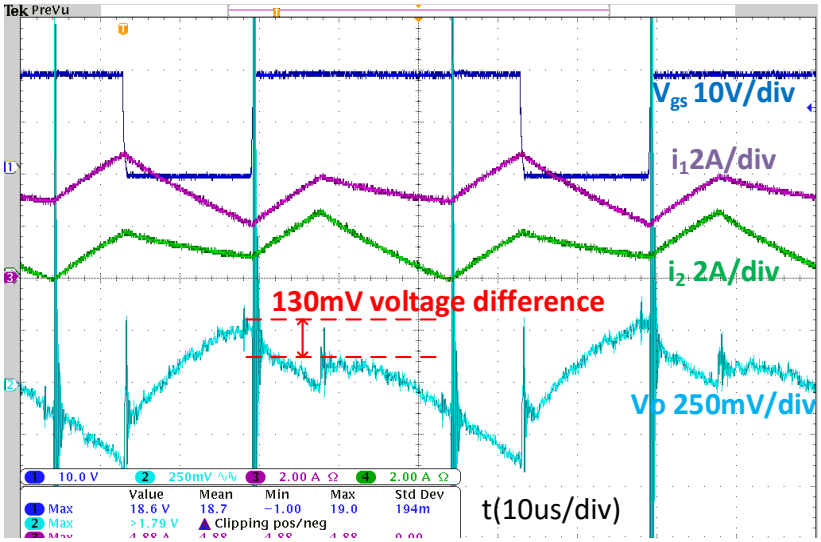


Figure 135 Output voltage waveforms under the condition of an imbalanced phase inductance

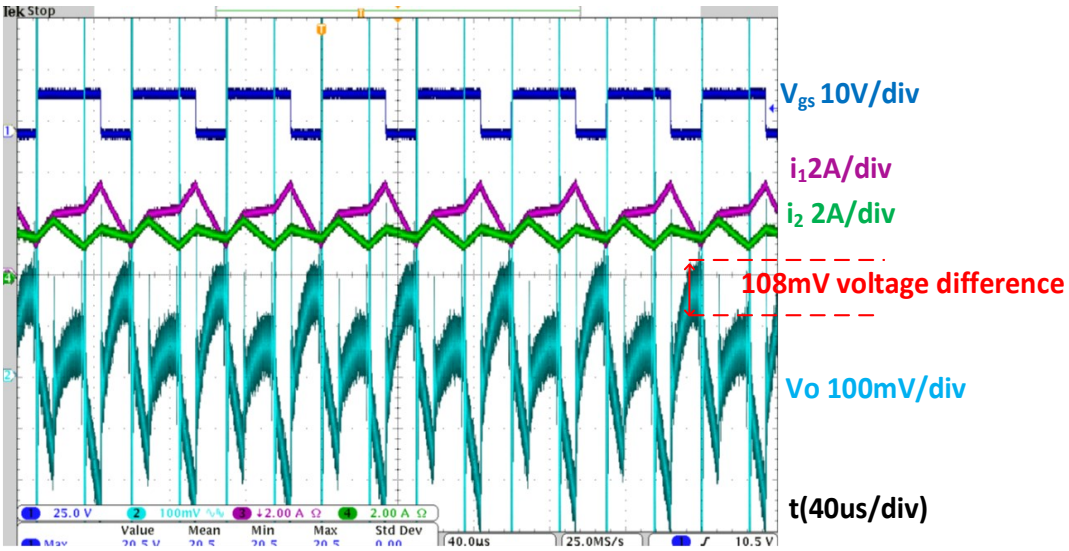


Figure 136 Output voltage waveforms under the condition of an imbalanced duty cycle

The experimental waveforms under imbalanced duty cycle and phase inductance conditions are shown in Figs. 135 and 136, respectively. In these two figures, the blue line is the gate-to-source drive signal vgs, and the purple and green lines are the two phases' currents, i1 and i2, respectively. From Fig. 136, it can be observed that the output voltage difference reaches 130 mV given different duty cycles, equaling 0.667 and 0.66. Moreover, the output voltage difference is 108 mV when the two-phase inductance difference is 10 uH.

Due the voltage ripple composing only 0.1 percent of the output voltage, in order to fully utilize the ADC voltage range, a high-pass filter is applied to the output voltage to eliminate the DC voltage of the output voltage. Then the AC ripple voltage will be changed to the 0–3.3V voltage range. The ripple voltage can be sampled by the DSP ADC voltage sensor. The voltage sensor loop is shown in Fig. 137. The voltage waveform comparison between the proposed high-pass filter output and the scope-measured AC voltage is shown in Fig. 138. The high-pass filter maintains the voltage ripple accuracy. The proposed method only needs compare the voltage ripple peak value difference. So, the potential time delay or peak value attenuation will not influence the peak value comparison result.

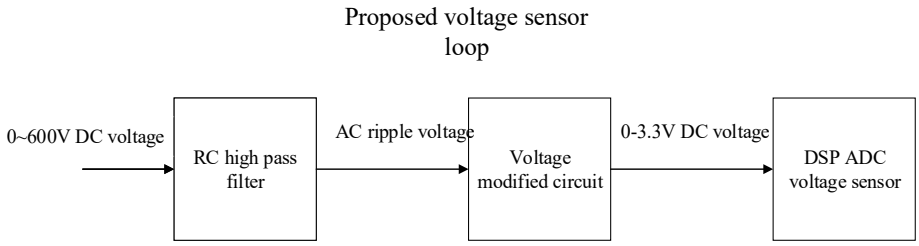


Figure 137 Proposed voltage sensor loop

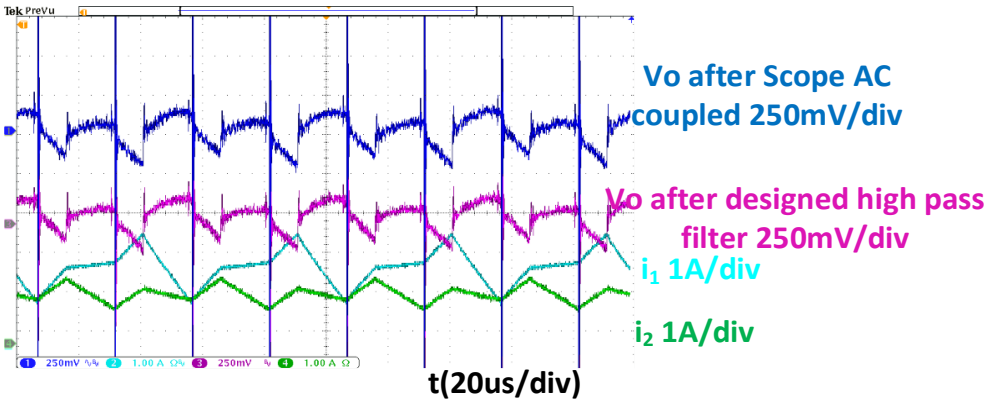


Figure 138 Proposed voltage sensor output waveforms

From Figs. 139 and 140, the switching process of the MOSFET introduces voltage spikes into the output voltage. These voltage spikes influence the judging of the maximum output voltage ripple. If the controller cannot sample the ripple voltage correctly, a balanced phase status cannot be attained. So, a spike filter needs to be applied to the output voltage waveform. The filter calculates the slope of each output voltage point, and points with a significantly higher slope value are treated as spike points. Filtering out the spikes in this way can improve the accuracy of our phase current diagnosis system. Then the controller will split a whole period into two half periods. Each half time period's voltage ripple value is respectively decided by the phase current value. Comparing the maximum values of the two half time periods' voltage ripple, the controller can diagnose the current's imbalanced status and adjust the phase duty cycle to reach a balanced status. The filtered output voltage waveforms of Figs. 141 and 142 are shown in Figs. 139 and 140, respectively.

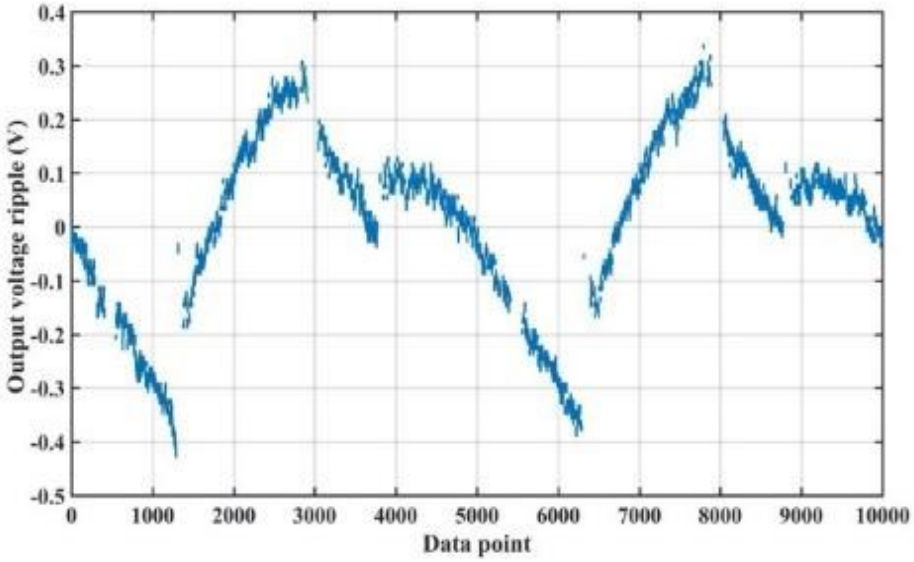


Figure 139 Filtered output voltage waveform under the condition of an imbalanced duty cycle

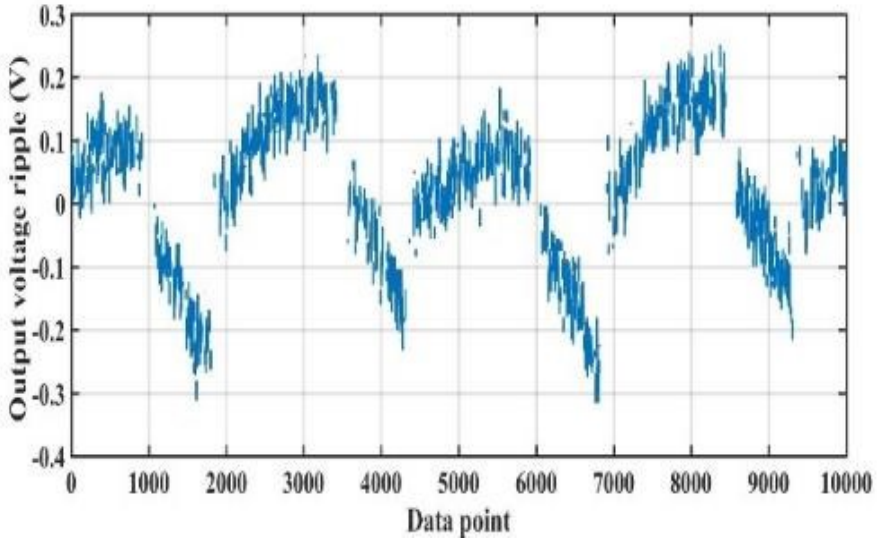


Figure 140 Filtered output voltage waveform under the condition of an imbalanced phase inductance when duty cycle is 66%

The phase current online adjustment process is shown in Fig. 141. In this figure, the purple line and the green line represent two phase currents, i1 and i2, respectively. By changing the duty cycle of each phase, the imbalanced phase current can be suppressed and eventually balanced. Fig. 142 shows the output voltage waveform when balanced. Each voltage ripple is the same under the balanced status.

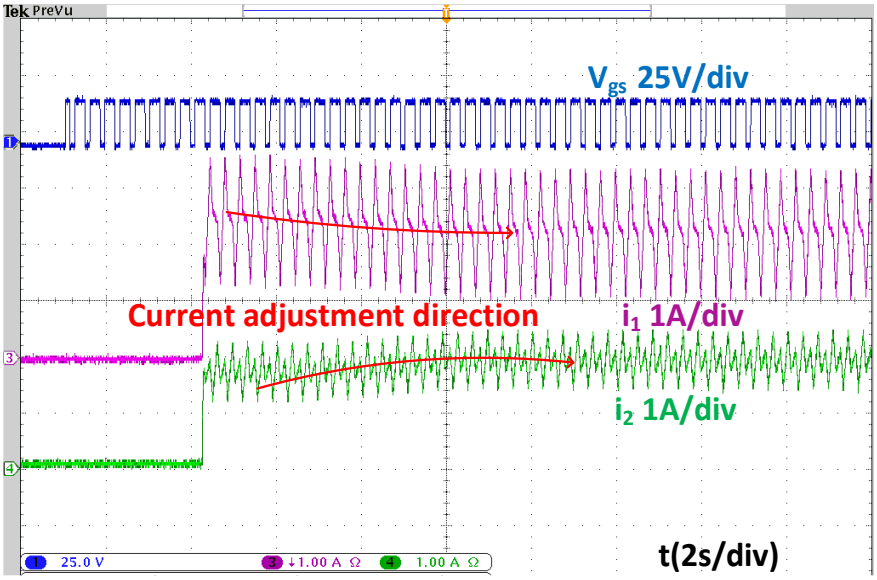


Figure 141 Dynamic adjustment process of the two-phase currents i1 and i2

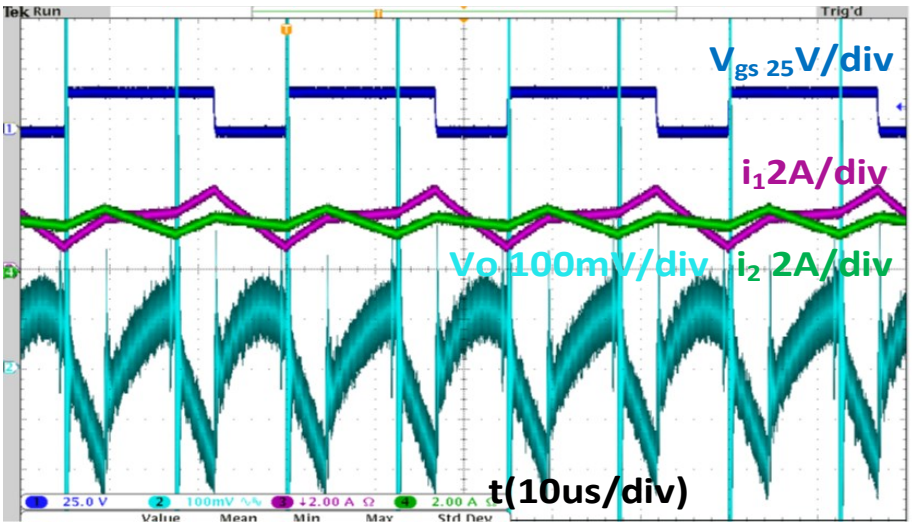
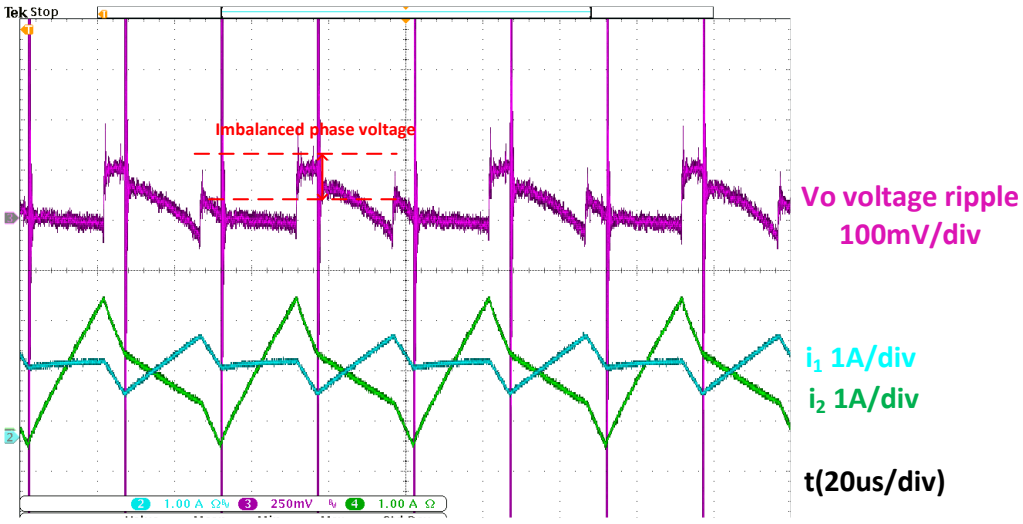


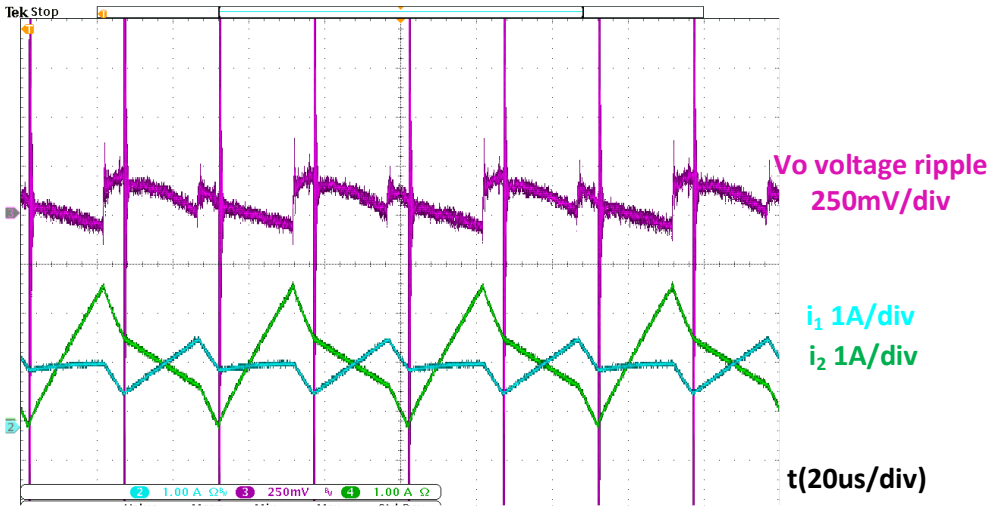
Figure 142 The output voltage ripple waveform under the balanced status when duty cycle >50%

The proposed sensorless current algorithm is also verified in other working conditions. Based on the above classifications, the imbalanced current status can be classified into 4 modes: (1) imbalanced phase inductance when the duty cycle is larger than 50%, (2) imbalanced phase inductance when the duty cycle is smaller than 50%, (3) imbalanced phase duty cycle when the duty cycle is larger than 50%, and (4) imbalanced phase duty cycle when the duty cycle is

smaller than 50%. The experimental waveform under mode 1 is shown in the Fig. 143-144. The experimental waveforms for mode 2, 3 and 4 are shown in Fig. 143-145 respectively.

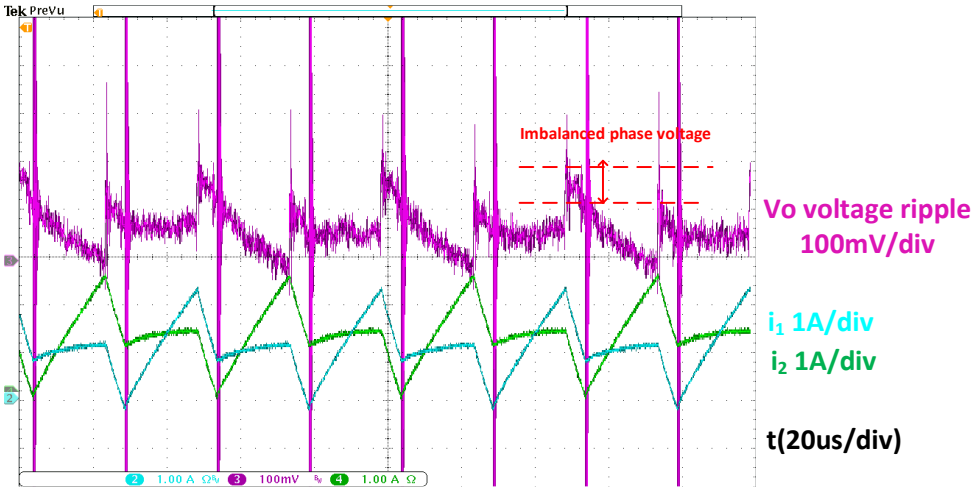


(a)

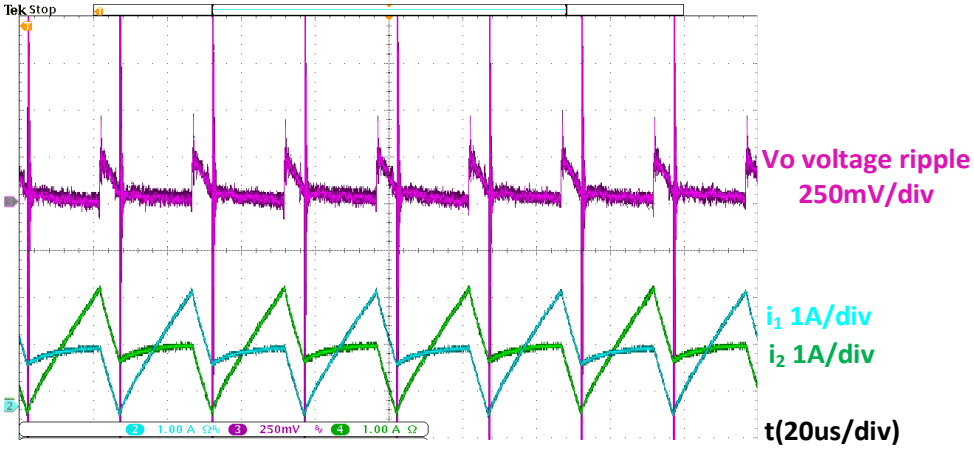


(b)

Figure 143 Imbalanced phase inductance output voltage waveforms when the duty cycle is smaller than 50%: (a) imbalanced current status, (b) balanced current status

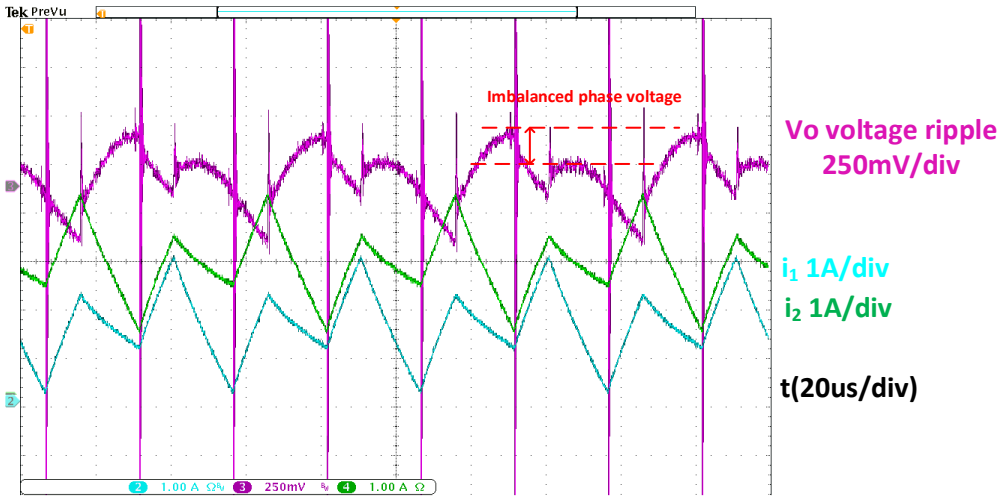


(a)

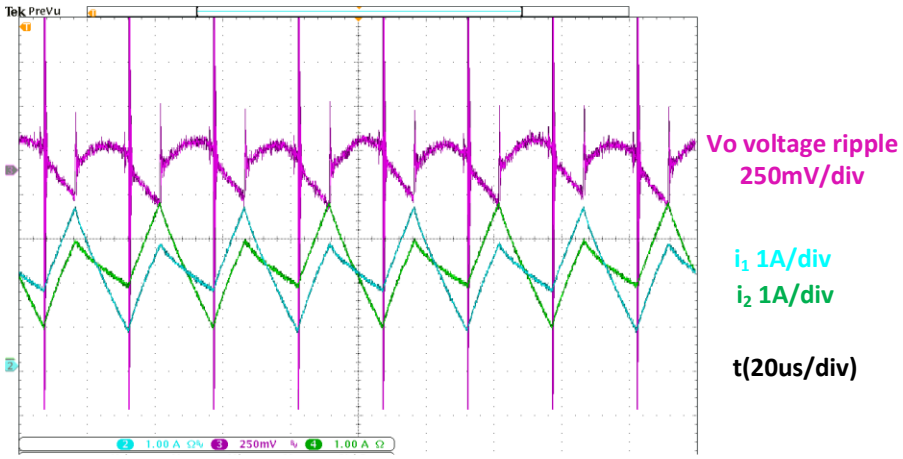


(b)

Figure 144 Imbalanced phase duty cycle output voltage waveforms when the duty cycle is smaller than 50%: (a) imbalanced current status, (b) balanced current status



(a)



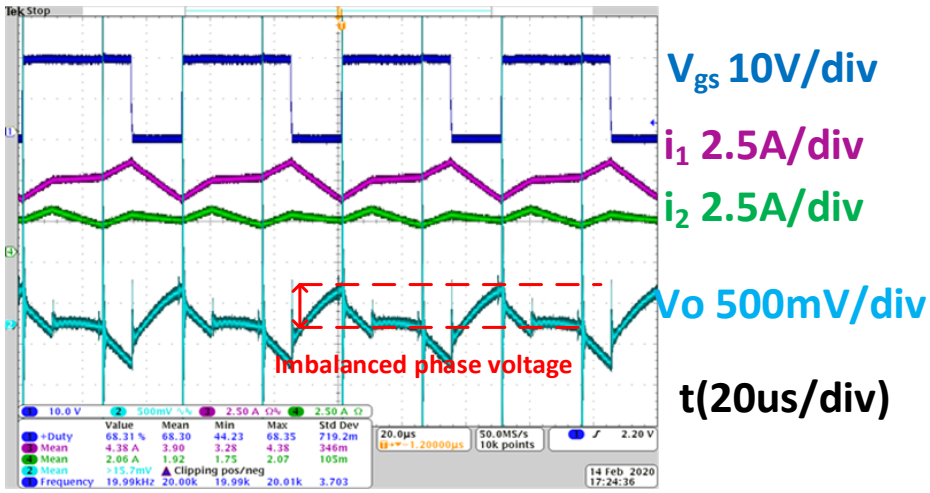
(b)

Figure 145 Imbalanced phase duty cycle output voltage waveforms when the duty cycle is larger than 50%: (a) imbalanced current status, (b) balanced current status

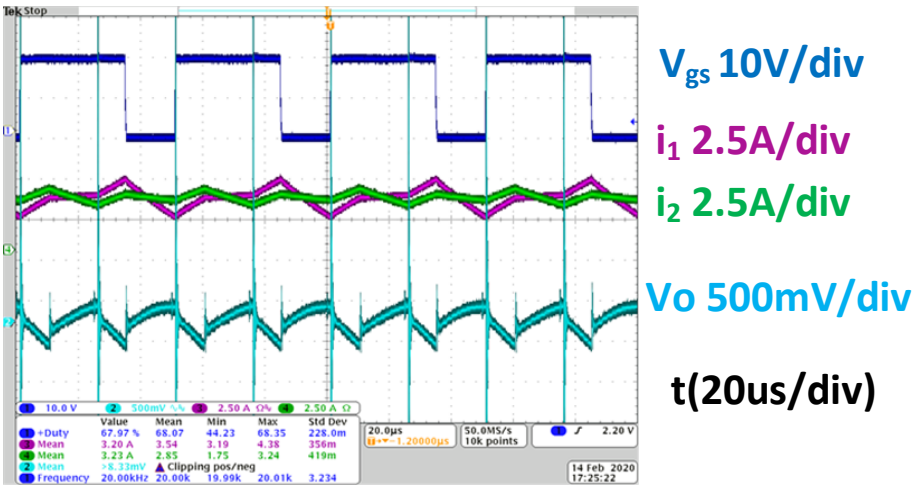
The experimental results well verified the theoretical analysis on the imbalanced phase current. If there is a phase current difference, the peak value of the output voltage ripple will reflect the imbalanced status. The system could diagnose the phase current distribution status by comparing the periodic peak value of the output voltage ripple.

Furthermore, the proposed sensorless current balancing method is also verified under different load, voltage, and input voltage conditions. Fig.146 shows imbalanced and balanced

waveforms under a 10 V input voltage, 20 kHz switching frequency, and 17 ohm resistance load condition Fig.147 shows the imbalanced and balanced current waveforms under a 10 V input, 30 kHz switching frequency, and 24.5 ohm resistance load condition. Fig.148 shows the imbalanced and balanced current waveforms under a 15 V input voltage, 20 kHz switching frequency, and 24.5ohm resistance load condition.

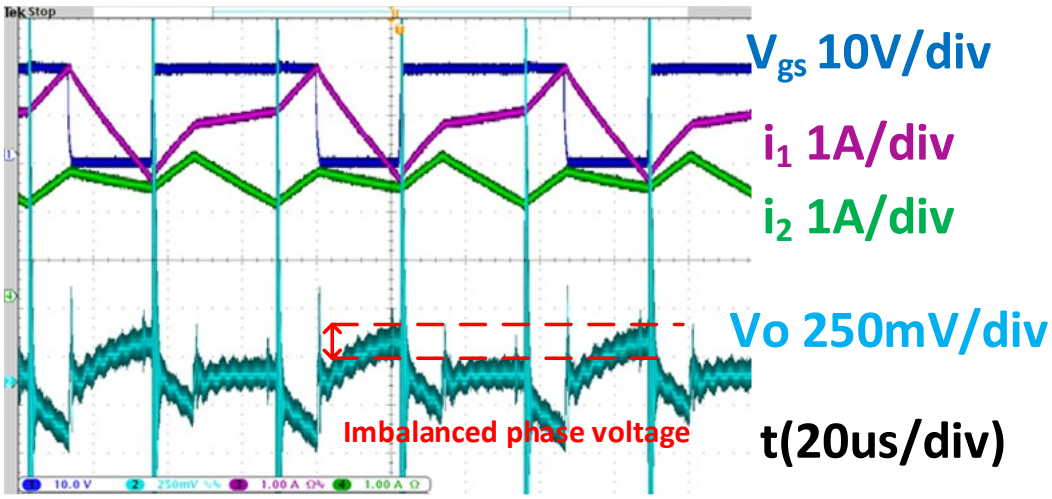


(a)

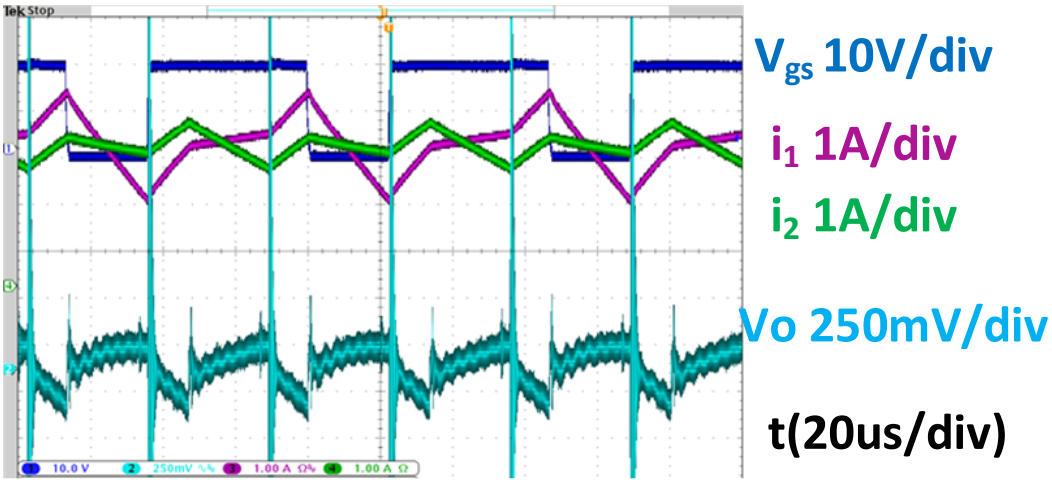


(b)

Figure 146 Output voltage waveforms under a 17ohm working condition: (a) imbalanced current status, (b) balanced current status

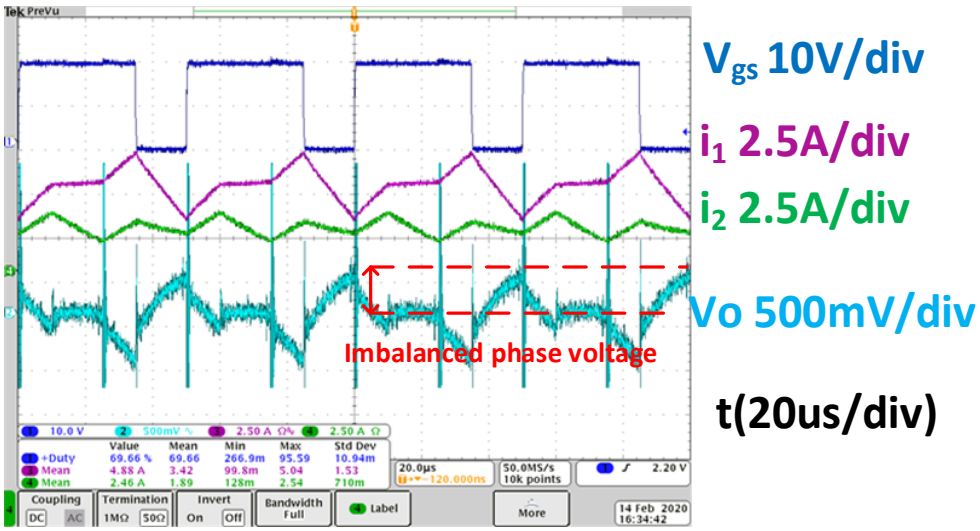


(a)

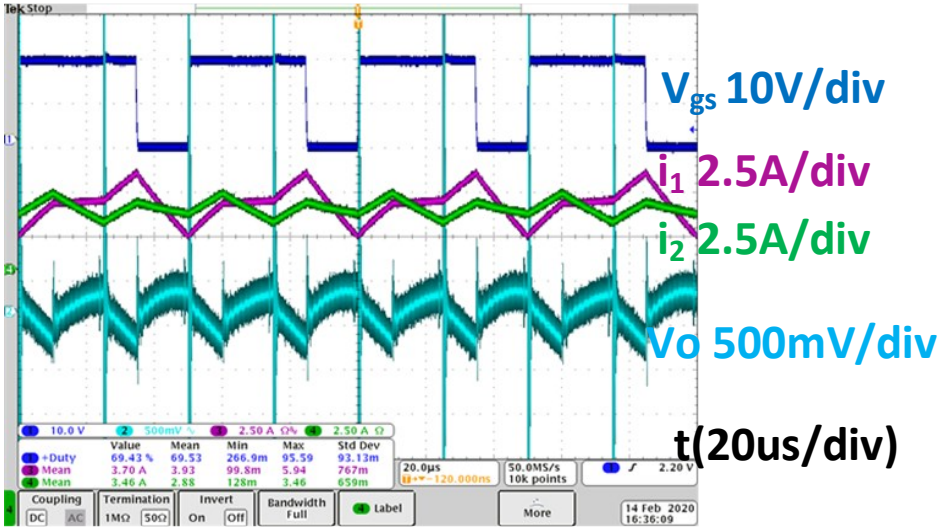


(b)

Figure 147 Output voltage waveforms under a 30 kHz switching frequency working condition: (a) imbalanced current status, (b) balanced current status



(a)



(b)

Figure 148 Output voltage waveforms under a 15 V input voltage working condition: (a) imbalanced current status, (b) balanced current status

From the experimental results, when the phase current is imbalanced, the voltage ripple peak value difference can be captured in all the test conditions. By adjusting the phase duty cycle, the phase current can realize a balanced status. In a phase inductance imbalanced condition, each phase average current can reach balanced status by adjusting the phase duty cycle, but the ripple current cannot be the same due to the inductance difference. In the phase

duty cycle imbalanced condition, both the average current and the ripple current can be made the same by adjusting the phase duty cycle.

4.2.5 Conclusions

This part describes a novel sensorless current control method for an interleaved boost converter. The proposed method realizes phase current balance by sampling the period output voltage ripple. The reasons for phase current imbalance can be classified into two main points: imbalanced phase inductance and unequal duty cycle. Hence, formulas that capture the relationship between the phase current status and the periodic output voltage ripple are derived. Instead of inserting a current sensor into the power loop, this method diagnoses the phase current distribution using the output voltage and adjusts the duty cycle to realize two-phase current balance. Eliminating the power loop current sensor can reduce design complexity and total system cost. The experimental results verify the feasibility of the proposed sensorless current control method.

Chapter 5 T-Type Traction Inverter Design

5.1 Introduction

As the increasing focus on the electrical vehicle and renewable energy. How to improve the electrical system efficiency and performance is a hot topic in power electronics research area .The traditional two-level inverter is still the main topology of current traction inverter topology. However, as the development of advanced inverter topology, 800V application become necessary for the traction inverter due to its lower current stress and higher efficiency. Both industry and academia has become to focus on the new topologies to solve the two-level inverter issue. The traditional level only has three output voltage level to modulate the output sin AC waveform as shown in figure.149. Compared to the tradition inverter topology, T-type inverter has five output voltage levels, so five output voltage levels could better modulate output AC waveform.

With the increasing power level of traction inverter, A higher efficiency and better performance topologies is essential for the high-power application. [175-181] focus on the control optimization of the T-type inverter. [175-177] reduce the power loss by applying another modulation control method.[178-179] reduce the voltage and current stress by modifying the topology of the T-type inverter. [180] proposed a new soft switching technology for the T-type inverter [181] focus on the balance control of the possible imbalanced neutral point voltage.The new wide band devices SiC and GaN is famous for their lower power loss and higher switching frequency. A lower power loss could help improve the inverter efficiency a lot [182-189].[182-184] build a full SiC T-type inverter to get a higher efficiency at a higher switching frequency.

[184-186] focus on the SiC and Si hybrid configuration. [187-189] summarize the benefit and switching characterization of the SiC application in T-type inverter In my research, A T-type inverter with GaN and IGBT are investigated. Meanwhile a hybrid control mode is proposed to optimization the overall system efficiency and save the cost of GaN.

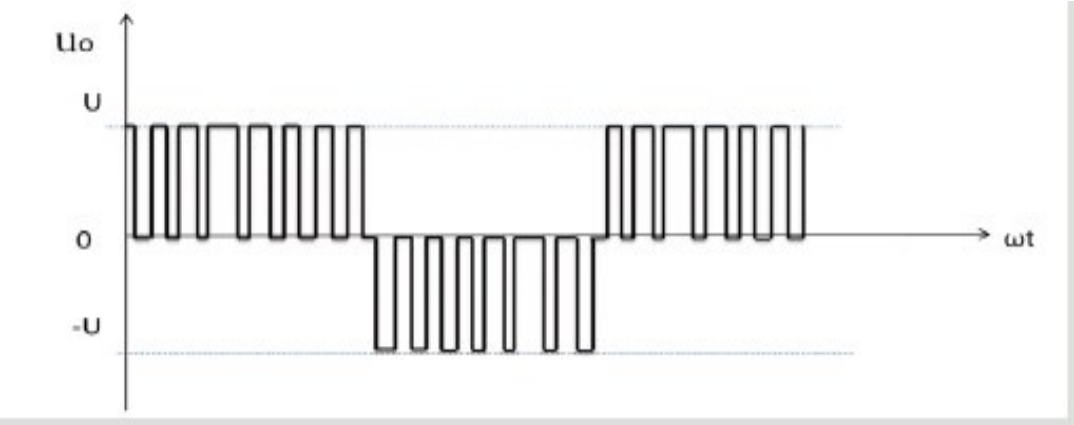


Figure 149 two level inverter output voltage level

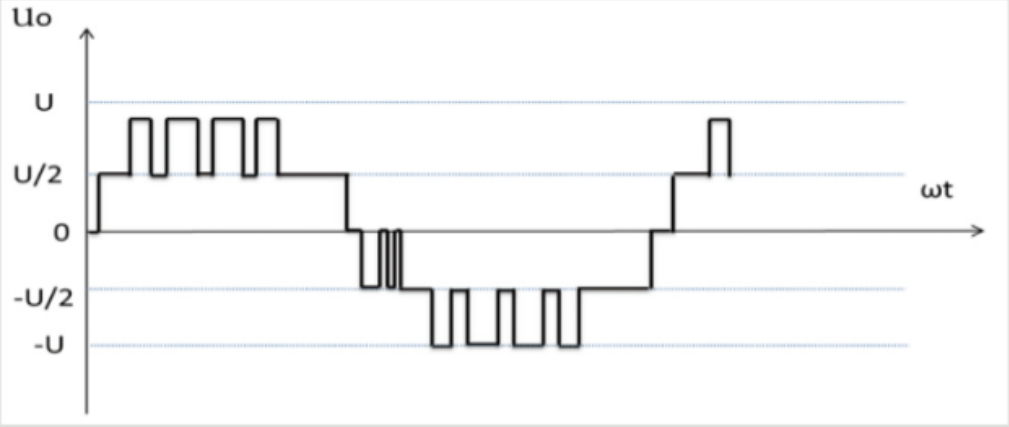


Figure 150 T-type inverter five output voltage levels

The T-type inverter work mode is shown in figure 151

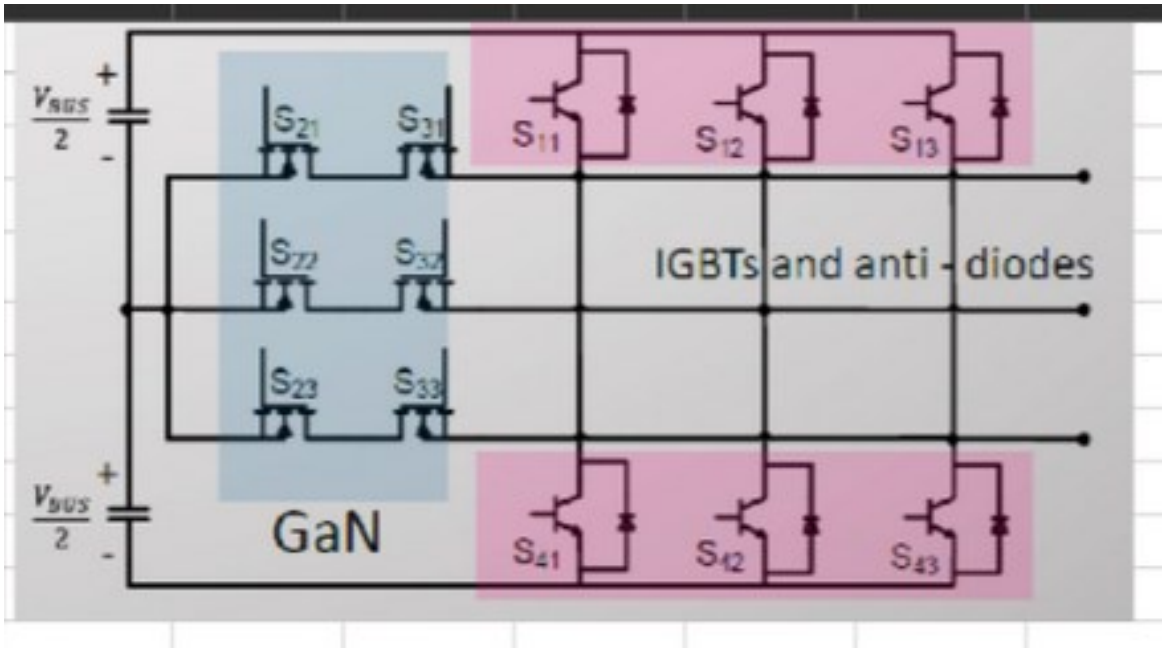


Figure 151 T-type inverter topology with GaN

5.2 The GaN Application in the T-Type Inverter

The topology of proposed T-type inverter with GaN application is shown in figure.151. The IGBT is used for the three-phase leg to undertake main current. The GaN is used in the mid bridge to realize soft switching.

(a) (b)

Figure 152 IGBT and GaN power MOSFET

FS450R12OE4 is selected as the IGBT power modules of the T-type inverter. It is a 1200V 450A three phase leg power module. IGBT power module will be used to undertake the high current load. GS-065-060-3-T is selected as the GaN power MOSFETS applied in the mid bridge. IGBT and GaN MOSFET is shown in the following table. The GaN has a much smaller switching loss compared to the IGBT. While IGBT has a much smaller condition loss due to a smaller Rdson. So let GaN undertake switching loss and IGBT undertake conduction loss could be higher efficiency way to realize a higher overall system efficiency.

Table 12 IGBT and MOSFET parameters

	FS450R12OE4	GS-065-060-3-T
V_{rate}	1200V	650V
I_C	650A	60A
V_f	1.65V	7V
R_{dson}	5mohm	25mhom
Eon	25mJ(600V450A 25C)	0.117mJ(400V 20A 25C)
Eoff	37mJ	0.017mJ
Ton/Toff	250ns/500ns	16ns/18ns

The work condition of the T-type inverter is shown in following figure. It can be seen that from b to c. when the top switching is off. The GaN will undertake the current in the dead band time. Then the Io will charge the Coss of the bottom IGBT to realize soft switching on to eliminate the turn on loss.

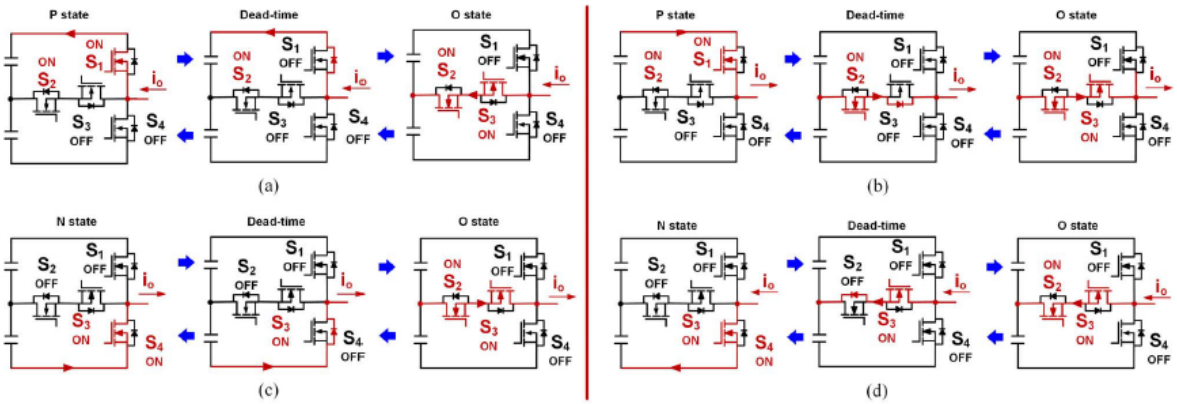


Figure 153 T-type inverter switching process

The power loss of the power stage can be classified as conduction loss, switching loss, or dead band loss.

The conduction loss equation is:

$$P_{cond} = I^2_{rms} R_{\text{dson}} \tag{101}$$

Here, I_{rms} is the RMS value of the MOSFET current. R_{dson} is the conduction resistance of the MOSFET.

The switching loss equation is:

$$P_{Switch} = f_s (E_{on} + E_{off}) \frac{U}{U_{ref}} \frac{I}{I_{ref}} \tag{102}$$

Here, E_{on} and E_{off} are the energy MOSFET turn on and turn off energy. U_{ref} is the reference voltage. I_{ref} is the reference current. U and I are the operation current and voltage of the MOSFET, respectively.

The dead band loss equation is:

$$P_{\text{dead}band} = V_{diobe} I f_s t_{deadband} \tag{103}$$

So the total overall system loss is:

$$P_{Total} = P_{core} + P_{conduction} + P_{switch} + P_{deadband} \tag{104}$$

In high or full load working conditions, T-type inverter will disable all the GaN Power MOSFETS. Inverter will work in typical three phase inverter mode. In high load working condition, Inverter will work in a lower switching frequency (20kHz) to reduce power loss. By applying proposed hybrid work mode, A much lower current rating GaN can be applied in the T-type inverter.

The surface mount GaN is selected as the power MOSFETs. The Gan System GS-065-060-3-T is a 650V 60A surface mount GaN power MOSFET. It has higher power density than typical TO-247 package. The three-phase leg layout is shown in the following figure.

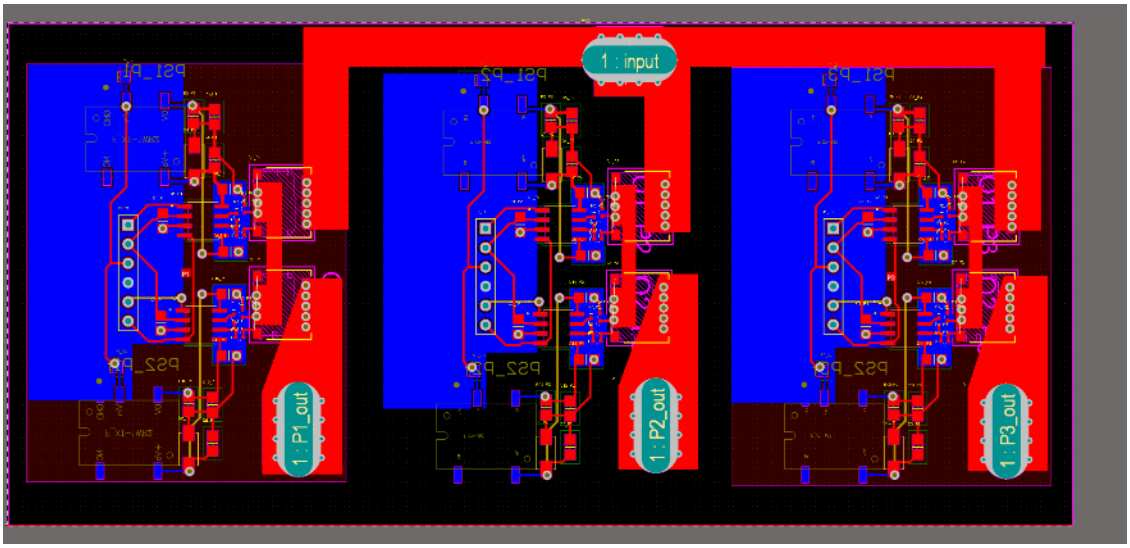


Figure 154 GaN Three phase layout PCB

5.3 Proposed Hybrid Control Method

Based on the load conditions of the traction inverter in a typical mission as shown in figure. It can be seen that in most of case, traction inverter work at a low work mode condition.

Modes	City	Highway	Top speed	Accelera -ting	Regenera -tion
Percentage of time	45%	40%	10%	5%	Braking
Load	10%	20%	7%	100%	30%

Figure 155 EV traction inverter work mode distribution

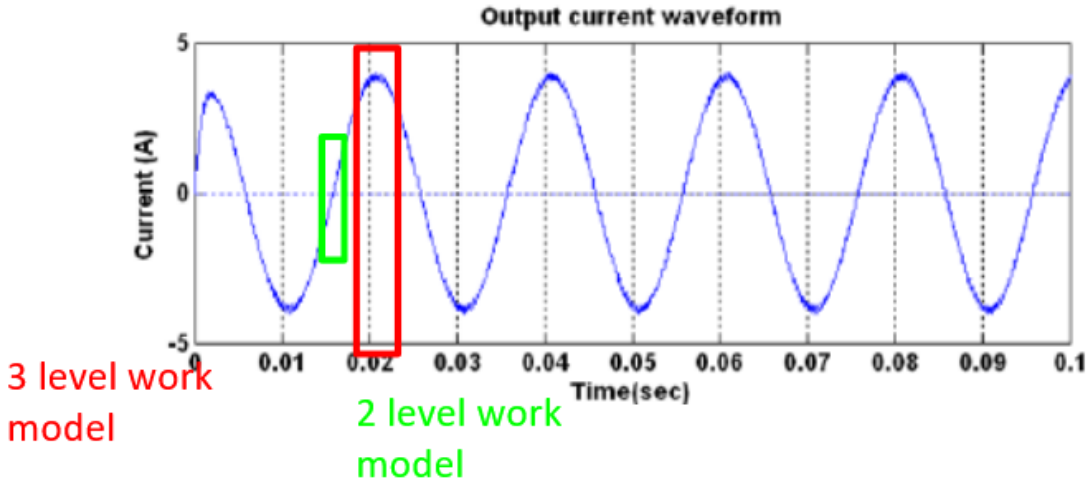


Figure 156 Hybrid control mode

So a hybrid control method is proposed. In the proposed work mode,T-type inverter work in T-Type soft switching mode in low power conditions. With the application of GaN, T-type inverter can work at a high switching frequency(200kHz) to reduce the output ripple and THD to realize a smoother work environment.

In order to verify the proposed hybrid control model A MATLAB Simulink model is built to verify it as shown in following figure. The input voltage is 800V. When the output AC

voltage is smaller than 400V, the traction inverter will work under t-type inverter model. When the AC output voltage is higher than 400V, the GaN MOSFET will be constantly turned off. The traction inverter will work at traditional inverter mode. The simulation waveform in the following to show the simulation waveforms to verify the effectiveness of the proposed waveform.

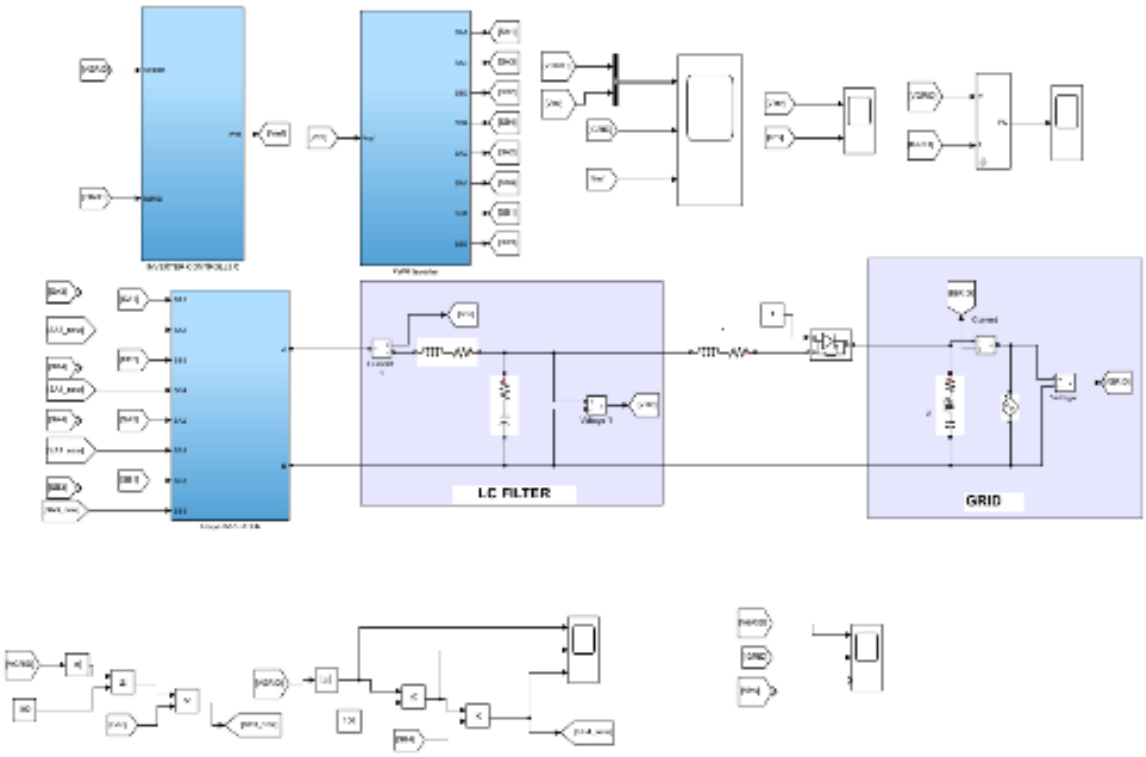


Figure 157 MATLAB Simulink model

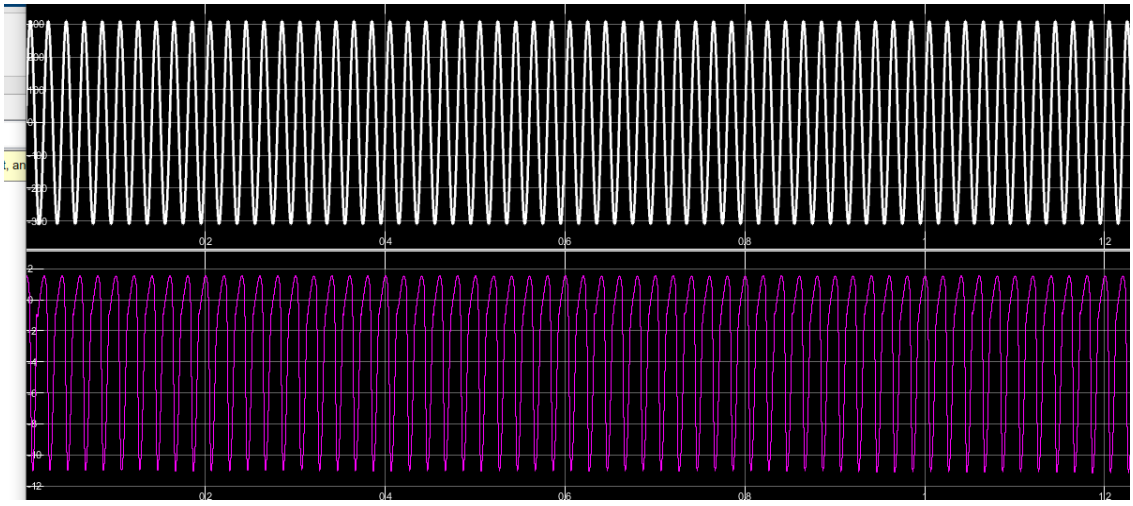


Figure 158 Simulink simulation waveforms

5.4 Conclusion

In this part, An effective application of GaN for traction inverter is proposed. The mid leg GaN can help IGBT realize soft switching to achieve a lower power loss. Meanwhile, a higher switching frequency also can have a smaller torque ripple. Furthermore, based on the EV traction inverter work load condition. A hybrid control method is proposed. The proposed method reduce the GaN MOSFET cost by only using GaN in the lower power condition. A MATLAB Simulink simulation model is built to verify the effectiveness of the proposed control method.

Chapter 6 DC Link Capacitor Degradation Investigation

6.1 Introduction

Metalized film capacitor (MCF) is widely used in traction inverters as the input DC link capacitor. MFCs are made of two layers of metalized films wrapped around a mandrel with clear margins at the opposite sides. The metalized film is composed of the dielectric base film and vaporized electrode layer above it. The commonly used dielectric film is then biaxially oriented polypropylene (BOPP) with a thickness of several micrometers. The potential factors for the capacitance decrease are voltage stress, current, temperature, humidity, etc. As an important part of a power converter. MCF is widely used as an input capacitor to maintain a stable input voltage and prove instant current. The capacitor value degradation could cause lower performance, even a system failure. Meanwhile, working conditions in an EV are different from other conditions. This paper is focused on the MCF capacitor degradation in EV working conditions.

The characteristic of MCF has been researched and discussed in [190]-[198]. [190]-[191] show the effect of inductance, DC voltage, ripple current, and crystallization regulation on the lifetime of the MCF. However, a continuous voltage and current condition in EV application are not considered. [192]-[196] investigate the influence of pulse current and voltage, but these papers do not consider a continuous high DC voltage influence. In [197]-[198], the research focuses on the character and performance of MCF. In [197], an investigation of the performance of the film capacitor in the three-phase Inverter is performed. But the degradation of MCF is not discussed. In [198], the performance of MCF under different temperature points are discussed, but the capacitance loss at different temperature point needs to be further discussed.

In this part, voltage stress, current value, and temperature are selected as the investigated factors. Three different voltage and temperature combinations are selected. The capacitors are tested under these conditions until the capacitance has dropped by 10% of the initial value. MCF capacitor capacitance degradation theory has been introduced. A two-stage capacitance value dropping model basic on electric vehicle working conditions is proposed. A DC link MCF capacitor test bench was set up. A total of eight capacitors curves were tested, and the experimental data were collected. Another DC-link capacitor short circuit phenomenon at extra high-temperature test conditions is discussed.

6.2 MCF Capacitor Degradation Principle

The film capacitor is composed of two film electrical coils. When the film capacitor is under working conditions, the frailest part could be vapored due to the heating and voltage stress. A glow discharge occurs in the micro-void. This discharge generates heat due to a high current density in the breakdown region, which causes evaporation of the electrode

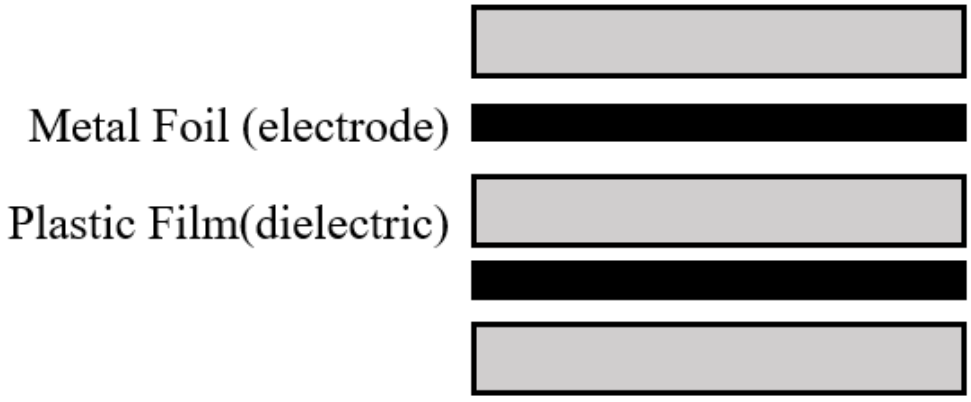


Figure 159 Capacitor degradation principle

layer around the void. Due to film capacitor self-healing characteristics, the vaporized area will be disconnected from other areas and smaller the effective area. So, the capacitor can still work in a lower capacitor value, as shown.

At elevated temperatures, dielectric films' volume increases due to thermal expansion. Usually, there is a thermal expansion difference between the electrode metallization film and dielectric film. Also, imbalanced temperature distribution will influence the structure of the film capacitor. The dielectric distance could be decreased due to the thermal expansion and imbalance in temperature distribution. So, the voltage stress could be increased by a higher working temperature. Lifetime could be lower at a higher temperature.

Apart from voltage and temperature, another vital stress factor, especially in DC link capacitors, is the ripple current. The RMS current could generate heating through the equivalent series resistance (ESR) of the film capacitor. The self-heating could result in a temperature rise. So, the influence of the ripple current could be the same as the influence of the temperature. Usually, Metallized film capacitors using PP as the dielectric are less affected by the ripple current due to a lower ESR value.

The estimated lifetime equation for tested MFC is shown in Eq (105). Based on the above capacitor value decreasing theory and our test condition. Temperature and voltage are selected as the influence parameters of the capacitor lifetime.

$$L = L_0 \left(\frac{V_0}{V}\right)^n 2^{\frac{T_0 - T}{10}} \tag{105}$$

where L0 is the reference lifetime at the reference voltage V0 and reference temperature T0.

6.3 The Test Bench Setup and Operating Conditions

An overview of the test setup is shown in Fig. 160. It consists of an inverter under test, a DC source, an isolation phase transformer, 16 thermocouples, two chillers, an inductive load (In phase, the inductor load value is changed to 350uH), and a data acquisition system (including three voltage and current sampling boards modules), and a desktop computer. Furthermore, the cooling system is composed of two chillers connected in series with increased cooling capability. In the experiment test, two voltage levels, 423.5V and 385V, are selected. Two temperature points 105C and 115C, are selected for the capacitor working temperature. Also, two capacitor RMS current points 30A and 90A, are selected to check the influence of DC-link capacitor RMS current. There is eight capacitance dropping curves in total. The various testing conditions are shown in Table . The capacitor temperature is obtained from six test points on the DC link capacitor as shown in Fig.161.

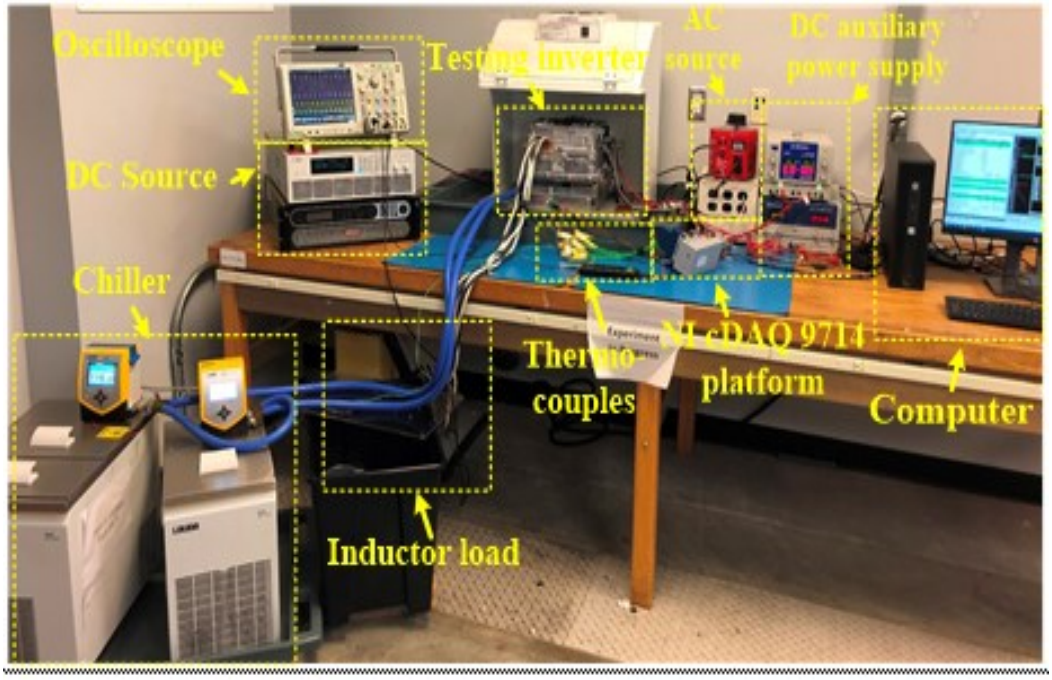


Figure 160 Test bench overview

Figure 161 Capacitor temperature test points

Table 13 Environmental tests and number of samples

Group number	Input voltage/V	Capacitor temperature/C	Capacitor Current/A	No. of samples
Phase1.1~1.4	385	110	30	4
Phase 1.5	385	115	30	1
Phase2.1	385	115	90	1
Phase2.2	423.5	105	90	1
Phase2.3	423.5	115	90	1

6.4 Two-stage Capacitance Degradation Model

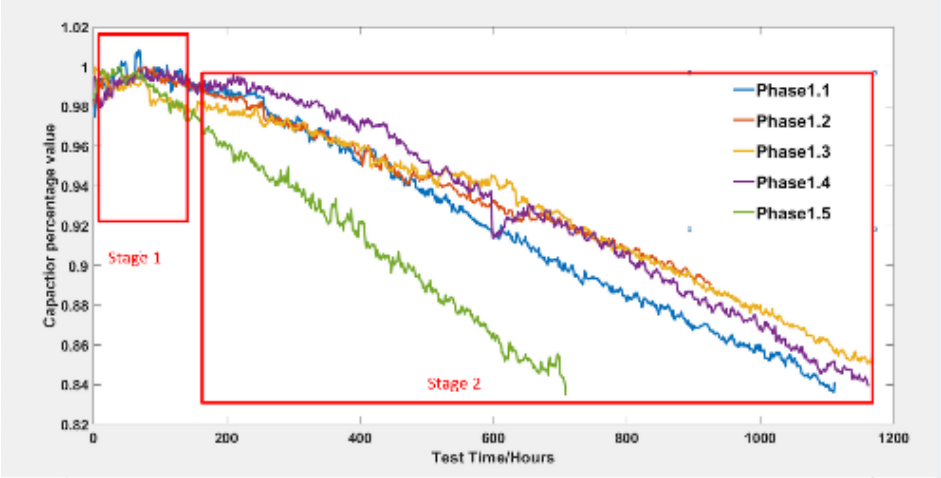


Figure 162 two-stage capacitance degradation model

Based on the test results, capacitor degradation can be classified into two stages. Stage one is the capacitance increasing stage. When a constant high voltage is applied to MCF, the voltage stress will make the distance between the positive and negative poles smaller. It will result in a capacitance increase during the initial period. The increasing time is decided by voltage and temperature. A higher temperature and voltage stress will increase the molecular activity rate and reduce the rising time. Meanwhile, higher voltage stress will result in a shorter pole distance to increase the capacitance value. So, the equations in the first stage are summarized as follows:

$$t = t_0 (\frac{V_0}{V})^{n_1} 2^{\frac{T_0 - T}{10}} \tag{106}$$

$$C_0 = C(\frac{V_0}{V})^{n_2} \tag{107}$$

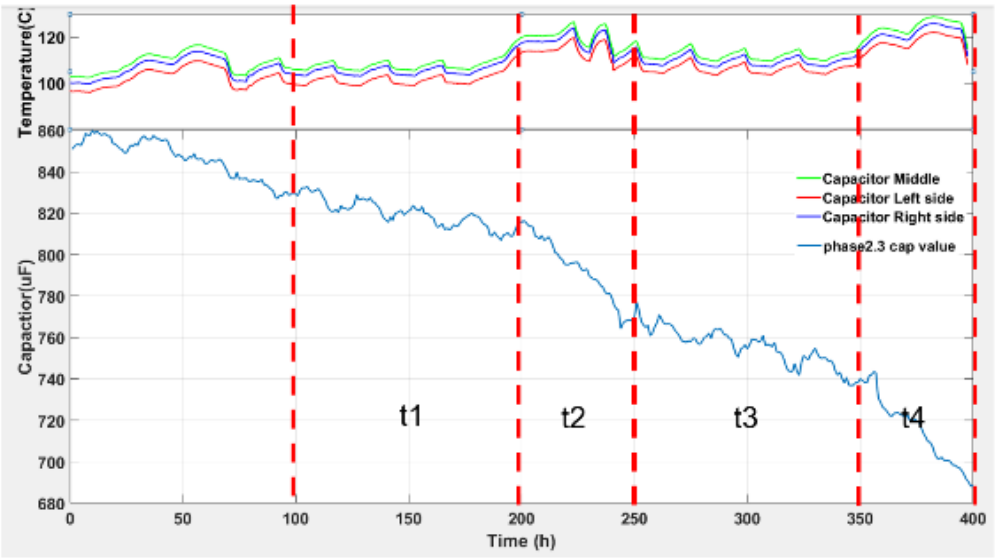


Figure 163 Capacitance changing with temperature

where t is the whole rising time of the first period, C is the highest capacitance value in the first period. t_0 and C_0 are the rising time and highest capacitance values, respectively, at reference voltage V_0, and temperature point T_0, n1, and n2 are correct factors.

For stage two, the capacitor is working under an almost constant voltage condition. Meanwhile, in an electric vehicle application, the actual voltage on the capacitor is always much smaller than the rated voltage of the capacitor. Therefore, it is different from the accelerated loss mode under pulsed voltage conditions. In this stage, the slop of the capacitor degradation curve can be treated as a fixed value. A high working condition voltage will increase voltage force to accelerate the degradation speed. A higher molecular activity rate in a higher temperature point will also lower the capacitor lifetime. The capacitor lifetime equation in the second period is shown:

$$L = L_0 \left(\frac{V_0}{V}\right)^{n_3} 2^{\frac{T_0 - T}{10}} \tag{108}$$

where L_0 is the reference lifetime at the reference voltage V_0 and reference temperature T_0. L is the lifetime at the working condition voltage V and temperature T.n3 is the correction factor.

Compared to other normal capacitance degradation theories. The MFC degradation slope will have a shape increasing when the capacitance value is extremely low. It can be explained that when the capacitance value is low. The effective section area is much lower than before. In the same size area, the voltage stress is

6.5 Test Results and Analysis

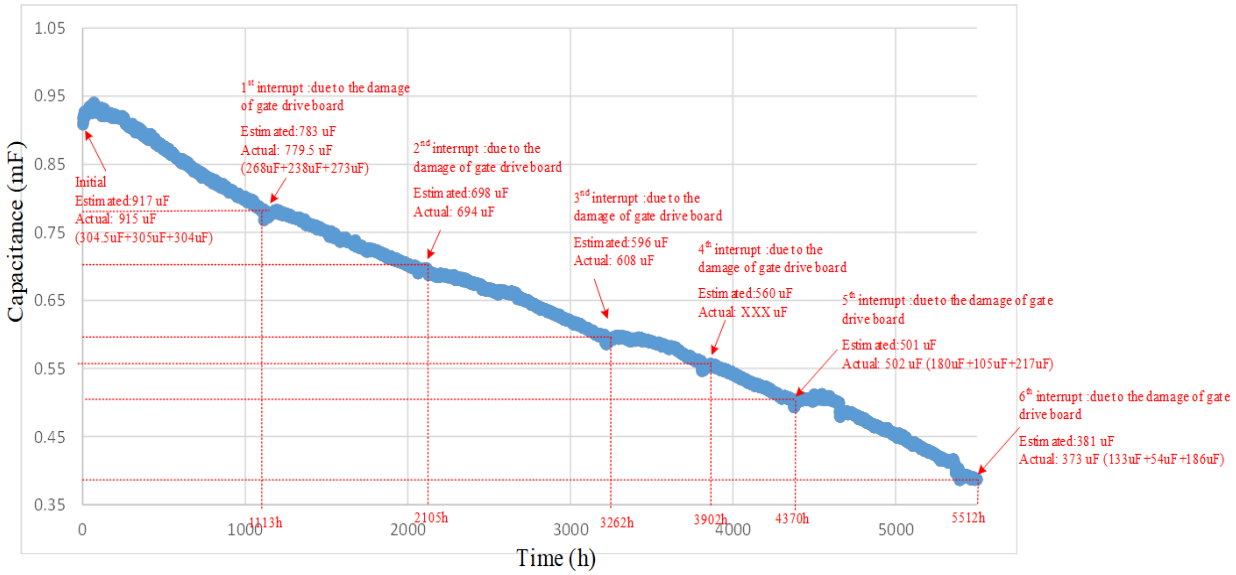


Figure 164 long term test capacitor value degradation curve.

In the phase 1 test, A capacitor was kept running for 5000 hours. This 5000-hour curve is composed of 6 periods. In each period, each curve is composed of two stages. The first stage is the capacitance increasing due to voltage stress. The second stage is the degradation in a fixed slope. After 5000 hours continuous test, the capacitance drops from 915uF to 317uF. Also in the second stage, degradation slope is almost fixed

In the capacitor degradation test, we selected a 10% capacitance decrease as the minimum target for all tests. Figure 165 shows all eight curves we obtained in test phase 1 and phase 2.

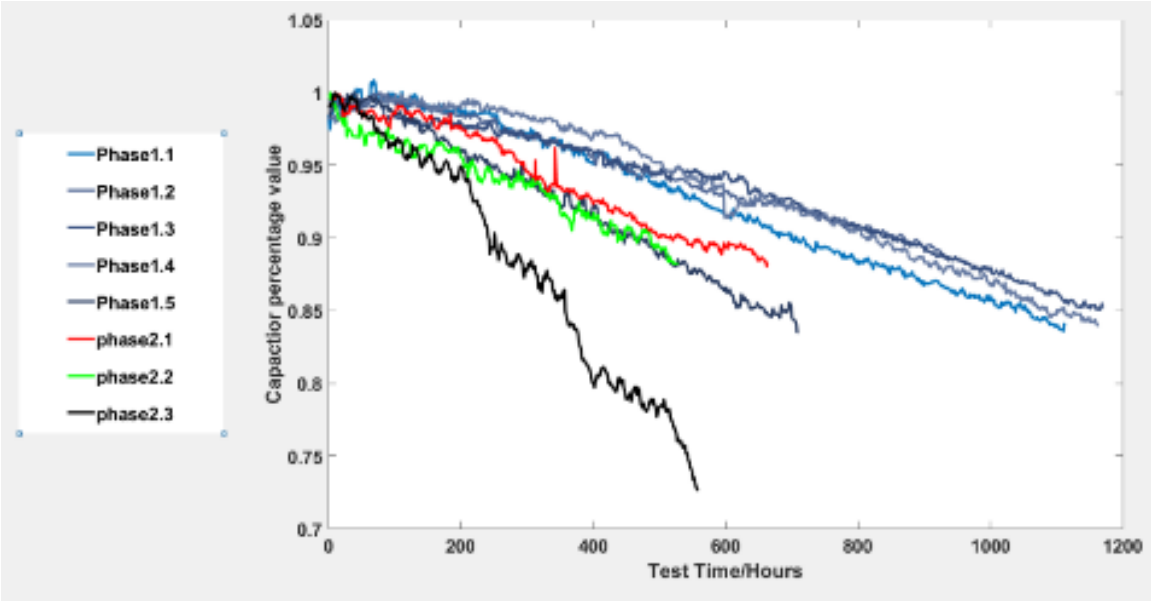


Figure 165 Capacitor degradation curves

Phase 2.3 has the highest temperature and voltage, so the dropping slope of phase 2.3 is the highest among all the tests. The calculated dropping slope value difference verifies our proposed capacitor value decreasing equation. The dropping slope of phase 1, phase 2.1, and phase 2.2 are similar. During the phase 1 period, the working condition is 385V/30A/110~115C (phases 1.1-1.4 are under 100C, and phase 1.5 is under 115C). For Phase 2.1, the working condition is 385V/90A/115C. The voltage for Phase I and Phase II was kept the same. By comparing the working conditions in the two phases, we can find that, although the RMS values of input capacitor ripple current is different, the working temperature is very similar. The slope of the capacitor degradation curves is almost identical. The influence of the capacitor current is very similar to that of the temperature.

We found that the capacitance dropping slope is sensitive to the temperature in the test, as shown in Fig 166. We can see that the slope during $t_2$and t_4 (higher temperature) is much larger than the temperature in t_1 and t_2 (lower temperature period). Also, in the t_1 and t_3 period, the capacitance variance is aligned with the temperature ripple.Proposed capacitor value decreasing equation. The dropping slope of phase 1, phase 2.1, and phase 2.2 are similar.

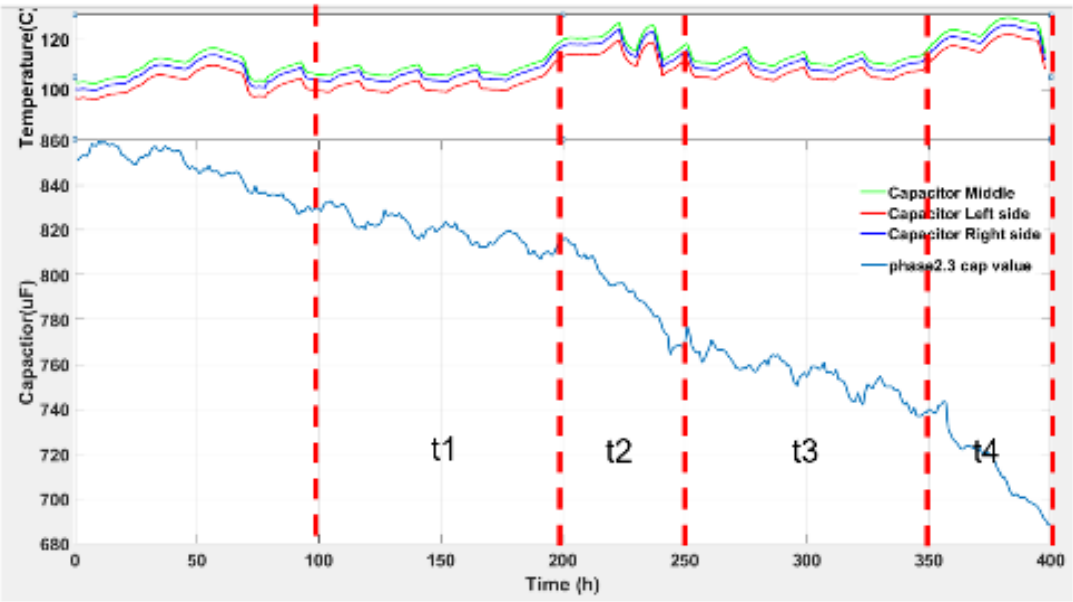


Figure 166 degradation curve with temperature changing

6.6 Capacitor Temporary Short Circuit

In a high voltage and temperature working condition. The capacitor could also have a temporary circuit issue. The equivalent parallel resistance could drop to zero, as shown in figure.167. However, this short circuit is not a permanent issue. The equivalent paralleled resistor could increase back to a normal value when the temperature goes down.

This phenomenon could be explained by voltage and temperature stress. When a high voltage is applied to MCF film, positive charges on the positive electrode and negative charges

on the negative electrode will generate a force to reduce the air gap. Meanwhile, a high temperature could cause the expansion of metal film. An expended metal film will also decrease the air gap length when the air gap length between positive and negative electrodes is small enough. A voltage breakdown will result in a temporary short circuit phenomenon. A high input voltage will let a short circuit happen at a lower temperature, as shown in the table.14. The capacitor equivalent resistance relation with working temperature is shown in fig.167 Also, the DC-link capacitor short circuit temperature point value will increase when the DC link voltage decreases, as shown in table 14.

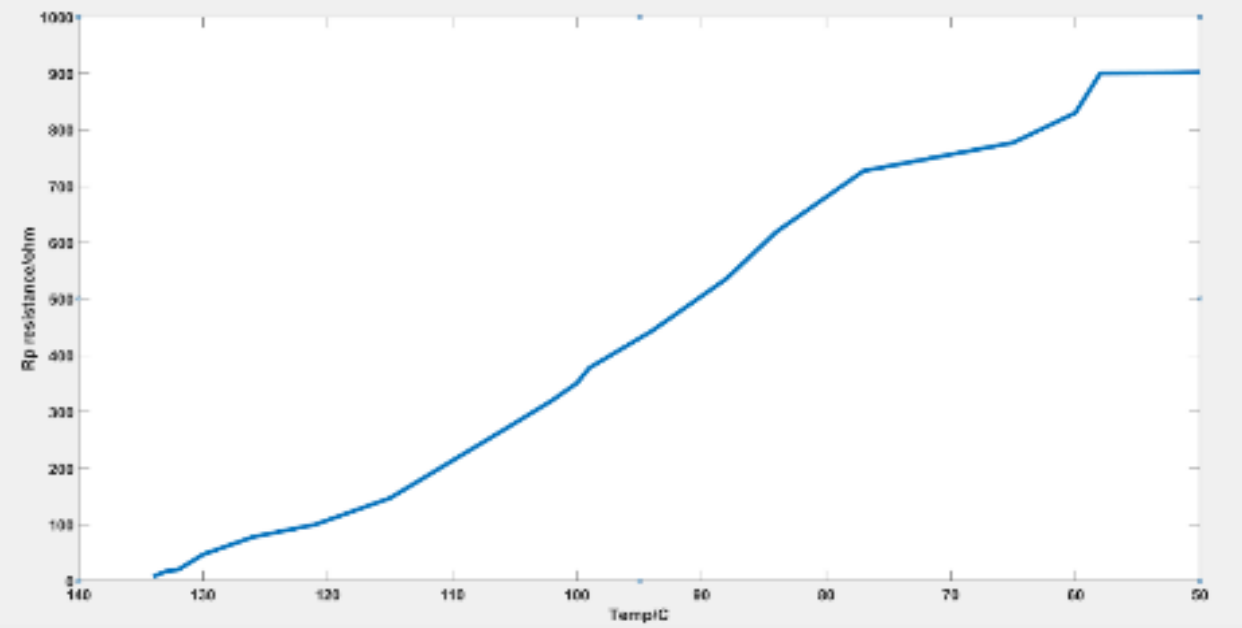


Figure 167 Capacitor equivalent paralleled resistance Rp value changing with temperature

Table 14 DC link capacitor short circuit point value

Input voltage/V	**Average short circuit point value/C**
423.5	132.5
400	136.7
385	139.5

6.7 Conclusions

In this part, the MCF degradation in the EV application is investigated. The voltage and temperature are selected as the major impact factors. The capacitor degradation curves are obtained at different voltages and temperature working points. Different from the previous accelerated loss or four stages loss models, the MCF degradation model in EV application can be developed as a two-stage model. In the first stage, the capacitor value will increase. Then it will drop in an almost fixed slope. Meanwhile, a temporary short circuit phenomenon in the extra high-temperature condition is discussed. Overall, this paper analyzes the dc-link MCF capacitor degradation and failure theory in EV work conditions.

Chapter 7 Conclusion

During my whole Ph.D period. My main research is focus on the Wide band Gao deveices application on the EV power converters application. My main contribution on the hardware design can be summarized as (1) High frequency and lower noise gate drive loop design.(2) Low parasitic parameters power loop design for the high current application.(3) High power density and low power loss inductor design with the newest Nano material My main contribution for the software design can be summarized (1)Close loop design for high-frequency application (2) Sensorless multiple phases current balance control.(3) Multiple control methods in DAB to improve the output performance. Multiple power converters have been built to verify the effectiveness of proposed hardware and software design.

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