Ga_2O_3-Based Devices for High Power Switching Applications

by

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Dedication

To my parents and my husband Subhajit.

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Abstract

Ga_2O_3 is emerging as an attractive semiconductor for high power devices, which is promising to enable efficient high-power switches in the 2-20 kV voltage range. This dissertation is focused on understanding and resolving the fundamental issues severely limiting the performance of Ga_2O_3-based transistors by a combination of device design and developing novel fabrication processes.

Thermal management is crucial for engineering the performance and reliability of the emerging Ga_2O_3 technology with potential applications in harsh environments. The effects of temperature on the electrical characteristics of Ga_2O_3 trench and regular Schottky barrier diodes (SBD) device structures were studied. The superior thermal stability of trench SBDs will be presented in this dissertation.

High-quality dielectrics are important for enabling high-performance Ga_2O_3 field effect transistors (FETs). Especially, in the case of Ga_2O_3 for which shallow p-type doping does not seem to be feasible, developing a robust dielectric with large breakdown voltage and low interface trap density is crucial to take full advantage of Ga_2O_3 potential for high power switching applications. Two gate dielectrics including ALD-Al_2O_3 and MOCVD-AlSiO were investigated for β-Ga_2O_3 MOS capacitors (MOSCAP) and deep UV-assisted capacitance-voltage measurements were used to characterize the interfacial and bulk properties of dielectrics. These results will be presented and a comparison between these two dielectrics will be discussed.

Rapid advancements have been reported on key device DC parameters such as threshold voltage, on-resistance, leakage current and breakdown voltage. However, there is still a lack of knowledge on the switching performance of Ga_2O_3-based power devices. A novel 3.5 kV Fin-FET structure was designed and tested using Silvaco TCAD device-circuit hybrid simulator. The impacts of electron mobility, substrate thickness and fin width/pitch size ratio on the switching performance will be presented which provide helpful insights for design and fabrication of Ga_2O_3 power FinFETs for low-waste power conversion applications.

α-Ga_2O_3, which is a meta-stable phase, has the largest band gap (5.3 eV) compared to other polymorphs of Ga_2O_3. Furthermore, the corundum-structure of α-Ga_2O_3 makes it a promising wide bandgap semiconductor candidate because of the ability to produce heterostructures with its (Al, In, Ga)$_2$O$_3$ alloys which will enable bandgap engineering. In order to achieve α-Ga_2O_3- devices with different geometries, it is essential to develop high etch-rate etching conditions with low surface damage and smooth etch surface morphology. Inductively-coupled plasma technique was used to study the dry etching of α-Ga_2O_3. The effect of BCl_3/Cl_2/Ar gas ratio, bias and plasma powers and chamber pressure on etch rate, surface roughness and mask selectivity will be presented in this dissertation.

Two main challenges of β-Ga_2O_3 are its relatively low electron mobility and unavailability of p-type doping. On the other hand, GaN, has a high electron mobility, high 2D charge (2DEG) density, moderate thermal conductivity, and p-type doping with Mg. Therefore, the integration of β-Ga_2O_3 with GaN can potentially enable the fabrication of novel GaN/Ga_2O_3 high-frequency and high-power devices combining the merits of both GaN and Ga_2O_3 in addition to novel optoelectronic devices. Heterogeneous integration of N-polar GaN and β-Ga_2O_3 substrates in nano-scale are proposed either via direct bonding or by adding an ALD-ZnO as the “glue” layer

to enhance bonding uniformity. The impact of post-annealing temperature on the structural characteristics and electrical quality of bonded interface will be discussed.

Chapter 1 Introduction

1.1 High Power Switches in Power Converters

1.1.1 Power Electronics and Semiconductor Switches

Currently, many people use "the information age" to describe the age in which we are living. This age can also be called as "the power age" because we are confronted with a lot of questions in our society that are related to the power and energy, such as how do we harvest energy in a way that is sustainable for our earth, how do we use it efficiently and how do we control the power. Power electronics is at the heart of this industrial revolution, which can be found in various applications ranging from data servers, electric vehicles, and motor drives for industrial robotics. It has been predicted that as much as ~80% electric energy would pass through power electronics

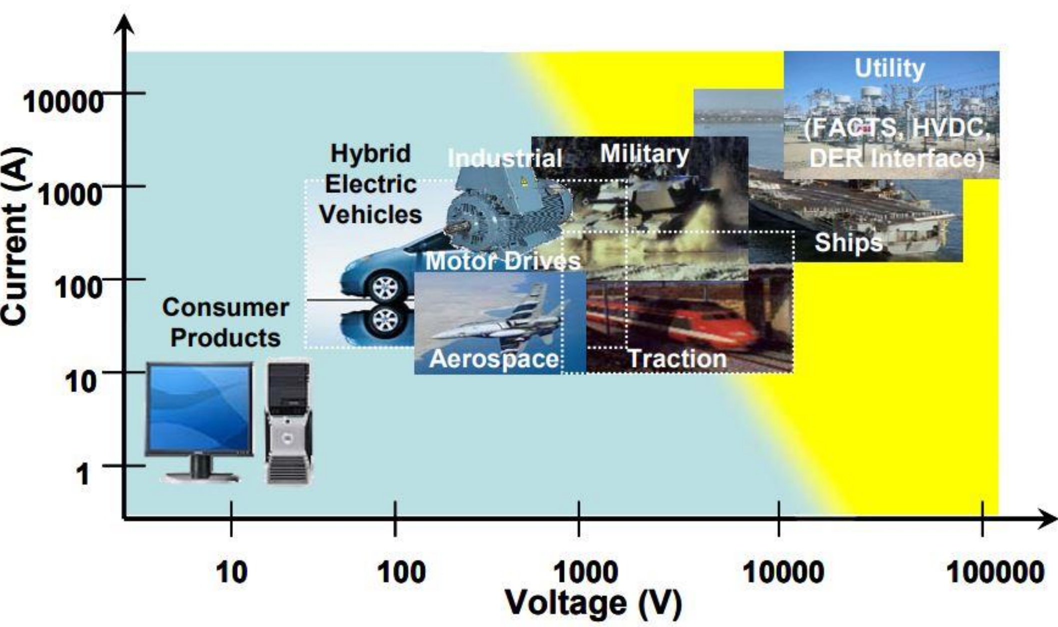

Figure 1.1 Voltage and current rating for different power electronics applications. [1]

between generation and consumption by 2030 [1]. However, more than 10% of generated electricity today is wasted through conversion losses apart from other losses. In addition, we are facing an urgent need for new device technologies to efficiently manage and distribute the power in the 2-20 kV rating, which is required in many advanced systems as shown in **Fig. 1.1**, including distributed power grids, high-speed vessels, and energy-intensive industrial and military systems.

Power electronics is the hardware system that uses semiconductor switching devices to convert electrical power flow from one form to another, such as AC/DC and the magnitude of current and voltage [2]. The conversion system requires some essential components, including a controller, semiconductor switches, passive components (capacitors, inductors, and transformers), heat sink, and packaging.

Figure 1.2 illustrates various conventional circuit elements that can be used for power conversion. The available circuit elements can be broadly classified into resistive, capacitive,

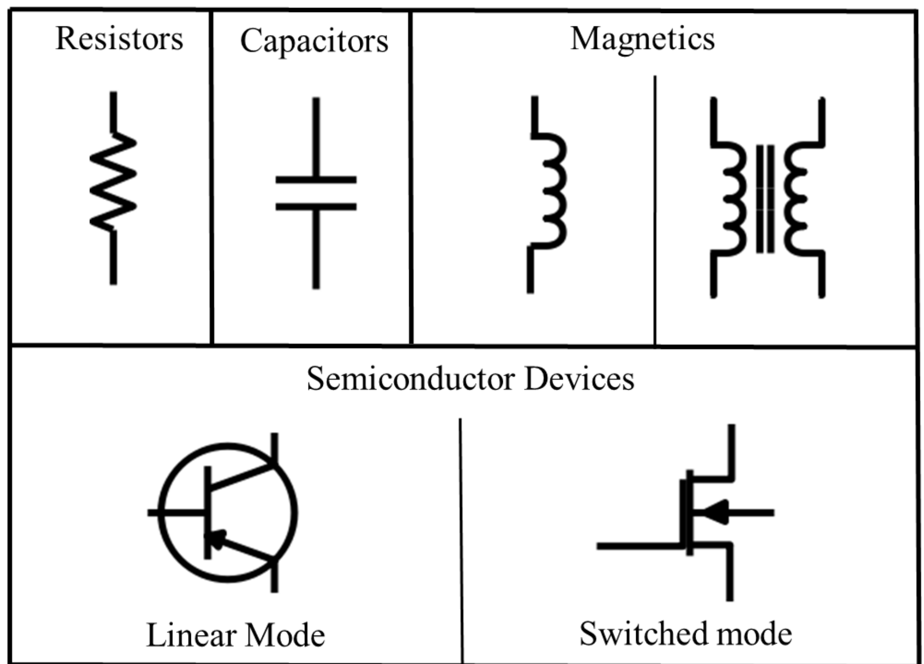

Figure 1.2 Various conventional circuit elements that can be used for circuit design.

magnetic devices including inductors and transformers, semiconductor devices operated in the linear mode (such as class A,B, AB amplifiers), or switched mode (such as in logic transistors operated in either saturation or cutoff). In the switching converter applications, where efficiency is the primary concern, resistive elements as well as linear-mode semiconductor amplifiers are not desired because of high power dissipation. Instead, capacitors and magnetic devices are essential elements because ideally they do not consume power. In addition, switched-mode semiconductor devices are also employed in the conversion circuits. For a switched-mode semiconductor device, when the device operates in the OFF-state, its current is zero despite of high blocking voltage and hence its power dissipation is zero. Similarly, when the device operates in the ON-state, its voltage drop is zero and hence its power dissipation is negligible. Therefore, capacitive and magnetic elements, as well as switched-mode semiconductor devices, are suitable for high-efficiency converters.

1.1.2 Key Metrics for Power Switches

An ideal power switch is capable of converting power flow from input to load with zero power dissipation, where the loads in systems may be inductive (motors and solenoids), resistive (heaters and lightbulb), or capacitive (transducers and LED lighting systems) [2]. The power delivered to a load is controlled by a periodic pulses of current generated by power switch with a control circuit. There are two states of the power switch, ON-state and OFF-state. As mentioned before, ideally there is no power dissipation during ON- and OFF- states. In addition, the transition between the on-state and off-state is instantaneous, resulting in no switching loss as well (**Fig. 1.3(a)**). However, in practice, power transistors exhibit a voltage drop in the ON-state due to the non-idealities associated with the transistor, such as resistive components in the device, and leakage current at a corresponding reverse voltage in the OFF-state, as shown in **Fig. 1.3(b)**. The

leakage current could increase upon illumination or at elevated temperatures. In addition, the power dissipation occurs during switching between ON- and OFF- states which results from non-zero voltage and current during transition period. At low operating frequencies, the ON-state power loss is usually dominant, making it desirable to develop power switches with low ON-state

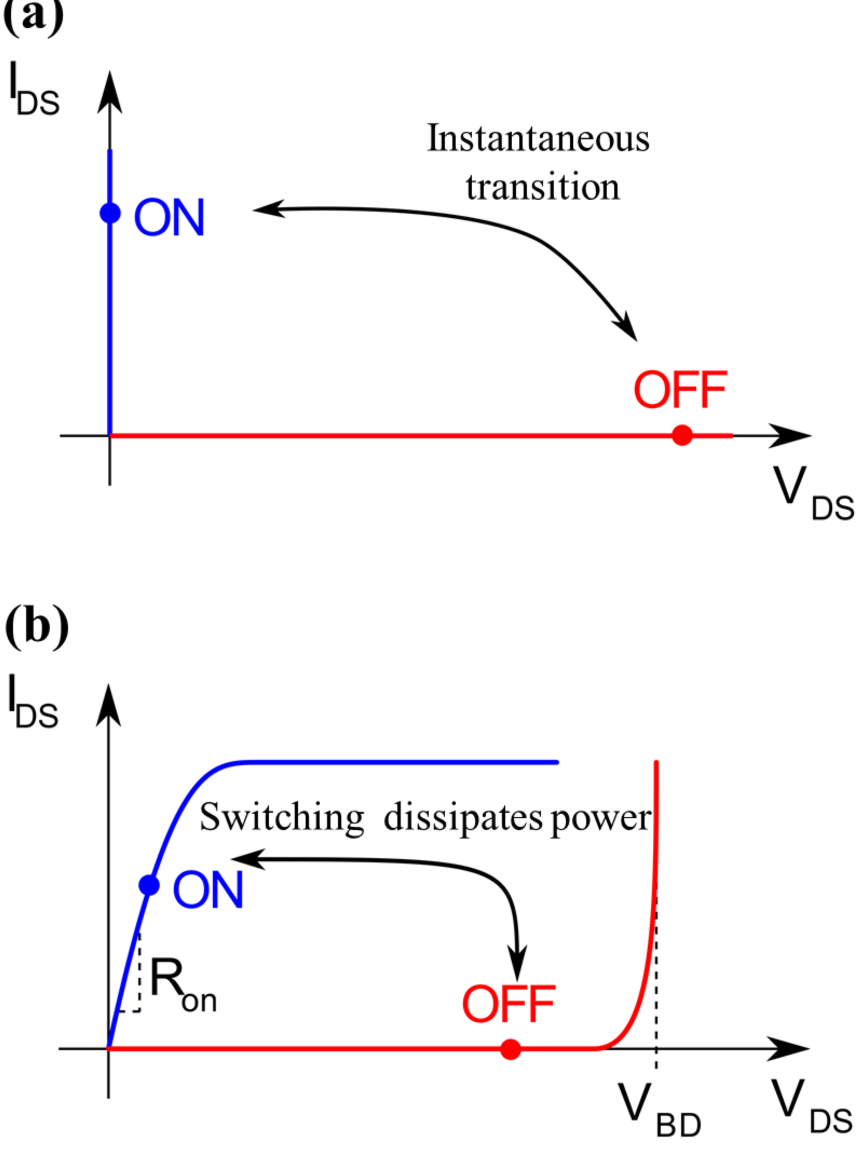

Figure 1.3 Characteristics of (a) an ideal power switch (b) a patricidal power switch with power dissipation.

voltage drops. In contrast, at high operating frequencies, the switching power losses are usually dominant, making it desirable to develop power switches with fast switching speed.

The waveforms of voltage and current across a switch are shown in **Fig. 1.4 (a)**. The total power losses as depicted in **Fig. 1.4(b)** can be written as

$$P_{LOSS} = \frac{1}{2}V_{OFF} \times I_{ON} \times t_{TURN-ON} + \frac{1}{2}V_{OFF} \times I_{ON} \times t_{TURN-OFF}$$
$$+V_{ON} \times I_{ON} \times t_{ON} + V_{OFF} \times I_{OFF} \times t_{OFF} \quad (1.1)$$

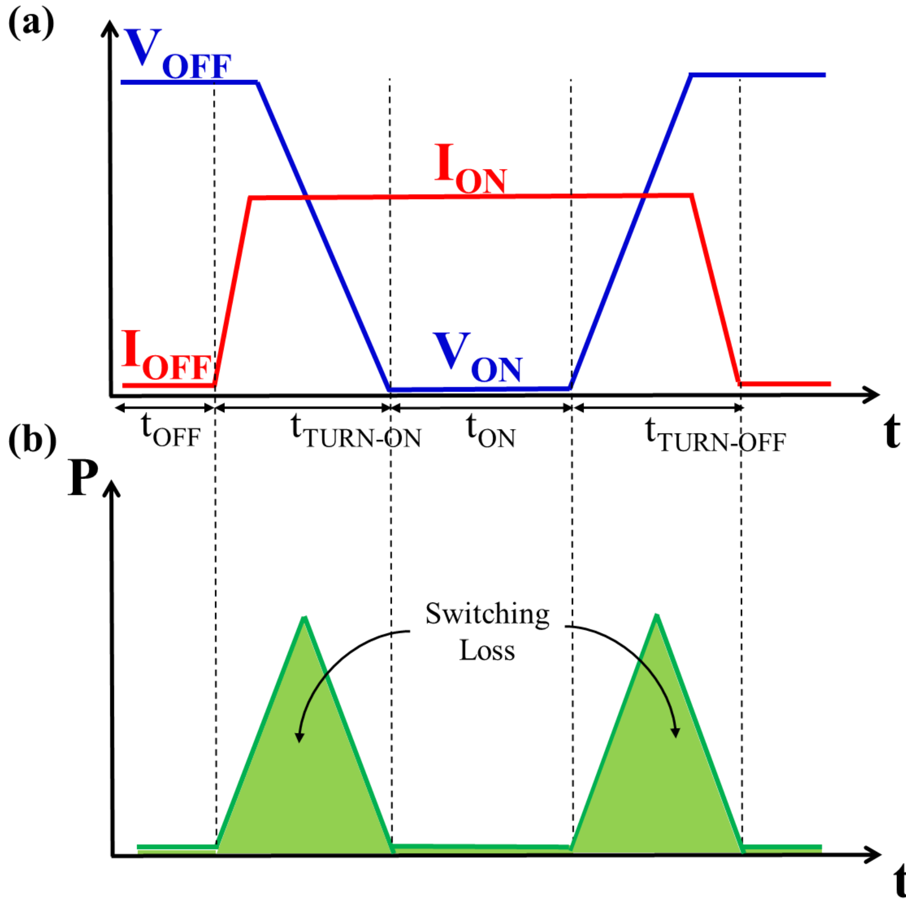

Figure 1.4 (a) The waveforms of voltage and current through the switch and (b) corresponding power loss.

where V_{ON}, I_{ON} and t_{ON} are the ON-state voltage current and time, V_{OFF}, I_{OFF}, and t_{OFF} are the OFF-state voltage, current and time, $t_{TURN-ON}$ and $t_{TURN-OFF}$are the turn-on and turn-off switching time.

1.2 Conventional Si-based Power Transistors

1.2.1 Unipolar Power Devices: V-MOSFET, VD-MOSFET, and U-MOSFET

The most commonly used Si-based unipolar power transistor is the power metal-oxide-semiconductor field-effect-transistor (MOSFET). Although other structures such as junction-gate field-effect transistor (JFET) or Static induction transistor (SIT) was explored in 1950s [3], they have not been widely exploited for power electronic applications because of their depletion-mode behaviors. In the mid-1970s, the first power MOSFET was developed using a V-groove etching process thanks to the different etch rates of Si crystal orientations [4], where the anisotropic wet etchants, such as Potassium hydroxide (KOH), tetra-methyl ammonium hydroxide (TMAH) and ethylene di-amine pyro-catechol (EDP) solutions, etches into (100) planes of silicon at a much faster rate than the (111) planes. The structure of the V-MOSFET is shown in **Fig. 1.5 (a)**. In contrast to the traditional planar MOSFET, the electrodes of power MOSFET are vertically arranged to distribute high current and the device has additional n- drift region to increase the blocking voltage. During the OFF-state, the gate is held at zero voltage which reverse-biases p-n junction J_1 between source and drain formed by p-base and n-drift regions. The device breakdown performance is determined by the reverse characteristics of the J_1 junction. A n+ source region is placed partially on top of the p-base region to enhance the ohmic contact with source electrode. The junction between the n+ region and the p-base region is shorted by the overlapping source

metal contact to avoid the formation of parasitic N-P-N transistor and improve the breakdown voltage. During the ON-state, a positive gate voltage is applied which creates an inversion layer under the gate dielectric same as in lateral MOSFET and the electrons flow from source to drain through the V-groove channel underneath the gate oxide and the n- drift region.

The advantage of the V-MOSFET structure is its more refined gate control and consequently high current for a given device area. However, the crowding electrical field near the bottom of the V-groove leads to not only the injection of hot electrons into the gate oxide driven

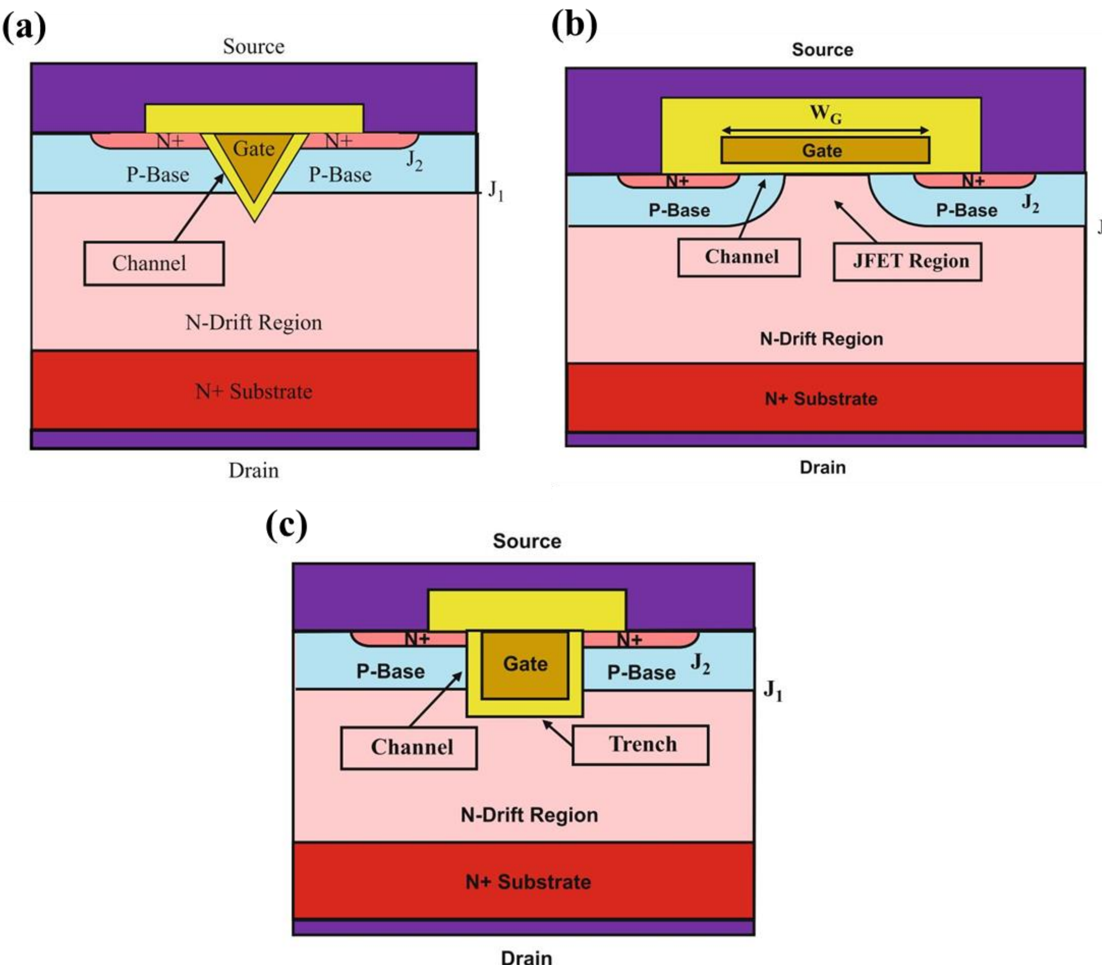

Figure 1.5 Cross-sectional schematics of power MOSFET structures: (a) V-MOSFET; (b) VD-MOSFET; (c) U-MOSFET [5].

by high electric field, but also the premature breakdown of the transistor. Both of them degrade the device performance.

To overcome this electrical field crowding effect under the V-groove, another planar device structure was proposed and known as vertical-diffusion MOSFET (VD-MOSFET) [5]. **Figure 1.5(b)** depicts the device structure of VD-MOSFET. The p-base and n+ regions are formed by a double-diffusion process upon n- drift region. As a result, the gate edges are protected by the p-base region, which reduces the electric field under the gate oxide and improve the breakdown voltage. Unlike the V-MOSFET, the VD-MOSFET does not require the anisotropic wet etching process, hence the etch-induced damages on the semiconductor is eliminated. However, the constriction of current in the junction field effect transistor (JFET) region between p-base and n-drift region introduces additional resistance to the R_{ON} in ON-state and puts limitation on the minimum gate length. To minimize the total internal resistance, a careful optimization of gate width is required for the device design.

In the 1980s, thanks to the development of dry etching techniques, the trench-gate MOSFET (U-MOSFET) was developed [6]. The structure of the U-MOSFET is similar to V-MOSFET, except for the U-shaped trench as shown in **Fig. 1.5(c)**. The gate electrode is patterned inside the trench after the formation of the gate oxide by thermal oxidation of the bottom and sidewalls. The JFET region is eliminated within U-MOSFET device structure as the trench extends beyond the bottom of the p-base region in order to form a channel connecting the n+ source region with the n-drift region. In this case, the n-drift region near gate electrode forms MOS structure and operates in the MOS accumulation mode. Consequently, this enables a significant reduction of the internal resistance when compared with the VD-MOSFET. Additionally, the cell pitch for the U-MOSFET structure can be designed much smaller to reduce the channel resistance contribution as

well. However, during the OFF-state, the electric field also crowds around the sharp trench corner. To improve both the breakdown voltage and the device reliability, the corners of the trench are rounded by wet etching techniques or shaded by ion implantation in practice. In general, among the three types of vertical MOSFETs, the U-MOSFET exhibits high current density, high breakdown voltage and high reliability. The optimization of this structure also enabled the improvement of the operating frequency up to 1 MHz for power MOSFETs [7].

1.2.2 Bipolar Power Devices: BJT, GTO, and IGBT

Today, within the operating voltage range below 200 V, Si-based power MOSFETs are the most commonly used power switches. However, in the power MOSFET structure, the power-handling capability was constrained by the internal resistance between the drain and source electrodes leading to significant power dissipation as well as the reduction in the efficiency of the power circuits in which they were utilized. Specifically, for the high voltage rating, a thick drift region with a low doping density is required, which increases the internal ON-resistance to an impractical value. Therefore, the bipolar devices were adopted in high voltage applications because the specific ON-resistance of the bipolar devices are lower than unipolar devices. This can be attributed to the conductivity modulation caused by the high-level minority carrier injection where the minority carrier density approaches or even exceeds the majority carrier density.

The first bipolar junction transistor (BJT) was first invented in 1947 [8]. After the development of photolithography and epitaxial deposition techniques for several decades, the first 500 V power BJT was demonstrated in the late 1970s [9]. In comparison with the conventional BJT, which has an either a p-n-p or an n-p-n semiconductor "*sandwich*" *structure*, the power BJT has an additional n-type lightly doped drift region to block high reverse voltage, as depicted in **Fig. 1.6(a)**. During the ON-state, the emitter-base p-n junction is forward-biased so that the electrons

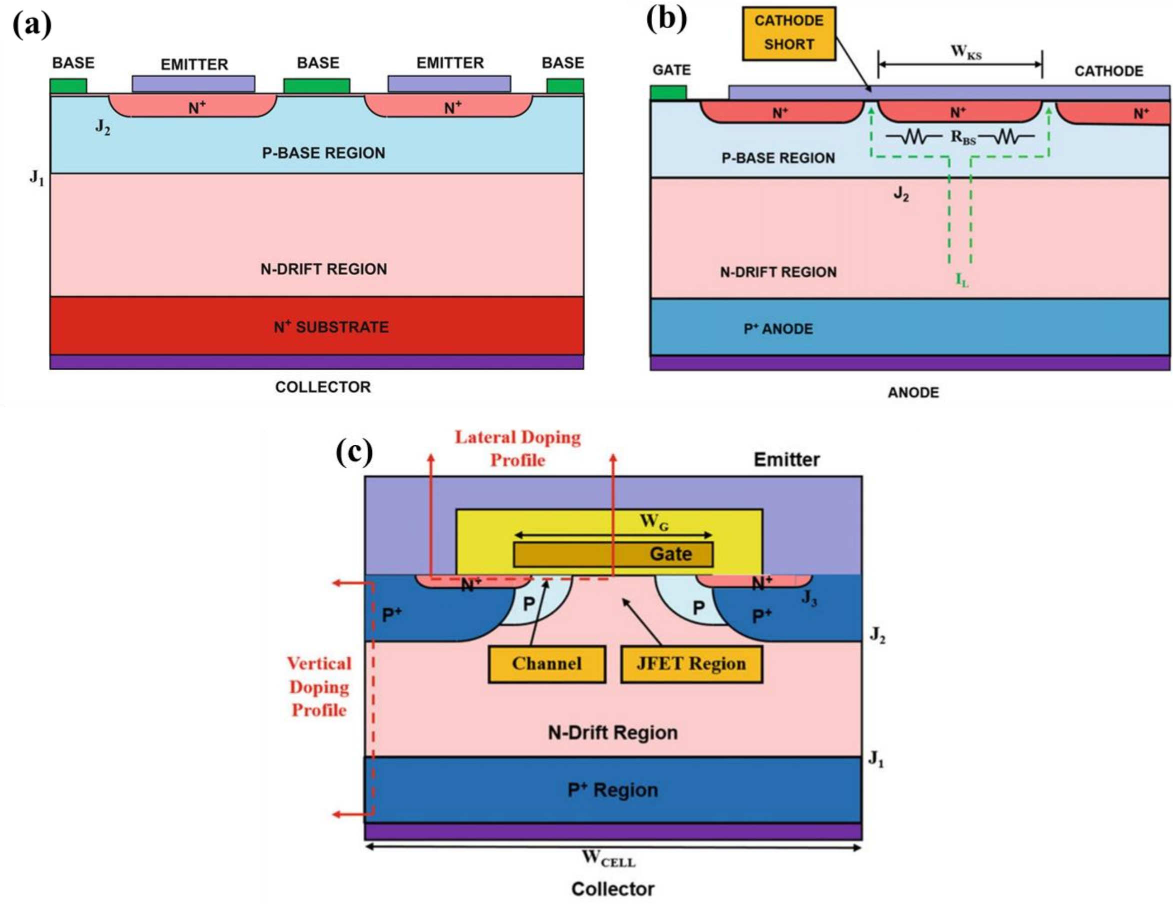

Figure 1.6 Cross-sectional schematics of bipolar power devices: (a) bipolar junction transistor (BJT); (b) gate turn-off thyristor (GTO); (c) insulated gate bipolar transistor (IGBT) [5].

are injected from n+ emitter region and diffuse into the base region. The base-collector junction is reverse-biased which pulls the minority carriers from base region to drift region, and finally reach the collector electrode [5]. During switching, a substantial amount of injected minority carriers are stored in the p-base and n-drift region, which needs to be recovered which prolongs the switching time and reduces the switching frequency compared to MOSFETs. Another major drawback of the power BJT is its low current gain, which limits the wide application of the devices.

The gate turn-off thyristors (GTOs) are developed for high voltage applications above 3 kV [5]. In addition, the power GTO provides both forward and reverse voltage blocking capability, making it suitable for AC power circuit applications. **Figure 1.6(b)** shows the GTO structure with

three p-n junctions in series. This results in two coupled BJTs: the first one is formed by n+ cathode/p-base/n-drift regions, and the second one is formed by p-base/n-drift/p+ anode regions. During the ON-state, a positive small gate current is applied to p-base region. Electrons are injected from n+ cathode region to p-base region, and then move into the n-drift region. The collector current of n-p-n transistor acts as base current for the coupled p-n-p transistor since n-drift region acts as its base. Hence, once current flow is initiated through the transistors, the two coupled BJTs are able to generate the base drive current for each other after an initial gate current supply which is referred as regenerative action. The GTO can remain in ON-state with a large current with very small voltage drop due to the positive feedback, which makes it energy-sufficient when compared with other bipolar transistors. This device can be turned off by applying a reverse gate current. Similar to power BJT, the main drawback of the GTO is its relatively long switching time because of long reverse recovery caused by the stored minority carriers. The switching frequency of GTO is limited to 1 kHz [5].

The first insulated gate bipolar transistor (IGBT) was reported in 1979 to overcome low current gain at high collector voltages which is considered as one of the major shortcomings of the bipolar power transistors for high voltage applications. The IGBT has become the most popular power device for high power (megawatt) applications. As shown in **Fig. 1.6(c)**, the IGBT is an improved hybrid coupled structure where a power MOSFET structure provides the gate drive current for coupled bipolar power transistor [5]. The bulk structure is formed by four n-p-n-p alternating layers. This again creates a basic thyristor structure. In order to suppress the thyristor operation within IGBT, a deep p+ diffusion is added to short the p-base region to the n+ emitter region. When a positive bias is applied to the gate of the IGBT structures, an inversion layer channel is created in the p-base region which allows the electrons flow from the n+ emitter region

to the N-base region. The electron current serves as the base drive current for the p-n-p transistor, which enhances the injection of holes from the p+ collector to n-base junction. The injected holes trigger the emitter current of the p-n-p transistor. The n-base (n-drift) region of the IGBT structures operates with high-level injection conditions during ON-state. Compared to bipolar transistors, due to the gate drive signal generated from a control circuit and applied to the power MOSFET, the IGBT can achieve compact, low cost, high input impedance and voltage-controlled operation. In addition, the source current of the power MOSFET is used to provide the base drive current for the bipolar power transistor, which is designed to carry most of the device current because of its superior ON-state characteristics.

However, IGBT has several disadvantages. The power MOSFET should have the same high-voltage blocking capability as the bipolar power transistor, which results in high ON-resistance in the power MOSFET structures. This thick drift region as well as the low current gain resulting from the bipolar power transistor, lead to a large device area in spite of typically carrying a tenth of the total device current. Hence the current density is reduced making the electronic circuit bulky and heavy. In addition, the reverse base drive current cannot be applied to the bipolar power transistor and therefore, the turn-off switching time is not ignorable. The limitation of the IGBT is the low switching frequency of below 50 kHz [5].

1.3 Introduction to Gallium Oxide

1.3.1 Evaluation of Materials for Power Switching Applications

Due to the limited material properties of Si, today's Si-based power electronic system is bulky, heavy and relatively inefficient. Wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), as well as ultra-wide-bandgap UWBG semiconductors, such as gallium oxide (Ga_2O_3) and diamond, have superior properties over Si for power switching

applications [10]. The performance of power switches is centered on the concurrent realization of low ON-resistance (R_{ON}), high breakdown voltage (BV), and low switching power losses. **Figure 1.7** compared the R_{ON} and BV of different materials [11]. The ON-resistance is calculated by

$$R_{ON,sp} = \frac{4V_{BD}^2}{\varepsilon \cdot \mu \cdot E_C^3} \tag{1.2}$$

where ε is permittivity, μ is carrier mobility, E_C is critical electric field. WBG and UWBG power devices can potentially achieve lower ON-resistance for the same BV. This enables a smaller pitch size, capacitances, and switching losses, as well as higher operating frequency, higher power density and conversion efficiency compared with similar voltage- and current-rated Si devices. Specifically, β-Ga_2O_3 has superior performance compared to Si and several second generation semiconductor materials such as GaAs and SiC. As opposed to other UWBG semiconductors such

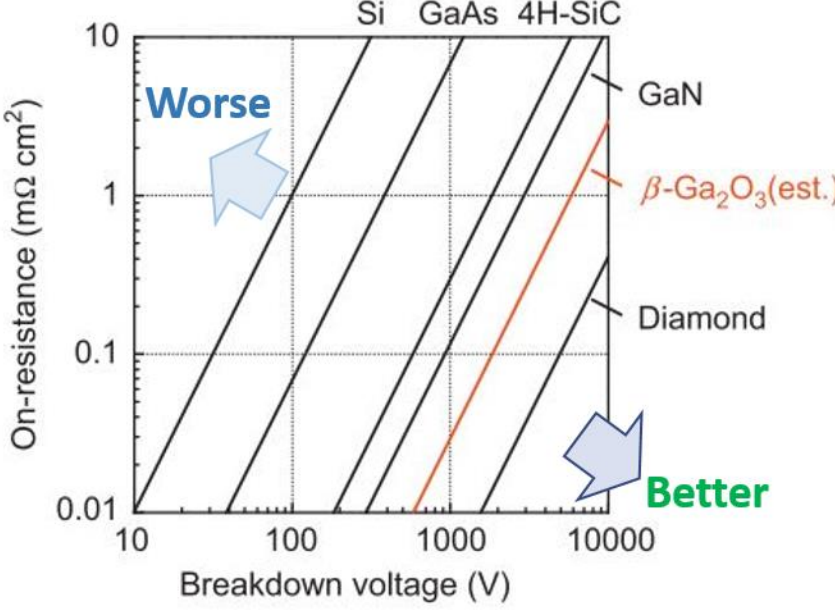

Figure 1.7 Theoretical unipolar performance limits of R_{ON} as a function of V_{BD} for β-Ga_2O_3 and other major semiconductors based power devices [11].

as diamond or AlN, the melt growth techniques are available for β-Ga_2O_3 to produce high-quality low-cost substrate. This will be elaborated in the following section.

Table 1.1 compared material properties of various materials. Among these materials, the large bandgap of Ga_2O_3 (5.1 eV for α-Ga_2O_3 and 4.8 eV for β-Ga_2O_3 [12]) allows high voltage operation. The primary obstacle to Ga_2O_3-based power devices is a low thermal conductivity, which causes the heat dissipation problem in high power operations. A possible solution is the integration of the Ga_2O_3 devices with a substrate which has a high thermal conductivity.

Among all the polymorphs of Ga_2O_3, β is the most stable phase, and is particularly attractive due to availability of melt growth techniques which enables production of low-cost large-area substrates. On the other hand, α-Ga_2O_3, which is a meta-stable phase, has the largest band gap [13]. Furthermore, the corundum-structure of α-Ga_2O_3 makes it a promising UWBG

Table 1.1 Physical properties of major power semiconductors [10], [19].

	Si	SiC	GaN	β-Ga_2O_3	α-Ga_2O_3	Diamond
E_g (eV)	1.1	3.3	3.4	4.8	5.1	5.5
E_C (MV/cm)	0.3	2.5	3.4	8.0	9.5	10
n-type doping	Yes	Yes	Yes	Yes	Yes	Difficult
p-type doping	Yes	Yes	Yes	No report	No report	Yes
μ_e (cm^2/Vs)	1300	800	1200	200	200	-
μ_h (cm^2/Vs)	450	320	150	-	-	2000
k_T (W/cmK)	1.3	4.2	1.5-2.5	0.1-0.2	No report	10-30
Baliga FOM	1	340	1450	3444	5767	24661

E_g: bandgap, μ_e/μ_h: electron/hole mobility, k_T: thermal conductivity, Baliga's FOM: $\varepsilon\mu E_C^3$ where ε is the permittivity.

semiconductor candidate because of the ability to produce hetero-structures with its $(Al,In,Ga)_2O_3$ alloys which will enable bandgap engineering. Moreover, it will allow hetero-epitaxial growth of various oxides with corundum crystal structure such as Fe_2O_3, and Cr_2O_3 [14], [15] as well as p-type oxides like Ir_2O_3 to enable designing different functional devices [14]–[16]. However, in contrast to β-phase, melt-growth techniques are not available for α-Ga_2O_3.

1.3.2 Melt-growth Technique for β-Ga_2O_3 Bulk Substrate

The availability of high-quality homogeneous bulk substrates is critical for growing high-quality epilayers with low dislocation density, where the leakage path for the carriers is reduced significantly and hence realizing high performance power devices. For most of the WBG semiconductor materials, such as GaN, SiC, diamond, etc., melt-growth technique is not possible. Therefore, they were only heteroepitaxially grown on largely lattice-mismatched foreign substrates at the early stage of technology development in contrast to the conventional semiconductors such as Si and GaAs. Later, the realization of bulk substrates by a vapor phase growth technique has enabled the growth of high-quality homoepitaxial layers and the free-standing bulk crystals could be obtained via self-separation processes for GaN or wet etching for SiC [17]–[19].

As oppose to most WBG semiconductors, the melt-growth techniques are available for β-Ga_2O_3, which makes β-Ga_2O_3 a very attractive candidate for power device applications. Multiple melt-growth techniques have been developed for β-Ga_2O_3 including edge-defined film fed growth (EFG), Czhochralski (Cz) method, floating zone technique and the vertical bridgman method [20]–[23]. So far, the EFG is the most successful bulk growth technique of β-Ga_2O_3 (**Fig. 1.8(a)**). In the EFG method, a board-shaped β-Ga_2O_3 crystal is grown between narrow iridium slits, through which the Ga_2O_3 melt is supplied by capillarity [24], [25]. The growth area can be much smaller

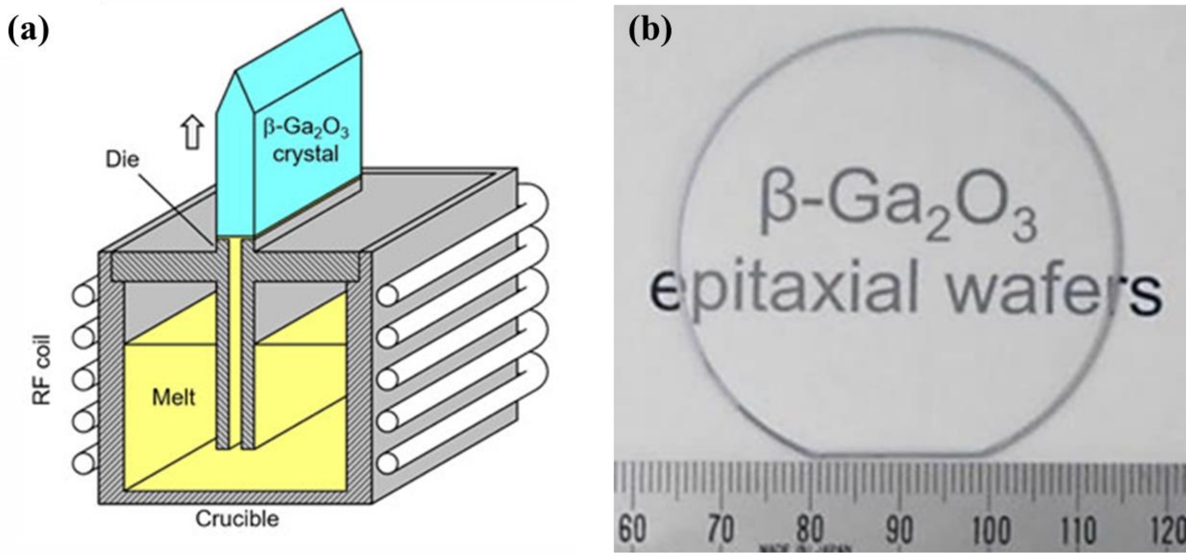

Figure 1.8 (a) Schematic of edge-defined film fed growth technique for the production of bulk β-Ga_2O_3 substrates [19]. (b) Photograph of 4-inch diameter single-crystal β-Ga_2O_3 wafer [26].

than that of other melt growth techniques, and, therefore, it is possible to minimize the dissociation and evaporation of the melt [19].

Currently, 25×25 mm^2 (010) wafers, 2-inch (-201) wafers, and 4-inch (001) wafers (**Fig. 1.8(b)**) with both n-type Sn-doping and semi-insulating Fe-doping are commercially available [26]. The dislocation density in EFG-grown β-Ga_2O_3 has been reported to be ~10^3 cm^{-2}, which is significantly lower than that in halide vapor phase epitaxy (HVPE)-grown GaN substrates (1.2×10^6-5.1×10^6 cm^{-2}) and is promising to for high power devices [17], [27].

1.3.3 Substrates for α-Ga_2O_3

In comparison, α-Ga_2O_3 is meta-stable at atmospheric pressure. As a result, the melt-growth is not available for α-Ga_2O_3. Hence it needs to be grown hetero-epitaxially on foreign substrates. Currently, only sapphire substrate (as large as 6-inch) has been used to grow high-quality α-Ga_2O_3. However, the dislocation density of an α-Ga_2O_3 epilayer on sapphire is as high as 10^{10} cm^{-2} because of the large lattice mismatch [28]. β-Ga_2O_3 can turn into α-Ga_2O_3 around 20-

22 GPa at room temperature [29]. In addition, it is possible to grow α-Ga_2O_3 crystals under 4.4 GPa at 1000 °C using β-Ga_2O_3 powder as the raw material [19], [29].

1.3.4 Current Status of Ga_2O_3-based Transistors

In the last decade, Ga_2O_3 power transistors has attracted a great deal of attention and shown excellent progress in high power switching applications [19], [30]. For power switches, normally-off (E-mode) transistors are typically more desirable over normally-on (D-mode) devices due to safety considerations and simplicity of gate-drive circuitry. The E-mode Ga_2O_3 MOSFETs can be realized by depleting the channel via a wrap-gate fin-array structure [31], an unintentionally doped Ga_2O_3 with low carrier concentration as channel [32], and gate-recessed structure with ALD SiO_2 as the gate dielectric [33]. The first E-mode MOSFETs was demonstrated in 2016, which consisted of Sn-doped Ga_2O_3 wrap-gate FinFETs on a native semi-insulating Mg-doped (100) β-Ga_2O_3 substrate [31]. These FinFETs exhibited normally-off operation with a threshold voltage around 1 V and an I_{ON}/I_{OFF} ratio higher than 10^5 which was mainly limited by high ON-resistance. The same group further developed the E-mode β-Ga_2O_3 transistors utilizing a recessed-gate process, as

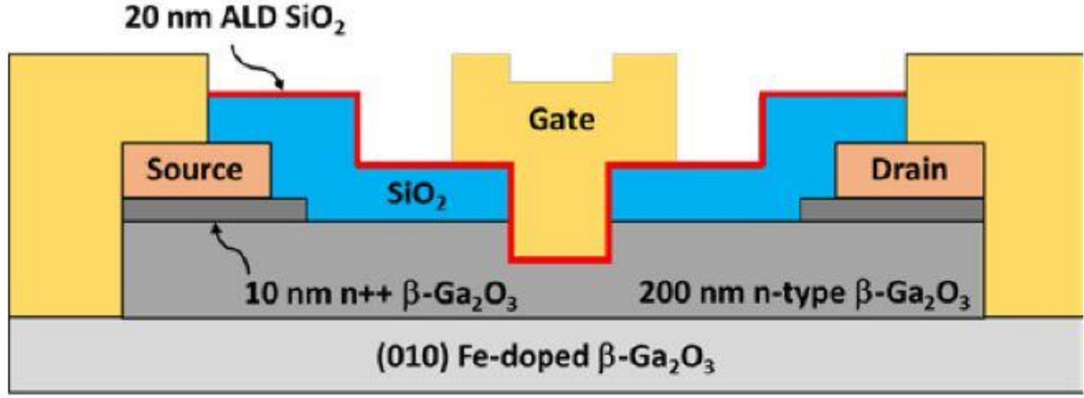

Figure 1.9 Cross-sectional schematic of enhancement-mode gate-recessed β-Ga_2O_3 MOSFET with L_{SD}=3 μm and L_G=1 μm [33].

shown in the **Fig. 1.9**. The recessed-gate structure depleted the channel under the gate followed by deposition of ALD SiO_2 as the gate dielectric [34].

Although breakdown voltage as high as 2 kV has been achieved on Ga_2O_3-based MOSFETs, the current densities reported so far are very low compared with their GaN counterparts which is mainly due to low channel mobility in this material system. To address this issue, modulation-doped field effect transistor (MODFET) has been demonstrated [35]–[38]. It was expected that the introduction of β-$(Al_xGa_{1-x})_2O_3$ and formation of two-dimensional electron gas (2DEG) would lead to enhancement of electron mobility in these structures. However, the highest room-temperature electron mobility reported, so far, in β-$(Al_xGa_{1-x})_2O_3$-Ga_2O_3 double-heterostructures has been only 180 $cm^2/V{\cdot}s$ limited by phonon scattering [36]. The electron mobility increased to 2790 $cm^2/V{\cdot}s$ at 50K. A maximum drain current of I_{DS}=257 mA/mm, a peak g_m of 39 mS/mm and a pinch off voltage of -7 V have been measured on MODFETs [35]. Very recently, the same group demonstrated a MODFET with a high breakdown voltage of 1.37 kV for

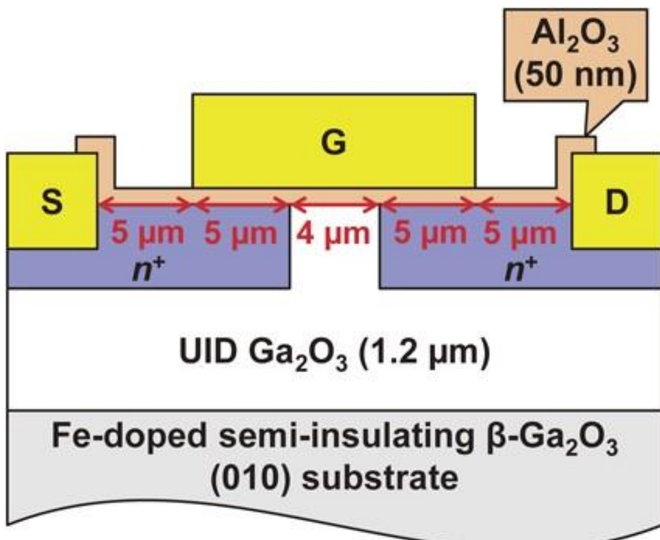

Figure 1.10 Cross-sectional schematic of the enhancement-mode β-Ga_2O_3 (010) MOSFET with Si+-implanted source/drain contacts and access regions [32].

a gate-to-drain separation (L_{GD}) of 16 μm having a specific ON-resistance of 120.1 mΩ.cm^2 using SiNx as the passivation dielectric (**Fig. 1.10**) [39].

For high voltage and high-power applications, vertical geometry are preferred to enhance packing density of devices and suppress the sensitivity of surface effects. Two types of vertical Ga_2O_3-based devices have been reported to date. Wong et al. fabricated a current aperture vertical transistor (CAVET) with a Mg-implanted current blocking layer (CBL) [40]. **Figure 1.11** shows the device structure of Ga_2O_3 CAVET. The selective area Mg-ion-implantation was implemented to form the CBL to block current from the aperture region other than any other paths. A recent study showed that the N-implanted CBL helps to improve the device characteristics as N atoms are more stable in β-Ga_2O_3, whereas Mg diffuses into active region during the post-implantation annealing [41]. Moreover, in this Ga_2O_3 CAVET, holes generated during the reverse bias will accumulate in the CBL. If the CBL is not grounded, the accumulation of holes in this region will lead to a large negative shift in threshold voltage resulting in device instability [42].

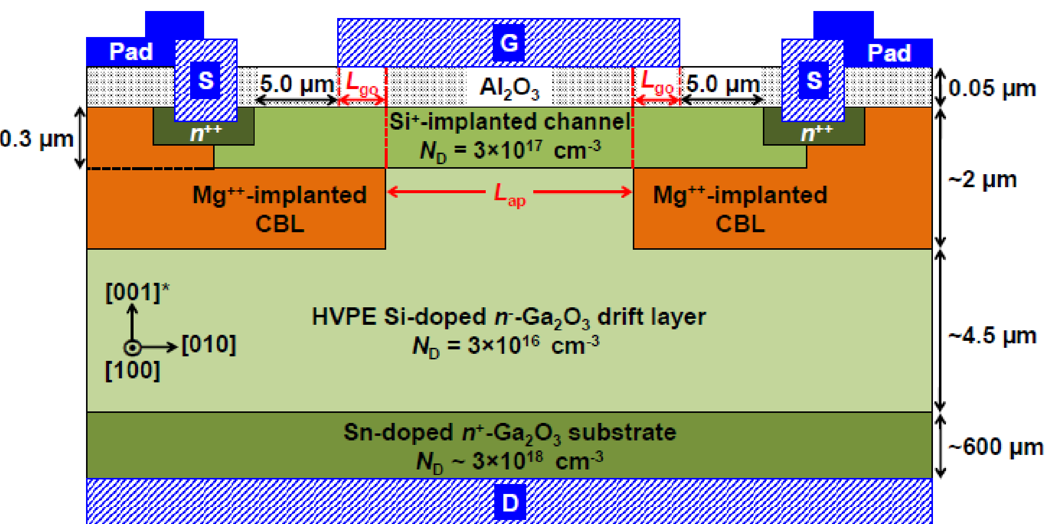

Figure 1.11 Cross-sectional schematic of β-Ga_2O_3 CAVET MOSFET with L_{go} = 2.5 μm and L_{ap} = 15 μm [40].

Owing to the development of a Ga_2O_3 dry etching process to achieve deep trenches > 1 µm, another E-mode Ga_2O_3 vertical FinFETs was proposed as depicted in **Fig. 1.12** [43]. This device has achieved BV of 2.6 kV, R_{ON} of 0.52 mΩ/cm^2 and record-high BFOM of 280 MW/cm^2 [43]. The positive threshold voltage was achieved by depleting the submicron-wide fin-shaped channels. The main issue in this device is the low electron mobility in the channel (30 cm^2/Vs) due to the surface roughness and interface-trapped charge caused by dry etching [43]. Additionally, the dry etching caused interface trap states between dielectric and Ga_2O_3 leading to current collapse and device degradation. Therefore, to enhance the performance of β-Ga_2O_3 FinFETs and improve their reliability, various techniques including wet etching, regrowth, and post-deposition annealing (PDA) may be investigated to improve the surface quality of the sidewalls [43].

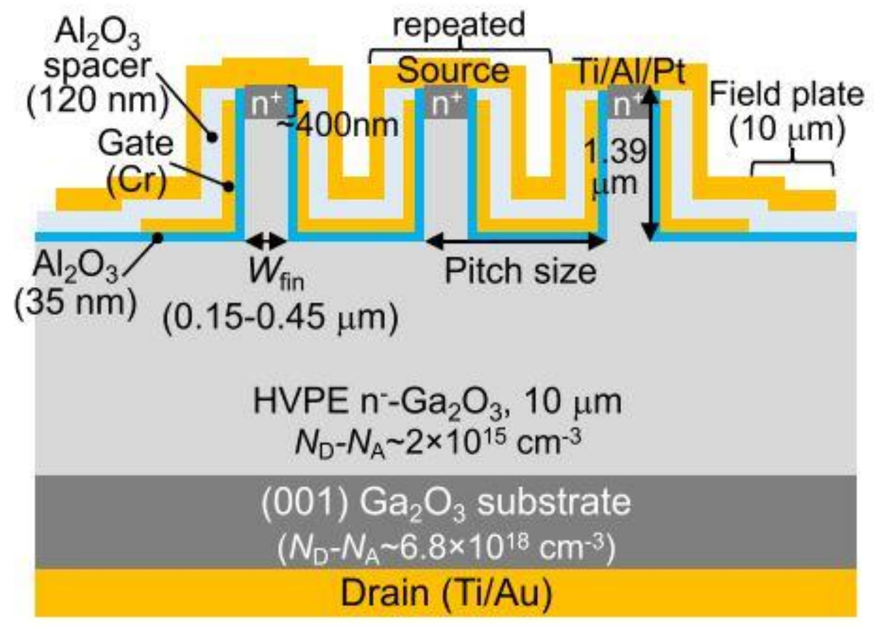

Figure 1.12 Cross-sectional schematic of β-Ga_2O_3 vertical Fin-FET power transistors [43].

1.4 Dissertation Overview

The objective of this dissertation is to understand and resolve the fundamental issues severely limiting the performance of β-Ga_2O_3 transistors by a combination of novel process, device design and modeling. Chapter 2 investigates the thermal stability of Ni/Ga_2O_3 trench Schottky barrier diode at temperatures ranging from 100 K to 650 K. The highly rectifying and thermally stable performance of these diodes offer considerable potential for high power Ga_2O_3 devices in harsh environments. Chapter 3 presents the dielectric study of Al_2O_3 and AlSiO for β-Ga_2O_3 in (001) orientation. Metal-Oxide-Semiconductor capacitors (MOSCAP) were fabricated and the interface and bulk properties were characterized using deep UV-assisted capacitance-voltage measurements. The AlSiO/Ga_2O_3 MOSCAPs achieve negligible hysteresis, low interfacial trap density, low leakage current, and high breakdown electric field up to 8.2 MV/cm. In Chapter 4, a device-circuit-integrated simulation is described to analyze the DC and switching characteristics of vertical Ga_2O_3 FinFET devices. The impact of electron mobility and Fin-field effect transistors (FET) structure on the OFF-state capacitances and switching characteristics is discussed. The total power loss of the input power at frequency of 200 kHz was reduced 82.2% for the demonstrated device structure with fully-filled interfin design. Chapter 5 in this dissertation provides further details on the chlorine-based dry etching technique for α-Ga_2O_3. Chapter 6 demonstrates the integration of Ga_2O_3 on the GaN substrate. The method achieved in this work is one of the promising approaches to combine the material merits of both GaN and Ga_2O_3 targeting the fabrication of novel high-frequency and high-power electronics as well as optoelectronic devices. Finally, Chapter 7 summarizes all of the essential remarks and understanding gained throughout this dissertation work and suggests future work that could be performed.

Chapter 2 Thermal Stability of Ni/β-Ga_2O_3 Trench Schottky Barrier Diodes

2.1 Introduction

2.1.1 Schottky Contact

A Schottky contact refers to a metal-semiconductor contact where a large potential energy barrier is formed for electrons. This barrier is called Schottky barrier. For an n-type semiconductor, to achieve a Schottky contact, the work function of the metal must be larger than the electron affinity of the semiconductor. The electron affinity of β-Ga_2O_3 is reported to be 4.00±0.05 eV [44]. According to the Schottky-Mott theory [45], [46], the metal/semiconductor Schottky barrier height φ_B obeys the relation:

$$e\varphi_B = e\varphi_M - \chi_S \tag{2.1}$$

where φ_M is the work function of the metal, and χ_S is the electron affinity of the semiconductor. The Schottky barrier has rectifying characteristics, which is suitable to be used as a diode. Currently, there are several Schotty contacts available for Ga_2O_3 such as Pt, Ni, Au, Cu, and Ir and their oxides with Schottky Barrier height ranging from 1 eV to 1.5 eV [10], [47]. Several experimental Schottky barrier values are consistent with the predicted values from Schottky-Mott theory[10]. However, the presence of surface states can modify the effective barrier heights by pinning the fermi level at surface neutral level which results in experimental barrier values differing from the theoretical values [48]–[50].

2.1.2 β-Ga_2O_3 Schottky Barrier Diodes

Schottky barrier diodes (SBD) are attractive for power switch applications to improve the efficiency of the motor controllers and power supplies, due to their fast switching speed and low threshold voltages compared to p-n diode. Additionally, the BV is strongly dependent of the bandgap of the semiconductor, which can take advantage of the ultra-wide bandgap property of Ga_2O_3 (5.1 eV for α-Ga_2O3 and 4.8 eV for β-Ga_2O_3) [12]. Ga_2O_3 Schottky diodes have numerous advantages over conventional Si rectifiers, achieving a critical electric field over 25 times larger and R_{ON} approximately 400 times lower at a given voltage [10]. These characteristics make Ga_2O_3 SBDs attractive for hybrid electric vehicles and energy-intensive industrial motors. Both lateral [51] and vertical β-Ga_2O_3 SBDs [52], [53] have been studied in recent years. Specifically, vertical SBDs with a backside electrode are preferred in ultra-high-power applications and can be realized in β-Ga_2O_3 materials system thanks to the availability of melt-grown β-Ga_2O_3 bulk substrates. High BV of over 1 kV has been reported in vertical SBDs by several groups [54]–[56]. A β-Ga_2O_3 trench SBD was first demonstrated by Sasaki et al [57] to decrease electric field and, consequently, current leakage due to thermionic field emission (TFE). Li et al. [58] later demonstrated trench SBDs with a BV of 1.23 kV, an ultra-low leakage current below 1 $\mu A/cm^2$, and a decent R_{ON} below 15 $m\Omega \cdot cm^2$. Very recently, the same group utilized field-plate technique to improve the BV of trench SBD up to 2.89 kV, and showed the highest Baliga's figure-of-merit (BV^2/R_{ON}) of 0.8 GW/cm^2 to date [59].

Despite of very promising results achieved on Ga_2O_3 SBDs, in practical device design, the instantaneous startup conditions require the diodes to be capable of operating under high current surge in the circuit. **Fig. 2.1** shows Si-based SBD with p-type regions are implanted in the n-type drift layer [5]. This p-type region has several functionalities. Firstly, it can provide the edge termination for SBDs by incorporation of a p+ guard ring overlapping the metal edge and screening

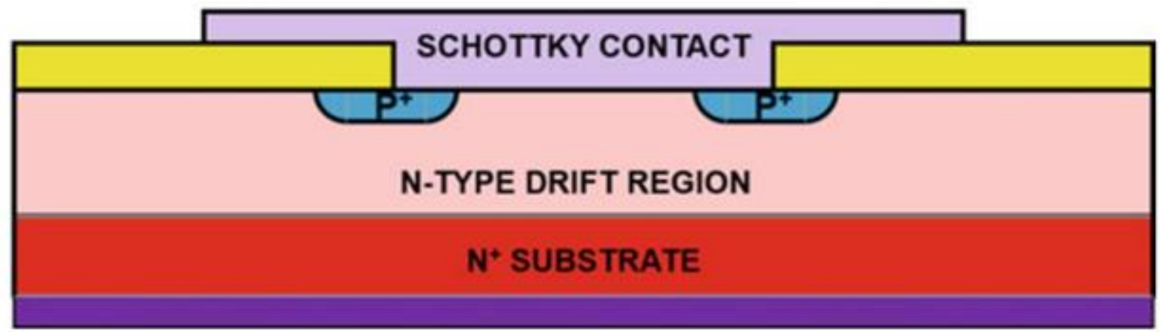

Figure 2.1 Schematic of Si-based SBD with implanted p+ area.

it from high electric fields. Secondly, the presence of the implanted p+ region also creates a p-n junction in parallel with the SBD. If the Schottky rectifier is operating with a low on-state Schottky voltage drop under normal operating conditions, the p-n junction does not get sufficiently forward biased to inject minority carriers into the drift region. This preserves the fast switching properties of the SBD which is essential for high-speed power switching application. Under surge current levels, where the diode is subjected to a very high on-state current density, the injection from the p-n junction (conductivity modulation) reduce the on-state voltage drop and power dissipation [5]. However, due to a combination of unavailability of p-type doping and large hole effective mass in β-Ga_2O_3 [60], fabrication of β-Ga_2O_3-based SBDs with p+ guard rings does not seem feasible for rectifying applications. Therefore, developing available p-type materials to form hetero-junction with β-Ga_2O_3 or other novel technologies that can accommodate surge current is necessary.

In addition, to enable high power applications in harsh environments (such as space exploration and deep oil extraction), it is important to investigate the thermal stability of Schottky contacts and temperature-dependent behavior of SBDs. The Schottky contacts need to be thermally stable and the interface between the metal and the Ga_2O_3 needs to be of high quality so that any defect-related leakage current is insignificant. Fares et al. [61] studied the thermal stability of

sputtered Tungsten as Schottky contact on (-201) Ga_2O_3 SBDs at high temperatures up to 775K. He et al. [62] investigated the electrical properties of Pt/(100) Ga_2O_3 SBDs at high temperatures up to 425K. As following, we demonstrate a novel Ni/β-Ga_2O_3 trench SBD structure and investigate its temperature-dependent electrical characteristics in comparison with regular SBDs.

2.2 Ni/β-Ga_2O_3 Trench Schottky Barrier Diodes

The schematic cross-section of the vertical trench SBDs is shown in **Fig. 2.2(a)** [63]. A top view microscope image of trench SBDs is shown in **Fig. 2.2(b)**. The devices are fabricated on an n-type β-Ga_2O_3 (001) bulk substrate with a 10μm lightly Si-doped epitaxial layer grown by halide phase vapor epitaxy. The 2” wafer was first diced into 1×1 cm^2 pieces, followed by an O_2 plasma treatment for 10min and HF cleaning for 10 minutes to remove residual hydrocarbons. Chlorine-based inductively coupled plasma (ICP) dry etching was performed on the backside of the sample to achieve better ohmic contact [64], followed by evaporation of Ti/Au (20/200 nm) as the cathode contact. Ni/Pt (20/100 nm) was then deposited and patterned via a lift-off process on the top surface, acting as the Schottky contact and the hard mask for the subsequent etching for trench

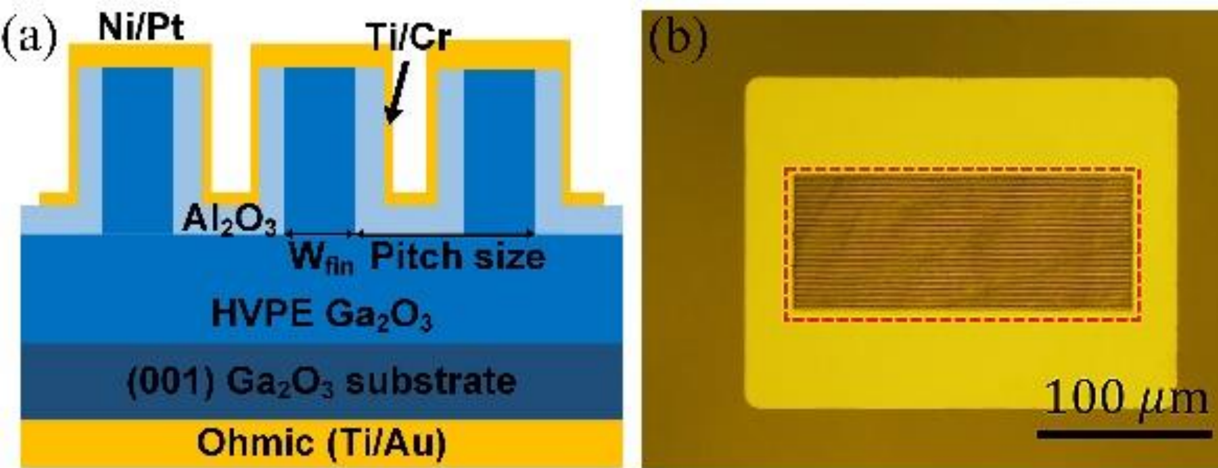

Figure 2.2 (a) Schematic of the Ga_2O_3 based trench SBDs. (b) Top-view microscope image of the fabricated Ga_2O_3 trench SBDs with a fin width of 1μm. The entire trench area enclosed by the red dashed line is used for calculating current densities for a fair comparison with regular SBDs.

formation. 1.3 µm-deep trenches were then formed using a gas mixture $BCl_3/Cl_2/Ar$ in the ICP etching with an etch rate of 87 nm/min. Patterns with various fin widths (1, 2, 3, and 4 µm) and

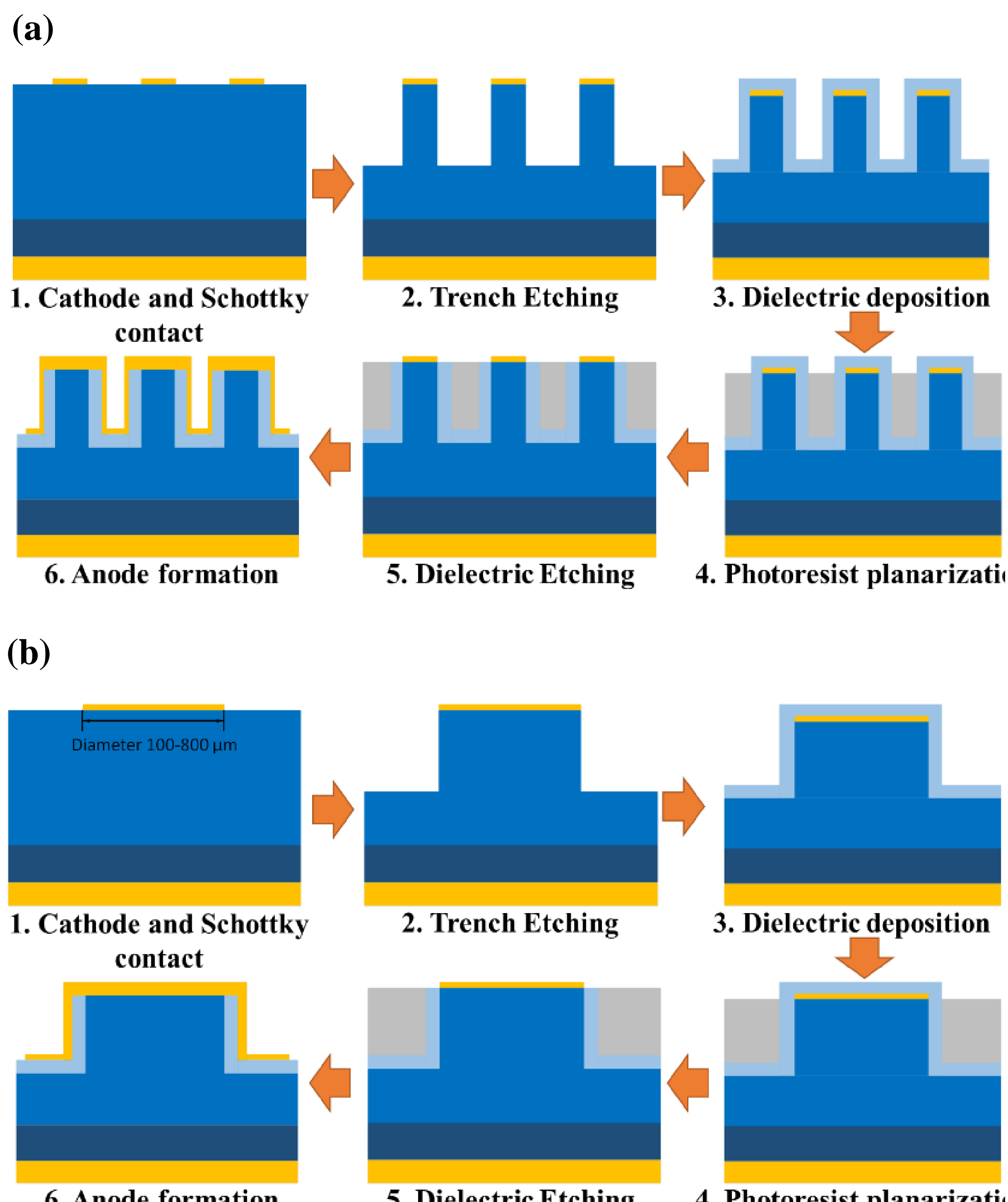

Figure 2.3 Schematic of process flows of (a) trench SBDs and (b) regular SBDs.

fin area ratios (20, 35, and 50%) were fabricated along [010] and [100] orientations. The wafer was then soaked in HCl for 10 min to remove the etch damage [65] prior to the deposition of 100 nm of Al_2O_3 at 150 °C using a plasma atomic layer deposition (ALD) system. The dielectric was then removed on top of Ni/Pt Schottky contacts using a photoresist planarization technique followed by dry etching and ashing in O_2 plasma for 1 hour to clean the byproduct of dry etching. The contact pads were formed by sputtering of Ti/Cr (10nm/300 nm) over the sidewall followed by device isolation. Regular SBDs with circular Schottky contacts were simultaneously fabricated on the same epi-structure for comparison (further details can be found in the supplementary material). The process flow for both trench and regular SBDs are demonstrated in **Fig. 2.3**. The 1×1 cm^2 sample was then diced into 4 separate dies after device fabrication was completed to enable temperature-dependent measurements, while the other dies were saved for BV measurements. This allowed us to measure and compare BV before and after stressing devices at high temperatures (up to 650 K). The fabrication process for both regular SBD and trench SBD is shown below.

I-V and Capacitance-Voltage (C-V) profiles were measured using a Keysight B1500A Semiconductor Parameter Analyzer connected to an MMR variable temperature micro probe system (VTMP) under high vacuum. BV measurements were performed using a Keysight B1505A Power Device Analyzer.

The carrier density is extracted from a linear fit to the $1/C^2$ vs V profile measured on a regular SBD with a diameter of 150 μm at temperatures ranging from 100 K to 600 K with step increment of 25 K. As shown in **Fig. 2.4**, an electron density of 3.1×10^{16} cm^{-3} was extracted at room temperature which remained relatively constant over a wide range of temperatures from 125K to 600K. All the free carriers were frozen out at temperatures below 100 K due to incomplete

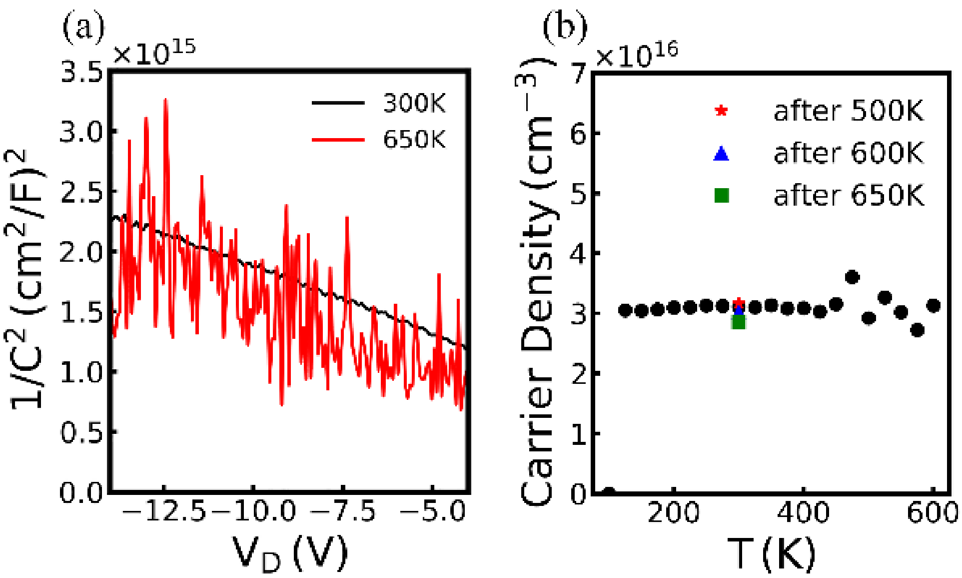

Figure 2.4 (a) $1/C^2$-V characteristic measured at 400 kHz. (b) Carrier density from C-V measurements at elevated temperatures on a regular SBD with a diameter of 150 μm.

ionization of the dopants and therefore no current could be measured at these temperatures. Fluctuations in extracted carrier density at elevated temperature (**Fig. 2.4(b)**) is due to the noisy C-V profile at these temperatures (**Fig. 2.4(a)**).

2.3 Current-voltage Characteristics

I-V profiles were measured on trench SBDs fabricated along [010] and [100] directions as well as regular SBDs. The trench SBDs fabricated in [010] direction showed superior IV characteristics, including ideality factors closer to unity and lower R_{ON}, compared to those fabricated in [100] direction. This observation is consistent with previous reported data [65]. Therefore, here we only report temperature-dependent behavior of trench SBDs fabricated along [010] direction and compare that with regular SBDs.

Figure 2.5 shows the I-V-T characteristics measured on a circular SBD with a dimeter of 150 µm and a trench SBD with a fin width of 2 µm and a fin area ratio of 20%. In comparison with regular SBDs, the trench SBDs showed slightly higher turn-on voltage (~ 0.16 V higher at 300K) due to the sidewall depletion caused by the adjacent MOS junction on the sidewalls of the trench. As temperature increased, the turn-on voltage decreased on both type of SBDs which is

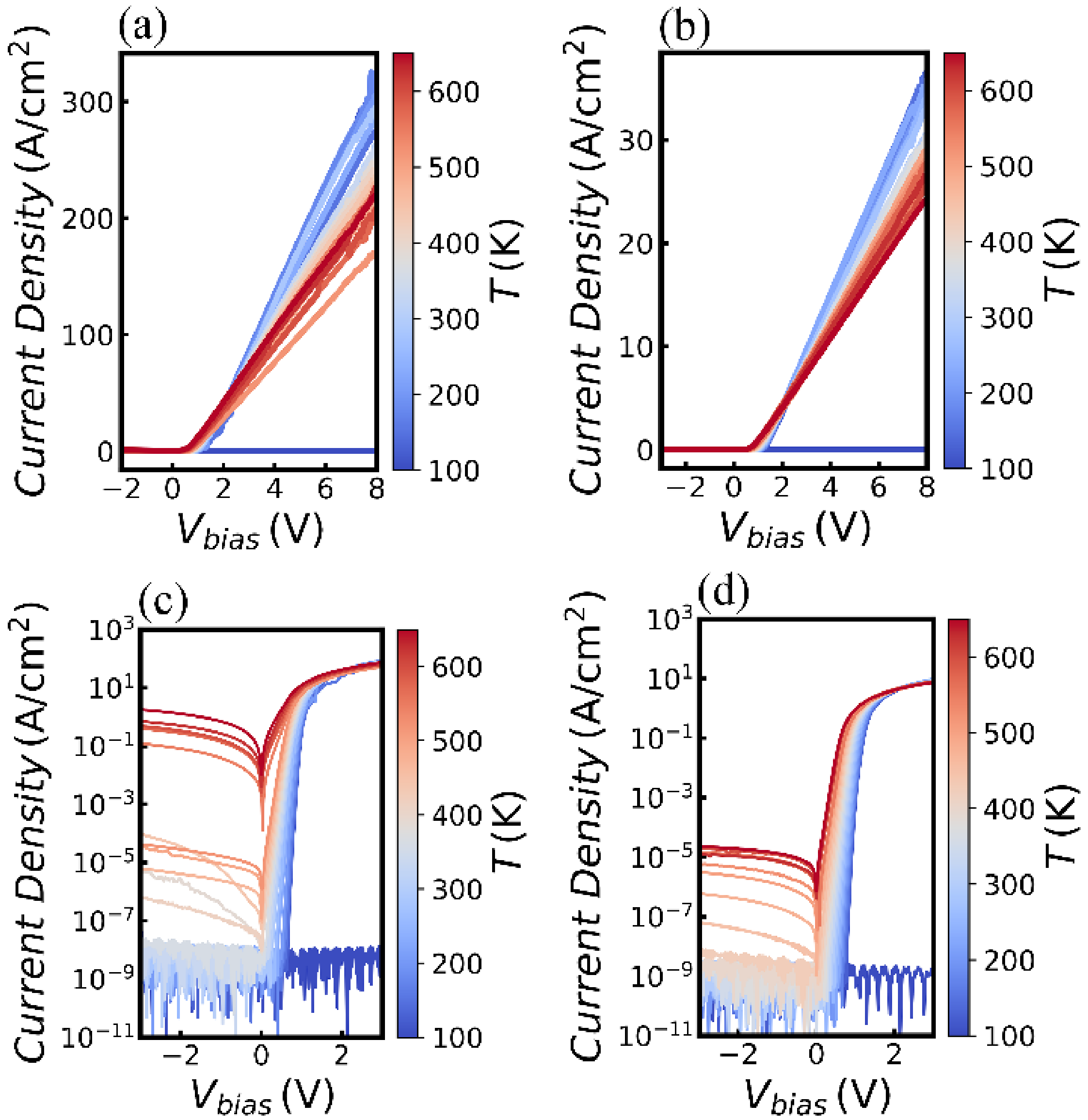

Figure 2.5 I-V-T characteristics in linear scale (top) and semi-log scale (bottom) measured on regular SBDs (left) with a diameter of 150 µm and trench SBDs (right) with a W_{fin} of 2µm and a fin area ratio of 20% at temperatures ranging from 100K to 650K with step increment of 25 K.

expected as the number of electrons with the required energy to pass over the Schottky barrier increases at higher temperatures. In the barrier-limited region (lower current density), the current density increased by increasing temperature which is expected from thermionic emission current transport. On the contrary, in the Ohmic region (higher current density), current density reduced as temperature increased because of lower electron mobilities in the current limiting series resistor at higher temperatures. The lower current densities in the trench SBD compared with that in the regular SBD is due to the restricted carrier path. Therefore, the R_{ON} of trench SBD is 210 $m\Omega/cm^2$, which is larger than that of regular SBD, 22.5 $m\Omega/cm^2$. The lowest R_{ON} achieved was 49 $m\Omega/cm^2$ which was measured on a trench SBD with fin width of 1 µm and fin ratio of 35%. The higher R_{ON} measured on our devices compared with that previously reported on trench SBDs fabricated on similar epi-structure [58] is due to (i) not annealing the ohmic contact and (ii) sputtering Cr as pad metal which has higher resistivity than Au. A large ON/OFF current ratio of 10^{10} was measured on both types of SBDs at room temperature. The leakage current remained under detection limit at high temperatures up to 550 K for trench SBDs, whereas it increased at temperatures above 350 K for regular SBDs. At 650K, the trench SBDs preserved their rectification with ON/OFF current ratio of more than 10^5, while the leakage current of regular SBD significantly increased resulting in an ON/OFF current ratio of only 10^1.

Figure 2.6 shows the leakage current measured at reverse bias of -3V as a function of temperature for regular SBDs and trench SBDs with various fin widths (1, 2, 3, and 4µm) and fin area ratio of 50%. The leakage current density on trench SBDs remains four orders of magnitude lower than that in the regular SBDs even at elevated temperatures. Similar leakage current was observed on the trench SBDs with different fin widths and the slight variation can be attributed

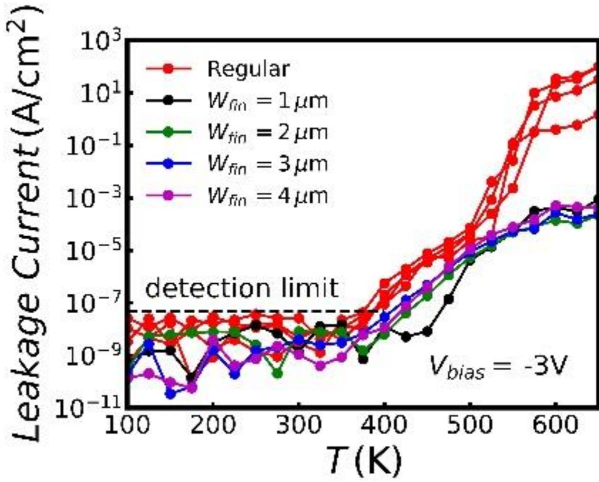

Figure 2.6 Leakage current characteristics as a function of temperature for trench SBDs with fin width of 1 µm, 2 µm, 3 µm and 4 µm and regular SBDs with diameter of 150 µm and 200 µm.

to the variations in the doping concentration and non-uniformities in the processing throughout the wafer.

The Schottky barrier height (Φ_B) and ideality factor (n) were determined assuming thermionic emission (TE) as the dominant current transport mechanism [66],

$$J = [A^* T^2 e^{-\frac{q}{kT}\phi_B}][e^{\frac{q}{nkT}(V - J \cdot A \cdot R_S)} - 1] \tag{2.2}$$

where A^* is the effective Richardson's constant, T is the absolute temperature, q is the electric charge, Φ_B is the Schottky barrier height, k is the Boltzmann's constant, and V is the applied voltage, R_S is the series resistance. Using an electron effective mass of 0.342 for β-Ga_2O_3, we assumed $A^* = 41.1\ A \cdot cm^{-2} \cdot K^{-2}$ to extract barrier height at each particular temperature [67]. **Figures 2.7 (a) and (b)** depict the linear fits to I-V characteristics measured at the entire temperature range from 100 K to 650 K and zoomed-in linear fits to I-V characteristics measured at high temperatures from 475 K to 650 K. **Figures 2.7 (b) and (c)** show the barrier height and ideality factor as a function of temperature extracted on the regular and trench SBDs under study. Ideality factors of 1.17 and 1.14 and barrier heights of 1.2 eV and 1.09 eV were extracted at room

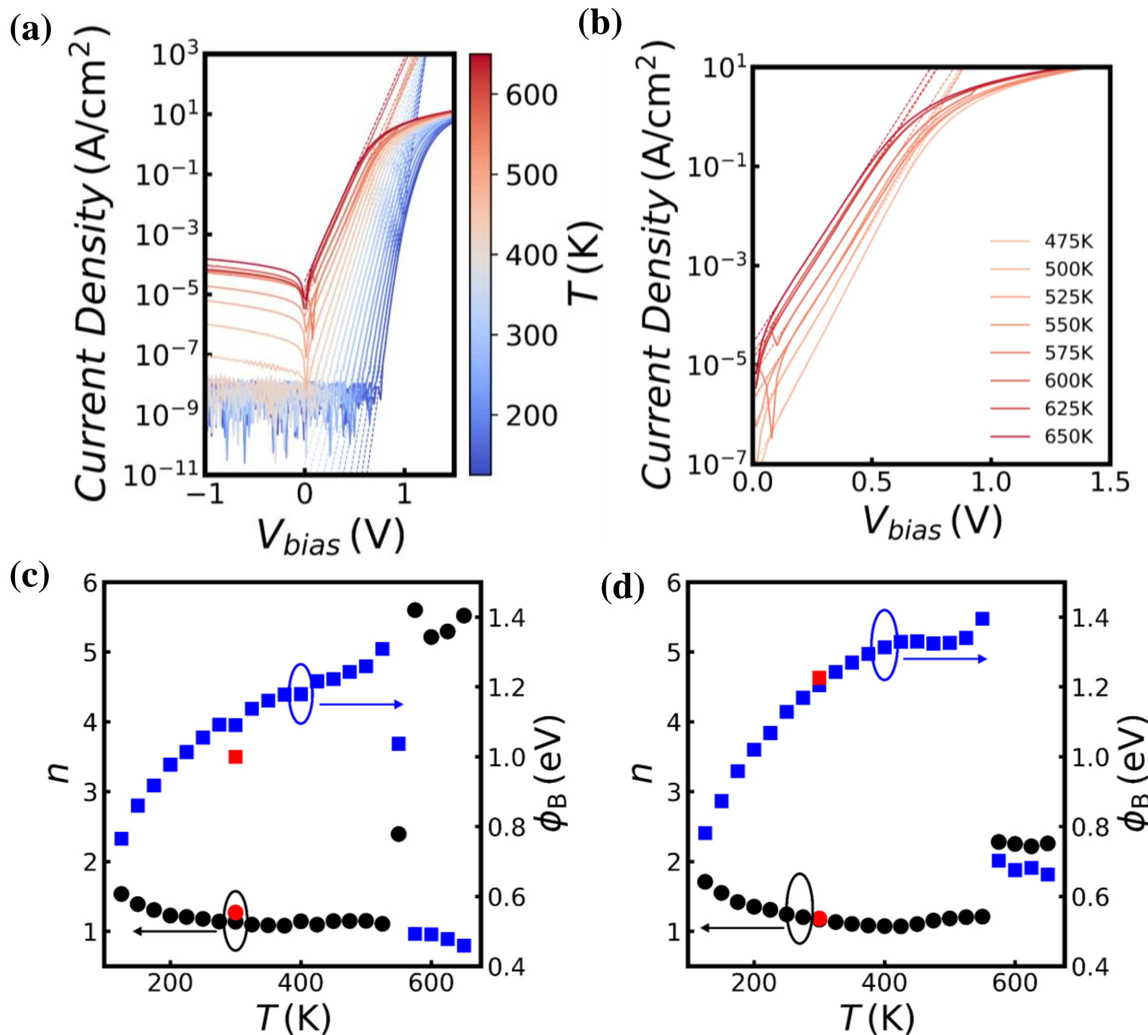

Figure 2.7 (a) Linear fit to I-V characteristics to extract ideality factor and Schottky barrier height. (b) zoomed-in linear fit to I-V characteristics measured at high temperatures from 475 K to 650K. The temperature dependence of ideality factor and Schottky barrier height are extracted for (c) regular SBD and (d) trench SBD. Red squares and dots are ideality factor and Schottky barrier height respectively extracted from I-V taken at 300K after measuring devices at temperatures up to 650K.

temperature on trench and regular SBDs, respectively. In the temperatures ranging from 100 K to 550 K, as temperature increases the ideality factor gets closer to unity and the barrier height increased from 0.8 eV to 1.3 eV. This trend has been previously observed in other semiconductor-metal Schottky contacts [68], [69] as well as Ga_2O_3-based Schottky diodes [70] and is attributed to the lateral inhomogeneity of the barrier height [71]–[73]. At higher temperatures (550K-650K),

the apparent barrier height decreased, and ideality factor increased abruptly in both regular and trench SBDs, which suggests that thermionic emission model is not valid at these temperatures and other mechanisms may be involved as well. We speculate that this could be due to the current leakage through the Al_2O_3 dielectric on the sidewall at higher temperatures. As will be discussed in the Chapter 3, Al_2O_3 deposited at 150 °C that was used for these devices is of poor quality,

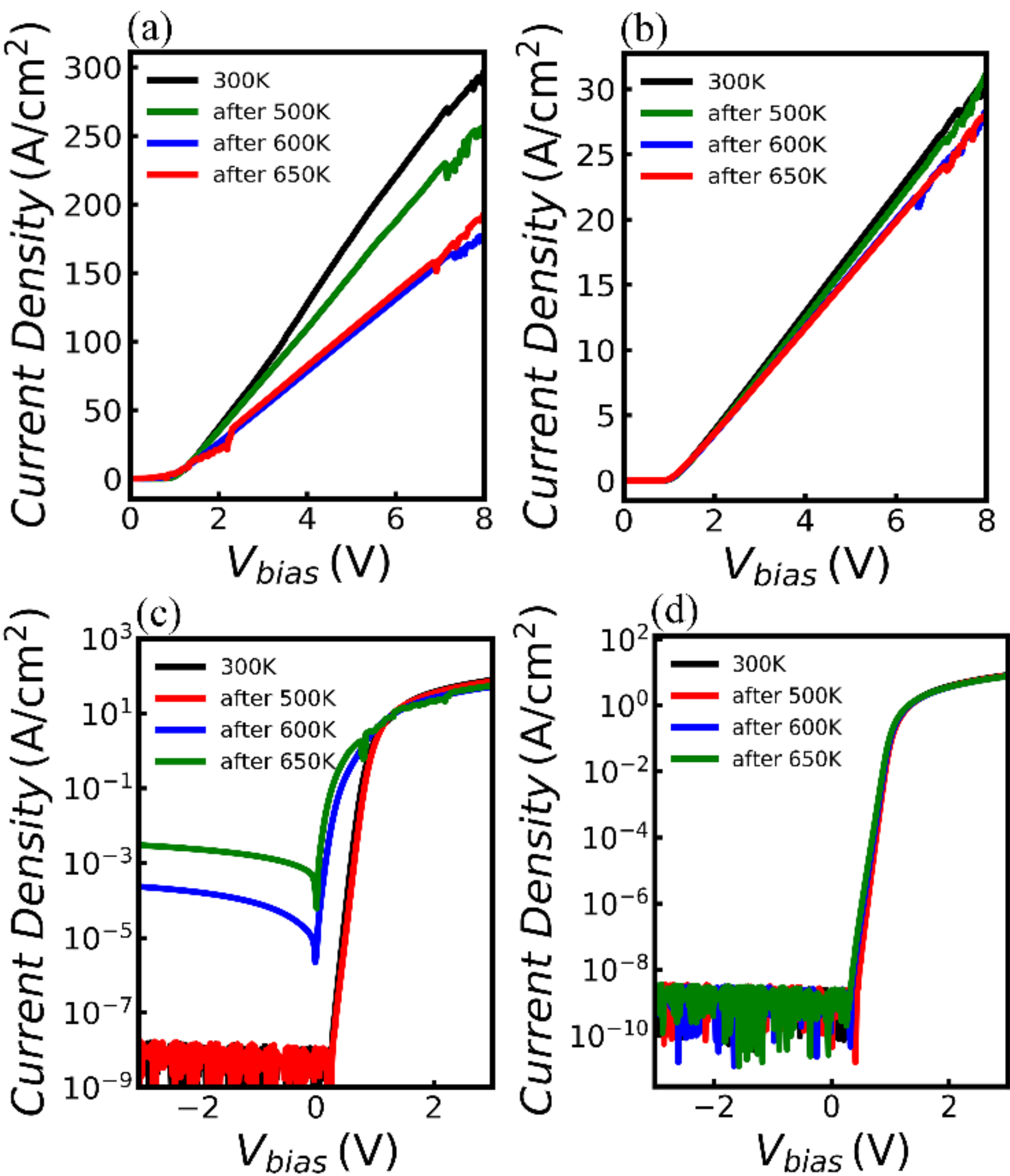

Figure 2.8 I-V characteristics in linear scale (top) and semi-log scale (bottom) taken at 300K after each temperature ramp for regular SBD (left) and trench SBD (right).

meaning the leakage current through this dielectric is very high and breakdown voltage is very low. Our studies shows that the quality of Al_2O_3 can be significantly improved by increasing the deposition temperature and post-metallization annealing.

2.4 Thermal Stability

The SBDs were measured again at room temperature after measurements were performed up to 500K, 600K, and 650K to determine whether high temperature measurements permanently affected the device performance. As shown in **Figure 2.8**, the trench SBD preserved its I-V characteristics, while the leakage current of the regular SBD increased and current density in forward bias decreased after heating up to 600 K. Reduction of forward current and an increase in leakage current after stressing device at high temperatures can be due to formation of defects in the material. Defect formation under forward bias seems to be more severe in regular SBDs compared to trench SBDs which will be the focus of a future study based on the hypothesis that the proximal trench sidewall may be sinks for defects. It is important to note that the barrier height and ideality factor did not change (red data points in **Fig. 2.7**) on the trench SBDs when devices were cooled down to room temperature after high temperature measurements, whereas the barrier height reduced on the regular SBD.

We also measured BV on several devices on the die which was used for temperature-dependent measurements as well as a separate die which had not been under temperature stress. **Figure 2.9** depicts maximum BV among all measured devices on both dies. Note that the maximum BV was achieved on the device which had not been under forward-bias stressing. A maximum BV of 1084 V was measured on the trench SBD with a W_{fin} of 1µm, which is larger than 662 V measured on the regular SBD with a diameter of 100 µm. The maximum BVs measured

after being maintained at high temperatures were lower on both types of SBDs, which suggests generation of defects along carrier path at high temperatures.

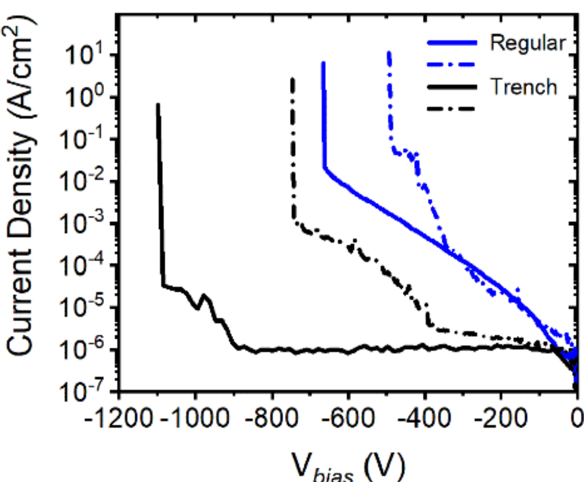

Figure 2.9 Reverse breakdown for trench SBD and regular SBD with (dash) and without (solid) high temperature ramp up to 650K. The maximum BV was extracted from trench SBD with fin width of 1µm and regular SBD with diameter of 100 µm. These devices had not been under forward-bias stressing.

2.5 Summary

In summary, the effects of temperature on the electrical characteristics of Ga_2O_3 trench and regular SBDs with Ni Schottky contacts were studied at temperatures ranging from 100 to 650K. At high temperatures, the trench SBDs maintained a high rectification ratio (10^5), which is four orders of magnitude higher than that on the regular ones. We attribute this higher thermal stability to reduced degradation under forward current stress in trench SBDs. The maximum achieved BV was reduced on both type of SBDs after temperature-dependent measurements up to 650 K.

Chapter 3 Investigation of Al_2O_3 and AlSiO Gate Dielectrics for β-Ga_2O_3

3.1 Introduction

3.1.1 Gate Dielectric

High-quality dielectrics are crucial for enabling high performance β-Ga_2O_3 FETs especially because achieving p-type conductive layer does not seem feasible for this material system. The material properties of high-quality gate dielectric include high dielectric constant, negligible gate leakage, and large breakdown field. Additionally, it must act as a barrier for both electrons and holes. As shown in **Fig. 3.1**, there are three types of band alignments: type I straddling, type II staggered, and type III broken gap. Among them, type I is the most suitable for the MOSFETs to offer adequate conduction and valence band offsets. Apart from material properties of dielectric, the interface state density (D_{it}) of dielectrics and bulk trap density (n_{bulk}) are also key performance metrics for assessment of dielectric quality. In particular, D_{it} results in the variation in the gate modulation, channel mobility and current collapse. Defects in poor dielectrics, leads to a leakage path and failure to achieve high critical breakdown field. In addition,

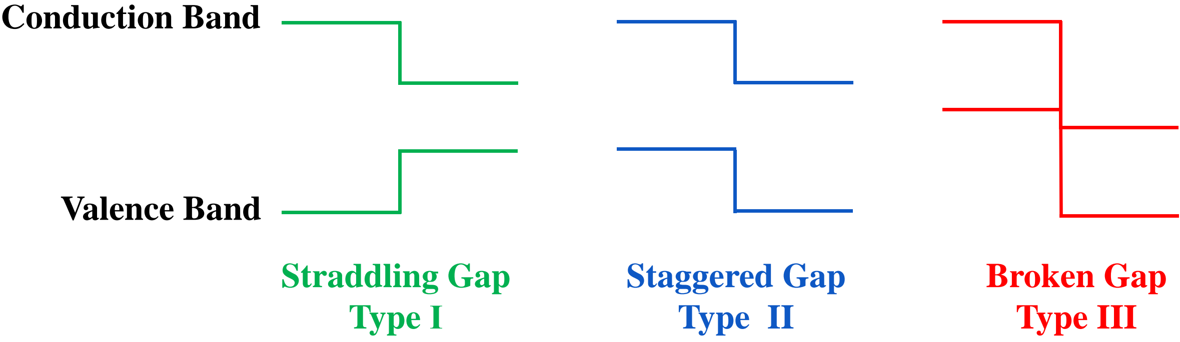

Figure 3.1 Three types of band alignment for semiconductor heterojunction.

the dielectric should be thermodynamically stable with the semiconductor and not react during processing. Moreover, many reliability issues should be considered such as threshold voltage variation, pre-mature dielectric breakdown and frequency-dependent dispersion. This dielectric degradation effects are crucial for reliable switching performance of high power devices.

In particular, given the ultra-wide bandgap of Ga_2O_3 of 4.8 eV, there are a relatively limited number of available gate dielectrics to achieve conduction band offsets ≥1eV favored for MOS structures. Currently, Al_2O_3, SiO_2, HfO_2 and their alloys or bilayer combinations are being extensively investigated in metal-oxide-semiconductor capacitors (MOSCAPs) and exploited for Ga_2O_3 based MOSFETs [43], [74]–[77]. A few studies on novel dielectrics for β-Ga_2O_3 such as ZrO_2, $LaAl_2O_3$, and $(Y_{0.6}Sc_{0.4})_2O_3$ films have been also reported, with each having different advantages over the others [78]–[80]. Further investigations on developing high-quality dielectric are still needed to improve the gate robustness of Ga_2O_3-based FETs to take advantage of its full potential.

3.1.2 Characterization Methods of Interface States

3.1.2.1 Terman method

The Terman method compares the ideal capacitance-voltage (C-V) and the low-frequency C-V curves to calculate the interface states density from the deviation of two curves. This method is valid based on the assumption that (i) the semiconductor and dielectric material are both ideal, thus their C-V response can be predicted mathematically; (ii) the low-frequency C-V curve can entirely reflect the information on interface state density. No traps are present in dielectric bulk or near interface. The Terman method has been utilized to characterize the interface state density in silicon based devices for decades. Silicon has relatively small bandgap and relatively large

minority carrier concentration which allows both the shallow and deep interface state to be ionized in manageable time scales.

Given the non-ideality of the semiconductor and dielectric materials, the deviations of their material properties from the theoretical values are not avoidable. Thus, the high-low frequency measurement is employed to replace the numerical calculated C-V curve in the Terman method. However, in the WBG and UWBG material systems with negligible hole concentration and generation rates, the trap emission time is very long at room temperature. Specifically, previous research showed the electron emission time from the state located around E_C-1.5 eV for GaN is estimated to be 10^7-10^8 years at room temperature [81]. The high-low frequency method may still be used in the WBG and UWBG system to a limited extent, as the minority carrier generation rate can increase at elevated temperatures. However, in order to create a comparable quantity of holes, the required high temperature would damage the device being tested.

3.1.2.2 AC Conductance method

This method measures the conductance change due to the charging and discharging of traps responding to the Fermi level moving above to below the energy of the trap. This method is very useful when the emission time of the trap is on the order of 10 ms (100 Hz) or shorter. When the time constant of the trap is smaller than that, only shallow traps can respond and the conductance signal becomes noisy. Similar to the Terman method, the temperature is often increased to allow for the measurement of deep traps near mid-bandgap for the WBG and UWBG material systems with the trap emission time on the order of years.

3.1.2.3 Deep Level Transient Spectroscopy (DLTS)

The deep level transient spectroscopy is a very sensitive and accurate technique which measures the change in capacitance due to changes in traps occupancy. The device under test

(DUT) is initially placed under reverse-bias (trap emptying pulse) to empty all the traps. Followed by a forward biased pulse (trap filling pulse) which results in traps capturing the carriers and getting filled. The DUT is then again placed under reverse bias (trap emptying pulse) by lowering the voltage to the initial voltage level. However, traps cannot respond to the change immediately due to its slow nature, rather emit electrons slowly over time. This results in a capacitance transient over time which can be accurately measured. By repeating this reverse-forward-reverse pulse sequence over a temperature range for different rate windows, different trap characteristics such as capture cross-section, activation energy level, and density can be extracted using Aarhenius plot. DLTS measurement is spectroscopic in nature such that it can resolve and identify traps present at different energy locations since traps at different energy location emit carriers at different rates. It can also resolve between donor and acceptor traps. Traditional DLTS is typically capacitance based on depletion region (e.g. p-n junction or Schottky diode). However, other electrical parameters such as current (I-DLTS) or voltage (CCDLTS, DDLTS) can be used to monitor the transient response resulting from change in trap occupancy. Another advantage of DLTS over AC Conductance is, while AC Conductance uses an AC frequency at a specific DC bias, DLTS generally pulses from a bias that is significantly higher than the trap energy level to a bias that is significantly lower than the trap energy. However, major disadvantage of DLTS is that it takes a long time to sweep over a large range of temperature especially for wide-bandgap devices. However UV illumination can be used to excite traps in combination with traditional DLTS method which is known as deep level optical spectroscopy (DLOS).

3.1.2.4 Deep UV-assisted Capacitance-Voltage Method

Recently, the deep ultraviolet photo-assisted capacitance-voltage (DUV-assisted C-V) was developed as an alternative technique to extract D_{it} for wide-bandgap semiconductors [82]–[85].

This method is utilized in this chapter and will be elaborated in details. Similar to the Terman method, this method tracks the change in the occupancy of the traps, enabled by the capture of electrons first from the conduction band by empty interfacial states and eventually by generated holes that accumulated at the semiconductor/dielectric interface. This technique relies on deep ultraviolet (DUV) illumination applied to devices biased in depletion to ensure all traps can be extracted from the C-V measurements. The energy of the deep UV light should be the same or large than that of the characterized semiconductor materials. The detailed procedure of this measurement will be elaborated in this chapter.

3.2 Al_2O_3 Gate Dielectric on β-Ga_2O_3 (001)

3.2.1 Motivation

High-quality gate dielectrics are critical for enabling high performance β-Ga_2O_3 FETs. As mentioned before, given the ultra-wide bandgap of Ga_2O_3 of 4.8 eV, there are a relatively limited number of available gate dielectrics to achieve conduction band offsets ≥1eV favored for MOS structures. Currently, Al_2O_3 is a most commonly used dielectric for β-Ga_2O_3 being extensively employed in Ga_2O_3-based devices due to its adequate conduction and valence band offsets. Moreover, the interfacial quality between Al_2O_3 and Ga_2O_3 has been extensively investigated and improved in various metal-oxide-semiconductor capacitors (MOSCAPs) studies. Specifically, Zeng et al. studied the D_{it} at the interface between β-Ga_2O_3 ($\bar{2}01$) and atomic layer deposited (ALD) SiO_2 using Terman method and conductance method [86]. Dong et al. exploited high-low frequency method to extract the interface state density in ALD Al_2O_3/β-Ga_2O_3(100) [77]. Using the same method, Kamimura et al. compared the interface states between Al_2O_3 and β-Ga_2O_3 in both ($\bar{2}01$) and (010) plane and showed that the interface state density in Al_2O_3/β-Ga_2O_3 ($\bar{2}01$)

are almost one order of magnitude higher than those in Al_2O_3/β-Ga_2O_3 (010) [87]. Nevertheless, the conventional Terman method, conductance method, and high-low frequency method may be limited to probing the D_{it} profile over the whole bandgap of β-Ga_2O_3 due to the long emission time of traps near valence band. Zeng et al. investigated the interface trap density of the SiO_2/β-Ga_2O_3 interface in ($\bar{2}01$), (010), and (001) orientations by the high-low frequency method with the low frequency capacitance measured via the Quasi-Static Capacitance-Voltage (QSCV) technique at high temperatures [88], [89].

DUV-assisted C-V was developed as an alternative technique to extract D_{it} for wide-bandgap semiconductors including GaN [82], [83], [85]. Using this method, several groups have studied the interface quality of various dielectrics for β-Ga_2O_3 [80], [90]–[92]. In particular, this technique was utilized to quantify the interface states in ALD Al_2O_3/β-Ga_2O_3 ($\bar{2}01$) [90], [91]. However, in these studies, the dielectric bulk traps were ignored, which may result in an inaccurate extraction of D_{it}. In addition, it is important to note that the interface states show asymmetry in different crystal planes of β-Ga_2O_3 which has a monoclinic crystal structure. Despite of many most successful Ga_2O_3-based power devices fabricated on (001) β-Ga_2O_3 using ALD Al_2O_3 as the gate barrier [43], [93]–[95], there has been no report on characterization of interface states and bulk traps in ALD Al_2O_3- (001) β-Ga_2O_3 metal-oxide-semiconductor capacitors (MOSCAPs).

3.2.2 Device Fabrication and Measurement Methods

The schematic cross-section of MOSCAPs is shown in **Fig. 3.2** [96]. MOSCAPs were fabricated on an n-type β-Ga_2O_3 (001) bulk substrate with a 9.9 μm lightly Si-doped (~5×10^{16} cm^{-3}) epitaxial layer grown by halide phase vapor epitaxy. It was shown before that etching Ga_2O_3 ($\bar{2}01$) in Piranha solution prior to the dielectric deposition reduced the density of interface states [90]. However, β-Ga_2O_3 (001) surface morphology changed and the roughness slightly increased

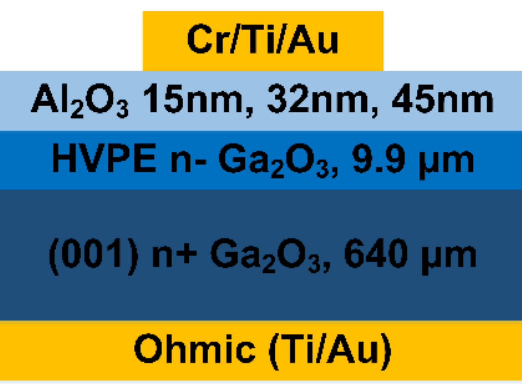

Figure 3.2 Schematic cross-section of MOSCAP structure.

by etching in Piranha as shown in **Fig. 3.3**. The samples were, therefore, soaked in 49% HF for 10 min prior to the deposition of Al_2O_3 dielectric layer. 15nm-, 32nm-, and 45nm-thick Al_2O_3 films were then deposited in ALD system using tri-methyl-aluminum (TMA) and H_2O as precursors on several samples. The ALD deposition temperature was varied from 150°C to 300°C. After dielectric deposition, post-deposition annealing (PDA) was performed at 500°C in O_2 or N_2 for 30 min. The ohmic contact on the backside of the sample was formed by a chlorine-based dry etching, followed by evaporation of Ti/Au (20/200 nm). No additional rapid thermal annealing (RTA) was performed. The circular gate contact of Cr/Ti/Au (10/20/200 nm) was then deposited and patterned via a lift-off process on the top surface.

The thickness of dielectric layer was confirmed using a J. A. Woollam M-2000 Ellipsometer. C-V measurements were performed at room temperature using a Keysight B1500A Semiconductor Parameter Analyzer. The frequency and amplitude of AC signals used for the C-V measurements were 1 MHz and 30 mV, respectively. The DC voltage was swept with a 50 mV step and a 0.6 V/s sweep rate. A 254 nm lamp with optical power density of 0.13 W/cm^2 was used as the deep UV illumination source for DUV-assisted C-V measurements.

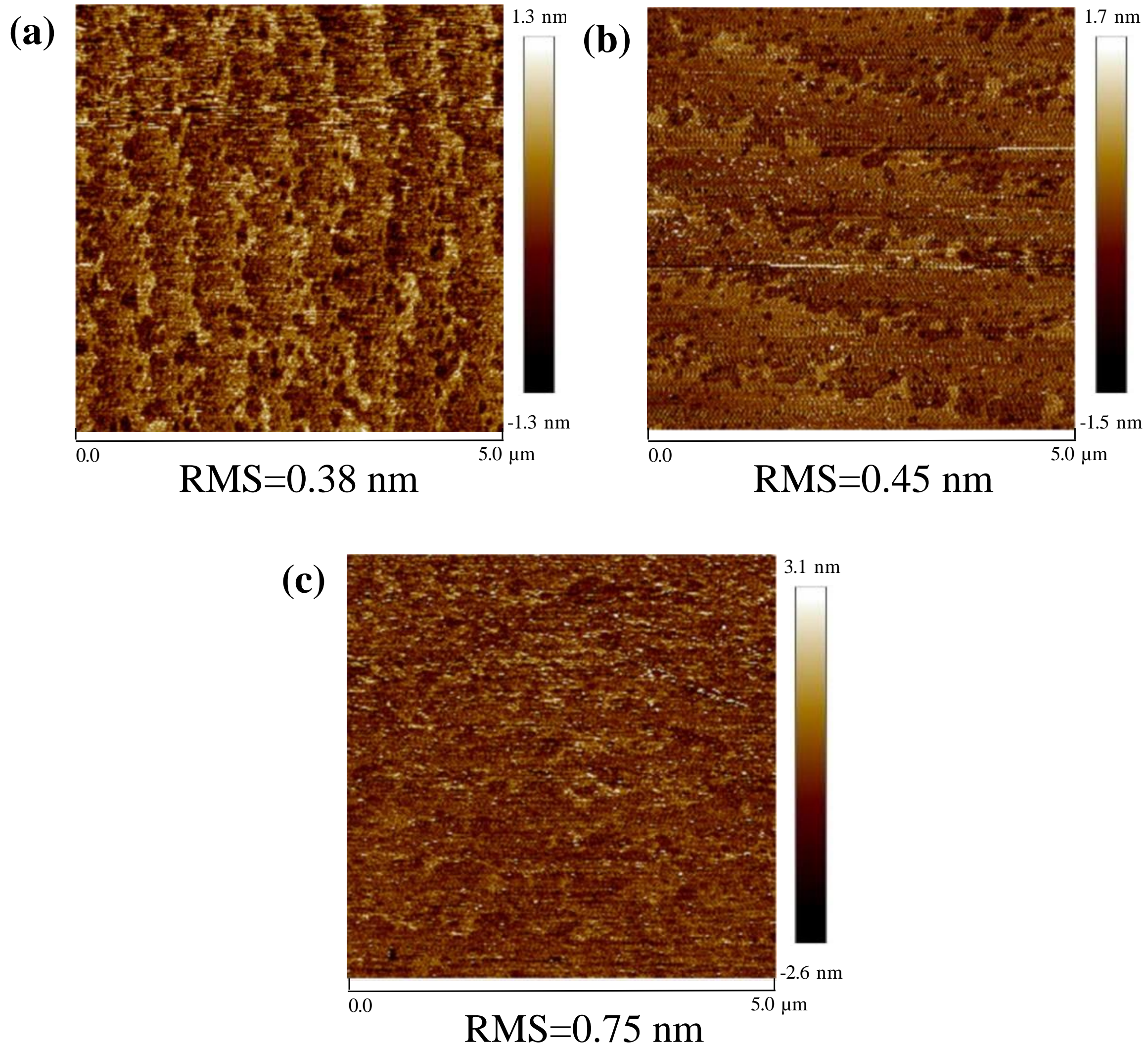

Figure 3.3 Surface morphology and RMS roughness of (a) as received sample and samples soaked in (b) HF and (c) Piranha for 90 min.

3.2.3 Impact of ALD Temperature and Post-deposition Annealing

Figure 3.4(a) shows C-V hysteresis measurements of three samples with ALD deposition temperature of 150°C, 250°C and 300°C. The gate bias was swept from -10 V to 3 V at room temperature. The Al_2O_3 thickness is 32 nm on all these three samples. Less hysteresis and higher dielectric constant were measured as deposition temperature increased. This is consistent with the finding of earlier work that showed a high deposition temperature improves the dielectric quality

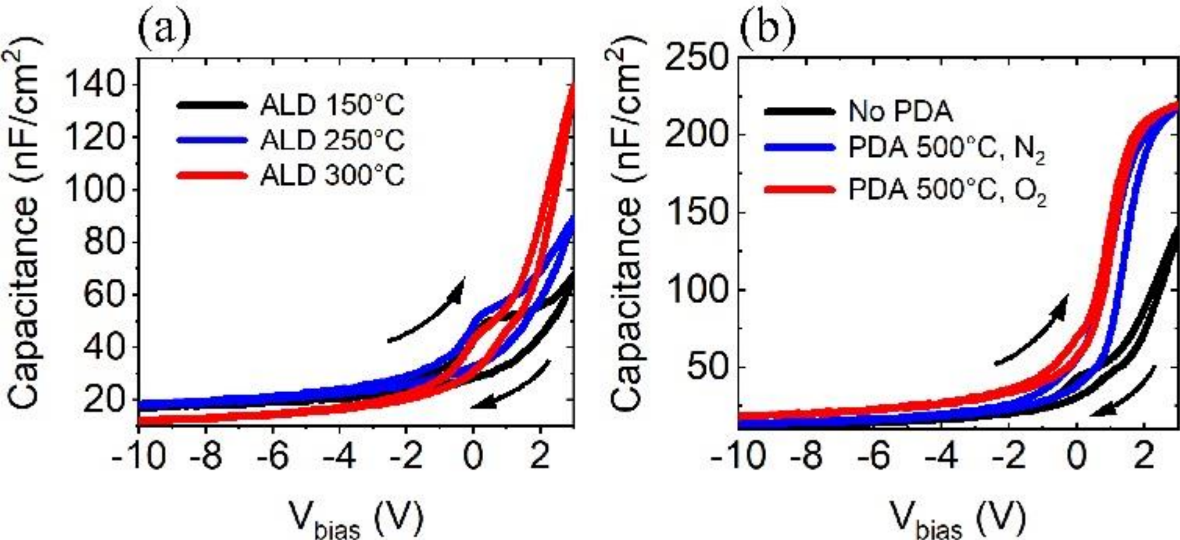

Figure 3.4 C-V hysteresis measurements of MOSCAPs at room temperature (a) with ALD deposition temperature of 150°C, 250°C and 300°C, (b) deposited at ALD 300°C, without PDA, with PDA 500°C for 30 min in N_2 or O_2.

due to formation of a thicker crystalline Al_2O_3 interlayer in the Al_2O_3/Ga_2O_3 interface [87], [97]. A ledge was observed in the C-V curves measured on samples with lower ALD deposition temperature of 150°C and 200°C, which can be attributed to bulk traps. This ledge disappeared in the C-V profile measured on sample with Al_2O_3 deposited at 300°C and the remaining hysteresis is associated with the interface states. We then studied the impact of PDA by fabricating three MOSCAPs with 32 nm thick ALD Al_2O_3 deposited at 300°C. **Figure 3.4(b)** shows that PDA at 500°C in both N_2 and O_2 significantly improved dielectric quality. A dielectric constant value of 8.7 and less hysteresis were both achieved in the MOSCAP samples with ALD deposition temperature of 300°C and PDA at 500°C in O_2 for 30 min.

Figure 3.5 summarizes forward I-V breakdown (BV) of MOSCAPs with various deposition temperatures and PDA conditions. A maximum BV of 25.3 V was measured on the MOSCAP with 32 nm-thick Al_2O_3 deposited at high temperature of 300°C (**Fig. 3.5(a)**). Compared with the MOSCAP without PDA, the BV of MOSCAPs increased when annealed in O_2 and

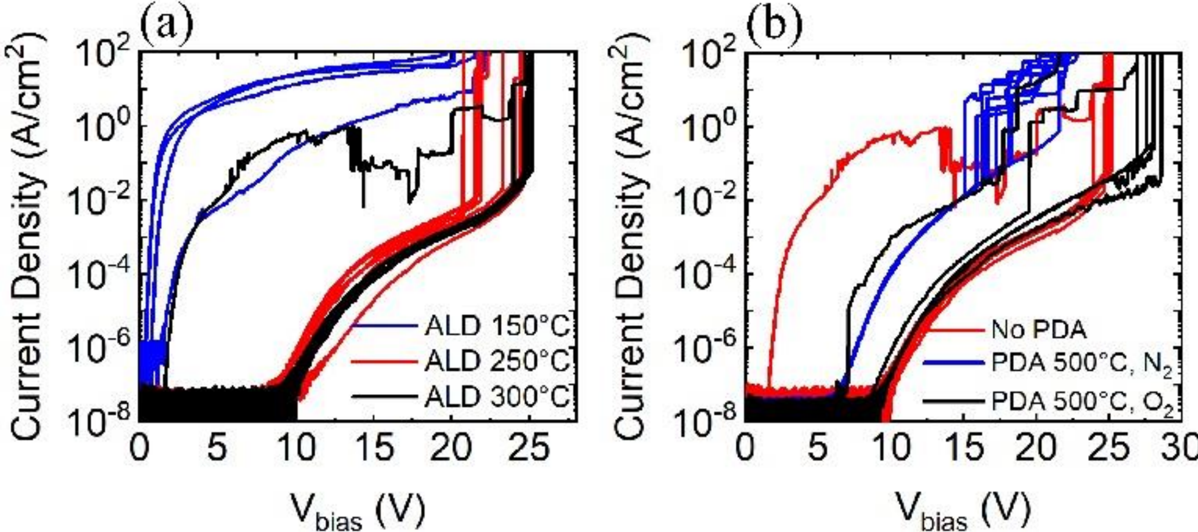

Figure 3.5 Forward I-V characteristics of MOSCAPs of (a) with ALD deposition temperature of 150°C, 250°C and 300°C, (b) deposited at ALD 300°C, without PDA, with PDA 500°C for 30 min in N_2 or O_2.

decreased when annealed in N_2, as shown in **Fig. 3.5(b)**. Previous reports [98]–[101] have shown that oxygen vacancies in as deposited Al_2O_3 film were suppressed after PDA treatment in O_2. Therefore, the observation of larger BV on samples annealed in O_2 could be due to lower oxygen vacancies. By extension, the PDA treatment in N_2 may lead to an increase in oxygen vacancies, resulting in the leakage path and reduced BV.

3.2.4 Deep UV-assisted C-V Measurement

The interface states and bulk traps were characterized by DUV-assisted C-V measurements at 1MHz frequency [85]. First, the voltage was swept from depletion to accumulation and then held for 10 min in the dark to ensure that all the traps were filled with electrons. Next, the second C-V measurement was performed in dark (indicated as "dark" in **Fig. 3.6**). The device was then held at -20 V and illuminated by 254 nm DUV for 1 min to ensure all traps were ionized. After the DUV illumination, the device was kept under depletion bias for 10 min to allow generated holes to move toward the Al_2O_3/Ga_2O_3 interface. A second C-V profile was then measured shown as red

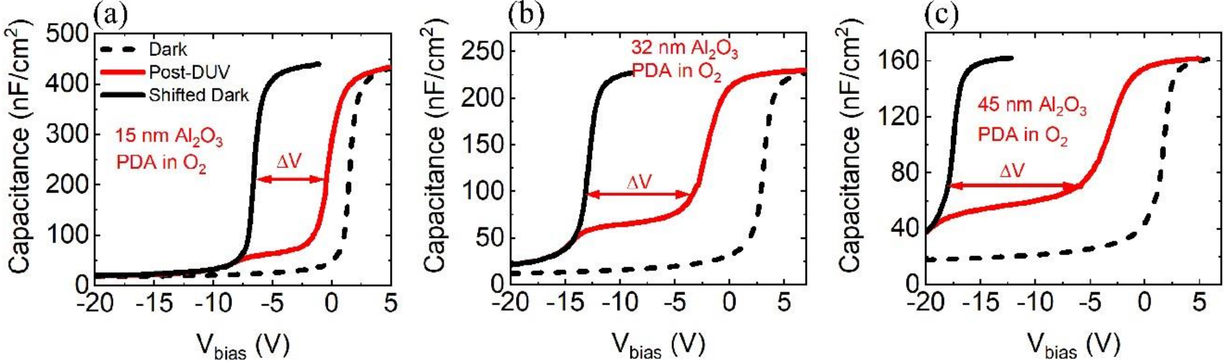

Figure 3.6 C-V characteristics of (a) 15 nm, (b) 32 nm, and (c) 45nm Al_2O_3 MOSCAPs with PDA in O_2.

curves in **Fig. 3.6**. A capacitance ledge can be observed in the post-DUV sweep (indicated as "post-UV" in **Fig. 3.6**) where interface states started being populated with electrons. The deep UV-assisted C-V measurements were performed on MOSCAPs with ALD deposition temperature of 300°C and PDA 500°C in O_2 as the lowest hysteresis was achieved among all the deposition and PDA conditions mentioned above. **Figure 3.6** shows the C-V profiles measured on various Al_2O_3 dielectric thicknesses of 15 nm, 32 nm and 45 nm. The ideal dark curve was shifted to match the capacitance value of the post-DUV curve in the deep depletion regime. ΔV is the voltage difference between the ideal dark curve and post-UV curve for a given capacitance, which is attributed to the electron captured by both interface states and bulk traps:

$$\Delta V = \frac{Aq}{C_{ox}}\left(N_{it} + \int_0^t \frac{xN_{bulk}(x)}{t}dx\right) \tag{3.1}$$

where A is the device area, q is electron charge, C_{ox} is the insulator capacitance, N_{it} is the number of captured electrons by interface states per unit area, N_{bulk} is the number of captured electrons by the dielectric bulk traps at the distance x from the metal per unit area, $\int_0^t \frac{xN_{bulk}(x)}{t}dx$ is the centroid of the charge distribution. The trap density (D_t) which is a combination of interface states and dielectric bulk traps can be calculated using the following relationship:

$$D_t = \frac{C_{ox}}{Aq}\frac{d\Delta V}{d\psi_s} = \frac{dN_{it}}{d\psi_s} + t\frac{dN_{bulk}}{2d\psi_s} = D_{it} + t\frac{n_{bulk}}{2} \tag{3.2}$$

where ψ_S is the surface potential, and can be calculated from the semiconductor capacitance and doping concentration (measured as 5.3×10^{16} cm^{-3}); D_{it} and n_{bulk} are the interface state and bulk trap. The D_t profile along with average D_t for MOSCAPs with various Al_2O_3 thicknesses are shown in **Fig. 3.7**. The extracted trap density exhibits a peak at the energy of ~0.5eV, corresponding to accumulated holes at the interface due to Al_2O_3/Ga_2O_3 valence band barrier. The rest of the charge in the D_t curve is associated with the interface states and bulk traps. The average D_t is calculated after removing the effect of accumulated holes following the technique developed by Yelluri et al [83].

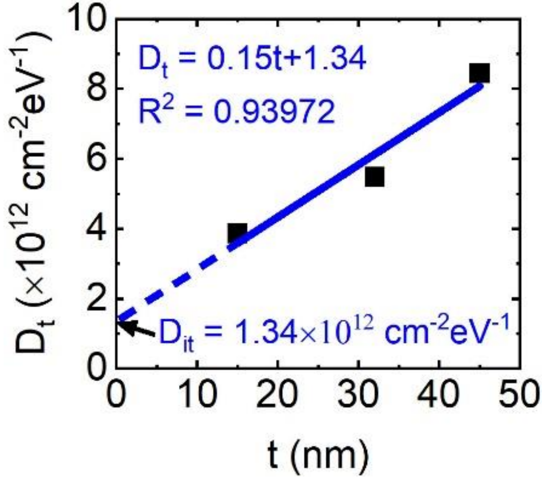

Figure 3.7 The linear fit of total trap density as a function of thickness.

Figure 3.8 shows the linear fit of average D_t as a function of dielectric thickness. Based on the physical model, an average D_{it} of 1.34×10^{12} cm^{-2}eV^{-1} was extracted from the y-intercept of the linear fit corresponding to a MOSCAP with "zero-thickness" dielectric. This interface state density measured on Al_2O_3/Ga_2O_3 (001) MOSCAPs is relatively larger than that previously measured for (010) and ($\bar{2}01$) orientations [87], [90], [91]. Previous research has shown that the formation of crystalline Al_2O_3 interlayer reduces the interface states in Al_2O_3/Ga_2O_3 interface [87]. Moreover, it is important to note that (001) is a strong cleavage plane with less surface adhesion

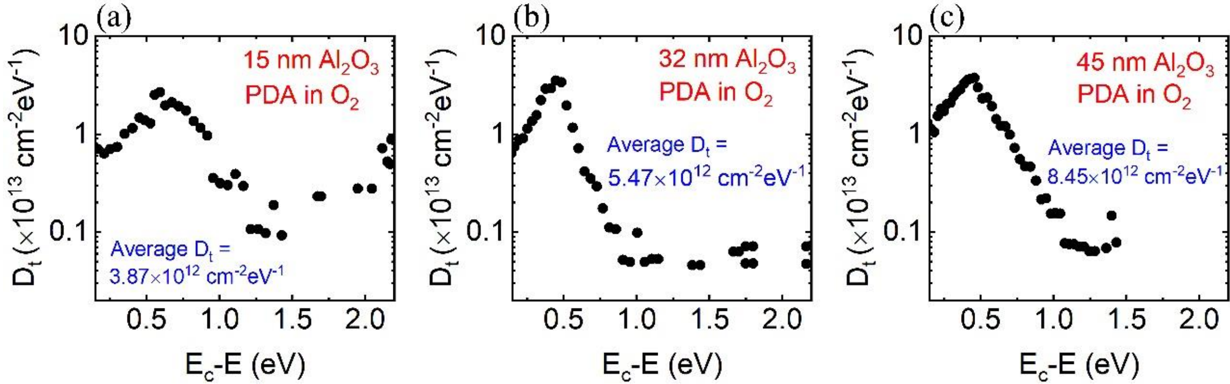

Figure 3.8 Trap density vs energy for (a) 15 nm, (b) 32 nm and (c) 45nm of Al_2O_3 MOSCAPs with PDA in O_2.

energy. Therefore, the larger interface state density in (001) orientation could be probably attributed to the less possibility of crystalline Al_2O_3 formation on the cleavage plane. Additionally, an average n_{bulk} of 2.98×10^{18} $cm^{-3}eV^{-1}$ was achieved from the slope of D_t versus thickness. This bulk trap density is demonstrated as the overall indicator for the dielectric quality.

3.3 AlSiO Gate Dielectric for β-Ga_2O_3 (001)

3.3.1 Motivation

Aluminum silicon oxide (AlSiO) has been proposed as a high-quality and reliable gate dielectric for GaN-based devices [102]–[104]. Alloying of Al_2O_3 with silicon to form amorphous AlSiO has the potential to incorporate the advantages of both SiO_2 (E_g = 9.0 eV) and Al_2O_3 (E_g = 6.7 eV) thus realizing high band offsets and high breakdown strength [103], [105]. A low interface states D_{it} of ~10^{12} cm^{-2} eV^{-1} was achieved in AlSiO on Ga-polar GaN using *metal-organic chemical vapor deposition (MOCVD) technique* and a dielectric lifetime of 20 years for electric fields higher than 3 MV/cm was predicted by Chan *et al.* [102], [106]. Chan *et al.* reported that AlSiO with a silicon composition up to 25% grown on Ga-polar GaN by MOCVD demonstrated a lower D_{it} and enhanced reliability compared to Al_2O_3 [102], [107]. Sayed *et al* studied the impact of GaN polarity and the effect of varying the Si compositions in AlSiO dielectric on the electrical

properties of MOS devices [105], [108]. Liu *et al* developed a systematic methodology to analyze the interfacial and bulk qualities of AlSiO on N-polar GaN using capacitance-voltage (C-V) methods, and showed a low D_{it} value of 4.4×10^{11} $cm^{-2}eV^{-1}$ [84], [85]. The same group also demonstrated that the post-metallization annealing of AlSiO/GaN MOSCAPs improved operation stability, reduced near-interface traps, and improved the low-leakage operation range under forward bias from 0-2.6 to 0-4 MV/cm [109]. The promising results of AlSiO as a dielectric for GaN-based devices motivated us to expand its applications to Ga_2O_3.

3.3.2 Device Fabrication

AlSiO/Ga_2O_3 MOSCAPs were fabricated on a 10 μm-thick lightly Si-doped (6.5×10^{16} cm^{-3}) Ga_2O_3 layer epitaxially grown by halide phase vapor epitaxy (HVPE) on an n+ β-Ga_2O_3 (001) substrate. Three samples were treated with three cycles of UV-ozone and 49% HF dip prior to the deposition of the AlSiO dielectric layer. One sample was treated differently, using only 49% HF, to understand the influence of UV-ozone clean on AlSiO/Ga_2O_3 interface quality. The AlSiO dielectric, with a silicon composition of 40%, was grown by metal organic chemical vapor deposition (MOCVD) in a close coupled showerhead chamber. The AlSiO deposition temperature was 700 °C, and the TMAl, Si_2H_6, and O_2 flows were 3.2 μmol/min, 3.2 μmol/min, and 4.4 mmol/min, respectively. The bandgap (E_g), conduction band offset (E_C) and valence band offset (E_V) of AlSiO (with a silicon composition of 40%) with respect to Ga_2O_3 were estimated to be 7.3 eV, 1.9 eV and 0.5 eV, respectively [110]–[112]. AlSiO with various thicknesses (10 nm, 20 nm, and 30 nm) were deposited on three different Ga_2O_3 samples treated by UV-ozone followed by an HF dip. 30 nm-thick AlSiO was deposited on the sample treated by only dipping in the HF. After the dielectric deposition, the Ohmic contact on the backside of the sample was achieved by

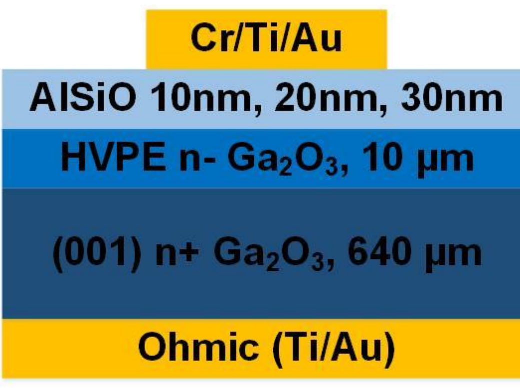

Figure 3.9 Cross-sectional schematic of the AlSiO/β-Ga_2O_3 (001) MOSCAP.

chlorine-based dry etching and following Ti/Au (20/200 nm) metal stack deposition. The circular gate contact of Cr/Ti/Au (10/20/200 nm) was then patterned on the front side of the sample. In the annealing study to improve device performance, the MOSCAPs were then annealed at 300 °C and 350 °C for 30 minutes in a vacuum chamber (~8×10^{-5} Torr).The cross-sectional schematic of a typical MOSCAP structure is shown in **Fig. 3.9**.

3.3.3 Impact of UV-Ozone Clean

To investigate the impact of UV-ozone clean on AlSiO/Ga_2O_3 properties, two dual C-V sweeps were conducted on the samples that were prepared using three cycles of UV-ozone and HF dip. In order to avoid any possible growth run-to-run variations, the two samples were co-loaded during the AlSiO deposition. The thickness of AlSiO on both samples were 30 nm. In the first C-V sweep, the voltage was swept from depletion to accumulation in the dark and then held for a 10 min electrical stress to ensure that all the near-interface slow and fast traps were filled with electrons, then the voltage was swept back to depletion. Then another C-V dual sweep was performed without electrical stress, in which only near-interface fast traps can respond. Note that fast traps can always induce hysteresis, whereas slow traps once filled would behave like fixed

charges and can no longer induce any hysteresis. This is because the emission time constant of slow traps is very long by definition. Moreover, in n-type Ga_2O_3 only a few holes are available to recombine with the trapped electr1ns due to low minority carrier generation rate in wide bandgap materials. Therefore, both near-interface fast and slow traps respond to the first C-V sweep with 10-min stress in accumulation. However, the filled slow traps remain occupied after the first C-V sweep, and only fast traps can respond to the second C-V sweep without the additional stress. The hysteresis for C-V measurement with and without stress were both higher for the sample that did not have the UV-ozone treatment as depicted in **Figs. 3.10(a) and (b)** and reported in **Table 3.1**.

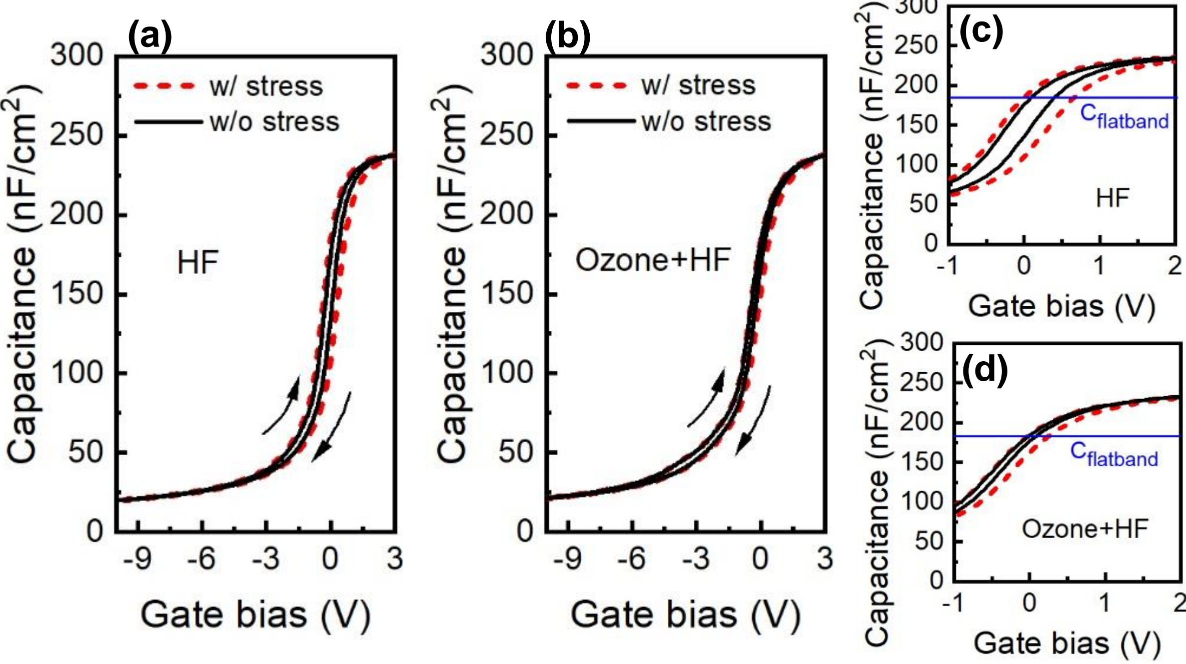

Figure 3.10 C-V sweeps of $AlSiO/Ga_2O_3$ MOSCAPs with surface pretreatment of (a) only three cycles of HF (b) three cycles of UV-ozone and HF dip. The corresponding zoom-in C-V sweeps between -1 V and 2 V are depicted for (c) only three cycles of HF (d) three cycles of UV-ozone and HF dip, respectively. The red dotted and black solid lines represent C-V sweeps with and without electrical stress for 10 minutes at an accumulation field of 1 MV/cm.

Table 3.1 Summary of hysteresis with and without stress ($\Delta V_{FB,\ w/\ stress}$ and $\Delta V_{FB,\ w/o\ stress}$), calculated near-interface fast and slow traps ($Q_{T,\ fast}$ and $Q_{T,\ slow}$), and fixed charge density (Q_F) for $AlSiO/Ga_2O_3$ MOSCAPs with surface treatment of only HF or UV-ozone and HF.

	$\Delta V_{FB,\ w/o\ stress}$ (V)	$\Delta V_{FB,\ w/\ stress}$ (V)	$Q_{T,\ fast}$ (cm^{-2})	$Q_{T,\ slow}$ (cm^{-2})
HF	0.29	0.64	4.2×10^{11}	5.1×10^{11}
HF+UV ozone	0.12	0.31	1.9×10^{11}	3.0×10^{11}

The corresponding zoom-in C-V sweeps between -1 V and 2 V for $AlSiO/Ga_2O_3$ MOSCAPs with surface pretreatment of (a) only three cycles of HF (b) three cycles of UV-ozone and HF are shown in **Figs. 3.10(c)** and **3.10(d)**, respectively.

The hysteresis ΔV_{FB} is defined to be the voltage shift between forward and reverse sweep at flatband capacitance (C_{FB}). C_{FB} is [113]

$$C_{FB} = \frac{1}{\frac{t}{\epsilon_0\epsilon_r}+\frac{L_D}{\epsilon_0\epsilon_s}} \tag{3.3}$$

where t is the dielectric thickness, and ϵ_0, ϵ_r are the vacuum permittivity and relative dielectric constant of AlSiO (measured to be 7.85), respectively. ϵ_s is relative permittivity of Ga_2O_3. L_D is the Debye length, which could be obtained by the equation [113]

$$L_D = \sqrt{\frac{\epsilon_0\epsilon_s kT}{N_d q^2}} \tag{3.4}$$

where k is Boltzmann constant, T is the measurement temperature, N_d is the doping of semiconductor (~ 6.5×10^{16} cm^{-3}), q is the electron charge. The density of near-interface traps close to the conduction band edge density Q_T can then be calculated by [84]

$$\Delta V_{FB} == \frac{qQ_T}{C_{OX}} = \frac{qQ_T}{\epsilon_0\epsilon_r}t \tag{3.5}$$

The calculated near-interface slow and fast trap density are summarized in **Table 3.1**. A combination of repeated UV-ozone and wet chemical treatment suppressed the fast and slow near-

interface traps significantly. This reduction in the density of near-interface traps suggests a cleaner surface with less defects due to the oxidation and removal of surface contaminants by a combination of UV-ozone and HF dip prior to the dielectric deposition [114]. Similar results were found previously on Ga-polar GaN high-electron mobility transistors (HEMT) with reduced current collapse by ozone oxidation and wet surface treatment before Si_3N_4 passivation [115].

A series of AlSiO/Ga_2O_3 MOSCAPs with 10 nm-, 20 nm- and 30 nm-thick AlSiO thicknesses were then fabricated in order to extract density of fixed charge, near-interface traps and density of interface states close to the conduction band edge, following the methodology in ref. [84]. A combination of UV-ozone followed by HF dip was employed as surface pretreatment prior to dielectric deposition for all these samples. The ΔV_{FB} values and the linear fit are plotted in **Fig. 3.11(a)**. The fact that the linear fit passes through the origin confirms that the measured fast/slow traps are at or near the dielectric interface. The fast trap density was extracted to be 2.18×10^{11} cm^{-2}, and the slow trap density excluding the contribution from fast traps was calculated

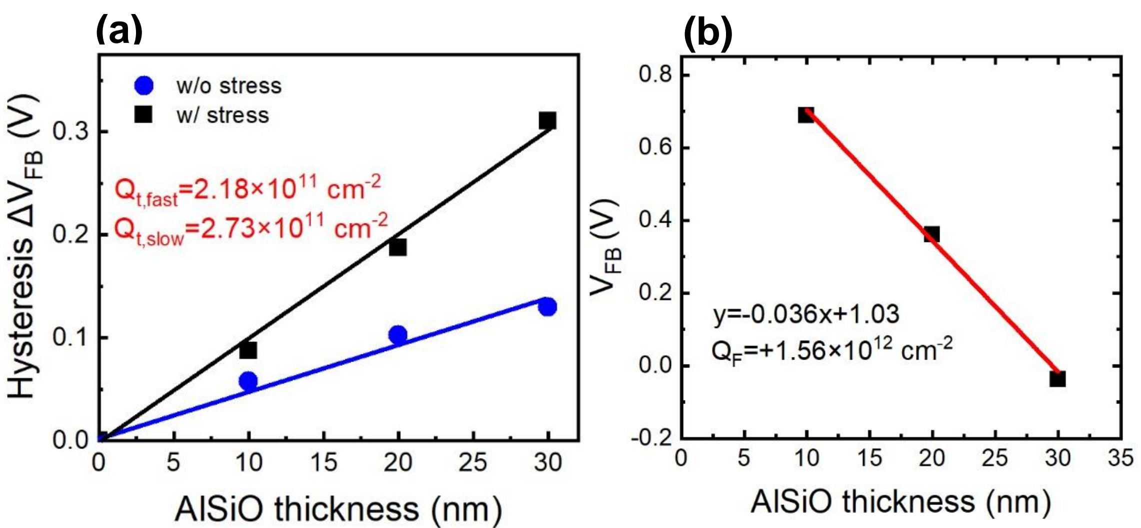

Figure 3.11 (a) Hysteresis ΔV_{FB} with and without stress, and (b) V_{FB} as a function of AlSiO thickness measured on AlSiO/Ga_2O_3 MOSCAPs.

to be 2.73×10^{11} cm^{-2} from the fitting slope and using **Eq. (3.5)**. Assuming negligible charges in the dielectric, the flat band voltage is given by [116],

$$V_{FB} = -\frac{qQ_F}{\epsilon_0\epsilon_r}t + \Phi_{MS} \tag{3.6}$$

where V_{FB} is the flatband voltage, Q_F is the net charge at the AlSiO/Ga_2O_3 interface, Φ_{MS} is the work function difference between metal and semiconductor. From the V_{FB}-thickness relationship shown in **Fig. 3.11(b)**, a net positive fixed interface charge of 1.56×10^{12} cm^{-2} was extracted from the fitting slope using **Eq. (3.6)**.

3.3.4 Interface States of AlSiO/Ga_2O_3

Figs. 3.12(a)-(c) shows the DUV-assisted C-V characteristics (left) and corresponding trap density (D_t) as a function of energy (right) for the MOSCAPs with 10 nm-, 20 nm-, and 30 nm-thick AlSiO, respectively. In these figures, the ideal dark curve was shifted to match the capacitance value of the post-UV curve in the deep depletion regime. This shift is caused by captured and accumulated holes at the interface and bulk dielectric. The trap density (D_t), which is a combination of interface states and dielectric bulk traps, was calculated

Average D_t for various thicknesses of AlSiO was calculated. **Figure 3.12(d)** shows the linear fit of average D_t as a function of AlSiO thickness. An average D_{it} of 6.63×10^{11} cm^{-2} eV^{-1} and n_{bulk} of 4.65×10^{17} cm^{-3}eV^{-1} were extracted from the y-intercept and slope of the linear fitting to **Eq. (3.2)**, respectively. This interface state density is approximately half of the D_{it} value that was measured using the same technique on ALD Al_2O_3 deposited on (001) Ga_2O_3 MOSCAPs fabricated by our group [96]. It is worth noting that in deep UV-assisted C-V measurements, bulk hole traps can be ionized via (i) exciting electrons from the trap to the conduction band and (ii) by generated holes in Ga_2O_3 tunneling and hopping through the traps.

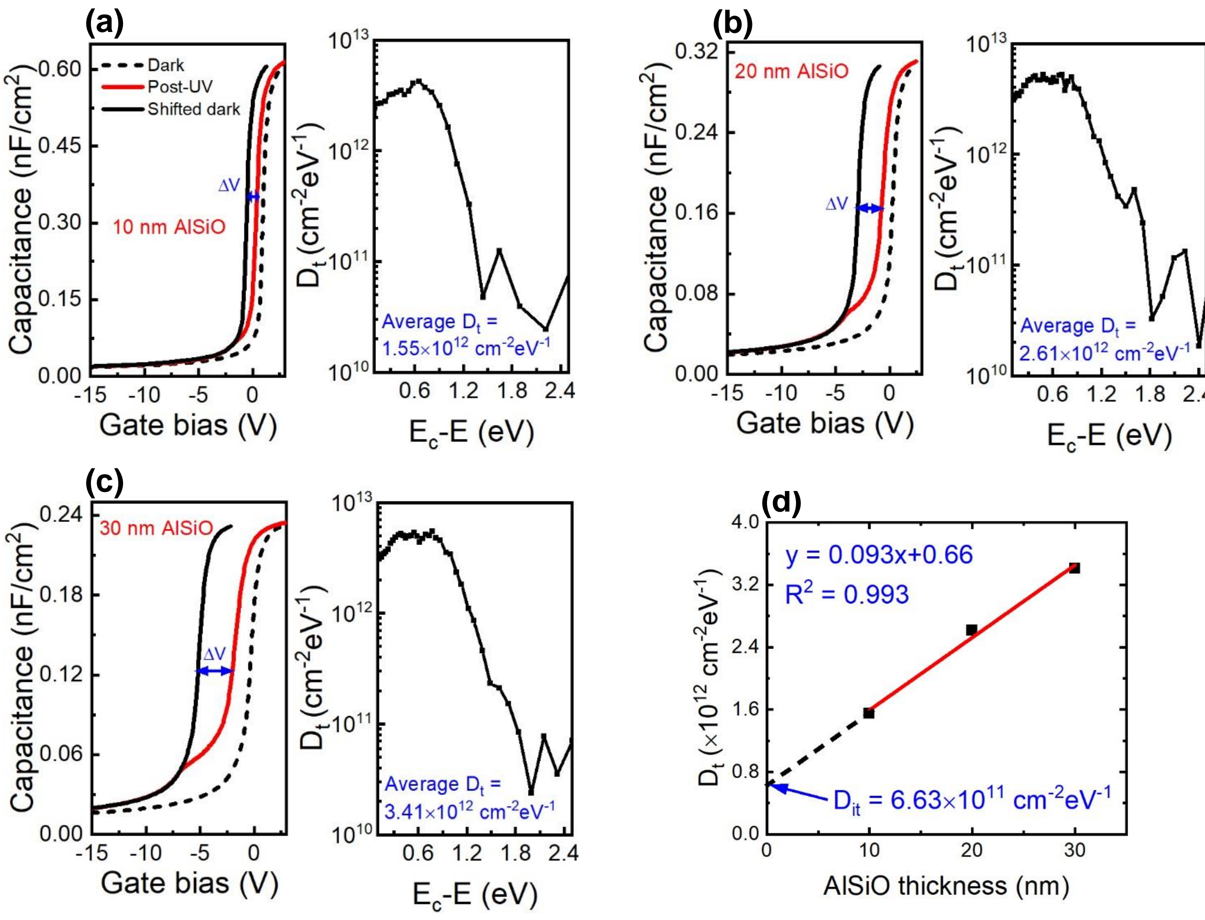

Figure 3.12 The measured C-V curves (left) and corresponding D_t profile (right) for (a) 10 nm-, (b) 20 nm-, and (c) 30 nm-thick AlSiO/Ga_2O_3 MOSCAPs. (d) The linear fit of average trap density as a function of AlSiO thickness. The y-axis intercept and slope correspond to the interface density (D_{it}) of 6.63 $\times 10^{11}$ cm^{-2} eV^{-1} and the bulk trap density (n_{bulk}) of 4.65×10^{17} cm^{-3} eV^{-1}.

3.3.5 Breakdown Voltage Comparison Between AlSiO and Al_2O_3

Figure 3.13 compares the forward breakdown voltage (BV) characteristics of 30-nm AlSiO/Ga_2O_3 MOSCAPs with our previous studies on ALD Al_2O_3/Ga_2O_3(001) MOSCAPs [96]. The avalanche breakdown occurred at ~7.8 MV/cm for both AlSiO and Al_2O_3 dielectrics. An operation range of ~3.7 MV/cm was achieved on AlSiO dielectric beyond which the leakage current was more than the detection limit current level (~ 5×10^{-8} A/cm^2). This value is larger than the corresponding value (~3.1 MV/cm) that was measured for the ALD-Al_2O_3. At electric fields

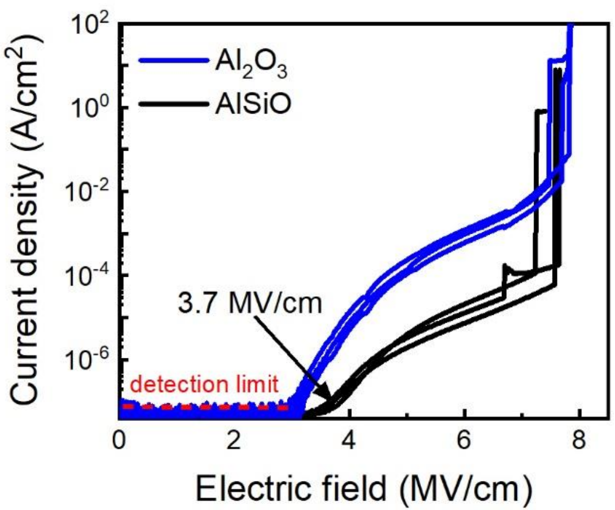

Figure 3.13 Forward-bias current-voltage characteristics of ALD-Al_2O_3/Ga_2O_3 and

above 4 MV/cm and below the BV, the AlSiO/ Ga_2O_3 MOSCAP exhibited two orders of magnitude lower gate leakage than that of ALD-Al_2O_3/Ga_2O_3 MOSCAPs. This lower leakage current could be attributed to the higher conduction band offsets of AlSiO (ΔE_C (AlSiO) = 1.9 eV, ΔE_C (Al_2O_3) = 1.5 eV) [110], [111], reduced field-induced trap generation and possible reduction of electron hopping from the Ga_2O_3 to the gate metal [109]. The promising results demonstrated in this paper show the potential for using AlSiO as high performance and more reliable gate dielectric for Ga_2O_3-based FETs.

3.3.6 Impact of Post-metallization Annealing

The impact of PMA on the forward operational reliability of AlSiO/Ga_2O_3 MOSCAPs was explored through step-stress C-V measurements, as depicted in **Fig. 3.14(a)-(c)** [117]. The AlSiO thickness was 30 nm for all the tested devices. First, the initial depletion-accumulation (D>A) C-V sweep was measured from -15 V to 2V and considered as a reference curve. Then the MOSCAP was stressed at a forward bias voltage for 10 seconds, and immediately swept backward from accumulation to depletion (A>D). The forward stress voltage was varied from 2 V to 15 V

sequentially, which corresponds to electric fields from 0.67 MV/cm to 5 MV/cm. The electric field (E_{field}) was calculated by gate bias divided by the dielectric thickness, assuming E_{field} is uniform inside dielectric. Flat-band voltage was calculated at flat-band capacitance of each C-V sweep, following Jian *et al.* [118]. The hysteresis (ΔV_{FB}) is the flat-band voltage difference between each A>D curve and the reference D>A curve. The relationship between extracted ΔV_{FB} and forward

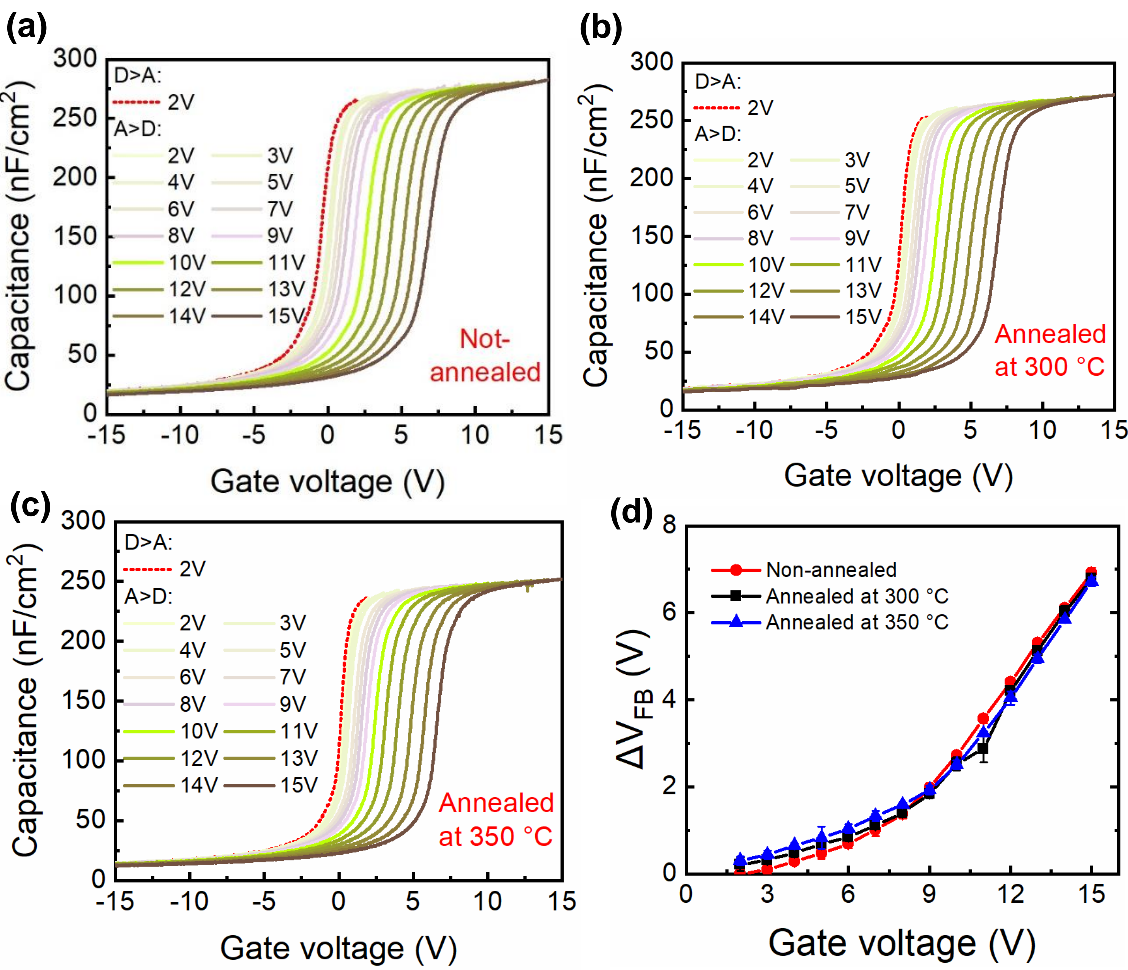

Figure 3.14 Forward step-stress C-V profiles of 30 nm $AlSiO/Ga_2O_3$ MOSCAPs: (a) not-annealed, (b) annealed at 300 ºC, and (c) annealed at 350 °C. The maximum accumulation voltage was increased for each sweep from 2V to 15V by a step voltage of 1 V. (d) Corresponding flat-band hysteresis ΔV_{FB} versus applied forward stress for 10 seconds. The depletion-accumulation (D > A) C-V curve from 2V to -15V was identified as a reference for accumulation-depletion (A > D) C-V profiles and ΔV_{FB} calculation.

stress voltage for five devices with and without PMA is shown in **Fig. 3.14(d)** statistically. No significant change of ΔV_{FB} between not-annealed and annealed samples was observed. The ΔV_{FB} increased with increasing the stress voltage on all three samples. Specifically, the ΔV_{FB} increased slightly up to 2 V at the forward stress of 9 V (3 MV/cm). Beyond the critical stress of 3 MV/cm, the ΔV_{FB} increased at a higher speed and reached to ~7V at a forward stress of 5 MV/cm. This trend of positive flat-band voltage shift suggests the existence of negative charge trapping in the dielectric dependent of the applied DC positive bias under accumulation region. Significant charge trapping occurring at high-field stress suggests electrons tunneling and hopping into the dielectric [119]. Note that the maximum stress field of 5 MV/cm in our study is approximately four times larger than that applied to the gate in vertical β-Ga_2O_3 Fin-FET on-state operation [43].

Figure 3.15 (a)-(c) shows typical reverse step-stress results for 30 nm AlSiO/Ga_2O_3 MOSCAPs. The reference A>D curve was swept from 5 V to -10 V. The following D>A C-V sweeps were taken after the gate bias was held at a negative depletion voltage for 3 minutes and then swept back to 5 V. The reason for non-uniform stress periods for forward and reverse bias is that the semiconductor shared the electric field partially when MOSCAP was biased at the reverse region, whereas, the dielectric withheld most of the electric field when the device was biased at the forward region. Therefore, the reverse bias has less stressing impact on the dielectric and the longer stress period was needed for reverse stability test to make the C-V flat-band voltage shifts more visible. The negative depletion bias was increased for each C-V sweep from -10V to -42 V by a step voltage of -2 V. The ΔV_{FB} is the voltage difference between measured D>A curve and reference A>D curve. The extracted ΔV_{FB} as a function of reverse stress voltage for five devices is illustrated in **Fig. 3.15(d)**. The hysteresis value reduced as annealing temperature increased. For the sample not-annealed or annealed at 350 °C, the ΔV_{FB} was almost stable until the reverse voltage

extended to ~-36 V and then the ΔV_{FB} changed significantly with increasing the voltage stress. On the other hand, the C-V sweeps of sample with PMA at 300 °C were almost identical to each other and ΔV_{FB} was stable until the reverse stress reached to -38V. Only slight increase in ΔV_{FB} was observed at reverse stress of -40 V and -42 V. This behavior is probably attributed to the reduction of defects/mobile ions at the interface and dielectric due to PMA at 300 °C. It should be mentioned that the accumulation capacitance of samples treated with PMA at 300 °C and 350 °C

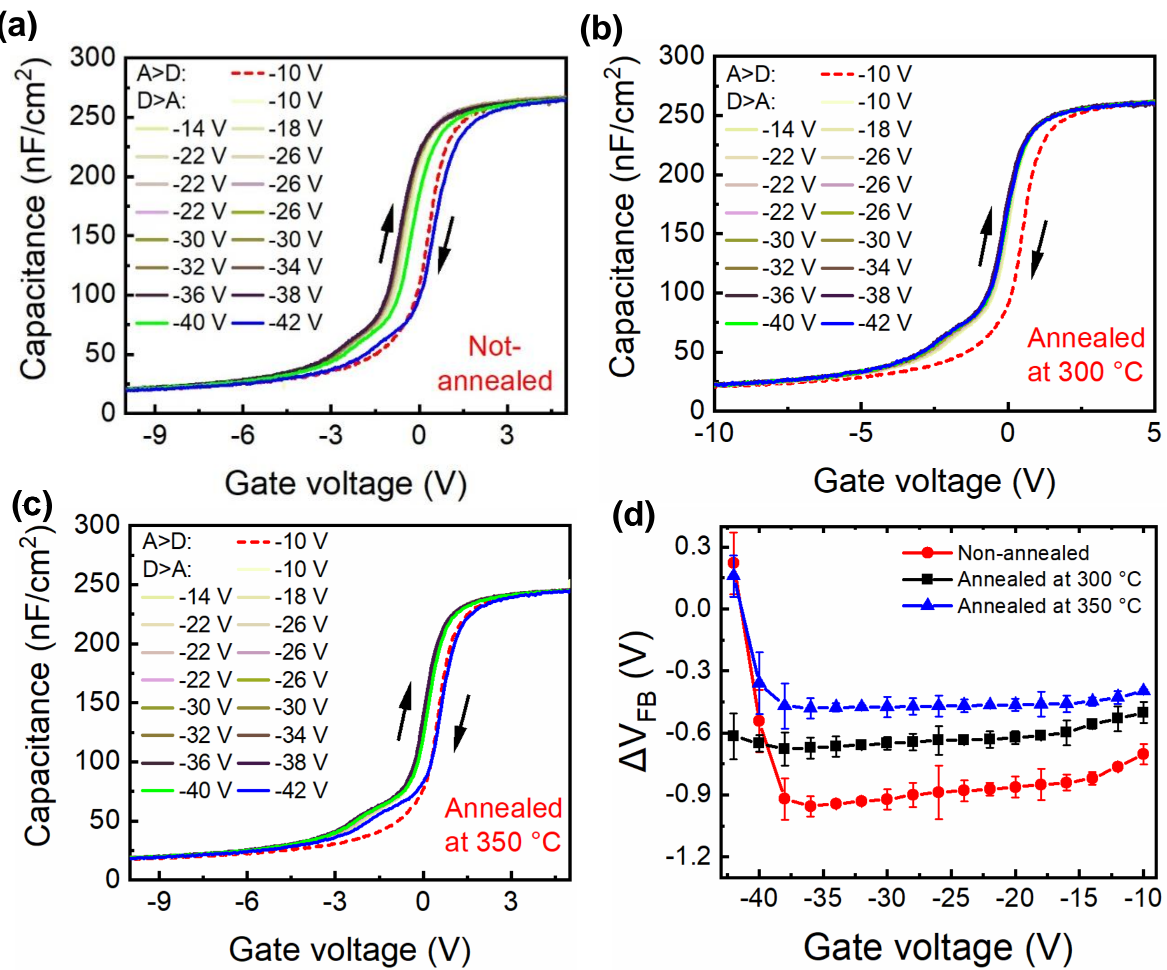

Figure 3.15 Reverse step-stress C-V profiles of 30 nm AlSiO/Ga_2O_3 MOSCAPs: (a) not-annealed, (b) annealed at 300 °C, and (c) annealed at 350 °C. The maximum depletion voltage was decreased for each sweep from -10V to -42V by a step voltage of -2 V. (d) Corresponding flat-band hysteresis ΔV_{FB} versus applied reverse stress for 3 minutes. The accumulation-depletion (A > D) C-V curve from 5V to -10V was identified as a reference for depletion-accumulation (A > D) C-V profiles and ΔV_{FB} calculation.

decreased from 265 nF/cm^2 (not-annealed) to 261 nF/cm^2 and 245 nF/cm^2, respectively. This decrease in accumulation capacitance can be explained by a dielectric degradation with lower dielectric constant probably due to the gate metal (Cr/Ti/Au) diffusion into dielectric during PMA at higher temperature [120]–[122].

To further explore the impact of PMA on the interface states near the conduction band edge, two C-V dual sweeps were conducted. In the first C-V sweep, the gate voltage was biased from depletion to accumulation, then held at accumulation for a 10 min stress prior to sweeping back to depletion. Since the first C-V sweep contains a stress, the measured hysteresis is associated with the behavior of both the slow and fast trap near the conduction band edge [109]. Next, another dual C-V sweep was performed without an electrical stress; the gate voltage was swept from depletion to accumulation and then immediately back to depletion, in which the slow traps were maintained occupied and only fast traps could respond. ΔV_{FB} extracted from the C-V measurements and calculated near-interface fast and slow traps are depicted in **Table. 3.2** for 30 nm AlSiO/Ga_2O_3 MOSCAPs. Annealing at 300 °C and 350 °C decreased both hysteresis values with and without electrical stress. Compared to sample without PMA treatment, the density of fast and slow traps was reduced by 68% and 6.7% for the sample with PMA at 300 °C. This decrease in the density of near-interface traps suggests that annealing reduced the interface defects or dangling bonds similar to our previously report on hysteresis reduction at the interface between

Table 3.2 Summary of hysteresis with and without stress ($\Delta V_{FB,\ w/\ stress}$ and $\Delta V_{FB,\ w/o\ stress}$), calculated near-interface fast and slow traps ($Q_{T,\ fast}$ and $Q_{T,\ slow}$) for not-annealed, annealed at 300 ºC and 350 °C AlSiO/Ga_2O_3 MOSCAPs. The AlSiO thicknesses were 30 nm.

	$\Delta V_{FB,\ w/o\ stress}$ (V)	$\Delta V_{FB,\ w/\ stress}$ (V)	$Q_{T,\ fast}$ (cm^{-2})	$Q_{T,\ slow}$ (cm^{-2})
Not-annealed	0.12	0.31	1.9×10^{11}	3.0×10^{11}
Annealed at 300 °C	0.05	0.23	5.6×10^{10}	2.8×10^{11}
Annealed at 350 °C	0.06	0.26	7.5×10^{10}	3.1×10^{11}

Al_2O_3 and (001) β-Ga_2O_3 [96]. It is noted that PMA at higher temperature of 350 °C resulted in less reduction in the density of near-interface fast traps and slight increase in slow traps with respect to PMA at 300 °C.

Figure 3.16(a) depicts the D_t as a function of energy for samples with and without PMA measured via deep UV assisted C-V methodology. **Figure 3.16(b)** shows the calculated average D_t statistics for samples with and without PMA. The average D_t was calculated for energy below E_C-0.15 eV, where the depletion capacitance dominates. The results show that, PMA at 300 °C reduced the density of traps occupying energy levels over the range of 0.15-1.5 eV away from the Ga_2O_3 conduction band. The average D_t for sample with PMA at 300 °C was calculated to be 3.06×10^{12} cm^{-2} eV^{-1}, which was smaller than the average D_t of 3.56×10^{12} cm^{-2} eV^{-1} calculated for not-annealed samples. PMA at 350 °C was found to increase the density of traps, which suggests a slightly degraded AlSiO/Ga_2O_3 interface and bulk dielectric.

Next, a series of AlSiO/Ga_2O_3 MOSCAPs with 10 nm-, 20 nm- and 30 nm-thick AlSiO thicknesses were annealed at 300 °C to characterize the interface states and bulk traps by deep

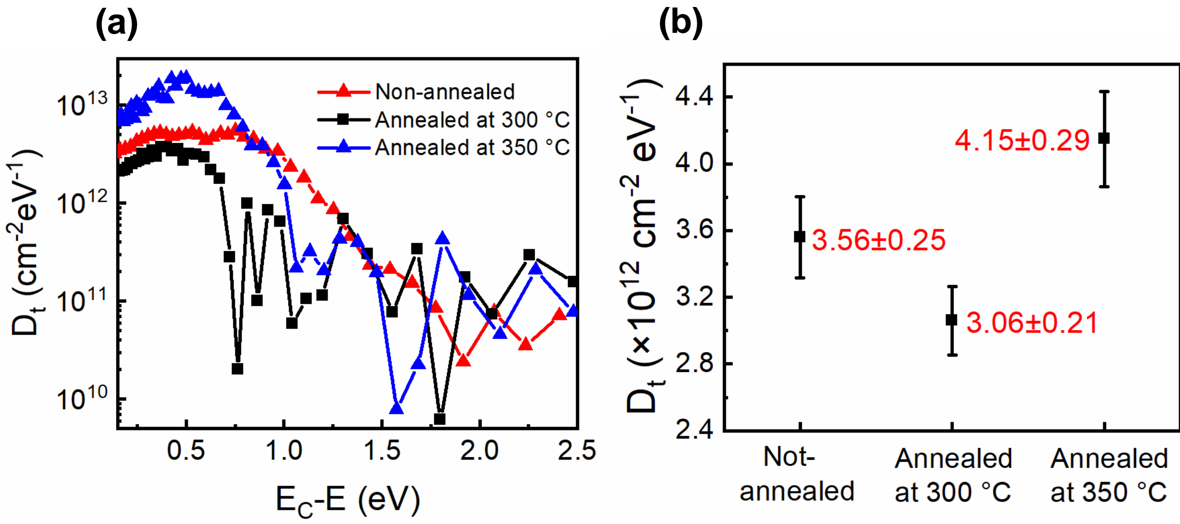

Figure 3.16 Total traps (D_t) as the function of energy and (b) average D_t for not-annealed, annealed at 300 ℃ and 350 °C AlSiO/Ga_2O_3 MOSCAPs. The AlSiO thicknesses were 30 nm for all the samples.

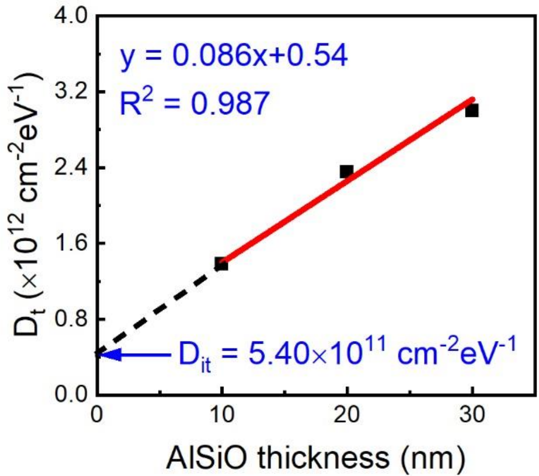

Figure 3.17 The linear fit of average trap density as a function of AlSiO thickness. The y-axis intercept and slope correspond to the interface density (D_{it}) of 5.4 $\times 10^{11}$ cm^{-2} eV^{-1} and the bulk trap density (n_{bulk}) of 4.3×10^{17} cm^{-3} eV^{-1}.

UV assisted C-V method. Further details about this methodology and physical analytical model can be found in Ref. [84]. **Figure 3.17** shows the linear fit of average D_t as a function of AlSiO thickness. The D_{it} of 5.4×10^{11} cm^{-2} eV^{-1} and n_{bulk} of 4.3×10^{17} $cm^{-3}eV^{-1}$ were extracted from the y-intercept and slope of the linear fit, respectively. Both interface state density and bulk traps are smaller than that was measured on AlSiO/Ga_2O_3 MOSCAPs without annealing, with corresponding D_{it} and n_{bulk} of 6.63×10^{11} cm^{-2} eV^{-1} and 4.65×10^{17} $cm^{-3}eV^{-1}$, respectively [96].

Figure 3.18 compares the forward I-V characteristics of AlSiO/Ga_2O_3 MOSCAPs with or without PMA treatment. The I-V characteristics presents two distinguishable regions: region I of low-leakage operation identified by the leakage current below the detection limit current level (~ 5×10^{-8} A/cm^2); and region II in which the gate leakage increases significantly until the gate bias approaches the avalanche breakdown. AlSiO with PMA at 300 °C extended the region of low-leakage operation from 0-3.7 MV/cm to 0-4 MV/cm compared with AlSiO not-annealed samples. In addition, the average breakdown field strength was measured to be 8.2 MV/cm at average

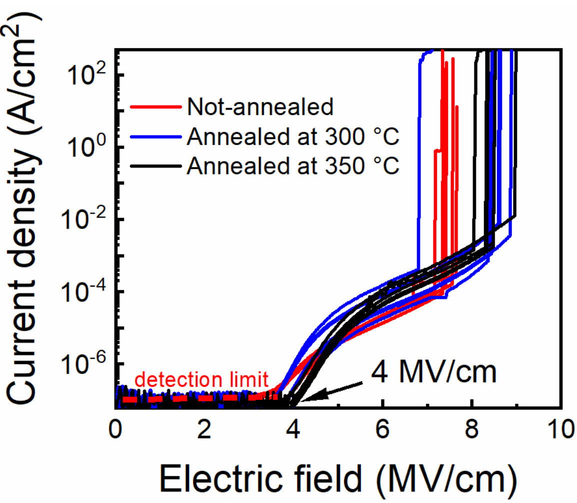

Figure 3.18 Forward leakage characteristics of AlSiO/Ga_2O_3 MOSCAPs with and without PMA. Annealing extended the region of low-leakage operation from 0-3.7 MV/cm to 0-4 MV/cm in the forward bias region.

leakage current of 1×10^{-3} A/cm^2 for AlSiO with PMA at 300 °C, which is higher than that of the underlying Ga_2O_3 and preferable for high power applications. No distinct improvement in low-leakage operation and breakdown strength were observed on sample with PMA at 350 °C. The results of lower-leakage operation and improved breakdown strength for AlSiO/Ga_2O_3 treated with PMA at 300 °C suggest a more reliable bulk dielectric with improved interface.

3.4 Summary

In summary, we studied the bulk quality and interfacial quality of two dielectrics, Al2O3 and AlSiO on Ga_2O_3. The interface state density (D_{it}) and bulk trap density (n_{bulk}) are extracted from fabricated MOSCAPs using deep UV-assisted capacitance-voltage method and an improved physical analytical model. The effects of the atomic layer deposition (ALD) deposition temperature and post-deposition annealing (PDA) condition are also studied for Al_2O_3. Increasing the deposition temperature and PDA at 500°C in O_2 seems to be an effective way to improve the

forward breakdown voltage (BV) and suppress capacitance-voltage hysteresis in Al_2O_3/β-Ga_2O_3 (001) MOSCAPs.

Additionally, negligible C-V hysteresis was achieved by a surface pretreatment that included three cycles of UV-ozone followed by an HF dip. Using deep UV assisted C-V method, an average interface state density of 6.63×10^{11} cm^{-2} eV^{-1} and a hole trap density in the bulk AlSiO of 4.65×10^{17} cm^{-3} eV^{-1} were quantified, which is half of that measured on ALD Al_2O_3/Ga_2O_3 MOSCAPs. Moreover, MOCVD AlSiO demonstrated more effective suppression of leakage current compared with ALD Al_2O_3 before avalanche breakdown occurred. We also studied the impact of post-metallization annealing on the operational reliability of MOCVD-grown AlSiO/β-Ga_2O_3 (001) MOSCAPs. No significant change was observed between the sample with and without PMA treatment in forward C-V step-stress measurements. A distinct improvement in reverse operational stability (test reverse stress from -10 to -42 V) was measured on AlSiO treated with PMA at 300 °C. The low gate leakage region was extended from 3.7 MV/cm to 4 MV/cm and the breakdown strength was enhanced from 7.8 MV/cm to 8.2 MV/cm for AlSiO/β-Ga_2O_3 MOSCAPs treated with PMA at 300 °C compared with not-annealed samples. Reliable step-stress C-V performance, negligible hysteresis and reduced interfacial and bulk trap density achieved in this work demonstrate promising results for the improvements of MOS-based Ga_2O_3 devices. Switching Performance Analysis of Ga_2O_3 Vertical Power FinFETs.

Chapter 4 Switching Performance Analysis of Ga_2O_3 Vertical Power FinFETs

4.1 Introduction

4.1.1 Switches for DC Converter

Non-resistive components are preferred in converter circuits to avoid power loss to improve efficiency. As shown in **Fig. 4.1(a),** a simplified circuit with a lossless single-pole double-throw (SPDT) switch that can act as a simplified DC-DC converter. When the switch is in position 1, the switch output voltage $v_s(t)$ is equal to the converter input voltage V_{in}. When the switch is in position 2, and the switch output voltage $v_o(t)$ is equal to zero. The switch position is varied periodically with frequency f_s and duty cycle D and the waveform of switch output voltage is illustrated in **Fig. 4.1(b)**. $v_s(t)$ is a rectangular waveform having period $T_s = 1/f_s$. The duty cycle D is defined as the fraction of period in which the switch is in position 1. In light of the Fourier analysis, the DC component of a periodic waveform is equal to its average value. Hence, the DC component of $v_s(t)$ is

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)dt = DV_{in} \tag{4.1}$$

As a result, the input voltage is converted into a different output voltage which can be varied by changing the duty cycle D. Moreover, the power dissipated by the switch during the voltage conversion is ideally zero. When the switch is in position-1, the voltage across it is zero and hence the power dissipation is zero. When the switch is in position-2, then the current through the switch is zero and the power dissipation is zero. So this SPDT switch resulted in lossless DC-DC

conversion. In addition to the desired DC component V_s, the switch output voltage $v_s(t)$ also contains high-order harmonics. In most applications such as DC converter, these harmonics should be removed. Therefore, a low-pass filter that passes DC and low-frequency signals and block high-frequency signals can be added to the circuit. **Figure 4.2** illustrates a schematic of a DC buck converter, which provides an output that is a step down from the input voltage. In the

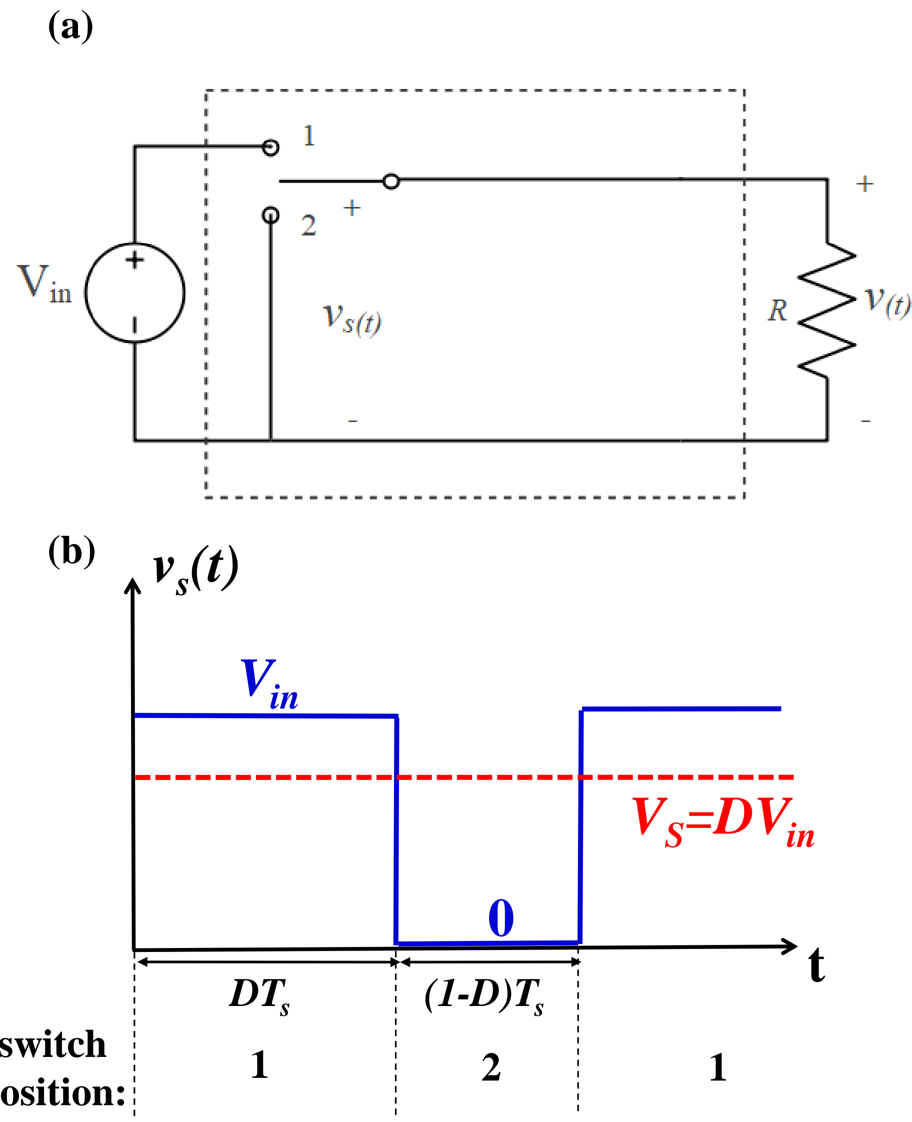

Figure 4.1 (a) Simplified circuit with single-pole double-throw (SPDT) switch that can change the DC component of the voltage. (b) Switch output voltage waveform $v_s(t)$.

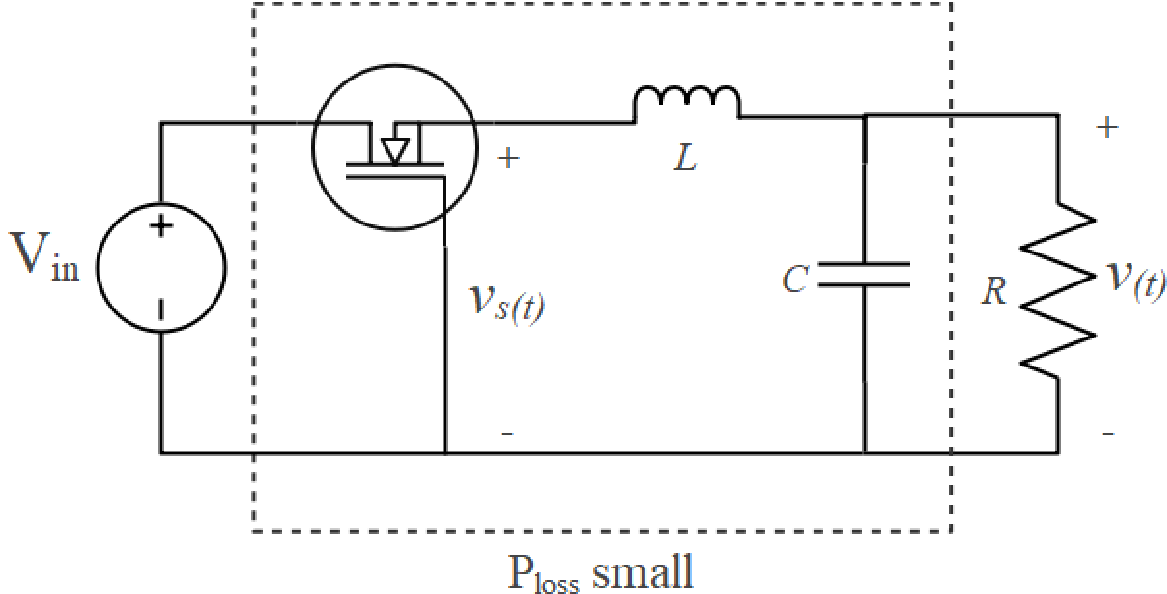

Figure 4.2 A schematic of DC buck-converter. The non-resistive components enclosed by the dashed line have negligible power loss in the circuit.

circuit, the SPDT switch is realized by a switched-mode semiconductor MOSFET. A second-order L-C low-pass filter is utilized to remove the harmonics of the switch output voltage. If the filter resonant frequency f_0 is sufficiently less than the switching frequency f_s of the transistor, then the filter can pass only the DC component of $v_s(t)$. Moreover, since the circuit only contains the switch, inductor, and capacitor, the efficiency of this DC converter can approach 100%. In other words, $V_o \times I_o = V_{in} \times I_{in}$. In practice, a feedback-loop control system is also used to regulate the output voltage.

4.1.2 Switching Process for Unipolar Devices

Figure 4.3 shows the turn-on process of power transistor during the power conversion. When the device is in OFF-state, before the gate bias is applied, current only flows through the inductive load and a free-wheeling diode circuit loop. The gate-to-source capacitance C_{GS} is

discharged (0 V). The entire output voltage drops on the switch. Both gate-to-drain and drain-to-source capacitances C_{GD} and C_{DS} are charged (3.5 kV). When a positive gate bias is applied, gate

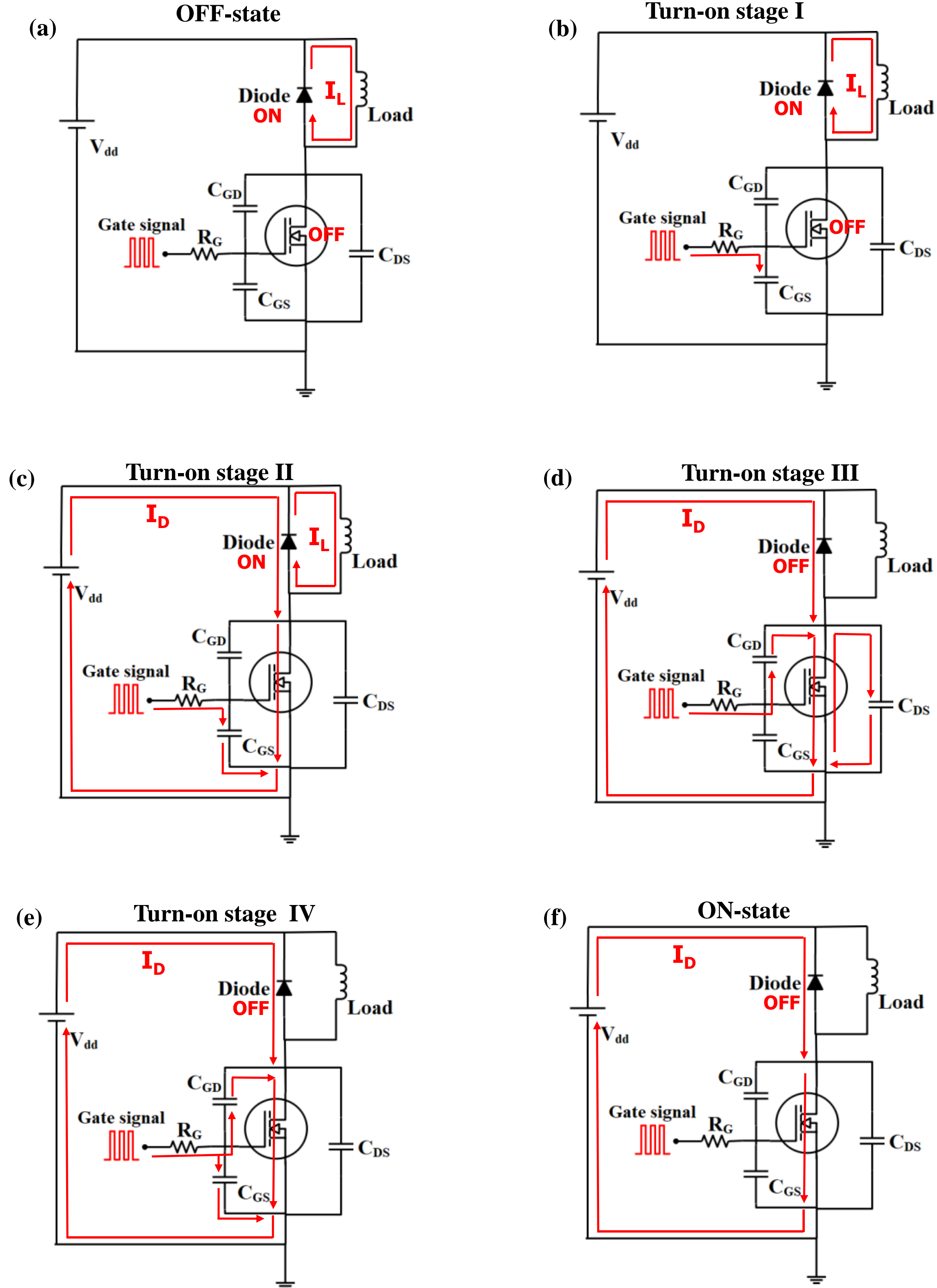

Figure 4.3 Illustration of turn-on switching transient of a semiconductor power transistor.

current I_G begins to charge the C_{GS}, as shown in the turn-on stage I in **Figure 4.3 (b)**. There is a delay time until V_{GS} reaches the threshold voltage V_{th}. During this time, the channel remains off, and no current is allowed flowing through the transistor. In turn-on stage II (**Fig. 4.3(c)**), when the V_{GS} reaches the threshold voltage, the channel is conductive. Nevertheless, only a small part of the load current passes through the switch, which is limited by the carrier density and conductivity of the channel. The rest of the load current still flows through the free-wheeling diode, making the diode forward biased and drain-bias of the transistor is maintained high ($v_D(t) = V_{DD}$). As the V_{GS} further increases, the channel in the device is more conductive, all the load current flows mainly through the power transistor instead of the free-wheeling diode. At this time, the gate voltage reaches Miller Plateau, in which the channel current begins to discharge the C_{GD} and C_{DS}. As a result, V_{GD} and V_{DS} both decrease. This is labeled as turn-on stage III, as shown in **Fig. 4.3 (d)**. In turn-on stage IV (**Fig. 4.3 (e)**), the C_{GS} is continued to be charged and the V_{GS} further increases until it reaches the $V_{GS,on}$. Then the transistor is in ON-state (**Fig. 4.3 (f)**). The output capacitances C_{GD} and C_{DS} are fully discharged. The current flowing through the transistor equals to the load current, and the voltage across the transistor is the $V_{DS,on}$.

The waveforms of gate voltage v_{GS}, drain current i_{DS} and voltage V_D, and power loss p_D are depicted in **Fig. 4.4(a)**. Similarly, the turn-off process is the reverse of turn-on process, as shown in **Fig. 4.4(b)** [5]. Once gate is discharged and reaches the Miller gate plateau voltage, the current across the switch remains constant. When the channel current starts dropping, the excess current begins to charge the two capacitors: C_{GD} and C_{DS}, presented by a V_D rise from $V_{DS,on}$ up to V_{DD} in the Miller Plateau in **Fig. 4.4(b)** [5]. After the drain is fully charged, the load current decreases to zero and channel is turned off. V_{GS} then continues to decrease and reaches 0V. The total fall time consists of Miller Plateau time and the time in which load current reaches zero. The

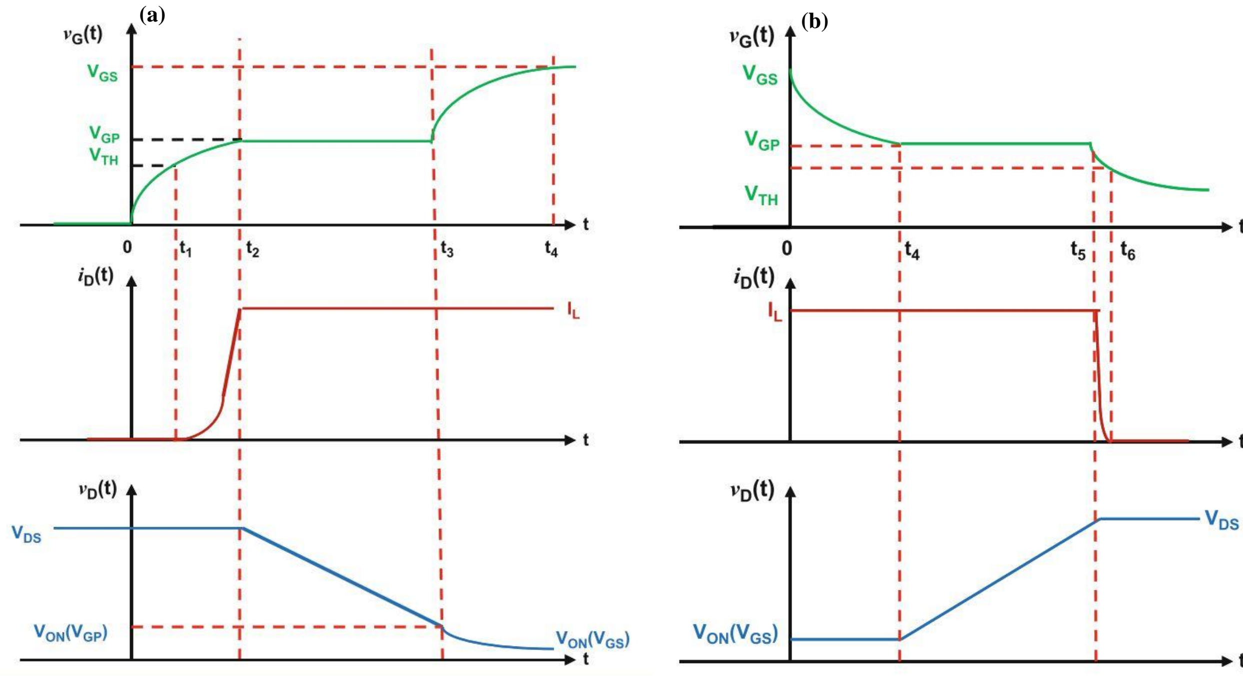

Figure 4.4 Waveforms for the power transistor during (a) turn-on and (b) turn-off process [5].

Miller Plateau is the major component of switching time and, therefore, contributes to the majority of switching loss [3].

4.1.3 Vertical Power FinFETs

The vertical FinFET structure was first demonstrated in GaAs material system for RF applications by Mishra et al [123], [124]. Then the vertical GaN power FinFET with submicron fin width was demonstrated in 2017 [125]. 1.2 kV vertical GaN power FinFETs were fabricated shortly after the first demonstration by the same group, with a record BFOM of 1440 MW/cm^2 and a switching FOM comparable to the state-of-the-art commercial 0.9-1.2 kV Si and SiC power transistors [126], [127]. **Figure 4.5** demonstrates the device structure of vertical GaN power FinFET [128]. It consisted of submicron fin-shaped channels to provide superior gate control and high channel density when compared with other the vertical devices such as trench MOSFETs or

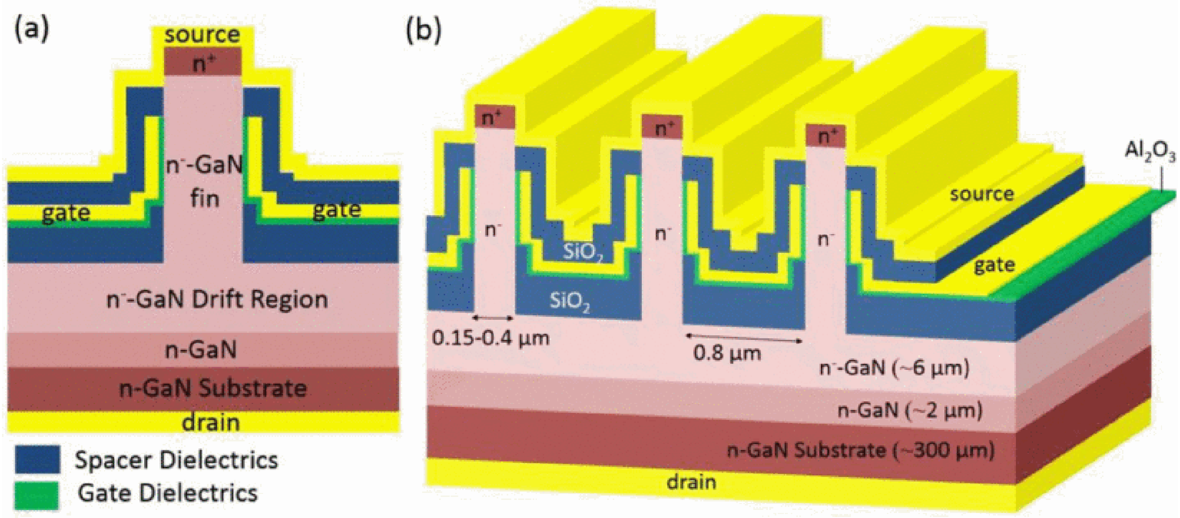

Figure 4.5 (a) Cross-sectional and (b) side-view three-dimensional schematics of vertical GaN power FinFETs [128].

CAVETs. Additionally, this fin channel enables e-mode operation by scaling off fin width and depleting the channel bi-directionally from sidewalls. In addition to the e-mode operation, another major advantage of this FinFET is that it only needs n-type semiconductor layers and does not require epitaxial regrowth, which allows the elimination of reverse recovery and power loss from body diode [5]. It also makes power FinFET structure attractive especially for semiconductors where selective-area doping is difficult (such as GaN) and one specific type of doping is not available (for p-type doping Ga_2O_3 and for n-type doping diamond) [10], [129], [130].

More recently, a similar structure was adopted in β-Ga_2O_3 material system [131]. Record breakdown voltage over 2.6 kV was demonstrated on β-Ga_2O_3 FinFETs with BFOM of 280 MW/cm^2 [43]. Despite rapid progress in Ga_2O_3 material and device technology, in which key static parameters, e.g. threshold voltage (V_{th}), on-resistance (R_{ON}), leakage and BV have been studied in vertical power FinFETs, there is still a lack of knowledge on the switching performance of β-Ga_2O_3-based FinFETs and the extent to which various factors, such as electron mobility in the fin

and the drift region, substrate thickness, and design parameters, can affect the switching performance and energy loss of these devices.

The highest electron mobility demonstrated in β-Ga_2O_3, so far, is ~180 cm^2/Vs for carrier density of 2.5×10^{16} cm^{-3} in films grown by metal organic chemical vapor deposition (MOCVD) [132]. This is higher than what has been achieved in halide vapor phase epitaxy (HVPE) grown epi-structure (130 cm^2/Vs for a carrier density of 5×10^{16} cm^{-3}) [133]. Regardless, the electron mobility in the bulk fin is typically much lower (~30 cm^2/Vs) due to dry etch damage and sidewall depletion [134]. The electron mobility in the fin can, however, be significantly improved using techniques such as acid treatment [65] or sidewall regrowth [135]. Substrate resistance is another factor that adds to the device on-resistance. Currently, commercially available n-type β-Ga_2O_3 substrates are ~600 μm thick with an electron density and mobility of ~3×10^{18} cm^{-3} and ~20 cm^2/ Vs, respectively [136], [137]. It is therefore of great importance to fully understand the impact of MOS channel, bulk fin and drift region mobilities and substrate thickness on the device characteristics and switching performance to better gauge the full potential of Ga_2O_3 FinFETs. Additionally, in a FinFET structure, the planar areas between fins add significantly to the off-state junction capacitances. It is, therefore, important to understand how the fin width/pitch size ratio affects the switching performance of these devices.

4.2 Device Design and TCAD Simulation

As following, ATLAS simulation platform was utilized for DC simulations and CV analysis of Ga_2O_3 FinFETs. We first compared the peak electric field and off-state capacitances in FinFETs with three different structures: (i) 30 nm-thick Al_2O_3 in the planar regions and partially-filled (PF) inter-fin areas and (ii) 130 nm-thick Al_2O_3 in the planar regions and PF inter-fin areas and (iii) 130 nm-thick Al_2O_3 in the planar regions and fully-filled (FF) inter-fin areas. A double-

pulse test circuit was then employed for switching analysis via TCAD device-circuit-integrated model [138]. Here, for the first time, the impact of electron mobility in the fin and drift region, substrate thickness and fin width/pitch size ratio on the off-state capacitances and switching performance were studied.

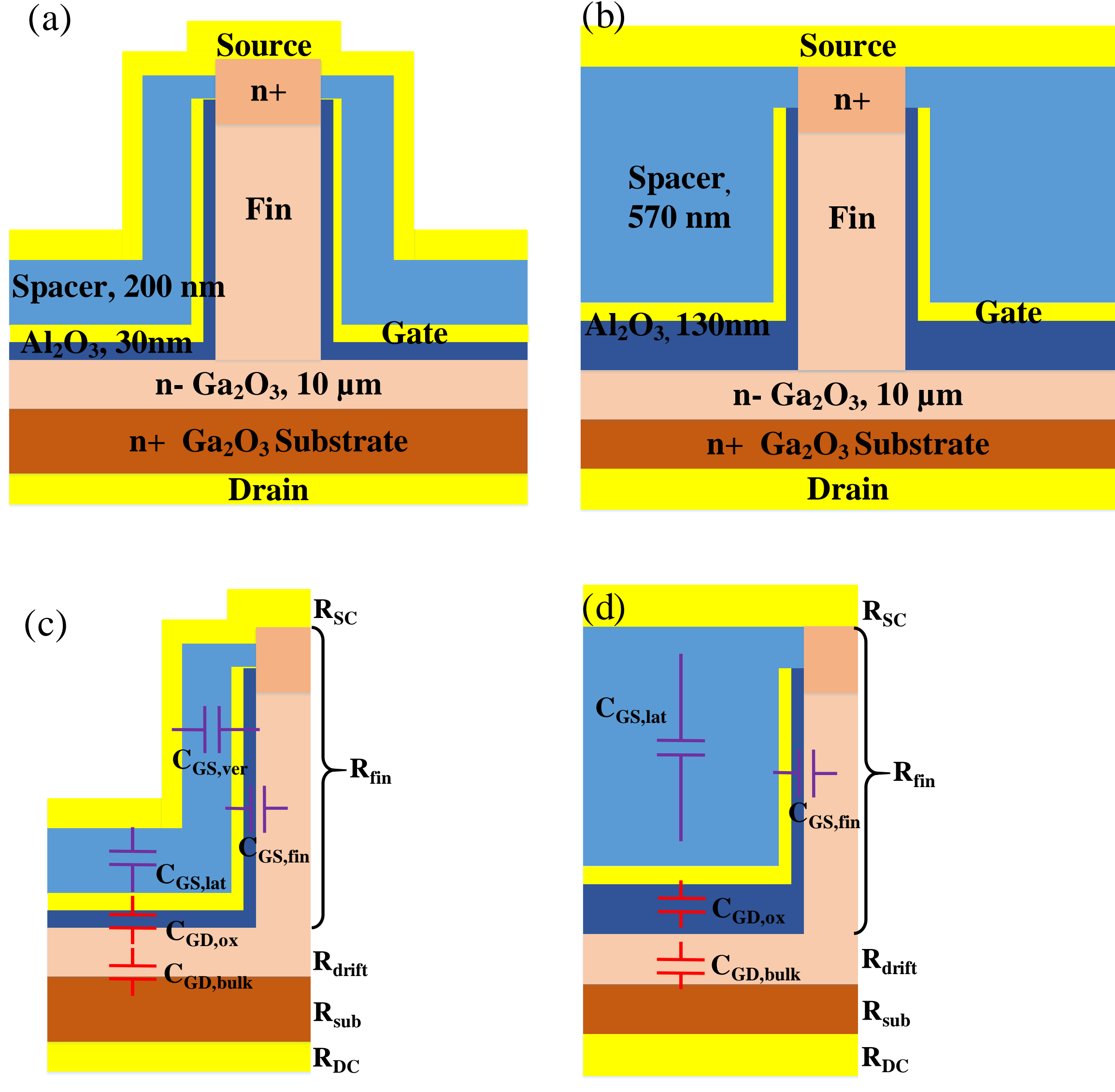

Figure 4.6 Schematic cross-section of Ga_2O_3 power FinFET with **(a)** partially-filled inter-fin, **(b)** fully-filled inter-fin and thicker dielectric layer in the inter-fin areas. Main capacitances and resistances in each structure are illustrated in **(c)** and **(d)**. The fin and drift regions were kept identical for both structures with fin width of 100 nm, fin height of 700 nm and drift region thickness of 10 µm. The 'ver', 'lat' and 'ox' represent 'vertical', 'lateral' and 'oxide', respectively.

Figure 4.6(a) shows the schematic of the first experimentally demonstrated E-mode Ga_2O_3 FinFET which has a 30 nm-thick Al_2O_3 as the gate insulator on the sidewalls and in the inter-fin areas and a partially filling (PF) SiO_2 spacer [139]. A new design is proposed here (shown in **Fig. 4.6(b)**), inspired by an earlier work on GaN power FinFETs [140], [141], with the inter-fin region fully filled (FF) by SiO_2, a planar source contact, and a 130 nm-thick Al_2O_3 gate insulator in the inter-fin areas. This new design with low-k dielectric full-filling (FF) the inter-fin areas can be fabricated utilizing plasma enhanced chemical vapor deposition (PECVD) or solution-based technique [142]. The thicker Al_2O_3 in the inter-fin area can be achieved by two separate atomic layer depositions (ALD) of Al_2O_3 as well as planarization technique as the following: First, 100 nm-thick ALD Al_2O_3 can be deposited uniformly. Then, a SiO_2 or photoresist planarization process can be performed to selectively etch away the Al_2O_3 on the sidewall and on top of the n+ Ga_2O_3 source and fin sidewalls using TMAH, in which the etch of Al_2O_3 with regard to SiO_2 is very selective. After SiO_2 removal, 30nm-thick Al_2O_3 layer cab be

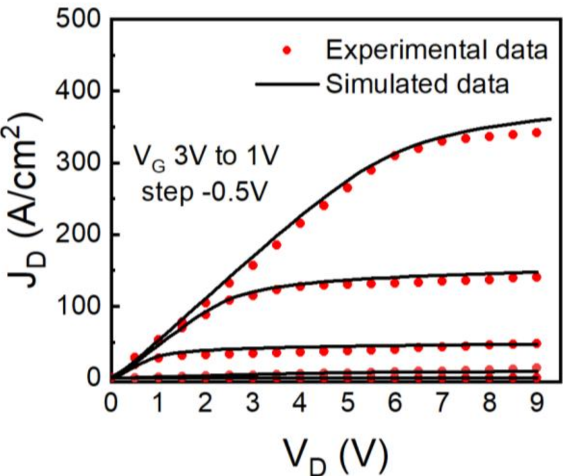

Figure 4.7 Comparison of I-V output characteristics of the simulated and fabricated Ga_2O_3 power FinFETs. [139] Copyright 2018 IEEE.

Table 4.1 Parameters used in the simulation calibration.

Parameters	Values
Average fin electron mobility (cm^2/Vs)	2
Drift region mobility (cm^2/Vs)	33
Bulk Ga_2O_3 electron mobility (cm^2/Vs)	20
Fin width (nm)	330
Fin height (nm)	770
n+ cap thickness (nm)	50
Drift region thickness (μm)	10
Bulk substrate thickness (μm)	600
Doping density (cm^{-3})	1.2×10^{16}

deposited by ALD to achieve 130 nm-thick and 30nm-thick Al_2O_3 in the inter-fin area and sidewalls, respectively.

The 2-D TCAD simulations described in this paper were performed using the Silvaco ATLAS simulator. The device physical models were established and calibrated based on experimental data in Ref [139]. A good agreement between experimental data and simulated results was achieved as shown in **Fig. 4.7**. The TCAD model was developed using the parameters depicted in **Table 4.1**, as given in Ref. [139]. The carrier continuity equations and Poisson equations were solved self-consistently, considering carrier generation, drift-diffusion, electron saturation velocity, and complete dopant ionization. In order to simplify the simulation, no thermal models were implemented, as the simulation of electro-thermal effect needs additional

Table 4.2 Parameters used in the PF and FF FinFET simulation.

Parameters	Values
Average fin electron mobility (cm^2/Vs)	30
Drift region mobility (cm^2/Vs)	130
Bulk Ga_2O_3 electron mobility (cm^2/Vs)	20
Fin width (nm)	100
Fin height (nm)	700
Drift region thickness (μm)	10
Bulk substrate thickness (μm)	600
Doping density (cm^{-3})	5×10^{16}

consideration of heat dissipation regions and 3-D device periphery geometries. A lower current is expected under a high voltage bias when self-heating effect is included; known as current collapse effect. PF and FF FinFETs were simulated assuming parameters shown in **Table 4.2**. Since the fin and drift regions of FF-FinFET were kept identical to PF-FinFET, both devices resulted in a nearly identical on-state DC characteristics such as threshold voltage (V_T) and on-resistance (R_{ON}).

4.2.1 Electric Field and Breakdown Voltage

Fig. 4.8(a) shows the simulated contour of electric field in Ga_2O_3 power FinFETs at drain voltage (V_D) of 3.5 kV in the off-state and **Fig. 4.8(b)** shows the corresponding electric field along a horizontal cutline across the fin bottom. The simulated devices include the PF-FinFET with

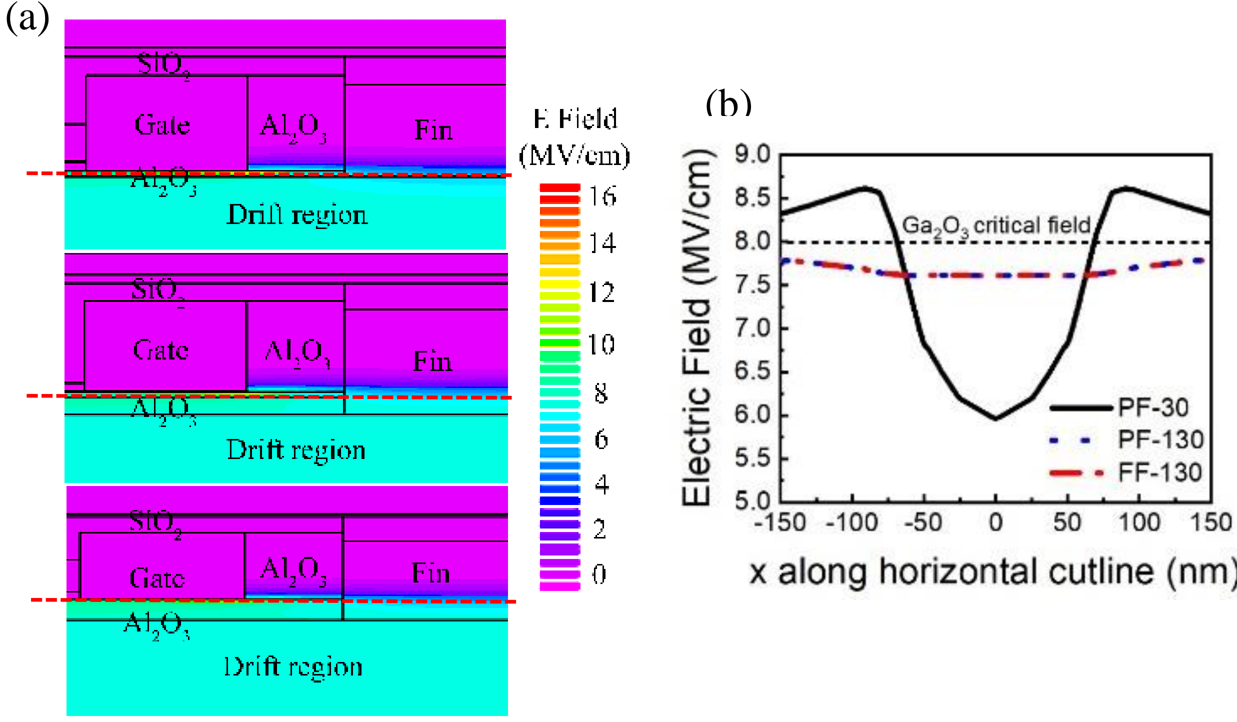

Figure 4.8 (a) Simulated contour of electric field in PF-30 (top), PF-130 (middle) and FF-130 (bottom) Ga_2O_3 power FinFET at drain voltage (V_D) of 3.5 kV; **(b)** Simulated electric field along a horizontal cutline across the fin bottom PF-30 (top), PF-130 (middle) and FF-130 (bottom) Ga_2O_3 power FinFETs.

Al_2O_3 gate insulator thicknesses of 30 nm and 130 nm, named as the PF-30 and PF-130, respectively; the FF-FinFET with 130 nm-thick Al_2O_3 layer in the inter-fin areas, named as FF-130. A thicker Al_2O_3 in the inter-fin areas in both PF-130 and FF-130 devices was found to reduce the voltage held in the Ga_2O_3 and consequently reduce peak electric field in the Ga_2O_3 under the off-state operation. The maximum electric field at the corner of fin was reduced from 8.6 MV/cm in the PF-FinFET with 30nm-thick Al_2O_3 to 7.6 MV/cm in the PF- and FF-FinFETs with 130 nm-thick Al_2O_3. Given the critical electric field of Ga_2O_3 is around 8 MV/cm, the PF-30 FinFET is expected to breakdown at V_D less than 3.5 kV, whereas the peak electric field in the PF-130 and FF-130 FinFET remains under the critical breakdown field at this voltage.

4.2.2 Junction Capacitances

The junction capacitances were also compared for these three different structures to study the impact of thicker Al_2O_3 layer in the inter-fin areas and FF-structure simultaneously. **Fig. 4.9(a)** depicts gate-to-source capacitance (C_{GS}) as a function of gate voltage (V_G) at zero drain voltage. C_{GS} plays a vital role as part of the input capacitance during device switching. C_{GS} in the device structure has components in both the inter-fin region and fin channel region (**Figs. 4.6(c) and (d)**). The latter one depends on V_G while the former is only a parasitic component independent of V_G. In the off-state, C_{GS} is dominated by capacitance in the inter-fin region; whereas in the on-state, it depends on both inter-fin region and accumulated electrons formed in the fin region. In both cases, a lower C_{GS} was observed in the FF-130 FinFET compared to the PF-130 and PF-30 FinFETs. When device is turned on, the PF-130 shows smaller gate-source capacitance compared with the PF-30 due to a thicker Al_2O_3 dielectric in the corner of the fin. We also studied the off-state C_{GS}, gate-drain (C_{GD}) and drain-source (C_{DS}) junction capacitances in these three structures. Fully filling the inter-fin area by SiO_2 reduced C_{GS} (**Fig. 4.9(b)**). C_{GD} remained almost unaltered by

either FF-structure or Al_2O_3 thickness in the inter-fin region **(Fig. 4.9(c))**. C_{DS} was nearly negligible in all device structures due to the screening effect of gate metal **(Fig. 4.9(d))**. Nevertheless, increasing the Al_2O_3 thickness slightly decreased C_{DS}. Since FF-130 FinFET structure showed larger breakdown voltage and smaller junction capacitances, we focused on this structure for the rest of the studies presented here.

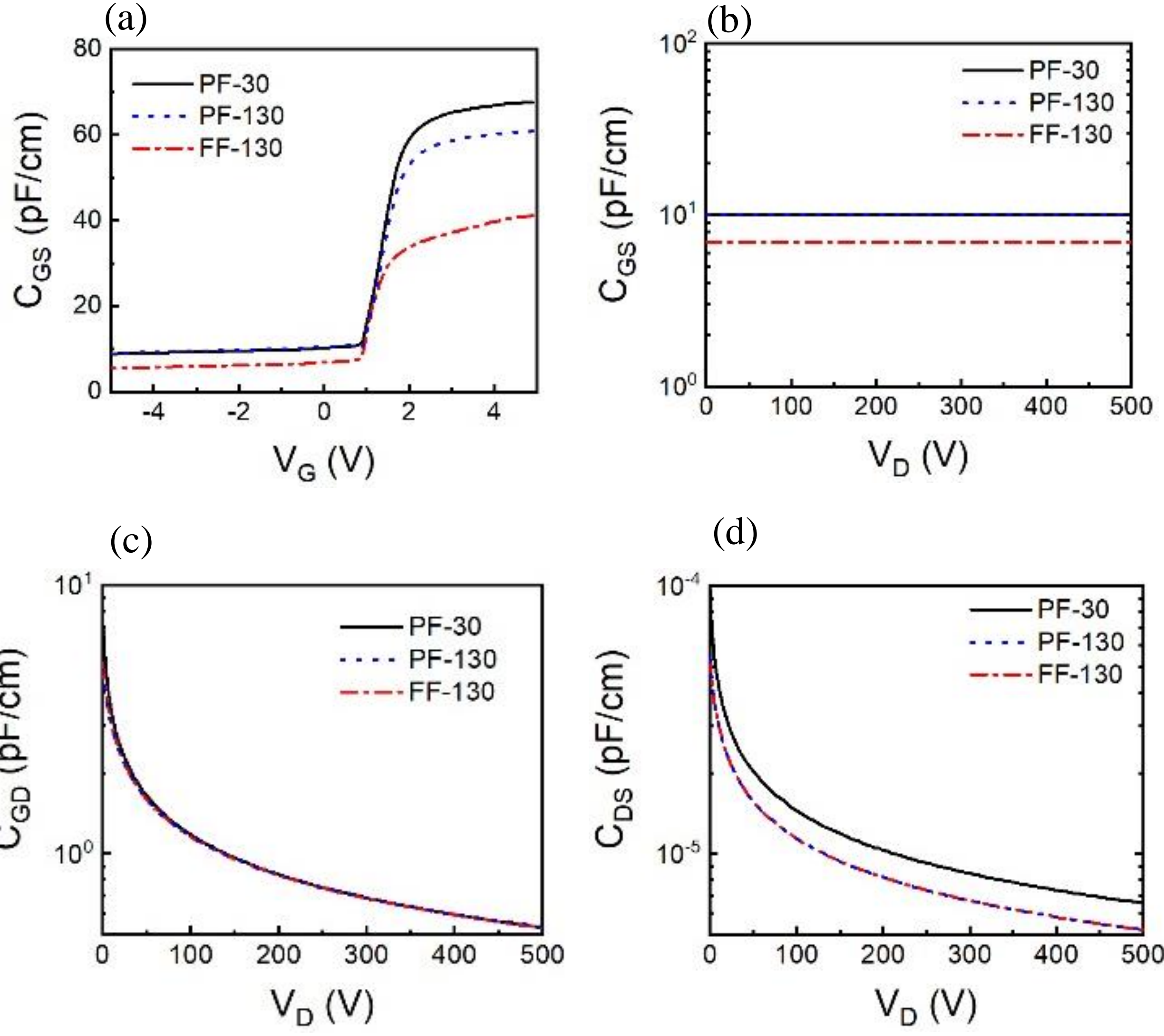

Figure 4.9 (a) Gate-source capacitance (C_{GS}) as a function of gate voltage at zero drain voltage; (b) Off-state gate-source capacitance (C_{GS}), (c) gate-drain capacitance (C_{GD}), and (d) drain-source capacitance (C_{DS}) as a function of drain voltage at zero gate voltage for PF-30 (black solid line), PF-130 (blue dotted line) and FF-130 (red dash-dotted line) Ga_2O_3 power FinFETs.

4.3 Single-Fin Analysis

To study the impact of electron mobility and substrate thickness on the switching performance of FF FinFETs, we simulated a single-fin structure shown in **Fig. 4.6(b)**. Four devices were studied; For device A, substrate thickness (T_{sub}), and electron mobility in the drift region (μ_{drift}), were assumed to be 600 µm, and 130 cm^2/Vs [133]. Electron mobility in the bulk fin (μ_{fin}) and in the MOS channel (μ_{MOS}) adjacent to the sidewall were set to 30 cm^2/Vs [139] and 2 cm^2/V, respectively. This was to study the impact of sidewall roughness caused by etch damages during the device processing and the interface states at the Ga_2O_3/dielectric interface leading to lower electron mobility [134], [143]. In this case, the majority of the current flows through the bulk fin channel. In comparison, the MOS channel and bulk fin mobilities were both set to 30 cm^2/Vs in device B. Detailed discussion on on-resistance and mobility analysis of vertical power FinFET can be found in Ref. [143]. In device C, electron mobilities in MOS channel, bulk fin and the drift region were all assumed to be 180 cm^2/Vs which is the highest room-temperature mobility demonstrated for β-Ga_2O_3 [132] with the assumption that the device design and processing are improved to eliminate the detrimental impact of dry etching on electron mobility in the channel. As above-mentioned, the electron mobility in the fin can be significantly improved using techniques such as acid treatment, annealing [65] or sidewall regrowth [135]. For device D, T_{sub} was reduced to 100 µm, while the electron mobility was kept the same as in device C. Substrate thinning is expected to also reduce the self-heating effects although not studied in this work. **Table 4.3** summarizes the parameters that were assumed in our simulations. A dielectric interface trap density (D_{it}) of 1.5×10^{12} cm^{-2} was assumed in all the presented calculations.

Table 4.3 Parameters of devices used in single-fin analysis.

Parameters	Values			
	A	B	C	D
MOS channel mobility	2	30	180	180
Bulk fin mobility (cm^2/Vs)	30	30	180	180
Drift region mobility (cm^2/Vs)	130	130	180	180
Bulk Ga_2O_3 electron mobility (cm^2/Vs)	20			
Fin width (nm)	100			
Fin height (nm)	700			
Drift region thickness (μm)	10			
Bulk substrate thickness (μm)	600	600	600	100
Doping density (cm^{-3})	5×10^{16}			

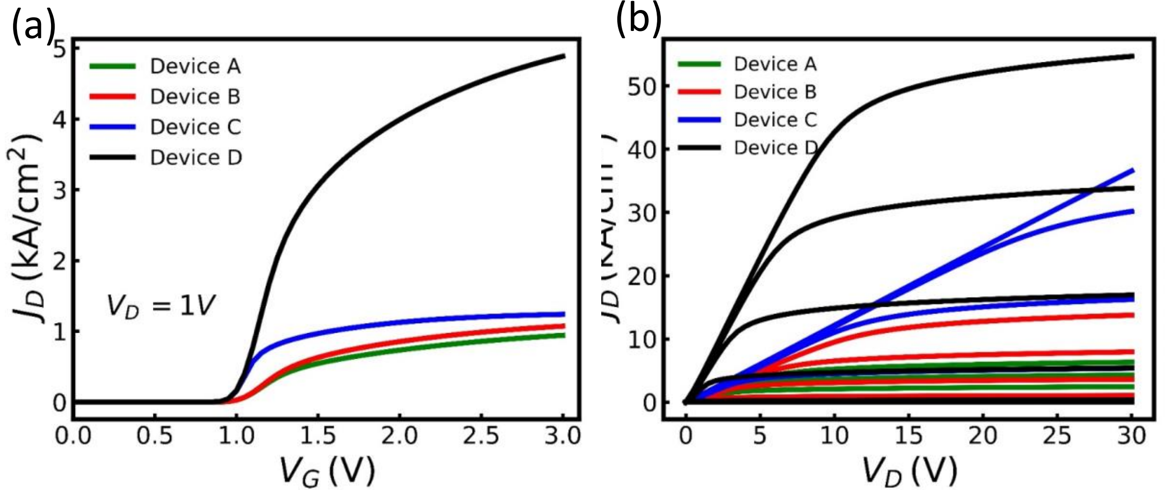

Figure 4.10 (a) Transfer and (b) output I-V characteristics in Device A: T_{sub} = 600 μm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, μ_{MOS} = 2 cm^2/Vs, Device B: T_{sub} = 600 μm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, μ_{MOS} = 30 cm^2/Vs, Device C: T_{sub} = 600 μm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, μ_{MOS} = 180 cm^2/Vs, and Device D: T_{sub} = 100 μm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, μ_{MOS} = 180 cm^2/Vs. The gate voltage (V_G) in Fig. 5(b) was swept from 0.5 V to 2V with a step of 0.25 V.

The transfer and output I-V characteristics are depicted in **Fig. 4.10**. These calculations suggest that increasing the mobilities, even to a maximum value demonstrated in Ga_2O_3, does not significantly improve the DC characteristic of Ga_2O_3 FinFETs. This is because the maximum

electron mobility in β-Ga_2O_3 (180 cm^2/Vs) is much lower than what can be achieved in the drift region in other wide bandgap semiconductors such as GaN or SiC (~1000 cm^2/Vs). On the other hand, thinning the substrate in device D resulted in three times larger current density than that in device A, B or C at V_G of 3V. Additionally, a lower knee voltage in device D can be explained by the reduced substrate resistance, and consequently, a larger portion of the applied voltage being held in the drift region rather than the substrate.

Table 4.4 shows a comparison of specific on-resistance (R_{ON},sp) in the three above-mentioned devices. R_{ON},sp was calculated by normalizing to the device cell. R_{ON},sp was reduced only 36.8% by increasing the electron mobility in the bulk fin, channel and the drift region to 180 cm^2/Vs. However, R_{ON},sp reduced 75.8% by reducing the substrate thickness from 600 µm to 100 µm. These calculations indicate that a thick Ga_2O_3 substrate is not only undesirable because of its low thermal conductivity, but also because it adds significantly to the R_{ON} due to the low electron mobility (20 cm^2/Vs) in the substrate.

Table 4.4 Comparison of specific on-resistance ($R_{ON,sp}$) in Device A: T_{sub} = 600 µm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, μ_{MOS} = 2 cm^2/Vs, Device B: T_{sub} = 600 µm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, μ_{MOS} = 30 cm^2/Vs, Device C: T_{sub} = 600 µm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, μ_{MOS} = 180 cm^2/Vs, and Device D: T_{sub} = 100 µm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, μ_{MOS} = 180 cm^2/Vs. R_{ON},sp is normalized to the device cell.

	Device A	Device B	Device C	Device D
$R_{ON,sp}$ ($m\Omega\cdot cm^2$)	10.08	8.89	6.37	1.54

A 3.5 kV, 20 A double-pulse test circuit was implemented via Silvaco TCAD simulation framework to study the switching performance of these devices (**Fig. 4.11(a)**). The Silvaco ATLAS device model was incorporated in the SPICE circuit by mixed-mode analysis. Using this hybrid model, one can start with a two-dimensional (2D) drift-diffusion model of the device and build all the way up to its circuit implementation to evaluate its switching performance. To expedite the simulations, the load was modelled as a current source and an ideal freewheeling

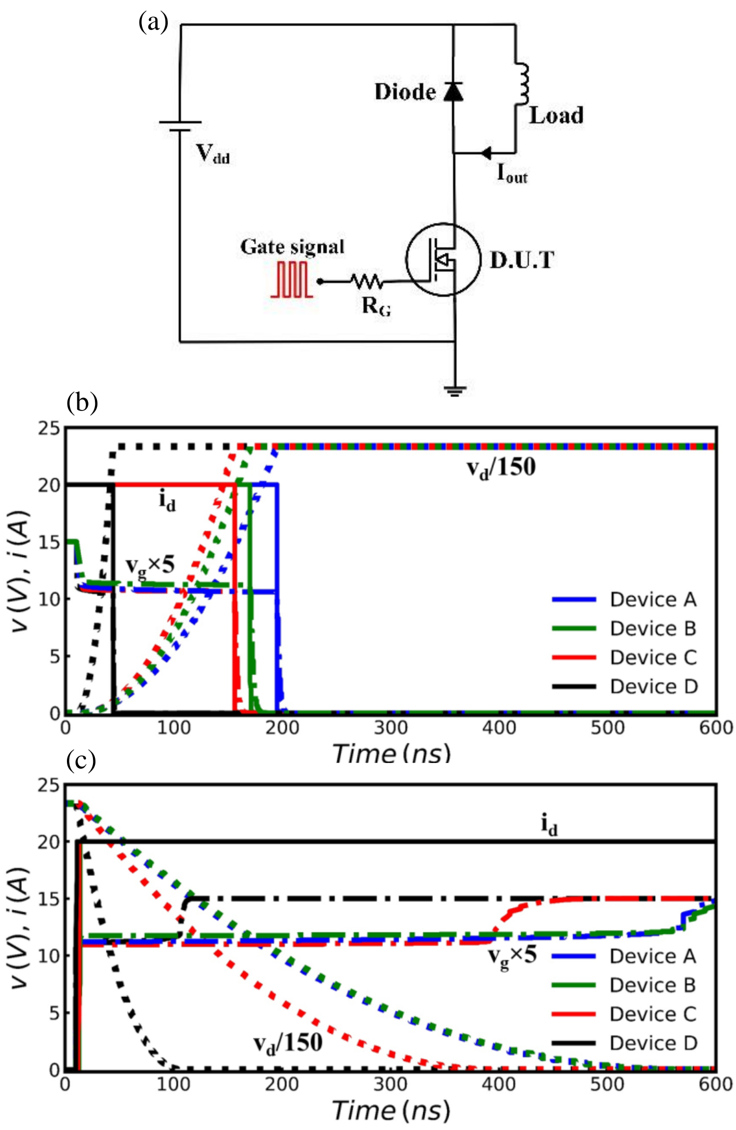

Figure 4.11 (a) The schematic of double-pulse circuit implemented in the mixed-mode TCAD simulation. Simulated (b) turn-off and (c) turn-on waveforms in Device A, B, C and D.

diode was implemented in the circuit following Ref [144]. The gate resistance (R_G) was set at 1.5 Ω for all the simulations. The gate driver turn-on and turn-off signal level were set at 3 V and 0 V, respectively.

Fig. 4.11(b) shows the switching waveforms during the turn-off transient. In device A, the fall time (t_f) is 184.7 ns, and the turn-off Δv/Δt is 18.95 kV/µs. The total gate charge is 2.02 µC, including a Q_{GD} of 1.99 µC. In device D, the fall time (t_f) is 33.8 ns, and the turn-off Δv/Δt is 103.6 kV/µs. The total gate charge was 367 nC, including a Q_{GD} of 362.3 nC. The reduced Miller plateau time and its corresponding fall time in device C are attributed to a reduced C_{GD} ($t=C_{GD}\times V_D/i_G$) in this device due to higher electron mobility in the fin and drift regions and lower series resistances because of the thinner substrate. A comparison between fall times in device A, B, C and D shows that substrate thinning is important to reduce the switching time. These steps occur in reverse during the device turn-on process. The turn-on switching waveforms of these three devices are shown in **Fig. 6(c)**. Device D had a total rise time of 95 ns, which is 82.9% lower than that in device A.

Figure 4.12 depicts the key switching metrics, including fall time (t_F), rise time (t_R), turn-off energy loss (E_F) and turn-on energy loss (E_R), as well as gate-drain charge (Q_{GD}). The switching frequency was 10 kHz for calculation of energy loss. Device D with 100 µm-thick substrate and ideal drift region and fin mobilities of 180 cm^2/Vs showed 82.6% improvement in the total switching time and 82.2% lower switching losses compared with Device A which had thicker substrate thickness (600 µm) and lower electron mobilities in the drift region (130 cm^2/Vs), bulk fin (30 cm^2/Vs) and MOS channel (2 cm^2/Vs).

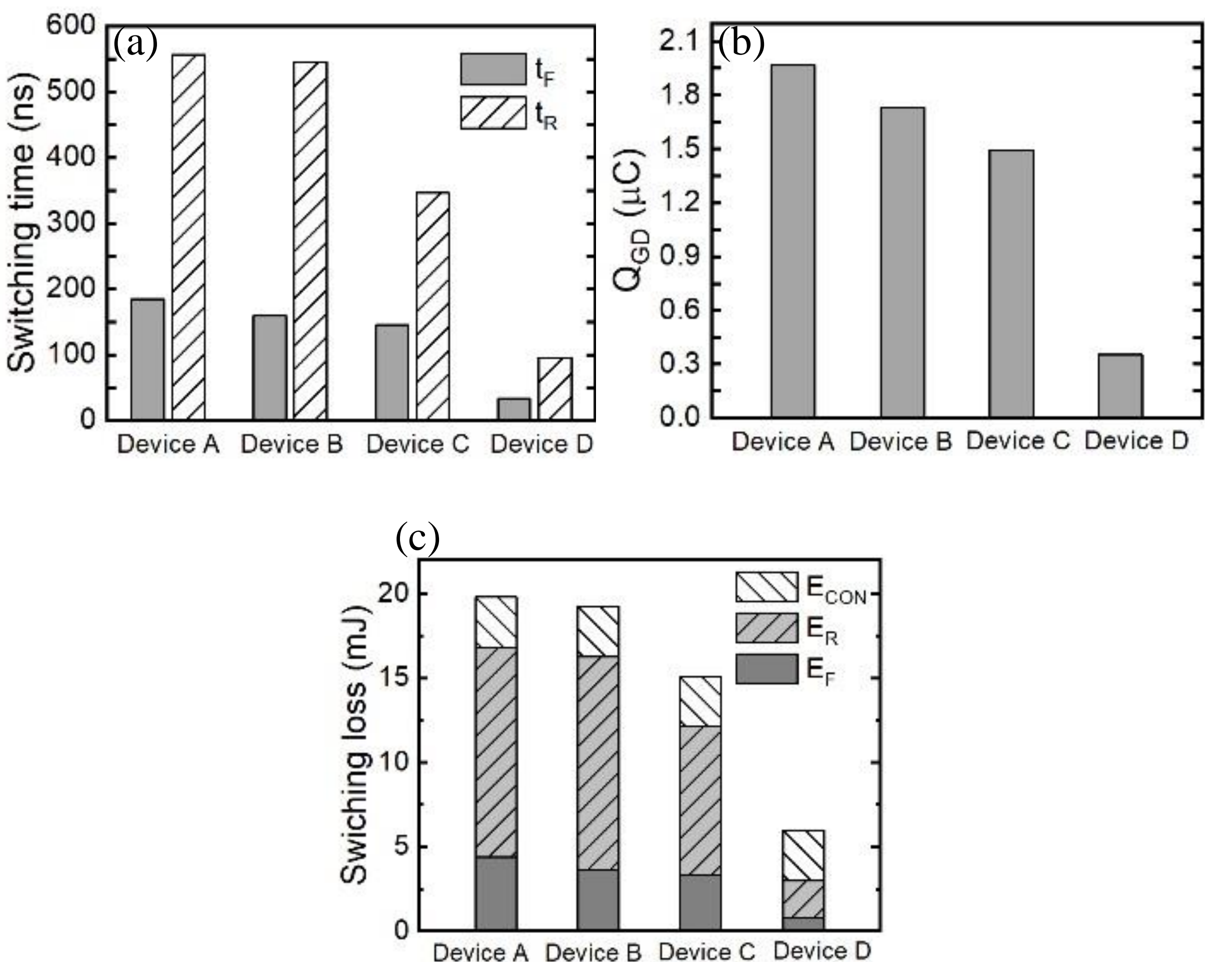

Figure 4.12 Key switching metrics extracted from the simulated double-pulse testing waveforms in Device A, B, C and D, including **(a)** fall time (t_F) and rise time (t_R), **(b)** gate-drain charge Q_{GD}, and **(c)** turn-off energy loss (E_F), turn-on energy loss (E_R) and conduction energy loss (E_{CON}) at switching frequency of 10 kHz.

Figure 4.13 shows the total switching energy loss as a function of operating frequency ranging from 10 kHz to 200 kHz. For a certain power loss, device D yielded four times larger switching frequency compared to that with device A/B/C which has lower electron mobilities and/or thicker substrate. The total power losses of device A, B, C and D were 4.85%, 4.69%, 3.50% and 0.89%, respectively, of the input power at frequency of 200 kHz. It is important to note that in this section the goal was to study the impact of intrinsic parameters on the switching frequency of these devices. Hence, a single-fin structure was employed to enhance the computation speed.

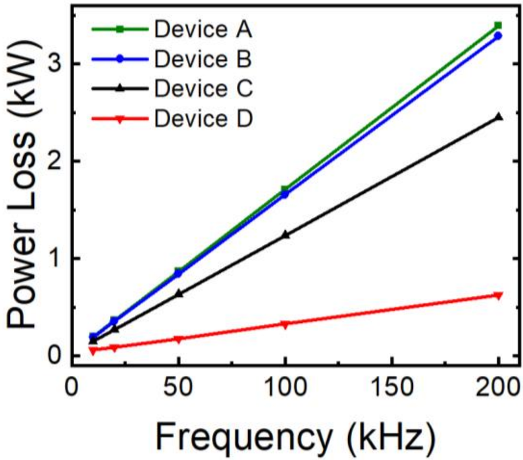

Figure 4.13 Power loss as a function of frequency from 10 kHz to 200 kHz in Device A: T_{sub} = 600 μm, μ_{drift} = 130 cm^2/Vs, μ_{fin} = 30 cm^2/Vs, Device B: T_{sub} = 600 μm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs, and Device C: T_{sub} = 100 μm, μ_{drift} = 180 cm^2/Vs, μ_{fin} = 180 cm^2/Vs. The input voltage was 3.5 kV, and the load current was 20 A.

Additionally, an arbitrary length (1μm) was chosen for the planar sections on each side of fin, which contributed significantly to the off-state junction capacitances. In the next section, we studied the impact of fin width/ pitch size ratio on the switching performance of these devices.

4.4 Multi-Fin Analysis

A double-fin unit cell (**Fig. 4.14**) was implemented to further investigate the impact of fin width/pitch size ratio on the switching performance in the multiple fin systems. For this purpose, the pitch size was fixed at 700 nm for all the simulations. This fixed pitch size ensures the same total die size, and hence, a fair comparison of DC and switching performance between different devices. Therefore, to change fin width/pith size ratio, the fin width and the fin-to-fin spacing were varied as shown in **Table 4.5**.

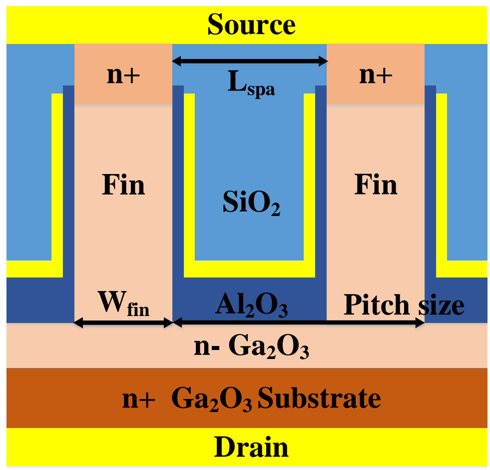

Figure 4.14 Schematic cross-section of unit cell of Ga_2O_3 power FinFETs.

Table 4.5 Parameters of devices used in the multi-fin analysis. The devices with fin widths of 100 nm, 200 nm, 300 nm, 400 nm at a given pitch size of 700 nm were named as the W_{fin}-100, W_{fin}-200, W_{fin}-300, and W_{fin}-400 respectively. The input voltage was 3000 V, and the load current was 20 A. $R_{ON,sp}$ was calculated by normalizing to the device active area.

Parameters	W_{fin}-100	W_{fin}-200	W_{fin}-300	W_{fin}-400
Fin-to-fin spacing (L_{spa}) (nm)	600	500	400	300
Pitch ratio (W_{fin}/Pitch size)	14.3%	28.6%	42.9%	57.1%
Doping in the fin (cm^{-3})	5×10^{16}	2×10^{16}	8×10^{15}	5×10^{15}
Doping in the drift region (cm^{-3})	5×10^{16}	5×10^{16}	5×10^{16}	5×10^{16}
V_{BR} (kV)	>3.5	>3.5	>3.5	>3.5
V_T (V)	~1.0	~1.0	~1.0	~1.0
$R_{ON,sp}$ ($m\Omega\cdot cm^2$)	3.76	3.58	3.55	3.54

Table 4.5 shows device parameters and corresponding DC characteristics in devices with various fin widths and fin-to-fin spacings. The substrate thickness was set at 100 μm, and the electron mobility in both fin and the drift was 180 cm^2/Vs. The doping in the fin was reduced as the fin width increased to keep V_T constant and equal to 1V for a fair comparison, while the doping in the drift region was 5×10^{16} cm^{-2} for all the devices. The doping in the fin can be tuned in practice by epitaxial growth using molecular beam epitaxy (MBE) or MOCVD. Similar R_{ON} and V_T were observed in these devices. It is important to note that, unlike single-fin simulations presented

earlier, in this section $R_{ON, sp}$ was calculated by normalizing to the total die size to draw a fair comparison between devices with different fin widths. Therefore, $R_{ON, sp}$ reported in this section are higher than those reported for the single-fin structure.

The switching performance was studied using the same double test circuit as discussed before. The length of unit-cell was adjusted to keep R_{ON} equal to 75 mΩ for all the simulations presented here. The switching frequency was 10 kHz for calculation of energy loss. The input voltage was 3000 V, and the load current was 20 A. As shown in **Fig. 4.15**, the total switching

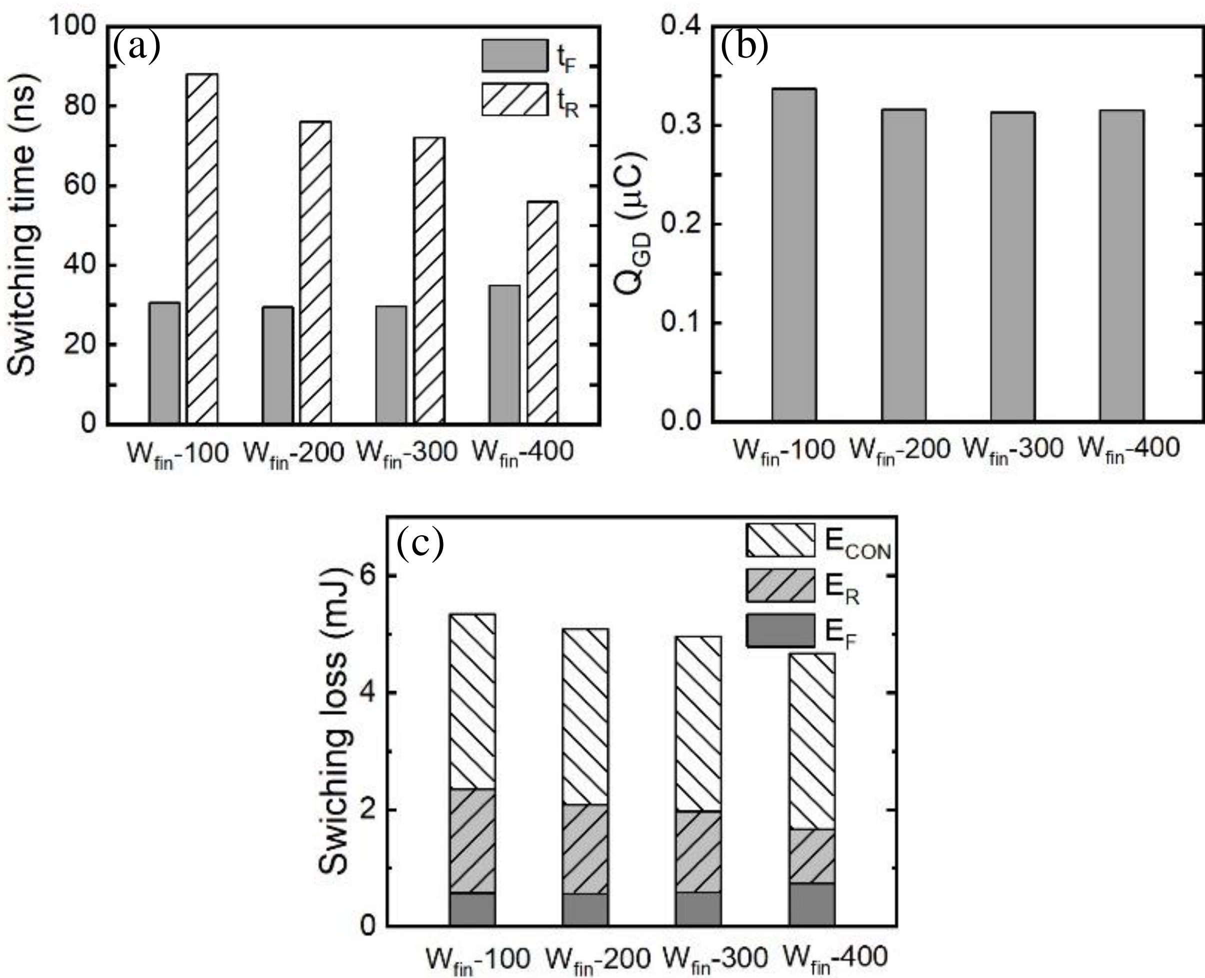

Figure 4.15 Key switching metrics extracted from the simulated double-pulse testing waveforms in Ga_2O_3 power FinFETs devices with fin widths of 100 nm, 200 nm, 300 nm, and 400 nm at a given pitch size of 700 nm. The input voltage was 3000 V, and the load current was 20 A.

time and switching losses reduced 23.3% and 12.7%, respectively, in the device with 400nm fin width (pitch ratio of 57.1%) compared with that in the device with fin width of 100 nm (pitch ratio of 14.3%). This can be explained by the reduction in the junction capacitances in the inter-fin region as L_{spa} was reduced in the device with larger fin width.

Figure 4.16 shows the total switching energy loss as a function of operating frequency ranging from 10 kHz to 200 kHz. The total power losses of W_{fin}-100, W_{fin}-200, W_{fin}-300, and W_{fin}-400 were 0.83%, 0.74%, 0.70% and 0.61% of the input power at frequency of 200 kHz, respectively.

The switching FOM ($R_{ON}\cdot Q_{GD}$) of 21.9 nC·Ω was reported for Ga_2O_3 power FinFET operating at 3 kV and 20 A. This value is comparable with other currently available state-of-art 0.8-1.2 kV Si, SiC and GaN devices with switching FOM ranging from 1.1 nC·Ω to 17 nC·Ω [141], [145]–[149]. Please note our device has significantly larger operating voltage and power rage. However, there is no complete data reported so far for the switching characteristics of the

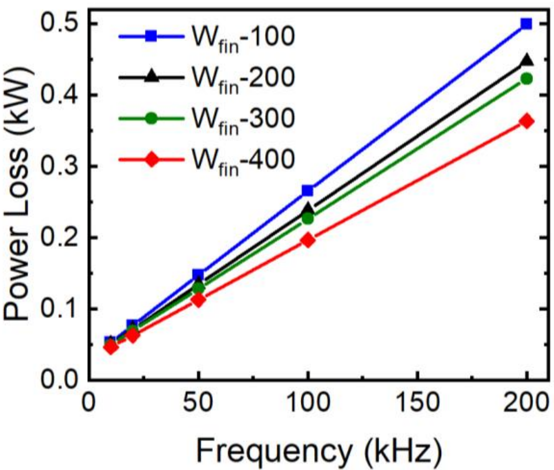

Figure 4.16 Power loss as a function of frequency ranging from 10 kHz to 200 kHz in Ga_2O_3 power FinFETs devices with fin widths of 100 nm, 200 nm, 300 nm, and 400 nm at a given pitch size of 700 nm.

devices with similar voltage class. Further studies are needed to assess the switching efficiency by modeling a simple boost/buck converter based on the designed Ga_2O_3 power FinFETs.

4.5 Summary

In this work, we designed a normally-off β-Ga_2O_3 FinFET with 3.5 kV breakdown voltage. The simulated electric field and off-state capacitances at V_D of 3.5 kV were compared using Silvaco TCAD simulation platform for two structures: (i) partially-filled (PF) FinFET and (ii) fully-filled (FF) FinFET with thicker dielectric in the inter-fin areas. The FF FinFET showed a smaller off-state C_{GS}. Also, the thicker Al_2O_3 in the inter-fin area in this device structure significantly reduced peak electric field at the corner of fin. The switching performance of β-Ga_2O_3 FinFETs was studied, for the first time, on the FF structure. The impact of electron mobility in the fin and the drift region, substrate thickness and fin width/pitch ratio on the rise/fall time as well as total switching loss was investigated. The device with 100 μm-thick substrate and ideal drift region, bulk fin and MOS channel mobilities of 180 cm^2/Vs achieved 82.6% improvement in the total switching time and 82.2% lower switching losses in 3.5 kV switching operation. Moreover, the total power loss of the input power at frequency of 200 kHz was reduced from 0.83% to 0.61% as pitch ratio reduced from 57.1% to 14.3% at a given pitch size of 700 nm. These findings show great promise for β-Ga_2O_3 power transistors and provide helpful insights for design of Ga_2O_3 FinFETs with enhanced characteristic.

Chapter 5 Chlorine-based Inductive Coupled Plasma Etching of α-Ga_2O_3

5.1 Introduction

5.1.1 ***Dry Etching***

Mesa etching is the key fabrication process to define the device geometry and isolate multiple devices on the same die. The mesa etching can be achieved by either wet etching or dry etching. Dry etching provides more directional (anisotropic) etching. It utilizes a plasma reaction, ion bombardment or a combination of both. The process is similar to the sputtering where the source target is replaced with the wafers to be etched. To obtain both high etch rate and etch selectivity, a simultaneous etching consisting of chemical and physical components are utilized and the process is called the reactive ion etching (RIE). The gas mixture is dissociated into radicals and ions under the high electromagnetic field. Free radicals, as chemical components in the dissociated mixture, react with atoms on the surface. These chemical reactions occur preferably at active sites where there are defects [150]. Since non-volatile byproducts act as micro-masks during the etching process, pure chemical etching results in rough surfaces. Ions, as physical components, which attack the sample surface simultaneously in the RIE system, can both create defects on the surface for the chemical reaction and remove non-volatile byproducts [150]. Ideally, the balanced chemical and physical etching in the RIE system can yield both high etch rate, good surface morphology and high selectivity.

A typical RIE system consists of a cylindrical vacuum chamber at the pressure maintained in a range between a few mTorr and a few hundred mTorr. The processed wafer is clamped on the

electrostatic chuck at the bottom the chamber and is electrically isolated from the rest of the chamber. Gas flows from small inlets in the top of the chamber, and exits to the exhaust orifice through the vacuum pump. The plasma is generated with an RF powered magnetic field. The system can typically support accurate deep etching capabilities for single wafer with size up to 6 inches.

In addition to the RF magnetic field which generates a high density source of plasma, inductively-coupled-plasma (ICP) etching incorporates a separate DC bias applied to the processed wafer. This independent control of DC bias provides separate control over ion energy and ion density, enabling high process flexibility. The plasma densities are 2-4 orders of magnitude higher than RIE, thus improving the bond breaking efficiency in the material being etched, while the increased ion density also enhances the desorption of etch products formed on the surface. In addition, the DC bias helps to create directional electric fields near the substrate and consequently achieve more anisotropic etch profiles.

5.1.2 Chlorine-based Dry Etching of β-Ga_2O_3

Chlorine-based dry etching was found to be more effective to etch β-Ga_2O_3 compared to fluorine-based dry etching [151]. Previous study compared the etch rates using the etchants of BCl_3, BCl_3/SF_6, CF_4/O_2, and BCl_3/O_2, and a maximum etch rate of 43.0 nm/min was achieved by pure BCl_3 whereas the etch rate of only 1.5 nm/min was achieved by CF_4/O_2 using similar etching power and pressure [151]. During the chlorine-based etching process, Cl radicals act as chemical etchants while Cl^+, BCl_2^+ and Ar^+ ions play a role in physical etching [152]. $GaCl_x$ is a volatile product for Ga_2O_3 under chlorine-based etches. At the same time, BCl_3 is effective to extract oxygen from Ga_2O_3 and form BCl_xO_y compounds [152].

Zhang et al. also studied the ICP etching of β-Ga_2O_3 (-201) in BCl_3/Ar chemistry and demonstrated etch rates above 150 nm/min using an RIE/ICP power combination of 60W/900W. They showed that adding Ar to BCl_3 did not change the etch rate significantly till it reaches a BCl_3/Ar flow rate of 25/15 sccm. Further increase in the Ar flow rate reduced the etch rate, which was unexpected. It is known that Ar^+ ions can help to remove the etch products and create active sites for chemical etching, which should lead to higher etch rates. However, since BCl_3 produces heavy BCl_2^+ and BCl_3^+ ions that participate in physical etching, BCl_3 itself can provide both chemical and physical etch components in the plasma and hence the addition of Ar may not result in an improvement of the etch rate and merely dilutes the plasma chemistry when the flow of Ar exceeds a certain value. To the best of our knowledge, no dry etching of α-Ga_2O_3 has not been reported before this study as following.

5.2 α-Ga_2O_3 Sample Preparation and Measurement Methods

We investigated the impact of critical ICP parameters such as BCl_3/Cl_2/Ar gas flow ratio, bias and plasma powers, and chamber pressure on etch rate and etched-surface roughness by varying one parameter within a reasonable range, while keeping others fixed. The etching time for each experiment was varied from 2 to 5 minutes.

α-Ga_2O_3 layers were grown on sapphire (0001) substrates by hydride vapor phase epitaxy (HVPE, which is a type of chemical vapor deposition (CVD) technique providing high-speed growth and high-purity crystals [153]. Sapphire (0001) substrates were used to grow the α-Ga_2O_3 on. The growth was conducted in an atmospheric horizontal reactor using gallium chloride and O_2 as the precursors. The gallium chloride was synthesized via the chemical reaction between Ga metal and HCl gas upstream in the reactor. N_2 was used as the carrier gas. The deposition temperature was fixed within the range of 525 to 650 °C. After the HVPE growth, the samples

were diced into 1×1 cm^2 pieces, cleaned in acetone, isopropanol (IPA), deionized water and blow-dried with a N_2 gun. The samples were then patterned with photoresist mask (Microchem SPR 220 (3.0) i-Line photoresist), mounted by Santovac 5 on 6", SiO_2 and Si_3N_4 coated silicon wafers.

Etching was performed in a LAM 9400 SE II, a transformer coupled plasma (TCP) system [154]. This system is equipped with a 13.56 MHz 1000W RF generator on the coil, and a 13.56 MHz 1000 W high accuracy at low output RF generator on the bias. The samples were clamped by a 700 V bipolar ESC with 8 Torr backside helium. The chuck temperature was maintained at 50 °C. Higher chuck temperature would make the etch byproducts more volatile, but at the same time it may result in the photoresist degradation.

α-Ga_2O_3 etch rates were determined by a Dektak XT stylus profilometer. Thickness of SiO_2 and photoresist films were measured using a Nanospec 6100 spectroscopic reflectometry after each etch. For each etch condition the etch rate was determined by a linear fit of three different etch durations. Etch selectivity of Si_3N_4, SiO_2 and SPR 220 with respect to α-Ga_2O_3 were calculated by dividing their etch rates by the etch rate of α-Ga_2O_3.

The surface morphology before and after etching was studied using Atomic force microscopy. The RMS surface roughness was estimated by averaging RMS surface roughness at three different spots on the etched surface. Scanning electron microscopy (SEM) was utilized to examine the quality of etched edge.

5.3 Impact of Critical ICP Parameters

5.3.1 Gas Ratio

In the first set of experiments plasma, power, bias power and chamber pressure were fixed at 500 W, 100 W, and 5 mTorr, respectively. Ar flow was maintained at 10 sccm and the ratio of BCl_3 to Cl_2 was varied while maintaining total gas flow at 40 sccm. For two BCl_3/Cl_2 gas mixtures,

we performed the etching with and without Ar to investigate the impact of Ar on etch rate, roughness and sidewall profile.

Etch rate, DC bias voltage, and corresponding surface roughness after etch for various BCl_3/Cl_2 flow rates are depicted in **Fig. 5.1**. By increasing the BCl_3 flow rate, DC bias voltage increases, leading to enhancement of bombardment energy of physical ion components, as seen in **Fig. 5.1(a)**. This enhancement resulted in faster etch rate of α-Ga_2O_3, similar to etching of β-Ga_2O_3 [151]. This is in contrast to dry etching of GaN, where Cl_2 is the primary etchant and the gas ratio of 70% Cl_2 achieves the highest etch rate [155].

As **Fig. 5.1(b)** shows, the etched-surface RMS roughness remained relatively unchanged for various BCl_3/Cl_2 gas ratios except for the case with 40 sccm BCl_3 and 10 sccm Ar. For the BCl_3/Cl_2 gas ratio of 40 sccm/0 sccm, the etch rate dropped significantly and the surface morphology degraded dramatically, leaving nano-particles on the surface (**Fig. 5.2**). This is probably due to insufficient Cl radicals (chemical etchants) and more Cl^+, BCl_2^+ and Ar^+ ions (physical etchants). Lack of sufficient chemical etchants leads to sputtering being the main etching mechanism. Interestingly, when we removed Ar from the gas mixture, the etch rate and surface

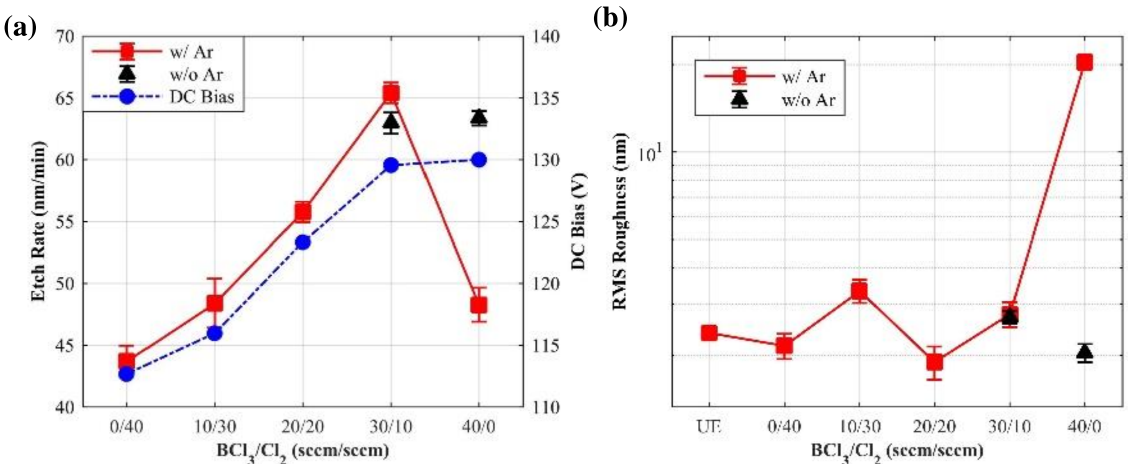

Figure 5.1 (a) Etch rate and DC bias voltage for varying BCl_3/Cl_2 ratio. (b) RMS roughness for varying BCl_3/Cl_2 ratio. In each case plasma power, bias power and chamber pressure were fixed at 500 W, 100 W, and 5 mTorr, respectively.

UE	Normal Etching	Surface damage
RMS: 2.39 nm	RMS: 2.77 nm	RMS: 20.38 nm

Figure 5.2 Surface morphology of unetched (UE) sample and samples etched at the gas ratio of 30/10/10 sccm and 40/0/10 sccm $BCl_3/Cl_2/Ar$. RMS roughness is computed as the average of three 5×5 μm^2 scans.

morphology both recovered. Ar^+ ions, as the physical etchants in the gas mixture, are expected to help to remove the etching byproducts and enhance the etch rate. Regardless, the density of physical etchants and chemical etchants must be in balance to achieve an optimum etch rate and smooth etch surface. For pure BCl_3, Cl^+ and BCl_2^+ act as physical etchants and work synergistically with Cl radicals as chemical etchants to achieve a high etch rate as well as smooth etched surface. However, by adding Ar to this gas mixture, the density of physical etchants is increased while density of Cl radicals remains relatively unaltered leading to a reduced etch rate and rough surface.

SPR, SiO_2 and Si_3N_4 mask selectivity for various BCl_3/Cl_2 gas ratios are depicted in **Fig. 5.3**. SiO_2 selectivity was 0.8 and remained roughly unaltered, whereas selectively of SPR increased from 0.2 to 1 and selectivity of Si_3N_4 increased significantly from 0.5 to 2 by reducing Cl_2 flow rate from 40 sccm to 0 sccm. This supports the idea that BCl_3 and Cl_2 contain different active species in the plasma. Similar to dry etching of GaN, Cl_2 is the primary etchant for SPR and Si_3N_4, while BCl_3 is far more effective in etching α-Ga_2O_3 and SiO_2.

The profiles of mesa structure of the samples after ICP etching at the optimal ratio of BCl_3:Cl_2 of 30:10 with and without Ar as well as pure BCl_3 and pure Cl_2 without Ar, were

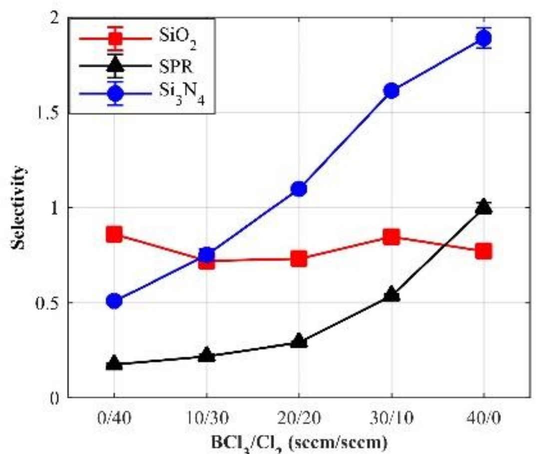

Figure 5.3 Selectivity of Ga_2O_3 with respect to SPR, SiO_2 and Si_3N_4 as a function of Cl_2/BCl_3 ratio with a constant 10 sccm Ar.

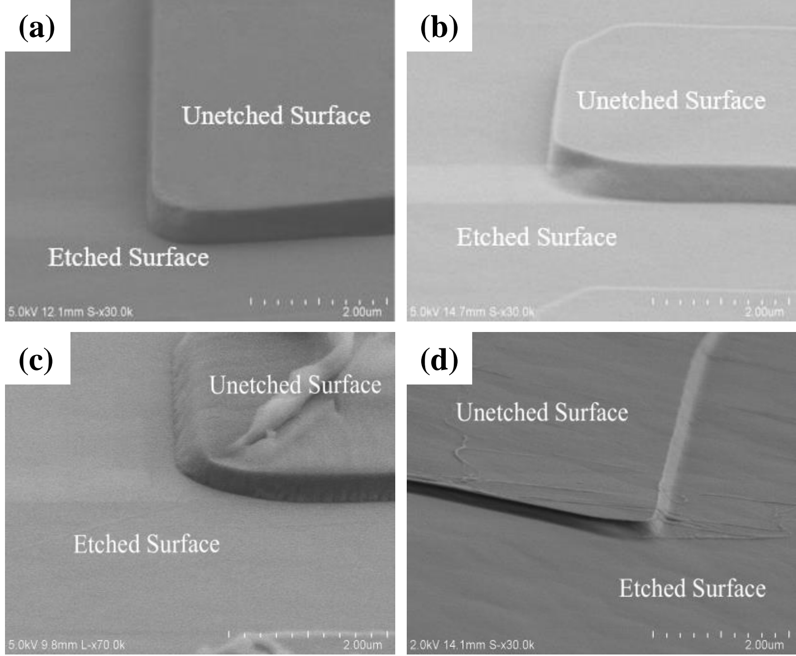

Figure 5.4 SEM images of samples etched by ICP using plasma and bias powers of 500W and 100 W with (a) 30/10/10 sccm BCl_3/Cl_2/Ar (b) 30/10 sccm BCl_3/Cl_2 (c) 40 sccm BCl_3 (d) 40 sccm Cl_2.

investigated by SEM. The images are taken after removal of the mask. As shown in **Fig. 5.4**, vertical profile and smooth surface morphology were achieved when a mixture of BCl_3:Cl_2 of 30:10 was used as oppose to etching by pure BCl_3 or pure Cl_2. The relatively round etched edge is probably due to the effect of chemical etching and mask erosion. Moreover, the addition of Ar to the etching gas mixture created a slightly more vertical etch profile.

5.3.2 Plasma and Bias Powers

In the next step, the gas mixture and chamber pressure were kept constant at BCl_3/Cl_2/Ar: 30/10/10 sccm and 5 mTorr, respectively, while the plasma and bias powers were varied. The plots demonstrated in **Fig. 5.5(a)** show that the etch rate increased roughly linearly by increasing either plasma power or bias power. It is important to note that both chemical reactive etchants and physical ion etchants coexist in a plasma. By increasing plasma power, the density of both radical etchants and ions increases. At the same time, increasing the bias power increases the energy of ions that reach to the surface. Increasing number of high-energy ions bombarding the surfaces creates more active sites on the surface and facilitate the chemical etching which leads to the etch rate enhancement.

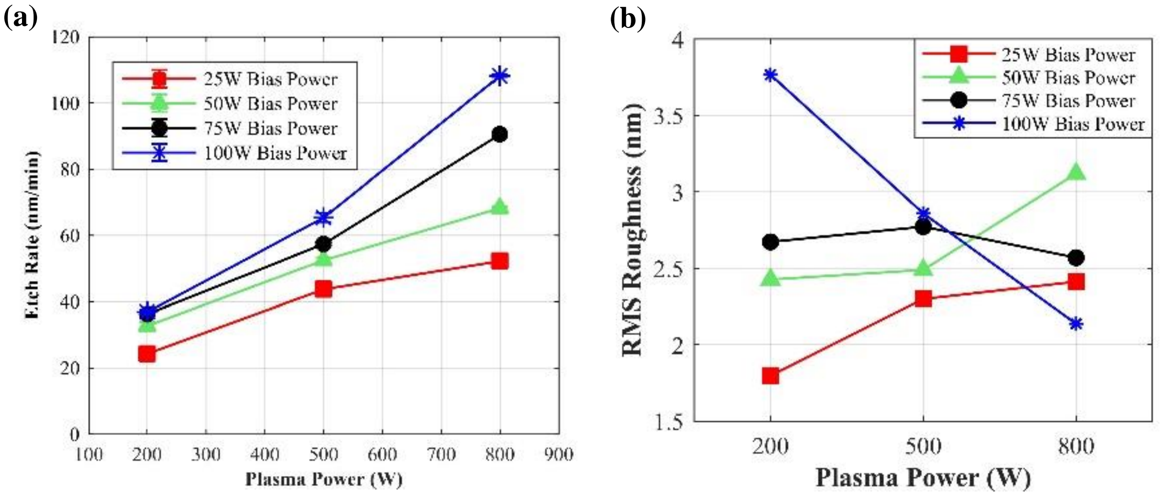

Figure 5.5 (a) Etch rate as a function of ICP plasma power. (b) RMS roughness as a function of ICP plasma power. Chamber conditions were 5 mTorr and 30/10/10 sccm BCl_3/Cl_2/Ar.

The effect of increasing plasma and bias power on the RMS roughness is shown in **Fig. 5.5(b)**. It is important to note that in ICP etching, the surface RMS roughness is lowest when the density of physical and chemical etchants are well balanced [150]. For each plasma power, the corresponding bias power to obtain an optimum combination of physical etchants and chemical etchants could be different. This explains different trends observed for RMS surface roughness as a function of plasma power for various bias powers in **Fig. 5.5(b)**.

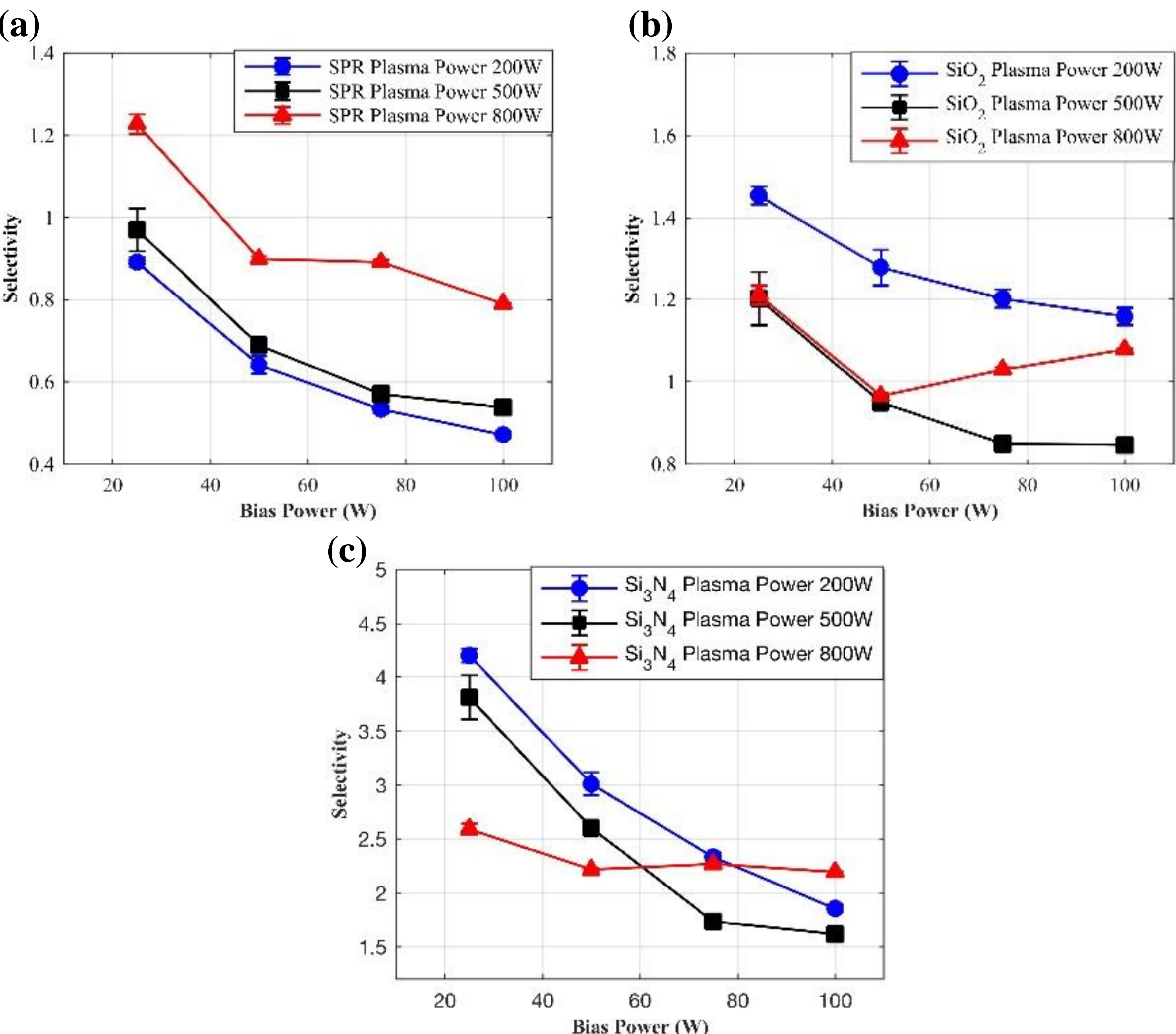

Figure 5.6 Selectivity of α-Ga_2O_3 as a function of bias power with respect to (a) SPR, (b) SiO_2 and (c) Si_3N_4. Chamber conditions were 5 mTorr and 30/10/10 sccm $BCl_3/Cl_2/Ar$.

Figure 5.6 shows the etch selectivity of α-Ga_2O_3 with respect to SPR, SiO_2 and Si_3N_4 as a function of bias power. The etch selectivity of Ga_2O_3 with respect to the photoresist, SiO_2 and Si_3N_4 falls by increasing either bias power or plasma power, except at higher plasma power. The etch selectivity reduction is due to an increase in physical etching components as the bias power increases, which results in less etch selectivity. At 800W plasma power, the selectivity levels slightly (resist and Si_3N_4) or even rises (SiO_2), driven principally by the stronger increase in Ga_2O_3 etch rate under these conditions, which is due to stronger bond dissociation energy of Si-O (799.6 kJ/mol) and Si-N (437.1kJ/mol) in comparison with Ga-O bond (374 kJ/mol) [156]. Thus, the etch rate of α-Ga_2O_3 continues to steadily increase while the etch rate of SiO_2 and Si_3N_4 is expected to increase slightly, followed by an increase of etch selectivity.

5.3.3 Pressure

In the last set of experiments, we studied the effect of chamber pressure on α-Ga_2O_3 etching while the plasma power/bias power were kept at 500W/100W and $BCl_3/Cl_2/Ar$ flow rate were kept

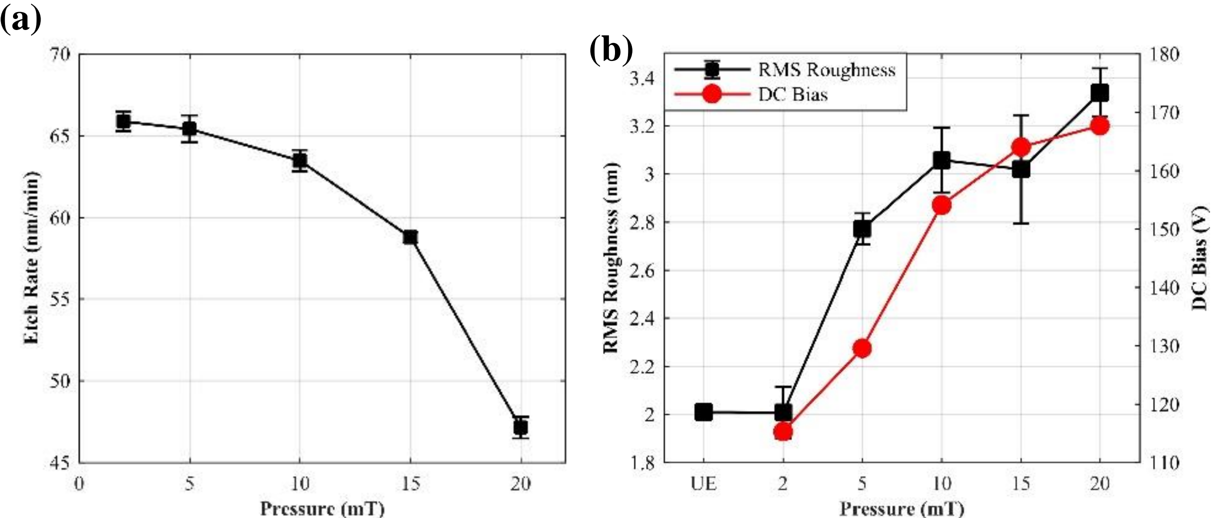

Figure 5.7 (a) Etch rate as a function of pressure. (b) RMS roughness and DC bias voltage as a function of pressure. Plasma power, bias power and gas ratio were 500 W, 100 W and 30/10/10 sccm $BCl_3/Cl_2/Ar$.

at 30/10/10 sccm. As shown in **Fig. 5.7(a)**, the etch rate decreased as the chamber pressure increased. We speculate that as the pressure in the chamber increases the scattering rate of plasma and ions in the sheath also increases which results in degradation of ion energy. It could also be explained by a fall in ion flux from the plasma source. At the same time, increasing the pressure results in a reduction in the volatility of byproducts, where the vapor pressure of $GaCl_3$ at 50 °C is 1 Torr [157], and consequently suppresses the etch rate.

As shown in **Fig. 5.7(b)**, the RMS surface roughness increases as the chamber pressure increases. This increase might result from unbalanced chemical and physical etching, in which

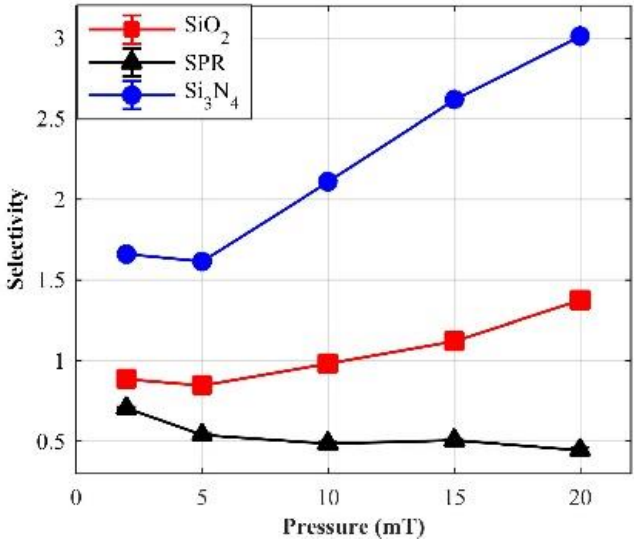

Figure 5.8 Selectivity of Ga_2O_3 with respect to SPR, SiO_2 and Si_3N_4 as a function of pressure. Plasma power, bias power and gas ratio were fixed at 500 W, 100 W and 30/10/10 sccm $BCl_3/Cl_2/Ar$.

Table 5.1 Bond energies and etch rates of Ga_2O_3, SPR, SiO_2 and Si_3N_4 using 50 sccm of Ar gas flow in a chamber pressure of 5 mTorr and plasma/bias power of 500W/100W.

ICP	Ga_2O_3	SPR	SiO_2	Si_3N_4
Bond Energy (kJ/mol)	374	/	799.6	437.1
Etch rate (nm/min)	25.6	30	20.1	25.5

ions are insufficient to create active sites for the chemical reaction, as well as sputtering to remove the protrusions and byproducts on the surface [150].

The mask selectivity for SPR, SiO_2 and Si_3N_4 were measured and are plotted in **Fig. 5.8**. The selectivity of SPR reduced, whereas the selectivity of SiO_2 and Si_3N_4 increased when the chamber pressure was increased. This is also probably due to the difference between bond energies. As is shown in **Table 5.1**, materials with higher bond energy have lower etch rates when etched by pure Ar plasma, which explains different trends of selectivity as the ion bombardment degrades at higher chamber pressure.

5.4 Summary

ICP was used to study dry etching of α-Ga_2O_3. The effect of $BCl_3/Cl_2/Ar$ gas ratio, bias and plasma powers and chamber pressure on etch rate, surface roughness and mask selectivity were investigated. In contrast to previous dry etching studies on GaN, and similar to β-Ga_2O_3, BCl_3 was found to be more effective than Cl_2 to etch α-Ga_2O_3. Additionally, the synergistic effect of Cl_2 and BCl_3 performs better than pure Cl_2 or BCl_3 in the ICP system. The high etch rate of 65 nm/min, nearly-vertical sidewalls and smooth etched surfaces were obtained at a plasma power of 500 W with a 30/10/10 sccm $BCl_3/Cl_2/Ar$ gas mixture, a bias power of 100 W and a chamber pressure of 5 mTorr. The Si_3N_4 hard mask showed the highest resistance to BCl_3-based etching compared to SiO_2 and photoresist. In general, more BCl_3 in the gas mixture, balanced plasma and bias power and lower pressure yield higher etch rates and smaller surface roughness.

Chapter 6 Heterogeneous Integration of N-polar GaN and β-Ga_2O_3

6.1 Introduction

6.1.1 Wafer Bonding

Wafer bonding is one of the packaging technologies which refers to the occurrence of adhesion between two mirror-polished surfaces [158]. The first Si-Si wafer-bonding was demonstrated in 1986 for silicon-on-insulator (SOI) applications [159]. After that, due to the flexibility in the choices of materials offered by wafer-bonding, it quickly spread into diverse applications, ranging from microelectromechanical systems (MEMS), microelectronics and optoelectronics. The commonly used and developed wafer bonding methods include direct bonding (fusion bonding), anodic bonding, eutectic bonding (using an intermediate eutectic "glue" layer), glass frit bonding (an intermediate glass layer.), adhesive bonding (using intermediate plastic agents), and thermo-compression bonding (using intermediate gold; press samples and heat in the range of 300-350 °C) [158].

Direct bonding is a wafer bonding process without any additional intermediate layers. The adhesion between two mirror-polished surfaces is mainly caused by chemical bonds when two surfaces are placed in contact. The two surfaces which should be sufficiently flat, smooth and clean. Otherwise, un-bonded areas (voids) can occur, as shown in **Fig. 6.1** [160]. The procedures of the direct bonding process can be divided into sample preparation, pre-bonding at room temperature and annealing at elevated temperatures.

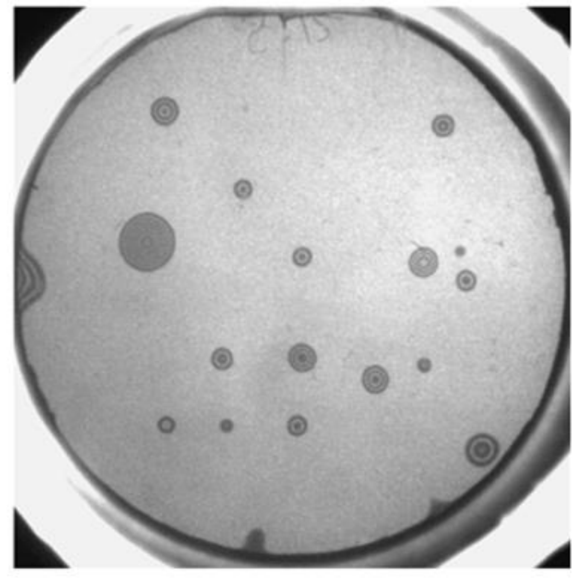

Figure 6.1 Infrared pictures for bonded Si-Si wafers with voids occurring at interface [160].

To enable low temperature bonding, surface activation method has been successfully used previously for heterogeneous bonding of various substrates [161], [162]. In this technique, surfaces of two samples are activated by atmospheric plasma treatment or ion beam bombardment, and subsequently placed into contact [163]. Specifically, atmospheric plasma treatment is effective to increase the surface energy with minimal surface bombardment to achieve bonding at low temperature [164], [165]. The ion beam bombardment employs Ar ions or neutral atoms to bombard the sample in an ultra-high vacuum which creates structural defects and may form an amorphous structure [166].

6.1.2 Sample Preparation for Bonding

The success of direct wafer bonding is critically relying on surface properties, chemical cleaning process, and ambient conditions when the bonding is performed [158]. The surfaces ready for bonding must be flat (no wafer-bow), smooth (surface roughness below 0.5 nm) and

cleaned to be free of any contaminants because the direct bonding is much more sensitive to particulates and even very small sub-micron size particulates can prevent the bond from occurring.

Sample smoothness and flatness can be achieved by chemical mechanical polishing (CMP), which is a process of smoothing surfaces with the combination of chemical etching and mechanical forces. The process utilizes an abrasive and corrosive colloid as well as a polishing pad. During CMP, the pad and sample are pressed together by a polishing jig with the slurry flowing slowly in between [167]. The polishing jig is rotated with different axes of rotation (i.e. not concentric) to improve the uniformity of the polishing. The purpose of CMP is to even out any irregular topography and reduce the surface roughness.

In addition to the surface smoothness, the area of bonded interface is extremely dependent on the number of particulates at the interface. The size of a particulate-induced void is a function of several factors, including the size of particulate, thicknesses of two samples, the stiffness of the materials, and the bonding energy of the surrounding bonded area [168]. **Figure 6.2** illustrates the particulate-induced void formed at the bonded interface. For two wafers with the same thickness t,

$$D = \left(\frac{2}{3}\frac{E}{(1-v^2)}\frac{t^3}{\gamma}\right)^{\frac{1}{4}}(2h)^{\frac{1}{2}} \tag{6.1}$$

where h is the diameter of the particle, D is the width of the void, E is the Young's modulus, v is the Poisson ratio, and γ is the bonding energy. Following this equation, for example, a 1 μm particle can form a 5 mm-diameter void in the room-temperature bonding of two 525 μm-thick silicon wafers [169]. Additionally, thinning the wafers and increasing the bonding strength through annealing (assuming the thermal conductivity of two wafers are similar to each other) can reduce the particle void diameter.

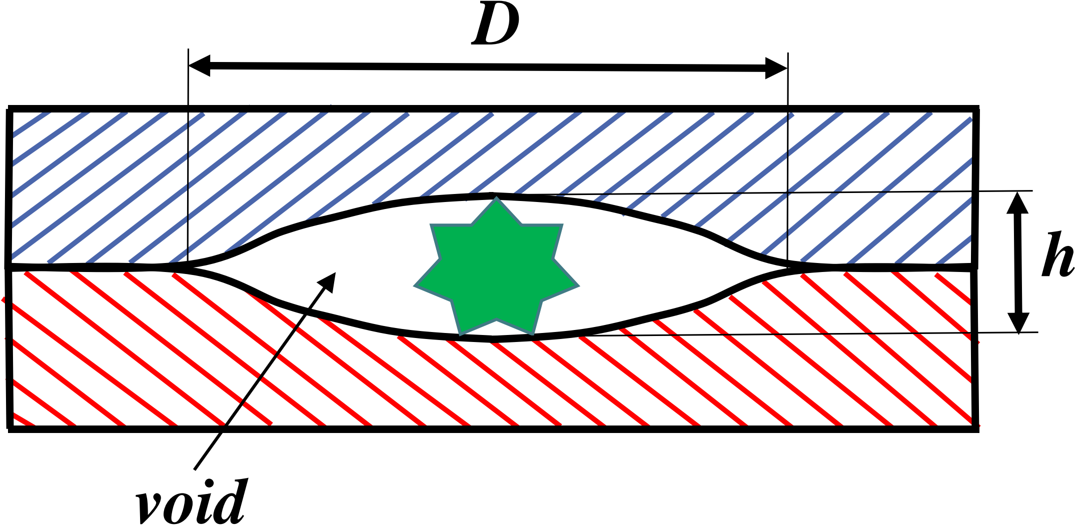

Figure 6.2 Diagram of particulate-induced void formed at the bonded interface.

There are many sources for particulates that must be considered for the bonding preparation: cleanroom air, glassware, liquid solutions, cleanroom wipes and handling tweezers. Specially, in order to not touch the sample surface and avoid any contamination, one should hold the sample on the side edge instead of surface corner using the tweezer. Thus, delicate handling and well-cleaved sample edges are very important. Additionally, the 45% cellulose/ 55% polyester blend (non-woven) cleanroom wipes are another difficult source of particulates to deal with. Particulates can adhere to the backside of the sample and transfer to the front later in the process, such as blow drying the sample with a N_2 gun. Moreover, any casual touch or contamination of sample surfaces during bonding preparation requires a thorough cleaning repeated from the beginning.

6.2 Motivation

GaN technology has been pushing the limits of power density, while providing the reliability and gain required in application [170]–[174]. To further increase the output power in

RF devices, UWBG materials have attracted interest due to their larger breakdown electric field and voltage. Regardless, each UWBG material system suffers from certain shortcomings such as unavailability of large-scale single-crystalline substrates for diamond, AlN, or c-BN. Additionally, the activation energy of dopants in these materials is relatively high. For example, activation energy of p-type and n-type dopants in diamond are ~0.37 eV [175] and 1.7 eV [176], respectively. Therefore, although theoretically a high electron/hole mobility is expected in diamond, experimentally the mobility is limited by impurity scattering and material quality. Similarly, AlN suffers from limitations of large-scale high-quality substrate and low electron mobility. On the other hand, large-scale high-quality β-Ga_2O_3 substrates can be produced by melt-growth techniques. Moreover, various n-type dopants (Sn, Ge, Si) with activation energy as low as 20 meV are available for Ga_2O_3 [177]–[181]. Nevertheless, β-Ga_2O_3 suffers from other limitations including low electron mobility and poor thermal conductivity [177]. The first β-Ga_2O_3 RF transistor was demonstrated by Green et al in 2017 [182], and device characteristics have been since improved by employing regrown contacts and reducing the gate length [34], [183]–[185]. Regardless, so far, the record f_T in such devices is only 27 GHz with a transconductance of 44 $mSmm^{-1}$ [184]. A MODFET [186] is not expected to significantly improve the device performance since the electron mobility in Ga_2O_3 is mainly limited by optical phonon scattering at room temperature and suppressing impurity scattering does not improve the room temperature electron mobility as typically observed in AlGaN-GaN and AlGaAs-GaAs heterostructures [187]–[190]s. Therefore, the nano-scale integration of β-Ga_2O_3 with GaN can potentially enable the fabrication of novel GaN/Ga_2O_3 higher power RF devices with high gain and efficiency at higher voltages combining the merits of both GaN and Ga_2O_3 [191], [192]. As an example, **Figure 6.3** shows the

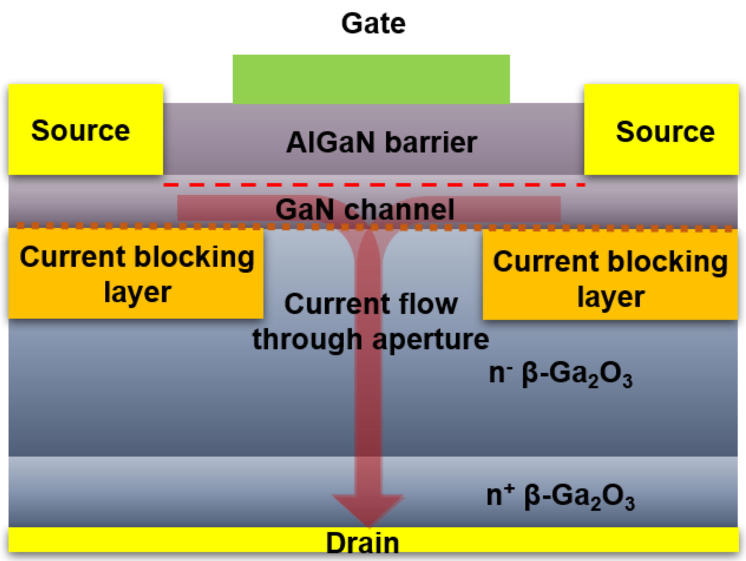

Figure 6.3 Schematic of Ga_2O_3/GaN wafer-bonded aperture vertical transistor (BAVET).

proposed GaN/Ga_2O_3 wafer-bonded aperture vertical transistor (BAVET) structure. An AlGaN-GaN HEMT structure is on top of a smooth Ga_2O_3 drain with a current blocking layer. During ON-state, the horizontal 2DEG carries current flowing from the source, through a planar gate, to the drain crossing over an aperture. During OFF-state, the 2DEG is pinched-off under the gate. A lightly doped n-type doped Ga_2O_3 drift region is utilized to hold voltage and the high field region is buried under the gate in the bulk Ga_2O_3 material. By combining the large breakdown field of Ga_2O_3 with high electron mobility of GaN, breakthrough device performance can be potentially achieved; beyond what has been demonstrated in GaN HEMTs. Apart from the power and RF applications, the availability of p-type doped GaN integrated on Ga_2O_3 can potentially enable optoelectronic applications such as deep UV photodetectors and light emitting diodes owing to their excellent radiation hardness, high thermal and chemical stabilities [193].

Regardless, hetero-epitaxial growth of high quality β-Ga_2O_3 on GaN is challenging because of their different crystal structures and mismatch in lattice constants. Considering the requirements

of large-scale transfer of high-quality Ga_2O_3 epi-structure and low temperature processing, another alternative approach is the direct bonding of β-Ga_2O_3 and GaN substrates. The traditional direct wafer bonding (fusion bonding) technology initially requires high-temperature annealing (> 600°C) which reduces the integration compatibility [194].

Bonding of Ga_2O_3 with Si, SiC and diamond has been already reported. Xu et al. reported bonding of β-Ga_2O_3 thin films onto the SiC and Si (001) substrates via a bonding interface layer, which can be an amorphous layer formed by argon (Ar) ion bombardment or an Al_2O_3 interlayer [195], [196]. The presence of an amorphous Al_2O_3 interlayer [195], [197] or a damaged layer due to ion-bombardment [198] at the bonded interface may not have any significant detrimental impact in these applications, where the goal is to improve heat extraction. However, an amorphous layer might not be desirable for applications where the bonded interface is within the active region of the device, such as in solar cells [199], [200] or BAVETs [201], [202]. Matsumae et al. demonstrated the hydrophilic bonding of an oxygen-plasma-activated β-Ga_2O_3 substrate with diamond substrate soaked in a hot Piranha solution without using an amorphous layer as a "glue" [203]. However, around 1 nm-thick lattice region was distorted at the β-Ga_2O_3/diamond interface probably due to the oxygen plasma treatment or thermal stress.

6.3 Direct Bonding

6.3.1 N-polar GaN Bonded with Ga_2O_3 (001)

Commercially available N-polar on-axis GaN substrates were used for this study. The (001) β-Ga_2O_3 wafer used for this work consisted of a 10 um-thick epitaxially grown by halide phase vapor epitaxy (HVPE) on a β-Ga_2O_3 (001) substrate. **Figures 6.4 (a) and (b)** depict the atomic force microscopy (AFM) images of the Ga_2O_3 (001) and N-polar GaN surfaces. Root-mean-square (RMS) surface roughnesses of 0.235 nm and 0.371 nm were measured on the Ga_2O_3 (001) and N-

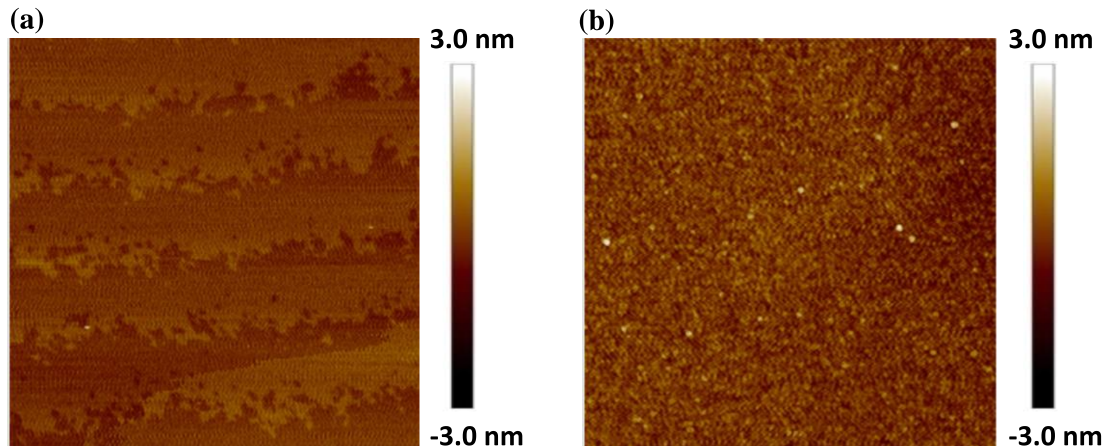

Figure 6.4 Surface morphology of Ga_2O_3 (001) and N-polar GaN. The RMS surface roughness roughnesses were 0.235 nm and 0.371 nm for Ga_2O_3 (001) and N-polar GaN, respectively.

polar GaN samples, respectively, which are suitable for the direct bonding without requiring additional chemical mechanical polishing (CMP). The wafers were then cleaved into 5×5 mm or 10×10 mm pieces. Both GaN and Ga_2O_3 samples were cleaned in acetone, isopropyl alcohol and de-ionized water, followed by the irradiation by oxygen plasma at 100W for 40 seconds in a downstream plasma descum equipment. Next, the samples were soaked in buffered hydrofluoric acid (BHF) for 30 seconds to remove surface contaminants and generate surface hydrophilic bonds, prior to surface activation using SUSS nP12 atmospheric plasma tool which improves the surface energy with minimum surface bombardment [203]. Then the β-Ga_2O_3 and GaN surfaces were placed into contact with each other and transferred to an EVG 510 bonding chamber. The bonding was conducted by a sequence of heating up to 200-400 °C for dehydration and applying the pressure of 4 MPa at 200-400 °C in vacuum for 3 hours. **Figure 6.5** shows the schematic process flow of surface activated direct bonding of Ga_2O_3 (001) and N-polar GaN substrates. The optical image of unpolished on-axis N-polar GaN bonded with Ga_2O_3 (001) is shown in **Fig. 6.6.** Newton's rings on

the right part of the sample were observed where the surfaces were not in contact with each other probably due to the concave surface and particulates on the surface. The surfaces are expected to be fully bonded if the flatness of the substrates is further improved and no cracks occurred during bonding.

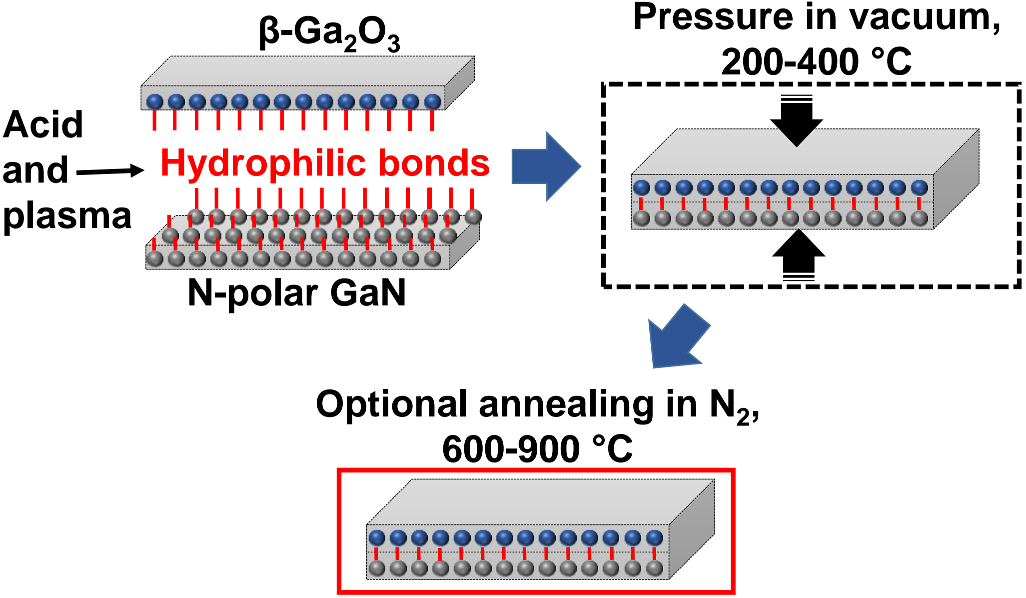

Figure 6.5 Schematic process flow of surface activated direct bonding of N-polar GaN and β-Ga_2O_3 (001) substrates.

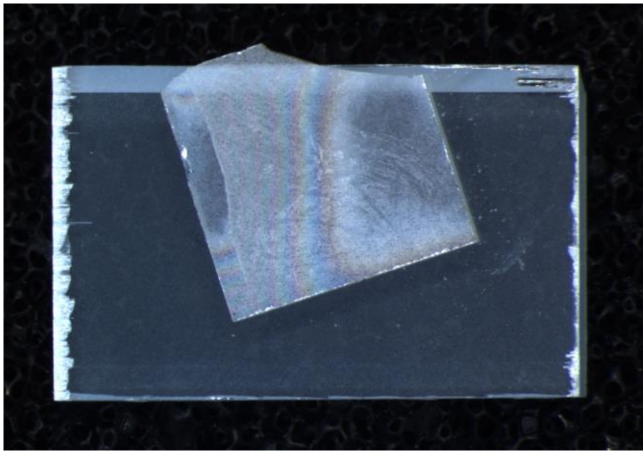

Figure 6.6 Optical images of N-polar on-axis GaN bonded with Ga_2O_3 (001).

To investigate the impact of post-annealing temperature on the quality of bonding interfaces, N-polar GaN/Ga_2O_3 (001) samples were annealed in vacuum for 15 minutes at different temperatures of 600 °C, 700 °C, 800 °C, and 900 °C with ramping up and down rates of 20C/min and 2C/min, respectively. The size and number of voids at the bonded interface was determined non-destructively using CSAM. **Figures 6.7 (a)-(e)** show the CSAM images on the bonded samples without or with various annealing temperatures. The area of voids was increased as post-annealing temperature increased from 600 °C to 900 °C. The void formation could have occurred during the temperature ramp up/down process probably due to particulates at the surface, outgassing at high temperatures and large difference between the thermal expansion coefficient of GaN (5.59×10^{-6} K^{-1}) and Ga_2O_3 (α_a=1.54×10^{-6} K^{-1}, α_b=3.37×10^{-6} K^{-1}, and α_c=3.15×10^{-6} K^{-1})

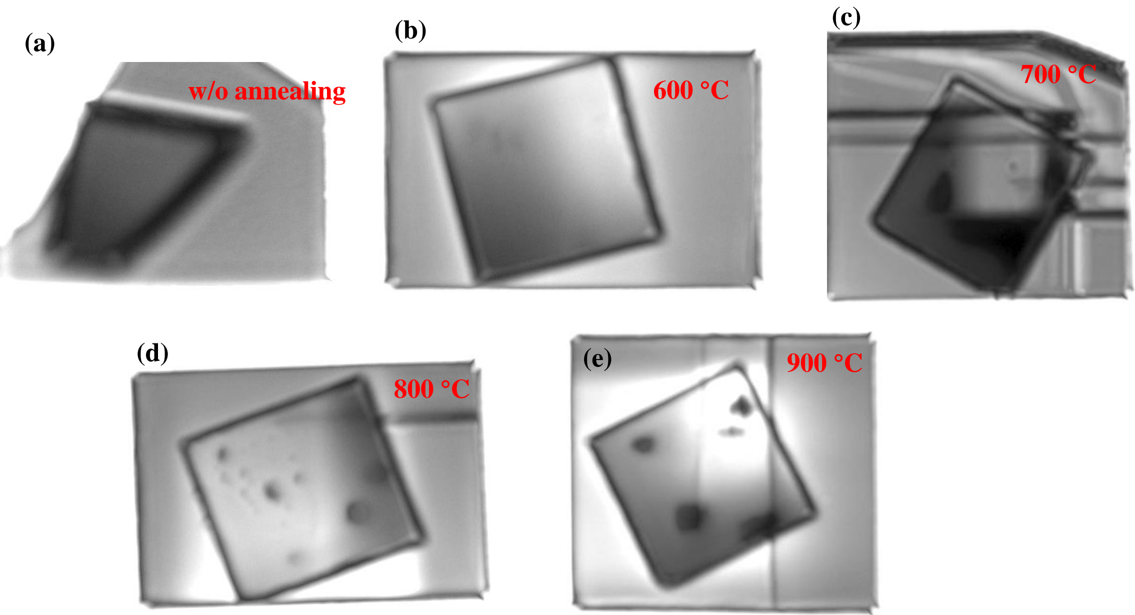

Figure 6.7 Scanning acoustic microscopy images performed on bonded samples (a) without annealing treatment, and annealing at temperatures of (a) 600 °C, (b) 700 °C, (c) 800 °C and (d) 900 °C in N_2 for 15 minutes.

[204], [205]. Reducing the ramp rate could help to mitigate this issue and will be discussed in the next section.

High resolution STEM-HAADF imaging was performed on the on-axis N-polar GaN/β-Ga_2O_3 (001) bonded interfaces. The specimens for STEM characterization were prepared by dicing followed by micro-sampling method using a Thermo-Fisher G4 650 Xe plasma dual-beam focused ion beam (FIB) instrument at the Michigan Center for Materials Characterization (MCMC) at the University of Michigan. A JEOL-JEM-3100R05 transmission electron microscope (TEM) at MCMC equipped with double aberration correctors was used for STEM imaging. **Figure 6.8 (a)** is a STEM-HAADF image taken from the N-polar GaN/(001)β-Ga_2O_3 bonded sample without annealing. The image was taken with the β-Ga_2O_3 side aligned along its [010] direction while the GaN side along a direction about 12° away from its $[11\overline{2}0]$ direction. Nevertheless, it can be seen from the image that the (001) β-Ga_2O_3 plane aligned well with the (001) GaN plane at atomic level flat which can also be seen from the FFT in the insert. **Figure 6.8 (b)** is a STEM-HAADF image taken from the N-polar GaN/β-Ga_2O_3 (001) bonded sample annealed at 900 °C in N_2 for 15 minutes. The image was taken with the β-Ga_2O_3 side aligned along its [010] direction while the GaN side along a direction about 4.4° away from its $[11\overline{2}0]$ direction. **Figure 6.8 (a)** indicates that the N-polar GaN and β-Ga_2O_3 surface can be atomically bonded without any loss in the crystallinity at the interfaces. This bonded interface without further post-annealing is almost ideal for future development of electronic and optoelectronic devices involving the β-Ga_2O_3/GaN integration. In contrast, an amorphous interlayer having a thickness of ~1.9 nm was formed between the N-polar GaN and the β-Ga_2O_3 during post-annealing at 900 °C as shown in **Fig. 6.8(b).**

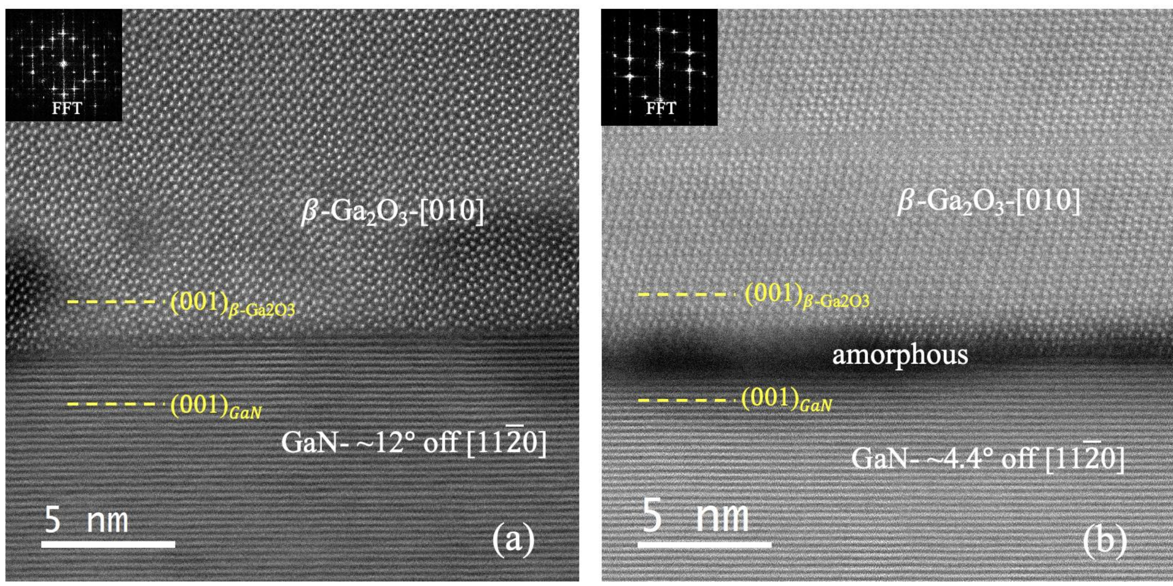

Figure 6.8 Cross-sectional STEM-HAADF images of the GaN/Ga_2O_3 (001) bonding interfaces (a) without annealing treatment, and annealing at 900 °C in N_2 for 15 minutes.

Despite the successful bonding of N-polar GaN and Ga_2O_3 (001), the bonded structure has the following issues: (i) The bonded area was only ~40% and the yield was lower than 50% probably because both GaN and Ga_2O_3 have higher mechanical hardness and any nano- or micro-roughness on the surface will lead to non-uniform bonding, which makes direct bonding more sensitive to the surface quality and roughness. (ii) The Ga_2O_3 (001) sample cracked very easily along the [100] cleavage plane when high pressure (4 MPa) was applied in the bonder. Moreover, the uneven chuck and the micro-roughness on the sample surface can increase the local pressure which exacerbated the cracking issue. Thus, we need to look for other Ga_2O_3 substrates in different crystal orientations. Currently, Ga_2O_3 substrates are commercially available in (001), (010) and (-201) crystal orientations [206]. Since the high pressure applied during the bonding can lead to Ga_2O_3 (010) sample crack along [100] and [001] orientation, we choose the Ga_2O_3 (-201) as a candidate for the rest of bonding study presented in this thesis.

6.3.2 N-polar GaN Bonded with Ga_2O_3 (-201)

Commercially available 680 μm-thick UID (-201) β-Ga_2O_3 substrate (carrier concentration ~2.3×10^{17} $cm^{-3}$and on-axis 413 μm-thick N-polar $(000\bar{1})$ GaN substrates (carrier concentration ~1×10^{18} cm^{-3})) were used for this work. **Figures 6.9(a) and 1(b)** depict the atomic force microscopy (AFM) images of the Ga_2O_3 (-201) and N-polar GaN surfaces. Root mean square (RMS) surface roughnesses of 0.20 and 0.61 nm were measured on the Ga_2O_3 and N- polar GaN samples, respectively. No additional chemical mechanical polishing (CMP) was performed on the samples prior to the bonding. The wafers were then cleaved into 5×5mm^2 or 10×10mm^2 pieces. Following the bonding process as shown in **Fig. 6.10(a)**, the direct bonding of N-polar GaN and Ga_2O_3 (-201) was also successfully achieved. A graphite sheet was added between the upper pressure chuck and sample to improve the chuck leveling and pressure balancing. N-polar GaN (5×5 mm^2) and Ga_2O_3 (-201) (10×10 mm^2) samples were fully bonded without any crack occurring in Ga_2O_3 sample as shown in **Fig. 6.10(b)**. This could be probably attributed to the different atomic arrangement and dangling bond density on the terminated surface as compared with that of (001).

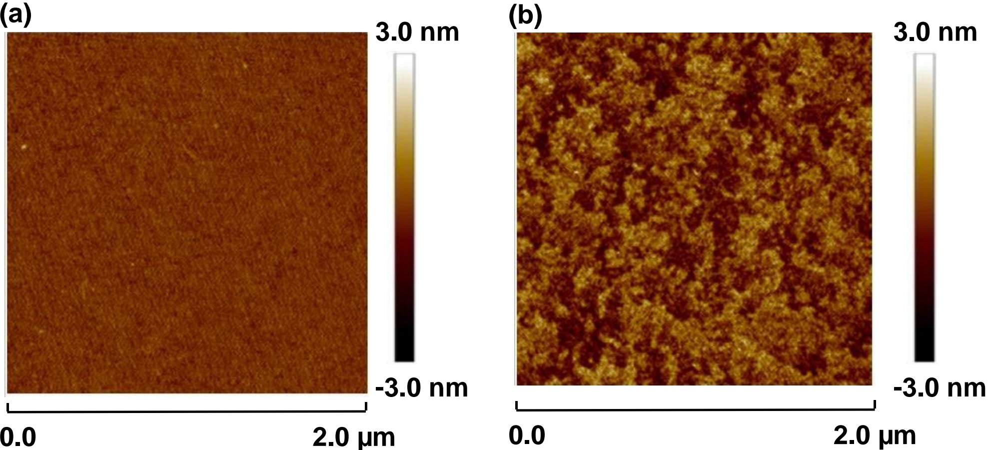

Figure 6.9 Surface morphology of (-201) Ga_2O_3 and $(000\bar{1})$ N-polar GaN substrates. The RMS surface roughnesses were 0.20 nm and 0.61 nm for (-201) Ga_2O_3 and $(000\bar{1})$ N-polar GaN, respectively.

Additionally, the strong cleavage plane of [100] is not perpendicular to the applied pressure in the bonder.

After bonding, Ti/Au (20/200 nm) was deposited on both the front and back sides of the sample. The cross-sectional schematic of the test structure is shown in **Fig. 6.11**. The electrical properties of the bonded interfaces were investigated by measuring the temperature-dependent

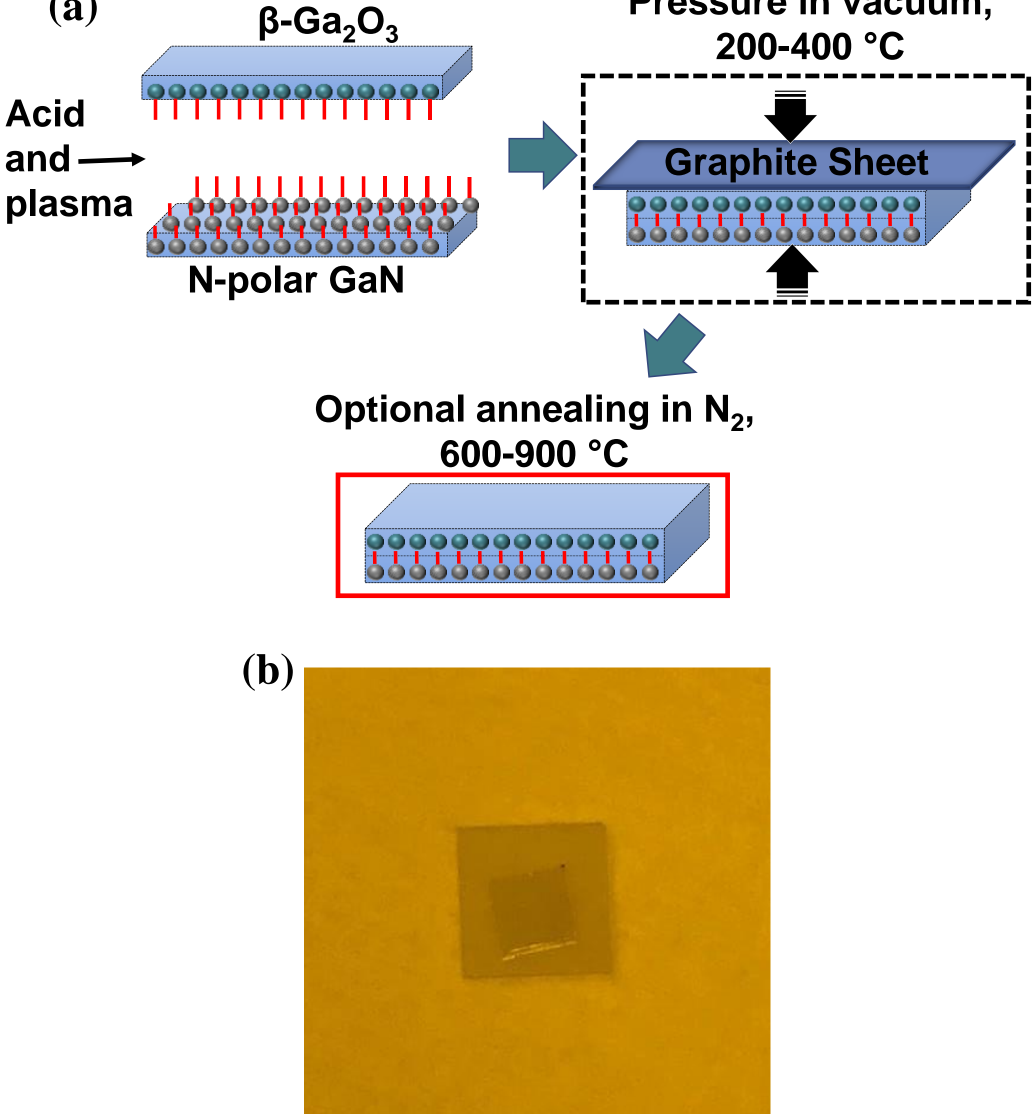

Figure 6.10 (a) Schematic process flow of surface activated direct bonding of N-polar GaN and β-Ga_2O_3 (-201) substrates. A graphite sheet was added between the upper pressure chuck and sample to improve the chuck leveling and pressure balancing. (b) Optical images of N-polar on-axis GaN bonded with Ga_2O_3 (-201).

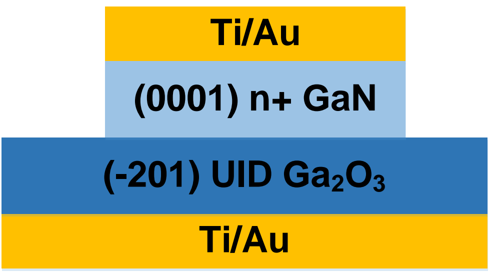

Figure 6.11 Cross-sectional schematic of the (-201) Ga_2O_3 /N-polar GaN test structure.

current-voltage (I-V-T) characteristics in vacuum using a Keysight B1500A Semiconductor Parameter Analyzer in conjunction with an MMR Technologies Variable Temperature Microprobe System. The temperature ramping rate is 2 °C/min. The Ga_2O_3 side was grounded, and the voltage bias was applied on the GaN side.

The temperature-dependent I-V characteristics were (**Fig. 6.12**) measured on the GaN/Ga_2O_3 bonded sample, in which Ga_2O_3 was grounded and the bias was applied to GaN. The

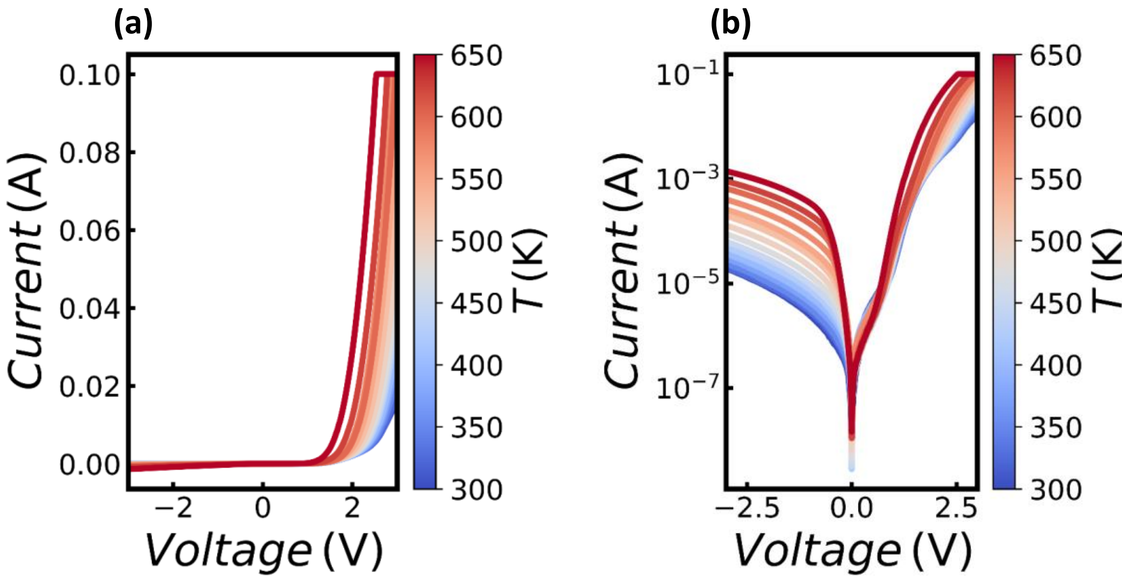

Figure 6.12 Temperature-dependent I-V measurements performed on GaN-Ga_2O_3 directed bonded sample from 300 K to 650 K. For these measurements, Ga_2O_3 was grounded and the bias was applied to GaN.

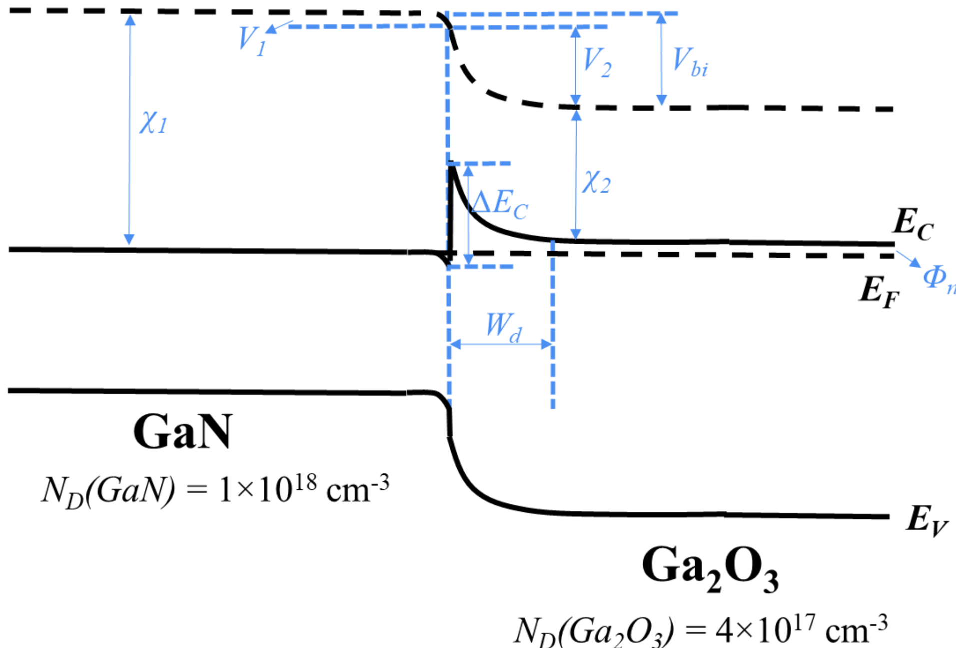

Figure 6.13 Band diagram of GaN and Ga_2O_3. The doping concentration in GaN and Ga_2O_3 bulk substrates are ~1×10^{18} cm^{-3} and ~4×10^{17} cm^{-3}, respectively.

I-V curves resemble that of a Schottky contact, indicating that there is a barrier between GaN and Ga_2O_3. A turn-on voltage of ~2.2 V was measured at room temperature which was reduced to 1.5 V at 650 K. The current density also increased by increasing the temperature as expected since more electrons have enough energy to pass the barrier.

The band diagram of GaN and Ga_2O_3 is shown in **Fig. 6.13**. A conduction band barrier forms at the GaN and Ga_2O_3 interface, which prevents electrons moving from GaN to Ga_2O_3. The build-in voltage (V_{bi}) and the depletion width (W_d) in Ga_2O_3 were calculated to be 0.54 eV and 38.7 nm, respectively, following the equations [113]:

$$V_{bi} = (\chi_1 - \chi_2) - \Phi_n = \Delta E_C - \Phi_n \tag{6.2}$$

$$W_d = \sqrt{\frac{2\epsilon V_{bi}}{qN_D}} \tag{6.3}$$

where χ is the electron affinity, Φ_n is the energy difference between Fermi level and conduction band. The theoretical band offset was calculated to be 0.6 eV from the difference of the electron affinity of GaN (4.1 eV) and Ga_2O_3 (3.5 eV) [207], [208], respectively. However, this band offset is almost always different from the theoretical calculation in practice due to the interface dipoles [209].

6.4 Bonding with a ZnO Interlayer

As discussed earlier, the direct bonding of β-Ga_2O_3 and N-polar GaN substrates was successfully demonstrated. The β-Ga_2O_3/GaN surfaces were atomically bonded without any readily identifiable loss in crystalline quality at the interface. The bonding area was only ~40% on (001) plane and almost 100% on (-201) plane. However, the bonded sample was very sensitive to the thermal treatment even though the ramping rate was as low as 2 °C/min. This hinders the fabrication of the BAVET devices as the lithography (pre- and post-baking of photoresist) is involved. Additionally, a large barrier between GaN and Ga_2O_3 prevents current flow which would be problematic for a device like BAVET. Hence, in order to increase the process window to ultimately develop large-scale wafer-bonding of β-Ga_2O_3 and N-polar GaN, ultra-high quality chemical mechanical polishing (CMP) or additional "glue" layer at the interface may need to be utilized to

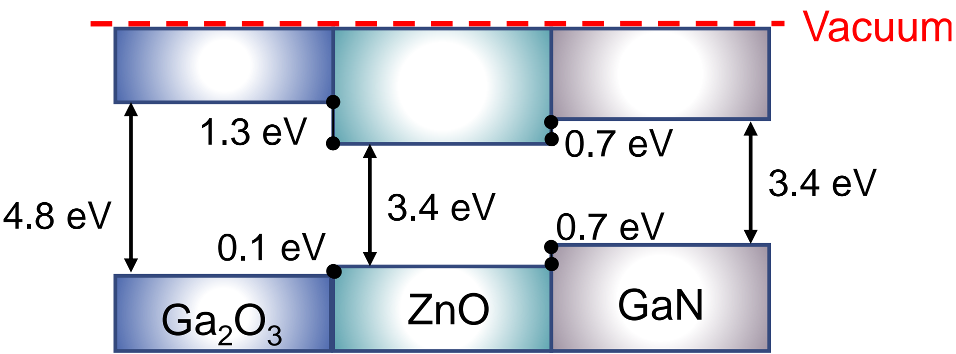

Figure 6.14 Energy level diagram of Ga_2O_3, GaN and ZnO.

enhance the bonding uniformity and strength. **Figure 6.14** shows the theoretical energy level diagram of Ga_2O_3, GaN and ZnO. The conduction band offsets between Ga_2O_3 and ZnO, and between GaN and ZnO are 1.3 eV and 0.7 eV, respectively [207], [208], [210]. In the second part of the Chapter 6, I used ZnO as a "glue" layer and investigated the temperature-dependent I-V characteristics of Ga_2O_3/ZnO/GaN test structure varying temperature from room temperature to 650 K. Additionally, the impact of high temperature annealing at 600 °C, 900 °C and 1100 °C in N_2 on the I-V characteristics was also investigated.

6.4.1 Experimental Details

Commercially available 680 μm-thick UID (-201) β-Ga_2O_3 substrate (carrier concentration ~2.3×10^{17} $cm^{-3}$and on-axis 413 μm-thick N-polar $(000\bar{1})$ GaN substrates (carrier concentration ~1×10^{18} cm^{-3})) were again used for this work. The surface morphology is depicted in **Fig. 6.9**. The wafers were then cleaved into 5×5mm^2 or 10×10mm^2 pieces. **Figure 6.15** shows the schematic process flow of the bonding of N-polar GaN and Ga_2O_3 substrates with a ZnO interlayer. Both 5×5

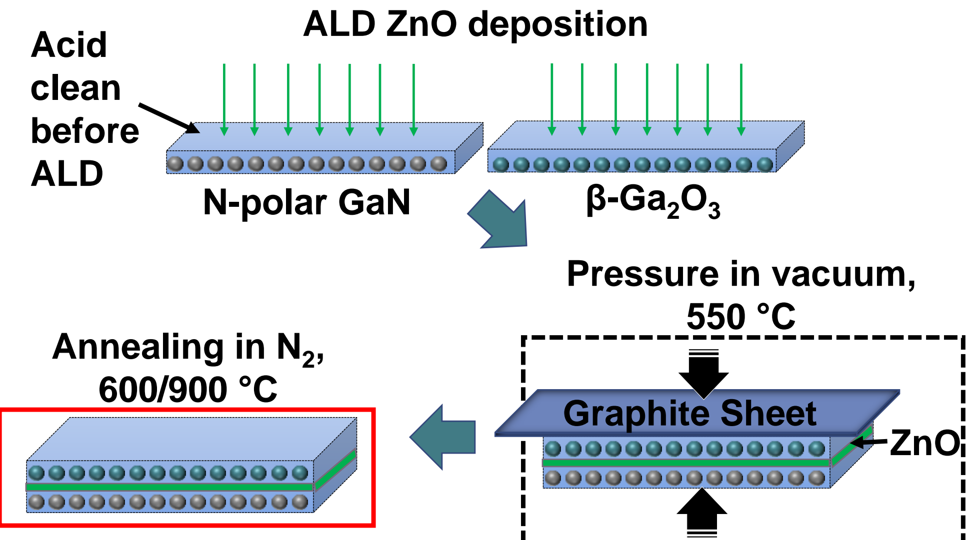

Figure 6.15 Schematic process flow of heterogeneous integration of N-polar GaN and Ga_2O_3 substrates with ZnO interlayer deposited by atomic layer deposition at 200 °C.

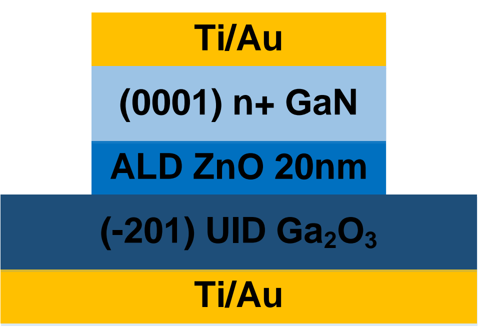

Figure 6.16 Cross-sectional schematic of the (-201) Ga_2O_3 /ZnO/N-polar

mm^2 GaN and 10×10 mm^2 Ga_2O_3 substrates were cleaned in acetone, isopropyl alcohol, and de-ionized water with ultra-sonication, followed by soaking in buffered hydrofluoric acid (BHF) for 30 seconds. The samples were then loaded immediately into the ALD chamber to minimize any surface contamination. 10 nm-thick ZnO was deposited on both N-polar GaN and (-201) Ga_2O_3 samples via thermal-ALD at 200 °C using Diethyl Zinc (DEZ) and water as the precursors. The thickness of ZnO film was measured using a Woollam M-2000 Ellipsometer on a Si monitor piece which was deposited in the same ALD chamber simultaneously with GaN and Ga_2O_3 samples. Next, the Ga_2O_3 and GaN samples were placed into contact with each other and transferred to an EVG 510 bonding chamber. The bonding was conducted at 550 °C under a pressure of 4 MPa in vacuum for 3 hours. After bonding, Ti/Au (20/200 nm) was deposited on both the front and back sides of the sample. To investigate the impact of post-annealing temperature on the quality of bonding interfaces, the N-polar GaN/ZnO/Ga_2O_3 test structure was annealed in N_2 for 30 minutes at various temperatures of 600 °C, 900 °C and 1100 °C with ramping up and down rates of 2 °C/min. It is very important to note that this low ramp rate was employed in order to minimize the void formation during annealing. As mentioned in the previous section, the ramping rate of 20 °C/min could easily create voids at the bonded interface especially for heterogeneous direct bonded samples

without any "glue" layer (**Fig. 6.7**). The cross-sectional schematic of the test structure is shown in **Fig. 6.16**.

6.4.2 Characterization of GaN/ZnO/Ga_2O_3 Bonded Structure

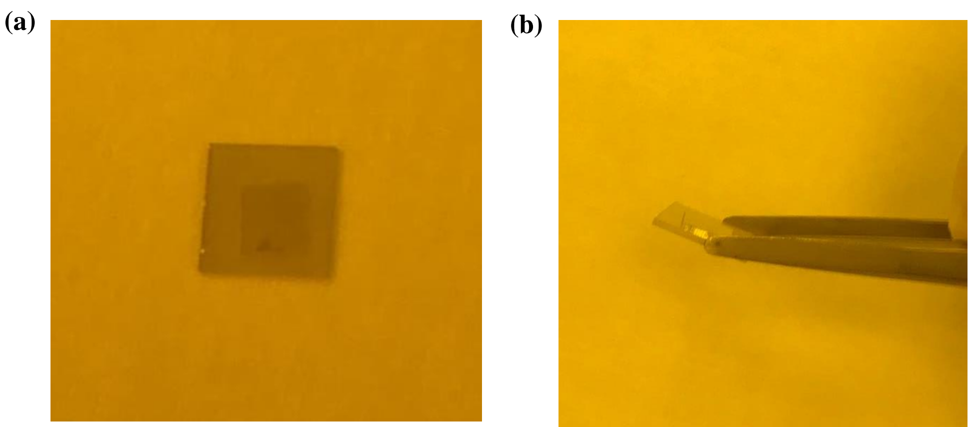

Figure 6.17 Optical (a) top-view and (b) side-view images of 10×10 mm^2 (-201) Ga_2O_3 bonded with 5×5 mm^2 $(000\bar{1})$ N-polar GaN substrates with a ZnO interlayer. The surfaces were 100% bonded.

Figure 6.17 shows the optical image of Ga_2O_3 (-201) bonded with on-axis N-polar GaN substrate. In our previous works, we demonstrated the direct bonding of Ga_2O_3 and N-polar GaN. Around 40% contact area was bonded and Newton's rings were observed where the surfaces were not in contact with each other [211]. Here, the surfaces were fully bonded. No Newton's rings were observed on the sample indicating a flat and clean interface. The 100% bonding area in this work is probably attributed to the ZnO "glue" layer, by which the bonding uniformity can be improved by the homogeneous ZnO surfaces at the bonding interface of ZnO/Ga_2O_3 and ZnO/GaN. Additionally, the hardness of ALD-ZnO thin film was reported to be 5.6 GPa [212], which is significantly lower than, the hardness of GaN (10.2 GPA) and β-Ga_2O_3 (8.9 GPa) [213], [214]. The soft 20-nm thick ZnO interlayer can probably compensate the nano-roughness on the surface, resulting in a flatter surface during bonding compared with the direct bonding.

Figures 6.18(a) and **5(b)** shows the I-V-T measurements performed on the as-bonded GaN/ZnO/Ga_2O_3 test structure at temperatures ranging from 300 K to 650 K with step increment

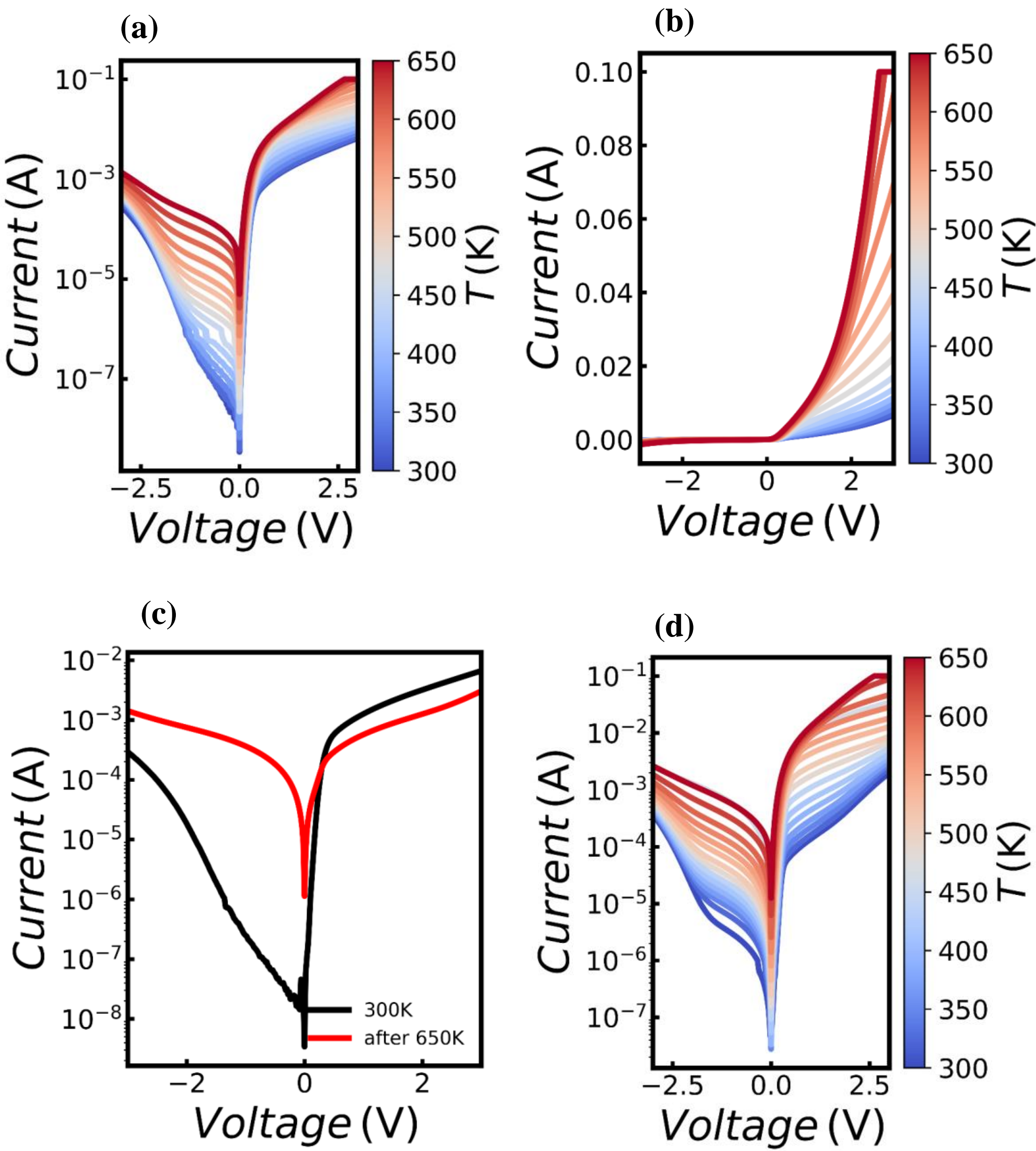

Figure 6.18 I-V-T characteristics measured at temperatures from 300 K to 650 K with step increment of 25 K for the test structure of Ga_2O_3/ZnO/N-polar GaN (a) in semi-log scale (b) in linear-scale. 5(c) I-V characteristics in semi-log scale taken at 300 K before and after temperature-dependent measurement. (d) I-V-T characteristics in semi-log scale measured after 48 hrs on the test structure of Ga_2O_3/ZnO/N-polar GaN (schottky behavior).

of 25 K. For these measurements, Ga_2O_3 was grounded, and the bias was applied to GaN. The as-bonded sample demonstrated a Schottky behavior, suggesting a barrier between GaN and Ga_2O_3, with more current flowing from Ga_2O_3 to GaN (forward bias) compared with that flowing from

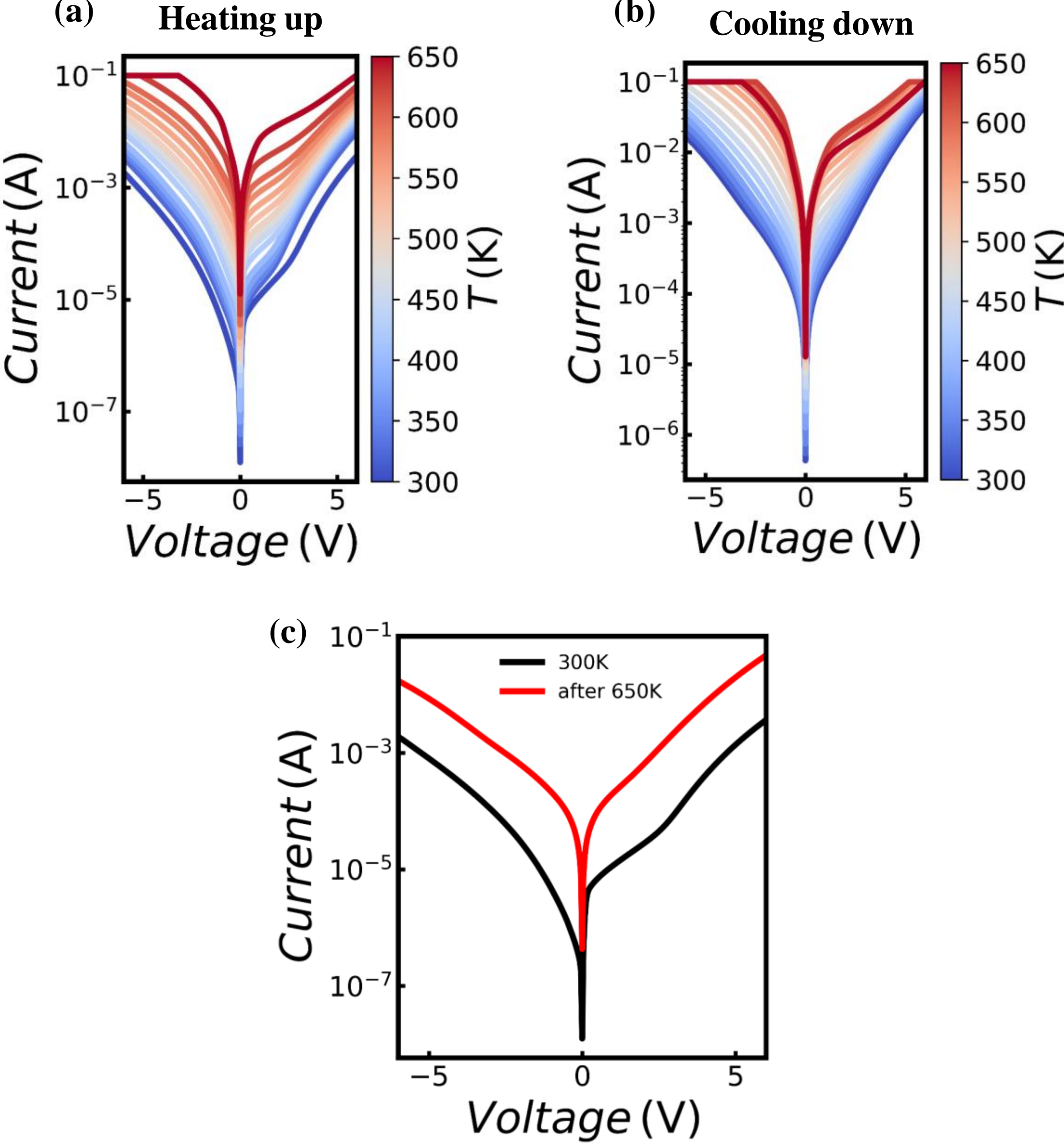

Figure 6.19 I-V-T characteristics in semi-log scale measured at temperatures (a) from 300 K to 650 K and (b) from 650 K to 300 K with step increment of 25 K for the test structure of Ga_2O_3/ZnO/N-polar GaN after annealing at 600 °C. (c) I-V characteristics in semi-log scale taken at 300 K before and after temperature-dependent measurement on the test structure of Ga_2O_3/ZnO/N-polar GaN after 600 °C.

GaN to Ga_2O_3 (reverse bias). As the measurement temperature increased, the turn-on voltage decreased, as expected for enhanced thermionic emission over the Schottky contact, at higher temperatures. A Schottky barrier of around 0.40 eV was extracted from the Richardson model. The

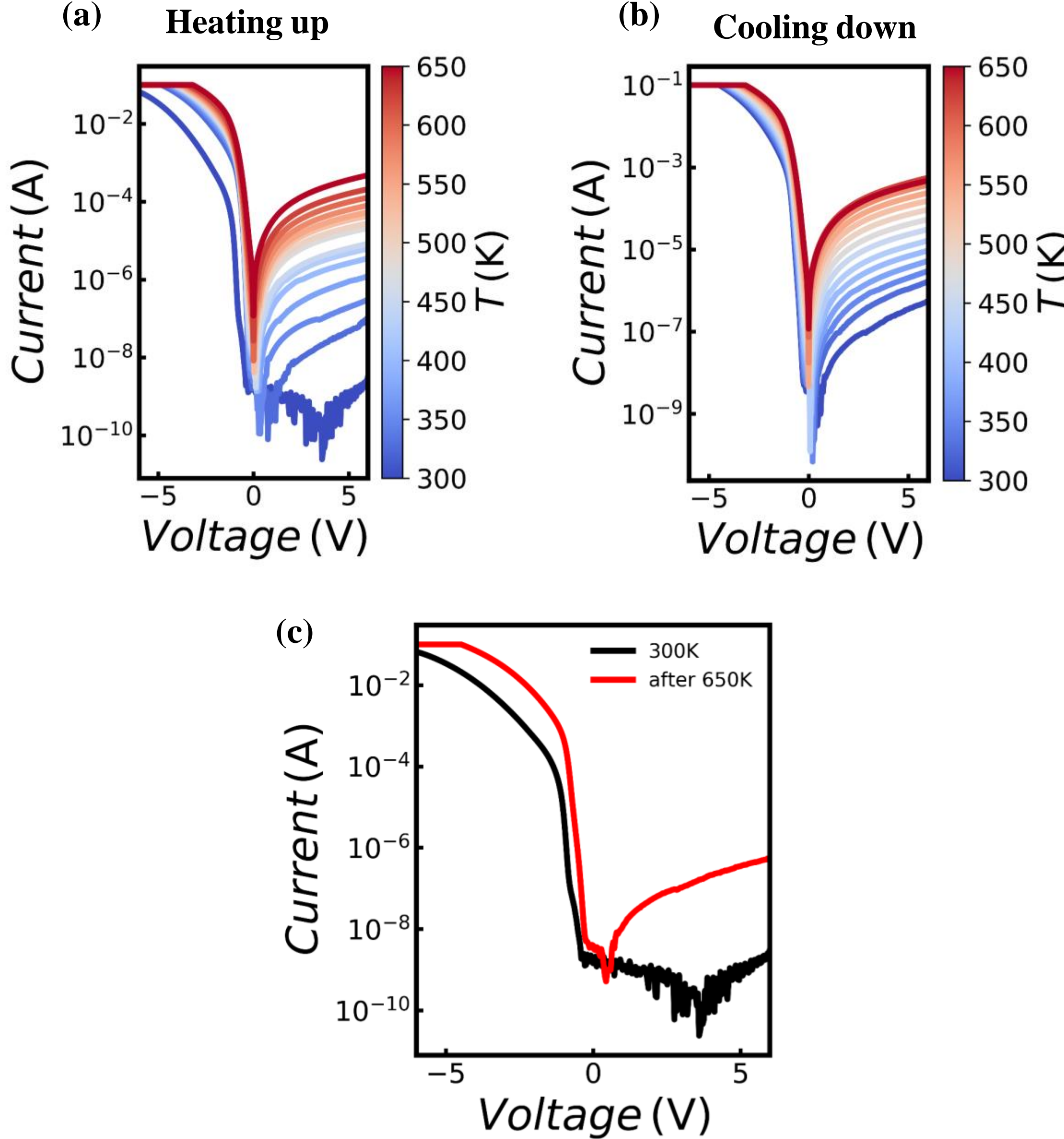

Figure 6.20 I-V-T characteristics in semi-log scale measured at temperatures (a) from 300 K to 650 K and (b) from 650 K to 300 K with step increment of 25 K for the test structure of Ga_2O_3/ZnO/N-polar GaN after annealing at 900 °C. (c) I-V characteristics in semi-log scale taken at 300 K before and after temperature-dependent measurement on the test structure of Ga_2O_3/ZnO/N-polar GaN after 900 °C.

test structure was measured again at room temperature after measurements were performed up to 650K to determine whether high temperature measurements affected the device performance. As shown in **Fig. 6.18(c)**, the test structure showed deviation of I-V curves before and after temperature-dependent measurements (up to 650 K) as compared in **Fig. 6.18(c)** and showed close to an ohmic behavior after the device was cooled down to room temperature and was measured again. However, the I-V characteristics almost recovered to its initial Schottky-like behavior after 48 hrs. This could be explained by the occupancy of ultra-slow traps in amorphous ALD-ZnO relaxing over time.

After annealing at 600 °C in N_2 for 30 min, the I-V curves showed more ohmic-like behaviors in both heating up (from 300 K to 650 K) and cooling down (650 K to 300 K) measurements (**Fig. 6.19(a) and (b)**). The maximum current density of 0.02 A/cm^2 at V_{bias} = 6 V on a test structure with ~5×5 mm^2 bonded area was measured at room temperature. The current density biased at negative voltage was increased to be a similar level to that biased at positive voltage. Then, the test structure was again measured at room temperature at the end of cooling down measurements performed from 650 K to 300 K. **Figure 6.19(c)** shows less current deviation before and after high temperature measurement compared with **Fig. 6.18(c)**. This motivates us to further anneal the devices at a higher temperature.

Surprisingly, further increasing the annealing temperature to 900 °C caused a substantial change in the I-V-T characteristics as shown in **Fig. 6.20(a) and (b)**. A significant conduction band barrier of ~ 0.21 eV occurred at the GaN/ZnO interface. High temperature measurement leads to a temporary increase in the current flowing from Ga_2O_3 to GaN at positive voltage bias, whereas less current deviation was measured when flowing from GaN to Ga_2O_3 at negative voltage bias, as shown in both **Fig. 6.20(b) and (c)**.

Figures 6.21(a) and (b) present the I-V-T characteristics of test structure measured from 300 K to 650 K and from 650 K to 300 K after 1100 °C annealing. The device demonstrated the ohmic-like characteristics. This time, only little shift of I-V curves under both positive and negative

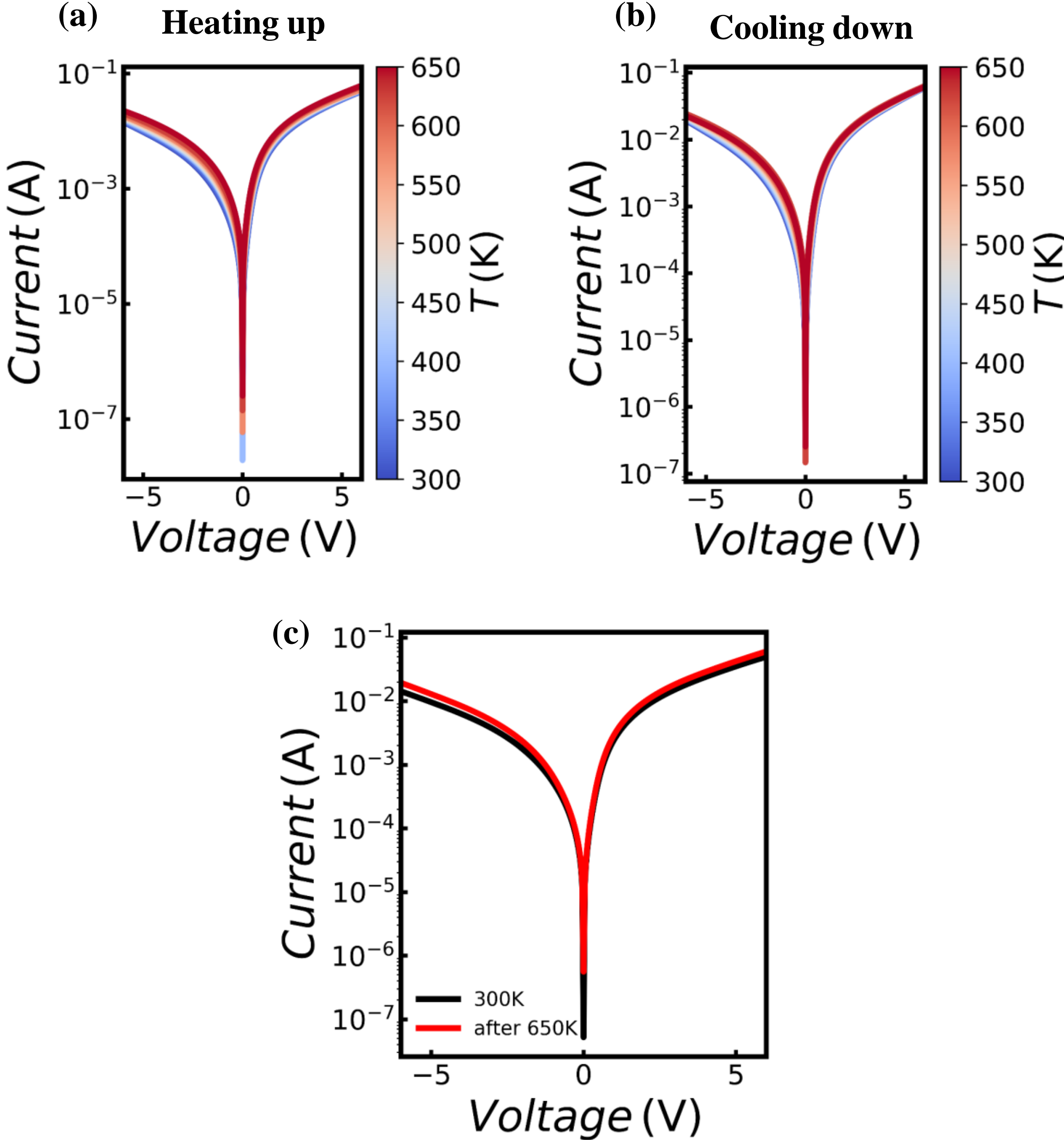

Figure 6.21 I-V-T characteristics in semi-log scale measured at temperatures (a) from 300 K to 650 K and (b) from 650 K to 300 K with step increment of 25 K for the test structure of Ga_2O_3/ZnO/N-polar GaN after annealing at 1100 °C. (c) I-V characteristics in semi-log scale taken at 300 K before and after temperature-dependent measurement on the test structure of Ga_2O_3/ZnO/N-polar GaN after 1100 °C.

voltage biases could be observed with subsequently elevated temperatures ramped up to 650 K and then ramped back down to 300 K. The maximum current density of 1.24 A/cm^2 at V_{bias} = 6 V was measured on a test structure with ~ 2×2 mm^2 bonded area. Please note that the GaN/ZnO/Ga_2O_3 sample was partially debonded during annealing at 1100 ℃. The resistance of 65 Ω were achieved at room temperature. As shown in **Fig. 6.21(c)**, the device almost preserved its I-V characteristics after high temperature measurement, exhibiting the annihilation/suppression of slow traps at the interface by 1100 °C annealing in N_2.

To understand what caused the barrier lowering, TEM and EDS element mapping were performed on the GaN/ZnO/Ga_2O_3 test structure after annealing at 1100 °C. The specimens for STEM characterization were prepared by dicing followed by micro-sampling method using a Thermo-Fisher G4 650 Xe plasma dual-beam FIB instrument. As shown in **Figs. 6.22** and **6.23**, the ZnO interlayer is fully crystallized having a Wurtzite crystal structure as if it has been grown

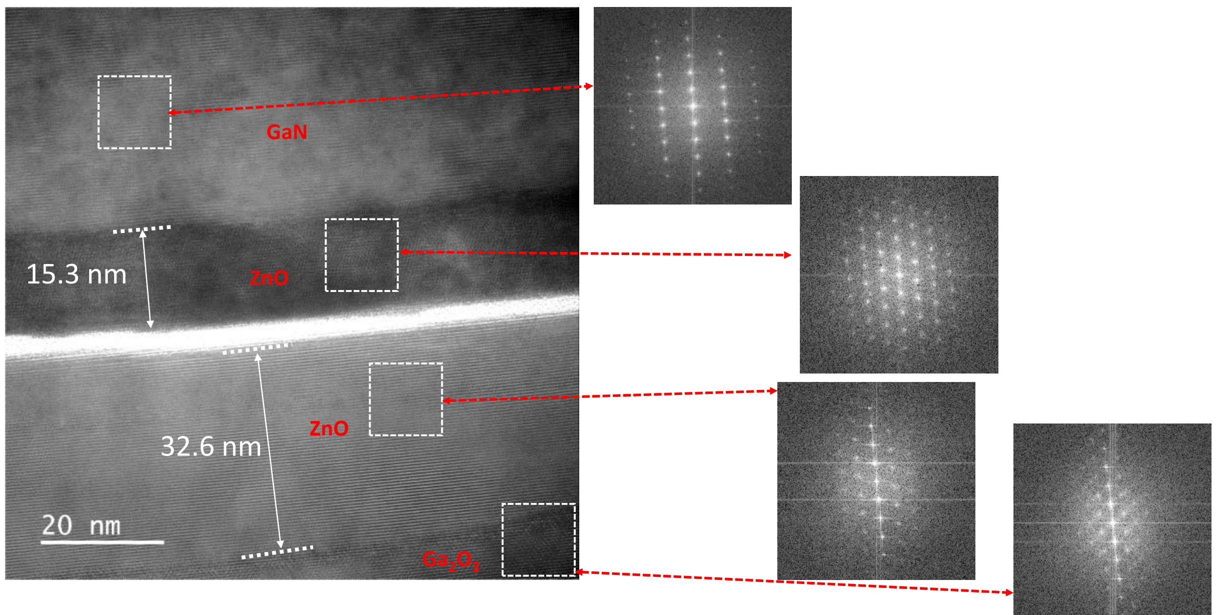

Figure 6.22 The HRTEM image was taken with the GaN crystal aligned along its [11-20]. It shows that the ZnO grown on GaN has been fully crystallized. There is a “gap” between the two ZnO layers.

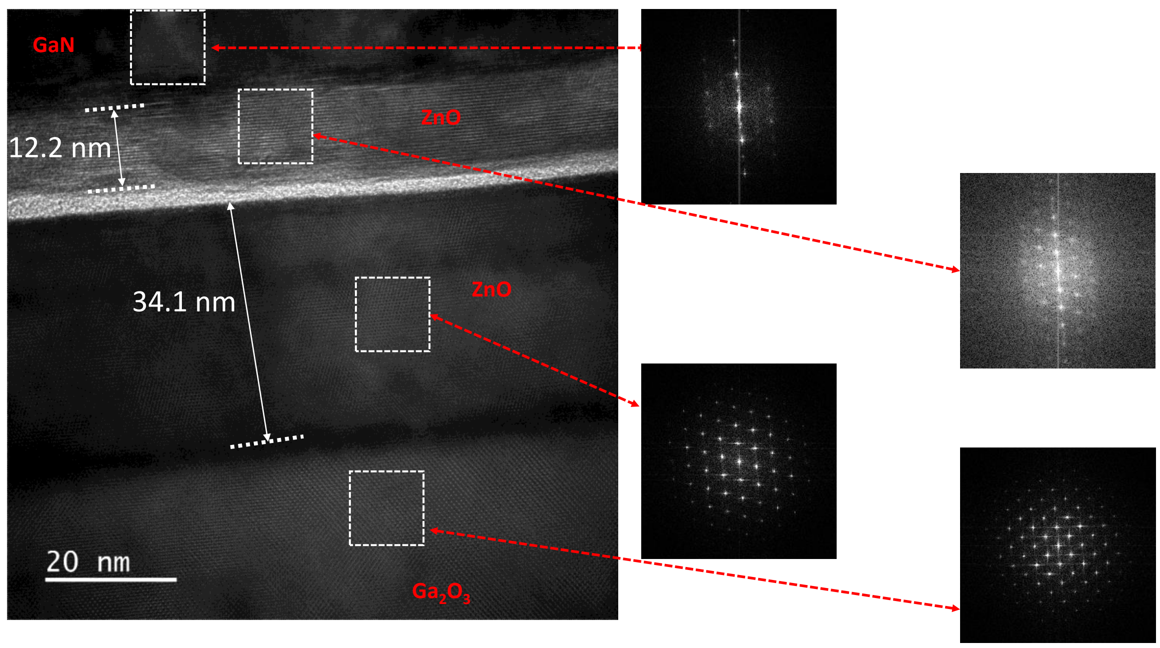

Figure 6.23 This HRTEM image was taken with the Ga_2O_3 crystal aligned along its [010]. It shows that the ZnO grown on Ga_2O_3 has been fully crystallized. There is a “gap” between the two ZnO layers.

epitaxially. In addition, ZnO is separated in two sections. The part attached to GaN has a thickness of 15.3 nm whereas the part attached to Ga_2O_3 has a thickness of 32.6 nm. This is surprising because ZnO films with equal thicknesses of 10 nm were deposited on GaN and Ga_2O_3 by ALD. The reason could be an increase in the volume due to the crystallization and reordering of atoms. Additionally, the ZnO attached GaN has a different crystal orientation compared with that of the ZnO attached to Ga_2O_3. This could be because ZnO crystallization process starts from two sides; one side that has interface with GaN and one side that has interface with Ga_2O_3, and since the underlying “seed” crystal has different orientations, ZnO crystallizes in two different orientations. We surmise that the shear stress caused by two different crystal orientations of ZnO results in the observed separation of the ZnO film. This means that instead of bonded interface being the plane of debonding as one may expect, the ZnO cracked and separated at the point where the two ZnO films with different crystal orientations meet. **Figure 6.24** shows the dark field and bright field of STEM and various

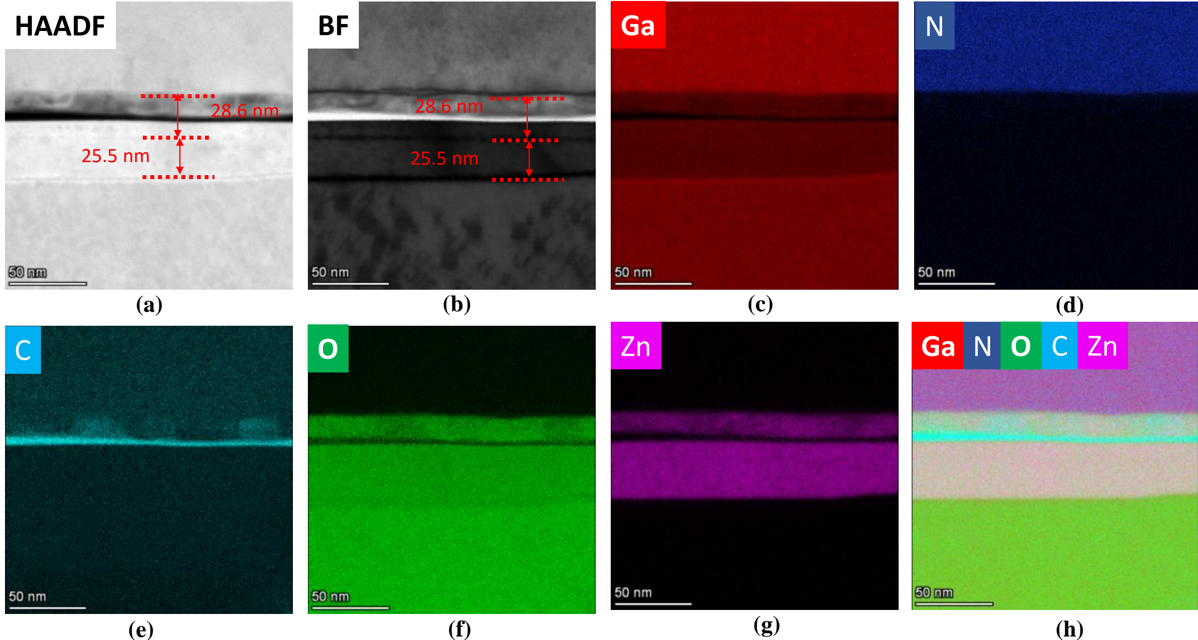

Figure 6.24 High-angle annular dark field (HAADF), bright-field (BF) scanning transmission electron microscopy (STEM), and element mapping.

element mappings. As shown in **Fig. 6.24(c)**, Ga has diffused into ZnO. Ga is a shallow n-type doping for ZnO and so this could lead to the ZnO becoming n-type, which combined with an intermixing of the interface can be contributing reasons for the barrier between GaN and Ga_2O_3 to be reduced as witnessed from the I-V characteristics.

To characterize the trap density in the Ga_2O_3/ZnO/GaN bonded structure after the crystallization of ZnO, the pulsed I-V measurements were performed on the test structure. The waveform of the pulsed voltage is shown in **Fig. 6.25(a)**. The voltage peak amplitude was swept from -6 to 6 V with a step size of 100 mV. The base voltage and pulse period used for the pulsed I-V measurements were 0 V and 10 ms, respectively. The rise and fall time were both 100 ns. Various pulse widths of 5, 10, 20, 50 and 100 μs were set in the measurement. The measurement was taken at the end of each pulse width (~5 μs).

Figure 6.25(b) presents the pulsed I-V characteristics measured at room temperature. Since coplanar waveguide probes with ground-signal-ground (GSG) could not be used on these devices,

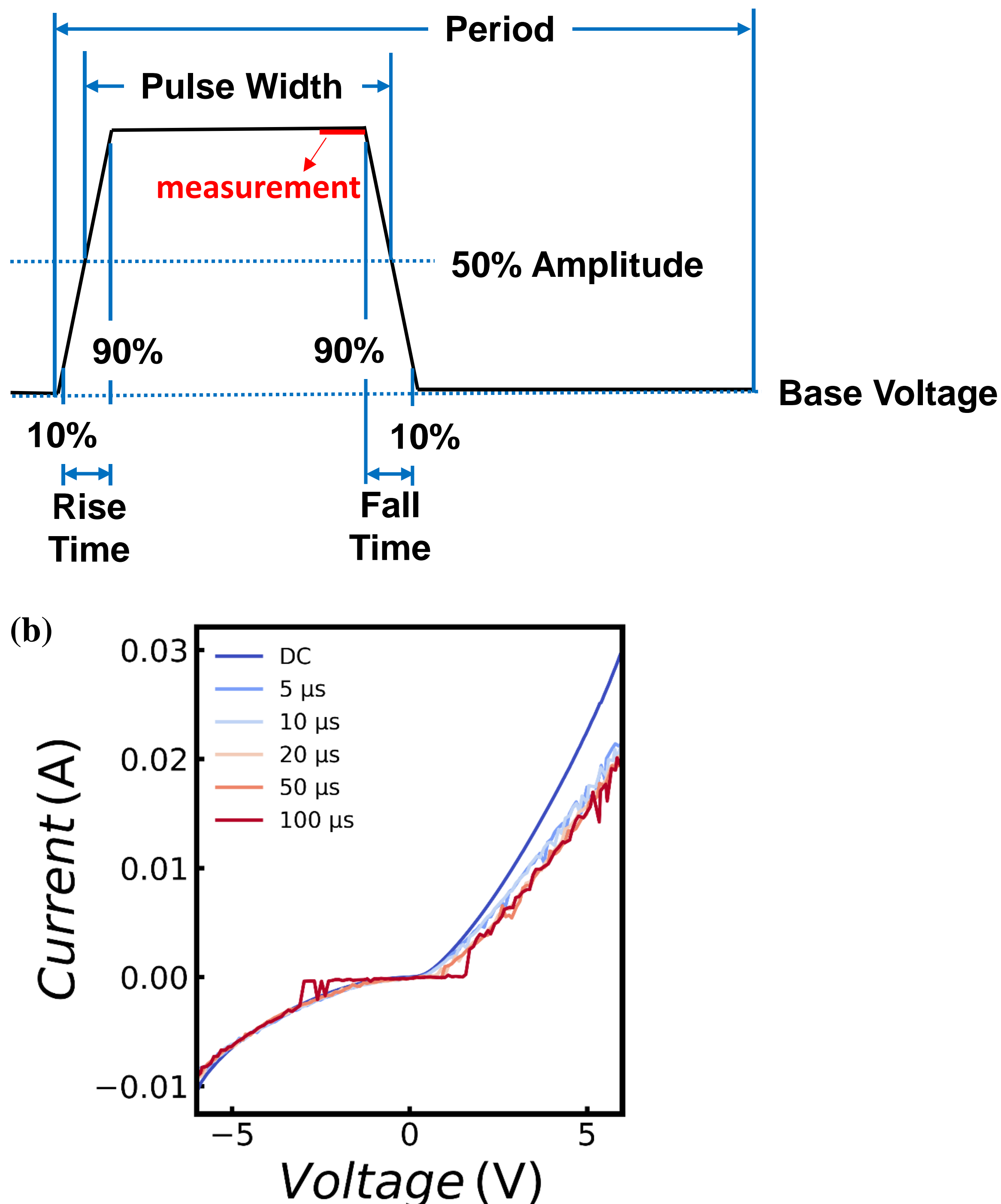

Figure 6.25 (a) Pulsed voltage waveform used for pulsed I-V measurement (b) DC and pulsed I-V characteristics with various pulse widths of 5, 10, 20, 50 and 100 μs.

the needle probes were instead used which caused noise valleys in the I-V curves. The pulsed current was slightly lower than that of the DC current which indicates the existence of traps at the interface/bulk. Additionally, although the DC I-V characteristics was ohmic-like, a turn-on voltage was observed on the pulsed I-V profile. This "trap-filled limit voltage" means that until a certain voltage, the supplied current only fills the traps in ZnO, once all traps are filled, the current can pass through the junction and that could be the reason for a sharp jump in the current at a certain voltage (V_{TFL}). The average bulk trap density was estimated to be 4×10^{18} cm^{-3} using the following equation:

$$\frac{qN_tL^2}{2\epsilon} = V_{TFL} \tag{6.4}$$

where L is the ZnO thickness and N_t is trap density (assumed to be uniform).

6.5 Summary

In the first part of this chapter, β-Ga_2O_3 and N-polar GaN substrate activated with acid and atmospheric plasma treatment were directly bonded by annealing at 200-400 °C under vacuum condition. Post-annealing at temperatures higher than 700°C increases the area of voids at bonded interfaces. This could be explained by a high ramp up rate (20 ℃/min) which leads to the void generation caused by the large difference between the thermal expansion coefficient of GaN and Ga_2O_3. The analysis of interface structures revealed that the β-Ga_2O_3/GaN surfaces were atomically bonded without any loss in crystalline quality. In the second part of this chapter, using a 20-nm thick ALD ZnO as a "glue" layer helped to achieve a fully bonded interface. No Newton's rings were observed on the sample which indicates a flat and clean bonded interface. Extensive temperature-dependent I-V measurements were conducted on the as-bonded Ga_2O_3/ZnO/N-polar GaN test structure and after annealing at 600, 900 and 1100 °C. A consistently ohmic-like characteristic was achieved by annealing the bonded wafers at 1100 °C in N_2, which is probably

due to crystallization of ZnO and diffusion of Ga into ZnO which makes it n-type doped. An average bulk trap density of 4×10^{18} cm^{-3} were quantified using pulsed I-V measurements.

Chapter 7 Conclusion and Future Work

7.1 Summary of Current Work

The research presented here was focused on the understanding and resolving the fundamental issues severely limiting the performance of β-Ga_2O_3 high power transistors by a combination of device design, fabrication process and materials growth techniques.

An introduction into the high power applications and suitable material candidates were presented in Chapter 1. The Ga_2O_3 material system is unique in that it has an ultra-wide bandgap (4.8 eV), high breakdown field (~8MV/cm), and a relatively wide n-type doping range (10^{16}-10^{20} cm^{-3}). Additionally, the melt growth techniques are available for β-Ga_2O_3 to produce high-quality low-cost substrate. Current progress in Ga_2O_3 based power transistors in various device geometries were also discussed.

Chapter 2 investigated the impact of temperature on the electrical characteristics of Ga_2O_3 trench SBDs compared with and regular SBDs fabricated on the same wafer. The trench SBDs showed superior thermal stability when devices operated at high temperatures up to 650 K. The trench SBDs were maintained highly rectifying (ON/OFF current ratio 10^5) performance at 650 K, which was four orders of magnitude higher than that in the regular diodes. I-V characteristics of the trench SBDs were recovered when the sample was cooled to room temperature after high temperature measurements, whereas the I-V characteristics of the regular SBDs were degraded. The results archived in the work showed promises for the development of the emerging Ga_2O_3 technology with potential applications in harsh environments.

Chapter 3 reported two gate dielectrics Al_2O_3 and AlSiO for enabling high-performance Ga_2O_3 FETs. MOSCAPs were fabricated and the deep UV-assisted capacitance-voltage measurements were developed to characterize the interfacial and bulk properties of dielectrics. Various surface pre-treatment and post-metallization techniques were compared. An average interface state density of 6.63×10^{11} cm^{-2} eV^{-1} was quantified on MOCVD-grown AlSiO/Ga_2O_3 MOSCAPs, which is half of that measured on ALD-deposited Al_2O_3/Ga_2O_3 MOSCAPs. Furthermore, the critical electric field of gate dielectric AlSiO was enhanced up to 8.2 MV/cm by post-metallization annealing at 350 °C. This record-high value is even higher than that of underlying Ga_2O_3 (8 MV/cm), which is helpful for taking advantage of the full potential of Ga_2O_3 for high power applications.

Chapter 4 presented switching performance analysis of a novel normally-off 3.5 kV β-Ga_2O_3 power FinFET using Silvaco TCAD simulation platform. For the first time, the impact of electron mobility in the channel and drift region, substrate thickness and fin width/pitch size ratio on the off-state capacitances and switching performance were studied. The total power loss of the input power at frequency of 200 kHz was reduced 82.2% for the demonstrated device structure with fully-filled inter-fin design. These findings provided helpful insights for design and fabrication of Ga_2O_3 FinFETs with enhanced switching performance for low-waste power conversion applications.

Chapter 5 developed inductively-coupled plasma dry etching technique for α-Ga_2O_3. For the first time, the high etch-rate etching conditions with low surface damage and smooth etch surface morphology was achieved for α-Ga_2O_3. The effect of BCl_3/Cl_2/Ar gas ratio, bias and plasma powers and chamber pressure on etch rate, surface roughness and mask selectivity were investigated. In contrast to previous dry etching studies on GaN, and similar to β-Ga_2O_3, BCl_3 was

found to be more effective than Cl_2 to etch α-Ga_2O_3. Additionally, the synergistic effect of Cl_2 and BCl_3 performs better than pure Cl_2 or BCl_3 in the ICP system. The Si_3N_4 hard mask showed the highest resistance to BCl_3-based etching compared to SiO_2 and photoresist.

In order to address the main challenges of Ga_2O_3 such as its relatively low electron mobility and current unavailability of p-type doping, for the first time, the heterogeneous integration of N-polar GaN and Ga_2O_3 substrates were demonstrated in Chapter 6. The TEM analysis of interface structures revealed that the Ga_2O_3/GaN surfaces were atomically direct bonded without any loss in crystalline quality. Using a 20-nm thick ALD-ZnO as a "glue" layer helped to achieve a fully bonded interface. No Newton's rings were observed on the sample which indicates a flat and clean bonded interface. Extensive temperature-dependent I-V measurements were conducted on the as-bonded Ga_2O_3/ZnO/N-polar GaN test structure and after annealing at 600, 900 and 1100 °C. A consistently ohmic-like characteristics was achieved by annealing the bonded wafers at 1100 °C in N_2. The integration of Ga_2O_3 and N-polar GaN substrates is promising for the development of novel GaN/Ga_2O_3 higher power RF devices with high gain and efficiency at higher voltages combining the merits of both GaN and Ga_2O_3.

7.2 Future Work

The results of this dissertation have expanded the available knowledge of Ga_2O_3-based power devices and have opened avenues for future work. I suggest several ideas for future researchers to pursue in the hopes of furthering energy security and sustainability for the benefit of society:

1. Ga_2O_3 power FinFETs

(i) Channel mobility after dry etching - Dry etching damage during mesa isolation and device processing causes surface roughness and interface-trapped charge that are detrimental for

device operation. Different techniques such as wet etching, MBE polishing and regrowth, and dielectric passivation can be utilized to eliminate the dry etching damage on the Ga_2O_3 and improve the channel mobility of the devices.

(ii) AlSiO as a gate dielectric - MOCVD-grown AlSiO was proposed for β-Ga_2O_3 in this dissertation. The negligible hysteresis, low interfacial trap density, low leakage current, and high breakdown electric field were achieved on AlSiO/Ga_2O_3 MOSCAPs. TEM/SIMS analysis can be performed on the of AlSiO/Ga_2O_3 interface to identify the structural cause of low interface states. This AlSiO gate dielectric can also be utilized in the FinFET devices.

(iii) Device geometry - The TCAD simulation results showed that the Ga_2O_3 power FinFET with a thicker Al_2O_3 dielectric in the planar regions and low-k SiO_2 fully-filling the inter-fin area can achieve smaller junction capacitances and superior switching performances. The device design developed in the dissertation can be easily incorporated into the Ga_2O_3 FinFET processing. For example, the fully-filled SiO_2 layer in the inter-fin area can be uniformly deposited by tetraethylorthosilicate (TEOS)-PECVD. The thicker Al_2O_3 (or AlSiO) dielectric in the planar regions can be achieved by adding additional step of planarization.

2. Ga_2O_3/GaN BAVETs

Composite device structures with Ga_2O_3/GaN can enable new frontiers of technological advancements by utilizing high voltage blocking capability of Ga_2O_3 and high mobility and thermal capability of GaN. However, this is a mammoth task since the Ga_2O_3/GaN bonded interface has to be pristine and the barrier to electron transport need to be minimized. Schottky diodes can be fabricated as a second test structure on n^- GaN/n^- Ga_2O_3 bonded materials. Temperature-dependent C-V, I-V and DLTS can be utilized to characterize the bonding interface

states. Surface-activating treatments and annealing in H_2, N_2, forming gas and/or O_2 can be further explored to improve the interface quality.

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