ADVANCED ELECTRONIC MATERIALS

Supporting Information

for *Adv. Electron. Mater.,* DOI: 10.1002/aelm.202200005

An Epitaxial Ferroelectric ScAlN/GaN Heterostructure Memory

Ding Wang, Ping Wang, Shubham Mondal, Subhajit Mohanty, Tao Ma, Elaheh Ahmadi, and Zetian Mi**

Supporting Information

An Epitaxial Ferroelectric ScAlN/GaN Heterostructure Memory

Ding Wang, Ping Wang, Shubham Mondal, Subhajit Mohanty, Tao Ma, Elaheh Ahmadi, and Zetian Mi**

Dr. D. Wang, Dr. P. Wang, S. Mondal, S. Mohanty, Prof. E. Ahmadi, Prof. Z. T. Mi,
Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, MI 48109, USA
E-mail: piwang@umich.edu, ztmi@umich.edu

Dr. T. Ma
Michigan Center for Materials Characterization (MC)2
University of Michigan
Ann Arbor, MI 48109, USA

1. Comparison of common ferroelectric materials with ScAlN

Materials	PZT	BTO	BFO	HfO_2-ZrO_2	ScAlN	ScGaN
P_r ($\mu C/cm^2$)	20-40	5-10	90-95	10-40	80-120	60-100
E_C (kV/cm)	~ 50	30-50	100-1500	80-2000	1500-6000	2000-3000
ε_r	~ 400	~ 200	~ 50	~ 30	12-20	~ 11
N (cycles)	$>1\times10^{15}$	$>1\times10^{10}$	$>1\times10^{11}$	$>1\times10^{11}$	$>1\times10^{7}$	$>1\times10^{3}$
E_g (eV)	~ 3.5	~ 3.28	2.2~ 2.7	4.3-5.9	4.9-5.7	~ 4.2
T_C (℃)	~ 400	~ 400	~ 700	0-500	>600	>430

Table S1. Comparison of Sc-III-N ferroelectrics with conventional ferroelectric materials.[1-6]

2. Stability of PFM patterns after litho-writing

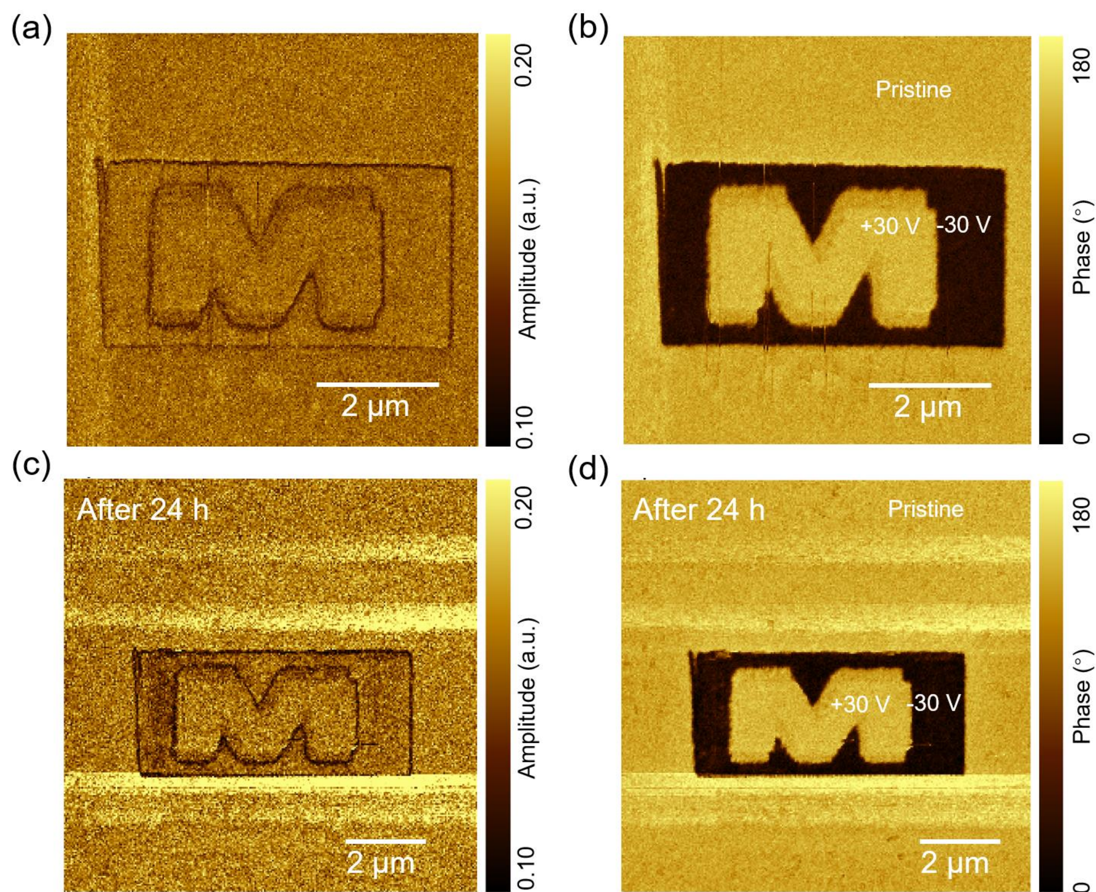

Figure S1. Amplitude and phase patterns after PFM litho-writing with ± 30 V and mapped at V_{AC} = 0.6 V, 30 kHz. The pristine piezoelectric phase exhibits the same contrast with the patterns written by +30 V, indicating a downward polarization, which agrees with the polarity of the substrate. The patterns are clearly obtainable after 24 h without almost no contrast change, thus excluding charge injection to the surface.

3. Linear plots of the I-V hysteresis loops in Figure 2

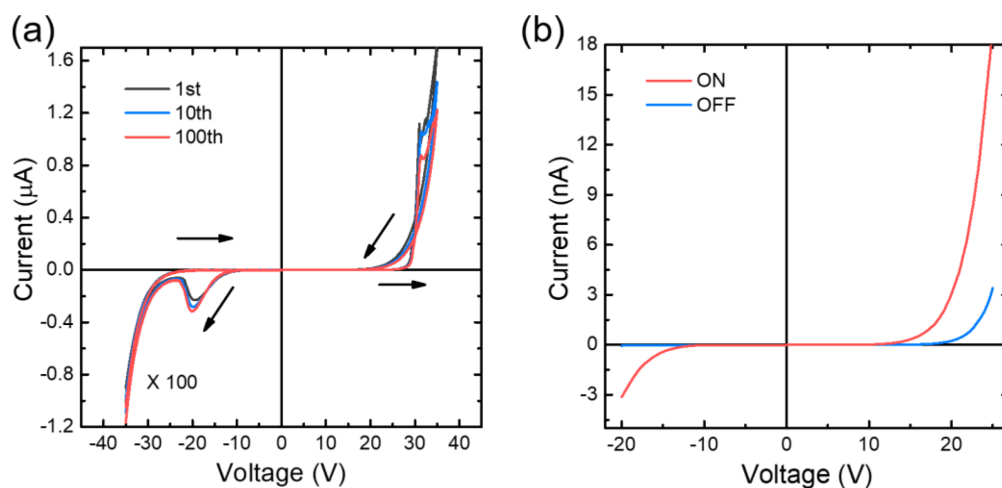

Figure S2. Linear-scale pots of the data shown in **Figure 2a** and **2b**. Due to the sharp polarity switching, a negative differential resistance region is created under reverse bias.

4. Uniformity of the I-V hysteresis loops shown in Figure 2a.

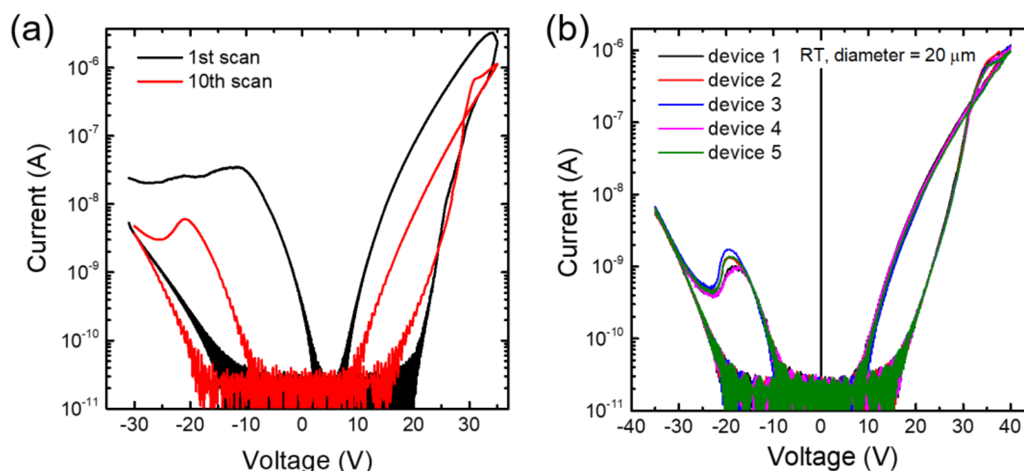

Figure S3. a) I-V loops with large ON/OFF ratio at initial scans. After several scans the I-V behavior becomes similar to other devices. b) I-V loops obtained from different devices on the same wafer. The almost overlapping curves indicate very good uniformity.

5. Polarization fatigue test for the sample shown in Figure 2.

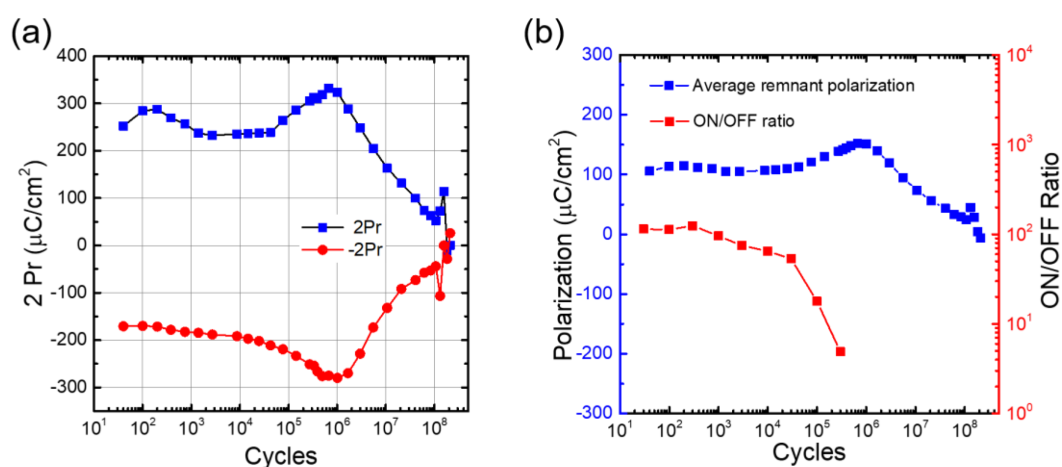

Figure S4. a) Typical polarization fatigue results for the sample in **Figure 2**. Sizeable switchable polarization can be observed up to 10^7 switching cycles. The fluctuation in the polarization values could be due to random states of interface traps/compensation charges, and the increase of measured polarization after ~ 10^5 cycles may result from the increase in

leakage current which causes an overestimation of the switchable polarization. b) Comparison of averaged remnant polarization with ON/OFF ratio after different bipolar switching cycles. The early setting-in of resistive fatigue is believed to be due to that charge injection occurs before domain pinning. [7]

6. *I-V curves after bipolar cycling*

As shown in **Figure S6a**, after significant bipolar cycling, the OFF current slowly increases with cycling number, causing decreasing ON/OFF ratio shown in **Figure S5b**. Further bipolar cycling leads to increase in both ON and OFF currents, and the current under positive and negative voltage become symmetric. Fitting the I-V curves before resistive fatigue using models including Poole-Frenkel emission, thermionic emission, direct or F-N tunneling is found difficult and results in unreasonable dielectric constants or barrier heights. This is understandable given the imperfect barrier shape and potential profile when charge compensation and depletion region are considered. After resistive fatigue, the I-V data can be well fitted by Poole-Frenkel emission model with relative dielectric constants of 12-15 which is consistent with the permittivity value from C-V measurement. We suspect that during cycling, charges were injected to domain boundaries and the interface, smearing the modulation effect of interface barrier and giving rise to bulk-conduction limited current.

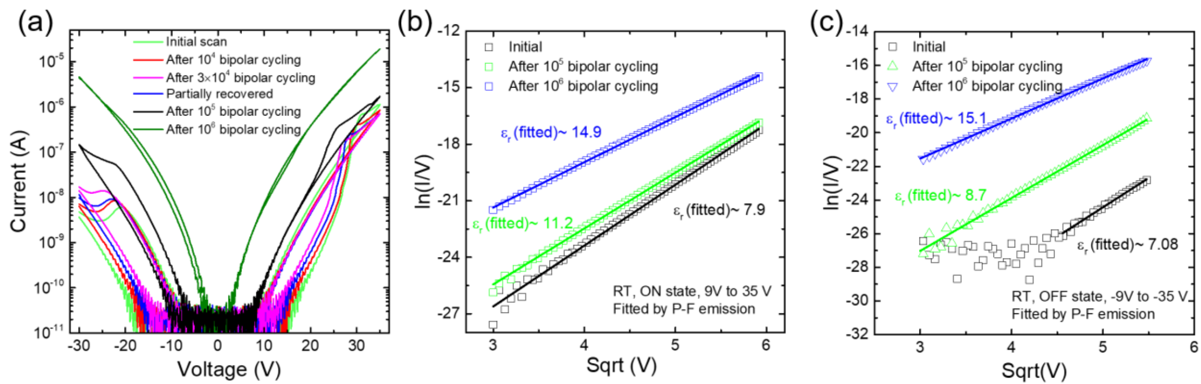

Figure S5. a) I-V hysteretic loops before and after resistive fatigue. The bipolar cycling was done by applying ± 35 V, 20 ms pulses repeatedly to the top electrode. The blue curve shows the I-V loop after 3×10^4 cycling and biasing at -40 V for 1 min. b, c) Fitting results (solid lines) using Poole-Frenkel emission model. Low relative dielectric constants (6 – 8 for different devices) were obtained for I-V data before resistive fatigue.

7. *Voltage profiles used to produce Figure 3*

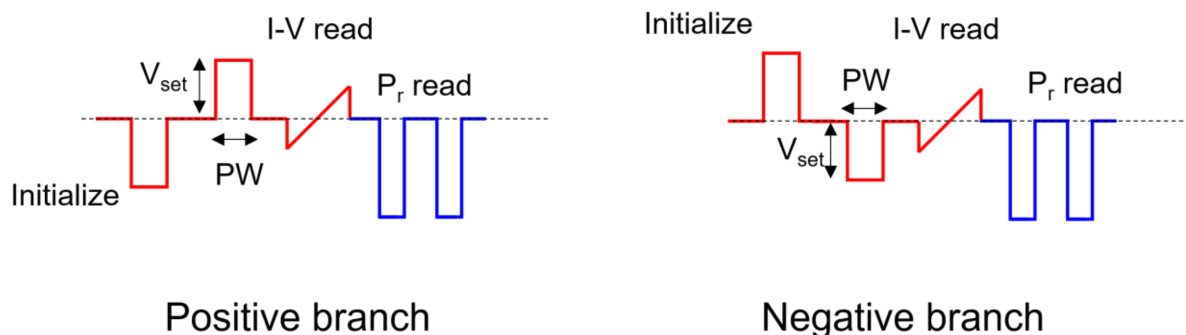

Figure S6. Schematics of the voltage profiles used to produce **Figure 3**. For **Figure 3a**, to build the positive branch (from -35 V to 35 V, counterclockwise), a – 35 V, 20 ms pulse was first used to initialize the polarization state to polarization up, then a write pulse with fixed pulse width but variable Vset was used to change the polarization state of the device and shown as the x-axis in **Figure 3a**. The current level at -17 V was subsequently captured and two pulses (- 60 V, 0.05 ms) were used to extract the polarization change as a consequence of the write pulse. The negative branch in **Figure 3a**, i.e., the data points from 35 V to – 35 V (counterclockwise), a +35 V, 20 ms pulse was used to initialize the polarization state and two -60 V, 0.05 ms pulses were used to extract polarization change. For **Figure 3b** and **3c**, the write pulse voltage was fixed at ± 35 V while the pulse width (PW) was varied.

8. *Evidence of a depletion region from C-V measurement*

Another two samples with different electrode carrier concentrations were prepared and the I-V hysteresis loops were shown in **Figure S8a**. As mentioned in the manuscript, the rectifying ratio increases with decreasing electrode carrier concentration. Further, the capacitances of three samples near zero bias were measured and shown in **Figure S8b**. As we can see, the capacitance values in the ON state are larger than those in the OFF state, indicating a space charge when the polarization is upward. [8] Using the method provided by Wen et al, the thicknesses of the space charge region and the dielectric constants of ScAlN were extracted and summarized in **Table S2**. The relative permittivity of GaN is considered to be 8.9. **Figure S8c** further shows the frequency dependent capacitances measured at zero bias voltage. The capacitances were found to be retainable after several days, suggesting that traps are not playing an important role.

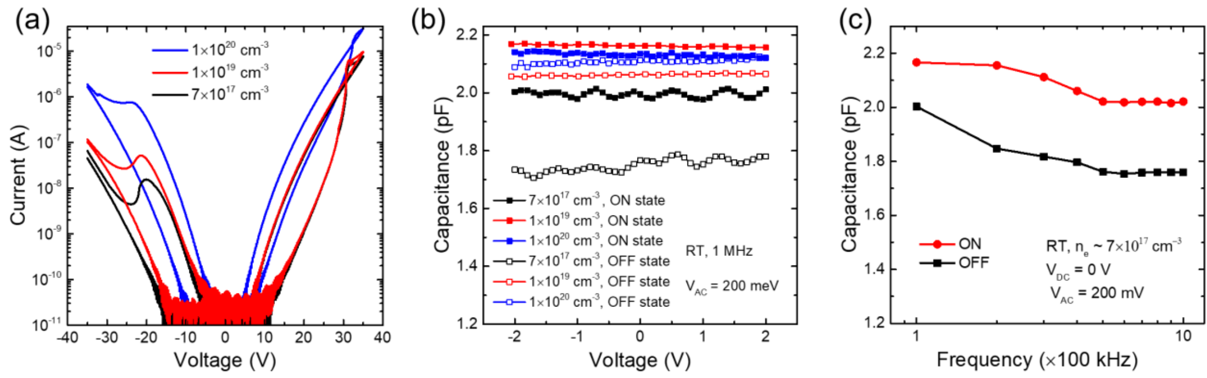

Figure S7. a) Dependence of I-V hysteresis loops on GaN electrode carrier concentration. With increasing carrier concentration, both the ON and OFF current increased while the increase in OFF current is more pronounced, resulting in reduced rectifying ratio. b) Low field capacitance measured after poling the devices to ON and OFF states. The capacitances under ON states are generally larger than those under OFF states. Decrease in GaN electrode carrier concentration results in enhanced capacitance modulation. c) Frequency dependence of the capacitance at zero bias for a device with the lowest carrier concentration. The decrease of capacitance with increasing frequency is consistent with that of a Metal-insulator-semiconductor capacitor. Measurements were done with 50-μm-diameter top electrodes.

Table S2. Dielectric constant and space charge region width extracted from the capacitance measurements.

n_e	C_{ON}	C_{OFF}	ε_r	W_D	*Ideal W_D
cm^{-3}	pF	pF	-	nm	nm
~ 7×10^{17}	2.014	1.767	11.59	10.7	694
~ 1×10^{19}	2.162	2.065	12.44	3.42	179
~ 1×10^{20}	2.136	2.112	12.29	0.81	32

* During calculation, dielectric constants of GaN and ScAlN are set as 8.9 and 12, and the spontaneous polarization of GaN and ScAlN are set to -3.5 μC/cm^2 and ± 60 μC/cm^2, respectively.

9. *Dependence of I-V hysteresis loop on electrode material and junction area.*

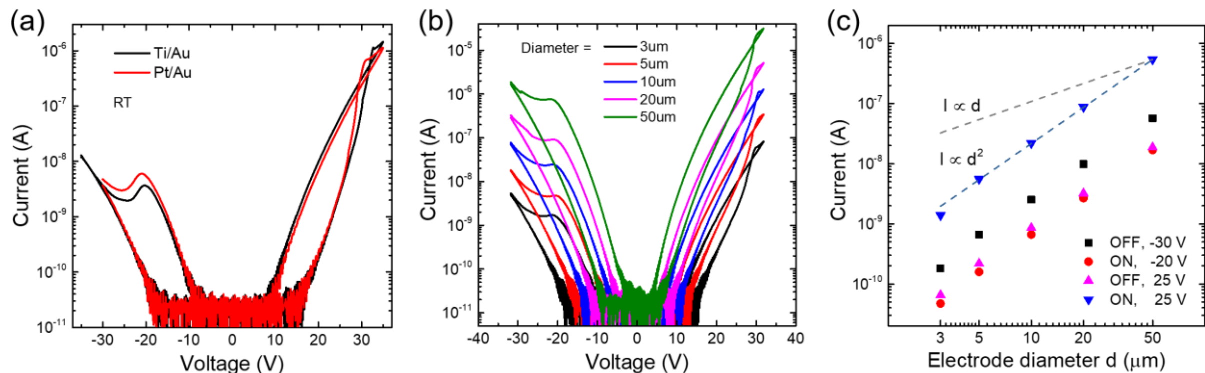

Figure S8. a) I-V hysteresis loops with different top electrode materials. The Pt/Au metal stack contains 50 nm Pt and 150 nm Au by e-beam deposition. b) I-V loops with different sizes of top electrodes. 200-nm-thick SiO_2 deposited by PECVD with small dry-etched openings was used to define electrode areas smaller than 10 μm in diameter. c) Size dependence of the device current sensed at different voltages. The almost uniform slopes parallel to $I \propto d^2$ indicate good area dependence.

10. *Temperature dependent measurements*

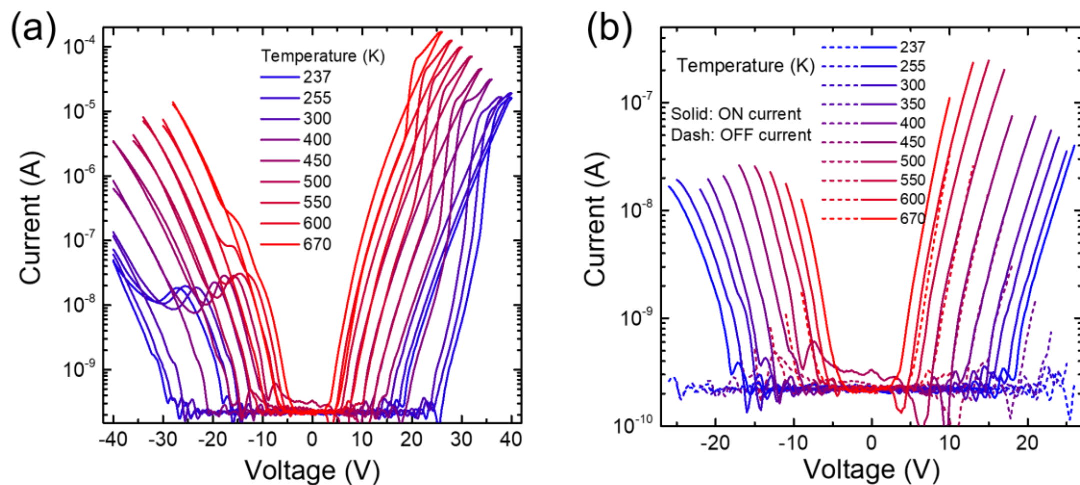

Figure S9. a) Hysteresis loops and b) ON/OFF current measured at different temperatures. With increasing temperature, enhanced thermionic current leads to drastic increase in OFF current, and results in reduced rectifying ratio.

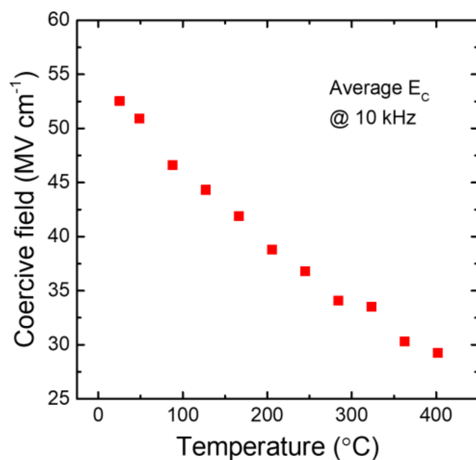

Figure S10. Coercive field at different temperatures. The coercive fields were extracted from the peak position in I-E loops and were averaged by two branches.

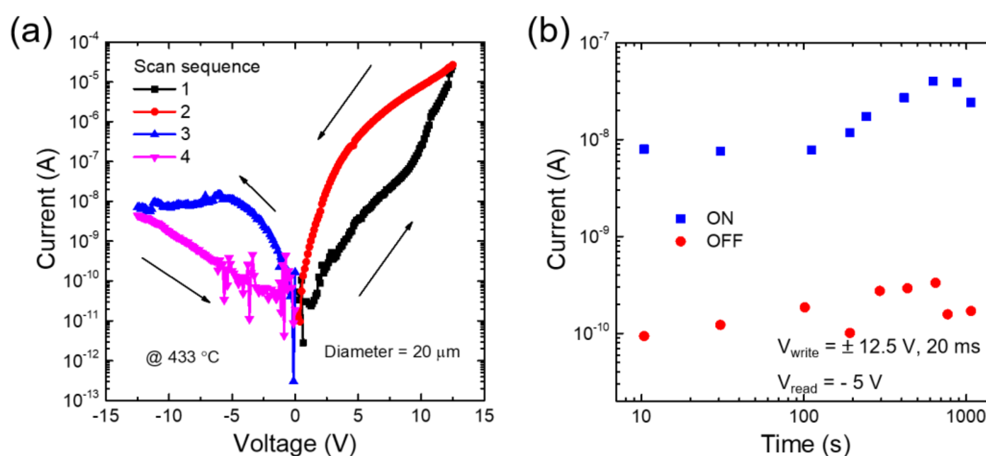

Figure S11. Resistive switching behavior in an optimized ScAlN/GaN heterostructure. a) Rectifying behavior in an optimized ScAlN/GaN heterostructure at 433 ℃ on a temperature-calibrated hotplate in air. The scan direction and sequence were indicated. b) Non-destructive readout of ON/OFF current at -5 V at 433 ℃.

Reference

[1] T. Mikolajick, S. Slesazeck, H. Mulaosmanovic, M. H. Park, S. Fichtner, P. D. Lomenzo, M. Hoffmann, U. Schroeder, J. Appl. Phys. **2021**, 129.

[2] H. Huang, J. F. Scott, *Ferroelectric materials for energy applications*, John Wiley & Sons, **2018**.

[3] P. Wang, D. A. Laleyan, A. Pandey, Y. Sun, Z. Mi, Appl. Phys. Lett. **2020**, 116.

[4] D. Wang, P. Wang, B. Wang, Z. Mi, Appl. Phys. Lett. **2021**, 119.

[5] P. Wang, D. Wang, N. M. Vu, T. Chiang, J. T. Heron, Z. Mi, Appl. Phys. Lett. **2021**, 118.

[6] H. C. L. Tsui, L. E. Goff, S. K. Rhode, S. Pereira, H. E. Beere, I. Farrer, C. A. Nicoll, D. A. Ritchie, M. A. Moram, Appl. Phys. Lett. **2015**, 106.

[7] X. Zou, L. You, W. Chen, H. Ding, D. Wu, T. Wu, L. Chen, J. Wang, ACS Nano **2012**, 6, 8997.

[8] Z. Wen, C. Li, D. Wu, A. Li, N. Ming, Nat. Mater. **2013**, 12, 617.