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An Epitaxial Ferroelectric ScAlN/GaN Heterostructure Memory

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Electrically switchable bistable conductance that occurs in ferroelectric materials has attracted growing interest due to its promising applications in data storage and in-memory computing. Sc-alloyed III-nitrides have emerged as a new class of ferroelectrics, which not only enable seamless integration with III-nitride technology but also provide an alternative solution for CMOS back end of line integration. In this paper, the resistive switching behavior and memory effect in an ultrawide-bandgap, high Curie temperature, fully epitaxial ferroelectric ScAlN/GaN heterostructure is reported for the first time. The structure exhibits robust ON and OFF states that last for months at room temperature with rectifying ratios of 60–210, and further shows stable operation at high temperatures (≈670 K) that are close to or even above the Curie temperature of most conventional ferroelectrics. Detailed studies suggest that the underlying mechanism is directly related to a ferroelectric field effect induced charge reconstruction at the hetero-interface. The robust resistive switching landscape and the electrical polarization engineering capability in the polar heterostructure, together with the promise to integrate with both silicon and GaN technologies, can pave the way for next-generation memristors and further enable a broad range of multifunctional and cross-field applications.

1. Introduction

Ferroelectric materials exhibit a spontaneous polarization that can be reoriented by an external electric field, the principle of which has been widely used to modify the barrier height or width in a metal–ferroelectric–metal capacitor or a ferroelectric/semiconductor heterostructure to make resistive switching memristors and programmable homojunctions.[1–5] With the increasing demand in big data storage and data-centric computing, there have been significant interests in ferroelectric resistive switching devices due to their promising applications in energy-efficient memory, neuromorphic and in-memory computing, and edge intelligence.[6–8] As a result, tremendous efforts have been devoted to fabricating resistive switching devices including ferroelectric tunnel junctions (FTJs), ferroelectric field effect transistors (Fe-FETs), and ferroelectric diodes based on the conventional perovskite- or fluorite-type ferroelectrics, as well as various newly discovered 2D ferroelectric materials.[8–15] On the process side, with silicon technology being the mainstream, the rigorous processing steps and strict elements control within the CMOS production line pose major challenges to the materials available for making ferroelectric memristors toward marketization.[16] On the material side, the low Curie temperature, small coercive field, and narrow bandgap of most conventional ferroelectrics (see detailed comparison in Table S1, Supporting Information) make related devices susceptible to strain/stoichiometry distortions, read/write operation, depolarization field and charge injection, etc., resulting in limited memory window and stability issues especially under harsh environments.[8,17–23] The demonstration of ferroelectricity in doped hafnium oxide and zirconium oxide and their alloyed variants brought new life to the ferroelectric memory community by being standard materials used in CMOS processes and has directed the boom in Fe-FETs, FTJs, and negative-capacitance FETs in the past decade.[24–27]

Very recently, Sc-alloyed wurtzite III-nitrides (Sc-III-Ns) have emerged as new members of the ferroelectrics family with high-temperature phase stability (up to 1100 °C), large tunable coercive field (1.5–6 MV cm^{-1}), remarkable switchable polarization (80–120 μC cm^{-2}), wide bandgap (4.9–5.6 eV), and unprecedented resistance to retention even on a polar semiconductor electrode, making these new materials promising candidates for memory applications that may outweigh conventional ferroelectrics in terms of lifetime and stability especially in harsh environments.[28–41] The wide synthesizing window also raises interests in a post-CMOS compatible processing technology.[42]

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In spite of these promises, there have been few demonstrations of ScAlN memory devices, which were only realized by using sputter deposition.[43,44] Compared to conventional sputter deposition, the epitaxial growth of ferroelectric ScAlN by molecular beam epitaxy (MBE) offers several critical advantages, including superior control over crystallinity, stoichiometry, thickness, doping, interface, and uniformity that are vital for the performance, stability, and yield of memory cells and arrays.[45–48] The single-crystalline nature of MBE-grown ScAlN can further offer a powerful approach to control the threshold variation, which has remained an unresolved issue for "the era of ferroelectrics."[8] Moreover, the fully epitaxial method and the electrically switchable polarization greatly extend the spontaneous/piezoelectric polarization engineering space in III-nitrides,[49] and further promise a seamless integration of ferroelectricity with the outstanding properties of III-nitrides and nitride-based electronics, optoelectronics, and piezoelectronics, which may enable a revolution in future all nitride-based energy-efficient memory circuits and edge-intelligence (EI) applications for harsh environments.[50,51] Moreover, given the mature nitride-on-silicon technology, high-quality ScAlN can be readily grown on Si substrate over a wide range of growth conditions,[46,52] enabling seamless integration with Si electronics especially for memory applications.

Critical to these promises and applications is a fundamental understanding and demonstration of the ferroelectricity and polarization engineering in a Sc-III-N/III-N heterostructure. In this article, we report on the first demonstration of a fully epitaxial ferroelectric ScAlN/GaN heterostructure memory. The coupling between the distinct resistive switching behavior and polarization orientation is further analyzed in detail. The structure exhibits robust ON and OFF states depending on electrical poling directions at room temperature, with an ON/OFF ratio of 60–210, retention time of over 3×10^6 s, and bipolar cycling of over 10^4 times. Polarization-resistance correlated measurements provided direct evidence of a ferroelectric polarization coupled resistive switching process. Besides, the conductance and capacitance rectifying ratios were found to decrease with increasing carrier concentration in the GaN electrode layer, suggesting a ferroelectric field effect induced charge reconstruction at the heterointerface, an effect that is being strongly desired for incorporating ScAlN into III-nitride devices. Furthermore, the memory effect exhibited weak dependence on operation temperature. A maximum rectifying ratio of ≈10 is well maintained even at 670 K, a temperature range that is close to, or even higher than the Curie temperature of most conventional ferroelectrics (Table S1,Supporting Information). These studies firmly establish ScAlN-based ferroelectric/III-nitride heterostructures as a viable candidate for ferroelectric-resistive memory, providing a new paradigm shift for next-generation memristors and all nitride-based monolithic integrated circuits for energy-efficient applications and harsh environments.

2. Results and discussions

Single-crystalline ScAlN films with a thickness of ≈100 nm were grown on commercial GaN/sapphire templates by radio-frequency plasma-assisted MBE following the growth of ≈120 nm Si-doped GaN bottom electrode layer with a carrier concentration of ≈ 1×10^{19} cm^{-3}. Ti/Au metal pillars with different diameters (3–50 µm) were then deposited as top electrodes, as schematically shown in **Figure 1**a (see Experimental

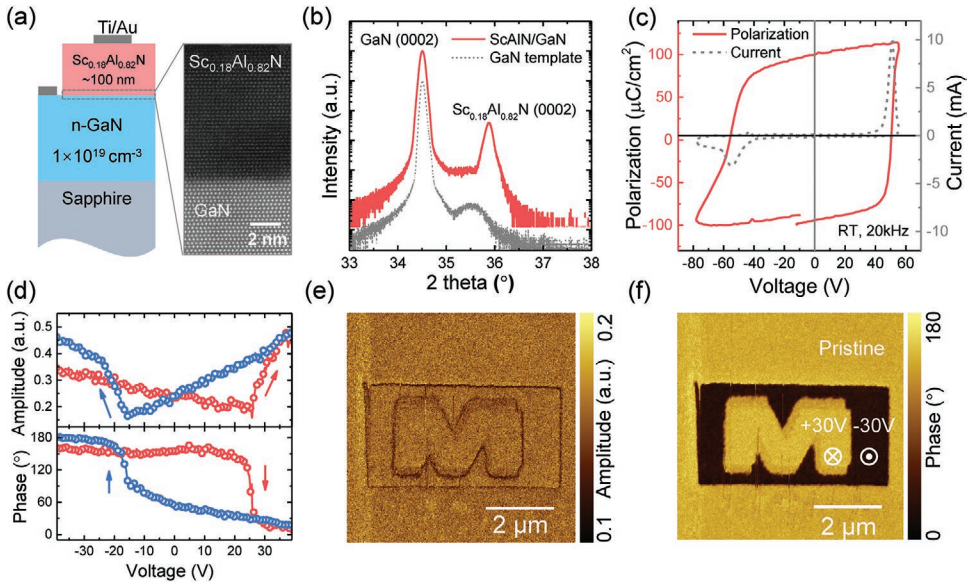

Figure 1. Ferroelectricity in the epitaxial ScAlN/GaN heterostructure. a) Schematic of the device structure and STEM image of the ScAlN/GaN interface. b) XRD 2θ-ω scan for the ScAlN/GaN sample. c) *P*–*V* and *I*–*V* loops measured using triangular input at 20 kHz at room temperature driven from the top electrode. d) Typical PFM phase and amplitude hysteresis loops measured at 30 kHz, room temperature. Butterfly-shape amplitude curve and ≈180° phase switching are observed. e,f) Amplitude and phase patterns after writing at ±30 V and mapped at V_{AC} = 0.6 V, 30 kHz. The pristine piezoelectric phase exhibits the same contrast with the patterns written by +30 V, indicating a downward polarization, which agrees with the polarity of the substrate. The contrary phase under the same poling direction in (d, f) stems from the phase value renormalization with different initial phase states during measurements.

Section for details on sample preparation). Otherwise mentioned, the results shown are collected from the sample with GaN electrode carrier concentration of ≈1×10^{19} cm^{-3} and top electrode diameter of 20 μm. The Sc content of the ScAlN layer was set to ≈18% to match the lattice of GaN to reduce misfit defects and dislocations.[47] As shown in the scanning transmission electron microscopy (STEM) image on the right side of Figure 1a, atomically ordered interface can be observed, showing good epitaxial quality. Figure 1b depicts the typical X-ray 2θ-ω scans on one ScAlN/n-GaN sample. The characteristic diffraction peak for ScAlN (0002) can be observed clearly, further confirming the wurtzite structure of the ScAlN film. The (0002) plane rocking curve full-width-at-half-maximum values (FWHMs) of all the ScAlN films were less than 400 arcsec, which is nearly one order of magnitude smaller than conventional sputtering and further confirms the excellent structural property.[30,46] Figure 1c displays the typical current–voltage (I–V) and polarization–voltage (P–V) hysteresis loops recorded using Radiant ferroelectric tester II at 20 kHz at room temperature. The remnant polarization was estimated as ≈90 μC cm^{-2}, consistent with previous reports.[29,39] The asymmetry in the P–V loop is ascribed to asymmetric electrode material. The ferroelectricity in the ScAlN/GaN heterostructure was also confirmed by piezo-response force microscopy (PFM). As shown in Figure 1d, the butterfly-shape amplitude diagram and the box-shape phase diagram with ≈180° separation suggested that the polarity of the film can be switched externally by an electric field. Figure 1e,f further shows the PFM out-of-plane phase and amplitude images of domains after writing. The 180° phase contrast, clear domain boundary, and uniform contrast in each poled region manifest that stable antiparallel domains can be written in the ScAlN layer. The low amplitude signal along the domain boundary indicates the cancelling contribution of opposite domains, which is characteristic of ferroelectrics. Those patterns were still detectable after 24 h, showing the stability of the polarity switched domains (Figure S1, Supporting Information).

To probe the resistive switching behavior, static I–V loops were measured by a B1500 semiconductor analyzer at room temperature. All voltages were applied to the top electrode while the bottom electrode was grounded. As shown in **Figure 2**a, the device exhibited clear, stable bipolar hysteresis loops with good repeatability, which remained virtually unchanged after 100 bipolar scans. A high current state is observed when sweeping back from positive bias, while a low current state is shown when scanning back from negative bias, manifesting a counterclockwise-clockwise rotation direction (Figure S2, Supporting Information, defined from linear-scale plots). Figure 2b further displays the current measured at small voltages after poling by voltage pulses. Under a poling pulse of +35 V (20 ms in width) on the top electrode, a high current state, namely the ON state, is established, featuring high current densities under both bias directions. Then, after a poling pulse of −35 V (20 ms in width), a low current state, or the OFF state is achieved, giving a rectification ratio of ≈100 at −17 V. The OFF current exhibits diode-like conduction, that is, the current under positive bias is larger than that under negative bias, while the ON current looks more symmetric with almost identical absolute turn on voltages (±10 V). Linear-scale plots of Figure 2a,b can be found in Figure S2, Supporting Information. For part of the devices, a relatively low OFF current or large ON current was measured during the first several scans, resulting in ON/OFF ratios exceeding 10^4. However, after several scans, the I–V curves stabilized and all devices showed no difference with those shown in Figure 2a, indicating very good uniformity (Figure S3, Supporting Information). The non-volatile nature of the ON and OFF states was explored by measuring the device current at −17 V after pulse poling for different retention times. As shown in Figure 2c, a slight decrease in ON current is noticed, while the OFF current remains stable possibly due to the detection limit. An ON/OFF ratio of ≈46 can still be retained after more than a month (3×10^6 s). The bipolar switching characteristics of the ScAlN/GaN heterostructure was tested by poling the ScAlN/GaN heterostructure repeatedly with ±35 V pulses and reading the current at −17 V. As shown in Figure 2d, the ON and OFF currents remain steady over 10^4 write/read cycles, and both increase drastically after ≈10^5 write/read cycles. The increase in OFF current is faster than in

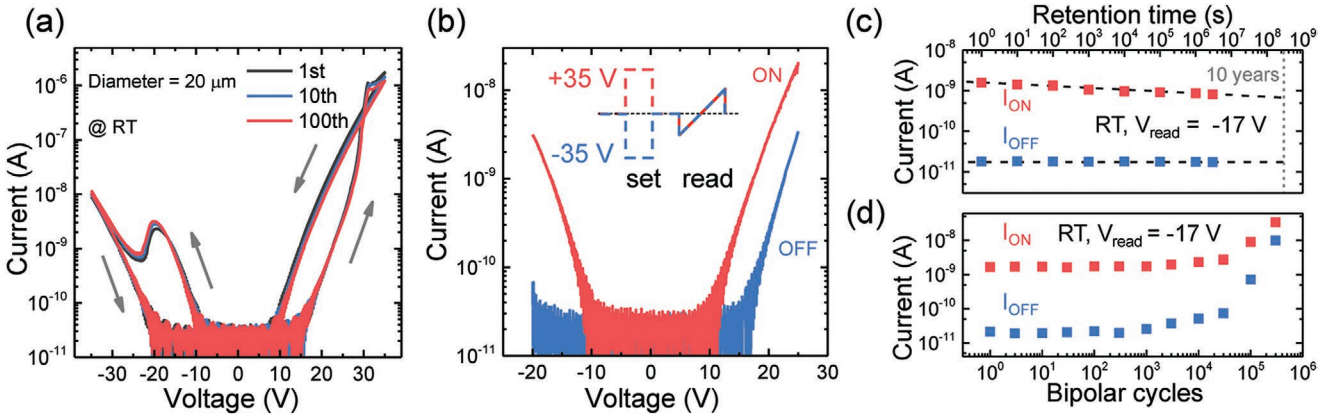

Figure 2. Resistive switching behavior in the ScAlN/GaN heterostructure memory. a) Typical I–V hysteretic loops at room temperature with a step size of 100 mV. The scan direction follows −35 V → 35 V→ −35 V. b) Non-destructive reading of the ON/OFF current, inset shows a sketch of the measurement sequence. The set pulse width is 20 ms. c) Retention properties and d) bipolar switching stability of the ScAlN/GaN heterostructure memory. The ON and OFF states are retainable over a month, and an ON/OFF ratio of ≈60 is maintained after 3×10^4 bipolar cycling (±35 V, 20 ms). A projected lifetime of >10 years is demonstrated.

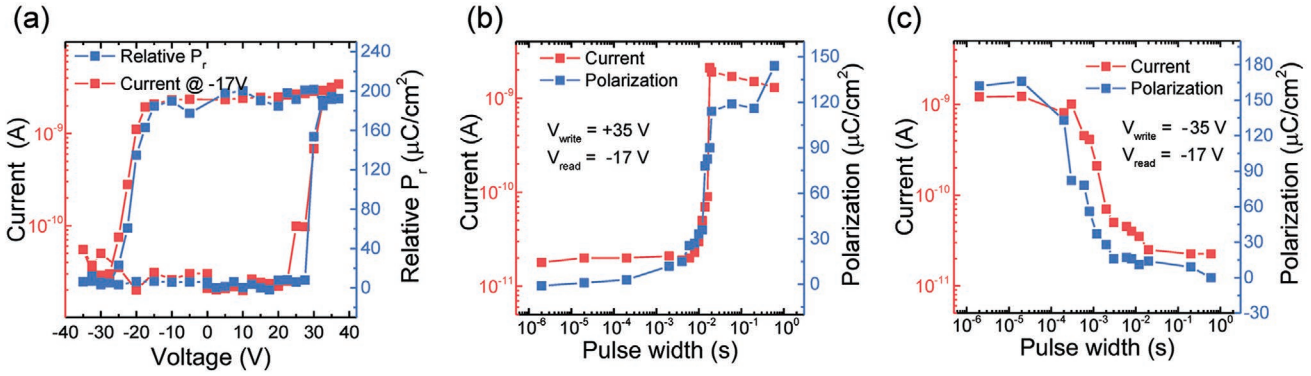

Figure 3. Simultaneous measurement of conductivity and polarization change. a) Conductivity hysteresis loop of the ScAlN/GaN heterostructure with corresponding relative polarization state. Two branches are plotted together to form a complete loop. The write pulse width was 50 ms. b,c) Pulse-width-dependent measurements. During the experiment, a preset pulse first sets the device to OFF (ON) state. Then a tunable write pulse is applied followed by a non-destructive current readout. Finally, two fixed trapezoidal waveforms are used to probe the relative polarization change after write pulse.

ON current, causing rectifying ratio to drop from ≈ 00 to ≈10 after 10^5 bipolar switching cycles. Polarization fatigue measurements showed sizeable remnant polarization with up to 10^7 switching cycles (Figure S4, Supporting Information). The early setting-in of resistive fatigue could be related to charge injection to the ScAlN/GaN interface, which will be explained later. With a larger negative poling voltage, or longer negative voltage poling time, the increased OFF current can be partly restored (Figure S5, Supporting Information). Those results show the great potential of ScAlN/GaN heterostructure as memory devices. It's noted that the switching cycles here is still lower than the state-of-the-art memory devices based on HfO_2 and lead zirconate titanate (PZT) (>10^9).[8] Optimization on the material quality and electrode materials will be of great importance to increase the endurance strength of related devices.

Summarizing Figures 1 and 2 brings us the idea that positive poling, after which polarization points downward, corresponds to the ON state, while upward polarization corresponds to the OFF state. To elucidate the relationship between resistive switching and ferroelectric switching, a modified write/read process is developed. First, a preset pulse (±35 V, 20 ms) was used to set the device to OFF (ON) state. Then a voltage and width-tunable write pulse was applied followed by a non-destructive current readout. Finally, two identical trapezoidal waveforms (switching + non-switching) were used to extract the polarization change. In this scenario, the conductivity of the heterostructure, and the polarization state corresponding to this conductivity, can be obtained simultaneously after each writing pulse. As shown in **Figure 3**a, the hysteretic resistive switching of the device exhibited almost identical shape with the *P*–*V* loop, with nearly the same threshold voltage and saturation behavior, which provides clear and direct evidence of a ferroelectric polarization modulated resistive switching process.[53] Figure 3b,c further showed the writing pulse width dependence of the resistive switching and polarization switching process. When the writing pulse width is small, negligible polarization or conductivity change is noticed. As the writing pulse width increases, the polarization difference before and after writing pulse slowly increases and saturates at $2P_r$ when pulse width is over certain values. The device current level, sensed at −17 V, shows the same trend. All these results strongly suggest a ferroelectric polarization orientation modulated resistive switching behavior in the ScAlN/GaN heterostructure. The gradual modulation of conductance with different pulse widths could be further utilized to build memory arrays that can mimic a biological learning rule called spike-timing-dependent plasticity (STDP).[54] The voltage profiles used to generate Figure 3a–c can be found in Figure S6, Supporting Information.

To explain the experimentally observed *I*–*V* hysteresis loops, we established the band diagrams for the ScAlN/GaN heterostructure considering the ferroelectric field effect and real-space charge reconstruction at the ScAlN/GaN interface. As schematically shown in **Figure 4**a,b, due to the ferroelectric field effect, when the ferroelectric polarization in ScAlN is downward after positive pulse writing, the positive polarization charges at the ScAlN/GaN interface will attract electrons near the interface and cause a downward bending of the band profile and an accumulation region; when the ferroelectric polarization in ScAlN is upward after negative pulse writing, the negative polarization charges at the ScAlN/GaN interface will repel electrons near the interface, leading to an upward bending of the band profile as well as a depletion region.[2] In the latter case, the total barrier height is increased, and an additional interface barrier is presented, which blocks the electron transport and results in the OFF state.[55] This model is further confirmed by growing ScAlN on GaN with different doping concentrations. As shown in Figure 4b, both ON and OFF current increases with increasing carrier concentration in the GaN electrode. As the OFF current increases faster, the maximum ON/OFF ratio drops from ≈210 to 60 when the carrier concentration of the n-GaN layer increases from $\approx 7 \times 10^{17}$ to $\approx 1 \times 10^{20}$ cm^{-3}. This is expected, since in the ON state the polarization is downward and the interface is already in accumulation. Further filling the interface with electrons causes negligible lowering of the barrier height. While in the OFF state, the polarization is upward, and the screening of the polarization charge is strongly enhanced by high doping concentration in the electrode layer, consequently a more pronounced reduction of the depletion region width and the interfacial barrier height. Following Wen's work, the depletion widths have been calculated based on capacitance–voltage (*C*–*V*) measurements at small voltages, indicating a

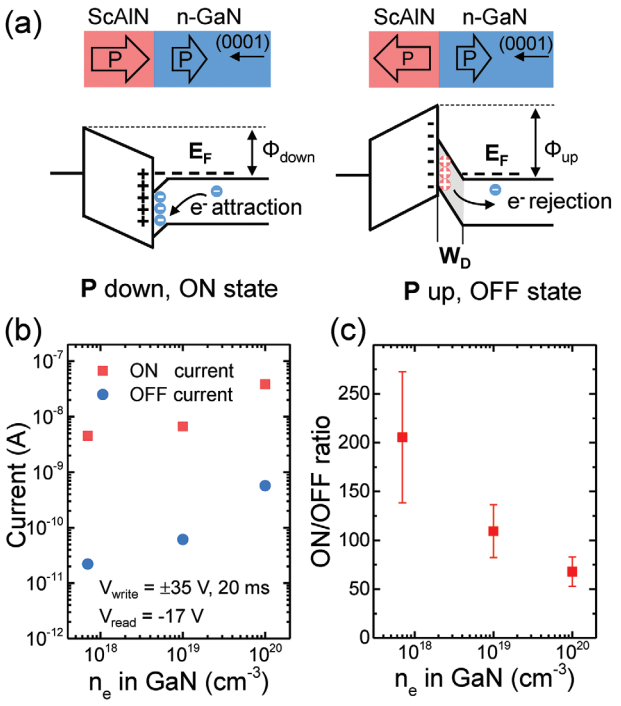

Figure 4. a) Schematics of energy band diagrams of the ScAlN/GaN heterostructure modulated by the polarization orientation in ScAlN. Φ_{up}, Φ_{down} are the effective barrier heights for electron transport. Due to ferroelectric field effect and charge screening, a space charge region and a higher effective barrier are built during **P** up operation. b) Dependence of ON/OFF current on carrier concentration in the GaN contact layer and c) corresponding ON/OFF ratio. Error bars in (c) are standard deviations calculated from ten different devices in each sample. Measurements were done with 50-µm-diameter top electrodes to enable better comparison of the OFF current. The spread of ON/OFF ratios with decreasing GaN carrier concentration indicates an enhanced effect of depolarization field.

reduction of equilibrium depletion width from ≈10 nm to less than 1 nm when the carrier concentration increases from ≈7×10^{17} to ≈1×10^{20} cm^{-3} (Figure S7 and Table S2, Supporting Information), consistent with the proposed model.[2] Fitting of the experimental *I*–*V* data indicates a linear dependence of $\ln(I/V)$ on the square root of *V* (Figure S5, Supporting Information). However, the extracted relative dielectric constant using Poole–Frenkel emission model (in the range of 6 to 8) is much smaller than that from *C*–*V* measurements (≈12), suggesting the conduction involved here is not dominated by polarization coupled trap-filling-factor change reported previously for a metal/ScAlN/metal capacitor.[44] The fast increase of current with voltage could indicate certain extent of tunneling current from the triangular barrier formed at the electrode/ferroelectric interface due to strong applied electric field.[4] Instead, the Poole–Frenkel emission model is found to fit the *I*–*V* curves very well after resistive fatigue, indicative of a transition from interface barrier modulated conduction to bulk Poole–Frenkel emission limited transport after cycling (Figure S5, Supporting Information). It is suspected that during bipolar cycling, excessive charges are injected to the ScAlN/GaN interface, which lowers the overall barrier height and causes leakage paths. This explains the early setting-in of resistive fatigue and the restoration behavior considering that charge injection has been reported to occur before domain wall pinning[56] and could be partially released upon back-filling or heating (Figure S5, Supporting Information). Besides, the shape of the *I*–*V* hysteresis loop is found to be independent of the electrode material (Figure S8, Supporting Information), which further shows that the rectifying effect stems from the ScAlN/GaN interface, rather than from a Schottky barrier. Due to the large oxygen affinity of Sc and Al, there could be a thin oxide layer between the top electrode and ScAlN surface.[44,45] If the conduction is modulated by the barrier height of the thin oxide layer, altering the electrode material should also change the work function of the electrode thereby the electrode–oxide interface barrier height, resulting in different rectifying ratios. However, this is not observed in our experiments. Those results together validate a ferroelectric field effect dominated resistive switching in the ScAlN/GaN heterostructure.

One may note that the depletion widths extracted are much smaller than the values from theoretical calculation considering the large polarization discontinuity and an ideal ScAlN/GaN interface (Table S2, Supporting Information). We suspect that the polarization charge at the interface could be slightly screened by interface traps introduced either during growth interruption or from the low purity Sc source (99.9%). Moreover, due to the strong chemical bonding at the ScAlN/GaN interface and the relatively small dielectric constant of ScAlN (thus stronger depolarization field), a thin non-switchable paraelectric ScAlN layer or pinned domains could exist, which significantly compensates the overall switchable polarization and weakens the ferroelectric field effect, leading to excessively attenuated depletion widths.[41,57] The latter is believed to be the main reason for the tailored depletion region in this work. Besides, vacancies could also accumulate at the interface and screen the polarization charges.[58] Nevertheless, our main concept is not affected. An effective remnant polarization may be introduced to quantitatively depict the charge reconstruction at the interface.

It has been reported that, due to significant electromigration of oxygen vacancies, filament conduction or electronic conductor–insulator transition could occur and dominate or contribute to the resistive switching process in ferroelectrics.[5] In our case, the complete reorientation of the wurtzite structure requires a holistic displacement of metal or nitrogen atoms, which may evoke some vacancy migration events.[57] By varying the diameter of the electrodes from 3 to 50 µm, the *I*–*V* hysteresis loop is found to be independent of junction area (Figure S8, Supporting Information), and no electroforming or current compliance is required to stabilize the switchable resistance, thereby excluding the formation of conductive filaments. On the other hand, the ON current in this work appears symmetric and is always larger than the OFF current under both biasing conditions, which is different from the typical diode-like hysteresis loop during electronic conductor–insulator transition.[59] Besides, the electromigration model by itself is bulk conduction and cannot account for the carrier concentration dependence shown in Figure 4c,d. Therefore, we conclude that for the ScAlN/GaN heterostructure in this work electromigration of defects like vacancies could exist but is not playing an important role.

Finally, a discussion on the high-temperature operation of the ScAlN/GaN memory is made. A wide bandgap of ≈5.5 eV

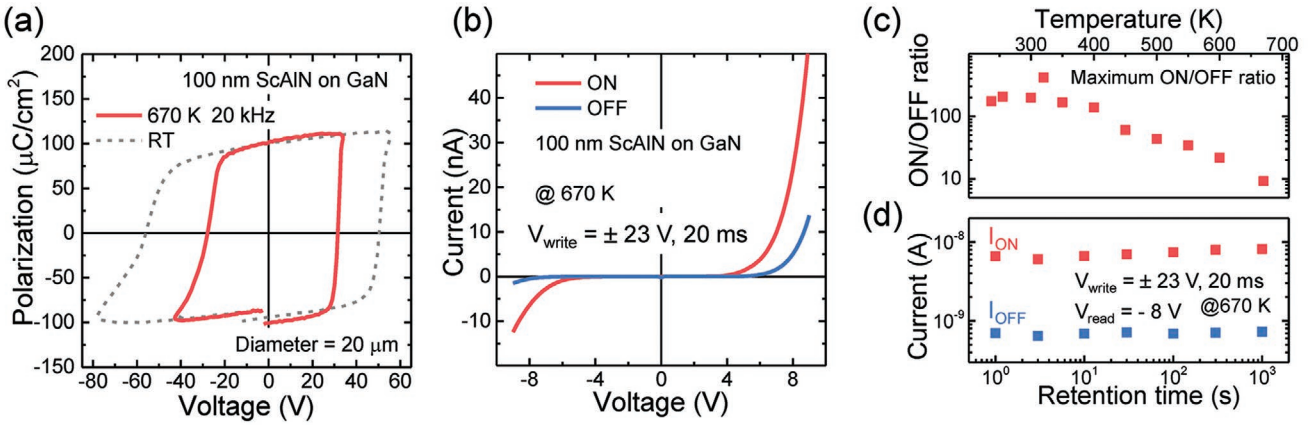

Figure 5. High-temperature performance of ScAlN/GaN heterostructure memory. a) *P–V* loop measured at 670 K on a hotplate. The temperature has been calibrated using a thermometer. b) ON and OFF currents probed at 670 K, showing the bistable conductivity. c) Dependence of ON/OFF ratio on operation temperature. Due to the strong temperature dependence of coercive field, the write and read voltage were gradually reduced with increasing temperature. The ON/OFF ratio is calculated as the maximum ON/OFF ratio in the non-destructive *I–V* readout. d) Retention test at 670 K on a hotplate using Keithley 2400.

has been reported for ScAlN with 18% Sc content,[46] which is above most of the ferroelectric materials reported (Table S1, Supporting Information). Besides, the conduction band offset between ScAlN with 18% Sc content and GaN is predicted to be ≈1.74 eV from first-principle calculations and ≈2.09 eV by X-ray photoelectron spectroscopy (XPS) measurements.[60,61] Those wide-bandgap characteristics, carrying over to ScAlN from III-nitrides, are expected to help suppress the thermally activated current at high temperatures. **Figure 5**a first compares the *P–V* loops at room temperature and at 670 K. A drastic drop of coercive field is observed at 670 K, while the remnant polarization keeps steady, in accordance with previous reports.[32] The writing pulse was consequently modified to ±23 V, 20 ms. Surprisingly, even at 670 K, the ON/OFF states are still attainable with a rectifying ratio of ≈10, as depicted in Figure 5b. This temperature is already quite close to the Curie temperature of many ferroelectric materials including HfO_2 (Table S1, Supporting Information). Figure 5c further delineates the temperature dependence of the maximum ON/OFF ratio for the ScAlN/GaN heterostructure memory. With the increase of ambient temperature, the maximum ON/OFF ratio drops slowly from ≈200 to 10 at 670 K, in contrast with the rapid decrease of ON/OFF ratios in a $BaTiO_3$-based FTJ.[62] The stability of the two states at high temperature is shown in Figure 5d, indicating a retention time over 10^3 s at 670 K. Corresponding *I–V* loops and ON/OFF currents at different temperatures can be found in Figure S9, Supporting Information. After optimization, an ON/OFF ratio of ≈100 can be still obtained even at 433 °C (Figure S11, Supporting Information). Those results confirm the superior stability of ScAlN/GaN-based memory, and provide a viable path for realizing memory devices for harsh environments such as aerospace and military applications.

3. Conclusions

In conclusion, we reported, for the first time, a stable epitaxial ScAlN/GaN heterostructure resistive memory and a detailed analysis of the coupling between resistive switching and ferroelectric polarization. The structure exhibits distinct ON and OFF states in response to external bias at room temperature, with a rectifying ratio of 60–210, retention time of over 3×10^6 s, and bipolar cycling over 10^4 times. Polarization-resistance coupled measurements showed the direct correlation between resistive switching and ferroelectric polarization switching. By fitting the *I–V* curves and tuning the carrier concentration of the GaN semiconductor electrode, the conductance modulation has been explained as electrical polarization engineering at the heterostructure interface. The memory effect exhibited weak dependence on operation temperature, maintaining a maximum rectifying ratio of ≈10 even at 670 K. With further optimization of the growth conditions,[63] electrode materials, device structures and especially the ferroelectric layer thickness, Sc-III-N-based memory devices with low operation voltage, high rectifying ratio, long retention time, and good endurance resistance comparable to other state-of-the-art memory devices are possible. These results suggest that ScAlN-based ferroelectric/III-nitride heterostructures can be potential candidates for ferroelectric-resistive memory, and are anticipated to open the route toward next-generation memristors and all nitride-based monolithic integrated logic circuits for power-efficient applications and harsh environments.

4. Experimental Section

The samples were grown using a Veeco GENxplor MBE system equipped with a radio-frequency (RF) plasma-assisted nitrogen source and a high-temperature effusion cell for Sc on commercial GaN/sapphire templates with a dislocation density of $\approx 5 \times 10^8$ cm^{-2}. Detailed growth conditions can be found in the previous papers.[39,46] The samples contained a 100-nm-thick ScAlN layer, and a 120-nm-thick n-GaN contact layer doped by Si. For n-GaN contact layer, the carrier concentration was varied from $\approx 7 \times 10^{17}$ to $\approx 1 \times 10^{20}$ cm^{-3} by tuning silicon cell temperature from 1050 to 1250 °C and further calibrated by room-temperature Hall effect measurements. Energy dispersive x-ray spectroscopy (EDS) was used to calibrate the Sc content in ScAlN in a Hitachi SU8000 scanning electron microscope (SEM). STEM specimens were prepared by a

Thermo Fisher Scientific Helios G4 UXe focus ion beam (FIB) and STEM images were collected using a JEOL 3100R05 aberration-corrected S/TEM operated at 300 kV, with a collection range of 59–200 mrad for high-angle annular dark-field (HAADF) imaging. Ti/Au and Pt/Au circular electrodes with diameters of 3–50 µm were lithographically patterned electrodes. 200-nm-thick SiO_2 deposited by PECVD with small dry-etched openings was used to define electrode areas smaller than 10 µm in diameter. The *P*–*V* loops were collected using a Radiant Precision Premier II ferroelectric tester driven from the top electrode. Current and capacitance were measured using B1500 semiconductor analyzer and Keithley 2400. Temperature-dependent measurements were done using a MMR temperature variable (70–780 K) probe station or on a hotplate in air. PFM results were captured in a NT-MDT Ntegra system using a conductive tip HQ:NSC35/PT from Mikromasch. During measurements, the tip frequency was 30 kHz and V_{AC} was 0.6 V.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

III-nitride memory, AlScN, ferroelectric, high-temperature memory

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