Energy-Efficient Circuits and Systems for Powering, Sensing and Actuating the Motions in Internet of Things

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical and Computer Engineering)
in the University of Michigan
2022

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Dedication

To my wife Xingye, my parents Changcao Peng and Xiaolan Zhao,

my advisor Dennis Sylvester, and Professor David Blaauw

for all your support and care.

Acknowledgements

The authors would like to thank Robert Gordenker and Professor Khalil Najafi at University of Michigan, for their support and contribution to my research projects.

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Abstract

The Internet-of-Things (IoT) has long been considered the next major computing class that has significant societal benefits on people's lives. With the miniaturization of the sensor nodes, the acquisition and analysis of data can be achieved in a broader range of environments, enabling applications such as precision healthcare, smart buildings, intelligent agriculture, and more. Motions are ubiquitous in these applications and can be utilized as an energy source to mitigate the power constraints associated with the sensor node scaling. Besides, many sensor nodes also acquire motion signals to reveal the information from the ambience, and some may even actively produce motions to achieve a more complex interaction with the environment (e.g., micro-robot). This thesis introduces three major topics on low-power circuit and system designs for IoTs related to motions. The first topic is to harvest kinetic energy from motions with piezoelectric energy harvesters (PEHs). To address the challenges in the impedance matching to PEHs, we present a sense-and-set (SaS) circuit that achieves the optimal energy extraction from the transducer and adapts to environmental variations. The SaS circuit is implemented with a single chip design, achieving a 5× power improvement in energy harvesting under periodic and random vibrations. The second topic is about sensing motions with ultra-low power MEMS capacitive accelerometers. To improve the critical trade-off between power and noise in MEMS accelerometers, we present a high-voltage biasing technique that significantly increase the MEMS sensing signal while maintaining mechanical stability with a novel technique called electrostatic mismatch compensation. The proposed accelerometer is implemented with 1 MEMS and 2 CMOS ICs, showing a 15× power-noise improvement over the prior state of the art. The third topic is about

generating motions with micro-robot design to achieve the Programmable Matter (PM) that can be configured into any arbitrary 3-D shapes with a program. The motion generation is achieved by the high-voltage electrostatic actuation, and we present a high-voltage generation and multiplexing (HVGM) chip to enable a 100V actuation with 200nW range power. We further integrate HVGM with several other ICs into a complete bare-die system that is placed in each PM unit, and controls its communication, computation, powering and actuation in a PM system. A second version controller is also proposed and implemented to be fully integrated on-chip but maintains the multi-functions that enables an intelligent PM system.

Chapter 1 Introduction

From the early 1960s, the development of computers has been characterized by computing platforms that emerged and became dominant over time, known as Bell's law [1]. From the huge workstation to personal computers and then to smartphone, a new class of less expensive and much more compact computers is developed approximately every decade to replace its predecessor. The next generation of computing platforms [2] [3] [4] has reached the millimeter scale in terms of system volume and was able to perform a complex function including sensing, computations, and communications in diverse emerging applications. In 1999, Kevin Ashton first used the term “the Internet of Things (IoT)” to describe future computing platforms where the Internet is connected to the physical world through ubiquitous sensors.

Combining the scaling of sensor node hardware, IoT becomes promising in a wide range of applications, such as monitoring the environment for pollutants, assessing water quality, improving agricultural productivity, providing precision healthcare and hence improving quality of life, and many more tasks [5].

Along with these opportunities, miniaturized IoT sensors also brought unique design challenges, which are mainly related to its power constraints from the small battery capacity. Besides, environmental motions results in more design complexities as they may interact with the IoT sensors and change how they acquire data and issue feedbacks [6]. This thesis introduces three projects, from three different angles on the interaction between miniaturized IoT designs and motions: 1) how to power IoTs by harvesting energy from motion; 2) how to sense motion while

maintaining both high resolution and low power; and 3) how to generate motions for a complete, intelligent micro-robot system.

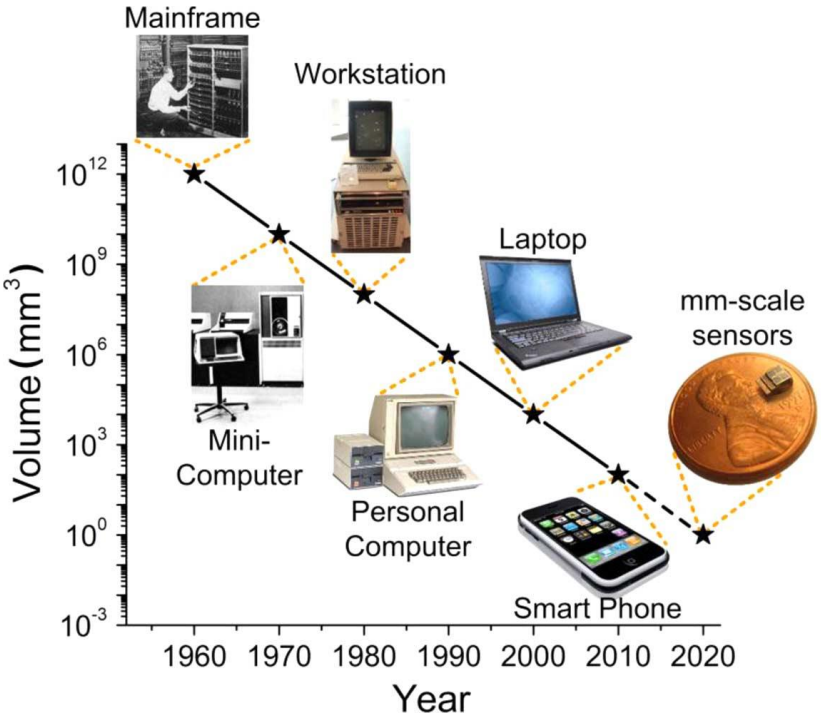


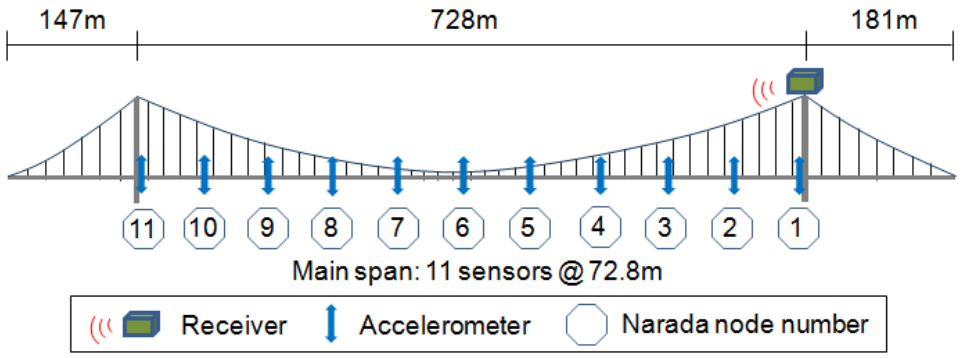
Figure 1.1: Bell's Law predicts continuous scaling of micro-size computing systems [2].

1.1 Powering Miniaturized IoT Sensor Nodes with Motions

Since IoT sensors work in a wide range of environments, power delivery is often not reliable or even accessible. While sensors can operate with integrated batteries, their battery life is usually limited due to the small battery size. Moreover, as the number of sensors increases in the network, recharging sensor batteries or maintain a wireless power delivery [7] can also be tricky and expensive. Energy harvesting from the ambient environment can significantly extend the lifetime of battery-powered systems, and in energy-autonomous systems it can even eliminate the use of batteries. To perform energy harvesting, a transducer is integrated with the sensor, and it captures energy from one or more renewable energy sources and converts them into usable electrical energy [8]. Kinetic energy harvester is usually deployed in the presence of object motion,

including vibrations, pressure and other activities, and the piezoelectric transducers become popular for kinetic energy harvesting due to their high power-density and good sustainability.

An interesting application of the piezoelectric energy harvester (PEH) is introduced by [9], where a series of wireless sensor nodes were attached to a bridge to acquire its vibration signature for structural health monitoring (SHM), as shown in Fig. 1.2. The wireless sensors are integrated with energy harvesting modules made of piezoelectric transducers and the vibration energy is harvested to power the SHM sensor nodes for long period of time (e.g., years) without replacing the batteries. In the energy harvesting module, the authors utilize the *Parametric Frequency Increased Generator* [10] *(PFIG)* technique to up-convert the vibration frequency to a higher value that maximizes the output power of a miniaturized piezoelectric transducer, providing a μW level harvested power from the bridge vibrations.



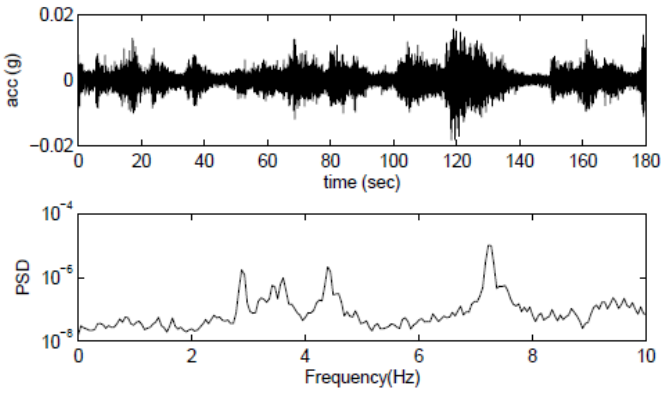


Figure 1.2: The deployment of the wireless sensors on the bridge (top) and the measured vibration acceleration waveform with its power spectrum density (bottom) [9].

However, there are several challenges associated with the use of piezoelectric energy harvesters in mm-scale sensor nodes. First, the efficiency of the PEH is highly related to the vibration frequency and its own resonant frequency, which is hard to meet in practical applications, since most ambient vibration sources have a relatively unstable, broadband frequency spectrum. Second, the PEH interface circuits that perform impedance matching can significantly impact the charge-extraction efficiency as well, and design challenges exist to compensate the intrinsic PEH parasitics to maximize output power. We present a new energy extraction technique, sense-and-set (SaS), to perform maximum-power-point tracking (MPPT) by dynamically sensing and setting the optimal voltage to the transducer. It also adapts to various input vibrations and load changes while maintaining maximum efficiency in extracting power from piezoelectric energy harvesters.

1.2 Sensing Motions with Ultra-Low Power and High Resolution

Motion detection and classification are becoming crucial for autonomous monitoring systems, including assistive living, rehabilitation, device stabilization and surveillance [11]. While the detection of motion can be achieved remotely via ultrasound motion sensors or image sensors, a directly attached sensor to the object (e.g., an accelerometer in a wearable device) is still preferable because of the high sensitivity and the continuous monitoring of the motion. MEMS capacitive accelerometers have become increasingly popular in motion-detection applications such as object monitoring, gesture recognition and tilt control [12] [13]. Consisting of a micro-mechanical spring-mass system, MEMS capacitive accelerometers are capable of high acceleration sensitivity while maintaining good linearity, low Brownian(mechanical) noise, good temperature consistency and miniaturized volume [14] [15]. An analog-front-end (AFE) interface circuit is

required to amplify the signals generated by the MEMS sensing elements, before it can be read out and utilized by other circuits such as analog-to-digital converters (ADCs).

The AFE circuit, usually implemented with the CMOS process, has its own noise floor that adds up to the readout signal. And since there is a fundamental noise-power trade-off inside the circuit design, it is difficult to achieve both sub-μW power and a mg-level resolution in measuring the acceleration. In Chapter 3, we present a unique accelerometer architecture in which, instead of keeping a good noise floor in the CMOS readout circuit design, we increase the signal amplitude from the MEMS side by applying a higher voltage bias on it. This high voltage bias, while it generates a linearly increase signal at the AFE input, reduces the stiffness of the MEMS accelerometer by electrostatic force to further increase the MEMS sensitivity. The proposed accelerometer achieves 40× signal gain than the conventional MEMS capacitive accelerometers, and it operates with 100nW range power to sense mg-level accelerations, achieving a larger than 10 times improvement on the power and resolution performance.

1.3 Creating Motions with Electrostatic Actuation by Nano-Watt Circuit

The concept of IoT was originally proposed to consist of sensors and computing resources. During its rapid development over the last two decades, actuators are also becoming a significant part of it and evolve more applications with micro-robot design. Recent research has presented an insect-sized robot named RoboBee [16], with wings driven by two alumina-reinforced piezoelectric actuators and integrated together with the electronics required for untethered flight.

Another research has brought the realization of programmable matter consists of tiny, mm-scale quasi-spherical robots called Catoms [17]. The concept of programmable matter (PM), defined as matter that can change its physical properties based on a user's input, has been pursued for a long time to achieve the ultimate vision of achieving a universal meta-material for use in

daily life. Improved 3D printing and VLSI/MEMS technology have enabled the realization of PM with millimeter-sized intelligent micro-robots [18]. PM consists of tiny, mm-scale quasi-spherical robots called Catoms, which can autonomously attach themselves in different positions to their neighbors using electrostatic forces. When different Catoms make surface contact, the difference in their surface potentials creates an electrostatic force, bonding them together (latching) or causing a rotation/movement (actuation). By combining thousands of Catoms, a morphable 3D structure can be programmed to take arbitrary shapes. The PM hardware structure can also be manipulated and changed externally while the resulting changes are tracked and captured using sensors inside each Catom and synchronized with a simulation/3-D model inside the software environment. Conversely, we can also modify the 3-D model through the software, and the Catoms will be actuated to reform the PM shape and reflect the change. This 2-way interaction induces a scalable, real-time, efficient, and expressive way of implementing a virtual reality. At the same time it creates an ensemble of micro-robots, which can interact with other communicating things through the IoT.

The realization of programmable matter (PM) requires a sophisticated system design, including geometry design, control algorithms, simulation, software-hardware co-design and industrial design [19] [20] [21] [22]. In this thesis we show for the first time a micro-controller design that resides in the Catom and supports its communication, computation, actuation and power management for autonomous operation. While introducing the complete micro-controller system using a chip stack, we focus on the chip layer that is related to actuation of the PM.

1.4 Dissertation Outline

This dissertation is composed of three chapters introducing the unique circuit and system designs for the above three topics. Chapter 2 presents a new energy extraction technique, sense-

and-set (SaS), to perform maximum-power-point-tracking (MPPT) in harvesting energy from piezoelectric energy harvesters (PEHs). Unlike previous PEH interface designs that relied on calibration to achieve high efficiency, SaS can automatically determine the optimal output voltage through a small "sensing phase" and thus keep maximum power extraction under arbitrary vibrations. The SaS circuit is fabricated with a 0.47 mm^2 single IC, and measured with 5.41× and 4.59× improvement in harvesting energy from periodic and pulsed vibrations, respectively.

Chapter 3 presents a triaxial MEMS capacitive accelerometer using a high-voltage biasing technique to achieve high resolution with ultra-low-power. The accelerometer system generates a pair of differential high-voltages and utilizes them to bias the MEMS structure, raising the MEMS signal way above the noise floor of the analog front end circuits. With the large signal-to-noise ratio, the proposed accelerometer system eliminates the power hungry low-noise amplifiers and signal chopping, and significantly improves the power-noise trade-off in the conventionally biased MEMS accelerometers. Moreover, the properly generated bias voltages compensate for the electrostatic mismatch on MEMS caused by using high voltages, and show a robust operation against MEMS process variation. The proposed accelerometer is fabricated with 1 MEMS and 2 CMOS chips, achieving a 121μg/ √ Hz input-referred noise floor with ±1.5g dynamic range, <1% linearity error and 184nW per-axis power (including high-voltage bias generation). Compared to prior arts, it achieves a 11.7× FoM improvement considering both power and noise specifications over the sensing bandwidth.

Chapter 4 presents a high-voltage-generation-and-multiplexer (HVGM) chip specially designed for electrostatic actuation of micro-robots for applications such as Programmable Matter (PM). PM consists of tiny, mm-scale quasi-spherical robots that can be combined and programmed to form any arbitrary 3-D shape autonomously. The HVGM individually controls 12 pairs of +/-

electrodes using a positive and negative charge pump and mux-structure, consuming only 286nW power when switching a 10pF electrode at 155V/s, and producing a differential voltage of 103V (29× voltage gain from 3.6V) in measurement. We also show a complete micro-system of stacked dies, measuring 3×1.4×1.1 mm, including the HVGM, a processor, radio, and harvester that achieves energy-autonomous operation, and can be integrated into a micro-robot "Catom" via a flexible PCB. Furthermore, we propose and fabricate the second version of the Catom controller that only consists of one chip, HVGMv2 for lower power and cost, while maintaining similar multi-functions of the stacked dies.

Each of Chapters 2 –4 is organized with first discussing on the design challenges, related previous works, and also the contribution of the proposed work. Then a detailed explanation of the proposed work will be given in the next 2~3 sections, including fundamental analysis and circuit implementation. In the conclusion parts, we will analyze the limitations of our work and propose future work for further improvement.

Chapter 2 An Efficient Piezoelectric Energy Harvesting Interface Circuit

2.1 Introduction

A piezoelectric energy harvester (PEH) converts mechanical strain into electrical charge by means of the direct piezoelectric effect [23], and the charge can be extracted to generate AC power (usually in the nW to mW range), which can be applied to the electrical load. The output power of a given PEH can be optimized in terms of these two processes. On one hand, the efficiency of the electro-mechanical energy conversion is optimized when the PEH is precisely vibrated at its resonant frequency, matching the natural characteristics of its mass-spring-damping system. This is rarely achieved in practical applications since most ambient vibration sources have a relatively unstable, broadband frequency spectrum [24]. Hence, some prior works have aimed to improve the bandwidth energy conversion, although with limited success [25] [26]. On the other hand, the design of interface circuits that perform impedance matching or maximum-power-point-tracking (MPPT) can significantly improve the charge extraction efficiency and thus increase the output power of the PEH. Most of the circuit techniques discussed in this thesis aim to improve the efficiency of this process rather than control the electro-mechanical conversion.

Among various interface circuits, full-bridge rectifiers (FBRs) are the most commonly used for their simplicity and stability [27] [28]. However, their power efficiencies are usually low since most of the PEH-generated charges are not extracted but remain within the large intrinsic capacitors of the PEHs. Several different techniques have been proposed to help with energy extraction from PEHs. The bias-flip (BF) technique, proposed by [29], manually sets a high bias-voltage at the PEH's output in order to extract more energy from a certain charge generated by the

PEH. When the charge generation (current) changes direction with the input vibration oscillation, the bias-voltage is flipped. This is performed adiabatically to limit the energy loss of the operation. Prior BF-based works generally achieved the highest power efficiency when compared to other energy extraction techniques, and they can be divided into two categories, synchronized switch harvesting on inductor (SSHI) [30] [31] [32] and synchronized switch harvesting on capacitor (SSHC) [33] [34] [35], depending on whether an inductor or a capacitor array is used for the voltage flip. Other charge extraction techniques, such as synchronous electric charge extraction (SECE) [36] and energy pile-up resonant circuit [37], are generally less power efficient than the BF-based circuits but offer other advantages such as being more suitable for non-periodic vibrations.

However, all the above techniques have disadvantages for maximum-power-point tracking (MPPT) while extracting energy from PEHs. Theoretically, SSHI and SSHC can achieve near-MPPT in energy harvesting, but they usually do not adapt to various input-vibration types (periodic or shock) and amplitudes, which decreases their power efficiencies in practical applications. SECE automatically adapts to different vibration amplitudes, but its efficiency is significantly degraded by the large intrinsic capacitor CP, and it generates unregulated output voltage for non-periodic vibrations.

In this chapter we present a sense-and-set (SaS) interface circuit for PEHs, which is fundamentally different from prior techniques and achieves MPPT for arbitrary input vibrations. The proposed SaS technique has the following advantages over prior art:

1. SaS dynamically senses the PEH's charge generation and sets the harvesting voltage accordingly. The power efficiency of SaS is thus adjusted to approach the theoretically limit.

2. SaS maintains MPPT for different vibration types, strengths/amplitudes and PEH characteristic parameters without the need to manually tune the circuit for each condition.
3. SaS produces rectified output voltage without an additional passive rectifier, which eliminates the conduct loss (voltage drop) associated with the rectifier diode and improves the efficiency, especially for low amplitude vibration (low voltage) applications.
4. SaS de-couples the output node from the input so that a fixed output voltage does not interfere with the MPPT. In previous techniques V_{OUT} needs to change with the vibration strength to achieve high power efficiency which clearly cannot be performed dynamically.

The remainder of this chapter is organized as follows. Section 2.2 presents the background of the PEH model and interface circuit approaches. The operation principle and implementation of the proposed SaS circuit are described in Sections 2.3 and 2.4, respectively. Section 2.5 shows the measurement results and analysis, while a conclusion is drawn in Section 2.6.

2.2 Related Works on the PEH Interface Circuit

2.2.1 Modeling of Piezoelectric Transducers

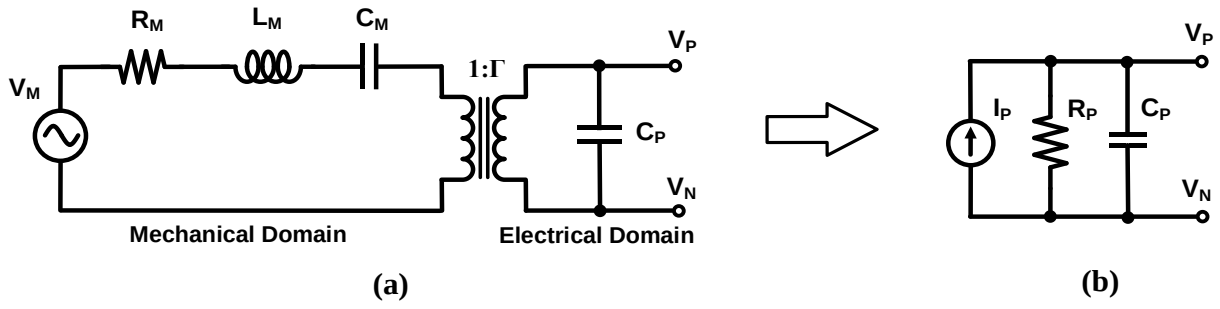


Figure 2.1: Modeling of piezoelectric transducer. (a) complete model with electromechanical coupling and (b) simplified model on resonant frequency.

The PEH or piezoelectric transducer generates electrical charges when the piezoelectric material is compressed or deflected by mechanical stress derived from external vibrations. It can be modeled as an electro-mechanical system as shown in Fig. 2.1(a). The left part of the model

illustrates the mechanical structure of the PEH, in which R_M, L_M and C_M are the equivalent circuit components for the mass-spring-damping system of the piezoelectric layer. With the electromechanical coupling factor Γ, power generated at the mechanical side is transformed to the electrical side and stored in the PEH intrinsic capacitor C_P. When the PEH is excited at or close to its resonant frequency, L_M and C_M are cancelled out, and the model can be simplified into a model without the transformer, as shown in Fig. 2.1(b), where

$$I_P = \frac{V_M}{\Gamma R_M} \tag{2.1}$$

$$R_P = \Gamma {R_M}^2 \tag{2.2}$$

I_P defines the charges generated by the PEH in a certain time, and R_P is the equivalent loss in the electro-mechanical conversion. According to the theory of maximum power transfer, the load receives maximum power

$$P_{max} = \frac{1}{4} {I_P}^2 R_P \tag{2.3}$$

from the current source when

$$V_P = V_{MPP} = \frac{1}{2} I_P R_P \tag{2.4}$$

However, the impedance of C_P is usually much smaller than R_P at the vibration frequency f (or ω). As a result, the V_P amplitude is much smaller than V_{MPP} even for the open-circuit condition

$$V_{P-OC} = I_P(R_P||X_{CP}) = \frac{I_P}{\omega C_P} \tag{2.5}$$

Since $1/\omega C_P \ll R_P, V_{P-OC} \ll V_{MPP}$. For the same I_P generated by the vibration, the low V_P value limits the power efficiency. Furthermore, V_P will be affected by the impedance-match condition between the PEH and interface circuits. The ideal interface circuit that delivers P_{max} to the load should achieve complete impedance matching to the PEH, where the load impedance $X_L = R_L + \omega L_L$ is given by

$$R_L = R_P, \qquad \omega L_L = \frac{1}{\omega C_P} \tag{2.6}$$

However, the required L_L value is usually hundreds of Henries, which is impractical for system-on-chip (SoC) or even on-board systems. Thus prior interface circuit designs tend to achieve better impedance match by placing V_P to be near V_{MPP}, which counteracts the negative effect of C_P. The following paragraphs will continue this discussion in more details.

2.2.2 Baseline Interface: Full-Bridge Rectifier

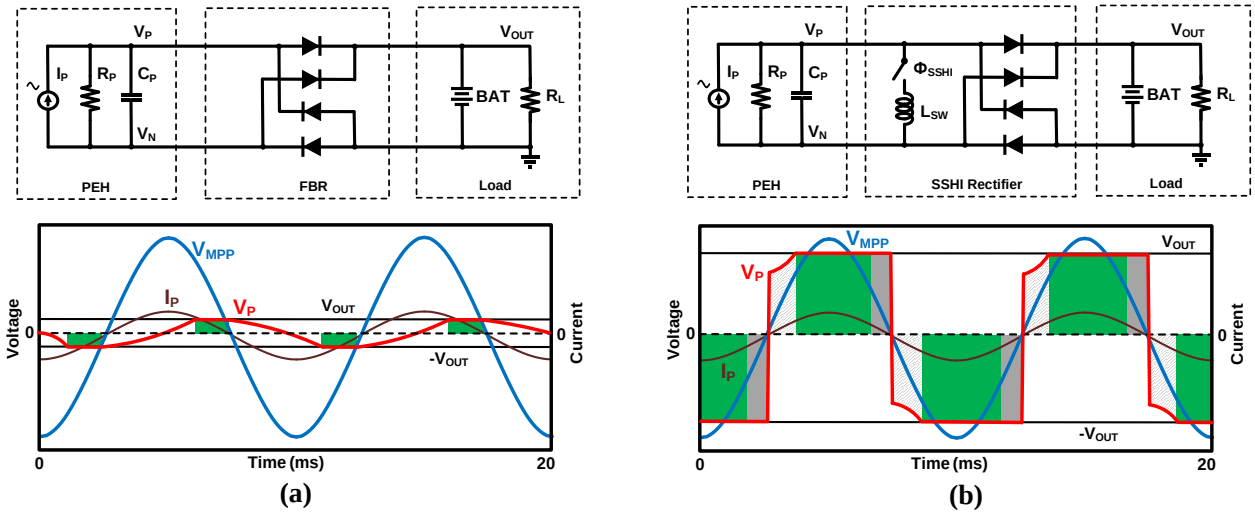


Figure 2.2: Schematic and waveform for piezoelectric energy harvesting through (a) FBR and (b) SSHI rectifier.

The FBR is the most widely used interface circuit that allows energy harvesting from PEHs. As shown in Fig. 2.2(a), the PEH current I_P first charges C_P until V_P reaches V_{OUT}. Then all of I_P will flow through the FBR diodes to the load (represented by the green region) except for the loss by R_P. When I_P changes direction with the input vibration, it must first discharge C_P to 0 and then repeat the voltage build-up process in the other direction. During the charge-discharge operation, no power is transferred through the rectifier.

In FBR circuits, the output voltage V_{OUT} must be between 0 and $V_{P\text{-}OC}$ in order to harvest energy from the PEH. Assuming ideal diodes (with no voltage drop) are used, the FBR delivers the maximum output power when V_{OUT} is equal to half of $V_{P\text{-}OC}$, according to [29].

$$P_{max-FBR} = fC_P{V_{P-OC}}^2 = \frac{{I_P}^2}{2\pi\omega C_P} \tag{2.7}$$

Comparing this to the theoretical maximum power we get

$$\frac{P_{max-FBR}}{P_{max}} = \frac{2}{\pi}\frac{1}{\omega C_P R_P} = \frac{2}{\pi Q_{PEH}} \tag{2.8}$$

where Q_{PEH} is the quality factor of the piezoelectric transducer. Since generally $1/\omega C_P \ll R_P$, then $Q_{PEH} \gg 1$ (in the range of 10-100 for most of PEHs), and the maximum output power delivered by a FBR is significantly lower than the theoretical maximum value.

2.2.3 Prior State of the Art: Bias-Flip Rectifiers

One reason for the low power efficiency of the FBR is that V_P is limited within $V_{P\text{-}OC}$, which is far below V_{MPP}, which is shown as the blue line in Fig. 2. 2(a). For the same PEH current I_P, this much lower voltage results in output power degradation. One effective way to improve is the efficiency is to manually set a bias voltage (usually higher than $V_{P\text{-}OC}$) on V_P so that the same

I_P produces larger output power. When I_P changes direction, the bias voltage is then flipped so that no energy is lost due to discharging C_P. The circuits that utilize such a "bias-flip" operation can be divided into two categories, SSHI [29] [30] [31] [32] and SSHC [33] [34] [35], depending on whether they use an inductor or a capacitor array for the voltage flip.

Fig. 2. 2(b) shows the schematic and waveform of an SSHI circuit. It still has an FBR for rectifying the output, but it has an additional switch-controlled inductor in parallel. V_P is set manually to be a fixed high voltage, as demonstrated by the red line. I_P will flow through the FBR to the load without charging C_P, as indicated by the green region. When I_P changes direction, discharging C_P is avoided by turning on the switch and shorting the PEH through the inductor L_{SW}. By precisely controlling the switch's turn-on period, Φ_{SSHI}, V_P will be adiabatically flipped to a slightly lower negative value due to the circuit loss during the flip. Then the inversed current IP charges V_P back to $V_{OUT,}$ and energy harvesting begins again at this voltage.

From previous discussions, we know that for each interface circuit, the energy extraction from the PEH peaks when V_P gets closer to V_{MPP}. In the SSHI circuit, that is when $V_P = V_{OUT} = Q_{BF}V_{P\text{-}OC}$, and the maximum power delivered by an SSHI rectifier is

$$P_{max-SSHI} = 2fC_P{V_{P-OC}}^2 Q_{BF} = \frac{{I_P}^2 Q_{BF}}{\pi\omega C_P} \tag{2.9}$$

where Q_{BF} is the combination of quality factors of the PEH and the C_PL_{SW} resonant circuit, and thus usually $1 \ll Q_{BF} < Q_{PEH}$. Again, we compare it to the theoretical maximum power

$$\frac{P_{max-SSHI}}{P_{max}} = \frac{4Q_F}{\pi}\frac{1}{\omega C_P R_P} = \frac{4Q_F}{\pi Q_{PEH}} \tag{2.10}$$

Although the power efficiency seems to be much better than that of an FBR, SSHI circuits does not achieve MPPT because the square-wave-shaped V_P does not track the waveform of V_{MPP},

which is defined by the vibration pattern (normally it will be a sine wave). In addition to the voltage-flip loss, which is shown by the dashed grey region in Fig. 2. 2(b), it also has a "dead time" when V_P is larger than $2V_{MPP}$ and all the current will flow through R_P instead of the FBR (solid grey region). More importantly, in order to achieve the peak output power, SSHI circuits must set the value of V_{OUT} wisely since it defines the amplitude of V_P, which further determines the output power. In practical applications, it is hard to predict $V_{P\text{-}OC}$ and set the correct V_{OUT} before the vibration happens. Also, the system output must be stable, not changing with the vibration's amplitude, and an additional voltage converter will be needed, which further decreases the total power efficiency.

These limitations were partly addressed by some recent energy extraction techniques, such as synchronous electric charge extraction (SECE) [36], which builds V_P by the input current I_P and harvests only at the peak value. However, these techniques lack the advantages of using a higher voltage at V_P, so the overall power efficiency is less than that of the BF-based technique.

2.3 Fundamentals of the Sense-and-Set Technique

To achieve MPPT for PEHs, V_P needs to be equal to V_{MPP}, whose waveform and amplitude varies with the vibration. Hence, there are two main challenges to dynamically adapt V_P to V_{MPP}:

1. Determining the value of V_{MPP}. It is not possible to directly observe V_{MPP} due to the large intrinsic C_P. Neither can we measure R_P in the circuit (and multiply it by I_P to get V_{MPP}) since it is not in the real electrical domain but derived from the electro-mechanical mode.
2. Maintaining V_P equal to V_{MPP}. If we determine V_{MPP} and V_P is adapted to the V_{MPP} level, its value will change with the oscillation. Since C_P is large, keeping V_P at/near V_{MPP} requires a large energy transfer to charge or discharge C_P, which results in

significant power loss.

Our proposed SaS technique addresses these two challenges by adiabatically estimating the value of V_{MPP} (the "sense" operation) and then adiabatically adjusting V_P to it (the "set" operation). The operation of sense and set will be introduced in the next paragraphs.

2.3.1 Sense Phase

As previously discussed in section II. A, a PEH's open-circuit voltage $V_{P\text{-}OC}$ is far less than V_{MPP}. The difference comes from the current that flows through C_P, and, hence, we can recover V_{MPP} by taking this current into account. Assuming the PEH is left in the open-circuit state, then

$$I_P = I_R + I_C \tag{2.11}$$

where I_R and I_C are the current flowing through R_P and C_P, respectively. I_R can be derived by V_P/R_P in which R_P is an unknown but fixed value for a given PEH. To measure I_C, we can wait for a short time period Δt and measure the voltage accumulation ΔV on capacitor C_P. I_C is approximately constant during Δt , and its value is given by

$$I_P = \frac{V_P}{R_P} + \frac{C_P \Delta V}{\Delta t} \tag{2.12}$$

Then V_{MPP} can be recovered by

$$V_{MPP} = \frac{1}{2} I_P R_P = \frac{1}{2}\left(V_P + \frac{R_P C_P}{\Delta t} \Delta V\right) \tag{2.13}$$

Since R_P, C_P and Δt are constant, we can "sense" V_{MPP} no matter what the current V_P is by measuring ΔV.

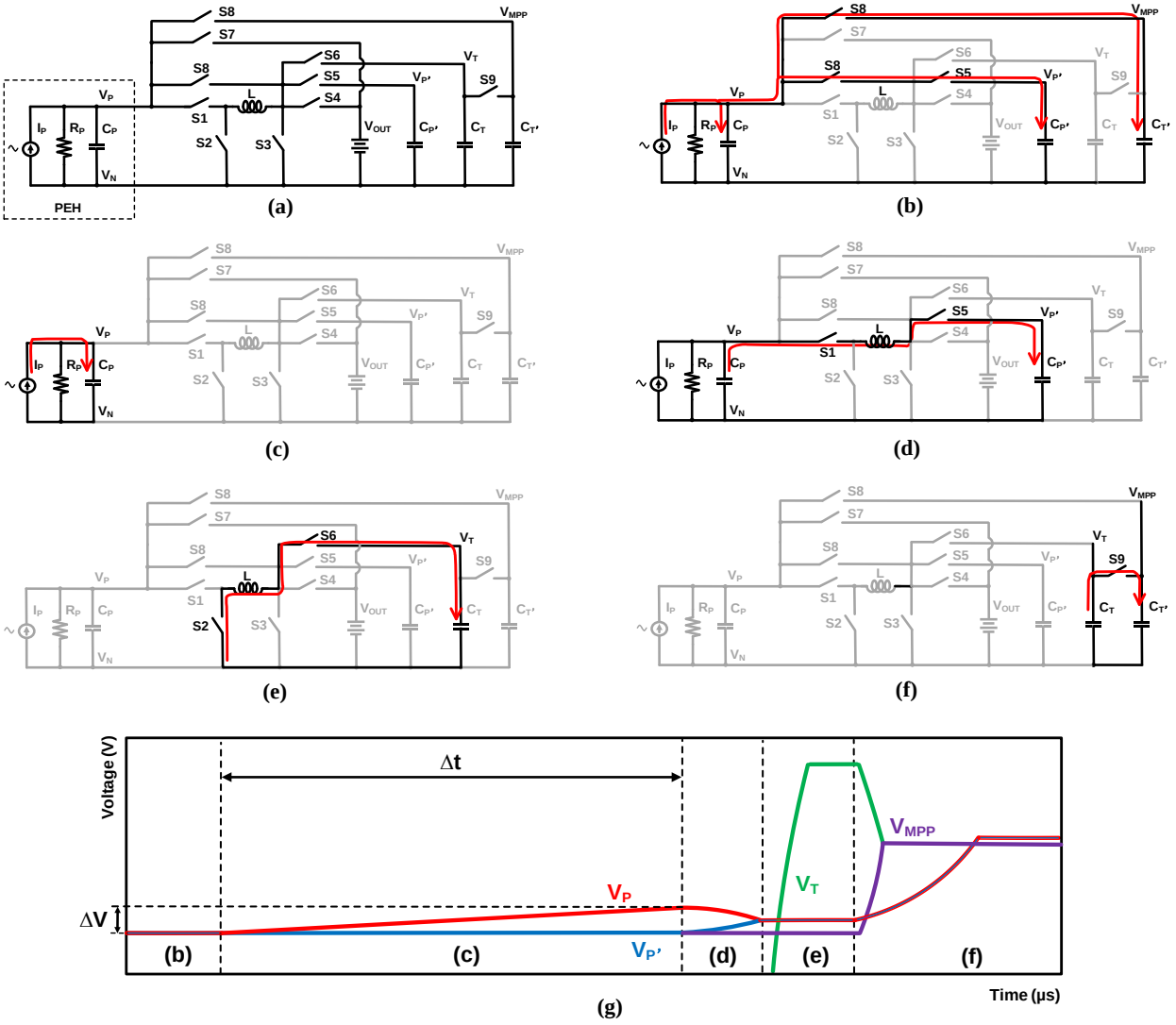


Figure 2.3: (a) SaS core circuit where C_P=$C_{P'}$, C_T=$C_{T'}$, (b) set initial voltage V_P on C_P, $C_{P'}$ and $C_{T'}$, (c) leave the PEH in open-circuit and let I_P only charge C_P, (d) short C_P and $C_{P'}$ through an inductor until their voltages merge, (e) transfer the energy in the inductor into the smaller capacitor, (f) short C_T and $C_{T'}$ to get V_{MPP}, and (g) waveforms showing the voltages for important nodes.

However, since we want to keep Δt relatively short (for the approximation that I_C is constant), the resulting ΔV is usually in the sub-mV range. In order to operate with such a small signal, it is necessary to design delicate amplification and offset-cancelling circuits, which induce large power overhead. Fortunately, the energy difference from ΔV on the capacitor C_P is not small due to the large value of C_P. In SaS we use an inductor-based amplification where we transfer the energy difference into a smaller capacitor to generate higher voltage (tens of mV). Then a serial-

to-parallel switched capacitor array is used to further convert it to higher voltage (hundreds of mV).

Fig. 2. 3(a) shows the SaS circuit schematic, which consists of multiple switches, capacitors and a shared inductor. It can be reconfigured to different sub-circuits during the sense phase as shown in Fig. 2. 3(b)-(f); the red curve shows the direction of current flow. Initially, C_P, $C_{P'}$ and $C_{T'}$ are at the same potential as they are all connected and charged by the PEH (b). When the sense phase begins, the PEH is left in open-circuit mode for the time Δt, and a voltage difference ΔV develops between C_P and $C_{P'}$ (c). Since C_P and $C_{P'}$ have relatively large capacitances, their energy difference is large, and we can use this for charge-based amplification. In Fig. 2. 3(d), we first short C_P and $C_{P'}$ through the inductor L to equalize their voltages, energizing L by

$$E_L = \frac{1}{2}\left[C_P {V_P}^2 + C_P(V_P + \Delta V)^2 - 2C_P\left(V_P + \frac{\Delta V}{2}\right)^2\right]$$

$$= \frac{1}{4} C_P \Delta V^2 \tag{2.14}$$

EL is then transferred into a much smaller capacitor CT in (e) to get a higher voltage VT

$$V_T = \sqrt{\frac{2E_L}{C_T}} = \sqrt{\frac{C_P}{2C_T}}\Delta V \tag{2.15}$$

By replacing the ΔV term in (2.13) with VT, we rewrite the VMPP expression as

$$V_{MPP} = \frac{1}{2} I_P R_P = \frac{1}{2}\left(V_P + V_T \frac{\sqrt{2C_T C_P {R_P}^2}}{\Delta t}\right) \tag{2.16}$$

If the constant $\sqrt{2C_TC_P{R_P}^2}/\Delta t$ is tuned to be 1, then V_{MPP} is the average of V_P and V_T. So in Fig.3 (f) we short C_T and $C_{T'}$ to generate V_{MPP} and we can set V_P to this value for MPPT operation.

2.3.2 Set Phase

The SaS circuit "sets" V_P to V_{MPP} after obtaining its value during the sense phase. The is performed by configuring the SaS circuit into an inductor-based up-down converter, as shown in Fig. 2. 4(a) and (b). Converting the voltage up and down are adiabatic processes; the blue path shows the charging or discharging current that energizes L, and the green path shows the energy-recycle back to the battery.

After converting V_P to V_{MPP}, the SaS maintains V_P around this value by disconnecting itself from the PEH, as shown in Fig. 2. 4(c). Then I_P gradually charges C_P, causing V_P to rise, and when $V_{P'}$ exceeds the preset threshold, SaS harvests from C_P by down-converting its voltage back to V_{MPP} to maintains MPPT. The harvested energy is then transferred to the load (battery), and V_{OUT} can be arbitrarily set regardless of the input amplitude.

The set phase lasts until V_{MPP} drifts away after a time period, and the SaS ceases energy harvesting and enters the sense phase again. The new sense phase happens at the old V_{MPP} value, and error-correction is performed to get the new V_{MPP}. Then SaS converts V_P to the new V_{MPP} and begins another round of harvesting. By re-sensing repeatedly at a higher frequency than the vibration, the SaS technique achieves energy harvesting that tracks V_{MPP} dynamically, as shown in Fig. 2. 4(c). Also, when the current crosses zero and changes its direction, there is a voltage flipping operation so that VP remains positive, as will be further explained in the next subsection.

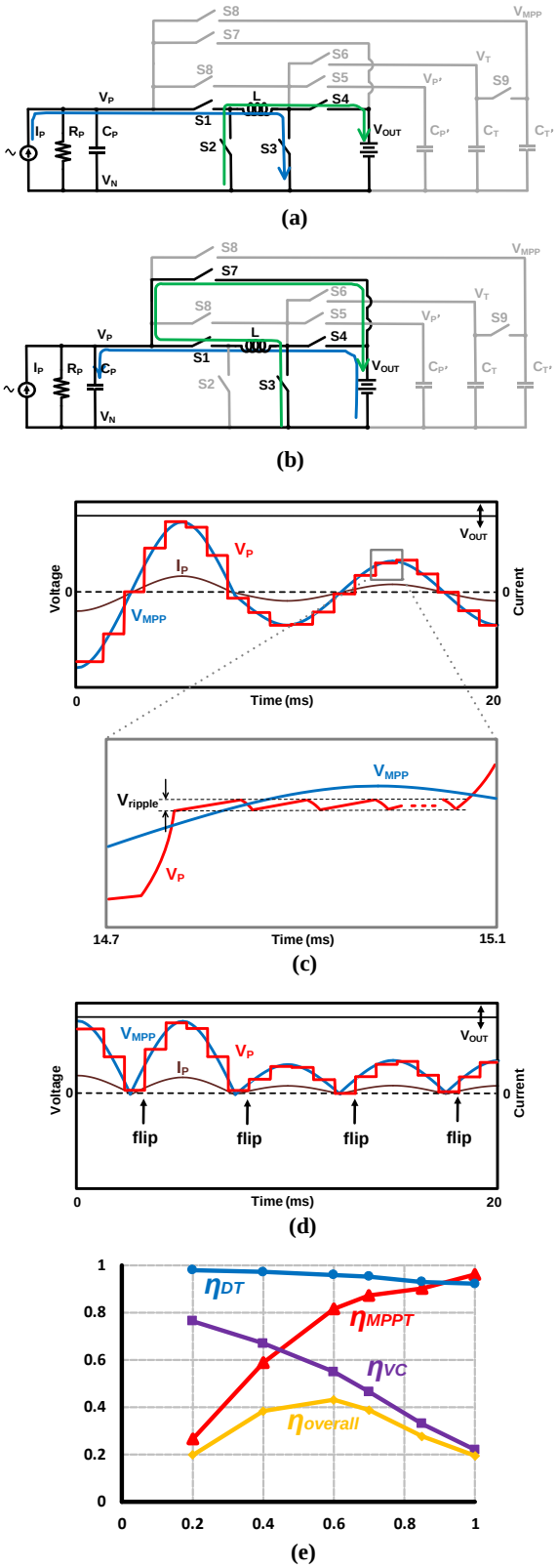


Figure 2.4: SaS rectifier in set phase. (a) down-convert operation and (b) up-convert operation, (c) SaS waveform (without voltage flip) and its zoomed-in region, (d) SaS waveform with voltage flip, and (e) SaS efficiency with different MPPT ratios.

Since SaS always performs energy harvesting near the maximum power-point, its power efficiency can approach 100% except for the loss caused by circuit non-ideality, which is given by

$$\frac{P_{SaS}}{P_{max}} = \eta_{MPPT}\eta_{DT}\eta_{VC} \tag{2.17}$$

In this equation, η_{MPPT} is the MPPT tracking error for V_P not perfectly following V_{MPP}, and η_{MPT} characterizes the dead-time loss since SaS does not harvest energy during the sense phase. There is a trade-off between η_{MPPT} and η_{DT} when choosing the sense-and-set frequency. More frequent SaS operations increases the V_{MPP} tracking precision and thus improve η_{MPPT}, but degrades η_{DT} because the circuit spends more time overall in determining V_{MPP}.

With the optimal frequency, the efficiency of $\eta_{MPPT}\eta_{DT}$ is usually around 85% or higher. However, the voltage conversion loss due to the switching and conduction activities usually dominate the total efficiency number. Although the inductor-based voltage converter has a high efficiency itself, it transfers the energy in C_P ($\propto C_P V_P^2$) which is several times larger than the energy generated by the PEH in each cycle ($\propto V_P^2/R_P$). Hence, the energy loss in the voltage conversion is amplified by this ratio, resulting in a low η_{VC}.

Figure 4(e) shows the post-pex simulation result for Equation (2.17). The X-axis is the proportion of V_P/V_{MPP} and Y-axis as the system overall efficiency. We know from previous sections that the efficiency should be optimized when V_P/V_{MPP} =1 in the ideal condition. However, larger V_P/V_{MPP} ratio results in larger amount of energy transfer, which significantly reduce η_{VC} as well as the overall efficiency. Hence, the system efficiency peaks at smaller V_P/V_{MPP} which means we track V_{MPP} at a proportion of its exact value. In such cases the overall efficiency is around 42%, mainly due to the low conversion efficiency. To further increase the overall efficiency, we could

probably use low-series-resistance (LSR) inductor or other converter topologies to reduce the conversion loss.

2.3.3 Flipping Phase

The advantages of SaS come from its dynamic adjustment of V_P according to the vibration waveform. However, this restricts the use of conventional rectifiers that handle negative voltages. To address this problem, we implemented a flipping phase which is a special case of the set phase. When the V_{MPP} generated in the sense phase is negative, it indicates that I_P has changed direction and V_{MPP} entered its negative half-cycle. V_P is then converted to this negative V_{MPP} as usual in the set phase but followed by a flipping operation where the connections to the two PEH terminals are swapped. As a result, V_P is flipped to the positive value and future V_{MPP} will stay positive until the next flipping happens.

The flipping phase happens twice for each vibration cycle and it ensures that V_P remains positive without use of rectifiers, as shown in Fig. 2.4 (d). Some energy loss may be incurred in the flipping operation, however, since the V_P values at the time of flipping is near zero the loss is typically negligible.

2.3.4 Calibration Phase

As previously mentioned in (2.16), it is necessary to tune the constant $\sqrt{2C_T C_P {R_P}^2}/\Delta t$ to be 1 so that V_{MPP} can be obtained by averaging V_P and V_T. Unlike C_P and C_T, the value of R_P is difficult to measure or control, and it varies among different PEHs. Moreover, there may be mismatches on V_T due to circuit non-idealities, resulting in inaccurate V_{MPP} estimates. To compensate for this, the SaS circuit performs self-calibration by adjusting the sense phase time Δt automatically without knowing the values of these parameters.

The calibration process is very similar to the sense phase in terms of obtaining V_{MPP}. But instead of entering the set phase, SaS converts VP to $2V_{MPP}$ and performs another sense operation at this voltage. If the voltage V_T appears to be negative (which means V_P was over-estimated in the previous sense phase due to a V_T constant larger than 1), SaS decreases Δt to get a lower V_T and compensate for the larger constant. The process is repeated, and Δt is adjusted in a digit-step manner until there is a positive V_T, which indicates over-tuning.

The calibration phase only needs to be performed once when SaS is connected to a new PEH. Once the right Δt value is tuned, the SaS circuit can harvest energy from the PEH with MPPT for arbitrary vibration inputs.

2.4 Circuit Implementation of Sense-and-Set

2.4.1 Inductor-Sharing Circuit

The top-level schematic of the proposed SaS circuit is shown in Fig. 2.5. The lower part is the inductor-sharing circuit, which performs the adiabatic SaS operations. In addition to what was described in the last section, there is one additional switch pair that connects PEH with the SaS input to assist the flipping phase. By combining the 'flip' switch with the up-down converter that was previously introduced, SaS eliminates the passive rectifier which limits the efficiency for low vibration (voltage) applications.

All switches are implemented with CMOS transmission gates but with different sizing considerations. For switches with only a control purpose, minimum-sized transistors are used for low switching loss. For the switches on the power path between the PEH and the load, the transistor sizes are selected to optimize the total conduction loss and switching loss during voltage conversion. A list of detailed switch sizes and other parameters can be found in Table 2.1.

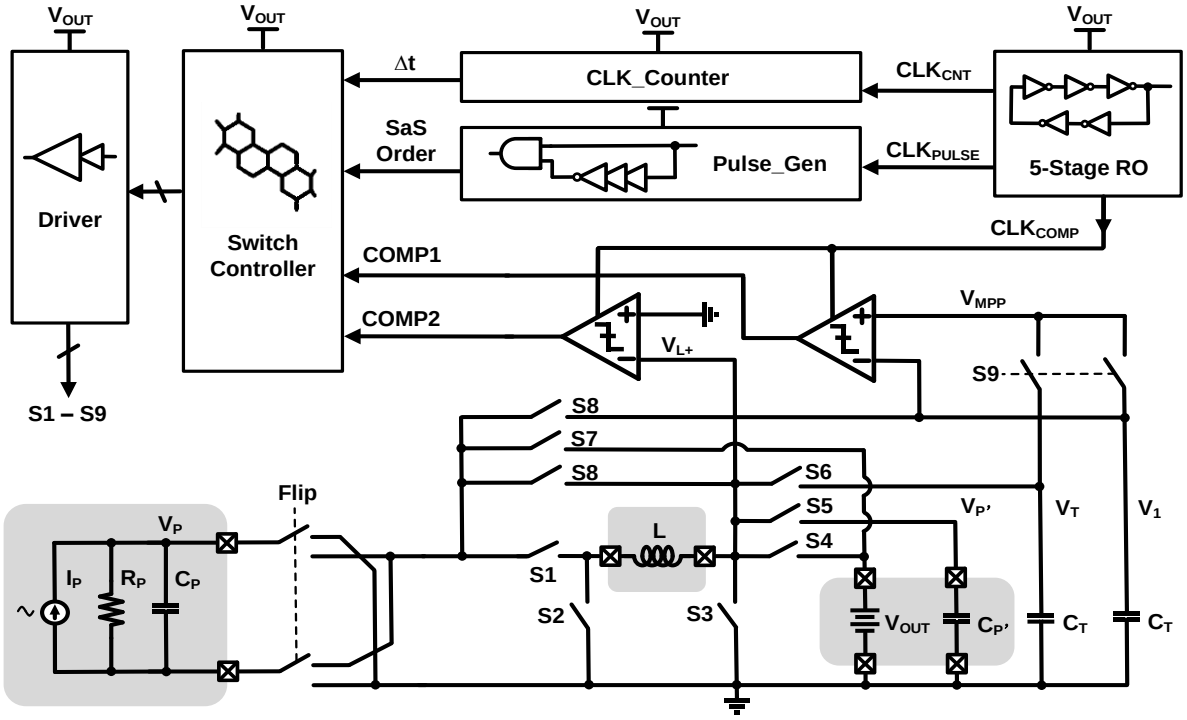


Figure 2.5: Top-level diagram for the proposed SaS circuit (greyed area indicates components that are off-chip).

Component	Parameters
S1 - S4, S7	W/L = 100µm/0.5µm
S5 - S6, S8 - S9	W/L = 0.5µm/0.3µm
Flip Switch	W/L = 200µm/0.5µm
C_P, $C_{P'}$	10nF
C_T, $C_{T'}$ *	1pF

Table 2.1: Circuit Parameters of the Sense-and-Set Circuit

* In order to increase V_T we prefer C_T to be small. However, there is a relatively large parasitic capacitor for the off-chip inductor, so we want to keep C_T large enough to overcome the parasitic loss during the amplification. The decrease on amplify ratio is then compensated by a parallel-to-serial switched capacitor circuit.

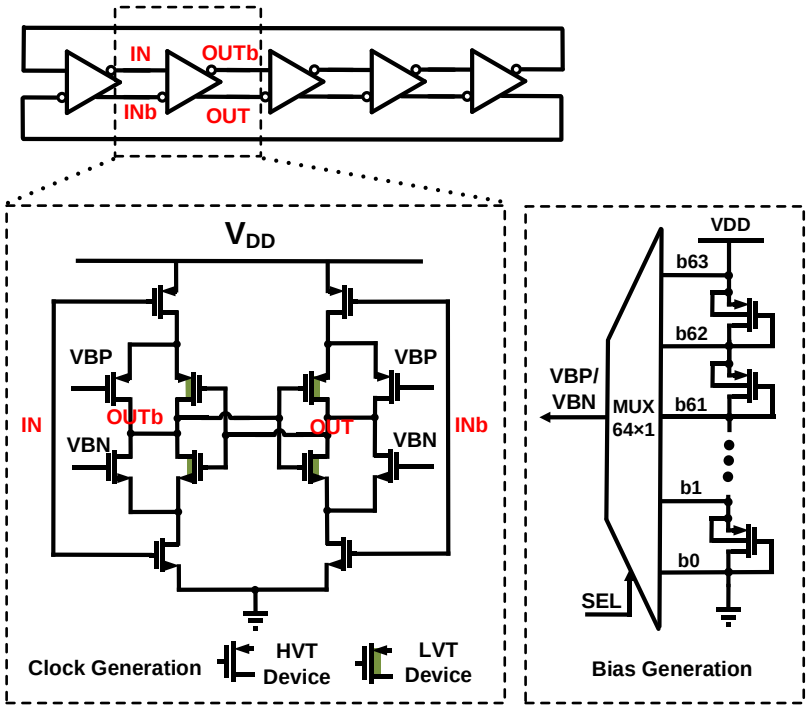
2.4.2 Clock Generator

SaS clocks are implemented on-chip and divided into three domains:

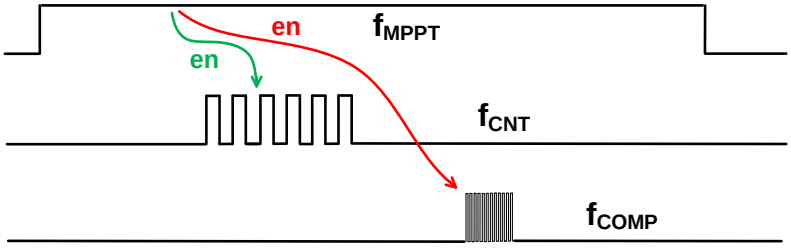
1. The MPPT clock (fMPPT) defines the frequency of SaS refreshing its VMPP value by performing SaS operations. This clock frequency, which is denoted by fMPPT, is usually in the 1 KHz range, tens of times higher than the vibration frequency.
2. The digital counter clock (fCNT) is related to the sense phase time Δt. Since $\Delta t = N_{CNT}/f_{CNT}$, a larger fCNT means finer control over Δt but higher power overhead. Hence the clock frequency is choses to be 100 kHz.
3. The comparator clock (fCOMP) runs the clocked-comparator and controls the switches for voltage conversion and is implemented to be 10 MHz in order to achieve high power efficiency by decreasing timing errors.

For low power operation, the three clocks are generated with the 5-stage ring oscillators (ROs) proposed by [38] to achieve constant energy-per-cycle across wide frequency range. As shown in Fig. 2. 6(a), the ROs consist of leakage-based inverters with an additional low-V_{th} (LVT) device pair in the middle. When the input voltage flips, the leakage path through the LVT latch controls the delay of output toggling and determines the oscillation frequency. Further tuning on the frequency can be achieved by adding a current path with the parallel transistors. The voltage to bias the parallel transistors (V_{BP} or V_{BN}) are generated by diode-connected transistors and selected with a 64-to-1 Multiplexer.

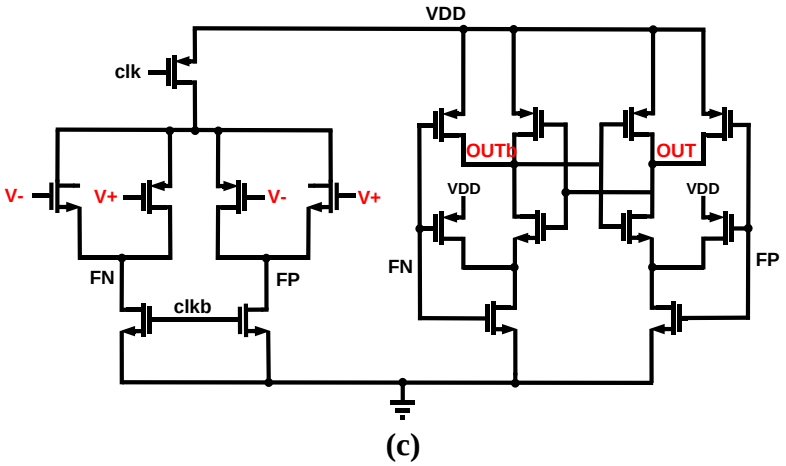
Among the three clocks, f_{MPPT} needs to be always-on in order to track V_{MPP} in real time. It will result in large power overhead if we run the oscillator at 10MHz and divide it to generate f_{MPPT}. Instead, we implemented three separate ROs in SaS, and the fast ROs (f_{CNT} and f_{COMP}) are only awoken when their controlled blocks are used. Fig.6 (b) shows the duty-cycled clocks for the counter and comparators.



(a)



(b)



(c)

Figure 2.6: (a) Circuit schematic of the 5-stage ring oscillator and its biasing circuit, (b) f_{CNT} and f_{CMOP} that run at higher frequency are awoken by f_{MPPT} at a specific time, and (c) the 2-stage comparator schematic.

2.4.3 Pulse Generation and the Clock Counter

The sequential SaS operation is hard-coded in the SaS, and its order is determined by the pulse generation circuit. The circuit takes f_{MPPT} as input, propagating its rising edge through multiple delay stages, and generates pulses that activate different switches in SaS. The delay cells are similar to what is used in clock generation, with specific bias voltage to control its delay and the pulse width.

Especially, the pulse width that defines Δt cannot be hard-coded as it needs to be adjustable during the calibration phase. So, we implemented a digital counter that counts f_{CNT} until it reaches a given number N. Then we have

$$\Delta t = \frac{N}{f_{CNT}} \tag{2.18}$$

where f_{CNT} determines the resolution of Δt, and N gives the range. The value of N is stored in another counter-like structure that is kept tuned during the calibration phase.

2.4.4 Comparators

The SaS circuit performs voltage conversion when it changes V_P. The voltage conversion efficiency η_{VC}, which dominates the overall SaS efficiency as we discussed, is affected by the timing error of the switches. To determine the correct timing signals for the switches, we implemented two comparators in SaS as shown in Fig. 2. 6(c). The first one compares V_P with the target voltage and produces turn-off signals when V_P has been converted to the target voltage. The second one performs cross-zero detection for the inductor L's current by measuring its terminal voltage and helps with the energy recycling from L.

In order to control the switching activities for voltage conversion while maintaining high efficiency, the comparator clock signal f_{COMP} needs to be approximately 10MHz to reduce timing error. We implemented f_{COMP} in a highly duty-cycled manner where only when a switching activity begins, the fastest oscillator is enabled and provides clocks to the comparator. Since the switching time is only a small portion of the total sense-and-set time, both the comparator and the corresponding oscillator will be idle for most of the time. By this technique we reduced the power consumption of timing control from 14.5μW to 151nW, as shown in Section 2.5.

2.4.5 Switch Controller and Switch Drivers

The sequential signals generated by the pulse generator, clock counter and comparators need to be mapped into the final control signals that apply to S1–S9. Thus, a look-up table is implemented, and the switch control signals are buffered to drive some of the large switches in SaS. The power supply for the switch controller as well as other circuit blocks comes from V_{OUT}, which is the harvested energy. But for testing purpose we use separate 2V supply so that we can quantify the power consumption by the SaS circuit. To extend the output voltage and the operation range of SaS, the switches can be implemented with high-voltage transistors, and a level converter may be inserted between it and the controller circuit.

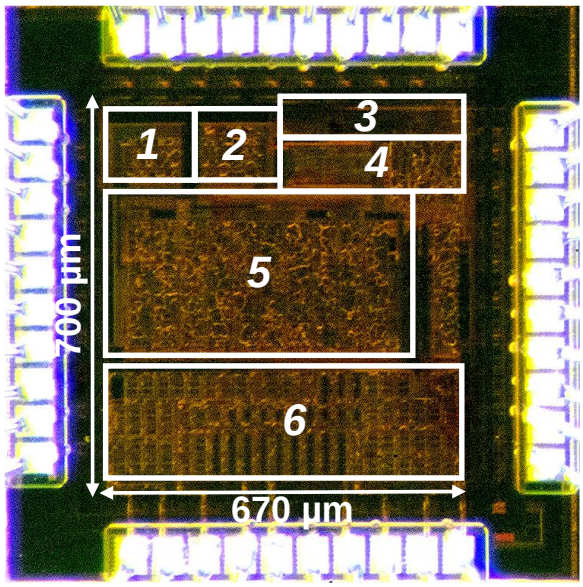


Figure 2.7: Micrograph of the test chip fabricated in 180-nm CMOS process. The active area of the circuit is 0.47 mm^2. 1: bias voltage generator; 2: ring oscillators; 3: scan chain for tuning; 4: clocked comparators; 5. Pulse generator; 6: Inductor sharing circuit.

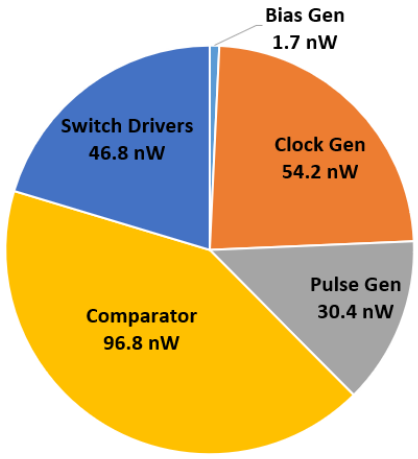


Figure 2.8: Breakdown of power consumptions of SaS sub-circuit blocks under normal operation. The total power (230nW) is measured in room temperature and the proportion numbers come from post-pex simulation.

2.5 Measurement Results and Analysis

The proposed SaS circuit [39] [40] is designed and fabricated in 180-nm CMOS process with a core area of 0.47 mm^2 as shown in Fig. 2.7. The measured leakage and active power in room temperature for SaS are 7nW and 230nW, respectively, and Fig. 2.8 shows the power proportion of each circuit block when SaS is in operation. In addition, 91% of the clock generation power and

88% of the comparator power are related to the high frequency operations (f_{COMP}), while the latter only take about 1% of the total operation time. The fabricated chip was tested with a commercially available piezoelectrical transducer, PPA-1022 from Mide Technology. The transducer was clamped on the PPA-9001 kit (position 0 with 11.2g tip mass) and mounted on a shaker table (Sentek Dynamic IA20N) as the vibration source. The transducer is excited with 85Hz sinusoidal signal (off-resonance), 53Hz sinusoidal signal (on-resonance) as well as pulse/chock signals.

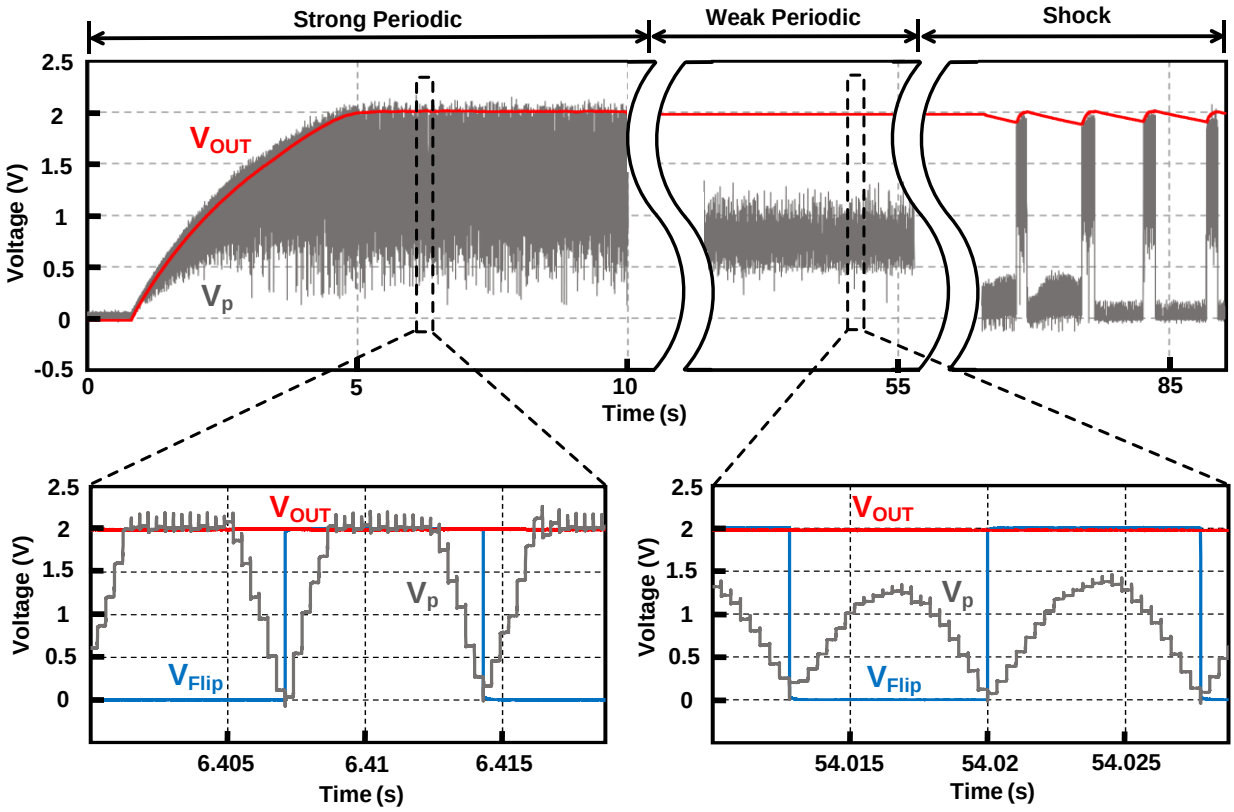


Figure 2.9: Measured transient waveform of V_P, V_{OUT} and the V_{Flip} (flip control signal) under different vibrations in the long term (top) and its zoom-in regions (bottom). Amplitude/frequency for strong and weak periodical vibrations are 2g/85Hz and 0.2g/85Hz, respectively. The shock vibration has an amplitude of 3g, with a (rough) period of 1 second.

Fig. 2.9 shows the SaS start-up and harvesting waveforms with 85Hz periodic and shock vibrations. Given an initial vibration to the PEH, the SaS circuit harvests energy from it and gradually builds up V_{OUT} and V_P amplitude until they reach 2V, the voltage limit for this CMOS

process. Since the V_{MPP} value for the strong vibration may exceed 2V, V_P stops tracking it but maintaining at 2V to approach V_{MPP}, and SaS performs partial MPPT for energy harvesting (left bottom in Fig. 2.9). This limitation can be removed by implementing the inductor sharing circuit in high voltage process so that higher V_{OUT} can be expected. When the input vibration is relatively weak (right bottom in Fig. 2.9), V_P tracks V_{MPP} for its whole period, and optimized energy extraction from the PEH is achieved. If the vibration is of pulse type, which is common in practical applications, V_P still tracks the input and performs MPPT for the activation period and remains static for the intermittent time. In addition, V_{OUT} is kept at the same value with the different vibration strengths and types, which decouples the output node from the input and makes SaS self-adaptable to various vibration sources.

We measured the electrical output power of the PEH using an SaS circuit and compared it with that obtained using an ideal FBR, which we implemented off-chip with active diodes (MAX40200 with <10mV voltage drop). Fig. 2.10 (a) and (b) show the measured output power versus different V_{OUT} values at the PEH resonant frequency. For low vibration strengths such as in Fig. 2.10 (a), the FBR power is limited by its low V_P, while the SaS circuit can convert V_P to higher values and tracks V_{MPP}. Therefore SaS achieves 4-5 times higher efficiency than the FBR (which means the FoM is around 4 to 5). For relatively stronger vibrations such as Fig. 2.10 (b), the resulting open-circuit voltage is higher and FBR achieves better power efficiency. In such cases V_{MPP} amplitude may be larger than 2V, and SaS can only converts V_P to 2V to approach V_{MPP}. As a result, the SaS achieves less efficiency gain over the FBR due to its voltage limitation.

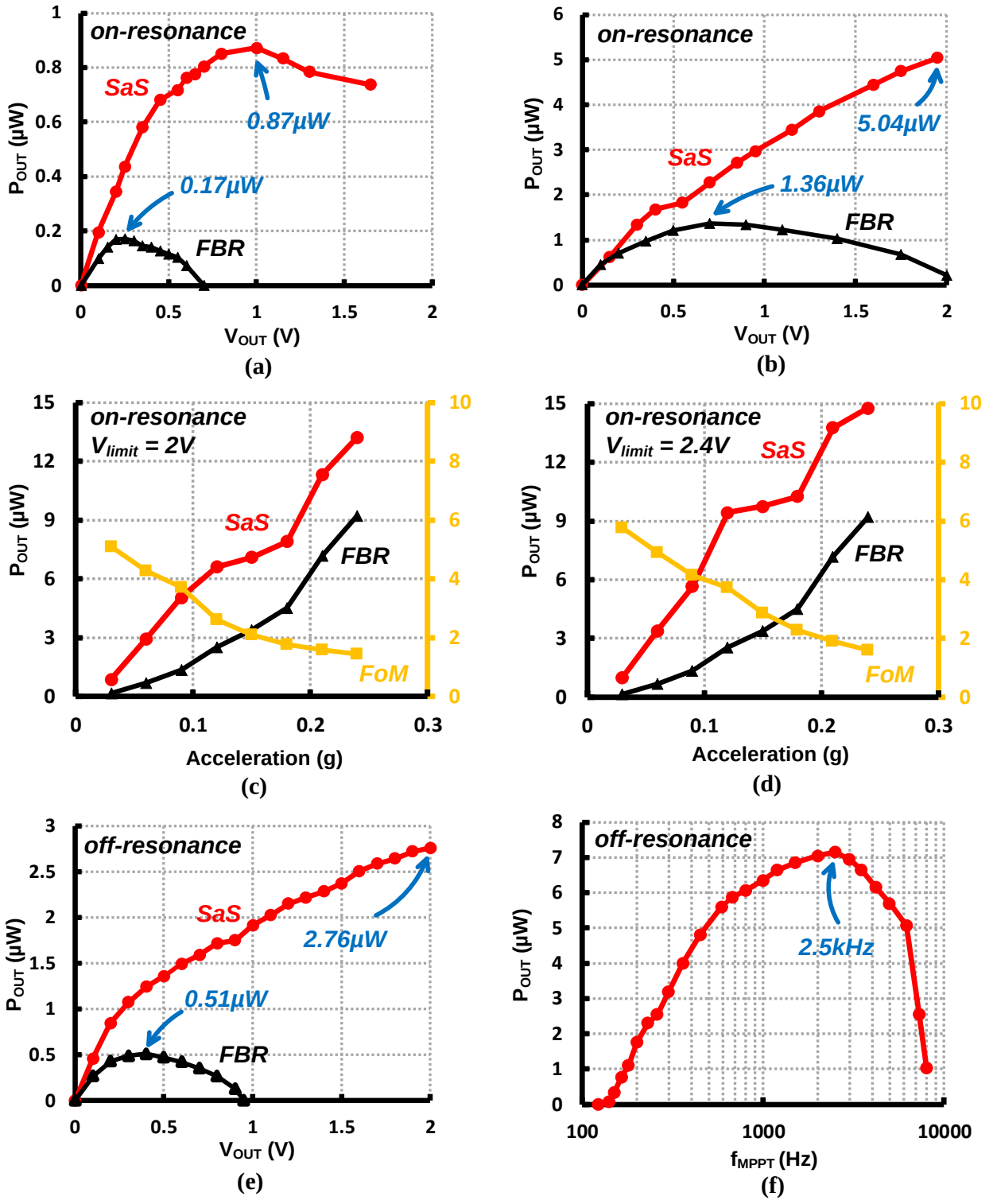


Figure 2.10: Measured output power of SaS and ideal FBR for (a) different V_{OUT} values with 0.03 g/53 Hz vibration, (b) different V_{OUT} values with 0.09 g/53 Hz vibration, (c) different vibration strengths with V_{limit}=2V, (d) different vibration strengths with V_{limit}=2.4V, (e) different V_{OUT} values with 0.5 g/85 Hz vibration and (f) different f_{MPPT} values and (f) different input vibration strengths.

Fig. 2.10 (c) shows the relationship of the output power of SaS and FBR over different vibration strengths. Given the mentioned process voltage limit (2V), the stronger input vibration is, the less efficiency gain can be achieved by SaS because V_P will be more limited. Hence the current version of SaS is suitable for low-amplitude-vibration applications, such as harvesting energy from wind-induced vibration of a window or the oscillation of a bridge under traffic. However, this disadvantage can be addressed by increasing the voltage limit by changing technology or transistor type. In Fig. 2. 10(d) we show that by temporarily increasing V_{limit} to 2.4V, the SaS achieves better FoM in all testing cases, especially for stronger vibration conditions. Further increase in V_{limit} can be done by implementing the voltage comparator and power switches in high voltage process, and in such case the SaS circuit could gain high FoM for wider input power range.

We also measured the output power and the corresponding FoM for off-resonance vibrations, as shown in Fig. 2. 10(e). The behavior of SaS stays similar except for the lower power level at the same vibration strength. Another factor that influences the SaS output power is f_{MPPT}, which determines how frequently SaS adapts V_P to V_{MPP}. A low f_{MPPT} results in a large tracking error and low η_{MPPT}, as shown in Fig. 2. 10(f), but if SaS adapts V_P too frequently, its dead-time will become evident, and η_{DT} is degraded. For the input vibration with 85 Hz frequency, SaS produces its maximum power with f_{MPPT} being 2.5 kHz, which is about 30 times faster than the vibration. Generally, the optimal value of f_{MPPT} will be between 20-35 times the vibration frequency according to the measurement results.

Publication	Process	Tech-nique	PEH Type	C_P	Frequency	Input Type	$V_{P\text{-}OC}$	FoM (periodic)	$\frac{FoM}{Q_{PEH*}}$	FOM (shock)	Input/output decoupling
JSSC 2010 [23]	0.35µm	SSHI	MIDE V22B	9nF	225Hz	Periodic	2.4V	4×	0.168	N/A	No
JSSC 2016 [24]	0.35µm	SSHI	MIDE V21/22B	9.6 - 27nF	134.6-229.6Hz	Periodic & Shock	0.8V	6.81×	0.286	2.69×	No
CAS 2017 [26]	0.25µm	SSHI	MIDE V22B	19nF	144Hz	Periodic	4.9V	2.07×	0.087	N/A	No
ISSCC 2018 [27]	0.18µm	SSHC	Custom MEMS	1.94nF	219Hz	Periodic	2.5V	3.58 - 8.21×	Unknown	N/A	No
JSSC 2017 [28]	0.18µm	SSHC	PSI-5A4E ($5mm^3$)	78.4pF	110kHz	Periodic	2V	4.83×	Unknown	N/A	No
JSSC 2017 [29]	0.35µm	SSHC	MIDE V21BL	45nF	92Hz	Periodic	2.5V	2.7-9.7×	0.057-0.206	N/A	No
ISSCC'18 [30]	40nm	SECE	MIDE PPA-1011	43nF	75.4 Hz	Periodic & Shock	2.85V	3.14×	0.132	4.20×	No
ISSCC'14 [31]	0.35µm	Energy pileup	Unknown	220nF	100Hz	Periodic	1.3V	4.22×	Unknown	N/A	No
This Work	0.18µm	SaS	MIDE PPA-1022	8nF	53Hz	Periodic & Shock	2.13V	5.12×	0.299	4.59×	Yes
					85Hz		0.95V	5.41×	0.316		

Table 2.2: Performance Comparison with State-of-the-Art Piezoelectric Energy Harvester Circuit.

*The value of Q_{PEH} is measured for this work to be 17.12, and the value for other works are estimated from the product datasheet. For example, from the datasheet of Mide V22B we know its capacitance CP=9nF and the serial resistor RM=2.4kΩ at f=100Hz. Using a common Γ value of 42, we calculated the quality factor of this device to be 23.8.

Table 2.2 compares the proposed SaS circuit with prior state-of-the-art works on piezoelectric energy harvesting. The first three columns show basic information about the circuits, and the next two columns summarize the specifications of the tested PEHs. The next three columns show the vibration frequency, input type and amplitude in which the PEHs were tested. The output

power of each PEH is measured using energy extraction techniques and normalized with their FBR counterpart, which gives each circuit's figure of merit (FoM).

Among the different techniques, SaS achieves a high FoM for the on-resonance (5.12×) and off-resonance (5.41×) input vibrations, as well as shock vibrations (4.59×) and weak vibrations (5.56×). Furthermore, from (2.8) we know that

$$\frac{P_{max-FBR}}{P_{max}} = \frac{2}{\pi Q_{PEH}} \propto \frac{1}{Q_{PEH}} \tag{2.19}$$

which means the FoM number is heavily related to the PEH parameters and does not solely reflect the improvements from the circuit techniques. Hence, we propose to normalize the FoM with $1/Q_{PEH}$ so that it reflects the harvester's output power as a ratio of its theoretical maximum value. Although Q_{PEH} varies with device tuning and setups, we have found two ways to obtain its value during testing:

3. Excite the PEH at its resonant frequency, and then plot the signal waveform which is used as the excitation input (same phase with IP) and the resulting PEH open-circuit voltage (VP). From the phase shift of these two waveforms we can calculate the effective quality factor Q for the RC network of PEH.
4. If the above method is not available, we can observe QPEH by giving the PEH a shock vibration. In such case VP will be a damped since wave, and according to the definition of quality factor, QPEH equals (to the first order) to the cycles that the sine wave decays to the 5% of its initial value.

For our PEH (Mide PPA-1022) the Q value is found to be 17.1 via the first method, and for prior papers we estimate the Q_{PEH} with its product datasheet. Using this normalized FoM, SaS achieves the highest gain (0.299 and 0.316) among all other energy extraction techniques for on-

and-off resonance vibration inputs. This confirmed the simulation results shown in Section III, and to further improve this FoM we could use low-series-resistance (LSR) inductor or other high-efficiency converter topology in future designs. In addition, SaS is the only technique that eliminates the input-output coupling effect. If V_{OUT} is high enough, its value doesn't need to be changed according to the input amplitude to guarantee the optimal harvesting condition. This feature helps SaS maintain a stable output voltage under vibration or load changes, making it suitable for various applications.

2.6 Conclusion

In conclusion, this chapter presents a new energy extraction technique, sense-and-set (SaS), for piezoelectric energy harvesting. SaS performs MPPT by dynamically sensing and setting the optimal voltage (V_{MPP}) for the PEH. It also adapts to various input vibrations and load changes while maintaining the peak output power. The SaS circuit was fabricated in 180-nm CMOS process with a core area of 0.47 mm^2 and static power of 7 nW. Tested with a commercial PEH (PPA-1022), the SaS chip extracted 5.41× and 4.59× more power from a PEH compared with that obtained with an ideal FBR, and the normalized performance number is the highest among all prior works.

Chapter 3 An Ultra-Low-Power Triaxial MEMS Accelerometer with High-Voltage Biasing and Electrostatic Mismatch Compensation

3.1 Introduction

MEMS capacitive accelerometers with CMOS readout circuits (RoC) are increasingly important in IoT for object monitoring and gesture recognition, due to their miniaturized volume and low noise operation. In prior works for capacitive MEMS accelerometers, there is a fundamental trade-off between its resolution and power, limiting their application in either high-resolution with high power [41] [42] [43] [44] [45] [46], or lower power but sacrificing the sensing resolution [47] [48] [49] [50]. The reason behind this is the trade-off between AFE noise and power. For high-resolution accelerometers, it needs to keep an ultra-low noise floor for its AFE circuit so that the signal-to-noise ratio (SNR) is not limiting its overall resolution. As a result, low noise amplifiers and signal chopping techniques are adopted to reduce the thermal noise and flicker noise, respectively, with trading-off the circuit power for their operation. The accelerometers can achieve a resolution <1mg, or power consumption of <1μW, but it remains challenging to break the trade-off and achieve both specifications simultaneously. For even higher resolution in μg levels, prior works adopts a feedback from the AFE output to the MEMS structure [51] [52], further reducing the Brownian noise. But similarly, this requires excessive power for the implementation and dramatically increases the overall power of the accelerometer.

One way to work around this resolution-power dilemma is to increase MEMS signals. Instead of reducing the AFE/MEMS noise and paying the power budget, we could increase the MEMS sensitivity so it can produce a larger signal with the same acceleration, equivalently

improving SNR and the accelerometer resolution. The increase in MEMS sensitivity can be achieved by two approaches: 1) reducing the stiffness of the MEMS spring and making it move a larger distance with the acceleration; 2) increasing the bias voltage on the MEMS to generate a larger electrical signal. The first approach requires re-designing the MEMS structure [53] and may cause the increase of Brownian noise. The second approach, while it seems to be promising with pure electrical implementation, will result in electrostatic feedback to the MEMS sensing element [54] [55]. The higher-than-normal bias voltage is a double-side blade that increases the MEMS sensitivity while destabilizing the MEMS operation and causing non-linear behaviors due to the existence of larger electrostatic force. It also raises challenges in generating sufficient, well-controlled high voltages with acceptable power overhead, and designing the AFE circuit according to the enlarged MEMS signals.

To address these challenges, we present a triaxial MEMS capacitive accelerometer [56], consisting of 1 MEMS chip and 2 CMOS chips, and with the following advantages:

1. The proposed accelerometer adopts a >10 higher MEMS bias compared to the conventional biasing scheme, resulting in a >40 larger MEMS signal. This significantly relieves the noise requirement for the AFE circuits, making it possible with nW-levels circuits.
2. Aware of the electrostatic feedback to the MEMS structure, the proposed accelerometer generates the high-voltage bias with an electrostatic-mismatch-compensation (EMC) technique described in this chapter. It guarantees an optimal MEMS biasing with large signal increase and sufficient dynamic range, while further compensating for process variation during the MEMS fabrication.

3. The high-voltage bias generation with EMC is implemented with a high-voltage companion chip that only consumes sub-μW in generating >40V bias voltage with <0.1% errors/ripples. The AFE circuit is also customized with ultra-low-power amplifier designs and high-voltage protection designs for better robustness.
4. Since the high-voltage biasing technique with EMC is newly proposed, we quantitatively analyze its performance with different chip samples and wafers, showing its robustness against process variation. We also test and confirm the good reliability of this technique by intentionally triggering the bias failure (pull-in) for >10000 times.

The remainder of this chapter is organized as follows. Section 3.2 presents the advantages and challenges of using high-voltage bias for MEMS capacitive accelerometers, and the analysis of electrostatic mismatch compensation. Section 3.3 and 3.4 describes in detail the implementation of the high-voltage companion chip and the MEMS-CMOS AFE chip, respectively. Section 3.5 shows the measurement of the proposed accelerometer system with its sensing performance and robustness against process variation. A conclusion is drawn in Section 3.6.

3.2 Proposed High-Voltage MEMS Biasing with Electrostatic Mismatch Compensation

3.2.1 Fundamentals of the MEMS Capacitive Accelerometer

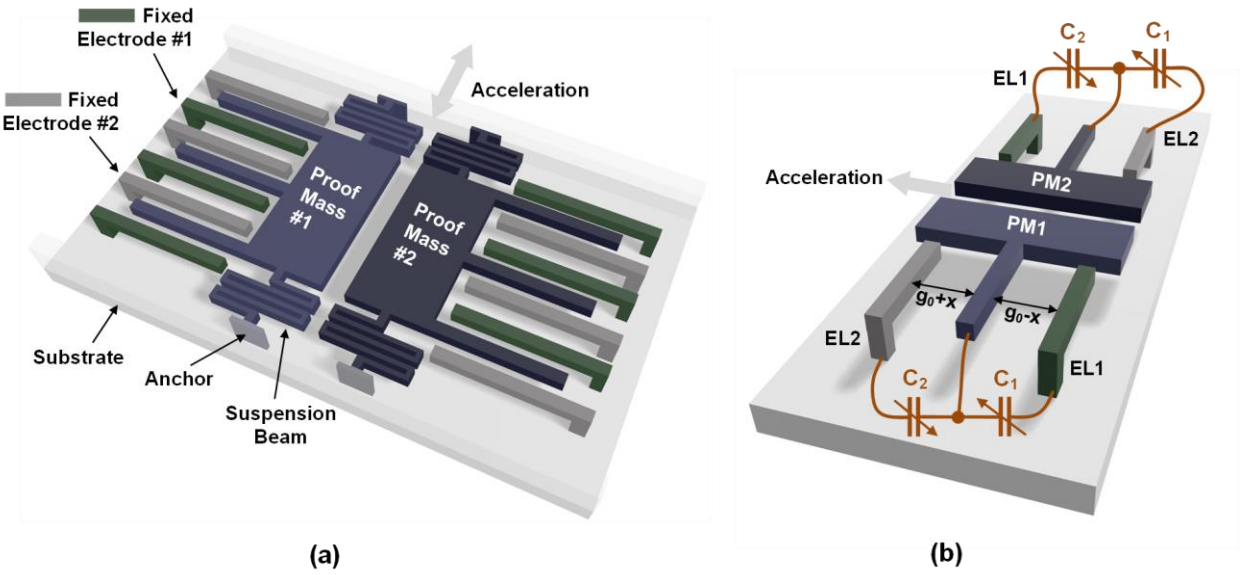


Figure 3.1: (a) Simplified diagram of a fully differential MEMS capacitive accelerometer; (b) zoomed-in diagram showing the coupling capacitance between the MEMS proof-masses and electrodes.

The sensing element of a MEMS capacitive accelerometer is a micro-mechanical structure consists of fixed electrodes and movable proof-masses. Both the electrode and the proof-mass have multiple fingers that cross-coupled together, forming the coupling capacitance between the fingers. When an acceleration occurs, the proof-mass fingers deflect from its initial position while the electrodes stay stationary (related to the substrate), changing the gap distance between them and causing a capacitance change that can be detected to reflect the acceleration.

Fig. 3.1(a) shows the simplified diagram of a fully-differential MEMS capacitive accelerometer that consists of two proof- masses and two electrodes. The proof-masses are anchored to the substrate via the suspension beams, and their displacement *x* under the acceleration *a* can be expressed as

$$\frac{dx}{da} = \frac{m}{k_m} = \frac{1}{\omega^2} \tag{3.1}$$

where m represents the proof-mass and k_m is the spring constant of the suspension beam. ω is the fundamental frequency of this mechanical system, which determines the bandwidth of the MEMS sensing element. The proof-mass displacement causes the capacitance change of C_1 and C_2 between itself and two neighbored electrode plates, as shown in Fig. 3.1(b). The C_1 and C_2 values are expressed as follows:

$$C_1 = \frac{\varepsilon A}{g_0 - x} \qquad C_2 = \frac{\varepsilon A}{g_0 + x} \tag{3.2}$$

In the equations, ε, A and g_0 stand for permittivity, the area of parallel-plates, and the initial gap distance between the centered proof-mass and the electrodes. Taking C_1 as an example, its capacitance sensitivity to the displacement can be then derived as

$$\frac{dC_1}{dx} = \frac{\varepsilon A}{(g_0 - x)^2} \tag{3.3}$$

Combining (3.1) and (3.3) we have the MEMS capacitance sensitivity to the acceleration as

$$\frac{dC_1}{da} = \frac{dC_1}{dx}\frac{dx}{da} = \frac{m\varepsilon A}{k_m(g_0 - x)^2} \tag{3.4}$$

To maintain a good linearity on sensing the accelerations, the MEMS is usually designed with a large mechanical stiffness k_m to make proof-mass displacement $x << g_0$, and both C_1 and C_2 will have constant sensitivities within the accelerometer measurement range:

$$\frac{dC_1}{da} = \frac{dC_2}{da} = \frac{m\varepsilon A}{k_m {g_0}^2} \tag{3.5}$$

The fully differential MEMS structure shown in Fig. 3.1(b) produces two pairs of C_1 and C_2 with the opposite sensitivity for accelerations. They are configured as a capacitive Wheatstone bridge that has 2× MEMS sensitivity than a single-ended sensing element, and possesses much better common-mode rejection to noise, offset, etc.

3.2.2 Motivation for High-Voltage MEMS Biasing

To convert the MEMS sensitivity (capacitance change) to a more convenient readout, the MEMS is usually biased with a voltage V_B so it can produce electrical signals that reflects the incoming accelerations. Fig.2(a) shows a conventional MEMS capacitive accelerometer with V_B being applied across the electrode side (EL1, EL2), and the voltage signal V_{IN} being read out from the proof-masses (PM1, PM2). The output sensitivity of the Wheatstone bridge is defined by

$$\frac{dV_{IN}}{dC} = \frac{V_B}{C_d + C_{par}} \tag{3.6}$$

where $C_d = \varepsilon A/g_0$ is the static capacitance of C_1 and C_2 without any accelerations, and C_{par} is the parasitic capacitance between the proof-mass and substrate. Combining (3.5) and (3.6) we have the MEMS sensitivity in the electrical domain:

$$\frac{dV_{IN}}{da} = \frac{dV_{IN}}{dC}\frac{dC}{da} = \frac{m\varepsilon A}{k_m {g_0}^2 (C_d + C_{par})} \tag{3.7}$$

All the right terms in (3.7) are constant, indicating a linear transformation from input accelerations to the voltage signals produced by the MEMS. However, the linearity largely depends on the assumption we made in (3.5) that the MEMS displacement is negligible compared to the gap distance, indicating small MEMS signal amplitude from μV to mV levels. The small signal needs to be conditioned and amplified by the analog front-end (AFE) before it can be utilized

by other circuits (e.g., analog-to-digital converters). While amplifying the MEMS signals, the AFE circuit also induces electrical noise that adds up to the mechanical noise (known as Brownian noise [57]) originated from the MEMS. In order to maintain a good signal-to-noise ratio (SNR), or the resolution of acceleration measurement, excessive designs are needed to balance the electrical/mechanical noise and achieve an overall low-noise for the accelerometer.

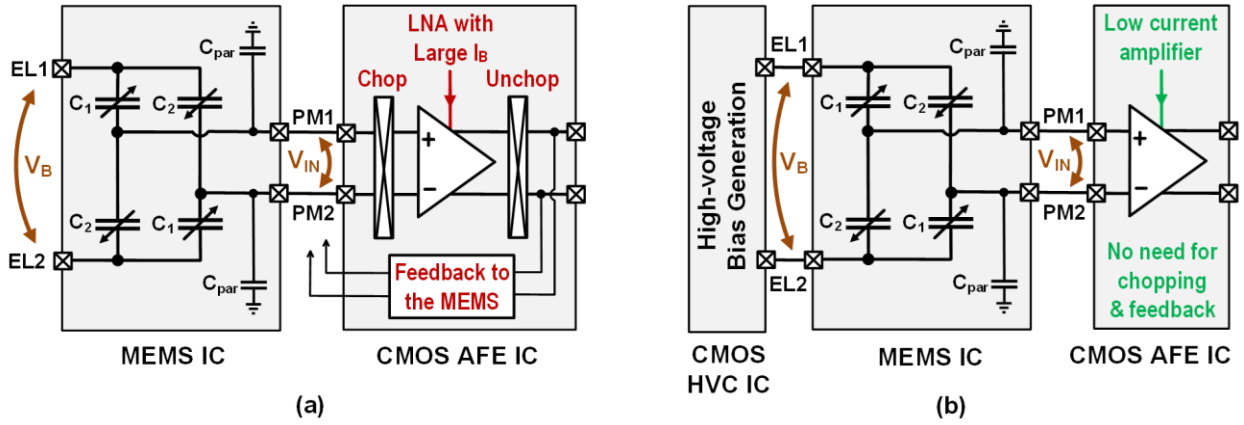


Figure 3.2: (a) The conventional scheme to readout sensing signals from MEMS capacitive accelerometer; (b) the proposed high-voltage biasing scheme that increases the MEMS signal and relaxes the AFE noise requirement for low power operation.

Fig. 3.2(a) shows a conventional scheme for the MEMS capacitive accelerometer, with several AFE techniques implemented in prior works to improve SNR. First, low noise amplifier (LNA) with large bias current is necessary in high-resolution accelerometer designs to suppress the in-band thermal noise from transistors and other circuit components. Second, signal-chopping is utilized either at the MEMS bias node or at the amplifier input to reduce the flicker noise that dominates in low frequency domains. The MEMS signal is chopped with a higher frequency than that of the input acceleration, and it is later unchopped to be recovered after the AFE circuit. Third, it can further increase the MEMS sen- sitivity to ng levels by monitoring the AFE circuit output, and using it for feedback controls on the proof-mass displacement.

However, all the above techniques require extra power, so there is a strong trade-off between the accelerometer power and resolution, which is consistent with the fundamental trade-

off between the AFE noise and power. In power-constrained applications such as IoT, it still remains challenging for MEMS capacitive accelerometers to achieve a sub-mg sensitivity with μW-level power consumption.

To overcome this power-noise dilemma, we propose to increase the MEMS signal rather than reducing noise to equivalently improve SNR. From (7) we know that the MEMS sensitivity is related to two factors: 1) the capacitance sensitivity to accelerations, and 2) the bias voltage being applied on the MEMS. The capacitance sensitivity, as we explained, is related to the Brownian noise and linearity of the MEMS design, and thus difficult to improve. Meanwhile, using higher bias voltages turns out to be a better solution because it can increase the MEMS signal proportionally without changing the MEMS specifications. Fig. 3.2(b) shows the proposed high-voltage biasing scheme for the MEMS capacitive accelerometer. By applying a significantly higher (e.g., 10× compared to the conventional scheme) bias voltage, the MEMS signal is raised way above the AFE circuit's noise floor. This eliminates the need for power hungry LNAs and signal chopping to suppress thermal noise and flicker noise, respectively, and we can design the AFE circuit with a nA-level supply current while still maintaining a good SNR.

Compared to the conventional scheme, the high-voltage biased MEMS accelerometer no longer possesses the trade-off between its AFE power and noise. Instead, its power-resolution performance is determined by what voltage levels can be applied to the MEMS at a given power budget. Section III introduces our design on the high-voltage-companion (HVC) chip that generates >10x higher DC-bias than the supply voltage, and only consumes nW-level active power. But before diving into the circuit details, in this chapter we would like to first explain the impact of electrostatic feedback, which determines the upper limit of the MEMS bias voltage in a more fundamental way.

3.2.3 Electrostatic Feedback of the High-Voltage Biasing

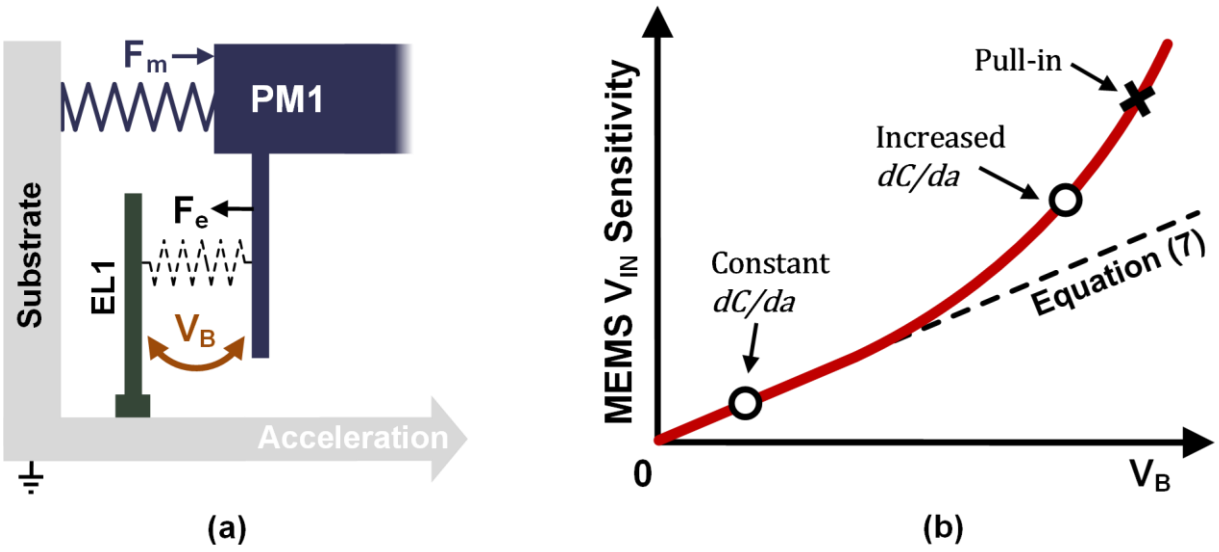


Figure 3.3: (a) Stress analysis of the proof mass when considering both mechanical force F_m and electrostatic force F_e; (b) with a fixed acceleration, the change of MEMS signal V_{IN} with increasing bias voltage V_B.

As discussed in the last subsection, one could achieve almost infinite signal gain by applying the highest possible voltage to the MEMS. However, the benefit of high-voltage bias is less straight-forward when considering the impact of bias voltage on the MEMS's mechanical movement. With the large voltage stress across the proof-mass and electrodes, it generates electrostatic force between them and results in an additional movement of the proof-mass. To quantitatively analyze the impact of the electrostatic force, we again take C_1 as an example to calculate the force between PM1 and EL1, as shown in Fig. 3.3(a). When a bias voltage V_B is applied across them, the total energy stored in C_1 is expressed by

$$E = C_1 {V_B}^2 \tag{3.8}$$

The electrostatic force Fe between PM1 and EL1 can be derived by

$$F_e = \frac{dU}{dx} = \frac{dC_1}{dx} {V_B}^2 = \frac{\varepsilon A {V_B}^2}{(g_0 - x)^2} \tag{3.9}$$

Note that F_e increases nonlinearly with the proof-mass displacement, and it is always a destabilizing (positive feedback) force that fights against the mechanical recovery force F_m by the MEMS suspension beam. In a stable MEMS system, F_e always needs to stay lower than F_m, or the electrostatic force will keep moving the proof-mass towards the electrode and eventually result in an electrostatic pull-in [58]. Taking the expression of F_m and F_e we have

$$k_m(g_0 - x) > \frac{\varepsilon A {V_B}^2}{(g_0 - x)^2} \tag{3.10}$$

or

$$V_B < \sqrt{\frac{k_m(g_0 - x)^3}{\varepsilon A}} \tag{3.11}$$

Equations (3.10) and (3.11) reveal an important trade-off between the MEMS bias voltage and the proof-mass displacement range. With a larger V_B applied to the MEMS, its proof-mass displacement needs to be constrained smaller to maintain $F_m > F_e$ and avoid pull-in. When V_B exceeds $k_m g_0^3/\varepsilon A$, the MEMS proof-mass will destabilize and pull-in even without any displacement (acceleration) applied, so it implies a theoretically maximum V_B that can be used to bias the MEMS. In Section 3.5 we show more results supporting this trade-off between V_B and the MEMS full-scale (measurement range).

Another angle of understanding the impact of V_B is through the change in the capacitance sensitivity of the MEMS that we derived in Equation (3.4). Intuitively, if the proof mass initially moves a distance x_1 with input acceleration, it becomes closer to the electrode and experiences a

greater attraction force from it. This will further move the proof mass with an additional distance x_2 so its overall displacement becomes $x_1 + x_2$ under the same acceleration. The proof mass behaves as it has a 'reduced stiffness' from the suspension beam, so we rewrite Equation (4) into

$$\frac{dC_1}{da} = \frac{m\varepsilon A}{(k_m + k_e)(g_0 - x)^2} \tag{3.12}$$

where k_m and k_e represent the mechanical stiffness (by suspension beams) and electrostatic stiffness (by high-voltage bias VB), respectively, and their value are express by

$$k_m = \frac{ma}{x} \qquad k_m = -\frac{2\varepsilon A {V_B}^2}{(g_0 - x)^3} \tag{3.13}$$

With a larger V_B, the MEMS's overall stiffness ($k_m + k_e$) becomes less, resulting in a higher capacitance sensitivity to acceleration. This further transfers into a non-linear increase in the MEMS signal V_{IN} at given accelerations shown in Fig. 3.3(b). When V_B is small, the electrostatic feedback is negligible and V_{IN} increases linearly with V_B, as described in equation (3.7). When V_B gets large and generates enough strong electrostatic force to the proof mass, a super-linear increase in V_{IN} will occur. While it brings extra benefits to the accelerometer's SNR, we should be aware of cost associated with the MEMS full-scale reduction and the risk of pull-in. This electromechanical trade-off is rarely utilized in prior works, and we will show our approach in the next subsections on how to generate the proper high voltage bias, and achieve an optimized accelerometer performance for different conditions.

3.2.4 Electrostatic Mismatch Compensation

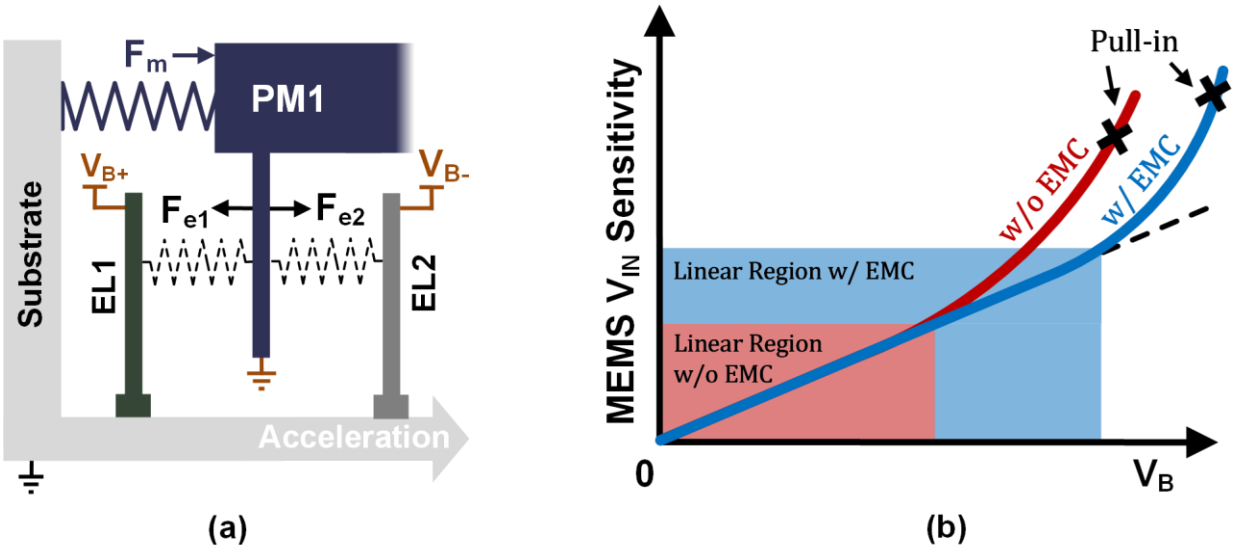


Figure 3.4: (a) The stress analysis of the proof mass in a differential MEMS structure; (b) the change in MEMS sensitivity with bias voltages for systems with/without electrostatic mismatch compensation (EMC).

To take advantage of the high-voltage bias while mitigating its side effect due to electrostatic feedback, we utilize the MEMS's differential structure and apply balanced +/- voltage on the two electrodes neighboring a proof mass. As shown in Fig. 3.4(a), EL1 is biased with a positive high-voltage V_{B+} while EL2 biased with a negative voltage $V_{B-} = -V_{B+}$. When PM1 is DC coupled to ground / substrate, it will experience equal electrostatic forces F_{e1} and F_{e2} from EL1 and EL2, respectively, but in opposite directions, so they are canceled. Then PM1 will no longer suffers from electrostatic feedback regardless of the value of V_{B+} and V_{B-}.

However, maintaining a balanced electrostatic force on PM1/PM2 is tricky in practical applications, and electrostatic feedback still exists due to electrostatic mismatch, defined as $F_{mis} = F_{e1} + F_{e2}$. There are two reasons for a non-zero electrostatic mismatch:

1. During MEMS fabrication, process variation can cause mismatch in the MEMS'S mechanical parameters (e.g., area A or gap distance g_0 in equation (3.9)). Circuit non-idealities also induced electrical mismatch, such as voltage errors and ripples, making it difficult to generate an exactly equalized V_{B+} and V_{B-}.

2. The value of Fe1 and Fe2 diverged with input acceleration, regardless of their equilibrium condition in the stationary state. With acceleration occurred, F_{mis} can be written as

$$F_{mis} = F_{e1} + F_{e2} = \frac{\varepsilon A {V_{B+}}^2}{(g_0 - x)^2} - \frac{\varepsilon A {V_{B-}}^2}{(g_0 + x)^2} \tag{3.14}$$

which is simplified as

$$F_{mis} = \varepsilon A {V_B}^2 \frac{4 g_0 x}{({g_0}^2 - x^2)^2} \tag{3.15}$$

When $x_2 << g_0^2$, F_{mis} increases proportionally with the proof-mass displacement. But if x grows large enough under strong accelerations, the increase of F_{mis} becomes dramatic and eventually converges into the single-ended electrostatic force described in (9).

For both reasons listed above, the electrostatic mismatch is exacerbated quadratically with the V_B increase, and thus need to be carefully considered in the high-voltage bias scheme for MEMS capacitive accelerometers. This chapter presents a technique called Electrostatic Mismatch Compensation (EMC) that strategically manipulates the bias voltages to improve the challenges raised by F_{mis}. The EMC technique has two goals:

1. Extending the linear region of MEMS sensitivity to higher V_B levels. As we discussed earlier, the electrostatic mismatch due to MEMS process variation and circuit nonideality becomes more obvious with larger V_B. To compensate for the mismatch, EMC directly equalizes F_{e1} and F_{e2} by inducing an intended voltage skew ΔV_B between V_{B+} and V_{B-}, and maintaining ultra-low voltage errors and ripples for ΔV_B. As a result, the sensitivity of the MEMS stays linear until a higher

V_B threshold, as shown in the blue curve in Fig. 3.4(b), and it guarantees a wider region of clean bias without electrostatic feedback on the MEMS.

2. Optimizing the trade-off between MEMS sensitivity and full-scale. At very large V_B, non-linearity appears in the MEMS sensitivity, and electrostatic mismatch is mainly caused by the proof-mass displacement (input acceleration). It is beneficial to get a higher MEMS sensitivity at the cost of losing its dynamic range, but the process must be properly controlled to guarantee the MEMS linearity to accelerations and avoid pull-in. EMC achieves this by carefully choosing the value of V_{B+} and V_{B-} so that sufficient dynamic range is met, and the pull-in point is pushed into a higher bias voltage. EMC also determines the safe margin on the bias voltages when considering the variation across MEMS chips/wafers.

As a summary, EMC aims to guarantee a more stable, predictable, and variation-robust MEMS operation when we utilize the high-voltage bias for better accelerometer SNR. The realization of EMC is through the high-voltage companion Chip that we demonstrate in Section 3.5.

3.3 Implementation of the High-Voltage Companion (HVC) Chip

3.3.1 High-Precision Bias Voltage Generation for EMC

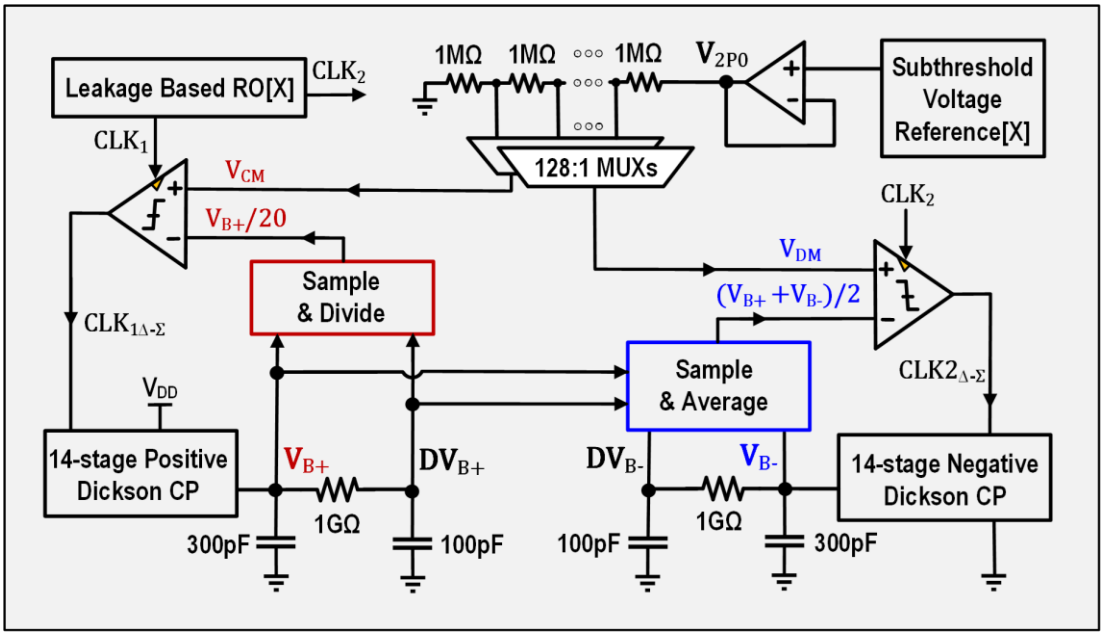


Figure 3.5: Top level diagram of the HVC chip.

The EMC technique relies on generating precisely controlled V_{B+} and V_{B-} with proper values to compensate for the MEMS process variation and CMOS circuit non-ideality. In this work, the high-voltage biases are up-converted from V_{DD} using Dickson charge pumps [59] for the large conversion ratio, chip integration, and high efficiency with low load current (V_{B+} and V_{B-} are DC voltages, and EL1/EL2 are purely capacitive).

Fig. 3.5 shows the positive and negative charge pumps on the HVC chip to generate V_{B+} and V_{B-}, respectively. The charge pump outputs are sampled and compared with the +/- reference voltages, and the comparison results modulate the charge pumps' operation in a delta-sigma manner to form a close-loop control on the bias voltages. In addition, V_{B+} and V_{B-} are in the range of 20-30V, so they must be divided before they can be compared with the reference voltages on the chip (0-2V). However, any voltage errors from the reference are amplified by the large division ratio (e.g., 20×) when they appear in the bias voltages. For example, the programmable reference voltages are multiplexed from a resistive voltage divider that divides 2V with 128 poly-resistors,

and the quantization error is 2V/128 ≈ 15mV. The resulting error on V_{B+} and V_{B-} will then become 15mV×20 = 300mV, making it difficult to achieve EMC with the required voltage precision.

To address this challenge, we only do voltage sampling and division (20×) for V_{B+} to control the positive charge pump. For V_{B-} we sample its arithmetic mean with V_{B+} and directly compare the mean value with the other reference voltage to determine the negative charge pump operation. As result, V_{B-} will follow the change of V_{B+} while keeping a programmable voltage skew $\Delta V_B = (V_{B+} + V_{B-})$ that is determined by the second comparison. In the other words, we refactor the bias voltages into a "common-mode" part and a "differential-mode" part:

$$V_{B+} = 20V_{CM} \tag{3.16}$$

$$V_{B-} = -20V_{CM} + 2V_{DM} \tag{3.17}$$

where V_{CM} and V_{DM} is the reference voltages that are used by the comparison for positive charge pump and negative charge pump, respectively. While the voltage error of V_{CM} is multiplied by 20 on both V_{B+} and V_{B-}, the V_{DM} error only has a 2× effect on $(V_{B+} + V_{B-})$. This greatly benefits EMC because when we re-write equation (14) with the condition $x << g_0$ (which is true within our accelerometer's measurement range), we have

$$F_{mis} = \frac{\varepsilon A(V_{B+} + V_{B-})(V_{B+} - V_{B-})}{{g_0}^2} \tag{3.18}$$

which shows that F_{mis} reduced proportionally with $\Delta V_B = (V_{B+} + V_{B-})$. Beside the quantitation errors that are improved with above technique, V_{B+} and V_{B-} may also suffer from the noise and fluctuation from the supply voltage if V_{CM} and V_{DM} are directly generated from V_{DD}. On the HVC chip, we instead implement the voltage to be divided with a subthreshold voltage reference [60]

that has a -41dB power supply rejection and a <1% error across 0°C - 100°C. Because the subthreshold voltage reference has a large current variation across temperatures, we buffer its output voltage before applying it to the voltage divider to guarantee a sufficient current that flows through the poly-resistors and generates precise V_{CM} and V_{DM}.

3.3.2 High Voltage Sampling Circuits for V_{B+} and V_{B-}

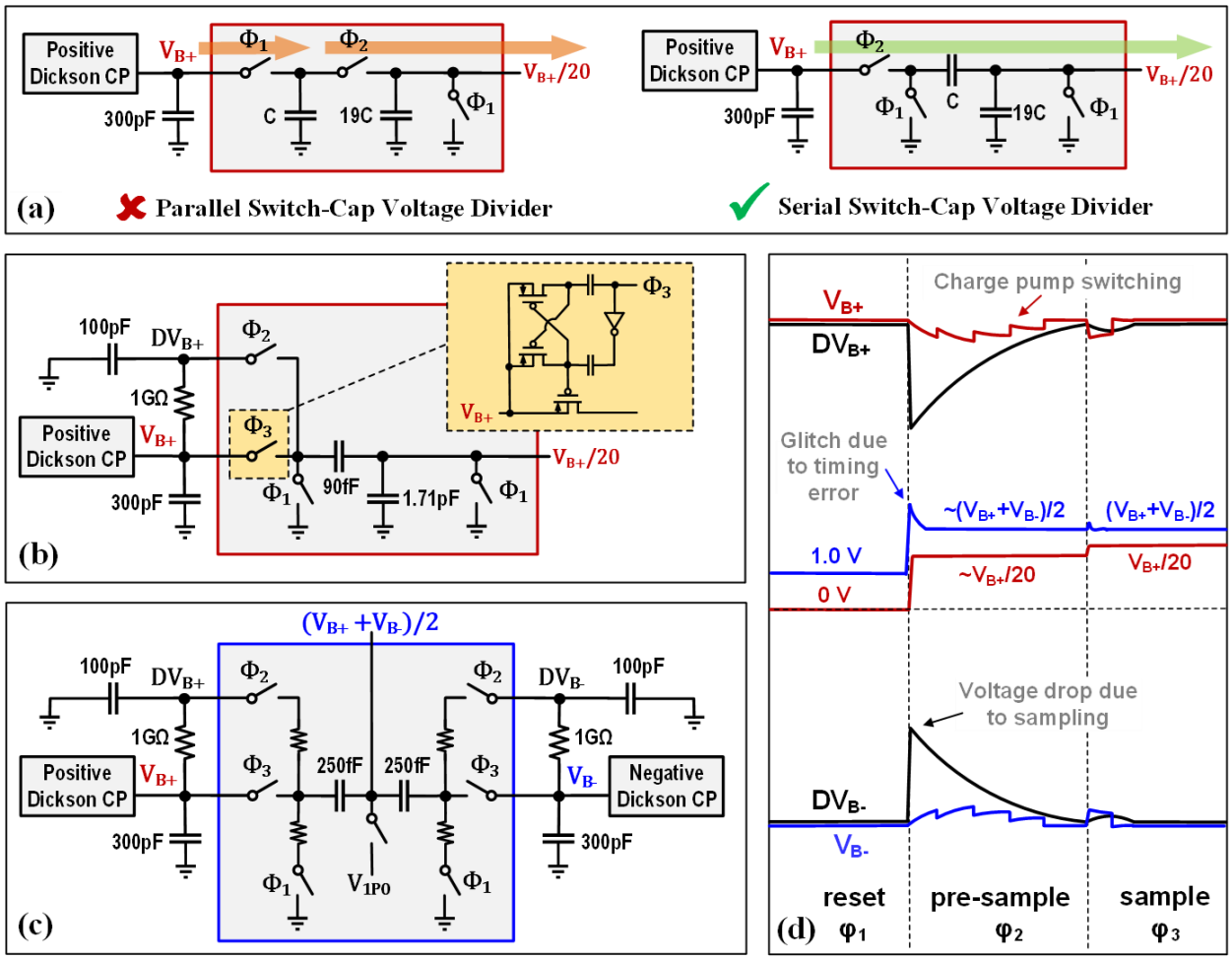


Figure 3.6: (a) Comparison between the voltage divider of parallel / serial switched capacitors, showing that the serial structure has a better AC path only controlled by Φ_2; (b) implementation of the V_{B+} sampling and division circuit, with a separated dirty V_{B+} to pre-charge the sampling nodes and reduce V_{B+} ripples; (c) implementation of the V_{B+} and V_{B-} average circuit and (d) conceptual waveform showing transient voltages (b) and (c).

Several circuit challenges are raised with sampling/dividing the high-voltage V_{B+} and V_{B-}. First, the switched-capacitor voltage divider induces a switching loss approximately equal to

$0.5fCV^2$, where f is as the sampling frequency, C as the sampling capacitance and V as the voltage swing. For the sufficiently fast charge pump feedback control required by EMC (e.g., f = 1000Hz, C = 100f F and V = 30V), the resulting power loss on V_{B+} and V_{B-} are in 100nW levels, and it takes even more power consumption from V_{DD} to replenish the bias voltage losses. To mitigate the power overhead due to frequently sampling/dividing the high-voltage nodes, we implement a serial-connected switched-capacitor voltage converter shown at the right part in Fig. 3.6(a). Unlike its parallel counterpart at the left, the serial switched-capacitor divider does not rely on the alternative Φ_1 and Φ_2 to update its output voltage ($V_{B+}/20$). Instead, its AC signal division is only related to Φ_2, so we can highly duty-cycle Φ_2 to keep it on and update $V_{B+}/20$ with any ripples and variations occurred at V_{B+}. Meanwhile, for Φ_1 we only turn it on once after a long time (e.g., seconds) so the sampling frequency will be in sub-Hz range, significantly saving the power.

A second challenge manifests itself when the storage capacitor (300pF) charge shares with the sampling capacitor, resulting in ripples on V_{B+} and V_{B-}. Although a large capacitor ratio is guaranteed, the ripples can be in 100mV levels due to the high-voltage scales of V_{B+} and V_{B-}, causing an unpredictable, transient F_{mis} to the MEMS and increasing the common-mode noise seen by the AFE circuits. To address this issue, we separate V_{B+} and V_{B-} from another two 'dirty' nodes, DV_{B+} and DV_{B-}, each through a large RC constant (τ = 1GΩ×100pF = 0.1s). During voltage sampling, DV_{B+} and DV_{B-} will first pre-charge the sampling capacitors to near V_{B+} and V_{B-} so that the ripples occur on the dirty nodes instead of the actual MEMS bias voltages. The dirty nodes' voltage loss will later be replenished by the charge pump, but through the large RC network. As a result, V_{B+} and V_{B-} only see charge pump ripples rather than the much larger sampling ripples.

Fig. 3.6(b) and (c) shows the final implementation of the high-voltage sampling and division/average circuits, while Fig. 3.6(d) describes the transient waveform during voltage

sampling. The pulse width of Φ_1 and Φ_2 remains short compared to the sampling period, and Φ_3 stays high for most of the time to provide an AC throughput as we discussed above. Timing switches are implemented with high voltage transistors with their control signals level-shifted by the capacitive level shifters in [61], also mitigating control power with low sampling frequency. Furthermore, in the voltage average circuit in Fig. 3.6(c), we include current-limiting resistors to reduce voltage spikes on $(V_{B+} + V_{B-})/2$ due to the timing difference of the V_{B+} and V_{B-} switches, and prevent the spike from damaging the comparator circuit.

3.3.3 Electrostatic Pull-In Detection and Protection

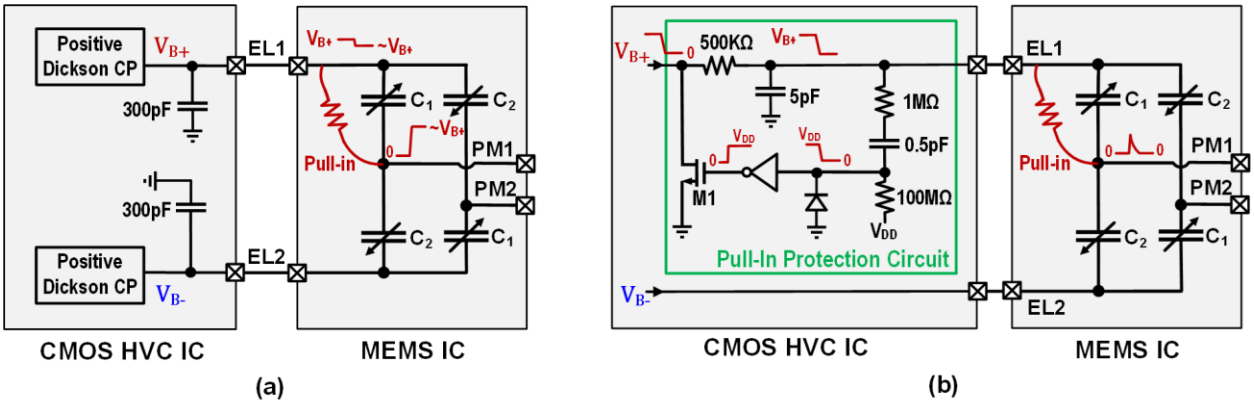


Figure 3.7: (a) Without the protection circuit, pull-in results in high-voltage stress in PM1 that can damage the AFE circuit; (b) with pull-in protection, the voltage drop in EL1 will ground V_{B+} and prevent damage to the AFE chip.

When EMC optimizes the trade-off between MEMS sensitivity and full-scale, it applies the highest V_{B+} and V_{B-} with a safe margin for input accelerations and MEMS process variation. However, it is still possible during the operation/calibration phase that an improper bias voltage is applied and triggers an electrostatic pull-in for the MEMS. While the pull-in is mechanically recoverable for the MEMS chip, it raises issues for the AFE chip because of the electrical contact between the proof-mass and electrode. As shown in Fig. 3.7(a), when PM1 pulls-in with EL1, the large storage capacitor at EL1 will charge PM1 to near V_{B+}. Since PM1 is connected to the

amplifier input on the CMOS AFE chip, the high- voltage may cause the breakdown of transistor's gate-oxide and permanently damage the AFE circuit.

To prevent this, we implement a pull-in detection and protection circuit on the HVC chip, as shown in Fig. 3.7(b). We first connect a smaller (5pF) capacitor to V_{B+} so that when PM1 pulls-in with EL1, the voltage drop at EL1 will be large and sufficient to be detected. The EL1 voltage drop is AC-coupled with a high-pass filter (0.5pF and 100MΩ) to generate a reset signal that ground V_{B+} via transistor M1. By controlling the bandwidth of this feedback, it can detect and ground V_{B+} before it generates a high-enough voltage spike that can damage the AFE circuit. After V_{B+} being grounded to 0, the electrostatic force between PM1 and EL1 disappears, and PM1 is recentered by the suspension beam. Meanwhile, in the pull-in protection circuit, V_{DD} will recharge the 0.5pF capacitor through the DC path (100MΩ), and the reset signal is retracted to enable V_{B+} rebuild its voltage.

3.4 Implementation of the MEMS and CMOS Analog Front End Chip

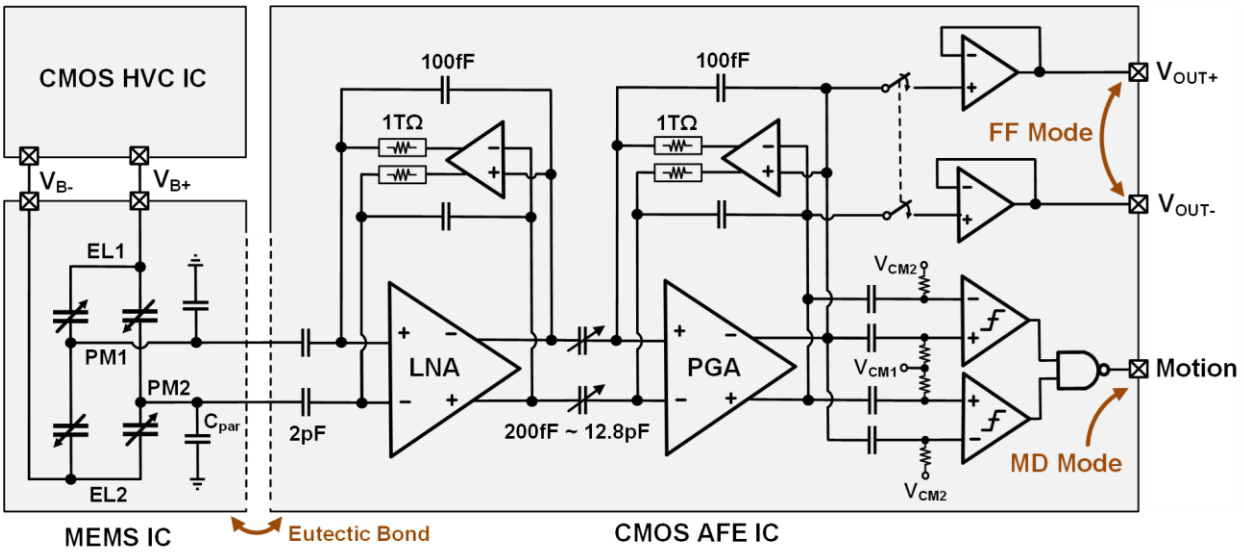


Figure 3.8: Top-level diagram showing the MEMS + CMOS AFE chip.

The HVC chip generates a proper pair of V_{B+} and V_{B-} with EMC and apply the bias voltages to the MEMS electrodes EL1 and EL2, respectively. When acceleration comes in, a differential MEMS signal V_{IN} is generated across PM1 and PM2 due to the MEMS capacitance change, and the signal is amplified by the CMOS AFE chip. Equation (3.7) shows that the MEMS signal declines with the proof-mass parasitic capacitance C_{par}, so to reduce C_{par} due to the MEMS-CMOS interconnect, we eutectically bond the MEMS and CMOS AFE circuit at the wafer level and then dice the wafer into 2-layer face-to-faced bonded MEMS-CMOS chips.

On the CMOS AFE chip, we adopt a 2-stage capacitive coupled amplifier design consisting of a low-noise amplifier (LNA) followed by a programmable-gain amplifier (PGA) as shown in Fig. 3.8. The LNA and PGA design is similar to [62] with auxiliary amplifiers to shift their output DC-levels to the input for maximized dynamic range. The detailed schematic of the LNA / PGA / auxiliary amplifier can be found in Fig. 3.9, and we generate tunable amplifier bias voltages (V_{BP1-3}) on chip to cover the temperature range of -40°C to 80°C and possible process variations. Both LNA and PGA consume nW-levels power, but their noise floor is far below the significantly increased MEMS signals, so a high SNR is achieved. The LNA input pair size is enlarged (W/L = 187µm/0.42µm), trading off the available chip area with a lower flicker noise.

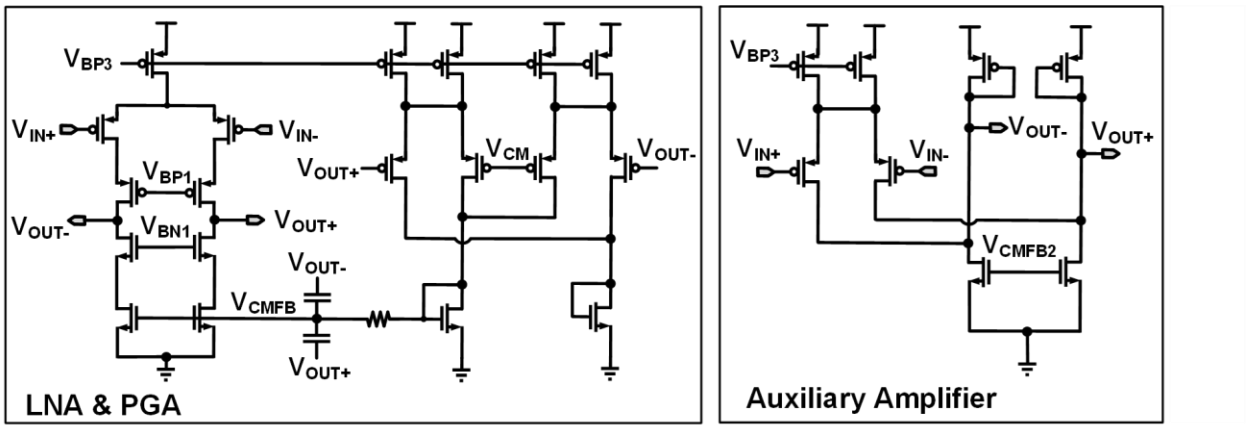


Figure 3.9: Schematic of LNA/PGA and the auxiliary amplifier shown in Fig. 3.8.

The system has two operating modes. In the full-function (FF) mode, the AFE circuit generates a rail-to-rail analog voltage output that covers a 1.5g measurement range for accelerations. In the absence of acceleration, we can switch to an ultra-low-power motion detection (MD) mode to only output a 1-bit signal when there is an acceleration exceeding our detection threshold. During the MD mode, V_{DD} is reduced from 2V to 1.2V, and the amplifier bias current is further reduced to sub-nA to save circuit power.

A main challenge for the AFE chip is its bandwidth design. Although the AFE low-pass corner is defined by the PGA bandwidth and can be directly modulated with the PGA bias current, its high-pass corner design remains difficult to implement. With the DC bias voltages V_{B+} and V_{B-}, the MEMS capacitor bridge can only sense the change of accelerations and produce AC signals. While it is acceptable for motion detection applications, this also means that the AFE circuit needs to define the high-pass corner with the amplifiers' feedback RC networks. With a feedback capacitor of 100fF for low-power operation, the resistance needs to be in Tera-Ohm levels to guarantee a low enough high-pass corner. We first implemented a 1TΩ feedback resistor with the pseudo-resistor [63], achieving a near-Hz high-pass corner. To detect very slow motions and reduce frequency variation from pseudo-resistors, we implemented a second version AFE that utilizes a sample- and-average-feedback resistor (SAFR, proposed in [64]) for a 100TΩ equivalent resistance, and pushed the AFE high-pass corner to sub-Hz.

3.5 Measurement Results and Analysis

3.5.1 Accelerometer Performance Measurements

We fabricate the HVC chip in a 180nm HVBCD process and the AFE chip in a 180nm MEMS-compatible process. Fig. 3.10 (a) and (b) show the die photo for the two ICs. The AFE chip is post-processed and eutectically bonded with the MEMS chip provided by InvenSense, Inc.

To test the fabricated accelerometer system, we mount the PCB with chip packages to a shaker table that gives acceleration excitations in three different angles, covering the X, Y and Z axis. We perform a test for all three axes, but only showing the Z-axis results in this thesis for simplicity.

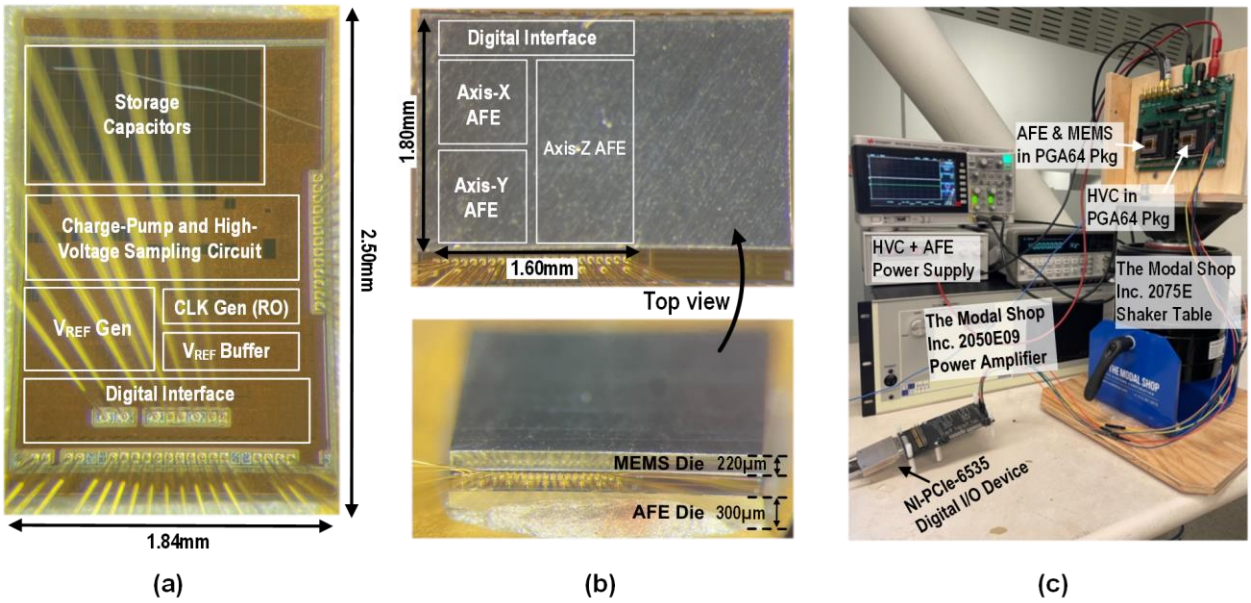


Figure 3.10: (a) HVC die photo; (b) CMOS die photo and the eutectically bonded MEMS-CMOS die; (c) testing setup for the accelerometer measurement.

Fig. 3.11 shows the measured transient waveform of the HVC output and the AFE output in both FF and MD modes. During cold start-up, HVC gradually builds up V_{B+} and V_{B-} while always maintaining a constant voltage skew ΔV_B = 1.2V for EMC. The ripples on ΔV_B is constrained within mV (0.1%) in steady state. In FF mode, the AFE output increases with the bias voltages as indicated in (3.7), and stabilizes with a 56dB signal-to-noise-and-distortion-ratio (SNDR) at V_{B+}=23.9V and V_{B-}=-22.7V. With the same bias condition, the AFE circuit can detect accelerations down to 3mg in MD mode, producing a one-bit detection signal at the output.

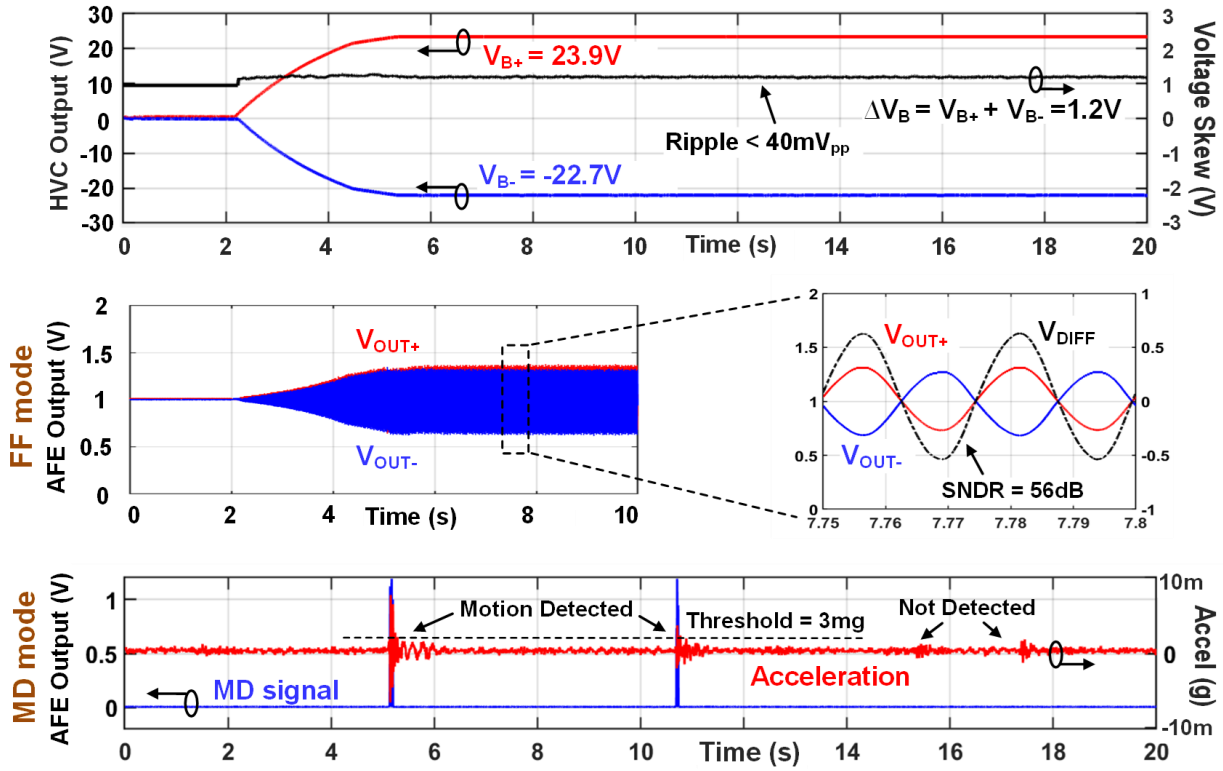


Figure 3.11: Measured transient waveform showing the HVC bias voltage generation from cold start, and the AFE output voltage in both FF and MD mode.

An important question is how to determine the value of V_{B+} and V_{B-} to achieve maximum signal increase while maintaining sufficient MEMS dynamic range. Since EMC is especially critical in the high-voltage domains, we measured a typical accelerometer sample and plot its sensitivity with all combinations of V_{B+} and V_{B-} that are larger than 20V, as shown in Fig. 3.12(a). While significantly unbalanced V_{B+}/V_{B-} results in MEMS pull-in due to the large electrostatic force mismatch, equal-valued V_{B+}/V_{B-} also fails to produce optimized sensitivity due to MEMS asymmetry and process variation. An optimal ΔV_B = 1.2V is observed for the highest accessible sensitivity for this chip sample. By keeping the 1.2V voltage skew, we plot the accelerometer sensitivity increase with V_{B+}/V_{B-} from 0V to 25V in Fig. 3.12(b). Similarly to Fig. 3.4(b), the accelerometer sensitivity first increases linearly with small bias and then becomes super-linear above 15V, finally pulling-in at around 25V. The MEMS has zero measurement range at the pull-

in point, so EMC backs off a few steps to V_{B+} = 23.9V and V_{B-} = -22.7V and maintains a >>20g proof- mass dynamic range. The proposed accelerometer gains a >40× higher sensitivity from its high-voltage biasing (with EMC), compared to biasing with the supply voltage in the conventional accelerometer scheme.

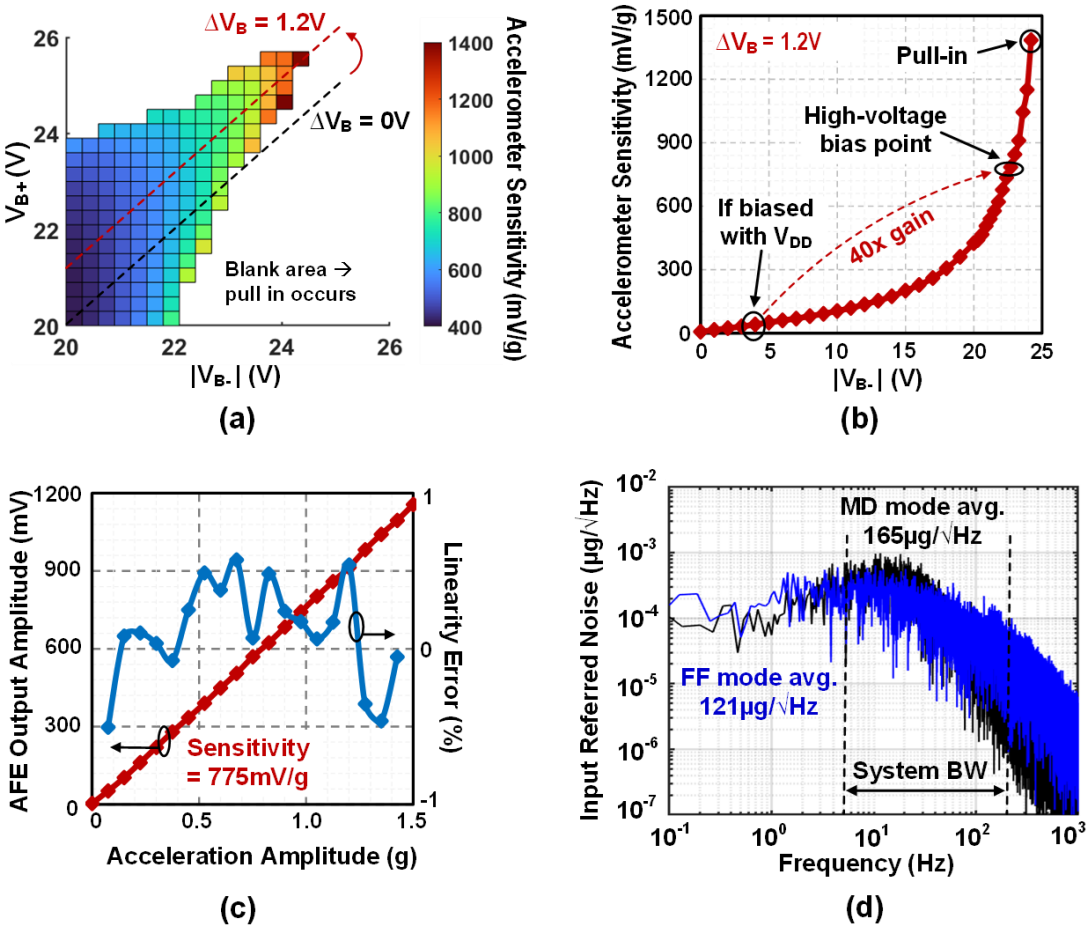


Figure 3.12: Measured results for (a) the accelerometer sensitivity with >20V V_{B+} and V_{B-}, showing an optimal 1.2V voltage skew; (b) the accelerometer sensitivity from 0-25V bias maintaining a 1.2V skew; (c) linearity of accelerometer output within the 1.5g full-scale; (d) the accelerometer input-referred noise (determines its resolution) in FF and MD mode.

With the EMC designated bias voltages, the MEMS proof mass has a significantly larger dynamic range than the accelerometer's full-scale (±1.5g defined by the AFE chip), thus guaranteeing good output linearity given by Equation (3.5). Fig. 3.12(c) demonstrate the accelerometer output voltage versus input accelerations, showing a 775mV/g sensitivity and a <1%

linearity error. Taking advantages of the large MEMS signal, the accelerometer achieves 121µg/ √ Hz and 165µg/ √ Hz input-referred noise floors for FF and MD modes (Fig. 3.12(d)) while only consuming 110nW and 22.4nW by the AFE chip.

It should be noted that the MEMS mechanical noise for this work is negligible in ng/ √ Hz range, and the overall accelerometer noise is dominated by the CMOS AFE circuit. More specifically, the low-frequency noise contributes most in the noise spectrum as shown in Fig. 3.12(d). Including the 223nW HVC power in generating the triaxial MEMS biases, the accelerometer system consumes a total of 184nW and 96nW per-axis in FF mode and MD mode, respectively. Table 3.1 summarizes and compares the performance of the proposed accelerometer with the prior art. Compared to prior arts, the proposed accelerometer with high-voltage biasing achieves a 11.7× improvement in FoM considering the power-noise product over bandwidth.

Publication	Process	Type	CMOS Area (mm^2)	# of Axis	MEMS-CMOS Integrated	Full Scale (g)	Bandwidth (Hz) [a]	Noise Floor ($\mu g/\sqrt{Hz}$)	Supply Voltage (V)	Power per Axis (μW)	FoM[c] (μW $\mu g/Hz$)
JSSC 2019 [3]	$0.5\mu m$	Capacitive	49.0	1	No	± 0.4	1 - 300	0.03	3.0	20000	34.6
JSSC 2015 [4]	$0.5\mu m$	Capacitive	7.80	1	No	± 1.2	300	0.2	7.0	23000	266
JSSC 2012 [6]	$0.35\mu m$	Capacitive	6.66	1	No	± 1.15	200	2	3.6	3600	509
JSSC 2017 [7]	$0.35\mu m$	Oscillation	6.00	1	No	± 20	40[b]	0.4	1.5	4370	276
VLSI 2018 [9]	$0.18\mu m$	Capacitive	1.14	1	No	± 8	50	970	1.0	0.181	24.8
ADXL-362 [10]	-	Capacitive	-	3	Yes	± 8	50	550	2.0	1.2	93.3
JSSC 2020 [8]	$0.13\mu m$(LV) $0.35\mu m$(HV)	Capacitive	17.6(LV) 26.0(HV)	1	No	± 0.55	400	0.022	1.4(LV) 12(HV)	17000	18.7
TCSI 2022[11]	$0.18\mu m$	Capacitive	1.65	1	No	± 12	2500	270	1.8	147	796
This work	$0.18\mu m$(LV) $0.18\mu m$(HV)	Capacitive	2.88(LV) 4.55(HV)	3	Yes	± 1.5	5 - 200	121[d]	2(LV) 2.4(HV)	0.184	1.59

[a] Some works are capable of sensing DC accelerations, but their noise floor is measured starting from a high-pass frequency similar to this work (5Hz).
[b] Estimated with the noise spectrum figure.
[c] A widely used FoM = power × noise floor ÷ $\sqrt{BW}$.
[d] FF mode result for a good comparison with prior works. In MD mode, the noise floor is $165\mu W/\sqrt{Hz}$ with 96nW power, achieving an FoM of 1.13.

Table 3.1: Performance Summary of the proposed MEMS accelerometer and comparison with prior works.

3.5.2 EMC measurement with process variation

The EMC optimized ΔV_B is 1.2V for the measured chip sample, but is it robust against MEMS process variation as the EMC promised? And how reliable is it to use high voltage biasing for mass-produced MEMS accelerometers in different batches? To answer these questions, we repeat the measurement process in Fig. 3.12(a) for 30 accelerometer samples from 5 different MEMS/CMOS wafers, and plot their optimal ΔV_B in Fig. 3.13(a). Ideally, it is best to use these ΔVBs individually for determining each chip's V_{B+} and V_{B-}, because it gives the optimal EMC and results in a higher accelerometer sensitivity (784mV/g) with sufficient MEMS dynamic range, as shown by red triangles in Fig. 3.13(b).

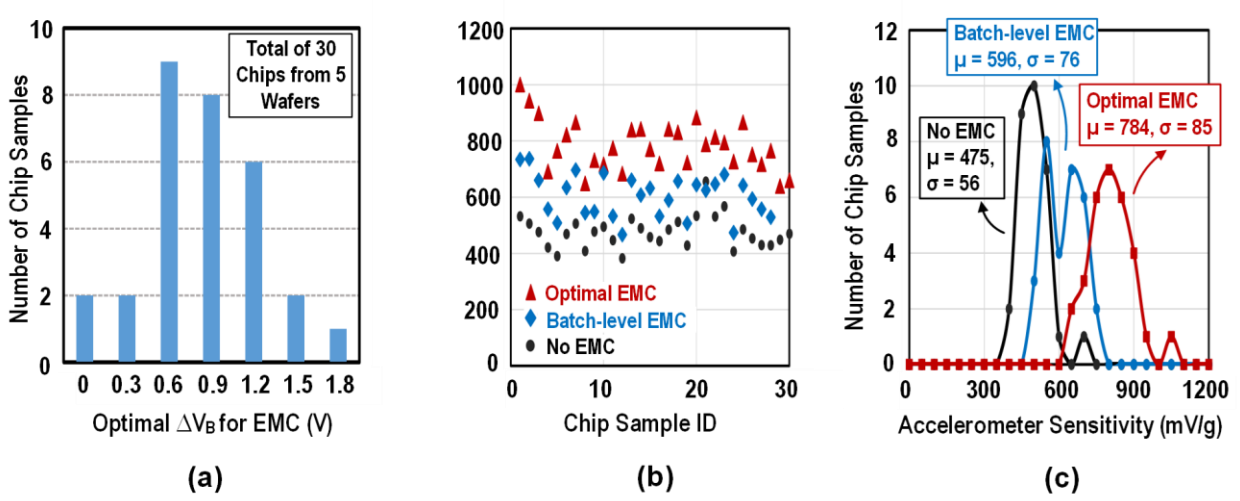


Figure 3.13: (a) Distribution of the optimal voltage skews ΔV_B (that achieves the highest bias voltage before pull-in) across 30 different MEMS/CMOS chips; (b) EMC designated accelerometer sensitivity for the 30 chip samples, with individually chosen ΔV_B (red triangle), wafer-average ΔV_B (blue diamond) and zero ΔV_B (black dot); (c) distribution of the results in (b).

Though each chip only needs a one-time calibration after fabrication, this may still increase the test cost in mass pro- duction. We also propose a 'batch level EMC' by measuring the subset of chips on the same wafer (in this test, 6 samples per wafer), and applied their average ΔV_B for all the chips on that wafer. The blue diamonds show the sensitivity of the accelerometer with this technique. Fig. 3.13(c) shows that the optimal (individual) EMC yields the highest mean sensitivity

of 784mV/g, a 1.65× increase over no EMC (simply applying $\Delta V_B = 0V$). Batch level EMC incurs a sensitivity penalty of 24% at 596mV/g from optimal EMC but remains 25% better than no EMC.

Finally, we perform a long-term, repeated pull-in test to characterize the accelerometer reliability in case of pull- ins due to large accelerations or improper MEMS bias. We intentionally trigger a pull-in with higher than normal V_{B+} and V_{B-}, and retract the bias voltages to recover from the pull-in. After >10000 pull-ins occur, we remeasure the accelerometer and it shows no performance degradation for both the MEMS structure and the AFE circuit, validating a safe operation with the use of high-voltage biases on the MEMS accelerometer

3.6 Conclusion

This chapter presents a triaxial MEMS capacitive accelerometer using high-voltage biasing to achieve high resolution with ultra-low power. The accelerometer consists of a MEMS sensing chip, an analog front-end chip, and a high voltage companion chip to generate the optimized bias voltage for the MEMS chip. By using the high-voltage bias, the MEMS signal is raised above the AFE noise floor, eliminating the power-hungry amplifier and signal-chopping in the conventional MEMS accelerometers. The high-voltage companion chip, while producing the programmable MEMS bias voltages, also compensates for the electrostatic mismatch raised by the high- voltage biases. The proposed accelerometer is fabricated and measured with a 121μg/ √ Hz input-referred noise floor and 184nW power (including bias generation), showing a 11.7× FoM improvement over prior arts.

Chapter 4 A High-Voltage Generator and Multiplexer for Electrostatic Actuation in Programmable Matter

4.1 Introduction

A key point to actuation in PM (and other micro-robotic applications) is the generation and control of high voltages (e.g., 100V) at the Catom surfaces (insulators). When different Catoms make surface contact, the difference in their surface potentials will create an electrostatic force, bonding them together (latching) or causing a rotation/movement (actuation). Prior on-chip high voltage generators [65] [66] [67] [68] [69] [70] [71] are capable of providing sufficient voltage levels for actuation, but their application is greatly limited due to the remaining challenges:

1. The high-voltage generation chip should be smaller than a few mm to be contained inside the Catom, ensuring that the whole Catom is light weight. This precludes the use of bulky off-chip components such as inductors and discrete capacitors, which are commonly used by boost converters [72] [73] [74] [75].
2. To allow different actuation patterns of a Catom, the high-voltage chip needs to support all 12 Catom surfaces with individual voltage control.
3. Given the small size of the Catom, energy resources (e.g., a tiny battery) are greatly limited inside the Catom. The high-voltage generation chip must consume sub-μW power to ensure system lifetime.
4. The Catom surface electrodes present only capacitive loads to the chip without DC current. Furthermore, the PM actuation frequency is low (less than 100Hz),

resulting in a low (nW level) reactive power. This makes it challenging to achieve high energy efficiency because the circuit power overhead (clock generation, switching loss, leakage) is not amortized over a large output current.

To address these challenges above, this chapter presents a new driving chip referred to as a High-voltage-generator-and- multiplexer (HVGM) [76] for Catom actuation and other capacitive MEMS actuators. The HVGM consists of a single pump with 12 novel high-voltage multiplexer circuits that enable individual control for each electrode output voltage, amortizing area and switching overhead/leakage. Furthermore, since the multiplexers can turn the electrodes off (0V) while keeping the pump active, we avoid discharge and recharge of flying pump capacitors, further saving significant energy. Implemented in a 70V process, we obtain a greater than 100V differential potential across an electrode pair with programmable voltage scale and slew rate at sub-µW power levels.

Moreover, we show a complete micro-system of stacked dies, measuring 3×1.4×1.1 mm, including the HVGM, a processor, radio, and harvester that achieves energy-autonomous operation, and can be integrated into a micro-robot "Catom" to realize PM. The first version of this micro-system has been fabricated and tested, while we are currently working on the second version, which is a complete system-on-chip design integrating all the functionalities on one chip.

The remainder of this chapter is organized as follows. Section 4.2 presents the Catom micro-controller design, which we show for the first time, emphasizing the actuation of the Catom and the single pump topology of the HVGM. Section 4.3 describes the implementation of HVGM in detail, including the design of high-voltage multiplexers for high voltages in positive and negative domains. Section 4.4 shows the measurement of the HVGM, with the current progress on the Catom integration and testing. Section 4.5 discusses HVGMv2, the next generation of the

Catom controller that only consists of one chip, and can support multiple functionalities covered by the Stack. Section 4.6 draws conclusions.

4.2 Programmable Matter with Electrostatic Actuation

4.2.1 Catom Design with Electrostatic Actuation

The building block for PM is a quasi-spherical module called a Catom, proposed in [18], that consists of 12 numbered square surfaces at contacts points of cells in a face-centered cubic lattice. These 12 surfaces are connected using hexagons and octagons to form a polyhedron as shown in Fig. 4.1(b). However, the angles between the surfaces are sharp and make it difficult to move/rotate, so the authors replaced hexagonal and octagonal planes with curved surfaces to obtain continuous surfaces as shown in Fig. 4.1 (c) and (d).

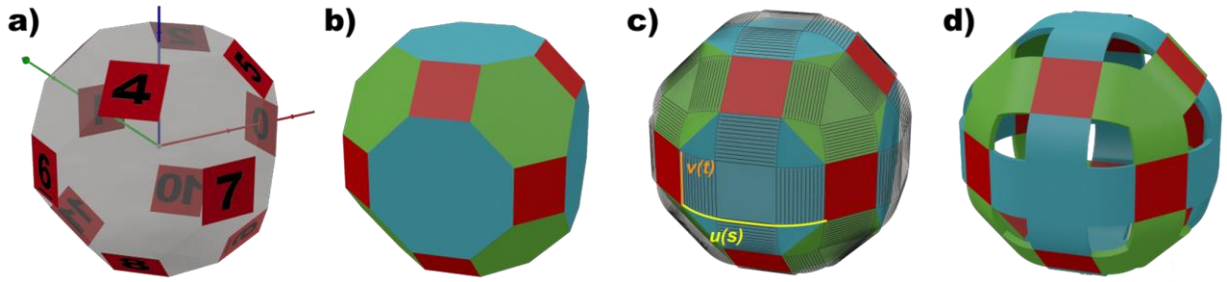


Figure 4.1: Geometrical design of a Quasi-Spherical Module (Catom) for Building Programmable Matter [2].

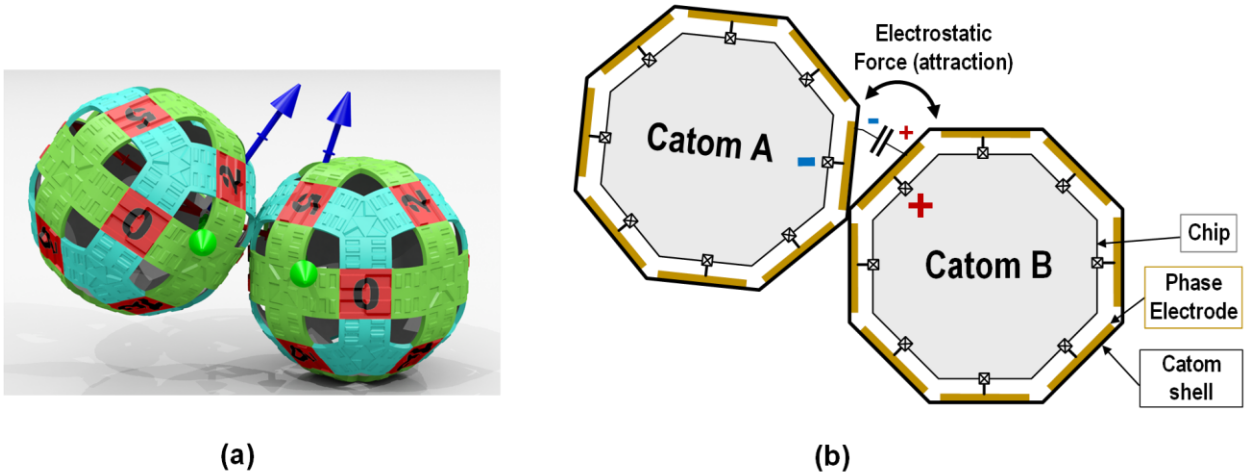


Figure 4.2: (a) The actuation (rotation) operation shown in [18] and (b) the 2-D diagram showing the electrostatic attraction force generation in this work.

Catom actuation includes Latch (stick to each other) and Actuate (move around each other) steps. The Catom surface is insulating and it creates a coupling capacitor when in contact with another Catom. If the electrodes at the inner side of their surface are charged to different potentials, as shown in Fig. 4.2, an electrostatic force will be produced to either latch or actuate the Catoms. The Catom surfaces (at the contact point) are designed to be flat, so the electrostatic force F_e is given by

$$F_e = \frac{\varepsilon_0 A V^2}{2d^2} \tag{4.1}$$

where ε is the vacuum permittivity, V is their electrode voltage difference, and A and d are the overlap area and distance of the two Catom surfaces, respectively.

To increase the latch force when two Catoms are in contact, design options include increasing A and V and/or decreasing d. However, the Catom surface size (determines A) and thickness/flatness (determines d) are limited by the resolution and cost of the fabrication process. Due to this, the most effective way to increase force is by applying higher voltages on the electrodes. With a 10× voltage on the Catom surface, a 100× larger force can be produced, which significantly increases the structural strength of PM in latch positions.

When PM re-configures and the Catoms need to be actuated, the generation of electrostatic force becomes more complex. To move a Catom in the right direction, it needs to change voltage on its multiple surface electrodes according to the condition of their adjacent Catoms. Both attractive force (by using +/- voltage on the 2 Catom surface) and repulsive force (+/+ or -/- voltage) may be used to create the proper force vector on a Catom. Furthermore, during the intermediate states of a Catom movement, the equivalent A and d of its surfaces will continually change, calling

for sophisticated control of voltage and timing. In the following sections, we introduce our design for the Stack, a multi-die system that controls the Catom's communication, computation, actuation and power management, emphasizing a specially designed high voltage generation chip that enables a flexible actuation control in a 3-D PM network.

4.2.2 The Stack: Micro-Controller inside the Catom

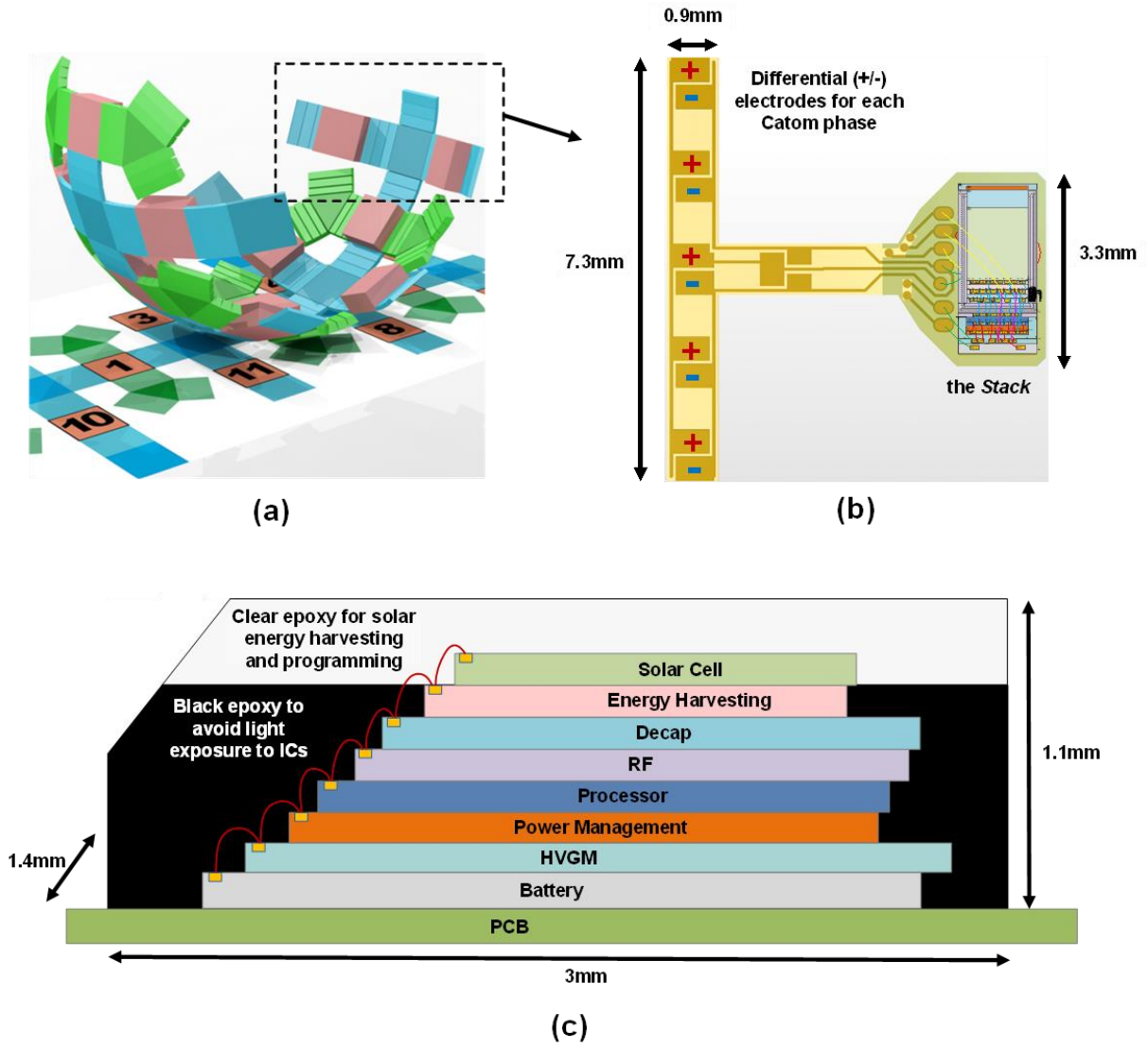


Figure 4.3: (a) The disassembled view of a Catom [18]; (b) the Flex-board design with the micro-controller stack and differential high voltage electrodes, and (c) the diagram showing the stack design with multiple custom IC layers.

The micro-controller for the Catom is a core part of PM hardware design, as it determines the scale, lifetime, intelligence and even physical properties of a PM system. In this thesis, we propose that the Catom's micro-controller consist of a stack of custom-designed integrated circuits (ICs), with the Stack connected to the Catom's surfaces via a flexible PCB board, as shown in Fig. 4.3.

The Stack consists of multiple custom IC layers (in bare die form) with different functionalities. A low power processor IC (ARM Cortex M0+), combined with the solar cell IC, provides the programming interface for the Stack via a Global Optical Communication protocol [77]. The protocol adopts the solar cell as a light receiver, and the external host can synchronize and send commands to one or more Catoms with only 100pJ/bit energy efficiency. When the Catom needs to send a message back to the host, it radios out the data through the short-range RF IC in the Stack. In addition to providing duplex communication, the processor IC also works with the high voltage generation chip (introduced in Section 4.3) to actuate the Catom intelligently using electrostatic force. Connectivity between IC layers in the Stack is achieved by M-Bus [78], an ultra-low power chip-to-chip bus design that uses 4 I/O pads.

The Stack is powered with an integrated thin-film battery layer [79]. Due to the small Catom size, the battery has limited capacity (6μAh), so we integrate an energy harvesting IC to harvest energy from the solar cell and extend Stack lifetime. In a condition with stable ambient light, the energy harvesting IC, along with the decap layer for energy storage and power management IC for power distribution, can produce sufficient energy for the Stack and enable energy autonomous operation. To fit the micro-controller into a Catom, the dies are thinned to 100μm each, and stacked together using wire-bonds for their interconnection. The stacked dies are encapsulated in black epoxy to protect against light and contaminants, while only exposing the

solar cell at the top for energy harvesting and programming purposes. The encapsulated Stack is then attached to a flexible PCB (only 80μm thick), and the high- voltages provided by the Stack are routed through differential (+/-) electrodes to the Catom's surfaces. The differential electrode on each surface makes it easier to implement the high voltage generation chip, and enables better alignment when two Catoms begin making contact. Overall Stack size is 3×1.4×1.1mm, and the micro-controller (including PCB) adds 8.8mg to the Catom weight.

4.2.3 HVGM: Energy-Efficient Scheme for Capacitive Actuators

The property of electrostatic actuation determines that we only need to generate high voltages on a purely capacitive load, with little DC current consumption induced on that load. In PM and many other capacitive MEMS actuators, the load capacitance can be small, in the pF range. This creates a very different condition from that of a common high-voltage converter, where increasing the power efficiency under a certain load current is more important than reducing the power overhead to get high voltages. Compared to inductor-based voltage converters [72], switched-capacitor implementations such as Dickson charge pumps are more suitable for low power scenarios [65] [66]. However, there are few works that achieve both a large voltage conversion ratio (20×) and the requisite ultra-low power consumption (sub-μW).

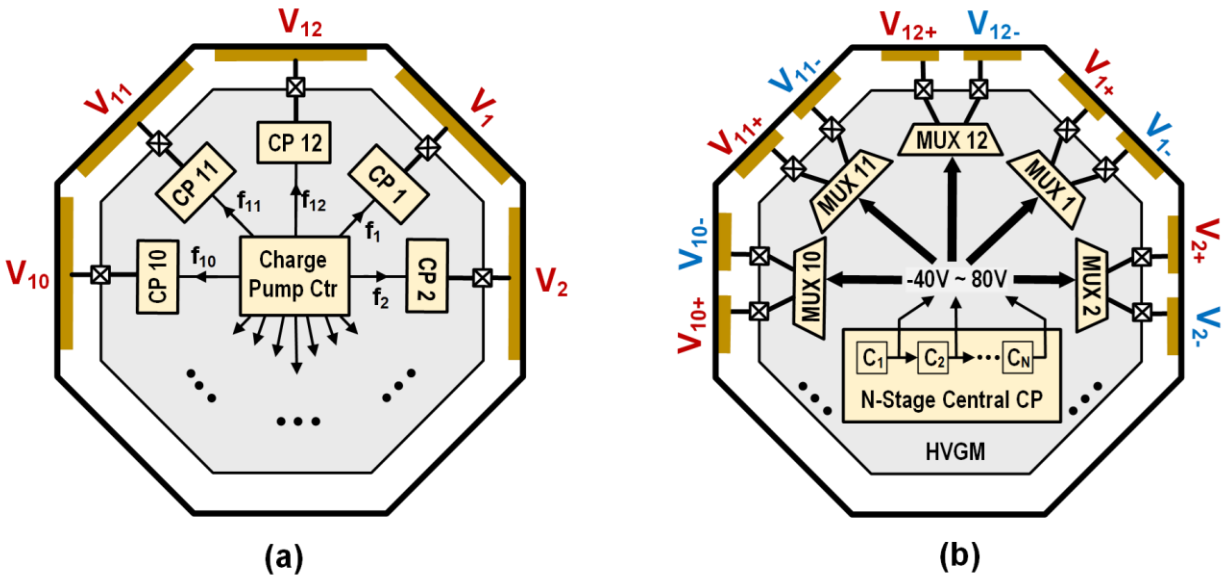


Figure 4.4: (a) The conventional Catom driving circuit that has 12 charge pumps and (b) HVGM with single charge pump and 12 high voltage multiplexers.

Moreover, the 12-phase Catom model requires that each of the phase electrodes be individually controlled. With the conventional driving scheme shown in Fig. 4.4a, each electrode needs to be driven by a separate charge pump, and the charge pump clocks $f_1 - f_2$ are toggled by a local controller to change their output voltages $V_1 - V_2$. Though it is straight forward, this scheme leads to excessive power and area overhead due to the duplication of charge pumps and the clock distribution network. In the envisioned industrial PM systems composed of thousands or even millions of Catoms, power overhead is critical due to the difficulties of power delivery and heat dissipation, while chip area is directly associated with the manufacturing cost per Catom.

Instead of having multiple charge pump copies for the 12 electrodes (capacitive load), the HVGM (Fig. 4.4b) only possesses a single pump (the central charge pump), which generates a variety of voltages from -40V to 80V, sampled from the charge pump output and all the intermediate stages. The design leverages a novel high-voltage multiplexer (HV-MUX) that selects from the charge pump voltages and drives each electrode with a unique voltage selection, achieving individual control of the Catom phases. Since a HV-MUX consumes much less power

and area than a charge pump, the HVGM greatly amortizes the power and cost overhead to support 12 electrodes with the high-voltage conversion ratio. Moreover, unlike charge pumps that need to be frequently turned on and off in a conventional scheme, the HVGM central charge pump is always running at its steady state, and the electrode voltage change is simply achieved by selecting different voltages with the HV-MUX. In this manner, we avoid discharge and recharge of the flying capacitors and other parasitic nodes in the charge pump, further reducing the active power of the HVGM to sub-μW levels.

4.3 Circuit Implementation of HVGM

4.3.1 Central Charge Pump

Fig. 4.5 shows the top-level schematic of the proposed HVGM chip. As explained in the previous section, a single Dickson charge pump is implemented with 22 positive stages ($D_1 - D_{22}$), 13 negative stages ($D_{-13} - D_{-1}$) and a 3.6V sup- ply/clock. This pump generates up to 80V and down to -40V, the former of which is the maximum achievable voltage al- lowed in this process. The central charge pump's output along with its intermediate voltages after each stage are individually selected by 12 positive and negative high-voltage multiplexers (HV-MUXP and HV-MUXN, respectively) to drive the Catom electrodes. During Catom actuation, the voltage changes at the electrodes are also controlled by HV-MUXs, decoupling the central charge pump from the electrodes and ensuring it continually operates in steady state for minimized switching loss.

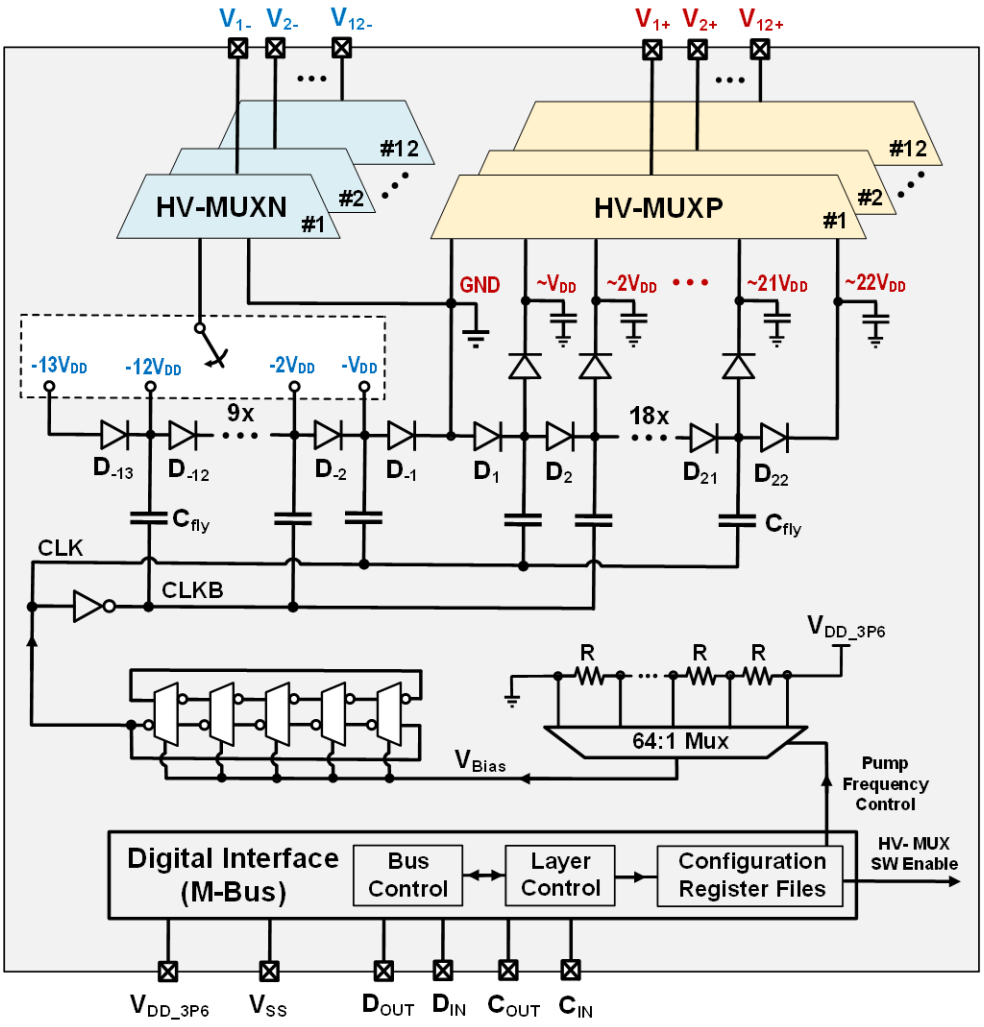


Figure 4.5: Top-level diagram of the proposed HVGM chip.

We note that the frequency of the central charge pump determines the maximum average power that can be delivered to the electrodes. For example, if all 12 electrodes need to be activated simultaneously with a large voltage swing (e.g., 0 to 80V), a faster clock frequency is required to maintain the steady state of the central charge pump while it draws more power from the supply. The clock frequency is generated locally and can be tuned with the digital interface and the re-configurable 64:1 bias voltage selector explained in Section 4.3.4.

To mitigate the power spikes that might occur on the central charge pump, its intermediate voltages are rectified and buffered with storage capacitors before connecting to the high voltage

multiplexers. However, in the negative voltage domain, a circuit implementation is limited by the device type in this process. Hence, we implemented the voltage selection with chip-level wire-bonding (the box indicated with a dashed line in Fig. 4.5), and the HV-MUXN only selects from either a negative voltage or ground voltage. Seen as a differential voltage across two Catom electrodes, the HV-MUXN provides a coarse voltage selection of ~40V, while the HV-MUXP provides fine grain control with a step size of ~3V across 80V. The details of designing the HV-MUXP and HV-MUXN will be explained in the following sections.

4.3.2 HV-MUX for Positive Electrodes (HV-MUXP)

The HVGM scheme greatly amortizes the circuit's area and power overhead by employing a single central charge pump with 12 high-voltage multiplexers. However, a main challenge for the HVGM is the implementation of the multiplexer circuit that works with high voltages but maintains low power/leakage. Fig. 4.6(a) shows a conventional analog multiplexer for electrode #1, where the mux switches S_1 −S_{22} are implemented with transmission gates. If the voltage to be multiplexed exceeds V_{DD}, a level shifter is required to boost the control signal to a higher DC level while keeping a regular voltage swing on V_{GS} to avoid gate oxide breakdown. Fig. 4.6(b) shows a PMOS-only implementation with a clocked level shifter [38] for lower static power. The PMOS body is connected to its source to avoid well leakage, but this also creates a parasitic diode from drain to body (D_{DB}) that results in a large reverse current when the electrode voltage is larger than the charge pump's intermediate voltages. For example, if S_{22} is turned on to drive the electrode with the highest voltage (~$22V_{DD}$), the charge on that electrode will then leak away through S_0−S_{22}, causing a failure to maintain the high voltage for actuation. To block the reverse current from the electrode to the charge pump, we therefore add diodes D_0 −D_{22}, which sit in the opposite direction from the parasitic diode of S_0 − S_{22}, as shown in Fig. 4.6(c). D_0 − D_{22} are arranged with serial

connections, lowering the reverse voltage stress on each diode to be within V_{DD} and further reducing their reverse current (leakage) to sub-pA levels. Though the electrode will have a larger conduction loss due to the serial-connected diodes, the overhead is quite negligible in our measurements because of the high-voltage and low-current condition.

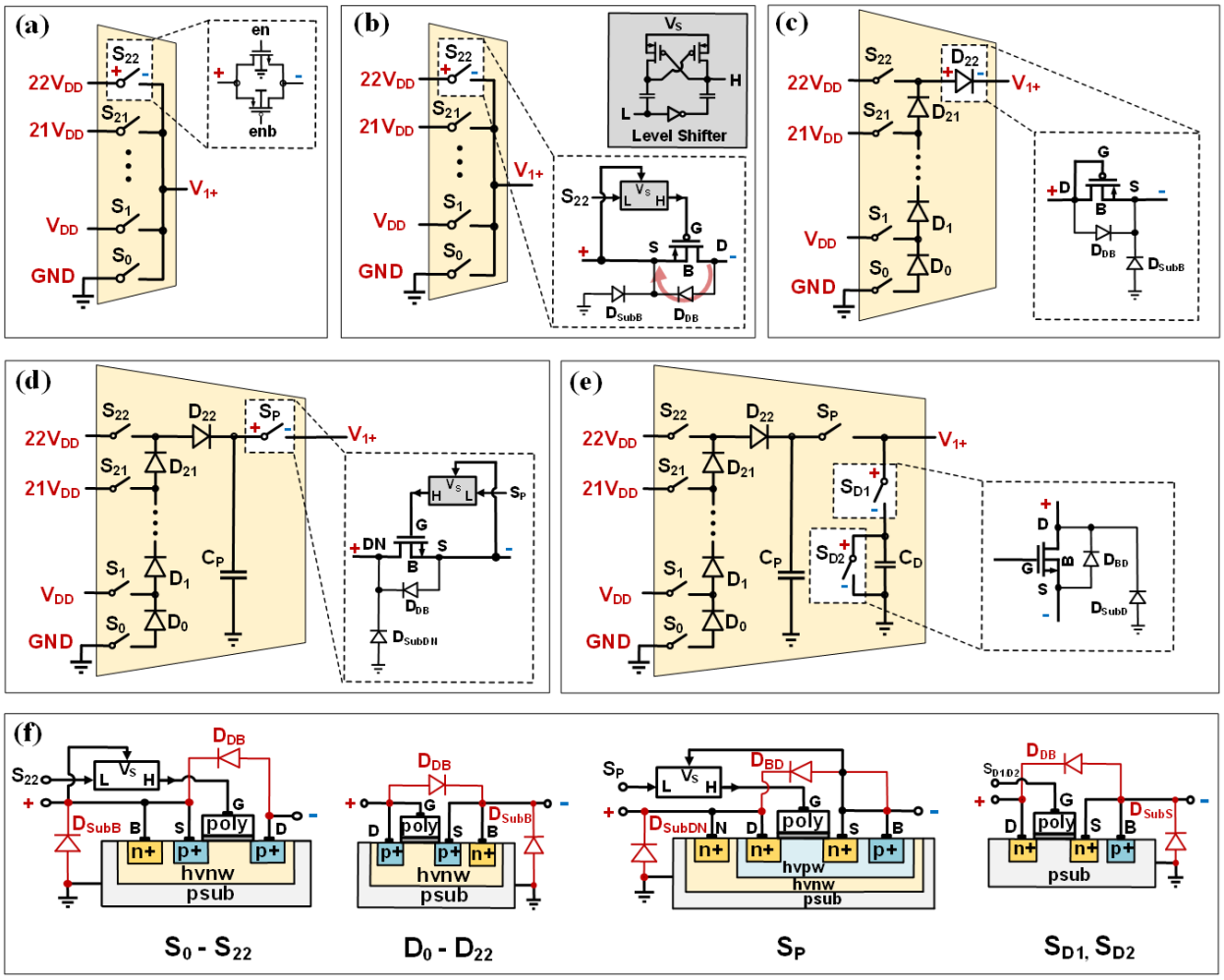


Figure 4.6: (a) a conventional analog multiplexer with transmission gate; (b) a level-shifted high-voltage analog multiplexer that has a risk of reverse current (red arrow); (c) the improved high-voltage multiplexer with current-blocking diodes; (d) further improved high-voltage multiplexer with switched-capacitor resistance to limit peak current; (e) the final high-voltage multiplexer implementation with controlled discharge path and (f) device details and cross-section view in (e).

A second challenge manifests when a voltage switch S_i (i ranges from 1 to 22) ramps up the electrode voltage V_{1+}, drawing a large in-rush charge from the central charge pump. Even though there are buffer capacitors at each stage of the central charge pump, we may still see large

voltage drops on any of the intermediate voltages (V_{DD} to $22V_{DD}$). Although the intermediate voltages can be gradually restored by the central charge pump, their sudden change can cause a failure of the level shifter, which is not recoverable once triggered. This is because the level shifter operates with a clock that constantly "refreshes" its output based on a stable DC value (V_S), and it can lose track when the DC value changes abruptly within a clock cycle. Hence, the charge transfer rate from the pump to electrodes must be carefully limited to guarantee stable voltages at all electrodes. In the HVGM, we implement a switch S_P after the last diode D_{22} along with a buffer capacitor C_P as shown in Fig. 4.6(d) to form a current- limiting resistance between the central charge pump and the electrode. The equivalent resistance in this path can be tuned by changing the switching frequencies of S_P and S_i, trading off the electrode charging speed with the power drawn from the central charge pump. The capacitance of C_P (200fF) is small compared to that of the electrode (10s of pF), so the voltage swing on C_P is large and cannot be used as V_S by the level shifter. Instead we level shift the S_P control signal based on the electrode voltage V_{1+}, which is slowly charged and hence easy to track, and we implement S_P with an NMOS transistor accordingly.

A third challenge is that with the addition of diodes $D_0 - D_{22}$, the central charge pump can only provide charge to the electrode (i.e., it cannot discharge). With no DC load current on the electrode, its voltage will decrease extremely slowly (through leakage), which is problematic for periodic actuation. Hence, we implement an intentional discharge path with switched-cap resistor S_{D1}, S_{D2}, and C_D. By using the regular supply voltage to control switches S_{D1} and S_{D2} in a non-overlapping way, we limit the charge transfer to $C_D V_{DD} V_{th}$ per cycle, and the electrode is gradually discharged at a controllable speed. When not discharging, both S_{D1} and S_{D2} are turned off, creating a stack effect to strongly reduce leakage at the electrode.

4.3.3 HV-MUX for Negative Electrodes (HV-MUXN)

Previous sections explained the advantages of having the electrodes driven by negative voltages, thereby increasing the voltage stress and achieving more electrostatic force. However, multiplexing the negative voltage requires a different approach than that proposed for positive voltages in the preceding section. In the HV-MUXN, the counterpart of the HV-MUXP, all switches are implemented with NMOS transistors because their control signals are level shifted from a lower potential side (from the central charge pump), as shown in Fig. 4.7(a). A high-voltage-n-well (hvnw) layer separates the NMOS body (P-type diffusion biased with negative voltage) from the chip substrate (grounded) to avoid substrate leakage. However, diodes $D_0 - D_{13}$ have the same parasitic diodes (S_{BD} and S_{BN}) as the switches $S_0 - S_{13}$, failing to block the reverse current if it occurs at the switches. Further, switches S_{D1}, S_{D2} and S_P would need to be PMOS, which is not possible since their n-well, which is connected to the negative voltage, would short to the P-type substrate through the well diode.

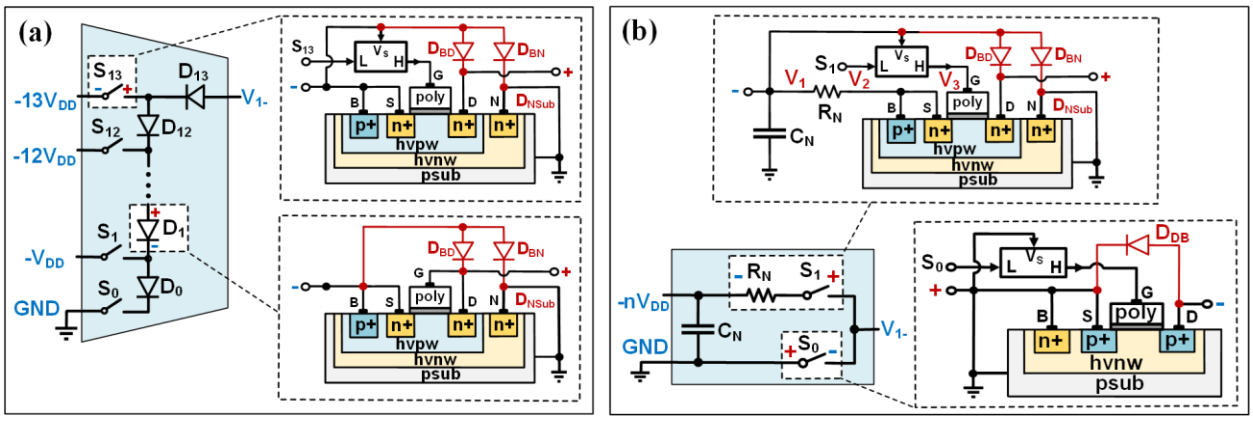


Figure 4.7: (a) Implementation of HV-MUXN similar to its positive counterpart but with reverse current issue. (b) the actual HV-MUXN implementation with dual voltage selection and poly-resistor to limit the current.

We instead opt for a simpler binary HV-MUXN that selects between one of the negative voltages and GND (Fig. 4.7(b)). While S_1 uses an NMOS with an hvnw layer, S_0 is imple- mented with PMOS transistors and its gate control signal is level shifted to toggle between $-V_{DD}$ and

ground. Since it is not possible to implement the switched-capacitor resistor with S_P, we use a poly resistor R_N to limit the current from the central charge pump to the negative electrode. However, the resistance of R_N is constrained to sub-MΩ due to chip area limits, which is insufficient to limit the current flow to μA levels under a large negative voltage (-40V). We therefore make S_1 a weakly turned-on switch that endures most of the voltage stress and effectively limit the current through it. This is achieved by level shifting its gate voltage V_3 from V_1 (instead of V_2 in the normal case) as shown in Fig. 4.7(b). Since the level shifter provides a shift that is smaller than V_{DD}, we have

$$V_G = V_3 < V_1 + V_{DD} \tag{4.2}$$

Meanwhile, when the NMOS transistor is turned on, then

$$V_2 = V_3 - V_{TH} \tag{4.3}$$

Combining (4.2) and (4.3) we have

$$V_2 < V_1 + V_{DD} - V_{TH} \tag{4.4}$$

or equivalently

$$V_2 - V_1 < V_{DD} - V_{TH} \tag{4.5}$$

This indicates that the voltage across R_N is always limited to less than ($V_{DD} - V_{TH}$) no matter how large the voltage is between the pump and the electrode. The current flow is therefore also limited to $(V_{DD} - V_{TH})/R_N$ independent of the voltage being multiplexed.

4.3.4 Peripheral Circuits in HVGM

The central charge pump and HV-MUXs provide a flexible and efficient way to achieve high-voltage actuation. The control logic for them can be summarized into two classes: 1) switch enable signals and 2) the frequency control signal, as shown in Fig. 4.5. The enable signals control the switching activities of the HV-MUXP and HV-MUXN, multiplexing and driving the electrode with proper voltages defined by the user. The frequency control signal is achieved by a leakage-based ring oscillator [61] as shown in Fig. 4.8. The ring oscillator consists of leakage-based inverters with an additional low-Vth (LVT) device pair in the middle. When the input voltage flips, the leakage path through the LVT latch controls the delay of output toggling and determines the oscillation frequency. Further tuning of the frequency can be achieved by adding a current path with the parallel transistors that are biased with V_{BN} (the PMOS parallel legs are disabled by biasing at V_{DD}). The voltage V_{BN} is generated by a poly-resistor divider and selected with a 64-to-1 multiplexer. It achieves a broad band frequency tuning range (30Hz - 1MHz measured at room temperature) for the charge pump and HV-MUXs, and therefore provides a wide range for Catom actuation speed.

The enable and frequency control signals are stored in configuration register files in the M-Bus block. As we previously mentioned, the HVGM is a member layer in the Catom stack, and it receives the actuation code through the CIN and DIN terminals and passes its working state to the other layers through C_{OUT} and D_{OUT}. When the HVGM is not changing its actuation mode (e.g., latching to another Catom/HVGM), most of the M-Bus block is power gated and only draws static current, further reducing the power overhead for the digital circuits.

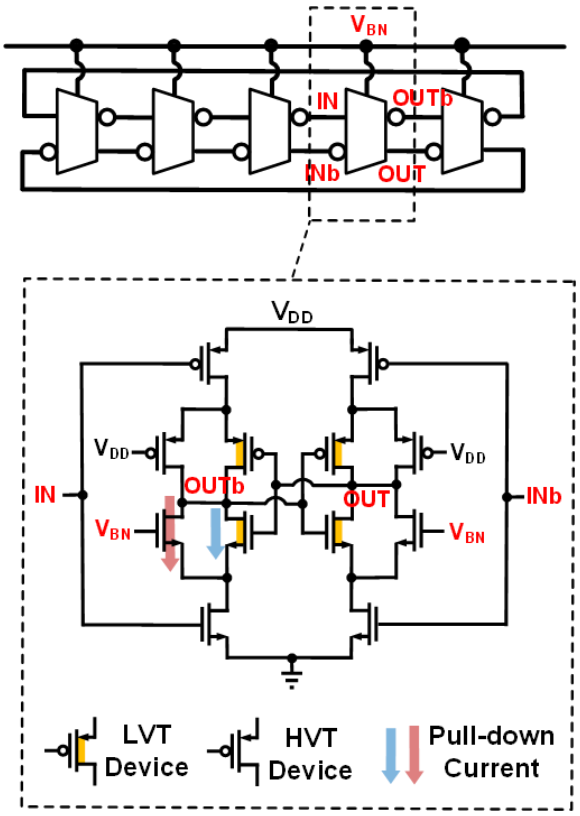


Figure 4.8: Leakage-based ring oscillator [80] with bias voltage VBN controlling the output frequency.

4.4 Measurement Results and Analysis

4.4.1 HVGM Measurement Results

HVGM is fabricated in a 180nm HVBCD process and occupies 3.67mm^2 including the area for 24 pads that connect to positive and negative electrodes in a Catom. Fig. 4.9 shows the HVGM die photograph.

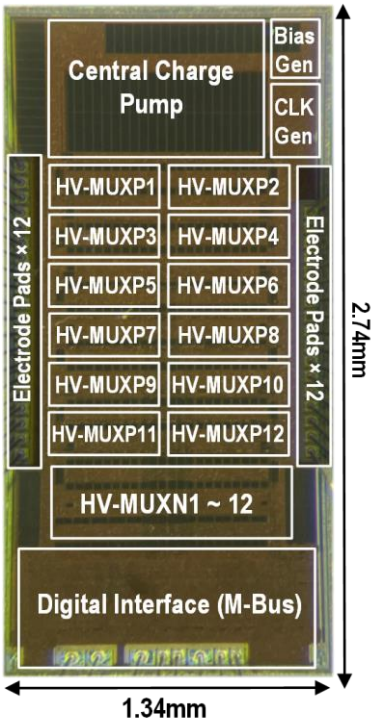


Figure 4.9: HVGM die photo.

In the idle state, the HVGM consumes 7nW power at room temperature from a 3.6V supply. In the latch state, it consumes 130nW to sustain a DC voltage of 100V on one pair of the +/- electrodes. When in the actuation state, however, the HVGM can trade off its active power with the actuation speed that is determined by the slew rate charging/discharging the electrode. Fig. 4.10 shows the transient waveform of the HVGM driving a 10pF electrode with the minimum and maximum actuation speeds. In the slowest actuation setting, the HVGM operates at a frequency of 625Hz, consuming 286nW average power to charge an electrode at 155V/s slew rate, which is sufficient for PM to achieve a 0.2Hz periodic actuation with 103V voltage swing (29× voltage gain). With the same load condition, the HVGM can support up to 60Hz actuation by increasing its frequency to 46kHz, consuming 14.1µW. Fig. 4.11 further demonstrates the frequency-power trade-off in more detail.

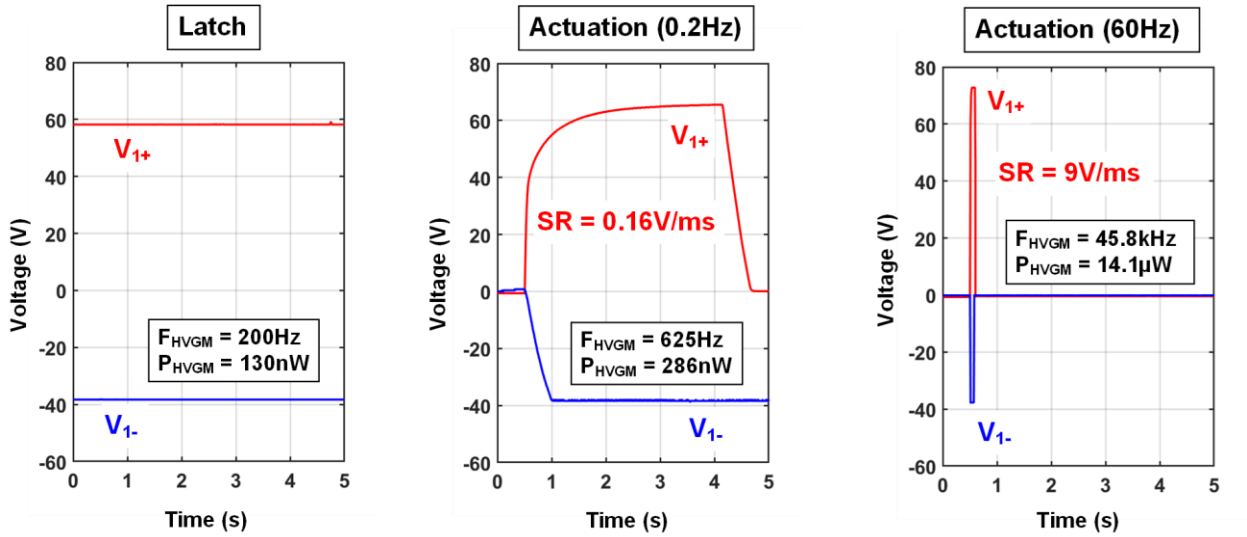


Figure 4.10: Measured transient waveform showing the electrode voltage to latch (left), slow actuate (middle) and fast actuate (right).

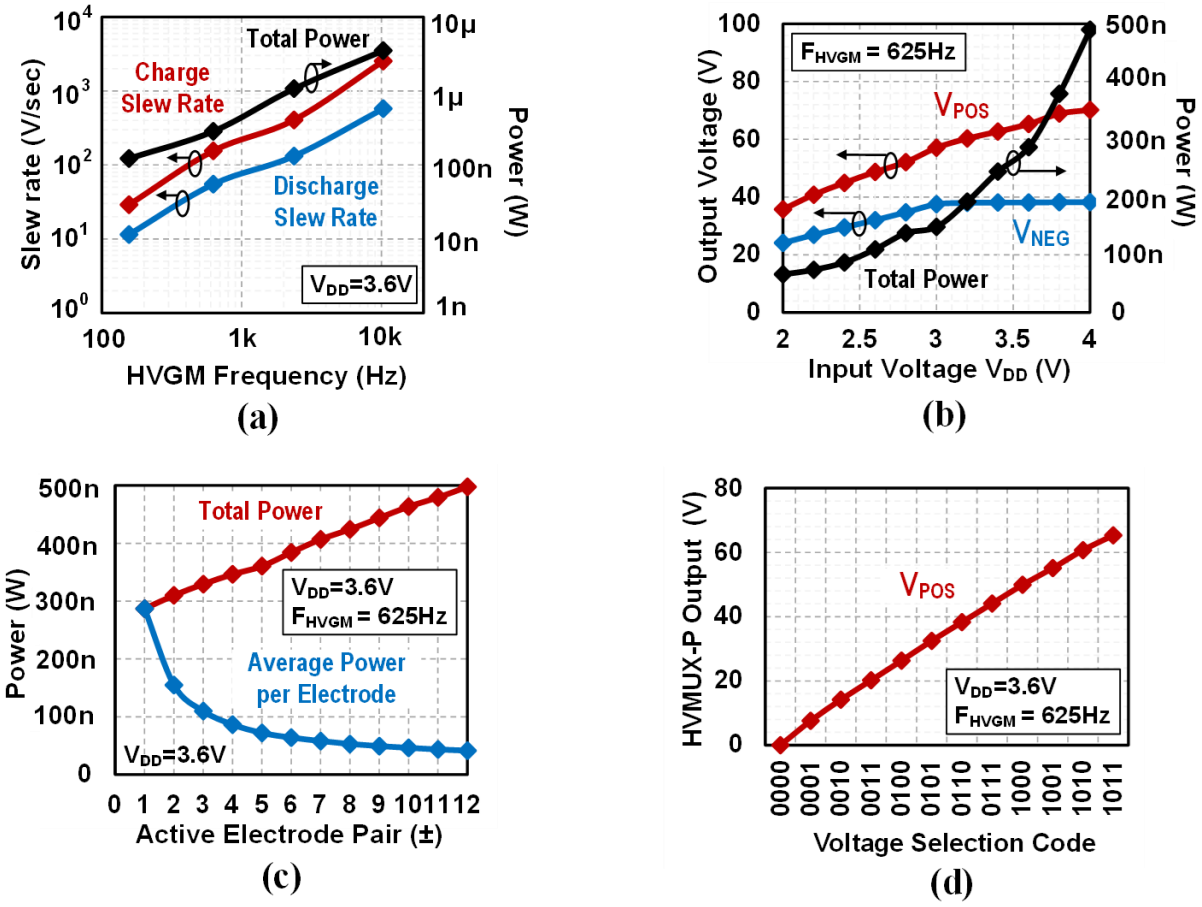


Figure 4.11: (a) Measured HVGM power versus the electrode slew rate at different clock frequencies; (b) measured HVGM output voltage and power with different supply voltages; (c) measured HVGM power with different number of electrode being activated; (d) measured HVGM output programmability.

The HVGM benefits from the single pump topology by significantly amortizing the charge pump power at higher electrode counts. This is confirmed by the measurement results in Fig. 4.11(b). With more electrodes being actively transitioned, the average power per electrode reduces from 286nW (1 electrode pair) to 41nW (12 electrode pairs). Fig. 4.11(c) shows the maximum HVGM voltage on the positive and negative electrodes with different supply voltages. In addition to driving the electrodes with the maximum voltage, the HVGM also provides programmable voltages with a 5V step depending on the actuation command type, as shown in Fig. 4.11(d).

Table 4.1 compares HVGM performance with prior on-chip high voltage generators. Though their load conditions vary, HVGM shows the highest voltage gain and lowest power consumption when generating high voltages that are sufficient for PM and many other micro-robot actuators. It is also the first to have fully programmable high voltages on multiple output ports, which further extends its application range towards IoT.

Publication*	Process	Circuit Type	V_{IN}	V_{OUT}	Voltage Gain	Output Frequency	Power ***	Load Condition	Output Adjustable	Number of Output
JSSC 2019 [6]	$0.35\mu m$	Charge Pump	3.3V	32.6V	9.9	DC	$97\mu W@DC$	-	No	1
ISSCC 2014 [7]	65nm	Charge Pump	2.75V	34V	12.3	DC	-	-	No	1
ISCAS 2011 [8]	$1\mu m$	Charge Pump + Rectifier	5V	33V	6.6	DC - 500Hz**	-	10pF	No	1
TCAS1 2015 [9]	$0.8\mu m$	HV Amp + Multiplexer	5V & 300V	290V	58.0 & 0.97	DC	90mW @ DC	10nF	No	1
ISCAS 2016 [10]	$0.8\mu m$	Voltage Doubler	15v	360.5V	24.0	DC - 60Hz	-	-	No	1
ICECS 2014 [11]	$0.13\mu m$	Charge Pump	1.2v	10.6V	8.8	DC - 100kHz**	$759\mu W@100kHz$	1pF	Yes	1
Ind. Elect. 2013 [12]	$0.6\mu m$	Charge Pump	6v	51V	8.5	DC - 1kHz**	-	1pF	No	1
This work	$0.18\mu m$	Charge Pump + Multiplexer	3.6v	103V	28.6	DC - 60Hz	130nW@DC 286nW@0.2Hz $14.1\mu W@60Hz$	10pF	Yes	12

* All works in the table are fully integrated high-voltage generators with no/light load.
** Estimated from the measurement results shown in the paper.
*** Some works did not report power number (but only efficiency) because they are not power constrained.

Table 4.1: Performance Summary of HVGM and comparison with prior works.

4.4.2 Stack and Catom Integration

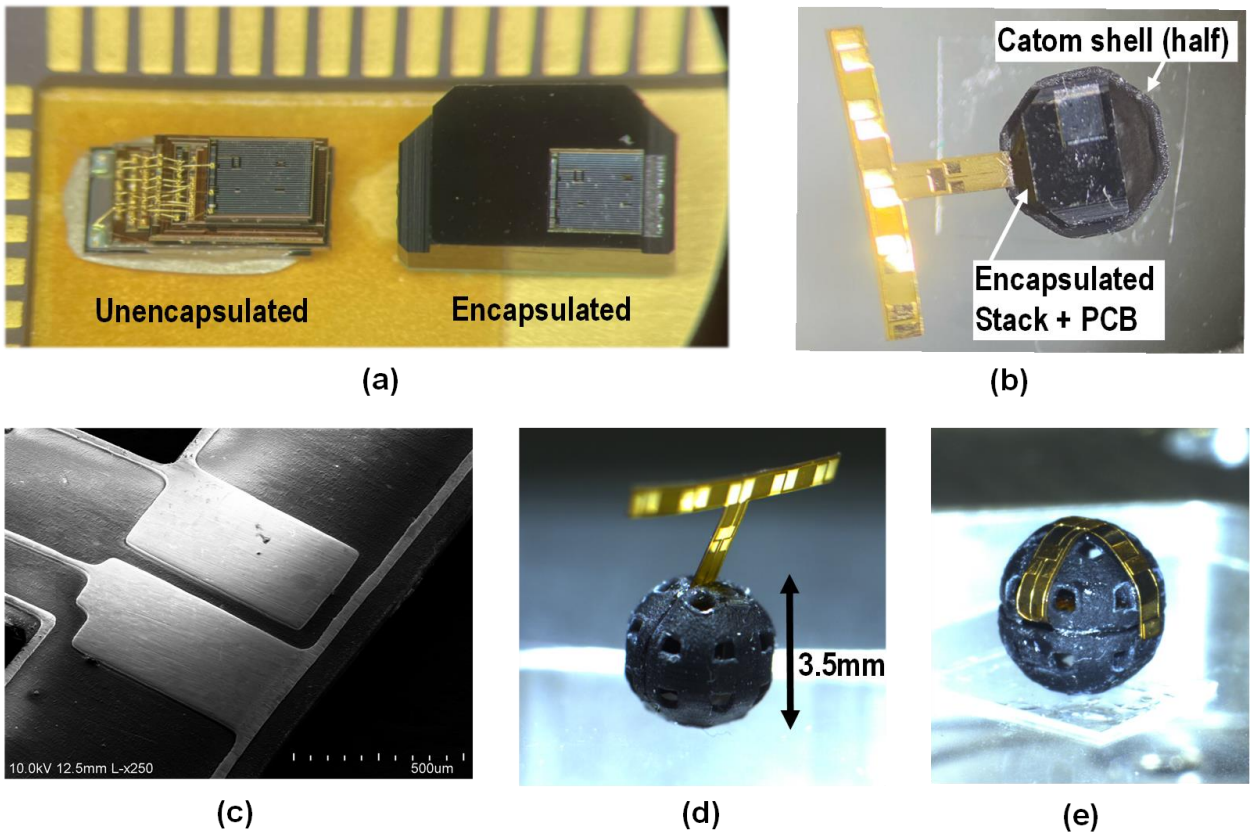


Figure 4.12: (a) The Stack photo with and without the black epoxy encapsulation; (b) encapsulated Stack fit in a half Catom shell and connected to the flexible PCB; (c) microscope image showing the differential electrode design on the flexible PCB; (d) full Catom with the Stack in it and an unattached flexible PCB; (e) full Catom with the Stack and flexible PCB attached to its surfaces.

The HVGM die is thinned and stacked with other ICs, as explained in Section 4.2.2, to form the Stack that resides in the Catom. Fig. 4.12(a) shows the Stack photo without and with the black epoxy, with 3×1.4×1.1mm size and 4.8mg weight after the encapsulation. The encapsulated Stack is then connected to the flexible PCB (80μm thick and 4mg weight) and fit into a Catom shell with ~3.5mm diameter, as shown in Fig. 4.12(b). The high voltage pads from the Stack (HVGM die) are wire-bonded to the flexible PCB, and connected to the differential electrodes that will be attached to the Catom surfaces. Fig. 4.12(c) shows the microscope image for a pair of the differential electrodes. The metals are carefully deposited and cleaned for a flat surface, which

guarantees close contact (smaller gap distance) with another Catom's electrodes and increases the electrostatic force.

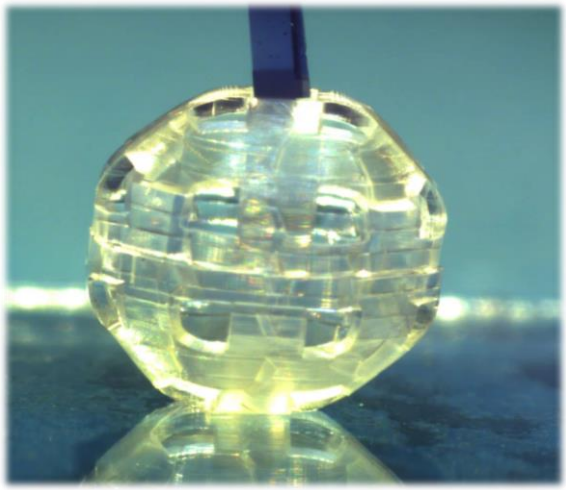


Figure 4.13: Catom hardware with transparent shell for solar energy harvesting and communication.

The Stack integration, the flexible PCB and full Catom shell are shown in Figs. 12(d) and (e). For the demonstration we only include the electrodes for the upper hemisphere of the Catom. In real applications, the Catom shell will be fabricated with a transparent material (Fig. 4.13) that enables the light to go through the shell and be received by the Stack. When the Stack is powered up, we have measured an electrostatic force sufficient to adhere/release a >1mg mass with the high voltages generated by the HVGM. We are currently running a real latching and actuation test with two fabricated Catoms, and will be publishing the new results soon.

4.5 HVGMv2: Single-Chip µ-Controller for the Catom

The Stack possesses multiple chip layers for complex functionalities, and it can take advantage of using different process for the Stack layers. For example, HVGM and the solar layer are implemented in a 180nm process for low leakage and high voltage tolerance, and the processor layer is implemented with a 28nm process for a higher logic density. However, chips need to be taped out separately and integrated at the bare-die level by wire-bonding, which significantly

increases the manufacturing cost to build PM. While we prototype the first generation of Catoms with the Stack design, we also propose the next generation Catom controller with everything integrated on one chip, HVGMv2.

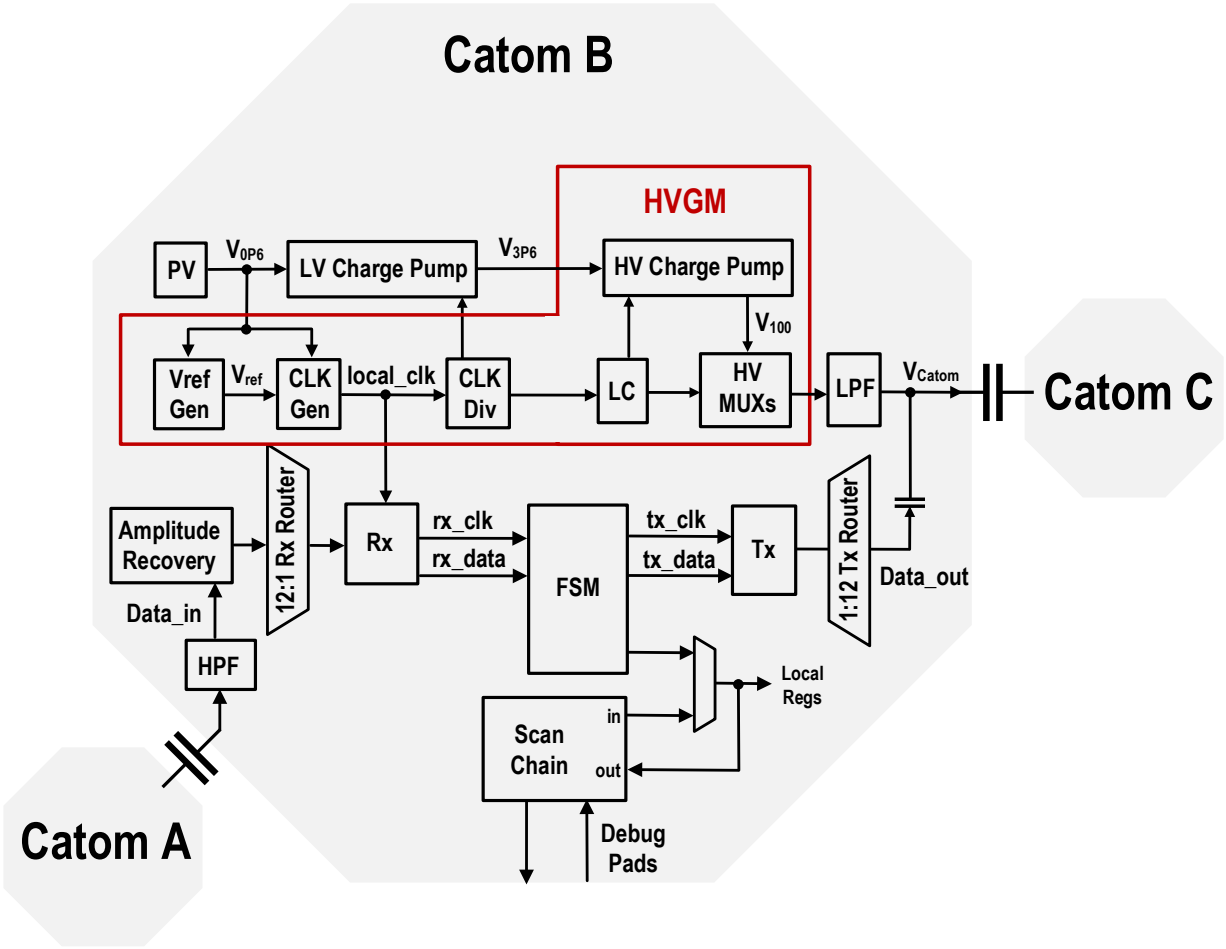


Figure 4.14: Top level diagram of HVGMv2.

As shown in Fig. 4.14, HVGMv2 includes the design of HVGM to maintain the high-voltage actuation capability, and it is implemented with the 180nm HVBCD process. However, the other layers (e.g., processor and RF) in the Stack could not be simply replicated in HVGMv2 due to the lower logic density and higher power. We instead implement a simple finite-state-machine (FSM) in HVGMv2 to process the instruction/program, and the RF block is eliminated by using a capacitive-coupling communication between neighboring Catoms. HVGMv2 has on-

chip photovoltaic (PV) cells for solar energy harvesting, and it also integrates a power management circuit to support fully autonomous PM operations.

Fig. 4.15 shows the HVGM die photo with 7.42 mm^2 area, including the pads for 24 electrodes. It is currently being tested, so in the following subsections we will briefly introduce each part of the circuit in HVGMv2. A complete test results will be published soon.

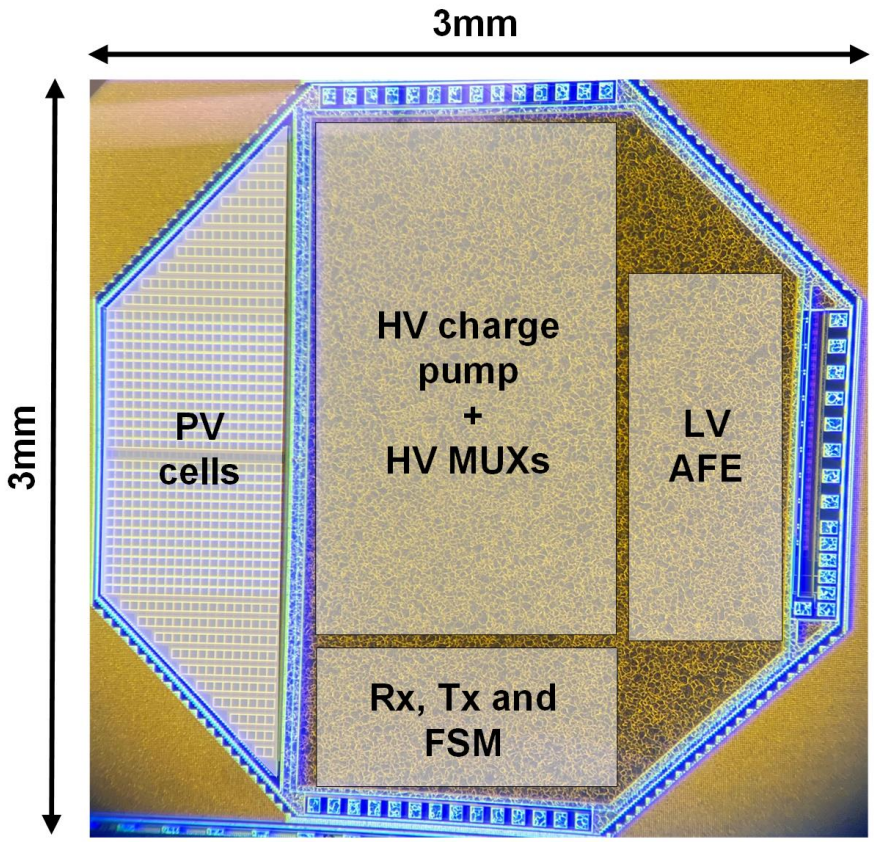


Figure 4.15: Die photo of HVGMv2.

4.5.1 Solar Energy Harvesting and Power Management

The red box in Fig. 4.14 shows the high-voltage actuation circuit in HVGMv2. Similar to that in HVGM, the HV charge pump generates the high voltages (e.g., V_{100}) for electrostatic actuation, and the high voltages are multiplexed by the HV-MUXs to drive the Catom electrodes. However, the HV charge pump takes 3.6V as its supply voltage (V_{3P6}), which is much higher than

the voltage provided by the PV cells. Another LV charge pump is utilized to convert the PV cell output V_{0P6} to V_{3P6}, and level converters are inserted between the two power domains for isolation purposes. The switching clocks required by the HV & LV charge pumps are generated in a similar way as in HVGM, but in the V_{0P6} power domain to significantly save the power for clocking.

The LV charge pump takes 0.6V as its input, but it is still higher than the PV cell voltage which is normally in the 0.3V – 0.4V range. This voltage gap could be resolved by using another voltage conversion circuit, but it will further degrade the power efficiency and increase circuit complexity. In HVGMv2, we instead opt for a 'stacked' PV cell structure proposed by [81] that combines a positive and a negative terminal to get 2× voltage across them. As shown in Fig. 4.16, the negative solar cells configure in the opposite direction to its positive counterpart, producing the +/- voltages at V_{solar+} and V_{solar-}, respectively. All the active circuits (e.g., inverters show at the right) in HVGMv2 use V_{solar-} as the common ground and V_{solar+} as the supply voltage, while the silicon substrate P_{sub} is floating between V_{solar+} and V_{solar-}.

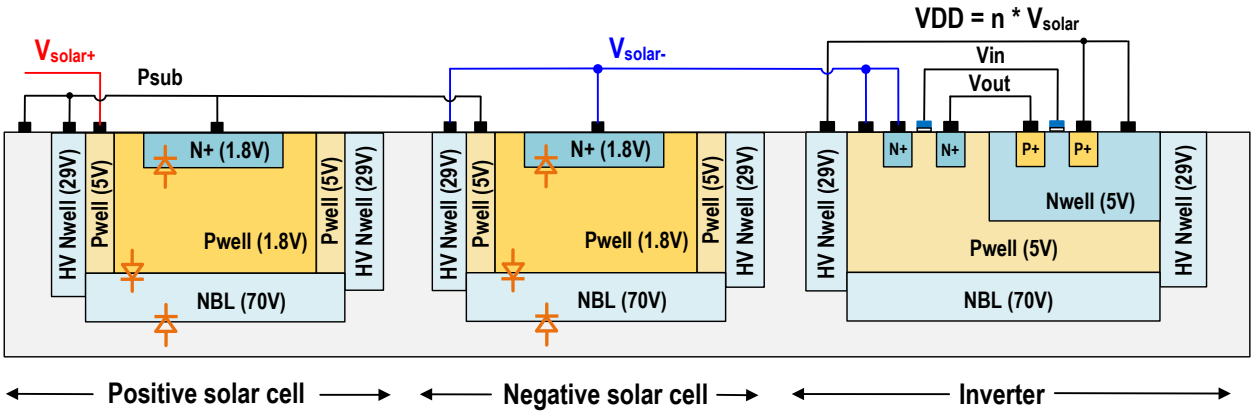


Figure 4.16: The cross-section view of the stacked PV cell structure in HVGMv2.

The PV cells in HVGMv2 are exposed to light to harvest solar energy, but the active circuits need to be shielded to prevent light-induced substrate leakage. Epoxy encapsulation used for the Stack does not work well for HVGMv2, because PV cells and circuits are on the same die.

Therefore, we propose a local shielding by using a solid, unslotted top metal plate to cover the circuit area, but exposing the PV cell area. The thick top metal will reflect most of the light down to silicon, and reduce the substrate leakage significantly.

4.5.2 Capacitive Coupling Communication

RF blocks are eliminated in HVGMv2 for better power efficiency and lower cost. As an alternative, the inter-Catom communication is achieved via the capacitive coupling channels between neighboring Catoms. That is said, a Catom can only transmit and receive information from another Catom when they 'latch' together and form a coupling capacitor between their phases. Previously in HVGM, this coupling capacitor is charged with differential DC voltages to generate electrostatic attraction force; but in HVGMv2 we also modulate the DC voltages with a high frequency AC signal that carries the information/program to Catoms.

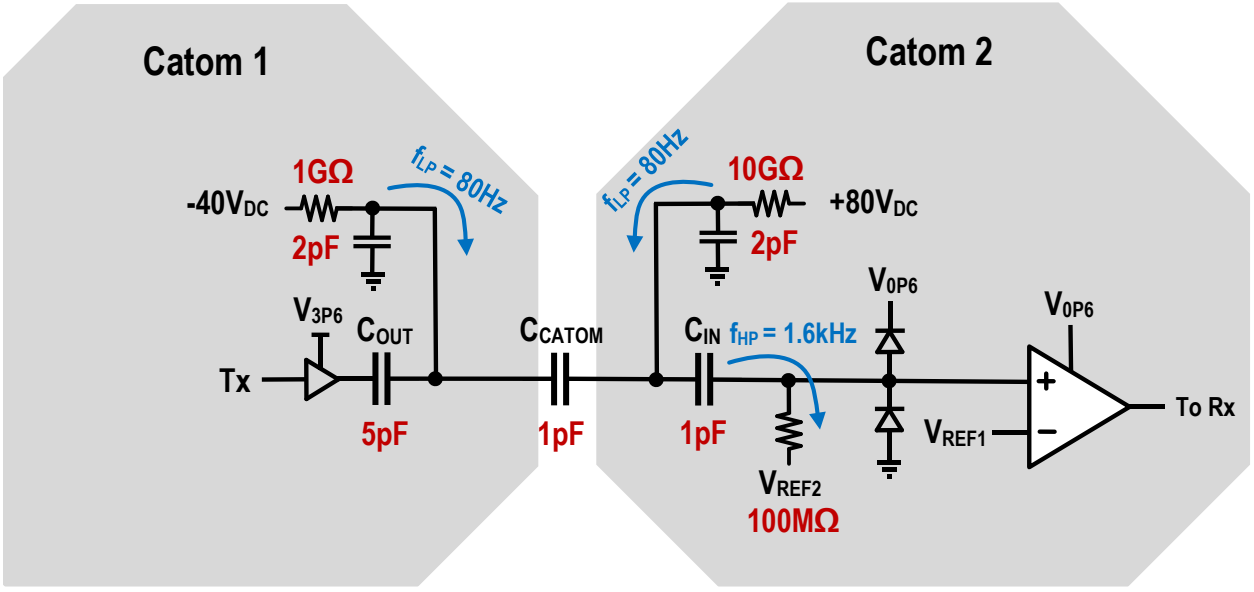


Figure 4.17: Analog front end design for the capacitive coupling communication in HVGMv2.

As shown in Fig. 4.17, the signal from Catom 1 data transceiver (Tx) is AC-coupled to the negative electrode, going through the inter-Catom capacitor (C_{CATOM}) to the positive electrode of Catom 2, and being de-coupled by the analog frond end of the receiver (Rx). The signal is high-

pass filtered at 1.6kHz while the DC high-voltages low-pass filtered at 80Hz, ensuring that the charge pump ripples will not couple into the communication channel. After the signal arrives at Catom 2, it first goes into a comparator that recovered the signal amplitude. Then the full-scale signal is fed into the input router, a 12:1 digital multiplexer that selects the first-arrived signal from 12 Catom phases and sends it to the Rx for demodulation.

4.5.3 Rx, Tx and FSM Design

When two Catoms latch together, their in-contact phases only form one channel for communication. Therefore, we send Manchester-encoded data through that channel for self-clocking. As shown in Fig. 4.18, a data package includes:

1. Training clocks (>9 bits): HVGMv2 locks its local clock frequency to the training clock, maintaining the right clock phase to read the incoming data.
2. Passcode (15 bits): The capacitive coupling channel between two Catoms may suffer from high-voltage ripples or environmental noise. HVGMv2 will only consider it a valid program when it detects a hard-coded passcode in the received sequence.
3. Routing information (1+4N bits): the data package can be passed from one Catom to another in a N-Catoms chain. The routing information tells the current receiver (e.g., Catom 1) where to pass this data package (e.g., to its phase-8 that is in contact with the next Catom in the chain).
4. Program (163 bits): the actual data used by the Catom, configuring its internal switches and determining the voltage changes at its 12 phases to realize PM.

Initially, the Rx is in idle state, waiting for any incoming sequence from the analog front end. When it receives sufficient numbers of training clocks, it locks to the input data rate and listens to the passcode. After detecting the correct passcode, the Rx block is fully awakes and

begins to demodulate the Manchester-encoded data package. After receiving the full length of data, the FSM processes the program information, modulate the sequence again and send to the next Catom. When Tx finishes broadcasting data, the whole digital block comes back to the idle state and waits for the next message.

Training CLK (all 1s)	Passcode 15 bits	Routing Info (1+4N) bits	Program 163 bits

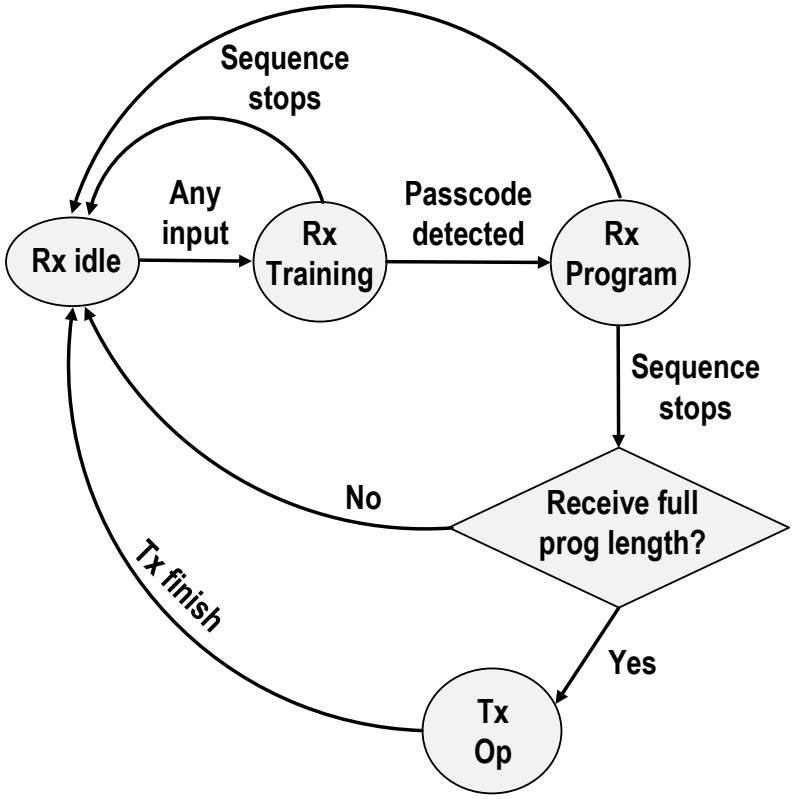


Figure 4.18: Data package for the HVGMv2 communication (top), and a simplified state transition diagram for the Tx + Rx + FSM (bottom).

4.6 Conclusion

This chapter presents a high-voltage-generation-and-multiplexing (HVGM) chip in a 180nm HVBCD CMOS process, which is specifically designed for the actuation of Catoms in PM

and other capacitive micro-actuators. The HVGM chip can individually control 12 pairs of +/- electrodes in a Catom, with its novel design on the high voltage multiplexers to either maintain a high voltage at the electrode (for latch) or change its voltage at a controlled speed (for actuation). The HVGM consumes only 130nW in latch mode and 286nW - 14.1μW in actuation mode depending on the speed, achieving 0 – 103V programmable voltages on the 12 electrode pairs. To achieve fully autonomous operation, the HVGM is integrated with other chip layers to form a complete microsystem of stacked dies, including a processor, radio, energy harvester and battery. The fabricated Stack is 4.6mm^3 size and weights 4.8mg, and it is integrated with a 3.5mm Catom and shows sufficient adhesive force and release of a >1mg mass using the high voltages generated by the HVGM. A second version of the Catom controller is also discussed, achieving a single-chip solution to support high-voltage actuation, energy harvesting, communication and data processing.

Chapter 5 Conclusion

5.1 Summary of Contribution

The miniaturized and intelligent IoT sensor nodes require new designs and techniques to address the challenges associated with its power and size constraints. This thesis presents circuit and system designs with sub-μW power consumption for long lifetime of continuously sensing, communicating and actuating with motions. Battery-less operations are enabled to harvest kinetic energy from ambient sources.

In Chapter 2, we discussed how to efficiently harvest kinetic energy to power batteryless sensor nodes with piezoelectric energy harvesters, or PEHs. We present a sense-and-set (SaS) rectifier circuit that maintains optimal energy extraction for different input excitation levels and output voltages. The proposed circuit is fabricated in 0.18-μm CMOS process with 0.47mm^2 core area, 230nW active power and 7nW leakage power. Measured with a commercial PEH device (Mide PPA-1022) at 85 Hz and 60 Hz vibration frequency, the proposed circuit shows 512% and 541% power extraction improvement (FoM) compared with an ideal full-bridge rectifier for on-resonance and off-resonance vibrations, respectively, while maintaining high efficiency across different input levels and PEH parameters.

In Chapter 3, we propose a novel architecture for the MEMS capacitive accelerometer that bypasses the fundamental trade-off between power and noise (resolution) in conventional accelerometers. We bias the MEMS with much higher voltages while maintaining its stability with electrostatic mismatch compensation, thereby improving the power/noise trade-off substantially.

The proposed accelerometer achieves a very low 121μg/ √ Hz input referred noise with only 184nW per-axis power, enabling a much longer lifetime when operate with limited battery capacity.

In Chapter 4, a high-voltage-generation-and-multiplexing (HVGM) chip is introduced to electrostatically actuate the Catom, a mm-scale micro-robot that can form into arbitrary structures or programmable matters (PM). The key challenges to achieving PM actuation are discussed in detail and solved by the proposed work, including >100V voltage generation with sub-μW power, the <3mm size constrains and the requirement for a complete and robust system integration. HVGM individually control 12 pairs of +/- electrodes using a positive and negative charge pump and mux-structure, consumes only 286nW in steady state and 533nW when transitioning a 10pF electrode at 155V/s, and produces a differential voltage of 103V (29× voltage gain from 3.6V input) in measurement. We also present a complete μ-controller design for the intelligent combination and actuation of programmable matter. The first generation of controller is implemented with a stacked-chip system, while the second controller design is implemented with a single-chip solution for communication, programming, and self-powering capabilities.

5.2 Directions for Future Research

5.2.1 Sense-and-Set Energy Harvesting

The proposed SaS circuit can achieve theoretically maximized power extraction from the PEHs. However, it still has the following limitations:

1. The highest voltage that SaS can 'set' is constrained by the process to be only 2V. However, for most of PEHs their V_{MPP} can go much higher than this, so the 2V limit becomes a bottleneck to further improving power efficiency.

2. SaS sets the optimal V_{MPP} to the PEH adiabatically, which infers a lossless operation. However, in real applications the SaS efficiency largely depends on the efficiency of the inductor-based voltage converter. When the SaS voltage becomes high, it is more challenging to achieve high efficiency due to the large conversion ratio.
3. The proposed SaS circuit can only improve power extraction in the 'electrical domain' shown in Fig. 2.2. However, the overall power delivered by the PEH is often limited by the electromechanical coupling inside the PEH. For example, if the vibration frequency is off from the PEH resonant frequency, its output power will decrease dramatically regardless of using SaS or FBR.

The first limitation mentioned above can be improved by using a process with higher voltage limit. For example, in Chapter 3 and 4 we introduce a HVBCD process that has ~70V voltage limit, which is sufficient for SaS to achieve a fully trackable V_{MPP} under any vibrations.

The second and third limitation are more complex and cannot be solved by using different process. In future work, the voltage converter must be carefully optimized, so that it has high enough efficiency to support the operation of SaS. Since it is generally challenging to achieve a >90% efficiency in μW-level voltage conversion, SaS may not prefer to set the highest possible voltage on PEH due to the large conversion loss. Instead, SaS may use a smaller V_P, sacrificing a portion of harvestable energy but saves the power loss significantly.

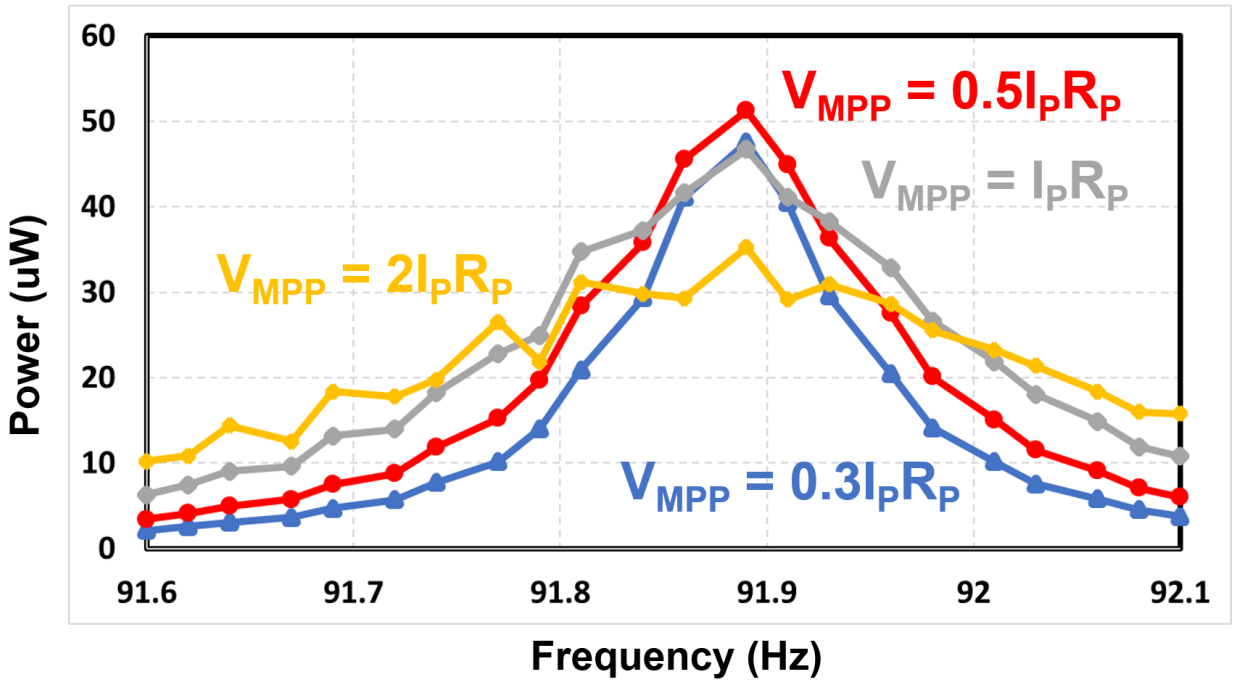


Figure 5.1: Power extraction from the PEH with different V_{MPP} ratio.

The last limitation refers to an interesting topic on wide-band PEHs. A conventional PEH has a steep frequency response as a result of its high-Q, so the electromechanical coupling has a very narrow band, usually within a few Hz. However, the environmental vibrations are usually wide-banded, so it is more important to maintain a high efficiency over a frequency range rather than just achieving the highest efficiency at the resonant frequency. Fig. 2.12 shows that V_{MPP} = ½ I_PR_P achieves the highest PEH power extraction at resonance frequency, but maintaining V_{MPP} = I_PR_P or even $2I_PR_P$ will produce a better off-resonant energy extraction. In addition, when the vibration is off-resonance, it is also possible to induce a phase shift between the V_{MPP} and vibration input to improve the output power. This can be achieved in future SaS implementations by using a digital processing circuit to compare the vibration frequency and the PEH resonant frequency, and automatically achieves the highest possible energy harvesting across the target bandwidth.

5.2.2 High-Voltage Biasing Technique for MEMS Capacitive Accelerometers

The high voltage bias technique eliminates the need for signal chopping at the MEMS bias nodes (AS1, AS2). However, it is also not capable of chopping due to the potential high switching loss, resulting in a pure AC sensing scheme that cannot measure DC accelerations. While this is acceptable for most motion-detection applications, it also limits the proposed accelerometer scheme in certain conditions such as measuring very-slow accelerations.

A second issue with the current implementation is that we determines a fixed value ΔV_B for each accelerometer, regardless of the actual V_{B+}/V_{B-} voltage. However, from Equation (3.18) we know that the electrostatic mismatch is proportional to both ΔV_B and V_{B+}/V_{B-}, so when the bias voltage changes, the same ΔV_B will result in a varying electrostatic mismatch and may cause unexpected MEMS behaviors.

For the first problem, although the proposed accelerometer can only sense AC accelerations, in future works we can define its high-pass corner to be very low (sub-Hz or even mHz) and guarantees the coverage on slow motions. This will require the implementation of ultra-high impedance in the amplifier chain, and extra design efforts to mitigate the flicker noise that dominates in low frequency domain. The second problem can be solved by designing a digital processing unit that monitors V_{B+}/V_{B-} and dynamically changes ΔV_B for a constant electrostatic mismatch. The ΔV_B value can also be tuned with different acceleration amplitudes, further trading-off the MEMS sensitivity with sufficient MEMS dynamic range.

5.2.3 Hardware Design for Future Generations of Programmable Matter

One big challenge in HVGM is the implementation of negative HV-MUXs. Due to the physical layers in this process, it is not possible to implement an N-to-1 mux for the negative voltages so its output remains un-programmable. Furthermore, the positive and negative electrodes

cannot swap their polarities due to similar reasons. This greatly limits the functionalities of HVGM in a PM system.

The second issue is that the charge/discharge operation in HVGM is non-adiabatic. This means that the energy been used for latching/actuation is not recycled, thus limiting the maximum actuation speed of Catoms within the certain power budget.

Another challenge for HVGMv2 lies in its capacitive communication. The single-channel coupling capacitor results in a one-way communication that Catom 1 can only send message to Catom 2, but never receives response from Catom 2 unless we utilize a time-division multiplexing (TDM) protocol. This is acceptable for the early stage PM, but eventually we will need duplex communication when there are large numbers of Catoms in the system.

To address the limitations discussed above, we can design and fabricate HVGM in an SOI process, where the physical layers are better isolated so we can implement the negative HV-MUXs without restrictions. The second issue could be improved by storing the discharged electrode energy into a capacitor/inductor, and later use it to re-charge the electrode to achieve a semi-adiabatic operation.

The duplex communication problem can be addressed by utilizing existing differential electrodes. In HVGMv2 that only supports uplink communication, Rx always sends out message with the negative electrode, and Tx gets the message with the positive electrode. But for each Catom phase, there is another +/- electrode pair that is idle now, but could be utilized in future implementation for downline communication (e.g., acknowledgement from Catom 2 to Catom 1). the target bandwidth.

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