# Investigation of p-type Oxide Semiconductor Thin Film Transistors for Complementary Metal Oxide Semiconductor Technologies

by

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical and Computer Engineering)
in the University of Michigan
2023

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*To my parents.*

*Thank you for everything.*

**Acknowledgements**

First and foremost, I would like to express my deepest gratitude to my research advisor, Professor Rebecca L. (Becky) Peterson, for her invaluable advice, continuous support, and patience during my PhD study in the University of Michigan. Without her guidance and support, I might have not been on the right track during this challenging journey. In addition, her precision in research gave me a chance to learn how to perform the research logically and systematically as well as how to think critically. She was not just an amazing advisor in research but also a great mentor in life for me. I again appreciate her willingness to help students in various aspects.

I would like to extend my sincere thanks to my doctoral committee, Prof. Neil Dasgupta, Prof. Emmanouil (Manos) Kioupakis, and Prof. Elaheh Ahmadi, for their willingness to serve on my committee and for their insightful feedback on research.

I also want to thank my master's research advisor at the University of Seoul, Prof. Changhwan Shin, for encouraging me to pursue graduate school and for the support.

I would like to thank all the PetersonLab group members, both current and former. It has been a pleasure working with them and discussing with my colleagues. In addition, I would like to thank all of my friends I met in University of Michigan for their emotional support.

I acknowledge the financial support from the Intel Corporation through a PMOS Intel Strategic Research Alliance (ISRA). I thank Intel Components Research for the fruitful discussion and their comments. I also thank the Department of Electrical Engineering and Computer Science (EECS) at the University of Michigan for their financial support. I am also thankful for all the

technical assistance from the staff of Department of EECS, Lurie Nanofabrication, and Department of Materials Science and Engineering. Working with them has been a great experience and have enabled me to finish this thesis.

Last but not least, I many thank my parents, Hyunwook Jo and Myungja Ahn, and my brother, Jaedeok Jo, for their unconditional support and encouragement. I always appreciate it.

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## Abstract

Today we are living through the fourth industrial revolution with new innovative technologies such as artificial intelligence, internet of things, autonomous robots, and other technologies. With the advent of these new technologies, the development of hardware needed to support them becomes ever more important. It requires not only the continuous advancement of conventional Si-based computing technology but also the flexibility to support novel technologies. To enable the continuous development of hardware technology, thin film electronics – especially, thin film transistors or TFTs – that are characterized by large area deposition, low temperature processing, as well as low complexity and cost are being actively investigated. Oxide semiconductors are a promising material for these TFT applications. Their unique properties such as wide bandgap, which leads to low leakage current, high breakdown voltage, and optical transparency, enable them to be used in new application areas. While n-type oxide semiconductors have been commercialized in display backplanes and are a quite mature technology, the absence of p-type oxide semiconductor TFTs with performance equivalent to n-type TFTs limits the further development of oxide semiconductor technology. Cuprous oxide ($Cu_2O$) is a well-known p-type oxide with high mobility up to 100 $cm^2V^{-1}s^{-1}$ and wide bandgap of ~2.6 eV. Building on this context, in this thesis p-type $Cu_2O$ thin film transistors were investigated for complementary metal-oxide semiconductor device technologies.

In general, TFT performance can be improved by reducing the TFT non-idealities and making the thin film itself have high mobility. Using RF-sputtered $Cu_2O$, I first investigated device-level issues to understand what limits device performance. The $Cu_2O$ TFT performance

was limited by high contact resistance and high interface traps/bulk defects. Second, to increase the mobility of the $Cu_2O$ thin film itself, the hole scattering mechanisms were studied. I found that in polycrystalline $Cu_2O$ thin films, the hole mobility is mainly limited by neutral impurity and grain boundary scattering. Third, since process temperature is an important factor in determining the film's electrical properties, I studied the effect of various $Cu_2O$ thin film processes on the electrical properties, given a constrained thermal budget.

Finally, since the Hall mobility of the $Cu_2O$ thin film is already ~10 $cm^2V^{-1}s^{-1}$ while field effect mobility is << 1 $cm^2V^{-1}s^{-1}$, I proposed methods to address the device issues identified earlier. To reduce the ohmic contact resistance to p-type $Cu_2O$, a nitrogen-doped $Cu_2O$ source/drain interlayer was introduced. Since nitrogen is a p-type dopant in $Cu_2O$, the addition of this layer alleviates Fermi-level pinning. In addition, dielectric engineering was performed to evaluate the interface trap density with high-*k* dielectrics, using both bottom gate and top gate TFT architectures. Furthermore, the effect of passivation of the $Cu_2O$ TFT on back-channel defects and device stability was investigated.

# Chapter 1 Introduction

## 1.1 Past, current, and future of computing technology

Today we are living in the era of the fourth industrial revolution, called Industry 4.0 [1]. It is characterized by artificial intelligence (AI), internet of things (IoT), autonomous robots, augmented/virtual reality, big data, 3D printing, and other technologies. These technologies enable cyber-physical systems by blurring the boundaries between the physical and digital worlds. Different from the first, second, and third industrial revolutions, which were characterized by a certain technology such as steam power, electricity, and computers/the internet, the fourth industrial revolution is based on the achievements of the previous industrial revolutions. It is especially based on the third industrial revolution, i.e., the computer or digital revolution. The computer revolution, which started in the 1960s, was enabled by the continuous successful "miniaturization" of transistors. Today, the world is radically changing through use of varied technologies that require continuous advances in semiconductor technology. Functional diversification in hardware technology to support these innovative technologies is becoming more and more important in this era.

Computing technology using complementary metal-oxide-semiconductor (CMOS) logic has dramatically grown over many decades since the early 1960s. By adhering to the oft-quoted scaling "rule" called Moore's law, the silicon industry advanced to successfully demonstrate transistors with feature sizes below 100 nm by 2003. However, since that time, the transistor scaling mechanisms that have enabled this exponential increase in the number of transistors per

chip have started to confront difficulties, as transistor dimensions approach the few-nanometer scale. Due to these physical limits, the scaling strategy was changed from conventional geometrical scaling to equivalent scaling by introducing innovative technologies such as strain [2], high-*k*/metal-gate [3], and FinFET [4]. Although today the semiconductor industry has reached sub-10 nm technology nodes [5], scaling has slowed down due to increasing process complexity and cost. Thanks to the introduction of extreme ultraviolet (EUV) lithography, semiconductor industry is anticipated to be able to carry on scaling for a few more generations. Nonetheless, it is predicted that in the near future the continued down-scaling of silicon-based transistors will be no longer possible due to quantum effects [6].

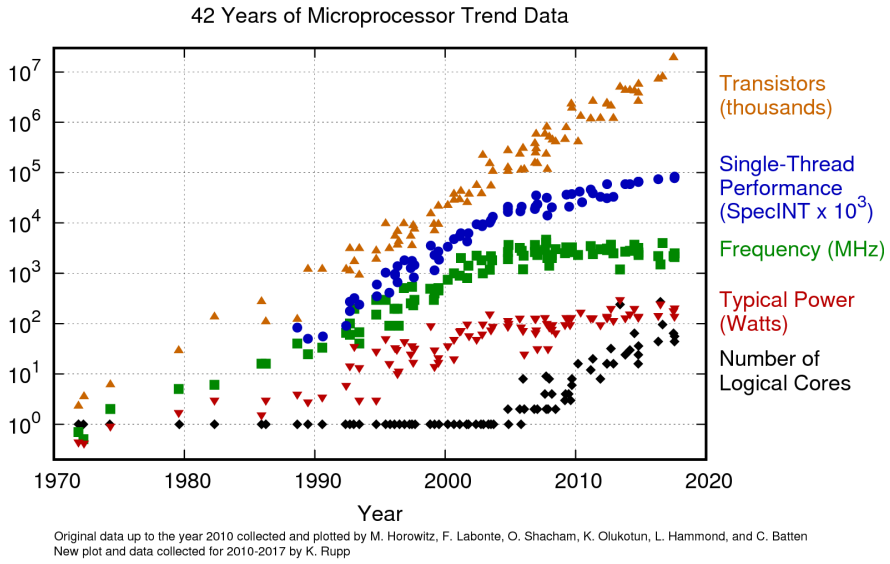



*Figure 1.1 Silicon microprocessor trend data. Adapted from [7].*

In addition, ever-increasing power density (Figure 1.1) is a critical issue in modern integrated circuits (ICs). As two-dimensional scaling approaches the physical limit, the incommensurate scaling of the power supply voltage ($V_{DD}$) has become a critical issue. Until the early-2000s, constant field scaling [8] enabled transistors to continuously improve their switching speed, allowing microprocessors to operate at higher and higher frequencies. This led to the

improvement of IC performance by enabling an increase in the number of computing steps performed in a certain amount of time. However, MOS transistors require a certain minimum change in gate voltage to increase the source-to-channel current by a factor of 10 due to the Boltzmann distribution of electrons at source/drain [9]: the subthreshold slope of the transistor cannot be lower than 60 mV·dec$^{-1}$ at 300K. Due to the Boltzmann limit, $V_{DD}$ could no longer by scaled linearly as dimensions were scaled down. This resulted in a dramatic increase in power density and associated self-heating. Constant-$V_{DD}$ scaling also made it difficult to continue increasing the operating frequency of new technology nodes. To control the power density and the corresponding heat emission, the operating frequency of CMOS has been stuck at a few GHz since the mid-2000s. This has limited the further performance improvement of the microprocessor, pushing vendors to adopt multi-core systems, instead of single core, to compensate for this frequency limitation.

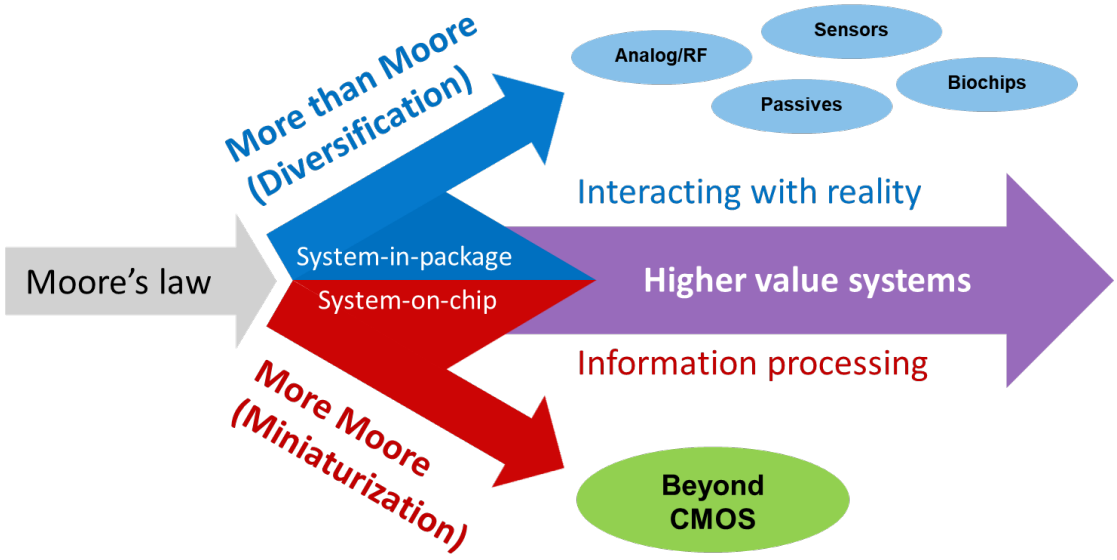



*Figure 1.2 International roadmap for devices and systems (IRDS): More Moore and More than Moore. Adapted from [10]*

As Moore's law reaches its twilight, the semiconductor industry has adopted two forward-looking strategies (Figure 1.2): "More Moore" and "More than Moore" [10]. The term "More Moore" focuses on continuous miniaturization with novel device architectures such as nanowire and nanosheet. Its goal is the continuous improvement of CMOS-based system-on-chip (SoC) technology. Beyond-CMOS devices and systems are also being actively explored for the future. Here, the idea is to exploit new concepts based on novel materials and physics to solve the fundamental issues described above. Such novel approaches include beyond-Boltzmann/steep-slope devices (with subthreshold slope < 60 $mV \cdot dec^{-1}$) such as negative capacitance FET [11] and tunnel FET [12], as well as beyond-von Neumann systems such as neuromorphic computing [13] and quantum computing [14].

The second strategy is "More than Moore", which implies the addition of non-CMOS-based technologies to CMOS-based technologies in order to achieve functional diversification [10]. Such non-digital functionalities could include RF communication, power control, passive components, and sensors. This is based on die-level integration, e.g. system-in-package (SiP), which means placing multiple dice with different functionalities in a single package. Since it is hard to encompass multiple functionalities at the wafer level, SoC and SiP technologies can be complementary to each other, while at the same time each technology can continue to evolve independently. To support this new approach, the International Technology Roadmap for Semiconductors (ITRS) [15], which has guided the semiconductor industry for many years, evolved in 2016 to become the International Roadmap for Devices and Systems (IRDS) [10] by expanding the focus from the individual device to the system. In line with Industry 4.0, the expanded approach of adding new functionalities to conventional digital devices is expected to support emerging technologies to connect the digital and physical worlds.

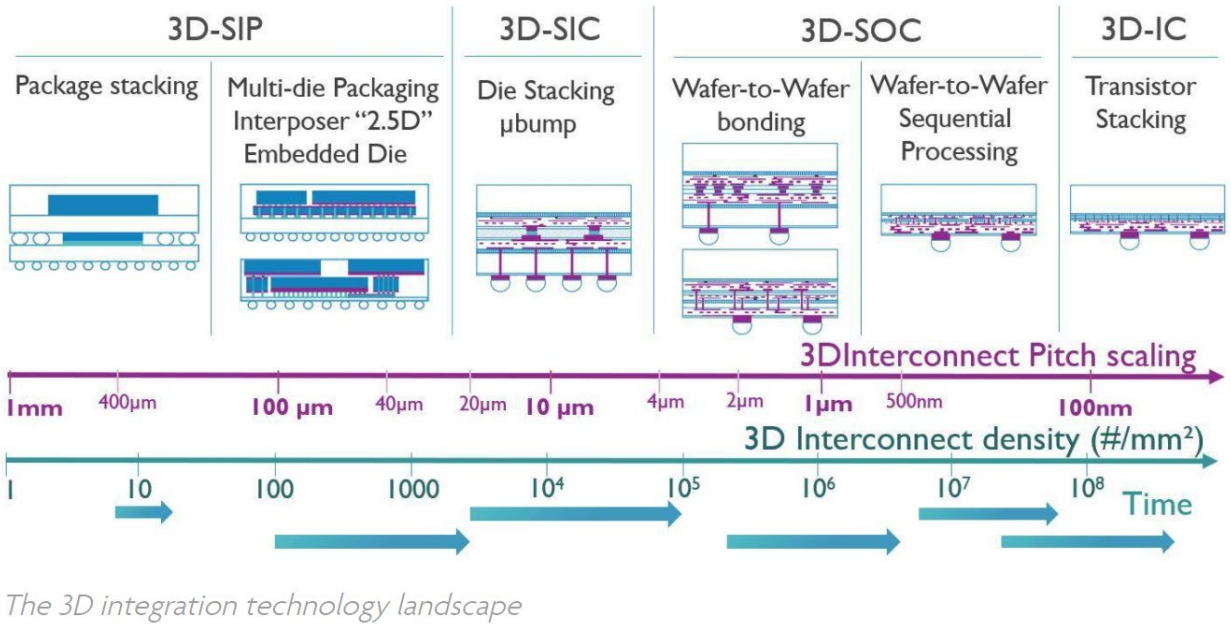



*Figure 1.3 The 3D integration technology landscape. Adapted from [16].*

Three-dimensional (3D) heterogeneous integration is the key to effectively combine non-digital devices with digital components. Diverse approaches (Figure 1.3) to combine these functionalities with digital components are being explored, ranging from package-level and wafer-level integration, to monolithic 3D integration (3D-IC) [17]. These 3D technologies have the ability to reduce interconnect resistance and parasitic capacitance to achieve high speed and low power. For 3D-SiP, package-on-package (PoP) is a common method to achieve system-level miniaturization. At the early stages in developing these 3D technologies, functional diversification was achieved by vertical package stacking using wire bonding. In addition, technologies for integrating multiple dice in a single package using an interposer, known as 2.5D integration, was also developed. As through-Si vias (TSV) and micro-bump technology become mature, 3D integration technologies are moving toward stacked-IC (3D-SIC) and 3D-SoC. In addition, wafer-to-wafer bonding or sequential process (i.e., transferring a BEOL semiconductor layer onto an already-patterned wafer) enables 3D integration with high interconnect density. Today 3D

integration research is starting to move toward monolithic 3D integration (3D-IC). Although these technologies are still at the research stage, diverse attempts to demonstrate 3D-ICs have been made using a wafer without additional process (e.g., bonding, thinning, and TSV). Although additional restrictions (e.g., process temperature limits) exist for back-end-of-line (BEOL) processes to protect front-end-of-line devices and the metal interconnect underneath the BEOL devices, 3D-IC is anticipated to enable continuous improvement in microprocessor performance and diverse functional integration.

### 1.2 Motivation for oxide-semiconductor thin film electronics

Thin film electronics, especially the thin film transistor (TFT), is a promising technology to support Industry 4.0 devices from IoT to wearable applications [18]. When compared to the traditional CMOS ICs, TFT technology is suitable for being fabricated on large area substrates at low cost, with low process complexity, and with low process temperature. The low thermal budget is key factor that enables flexible, foldable, and stretchable electronics by allowing the use of diverse substrates, as well as BEOL device fabrication for monolithic 3D integration. Many circuits based on thin film technology already have been demonstrated, ranging from near-field communication tags [19] and analog-to-digital converters [20], to flexible microprocessors [21]. These show the possibilities of TFT-based electronics. Today mainstream materials [22] that support TFT technology are amorphous silicon (a-Si), low-temperature polysilicon (LTPS), and amorphous oxide semiconductors, especially, amorphous indium-gallium-zinc-oxide (a-IGZO). Furthermore, novel materials such as carbon nanotubes [23] and 2D materials [24] are also being investigated for future flexible electronics.

Oxide semiconductors, that is, metal oxides, offer many advantages for thin film transistors. They can be realized using low temperature processing, can be fabricated on large area substrates, and have good mobility of 1 – 20 $cm^2V^{-1}s^{-1}$ [22]. The conduction band of n-type oxides is formed by overlapped *s*-orbitals, which enables high electron mobility even when the film is amorphous in structure [25]. This feature makes these materials favorable for large area deposition with good uniformity. These advantages have enabled the growth of the display industry using a n-type oxide semiconductor, a-IGZO, in the display backplane [22]. Furthermore, the wide bandgap property of amorphous n-type oxides, with optical transparency, high breakdown voltage, and low leakage current have allowed researchers to explore new application areas, ranging from transparent electronics to BEOL memory/power control applications [9], [26]. However, currently oxide semiconductor technology relies on n-type unipolar devices, due to lack of high-performance p-type oxide semiconductors. The absence of p-type thin film semiconductors with performance similar to that of the n-type materials is the one of the biggest obstacles that limit the further development of thin film semiconductor technology.

### 1.3 Opportunities in p-type oxide semiconductor thin film transistors

Development of p-type oxide semiconductor TFTs [27] that perform as well their n-type counterparts could unambiguously enable a significant advance in oxide technology. It would enable oxide semiconductor technology to demonstrate more efficient and complex circuits [28], building on the long history of Si CMOS technology, as well as to find new application areas. While conduction band formation is favorable due to the overlapped *s*-orbitals, the formation of the valence band maximum (VBM) is fundamentally difficult due to the localized oxygen *p* orbital. This causes most p-type oxides to have a flat VBM with a large hole effective mass and low hole

mobility. For example, while indium oxide ($In_2O_3$), a common n-type oxide [29], has an electron effective mass of ~0.3$m_0$, its hole effective mass is ~38$m_0$. This discrepancy illustrates the challenges in realizing p-type oxides [30]. Although there have been enormous efforts to achieve p-type doping with well-known n-type oxides such as zinc oxide (ZnO) and $In_2O_3$, there has not been any significant success [30]. To achieve high mobility p-type oxides, a chemical design concept to alleviate VBM localization was proposed in 1997 [31]. The chemical design concept and following study [32] showed that using metal cations with occupied *d* or *s* states near the VBM can effectively improve hybridization with oxygen 2*p*. Using these guidelines, many researchers have worked to demonstrate p-type oxides.

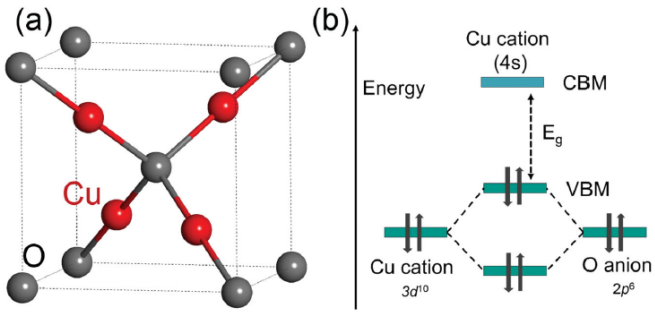



*Figure 1.4 (a) $Cu_2O$ crystal structure and (b) schematic illustration of valence band formation in $Cu_2O$. © 2016 John Wiley & Sons, Inc. Reprinted, with permission, from [33].*

Today Cu-based oxides and Sn-based oxides are the most well-known p-type oxides [27], [30], [33]. Binary copper oxide, specifically cuprous oxide ($Cu_2O$), has been extensively explored due to its special orbital structure (Figure 1.4). Since the energy level of the copper cation with closed shell configuration (*i.e.*, $d^{10}s^0$) is similar to that of the oxygen anion, it is favorable to form the valence band due to hybridization between the O 2*p* orbitals and the closed shell Cu $3d^{10}$ orbitals, thereby enabling a reasonably high hole mobility. In addition, to improve the optical transparency, Cu-based ternary oxides with delafossite structure, which have the form of $CuMO_2$

(where M = Al [31], Ga [34], In [35], etc.), also have been studied. Another promising p-type option is thin monoxide (SnO) with a pseudo-closed $ns^2$ orbital of the metal cation, in which the valence band maximum is formed by hybridization of the Sn 5*s* and oxygen 2*p* orbitals. The strong interaction between the cation *s* orbitals, which are spatially more extended than *d* orbitals, with oxygen 2*p* orbitals [30], [36], [37] enables SnO to have a relatively low effective hole mass. Furthermore, to achieve even stronger hybridization of VBM, there have been attempts to use chalcogens such as S, Se, and Te to replace oxygen in both Cu- and Sn-based oxides [38]–[40]. In addition, other p-type oxides [30] such as spinel oxides, Cr-based oxides, and nickel oxide (NiO) also have been studied, and there are ongoing efforts to identify promising p-type oxides using advanced computational methods [41]. Among the p-type options, $Cu_2O$ has a record high mobility of > 100 $cm^2V^{-1}s^{-1}$ [42] with low effective hole mass = $0.58m_0$ [43] (Table 1.1). Due to these excellent electrical properties, there have long been efforts to explore the use of $Cu_2O$ in high performance TFTs [33] and solar cells [44], [45].

*Table 1.1 Comparison of p-type oxides, from ref. [30], [33]*

| Material Properties | $Cu_2O$ | SnO | NiO |
|---|---|---|---|
| Effective mass, $m^*$ ($m_0$) | 0.58 | 2.05 | - |
| Band gap, $E_g$ (eV) | 2.1 – 2.6 | 0.7 | 3.6 – 4.0 |
| Reported Hole mobility, $\mu_p$ ($cm^2V^{-1}s^{-1}$) | Up to > 100 | Up to ~19 (Typically, 1–5) | Up to > ~29 |

To demonstrate high performance p-type oxide semiconductor thin film transistors, there are two strategies. One is choosing a high mobility p-type oxide. For TFT applications, transparency is not always required (*e.g.*, BEOL devices on Si MOSFET). It was observed that, although materials with the $CuMO_2$ structure can have a larger bandgap and thus better transparency, they also tend to have a larger hole effective mass and thus lower hole mobility than

$Cu_2O$ [30]. In addition, in contrast with transparent conducting oxides that require high carrier concentration to achieve low resistivity, a high carrier concentration is detrimental for TFT applications since it hinders on/off switching. Thus, I focus on materials with high hole mobility and non-degenerate carrier concentrations, over materials with wideband optical transparency. The second, complementary strategy is to address device issues to enable the TFT field effect mobility to be close as possible to the intrinsic hole mobility.

Since $Cu_2O$ exhibits a high intrinsic mobility with a hole carrier concentration of $\sim 10^{15}$ $cm^{-3}$ [44], it satisfies the first condition. However, there remain several challenges to using $Cu_2O$ in p-type TFTs. First, the reported field effect mobility in TFTs is typically much lower than the Hall mobility. Second, a wide range of mobility values for p-type $Cu_2O$ thin film have been reported. In many cases, the reported mobility was lower than the theoretically-estimated mobility value. Third, the $Cu_2O$ mobility has been observed to be strongly influenced by the process temperature. Therefore, to utilize the intrinsic advantages of $Cu_2O$, a fundamental understanding is needed of the factors limiting both the Hall mobility (which represents the maximum achievable performance) as well as the field effect mobility that can be practically achieved in TFTs.

## 1.4 Thesis Objectives

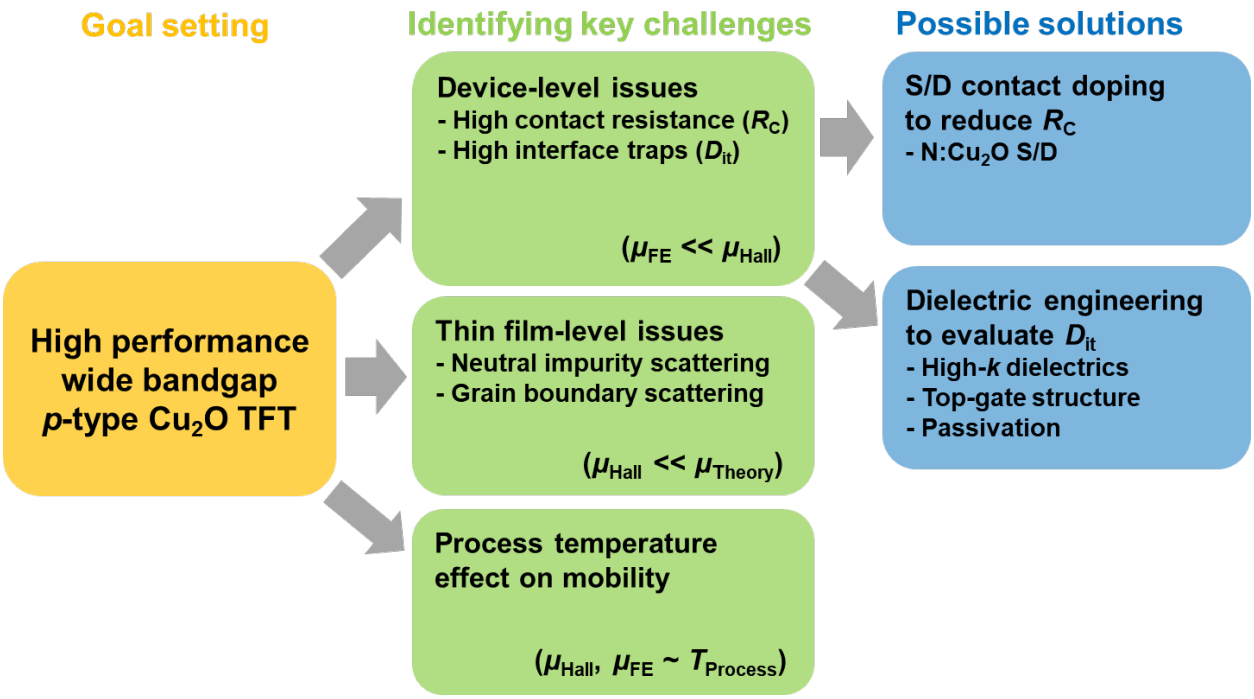



*Figure 1.5 Thesis objective and overview*

The overarching objectives of this thesis (Figure 1.5) are to make advances in p-type $Cu_2O$ thin film semiconductors and identify the key challenges that limit TFT performance, in order to ultimately achieve high performance p-type TFTs. The p-type $Cu_2O$ layers are fabricated using RF magnetron sputtering. First, I investigate device-level methods to reduce the mobility gap between field effect mobility ($\mu_{FE}$) and Hall mobility ($\mu_{Hall}$). To address this, I focus on comprehensive studies of contact resistance and interface traps in $Cu_2O$ thin film transistors. Second, I seek to understand why the measured Hall mobility is less than the theoretically-predicted hole mobility. I perform temperature-dependent Hall measurements to investigate and compare hole scattering mechanisms in $Cu_2O$ thin film and bulk substrates, and compare the results with first-principles theory performed by a collaborator. Third, I explore the effect of process temperature on $\mu_{FE}$ and

$\mu_{Hall}$. $Cu_2O$ TFTs with various process temperatures and conditions were investigated to correlate the thermal budgets and electrical properties.

Based on these studies, I identify several possible solutions to improve $Cu_2O$ TFT performance. My analysis shows that device-level problems are the most critical since the $\mu_{Hall}$ of my thin films is already $\geq 10$ $cm^2V^{-1}s^{-1}$. To reduce the high contact resistance and reduce the number of interface traps in my p-type $Cu_2O$ TFTs, I pursue two novel approaches: (1) the insertion of a nitrogen-doped $Cu_2O$ between the source/drain metal and the $Cu_2O$ semiconductor to reduce contact resistance, since my collaborator has predicted that nitrogen-doping can increase the hole concentration in $Cu_2O$; and (2) the modification of the dielectric/semiconductor interface at both the front and back channel to address interface trap issues.

### 1.5 Thesis Overview

In Chapter 2, I demonstrate deposition of p-type $Cu_2O$ thin films using RF magnetron sputtering. Thin film properties were investigated using diverse techniques such as electron beam and X-ray diffraction. P-type $Cu_2O$ thin film transistors were fabricated. Then, to understand the mobility gap between the field effect mobility and Hall mobility of $Cu_2O$, device characterization was performed to analyze the impact of contact resistance and interface traps on TFT performance. In Chapter 3, I investigate hole scattering mechanisms by performing temperature-dependent Hall measurements on my RF-sputtered polycrystalline $Cu_2O$ thin film and compare with a naturally-formed single crystalline bulk $Cu_2O$ substrate. To understand why the Hall mobility is lower than the theoretically-predicted value, my measured hole mobility in $Cu_2O$ was compared to analytical models of phonon, grain boundary, ionized impurity, and neutral impurity scattering, and compared to the results to first-principles theory performed by my collaborator. In Chapter 4, I

explore the effects of process temperature on $Cu_2O$ thin films and their TFT performance. The required thermal budgets are different for the diverse applications. Since the process temperature is a critical factor that determines TFT performance, the material, electrical, and optical properties were investigated for $Cu_2O$ thin films processed at room temperature, 400°C, and 600°C. In Chapter 5, building on my collaborator's prediction of degenerate doping of $Cu_2O$ using nitrogen, I develop a deposition process for nitrogen-doped $Cu_2O$ (N:$Cu_2O$) and characterize the films. By using a heavily-doped N:$Cu_2O$ S/D interlayer, I reduce the contact resistance of my p-type $Cu_2O$ thin film transistors. In Chapter 6, I explore high-*k* dielectric to alleviate the high trap density at the dielectric-to-channel interface of $Cu_2O$ TFTs. A $HfO_2$ dielectric layer was tested as a gate dielectric in both the bottom-gate and top-gate TFT structures. In addition, a high-*k* passivation layer was introduced to the $Cu_2O$ TFT to understand its effect on back-channel defects. The thesis concludes with Chapter 7, which summarizes the contributions to date and recommends future research directions.

# Chapter 2 Causes of the Difference between Hall mobility and Field Effect Mobility for p-type RF Sputtered $Cu_2O$ Thin Film Transistors

## 2.1 Introduction

With the successful development of n-type oxide semiconductor thin film transistors (TFTs), many researchers are extensively exploring their counterpart, p-type TFTs, for complementary metal oxide semiconductor (CMOS)-based applications [27], [33], [46]. CMOS integrated circuits (ICs) have many advantages over unipolar (i.e., n-type only) circuits. Their merits include lower power consumption and heat dissipation, reduced circuit complexity, as well as increased immunity to noise [47]. In addition, the development of p-type oxide semiconductors will enable oxide semiconductor technology for new applications beyond commercial display backplanes [48], such as flexible/foldable electronics and back-end-of-line devices on Si-based ICs [49], [9], [50]–[52], [42], [53]–[61].

Cuprous oxide ($Cu_2O$) has p-type properties that originate primarily from Cu simple vacancies acting as acceptors [62]–[64], and its Cu 3*d* orbital can favorably form a delocalized valence band maximum with the O 2*p* orbital because they have comparable energy levels [31], [33]. Furthermore, the abundant availability, low price, non-toxic nature, and direct band gap (2.1 – 2.6 eV [33], [65], [66]) of $Cu_2O$ are desirable. With these advantages, $Cu_2O$ has been explored using diverse deposition methods [33]. In particular, dc/RF magnetron sputtering is considered to be one of the most promising thin-film deposition methods, since its cost-effective process and its capability for large area deposition make it suitable for manufacturing.

Previous studies have confirmed the p-type properties and TFT performance of $Cu_2O$ deposited by sputtering [54]–[57], [67]. It has been observed that there is a huge difference between a film's Hall mobility ($\mu_{Hall}$) and the field effect mobility ($\mu_{FE}$) achieved within a TFT. For example, while $\mu_{Hall}$ values ranged from 16 to 256 $cm^2V^{-1}s^{-1}$ for poly-crystalline films [54]–[56], [68]–[70], $\mu_{FE}$ values ranged from 0.0023 to 0.54 $cm^2V^{-1}s^{-1}$ [54]–[56], [67] for poly-crystalline films and $\mu_{FE}$ = 2.4 $cm^2V^{-1}s^{-1}$ for nano-crystalline film [57]—much lower than the values of $\mu_{Hall}$. Films deposited by other methods, such as pulsed laser deposition and atomic layer deposition [33], [42], [58], have reported $\mu_{FE} > 1$ $cm^2V^{-1}s^{-1}$. However, the $\mu_{FE}$ values are still much lower than the reported $\mu_{Hall}$ values. To address this fundamental knowledge gap, I performed a comprehensive study to determine the factors that limit the $\mu_{FE}$ values achieved in p-type $Cu_2O$ TFTs.

In this chapter, using copper oxide films of different thicknesses, I correlate the $CuO_x$ material properties with electrical characteristics. With electrical measurements, I analyzed the factors that can cause a gap between $\mu_{Hall}$ and $\mu_{FE}$ in $Cu_2O$ TFTs. I determined that the dominant limiting factors in the TFTs are dielectric-semiconductor interface traps ($D_{it}$) and contact resistance ($R_C$), both of which can be improved in the future to achieve high-performance p-type $Cu_2O$ TFTs. Note that I have published the results described in this chapter (except for section 2.3.4) in reference [71].

## 2.2 Experimental Methods

To fabricate p-type copper oxide ($CuO_x$) TFTs with different film thicknesses, a 100-nm $SiO_2$ layer was thermally grown on a heavily-doped Si wafer in a furnace. Then, using RF magnetron sputtering (RFMS), $CuO_x$ was deposited on top of the $SiO_2$/Si. For the RFMS process, a 3-inch Cu (99.99%) metal target was used in a Kurt J. Lesker PRO Line PVD 75 with a target-to-substrate distance of ~16 cm. The deposition conditions were as follows: RF power of 300 W, process pressure of $5 \times 10^{-3}$ Torr, $O_2$:Ar ratio of 0.2 ($O_2$ = 5.35 sccm and Ar = 26.75 sccm), and deposition at room temperature with deposition times of 20 s, 39 s, 79 s, and 158 s. Following thin film deposition, a post-deposition anneal (PDA) was performed at 600 ℃ in vacuum (~$1 \times 10^{-5}$ Torr) for 10 mins. After PDA, ellipsometry measurements showed that the film thicknesses were approximately 10 nm, 20 nm, 40 nm, and 80 nm. To form active layer islands, the $CuO_x$ films were patterned via photolithography and wet etching. Before contact formation, an $O_2$ plasma descum process was performed. To form source/drain contacts, 20 nm Ni followed by 80 nm Au were deposited and patterned using an e-beam evaporator and photolithography. In addition to TFTs, sheet resistance ($R_{sh}$) patterns (cloverleaf shape) were made for van der Pauw (*vdP*) measurement and transmission line method (TLM) test structures were included to extract contact resistance [72]. These test structures were fabricated at the same time as the TFTs, on the same samples. For Hall measurements, a separate sample was fabricated using the same process on a glass substrate, using the *vdP* configuration (cloverleaf pattern).

Metal-oxide-semiconductor capacitors (MOSCAPs) were also fabricated with the $CuO_x$ films. First, 100 nm Mo was deposited on glass wafers by RFMS. Next, a 120-nm $SiO_2$ layer was deposited by plasma-enhanced chemical vapor deposition at 200 ℃, followed by rapid thermal

annealing at 520 °C for 3 min to densify the $SiO_2$. Then, $CuO_x$ film deposition and Ni/Au contact formation were performed using the processes described above.

Material properties of the $CuO_x$ films were investigated by grazing incidence X-Ray diffraction (GIXRD), X-ray absorption near-edge structure (XANES) analysis, scanning electron microscopy (SEM), transmission electron microscopy (TEM), high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), energy dispersive X-ray spectroscopy (EDS), and conductive atomic force microscopy (C-AFM).[1] For the XANES analysis, Cu(I) and Cu(II) fractions were obtained from X-ray absorption spectroscopy (XAS) at the copper K-edge. The spectra were fit by linear combination fitting method (R-factor < 0.0007 and Chi-squared < 0.022) using the XAS Athena software [73].[2] For electrical measurements, an HP4156A semiconductor parameter analyzer, an HP4284A LCR meter, and an Accent HL5500PC Hall measurement system were used in air, at room temperature, in the dark.

[1] C-AFM was performed by EAG Labs, and Dr. Adedapo A. Oni at Intel (the sponsor of this work) performed transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDS).

[2] The XANES data and analysis were performed by my collaborator, Julia D. Lenef, a doctoral student at UM in Materials Science and Engineering working with Prof. Neil Dasgupta. The XANES data was taken at the Advanced Photon Source, a U.S. Department of Energy (DOE) facility using beamline 20-ID-B, C at Argonne National Laboratory, proposal ID 66474. We thank Dr. David Mandia at ANL for his assistance with XANES.

## 2.3 Results and Discussion

### *2.3.1 Material properties of RF-sputtered $CuO_x$ thin films*

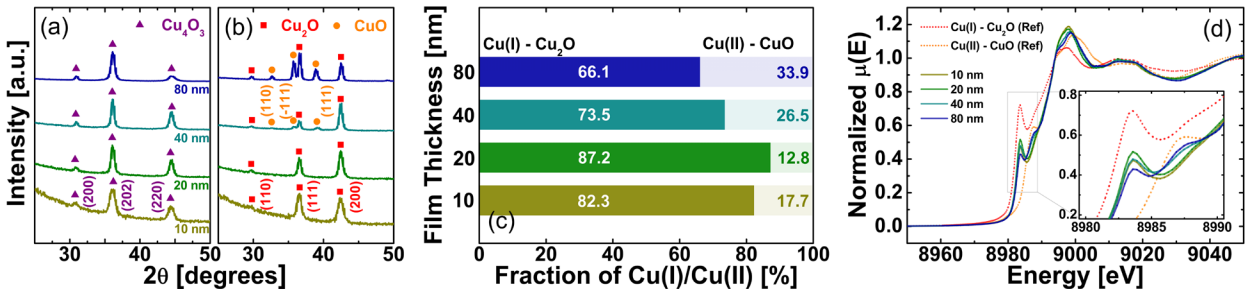



*Figure 2.1 GIXRD data for (a) as-deposited films and (b) films after post-deposition annealing (PDA), for films with different thickness: 10 nm, 20 nm, 40 nm, and 80 nm. (c) Fractions of Cu(I) and Cu(II) obtained from XANES data shown in (d), for films after PDA. The dotted lines in (d) show XANES data from $Cu_2O$ and CuO powder references with Cu(I) and Cu(II) oxidation states, respectively. © 2020 IEEE. Reprinted, with permission, from [71].*

The film phase and composition of the post-annealed $CuO_x$ films with different thicknesses (*i.e.*, 10 nm, 20 nm, 40 nm, and 80 nm) were analyzed using GIXRD and XANES. As shown in Figure 2.1, different thickness films showed different $CuO_x$ phase after PDA at 600 °C in vacuum. As-deposited films all showed $Cu_4O_3$ phase, regardless of thickness (Figure 2.1(a)). After PDA, the phase transformed to $Cu_2O$ (10 and 20 nm films) or a $Cu_2O$ + CuO mixed phase (40 and 80 nm films) (Figure 2.1(b)). Specifically, GIXRD of the 40 nm film showed $Cu_2O$ peaks with minor CuO peaks while the 80 nm film showed $Cu_2O$ + CuO mixed phase peaks.

The Cu(I)/Cu(II) fraction of each film was also quantitatively evaluated (Figure 2.1(c)) by linear combination fitting within the XANES region (Figure 2.1(d)). The 20 nm film showed the highest Cu(I) fraction of 87.2%. As the film thickness increased to 80 nm, the Cu(I) fraction decreased from 87.2% to 66.1%, while the Cu(II) fraction increased from 12.8% to 33.9%. These trends are well matched with the GIXRD results. The difference in phase after PDA is likely due to the following reactions, as explained in a study on the copper oxide phase [74]: oxygen reduction,

i.e., 2 $Cu_4O_3$ → 4 $Cu_2O$ + $O_2$, and oxidation, i.e., 2 $Cu_4O_3$ + $O_2$ → 8 CuO. For thinner films (10–20 nm), during vacuum annealing, the $O_2$ released by $Cu_4O_3$ reduction may be able to entirely escape from the film, allowing a nearly complete reduction to the $Cu_2O$ phase. On the other hand, for thicker films (40–80 nm), $O_2$ may not be able to fully escape from the thick layer, causing oxidation of some of the $Cu_4O_3$ to CuO. These competing oxidation and reduction processes, combined with $O_2$ diffusion, may lead to the observed $Cu_2O$ + CuO mixed phase.

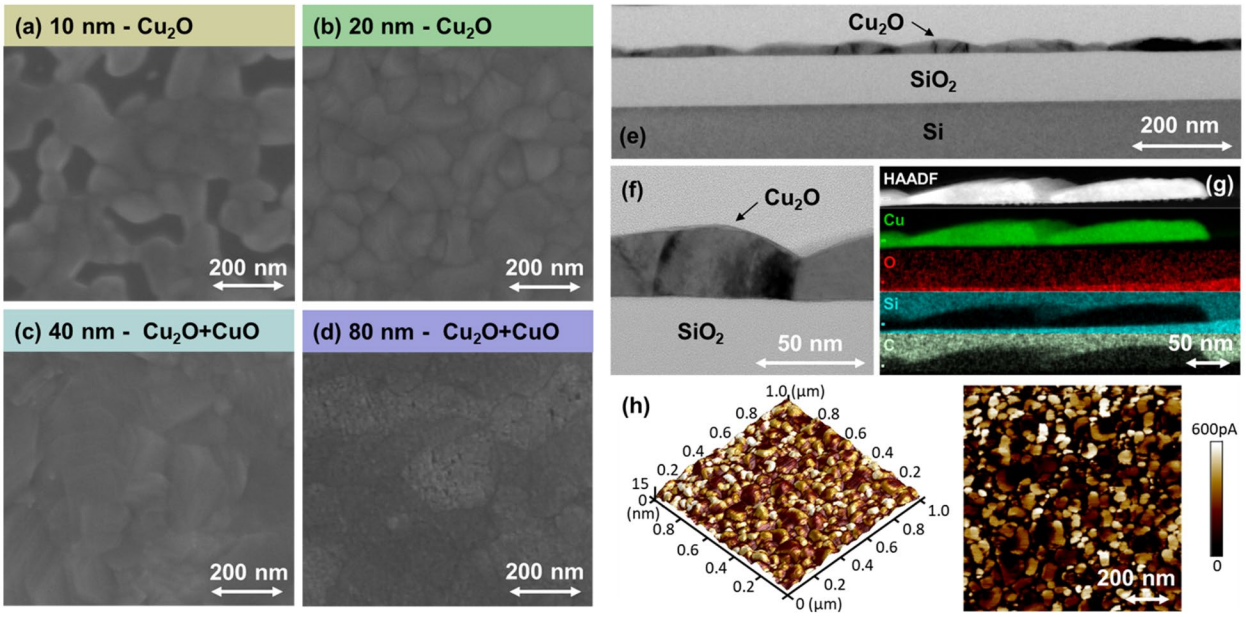



*Figure 2.2 SEM images of $Cu_2O$ films with different film thickness: (a) 10 nm, (b) 20 nm, (c) 40 nm, and (d) 80 nm films on $SiO_2$/Si. (e), (f) TEM images of the 20 nm $Cu_2O$ film on $SiO_2$/Si. (g) HAADF-STEM image and EDS mapping (Cu, O, Si, and C) of the 20 nm $Cu_2O$ film on $SiO_2$/Si. (h) Surface topography (left) and vertical current (right) in a 20 nm $Cu_2O$ film deposited on Si, obtained by C-AFM. © 2020 IEEE. Reprinted, with permission, from [71].*

The morphology of the different thickness films was investigated via SEM shown in Figure 2.2(a-d). The 10 nm film has a discontinuous surface. Dense surface morphology was observed for the 20 nm film. The 40 nm and 80 nm films had different surface morphologies, likely due to the formation of the CuO phase, as shown in the GIXRD and XANES results. Figure 2.2(e-f) present TEM images of the 20 nm $Cu_2O$ film. The film has a coalesced island-like morphology, with some variation observed in grain size and thickness. For this $Cu_2O$ film, it appears that

individual grains are vertically homogenous (Figure 2.2(f)). Based on the HAADF-STEM image and EDS mapping results (Figure 2.2(g)), there was no apparent segregation of Cu metal, carbon, or silicates that might limit or interrupt hole transport within the grains or at the grain boundaries/surface.

Figure 2.2(h) shows C-AFM scans for the 20 nm $Cu_2O$ film. The film has a root mean square surface roughness of 3.23 nm. From the C-AFM measurement of vertical current, I observe that the $Cu_2O$ grains are more conductive than the grain boundaries. The insulating nature of the grain boundaries may limit hole current flow due to grain boundary scattering and/or formation of electrical potential barriers at the grain boundaries, as has been found in other polycrystalline films [75], [76].

### *2.3.2 Electrical properties of RF-sputtered $CuO_x$ thin films*

The sheet resistance ($R_{sh}$) of each film was measured using van der Pauw (*vdP*) method. The measured $R_{sh}$ values varied with film thickness, as shown in Table I. For thin films (10 nm – 20 nm), $R_{sh}$ decreased from $8.5\times10^{10}$ Ω/□ to $3.2\times10^{9}$ Ω/□ as the film thickness increased. Since both films have the same $Cu_2O$ phase, and the decrease in $R_{sh}$ is much greater (1/27×) than that predicted solely by the change in film thickness (1/2×), I postulate that the high $R_{sh}$ of the 10 nm film is likely caused by the discontinuous film morphology. As the film thickness increased from 20 nm to 40 nm, a further significant reduction in $R_{sh}$ (1/38×) was observed as the Cu(II) fraction increased from 12.8% to 26.5%.

It has been previously shown for sputtered, unintentionally doped $CuO_x$ films that $Cu_2O_{1\pm\delta}$ films have hole carrier concentrations ($p$) of ~$10^{15}$–$10^{17}$ $cm^{-3}$ while $CuO_{1\pm\delta}$ films have significantly greater hole concentrations of $p$ ~$10^{17}$–$10^{21}$ $cm^{-3}$ [44]. Thus, the increase in CuO content in the

40-nm film compared to the 20 nm film may lead to a dramatic reduction in $R_{sh}$. In addition, the larger grain size observed in SEM (Figure 2.2(c)) may also contribute to the lower $R_{sh}$ by reducing grain boundary scattering. As the film thickness increased from 40 nm to 80 nm, $R_{sh}$ increased. The CuO phase is known to have a higher hole effective mass ($m^*$) than the $Cu_2O$ phase (and therefore a lower hole mobility). For $Cu_2O$, the calculated and experimentally-obtained light hole $m^*$ are $0.36–0.5m_0$ [63], [77] and $0.58m_0$ [43], respectively. For CuO, the reported average hole $m^*$ is $1.87m_0$ [78] from theory and $7.9m_0$ [79] from experiments. It has also been shown that RFMS CuO films have relatively low Hall mobility of 0.05–6 $cm^2V^{-1}s^{-1}$ [80], [81]. Thus, the increased CuO composition of the 80-nm film may cause an overall increase in resistivity, which is observed as an increase in $R_{sh}$. Finally, when comparing to n-type thin film oxides such as amorphous indium-gallium-zinc-oxide (*a*-IGZO), which has an electron $m^*$ of $0.2m_0$ [22], it is clear that $Cu_2O$ is the more suitable phase for p-type TFTs.

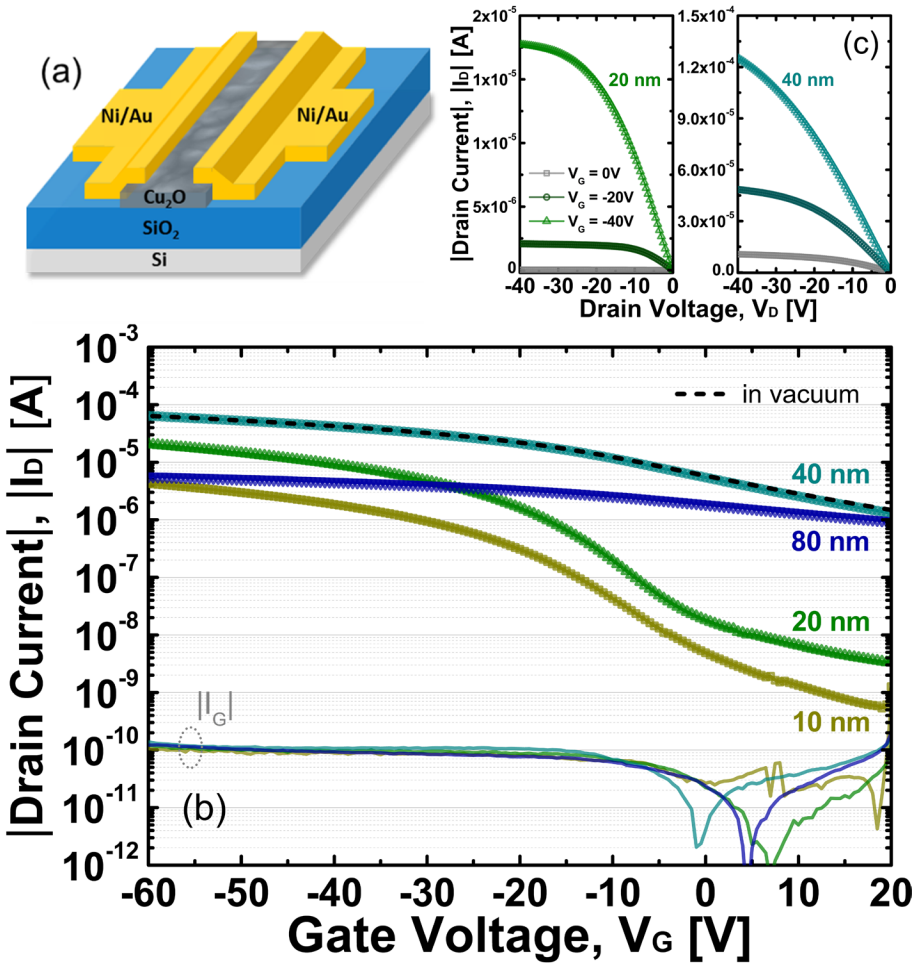



*Figure 2.3 (a) Schematic of the p-type $Cu_2O$ thin film transistor with back-gate structure. (b) Drain current, gate current versus gate voltage ($I_D$, $I_G$ vs. $V_G$) with different film thickness: 10 nm, 20 nm, 40 nm, and 80 nm. The measured TFTs have W/L = 3000 µm/100 µm and 100 nm $SiO_2$ dielectric layer. The dashed line indicates behavior of a 40 nm thick TFT in vacuum. For this measurement, the roughing pump was run for approximately 24 hr before measurement. The drain voltage, $V_D$, is −10 V for all TFTs. (c) $I_D$ vs. $V_D$ curves of the 20-nm and 40-nm TFTs. © 2020 IEEE. Reprinted, with permission, from [71].*

*Table 2.1 Material properties and electrical characteristics of p-type $CuO_x$ thin film transistor with different film thickness. © 2020 IEEE. Reprinted, with permission, from [71].*

| | 10 nm | 20 nm | 40 nm | 80 nm |
|---|---|---|---|---|
| Film phase | $Cu_2O$ | $Cu_2O$ | $Cu_2O$+CuO | $Cu_2O$+CuO |
| Cu(I) (%) | 82.3 | 87.2 | 73.5 | 66.1 |
| Cu(II) (%) | 17.7 | 12.8 | 26.5 | 33.9 |
| $\mu_{FE}$ ($cm^2V^{-1}s^{-1}$) | 0.013 | 0.059 | 0.107 | 0.005 |
| $I_{on}/I_{off}$ ratio | ×3388 | ×5469 | ×49 | ×6.1 |
| $SS_{min}$ (V/dec) | 9.29 | 8.05 | 29.51 | 65.34 |
| $R_{sh}$ (Ω/□) from *vdP* | $8.5\times10^{10}$ | $3.2\times10^{9}$ | $8.3\times10^{7}$ | $1.5\times10^{8}$ |
| $D_{it}$ ($cm^{-2}eV^{-1}$) | $3.34\times10^{13}$ | $2.89\times10^{13}$ | - | - |

*Table 2.2 Contact resistance measured by transmission line method (TLM). © 2020 IEEE. Reprinted, with permission, from [71].*

| | 10 nm | 20 nm | 40 nm | 80 nm |
|---|---|---|---|---|
| $2R_CW$ (Ω-cm) @ $V_G = 0V$ (@ $V_G = -40V$) | 165M (847k) | 16M (82k) | 32k (4k) | 99k (44k) |
| $\rho_c$ (Ω-$cm^2$) | 354k | 26k | 6.29 | 18 |
| $R_{sh}$ (Ω/□) from TLM | $1.92\times10^{10}$ | $2.32\times10^{9}$ | $3.97\times10^{7}$ | $1.33\times10^{8}$ |
| $2R_C/R_T$ % for W/L = 3000/100 µm/µm @ $V_G = 0V$ (@ $V_G = -40V$) | 46.2% (40.1%) | 40.0% (32.9%) | 7.4% (5.3%) | 6.9% (7.0%) |

Thin film transistors (TFTs) were fabricated with $CuO_x$ films of different thicknesses. The electrical test results are shown in Figure 2.3. In the TFTs, a patterned channel layer was used to minimize the impact of fringing current and gate leakage current, which can lead to overestimation of $\mu_{FE}$ [76]. The TFTs have $\mu_{FE}$ of 0.005 – 0.1 $cm^2V^{-1}s^{-1}$, as listed in Table 2.1. The linear $\mu_{FE}$ was calculated using the following equation: $\mu_{FE} = g_m(C_{OX}V_{DS}W/L)^{-1} = (\partial I_D/\partial V_{GS})(C_{OX}V_{DS}W/L)^{-1}$, where $g_m$ is the transconductance, $I_D$ is the drain current in linear region, $C_{OX}$ is gate oxide capacitance per unit area, and $W/L$ is the channel width/length ratio. Among the different devices, a maximum on/off current ($I_{on}/I_{off}$) ratio of ~$5 \times 10^3$ and a $\mu_{FE}$ mobility of 0.059 $cm^2V^{-1}s^{-1}$ were observed for the 20 nm $Cu_2O$ TFT, which also has the highest Cu(I) fraction. Across devices tested on five different samples, the field-effect mobility for 20-nm $Cu_2O$ TFTs varied between 0.032 and 0.059 $cm^2V^{-1}s^{-1}$, indicating the good repeatability and consistency of my results. As discussed above, since $Cu_2O$ has more attractive p-type properties, a higher Cu(I) fraction should correlate with better TFT performance, as observed here. While thin $Cu_2O$ films (10–20 nm) showed $I_{on}/I_{off}$ ratios higher than those of thicker films, a large off-current was still observed. The relatively large off current may be due to minority carrier accumulation [53] and/or minority carrier injection from S/D to channel enabled by Fermi level pinning [59]. Although the phase of both the 10 nm and 20 nm films is $Cu_2O$, the 40 nm TFT has the highest on-current, possibly due to the more dense and continuous film, as observed in SEM (Figure 2.2(c)). The 40 nm TFT also has the highest $\mu_{FE}$ of 0.1 $cm^2V^{-1}s^{-1}$, which may originate from the larger grain size and/or decrease of contact resistance (see Table 2.2). In the case of the 80 nm film with an increased CuO composition, the TFT has lower $\mu_{FE}$ and $I_{on}$. The high off-current level for these thick films may be due to current flowing through an additional, parallel conduction path.

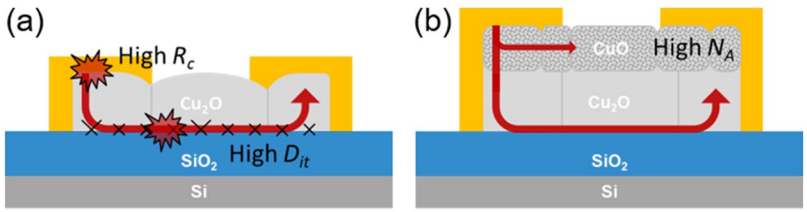



*Figure 2.4 (a) Illustration of the possible current flow paths in (a) thin (10 nm–20 nm) $CuO_x$ TFTs with high contact resistance and interface scattering and (b) thick (40 nm–80 nm) $CuO_x$ TFTs with vertically non-homogenous films. © 2020 IEEE. Reprinted, with permission, from [71].*

To determine whether the high-off current is due to an oxygen- or water-related surface accumulation layer, vacuum treatment was performed. The 40 nm thick TFT was kept under a roughing vacuum for ~24 hours, and then the device was measured in vacuum (dashed line in Figure 2.3(b)). Since the vacuum treatment did not affect TFT performance, the high off-current observed for thicker channels (40–80 nm) may originate from a highly-doped CuO layer, rather than from a surface accumulation layer created by adsorbed oxygen or water. As shown in Figure 2.4(b), the thicker films may not be vertically homogeneous: a conductive CuO surface layer may form an additional current flow path. The existence of such a structure is further supported by the GIXRD results and SEM images showing different surface morphology.

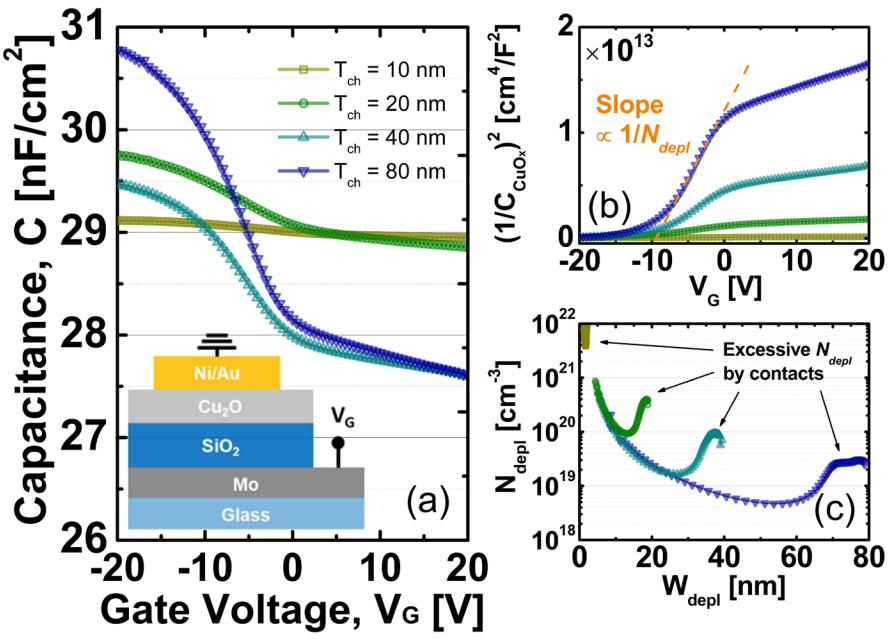



*Figure 2.5 (a) Capacitance versus gate voltage (C vs. $V_G$) of MOSCAPs with different $CuO_x$ film thickness: 10 nm, 20 nm, 40 nm, and 80 nm. (b) $(1/C_{CuOx})^2$ vs. $V_G$ plot. (c) Depletion carrier concentration ($N_{depl}$) vs. depletion width ($W_{depl}$) plot. © 2020 IEEE. Reprinted, with permission, from [71].*

To obtain a deeper understanding of the p-type properties of $CuO_x$, MOS capacitors were also fabricated. To eliminate silicon gate depletion effects, the capacitors were fabricated using a metal bottom gate, instead of the heavily-doped Si bottom gate. The $C$ vs. $V_G$ plots in Figure 2.5(a) show clear accumulation and depletion behavior, in agreement with the p-type TFT I-V curves. From the measured $C$-$V$ data, the depletion charge concentration ($N_{depl}$) was calculated using: $N_{depl} = -2/(q\varepsilon_0\varepsilon_{CuOx}A^2|d(1/C_{CuOx}^2)/dV_G|)$, where $C_{CuOx} = (C_{SiO2} \times C_{Total})/(C_{SiO2} - C_{Total})$ is the $CuO_x$ depletion capacitance, $q$ is the electron unit charge, $\varepsilon_0$ is the permittivity of free space, and $A$ is the capacitor area [82]. Here $\varepsilon_{CuOx}$ is the $CuO_x$ dielectric contact, which was assumed to be 7.11–22, as reported in [83], [84], to match depletion width ($W_{depl}$) with the physical thickness. In Figure 2.5(b), I observe that the slope of $(1/C_{CuOx})^2$ vs. $V_G$ is proportional to $1/N_{depl}$. $N_{depl}$ vs. the $W_{depl}$ is shown in Figure 2.5(c). I note that the minimum $N_{depl}$ observed is much higher than the $p$ level (~$10^{15}$–$10^{17}$ $cm^{-3}$) observed previously in sputtered $Cu_2O_{1\pm\delta}$ [44] and that measured in my Hall

measurements, described below. I note that at room temperature, the value of $p$ is not equal to acceptor doping concentration ($N_A$) due to the high acceptor activation energy ($E_A$) and high compensation ratio ($N_D/N_A$) [68]. In addition, from $C$-$V$, I note that the $N_{depl}$ value rises as the depletion region expands to reach the top ohmic electrode. The large value of $N_{depl}$ under full depletion (indicated by arrows in Figure 2.5(c)) is likely caused by reaction of the metal ohmic contact (here, Ni) with $Cu_2O$ to form a heavily-doped region at the top interface. Such metal-to-$Cu_2O$ interfacial reactions have been discussed in previous studies [44], [85]. This heavily-doped top region makes it impossible to fully deplete the MOSCAPs made with 10-nm and 20-nm $CuO_x$, and $N_{depl}$ cannot reach its minimum, bulk value. For the same reason, the 10-nm and 20-nm MOSCAPS have relatively large $C_{depl}/C_{acc}$ ratios, i.e. they exhibit minor capacitance modulation.

In contrast with the MOSCAP structure, the TFTs do not have a metal layer on the back channel. Therefore, the 10-nm and 20-nm $CuO_x$ TFT channels can be fully depleted and exhibit high $I_{on}/I_{off}$ ratios. For thicker films, there is a larger region of $CuO_x$ film thickness that can be depleted before the influence of the top Ni/Au contact is felt. Thus a larger swing in the capacitance during depletion to accumulation is observed. In addition, the heavily-doped region at the bottom of the film (i.e. at small $W_{depl}$) has been observed previously in TFTs and is attributed to trapped charge at the interface [56], [60].

### *2.3.3 Device level issues: non-idealities in thin film transistor*

Using Hall samples, I measured a Hall mobility ($\mu_{Hall}$) of 12.1 $cm^2V^{-1}s^{-1}$ and a hole concentration of $2.04 \times 10^{16}$ $cm^{-3}$ for a 38-nm thick film. This mobility is much greater than the $\mu_{FE}$ of 0.005–0.1 $cm^2V^{-1}s^{-1}$ measured for the 10 to 80-nm thick films. In principle, TFTs can have a field-effect mobility that is equal to the Hall mobility; this has observed experimentally in n-type zinc tin oxide TFTs [86]. Thus, the low $\mu_{FE}$ of my p-type $Cu_2O$ TFTs may originate from non-idealities in the TFTs. The Hall sample and TFTs have different current flow paths. In a Hall sample, current flows via the bulk of the film, whereas in a TFT, current flows at the gate insulator interface, as shown in Figure 2.4(a). Thus, the value of $\mu_{Hall}$ is mainly determined by fundamental scattering mechanisms, such as grain boundary scattering and impurity scattering, whereas $\mu_{FE}$ is additionally affected by TFT non-idealities. For my long-channel TFTs, I can assume that short-channel effects are negligible. Thus, I focus on investigating the effects on $\mu_{FE}$ of the S/D contact resistance and of interface scattering or traps at the channel-to-dielectric junction.

First, the effect of contact resistance ($R_C$) was investigated. The FE mobility of a TFT with non-zero contact resistance, $\mu_{FE,c}$, can be expressed: $\mu_{FE,c} = \mu_{FE,0}(1 + 2R_C/R_{CH})^{-1}$, where $\mu_{FE,0}$ is the FE mobility when $R_C$ is negligible and $R_{CH}$ is the channel resistance [87]. Here, $R_C$ and $R_{CH}$ can be functions of the applied electric fields. When the ratio of $2R_C/R_{CH}$ becomes significant (> 10%) the effective mobility of the TFT is reduced. In essence, for the same applied voltage, the *IR* voltage drop across the contacts reduces the voltage seen across the semiconductor channel, lowering $I_D$. To find a suitable contact metal, I consider the sum of the electron affinity ($\chi$) and band gap ($E_G$), which totals ~5.49 eV for $Cu_2O$ [88] and ~5.42 eV for CuO [79]. Thus, I require a metal with a workfunction ≥ 5 eV to make an ohmic contact. For this reason, previous studies have mainly used Ni (5.04–5.35 eV), Au (5.31–5.47 eV), and Pt (5.12–5.93 eV) as source/drain contacts

for $CuO_x$ TFTs [33], [89]. My TFTs showed similar performance with Ni/Au ($\mu_{FE}$ = ~0.06 $cm^2V^{-1}s^{-1}$) and Pt/Au ($\mu_{FE}$ = ~0.04 $cm^2V^{-1}s^{-1}$) contacts, possibly due to Fermi level pinning [59]. Since metal adhesion was an issue with Pt/Au contacts, Ni/Au metal was used in this work and $R_C$ was quantified using TLM analysis [72].

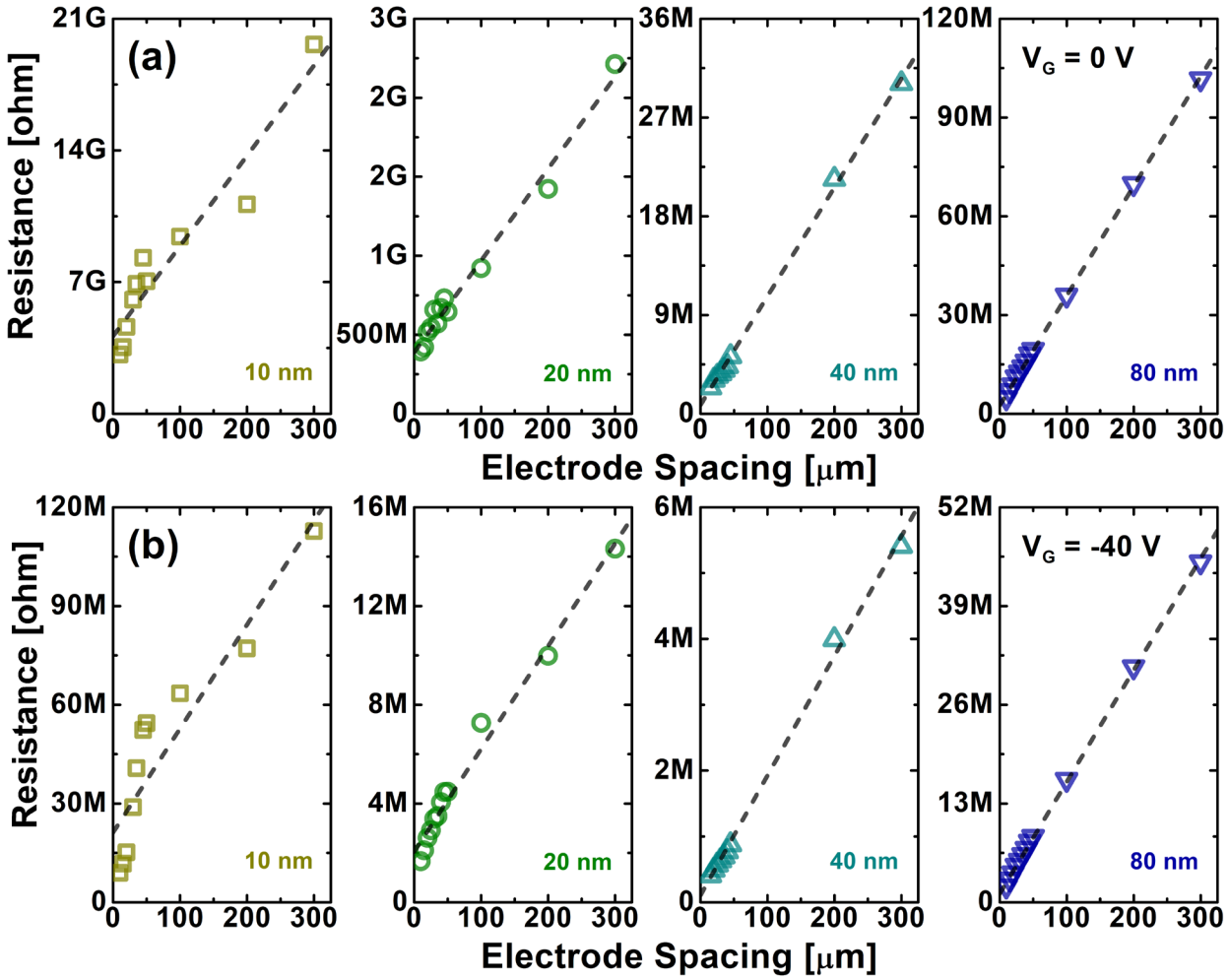



*Figure 2.6 Transmission line measurement results with different $CuO_x$ thin film thickness: 10 nm, 20 nm, 40nm, and 80 nm. Resistance versus electrode spacing plots when (a) gate voltage ($V_G$) = 0 V and (b) $V_G$ = −40 V.*

$CuO_x$ films with different thicknesses have different width-normalized contact resistance, $R_C W$, values, as shown in Table 2.2 and Figure 2.6. The thinner films have much higher $2R_C W$ values at $V_G$ = 0 V (16–165 MΩ-cm) than the thicker films (32–99 kΩ-cm). The corresponding specific contact resistance, $\rho_c$, was 26–345 kΩ-cm$^2$ for the thin films and 6.29–18 Ω-cm$^2$ for the thick films. Even though the contact resistance is relatively high, especially for the thin channel TFTs, linear $I_D$ vs. $V_D$ characteristics were observed in the linear region of operation, as presented in Figure 2.3(c). As the film thickness increased from 20 nm to 40 nm, a significant reduction in the $2R_C W$ value from 16 MΩ-cm to 32 kΩ-cm was observed. This may be due to the vertical in-homogeneity of the thick films, illustrated in Figure 2.4(b), such that the semiconductor contact is made to heavily-doped CuO rather than more lightly-doped $Cu_2O$. The heavily-doped CuO layer may form a low-resistance tunneling barrier to the Ni.

To assess the impact of contact resistance on TFT performance, using the extracted contact resistance parameters I predict the ratio of contact resistance to total channel resistance, $2R_C/R_T$, where $R_T = R_{CH} + 2R_C$ and $R_{CH} = r_{ch} \times L$, for p-type $CuO_x$ TFTs with $W/L$ = 3000/100 μm/μm. The results are shown in Table 2.2. For thin films, the $2R_C/R_T$ value at $V_G$ = 0 V is high at ≥ 40%. Moreover, the contact resistance for thin channel layer TFTs is modulated by the applied gate voltage: at $V_G$ = −40 V, $2R_C/R_T$ is 33%. In contrast, the thicker films have a much lower $2R_C/R_T$ value of ~7%, which is very weakly gated, especially for the 80-nm device. The lack of a significant gating effect on contact resistance of the thick TFTs points to the effectiveness of the heavily-doped CuO top layer in forming a quasi-ohmic tunneling contact. It is expected that the formation of ohmic contacts to p-type $Cu_2O$ may be difficult due to the charge neutrality level location ~0.8 eV above the valence band maximum that leads to a required metal work function of ≥ 7 eV, based on the approach described in [90], [91]. The impracticality of obtaining such a

high metal workfunction indicates that tunneling conduction mechanism is critical to demonstrate low $R_C$ for high-performance $Cu_2O$ TFTs [92], although more work is still needed to reduce the contact resistance further.

Second, the density of interface states was extracted based on the minimum subthreshold slope (*SS*) of the TFTs. The following equation can express the density of interface states: $D_{it} = [(SS \log_{10}(e)/(kT/q)) - 1] \times C_{OX}/q$, where $k$ is the Boltzmann constant, $T$ is temperature. Here $C_{OX}$ for 100-nm $SiO_2$ is taken to be $3.45\times10^{-8}$ F/cm$^2$. The calculated $D_{it}$ at the channel-to-dielectric interface was $3.34 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$ and $2.89 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$ for the 10 nm TFT and the 20 nm TFT, respectively. These values are similar to those previously reported for spray-coated $Cu_2O$-$SiO_2$ (~$5.6 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$) [60] and sputtered $Cu_2O$-$SrTiO_3$ (~$3.3 \times 10^{13}$ cm$^{-2}$ eV$^{-1}$) [56] interfaces. For the thicker films, the $D_{it}$ value calculated from *SS* is ~$10^{14}$ cm$^{-2}$ eV$^{-1}$. However, this *SS* value may be degraded due to additional conduction paths (i.e. the CuO layer illustrated in Figure 2.4(b)) that lower the $I_{on}/I_{off}$ ratios ratio. Such high $D_{it}$ can cause threshold voltage ($V_T$) shifts and mobility degradation due to charge trapping/free carrier scattering at the interface. For comparison, n-type *a*-IGZO film have achieved $D_{it}$ of ~$10^{11}$ cm$^{-2}$ eV$^{-1}$ with $\mu_{FE} > 10$ cm$^2$V$^{-1}$s$^{-1}$ [22]. In this work, I have used a $SiO_2$ gate dielectric. Others have reported lower $D_{it}$ values ($6.8 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$) when using a $Cu_2O$-$HfO_2$ interface [93]. Therefore, to improve gate-to-channel coupling and reduce interface traps, in the future it will be critical to identify suitable high-*k* dielectrics for $Cu_2O$ TFTs.

### *2.3.4 TCAD simulation methods and results*

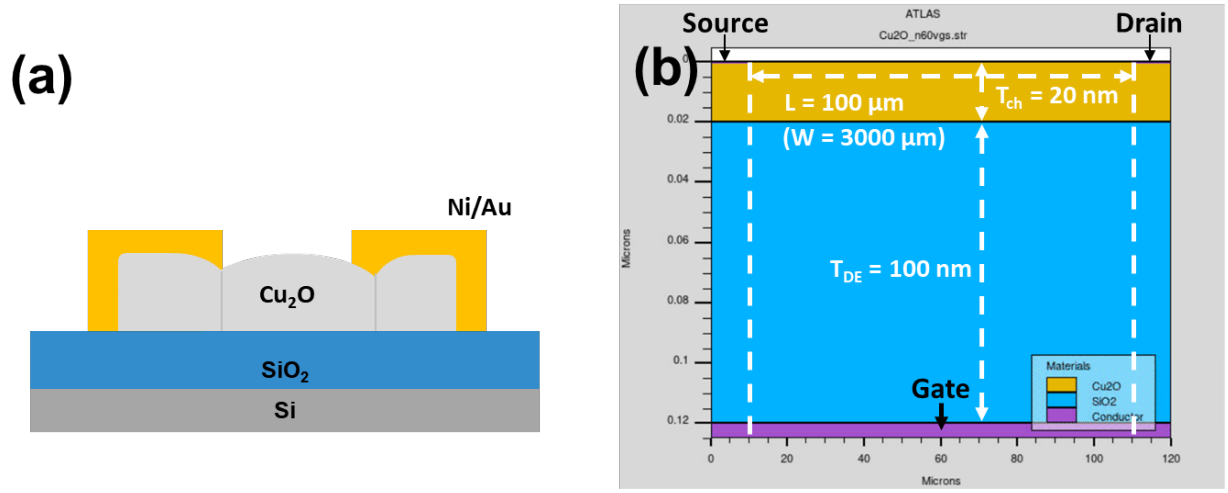



*Figure 2.7 (a) 2D schematic illustration of $Cu_2O$ thin film transistor used in experiment with back-gate structure. (b) 2D simulation structure in Silvaco ATLAS TCAD simulation.*

To understand device level issues in the $Cu_2O$ thin film transistor, in addition to the experimental analyses, 2D numerical simulation was performed using Silvaco ATLAS TCAD software [94]. Figure 2.7(a) and (b) shows the 2D structure of $Cu_2O$ thin film transistor used in experiments and simulations, respectively. To model the experimentally fabricated device results, the 2D simulation structure was built with the dimensions: $SiO_2$ dielectric thickness ($T_{DE}$) = 100 nm (with dielectric constant = 3.9), $Cu_2O$ channel thickness ($T_{ch}$) = 20 nm, channel length/width = 100 µm/3000 µm. In addition, a heavily-doped n-type silicon layer was used as back-gate with work function of 4.7 eV and the S/D contact metal was assigned a 5.1 eV work function to mimic Ni. For the $Cu_2O$ thin film, the mobility was set to 10 $cm^2V^{-1}s^{-1}$ [95], which is the value obtained experimentally from Hall measurements using a 20 nm $Cu_2O$ thin film sample. Other material parameters are based on values reported in the literature: an effective conduction band density of states, $N_C$, of $2.43\times10^{19}$ $cm^{-13}$ [96], an effective valence band density of states, $N_V$, of $1.05\times10^{19}$ $cm^{-13}$ [97]. The valence band maximum, $E_g + \chi_e$, was calculated to be 5.49 eV from $E_g$ = 2.1 eV and $\chi_e$ = 3.39 eV [88].

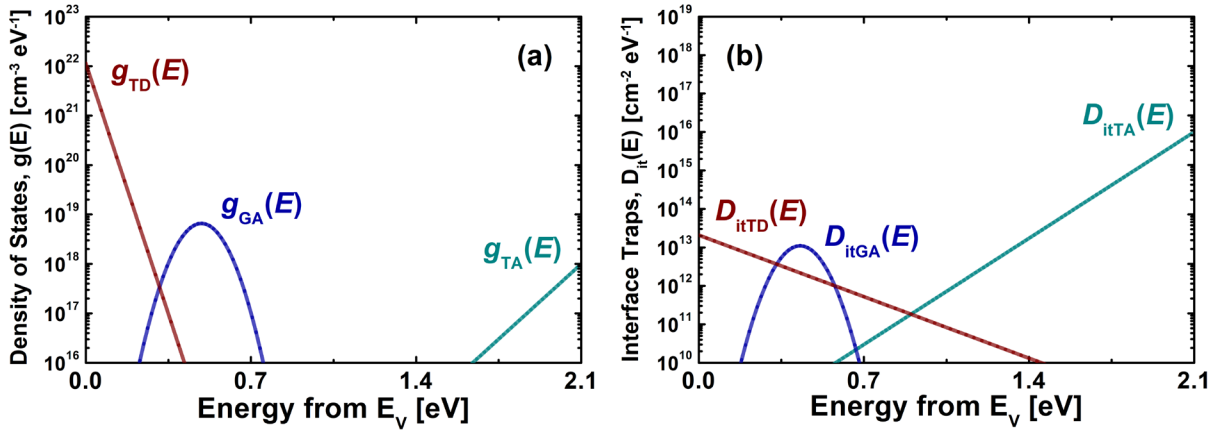



*Figure 2.8 Plots of the sub-band gap density of state profiles in $Cu_2O$ used to model: (a) bulk defect states and (b) interface trap states. For the bulk defects, g(E), the curves labelled $g_{TA}$, $g_{GA}$, $g_{TD}$ indicate the acceptor-like tail sates near $E_C$, the acceptor-like Gaussian deep states, and the donor-like tail states near $E_V$, respectively. For the interface traps, $D_{it}(E)$, located at the channel-dielectric junction, the curves labelled $D_{itTA}$, $D_{itGA}$, $D_{itTD}$ refer to acceptor-like interface traps, acceptor-like Gaussian interface traps, and donor-like interface traps.*

For oxide semiconductors, the sub-bandgap density of states (*i.e.*, the defect states) are critical material parameters. The defect states of oxide semiconductor are commonly modeled by a combination of donor- and acceptor-like band tail states and mid-gap states with Gaussian distribution [94], [98]–[101]. To explain the electrical properties of the $Cu_2O$ thin films used in our TFTs, the bulk defect and interface trap states were defined as shown in Figure 2.8. The total density of states (DOS) in the bulk, $g(E) = g_{TA}(E) + g_{GA}(E) + g_{TD}(E)$, is defined by:

$$g_{TA}(E) = N_{TA} \times exp\left[\frac{(E-E_C)}{W_{TA}}\right],$$

$$g_{GA}(E) = N_{GA} \times exp\left\{-\left[\frac{(E_{GA}-E)}{W_{GA}}\right]^2\right\}, \text{ and}$$

$$g_{TD}(E) = N_{TD} \times exp\left[\frac{(E_V-E)}{W_{TD}}\right],$$

where $E$ is the trap energy, $N$ is the peak density of states, $W$ is the characteristic decay energy. The subscripts $T$, $G$, $A$, $D$ means tail states, Gaussian deep states, acceptor-like states, and donor-like states, respectively.

Similarly, the interface trap density, $D_{it}(E) = D_{itTA}(E) + D_{itGA}(E) + D_{itTD}(E)$, is given by:

$$D_{itTA}(E) = N_{itTA} \times exp\left[\frac{(E-E_C)}{W_{itTA}}\right],$$

$$D_{itGA}(E) = N_{itGA} \times exp\left\{-\left[\frac{(E_{itGA}-E)}{W_{itGA}}\right]^2\right\}, \text{ and}$$

$$D_{itTD}(E) = N_{itTD} \times exp\left[\frac{(E_V-E)}{W_{itTD}}\right],$$

where $N_{it}$ is the peak interface trap density, and $W_{it}$ is the characteristic decay energy. The concentration and distribution of the defect states strongly affect the TFT performance.

*Table 2.3 TCAD simulation parameters to express the sub-band gap density of state of $Cu_2O$.*

| Symbol (Unit) | Description | Value |
|---|---|---|
| Bulk defect parameters | | |
| $N_{TA}$ ($cm^{-3}eV^{-1}$) | Acceptor-like tail state peak density at bulk | $1\times10^{18}$ |
| $W_{TA}$ (eV) | Acceptor-like tail state width at bulk | 0.1 |
| $N_{TD}$ ($cm^{-3}eV^{-1}$) | Donor-like tail state peak density at bulk | $1.14\times10^{22}$ |
| $W_{TD}$ (eV) | Donor-like tail state width at bulk | 0.03 |
| $N_{GA}$ ($cm^{-3}eV^{-1}$) | Acceptor-like Gaussian states peak density at bulk | $6.6\times10^{18}$ |
| $E_{GA}$ (eV) | Acceptor-like Gaussian states peak position at bulk | 1.61 (relative to the CB) |
| $W_{GA}$ (eV) | Acceptor-like Gaussian state width at bulk | 0.103 |
| Interface defect parameters | | |
| $N_{itTA}$ ($cm^{-2}eV^{-1}$) | Acceptor-like tail state peak density at interface | $1\times10^{16}$ |
| $W_{itTA}$ (eV) | Acceptor-like tail state width at interface | 0.11 |
| $N_{itTD}$ ($cm^{-2}eV^{-1}$) | Donor-like tail state peak density at interface | $2.08\times10^{13}$ |
| $W_{itTD}$ (eV) | Donor-like tail state width at interface | 0.19 |
| $N_{itGA}$ ($cm^{-2}eV^{-1}$) | Acceptor-like Gaussian states peak density at interface | $1.1\times10^{13}$ |
| $E_{itGA}$ (eV) | Acceptor-like Gaussian states peak position at interface | 1.67 (relative to the CB) |
| $W_{itGA}$ (eV) | Acceptor-like Gaussian states width at interface | 0.095 |
| $Q_F$ ($cm^{-2}$) | Fixed charge | $-1\times10^{11}$ |
| Contact parameters | | |
| $\rho_C$ (Ω-cm) | Contact resistance | $19\times10^{3}$ |

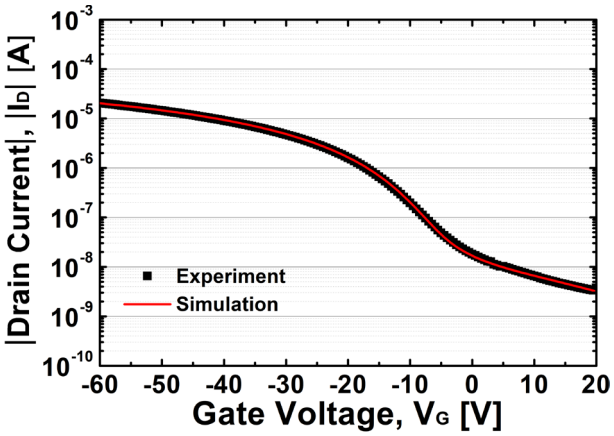



*Figure 2.9 Comparison between experimental data and TCAD simulation result for drain current versus gate voltage ($I_D$ vs. $V_G$) for a $Cu_2O$ thin film transistor. The drain voltage ($V_D$) value is −10 V.*

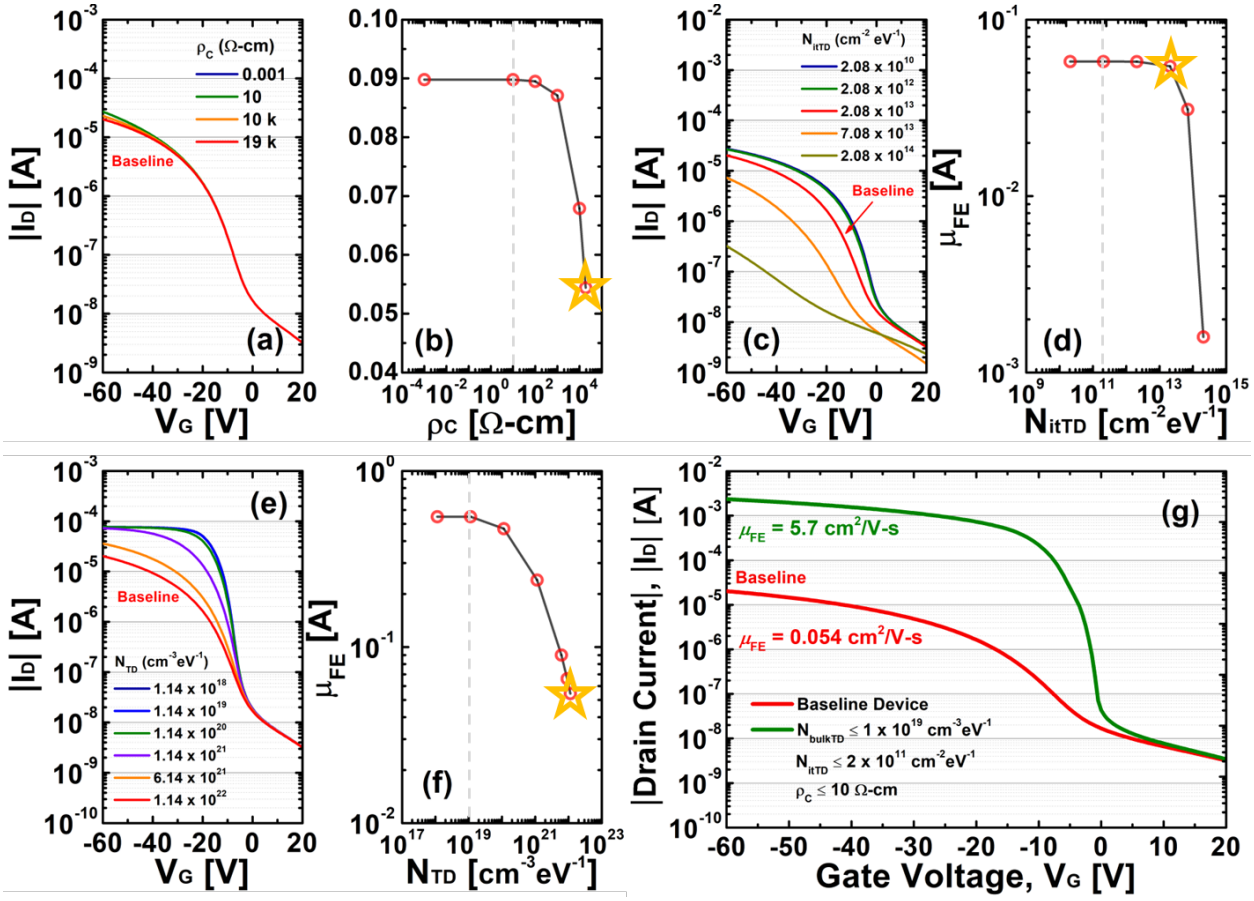



*Figure 2.10 Effect of varying the (a, b) contact resistance, (c, d) donor-like tail state peak density at the interface, and (e, f) donor-like tail state peak density in the bulk on drain current and field effect mobility. For (a, c, e), the red line indicates the baseline device. For (b, d, f), the star indicates the field effect mobility of the baseline device. (g) Comparison of simulation results for the baseline device and an optimized device with low contact resistance and low interface/bulk traps. The dashed lines in (b, d, f) indicate the maximum values of each parameter that can be present before the field effect mobility begins to decrease. For all plots, the drain voltage, $V_D$, is −10 V.*

To match the experimental results, TCAD simulation was performed with the parameter values shown in Table 2.3. In addition to the parameters mentioned already, a non-zero contact resistance was also included in the simulation in order to fit the experimental results. The experimentally obtained values (*i.e.*, $D_{it} = 2.08\times10^{13}$ $cm^{-2}eV^{-1}$ and $\rho_c = 26$ kΩ-cm) were used as starting points. By slightly modifying the fitting parameters, a good fit was obtained. The simulation curve in Fig. 2.9 and the baseline curves shown in Fig. 2.10 illustrate the simulation results for the parameter values listed in Table 2.3.

After achieving a good fit to our experimental data, I performed further simulations to understand the impact of three simulation parameters: the donor-like tail state peak density in the bulk ($N_{TD}$), the donor-like tail state peak density at the interface ($N_{itTD}$), and the contact resistance ($\rho_c$). Other parameters will also affect device performance, but it is expected that these three parameters will play a critical role in TFT behavior, as discussed in the experimental section.

To understand the effect of the contact resistance, interface traps, and bulk defects on the field effect mobility, multiple simulations were performed iterating each parameter in turn while keeping the remaining fitting parameters as listed in Table 2.3. Figure 2.10(a) and (b) shows the relationship between contact resistance and TFT performance. When $\rho_C < 10$ Ω-cm, the field effect mobility increases to ~1.64× of its baseline value. Further reductions in contact resistance do not yield additional benefit. This indicates that solving contact resistance issues is critical. Nonetheless, the improved field effect mobility is still much lower than the intrinsic mobility, which is set to 10 $cm^2V^{-1}s^{-1}$ in the simulation, due to high interface/bulk traps.

Figure 2.10(c-f) shows the impact of varying $N_{TD}$ or $N_{itTD}$. The results indicate that a maximum field effect mobility can be obtained if $N_{TD} \leq 1\times10^{19}$ $cm^{-3}eV^{-1}$ and $N_{itTD} \leq 2\times10^{11}$ $cm^{-2}eV^{-1}$.

These TCAD simulation results indicate that all three parameters must be addressed in order to obtain a field effect mobility that is close to the intrinsic mobility. To demonstrate this, a final simulation was performed with bulk defects/interface traps at the threshold values obtained above ($N_{TD} = 1\times10^{19}$ cm$^{-3}$eV$^{-1}$, $N_{itTD} = 2\times10^{11}$ cm$^{-2}$eV$^{-1}$ and $\rho_C$ = 10 Ω-cm). The results are shown in Figure 2.10(g): the field effect mobility was improved from 0.054 cm$^2$V$^{-1}$s$^{-1}$ to 5.7 cm$^2$V$^{-1}$s$^{-1}$. These simulation results indicate that our current experimental TFT performance is limited by high bulk/interface traps ($N_{TD} = 1.14\times10^{22}$ cm$^{-3}$eV$^{-1}$ and $N_{itTD} = 2.08\times10^{13}$ cm$^{-2}$eV$^{-1}$) and high contact resistance ($\rho_C$ = 19 kΩ-cm). It is clear that reduction of the high trap density at the interface, reduction of the high trap density in the bulk and reduction the contact resistance must be done in concert to obtain high performance p-type $Cu_2O$ thin film transistors.

## 2.4 Conclusion

Thin film p-type semiconductors are urgently needed for film CMOS circuitry. $Cu_2O$ has promising material properties, but previous work has found that the field effect mobility of TFTs is much lower than the measured Hall mobility. Here, I have comprehensively investigated $CuO_x$ TFTs as a function of channel layer thickness. I found that lowering both contact resistance and interface traps are the keys to reducing the gap between $\mu_{Hall}$ and $\mu_{FE}$. Because $Cu_2O$ films exhibit a high $\mu_{Hall}$, here measured to be 12.1 cm$^2$V$^{-1}$s$^{-1}$, I believe that $Cu_2O$ has significant potential as a p-type candidate for future oxide semiconductor CMOS TFT technologies.

# Chapter 3 Experimental and theoretical study of hole scattering in RF sputtered p-type $Cu_2O$ thin films

## 3.1 Introduction

In the previous chapter [71], I evaluated TFT performance with RF sputtered $Cu_2O$ thin film and found two key issues. First, the field-effect (FE) mobility is much lower than the film Hall mobility. This issue can be addressed by improving the source/drain contact and reducing defect states at the gate dielectric/semiconductor interface. Second, the $Cu_2O$ thin film itself had much lower Hall mobility ($\mu_{Hall}$) compared to that predicted by theory or measured experimentally under different process conditions—previous studies [33], [42], [102] reported $\mu_{Hall}$ > ~50 $cm^2V^{-1}s^{-1}$. Various methods have been proposed to improve charge transport in $Cu_2O$ thin films [92], [97], [103], [104]. Here I seek to understand hole scattering mechanisms in order to identify pathways to improve thin film mobility.

To understand the scattering mechanisms that limit the Hall mobility, in this chapter I use theory and experiment to compare hole transport in a RF sputtered polycrystalline (*pc*) $Cu_2O$ thin film with hole transport in a single-crystalline (*sc*) $Cu_2O$ bulk substrate. Using temperature-dependent Hall measurements, analytical models, and first-principles density functional theory (DFT) calculations, I identified the dominant scattering mechanisms in my *pc*-$Cu_2O$ thin film to be neutral impurity scattering coming from acceptors and grain boundary scattering. In *sc*-$Cu_2O$, theory predicts an intrinsic mobility of 106 $cm^2V^{-1}s^{-1}$ limited by polar optical phonon scattering, which agrees with analytical interpretation of the experimental Hall data. By understanding what

limits hole mobility in $Cu_2O$ substrates and thin films, I point the way toward future process improvements to enable p-type oxide electronics. Note that I have published the results described in this chapter in reference [95].

### 3.2 Experimental Methods

To experimentally investigate hole transport in $Cu_2O$, I prepared a (111)-oriented $Cu_2O$ natural single-crystal substrate (thickness ~500 μm), which was purchased from SurfaceNet GmbH. The *sc*-$Cu_2O$ sample was diced into 0.5 cm by 0.5 cm pieces and then cleaned using acetone and isopropyl alcohol (IPA). To deposit a 20 nm *pc*-$Cu_2O$ thin film, I used RF magnetron sputtering (Kurt J. Lesker PRO Line PVD 75) at room temperature on glass using a Cu metal target. I then annealed the thin film at 600 ℃ for 10 min in vacuum. After annealing, I observed that the film has $Cu_2O$ phase with Cu(I) and Cu(II) fractions of 87.2% and 12.8%, respectively [71]. Further film characterization can be found in my previous work [71]. To fabricate van der Pauw geometry Hall structures, Ni/Au contacts were deposited by e-beam evaporation, with patterning done via metal shadow mask for the *sc*-$Cu_2O$ bulk substrate and via photolithography after wet etching to form a cloverleaf pattern for the *pc*-$Cu_2O$ thin film. Temperature-dependent Hall measurements were taken in the dark in vacuum using an Accent HL5500PC Hall measurement system with 0.41 T, with temperatures varying from 200 K to 400 K. Within the measured temperature range, the symmetry factor, $Q = R_{vertical}/R_{horizontal}$, was 1.18–1.23 for the *pc*-$Cu_2O$ thin film and 1.00–1.20 for the *sc*-$Cu_2O$ bulk substrate [105]. This indicates that the asymmetry of the samples is negligible, since the error in sheet resistivity is < 1% as long as $Q < 1.41$.

## 3.3 Results and Discussion

### *3.3.1 Temperature-dependent Hall measurements*

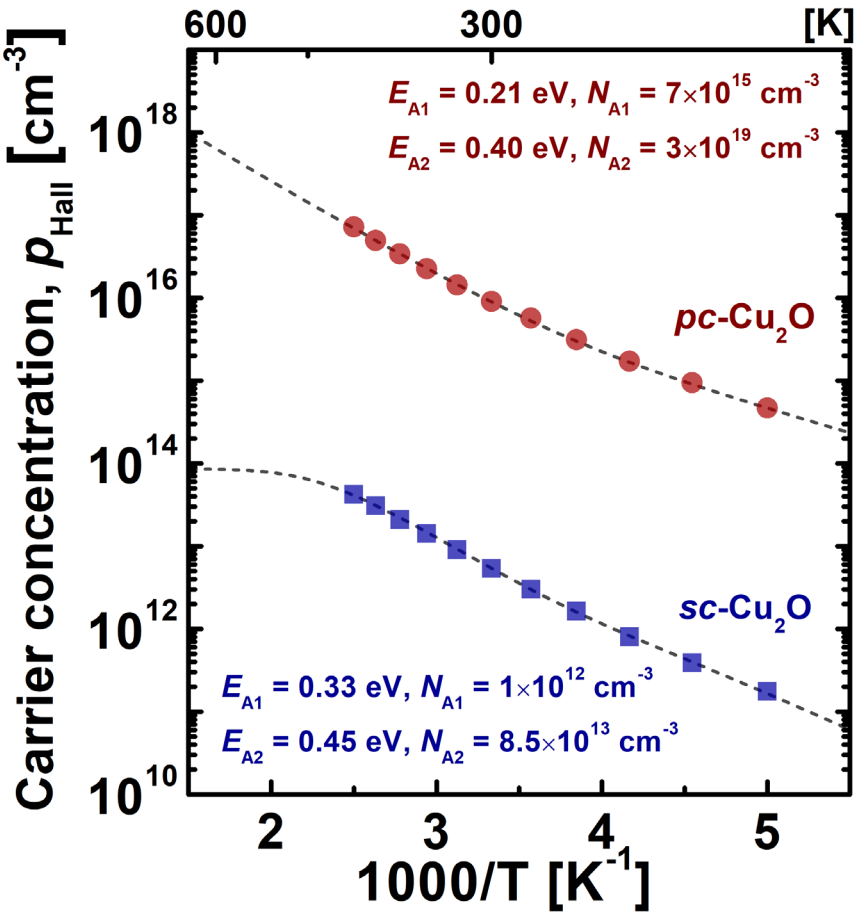



*Figure 3.1 Temperature-dependent carrier concentration ($p_{Hall}$ vs. 1000/T) of a poly-crystalline (pc) $Cu_2O$ thin film (red circles) and a single-crystalline (sc) $Cu_2O$ bulk substrate (blue squares), which have thickness of 20 nm and 500 µm, respectively. The dashed lines indicate fits to Eq. (1) using the parameters given in the figure. Reproduced from [95], with the permission of AIP Publishing.*

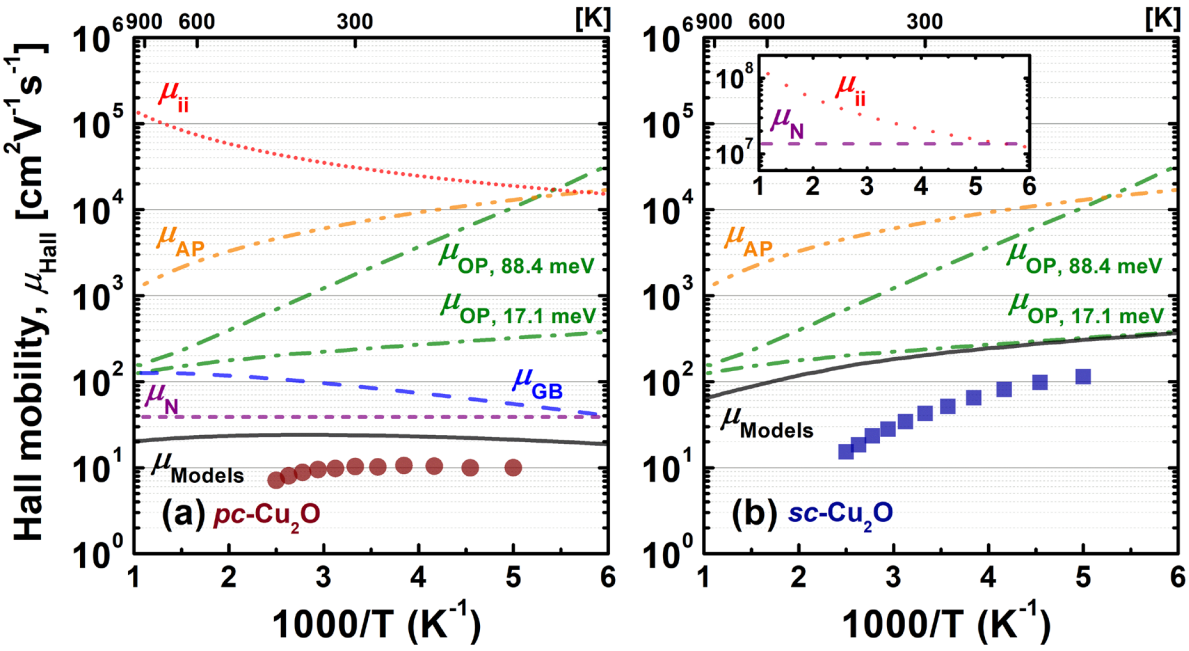



*Figure 3.2 Temperature-dependent Hall mobility ($\mu_{Hall}$ vs. 1000/T) for (a) 20-nm thick poly-crystalline (pc) $Cu_2O$ thin film (red circles) and (b) 500-μm thick single-crystalline (sc) $Cu_2O$ bulk substrate (blue squares). Symbols indicate the experimental data, while lines represent the predicted mobility values due to ionized impurity scattering (ii), neutral impurity scattering (N), grain boundary scattering (GB), and optical phonon (OP) and acoustical phonon (AP) scattering, as well as the total predicted mobility (Models), as labelled. Reproduced from [95], with the permission of AIP Publishing.*

The measured Hall hole concentration and mobility are shown as a function of temperature in Figure 3.1 and Figure 3.2, respectively. In Figure 3.1, I note that the semi-log plot of hole concentration versus inverse temperature for both the *pc*-$Cu_2O$ thin film and the *sc*-$Cu_2O$ bulk substrate are non-linear. This points to the existence of two acceptors, as predicted by theory [62], [64], [106]. The temperature dependence of hole carrier concentration ($p$) was fit using the following analytical expression considering two acceptors with two different activation energies [107], [108].

$$p = N_{A1}^- + N_{A2}^- = \frac{N_{A1}}{1+\frac{g_A p}{N_V e^{-E_{A1}/kT}}} + \frac{N_{A2}}{1+\frac{g_A p}{N_V e^{-E_{A2}/kT}}}, \tag{2.1}$$

where $N_V = 2(2\pi m_h^* kT/h^2)^{3/2}$ is the effective density of valence band states, $N_{A1}$ and $N_{A2}$ are the concentrations of two acceptors, $m_h^*$ is the hole effective mass equal to $0.58m_0$ [43], $k$ is the Boltzmann constant, $T$ is the temperature, $h$ is Planck's constant, $g_A$ is the degeneracy factor (here assumed to be 1), and $E_{A1}$ and $E_{A2}$ are the activation energies of the two acceptor states.

To fit the measured data to Eq. (2.1), I note that theory predicts that the copper simple vacancy ($V_{Cu}$) and copper split vacancy ($V_{Cu}^{Split}$) are the dominant acceptors in $Cu_2O$ [62], [64], [106] with $E_A = 0.23$ eV and 0.47 eV above valence band maximum respectively [62]. Thus I used these as the initial values of $E_{A1}$ and $E_{A2}$. I iterated the values of $N_{A2}$ and $E_{A2}$ to fit the high temperature region of the measured $p_{Hall}$ vs $1000/T$ curve, and then iterated the values of $N_{A1}$ and $E_{A1}$ to fit the low temperature region. The final parameters and fits to Eq. (2.1) are shown in Figure 3.1. I found that $E_{A1}$ and $E_{A2}$ are equal to 0.21 eV and 0.40 eV for *pc*-$Cu_2O$, and 0.33 eV and 0.45 eV for *sc*-$Cu_2O$. These values are accurate to 0.01 eV. Because the values of $E_A$ are much greater than the thermal energy at 400 K (i.e., 35 meV), most of the acceptors will not be ionized at the temperatures measured here. Thus, while the total $N_A$ values ($N_{A1} + N_{A2}$) are $3\times10^{19}$ $cm^{-3}$ for the *pc*-$Cu_2O$ thin film and $8.6\times10^{13}$ $cm^{-3}$ for the *sc*-$Cu_2O$ bulk substrate, the measured values of $p_{Hall}$ at room temperature are far less (Figure 3.1): $9.1\times10^{15}$ $cm^{-3}$ for the *pc*-$Cu_2O$ thin film and $5.4\times10^{12}$ $cm^{-3}$ for the s*c*-$Cu_2O$ bulk substrate. For the *pc*-$Cu_2O$ thin film, a higher carrier concentration was observed. According to a previous study [92], acceptor levels in $Cu_2O$ tend to decrease as process temperature increases. Thus, I attribute the higher level of acceptor states in the *pc*-$Cu_2O$ thin film to intrinsic defects formed during RF sputter deposition. Since the *sc*-$Cu_2O$ bulk substrate is a natural crystal, not synthesized in the lab, its formation conditions are unknown and cannot be directly compared.

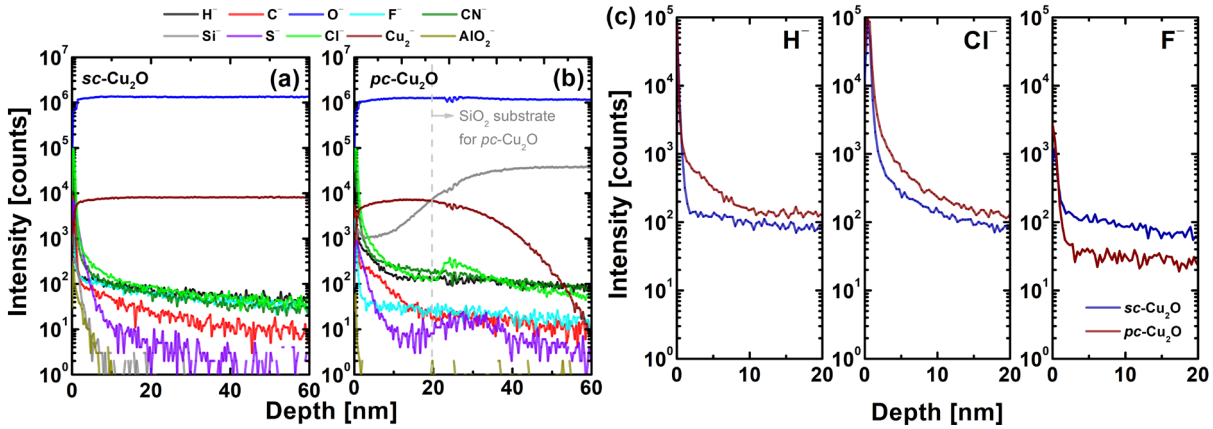



*Figure 3.3 Time-of-flight secondary ion mass spectrometry (ToF-SIMS) results for the (a) sc-$Cu_2O$ bulk substrate and (b) pc-$Cu_2O$ thin film on $SiO_2$/Si substrate. (c) Comparison of H, Cl, and F, which can function as extrinsic donors for these two samples. There is no significant difference in the impurity levels between the two samples. Reproduced from [95], with the permission of AIP Publishing.*

In Eq. (2.1), I neglected the effect of ionized donors. It is known that copper interstitials at octahedral ($Cu_i^{oct}$) and tetrahedral ($Cu_i^{tet}$) sites can act as deep donors positioned 1.18 eV and 1.23 eV below the conduction band minimum, respectively [109]. With an electron effective mass ($m_e$*) of $Cu_2O$ [43] = 0.99$m_0$, the estimated donor ionization rate ($n/N_D$) based on these intrinsic defects is much lower (< 1/1000×) than $p/N_A$ according to the equation [110] $n \approx (n_0 N_D)^{1/2}\exp(-E_A/2kT)$, where $n_0 = 2(m_e{*}kT/2\pi\hbar^2)^{3/2}$. Extrinsic defects such as hydrogen (H) [64], fluorine (F) and chlorine (Cl) [111], are also predicted to act as donors in p-type $Cu_2O$. Using time-of-flight secondary ion mass spectrometry, I find both the *pc*-$Cu_2O$ thin film and *sc*-$Cu_2O$ bulk substrate have low impurity levels of H, F, and Cl, compared to host atoms (Cu and O) (Figure 3.3). These results indicate that my assumption that $N_D \cong 0$ cm$^{-3}$ is acceptable.

### *3.3.2 Thin film level issues: hole scattering mechanisms*

The measured Hall mobility is shown by symbols in Figure 3.2. The trends are quite different for the two samples. The *pc*-$Cu_2O$ thin film shows low and nearly constant mobility with temperature, with only a slight roll-off at the highest and lowest temperatures measured. In contrast, the *sc*-$Cu_2O$ bulk substrate shows a strong increase in mobility as temperature decreases. To understand these trends, I have modelled five scattering mechanisms using analytical equations: (1) ionized impurity scattering, (2) neutral impurity scattering, (3) grain boundary scattering and (4, 5) acoustical and optical phonon scattering. For ionized impurity scattering, the following model was used [112], [113]:

$$\mu_{ii} = r_H \frac{128\sqrt{2\pi}(\varepsilon_{Cu2O}\varepsilon_0)^2(kT)^{3/2}}{\sqrt{m^*}N_i Z^2 q^3}\left[\ln(1+b) - \frac{b}{1+b}\right]^{-1}, \tag{2.2}$$

where $b = 24m^*kT(\lambda/\hbar)$ and $\lambda = ((pq^2)/(\varepsilon_{Cu2O}\varepsilon_0 kT))^{-1/2}$. Here, $\lambda$ is the Debye (screening) length, $Z$ is the charge on the impurity in units $q$, $r_H$ is the Hall-to-drift mobility ratio (=1.93) [113], $\varepsilon_{Cu2O}$ is the dielectric constant of $Cu_2O$ (=7.11) [83], and $N_i$ is the ionized impurity density (= $p$). The neutral impurity scattering was estimated using Erginsoy's model [114]–[116]:

$$\mu_N = \frac{\pi^2 m^* q^3}{10\epsilon_S\epsilon_0 n_N h^3}, \tag{2.3}$$

where $n_N$ is the density of the neutral impurity. Since the acceptor ionization rate ($p/N_A$) is < 1% for *pc*-$Cu_2O$ and < 10% for *sc*-$Cu_2O$ based on the extracted values using Eq. (2.1), I assumed $n_N = N_A$. Note that the neutral impurity scattering model is temperature independent. The grain boundary scattering model [75] used is:

$$\mu_{GB} = \sqrt{\frac{q^2L^2}{2\pi m^* kT}}\, exp\left(-\frac{q\Phi_B}{kT}\right), \tag{2.4}$$

where $L$ is the grain size (diameter) and $\Phi_B$ is the potential barrier height at the grain boundary. Finally, I considered both acoustic (AP) and optical (OP) phonon scattering [117]–[119], i.e.,

$$\mu_{AP} = 3.2 \times 10^{-5}(m^*/m)^{5/2} c_{ll} T^{-3/2} E_1^{-2}, \tag{2.5}$$

where $c_{ll} = (c_{11} + c_{12} + 2c_{44})/2$ is the elastic constant [119] of $Cu_2O$ (= $1.24\times10^{12}$ dyn/cm$^2$) [120] and $E_1$ is the deformation potential of valence band (= 2 eV) [119], and

$$\mu_{OP,i} = \frac{0.87}{(m_{pi}/m)\alpha_i \hbar\omega_{li}}\left[\frac{exp(z_i)-1}{z_i^{1/2}}\right] G(z_i) e^{-\xi}, \tag{2.6}$$

where $z_i = \hbar\omega_{li}/kT$ ($\hbar\omega_{li}$ is in eV), $G(z_i)e^{-\xi}$ is the Howarth and Sondheimer function [121], the values of which are available in graphical and tabulated form, $\alpha_i = (m^*/m)^{1/2}(\mathrm{Ry}/\hbar\omega_{li})^{1/2}(\varepsilon_\infty^{-1}-\varepsilon_0^{-1})$ is the polar coupling constant (where $\varepsilon_\infty = 6.46$ and $\varepsilon_0 = 7.11$) [83], $m_{pi} = m^*(1+ \alpha_i/6)$ is the polar mass, $\hbar$ is the reduced Plank constant, $\omega_{li}$ is the frequency of the longitudinal optical (LO) phonon, $\xi$ is the reduced Fermi energy, and Ry is the Rydberg of energy. Here I considered only the two dominant optical phonon energies, which have $\hbar\omega_l$ of 88.4 meV and 17.1 meV. These values were determined by the first-principles calculations described below and are similar to those previously reported by others [119]. The scattering models were combined using Matthiessen's rule: $1/\mu_{Models} = 1/\mu_{OP} + 1/\mu_{AP} + 1/\mu_{ii} + 1/\mu_N + 1/\mu_{GB}$, and fit to the experimentally-obtained Hall measurement data.

Figure 3.2(a) shows the fitting result for the *pc*-$Cu_2O$ thin film. Here, for grain boundary scattering a grain size ($L$) of 100 nm is used based on the scanning electron microscopy image shown in my previous work [71], while $\Phi_B$ is set at 35 meV. The latter value is chosen to fall between the values of $\Phi_B$ previously reported for H:$Cu_2O$ (64 – 80 meV) [104] and those reported

for polysilicon (5 – 22 meV) [75]. I find that for the *pc*-$Cu_2O$ thin film, neutral impurity scattering and grain boundary scattering are the dominant scattering mechanisms. It was previously observed that, for wide bandgap materials with deep dopants, the effect of the neutral impurity becomes dominant as the dopant concentrations increase [122]. Since I did not consider intrinsic donors, extrinsic donors, or neutral defect complexes, the calculated $\mu_{ii}$ and $\mu_N$ represent an upper bound on mobility. I previously confirmed [71] via conductive atomic force microscopy that the grain boundaries are insulating compared to grains themselves. This supports my finding here that grain boundary scattering is one of the main factors limiting Hall mobility. Therefore, in order to increase the Hall hole mobility of *pc*-$Cu_2O$ thin films, it is necessary to decrease $N_A$ and other neutral scattering sites, as well as increase the crystalline grain size.

Figure 3.2(b) shows the measured Hall hole mobility for the *sc*-$Cu_2O$ bulk substrate. The *sc*-$Cu_2O$ bulk substrate showed higher Hall mobility (42.6 $cm^2V^{-1}s^{-1}$) compared to the *pc*-$Cu_2O$ thin film (10.3 $cm^2V^{-1}s^{-1}$) at 300 K, likely due to the absence of grain boundary scattering and reduced impurity scattering. When modelling *sc*-$Cu_2O$, since the sample is single-crystalline I neglect grain boundary scattering but consider all other types. I find that the dominant scattering mechanism is optical phonon scattering. I also observe that, since total acceptor concentration and $p_{Hall}$ are much higher in *pc*-$Cu_2O$ than in *sc*-$Cu_2O$ (Figure 3.1), the impact of ionized impurity scattering and especially neutral impurity scattering (from non-ionized acceptors) on $\mu_{Hall}$ will be more significant in *pc*-$Cu_2O$. In contrast, these scattering mechanisms do not significantly affect hole transport in *sc*-$Cu_2O$. I note that for both *pc*-$Cu_2O$ and *sc*-$Cu_2O$, there is a difference between the scattering model and the experimental data, especially in the high temperature region. This gap may originate from the presence of additional scattering mechanisms such as piezoelectric scattering, or from non-optimized scattering parameters [119].

Surface states can also contribute to transport. In my previous work, I compared the effect of measurement ambient on thin film transistor (TFT) performance, and showed that for a 40-nm thick $Cu_2O$ TFT there was no difference in device behavior measured in air and in vacuum [71]. Since the *pc*-$Cu_2O$ films were prepared similarly in this work, I do not expect a significant surface effect in my Hall measurements, which were performed in vacuum. For the *sc*-$Cu_2O$ bulk sample, I measured Hall mobility in air and in vacuum, and found that the mobility values agree within ~7% (45.4 $cm^2V^{-1}s^{-1}$ at 295K in air; 42.6 $cm^2V^{-1}s^{-1}$ at 300K in vacuum). Thus I conclude that surface states do not play a significant role in the Hall transport results presented here.

### *3.3.3 Theoretically-estimated hole mobility*

In order to better understand phonon scattering in $Cu_2O$, our collaborators, Prof. E. Kioupakis and Dr. Zihao Deng, used first-principles calculations to calculate scattering caused by different phonon modes. To theoretically estimate the hole mobility in $Cu_2O$, we performed DFT-level carrier mobility calculations starting from the local density approximation exchange-correlation functional [123] within Quantum ESPRESSO [124]. Valence pseudopotentials were utilized, with copper having 3*d*, 4*s*, and 4*p* in the valence and oxygen having 2*s* and 2*p* in the valence. Lattice constants were relaxed and are in good agreement with experiment [83], being underestimated by only 0.66%. A plane wave cutoff of 120 Ry was found to converge the DFT band gap to 1 meV/atom and system total energy to 1 mRy/atom. Phonon frequencies were calculated using density functional perturbation theory [125] on a 6 × 6 × 6 Brillouin-zone (BZ) sampling grid. The electron-phonon coupling matrix elements were evaluated with density functional perturbation theory [125] and interpolated to fine electron-phonon BZ sampling meshes

up to 54 × 54 × 54 using maximally localized Wannier functions [126] within the Electron-Phonon-Wannier code [127]. Polar corrections to the electron-phonon matrix elements were implemented [128]. The phonon-limited hole mobility was evaluated as a function of temperature with the iterative Boltzmann Transport Equation method [129] for states within a 0.4 eV energy window below the valence band maximum.

We first studied the hole mobility in $Cu_2O$ by excluding scattering from impurities and grain boundaries. By only considering scattering from phonons, we obtain an intrinsic upper limit for the mobility.

*Table 3.1 Calculated hole mobility as a function of phonon BZ sampling grid size, illustrating the convergence of room-temperature hole mobility as the grid size increases. Reproduced from [95], with the permission of AIP Publishing.*

| phonon BZ sampling grid size | Hole mobility at 300 K ($cm^2V^{-1}s^{-1}$) |
|---|---|
| 30×30×30 | 88 |
| 48×48×48 | 103 |
| 54×54×54 | 106 |

Table 3.1 shows the calculated room-temperature hole mobility for different density BZ sampling grids. The converged hole mobility at 300 K for $Cu_2O$ was found to be 106 $cm^2V^{-1}s^{-1}$, which agrees with some of the highest experimental values reported in the literature, such as 90 $cm^2V^{-1}s^{-1}$ by Matsuzaki *et al.* [102] and 107 $cm^2V^{-1}s^{-1}$ by Zou *et al.* [42]. Only one experimental study reported a significantly higher hole mobility for $Cu_2O$ of 256 $cm^2V^{-1}s^{-1}$ [70]. Our calculations confirm the superiority of the hole mobility of $Cu_2O$ compared to other p-type oxide semiconductors.

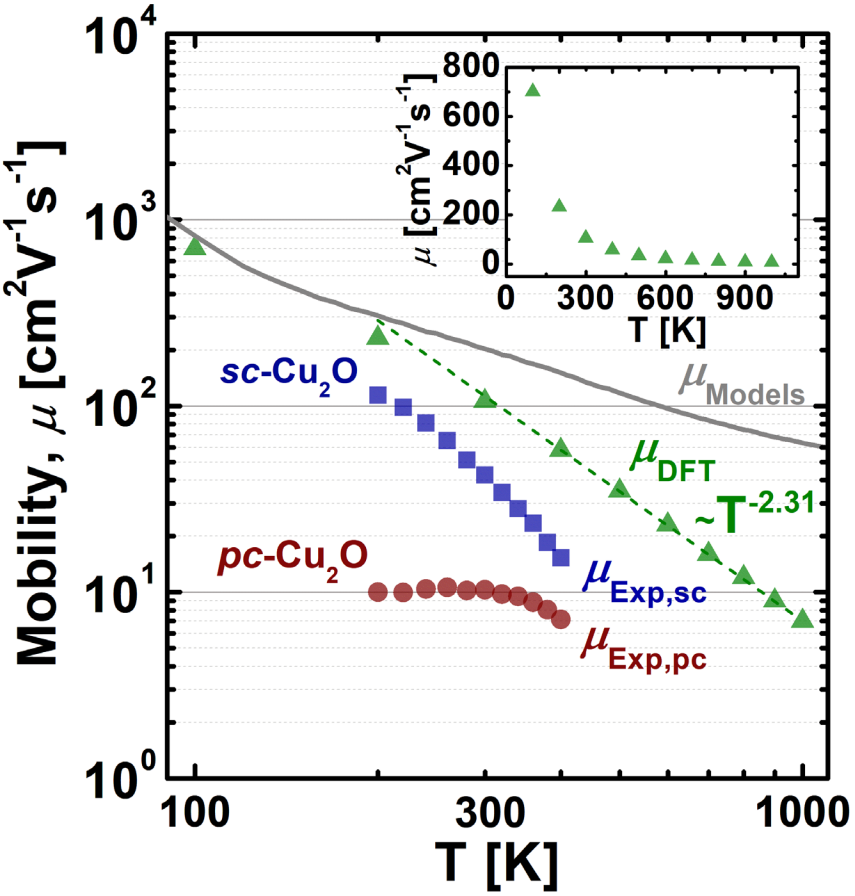



*Figure 3.4 Temperature-dependent mobility (μ vs. T), comparing experimental results from the single-crystalline (sc) $Cu_2O$ bulk substrate ($\mu_{Exp,sc}$) and polycrystalline (pc) $Cu_2O$ thin film ($\mu_{Exp,pc}$) with calculated results ($\mu_{DFT}$). The pc-$Cu_2O$ thin film sample and the sc-$Cu_2O$ bulk substrate have thickness of 20 nm and 500 μm, respectively. The grey solid line indicates the fitting model result, $\mu_{Models}$, as shown in Fig. 3.2. The green dashed line is a power law fit to the measured data from 400 K to 1000 K. In this high temperature range, the calculated mobility is proportional to $T^{-2.31}$. The inset shows a linear plot of DFT mobility vs. temperature for comparison. Reproduced from [95], with the permission of AIP Publishing.*

To understand the dominant hole scattering mechanisms, we calculated the temperature-dependent hole mobility (Figure 3.4) by iteratively solving the Boltzmann transport equation. Our calculations predict that $Cu_2O$ has a hole mobility of 702 $cm^2V^{-1}s^{-1}$ at 100 K, and the mobility is dramatically reduced to 9 $cm^2V^{-1}s^{-1}$ when the temperature is increased to 1000 K. As temperature is gradually increased, more phonon modes are thermally activated, which enhances the scattering of holes by lattice vibrations. For temperatures above 400 K, the calculated hole mobility approximately follows a $T^{-2.31}$ power law, indicating that the dominant scattering mechanism is polar optical phonon scattering [130]. The experimentally-measured mobility for *sc*-$Cu_2O$ bulk substrates shows a slightly different mobility trend as the temperature increases. This indicates that in our *sc*-$Cu_2O$ bulk substrate, it is likely that additional scattering factors besides polar optical phonon scattering are also contributing.

To gain a deeper understanding of the phonon modes that contribute to the scattering of holes in $Cu_2O$, we calculated the mode-resolved hole scattering rate as a function of hole energy. The results are shown in Figure 3.5(a). Typically, the dominant scattering mechanism at room temperature in oxide materials is polar optical phonon scattering, e.g. as in rutile-$GeO_2$ [131]. This is also the case for $Cu_2O$. When the hole energy is within 0.01 eV of the valence band maximum, the largest contribution to the scattering rate comes from a low-frequency polar mode (mode 11 with phonon energy of 17.1 meV). Another high-frequency polar mode (mode 18, 88.4 meV) has the second largest contribution, but with an order of magnitude smaller scattering rate. These two modes are primarily associated with the vibration of the light oxygen atoms (Figure 3.5(b) and (c)), and thus have a relatively high frequency. The two phonon energies calculated here (88.4 meV and 17.1 meV) are similar to the previously reported values [119]: 79.5 meV and 18.5 meV. At

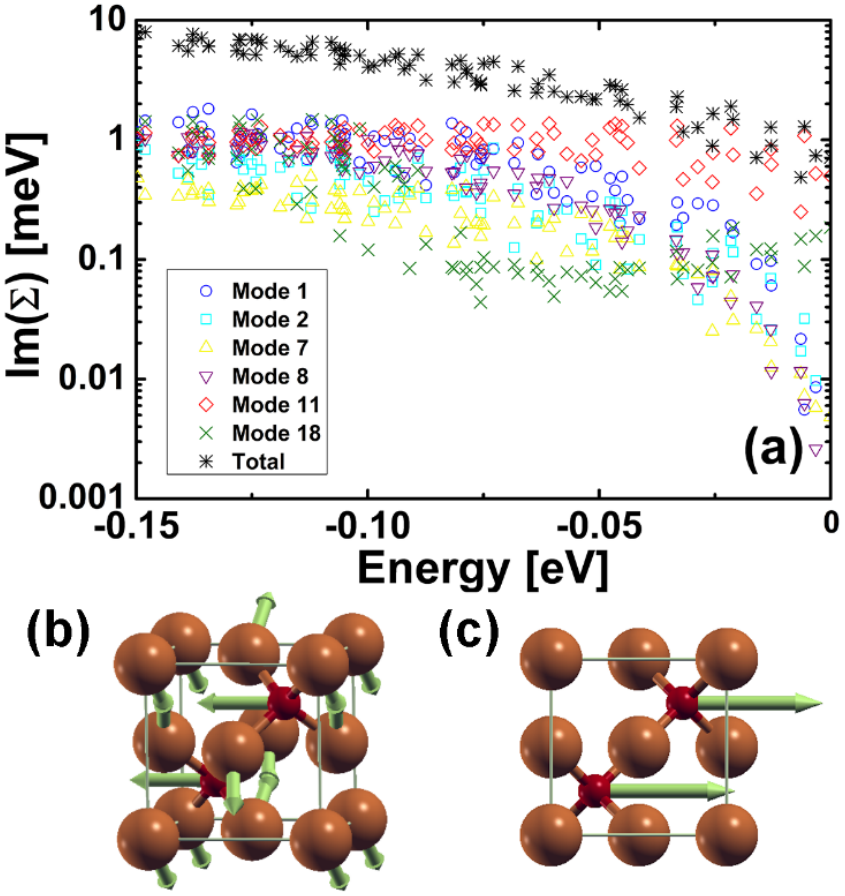



*Figure 3.5 (a) The imaginary part of the calculated hole self-energy, Σ, in $Cu_2O$, resolved by phonon mode. The y-axis corresponds to the carrier scattering rate or inverse scattering lifetime – larger values mean stronger scattering. The valence band maximum is at 0 eV on the x-axis. The total self-energy is decomposed into the contribution from the dominant phonon modes. Modes are numbered in order of increasing frequency. Modes 1–3 indicate acoustic phonons while modes 4–18 indicate optical phonons. (b) and (c) Ball and stick diagrams of atomic displacements corresponding to the dominant polar optical phonon modes 11 and 18, respectively. The large brown atoms are Cu, and the small red atoms are O. Green arrows indicate the direction of atomic vibrations. Reproduced from [95], with the permission of AIP Publishing.*

higher temperatures, when the hole energy is greater than 25 meV, two low-frequency acoustic modes (modes 1 and 2) start to have sizable hole scattering rates. This indicates that the hole mobility of $Cu_2O$ is limited by multiple phonon modes at room temperature and above. These results may explain the significant mismatch in the high temperature region between the DFT calculations and fitting model (Figure 3.4), which considers only one acoustic mode and two optical modes. We note that the room temperature mobility obtained from first-principles theory (106 $cm^2V^{-1}s^{-1}$) is more than twice that obtained by experiment for *sc*-$Cu_2O$ (42.6 $cm^2V^{-1}s^{-1}$). We attribute this discrepancy to additional scattering mechanisms present in the natural bulk crystal such as crystalline structural or point defects, incorporation of impurities that have not yet been identified, omission of quadrupole corrections in the calculations of electron-phonon scattering, which have only recently been implemented in first-principles codes [132], and typical error in the evaluation of material parameters with DFT, such as the carrier effective masses, that directly affect the calculated mobility values [129].

### 3.4 Conclusion

To summarize, I have experimentally investigated hole transport and scattering mechanisms in $Cu_2O$ by comparing temperature-dependent Hall measurements of an RF-sputtered *pc*-$Cu_2O$ thin film with a *sc*-$Cu_2O$ bulk substrate and interpreting the results using first-principles calculations as well as analytical models. I showed that for *sc*-$Cu_2O$ bulk substrates, the Hall mobility was mainly limited by phonon scattering. Our calculations showed that bulk intrinsic $Cu_2O$ can have a high hole mobility of 106 $cm^2V^{-1}s^{-1}$, and that the phonon modes that most strongly contribute to hole mobility have phonon energies of 88.4 meV and 17.1 meV. On the other hand, for *pc*-$Cu_2O$ thin films the dominant scattering mechanism is neutral impurity

scattering from acceptors, while another significant factor is grain boundary scattering. Therefore, to obtain p-type $Cu_2O$ thin films with hole mobility approaching that of bulk substrates, it is critical to increase grain size and to reduce the concentration of intrinsic acceptors to minimize the effect of neutral defects. This may be achievable by increasing the deposition temperature or annealing temperature, within the thermal budget required by the application. Furthermore, new approaches to control intrinsic acceptors, extrinsic donors, and neutral defect complexes also may be required. Finally, more work is needed to correlate thin film process conditions with hole transport and scattering mechanisms in order to improve p-type semiconductor properties to realize future electronic devices.

# Chapter 4 Process Temperature Effect on p-type RF Sputtered $Cu_2O$ Thin Film Transistors

## 4.1 Introduction

Process temperature is critical factor for many key thin film electronics applications. For instance, applications such as back-end-of-line devices on silicon metal-oxide-semiconductor field effect transistor (MOSFET) and flexible device platforms require a relatively low thermal budget to protect front-end-of-line Si MOSFETs and interconnects or to use new types of substrates instead of a silicon wafer. In previous studies [92], it was observed that the electrical characteristics of $Cu_2O$ thin films were highly affected by process temperatures and conditions. To use this material for diverse applications, each with a unique thermal budget, it is critical to understand the effect of process temperature on $Cu_2O$ thin films. Thus, in this chapter, I investigated the electrical and material properties of sputtered $Cu_2O$ thin films deposited at different temperatures and under varying deposition conditions.

## 4.2 Experimental Methods

*Table 4.1 Copper oxide thin film deposition conditions described in this chapter along with the films' dominant crystal structures, as determined by XRD. Each column represents a unique set of process conditions. Here, $T_{Dep}$ is the deposition temperature, $T_{PDA}$ is the temperature of the post-deposition anneal (PDA), and PP is the deposition process pressure. RT indicates room temperature (no intentional heating.)*

| Condition | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| Sputter target | Cu | Cu | Cu | Cu | Cu | Cu |
| $T_{Dep}$ (°C) | RT | 200–450 | 600 | RT | RT | RT |
| $T_{PDA}$ (°C) | No PDA | No PDA | No PDA | 400 | 500 | 600 |
| RF power (W) | 300 | 300 | 300 | 300 | 300 | 300 |
| PP (mTorr) | 5 | 5 | 5 | 5 | 5 | 5 |
| $O_2$:Ar | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 | 0.20 |
| XRD | $Cu_2O$ | $Cu_2O$+CuO | $Cu_2O$ | Unknown | $Cu_2O$+CuO | $Cu_2O$ |

| Condition | G | H | I | J | K | L | M |
|---|---|---|---|---|---|---|---|
| Sputter target | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ |
| $T_{Dep}$ (°C) | RT–200 | 400 | 400 | 400 | 400 | 400 | 400 |
| $T_{PDA}$ (°C) | No PDA | No PDA | No PDA | 400 | No PDA | No PDA | No PDA |
| RF power (W) | 300 | 300 | 300 | 300 | 300 | 300 | 300 |
| PP (mTorr) | 5 | 5 | 5 | 5 | 4–2 | 5 | 5 |
| $O_2$:Ar | 0 | 0 | 0.02 | 0.02 | 0.027–0.056 | 0.025–0.030 | 0.035–0.05 |
| XRD | $Cu_2O$ | Cu+$Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$ | $Cu_2O$+CuO |

To understand the effect of process temperature on $Cu_2O$ thin films, diverse $Cu_2O$ thin films were prepared under different conditions using RF magnetron sputtering (RFMS). A Kurt J. Lesker PRO Line PVD 75 was used to sputter the films. The $Cu_2O$ thin films were prepared using a Cu(99.99%) metal target or a $Cu_2O$(99.9%) target. I varied the deposition temperature ($T_{Dep}$), the post-deposition anneal temperature ($T_{PDA}$), the RF power, the sputtering process pressure, the $O_2$:Ar ratio during sputtering, and the deposition time. Process parameters for each film described in this chapter are shown in Table 4.1. Here we compare $Cu_2O$ films deposited at room temperature, 400 °C, and 600 °C. Note that other deposition conditions must change as deposition temperature

is varied in order to obtain $Cu_2O$-phase films. For instance, for the column K conditions, the process pressure was varied while keeping the oxygen flow constant (causing a change in the $O_2$:Ar ratio), in order to obtain films with $Cu_2O$ phase. The PDA was performed in the RFMS chamber, in vacuum, for 10 mins. After deposition, all thin film had a thickness of 20–25 nm. Note that throughout this chapter, when using the term "process temperature," $T_{proc}$, we mean the maximum temperature that was used during film processing, i.e., $T_{proc} = \max(T_{Dep}, T_{PDA})$.

To understand the electrical properties of thin films made with different process temperature, we fabricated thin film transistors (TFTs) and Hall samples and measured the field effect mobility and Hall mobility. To make $Cu_2O$ thin film transistors, the $Cu_2O$ thin films were deposited on $SiO_2$/Si substrates. This forms a back-gate structure with a 100-nm $SiO_2$ gate oxide. The $Cu_2O$ channel layer was patterned using a wet etch. Then, metal layers, comprised of 20 nm nickel and 80 nm gold, were deposited using e-beam evaporation and patterned via photolithographic lift-off to form the source/drain contacts. To prepare the Hall samples, $Cu_2O$ thin films were deposited on glass wafers and wet etched to form van der Pauw (vdP) patterns. The metal contacts to the vdP structures were formed using a liftoff photolithography process, using the same metallization process used for TFTs.

For material analysis, grazing incidence X-ray diffraction (GIXRD) and scanning electron microscopy (SEM) measurements were performed to investigate crystallinity and grain size/surface morphology. Time-of-flight secondary ion mass spectrometry (ToF-SIMS) was used to analyze the atomic composition. For electrical measurements, I used an HP4156A semiconductor parameter analyzer for TFT *I-V* measurements and an Accent HL5500PC Hall measurement for Hall measurements. All electrical measurements were performed in air, in the

dark, at room temperature. Finally, characterization of the films' optical properties was carried out by ellipsometry.

## 4.3 Results and Discussions

### *4.3.1 Material properties as a function of process temperature*

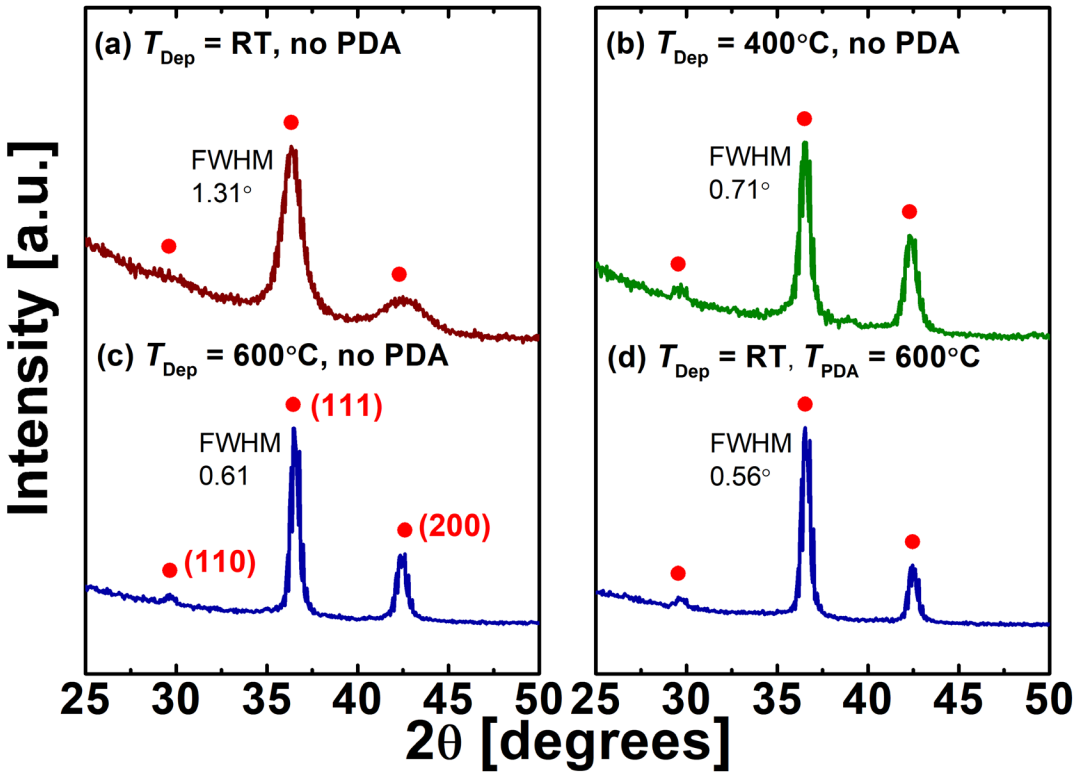



*Figure 4.1 XRD results, normalized to the same height. The $Cu_2O$ thin films were prepared with (a-c) different deposition temperature and (d) with a post-deposition anneal. The film deposition conditions used for (a, b, c, and d) correspond to columns A, I, C, and F, respectively, in Table 4.1. The full width at half maximum (FWHM) values shown in each plot were calculated for the (111) peak.*

To study the effect of process temperature on $Cu_2O$ thin films, I first deposited $Cu_2O$ thin films at room temperature, 400 °C, and 600 °C. To obtain the $Cu_2O$ phase with (111) dominant peaks at these three different deposition temperatures, I had to use different deposition conditions, as listed in Table 4.1. As shown in Figure 4.1, according to XRD all three films have $Cu_2O$ phase. As the process temperature increased, a narrower (111) peak was observed. The full width at half

maximum (FWHM) of the (111) peak decreased from 1.31° to 0.61° as the deposition temperature increased from RT to 600 ℃. Since the peak width is inversely proportional to the crystallite size [133], it is expected that the 600 ℃ $Cu_2O$ thin film must have a larger grain size than the RT $Cu_2O$ thin film. It is interesting to explore whether the film obtained via deposition at 600 ℃ is equivalent to that deposited at room temperature but annealed (PDA) at 600 ℃. As shown in Figure 4.1(c, d), while the two films have similar relative peak heights, the $Cu_2O$ thin film that was deposited at room temperature followed by a PDA at 600 ℃ (condition F) has a slightly narrower FWHM of 0.56° compared to the $Cu_2O$ deposited at 600 ℃ with no PDA (condition C), which has a FWHM of 0.61°.

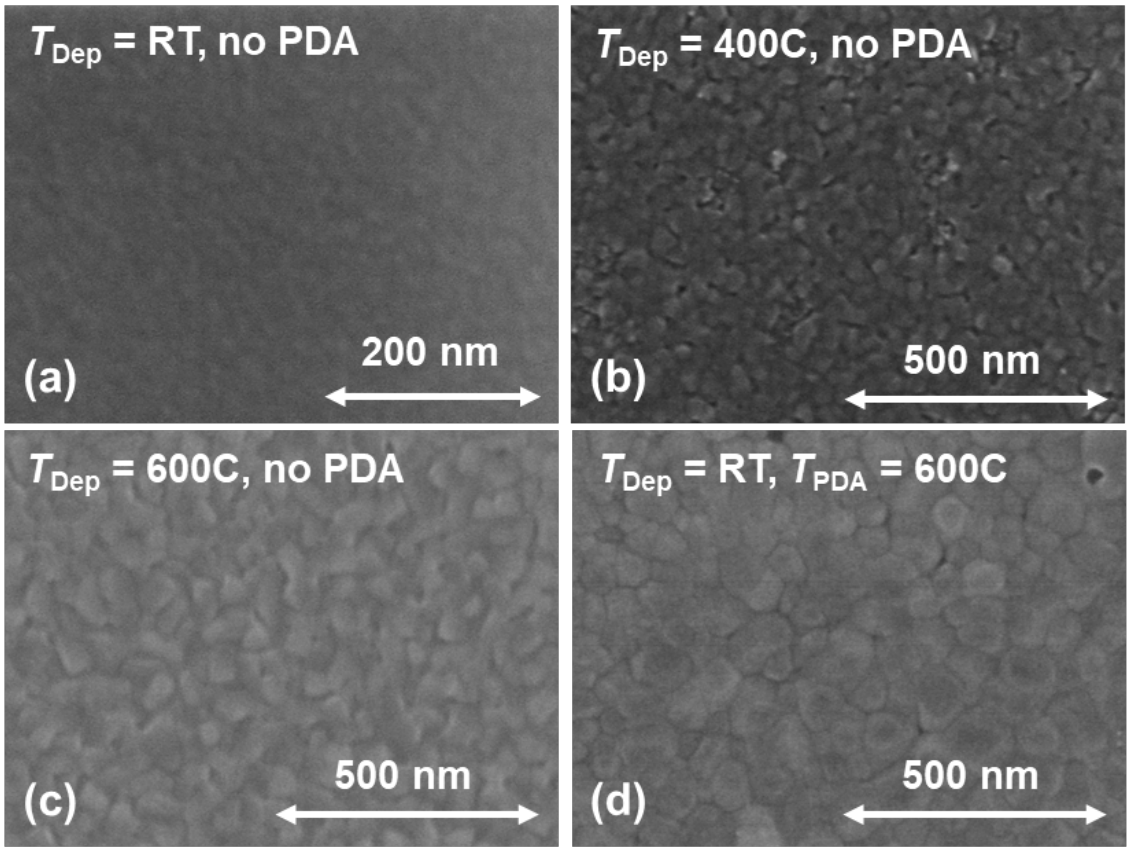



*Figure 4.2 Scanning electron microscopy (SEM) images of $Cu_2O$ thin films made with different deposition temperatures ($T_{Dep}$) and post-deposition anneal temperature ($T_{PDA}$). The $Cu_2O$ thin films were deposited at (a) room temperature, (b) 400 ℃, (c) 600 ℃. The film shown in (d) was deposited at room temperature and annealed at 600 ℃. The film deposition conditions used for (a, b, c, and d) correspond to columns A, I, C, and F, respectively, in Table 4.1. As shown in Table 4.1, for these four films, the $O_2$:Ar ratio was varied in order to obtain $Cu_2O$ phase.*

The $Cu_2O$ grain morphology and grain size in the thin films was investigated using SEM. Figure 4.2 shows SEM images of the surfaces of $Cu_2O$ thin films made using different deposition temperatures ($T_{Dep}$) and post-deposition anneal temperature ($T_{PDA}$). As seen in Figure 4.2(a-c), as $T_{Dep}$ increased from RT to 600 °C, the grain size increased. While both Figure 4.2(c) and (d) have the same maximum process temperature of 600 °C, the differing process conditions for the two films led to different surface morphology. The average grain size of the film that was deposited at room temperature followed by a PDA at 600 °C (Figure 4.2(d)) is larger than that of a $Cu_2O$ film deposited at 600 °C with no PDA (Figure 4.2(c)). This trend agrees with the XRD FWHM results discussed above.

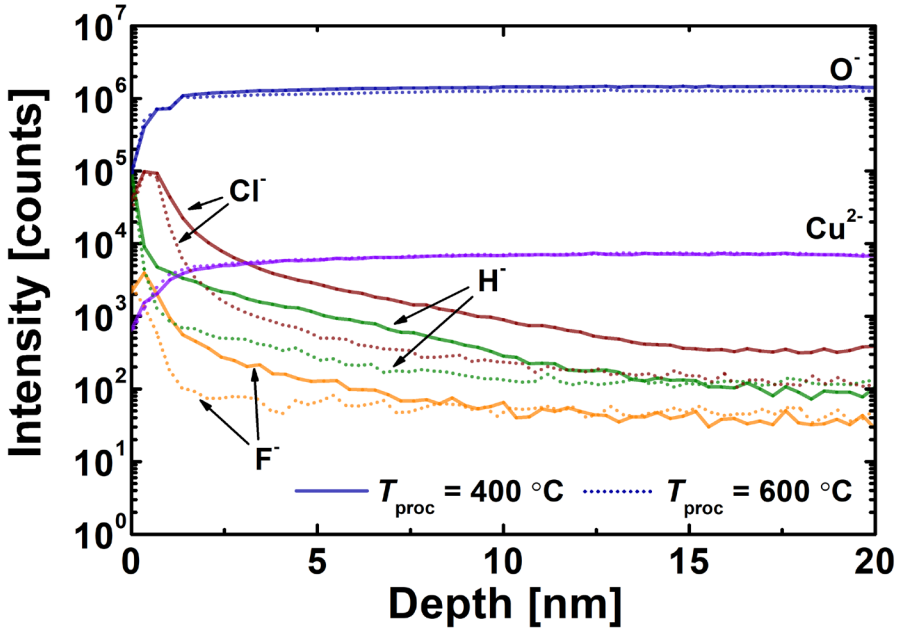



*Figure 4.3 ToF-SIMS measurement of ion depth profiles for two $Cu_2O$ films. The solid lines indicate data from the film made with deposition temperature ($T_{Dep}$) of 400 °C without a post-deposition anneal (PDA), while the dashed lines indicate the film deposited at room temperature with $T_{PDA}$ = 600 °C. These film deposition conditions correspond to columns I and F, respectively, in Table 4.1.*

We also compared the effect of process temperature on the incorporation of impurities. As shown in Figure 4.3, ToF-SIMS detected a similar level of host ions (O and Cu) for both the 400 ℃- (condition I) and 600 ℃-processed (condition F) thin films, which is expected since both films have $Cu_2O$ phase. On the other hand, different impurity levels were detected in the two films. The film deposited at 600 ℃ has lower levels of hydrogen, fluorine, and chlorine. It is suspected that the higher process temperature suppressed their incorporation or allowed them to be removed from the film during the process. In particular, a 4× reduction of Cl was observed at the interface between $Cu_2O$ and $SiO_2$ (i.e., at a depth of approximately 20 nm). As discussed in Chapter 3, hydrogen, fluorine and chlorine each [64], [134] can act as donors in p-type $Cu_2O$ by compensating the intrinsic acceptor, copper vacancies [62]. Thus, the greater concentration of Cl in the 400 ℃ film may negatively affect hole transport and device performance. In addition, the presence of these impurities may increase neutral or ionized impurity scattering [71] by increasing the concentration of scattering sites. So, controlling impurities may be critical to maximize the mobility of $Cu_2O$ thin films for a given thermal budget.

### *4.3.2 Electrical properties as a function of process temperature*

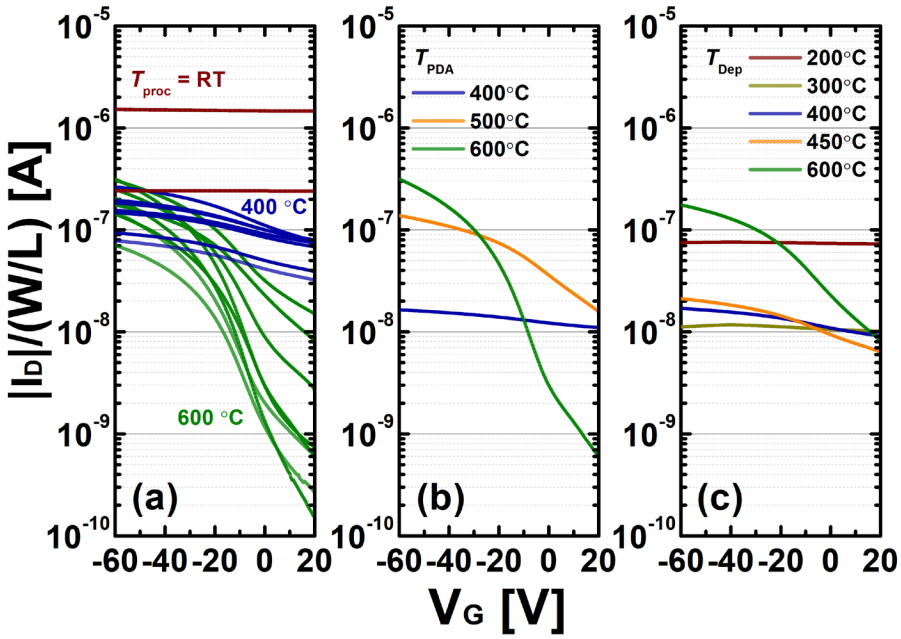



*Figure 4.4 Normalized drain current, $I_D \cdot (W/L)^{-1}$, versus gate voltage ($V_G$) of various p-type $Cu_2O$ thin film transistors: (a) compares films made with different processes (conditions A, C, F, and I–L from Table 4.1), where the labelled process temperature indicates the maximum of the film deposition temperature and PDA temperature; (b) compares films with different post-deposition temperature ($T_{PDA}$) (conditions D–F); (c) compares films with different deposition temperature ($T_{Dep}$) (conditions B and C). A drain voltage ($V_D$) of −10 V was used for all measurements. Note that, for (a), the 400 °C $Cu_2O$ films were prepared using a $Cu_2O$ target and, for the RT and 600°C films in (a) and for all films shown in (b) and (c), the films were deposited using a Cu target.*

Next, $Cu_2O$ thin film transistors (TFT) were fabricated to evaluate the films' electrical characteristics. To assess the impact of process conditions on electrical performance, TFTs were fabricated with various $T_{Dep}$, $T_{PDA}$, process pressure, and $O_2$:Ar ratios. Note that, as discussed in the Table 4.1, $Cu_2O$ films processed at RT and 600°C were deposited using Cu metal target (conditions A–F) and $Cu_2O$ films at 400°C were deposited using $Cu_2O$ target (conditions G–M) to obtain pure $Cu_2O$ phase. Figure 4.4(a) shows all of the $Cu_2O$ TFT results as a function of the maximum process temperature. The as-deposited $Cu_2O$ TFTs (the line labelled $T_{proc}$ = RT, condition A) did not show field effect behavior. As the process temperature increased to 400 °C (condition I–L), the TFTs started to show field effect behavior. As the process temperature increased again to 600 °C (condition C and F), the on/off current ratio increased.

Figure 4.4(b) shows *I-V* curves for $Cu_2O$ TFT made of films with different post-deposition anneal (PDA) temperature (conditions D–F with Cu metal target). For PDA below 600 °C, the film showed a $Cu_2O$+CuO mixed phase; it was not pure $Cu_2O$. Similarly, for depositions done using a Cu target with different deposition temperatures (Figure 4.4(c)) (conditions B and C), we obtained pure $Cu_2O$ phase only at 600 °C. Regardless of the copper oxide phase, a higher deposition temperature or a higher PDA temperature led to improved field effect behavior. We note that $Cu_2O$ and CuO typically have different electrical properties. As discussed in the Section 2.3.2, the $Cu_2O$ phase is more suitable for TFT applications than the CuO phase due to its lower effective mass and moderate carrier concentration [71]. CuO tends to be heavily doped via intrinsic Cu vacancies which act as acceptor-like defects [44], [78], and it has a higher effective mass, compared to $Cu_2O$ [79]. In addition, $Cu_2O$ has wider bandgap ($E_G$ = 2.1–2.7 eV [33]) compared to CuO ($E_G$ = 1.1–1.4 eV [135], [136]). Thus, to achieve high performance wide-bandgap p-type oxide TFTs, for the remainder of our discussion we mainly focus on phase-pure $Cu_2O$ thin films made using different process temperatures.

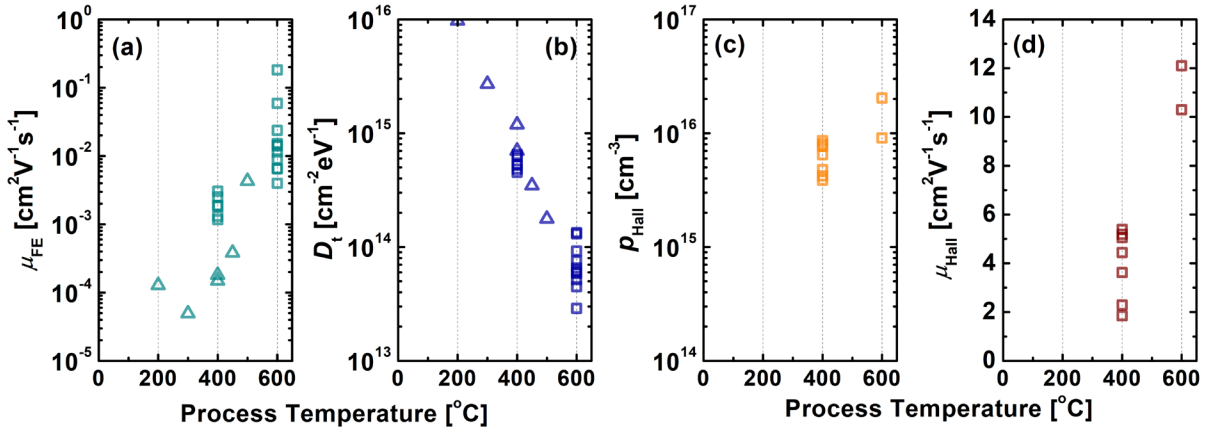



*Figure 4.5 The extracted (a) field effect mobility ($\mu_{FE}$) and (b) trap density ($D_t$), extracted from the I-V curves shown in Figure 4.4. The trap density includes both interface traps and grain boundary traps. The square symbols and triangle symbols indicate results obtained from $Cu_2O$ phase and $Cu_2O$+CuO mixed phase films, respectively. The measured (c) Hall carrier concentration and (d) Hall mobility of $Cu_2O$ thin films made with different process temperature. The Hall measurement results for 600 °C-$Cu_2O$ are the same as those described in Sections 2.3.3 and 3.3.2 [71], [95]. In Table 4.1, the film deposition conditions used for (a) and (b) are columns B–F and I–M, and the conditions used for (c) and (d) are F and I–L.*

To evaluate the TFT performance quantitatively, we extracted the field effect mobility and trap density from the Figure 4.4 results. The results are shown in Figure 4.5(a). As described in Section 2.3.3, the field effect mobility was calculated using the following equation (3.1):

$$\mu_{FE} = \left(\frac{dI_D}{dV_{GS}}\right)\left(\frac{C_{OX}V_{DS}W}{L}\right)^{-1}, \tag{3.1}$$

where $I_D$ is the drain current, $V_D$ is the drain voltage, $C_{OX}$ is the gate oxide capacitance per unit area, $W$ is the channel width, and $L$ is the channel length. The calculated field effect mobility ranges from 0.001 to 0.005 $cm^2V^{-1}s^{-1}$ for 400 ℃-$Cu_2O$ thin films and from 0.004 to 0.060 $cm^2V^{-1}s^{-1}$ for the 600 ℃-$Cu_2O$ thin films. The field effect mobility tends to increase with increasing process temperature. The 400 ℃ thin film samples that have $Cu_2O$+CuO mixed phase have lower field effect mobility than $Cu_2O$ samples possibly due to larger effective mass of CuO.

Figure 4.5(b) shows the calculated trap density ($D_t$). This value is extracted from the minimum subthreshold slope, *SS*, of the TFT via the following equation (3.2) as described in Section 2.3.3:

$$D_t = \left(\frac{SS\log_{10}e}{kT/q} - 1\right)\frac{C_{OX}}{q}, \tag{3.2}$$

where $k$ is the Boltzmann constant, $T$ is the temperature, $q$ is the electronic charge, and $C_{OX}$ is the gate oxide capacitance. The $D_t$ for polycrystalline $Cu_2O$ TFTs arises from both interface traps and grain boundary traps. The $D_t$ for the 600 ℃ $Cu_2O$ thin films ($2.9\times10^{13}$–$1.3\times10^{14}$ $cm^{-2}eV^{-1}$) is lower than that of the 400 ℃ $Cu_2O$ thin film ($3.6$–$6.5\times10^{14}$ $cm^{-2}eV^{-1}$). The lower $D_t$ possibly originates from the increased grain size. For polycrystalline TFTs, grain boundaries are considered a key trap site [137]. In addition, increasing the processing temperature may reduce the density of dangling bonds at the channel-to-dielectric interface. The high $D_t$ of the 400 ℃ $Cu_2O$ thin film can lead to a low field effect mobility by impeding hole transport at the interface [71].

To increase our understanding of the electrical properties of the $Cu_2O$ thin films, we performed Hall measurements of samples processed at different temperatures (conditions I–L and F). As shown in Figure 4.5(c) and (d), the Hall mobility of 400 ℃ $Cu_2O$ thin film varies from 1.85 to 5.39 $cm^2V^{-1}s^{-1}$ depending on the deposition conditions (i.e., process pressure and $O_2$:Ar ratio), while $Cu_2O$ films prepared at 600 ℃ have higher hole mobility, ranging from 10.3 to 12.1 $cm^2V^{-1}s^{-1}$ [71], [95]. The corresponding Hall hole concentration was 4–9×$10^{15}$ $cm^{-3}$ for 400 ℃ $Cu_2O$ thin films and 9×$10^{15}$–2×$10^{16}$ $cm^{-3}$ for the 600 ℃ $Cu_2O$ thin films. In comparing the TFT results and Hall measurement results, we speculate that the improved Hall mobility may originate from the increased grain size which reduces the trap density. The higher Hall mobility is also likely facilitated by the reduced impurity level. There is a large gap between the measured field effect mobility and Hall mobility. This discrepancy may come from non-idealities in the TFTs, as described in Section 2.3.3 [71].

For back-end-of-line devices on top of silicon MOSFET, the maximum process temperature is typically considered to be ~450 ℃ [138]. To determine the suitability of $Cu_2O$ material for low process temperature applications, we investigated the impact of varying deposition conditions while keeping the process temperature set at 400 ℃ (conditions I–L). As the $O_2$:Ar ratio increases from 0.020 to 0.030 at the same process pressure of 5 mTorr (conditions I and L), the Hall mobility decreased from 3.62 to 1.85 $cm^2V^{-1}s^{-1}$. The corresponding hole carrier concentration increased from 6.5×$10^{15}$ $cm^{-3}$ to 8.6×$10^{15}$ $cm^{-3}$. The increased $O_2$:Ar ratio seems to increase the intrinsic acceptor concentration (i.e., copper vacancies). This may reduce the Hall mobility by increasing impurity scattering.

It was previously reported that the electrical properties of $Cu_2O$ thin films depend on their orientation. Previous work [139] showed that [100]-oriented thin films (i.e., exhibiting a dominant

$Cu_2O$(200) XRD peak) showed higher Hall mobility with more dense surface morphology than [111]-oriented thin films (i.e., with $Cu_2O$(100) XRD peak). In the future, the orientation can be controlled by modifying process parameters including the oxygen flow and process pressure [140].

Our work on 400 ℃ thin films indicates that it is important to optimize process conditions to maximize thin film mobility. Nonetheless, as shown in Figure 4.4, weak field effect behavior was observed for 400 ℃ thin films possibly due to the excessively high trap level of $> 10^{14}$ $cm^{-2}eV^{-1}$. Further work is required to reduce the high trap density to maximize device performance within the BEOL thermal budget.

The $Cu_2O$ thin films made with a maximum process temperature of 600 ℃ showed a wide range of electrical performance. As we observed in the material analyses above, the materials properties are affected by whether the maximum process temperature occurs during deposition or PDA (i.e., it depends whether it is $T_{dep}$ or $T_{PDA}$). The $Cu_2O$ thin film with $T_{PDA}$ = 600 ℃ (condition F) showed a significantly higher field effect mobility (up to 0.060 $cm^2V^{-1}s^{-1}$) than that obtained with $T_{Dep}$ = 600 ℃ (~0.007 $cm^2V^{-1}s^{-1}$) (condition C). As shown in Figure 4.2, these films have different structural properties: a larger grain size was observed when $T_{PDA}$ = 600 ℃. The corresponding FWHM of (111) peak was 0.56° for $Cu_2O$ with $T_{Dep}$ = 600℃ and 0.61° for $Cu_2O$ with $T_{Dep}$ = 600 ℃. For these reasons, although the process temperature is kept the same, a wide range of field effect and Hall mobility value were observed at each process temperature.

### *4.3.3 Optical properties as a function of process temperature*

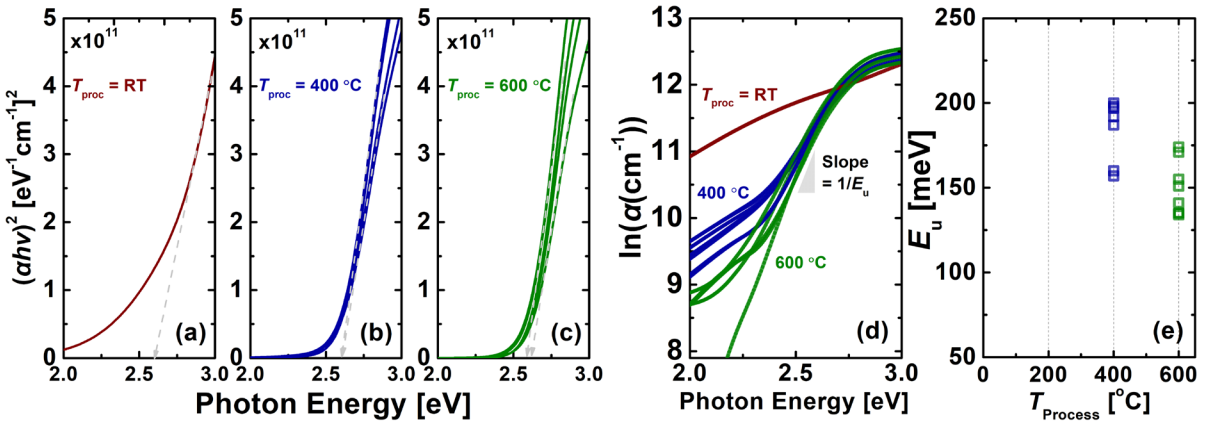



*Figure 4.6 Optical properties of $Cu_2O$ thin films with different process temperatures. Here, the process temperature indicates the maximum temperature of the deposition temperature ($T_{Dep}$) and post-deposition anneal temperature ($T_{PDA}$). Tauc plots, $(\alpha h\upsilon)^2$ versus photon energy, for (a) RT, (b) 400°C, and 600°C $Cu_2O$ thin films. (d) $\ln(\alpha(cm^{-1}))$ versus photon energy plot and (e) Urbach energy for films made with different process temperatures. The film deposition conditions used for RT, 400°C, and 600°C samples correspond to columns A, I–L, and C, F, respectively, in Table 4.1.*

To gain insight into the structural disorder of $Cu_2O$ thin films, optical analysis was performed. Based on Tauc plots (Figure 4.6(a-c)), the estimated energy band gap size was ~2.6 eV for all $Cu_2O$ thin films. This confirms their $Cu_2O$ phase. The optical data was analyzed to determine the Urbach energy [92], [141]. The Urbach energy is one way to quantify the energetic disorder present in a film. It can be evaluated by fitting the following equation (3.3) to the measured data:

$$\alpha(\nu) = \alpha_0 \exp\left(\frac{h\upsilon}{E_u}\right), \tag{3.3}$$

where $\alpha$ is the absorption coefficient, $h$ is Planck's constant, $h\upsilon$ is the photon energy, $\alpha_0$ is a constant, and $E_u$ is the Urbach energy. The value of $E_u$ can be obtained by taking the inverse of the slope of $\ln(\alpha)$ vs. $h\upsilon$. As shown in Figure 4.6(d-e), the 600 °C $Cu_2O$ film has a sharper Urbach tail than the films made at lower temperatures. The corresponding $E_u$ was 157–200 meV for 400 °C $Cu_2O$ thin films and 134–174 meV for 600 °C $Cu_2O$ thin films. This means that $Cu_2O$ thin films processed at higher process temperatures tends to have lower structural disorder. Previous work

[139] showed that the Urbach energy depends on not only the temperature but also on the thin film orientation. These optical results are thus consistent with the trap analysis results discussed above.

### 4.4 Conclusions

In this work, we investigated effect of process temperature on $Cu_2O$ thin films and their transistors by characterization the materials properties and electrical properties. As the process temperature increases, better crystallinity was observed with a larger grain size. In addition, higher process temperatures more effectively reduced the defect state concentration. In the electrical domain, $Cu_2O$ thin films processed at higher temperatures have a higher field effect mobility and a lower density of traps. However, for a given temperature, a wide range of field effect mobility and Hall mobility values were observed. Thus, future work is needed to fully optimize the deposition conditions. Finally, optical analysis showed that higher process temperature is correlated with a lower defect concentration. In understanding the impact of process temperature on material and electrical properties, this work provides key insights into the thermal budget required to realize $Cu_2O$ thin film-based electronics.

## Chapter 5 N:$Cu_2O$ S/D to reduce contact resistance of p-type $Cu_2O$ thin film transistor

### 5.1 Introduction

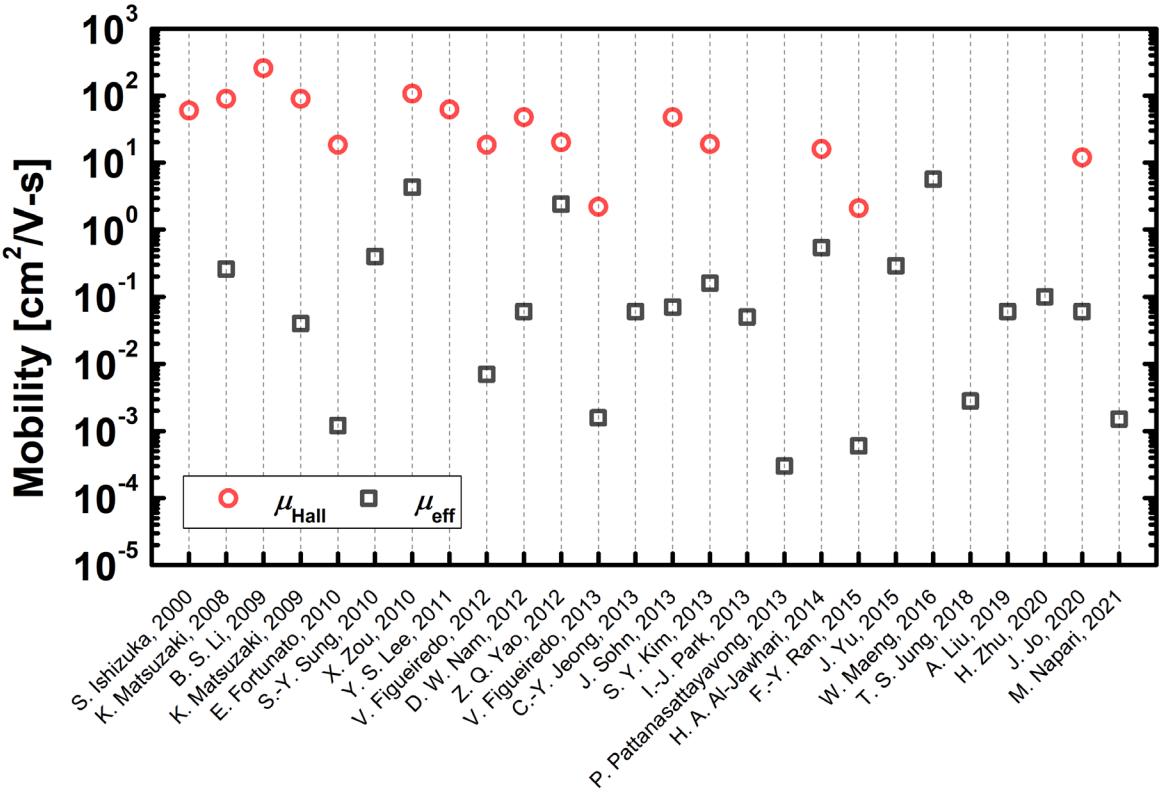



*Figure 5.1 Reported values for Hall mobility ($\mu_{Hall}$) of $Cu_2O$ thin films and effective mobility ($\mu_{eff}$) of $Cu_2O$ thin film transistors. The mobility data is taken from refs [42], [50], [54], [55], [57], [58], [60], [67], [70], [71], [102], [113], [142]–[154].*

As we have shown in the previous chapters, RF sputtering at room temperature followed by post-deposition anneal at 600°C can be used to obtain cuprous oxide ($Cu_2O$) with a reasonably high Hall hole mobility of > 10 $cm^2V^{-1}s^{-1}$ and a bandgap > 2 eV. However, I found that the field

effect mobility ($\mu_{eff}$) of the corresponding TFT is much lower than the Hall mobility ($\mu_{Hall}$) of the same $Cu_2O$ film. As explained in Chapter 2, the low $\mu_{eff}$ value mainly originates from high contact resistance and interface traps. Similar observations – of much lower field effect mobility ($\mu_{eff}$) compared to Hall mobility ($\mu_{Hall}$) for $Cu_2O$ – have been reported for more than 20 years (Figure 5.1) [42], [50], [54], [55], [57], [58], [60], [67], [70], [71], [102], [113], [142]–[154]. Nonetheless, the high intrinsic mobility of $Cu_2O$ is still an attractive feature compared to other p-type oxides that have low intrinsic mobility [33]. Thus, inspired by Chapter 2 [71], here I seek to address one of the device level issues identified already – contact resistance – in order to demonstrate high performance $Cu_2O$ TFTs.

For p-type wide-bandgap oxides, the valence band maximum (VBM) tends to be located well below the vacuum level. For $Cu_2O$, the VBM is positioned ~5.49 eV below vacuum level [88]. Although some metals such as nickel (Ni), platinum (Pt), and palladium (Pd) have work functions greater than 5 eV [89], the position of the $Cu_2O$ charge neutrality level and resultant Fermi level pinning makes it hard to use work function engineering to form ohmic junctions [155]. With its charge neutrality level located 0.8 eV above the VBM [91], ohmic contacts to $Cu_2O$ require an unrealistically high metal work function of > 7 eV [71], [90]. For these reasons, previous $Cu_2O$ TFTs exhibited high contact resistance [71], [92]. The most common way to achieve stable ohmic contact when Fermi-level pinning is present is to form a tunneling barrier via heavily doping the semiconductor at the contact interface. For $Cu_2O$, a doping level of $p > 10^{19}$ $cm^{-3}$ is predicted to be required in order to achieve field emission through the potential barrier (i.e., carrier tunneling) [156]. Thus, demonstrating heavily-doped $Cu_2O$ is essential to achieve low ohmic contact resistance.

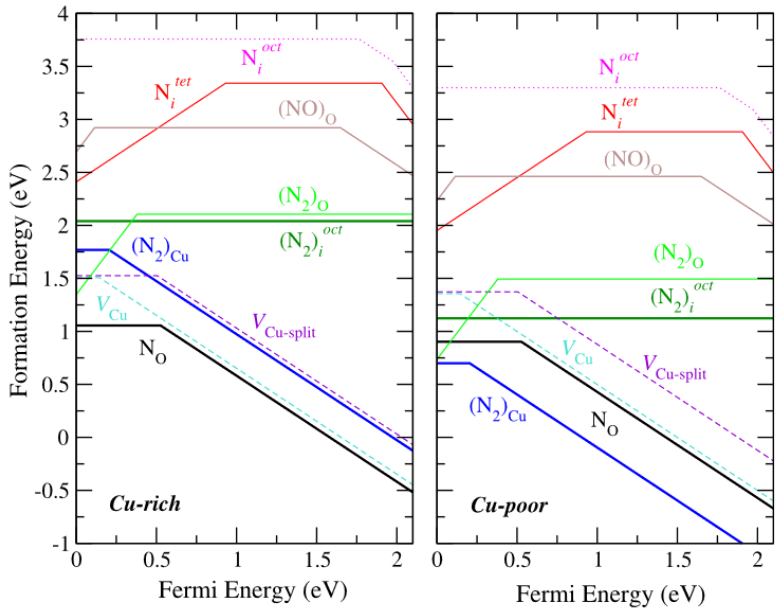


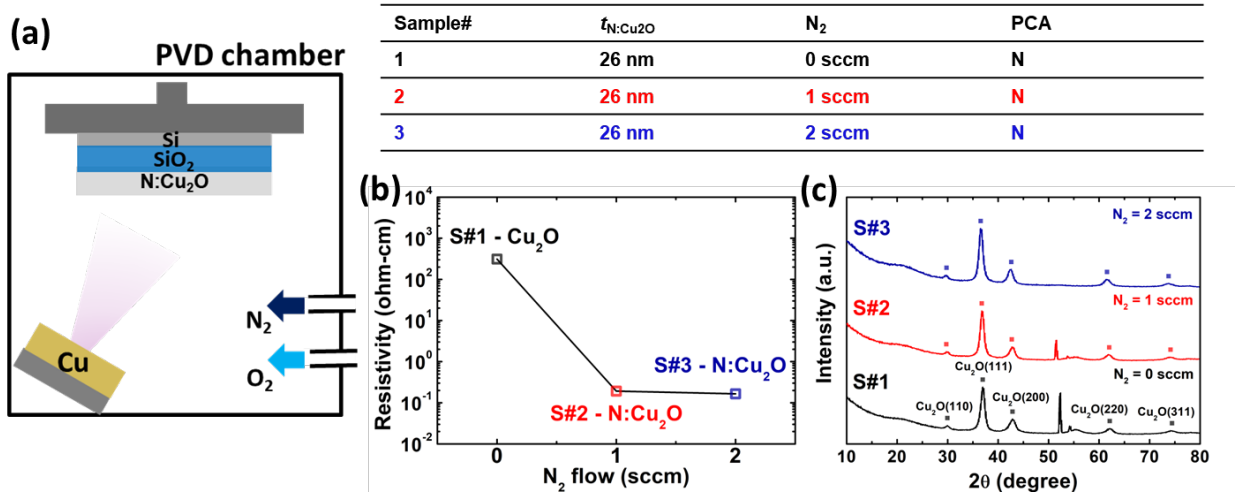

*Figure 5.2 Formation energy versus Fermi energy: role of nitrogen in $Cu_2O$. Reproduced from [157], with the permission of AIP Publishing.*

Nitrogen ($N_2$) is predicted to form a p-type dopant in $Cu_2O$ [157]. Theory predicts that the substitution of diatomic nitrogen on Cu sites ($(N_2)_{Cu}$) and nitrogen substitution on oxygen sites ($N_O$) have lower formation energies than the intrinsic acceptors of $Cu_2O$, namely the Cu simple vacancy ($V_{Cu}$) and Cu split vacancy ($V_{Cu}^{Split}$). In particular $(N_2)_{Cu}$ has a activation energy level of 0.20 eV under Cu-poor condition [157], which is lower than those of intrinsic dopants: $V_{Cu}$ = 0.23 eV and $V_{Cu}^{Split}$ = 0.47 eV [62]. Thus, the introduction of nitrogen can effectively increase the hole carrier concentration in $Cu_2O$. Previous studies have experimentally demonstrated nitrogen doping using RF magnetron sputtering [158], [159] and have confirmed the increased carrier concentration up to $> 10^{19}$ $cm^{-3}$ for N:$Cu_2O$ [159], which is higher than the reported intrinsic carrier concentration [44] of $< 10^{17}$ $cm^{-3}$. For metal-to-N:$Cu_2O$ contacts, a specific contact resistance [156] of $< 10^{-3}$ ohm-$cm^2$ was reported. This indicates that nitrogen doping may be an effective way to reduce contact resistance. Although there are some works on N:$Cu_2O$ contact

resistance layers used for photovoltaic applications [159], there are no studies of the effects of N:$Cu_2O$ on ohmic contacts in $Cu_2O$ TFTs.

Here, we demonstrate $Cu_2O$ TFTs with improved effective mobility by the addition of nitrogen-doped $Cu_2O$ (N:$Cu_2O$) source/drain interfacial layers, fabricated using room temperature RF magnetron sputtering. We explain the improvement in TFT performance by characterizing contact resistance using transfer length measurements and by measuring the effective barrier height. We found that the addition of a N:$Cu_2O$ contact layer improved $\mu_{eff}$ of our $Cu_2O$ TFTs by enabling tunneling from the metal into N:$Cu_2O$ combined with a lowered potential barrier at the N:$Cu_2O$: $Cu_2O$ valence band offset.

## 5.2 Experimental Methods




| Sample# | $t_{N:Cu2O}$ | $N_2$ | PCA |
|---|---|---|---|
| 1 | 26 nm | 0 sccm | N |
| 2 | 26 nm | 1 sccm | N |
| 3 | 26 nm | 2 sccm | N |

*Figure 5.3 (a) Schematic of the PVD chamber used to deposit N:$Cu_2O$ thin films. (b) Resistivity versus $N_2$ flow (0–2 sccm) for room temperature-deposited N:$Cu_2O$. (c) XRD results for N:$Cu_2O$ thin films with different $N_2$ flow (0–2 sccm). The table shows key sample information: sample number, N:$Cu_2O$ thin film thickness ($t_{N:Cu2O}$), $N_2$ gas flow, and post-contact anneal (PCA) condition (N=none).*

N:$Cu_2O$ thin films were prepared by RF magnetron sputtering (RFMS) using a Kurt J. Lesker PRO Line PVD 75. Copper oxide thin films were deposited on $SiO_2$/Si wafers at room

temperature under nitrogen ($N_2$) gas as shown in Figure 5.3(a). For materials characterization samples, the $O_2$ and Ar flow rates were kept constant at 2.54 sccm and 25.48 sccm, respectively, while the $N_2$ gas flow rate was varied from 0 to 2 sccm. The source was a 3-inch Cu (99.99%) metal target, the RF power was 200 W, and a deposition time of 100 s was used to obtain a film thickness of ~26 nm.

To fabricate $Cu_2O$ TFTs with N:$Cu_2O$ S/D, we first prepared a 100-nm $SiO_2$/Si wafer. A 20 nm $CuO_x$ film was deposited on the wafer using the Cu metal target with the following conditions: RF power of 300 W, $O_2$ = 5.35 sccm, Ar = 24.38 sccm, the substrate at room temperature, with a deposition time of 39 s. Next, a post-deposition anneal (PDA) was carried out in the PVD chamber at 600 ℃ in vacuum for 10 min. After that, the active layer was patterned via wet etching. Then, after photolithography to open up the source/drain areas, selective N:$Cu_2O$ regrowth was performed in the source/drain regions with $N_2$ = 1 sccm. Three different samples were prepared with N:$Cu_2O$ thickness of 5 nm, 8 nm, and 13 nm. Finally, Ni/Au contacts (20 nm/80 nm) were deposited using an e-beam evaporator. An $O_2$ plasma descum was performed before contact metal deposition. After metal deposition, a post-contact anneal (PCA) was performed at 200 ℃ in $N_2$ ambient for 1 min using a rapid thermal process tool. On each sample, in addition to TFTs, transfer length measurement (TLM) test structures were added to measure contact resistance. For the TLM test structures, the active layer was patterned and metal contacts were formed with electrode spacing varying from 10 μm to 40μm with a 5 μm step size. For four point probe measurements, a cloverleaf-shape van der Pauw configuration was used.

An HP4156A semiconductor parameter analyzer was used for TFT $I_D$ vs. $V_G$ and $I_D$ vs. $V_D$ measurements and four point probe measurements. A Keysight B1505A power device analyzer and heated substrate stage was used for TLM measurements. An Accent HL5500PC Hall

measurement system was used for Hall measurements. All electrical measurements were performed in air and in the dark. For temperature-dependent measurements, the substrate temperature was increased from 300 K to 340 K in 10 K steps. A Rigaku SmartLab XRD was used for grazing incidence X-ray diffraction (GIXRD).

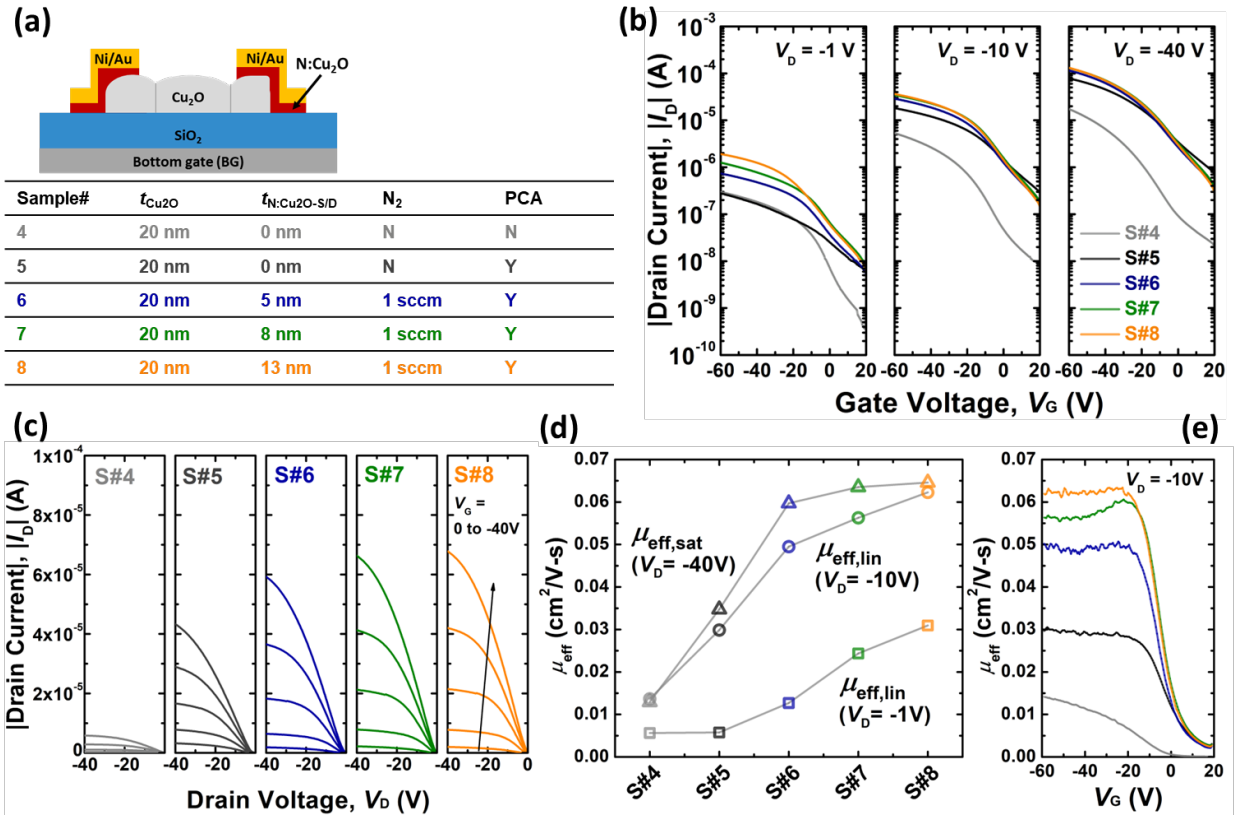
## 5.3 Results and Discussion

### *5.3.1 Development of N:$Cu_2O$ thin film*

To study N:$Cu_2O$, three thin film samples were prepared via room temperature RF magnetron sputtering using $N_2$ flow of 0 sccm (sample S#1), 1 sccm (S#2), and 2 sccm (S#3). The $Cu_2O$ thin film electrical properties were investigated via four point probe measurements using the van der Pauw configuration. As $N_2$ gas was introduced and its flow increased, the film resistivity ($\rho$) was significantly reduced (< ~1/2000×) from 312 Ω-cm to ~0.16 Ω-cm, as shown in Figure 5.3(b). Since $\rho = (q\mu_p p)^{-1}$, where $q$ is the electron unit charge, $\mu_p$ is the hole mobility, and $p$ is the hole carrier concentration, the decreased $\rho$ likely indicates an increase in p-type doping due to the incorporation of nitrogen in $Cu_2O$.

To assess the crystal phase, grazing incidence X-ray diffraction (GIXRD) was used (Figure 5.3(c)). Since a phase change can lead to changes in the bandgap that deleteriously affect band alignment between the source/drain and TFT channel, it is important to maintain the $Cu_2O$ cubic $Pn\bar{3}m$ crystal phase during nitrogen incorporation. All samples showed $Cu_2O$ phase by GIXRD regardless of the $N_2$ gas flow, which ranged from 0 to 2 sccm. This indicates that although the resistivity was dramatically lowered by nitrogen incorporation, no phase change nor phase separation occurred in the host $Cu_2O$ material.

### *5.3.2 $Cu_2O$ thin film transistor with N:$Cu_2O$ S/D interlayer*




| Sample# | $t_{Cu2O}$ | $t_{N:Cu2O-S/D}$ | $N_2$ | PCA |
|---|---|---|---|---|
| 4 | 20 nm | 0 nm | N | N |
| 5 | 20 nm | 0 nm | N | Y |
| 6 | 20 nm | 5 nm | 1 sccm | Y |
| 7 | 20 nm | 8 nm | 1 sccm | Y |
| 8 | 20 nm | 13 nm | 1 sccm | Y |

*Figure 5.4 (a) Schematic of a $Cu_2O$ TFT with a N:$Cu_2O$ contact layer, coated with a probing layer of 20 nm Ni / 80 nm Au. (b) Drain current versus gate voltage ($I_D$ vs. $V_G$) curves. (c) Drain current versus drain voltage ($I_D$ vs. $V_D$) for different gate voltages ($V_G$ = 0 V, −10 V, −20 V, −30 V and −40 V). (d) $\mu_{eff}$ of samples with different N:$Cu_2O$ contact layer thickness. (e) Effective mobility as a function of gate voltage ($\mu_{eff}$ vs. $V_G$) with $V_D$ = −10 V. The table shows key sample information: sample number, $Cu_2O$ thin film thickness ($t_{Cu2O}$), N:$Cu_2O$ contact layer thickness ($t_{N:Cu2O}$), $N_2$ gas flow, and post-contact anneal (PCA) condition (N=no, Y=yes). Samples S#4 and S#5 are $Cu_2O$ TFTs with no N:$Cu_2O$ contact layer. Sample S#5 was treated with PCA and S#4 was not. Samples S#6, S#7, S#8 are $Cu_2O$ TFTs with N:$Cu_2O$ contact layers of various thickness, and were all treated with PCA.*

Having demonstrated the feasibility of doping $Cu_2O$ by nitrogen incorporation, to understand the effect of a N:$Cu_2O$ contact layer on TFT performance, $Cu_2O$ TFTs were made having a N:$Cu_2O$ contact layer of various thickness (5, 8 and 13 nm for samples S#6, S#7, and S#8, respectively). The devices were treated with a post-contact anneal (PCA) at 200°C for 1 min in $N_2$ ambient. For comparison, one device without a N:$Cu_2O$ contact layer was made without PCA

(S#4). The sample list and a TFT cross-section are provided in Figure 5.4(a). The electrical measurement results are shown in Figure 5.4.

After PCA, the $Cu_2O$ TFT ON-current of S#5 was observed to increase compared to that S#4, which was not treated with a PCA. This increase may be caused by exposure of channel layer during the PCA [160], since these devices lack a back channel passivation layer. When a 5nm N:$Cu_2O$ contact layer was introduced (#S6 in Figure 5.4(b) and (c)), the ON-current improved further by a factor of ~3×. As the N:$Cu_2O$ contact layer thickness increased from 5 nm (S#6) to 13 nm (S#8), the ON-current increased again by about 7×. Comparing S#7 (8 nm N:$Cu_2O$ layer) and S#8 (13 nm N:$Cu_2O$ layer), the ON-current improvement appears to saturate as the contact layer thickness increased.

To understand the reasons for these ON-current changes, the effective linear mobility ($\mu_{eff,lin}$) and saturation mobility ($\mu_{eff,sat}$) were extracted from the measured *I-V* curves using equations (5.1) and (5.2):

$$\mu_{eff,lin} = \frac{\partial I_{D,lin}}{\partial V_{GS}} \frac{L}{C_{OX} V_{DS} W} \tag{5.1}$$

$$\mu_{eff,sat} = \left( \frac{\partial \sqrt{I_{D,sat}}}{\partial V_{GS}} \right)^2 \frac{2L}{C_{OX} W} \tag{5.2}$$

where $I_{D,lin}$ is the drain current in the linear region, $I_{D,sat}$ is the drain current in the saturation region, $C_{OX}$ is the gate oxide capacitance per unit area, and $W/L$ is the channel width/length (3000 μm/100 μm for our TFTs). Note that these equations do not explicitly include contact resistance. Rather, the presence of a non-zero contact resistance, $R_C$, at the source and again at the drain, for a total of $2R_C$, reduces the voltage along the channel, thereby reducing the value of $\mu_{eff}$ extracted via equations (1) and (2) from the measured *I-V* curves.

We first compared the effect of PCA on $Cu_2O$ TFTs with and without a N:$Cu_2O$ layer (S#5 vs. S#4). The $\mu_{eff}$ increases for TFTs treated with PCA process as shown in Figure 5.4. This increase could be due to an increase in channel conductivity and/or a reduction in contact resistance. Next, we examine $\mu_{eff}$ values for TFTs with different N $Cu_2O$ layer thickness, using the $Cu_2O$ TFT with PCA (S#5) as a baseline for comparison. The $\mu_{eff}$ value increases when a N:$Cu_2O$ layer is added and increases further as its thickness increases (S#6–S#8). Since the channel resistance should be the same for all samples treated by PCA, we can tentatively attribute the improvement in $\mu_{eff}$ to a reduction in $R_C$.

As shown in Figure 5.4(d) for $V_D = -1$ V, the baseline device (S#5) has $\mu_{eff,lin}$ of 0.006 $cm^2V^{-1}s^{-1}$, while with the addition of a 13 nm N:$Cu_2O$ contact layer (S#8), the $\mu_{eff,lin}$ value increased by ~5 times to 0.031 $cm^2V^{-1}s^{-1}$. For sample S#8, $\mu_{eff,sat}$ reaches a value of 0.065 $cm^2V^{-1}s^{-1}$, which is the maximum value obtained in this study. We note that for S#8, the $\mu_{eff,sat}$ value agrees well with the $\mu_{eff,lin}$ value of 0.062 $cm^2V^{-1}s^{-1}$ obtained with $V_D = -10$ V. For all samples, the $\mu_{eff,lin}$ values for $V_D = -1$ V are much lower than those $V_D = -10$ V, which indicates that the contacts may not be linear. In non-linear contacts, a diode-like contact drop will occur across the contact. For $V_D = -1$ V, this voltage drop may comprise a significant fraction of $V_D$, thereby artificially reducing the extracted $\mu_{eff}$ values. On the other hand, for $V_D = -10$ V, the voltage drop is a small fraction of $V_D$, leading to a higher $\mu_{eff}$ for the same channel. The effective mobility as a function of gate voltage, is shown in Figure 5.4(e) for $V_{D,lin} = -10$ V. As the device turns on, $\mu_{eff,lin}$ plateaus. The plateau occurs at higher $\mu_{eff,lin}$ values for the TFTs with N:$Cu_2O$ contact layers.

To gain insight into charge transport at the source/drain contacts, we next examine the $kT/E_{00}$ values, where the $E_{00} = (qh/4\pi)(p/m^*\varepsilon_s\varepsilon_0)^{-1/2}$ is the characteristic energy that is related to the tunneling probability [161]–[163]. Here, $m^*$ is the effective mass, $k$ is the Boltzmanns constant,

$T$ is absolute temperature, $h$ is Planck's constant, $\varepsilon_s$ is the dielectric constant of $Cu_2O$, and $\varepsilon_0$ is the permittivity of free space. From literature [162], $kT/E_{00} \gg 1$ implies thermionic emission is the dominant transport mechanism, $kT/E_{00} \ll 1$ implies field emission, and a $kT/E_{00}$ value of approximately 1 indicates thermionic field emission. For $m^* = 0.58$ [43] and $\varepsilon_s = 7.11$ [83] for $Cu_2O$, the hole carrier concentration required to achieve $kT/E_{00} = 1$ is $8\times10^{18}$ $cm^{-3}$. Hall measurements of S#1 yielded a hole carrier concentration of $\sim3\times10^{14}$ $cm^{-3}$. (We note that in N:$Cu_2O$, $p \ll N_A$ due to the relatively high activation energy of p-type defects [64].) N:$Cu_2O$ samples S#2 and S#3 did not yield satisfactory Hall measurement results, but according to previous work [159], for our sample S#2's resistivity of 0.16 Ω-cm, the estimated $p$ is $\geq 10^{19}$ $cm^{-3}$. Based on this estimate, $kT/E_{00} \leq 1$, and we expect the conduction across metal-N:$Cu_2O$ contacts to be dominated by thermionic field emission (TFE) or field emission (FE).

### *5.3.3 Contact resistance and transport mechanisms with N:Cu₂O S/D interlayer*

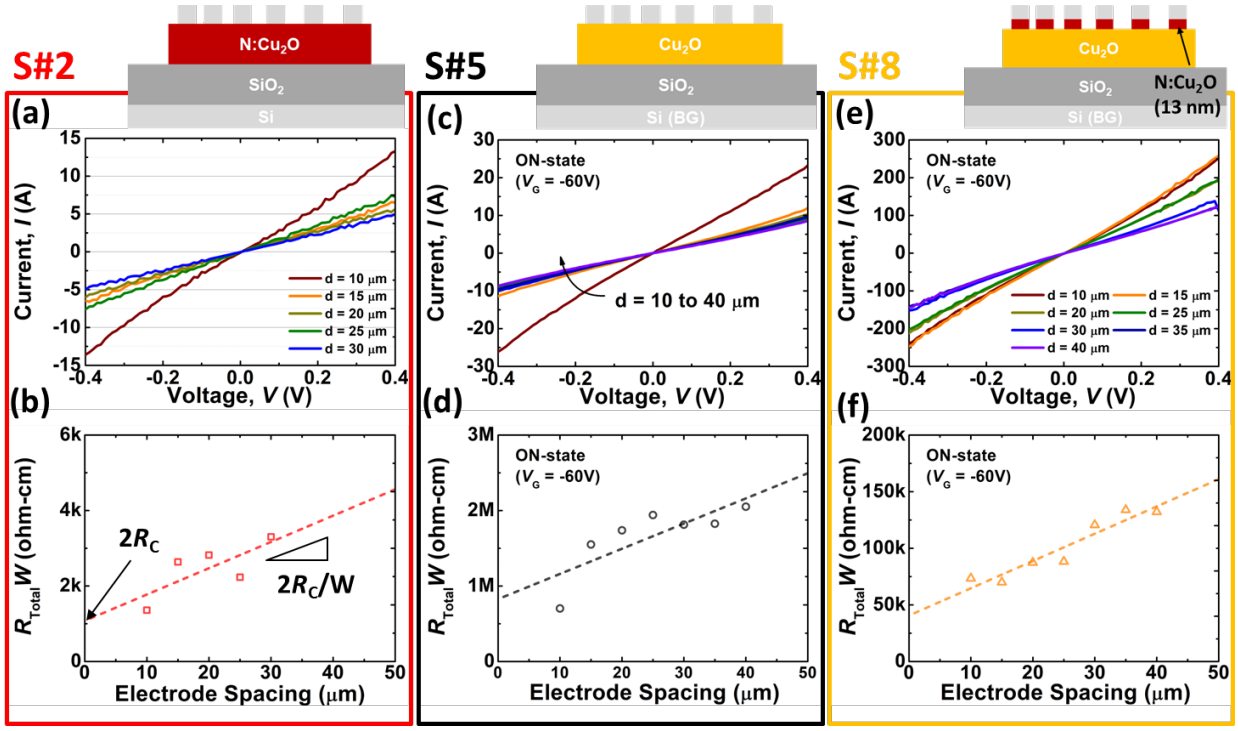



*Figure 5.5 (a, c, e) Current−voltage (I−V) curves and (b, d, f) transfer length measurement (TLM) plots. TLM resistance values were extracted for the voltage region ranging from −0.2 V to +0.2 V. Sample S#2 is the room temperature N:Cu₂O thin film, measured with no gate voltage applied. Samples S#5 and S#8 are Cu₂O thin films without a N:Cu₂O layer and with a 13 nm N:Cu₂O contact layer, respectively, both measured on the ON-state with $V_G$=−60V.*

*Table 5.1 Contact properties of three TFTs. The effective barrier height, $\varphi_{b,eff}$, was obtained using the thermionic emission (TE) model.*

| | **S#2 – N:Cu₂O layer only & w/o PCA with no $V_G$ applied** | **S#5 – w/o N:Cu₂O layer & w/ PCA @ $V_G$ = −60V** | **S#8 – w/ 13 nm N:Cu₂O layer & w/ PCA @ $V_G$ = −60V** |
|---|---|---|---|
| $2R_CW$ (Ω-cm) | 1.08k | 826k | 40.6k |
| $R_{sh}$ (Ω/□) | $6.97\times10^5$ | $3.34\times10^8$ | $2.41\times10^7$ |
| $L_T$ (μm) | 7.72 | 12.4 | 8.42 |
| $\rho_C$ (Ω-cm²) | 0.416 | 511 | 17.1 |
| $\varphi_{b,eff}$ (eV) | - | 0.661 | 0.573 |

To quantify the contact resistance, transfer length measurements (TLM) were performed at several different gate voltage values, $V_G$. Here we investigated Ni/Au contacts to three samples: S#2, a N:$Cu_2O$ thin film; S#5, a $Cu_2O$ thin film; and S#8, a $Cu_2O$ thin film with a 13 nm N:$Cu_2O$ layer positioned between the $Cu_2O$ and the metal. As shown in Figure 5.5(a, c, e), sample S#2 has linear *I-V* behavior while samples S#5 and S#8 showed quasi-ohmic *I-V* behavior. To quantitatively evaluate the contact, the width-normalized contact resistance, $2R_CW$, was extracted from the TLM plots (Figure 5.5(b, d, f)) using the following equation (5.3) [164]:

$$R_TW = R_{sh}d + 2R_CW = R_{sh}(d + 2L_T), \tag{5.3}$$

where $R_TW$ is the total width-normalized resistance, $R_{sh}$ is the sheet resistance, $d$ is the electrode spacing, and $L_T$ is the transfer length. In the $R_TW$ vs. $d$ plots in Figure 5.5(b, d, f), the slope of the trendline, the $y$ intercept, and the $x$ intercept correspond to $R_{sh}$, $2R_CW$, and $-2L_T$, respectively. We also calculated the specific contact resistance $\rho_C = L_T^2 \times R_{sh}$. The extracted values of these parameters are given in Table 5.1.

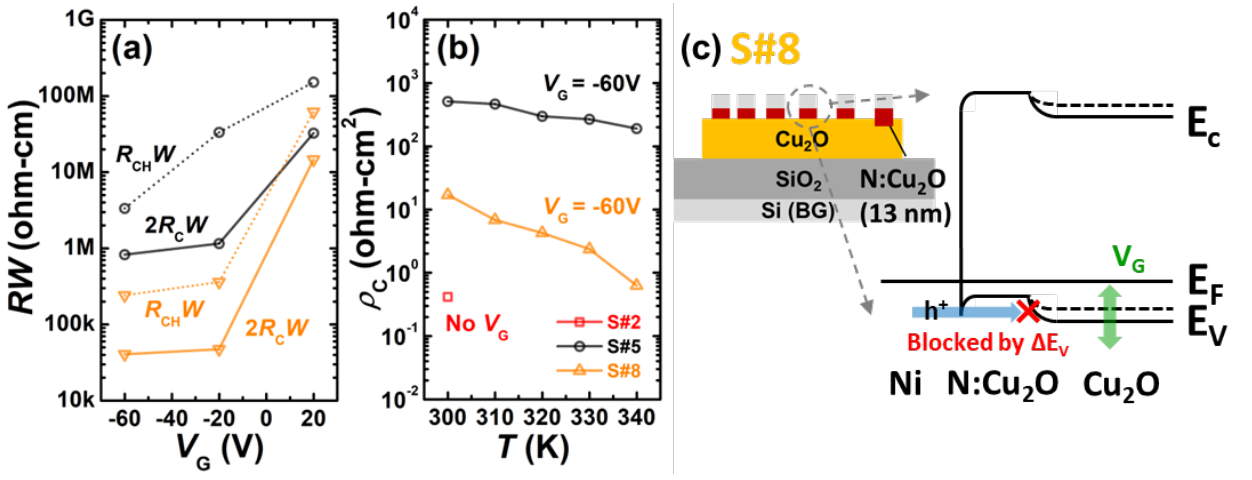



*Figure 5.6 Plots of (a) width-normalized channel resistance, $R_{CH}$, and contact resistance, $R_C$, as a function of gate voltage ($V_G$), (b) specific contact resistance, $\rho_C$, as a function of temperature (300–340 K) and (c) energy band diagram showing Ni/Au-to-N:$Cu_2O$ (S#8) contacts. Sample #8 has a $Cu_2O$ conduction layer with a 13 nm N:$Cu_2O$ contact layer.*

Based on these results, we assessed the effect of the N:$Cu_2O$ layer on contact resistance. The addition of a 13-nm N:$Cu_2O$ contact layer reduces the width-normalized contact resistance in the ON-state (at $V_G = -60$ V) by a factor of 20×, from 826 kΩ·cm for S#5 to 40.6 kΩ·cm for S#8, as shown in Figure 5.6(a) and Table 5.1. The transfer length, $L_T$, was reduced from 12.4 μm for S#5 to 8.42 μm for S#8. Since $L_T$ is the effective length of the contact [164], it is important to have a low $L_T$ in order to achieve device scaling. In the ON-state, $\rho_C$ was reduced from 511 Ω·cm$^2$ for S#5 to 17.1 Ω·cm$^2$ when a 13-nm N:$Cu_2O$ contact layer is added (S#8) (Figure 5.6(b)).

We note that $\rho_C$ for the N:$Cu_2O$ only sample (S#2) is 0.416 Ω·cm$^2$. This implies that transport across the metal/N:$Cu_2O$ contact is indeed governed by TFE or FE, as we predicted. The much higher $\rho_C$ value for the N:$Cu_2O$/$Cu_2O$ contact (S#8) implies that, in addition to the increased doping level in N:$Cu_2O$ compared to $Cu_2O$, another factor must be at play in determining the contact properties of sample S#8. To better understand this, we measured the temperature-dependence of $\rho_C$. A narrow temperature range (300K–340K) was used to ensure that the thin film phase of $Cu_2O$ remains unchanged [160]. For sample S#5 and S#8, $\rho_C$ decreases with increased temperature. The $\rho_C$ of both contacts significantly decreases over the measured temperature range, indicating that thermionic emission is dominant [165]. We used the thermionic emission (TE) model to extract the effective barrier height, $\varphi_{b,eff}$, via the following equation (5.4) [163]:

$$\rho_{C,TE} = \frac{k}{qA^*T} exp\left(\frac{q\varphi_{b,eff}}{kT}\right), \tag{5.4}$$

Here $A^*$ is the Richardson constant, equal to $120(m^*/m_0)$ [164] or 69.6 A cm$^{-2}$K$^{-2}$ for a $Cu_2O$ hole effective mass of $m^* = 0.58m_0$ [43].

For the baseline sample (S#5), the room temperature $\varphi_{b,eff}$ value for the ON-state is 0.661 eV. The moderately high value of $\varphi_{b,eff}$ for S#5 explains the non-linear *I-V* behavior of the contacts observed in Figure 5.5(c). With the addition of a 13-nm N:$Cu_2O$ contact layer (S#8), the

$\varphi_{b,eff}$ value is lowered to 0.573 eV. For S#8, since we know that transport across the metal-N:$Cu_2O$ junction is via TFE or FE, the potential barrier observed here likely originates from the non-zero valence band offset [166], $\Delta E_V$, between N:$Cu_2O$ and $Cu_2O$, as illustrated in Figure 5.6(c). The valence band offset between N:$Cu_2O$ and $Cu_2O$ causes thermionic emission-like behavior of the contact, leading to non-linear *I-V* for S#8 (Figure 5.5(e)). Conceptually, the elevated temperature may increase the number of carriers going over the N:$Cu_2O$ to $Cu_2O$ barrier due both to the higher thermal energy (thermionic emission) and to slight lowering of the barrier height due to increased activation of deep intrinsic acceptors. Both of these effects may contribute to the temperature-dependence of $\rho_C$ in S#8.

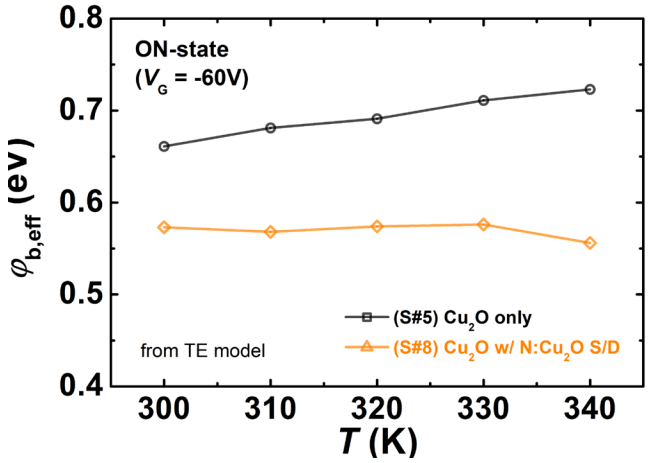



*Figure 5.7 Effective barrier height, $\varphi_{b,eff}$, in the ON-state ($V_G$ = −60 V) as a function of temperature (300–340 K). The $\varphi_{b,eff}$ values were extracted using the thermionic emission model, i.e. equation (4).*

In addition, we note that the effective barrier height of S#5 is strongly temperature-dependent (Figure 5.7). This phenomena has been observed in other oxide semiconductors, such as $Ga_2O_3$ [165], and has been attributed to spatial inhomogeneity of the barrier [167]. To assess this inhomogeneity, we use the model [167] given in equation (5.5):

$$\varphi_{b,eff} = \varphi_{b0} - \sigma_0^2 \frac{q}{2kT}, \tag{5.5}$$

where $\varphi_0$ is the mean barrier height and $\sigma_0$ is the standard deviation. We find that $\varphi_0$ = 1.191 eV and $\sigma_0$ = 0.165 eV for sample S#5. The inhomogeneity of the barrier height may originate from the nanocrystalline structure and rough surface of our $Cu_2O$ thin film, observed by transmission electron microscopy in our previous paper [71]. For S#8, the effective barrier height is a weak function of temperature indicating that the barrier is fairly homogeneous.

We also observe that the contact resistance is modulated by gate voltage in both S#5 and S#8 (Figure 5.6(a)). In S#8, which has a 13 nm N:$Cu_2O$ contact layer, the width-normalized contact resistance changes from 14.6 MΩ·cm in the OFF-state to 40.6 kΩ·cm in the ON-state. Here, we define the OFF-state at $V_G$ = 20 V and the ON-state at $V_G$ = −60 V. Gate modulation of contact resistance is common in TFTs when the bottom gate extends underneath the source/drain contacts [53], [168]. In this device configuration, the applied gate voltage changes the carrier concentration in the semiconductor underneath the metal contact. For thin channels, the conductivity of the semiconductor can be changed significantly as the gate voltage changes [169]. The resultant change in Fermi level position changes the effective barrier height, leading to gate-modulated contact resistance.

Finally, we note that while the S#8 value represent a significant improvement over S#5, the contact resistance of the metal/N:$Cu_2O$/$Cu_2O$ structure is still too high: high-quality ohmic contacts require $\rho_C < 10^{-3}$ Ω·cm$^2$ and channel length scaling for high frequency circuits will require $L_T$ below 1 μm.

## 5.4 Conclusion

In this work, we developed room temperature deposition processes for N:$Cu_2O$ thin films using RF magnetron sputtering. The ohmic contact specific resistance of Ni/Au to N:$Cu_2O$ was shown to be low, 0.416 $\Omega \cdot cm^2$. To reduce the contact resistance of $Cu_2O$ thin film transistors, we incorporated a N:$Cu_2O$ contact layer along with a post-contact anneal. Transfer length measurements showed that the width normalized contact resistance was reduced 1/20× by incorporation of the N:$Cu_2O$ contact layer. This reduction in contact resistance causes an improvement in the linear effective mobility by 4× from 0.014 $cm^2V^{-1}s^{-1}$ to 0.062 $cm^2V^{-1}s^{-1}$. While charge transport across the N:$Cu_2O$-to-metal junction is via thermionic field emission or field emission, the non-zero valence band offset between N:$Cu_2O$ and $Cu_2O$ leads to thermionic emission within the Ni/Au-N:$Cu_2O$-$Cu_2O$ ohmic contact. The addition of a N:$Cu_2O$ contact layer lowers the effective barrier height from 0.661 eV to 0.573 eV. Based on these results, we conclude that the observed improvement of the effective mobility upon incorporation of a heavily p-doped N:$Cu_2O$ layer under the source/drain metal contacts comes from reduction of the ohmic contact resistance. Although much work remains to achieve high performance p-type $Cu_2O$ TFTs, here we have shown a novel method to reduce the contact resistance, a critical factor to realize future complementary oxide-based thin film circuits.

# Chapter 6 Dielectric engineering for $Cu_2O$ thin film transistor

## 6.1 Introduction

*Table 6.1 Effect of gate dielectric on $Cu_2O$ TFT performance.*

| $Cu_2O$ Process Module | Phase | Dielectric | $D_{it}$ ($cm^{-2}$ $eV^{-1}$) | $\mu_{FE}$ ($cm^2V^{-1}s^{-1}$) | Ref# |
|---|---|---|---|---|---|
| Spray-coating | $Cu_2O$ | $SiO_2$ | $5.6 \times 10^{13}$ | $10^{-4} - 10^{-3}$ | [60] |
| RFMS | $Cu_2O$ | $SiO_2$ | $2.89 \times 10^{13}$ | 0.06 | [71] |
| Solution Process | $CuO_x$ | $SiO_2$ | $1.64 \times 10^{12}$ – $1.57 \times 10^{13}$ | $10^{-4} - 0.32$ | [170] |
| DCMS | $Cu_2O$ | $(TiO_2)_x(Al_2O_3)_{1-x}$ | 1.85 × 1014 | $2.3 \times 10^{-3}$ | [149] |
| | | $SrTiO_3$ | $3.32 \times 10^{13}$ | 1.64 | |
| Pulse laser deposition | $CuO_x$ | $HfO_2/SiO_2$ | $1.6 \times 10^{12}$ | - | [171] |
| Pulse laser ablation | $Cu_2O$ | $HfO_2/SiO_2$ | $6.7 \times 10^{11}$ | 2.7 (sat.) | [93] |

In the previous chapters, I discussed the origin of the gap between field effect mobility and Hall mobility and confirmed that the difference between these two values is mainly due to high contact resistance and high interface trap density. In Chapter 5, a N:$Cu_2O$ S/D interlayer was introduced into $Cu_2O$ thin film transistors to alleviate contact resistance. In this Chapter, we seek to address the high interface trap density in order to demonstrate high performance $Cu_2O$ thin film transistors. For polycrystalline $Cu_2O$ thin films, a high trap density may originate from the traps that exist not only at the interface but also at the grain boundaries. In Chapter 4, we examined the effect of process temperature on trap states. A higher process temperature led to lower trap density, likely due to a concurrent increase in the average grain size.

In this chapter, trap states at the semiconductor-to-dielectric interface will be investigated. As shown in Table 6.1, the lowest interface trap ($D_{it}$) reported to date is for $HfO_2$ gate dielectric. Clearly, choosing an appropriate dielectric is important to minimize $D_{it}$. In this chapter we also will show preliminary investigations into the effects of passivation, i.e. the addition of a back-channel dielectric, on the $Cu_2O$ thin film transistor behavior. In other TFT technologies, passivation layers have been shown to be critical for device stability, i.e. to minimize the extent to which the channel layer is affected by the environment [172]. Furthermore, the interface trap density at the back channel is also an important factor in determining TFT behavior, in addition to the front channel trap density. While the effect of gate dielectrics on TFT performance has been studied (as shown in Table 6.1), very few investigations of the $Cu_2O$ back-channel surface (i.e., passivation) have been performed. One previous study [173] of back-channel passivation via sulfur treatment showed that the on/off-current ratio could be improved by passivating the back-channel defects. This early result indicates the importance of addressing back-channel defects. Thus, in this chapter the use of alternate gate dielectrics and the effect of back-channel passivation on device performance will be studied.

## 6.2 Experimental Methods

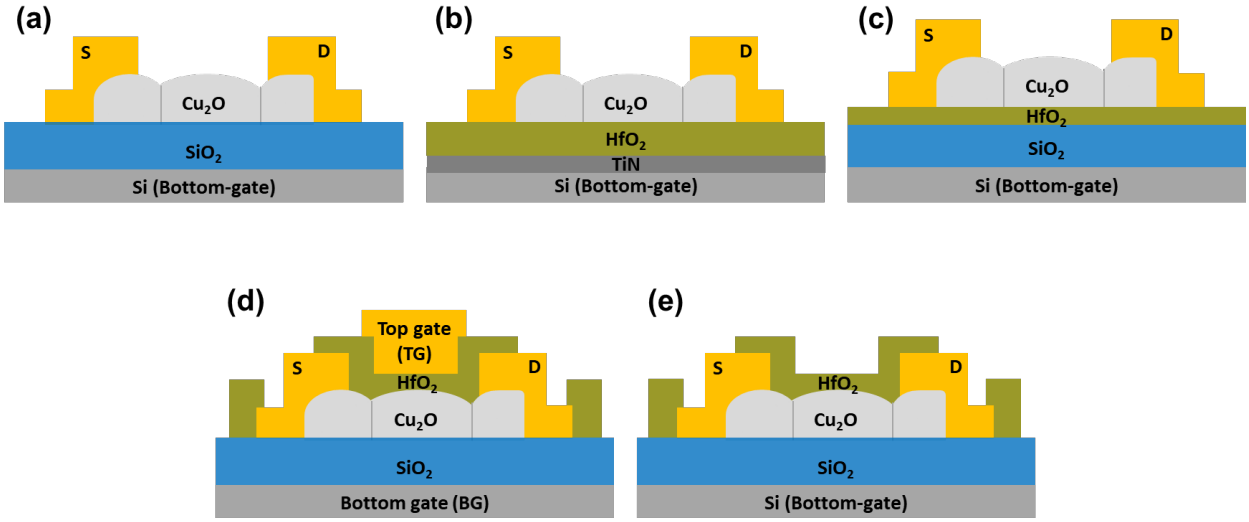



*Figure 6.1 Schematics of the thin film transistor structures used in this chapter: (a) back-gate (BG) with a low-k gate dielectric, (b) BG with a high-k gate dielectric, (c) BG with a high-k/low-k gate dielectric bilayer, and (d) top-gate high-k gate dielectric, and (e) BG device with a low-k gate dielectric and a back-channel $HfO_2$ passivation layer.*

A bottom-gate (BG) Si substrate and thermally-grown $SiO_2$ layer have been used as the gate electrode and dielectric in all of the TFTs reported so far in this thesis (Figure 6.1(a)). To understand the effect of high-*k* dielectrics on $Cu_2O$ thin film transistors, a TiN metal gate was deposited on bare Si to form the gate electrode and the $SiO_2$ layer was replaced with $HfO_2$, a high-*k* dielectric (Figure 6.1(b)). These substrates were prepared by our Intel collaborators. Then, I fabricated TFTs as described in previous chapters: a 20 nm $Cu_2O$ thin film was deposited on top of the gate/gate dielectric stack at room temperature and subjected to a 600 °C post-deposition anneal, and source/drain Ni/Au metal electrodes were deposited and patterned. This BG high-*k* dielectric structure was used to evaluate the interface trap density with $HfO_2$ dielectric. To understand the interface between $HfO_2$ and $Cu_2O$, separate BG TFTs were made with a $HfO_2/SiO_2$ bilayer gate dielectric (Figure 6.1(c)). A thin $HfO_2$ layer was deposited on top of a thermally-grown

$SiO_2$ dielectric layer using atomic layer deposition (ALD). This allowed us to separate the effects of the HfO2 gate interface from any effects due to the TiN gate electrode layer.

Thin film transistors with a top gate high-*k* dielectric structure (Figure 6.1(d)) were also evaluated. For the top gate TFTs, after formation of S/D contacts, a 30-nm $HfO_2$ layer was deposited via ALD. Then, a Ni/Au top gate contact was formed by photolithography. Finally, the effect of passivation layers on $Cu_2O$ thin film transistor performance was studied using the structure shown in Figure 6.1(e). A $HfO_2$ or $Al_2O_3$ passivation layer was deposited on top of the $Cu_2O$ layer after device fabrication to passivate the back-channel of $Cu_2O$. In all cases, to prepare the $HfO_2$ and $Al_2O_3$ high-*k* layers, tetrakis(dimethylamino)hafnium (TDMAH) precursor + $H_2O$ (thermal) and trimethyl aluminum (TMA) precursor + $O_3$ (ozone) recipes were used, respectively, for ALD at 200 °C.

## 6.3 Results and Discussions

### *6.3.1 High-k dielectric with bottom gate structure*

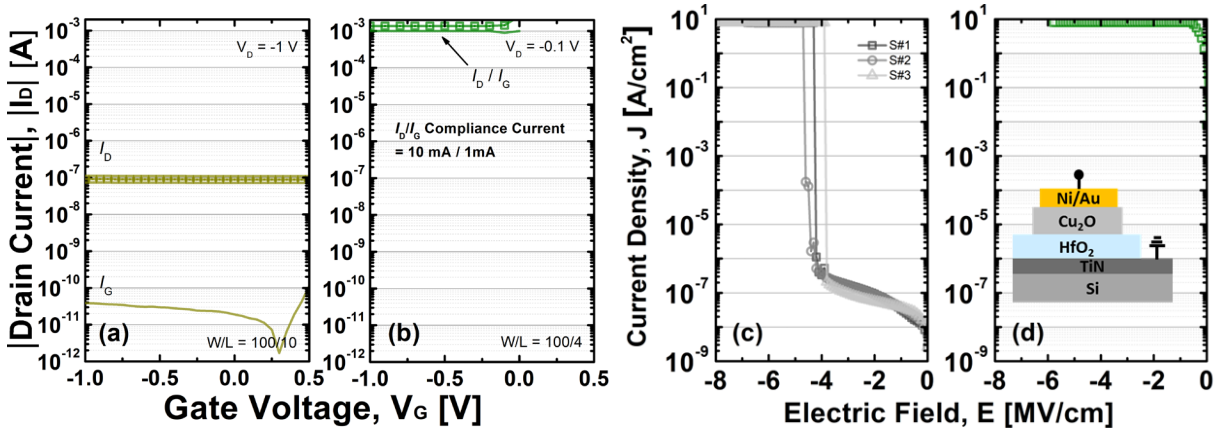



*Figure 6.2 Back-gate $HfO_2$ thin film transistor $I_D$-$V_G$ curves for (a) as-deposited $CuO_x$ and (b) 600 °C-annealed $Cu_2O$. The compliance current of the drain (gate) current is 10 mA (1 mA). Capacitor J-E measurements for (c) a metal-$HfO_2$-metal (MIM) structure and (d) a metal-$Cu_2O$-$HfO_2$-metal (MIS) structure. For all devices, the $HfO_2$ thickness is 10 nm and the $Cu_2O$ thin film thickness is 20 nm.*

First, $Cu_2O$ thin film transistors with back-gate $HfO_2$ dielectric structure were evaluated. Figure 6.2(a) and (b) show the TFT results for as-deposited and 600 °C-annealed thin film, respectively. After post-deposition anneal (PDA) at 600 °C, the TFT showed very high leakage current. We hypothesize that the dramatic rise in drain and gate leakage current may be due to metal interdiffusion between the $HfO_2$ and $Cu_2O$ during the PDA. This indicates that the $HfO_2$ / $Cu_2O$ stack cannot tolerate the 600 °C PDA temperature. To assess the possibility of Cu/Hf interdiffusion, metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) capacitors were fabricated. A 10-nm $HfO_2$ layer was used in both. The $Cu_2O$ layer in the MIS capacitor was treated with a 600 °C PDA. The measured current density – electric field plots are shown in Figure 6.2(c) and Figure 6.2(d). The MIM capacitor had breakdown electric field of 3.9–4.7 MV/cm (Figure 6.2(c)). On the other hand, the MIS capacitor with a $Cu_2O/HfO_2$ interface exhibits breakdown near zero electric field.

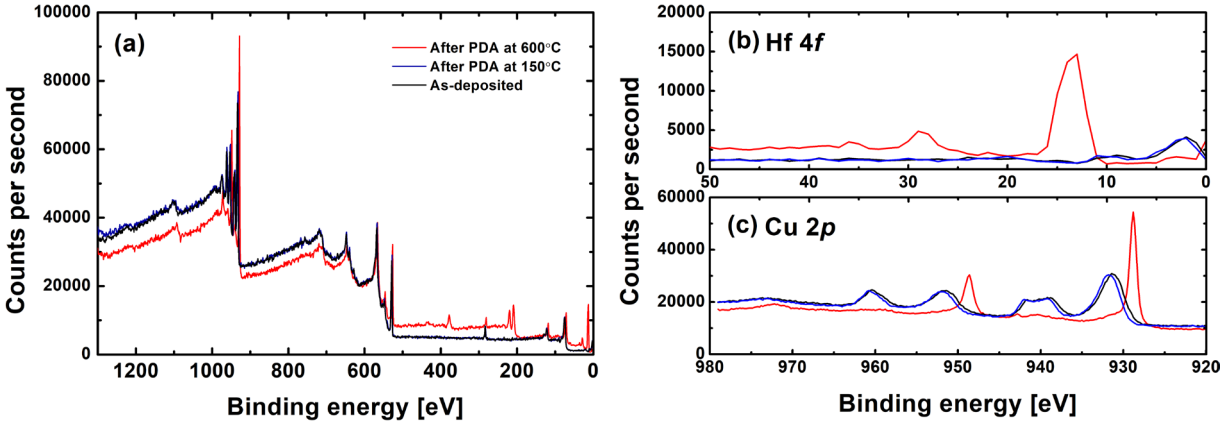



*Figure 6.3 X-ray photoelectron spectroscopy (XPS) results for three $CuO_x$ films deposited on top of a 33-nm $HfO_2$ layer. The three films are: as-deposited CuO, CuO annealed in air at 150 °C and $CuO_x$ annealed in vacuum at 600 °C. (a) Shows the wide scan results, while (b) and (c) show the core scan results for Hf 4f and Cu 2p, respectively.*

To assess Cu/Hf interdiffusion via X-ray photoelectron spectroscopy (XPS),[3] three copper oxide thin films were made with different PDA conditions: as deposited, 150 ℃ anneal in air, and 600 ℃-anneal in vacuum. Figure 6.3(a) shows the XPS wide scan results of the three samples and Figure 6.3(b) and (c) show the XPS core scan results for Hf 4*f* and Cu 2*p*, respectively. The as-deposited and the 150℃-annealed samples have similar features. The 600 ℃-annealed copper oxide thin film has several differences. In the Hf 4*f* trace, it exhibits a peak at ~14 eV. The peak is possibly related to the Hf(0) $4f_{7/2}$ peak seen in Hf metal [174]. In the Cu 2*p* core scan (Figure 6.3(c)), [175], the strong peaks observed at ~930 and ~950 eV may be related to Cu metal. This is contrast to the $Cu^{2+}$ $2p_{3/2}$ satellite peaks at ~960 eV and at ~940 eV that were observed for the as-deposited and 150 ℃ PDA-treated samples. These results indicate that Cu/Hf interdiffusion and redox reactions may have occurred during the 600 ℃ PDA process. To understand the role of process temperature in these diffusion processes, next I tested samples prepared with different process temperatures.

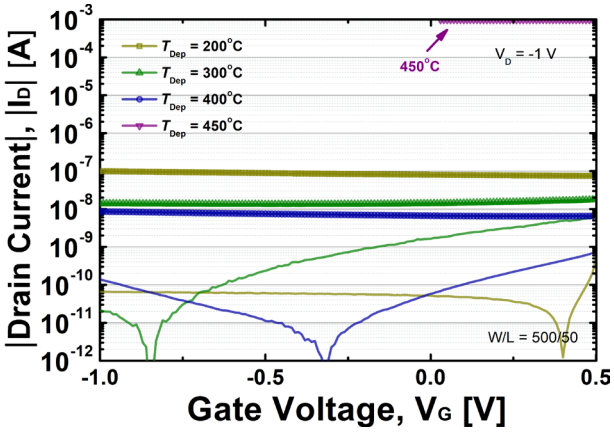



*Figure 6.4 Drain current versus gate voltage ($I_D$ vs. $V_G$) curves for back-gate thin film transistors made with a 10 nm $HfO_2$ gate insulator and copper oxide semiconductor films deposited at different temperatures. The symbols indicate $I_D$ and the solid lines indicate $I_G$ traces.*

[3] XPS was performed by Dr. Kaan Oguz at Intel (the sponsor of this work)

To understand the maximum temperature that the $HfO_2$ can tolerate, thin film transistors were fabricated with copper oxide ($CuO_x$) films processed at different temperatures – the $CuO_x$ with the below 600 °C deposition temperature showed $Cu_2O$+CuO mixed phase as discussed in the section 4.3. The $CuO_x$ thin films were deposited at temperatures ranging from 200 to 450 °C on top of a 10nm $HfO_2$ layer. As shown in Figure 6.4, a high leakage current was observed when the deposition temperature reached 450 °C. This means that the $HfO_2$ layer cannot tolerate process temperatures of > 400 °C. Although a $HfO_2$ gate dielectric, having an effective oxide thickness (EOT) of about 2.6 nm, was used to obtain better channel-to-dielectric coupling, the $Cu_2O$ deposited at 400 °C was not able to demonstrate on/off switching within the gate voltage region measured. That lack of observed field effect may be due to a high defect states density, as discussed in Chapter 4.

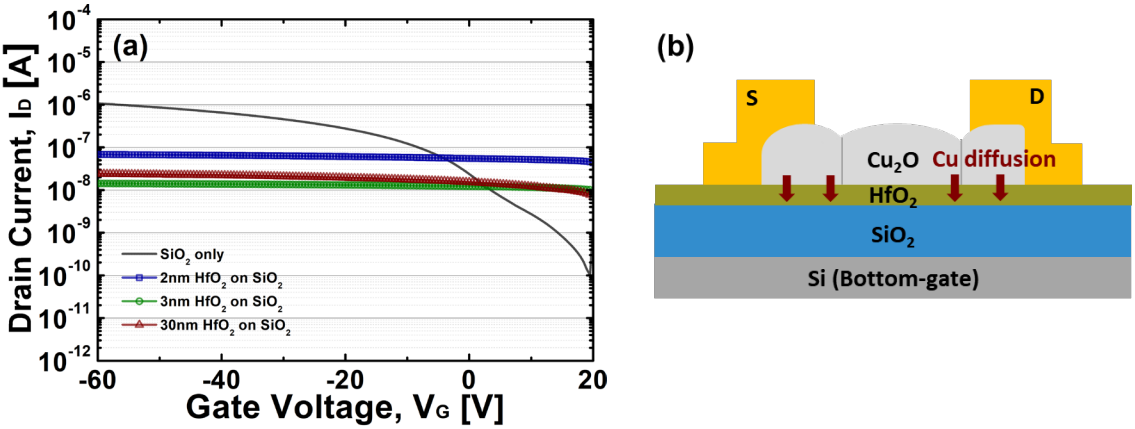



*Figure 6.5 (a) Drain current versus gate voltage ($I_D$ vs. $V_G$) curves for back-gate $HfO_2/SiO_2$ bilayer thin film transistors with different $HfO_2$ thickness: 2 nm, 3 nm, and 30 nm $HfO_2$ on $SiO_2$, compared to the behavior of a TFT with no $HfO_2$ layer. The drain voltage for all measurements is −1 V. (b) Illustration of possible Cu diffusion occurring within the 600 °C-PDA $Cu_2O$ TFTs with $HfO_2/SiO_2$ bilayer dielectrics.*

According to previous studies [176]–[179], a very thin high-*k* dielectric layer such as $Al_2O_3$, $HfO_2$, and $TiO_2$ can be used as a Cu diffusion barrier. Thus, to evaluate the effect of a $HfO_2$ high-*k* dielectric on the interface trap density, a thin $HfO_2$ layer (2 nm or 3 nm) was deposited on top of

the $SiO_2$ gate dielectric layer (Figure 6.1(c)), prior to deposition of a 20-nm $Cu_2O$ layer deposited at room temperature with a PDA at 600 ℃. The TFT electrical measurements results are shown in Figure 6.5(a). The thin film transistors that have a $HfO_2/SiO_2$ bilayer showed nearly flat $I_D$-$V_G$ curves. It indicates that a thin $HfO_2$ layer is not effective as a Cu-diffusion barrier when faced with a 600 ℃ PDA. Even with a thicker $HfO_2$ layer of 30 nm, it still showed the same issue. I surmise that Cu diffusion into the thin $HfO_2$ layer causes $Cu_2O$ to change its metal-oxide composition near the interface, degrading its semiconductor properties. Although the thin high-*k* layer is effective to minimize formation of Cu-silicide by reaction between Cu and Si [176]–[179], it was not enough to keep the TFT channel characteristics. Further work to understand and mitigate Cu interdiffusion and redox with high-*k* dielectrics is required in order to push the $Cu_2O$ BG TFT technology forward. Since neither a single $HfO_2$ layer nor a $HfO_2/SiO_2$ bilayer were effective to mitigate interdiffusion/redox with 600 ℃-PDA $Cu_2O$, I next explored a top gate structure that uses a $HfO_2$ dielectric layer.

### *6.3.2 High-k dielectric with top gate structure*

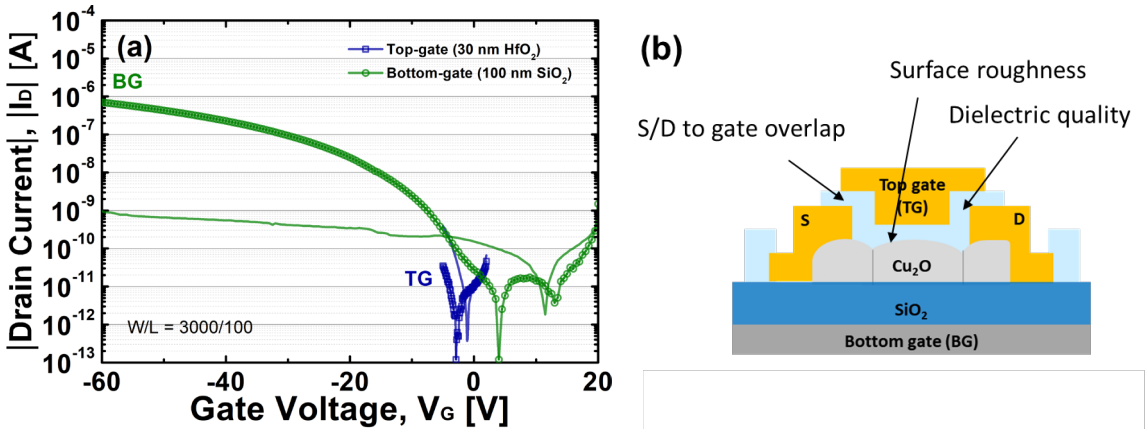



*Figure 6.6 (a) Drain current versus gate voltage ($I_D$ vs. $V_G$) curves for 600 ℃-PDA $Cu_2O$ thin film transistors with a top-gate structure and a 30 nm $HfO_2$ gate dielectric. Here, TG indicates the top-gate voltage sweep (with $V_D = -1$ V) and BG means the bottom-gate voltage sweep (with $V_D = -10$ V). Symbols indicate the drain current ($I_D$) and solid lines indicate gate current ($I_G$). (b) The schematic illustrates the possible causes of the high gate leakage current observed in the TG TFT with $HfO_2$ gate dielectric.*

As shown in Chapter 4, $Cu_2O$ annealed at 400 ℃ was unable to yield good TFT behavior due to its high trap density. Therefore, I next attempted to integrate a high-*k* gate dielectric with a $Cu_2O$ film annealed at 600 ℃ using a top-gate structure (Figure 6.1(d)). This architecture greatly minimizes the possibility of interdiffusion/redox between $Cu_2O$ and the gate dielectric, since the thermal budget during top gate dielectric deposition and the subsequent TFT fabrication steps is relatively low. The top gate dielectric consisted of 30 nm $HfO_2$ and the top gate electrode is made from Ni/Au. In this device, I maintained the $Si/SiO_2$ bottom gate, and thus the resulting TFT has a dual-gate structure, with separated bottom and top gate electrodes. The electrical measurements results are shown in Figure 6.6. The TG measurement shows high gate leakage current. The high gate leakage current may be related to the source/drain to gate overlap (i.e., mask design), poor dielectric quality, or excessive surface roughness. As shown in Figure 2.2, TEM showed that the $Cu_2O$ films have varied grain size and height with a nonuniform surface. Although the top-gate structure can effectively minimize Cu diffusion/redox, there are other problems that still need to be addressed. More work is needed to successfully demonstrate a high-*k* dielectric top gate TFT. One interesting observation from Figure 6.6 is that the top-gate dielectric deposition causes improvements in the bottom-gate TFT curves: the *SS* is reduced and the on/off current ratio increased. Thus, in the following section, the effect of top-gate dielectric (i.e., the addition of a passivation layer) will be explored to improve BG TFT performance.

### *6.3.3 Passivation*

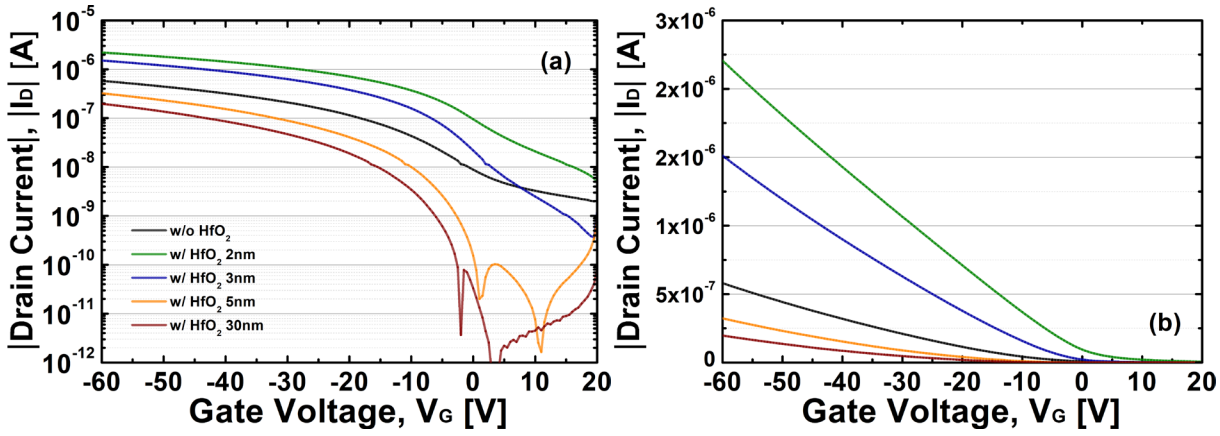



*Figure 6.7 I-V curves for 600 °C-PDA $Cu_2O$ thin film transistors without a passivation layer and with different $HfO_2$ passivation layer thickness: 2 nm, 3 nm, 5 nm, and 30 nm. Drain current versus gate voltage ($I_D$ vs. $V_G$) curves are shown (a) on a semi-log scale and (b) using a linear scale. The drain voltage ($V_D$) for all measurements is −1 V*

*Table 6.2 Electrical properties of $Cu_2O$ thin film transistors with different $HfO_2$ passivation layer thickness.*

| **$HfO_2$ thickness** | **no $HfO_2$** | **2 nm** | **3 nm** | **5 nm** | **30 nm** |
|---|---|---|---|---|---|
| $\mu_{FE,lin}$ ($cm^2V^{-1}s^{-1}$) for $V_D = -1$ V | 0.013 | 0.039 | 0.031 | 0.009 | 0.006 |
| $I_{on}/I_{off}$ ratio | 287 | 432 | 1273 | $> 10^3$ | $> 10^4$ |
| $SS_{min}$ (V/dec) | 11.09 | 10.99 | 7.37 | 0.59 | 0.36 |
| $V_T$ (V) | −18.1 | −4.9 | −12.7 | −24.4 | −27.7 |
| $R_{sh}$ (Ω/sq) | $2.39\times10^9$ | $6.27\times10^8$ | $1.26\times10^9$ | $1.10\times10^{12}$ | $7.37\times10^{10}$ |

The I-V curves for TFTs made with $HfO_2$ passivation layer (Figure 6.1(e)) of varying thickness are shown in Figure 6.7 and the properties are summarized in Table 6.2. The presence of a $HfO_2$ passivation layer improves the on/off current ratio and lowers the subthreshold slope. With the addition of a 2 nm passivation layer, the field effect mobility was improved by ~3× with a slightly improved on/off current ratio (~1.5×). However if the $HfO_2$ passivation layer gets too thick, some deleterious effects are observed. Namely, for TFTs with a 30 nm $HfO_2$ passivation layer, the field effect mobility degraded by ~2× however the on/off current ratio was dramatically improved from 287 (without passivation) to $>10^4$ (with 30 nm passivation). Similarly, the

subthreshold slope was reduced from 11.09 V/dec to 0.36 V/dec and the $V_T$ value shifted from −18.1 V to −27.7 V. The shift in $V_T$ may be due to trapped charge or defects at the $Cu_2O$-to-$HfO_2$ interface. Based on the subthreshold slope, the estimated interface trap density was reduced from $4\times10^{13}$ $eV^{-1}cm^{-1}$ for the baseline device to $1\times10^{12}$ $eV^{-1}cm^{-1}$ for the device with a 30 nm passivation layer. This indicates that addressing back-channel defects and/or passivating the back surface is a key pathway to improve TFT performance. The corresponding sheet resistance was also studied via four-point probe measurements. As shown in Table 6.2, the measured sheet resistance ($R_{sh}$) decreased when 2 nm or 3 nm passivation layers are added. When the $HfO_2$ passivation layer increases to 5 nm and then to 30 nm, the sheet resistance increased again. The measured $R_{sh}$ values were well matched with the $I_D$-$V_G$ results at $V_G = 0$ V; that is to say, the change in measured sheet resistance may be due, in part, to threshold voltage shifts which shift the TFT turn-on from enhancement mode to depletion mode. The shift in threshold voltage may possibly be due to diffusion/redox between $HfO_2$ and $Cu_2O$ and/or to a change in the $Cu_2O$ layer composition that occurs during the $HfO_2$ ALD process, which occurs at 200°C in vacuum. A deeper understanding of the chemical reactions and material properties at the interface is required in the future.

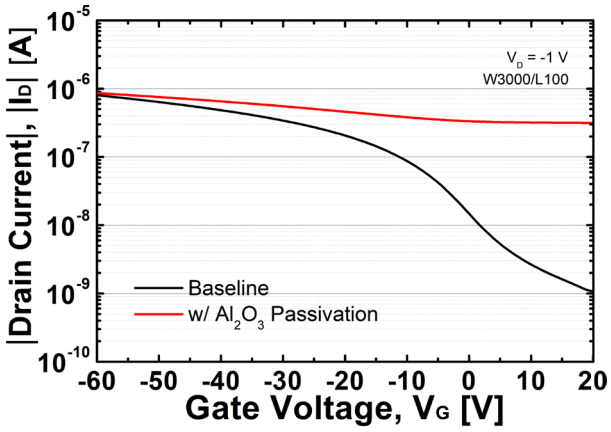



*Figure 6.8 600℃-PDA $Cu_2O$ thin film transistor behavior without a passivation layer and with a 30 nm $Al_2O_3$ passivation layer.*

*Table 6.3 Electrical properties of $Cu_2O$ thin film transistors made with and without a 30 nm $Al_2O_3$ passivation layer.*

| | **No passivation layer (baseline)** | **with $Al_2O_3$ passivation layer** |
|---|---|---|
| $\mu_{FE,lin}$ ($cm^2V^{-1}s^{-1}$), $V_D = -1$ V | 0.020 | 0.010 |
| $I_{on}/I_{off}$ ratio | 676 | 3 |
| $SS_{min}$ (V/dec) | 10.45 | - |
| $R_{sh}$ (Ω/sq) | $5.48\times10^8$ | $2.92\times10^7$ |

An $Al_2O_3$ dielectric was also tested as a passivation layer. As shown in Figure 6.8, with the addition of a 30 nm $Al_2O_3$ passivation layer, the on current level remained unchanged. However, the on/off current ratio was degraded; the off current increased significantly upon addition of the $Al_2O_3$ passivation layer. Based on four-point probe measurements, the corresponding sheet resistance was reduced from $5.48\times10^8$ Ω/sq to $2.92\times10^7$ Ω/sq. Similar to the case with $HfO_2$, these results indicate that there may be reactions and interdiffusion between $Cu_2O$ and the $Al_2O$ passivation layer. Based on a previous study [154], the increased off-current might be explained by the following reaction between $Cu_2O$ and TMA precursor (*i.e.*, $Al(CH_3)_3$): $2Cu_2O + Al(CH_3)_3 \rightarrow CuAlO_2 + 3Cu + 2CH_4(g) + CH_{ads}$. During the first ALD cycle, this reaction may occur, leading to the formation of highly-conductive $CuAlO_2$ and Cu, which may cause a high off current. The

high conductivity of $CuAlO_2$ was reported with carrier concentration up to $5.4\times10^{18}$ $cm^{-3}$ [31], [180], much higher than that of $Cu_2O$ [44]. Further studies to adjust the deposition conditions and thickness may be useful to more fully evaluate the potential of the $Al_2O_3$ passivation layer.

I also note that in n-type AOS TFTs, it has been found that passivation layers are critical for ensuring ambient device stability and bias stress stability. The addition of $HfO_2$ passivation had the positive effect on the device performance of $Cu_2O$ thin film transistor. Further work is needed to improve our understanding of the relationship between back-channel trap states and passivation layers.

### 6.4 Conclusions

In this chapter, I explored high-*k* dielectrics for $Cu_2O$ thin film transistors. To understand the high interface trap density observed in some devices, TFTs with $HfO_2$ high-*k* dielectric were investigated using both a bottom gate structure and a top gate structure. The bottom-gate TFTs, with $HfO_2$ single layer or $HfO_2/SiO_2$ bilayer gate dielectrics cannot tolerate 600 ℃ process temperature without exhibiting performance degradation due to Cu/Hf diffusion and redox. While in principle, top-gate structure could be used to address the Cu-diffusion issue, in the top gate TFTs made here, other issues caused a high gate leakage current. Further optimization of mask designs and process conditions is required to enable TFTs with a top-gate structure. Finally, high-*k* passivation layers were investigated to determine whether they can minimize the back-channel defect states. When a thin $HfO_2$ passivation layer was deposited on the back-channel region of a $Cu_2O$ TFT, improved on-current and subthreshold slope were observed, however there were tradeoffs observed for thicker (30 nm) $HfO_2$ layer which exhibited decreased on current. Thus, we have determined that addition of a suitable passivation layer is important to obtain stable device

performance. Furthermore, since performance improvements were observed with the $HfO_2$ passivation layer, further optimization is needed to maximize the device performance.

# Chapter 7 Conclusion and Future work

## 7.1 Conclusion

The thesis work enables advances in p-type $Cu_2O$ thin film transistors (TFTs) to demonstrate complementary metal-oxide semiconductor (CMOS) technologies by investigating key challenges and proposing solutions. Although n-type oxide semiconductor TFTs have been successfully used in display applications, the lack of a p-type counterpart having similar device performance frustrates development of an all-oxide CMOS technology. An oxide-based CMOS technology would reduce circuit complexity, while opening new application areas that take advantage of its transparency, high breakdown voltage, and low leakage current. While $Cu_2O$ material has been actively studied due to its high hole mobility, its TFT device performance has remained stalled without significant improvement for more than a decade.

With the goal of developing high-performance wide-bandgap p-type $Cu_2O$ TFTs, here a comprehensive study of p-type $Cu_2O$ TFTs was performed, investigating devices, materials, and theory. First of all, the key challenges that limit device performance were identified at the device level and at the thin film level. It was confirmed that the effective field effect mobility can be improved by reducing the high contact resistance and high density of interface traps. The thin film mobility can be increased by controlling neutral impurity and grain size. Both mobilities are also strongly affected by process temperature. Finally, to address the problems that suppress the field effect mobility, the N:$Cu_2O$ S/D contact layer was suggested to reduce the high contact resistance and high-*k* dielectric engineering was performed to address the high interface traps. In sum, this

thesis clearly explains the factors that need to be addressed to improve device performance and suggests possible methods to further advance p-type $Cu_2O$ TFTs.

This in-depth study included device fabrication, electrical test, and simulation as well as materials synthesis and characterization. The main contributions of this thesis can be summarized as follows:

1. P-type $Cu_2O$ thin films were experimentally demonstrated using RF magnetron sputtering. A post-deposition anneal (PDA) at 600 °C in vacuum was performed. The film crystal phase achieved after PDA was found to be dependent on the film thickness. X-ray diffraction techniques showed that a 20 nm thin film enabled phase-pure $Cu_2O$, with a Cu(I) fraction of 87.2% and Cu(II) fraction of 12.8%. According to the literature [44], $Cu_2O$ has a lower effective mass than CuO, which indicates that increasing the Cu(I) fraction in $Cu_2O$ thin films is critical to increase hole mobility. Electron beam techniques revealed that the surface morphology also varies with film thickness. The 20 nm $Cu_2O$ thin film has an island-like morphology. No segregation of Cu was observed within the grains. In addition, the grains were found to be more conductive compared to the grain boundaries. This means that lateral conduction in the $Cu_2O$ film may be limited by grain boundaries. Thus, from the viewpoint of $Cu_2O$ material preparation for high performance p-type TFT, it is critical to achieve a pure $Cu_2O$ phase thin film with a large grain size.
2. Thin film transistors (TFTs) were fabricated using the $Cu_2O$ thin film process described above. The p-type $Cu_2O$ TFTs exhibited a field effect mobility of ~0.06 $cm^2V^{-1}s^{-1}$, much lower than the Hall mobility of ~10 $cm^2V^{-1}s^{-1}$. Based on the transmission line method (TLM), the extracted specific contact resistance was 26 kΩ-$cm^2$. The estimated ratio of contact resistance to total resistance ($2R_C/R_T$) was ~40%. Although the $2R_C/R_T$ value was

reduced as negative gate voltage was applied – from 40% at off-state to 33% at on-state – it is still high. An interface trap density ($D_{it}$) of ~$3 \times 10^{13}$ $cm^{-2}eV^{-1}$ was extracted from the TFT sub-threshold region. The effect of these non-idealities on TFT performance were supported by TCAD simulation. In brief, I found that the large gap between $\mu_{FE}$ and $\mu_{Hall}$ originates from high $R_C$ and high $D_{it}$.

3. The hole scattering mechanisms that limit $\mu_{Hall}$ of the $Cu_2O$ thin films were investigated via temperature-dependent Hall measurements. I compared a polycrystalline $Cu_2O$ thin film (*pc*-$Cu_2O$) sample and a single crystalline $Cu_2O$ bulk (*sc*-$Cu_2O$) sample. The temperature-dependence of the hole concentration was analyzed using a two-acceptor model. The activation energies of the two acceptors are 0.21 eV and 0.40 eV for *pc*-$Cu_2O$ and 0.33 eV and 0.45 eV for *sc*-$Cu_2O$. The temperature-dependence of mobility was analyzed using models of optical/acoustic phonon scattering, neutral/ionized impurity scattering, and grain boundary scattering. My analysis showed that neutral impurity and grain boundary scattering are the dominant scattering mechanisms in *pc*-$Cu_2O$, while phonon scattering is the dominant factor for *sc*-$Cu_2O$. This result indicates that the neutral impurity concentration and grain size need to be controlled to maximize the intrinsic hole mobility of $Cu_2O$.
4. The effect of process temperature on TFT behavior was studied using material, electrical, and optical characterization. The temperature at which post-deposition annealing or deposition is performed during $Cu_2O$ thin film synthesis is a critical factor in determining the field effect mobility and Hall mobility. Higher process temperatures led to better crystallinity and larger grain size. In addition, ToF-SIMS detected lower concentrations of chlorine impurities which can act as donors (*i.e.*, hole killers) and as scattering centers.

The corresponding electrical properties show that TFTs made with higher process temperatures have relatively higher field effect mobility, higher Hall mobility, and lower trap density. Optical results showed that $Cu_2O$ thin film processed at 600°C has the lowest structural disorder, which agrees well with the electrical results. The wide range of field effect and Hall mobility obtained indicates that optimizing the deposition and post-deposition process conditions is important to minimize the thermal budget.

5. To reduce the contact resistance, a nitrogen-doped $Cu_2O$ ($N:Cu_2O$) thin film was developed by introducing $N_2$ gas during RF magnetron sputtering. As the $N_2$ gas flow increased, the thin film resistivity ($\rho$) was reduced by more than 1000× from 312 Ω-cm to ~0.2 Ω-cm. By adding a 13-nm $N:Cu_2O$ interlayer in the source/drain region of $Cu_2O$ TFTs, the $\mu_{eff}$ was increased from 0.006 $cm^2V^{-1}s^{-1}$ to 0.031 $cm^2V^{-1}s^{-1}$ (~5×). TLM results showed that the specific contact resistance is reduced from 511 Ω-$cm^2$ to 17.1 Ω-$cm^2$ (~1/20×). Based on the thermionic emission model, I found that the addition of the $N:Cu_2O$ S/D interlayer lowered the effective barrier height from 0.66 eV to 0.57 eV. This work shows that the addition of a heavily-doped $Cu_2O$ S/D interlayer can effectively reduce the contact resistance of $Cu_2O$ TFTs.
6. To address the high density of interface traps, dielectric engineering for the $Cu_2O$ thin film transistor was performed. Since the $Cu_2O$ thin film transistors with an $SiO_2$ gate dielectric layer showed a high interface trap density, $HfO_2$ was evaluated as an alternate gate oxide. For TFTs with a bottom-gate (BG) structure, the exposure to a 600°C post-deposition anneal (that is required to form high-quality $Cu_2O$) caused Cu/Hf interdiffusion and redox for both $HfO_2$ single layer dielectrics and $HfO_2/SiO_2$ bilayer dielectrics. Since this interdiffusion made it difficult to demonstrate BG $HfO_2$ TFTs, the top-gate TFT

architecture was investigated using a 30 nm $HfO_2$ top gate dielectric. The preliminary results showed a high gate leakage current, possibly due to excessive gate-to-source/drain overlap, surface roughness, or other issues. Further study is required to identify pathways to achieving high-*k* dielectrics in $Cu_2O$ thin film transistors. Finally, addition of a passivation layer was investigated to address the back-channel defects. The addition of a $HfO_2$ passivation layer improved the on-current and the subthreshold slope. However, there is a trade-off between $HfO_2$ thickness and the TFT improvements, so future optimization of passivation layer thickness is required.

In addition to the topics discussed in this thesis, I demonstrated thin film transistors made using copper oxide semiconductor layers grown by atomic layer deposition (ALD). The ALD growth was performed by my collaborator, Julia L. Lenef. Here, it was observed that, regardless of the process module (i.e., ALD or PVD), TFTs have similar device performance after 600 °C PDA. Further discussion of our ALD $Cu_2O$ TFT results can be found in ref. [181]. I also performed temperature-dependent TFT measurements using PVD and ALD $Cu_2O$ TFTs to extract the Arrhenius activation energy, which are similar to the intrinsic acceptor levels that were theoretically estimated by my collaborator, Zihao Deng. Further details on these results can be found here [182]. Thus, the body of work done as part of this thesis provides key insights for wide bandgap high performance $Cu_2O$ thin film transistors for future oxide-based CMOS technologies. Some of the results in or related to this thesis have been already published in numerous journal articles [71], [95], [98], [181] and conference presentations [183]–[191], and others are expected to be published in the near future.

## 7.2 Future Work

The development of wide bandgap high performance p-type $Cu_2O$ thin film transistors is critical to demonstrate future oxide semiconductor thin film electronics based on CMOS devices, which will enable diverse applications. Continuous effort is required to push the boundaries of p-type $Cu_2O$ thin film transistor technology. As discussed in this thesis, I have identified the key challenges that limit TFT performance but more work is needed to solve the problems originating from contact resistance and interface traps. In addition, since a thermal budget of 400 ℃ was not sufficient to achieve satisfactory $Cu_2O$ TFT operation, optimizing the device performance at low process temperature remains an important challenge to enable diverse applications such as BEOL device on Si MOSFET and flexible electronics. Finally, although in this thesis I focused on addressing device-level issues, further work is needed to control and minimize charge carrier scattering in order to maximize the intrinsic mobility. Based on the results in this thesis, it is expected that following works will enable the further improvement of the $Cu_2O$ thin film transistor.

1. **Realization of single-crystalline or single grain $Cu_2O$ thin film transistors to avoid grain boundary traps.** According to Chapter 2 and Chapter 3, interface traps and grain boundary traps are critical factors that limit field effect mobility in $Cu_2O$ TFTs. Demonstrating single-crystalline or single grain $Cu_2O$ without grain boundaries would enable us to understand the relationship between field effect mobility and grain boundary traps. Recently, there was a report [192] on grain boundary-free Sb:$Cu_2O$ TFT with a novel vertical structure and high field effect mobility. This indicates the importance of controlling the grain boundaries that limit hole transport.
2. **Determining the effect of $Cu_2O$ thin film orientation on $Cu_2O$ thin film transistor.** As discussed in Chapter 4, a wide range of Hall mobility and field effect mobility was

observed at a given temperatures. According to a previous study [139], the Hall mobility and surface morphology of the $Cu_2O$ thin film depends on the grain orientation of the film. More investigation is needed to understand the relationship between field effect mobility and crystal orientation. By studying TFT performance for different grain orientations, we can identify pathways to maximize the field effect mobility at a given thermal budget.

3. **Heavily doped $Cu_2O$ source/drain to reduce contact resistance.** In Chapter 5, it was confirmed that while incorporation of a N:$Cu_2O$ layer at the source/drain reduces the contact resistance, the contacts are still not fully linear and have too large a resistance. To achieve low resistance ohmic contacts, we should develop other technologies to achieve heavily-doped $Cu_2O$. In addition to nitrogen, my collaborators predicted that sulfur can also act as p-type dopant in $Cu_2O$ [182]. It would be interesting to explore whether TFT with S:$Cu_2O$ source/drains have ohmic conduction. Furthermore, another approach to reduce contact resistance is via a metal-interlayer-semiconductor (MIS) contact, which has been shown to alleviate Fermi-level pinning in p-type SnO [59]. Exploring MIS contacts for $Cu_2O$ channels may also be worthwhile, since $Cu_2O$ contacts also suffer from Fermi level pinning [71]. Clearly, there are many routes to solve the contact resistance issues for wide bandgap p-type $Cu_2O$.

   To effectively design $Cu_2O$ contacts, a robust understanding of key materials parameters such as electron affinity, Fermi level, and bandgap is needed. Although some values have been reported for electron affinity (= ~3.1 eV) and work function (= ~4.84 eV) of $Cu_2O$ [44], further theoretical and experimental work to validate these values also would greatly facilitate the design of $Cu_2O$ electronic devices.

4. **Optimization of p-type $Cu_2O$ thin film transistors using top-gate structure with high-*k* dielectric.** The top-gate structure is an effective way to evaluate high-*k* dielectrics while avoiding issues related to process temperature induced Cu diffusion. However, as discussed in Chapter 6, a high gate leakage current was observed in my preliminary results on top gate TFTs, possibly due to excessively large gate-to-source/drain metal overlap. Since a metal-$HfO_2$-metal structure can form localized conducting paths, such as those characteristically used in memristors [193], [194], such memory phenomena need to be minimized in TFTs. Thus, future work is needed on mask design to minimize the gate-to-source/drain overlap, and on optimizing the dielectric thickness to minimize memristive behavior while obtaining maximum capacitive coupling. Once an optimized top-gate structure can be realized, comprehensive evaluation of the impact of high-*k* dielectrics on $Cu_2O$ TFT performance, including interface traps, will be needed.

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