N-polar GaN HEMT with HfO_2 as Gate Dielectric for mm-wave Applications

by

Subhajit Mohanty

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical and Computer Engineering)
in the University of Michigan
2023

Doctoral Committee:

Assistant Professor Elaheh Ahmadi, Chair
Professor Cagliyan Kurdak
Professor Wei Lu
Professor Zetian Mi
Professor Umesh K. Mishra

Subhajit Mohanty

subhajit@umich.edu

ORCID iD: 0000-0002-1469-5363

© Subhajit Mohanty 2023

Dedication

To my dad, mom, my wife Ashley and my cat Olivia.

Acknowledgements

"If I have seen further, it is by standing on the shoulders of giants."

– Sir Isaac Newton

It has been a wonderful five years in the WBME lab. I would like to express my deepest appreciation to my advisor, Prof. Elaheh Ahmadi, for her unwavering support and guidance. I remember the first day when I joined her lab with little knowledge of fabrication, GaN or HEMT. She taught me the concepts and guided me through the process from scratch and after five years I feel much more confident in the field of GaN electronics. She has helped me evolve not only as a researcher, but also as a holistic person. I have been truly fortunate to have Elaheh as my advisor. This endeavor would not have been possible without the inspiration and help of Prof. Umesh Mishra. His insightful suggestions for my research results helped me approach problems in a novel way. I am incredibly grateful to Prof. Wei Lu for introducing me to many new devices and concepts in course EECS 521. I want to thank Prof. Zetian Mi for his encouragement and collaboration work in ScAlN and DLTS. Many thanks to Brian, Onur, and Xun at Prof. Mishra's group for answering my fabrication questions, which helped me establish the fabrication process flow here at UMich. I could not thank Matt Guidry more for guiding me through the network parameter analyzer measurement setup.

I cherish the moments I spent with my labmates at UMich. Kam helped me with regrowth in my fabrication process. Though it is just a small part of the collaboration, it is such a crucial step in my HEMT device. Many thanks to Sandra for preparing all the documents for DC testing lab. I

have always enjoyed the time I spent working with Ashley, Oguz, Stefan, Irfan, Xin, Harsh, Ethan, Christopher, Tomas in cleanroom where I learned many new things at each step of my life. Ashley trained me on various clean room tools and taught me the basics of fabrication. She helped me navigate the initial years of academic life smoothly. Thank you Xin, Ruby and Wen for keeping the dude-vibe in our group. I also learnt a lot working with Prof. Mi's lab members, Ping, Ding, and Ayush.

Lurie Nanofabrication Facility (LNF) has been an important part of my PhD journey for the past five years. The staff members were extremely helpful. There were situations where I had to contact them at night and received a response from the staff. Special thanks go to Shawn for helping me a lot with lithography on stepper and plasma etch with Lam tool. I would also like to thank Matt for helping me with ALD and Vishva for helping me with e-beam lithography.

I am also extremely grateful to the ECE staff, especially Kristen, who has helped me with all the administrative procedures. Radlab staff Michelle and Kim were the most efficient people I have worked with, and they always provided me with fast and accurate solutions to my needs. I also thank John for providing me with an opportunity to represent as an ECE student ambassador.

I would to thank the primary funding agency Office of Naval Research for supporting my research financially. I would also like to thank Rackham which has also extended financial support for conference and fellowships at the time of need.

I would also like to thank my friends from India who has made my stay in the US wonderful. Saket has been a constant part of my life for the past five years. Thanks to Nagesh, Mahitosh and Debu for treating me delicious Indian food at ICC coop.

I would like to express my deepest gratitude to my wife Ashley and cat Olivia who have been always there by my side during PhD journey. Our cat Olivia was a great emotional booster during

the Ph.D.. Lastly, I cannot be more thankful to my parents who have been there with me at each step of my life. Their inspiration and blessings have established me as I am today.

Table of Contents

Dedication ii

Acknowledgements iii

List of Tables ix

List of Figures x

Abstract xiv

Chapter 1 Introduction 1

1.1 RF Wireless Communication 1

1.2 Key Performance Index 3

1.2.1 High f_T and f_{max} 3

1.2.2 Power and Efficiency 4

1.3 Why GaN 5

1.3.1 High Frequency of Operation 5

1.3.2 High Power and Efficiency 6

1.3.3 Less Design Complexity 7

1.3.4 Wide Temperature Range 8

1.3.5 Reliability and Robustness 8

1.4 Why N-polar 11

1.4.1 Strong Confinement from Back-barrier 12

1.4.2 Improved Scaling 13

1.4.3 Improved Ohmic contact 13

1.4.4 GaN Cap in Access Region 15

1.4.5 Reduced Leakages 16

1.4.6 Comparison of Device Performance ... 17
1.5 Dissertation Overview ... 19
Chapter 2 Investigation and Optimization of HfO_2 Gate Dielectric on N-polar GaN ... 21
2.1 Introduction ... 21
2.1.1 Why HfO_2 ... 21
2.1.2 Characterization Methods of Interface States ... 23
2.1.3 Chapter Overview ... 26
2.2 As-deposited HfO_2 on GaN HEMT Epi-structure ... 26
2.2.1 Device Fabrication ... 26
2.2.2 Results and Discussion: ... 28
2.3 HfO_2 Characterization on GaN MOSCAPs ... 32
2.3.1 Device Fabrication ... 32
2.3.2 Results and Discussion ... 33
2.4 Conclusion ... 40
Chapter 3 N-polar GaN MIS-HEMT with High-k ALD HfO_2 as Gate Dielectric ... 42
3.1 Introduction ... 42
3.2 Device Fabrication ... 43
3.3 Results and Discussion ... 44
3.4 Conclusion ... 49
Chapter 4 N-polar Deep Recessed (NPDR) HEMT with HfO_2 as gate dielectric ... 50
4.1 Introduction ... 50
4.2 Device fabrication ... 51
4.3 Results and Discussion ... 53
4.4 HfO_2 Thickness series ... 56
4.5 Conclusion ... 60

Chapter 5 Design of Ultra-scaled-channel N-polar GaN HEMTs with High Charge Density: A Study of Hole Traps and Their Impact on Charge Density in the Channel 61

5.1 Introduction 61

5.2 Simulation Framework 63

5.3 Results and Discussion 63

5.3.1 Hole Traps and Their Impacts on 2DEG Density 63

5.3.2 Estimation of Hole Trap Density and Energy Level at AlN/GaN NPI 68

5.3.3 Si Doping to Prevent Hole Trap Ionization 69

5.4 Conclusion 74

Chapter 6 Future Work 75

6.1 N-polar Deep Recessed HEMT with $HfZrO_2$ as gate dielectric 75

6.2 Improvement in HfO_2 leakage: 76

6.3 Regrown Ohmic contact improvement: 76

6.4 Scaled HEMTs for high frequency application: 77

Bibliography 78

List of Tables

Table 1.1 Material properties of various materials [1]. 4

Table 2.1. Summary of the techniques that were employed for surface preparation, in-situ pretreatment, ALD deposition, and post-deposition annealing. 33

Table 2.2 Effect of in-situ TMA/N2 plasma on various bulk and interface characteristics. 34

Table 2.3. Effect of Rapid thermal annealing ambience on bulk and interface characteristics. ... 35

Table 2.4 Effect of various surface cleaning methods on bulk and interface characteristics. 38

List of Figures

Figure 1.1 RF frequency range and various applications (a) commercial (b) military applications. 1

Figure 1.2 Projected market growth for RF front end. 2

Figure 1.3 Schematic of HEMT with various device parameters 3

Figure 1.4 Johnson Figure of Merit (JFoM) for various material systems [1]........ 5

Figure 1.5 A comparison of output power vs frequency for different material systems [5]........ 6

Figure 1.6 A comparison of multistage GaAs vs GaN Power amplifier (PA) [6]. 7

Figure 1.7 Component count for a massive MIMO antenna [5]. 8

Figure 1.8 Technology comparison of Mean-Time-To-Failure versus Channel Temperature. https://www.mpdigest.com/2019/10/24/gan-on-sic-is-driving-advances-in-radar-applications/. .. 9

Figure 1.9 (a) Importance of various material parameters for various commercial applications [8] (b) Impact of GaN device Characteristics on system level advantages [9]. 10

Figure 1.10 GaN Wurtzite crystal structure in (a) Ga-face (b) N-face, with spontaneous polarization vector. 11

Figure 1.11 Epi-structure, charge profile, and band diagram of typical Ga-polar (left) and N-polar (right) hetero-structures. The 2DEG forms below the barrier in Ga-polar. This is in contrast with N-polar hetero-structures in which the 2DEG forms on top of the barrier and leads to better confinement of the 2DEG, more gate control specially in scaled HEMTs, and lower ohmic contact resistance [17]. 12

Figure 1.12 (a) Band diagram of GaN/InN regrown region in N-polar GaN HEMT. A large bandoffset of 1eV exists at GaN/InN interface. (b) band diagram of GaN/gradedInGaN/InN regrown region [28]. 14

Figure 1.13 (a) Device cross-sectional schematic (not drawn to scale) and epitaxial layer profile of the N-polar deep recess (NPDR) MISHEMT with the foot-gate self-aligned to the GaN cap recess. (b) Energy band diagram comparing the vertical profiles under the gate electrode as compared to the access region with the addition of a GaN cap layer........ 16

Figure 1.14 A schematic of a Ga-Polar HEMT band diagram at (a) equilibrium and (b) with a reverse gate-drain voltage applied. (c) and (d) give the energy band diagram of a N-Polar HEMT

with a thin AlGaN top-barrier at equilibrium and at a reverse gate-drain voltage bias, respectively [31]. 17

Figure 1.15 W-Band output power density of various GaN device technologies over time. Traditional Ga-polar AlGaN/GaN HEMTs have saturated around 2 W/mm while N-polar GaN has recently demonstrated 7.94 W/mm [17]. 18

Figure 2.1 Schematic of the structures studied in this work (a) HfO_2 on SiN (b) HfO_2 on AlGaN after removal of SiN and (c) HfO_2 on GaN after removal of SiN and AlGaN cap layer. 27

Figure 2.2CV profile measured at different frequencies on MOSCAP-C with 15nm-thick HfO_2which (a) was not annealed and annealed for (b) 1min and (c) 5 min at 400°C in N_2. 28

Figure 2.3 CV profiles measured at 1 MHz on MOSCAPs with various HfO_2 thicknesses. 29

Figure 2.4 Capacitance measured at 0 V versus HfO_2 thickness. 30

Figure 2.5 CV profile measured at different frequencies on (a) MOSCAP-B and (b) MOSCAP-C. 31

Figure 2.6 Fabrication process flow of HfO_2/N-polar GaN MIS structure. 32

Figure 2.7 Forward bias Current-Voltage (CV) characteristics of N_2 annealed (Sample 3), N_2+O_2 annealed (Sample 4) and O_2 annealed (Sample 5). 36

Figure 2.8 Density of states (D_{it}) profile as the function of energy for Sample 1 (baseline), 6 and 7 (UV + Ozone). 37

Figure 2.9 (a) C-V hysteresis (b) HF C-V for fast and slow trap estimation (c) Forward flatband voltage shift for Sample-7. 39

Figure 3.1 (a) Schematic diagram of N-polar MIS-HEMT with 10.7 nm thick HfO_2 as gate dielectric (b) C-V characteristics (green) and 2DEG charge density (green) measured on MOSCAP with 100 μm diameter, the blue curve shows the 2DEG concentration with gate bias voltage. .. 42

Figure 3.2 (a) Output characteristics and (b) Corresponding gate leakage current for Vgs from -8 V to 0 V with 2 V increments. The extracted Ron is 1.28 Ω-mm at Vgs = 0V. 43

Figure 3.3(a) Transfer characteristics (blue) and trans-conductance (green) at V_{DS} = 3 V (b) drain current and gate leakage in semi-log scale. The subthreshold slope is 135.7 mS/dec. 44

Figure 3.4 Dual Pulsed-IV measurement was measured with pulse width and duty-cycle 10 μs and 0.1% respectively at various gate and drain quiescent voltages. Corresponding (a) I_D-V_D (b) I_D-V_G (c) g_m and (d) normalized I_{DSS}, R_{ON}, g_m, ΔV_{TH}. 45

Figure 3.5 Breakdown voltage (BV) of device with different gate-drain distance (L_{gd}) with various gate lengths and corresponding error in BVs. 46

Figure 3.6 (a) RF performance HEMT, Contour plots of fT and fmax w.r.t. V_{GS} and V_{DS} without pad de-embedding. 47

Figure 3.7. Large signal performance of the device at 4 GHz. (a) Dependence Pout and PAE on VDS and Power performance at VDS =4 V, I_{DSS} = 100 mA/mm. 49

Figure 4.1 Device cross-sectional schematic and epitaxial layer profile of the N-polar deep recess (NPDR) with HfO_2 as gate dielectric (b) Energy band diagram comparing the vertical profiles under the gate electrode as compared to the access region with the addition of a GaN cap layer 50

Figure 4.2 (a) Output characteristics and for Vgs from -8 V to 0 V with 2 V increments. The extracted Ron is 1.28 Ω-mm at Vgs = 0V. 51

Figure 4.3(a) Transfer characteristics (blue) and trans-conductance (green) at V_{DS} = 3 V (b) drain current and gate leakage in semi-log scale. The subthreshold slope is 111.2 mS/dec. 52

Figure 4.4 (a) RF performance HEMT, Contour plots of fT and fmax w.r.t. VGS and VDS 52

Figure 4.5. Large signal performance of the device at 4 GHz. (a) Dependence Pout and PAE on VDS and Power performance at VDS =9 V, I_{DSS} = 100 mA/mm. 53

Figure 4.6 Dual Pulsed-IV measurement was measured with pulse width and duty-cycle 10 µs and 0.1% respectively at various gate and drain quiescent voltages. 54

Figure 4.7 CV hysteresis and IdVg hysteresis for sample-A, B & C with 10.1 nm, 7.1 nm, 4.4 nm HfO_2 thickness respectively. The hysteresis decreases with increase in HfO2 thickness. 55

Figure 4.8 Normalized I_{DSS}, normalized dynamic Ron, and Vth shift was measured for three devices D4, E4, F4 which has 1µm, 1.5µm, 2µm gate-to-drain distance for three samples with three different gate dielectric thickness (a)10.1nm, (b)7.1nm, (c)4.4nm. All the parameters were almost same indicating that traps in the gate-to-drain region does not cause DC-RF dispersion 57

Figure 4.9 Various parameters (Normalized IDSS, normalized dynamic Ron, and Vth shift) were compared for three samples (Sample-A, B & C) with three different gate dielectric thickness 10.1nm, 7.1nm, 4.4nm respectively for same devices (a) D4 with Lsd=1 µm (b) E4 with Lsd=1.5 µm 55

Figure 4.10. Large signal performance at 4 GHz for three samples (Sample-A, B & C) with three different gate dielectric thickness 10.1nm, 7.1nm, 4.4nm respectively for same devices. Dependence P_{out} and PAE on V_{DS} and Power performance at different V_{DS}, I_{DSS} = 100 mA/mm.59

Figure 5.1 Schematic cross-section of epi-layer, **(b)** the band diagram with donor trap at E_t = 715 meV for $N_t = 3\times10^{13}$ cm^{-2}, **(c)** different charges present in the structure along c-axis. Traps are assumed to be present at AlN/GaN NPIs. Ionized hole traps are positively charged. 62

Figure 5.2 **(a)** Band diagrams for epi-structure described in Fig. 4.1 (a) with 2nm-thick AlN interlayer assuming hole trap with energy of 715 meV and different trap densities at NPIs for barrier height of 0.3 eV at GaN channel surface, **(b)** magnified band diagram near VB at barrier-

buffer interface, **(c)** Density of ionized traps shown for all the 14 NPIs, for three different trap densities throughout the epi-structure. 65

Figure 5.3 (a) Band diagrams for epi-structure described in Fig. 4.1 (a) with 4 nm-thick AlN interlayer assuming hole trap with energy of 715 meV and different trap densities at NPIs for barrier height of 0.3eV at GaN channel surface, (b) magnified band diagram near VB at barrier-buffer interface, (c) Density of ionized traps shown for all the 14 NPIs for three different trap densities throughout the epi-structure. 66

Figure 5.4**.** 2DEG vs donor trap energy varying trap density for AlN interlayer thickness of (a) 2 nm and (b) 4 nm for epi-structure described in Fig. 4.1(a) with 10 nm channel thickness. (c) 2DEG vs donor trap energy, assuming N_t= 3×10^{13} cm^{-2} (d) 2DEG vs donor trap densities, assuming E_t = 215 meV for epi-structure described in Fig. 4.1(a) with 4nm-thick AlN interlayer and varying GaN channel thickness. 67

Figure 5.5 2DEG density as a function of GaN channel experimentally measured (red circles), simulated including hole traps with 0.3 eV barrier height, density and energy of 3×10^{13} cm^{-2} and 280 meV w.r.t. valence band (blue squares), and simulated without including traps (green stars). 68

Figure 5.6 (a) Series-A: doping in 15 nm thick GaN at the interface between the digital-alloy barrier and buffer layer; corresponding band diagram for AlN interlayer thickness of (b) 2 nm, (c) 4 nm for various doping level at E_t = 280 meV with N_t = 3×10^{13} cm^{-2} **(d)** 2DEG density as a function of Si doping concentration. 70

Figure 5.7 **(a)** Series-B: doping in digital-alloy barrier, **(b)** corresponding band diagram for 4 nm AlN interlayer with different doping density for E_t = 280 meV, N_t = 3×10^{13} cm^{-2} and **(c)** 2DEG density as a function of Si doping concentration in barrier (series-B) and at the back-barrier GaN buffer interface (series-A). 71

Figure 5.8 **(a)** Series C doping strategy: doping in both back-barrier and the buffer layers, **(b)** corresponding band diagram for 4 nm AlN interlayer with different doping density for E_t = 280 meV, N_t = 3×10^{13} cm^{-2} and **(c)** corresponding 2DEG variation with back-barrier doping. 72

Figure 5.9 (a) Optimized epi-structure with Series-C doping, blue colour shows changed thickness of layers from structure in Fig. 4.1(a). (b) band diagram, (c) 2DEG is independent of trap density and energy over a wide range since all the traps are neutralized by Si doping, (d) 2DEG vs GaN channel thickness for the optimized design series-C doping of 8×10^{18} cm^{-3}, N_t = 3×10^{13} cm^{-2} at E_t = 280 meV, (e) A wide range of doping (6×10^{18} cm^{-3}-1×10^{19} cm^{-3}) shows lower parasitic and zero trap ionization. 73

Figure 6.1 Figure 6.1 (a) Energy vs polarization diagram for ferroelectric, non-ferroelectric and subsequent negative capacitance from combined (ferroelectric+non-ferroelectric) material [115] (b) Device cross-sectional schematic and epitaxial layer profile of the N-polar deep recess (NPDR) with $HfZrO_2$ as gate dielectric 75

Figure 6.2 (a) Device cross-sectional schematic and (b) SEM image of high aspect ration N-polar deep recess (NPDR) HEMT with T-gate [2] 77

Abstract

N-polar GaN-based HEMTs have shown tremendous promises for high-power high-frequency (30-110 GHz) applications due to several advantages such as better pinch-off, low ohmic contact and better gate control. To further achieve higher frequency of operation while maintaining high power, the gate-to-channel distance and gate length need to be scaled down simultaneously to avoid short-channel effects (SCEs). However, extreme scaling of gate-to-channel distance will result in higher gate leakage current which requires thick dielectrics and in-turn reduces gate-to-channel distance and gate control. This requires high-k dielectric as gate insulator whose small effective oxide thickness (EOT) can suppress gate leakage while maintaining good gate control.

This dissertation primarily is focused on developing HfO_2 as gate dielectric for ultra-thin N-polar GaN HEMT application.

In the first part of the dissertation, the impact of various surface cleaning, in-situ atomic layer deposition (ALD) pre-treatment, ALD deposition method and post-deposition annealing ambiance on interface properties of HfO_2/ N-polar GaN was studied via UV-assisted C-V and current-voltage characterization methods. A combination of the BHF and piranha cleaning with UV-ozone pretreatment followed by thermal HfO_2 improved the interface between HfO_2 and N-polar GaN quality significantly. Further annealing in O_2 increased the breakdown voltage, and reduced the interface states compared to annealing in N_2. The lowest average interface trap density was achieved to be 1.64×10^{12} cm^{-2} eV^{-1} with breakdown field of 3.14 MV/cm.

All the processes developed previously were used for fabrication of planar N-polar GaN MIS-HEMTs. The dual pulsed-IV measurements suggest that there are two competing mechanisms at play during device operations resulting in anti-dispersion and dispersion at the same time. Additionally, to reduce the DC-RF dispersion, N-polar deep recess (NPDR) HEMTS with HfO_2 as gate dielectric have been explored. BCl_3/SF_6 selective dry etch was developed to realize deep-recess structure with thin AlGaN cap as etch stop layer. The HEMTs exhibited a peak saturation current of 1.1A/mm with f_T=18.1GHz and f_{max} = 66.1 GHz. The HEMTs biased in class AB at V_{DS}=9 V and I_{DS}=100 mA/mm at 4 GHz frequency demonstrated a max output power of 1.53 W/mm with associated PAE of 45.4%. Pulsed IV measurements reveal that the deep recess structure did not exhibit DC-RF dispersion from surface traps present in drain access region. Rather the traps present in the gate dielectric cause dispersion which has been shown to depend on the thickness of the dielectric. In fact, the dispersion is less than 10% at a very thin dielectric of 4.4 nm.

It is reported that interfacial nitrogen vacancies at negative polarization interface (NPI) were the source of these hole/donor traps. Using the Silvaco TCAD simulation platform, for the first time, the effect of hole traps density and energy level on 2DEG density in N-polar HEMT structures was studied. Comparing the calculated 2DEG density with that of experimental results, hole trap density and activation energy were estimated. The results showed that Si doping in both the barrier and at barrier-buffer interface effectively neutralizes the traps present throughout the epi-structure while simultaneously modulating the 2DEG charge density. Moreover, an epi-structure was designed to enable aggressive scaling of the channel (5nm-thick) in N-polar GaN HEMTs while maintaining a large 2DEG density of approximately 2.6×10^{13} cm^{-2} with minimal parasitic.

Chapter 1

Introduction

1.1 RF Wireless Communication

RF wireless communication is touching every aspect of life such as health, communication, and defense. In the military defense industry, radars in early warning system, counter measure warfare, etc. use a wide range of frequency spectrum from MHz to GHz. Terahertz imaging is used in food and plastic inspection to complex imaging machines used for health monitoring. Mobile communication base stations operate in lower GHz spectrum (~3.5 -25 GHz) with demand to go

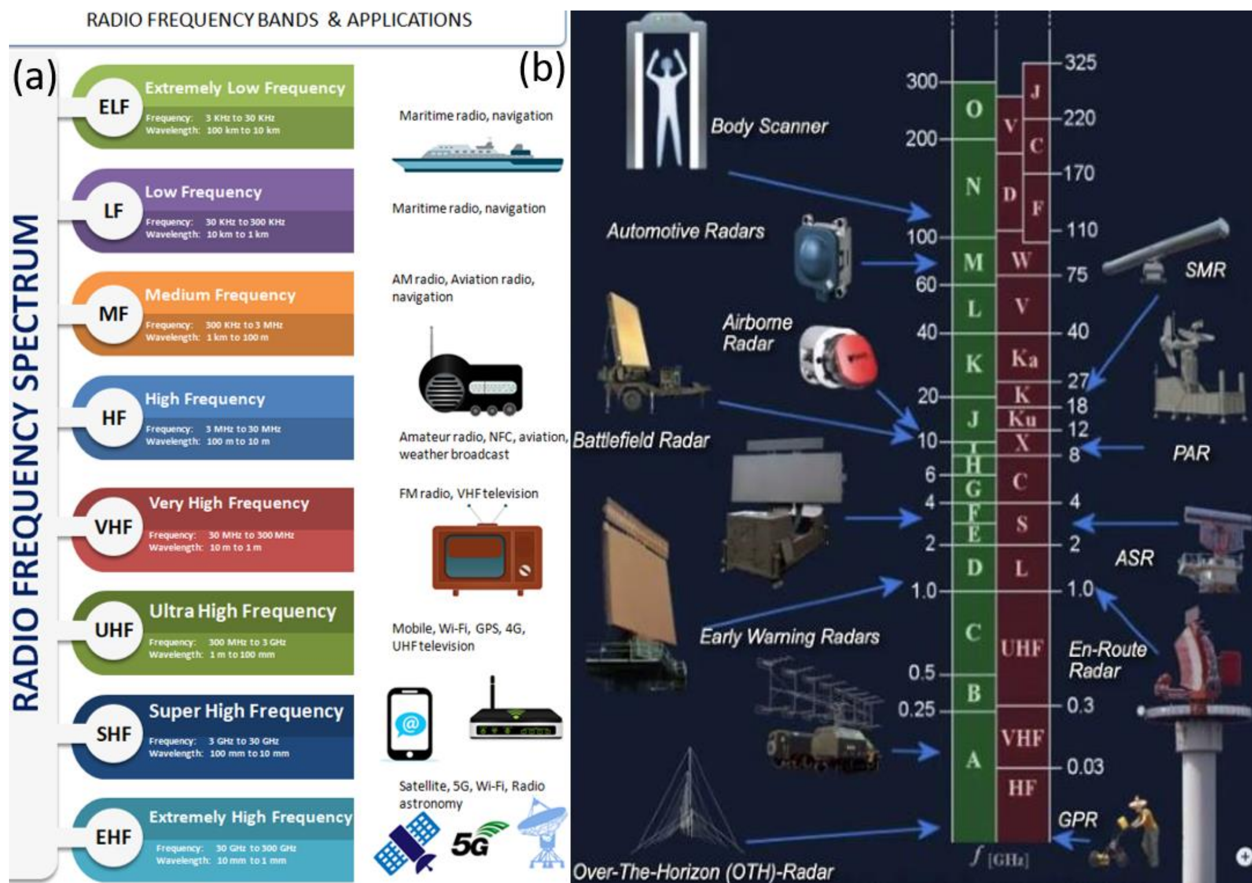


Figure 1.1 RF frequency range and various applications (a) commercial (b) military applications.

towards higher frequency. With telecommunication traffic data being projected to grow significantly higher by early 2030, high resolution, faster data and low latency is the need of the hour. This in turn requires advanced electronics with higher frequency of operation and wide bandwidth. Many such electronics operate over a wide range of frequency spectrum and bandwidth and are rapidly evolving. For instance, only a few years ago, the telecommunication industry was debating the feasibility of 5G. In few years span, not only the standards has been decided, but also prototypes and field trials have already been demonstrated successfully. Now it is in use en-masse for commercial mobile communication. There is not a shred of doubt that the next decade belongs to 5G and RF. However, this poses several design challenges to the RF and device engineer. Electronics need to be compatible with a wide range of frequency and bandwidth. Power, efficiency, bandwidth, and speed all need to be taken into account. Emerging segments such as

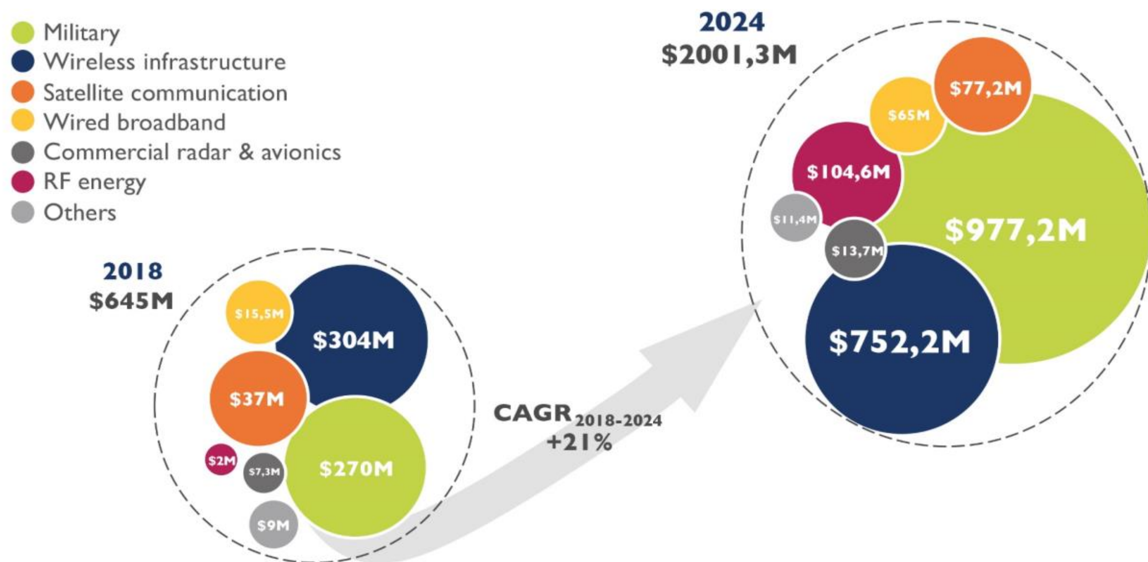


Figure 1.2 Projected market growth for RF front end.

satellite communication (SatCom) and consumer handsets present new opportunities as well as challenges. According to the market research, by Yole Développement (Yole), the power amplifier module is poised to grow from US$5.4 billion in 2019 to US$8.9 billion by 2025 with CAGR of 11%. The overall RF front end connectivity market will grow to US$25.4 billion from US$15 billion with CAGR of 11%.

1.2 Key Performance Index

1.2.1 High f_T and f_{max}

Current gain cutoff- frequency (f_T) [2] and power-gain cutoff frequency (f_{max} [3]) are two important parameters for RF application. These two in turn, depend on many device parameters (Fig 1.3). To improve the frequency of operation, it is necessary to increase the trans-conductance of amplifier while reducing parasitic resistances and capacitances.

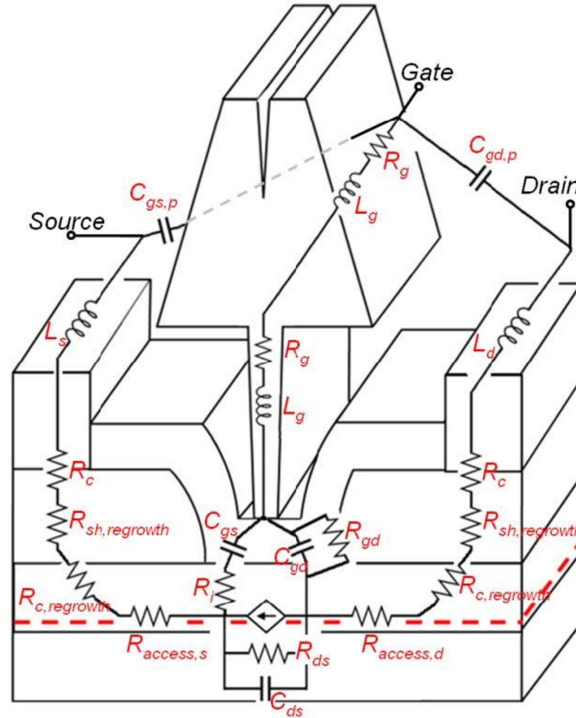


Figure 1.3 Schematic of HEMT with various device parameters [116].

$$f_T = \frac{g_m}{2\pi\left\{\left(C_{gs}+C_{gd}\right)(1+\frac{R_s+R_d}{R_{ds}})+C_{gd}\cdot g_m\cdot(R_s+R_d)\right\}} \approx \frac{v_s}{2\pi L}$$

$$f_{max} = \frac{\frac{g_m}{2\pi(C_{gs}+C_{gd})}}{\sqrt{\frac{4}{R_{ds}}\left(R_g+R_s+R_i\right)+8\pi\cdot f_T\cdot C_{gd}\left(2R_g+R_s+R_i\right)}}$$

1.2.2 Power and Efficiency

RF transistors should be able to produce high power in the intended frequency of operation. For instance, for radar applications, the power requirement depends on the fourth power of distance. Power density is another parameter which impacts the device dimension and subsequent cost. Efficiency is another parameter which is essential for component count and thermal management of the entire system.

Table 1.1 Material properties of various materials [4].

	Si	GaAs	GaP	4H-SiC	Diamond	GaN	AlN
Band gap (Eg) (eV)	1.1	1.4	2.3	3.2	5.5	3.4	6.2
Thermal Conductivity (W/cm.K)	1.5	0.5	1.1	4.9	20	1.3	3.9
Melting Point (K)	1683	1513	1740	2830	3773	2791	3273
Electron Saturation Velocity (cm/s)	1	2	1.25	2	2.7	2.5	1.4
Electron mobility (cm^2/V.s)	1400	8500	350	950	2200	1000	135
Hole mobility (cm^2/V.s)	600	400	100	120	1600	30	14
Dielectric Constant	11.8	12.5	11.1	9.7	5.5	8.9	8.5
Breakdown Field (E_C) (MV/cm)	0.3	0.6	1	2	10	2.6	2
JFOM ($\frac{v_{sat} \cdot E_C}{2\pi}$) (normalized to Si)	1	0.93		14		17	
BFOM ($\frac{\varepsilon_S \cdot \mu \cdot E_g^3}{2\pi}$) (normalized to Si)	1	16		430		990	

1.3 Why GaN

So the question is: which material system will dominate the RF market? Gallium Nitride has surfaced as a candidate for high power and high frequency applications due to its unique properties, including a large bandgap of 3.4 eV, large breakdown electric field of 2.6 MV/cm, and high electron mobility and saturation velocity (**Table 1.1** [4]) which provides following advantages:

1.3.1 High Frequency of Operation

As mentioned before, current gain cut-off frequency (f_T) and power gain cut-off frequency (f_{max}) are the two most critical parameters for RF applications. High mobility and high 2DEG charge reduce the channel resistance in the device which improves the frequency. High 2DEG charge also improves the semiconductor-metal contact resistance by improving the channel access resistance. Moreover, GaN also possesses comparatively lower dielectric constant which reduces the parasitic capacitances in the device improving f_T [2] and f_{max} [3] additionally.

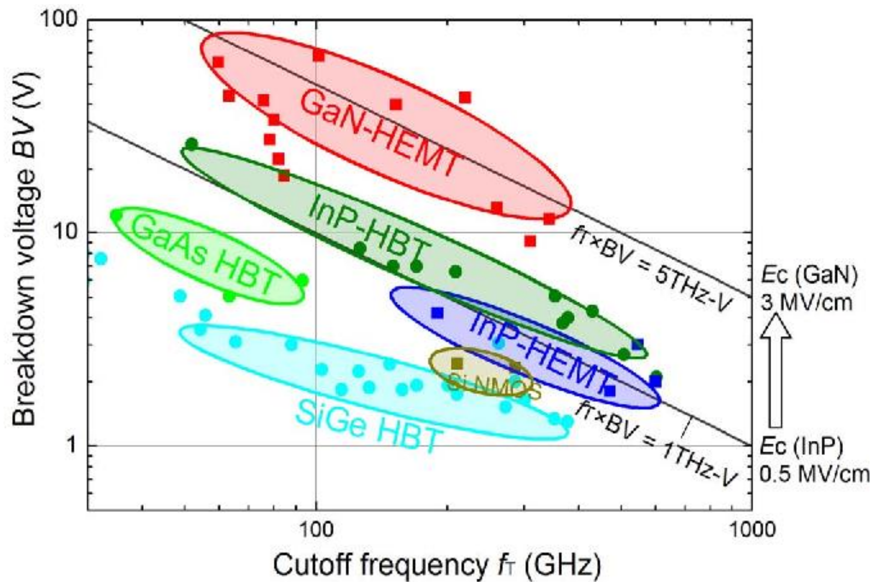


Figure 1.4 Johnson Figure of Merit (JFoM) for various material systems [1].

1.3.2 High Power and Efficiency

GaN has a larger bandgap and higher breakdown electric field which allows it to operate at significantly higher voltages as compared to other material systems such as Si, GaAs and InP. As device dimensions are scaled smaller to increase the operating frequency, this in turn deteriorates the breakdown voltage (BV) which limits the dynamic range of operation. The product of f_T and BV is commonly referred as Johnson figure of merit (JFoM) which is used to benchmark various high-speed device technologies. GaN-HEMTs demonstrate the highest JFoM almost an order higher than Si and GaAs devices as shown in **Fig. 1.4** [1].

Additionally, power is directly related to breakdown voltage. GaN, due to its wide bandgap, has a high critical electric field, and therefore, a larger breakdown voltage at a given frequency compared to other available high frequency semiconductor materials including Si, InP, and GaAs. Therefore, GaN-based transistors have demonstrated superior power performance over a wide frequency range (**Fig. 1.5** [5]). The emergence of GaN technology operating at 28 V to 50

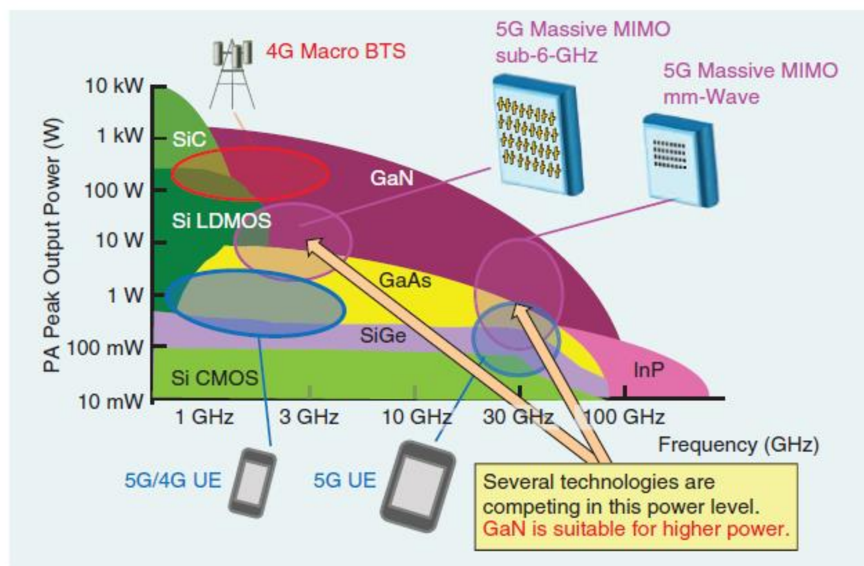


Figure 1.5 A comparison of output power vs frequency for different material systems [5].

V on a low RF loss, a high thermal conductivity substrate like silicon carbide (SiC) has opened up a range of new possibilities.

1.3.3 Less Design Complexity

The most power-consuming element of radio transmitter is the power amplifier (PA) (> 60%). Hence any improvement in its power consumption and efficiency will have a significant impact on the entire circuit complexity. Since GaN has a high power density, it requires less number of amplifiers to achieve the same amount of gain and RF power output. For instance, as shown in **Fig. 1.6** [6], in the case of GaAs, multiple amplifier stages and branching with seven amplifiers are required to achieve a specific power level. To do so, RF dividers and combiners are utilized to distribute and combine the output powers of each stage. However, since GaN has a higher power density, hence the same power can be achieved by cascading few GaN PAs. Additionally, GaN is preferable due to the following: (i) simplified circuitry by eliminating peripheral components, reducing power loss, hence improving efficiency (ii) GaN has higher power density, hence requires smaller devices compared to GaAs and thereby providing competitive cost benefits (iii) GaN has a higher thermal conductivity which may simplify the cooling requirements (iv) the high BV of GaN material system eliminates the use of RF limiter

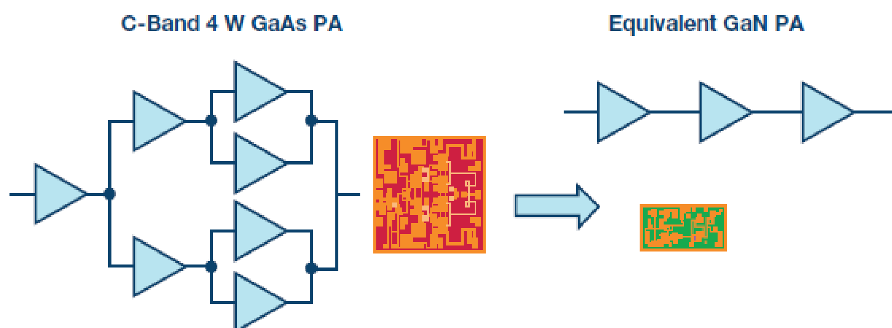


Figure 1.6 A comparison of multistage GaAs vs GaN Power amplifier (PA) [6].

used to protect the LNA from high voltages which reduces overall size and complexity. This can further be seen from **Fig. 1.7** which illustrates the component count in a massive MIMO antenna for various device technologies [5].

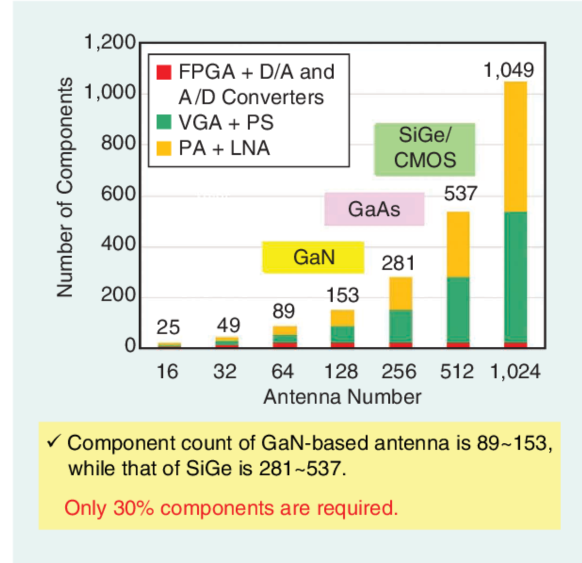


Figure 1.7 Component count for a massive MIMO antenna [5].

1.3.4 Wide Temperature Range

Low bandgap devices are particularly susceptible to high temperature failure. In the case of Si, at higher temperature, the intrinsic carrier concentration exceeds the doping level rendering the device inoperable which limits its operational temperatures below 100 °C. However, the intrinsic carrier concentration is about twelve orders of magnitude lower in GaN [7], which allows them to operate at high temperatures. The lower intrinsic carrier concentration also translates to lower intrinsic leakage current and low noise in GaN HEMTs.

Similarly, at low temperatures, carrier freeze-out effect renders S-based devices inoperable. In contrast, 2DEG forms in the lower bandgap material in a GaN/AlGaN HEMT which does not freeze-out. Moreover, lower temperature improves the mobility of electrons. Deep space applications exploit this low temperature feature to design extremely low noise, high gain microwave devices.

1.3.5 Reliability and Robustness

Mean time to failure (MTTF) is a parameter used to characterize reliability and robustness of a device structure. GaN demonstrates one order higher MTTF compared to Si and GaAs (Fig. 1.8).

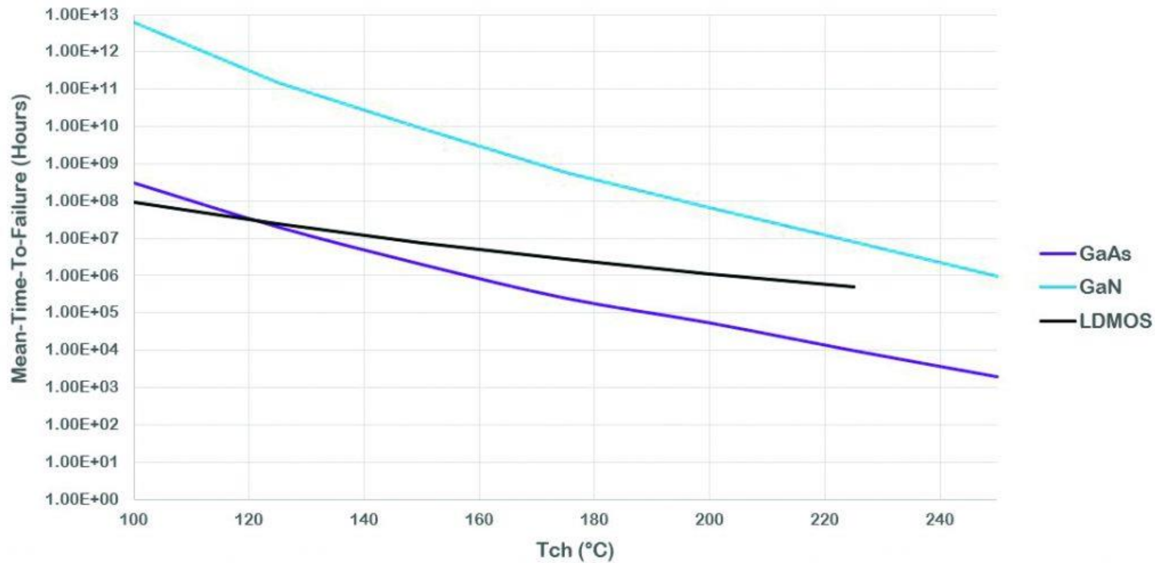
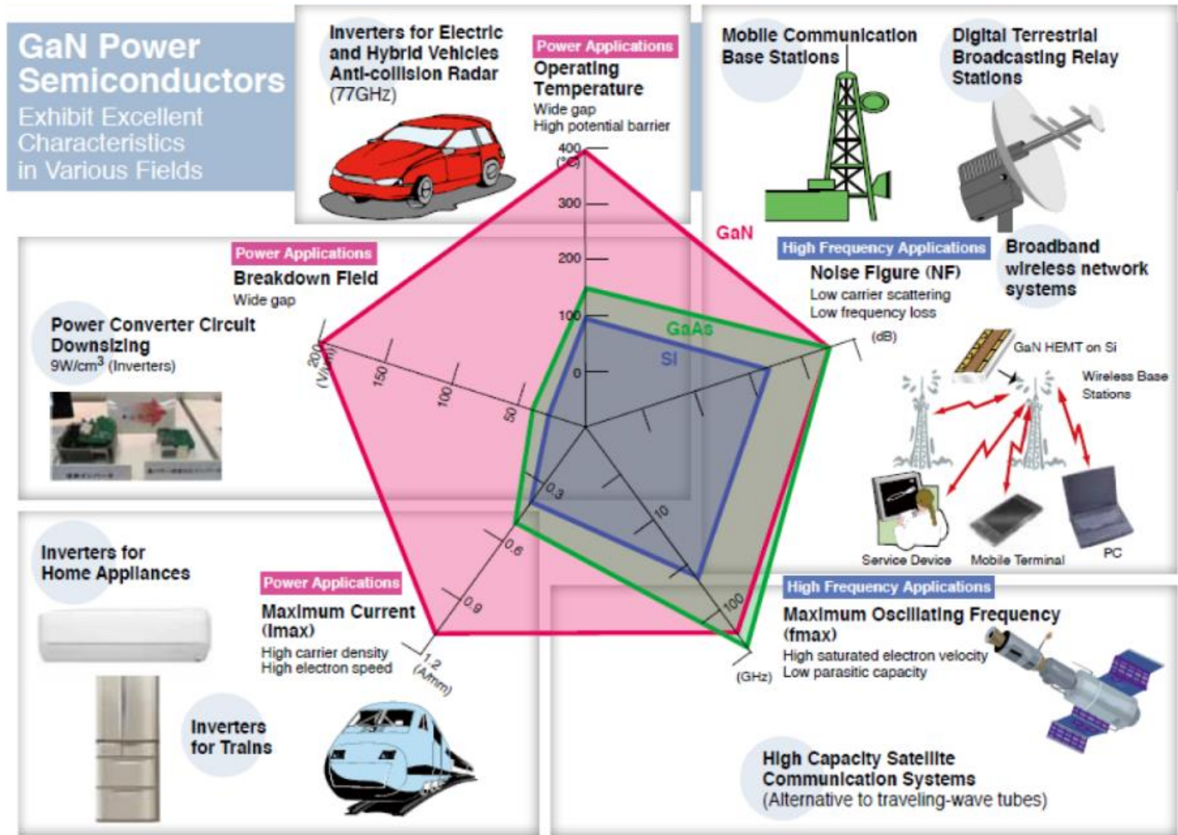


Figure 1.8 Technology comparison of Mean-Time-To-Failure versus Channel Temperature. https://www.mpdigest.com/2019/10/24/gan-on-sic-is-driving-advances-in-radar-applications/.

In summary, GaN-based RF and power electronics are going to define many crucial "more-electric" transportation systems and communication systems in near future. This relies on the enhanced efficiency in conversion processes afforded by wide bandgap materials from kHz to GHz frequency spectrum. In particular, there is a need for efficient solid-state power amplification to replace complex, low-efficiency multi-stage circuits and bulky and fragile vacuum tubes in defense applications. Additionally, in the era of internet of things (IoT), artificial intelligence and autonomous vehicles, there is an urgent need for high-power and high frequency transistors that can facilitate ultra-fast, highly reliable, and low latency wireless networks. To serve these needs, transistors which can provide a combination of high power density and high efficiency at high frequencies are required. **Figure 1.9** summarizes the importance of various material parameters for different applications [8] and illustrates the impact of GaN device characteristics on the PA metrics and system-level advantages [9].



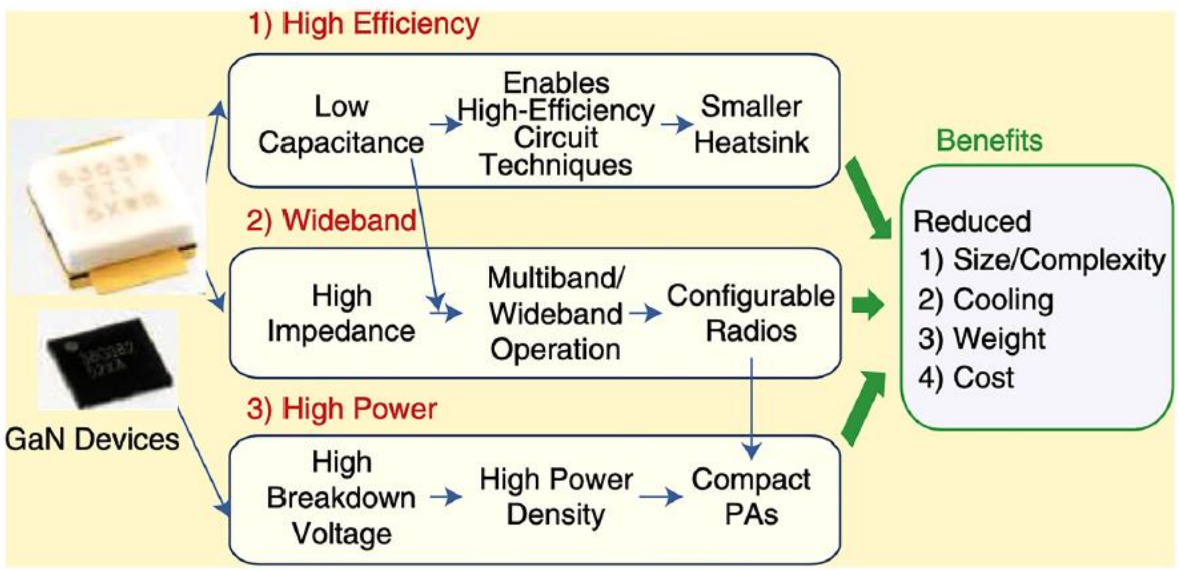


Figure 1.9 (a) Importance of various material parameters for various commercial applications [8] (b) Impact of GaN device Characteristics on system level advantages [9].

1.4 Why N-polar

GaN is most stable in a Wurtzite crystal structure as shown in **Fig. 1.10**. This crystal structure lacks inversion symmetry, with the polarization field in the material depending on the crystal orientation. When the crystal is oriented in the [0001] direction, it is terminated with Ga atoms on the surface and has negative net polarization, which is known as Ga-polar or Ga-face. On the other hand, the $[000\bar{1}]$ orientation is terminated with N atoms and has positive net polarization, which is called N-polar or N-face. GaN-based optoelectronic and electronic devices for commercial applications have been mainly developed on Ga-polar GaN templates due to less complexity of epitaxial growth compared with that on N-polar [10–16]. Nonetheless, N-polar GaN-based HEMTs have several advantages over Ga-polar GaN-based HEMTs that make them a promising candidate for highly scaled devices.

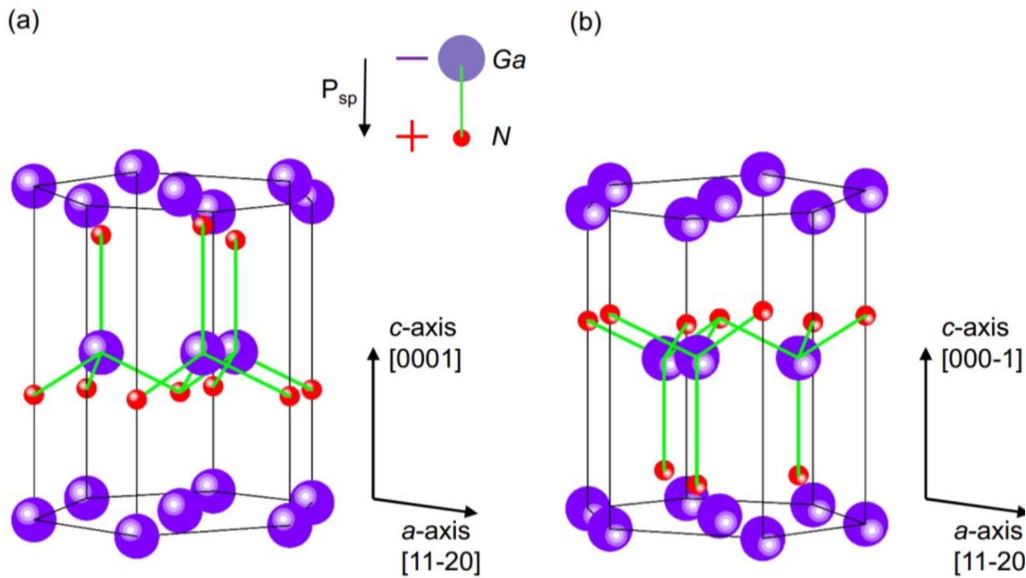


Figure 1.10 GaN Wurtzite crystal structure in (a) Ga-face (b) N-face, with spontaneous polarization vector.

1.4.1 Strong Confinement from Back-barrier

The epi-structure and corresponding band diagram with 2DEG wave-function for Ga-polar and N-polar HEMT is shown in **Fig. 1.11** [17]. As negative gate voltage is applied, it depletes the 2DEG channel and turns off the HEMT. In Ga-polar HEMT, the negative gate bias pushes the electron wave function away from the gate whereas in N-polar it is sandwiched by the underlying back-barrier. This improves confinement results in a sharp pinch-off characteristics in N-polar HEMTs as well as reduces output conductance which improves the short channel effects (SCEs) of HEMTs. Several simulation studies [18,19] supported these predictions.

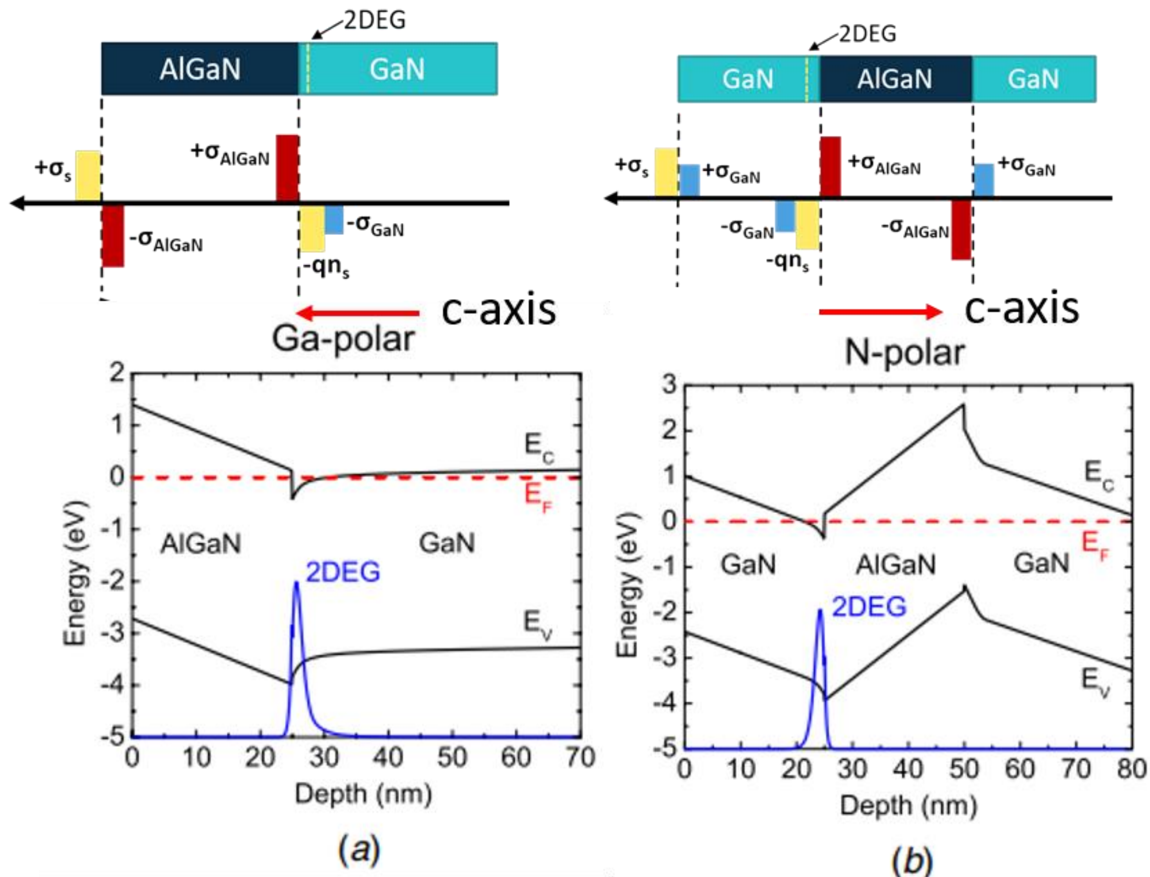


Figure 1.11 Epi-structure, charge profile, and band diagram of typical Ga-polar (left) and N-polar (right) hetero-structures. The 2DEG forms below the barrier in Ga-polar. This is in contrast with N-polar hetero-structures in which the 2DEG forms on top of the barrier and leads to better confinement of the 2DEG, more gate control specially in scaled HEMTs, and lower ohmic contact resistance [17].

1.4.2 Improved Scaling

The current gain cut-off frequency depends on gate length (Lg) in the first order which can be enhanced significantly by reducing the gate length. However, this can lead to SCEs such as lowered output resistance, limited benefits in trans-conductance because of diminished charge control and threshold voltage variation with gate length [20][21]. SCEs can be alleviated significantly by proportionately scaling down the gate-to-channel thickness while simultaneously reducing gate length which is referred as high aspect ratio design [22][23][24]. In Ga-polar HEMTs, the 2DEG concentration depends on the AlGaN barrier composition and thickness [25]. Higher the composition and thickness higher the 2DEG. Hence reducing the barrier thickness leads to a reduction in the 2DEG concentration which is not desirable as it increases the sheet and contact resistances. Therefore, a tradeoff exists between barrier thickness and RF frequency in Ga-polar HEMTs.

On the contrary, the 2DEG concentration in N-polar HEMTs depends additionally on the back-barrier thickness, composition and doping [26]. Thus, it is possible to achieve a thinner channel required for high frequency applications while maintaining higher 2DEG by increasing the thickness or polarization of backbarrier. InAlN back-barriers are particularly attractive since it has higher polarization while being lattice-matched to GaN removing upper limit on the thickness of back-barrier due to strain limitation [27]. The additional back-barrier design breaks the trade-off that exists with Ga-polar HEMT and provides designers with an additional knob to improve the HEMTs.

1.4.3 Improved Ohmic contact

As shown in **Fig. 1.11(a)**, the top layer in Ga-polar HEMT is AlGaN which has a higher bandgap making it difficult to achieve a good ohmic contact with the 2DEG. One possible way is

to etch down the barrier layer under the source/drain ohmic contacts selectively. However this reduces the 2DEG concentration as it depends on AlGaN barrier the thickness [25] as discussed previously.

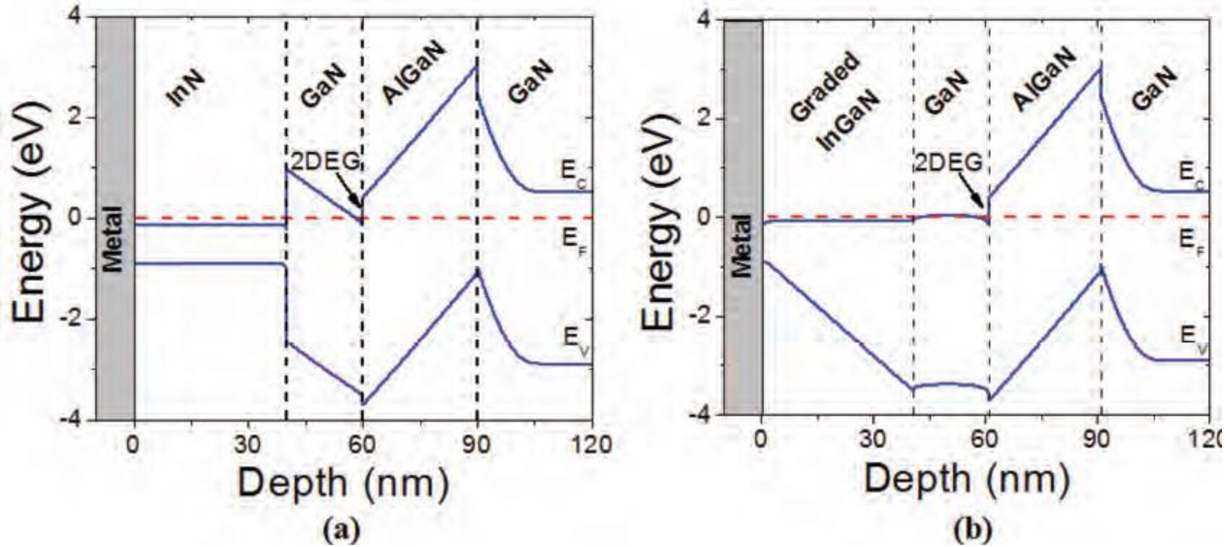


Figure 1.12 (a) Band diagram of GaN/InN regrown region in N-polar GaN HEMT. A large bandoffset of 1eV exists at GaN/InN interface. (b) band diagram of GaN/gradedInGaN/InN regrown region [28].

In contrast, the top layer is low band-gap GaN in N-polar HEMT which results in a lower contact resistance. Moreover, even smaller contact resistance can be achieved by using selective-area ohmic regrowth. A non-alloyed metal–2DEG contact resistance of < 0.03 Ω·mm obtained in N-polar GaN HEMTs through selective-area regrowth of graded n^+ InGaN has remained the lowest in III-nitride transistors to date [28]. In this work, an n^+ InN was regrown in source/drain regions on N-polar HEMT structures. A very low Metal-to-InN contact resistance of 5 Ω.µm was achieved, which was attributed to the pinning of the conduction band of InN under the fermi level resulting in a surface accumulation layer with a 2DEG charge density of 1×10^{13} cm^{-2}. However, InN on GaN results in the conduction band discontinuity of 1 eV, which can negatively affect metal-to-2DEG contact resistance. This was resolved by introducing a graded n+ InGaN in-between, which brings the conduction band down because of formation of a 3D electron gas due to the positive

polarization of InGaN layer [28] as shown in **Fig. 1.12**. The graded layer was grown by reducing the Ga flux gradually while maintaining the temperature constant. The contact resistance of 23 Ω-μm was achieved with 0-63% InGaN grading with doping 1×10^{19} cm^{-3} which can be further reduced by increasing final Indium percentage and doping.

For applications that do not need such ultra-low contact resistance, regrown n^+ GaN has been used for non-alloyed ohmic contacts. Regrowth of an n^+ GaN is simpler than a graded InGaN film and can also result in low contact resistances ranging from 0.058 Ω-mm [29] to 0.16 Ω-mm [30] depending on the growth quality and doping concentration. It is important to note that non-alloyed ohmic contacts are not only important to obtain low contact resistance, but also to eliminate non-ideal effects such as dispersion observed in N-polar HEMTs with alloyed contacts [31]. A very large degradation in saturation current was observed during pulsed-IV measurements on N-polar HEMTs with alloyed contact due to the combination of a positive V_{th} shift and a degradation of the trans-conductance whereas non-alloyed contact measured in this study showed negligible dispersion [31].

1.4.4 GaN Cap in Access Region

Planar GaN HEMTs suffer from surface trap related current collapse and knee walkout commonly known as DC-RF dispersion. During device operations, traps present on the surface can capture electrons and become negatively charged. These negatively charged traps act as a virtual gate and deplete the 2DEG channel underneath which increases the on-resistance and reduces the drain current. Traditionally, PECVD SiN passivation or field-plates have been utilized to reduce the dispersion which introduce additional parasitic capacitances rendering them undesirable for mm-wave applications. By introducing a GaN cap in the access region [32], it moves the surface

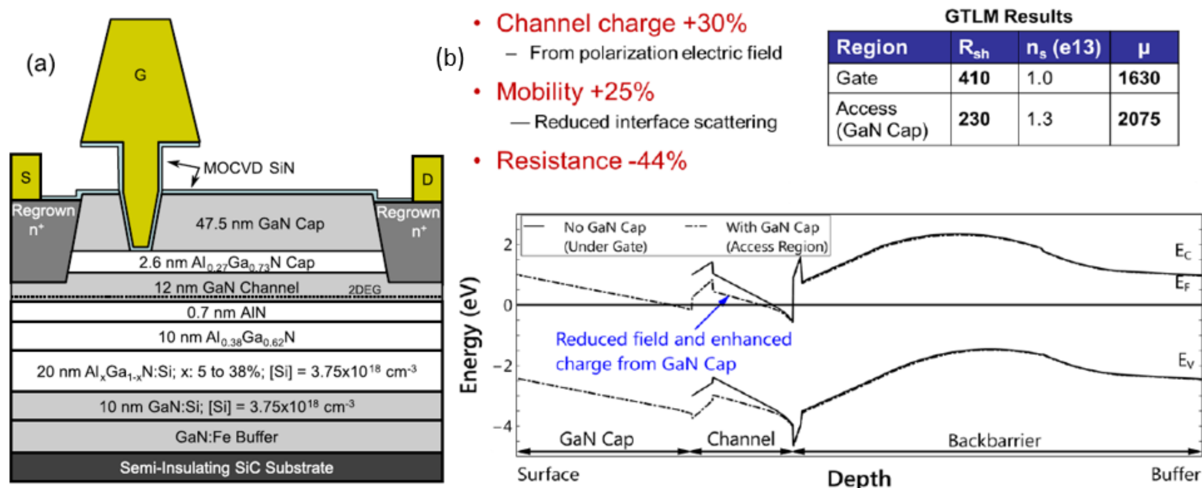


Figure 1.13 (a) Device cross-sectional schematic (not drawn to scale) and epitaxial layer profile of the N-polar deep recess (NPDR) MISHEMT with the foot-gate self-aligned to the GaN cap recess. (b) Energy band diagram comparing the vertical profiles under the gate electrode as compared to the access region with the addition of a GaN cap layer.

traps away from the channel and makes the pinch-off voltage in the access region more negative (-30V), consequently resulting in less DC-RF dispersion.

Additionally, the GaN cap enhances the conductivity of the access regions for three reasons. The introduction of GaN cap layer reduces the vertical electric field in the access region as shown in the **Fig. 1.13(b)**. This pushes the conduction band downwards in the channel which leads to an increase in 2DEG concentration. Moreover, the reduction in vertical electric field improves the lateral mobility. Third, the surface is moved away from the channel which reduces the surface scattering and further improves the mobility. These combined effects have shown to reduce the sheet resistance from 325 Ω/sq in the gate region to 220 Ω/sq in the access region in these NPDR structures.

1.4.5 Reduced Leakages

Since the Schottky barrier to GaN is lower than that on AlGaN, the early N-polar GaN HEMTs suffered from significantly larger gate leakage than that often observed on Ga-polar

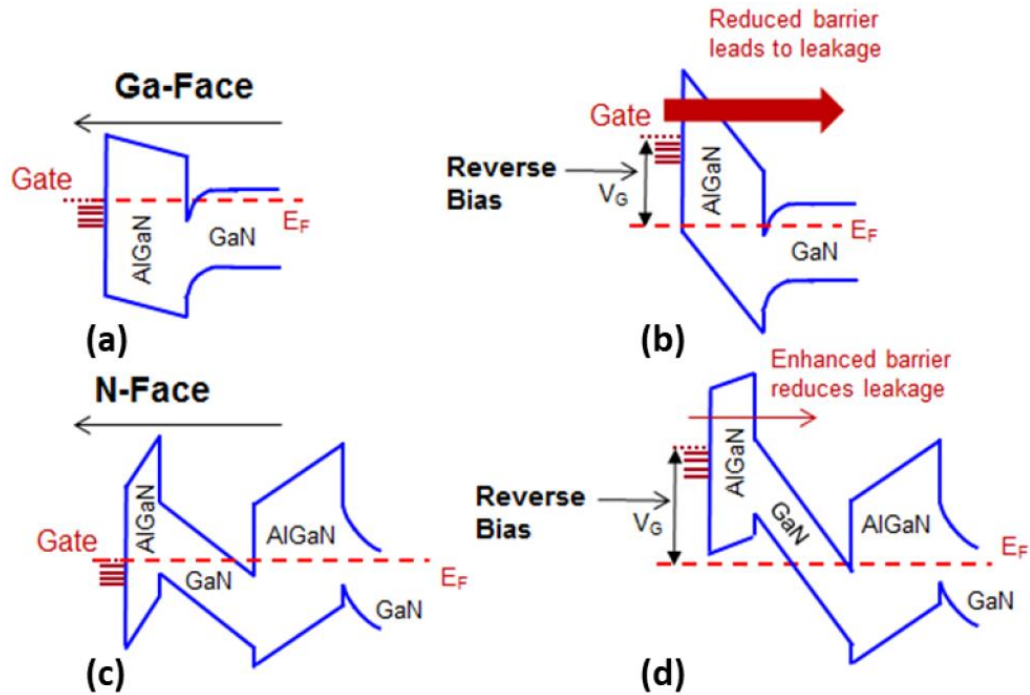


Figure 1.14 A schematic of a Ga-Polar HEMT band diagram at (a) equilibrium and (b) with a reverse gate-drain voltage applied. (c) and (d) give the energy band diagram of a N-Polar HEMT with a thin AlGaN top-barrier at equilibrium and at a reverse gate-drain voltage bias, respectively [31].

HEMTs. A 25 nm thick 10% AlGaN cap layer was also introduced in these N-polar HEMTs to increase the Schottky barrier and reduce the gate leakage. This AlGaN cap layer in N-polar HEMT structures reduces the gate leakage not only by increasing the Schottky barrier height, but also by reducing the tunneling current under large reverse gate biases. The latter is a unique feature in N-polar HEMT structures due to the opposite polarization field in these structures compared with that in Ga-polar HEMTs [31] (**Fig. 1.14**). Introducing the AlGaN cap layer resulted in a significantly lower gate leakage current with more than a three-fold increase in breakdown voltage.

1.4.6 Comparison of Device Performance

Reported Ga-polar HEMTs and monolithic microwave integrated circuits (MMICs) have demonstrated excellent performance from Ka-band (27-40 GHz) through W-band (75-110 GHz).

In Ka-band, HEMT devices offering 9.7 and 10.5 W/mm of output power (*P*o) and power-added efficiencies (PAE) of 43% and 33% at 30 and 40 GHz respectively have been demonstrated [33,34]. Devices have also been demonstrated with output power of 3.1 and 4.3 W/mm at 30-GHz with PAE of 52% by Moon et al [33]. MMICs of highly scaled devices have also been recently reported with a PAE of 59% at 32 GHz but the power density at the output stage was limited to 440 mW/mm [35]. As frequency of operation increases, the output power and efficiency reduce due to trade-off between power and frequency that depends on the semiconductor properties such as bandgap and electron mobility. At 83 GHz, a MMIC with a peak PAE of 27% and *P*o of 1.7 W/mm has been demonstrated [36]. At 94 GHz, a pre-matched device with 24.2% PAE and 1.5 W/mm Po [37] was reported and at 86 GHz, Niida et al. have reported 3.6 W/mm with 12.7% PAE [38].

Alternatively, as discussed before, N-polar HEMT offer additional degrees of freedom to design the devices due to its natural back barrier, inverted polarization and better confinement which is conducive to mm-wave application. Using N-polar GaN with deep recess gate structure,

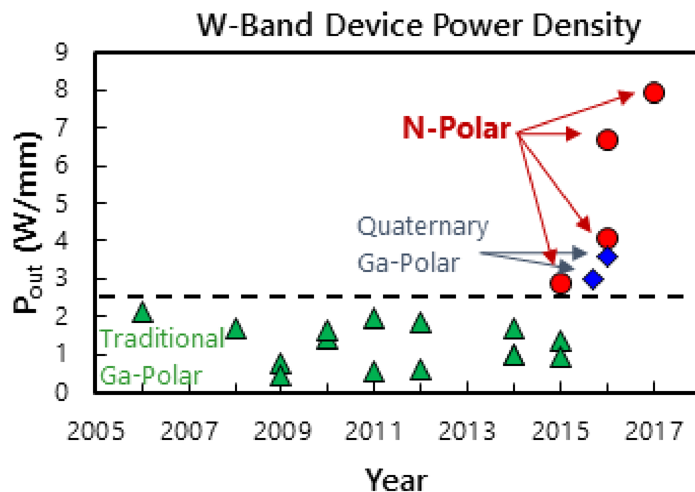


Figure 1.15 W-Band output power density of various GaN device technologies over time. Traditional Ga-polar AlGaN/GaN HEMTs have saturated around 2 W/mm while N-polar GaN has recently demonstrated 7.94 W/mm [17].

6.7W/mm at 94 GHz with 14.4% associated PAE using a realigned gate process and 27.8% PAE with 8W/mm at 94 GHz using a self-aligned gate process have been reported. This is more than twice of the output power typically measured on conventional Ga-polar GaN HEMTs with more than twice the efficiency as well (**Fig. 1.15**). Romanczyk et al. [39] have reported peak PAE of 55.9% measured at 14 V with an associated *P*o of 5.3 W/mm and 52.5% PAE with 8.08 W/mm at 20 V at 30GHz. No devices to date had demonstrated constant output power density over frequency range as expected in an ideal device (since power density is not a function of frequency; output power is). Romanczyk et al [39] have reported the N-polar device with 7.94W/mm output power at W-Band, Ka-Band and X-Band, the first device to do so.

1.5 Dissertation Overview

The goal of this dissertation is to explore high-k as dielectric for ultra-thin N-polar HEMT for mm-wave Applications. We have developed high quality thermal HfO_2 ALD films on N-polar GaN and used this as dielectric to fabricate and characterize the N-polar HEMT which has better performance.

Chapter 2 presents the dielectric study of HfO_2 on N-polar GaN. Metal-Oxide-Semiconductor capacitors (MOSCAP) were fabricated to study the interface and bulk properties of HfO_2 using deep UV-assisted capacitance-voltage measurements. Different surface cleaning method, in-situ plasma activation, ALD deposition method and annealing environment was systematically studied to achieve better quality HfO_2. The HfO_2 /GaN MOSCAPs achieve small hysteresis, low interfacial trap density, low leakage current, and moderate breakdown electric field.

Chapter 3 utilizes the developed HfO_2 dielectric to fabricate N-polar MISHEMT. Several fabrication steps were developed in the cleanroom such as slow GaN etch to reduce the impact of plasma on surface states during etching thin layers, regrown source/drain to achieve low ohmic

contact, HfO_2 etching using BCl_3 plasma. DC, pulsed-IV, BV and small signal RF measurements were carried out to analyze and understand the operation of N-polar HEMT with HfO_2 as dielectric.

In Chapter-4, N-polar deep recessed HEMT (NPDR) were demonstrated with HfO_2 as gate dielectric. Additional fabrication steps were introduced such as selective BCl_3/SF_6 etch to achieve recess under gate and source/drain with smooth surface. HfO_2 thickness series was performed to understand the effect of gate dielectric bulk traps on DC-RF dispersion.

In Chapter 5, an attempt was made to develop a thin channel HEMT epi-layer with large 2DEG concentration using Silvaco TCAD simulation. GaN/AlN digital alloy was used as backbarrier since AlN has higher polarization and digital alloy has better thermal conductivity compared to bulk GaN. Impact hole traps in GaN/AlN HEMT system was studied and various doping scheme with band engineering was used to eliminate its effect. The effect of various inter-layer thickness, doping were studied to obtain an optimized structure with minimum parasitic over wide range of doping. 2DEG as high as 3×10^{13} cm^{-2} was achieved both from simulation and experimentally. However the mobility was extremely small (~600 $cm^{-2}/V.s$).

Chapter 2
Investigation and Optimization of HfO_2 Gate Dielectric on N-polar GaN

2.1 Introduction

2.1.1 Why HfO_2

N-polar GaN HEMT has demonstrated much higher power density and efficiency which has positioned itself as a major contender for RF applications as discussed in the previous chapter. However, the demand for faster data, higher bandwidth is increasing which requires higher and higher frequency of operation. The frequency of operation can be further enhanced significantly by reducing the gate length. This however can lead to short-channel effects (SCEs) such as lowered output resistance, limited benefits in trans-conductance because of diminished charge control and threshold voltage variation with gate length [20][21]. However, SCEs can be alleviated significantly by reducing the gate-to-channel thickness while reducing gate length which is commonly referred as a high aspect ratio design [22][23][24]. This high aspect ratio scaling typically leads to higher gate leakage due to thinner barrier and higher electron tunneling probability. This leakage can be suppressed by a thick insulator layer between channel and gate metal; however, this reduces the gate capacitance. High-k dielectrics such as HfO_2 are particularly advantageous in such scenarios since a thicker dielectric can be deposited without altering the gate capacitance. Hence it is important to develop a high-k dielectric with superior interface states and border traps to enable next-generation high-power high-frequency N-polar GaN-based transistors.

Several groups have studied high-k dielectrics, including HfO_2, ZrO_2, and $HfZrO_2$ on Ga-polar GaN HEMTs [40–52]. Saadat et al. [42] compared Al_2O_3, HfO_2, and a stack of Ga_2O_3+HfO_2 as gate dielectrics. Their studies revealed that while HEMTs with Al_2O_3 gate dielectric show the best trans-conductance and dispersion performance, the Ga_2O_3 + HfO_2 combination has the best maximum drain current density, low interface traps, and negligible hysteresis along with trans-conductance that is comparable to that of standard Ni/Au/Ni Schottky-gated HEMTs because of the high capacitance of the high-k dielectric. Moreover, using Ga_2O_3 + HfO_2 as the gate dielectric reduced the gate leakage by more than five orders of magnitudes compared with the HEMT without any gate dielectric. Chen et al [53] investigated ZrO_2 as gate dielectric in Ga-polar GaN HEMTs and compared dc and RF characteristics of these HEMTs with those with Schottky contact gate. They showed that the MOS-HEMTs with ZrO_2 gate insulator layer significantly reduced the gate leakage current and microwave performance of the devices. The device linearity was also improved due to its flat and wide trans-conductance (g_m) distribution. Stoklas et al [54] studied the impact of atomic layer deposition (ALD) deposition technique using photo-assisted capacitance transients (photo-C-t) method and reduced the D_{it} value from 1×10^{13} cm^{-2} eV^{-1} to 2-3×10^{12} cm^{-2} eV^{-1} by replacement of thermal-ALD with ozone-ALD. Jung et al [55] demonstrated a surface state density (measured using conventional Terman method) of 6.77×10^{11} cm^{-2} eV^{-1} at Ec-0.3 eV by in situ NH_3 ALD plasma passivation. Chang et al [56] reported D_{it} of 5-10×10^{11} cm^{-2} eV^{-1} at mid bandgap at the interface between thermal ALD deposited HfO_2/Al_2O_3 bilayer dielectric and GaN using conventional Terman method which is not accurate for wide bandgap semiconductors.

All the aforementioned studies have focused on depositing the HfO_2 dielectric on Ga-polar GaN. However, the polarity of GaN (Ga-polar vs N-polar) plays an important role in deciding the dielectric-semiconductor interface quality. It has been observed that N-polar GaN surface is more

reactive as compared to Ga-polar resulting in higher incorporation of impurities and higher surface states [57]. A recent study has also showed the GaN polarity impacts the interface sharpness between oxide and GaN, thus resulting in different capacitance-voltage (CV) characteristics [58]. Yang et al [59] have studied the effects of surface pretreatment, dielectric growth, and post deposition annealing on interface electronic structure and polarization charge compensation of Ga- and N-face bulk GaN. Meyer et al [60] is the only report on HfO_2 on N-polar AlGaN-GaN HEMTs, in which they showed that HfO_2-insulated gate devices improved the reverse-bias gate leakage current as compared to reference Schottky devices, however failed to pinch-off the device even with 1.5 μm gate length.

2.1.2 Characterization Methods of Interface States

Terman Method

The Terman method compares the ideal capacitance-voltage (C-V) and the low-frequency C-V curves to calculate the interface states density from the deviation of two curves. This method is valid based on the assumption that (i) the semiconductor and dielectric material are both ideal, thus their C-V response can be predicted mathematically; (ii) the low-frequency C-V curve can entirely reflect the information on interface state density. No traps are present in dielectric bulk or near interface. The Terman method has been utilized to characterize the interface state density in silicon based devices for decades. Silicon has relatively small bandgap and relatively large minority carrier concentration which allows both the shallow and deep interface state to be ionized in manageable time scales.

Given the non-ideality of the semiconductor and dielectric materials, the deviations of their material properties from the theoretical values are not avoidable. Thus, the high-low frequency measurement is employed to replace the numerical calculated C-V curve in the Terman method.

However, in the WBG material systems with negligible hole concentration and generation rates, the trap emission time is very long at room temperature. Specifically, previous research showed the electron emission time from the state located around E_C-1.5 eV for GaN is estimated to be 10^7-10^8 years at room temperature [61]. The high-low frequency method may still be used in the WBG system to a limited extent, as the minority carrier generation rate can increase at elevated temperatures. However, in order to create a comparable quantity of holes, the required high temperature would damage the device being tested.

AC Conductance method

This method measures the conductance change due to the charging and discharging of traps responding to the Fermi level moving above to below the energy of the trap. This method is very useful when the emission time of the trap is on the order of 10 ms (100 Hz) or shorter. When the time constant of the trap is smaller than that, only shallow traps can respond and the conductance signal becomes noisy. Similar to the Terman method, the temperature is often increased to allow for the measurement of deep traps near mid-bandgap for the WBG material systems with the trap emission time on the order of years.

Deep Level Transient Spectroscopy (DLTS)

The deep level transient spectroscopy is a very sensitive and accurate technique which measures the change in capacitance due to changes in traps occupancy. The device under test (DUT) is initially placed under reverse-bias (trap emptying pulse) to empty all the traps. Followed by a forward biased pulse (trap filling pulse) which results in traps capturing the carriers and getting filled. The DUT is then again placed under reverse bias (trap emptying pulse) by lowering the voltage to the initial voltage level. However, traps cannot respond to the change immediately due to its slow nature, rather emit electrons slowly over time. This results in a capacitance transient

over time which can be accurately measured. By repeating this reverse-forward-reverse pulse sequence over a temperature range for different rate windows, different trap characteristics such as capture cross-section, activation energy level, and density can be extracted using Aarhenius plot. DLTS measurement is spectroscopic in nature such that it can resolve and identify traps present at different energy locations since traps at different energy location emit carriers at different rates. It can also resolve between donor and acceptor traps. Traditional DLTS is typically capacitance based on depletion region (e.g. p-n junction or Schottky diode). However, other electrical parameters such as current (I-DLTS) or voltage (CCDLTS, DDLTS) can be used to monitor the transient response resulting from change in trap occupancy. Another advantage of DLTS over AC Conductance is, while AC Conductance uses an AC frequency at a specific DC bias, DLTS generally pulses from a bias that is significantly higher than the trap energy level to a bias that is significantly lower than the trap energy. However, major disadvantage of DLTS is that it takes a long time to sweep over a large range of temperature especially for wide-bandgap devices. However UV illumination can be used to excite traps in combination with traditional DLTS method which is known as deep level optical spectroscopy (DLOS).

Deep UV-assisted Capacitance-Voltage Method

Recently, the deep ultraviolet photo-assisted capacitance-voltage (DUV-assisted C-V) was developed as an alternative technique to extract D_{it} for wide-bandgap semiconductors [62–65]. This method is utilized in this chapter and will be elaborated in details. Similar to the Terman method, this method tracks the change in the occupancy of the traps, enabled by the capture of electrons first from the conduction band by empty interfacial states and eventually by generated holes that accumulated at the semiconductor/dielectric interface. This technique relies on deep ultraviolet (DUV) illumination applied to devices biased in depletion to ensure all traps can be

extracted from the C-V measurements. The energy of the deep UV light should be the same or large than that of the characterized semiconductor materials. The detailed procedure of this measurement will be elaborated in this chapter.

2.1.3 Chapter Overview

In the first part of this chapter, we investigated HfO_2 on N-polar HEMT structure by performing frequency dependent capacitance-voltage measurements on metal-oxide-semiconductor capacitors (MOSCAPs). The impact of annealing on the quality of HfO_2 was studied. Moreover, we compared the CV characteristics of MOSCAPs with HfO_2 deposited on GaN channel with that deposited on the AlGaN cap layer.

In the second part of this chapter, the impact of various surface preparations, in-situ ALD plasma pre-treatments, deposition and annealing conditions on the D_{it} of HfO_2 on N-polar GaN were investigated. Interface trap density (D_{it}), border trap density, breakdown voltage (BV) and dielectric constant were measured and optimized for HfO_2/N-polar GaN MOSCAPs.

2.2 As-deposited HfO_2 on GaN HEMT Epi-structure

2.2.1 Device Fabrication

The N-polar HEMT structure used for this study is shown in **Fig. 2.1** and was epitaxially grown by metal-organic chemical vapor deposition (MOCVD) on a miscut sapphire substrate. A graded Si-doped AlGaN backbarrier is typically used in these heterostructures to suppress current dispersion caused by hole traps at the interface with net negative polarization charge [66,67]. The details of growth are discussed elsewhere [68–70]. The 2nm-thick $Al_{0.08}GaN$ layer on top is to reduce the gate current leakage. MOCVD grown N-polar HEMT structures are typically capped in-situ with 5 nm-thick SiN_x dielectric. The SiN_x cap protects N-polar surface from being

roughened by the developer during the device fabrication [71,72]. It can also function as gate dielectric [32,72,73].

For this purpose, the ohmic contacts were created by E-beam evaporation using a metal

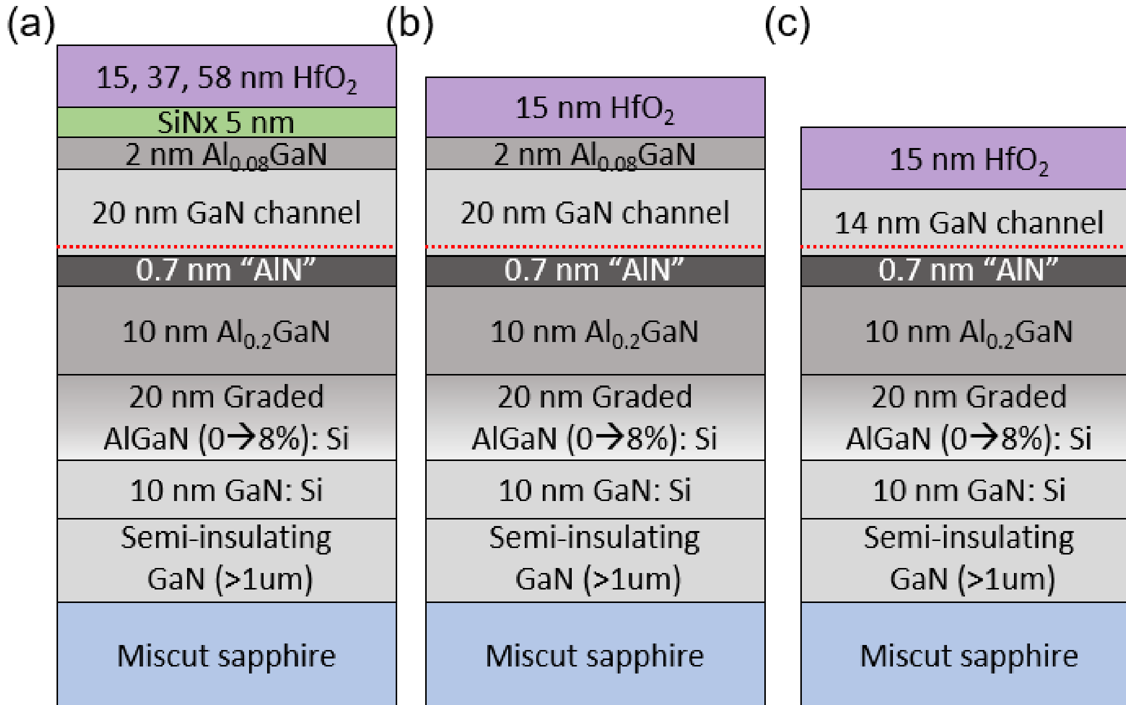


Figure 2.1 Schematic of the structures studied in this work (a) HfO_2 on SiN (b) HfO_2 on AlGaN after removal of SiN and (c) HfO_2 on GaN after removal of SiN and AlGaN cap layer.

stack of Ti/ Al/ Ni/ Au (20/100/10/100 nm), which was then annealed at 820° C for 30 seconds in a N_2 gas atmosphere. HfO_2 was then blanket-deposited over the whole wafer, using plasma enhanced atomic layer deposition (ALD) with the chamber conditioned to 250℃ in Argon ambient. The dielectric thickness was verified using ellipsometry on Si pieces co-loaded as control samples. Sample-A was not annealed after HfO_2 deposition, while sample-B and sample-C were annealed at 400℃ in a N_2 gas atmosphere for 1 min and 5 min, respectively. This was followed by gate metal deposition (30 nm Ti/ 600 nm Au) via E-beam evaporation. Capacitor sizes on each sample ranged in diameter from 50 μm to 800 μm.

To investigate the impact of annealing on HfO_2 quality, we first fabricated a set of MOSCAPs with 15 nm-thick HfO_2 deposited directly on MOCVD-SiN_x as shown in **Fig. 2.1(a)**.

2.2.2 Results and Discussion:

Figure 2.2(a) demonstrates the representative CV profiles measured at different frequencies on Sample-A. CV profiles measured at frequencies below 800 kHz are drastically different from an ideal CV profile expected on a hetero-structure having a two-dimensional electron gas (2DEG). They do not show a saturated capacitance. Attempts to measure these devices at positive voltage were unsuccessful due to high ac current leakage. The 2DEG density extracted from these CV profiles is ~3×10^{12} cm^{-2} which is much lower than that extracted from Hall measurement (~1.1×10^{13} cm^{-2}) on this hetero-structure. This indicates existence of slow trap states in HfO_2, which can only respond at

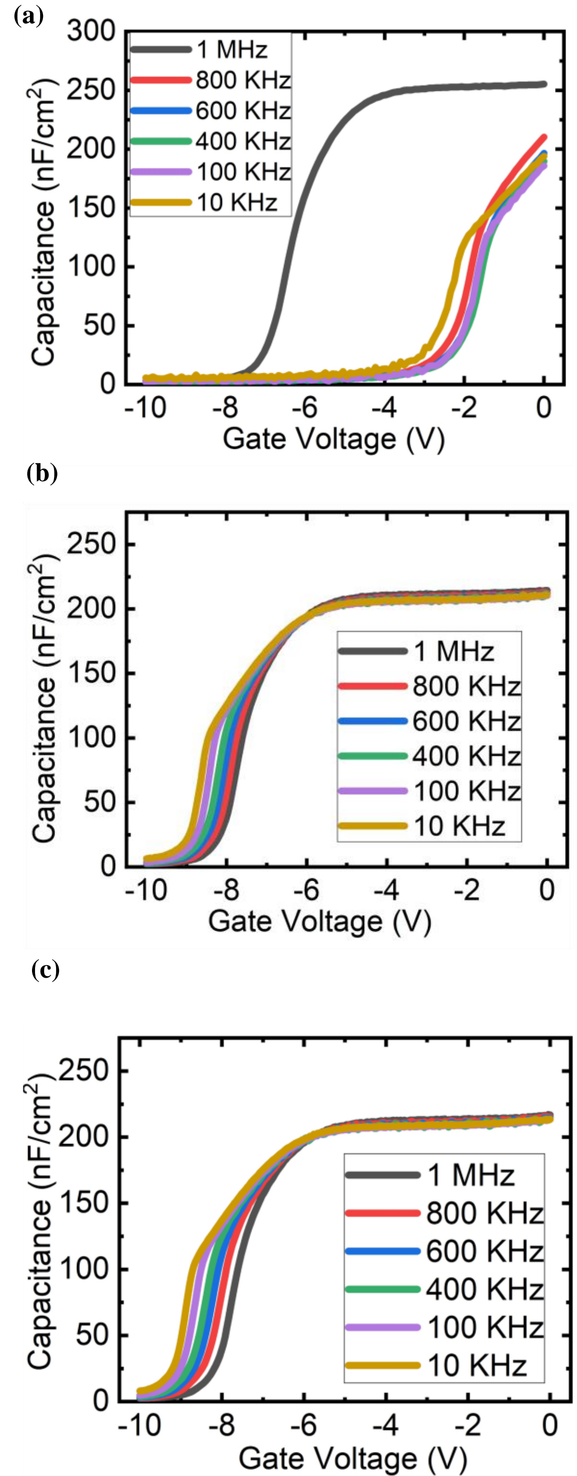


Figure 2.2 CV profile measured at different frequencies on MOSCAP-C with 15nm-thick HfO_2 which (a) was not annealed and annealed for (b) 1min and (c) 5 min at 400℃ in N_2.

frequencies below 800 kHz. The positive shift in threshold voltage compared to the expected value of ~8V also points to negative charges in dielectric. At 1 MHz, these traps can no longer respond and therefore the CV profile looks closer to an ideal one. By annealing HfO_2 at 400℃ in N_2 ambient before gate metal deposition, the CV profile measured at 1 MHz remained unchanged, whereas the other CV profiles measured at lower frequencies become closer to an ideal curve (**Fig. 2.2 (b) and (c)**). As the measurement frequencies reduces, the pinch-off voltage of these MOSCAPs move toward more negative values. Annealing for 5 min did not change the MOSCAP characteristics significantly, and therefore, we annealed HfO_2 for 1 min for all other devices discussed in this work.

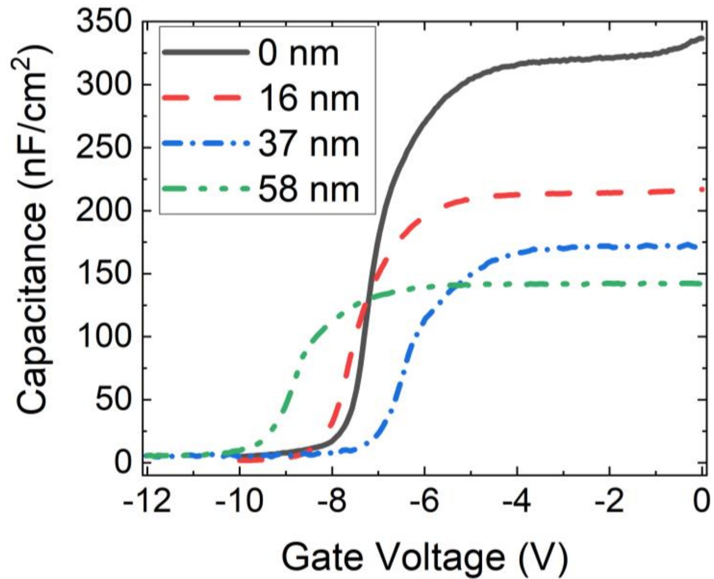


Figure 2.3 CV profiles measured at 1 MHz on MOSCAPs with various HfO_2 thicknesses.

To determine HfO_2 dielectric constant, a set of MOSCAPs were then fabricated varying HfO_2 thickness from 0 nm to ~57 nm. **Figure 2.3** shows CV profiles measured at 1MHz on these MOSCAPs. **Figure 2.4** depicts 1/C as a function of HfO_2 thickness, in which C is the capacitance density at 0V measured at 1MHz on these MOSCAPs. A dielectric constant value of 17 was extracted for HfO_2 via linear fit to this plot which is close to the dielectric constants reported in the literature for HfO_2 [74,75]. Using a linear fit to 1/C on MOSCAPs with different HfO_2 thicknesses, which are otherwise fabricated identically, allows us to identify dielectric constant accurately

without making assumptions for dielectric constants of other underlying layers including GaN, AlGaN, SiN_x, and the non-idealities at their interfaces.

The 2DEG density was also extracted on these MOSCAPs by integrating the CV profile and is plotted as a function of HFO_2 thickness. As depicted in **Fig. 2.4**, the 2DEG density decreases as the HfO_2 thickness increases. This behavior can be explained by assuming fixed negative charges uniformly distributed in the HfO_2. As HfO_2 thickness increases, the total negative charge in HfO_2 increases which results in 2DEG depletion. The ΔV_{th} due to the fixed negative charge in dielectric and reduction in 2DEG density is a positive value. On the other hand, increasing HfO_2 thickness leads to reduction of the capacitance density, and consequently, $\Delta V_{th} < 0$. Due to these opposite effects, the variation of threshold voltage as a function of HfO_2 thickness is not monotonic.

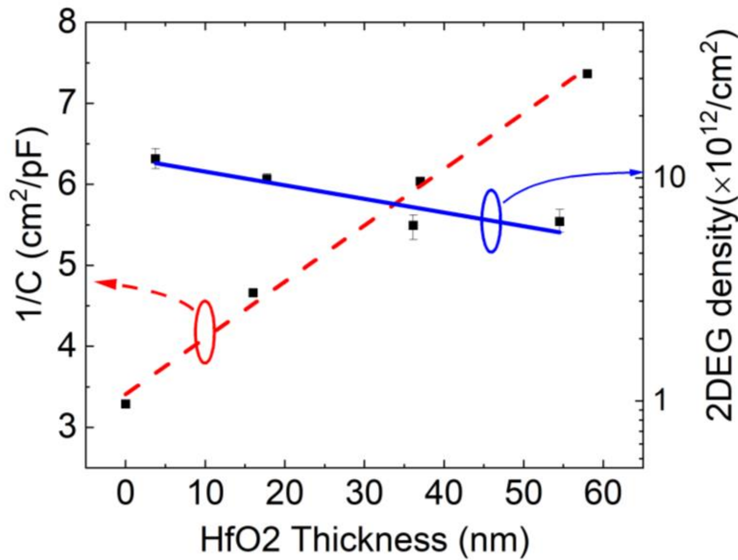


Figure 2.4 Capacitance measured at 0 V versus HfO_2 thickness.

For ultra-scaled HEMTs, it is desirable to reduce the distance from gate to the channel as much as possible to eliminate short channel effects [22,76]. For this purpose, it is advantageous to deposit HfO_2 directly on the HEMT structure and remove any dielectric with lower dielectric

constant. Therefore, in the next step, we studied the impact of HfO_2 deposited directly on the AlGaN cap (MOCVD-SiN_x was removed) and GaN channel (MOCVD-SiN_x and AlGaN cap were removed). For this purpose, MOCVD-SiN_x was etched by diluted hydrofluoric acid (1:1 HF:DI) after formation of Ohmic contact, followed by HfO_2 deposition on AlGaN cap (**Fig. 2.1(b)**). The sample was then annealed at 400℃, followed by gate metal deposition as discussed earlier. To fabricate MOSCAPs with HfO_2 deposited directly on the GaN channel (**Fig. 2.1(c)**), SiN was first removed using diluted hydrofluoric acid (1:1 HF:DI). We then removed the AlGaN cap and part of GaN channel using a low-etch-rate (~0.5 nm/min) chlorine-based inductively coupled plasma etching, resulting in a 14 nm-thick GaN channel. After dry etch, the surface was exposed to UV-Ozone for an hour and then etched in HF for 30 sec to help remove surface damage caused by dry etching.

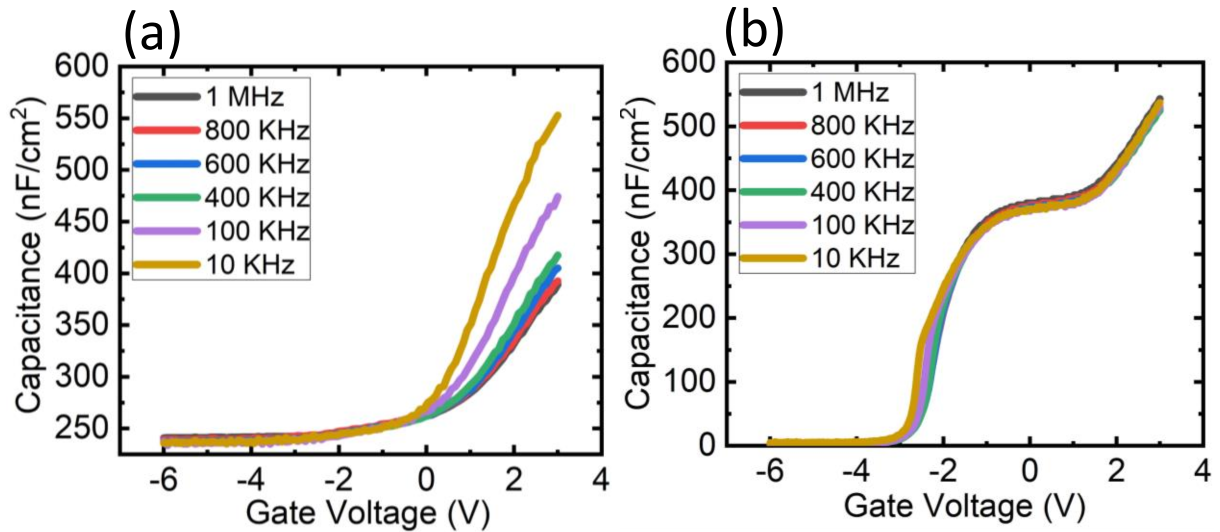


Figure 2.5 CV profile measured at different frequencies on (a) MOSCAP-B and (b) MOSCAP-C.

As depicted in **Fig. 2.5 (a)**, it was not possible to pinch-off MOSCAPs with HfO_2 deposited on AlGaN cap and applying voltages beyond -6V led to very high leakage which made capacitance measurements beyond this voltage impossible. This could be due to reaction of oxide in HfO_2 with Al in AlGaN cap and formation of a poor-quality Al_2O_3 interface during the annealing at 400℃.

This poor-quality interlayer is full of traps which leads to the pinning of the fermi level. Therefore, by applying gate voltage, the fermi level in the channel does not move. On the contrary, when AlGaN cap layer was removed by low etch rate/low damage dry etching technique and HfO_2 was deposited directly on GaN, normal CV profiles were measured. These MOSCAPs showed much lower pinch-off voltage which is due to a combination of higher gate capacitance, because of lower distance between gate and the channel, and a thinner GaN channel which leads to lower 2DEG density in the channel. A charge density of 4.9×10^{12} cm^{-2} was calculated on these MOSCAPs.

2.3 HfO_2 Characterization on GaN MOSCAPs

2.3.1 Device Fabrication

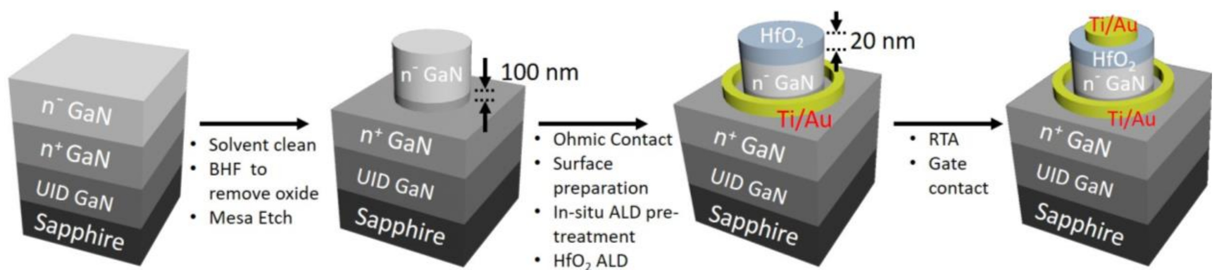


Figure 2.6 Fabrication process flow of HfO_2/N-polar GaN MIS structure.

Metal-insulator-semiconductor (MIS) capacitors were fabricated to characterize the interface states between HfO_2 and N-polar GaN. The fabrication process is shown in **Fig. 2.6**. The N-polar epitaxial layers were grown by metal organic chemical vapor deposition (MOCVD on 4° miscut c-plane sapphire substrates). From bottom to top, the epitaxial layers included 660 nm unintentionally doped GaN, 660 nm n+ GaN:Si with a doping concentration of 3.5×10^{18} cm^{-3} and 530 nm n-GaN with a doping concentration of 2×10^{17} cm^{-3}. Chlorine-based mesa etch was performed till n+ GaN layer was exposed, followed by evaporation of ohmic metal stack Ti/Au (30/200 nm). Several samples were fabricated with various surface pretreatments using wet

chemical etching combinations and UV-ozone prior to ALD deposition. The samples were loaded immediately into ALD chamber to minimize any native oxide formation and surface contamination. Various in-situ plasma treatments in the ALD chamber were implemented prior to deposition of 20 nm-thick HfO_2. The HfO_2 was deposited via thermal- or plasma- ALD in a Veeco Fiji ALD reactor and the thickness was measured using ellipsometer on a co-loaded Si sample. After dielectric deposition, rapid thermal annealing (RTA) at 400°C was performed for 1 min on all the samples, followed by deposition of a gate metal stack (Ti/Au :20/200 nm). **Table 2.1** summarizes the techniques that were employed for surface preparation, in-situ pretreatment, ALD deposition, and post-deposition annealing.

2.3.2 Results and Discussion

UV-assisted CV measurement was employed to calculate the interface state density following the methodology developed by Swenson et al [62]. CV measurements were taken at room temperature using a Keysight B1500 semiconductor parameter analyzer. The frequency and amplitude of AC signals were 1 MHz and 30 mV, respectively. The DC voltage sweep was set with a step voltage of 30 mV and a sweep rate of 0.6 V/s. A 365 nm lamp with an optical power

Table 2.1. Summary of the techniques that were employed for surface preparation, in-situ pretreatment, ALD deposition, and post-deposition annealing.

Sample #		1	2	3	4	5	6	7
Surface preparation	BHF (1:50)	✓	✓					
	Piranha (1:5) + BHF (1:50)			✓	✓	✓	✓	
	Piranha (1:5)+ BHF (1:50) + UV/ozone							✓
ALD Pre-treatment	No pre-treatment	✓						
	TMA/N_2 plasma		✓	✓	✓	✓	✓	✓
ALD	HfO_2 Plasma	✓	✓	✓	✓	✓		
	HfO_2 thermal						✓	✓
Annealing	N_2	✓	✓	✓				
	N_2, then O_2				✓			
	O_2					✓	✓	✓

density of 0.13 W/cm^2 was used as the UV illumination source for sufficient hole generation. The dielectric constant was determined from the accumulation capacitance obtained from the dark CV curve during the UV assisted C-V measurement as mentioned by Swanson et al [62] and Liu et al [77]. The dark curve represents the ideal state of MOSCAP where all the interface traps are neutral (filled donor states). The average forward breakdown field (E_{BD}) (MV/cm) was also calculated by simply dividing breakdown voltage (BV) with dielectric thickness (t_{HfO_2}) using the following relation:

$$E_{BD} = BV/t_{HfO_2} \quad (1)$$

In the accumulation region, there is negligible voltage drop across the accumulation layer and almost all the voltage appears across the dielectric thickness. However, it is note-worthy that Electric field would be much higher at gate metal edges where breakdown first occurred compared with the center of gate metal as demonstrated by Roy et al [78] using silvaco TCAD simulation. However, this fact applies to all the samples and so the improvement in the breakdown field can be attributed to the improvement in the dielectric quality.

To gauge the improvements by various methods implemented, a baseline sample (Sample 1) that did not have any in-situ surface treatment was fabricated and characterized. The average density of states over the 0.15-2eV energy range were measured to be 7.24×10^{12} cm^{-2} eV^{-1} which was very high and undesirable for device applications. The effect of self-cleaning using in-situ tri-methyl-aluminum (TMA)/N_2 plasma (Sample 2) prior to HfO_2 deposition was first studied and compared

Table 2.2 Effect of in-situ TMA/N_2 plasma on various bulk and interface characteristics.

Sample	1	2
Cleaning	BHF (1:50)	
Pre-treatment	No pre-treatment	TMA/N2 plasma
Dielectric constant	15.3	16.3
BV field (MV/cm)	2.83	2.72
Integrated D_t ($x10^{12}$ cm^{-2})	14.7	11.9
Average D_t ($x10^{12}$ eV^{-1} cm^{-2})	7.24	6.33

with the baseline sample 1. This method has been reported to suppress frequency dispersion and passivate the Al_2O_3/GaN, HfO_2-InGaAs interfaces[79][80][81]. Both samples 1 and 2 were cleaned with (1:50) diluted BHF for 90 seconds before transferring into the ALD chamber. For sample 2, a five-cycle alternating N_2/TMA pulse was applied in-situ on the surface prior to HfO_2 deposition. Each cycle consisted of a N_2 plasma pulse (20 mTorr, plasma power of 100W for 2s), followed by a short TMA pulse (40 ms), and another N_2 plasma pulse (2s) followed by Ar purge (2s) and N_2 stabilization (10s) in sequence. After deposition, the samples were both annealed in N_2 atmosphere [82]. The incorporation of N_2/TMA as a surface pretreatment for sample 2 increased the dielectric constant marginally from 15.3 to 16.3 and reduced the average interface states marginally from 7.24×10^{12} cm^{-2} eV^{-1} to 6.33×10^{12} cm^{-2} eV^{-1} as shown in **Table 2.2**. This could be explained by possible removal of hydrocarbons and hydroxylates resulting in a cleaner surface.

The effect of rapid thermal annealing (RTA) conditions was then studied. Sample 3 was annealed in N_2 ambience, whereas sample 4 was annealed in N_2 followed by O_2 and sample 5 in pure O_2 ambience. All three samples were cleaned with 1:5 diluted piranha (adding 10ml of 30% hydrogen peroxide solution to 50ml of concentrated sulfuric acid) for 5 min and 1:50 diluted BHF (adding 10ml of concentrated BHF solution to 500ml of DI water) for 90 sec followed by in-situ TMA/N_2 plasma prior to plasma HfO_2 deposition at 250 °C. Annealing in N_2/O_2 (sample 4) and O_2 (sample 5) resulted in a smaller D_{it} and higher dielectric constant and breakdown field

Table 2.3. Effect of Rapid thermal annealing ambience on bulk and interface characteristics.

Sample	3	4	5
Annealing	N_2	N_2, then O_2	O_2
Dielectric constant	13.8	13.9	14.5
BV field (MV/cm)	2.33	2.79	2.75
Integrated D_t ($\times10^{12}$ cm^{-2})	8.45	3.3	3.53
Average D_t ($\times10^{12}$ eV^{-1} cm^{-2})	7.56	4.5	5.76

compared with annealing in N_2 only (Sample 3) as shown in **Fig. 2.7 and Table 2.3**. The improvement in bulk properties of dielectric could be attributed to the reduction of oxygen vacancies as previously reported in oxide based dielectrics such as HfO_2 and Al_2O_3 [83][84][85][86][87].

Yeluri et al [63] reported a ledge in post-UV CV curve and a peak in D_{it} curve which has been attributed to accumulation of holes at Al_2O_3-GaN valence band interface due to positive valence band offset (VBO). Similar results have also been reported in other dielectrics and semiconductor material system with positive VBO [64][87]. Though HfO_2 has similar positive band offset, such ledges were observed clearly in the samples that were not annealed in O_2 (1, 2, 3). However, the ledges were reduced significantly in oxygen annealed samples (Sample 4, 5, 6 and 7) as shown in **Fig. 2.8**. Although only density of states profiles for samples 6 and 7 are shown in **Fig. 2.8**, similar behavior was also observed on samples 4 and 5. Previous studies showed that the reduced oxygen content or increased oxygen vacancies at interface leads to downward

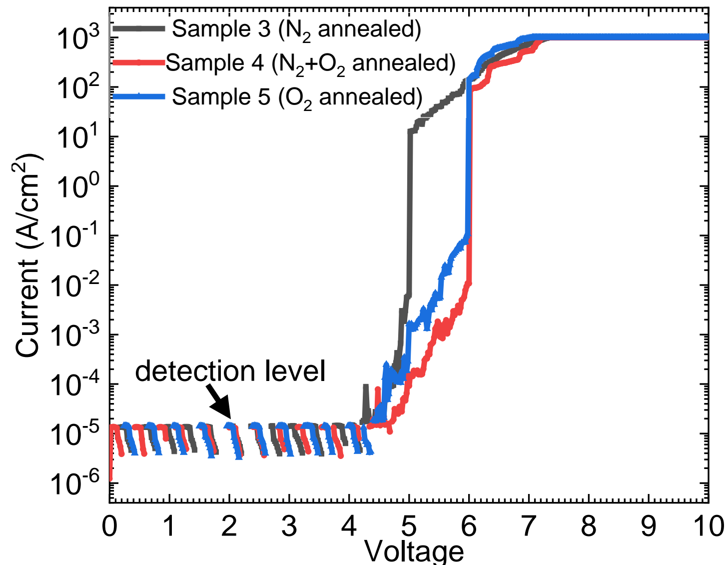


Figure 2.7 Forward bias Current-Voltage (CV) characteristics of N_2 annealed (Sample 3), N_2+O_2 annealed (Sample 4) and O_2 annealed (Sample 5).

movement of valence band of ALD-HfO_2 with respect to GaN [88]. On the other hand, increasing oxygen content or reducing O-vacancies moves the valence band upwards reducing the VBO. A higher oxygen-content can reduce VBO as small as 0.51 eV which presents little barrier for hole confinement [88] and hence elimination of the ledge. This small VBO can further be helpful in improving reverse breakdown voltage by preventing an increase in the electric field in the dielectric due to hole accumulation [89]. Additionally, it has been observed that UV-ozone surface treatment can be utilized for Al_2O_3/GaN band alignment engineering [90]. There is also a small peak in D_{it} profile (**Fig. 2.8**) near E-Ec = 0.3eV which has also been observed by Zhang et al [88] and was attributed to oxygen vacancies.

The effect of ALD deposition technique was also studied through comparing the properties of HfO_2 deposited using thermal-ALD (sample 6) and using plasma-ALD (sample 5). Both two samples were cleaned using (1:5) diluted piranha for 5 min and (1:50) diluted BHF for 90 sec followed by TMA/N_2 plasma pre-treatment prior to ALD. The samples were then annealed in oxygen at 400°C for 1 min. The deposition of HfO_2 using thermal ALD improved the breakdown

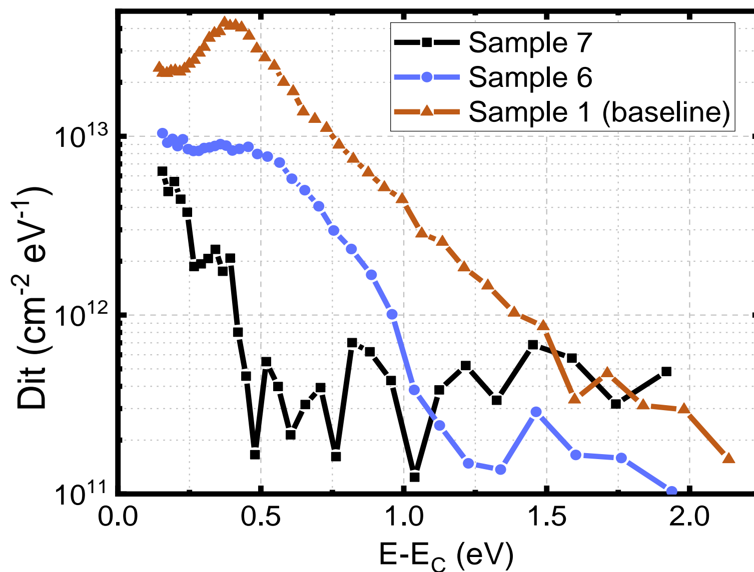


Figure 2.8 Density of states (D_{it}) profile as the function of energy for Sample 1 (baseline), 6 and 7 (UV + Ozone).

Table 2.4 Effect of various surface cleaning methods on bulk and interface characteristics.

Sample	6	7
Cleaning	Piranha (1:5)+ BHF (1:50)	Piranha (1:5) + BHF (1:50) + UV-Ozone
Dielectric constant	15.1	15.9
BV field (MV/cm)	3.11	3.14
Integrated D_t ($x10^{12}$ cm^{-2})	4.89	1.46
Average D_t ($x10^{12}$ $eV^{-1}cm^{-2}$)	5.86	1.64

field from 2.75 MV/cm to 3.11 MV/cm and increased the dielectric constant from 14.5 to 15.1 (**Table 2.2** and **2.4**). The interface state density for the thermal-ALD sample was 5.86×10^{12} cm^{-2} eV^{-1}, which is similar to the plasma-ALD sample (5.76×10^{12} cm^{-2} eV^{-1}). The improvements in both dielectric and breakdown field values are possibly due to the absence of plasma damage for thermal-ALD. For the same reason, it was expected that the D_{it} of thermal ALD would be lower as compared to plasma, however it remained unchanged which needs further study. A possibility could be the residues of H_2O resulting in chemical vapor deposition (CVD) type of growth during initial cycles.

Finally, we studied the effect of UV-Ozone clean on interface states (D_t). The characterization results of UV-assisted C-V measurements of these samples are summarized in **Table 2.4**. The density of interface states profiles measured on these samples and the baseline sample (sample 1) are demonstrated in **Fig. 2.8**. Both samples were treated with (1:5) diluted Piranha etch and then treated with (1:50) diluted BHF solution. Sample 7 was treated additionally with UV-ozone ex-situ for 15 min. Then the samples were loaded into ALD chamber immediately and an in-situ N_2/TMA plasma passivation was performed followed by thermal-ALD deposition of HfO_2 at 250 °C. UV-ozone treatment (sample 7) significantly reduced the average surface states

from 5.86×10^{12} cm^{-2} eV^{-1} to 1.64×10^{12} cm^{-2} eV^{-1}. The lowest average surface states of 1.64×10^{12} cm^{-2} eV^{-1} was measured on Sample 7 as shown in **Fig. 2.8**, which is four times less than the baseline sample 1 and the integrated D_{it} value was reduced by one order of magnitude. The near band-edge interface states are close to 6×10^{12} cm^{-2} eV^{-1} and drops to $4\text{-}5\times10^{11}$ cm^{-2} eV^{-1} rapidly and remains constant throughout. This is the lowest surface states achieved in this study with a breakdown field of 3.1 MV/cm. The lower D_{it} value reported in this paper using UV-Ozone cleaning could be due to the formation of a thin layer of Ga_2O_3 [90,91] which facilitates the subsequent HfO_2 deposition which has also been reported in literature. Tingting et al [91] attributed the improvements in ohmic and Schottky contact to formation of an interfacial gallium oxide layer formed by UV-ozone treatment. Kim et al [90] showed that UV-ozone treatment increased the Ga-O content of surface and the Ga-O/Ga-N ratio increased with longer UV-ozone treatment which resulted in a more uniform Al_2O_3 dielectric deposition and improved the band alignment. First principle calculations performed by Zhang et al. [88] showed that oxygen vacancies increase the density of interface states which can lead to fermi-level pinning. Moreover, different oxygen vacancy level relates to different valence band offset and conduction band offset. UV-ozone treatment reduces oxygen vacancies by forming Ga-O bond (interfacial passivation layer) and alters the interface oxygen

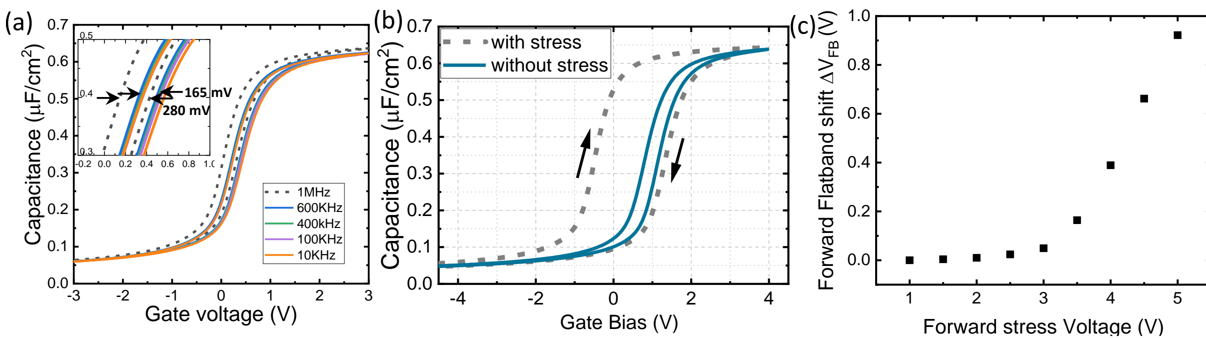


Figure 2.9 (a) C-V hysteresis (b) HF C-V for fast and slow trap estimation (c) Forward flatband voltage shift for Sample-7.

content which can change the band offset [88]. This has been observed in our oxygen annealed samples as shown in **Fig. 2.8** as described previously.

The dielectric interface on sample 7 was further characterized via frequency-dependent CV measurements (**Fig. 2.9(a)**). The frequency dispersion remained negligible and CV hysteresis remained almost constant and extremely low (165 mV) at different frequencies which is also indicative of superior dielectric quality and interface. The very first measurement at 1MHz showed higher hysteresis value (280mV) which is specific to the first measurement and irrespective of the value of frequency. The hysteresis values reduced to ~165 mV for subsequent measurements and were repetitive across devices. This is due to the trapping of electrons by slow traps present at interface which shifts C-V curve towards right reducing hysteresis. However, the slow traps cannot release the electrons immediately for subsequent frequency measurements resulting in smaller hysteresis. The slow and fast near-interface traps, measured at 1MHz using the methodology in ref. [77], on Sample-7 were 1.39×10^{12} cm^{-2} and 5.78×10^{12} cm^{-2} eV^{-1}, respectively as shown in **Fig. 2.9(b)**. The forward bias dependent flatband voltage shift was also measured at 1MHz using the methodology described in ref. [92] to test the reliability of the dielectric. The gate voltage at weak accumulation voltage (V_G = 1V, field = 0.045MV/cm) was assumed to be the baseline as shown in **Fig 2.9(c)**. The flatband voltage was almost constant initially and increased rapidly as the gate voltage increased beyond 3V (1.4 MV/cm) due to charge injection into the dielectric.

2.4 Conclusion

In summary, we first studied ALD-HfO_2 as dielectric on N-polar HEMT epi-structures by fabrication and characterization of HEMT-MOSCAPs. A significant difference was observed between the CV profile measured at 1 MHz and CV profiles measured at lower frequencies, when post-deposition annealing was not performed. A post-annealing at 400 °C in N_2 seemed effective

to reduce frequency dispersion and obtain well-behaved CV profiles. A dielectric constant value of 17 was extracted for HfO_2 via a linear fit to 1/C on MOSCAPs with different HfO_2 thicknesses. HfO_2 deposition on AlGaN cap led to pinning of the fermi level, perhaps due to chemical reaction between oxygen in HfO_2 and aluminum in AlGaN and formation of a poor-quality Al_2O_3 at the interface. On the other hand, deposition of HfO_2 on SiN or directly on GaN channel resulted in well-behaved CV profiles. However, the UV-CV measurements reveal the presence of high level of interface states between HfO_2 and GaN MOSCAPs. Hence, the impact of various surface cleaning, in-situ ALD pre-treatment, ALD deposition method and post-deposition annealing ambience on interface properties of HfO_2/ N-polar GaN was studied further via UV-assisted CV and current-voltage characterization methods. A combination of the BHF and piranha cleaning with 15 min UV-ozone pretreatment followed by thermal HfO_2 deposition at 250°C improved the interface between HfO_2 and N-polar GaN quality significantly. The lowest average interface trap density was achieved to be 1.64×10^{12} cm^{-2} eV^{-1} with breakdown field of 3.14 MV/cm. Annealing in O_2 improved the breakdown, removed the peak in the D_{it} profile, and reduced the interface states. All the processes (piranha clean, BHF clean, UV ozone pre-treatment, N_2/TMA plasma pre-treatment, annealing in O_2 environment) developed here are compatible with standard N-polar GaN-HEMT processing and can be used for fabrication of N-polar GaN HEMTs which will be discussed in the next chapter.

Chapter 3

N-polar GaN MIS-HEMT with High-k ALD HfO_2 as Gate Dielectric

3.1 Introduction

As mentioned in Chapter-1, to increase frequency of operation higher while maintaining high power, the gate length of the HEMT needs to be further scaled down. However, decreasing gate length alone leads to short-channel effects (SCEs) including increased output resistance, drain induced barrier lowering (DIBL) which leads to threshold voltage variation, and loss of trans-conductance with decreasing gate length [20–22]. The SCEs can be mitigated to a significant extent by keeping aspect ratio constant, i.e. reducing the gate-to-channel distance and gate length simultaneously [22]. However, extreme scaling of gate-to-channel distance will result in higher gate leakage current which requires thick dielectrics and in-turn reduces gate-to-channel distance and gate control. This mandates to transition away from SiN dielectric, which has been primarily

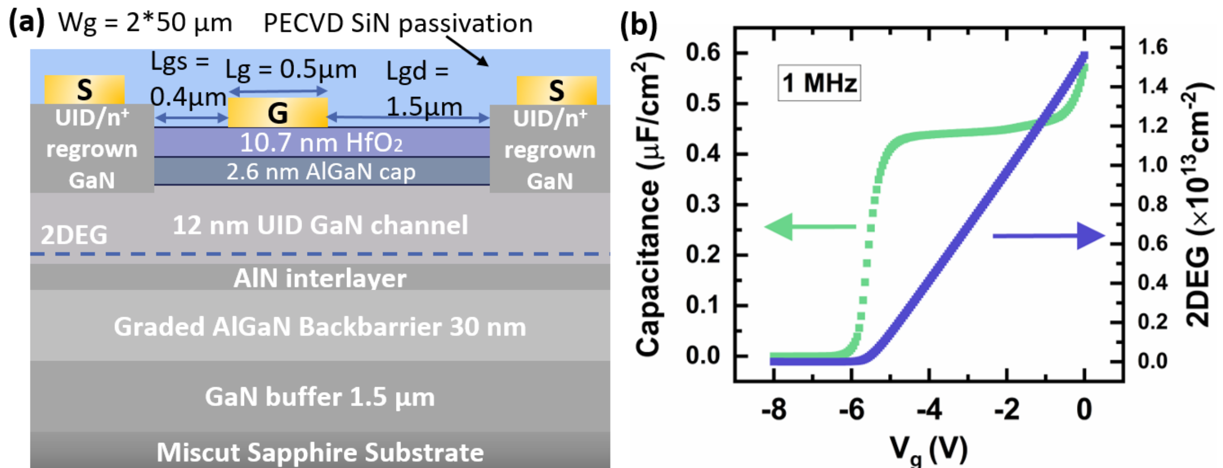


Figure 3.1 (a) Schematic diagram of N-polar MIS-HEMT with 10.7 nm thick HfO_2 as gate dielectric (b) C-V characteristics (green) and 2DEG charge density (green) measured on MOSCAP with 100 µm diameter, the blue curve shows the 2DEG concentration with gate bias voltage.

used in N-polar GaN HEMTs, to high-k dielectric such as HfO_2 or ZrO_2. Small effective oxide thickness (EOT) of these high-k dielectrics can suppress gate leakage while maintaining good gate control. As mentioned in chapter-2, we developed ALD HfO_2 on GaN MISCAP with low interface states and border traps [93]. In this work, we have incorporated the same in our N-polar regrown MIS-HEMT fabrication and have achieved extremely low gate leakage with decent RF performance which shows promise for next-generation high-power high-frequency RF applications.

3.2 Device Fabrication

MOCVD-grown N-polar GaN HEMT epi-structure on miscut sapphire commercially available from Transphorm Inc. used for this study [94,95]. The schematic of the epi-structure and fabricated device dimensions are shown in **Fig. 3.1(a)**. SiO_2 and Al_2O_3 were used as the hard mask and etch stop, respectively, to define the source/drain regrown area and subsequently a UID-GaN/n^{++} GaN (10 nm/60 nm) was regrown by plasma-assisted molecular beam epitaxy (PAMBE) for better ohmic contacts. Device isolation was achieved by ion implantation with Aluminum to form high-resistive region between devices. Then, the sample underwent a sequence of wet

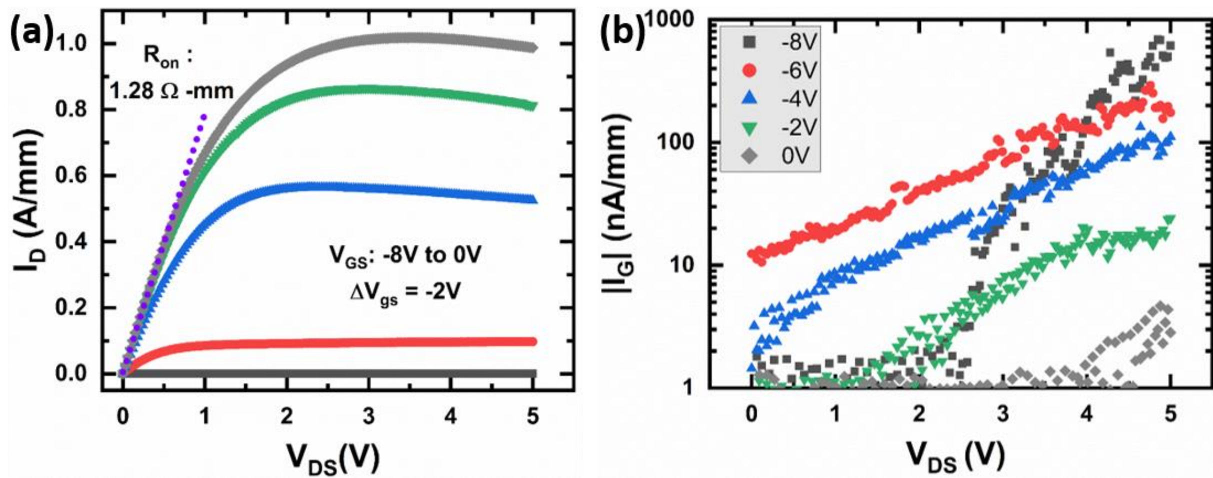


Figure 3.2 (a) Output characteristics and (b) Corresponding gate leakage current for Vgs from -8 V to 0 V with 2 V increments. The extracted Ron is 1.28 Ω-mm at Vgs = 0V.

cleaning, UV-ozone conditioning and in-situ ALD plasma treatment prior to deposition of thermal ALD HfO_2 [93]. HfO_2 was removed under the contact area using a BCl_3-based dry etch and the surface treatment of hydrochloric acid wet etch was performed immediately before 30 nm/200 nm of Ti/Au metal deposition by electron-beam evaporation as source and drain electrodes. A very low Metal-to-GaN contact resistance of 0.1 Ω·mm was measured from un-passivated Transfer Length Measurement (TLM) because of the regrown UID/n^{++} GaN film which has a very low sheet resistance (R_{sh}) of only 69.5 Ω/sq. Finally, 30/420 nm of Ti/Au optical gate and contact pads were patterned via liftoff. The sample was then passivated with 120 nm PECVD SiN followed by bondpad etch to open windows for probing.

3.3 Results and Discussion

A combination of a capacitance-voltage (C-V) measurement (**Fig. 3.1(b)**) and gated TLMs (GTLMs) on passivated structure exhibited a 2DEG density of 1.58×10^{13} cm^{-2} with R_{sh} of 320 Ω/sq, and mobility (μ) of 1416 $cm^2/V \cdot s$ at $V_G = 0$ V. DC measurements were performed on a device with $W_G = 2 \times 50$ μm, $L_G = 500$ nm, $L_{GS} = 400$ nm, $L_{GD} = 1.5$ μm as shown in **Fig. 3.2**. The

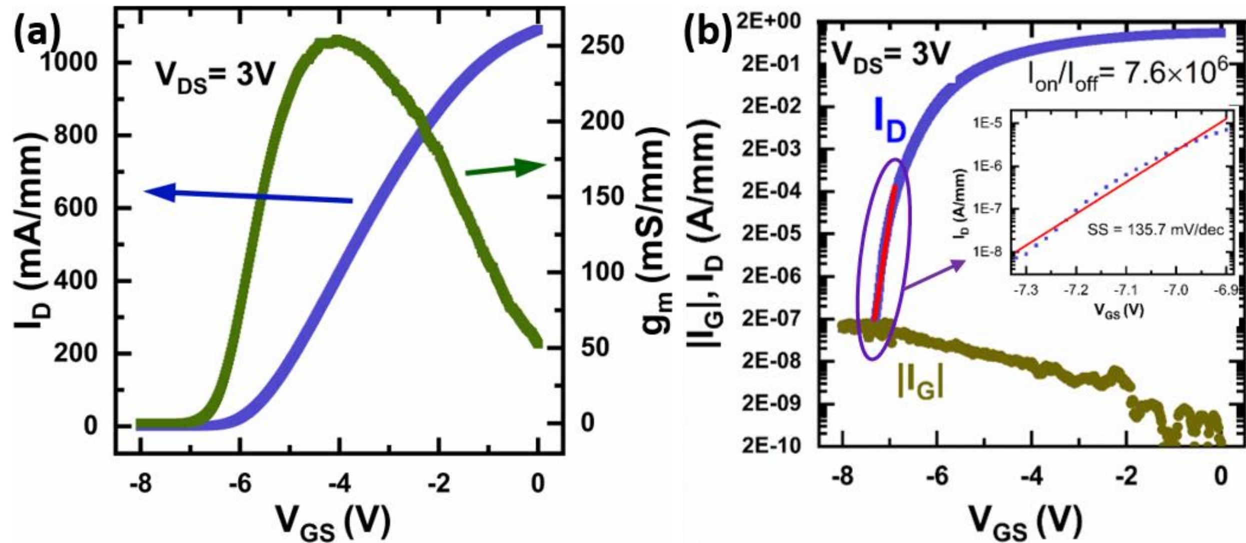


Figure 3.3 (a) Transfer characteristics (blue) and trans-conductance (green) at $V_{DS} = 3$ V (b) drain current and gate leakage in semi-log scale. The subthreshold slope is 135.7 mS/dec.

output characteristics demonstrated a maximum I_{DS} of 1.02 A/mm and an ON-resistance (R_{ON}) of 1.28 Ω·mm at V_{GS} = 0 V with typical self-heating behavior on sapphire substrate [96]. The transfer characteristics showed a peak trans-conductance (g_m) of 254 mS/mm, pinch-off voltage (V_P) of -7.3 V and a subthreshold swing of 135.7 mV/dec at V_{DS} = 3 V as depicted in **Fig. 3.3**. The device revealed an OFF-state current of 1.5×10^{-7} A/mm at V_{DS} = 3V with I_{ON}/I_{OFF} ratio of 7.6×10^{6}. The gate leakage current was measured to be extremely low (~10 nA/mm) and increased to 200 nA/mm with an increase in V_{GD} = -11V as shown in **Fig. 3.3(b)**.

To determine the presence of surface traps, pulsed-IV measurements were conducted on a device with L_{SD} of 600 nm and L_G of 500 nm, and W_G of 2 × 75 µm (**Fig. 3.4**) by using Keysight B1525A

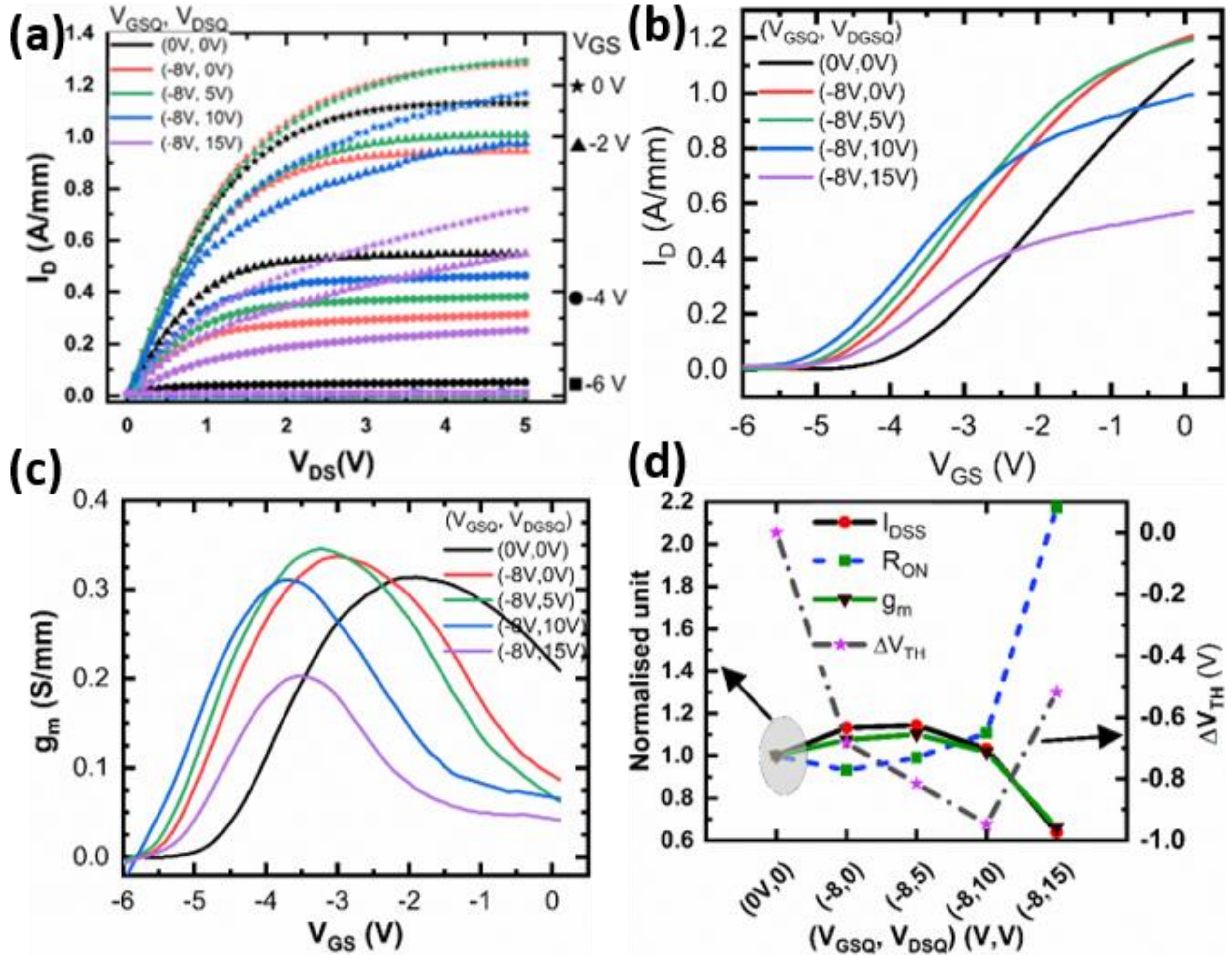


Figure 3.4 Dual Pulsed-IV measurement was measured with pulse width and duty-cycle 10 µs and 0.1% respectively at various gate and drain quiescent voltages. Corresponding (a) I_D-V_D (b) I_D-V_G (c) g_m and (d) normalized I_{DSS}, R_{ON}, g_m, ΔV_{TH}.

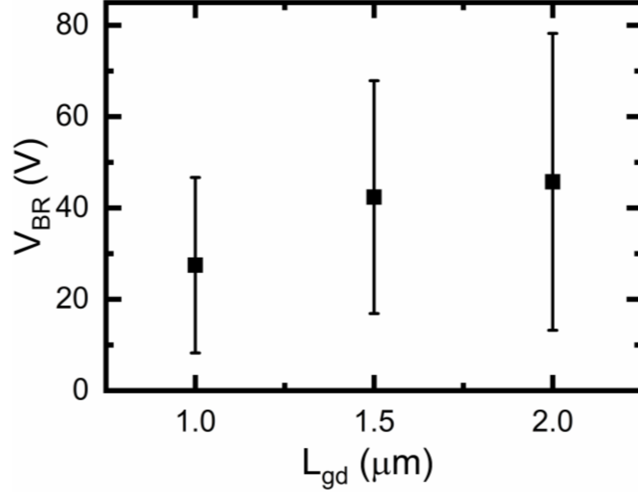


Figure 3.5 Breakdown voltage (BV) of device with different gate-drain distance (L_{gd}) with various gate lengths and corresponding error in BVs.

dual pulsed-IV setup with pulse width and duty cycle 10 μs and 0.1% respectively. The pulsed-IV gate and drain quiescent-bias voltages (V_{GSQ}, V_{DSQ}) started at cold-bias (0 V, 0 V) and then V_{GSQ} was reduced to pinch-off voltage (-8 V, 0 V) of the device followed by the drain quiescent voltage increment in 5 V increments till 15 V as shown in **Fig. 3.4**. The gate and drain voltages were pulsed in each period from the quiescent voltages (V_{GSQ}, V_{DSQ}) to corresponding V_{GS} and V_{DS} value. Final I_D values were measured by averaging the instantaneous drain current over the stable portion of the pulse. The maximum drain current for cold-bias (**Fig. 3.4(a)**) is slightly higher than the DC measurement (**Fig. 3.2**) due to absence of self-heating during pulsed IV measurements. Moreover, the drain current increased at quiescent points (-8 V, 0 V) and (-8 V, 5 V) before started collapsing later at V_{DSQ} = 10 V and 15 V which suggests that there are two competing mechanisms at play during device operations. This behavior was also observed in trans-conductance measurements (I_D-V_G, g_m and ΔV_{th}). This can be explained by a combination of donor traps under gate and surface traps in the gate-drain region. When the device is biased in the OFF-state (V_{GSQ} = -8V), the donor traps under the gate get ionized and contributes additional electrons into the 2DEG resulting in a higher saturation current, more negative threshold voltage and higher trans-conductance. However,

when the drain field is high (V_{DSQ} = 10, 15V), the surface traps near gate in the gate-drain region can capture electrons causing a virtual gate in the drain access region [97]. This virtual gate depletes 2DEG charges in the channel and results in reversal trend in I_{DSS} and other parameters as shown in **Fig. 3.4(d)**.

Three terminal off-state breakdown voltage was measured using Drain current injection (DCI) method developed by Alamo et al [98] using Keysight B1500A Semiconductor Device Parameter Analyzer. In the DCI method, a fixed drain current of 1 mA/mm was injected while the gate-source of V_{GS}. A total of 18 devices were measured for each value of L_{gd}. As shown in **Fig. 3.5**, though the mean BV increases with increase in L_{gd} the standard deviation for each L_{gd} is very high, which could be due to dielectric nonuniformity. The BV is higher than the N-polar GaN HEMTs with in-

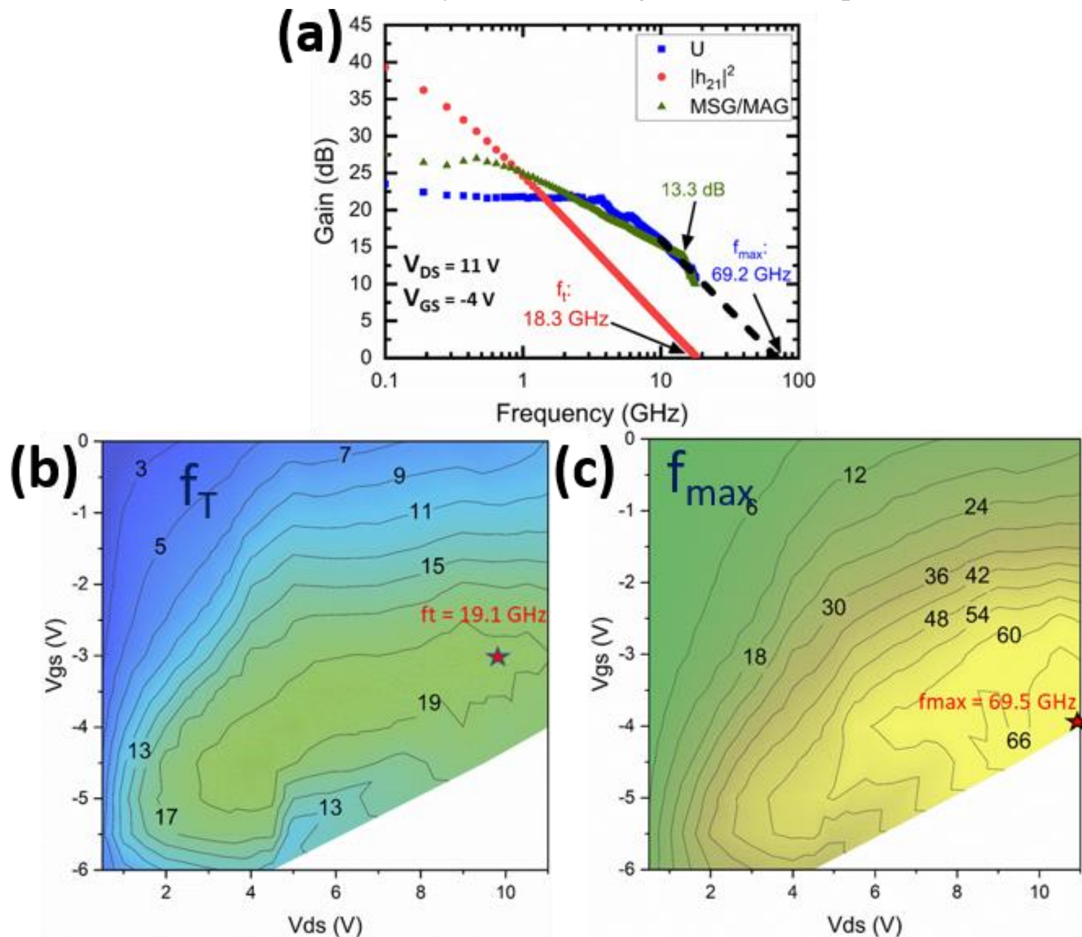


Figure 3.6 (a) RF performance HEMT, Contour plots of fT and fmax w.r.t. V_{GS} and V_{DS} without pad de-embedding.

situ MOCVD SiN as gate dielectric with similar 2DEG concentration [31]. The cause of the premature breakdown could be because of higher vertical electric field due to higher 2DEG concentration, weak trappy HfO_2/AlGaN interface. At high drain biases, the hot electrons can cause further damage to the interface voltage is swept from on-state to below pinch-off. The maximum drain voltage at which entire drain current switches entirely to gate current is defined as breakdown voltage (BV) irrespective of V_{GS}. A total of 18 devices were measured for each value of L_{gd}. Though the mean BV increases with increase in L_{gd} the standard deviation for each L_{gd} is very high, which could be due to dielectric non-uniformity. The BV is higher than the N-polar GaN HEMTs with in-situ MOCVD SiN as gate dielectric with similar 2DEG concentration [31]. The cause of the premature breakdown could be because of higher vertical electric field due to higher 2DEG concentration, weak trappy HfO_2/AlGaN interface. At high drain biases, the hot electrons can cause further damage to the interface.

The small-signal RF S-parameters were measured up to 18 GHz using a Keysight N5247B network analyzer calibrated to the probe tips via a Short-Open-Load-Thru (SOLT) calibration method from an off-wafer impedance substrate standard. The device with $W_G = 2 \times 50$ μm, $L_G =$ 500 nm, $L_{GS} = 400$ nm, and $L_{GD} = 1.5$ μm demonstrated a peak $f_T = 19.1$ GHz ($f_T \times L_G = 9.55$ GHz-μm) at V_{DS}= 10V and V_{GS} = -3V and a peak f_{max} = 69.5 GHz at V_{DS} = 11V and V_{GS} = -4V (**Fig. 3.6**). Due to increase in the leakage current at higher bias points, the S-parameters could not be measured for higher V_{DS}. The f_{max} and f_T measured on this device are higher than those measured on the N-polar HEMTs with SiN as gate dielectric with similar dimensions and EOT [31].

Loadpull measurements were carried out at Prof. Umesh Mishra's lab at UCSB using a continuous wave Maury microwave load pull system. The device was biased in class AB and the

I_{DSS} was swept at fixed V_{DSQ} to find the peak power added efficiency (PAE). The I_{DSS} at peak PAE was used for biasing point for the device for subsequent power measurements. The V_{DSQ} was swept for power measurements till the gate leakage is high while keeping the I_{DSS} constant. The device observed a transducer gain G_T of 9.56 dB, output power density Pout of 17.56 dBm and PAE of 42.54% at I_{DSS}=100 mA/mm and V_{DSQ}=4V as shown in Fig. 3.7. The gate leakage started to increase exponentially after V_{DSQ}=4V drain bias which prevented us from measuring at higher voltages.

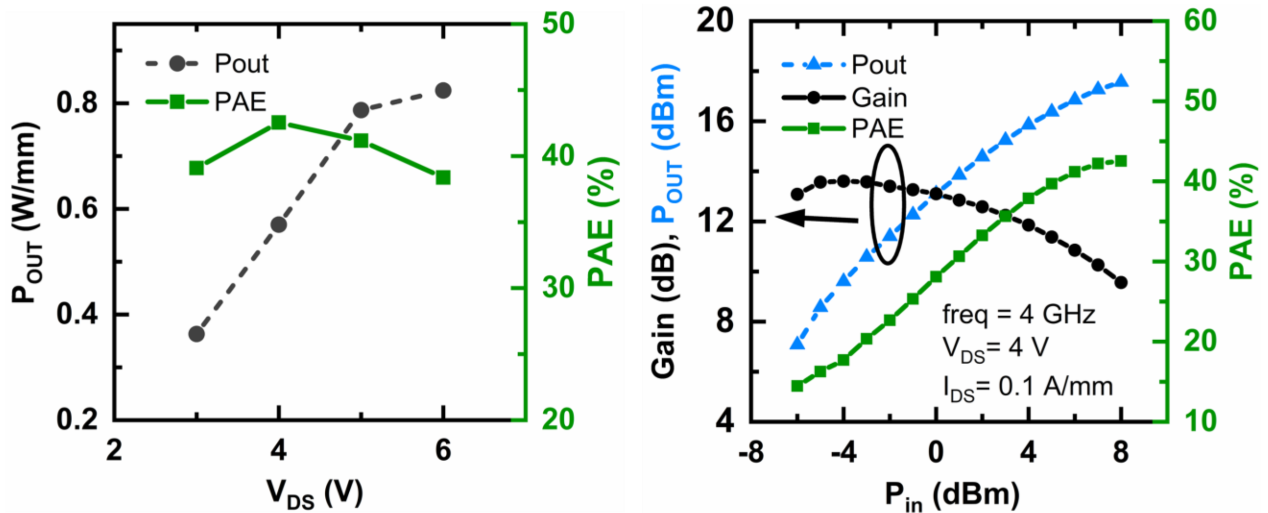


Figure 3.7. Large signal performance of the device at 4 GHz. (a) Dependence P_{out} and PAE on V_{DS} and Power performance at V_{DS} =4 V, I_{DSS} = 100 mA/mm.

3.4 Conclusion

We reported, for the first time, N-polar MIS-HEMT with HfO_2 as gate insulator deposited with thermal ALD. Pulsed IV measurements revealed two competing trapping mechanisms in the device. The MIS-HEMT demonstrated very low gate leakage, higher trans-conductance and f_T, f_{max} values as compared to the HEMTs with SiN as dielectric. This shows promises for ultra-thin channel high-aspect ratio HEMT devices for high frequency applications.

Chapter 4

N-polar Deep Recessed (NPDR) HEMT with HfO_2 as gate dielectric

4.1 Introduction

It was observed in the previous chapter that traps in the gate-to-drain access region are responsible for the DC-RF dispersion. As mentioned in the Chapter 1 [39,99], N-polar deep recess (NPDR) structures can reduce this dispersion significantly. The epi-layer schematic of a N-polar deep recessed (NPDR) HEMT is shown in Fig. 4.1. The only difference with planar HEMT is the in-situ grown GaN cap region on top of AlGaN cap layer. This GaN cap layer is recessed etched during HEMT fabrication. By introducing a GaN cap in the access region [32], the surface traps are moved away from the channel and the pinch-off voltage in the access region becomes more negative (~ -30 V). Hence any change in surface potential in the access region would not change the channel potential, consequently resulting in significantly less DC-RF dispersion. Additionally,

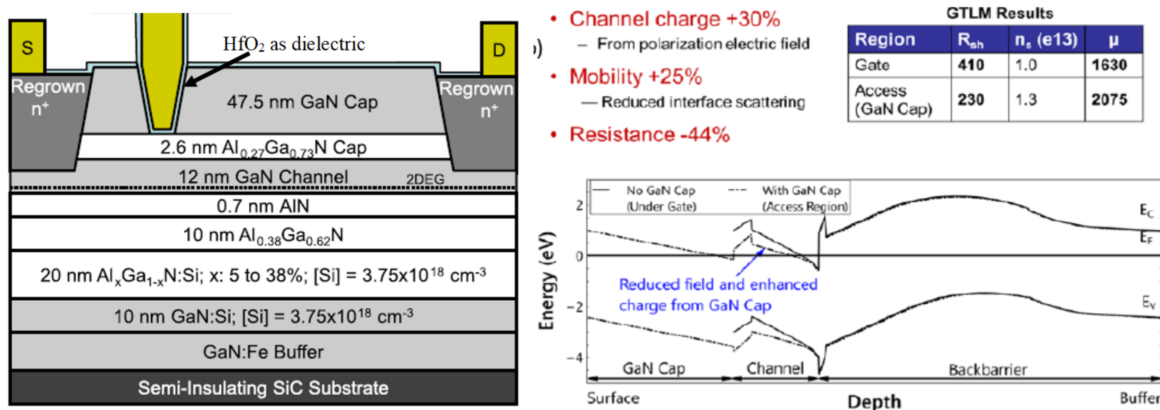


Figure 4.1 Device cross-sectional schematic and epitaxial layer profile of the N-polar deep recess (NPDR) with HfO_2 as gate dielectric (b) Energy band diagram comparing the vertical profiles under the gate electrode as compared to the access region with the addition of a GaN cap layer

the GaN cap is advantageous as it enhances the conductivity of the access regions for three reasons

as described in Chapter 1: (i) The introduction of GaN cap layer reduces the vertical electric field in the channel as shown in Fig. 4.1. This pushes the conduction band downwards which leads to an increase in the 2DEG concentration. (ii) The reduction in vertical electric field improves lateral mobility. (iii) The surface is moved away from the channel which reduces the surface scattering and further improves the mobility.

In this work, the NPDR HEMT structure is combined with high-k HfO_2 for RF application. I also fabricated three different samples with a HfO_2 thickness series to understand the effect of HfO_2 thickness on various HEMT characteristics if any.

4.2 Device fabrication

The device fabrication process is almost similar to planar HEMT except for a few additional intermediate steps due to the in-situ GaN cap in NPDR HEMT epi-structure. SiO_2 and Al_2O_3 were used as the hard mask and etch stop layer, respectively, to define the source/drain regrown area. The

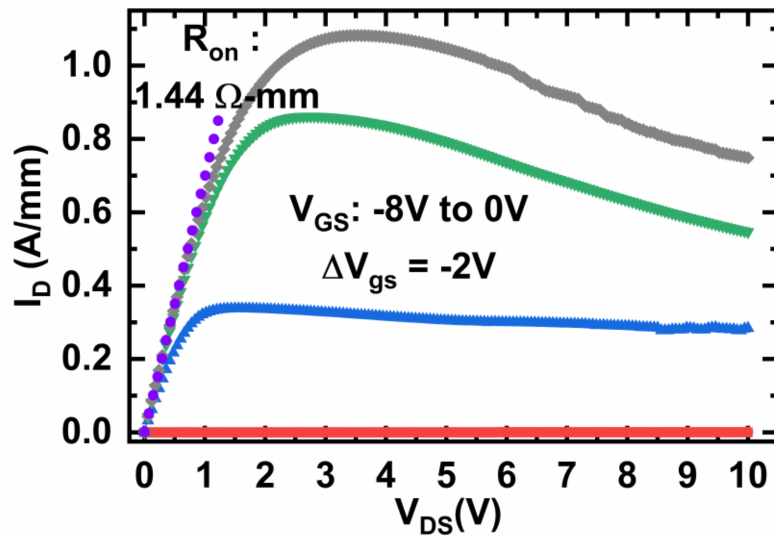


Figure 4.2 (a) Output characteristics and for Vgs from -8 V to 0 V with 2 V increments. The extracted Ron is 1.28 Ω-mm at Vgs = 0V.

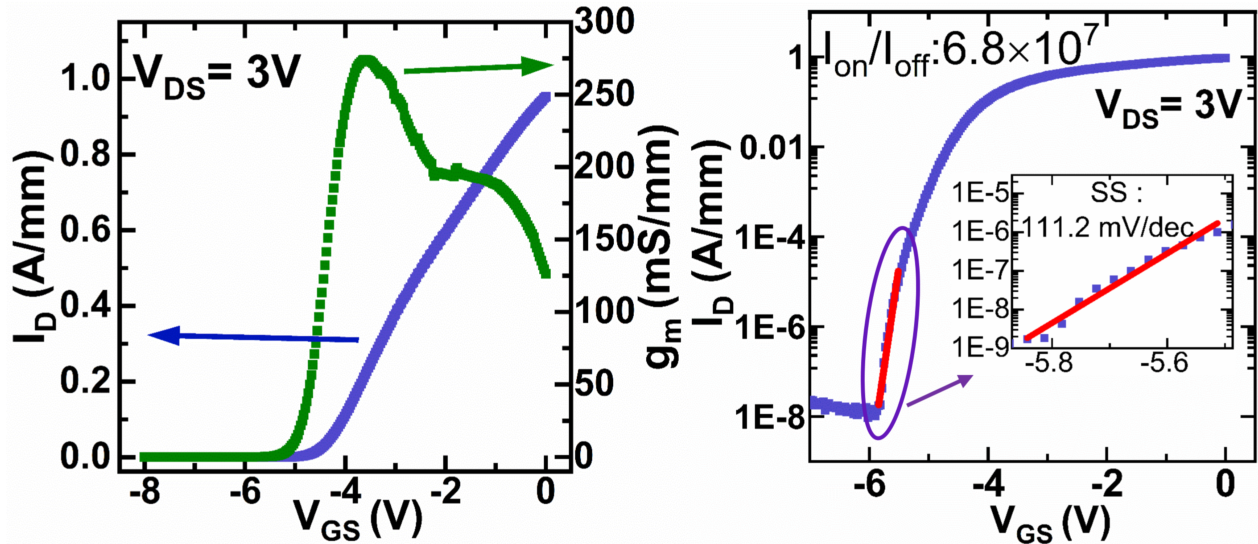


Figure 4.3 (a) Transfer characteristics (blue) and trans-conductance (green) at V_{DS} = 3 V (b) drain current and gate leakage in semi-log scale. The subthreshold slope is 111.2 mS/dec.

GaN cap was etched with a selective BCl_3/SF_6 dry etch which has 20:1 selectivity with AlGaN layer resulting in a smooth surface. Subsequently a UID-GaN/n_{++} GaN (10 nm/60 nm) was regrown by plasma-assisted molecular beam epitaxy (PAMBE) for better ohmic contacts. Device isolation was achieved by ion implantation with Aluminum. Subsequent I-V measurements of isolation test structures revealed 3.4 nA/mm leakage current in buffer. A recess etch was then performed under the gate area using BCl_3/SF_6 selective dry etch using, followed by a sequence of wet cleaning, UV-ozone conditioning and in-situ ALD plasma treatment prior to deposition of thermal ALD HfO_2 [93]. HfO_2 was removed in source and drain regions using a selective BCl_3-based dry etch, followed by

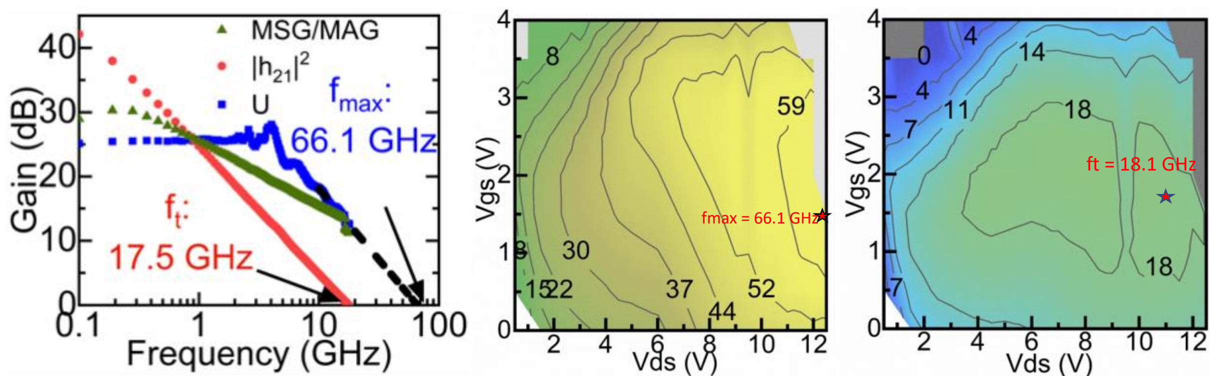


Figure 4.4 (a) RF performance HEMT, Contour plots of fT and fmax w.r.t. VGS and VDS without pad de-embedding.

hydrochloric acid wet etching prior to deposition of 30 nm/200 nm of Ti/Au metal stack by electron-beam evaporation. Metal-to-GaN contact resistance of 0.4 Ω·mm was measured from un-passivated Transfer Length Measurement (TLM) because of the regrown UID/n^{++} GaN film which has a very low sheet resistance (R_{sh}) of only 101 Ω/sq. Finally, 30/420 nm of Ti/Au optical gate and contact pads were patterned via liftoff. Unlike the planar HEMTs, the sample was not passivated with PECVD SiN since in-situ GaN cap acts as a passivation layer.

4.3 Results and Discussion

DC measurements were performed on a device with $W_G = 2 \times 50$ µm, $L_G = 500$ nm, $L_{GS} = 400$ nm, $L_{GD} = 1$ µm as shown in Fig. 4.2. The output characteristics demonstrated a maximum I_{DSS} of 1.02 A/mm and an ON-resistance (R_{on}) of 1.44 Ω·mm at $V_{GS} = 0$ V with typical self-heating behavior on sapphire substrate [96]. The transfer characteristics showed a peak trans-conductance (g_m) of 274 mS/mm, pinch-off voltage (V_P) of -4.6 V and a subthreshold swing of 111.2 mV/dec at $V_{DS} =$ 3 V as depicted in Fig. 4.3. The device revealed an OFF-state current of 1.5×10^{-7} A/mm at $V_{DS} =$ 3V with I_{ON}/I_{OFF} ratio of 6.8×10^7.

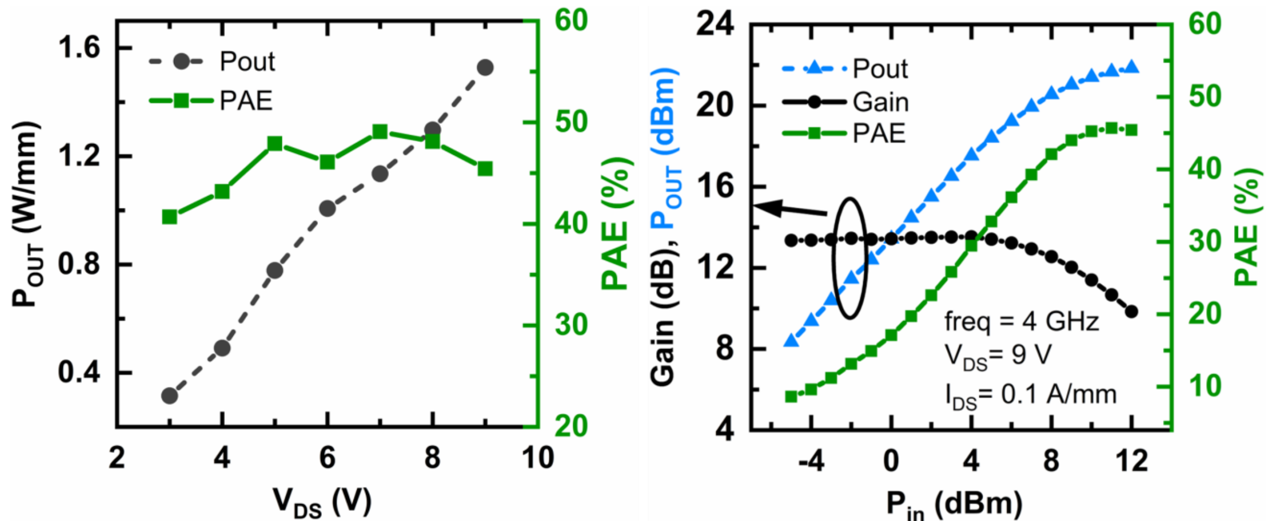


Figure 4.5. Large signal performance of the device at 4 GHz. (a) Dependence P_{out} and PAE on V_{DS} and Power performance at V_{DS} =9 V, I_{DSS} = 100 mA/mm.

The small-signal RF S-parameters were measured up to 18 GHz using a Keysight N5247B network analyzer calibrated to the probe tips via a Short-Open-Load-Thru (SOLT) calibration method on an off-wafer impedance substrate standard. The device with $W_G = 2 \times 50$ µm, $L_G = 500$ nm, $L_{GS} = 400$ nm, and $L_{GD} = 1$ µm demonstrated a peak $f_T = 18.1$ GHz ($f_T \times L_G = 9.55$ GHz-µm) at $V_{DS} = 10.5$V and $V_{GS} = -1.5$V and a peak fmax = 66.1 GHz at $V_{DS} = 12.5$V and $V_{GS} = -2.5$V (Fig. 4.4). Loadpull measurements were carried out at Prof. Umesh Mishra's lab at UCSB using a continuous wave Maury microwave load pull system. The device was biased in class AB and the I_{DSS} was swept at fixed V_{DSQ} to find the peak power added efficiency (PAE). The I_{DSS} at peak PAE was used for biasing point for the device for subsequent power measurements. The V_{DSQ} was swept for power measurements till the gate leakage is high while keeping the I_{DSS} constant. The device observed a transducer gain G_T of 9.84 dB, output power density Pout of 21.84 dBm and PAE of 45.4% at I_{DSS}=100 mA/mm and V_{DSQ}=9V as shown in Fig. 4.5. The gate leakage started to increase exponentially after 9 V drain bias which prevented us from measuring at higher voltages.

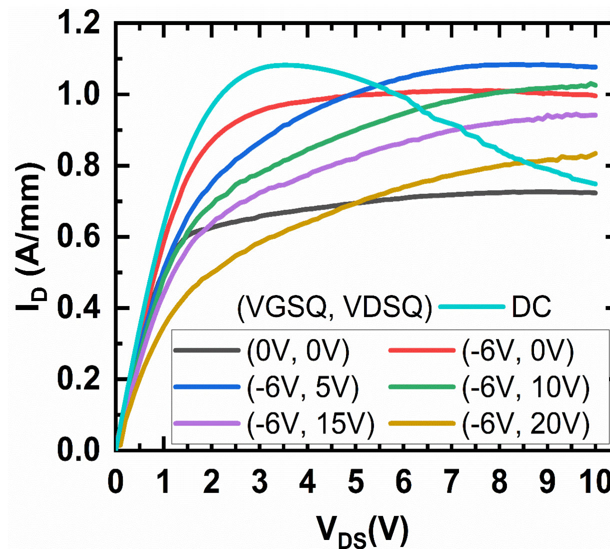


Figure 4.6 Dual Pulsed-IV measurement was measured with pulse width and duty-cycle 10 µs and 0.1% respectively at various gate and drain quiescent voltages.

To determine the suppression of surface traps, pulsed-IV measurements were conducted on the same device with Keysight B1525A dual pulsed-IV setup with pulse width and duty cycle of 10 μs and 0.1% respectively. The pulsed-IV gate and drain quiescent-bias voltages (V_{GSQ}, V_{DSQ}) started at cold-bias (0 V, 0 V) and then V_{GSQ} was reduced to higher than pinch-off voltage (-6 V, 0 V) of the device followed by the drain quiescent voltage increment in 5 V increments till 20 V as shown in Fig. 4.6. The gate and drain voltages were pulsed in each period from the quiescent voltages (V_{GSQ}, V_{DSQ}) to corresponding V_{GS} and V_{DS} value. Final I_D values were measured by averaging the instantaneous drain current over the stable portion of the pulse. As can be seen from Fig. 4.6(a), the device shows both anti-dispersion and dispersion as discussed previously. This behavior was also observed in transfer measurements (I_D-V_G, g_m and ΔVth) as can be seen in Fig. 4.6(b). Similar behavior was observed in various other measured devices.

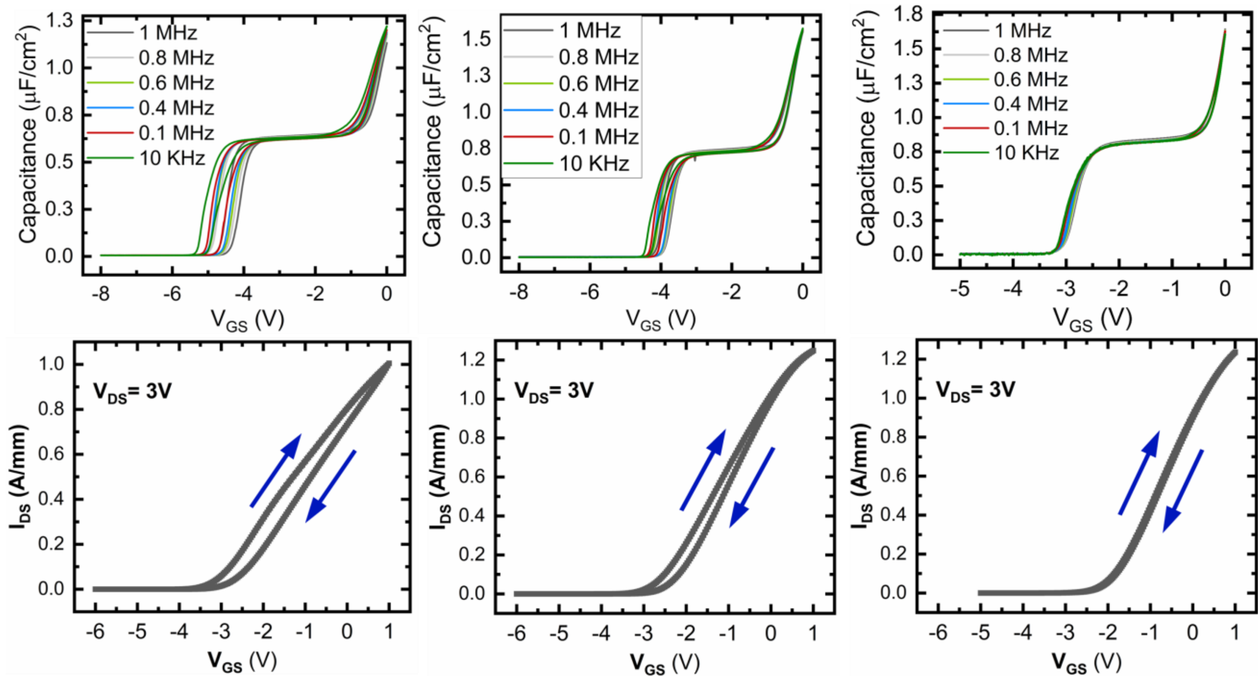


Figure 4.7 CV hysteresis and IdVg hysteresis for sample-A, B & C with 10.1 nm, 7.1 nm, 4.4 nm HfO_2 thickness respectively. The hysteresis decreases with increase in HfO2 thickness.

4.4 HfO_2 Thickness series

As discussed earlier, the in-situ GaN acts as self-passivating layer in the access region. However, the devices still showed significant dispersion. The reason could lie inside HfO_2 dielectric. To further investigate the reason for such high dispersion, three NPDR HEMTs with three different HfO_2 thickness (10.1 nm, 7.1 nm, 4.4 nm) were fabricated. Since the HEMTs were fabricated together and only difference is the dielectric thickness, any variation in characteristics between the samples can be attributable to gate dielectric. These set of samples were treated with piranha solution for 5 min as compared to 1 min for the previous deep recess samples.

All three samples exhibited charge density of 1.6-1.8x10^{13} cm^{-2}. The regrown contact resistance was 0.25-0.3 ohm-mm. C-V hysteresis was measured to be 0.46V, 0.3V and <0.05V for samples with 10.1 nm (sample A), 7.1 nm (sample B), 4.4 nm (sample C) HfO_2 thickness, respectively. Similarly, the I_D-V_G hysteresis decreased with HfO_2 thickness as shown in fig 4.7.

Pulsed-IV measurements were carried out to understand the source of DC-RF dispersion observed earlier. Drain saturation current in the on-state (I_{DSS} at Vg=0V), dynamic R_{on}, peak transconductance at V_D=3V (g_m), change in threshold voltage (ΔV_{th}) was observed in the pulsed-IV measurement. Three devices D4, E4, F4 with different gate-to-drain distances of 1 um, 1.5 um, 2 um, respectively, were measured for all three samples (Sample-A, B,C) to understand the effect of gate-drain field on DC-RF dispersion. The surface traps are activated by the field present between gate and drain which reduces with L_{GD}. Therefore, for a fixed (V_{GSQ}, V_{DSQ}), device D4 is expected to have the highest field in the access region, while device F4 is expected to have the lowest field. The pulsed-IV results are shown in Figs. 4.8 and 4.9. The parameters (I_{DSS}, R_{on}, ΔV_{th}) remain almost unchanged between the devices D4, E4 and F4 at various gate and drain quiescent biases as shown in figure 4.8 (a,b,c). Similar behavior was also observed in sample-B and sample-

C. This indicates that although the surface electric field between gate and drain is varying significantly, it has no effect on the channel which proves the effectiveness of the deep recessed architecture.

Figure 4.9 presents the same DC-RF dispersion data for a particular device across different samples which have different HfO_2 dielectric thickness as mentioned before. As can be seen, on sample-A which has the thickest (10.1 nm) HfO_2, the normalized I_{DSS} varies significantly for different bias

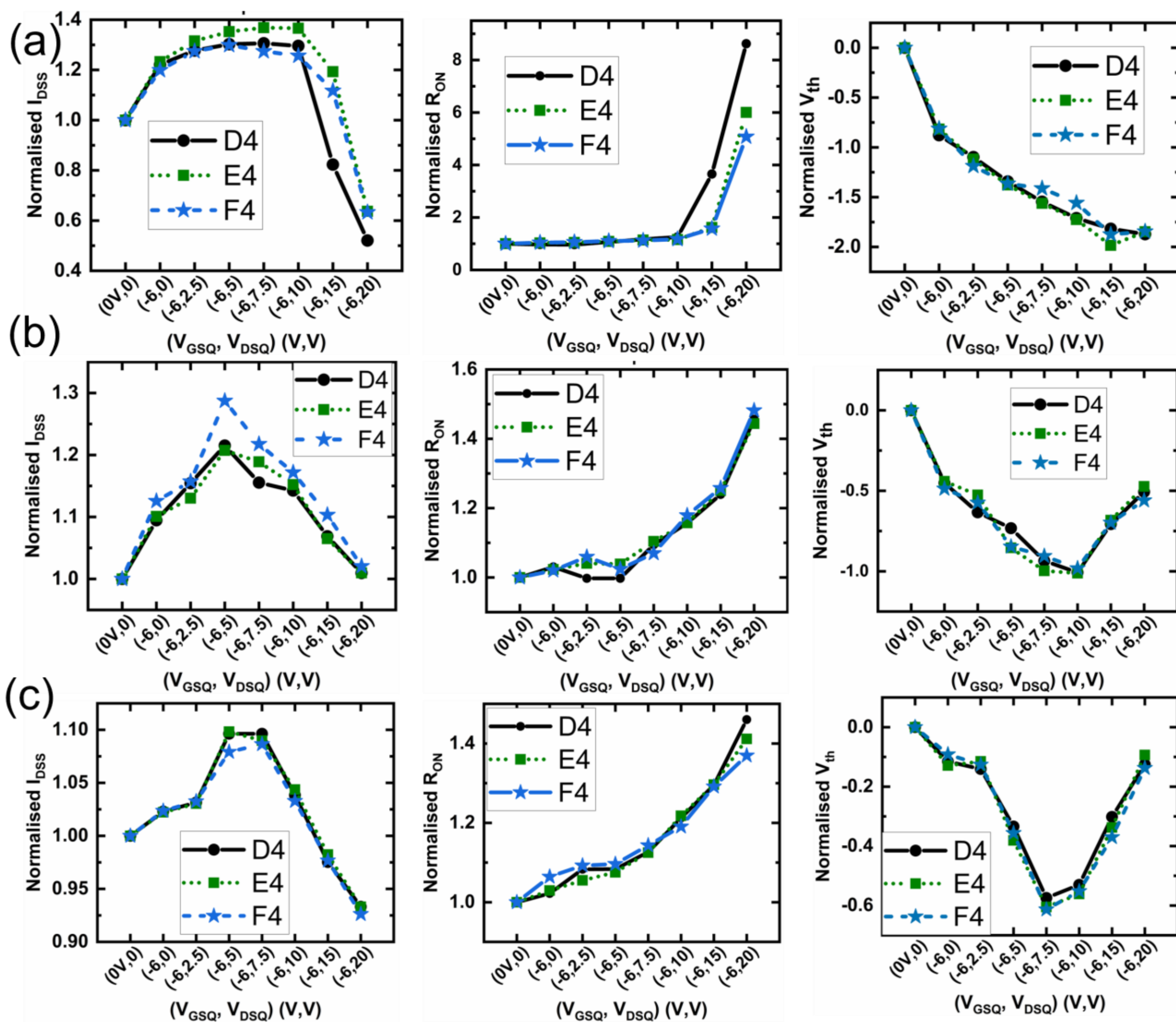


Figure 4.8 Normalized I_{DSS}, normalized dynamic Ron, and Vth shift was measured for three devices D4, E4, F4 which has 1µm, 1.5µm, 2µm gate-to-drain distance for three samples with three different gate dielectric thickness (a)10.1nm, (b)7.1nm, (c)4.4nm. All the parameters were almost same indicating that traps in the gate-to-drain region does not cause DC-RF dispersion

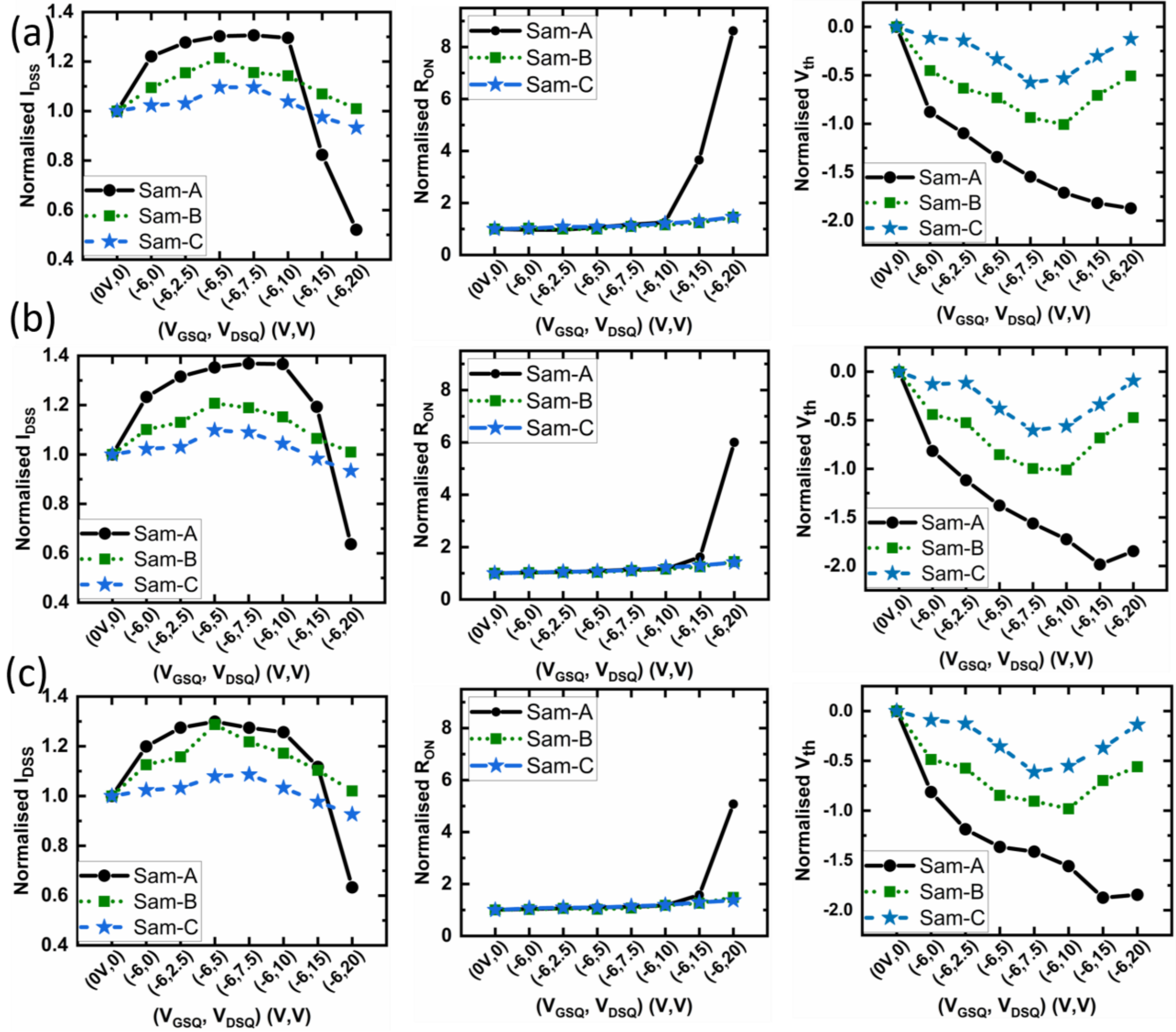


Figure 4.9 Various parameters (Normalized IDSS, normalized dynamic Ron, and Vth shift) were compared for three samples (Sample-A, B & C) with three different gate dielectric thickness 10.1nm, 7.1nm, 4.4nm respectively for same devices (a) D4 with Lsd=1 µm (b) E4 with Lsd=1.5 µm (c) F4 with Lsd=2 µm.

points. The maximum deviation is around 30% from cold vias (V_{GSQ}=0V, V_{DSQ}=0V). Moreover, most of the deviation (~20%) from cold bias occurs during gate lag (V_{GSQ}= -6V, V_{DSQ}=0V). The subsequent change in I_{DSS} is small as the drain quiescent voltage V_{DSQ} increases from 0V to 20V. The I_{DSS} shift is directly correlated to the negative shift in threshold voltage. As the gate and drain quiescent voltages increase, the threshold voltage shifts in negative direction causing the I_{DSS} to increase. This shift is the highest in thicker HfO_2 and vice versa. It is important to observe that the

dynamic Ron did not change across samples which indicates that the channel resistance in the access region remain unaffected by surface electric field indicating no effect of traps on channel. This behavior was also observed in other two devices namely E4 and F4 which indicates that there are bulk traps present in the HfO_2 which is thickness dependent and affects the DC-RF dispersion. These traps also cause the leakage current through the dielectric resulting in premature breakdown of device. As a result, the device with 4.4nm HfO_2 thickness breaks down at V_{DD}=5V. Additionally, this explains the BV measurement that BV is not dependent on gate-to-drain distance L_G.

The loadpull measurements were carried out at University of California, Santa Barbara using a Maury microwave system at 4GHz as shown in Fig. 4.10. The large signal load pull was limited by premature dielectric breakdown for all three devices. However, the sample-A demonstrated

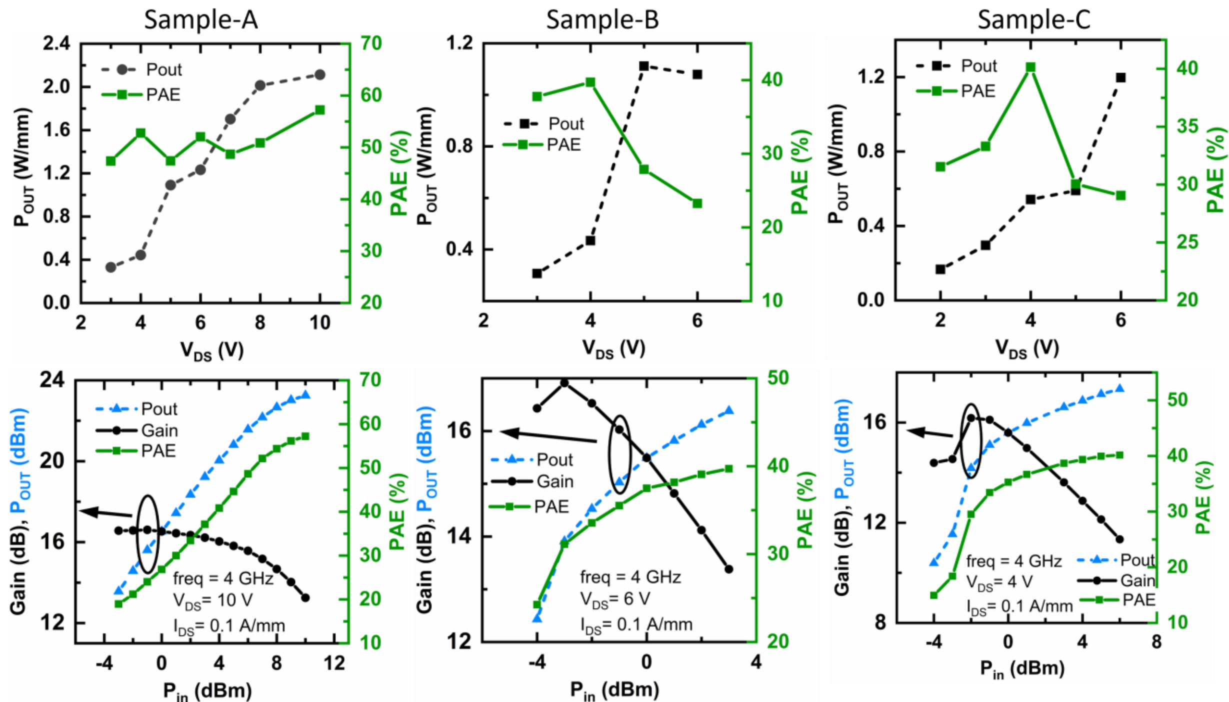


Figure 4.10. Large signal performance at 4 GHz for three samples (Sample-A, B & C) with three different gate dielectric thickness 10.1nm, 7.1nm, 4.4nm respectively for same devices. Dependence P_{out} and PAE on V_{DS} and Power performance at different V_{DS}, I_{DSS} = 100 mA/mm.

better performance than the previous deep recess HEMT as shown in Fig. 4.5. This could be because of the cleaner surface because of longer piranha treatment of the sample before HfO_2 deposition.

4.5 Conclusion

In summary, we reported first demonstration of N-polar deep recessed HEMT with HfO_2 as dielectric. The device exhibited peak saturation current of 1.1 A/mm, external transconductance 274 mS/mm, and I_{ON}/I_{OFF} ratio of 6.8×10^7. The device demonstrated a small signal current gain cut-off frequency of 18.1 GHz and power gain cut-off frequency of 66.1GHz. Loadpull measurements reveal that max out power achieved was 1.53W/mm at with PAE of 45.4% at I_{DSS}=100 mA/mm and V_{DSQ}=9V. The device may offer more power capability with improvement in HfO_2 dielectric. PulsedIV measurements reveal dependence of dispersion on traps present in HfO2 dielectric which affects the threshold voltage, hence the peak saturation current.

Chapter 5
Design of Ultra-scaled-channel N-polar GaN HEMTs with High Charge Density: A Study of Hole Traps and Their Impact on Charge Density in the Channel

5.1 Introduction

It is now well-stablished fact that donor-like surface states provide electrons to the channel in Ga-polar AlGaN/GaN hetero-structures [100]. Therefore, doping the barrier with n-type donors such as silicon (Si) is not required to form 2DEG in Ga-polar HEMT structures. It is also shown that n-type doping of the barrier is not required to form 2DEG in N-polar HEMT structures [101]. However, in contrast to Ga-polar HEMT structures, a large DC-RF dispersion and anomalous output conductance [102] were observed when the barrier was not Si-doped in N-polar GaN HEMT structures. It is shown that the observed current dispersion is attributed to hole/donor traps 60 meV above the valence band (VB) at (Al, Ga) N/GaN interface with net negative polarization charge [103]. In the absence of n-type doping in the back-barrier, the VB becomes very close to the fermi level and consequently the hole traps are ionized (similar to **Fig. 5.1(b)**), imaging more charge in the channel leading to a larger DC current. These traps cannot respond at high frequencies causing current collapse [16][103]. Similar donor/hole trap was also found at InGaN/GaN interface with negative polarization charge and was measured to be ~70 meV from VB via deep level transient spectroscopy (DLTS) with a trap density of at least 4×10^{11} cm^{-2} [104]. There are also reports of deep hole traps present at 700 meV [105]and 790 meV [106] in InGaN/GaN multiple-quantum-well (MQW) LED system and shallow donor levels at 77 and 91 meV in AlGaN/InGaN/GaN LED system [107]. Very recently, using positron annihilation

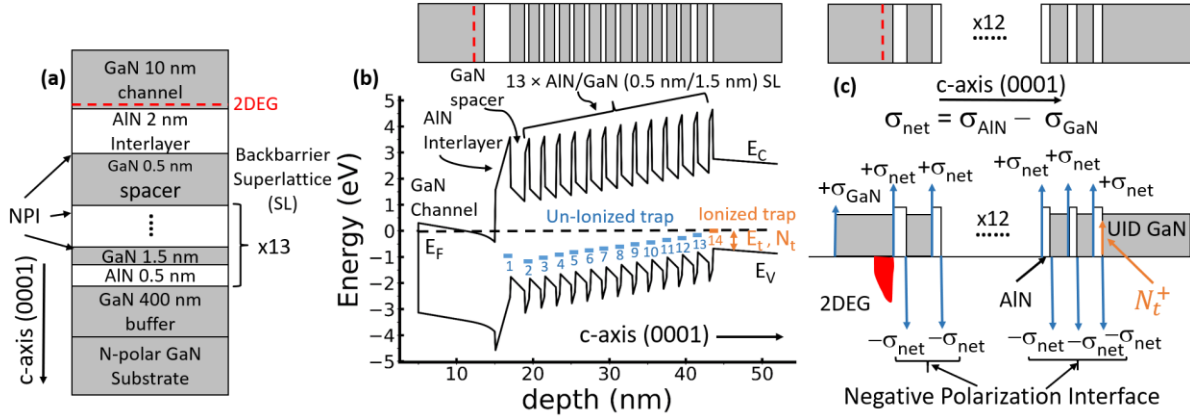


Figure 5.1 Schematic cross-section of epi-layer, **(b)** the band diagram with donor trap at E_t = 715 meV for $N_t = 3\times10^{13}$ cm^{-2}, **(c)** different charges present in the structure along c-axis. Traps are assumed to be present at AlN/GaN NPIs. Ionized hole traps are positively charged.

spectroscopy [108], interfacial nitrogen vacancies (V_N) present at negative polarization interface (NPI) were determined to be the source of these hole/donor traps. Nevertheless, so far, there has been no rigorous study on the relationship between the hole traps and 2DEG density in N-polar HEMT structures.

In this work, we have adapted the epi-structure in Ref [24][109] which has been reproduced in Figure 5.1 with band diagram and charge distribution. We studied the effect of hole traps density and energy level on 2DEG density in N-polar HEMT structures using the Silvaco TCAD simulation platform. Here, we show that exclusion of the hole traps in the 2DEG calculations leads to an underestimation of 2DEG density in N-polar GaN HEMT structure, especially for barriers with high Al content. Comparing the calculated 2DEG density with that of experimentally measured on N-polar GaN HEMT structures grown by plasma-assisted molecular beam epitaxy (PAMBE), we found an estimation for the hole trap energy and density in AlN/GaN NPIs. Si doping profiles were then examined to prevent ionization of hole traps. A barrier structure was designed to achieve high charge density in ultra-scaled N-polar HEMTs.

5.2 Simulation Framework

The strain-dependent material structure, spontaneous and piezoelectric polarization were included in the simulation to introduce the correct polarization charges at the heterointerfaces. Built-in models in Silvaco Atlas were utilized to set the polarization (POL.SET3) and band parameters (KP.SET3) for GaN and AlN material systems [110–112]. N-polar epi-structure was implemented by setting negative polarization scale in the model. The interface traps present at AlN/GaN NPIs have been added to the models with characteristic energy level (E_t) and density (N_t). Fermi-dirac carrier statistics with incomplete ionization of impurities and Shockley-Read-Hall (SRH) recombination model were incorporated in the simulation. The Schottky contact on GaN channel and cathode under GaN buffer have been implemented as floating electrode which is best simulated by specifying current boundary conditions. Newton solver was used to obtain convergence for the Poisson's equation at each mesh-node to calculate charge density.

5.3 Results and Discussion

5.3.1 Hole Traps and Their Impacts on 2DEG Density

The schematic cross-section of the AlN/GaN HEMT structure studied in this section is shown in **Fig. 5.1(a)**. The back-barrier consists of 13 period AlN/GaN (0.5 nm/1.5 nm) digital alloy (equivalent to a 26 nm-thick $Al_{0.25}Ga_{0.75}N$ film). A digital alloy barrier has been previously used to prevent growth interruptions [109][113]. The 2DEG present in 10nm-thick GaN channel is separated from the back-barrier by a 0.5nm-thick GaN spacer and a 2nm- or 4nm- thick AlN interlayer. UID doping for GaN and AlN layers were assumed to be 5×10^{16} cm^{-3} and 5×10^{17} cm^{-3}, respectively.

The band diagram corresponding to this N-polar GaN HEMT structure with a 2nm-thick AlN and assuming hole traps with a density and energy of 3×10^{13} cm^{-2} at 715 meV at NPIs is illustrated in **Fig. 5.1(b)**. These values are randomly chosen for the sake of illustration; however, a wide range of trap densities and energies have been studied and will be discussed in this manuscript. The barrier height on GaN surface was assumed to be 0.3eV, which is consistent with what has been observed experimentally for N-polar GaN bare surface [114]. There are 14 NPIs in this heterostructure. The corresponding charges present in the structure, including polarization charges, 2DEG, and ionized hole traps are shown in **Fig. 5.1(c)**. It was reported experimentally that even in the absence of n-type doping, a large-density 2DEG (more than 10^{13} cm^{-2}) can be formed in N-polar HEMT structures [101][109]. This negative charge must be compensated by an equal amount of positive charge to maintain charge neutrality. In the absence of n-type doping in the epi-structure, one source of positive charges is the unintentional oxygen doping present in AlN and GaN, but this is insufficient to provide large density of 2DEG. Additionally, in the absence of Si-doping, due to polarization field, the VB becomes very close to the fermi level at NPIs, which would in theory lead to formation of a hole gas. Instead, hole/donor traps at these interfaces become ionized (positively charged), providing the positive charge required to satisfy charge neutrality in the system.

The epi-structure in **Fig. 5.1(a)** was simulated for a wide range of trap densities (10^{12} cm^{-2}- 8×10^{13} cm^{-2}) and the corresponding band diagram is illustrated in **Fig. 5.2(a)**. For very low trap densities (e.g. 1×10^{12} cm^{-2}), the ionization of only one trap is not sufficient to compensate the 2DEG, as a result, trap-14 crosses the fermi level and gets fully ionized. As the valence band comes closer to fermi level, several traps at different NPIs cross the fermi level resulting in complete ionization of these traps (**Fig. 5.2(b)**). For instance, for a trap density of 1×10^{12} cm^{-2}, traps at NPIs

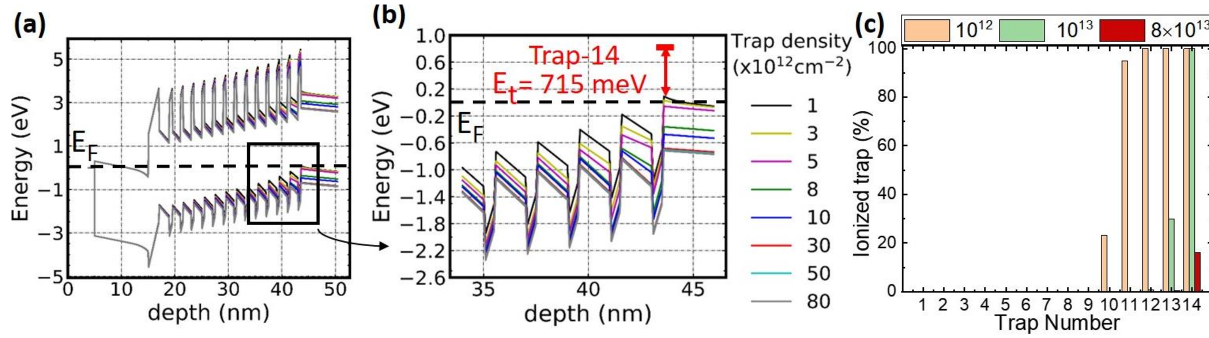


Figure 5.2 **(a)** Band diagrams for epi-structure described in Fig. 4.1 (a) with 2nm-thick AlN interlayer assuming hole trap with energy of 715 meV and different trap densities at NPIs for barrier height of 0.3 eV at GaN channel surface, **(b)** magnified band diagram near VB at barrier-buffer interface, **(c)** Density of ionized traps shown for all the 14 NPIs, for three different trap densities throughout the epi-structure.

from 10 to 14 are all completely ionized, and the rest of the traps are partially ionized (**Fig. 5.2(c)**). However, for trap densities equal and beyond 3×10^{13} cm^{-3}, the fermi level gets pinned at trap-14, and the VB cannot get closer to the fermi level. As an example, for a trap density of 8×10^{13} cm^{-2}, trap numbers 13 and 14 are only partially ionized which provides sufficient amount of positive charge to satisfy charge neutrality in the system. **Figure 5.2(c)** demonstrates the percentage of ionized traps for three different trap densities at each NPI. As shown in this figure, traps present at interface-14 play a major role in 2DEG modulation at all trap densities and trap energies.

The trap ionization profile changes significantly as the AlN interlayer thickness increases. Increasing AlN thickness is required in ultra-scaled channel N-polar GaN HEMT structures to maintain a large 2DEG density in the channel. **Figure 5.3(a)** illustrates the band diagram for the N-polar HEMT structure shown in **Fig. 5.1(a)** having 4 nm-thick AlN interlayer with varying hole trap density at the NPIs. The positive electric field in AlN interlayer pulls up the VB as AlN thickness increases. Therefore, in contrast with 2nm-thick AlN interlayer, in this case the VB at NPI-1 becomes very close to the fermi level (**Fig. 5.3(b)**). Hence, the entire valence band throughout the interlayer and the digital alloy back-barrier gets closer to fermi level. **Figure 5.3(c)** demonstrates the percentage of ionized traps for three different trap densities at each NPI. For a

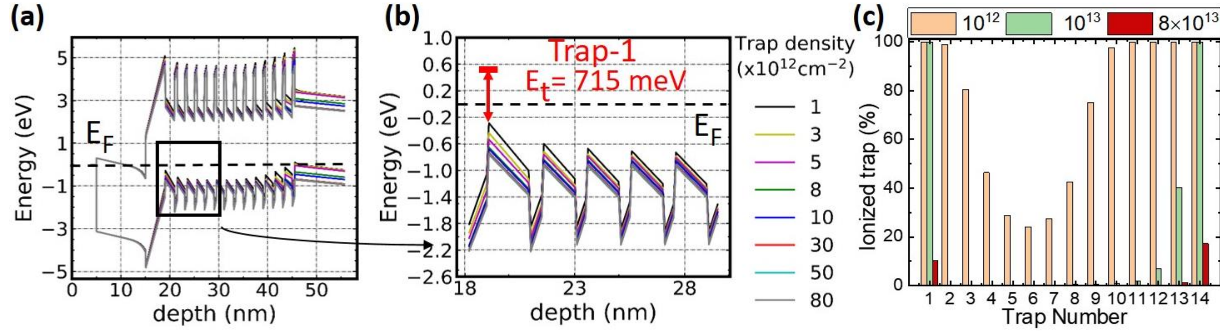


Figure 5.3 (a) Band diagrams for epi-structure described in Fig. 4.1 (a) with 4 nm-thick AlN interlayer assuming hole trap with energy of 715 meV and different trap densities at NPIs for barrier height of 0.3eV at GaN channel surface, (b) magnified band diagram near VB at barrier-buffer interface, (c) Density of ionized traps shown for all the 14 NPIs for three different trap densities throughout the epi-structure.

trap density of 1×10^{12} cm^{-2}, traps near NPI-1 and NPI-14 are fully ionized, while a significant portion of hole traps at other NPIs are also ionized as shown in **Fig. 5.3(c)**. As we increase trap density beyond 3×10^{13} cm^{-3}, the fermi level gets pinned both at trap-1 and 14 and fully ionized whereas traps at other NPIs remain unionized. This contrasts with the previous case of 2 nm AlN interlayer in which only the traps near NPI-14 was ionized, and the traps at NPI-1 remained far below the VB.

The 2DEG density as a function of trap energy for various trap densities was calculated in the 10 nm-thick channel N-polar GaN HEMT structure shown in **Fig. 5.1(a)** with 2 nm and 4 nm-thick AlN interlayer and in the results are shown in **Figs. 5.4(a)** and **(b)**, respectively. For a certain trap energy, the 2DEG density increases as the trap density increases. This increase is more prominent for hole traps at higher energy levels. Moreover, the additional trap ionization in the N-polar GaN HEMT structure with 4 nm-thick AlN interlayer modulates the 2DEG charge more significantly as evident from **Figs 5.4(a)** and **(b)**. For 2 nm-thick AlN interlayer, there is little variation in 2DEG charge density with trap density. However, for 4 nm-thick AlN interlayer, the variation is significant due to additional trap ionization near the channel and mid-barrier. As a result, higher trap density and trap energy lead to higher trap ionization and hence higher 2DEG

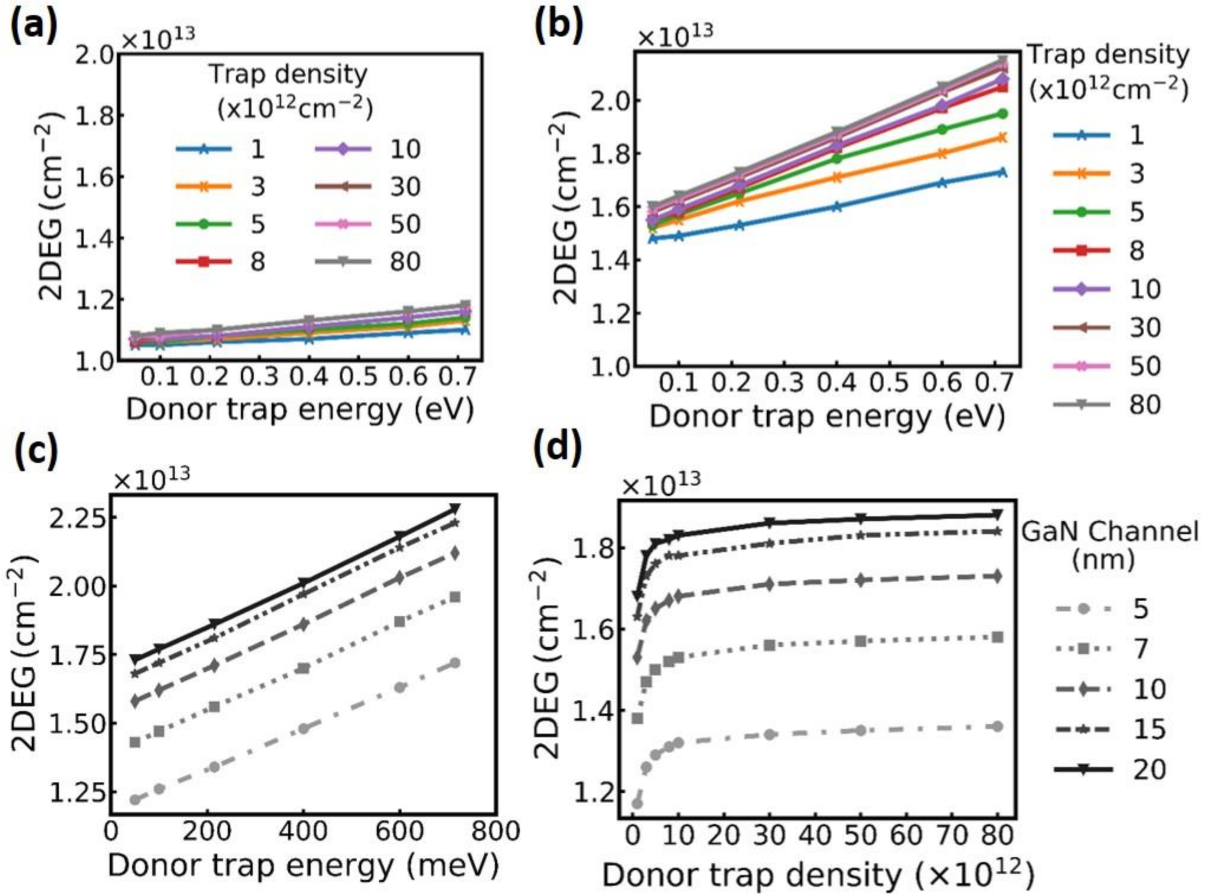


Figure 5.4. 2DEG vs donor trap energy varying trap density for AlN interlayer thickness of (a) 2 nm and (b) 4 nm for epi-structure described in Fig. 4.1(a) with 10 nm channel thickness. (c) 2DEG vs donor trap energy, assuming $N_t = 3\times10^{13}$ cm^{-2} (d) 2DEG vs donor trap densities, assuming $E_t = 215$ meV for epi-structure described in Fig. 4.1(a) with 4nm-thick AlN interlayer and varying GaN channel thickness.

density. **Figure 5.4(c)** shows 2DEG density as a function of trap energy level for an N-polar GaN HEMT structure with 4 nm-thick AlN interlayer and various channel thicknesses. As expected, 2DEG density increases by increasing the channel thickness. The 2DEG charge shows almost linear dependence with trap energy level which is consistent across the GaN channel thickness. **Figure 5.4(d)** depicts 2DEG density as a function of trap density assuming trap energy level of 215 meV. At lower trap densities, the 2DEG density increases with trap density. This can be explained by the band diagrams shown in **Figs. 5.2(b) and 3(b)**. At lower trap densities, since the traps can cross the fermi level without the fermi level getting pinned, the electric field in the AlN

interlayer and the channel reduces by increasing trap densities which leads to an increase in 2DEG density (**Figs. 5.2(b) and 5.3(b)**: black to green line). However, for a sufficiently large trap density ($\geq 1\times10^{13}$ cm^{-2}), the fermi level gets pinned at the trap level (**Figs. 5.2(b) and 5.3(b)**: purple to grey line). Therefore, the electric field in the channel remains unaltered by further increasing the trap density. As a result, the 2DEG density saturates and remains unchanged by further increasing the trap density. For instance, for trap level at 215 meV, the 2DEG is almost constant for trap densities larger than 3×10^{13} cm^{-2}.

5.3.2 Estimation of Hole Trap Density and Energy Level at AlN/GaN NPI

As mentioned earlier, hole trap energy and density have not yet been measured for AlN/GaN NPIs. In this work, a set of samples with epi-structure shown in **Fig. 5.1(a)** with 4nm-thick AlN interlayer and GaN channel thicknesses of 7 nm, 10 nm, and 15 nm were grown via PAMBE on 5×5 mm^2 semi-insulating N-polar GaN substrates commercially available from NGK

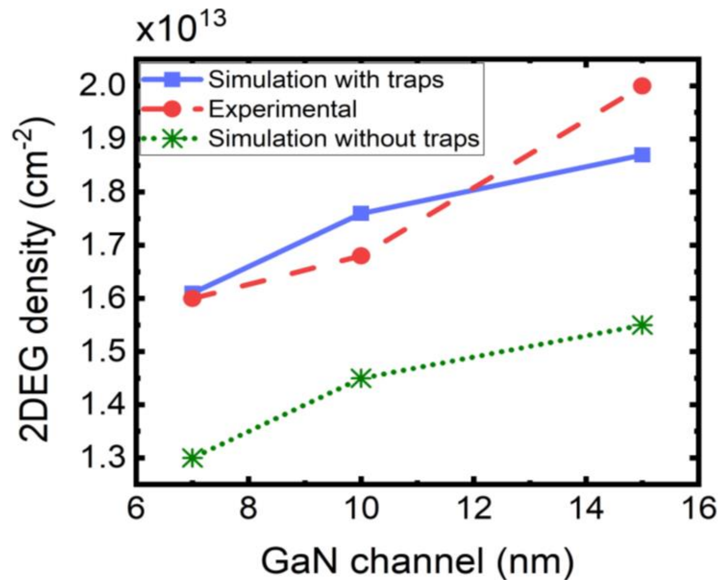


Figure 5.5 2DEG density as a function of GaN channel experimentally measured (red circles), simulated including hole traps with 0.3 eV barrier height, density and energy of 3×10^{13} cm^{-2} and 280 meV w.r.t. valence band (blue squares), and simulated without including traps (green stars).

insulators LTD. in a Veeco GenXplor MBE system. The details of growth conditions are explained elsewhere [24]. The 2DEG density was measured on these samples using Van der Pauw Hall measurements and is depicted in **Fig. 5.5**. The 2DEG density for these structures was simulated without including traps, which led to an underestimation of charge density in N-polar GaN HEMT structures as shown in **Fig. 5.5**. A barrier height of 0.3 eV was assumed on the N-polar GaN surface for all these calculations. Low barrier heights (0.3 eV and 0.15 eV) have been reported previously on the N-polar GaN surface [114]. We then included hole traps in the model and calculated the 2DEG density varying trap energy and trap density. A good agreement between experimental data and calculated values was reached assuming hole traps with a density and energy of 3×10^{13} cm^{-2} and 280 meV with respect to the valence band, respectively.

5.3.3 Si Doping to Prevent Hole Trap Ionization

As discussed above, hole traps are a significant source of electrons in N-polar GaN HEMT structures with large 2DEG densities. However, these hole traps are slow and cannot respond at high frequencies, and therefore are detrimental for device operations as they cause non-idealities such as current collapse and anomalous output conduction [16]. It is therefore crucial to supply enough electrons via Si doping in N-polar GaN HEMTs to push the hole traps down and far from the fermi level to prevent them from being ionized [103]. For this purpose, we have examined three sets of Si doping profiles.

In series-A, a 15 nm-thick Si-doped GaN layer was inserted below the back-barrier (**Fig 5.6(a)**). **Figures 5.6(b)** and **(c)** show the corresponding band structure for 2 nm-thick and 4 nm AlN interlayer, respectively, assuming hole traps with a density of 3×10^{13} cm^{-2} at 280 meV from the VB. As illustrated in **Fig. 5.6(b)**, in the structure with 2nm-thick AlN interlayer, a Si concentration of 8×10^{17} cm^{-3} is not sufficient to fully compensate the 2DEG charge to maintain

charge neutrality. Therefore, the VB remains very close to the fermi level which is still pinned to the hole trap at NPI-14. For a sufficiently high Si doping concentration (9×10^{18} cm^{-3}), all the traps are neutralized and VB moves away from the fermi level. Further increasing the Si doping concentration (1×10^{19} cm^{-3}) does not increase the 2DEG charge, rather it brings the conduction band closer to fermi level in the GaN buffer layer creating a parallel channel (**Fig. 5.6(c)**). As a

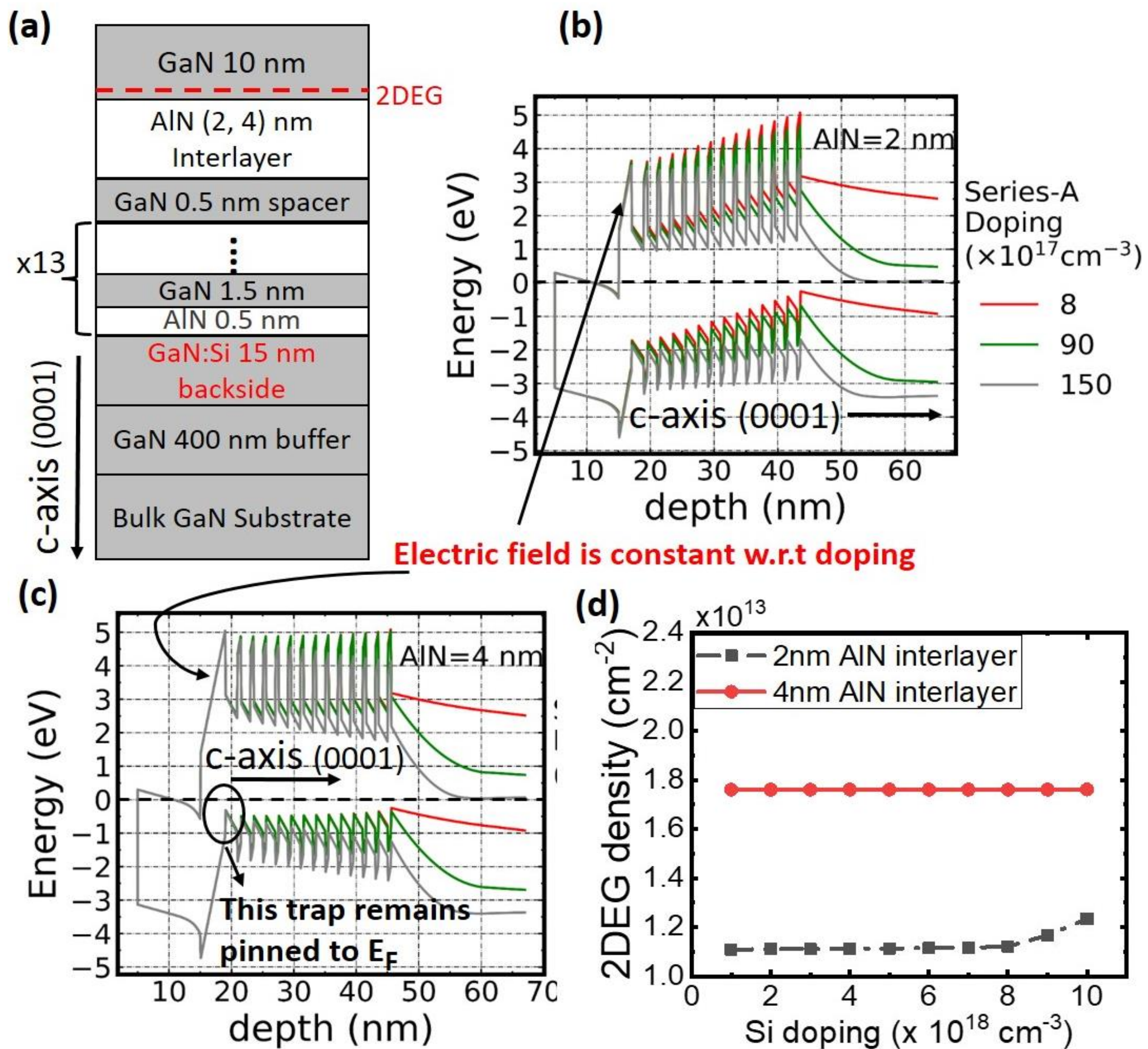


Figure 5.6 (a) Series-A: doping in 15 nm thick GaN at the interface between the digital-alloy barrier and buffer layer; corresponding band diagram for AlN interlayer thickness of (b) 2 nm, (c) 4 nm for various doping level at E_t = 280 meV with $N_t = 3\times10^{13}$ cm^{-2} **(d)** 2DEG density as a function of Si doping concentration.

result, the 2DEG density has little dependence on series-A delta doping as the electric field both in the GaN channel and AlN inter-layer remains constant (**Figs. 5.6(b)** and **(c)**) and it remains relatively constant for different doping concentrations (**Fig. 5.6(d)**). A similar trend was observed in the epi-structure with 4 nm-thick AlN interlayer. As opposed to the previous case, there is no optimum Si doping concentration to neutralize the traps at all the NPIs. The series-A delta doping has little effect on traps near the channel. The trap at NPI-1 cannot be compensated by this strategy even at extremely high doping concentrations which forms parasitic channel in the buffer. Therefore, the fermi-level remains pinned at trap-1 for all different Si doping concentrations, meaning this doping scheme is not suitable for thick AlN interlayer.

In series-B (**Fig. 5..7 (a)**), the entire AlN/GaN digital barrier was doped with Si. The corresponding band diagrams for hole traps at 280 meV with varying Si doping concentration are shown in **Fig. 5.7(b)** for a N-polar HEMT structure neutralizes most of the hole traps (NPI-1 to NPI-13) effectively except traps at NPI-14 which remains ionized even for very high doping concentrations. By increasing the Si doping beyond 5×10^{18} cm^{-3}, the trap at NPI-1 becomes neutralized allowing the VB to move down and away from the fermi level. Therefore, further increasing Si concentration reduces the electric field in the AlN interlayer and modulates the 2DEG

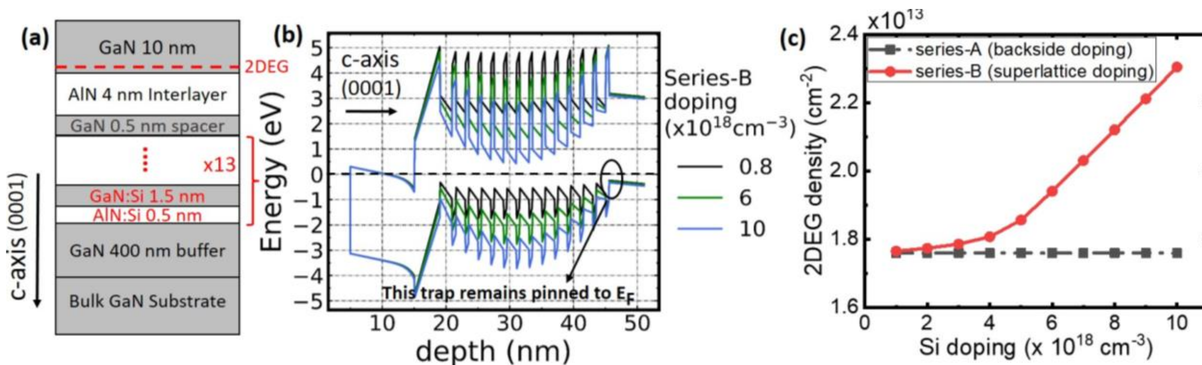


Figure 5.7 **(a)** Series-B: doping in digital-alloy barrier, **(b)** corresponding band diagram for 4 nm AlN interlayer with different doping density for E_t = 280 meV, N_t = 3×10^{13} cm^{-2} and **(c)** 2DEG density as a function of Si doping concentration in barrier (series-B) and at the back-barrier GaN buffer interface (series-A).

(**Fig. 5.7(c)**) unlike series-A doping where the 2DEG density was almost independent of doping. Moreover, as we increase the doping concentration in the barrier, the conduction band comes closer to the fermi level resulting in the formation of a parallel channel inside the barrier. This sets a limit to the doping level and hence the 2DEG density in the channel.with 4 nm-thick AlN interlayer. At low Si doping concentration, the hole traps remain ionized and the band diagram remains relatively unaltered, and therefore, the 2DEG density does not change. Increasing the Si doping concentration.

As discussed above, series-B doping scheme compensates traps at channel-barrier interface whereas series-A doping profile effectively compensates traps near barrier-buffer interface. Moreover, the barrier doping modulates 2DEG effectively, unlike series-A doping scheme where the 2DEG density was almost independent of doping concentration. Therefore, it is imperative to dope both barrier and the buffer (**Fig. 5.8(a)**: series-C doping scheme) in order to take advantage of both. As shown in **Fig. 5.7(b)**, a doping concentration of 4×10^{18} cm^{-3} can compensate the traps at NPIs in the middle of the barrier. However, it is not enough to compensate the traps at NPI-1 and NPI-14. A Si doping concentration of 6×10^{18} cm^{-3} is sufficient to neutralize all the traps. Increasing the doping further to 8×10^{18} cm^{-3} leads to formation of parallel channels in the barrier.

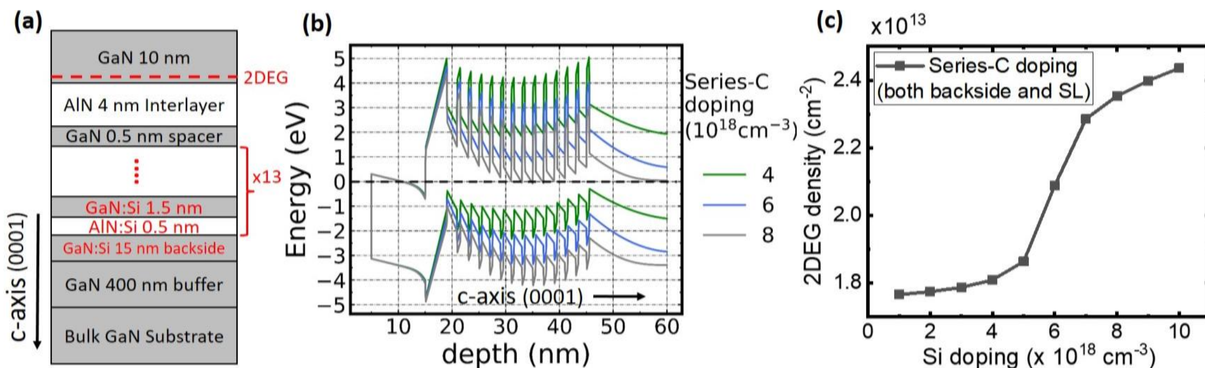


Figure 5.8 **(a)** Series C doping strategy: doping in both back-barrier and the buffer layers, **(b)** corresponding band diagram for 4 nm AlN interlayer with different doping density for E_t = 280 meV, $N_t = 3\times10^{13}$ cm^{-2} and **(c)** corresponding 2DEG variation with back-barrier doping.

This is not desirable for fabrication of HEMTs since the channel formed within the barrier has low electron mobility due to ionized impurity scattering. Therefore, the window for optimum doping concentrations seems to be extremely narrow using this Si doping scheme.

To increase the range of optimum Si doping concentrations in the barrier, we propose band engineering in which entire band diagram can be manipulated by controlling the thickness of each individual layers as shown in **Fig. 5.9(a) and 5.9(b)**. The aim of controlling the thickness of each layer in the barrier is to maintain the entire band diagram edges at one energy level unlike **Fig. 5.7(b) and 5.8(b)**. The conduction band at barrier-buffer interface is decided by the series-A delta doping in 15nm thickness at that interface. From **Fig. 5.7(b) or 5.8(b)**, the conduction band needs to be moved up to avoid parallel channel as it is too close to fermi level. Since GaN layers have negative electric field inside, increasing GaN thickness at the bottom of the barrier will move the conduction band away from fermi level. In a similar manner, the band edge and conduction band

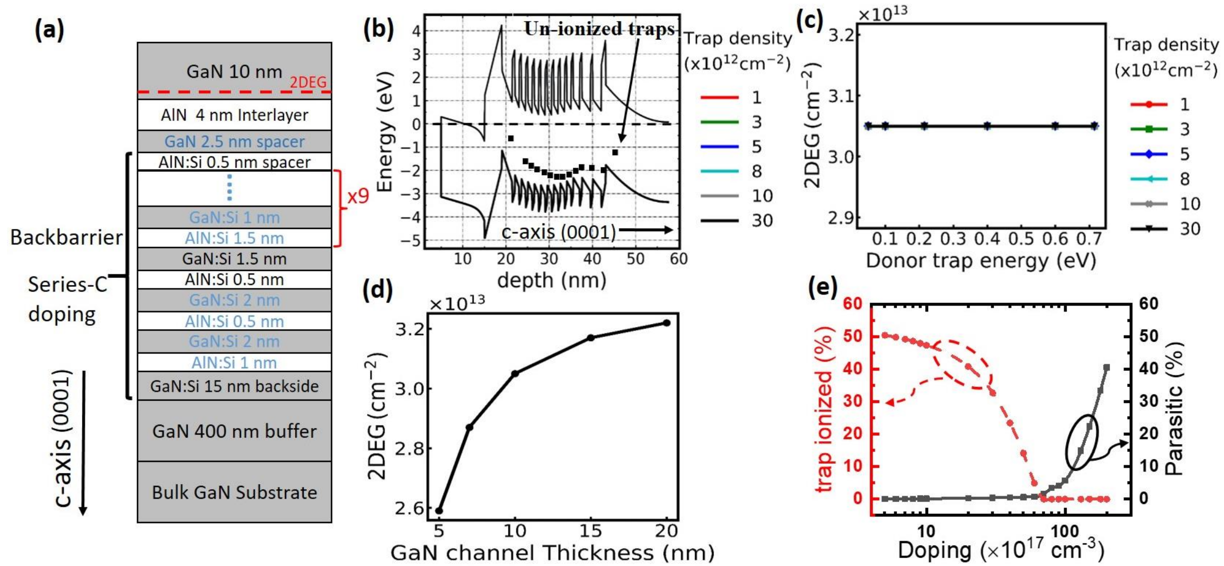


Figure 5.9 (a) Optimized epi-structure with Series-C doping, blue colour shows changed thickness of layers from structure in Fig. 4.1(a). (b) band diagram, (c) 2DEG is independent of trap density and energy over a wide range since all the traps are neutralized by Si doping, (d) 2DEG vs GaN channel thickness for the optimized design series-C doping of $8{\times}10^{18}$ cm^{-3}, N_t = $3{\times}10^{13}$ cm^{-2} at E_t = 280 meV, (e) A wide range of doping ($6{\times}10^{18}$ cm^{-3}-$1{\times}10^{19}$ cm^{-3}) shows lower parasitic and zero trap ionization.

inside AlN interlayer is almost fixed by the 2DEG density since even small change in band banding in channel can result in large change in 2DEG charge. From **Fig 5.7(b) or 5.8(b)**, it is apparent to bring the conduction band closer to the fermi level which is achieved by increasing thickness of AlN and reducing thickness of GaN layers in the barrier around that area due to the positive and negative electric field inside AlN and GaN respectively. This helps to achieve almost uniform band structure in the barrier while reducing the formation of parasitic channels and allowing to increase 2DEG density by increasing the doping level (**Figs. 5.9 (b)** and **(c)**). As a result, a wide range of doping from 6×10^{18} cm^{-3} (MBE Si cell temperature 1167 $^{\circ}C$) to 1×10^{19} cm^{-3} (MBE Si cell temperature 1185 $^{\circ}C$) can be employed to keep both trap ionization and parasitic channel charges below 5% as illustrated in **Fig. 5.9(e)**. As shown in **Fig. 5.9(d)**, this optimized design of epi-structure enables maintaining a very large 2DEG density (~3×10^{13} cm^{-2}) in N-polar GaN HEMT with ultra-scaled 5 nm-thick channel.

5.4 Conclusion

In summary, we studied the impact of hole traps on 2DEG density in N-polar GaN HEMT structures. We showed that excluding hole traps when calculating 2DEG density results in an underestimation of charge density in these heterostructures. Comparing simulation results with experimental data, we estimated a hole trap with a density of 3×10^{13} cm^{-2} at 280 meV above the valence band at AlN/GaN NPIs. To prevent these hole traps from ionization, we proposed and studied three different doping schemes. The results showed that Si doping in both the barrier and at barrier-buffer interface effectively neutralizes the traps present throughout the epi-structure while simultaneously modulating the 2DEG charge density. Moreover, an epi-structure was proposed to enable aggressive scaling of the channel (5nm-thick) in N-polar GaN HEMTs while maintaining a large 2DEG density of approximately 2.6×10^{13} cm^{-2}.

Chapter 6
Future Work

6.1 N-polar Deep Recessed HEMT with $HfZrO_2$ as gate dielectric

Recently, negative capacitance has been demonstrated by multi-layer HfO_2 and ZrO_2 on Si with an ultra-thin SiO_2 interlayer Figure. 6.1 (a) [115]. Simultaneous existence of lateral polar (orthorhombic FE) and non-polar film (tetragonal AFE) thin film system flattens the energy vs polarization landscape which increases permittivity of the overall system which is known as negative capacitance. This negative capacitance has shown enhancement in gate capacitance with lowering the effective oxide thickness (EOT). Moreover, it presents with an advantage of one order lower leakage current. This gate dielectric

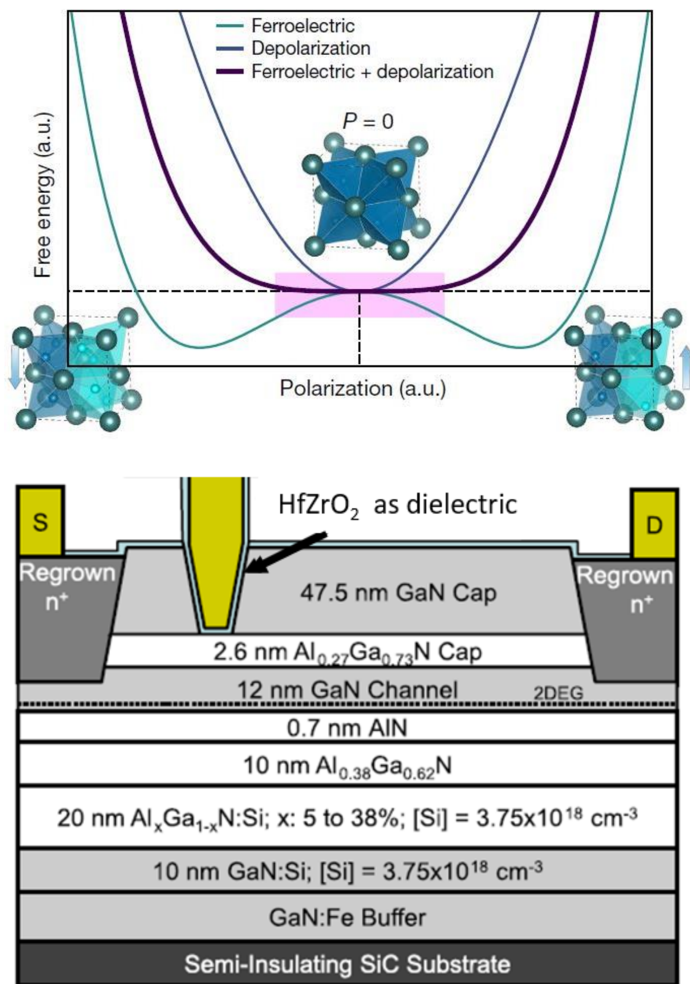


Figure 6.1 (a) Energy vs polarization diagram for ferroelectric, non-ferroelectric and subsequent negative capacitance from combined (ferroelectric+non-ferroelectric) material [115] (b) Device cross-sectional schematic and epitaxial layer profile of the N-polar deep recess (NPDR) with $HfZrO_2$ as gate dielectric

stack can be explored to achieve capacitance enhancement, lower leakage and extremely thin EOT for GaN material system to address ultra-thin GaN HEMT for gate (frequency) scaling. The proposed device structure is shown in Figure. 6.1 (b).

6.2 Improvement in HfO_2 leakage:

The high leakage in HfO_2 prevented the device in achieving full potential such as in load-pull measurements. The leakage and breakdown characteristics of ALD HfO_2 needs further investigation. Inserting a thin layer of SiN or Al_2O_3 on AlGaN could further improve the interface and potentially reduce the gate leakage. Doping HfO_2 with Silicon to increase the crystallization temperature needs to be investigated as well. Even though the HfO_2 was developed for GaN, the actual application is on AlGaN surface. We believe that the Hf interacts with Aluminum in AlGaN to create an intermixing layer which needs to be investigated. $(NH_4)_2S$ is widely used in GaAS HEMT fabrication to passivate GaAs surface which can be also explored to passivate GaN surface before dielectric deposition.

6.3 Regrown Ohmic contact improvement:

Resistances especially ohmic source/drain contact resistance are critical parameter for both DC and RF characteristics of HEMTs. The contact resistance was 0.1ohm-mm for planar HEMT which increased to ~0.3 ohm-mm for deep-recess HEMT. This could be due to the introduction of additional BCl_3/SF_6 selective dry etch which creates roughness on etch stop layer. The etch is well optimized for sub-micron features, however, etch rate is much slower and non-uniform for large features which creates roughness. The dry etch parameters especially gas ratio needs to be studied for large features to create a smooth surface.

6.4 Scaled HEMTs for high frequency application:

The HEMTs discussed in the thesis consists of optical gates with 500-700 nm dimensions. However, to further increase the operating frequency, the gate length needs to be scaled down

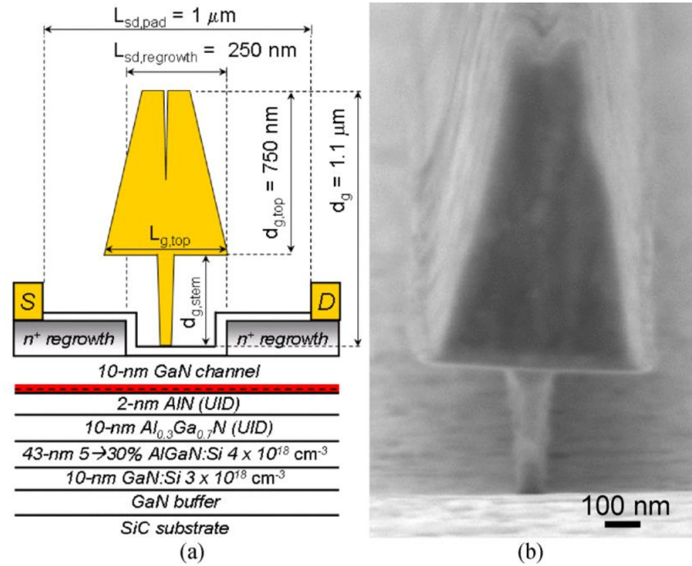


Figure 6.2 (a) Device cross-sectional schematic and (b) SEM image of high aspect ration N-polar deep recess (NPDR) HEMT with T-gate [117]

below 100 nm. Ebeam T-gates are typically used in RF HEMTs to achieve high fT while reducing Rg with large gate top to achieve high fmax as shown in Figure 6.2. Tall T-gates are necessary to minimize the fringe capacitance from the wide gate top to gate and drain.

Bibliography

[1] Shinohara K, Regan D, Corrion A, Brown D, Cunningham M, Butler C, Schmitz A, Kim S, Holden B, Chang D, Margomenos A and Micovic M 2012 Deeply-Scaled E / D-Mode GaN-HEMTs for Sub-mm- Wave Amplifiers and Mixed-Signal Applications 17–20

[2] Tasker P J and Hughes B 1989 Importance of Source and Drain Resistance to the Maximum fT of Millimeter-Wave MODFET's *IEEE Electron Device Lett.* **10** 291–3

[3] Schwierz F and Liou J J 2002 *Modern Microwave Transistors: Theory, Design, and Performance* (Wiley)

[4] Ahmadi E 2015 *Growth Optimization of III-N Electronic Devices by Plasma-Assisted Molecular Beam Epitaxy* (University of California Santa Barbara)

[5] Inoue A 2021 Millimeter-Wave GaN Devices for 5G: Massive MIMO Antenna Arrays for Sub-6-Ghz and mm-Wave Bandwidth *IEEE Microw. Mag.* **22** 100–10

[6] Benson K 2017 GaN Breaks Barriers — RF Power Amplifiers Go Wide and High *Analog Dialogue* 1–3

[7] Kemerley R T, Wallace H B and Yoder M N 2002 Impact of wide bandgap microwave devices on DoD systems *Proc. IEEE* **90** 1059–64

[8] Anon Lecture 6. GaN-devices

[9] Ma R, Teo K H, Shinjo S, Yamanaka K and Asbeck P M 2017 A GaN PA for 4G LTE-Advanced and 5G: Meeting the Telecommunication Needs of Various Vertical Sectors Including Automobiles, Robotics, Health Care, Factory Automation, Agriculture,

Education, and More *IEEE Microw. Mag.* **18** 77–85

[10] DenBaars S P, Feezell D, Kelchner K, Pimputkar S, Pan C-C, Yen C-C, Tanaka S, Zhao Y, Pfaff N, Farrell R, Iza M, Keller S, Mishra U, Speck J S and Nakamura S 2013 Development of gallium-nitride-based light-emitting diodes (LEDs) and laser diodes for energy-efficient lighting and displays *Acta Mater.* **61** 945–51

[11] Neufeld C J, Toledo N G, Cruz S C, Iza M, DenBaars S P and Mishra U K 2008 High quantum efficiency InGaN/GaN solar cells with 2.95 eV band gap *Appl. Phys. Lett.* **93** 143502

[12] Cho Y-H, Gainer G H, Fischer A J, Song J J, Keller S, Mishra U K and DenBaars S P 1998 "S-shaped" temperature-dependent emission shift and carrier dynamics in InGaN/GaN multiple quantum wells *Appl. Phys. Lett.* **73** 1370–2

[13] Nakamura S, Senoh M, Iwasa N and Nagahama S 1995 High-Brightness InGaN Blue, Green and Yellow Light-Emitting Diodes with Quantum Well Structures *Jpn. J. Appl. Phys.* **34** L797–9

[14] Vampola K J, Iza M, Keller S, DenBaars S P and Nakamura S 2009 Measurement of electron overflow in 450 nm InGaN light-emitting diode structures *Appl. Phys. Lett.* **94** 061116

[15] Narukawa Y, Sano M, Sakamoto T, Yamada T and Mukai T 2008 Successful fabrication of white light emitting diodes by using extremely high external quantum efficiency blue chips *Phys. status solidi* **205** 1081–5

[16] Pimputkar S, Speck J S, DenBaars S P and Nakamura S 2009 Prospects for LED lighting *Nat. Photonics* **3** 180–2

[17] Wong M H, Keller S, Dasgupta N S, Denninghoff D J, Kolluri S, Brown D F, Lu J,

Fichtenbaum N A, Ahmadi E, Singisetti U, Chini A, Rajan S, DenBaars S P, Speck J S and Mishra U K 2013 N-polar GaN epitaxy and high electron mobility transistors *Semicond. Sci. Technol.* **28** 074009

[18] Park P S and Rajan S 2011 Simulation of Short-Channel Effects in N- and Ga-Polar AlGaN/GaN HEMTs *IEEE Trans. Electron Devices* **58** 704–8

[19] Guerra D, Saraniti M, Faralli N, Ferry D K, Goodnick S M and Marino F A 2010 Comparison of N- and Ga-Face GaN HEMTs Through Cellular Monte Carlo Simulations *IEEE Trans. Electron Devices* **57** 3348–54

[20] Breitschädel O, Kley L, Gräbeldinger H, Hsieh J ., Kuhn B, Scholz F and Schweizer H 2001 Short-channel effects in AlGAN/GaN HEMTs *Mater. Sci. Eng. B* **82** 238–40

[21] Endoh A, Yamashita Y, Ikeda K, Higashiwaki M, Hikosaka K, Matsui T, Hiyamizu S and Mimura1 T 2003 Fabrication of sub-50-nm-gate i-AlGaN/GaN HEMTs on sapphire *Phys. status solidi* **2371** 2368–71

[22] Jessen G H, Fitch R C, Gillespie J K, Via G, Crespo A, Langley D, Denninghoff D J, Trejo M and Heller E R 2007 Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices *IEEE Trans. Electron Devices* **54** 2589–97

[23] Mohanty S, Diez S, Jian Z (Ashley) and Ahmadi E 2020 Design of ultra-scaled-channel N-polar GaN HEMTs with high charge density: A systematic study of hole traps and their impact on charge density in the channel *J. Appl. Phys.* **128** 235701

[24] Diez S, Mohanty S, Kurdak C and Ahmadi E 2020 Record high electron mobility and low sheet resistance on scaled-channel N-polar GaN/AlN heterostructures grown on on-axis N-polar GaN substrates by plasma-assisted molecular beam epitaxy *Appl. Phys. Lett.* **117** 042102

[25] Ambacher O, Smart J, Shealy J R, Weimann N G, Chu K, Murphy M, Schaff W J, Eastman L F, Dimitrov R, Wittmer L, Stutzmann M, Rieger W and Hilsenbeck J 1999 Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures *J. Appl. Phys.* **85** 3222

[26] Brown D F 2010 *Growth of N-polar GaN-based Materials and High Electron Mobility Transistors by Metal Organic Chemical Vapor Deposition* (University of California, Santa Barbara)

[27] Lu J, Denninghoff D, Yeluri R, Lal S, Gupta G, Laurent M, Keller S, Denbaars S P and Mishra U K 2013 Very high channel conductivity in ultra-thin channel N-polar GaN/(AlN, InAlN, AlGaN) high electron mobility hetero-junctions grown by metalorganic chemical vapor deposition *Appl. Phys. Lett.* **102**

[28] Dasgupta S, Nidhi, Brown D F, Wu F, Keller S, Speck J S and Mishra U K 2010 Ultralow nonalloyed Ohmic contact resistance to self aligned N-polar GaN high electron mobility transistors by In(Ga)N regrowth *Appl. Phys. Lett.* **96** 143504

[29] Denninghoff D, Lu J, Ahmadi E, Keller S and Mishra U K 2013 N-polar GaN/InAlN/AlGaN MIS-HEMTs with 1.89 S/mm extrinsic transconductance, 4 A/mm drain current, 204 GHz fT and 405 GHz f max *Device Res. Conf. - Conf. Dig. DRC* **33** 197–8

[30] Romanczyk B, Zheng X, Guidry M, Li H, Hatui N, Wurm C, Krishna A, Ahmadi E, Keller S and Mishra U K 2020 W-Band Power Performance of SiN-Passivated N-Polar GaN Deep Recess HEMTs *IEEE Electron Device Lett.* **41** 349–52

[31] Steven M. Wienecke *PhD Dissertation, N-Polar Deep Recess MISHEMTs for mm-Wave Applications* (University of California, Santa Barbara)

[32] Wienecke S, Romanczyk B, Guidry M, Li H, Zheng X, Ahmadi E, Hestroffer K, Megalini L, Keller S and Mishra U K 2016 N-Polar Deep Recess MISHEMTs with Record 2.9 W/mm at 94 GHz *IEEE Electron Device Lett.* 1–1

[33] Moon J S, Wong D, Hu M, Hashimoto P, Antcliffe M, McGuire C, Micovic M and Willadson P 2008 55% PAE and High Power Ka-Band GaN HEMTs With Linearized Transconductance via n+ GaN Source Contact Ledge *IEEE Electron Device Lett.* **29** 834–7

[34] Palacios T, Chakraborty A, Rajan S, Poblenz C, Keller S, DenBaars S P, Speck J S and Mishra U K 2005 High-power AlGaN/GaN HEMTs for Ka-band applications *IEEE Electron Device Lett.* **26** 781–3

[35] Micovic M, Brown D F, Regan D, Wong J, Tang Y, Herrault F, Santos D, Burnham S D, Tai J, Prophet E, Khalaf I, McGuire C, Bracamontes H, Fung H, Kurdoghlian A K and Schmitz A 2016 High frequency GaN HEMTs for RF MMIC applications *2016 IEEE International Electron Devices Meeting (IEDM)* pp 3.3.1-3.3.4

[36] Margomenos A, Kurdoghlian A, Micovic M, Shinohara K, Brown D F, Corrion A L, Moyer H P, Burnham S, Regan D C, Grabar R M, McGuire C, Wetzel M D, Bowen R, Chen P S, Tai H Y, Schmitz A, Fung H, Fung A and Chow D H 2014 GaN Technology for E, W and G-Band Applications *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)* pp 1–4

[37] Brown D F, Williams A, Shinohara K, Kurdoghlian A, Milosavljevic I, Hashimoto P, Grabar R, Burnham S, Butler C, Willadsen P and Micovic M 2011 W-band power performance of AlGaN/GaN DHFETs with regrown n+ GaN ohmic contacts by MBE *2011 International Electron Devices Meeting* pp 19.3.1-19.3.4

[38] Niida Y, Kamada Y, Ohki T, Ozaki S, Makiyama K, Minoura Y, Okamoto N, Sato M, Joshin K and Watanabe K 2016 3.6 W/mm high power density W-band InAlGaN/GaN HEMT MMIC power amplifier *2016 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)* (IEEE) pp 24–6

[39] Romanczyk B, Wienecke S, Guidry M, Li H, Ahmadi E, Zheng X, Keller S and Mishra U K 2018 Demonstration of Constant 8 W/mm Power Density at 10, 30, and 94 GHz in State-of-the-Art Millimeter-Wave N-Polar GaN MISHEMTs *IEEE Trans. Electron Devices* **65** 45–50

[40] Lee M H, Wei Y-T, Chu K-Y, Huang J-J, Chen C-W, Cheng C-C, Chen M-J, Lee H-Y, Chen Y-S, Lee L-H and Tsai M-J 2015 Steep Slope and Near Non-Hysteresis of FETs With Antiferroelectric-Like HfZrO for Low-Power Electronics *IEEE Electron Device Lett.* **36** 294–6

[41] Chiu H-C, Wu C-H, Chi J-F and Chien F-T 2014 Device characteristics of AlGaN/GaN MIS–HEMTs with high-k HfxZr1−xO2 (x = 0.66, 0.47, 0.15) insulator layer *Microelectron. Reliab.* **54** 1282–7

[42] Saadat O I, Chung J W, Piner E L and Palacios T 2009 Gate-First AlGaN/GaN HEMT Technology for High-Frequency Applications *IEEE Electron Device Lett.* **30** 1254–6

[43] Abermann S, Pozzovivo G, Kuzmik J, Strasser G, Pogany D, Carlin J-F, Grandjean N and Bertagnolli E 2007 MOCVD of HfO_2 and ZrO_2 high- *k* gate dielectrics for InAlN/AlN/GaN MOS-HEMTs *Semicond. Sci. Technol.* **22** 1272–5

[44] Liu C, Chor E F and Tan L S 2007 Enhanced device performance of AlGaN/GaN HEMTs using HfO_2 high- *k* dielectric for surface passivation and gate oxide *Semicond. Sci. Technol.* **22** 522–7

[45] Hatano M, Taniguchi Y, Kodama S, Tokuda H and Kuzuhara M 2014 Reduced gate leakage and high thermal stability of AlGaN/GaN MIS-HEMTs using ZrO_2/Al_2O_3 gate dielectric stack *Appl. Phys. Express* **7** 044101

[46] Ye G, Wang H, Arulkumaran S, Ng G I, Hofstetter R, Li Y, Anand M J, Ang K S, Maung Y K T and Foo S C 2013 Atomic layer deposition of ZrO2 as gate dielectrics for AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors on silicon *Appl. Phys. Lett.* **103** 142109

[47] Balachander K, Arulkumaran S, Ishikawa H, Baskar K and Egawa T 2005 Studies on electron beam evaporated ZrO_2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors *Phys. status solidi* **202** R16–8

[48] Kuzmik J, Pozzovivo G, Abermann S, Carlin J-F, Gonschorek M, Feltin E, Grandjean N, Bertagnolli E, Strasser G and Pogany D 2008 Technology and Performance of InAlN/AlN/GaN HEMTs With Gate Insulation and Current Collapse Suppression Using Zr$\hbox{O}_{\bm 2}$ or Hf $\hbox{O}_{\bm 2}$ *IEEE Trans. Electron Devices* **55** 937–41

[49] Seok O, Ahn W, Han M-K and Ha M-W 2013 High on/off current ratio AlGaN/GaN MOS-HEMTs employing RF-sputtered HfO2 gate insulators *Semicond. Sci. Technol.* **28** 025001

[50] Sugiura S, Kishimoto S, Mizutani T, Kuroda M, Ueda T and Tanaka T 2008 Normally-off AlGaN/GaN MOSHFETs with HfO2 gate oxide *Phys. status solidi* **5** 1923–5

[51] Yue Y, Hao Y, Zhang J, Ni J, Mao W, Feng Q and Liu L 2008 AlGaN/GaN MOS-HEMT With $\hbox{HfO}_{2}$ Dielectric and $\hbox{Al}_{2}\hbox{O}_{3}$ Interfacial Passivation Layer Grown by Atomic Layer Deposition *IEEE Electron Device Lett.* **29** 838–40

[52] Choi W, Seok O, Ryu H, Cha H-Y and Seo K-S 2014 High-Voltage and Low-Leakage-Current Gate Recessed Normally-Off GaN MIS-HEMTs With Dual Gate Insulator Employing PEALD-SiNx RF-Sputtered-HfO2 *IEEE Electron Device Lett.* **35** 175–7

[53] Chen C-H, Chiu H-C, Chien F-T, Chuang H-W, Chang K-J and Gau Y-T 2012 High thermal stability and low hysteresis dispersion AlGaN/GaN MOS-HEMTs with zirconia film design *Microelectron. Reliab.* **52** 2551–5

[54] Stoklas R, Gregušová D, Hasenöhrl S, Brytavskyi E, Ťapajna M, Fröhlich K, Haščík, Gregor M and Kuzmík J 2018 Characterization of interface states in AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors with HfO 2 gate dielectric grown by atomic layer deposition *Appl. Surf. Sci.* **461** 255–9

[55] Jung W S, Lim D, Han H, Sokolov A S, Jeon Y R and Choi C 2018 Influence of in-situ NH3 plasma passivation on the electrical characteristics of Ga-face n-GaN MOS capacitor with atomic layer deposited HfO2 *Solid. State. Electron.* **149** 52–6

[56] Chang Y C, Huang M L, Chang Y H, Lee Y J, Chiu H C, Kwo J and Hong M 2011 Atomic-layer-deposited Al2O3 and HfO2 on GaN: A comparative study on interfaces and electrical characteristics *Microelectron. Eng.* **88** 1207–10

[57] Yeluri R, Swenson B L and Mishra U K 2012 Interface states at the SiN/AlGaN interface on GaN heterojunctions for Ga and N-polar material *J. Appl. Phys.* **111** 1–6

[58] Sayed I, Bonef B, Liu W, Chan S, Georgieva J, Speck J S, Keller S and Mishra U K 2019 Electrical properties and interface abruptness of AlSiO gate dielectric grown on 000 1¯N-polar and (0001) Ga-polar GaN *Appl. Phys. Lett.* **115** 0–4

[59] Yang J, Eller B S and Nemanich R J 2014 Surface band bending and band alignment of plasma enhanced atomic layer deposited dielectrics on Ga- and N-face gallium nitride *J.*

Appl. Phys. **116** 123702

[60] Meyer D J, Katzer D S, Deen D A, Storm D F, Binari S C and Gougousi T 2011 HfO2-insulated gate N-polar GaN HEMTs with high breakdown voltage *Phys. status solidi* **208** 1630–3

[61] Hashizume T, Alekseev E, Pavlidis D, Boutros K S and Redwing J 2000 Capacitance–voltage characterization of AlN/GaN metal–insulator–semiconductor structures grown on sapphire substrate by metalorganic chemical vapor deposition *J. Appl. Phys.* **88** 1983–6

[62] Swenson B L and Mishra U K 2009 Photoassisted high-frequency capacitance-voltage characterization of the Si3N4/GaN interface *J. Appl. Phys.* **106** 064902

[63] Yeluri R, Liu X, Swenson B L, Lu J, Keller S and Mishra U K 2013 Capacitance-voltage characterization of interfaces between positive valence band offset dielectrics and wide bandgap semiconductors *J. Appl. Phys.* **114** 083718

[64] Liu W, Sayed I, Georgieva J, Chan S, Keller S and Mishra U K 2020 A systematic and quantitative analysis of the bulk and interfacial properties of the AlSiO dielectric on N-polar GaN using capacitance–voltage methods *J. Appl. Phys.* **128** 074101

[65] Liu W, Sayed I, Gupta C, Li H, Keller S and Mishra U 2020 An improved methodology for extracting interface state density at Si3N4/GaN *Appl. Phys. Lett.* **116** 1–6

[66] Lu J, Denninghoff D, Yeluri R, Lal S, Gupta G, Laurent M, Keller S, DenBaars S P and Mishra U K 2013 Very high channel conductivity in ultra-thin channel N-polar GaN/(AlN, InAlN, AlGaN) high electron mobility hetero-junctions grown by metalorganic chemical vapor deposition *Appl. Phys. Lett.* **102** 232104

[67] Lu J, Zheng X, Guidry M, Denninghoff D, Ahmadi E, Lal S, Keller S, Denbaars S P and Mishra U K 2014 Engineering the (In, Al, Ga)N back-barrier to achieve high channel-

conductivity for extremely scaled channel-thicknesses in N-polar GaN high-electron-mobility-transistors *Appl. Phys. Lett.* **104** 092107

[68] Romanczyk B, Wienecke S, Guidry M, Li H, Hestroffer K, Ahmadi E, Zheng X, Keller S and Mishra U K 2016 mm-Wave N-polar GaN MISHEMT with a self-aligned recessed gate exhibiting record 4.2 W/mm at 94 GHz on Sapphire *2016 74th Annual Device Research Conference (DRC)* (IEEE) pp 1–2

[69] Zheng X, Guidry M, Li H, Romanczyk B, Ahmadi E, Hestroffer K, Wienecke S, Keller S and Mishra U K 2017 N-polar GaN MIS-HEMTs on sapphire with a proposed figure of merit fmax·V *2017 75th Annual Device Research Conference (DRC)* (IEEE) pp 1–2

[70] Brown D F, Rajan S, Keller S, Hsieh Y-H, DenBaars S P and Mishra U K 2008 Electron mobility in N-polar GaN/AlGaN/GaN heterostructuress *Appl. Phys. Lett.* **93** 042104

[71] Zheng X, Li H, Ahmadi E, Hestroffer K, Guidry M, Romanczyk B, Wienecke S, Keller S and Mishra U K 2016 High frequency N-polar GaN planar MIS-HEMTs on sapphire with high breakdown and low dispersion *2016 Lester Eastman Conference (LEC)* (IEEE) pp 42–5

[72] Zheng X, Li H, Guidry M, Romanczyk B, Ahmadi E, Hestroffer K, Wienecke S, Keller S and Mishra U K 2018 Analysis of MOCVD SiNx Passivated N-Polar GaN MIS-HEMTs on Sapphire With High f_max.V_DS,Q$ *IEEE Electron Device Lett.* **39** 409–12

[73] Romanczyk B, Guidry M, Wienecke S, Li H, Ahmadi E, Zheng X, Keller S and Mishra U K 2016 W-band N-polar GaN MISHEMTs with high power and record 27.8% efficiency at 94 GHz *2016 IEEE International Electron Devices Meeting (IEDM)* (IEEE) pp 3.5.1-3.5.4

[74] Zhang X-Y, Hsu C-H, Lien S-Y, Wu W-Y, Ou S-L, Chen S-Y, Huang W, Zhu W-Z, Xiong F-B and Zhang S 2019 Temperature-Dependent HfO2/Si Interface Structural Evolution and

its Mechanism *Nanoscale Res. Lett.* **14** 83

[75] Lin Y-S, Puthenkovilakam R and Chang J P 2002 Dielectric property and thermal stability of HfO2 on silicon *Appl. Phys. Lett.* **81** 2041–3

[76] Guerra D, Akis R, Marino F A, Ferry D K, Goodnick S M and Saraniti M 2010 Aspect Ratio Impact on RF and DC Performance of State-of-the-Art Short-Channel GaN and InGaAs HEMTs *IEEE Electron Device Lett.* **31** 1217–9

[77] Liu X, Yeluri R, Kim J, Lal S, Raman A, Lund C, Wienecke S, Lu J, Laurent M, Keller S and Mishra U K 2013 In-situ metalorganic chemical vapor deposition and capacitance-voltage characterizations of Al 2 O 3 on Ga-face GaN metal-oxide-semiconductor capacitors *Appl. Phys. Lett.* **103** 053509

[78] Roy S, N. Alem, A. Bhattacharyya, A. Chmielewski, S. Krishnamoorthy, P. Ranga, M. Scarpulla R S 2021 Growth and Characterization of In Situ MOCVD-Grown Al2O3 Dielectric / (010) β-Ga2O3 Interface *Electron. Mater. Conf.*

[79] Son J, Chobpattana V, McSkimming B M and Stemmer S 2015 In-situ nitrogen plasma passivation of Al 2 O 3 /GaN interface states *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.* **33** 020602

[80] Chobpattana V, Mates T E, Mitchell W J, Zhang J Y and Stemmer S 2013 Influence of plasma-based in-situ surface cleaning procedures on HfO 2 /In 0.53 Ga 0.47 As gate stack properties *J. Appl. Phys.* **114** 154108

[81] Chobpattana V, Son J, Law J J M, Engel-Herbert R, Huang C-Y and Stemmer S 2013 Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities *Appl. Phys. Lett.* **102** 022907

[82] Clymore C J, Mohanty S, Jian Z A, Krishna A, Keller S and Ahmadi E 2021 HfO 2 as gate

insulator on N-polar GaN-AlGaN heterostructures *Semicond. Sci. Technol.*

[83] Tse K, Liu D, Xiong K and Robertson J 2007 Oxygen vacancies in high-k oxides *Microelectron. Eng.* **84** 2028–31

[84] Clark S J, Lin L and Robertson J 2011 On the identification of the oxygen vacancy in HfO2 *Microelectron. Eng.* **88** 1464–6

[85] Uenuma M, Takahashi K, Sonehara S, Tominaga Y, Fujimoto Y, Ishikawa Y and Uraoka Y 2018 Influence of carbon impurities and oxygen vacancies in Al2O3 film on Al2O3/GaN MOS capacitor characteristics *AIP Adv.* **8**

[86] Perevalov T V., Tereshenko O E, Gritsenko V A, Pustovarov V A, Yelisseyev A P, Park C, Han J H and Lee C 2010 Oxygen deficiency defects in amorphous Al2O3 *J. Appl. Phys.* **108**

[87] Jian Z, Mohanty S and Ahmadi E 2020 Deep UV-assisted capacitance-voltage characterization of post-deposition annealed Al2O3/ β -Ga2O3(001) MOSCAPs *Appl. Phys. Lett.* **116** 1–6

[88] Zhang Z, Cao R, Wang C, Li H-B, Dong H, Wang W, Lu F, Cheng Y, Xie X, Liu H, Cho K, Wallace R and Wang W 2015 GaN as an Interfacial Passivation Layer: Tuning Band Offset and Removing Fermi Level Pinning for III–V MOS Devices *ACS Appl. Mater. Interfaces* **7** 5141–9

[89] Gupta C, Chan S H, Pasayat S S, Keller S and Mishra U K 2019 Reverse breakdown studies of GaN MOSCAPs and their implications in vertical GaN power devices *J. Appl. Phys.* **125** 124101

[90] Kim K, Ryu J H, Kim J, Cho S J, Liu D, Park J, Lee I K, Moody B, Zhou W, Albrecht J and Ma Z 2017 Band-Bending of Ga-Polar GaN Interfaced with Al2O3 through

Ultraviolet/Ozone Treatment *ACS Appl. Mater. Interfaces* **9** 17576–85

[91] Tingting Y, Xinyu L, Yingkui Z, Chengzhan L, Ke W and Guoguo L 2009 Impact of UV/ozone surface treatment on AlGaN/GaN HEMTs *J. Semicond.* **30** 124001

[92] Sayed I, Liu W, Romanczyk B, Georgieva J, Chan S, Keller S and Mishra U K 2020 Improved operation stability of in situ AlSiO dielectric grown on (000-1) N-polar GaN by MOCVD *Appl. Phys. Express* **13**

[93] Mohanty S, Sayed I, Jian Z (Ashley), Mishra U and Ahmadi E 2021 Investigation and optimization of HfO2 gate dielectric on N-polar GaN: Impact of surface treatments, deposition, and annealing conditions *Appl. Phys. Lett.* **119** 042901

[94] Keller S, Li H, Laurent M, Hu Y, Pfaff N, Lu J, Brown D F, Fichtenbaum N A, Speck J S, DenBaars S P and Mishra U K 2014 Recent progress in metal-organic chemical vapor deposition of $\left(000\bar{1} \right)$ N-polar group-III nitrides *Semicond. Sci. Technol.* **29** 113001

[95] Bisi D, Romanczyk B, Liu X, Gupta G, Brown-Heft T, Birkhahn R, Lal R, Neufeld C J, Keller S, Parikh P, Mishra U K and McCarthy L 2021 Commercially Available N-polar GaN HEMT Epitaxy for RF Applications *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)* (IEEE) pp 250–4

[96] Kuzmik J, Javorka R, Alam A, Marso M, Heuken M and Kordos P 2002 Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method *IEEE Trans. Electron Devices* **49** 1496–8

[97] Vetury R, Zhang N Q, Keller S and Misha U K 2001 The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs *IEEE Trans. Electron Devices* **48** 560–6

[98] Bahl S R and del Alamo J A 1993 A new drain-current injection technique for the

measurement of off-state breakdown voltage in FETs *IEEE Trans. Electron Devices* **40** 1558–60

[99] Liu W, Romanczyk B, Guidry M, Hatui N, Wurm C, Li W, Shrestha P, Zheng X, Keller S and Mishra U K 2021 6.2 W/Mm and Record 33.8% PAE at 94 GHz from N-Polar GaN Deep Recess MIS-HEMTs with ALD Ru Gates *IEEE Microw. Wirel. Components Lett.* **31** 748–51

[100] Ibbetson J P, Fini P T, Ness K D, DenBaars S P, Speck J S and Mishra U K 2000 Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors *Appl. Phys. Lett.* **77** 250–2

[101] Ahmadi E, Wu F, Li H, Kaun S W, Tahhan M, Hestroffer K, Keller S, Speck J S and Mishra U K 2015 N-face GaN/AlN/GaN/InAlN and GaN/AlN/AlGaN/GaN/InAlN high-electron-mobility transistor structures grown by plasma-assisted molecular beam epitaxy on vicinal substrates *Semicond. Sci. Technol.* **30** 1–8

[102] Wong M H, Singisetti U, Lu J, Speck J S and Mishra U K 2012 Anomalous Output Conductance in N-Polar GaN High Electron Mobility Transistors *IEEE Trans. Electron Devices* **59** 2988–95

[103] Rajan S, Chini A, Wong M H, Speck J S and Mishra U K 2007 N-polar GaN∕AlGaN∕GaN high electron mobility transistors *J. Appl. Phys.* **102** 044501

[104] Schaake C A, Brown D F, Swenson B L, Keller S, Speck J S and Mishra U K 2013 A donor-like trap at the InGaN/GaN interface with net negative polarization and its possible consequence on internal quantum efficiency *Semicond. Sci. Technol.* **28** 105021

[105] Kim J W, Song G H and Lee J W 2006 Observation of minority-carrier traps in InGaN/GaN multiple-quantum-well light-emitting diodes during deep-level transient spectroscopy

measurements *Appl. Phys. Lett.* **88** 1–4

[106] Fang Z Q, Look D C, Lu C and Morkoç H 2000 Electron and hole traps in GaN p-i-n photodetectors grown by reactive molecular beam epitaxy *J. Electron. Mater.* **29** 19–23

[107] Osiński M, Zeller J, Chiu P C, Phillips B S and Barton D L 1996 AlGaN/InGaN/GaN blue light emitting diode degradation under pulsed current stress *Appl. Phys. Lett.* **69** 898–900

[108] Prozheeva V, Makkonen I, Li H, Keller S, Mishra U K and Tuomisto F 2020 Interfacial N Vacancies in GaN/(Al,Ga)N/GaN Heterostructures *Phys. Rev. Appl.* **13** 044034

[109] Wong M 2009 *N-face GaN-based Materials and Microwave Transistors by Plasma-Assisted Molecular Beam Epitaxy* (PhD Thesis, UCSB, CA)

[110] Chuang S L 1996 Optical gain of strained wurtzite GaN quantum-well lasers *IEEE J. Quantum Electron.* **32** 1791–800

[111] Chuang S and Chang C 1996 K·p method for strained wurtzite semiconductors *Phys. Rev. B - Condens. Matter Mater. Phys.* **54** 2491–504

[112] Anon *Device Simulation Software, ATLAS User's Manual, Silvaco Int., Santa Clara, CA, 2015.*

[113] Pasayat S S, Ahmadi E, Romanczyk B, Koksaldi O, Agarwal A, Guidry M, Gupta C, Wurm C, Keller S and Mishra U K 2019 First demonstration of RF N-polar GaN MIS-HEMTs grown on bulk GaN using PAMBE *Semicond. Sci. Technol.* **34** 045009

[114] Janicki Ł, Misiewicz J, Siekacz M, Turski H, Moneta J, Gorantla S, Skierbiszewski C and Kudrawiec R 2019 Sensitivity of N-polar GaN surface barrier to ambient gases *Sensors Actuators, B Chem.* **281** 561–7

[115] Cheema S S, Shanker N, Wang L-C, Hsu C-H, Hsu S-L, Liao Y-H, San Jose M, Gomez J, Chakraborty W, Li W, Bae J-H, Volkman S K, Kwon D, Rho Y, Pinelli G, Rastogi R,

Pipitone D, Stull C, Cook M, Tyrrell B, Stoica V A, Zhang Z, Freeland J W, Tassone C J, Mehta A, Saheli G, Thompson D, Suh D I, Koo W-T, Nam K-J, Jung D J, Song W-B, Lin C-H, Nam S, Heo J, Parihar N, Grigoropoulos C P, Shafer P, Fay P, Ramesh R, Mahapatra S, Ciston J, Datta S, Mohamed M, Hu C and Salahuddin S 2022 Ultrathin ferroic HfO2–ZrO2 superlattice gate stack for advanced transistors *Nature* **604** 65–71

[116] Denninghoff D J 2012 *Highly Scaled N-polar GaN MIS-HEMTs* (University of California, Santa Barbara, USA)

[117] Denninghoff D J, Dasgupta S, Lu J, Keller S and Mishra U K 2012 Design of high-aspect-ratio T-Gates on N-Polar GaN/AlGaN MIS-HEMTs for High f max *IEEE Electron Device Lett.* **33** 785–7