ADVANCED MATERIALS

Supporting Information

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Ultrathin Nitride Ferroic Memory with Large ON/OFF Ratios for Analog In-memory Computing

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Note 1. PUND and C-V measurements

P-E loops with different V_{max} have been measured on a 10 μm diameter device, and results are shown in **Figure S1**. Square-shape P-E loops can be observed, with remnant polarization of 20-30 μC/cm^2, consistent with the PUND results. The P-E loop becomes poor-shaped when V_{max} is large due to enhanced leakage currents.

During PUND measurement, square pulse trains were applied to the Au/Ti/ScAlN/n-GaN capacitors, and the response currents at different pulse voltages are shown in **Figure S2(a)**. The switchable polarization was evaluated [1] and shown in **Figure 1(h)** in the main text.

Figure S2(b) displays the C-V loop shown in **Figure 1(h)** and the corresponding dissipation factor. During the measurement the overall tanδ was less than 1, ensuring the accuracy of the measurement. Frequency dependent C-V curves are further displayed in **Figure S2(c)**. An asymmetric butterfly shape C-V hysteretic loop can be seen from 0.1 MHz to 2 MHz, indicating the hysteresis is from ferroelectric switching.

Note 2. Resistive switching mechanisms

The conduction band profiles with different oxide layer thicknesses were calculated based on self-consistent solutions of coupled Schrodinger-Poisson equations. The bandgap (6.3 eV in this calculation) and dielectric constant (10 in this simulation) of the oxide were approximated from Sc_2O_3 and Al_2O_3. For ScAlN with 30% of Sc, a bandgap of 5.2 eV and dielectric constant of 16 were used. The spontaneous polarization in ScAlN was set to –15 μC/cm^2 for P down and +15 μC/cm^2 for P up condition, and the doping concentration of GaN was 2×10^{19} cm^{-3}. Donor-like traps with a sheet concentration of 5×10^{12} cm^{-2} was added to the ScAlN/GaN interface to account for interface imperfections. As shown in **Figure S3(a)**, when the surface is free of oxide layer, the energy barrier for P up condition is higher than that for P down condition. In this case, the device will be set to ON after positive voltage sweep, which explains the resistive switching behavior in thick ScAlN/GaN heterostructures.[2] With increasing oxide layer thickness, the energy

barrier for P up condition quickly decreases, accompanied by an increase in the energy barrier for P down condition. A transition occurs when the oxide thickness exceeds 2 nm, after which the energy barrier for P up condition is lower than that for P down condition. That means, a positive voltage sweep will set the device to OFF state instead of ON state, which is exactly the case in this work. From TEM, the oxide layer is estimated to be 3-5 nm, consistent with the band profile calculations.

To further test our assumption, a reference sample with the same structure grown under the same condition was prepared. The sample was loaded into an e-beam evaporator immediately after taking out from the MBE chamber to avoid surface oxidation. Ti electrodes were then defined by lithography and dry etching. As shown in **Figure S3(b)**, a similar C-V hysteretic loop can be observed, which could be ascribed to the polarity change of the ScAlN barrier layer. A relative permittivity of ~ 14.4 can be extracted at zero bias, which is more reasonable due to less surface oxidation. Interestingly, the I-V curve showed a counterclockwise-clockwise rotation, as shown in **Figure S3(c)**. The device can be set to "ON" by positive voltage sweep and "OFF" by negative voltage sweep, opposite to the devices with relatively thick surface oxide as shown in the manuscript. This agrees well with the predictions from the band profile calculation.

Figure S3(d) displays the electrode-size dependent I-V loops. The I–V hysteresis loop is found to be independent of junction area, and no electroforming or current compliance is required to stabilize the switchable resistance, thereby excluding the formation of conductive filaments. The counterclockwise C-V hysteresis loop indicates trapping is not playing a dominant role. The effect of vacancy migration has been excluded in our previous work.[2] The effect of a conductor-insulator can be naturally ruled out by the opposite ON/OFF operation in the reference sample.

Therefore, we believe the resistive switching behavior in this work is a combined effect of surface oxide and ferroelectric polarization switching in the ScAlN layer.

Note 3. Reliability studies

Figure S4(a) depicts the I-V loops measured in 20 randomly distributed devices,

showing very good uniformity.

Figure S4(b) displays the I-V loops after different bipolar switching cycles. As shown in the figure, even after 10^4 switching cycles, the device exhibited distinct hysteretic I-V loops with clear ON/OFF operation, indicating good endurance resistance.

Figure S4(c)(d) show the ON/OFF currents under -4 to 0 V measured after different retention time. The almost overlapped I-V curves after up to 10^5 s indicates excellent retention performance.

Figure S4(e)(f) show the retention characteristics at different temperatures.

Note 4. Image processing

Due to the limitations of our measurement setup, it is right now difficult to apply nine voltage pulses at the same time. As a compromise, we did the VMM operation using an array with three different devices. During measurement, the bottom electrodes of the devices were connected with each other for reading of the current sum, while set/read voltage pulses were applied via three probes in contact with the top electrodes according to the set/read scheme shown in **Figure S5**. The current readout shows reasonable accuracy compared with the VMM results from software calculation, suggesting that the proposed nitride memory can be used for accurate VMM operations.

To perform image processing, the intensity value of each pixel, which represents the brightness of the pixel in the input image, is multiplied by the kernel weight. The output is then the sum of the products of the intensity values of the input pixels and the kernel weights. The intensities of the pixels are encoded into voltages according to the mapping scheme shown in **Figure 3h**, and the weight of each element in the kernel matrix is converted into the conductance of the synaptic devices. Finally, multiplication of the intensity values of the input pixels by the kernel weights can be achieved using Ohm's law, and the accumulation can be achieved using Kirchhoff's law. For simplicity, in this work, multiplication operation was done in real devices, while accumulation operation was performed in the software end. First, nine different

devices were programmed to the desired conductance according to the kernel. Then, the whole image was used as input for every device, and the output current from each device was collected and summation operation was done using home-written code. **Figure S6** displays the kernels used for image processing, and the output current for each multiplication operation. Due to the limitation of the setup, the maximum number of pulses during each measurement is 1001, and the vertical-line shape noise is attributed to parasitic effects or the trapping process in the initial pulses of each input pulse train. The output from "mean" operation was reused during "edge" operation to save time.

Note 5. Fitting of nonlinear weight update and benchmark

During simulation, non-ideal device properties, including nonlinear weight update, device-to-device weight update variation, and cycle-to-cycle weight update variation are considered. Device-to-device variation and cycle-to-cycle variation are estimated by measuring the weight update characteristics in multiple cycles and multiple devices. The nonlinear weight update property is incorporated by fitting the nonlinearity value following the model proposed by Pai-Yu Chen et al [3] as shown in **Figure S7**.

To compare with other analog synaptic devices, the device performance has been benchmarked with those provided in the manual of NeuroSim as shown in **Table S1**. The ferroelectric nitride memristor showed the highest ON/OFF ratio and best online learning accuracy in the classification task.

Note 6. Possible ways to integrate with Si CMOS technology

Although the device in this work was grown on GaN/sapphire substrate, the n-GaN layer can be replaced by other metals such as Al or Mo which can be prepared on Si via CMOS compatible processes. Recently, our group have successfully grown ferroelectric ScAlN on commercial Mo/Sc_2O_3/Si substrates under CMOS-compatible

temperature, showing high possibility of integration with Si technology. Besides, while previous GaN on Si technology has been focusing on improving the quality of the nitride layer to maintain the high performance of HEMTs, the memristors here, which rely on the ferroelectricity in ScAlN, are less sensitive to material quality thus can alleviate the stress on the GaN/Si growth. Based on the discussions above, there could be two ways to integrate with Si: (1) Since the ScAlN layer can be prepared on metal using a CMOS compatible process, the memristor and peripheral circuitry may be fabricated using via BEOL processing; (2) As the memristor is less material quality sensitive, the required layer stack, ScAlN/GaN/Si, can be prepared first then processed by CMOS compatible fabrication steps to build the memristor and peripheral circuitry.

Reference

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[2] D. Wang, P. Wang, S. Mondal, S. Mohanty, T. Ma, E. Ahmadi, Z. T. Mi, Adv Electron Mater **2022**, 2200005.

[3] P. Y. Chen, X. C. Peng, S. M. Yu, 2017 Ieee International Electron Devices Meeting (Iedm) **2017**, 6.

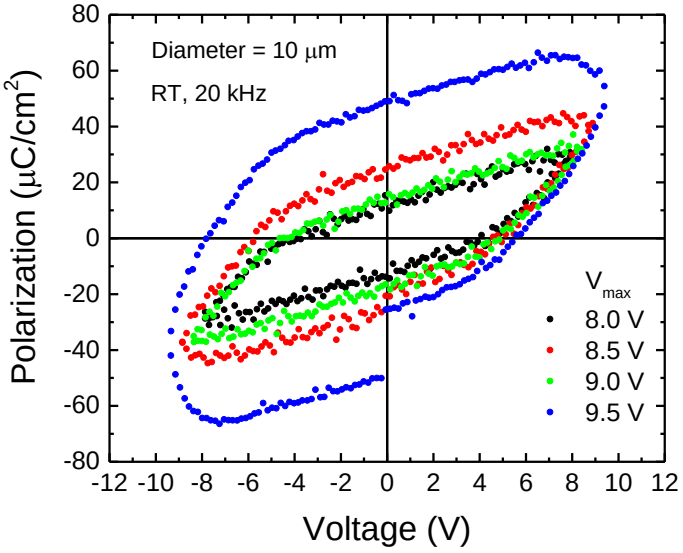


Figure S1. Typical P-E loops measured on one 10 μm diameter device. Triangular shape waveforms were used, and the measurement was performed at room temperature, 20 kHz.

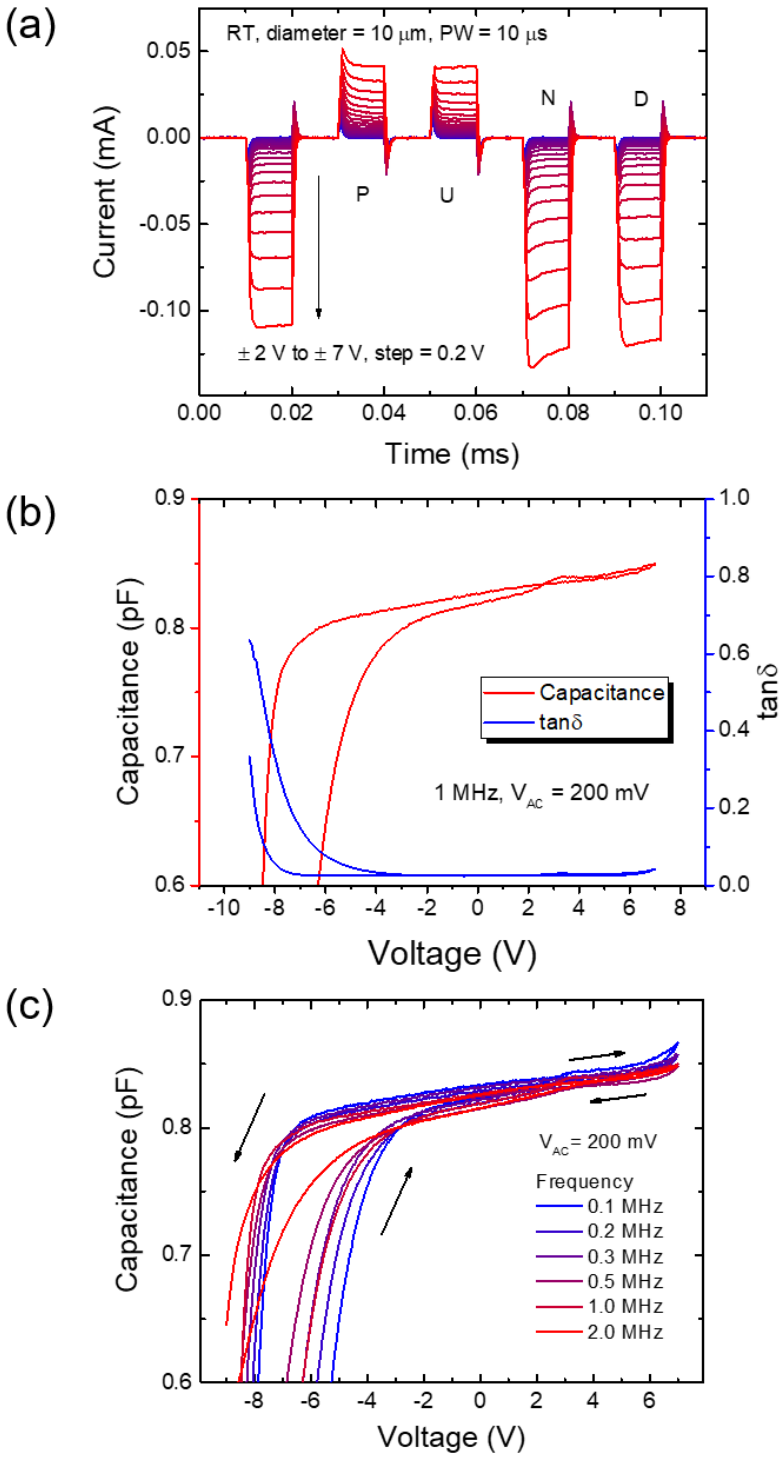


Figure S2. (a) Current response during voltage-dependent PUND measurements used for extracting switchable polarization in Figure 1(f). (b) C-V hysteretic loop shown in Figure 1(h) with corresponding dissipation factor. (c) Frequency-dependent C-V hysteretic loops.

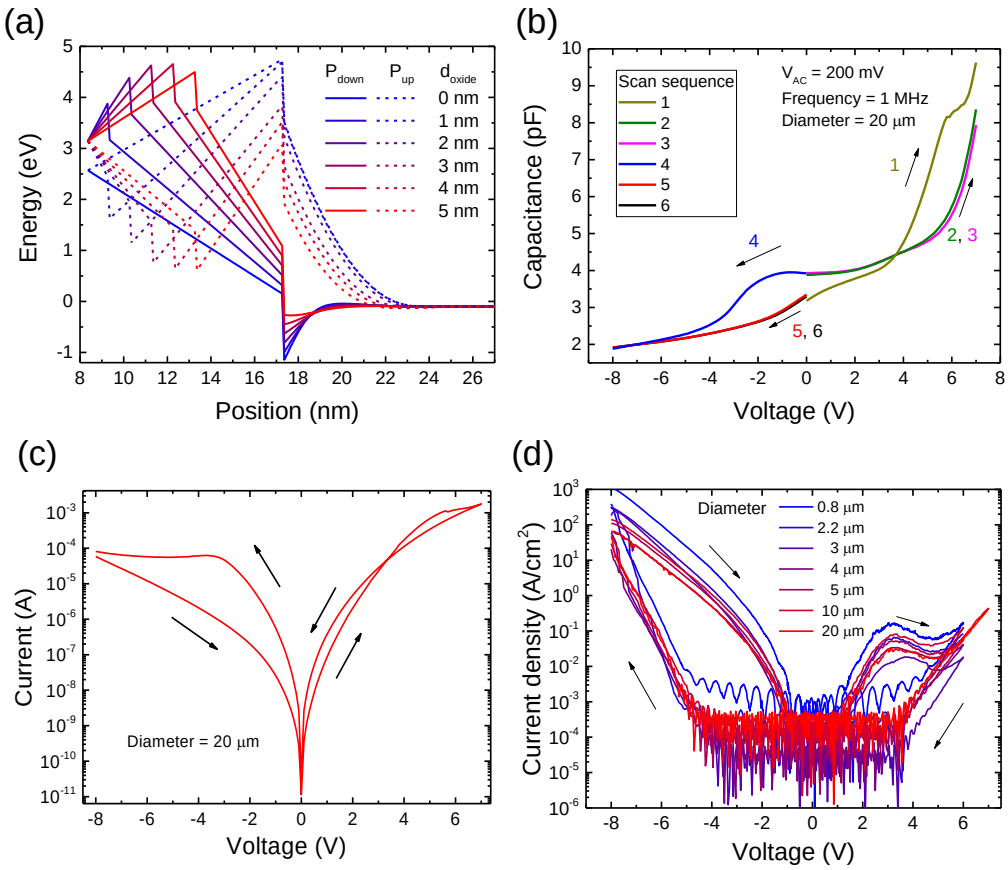


Figure S3. (a) Conduction band profiles calculation results, showing the transition of ON/OFF states with varying oxide layer thickness. The total barrier thickness is fixed. (b) C-V hysteretic loops measured on the oxide-attenuated reference sample. The sweeping sequences have been indicated by numbers and arrows. (c) I-V loops measured on the oxide-attenuated reference sample, showing an opposite rotation direction. (d) Electrode-size dependent I-V loops. The I–V hysteresis loop is found to be independent of junction area, and no electroforming or current compliance was required to stabilize the switchable resistance. The deviation of the 0.8 μm device could be due to processing variations

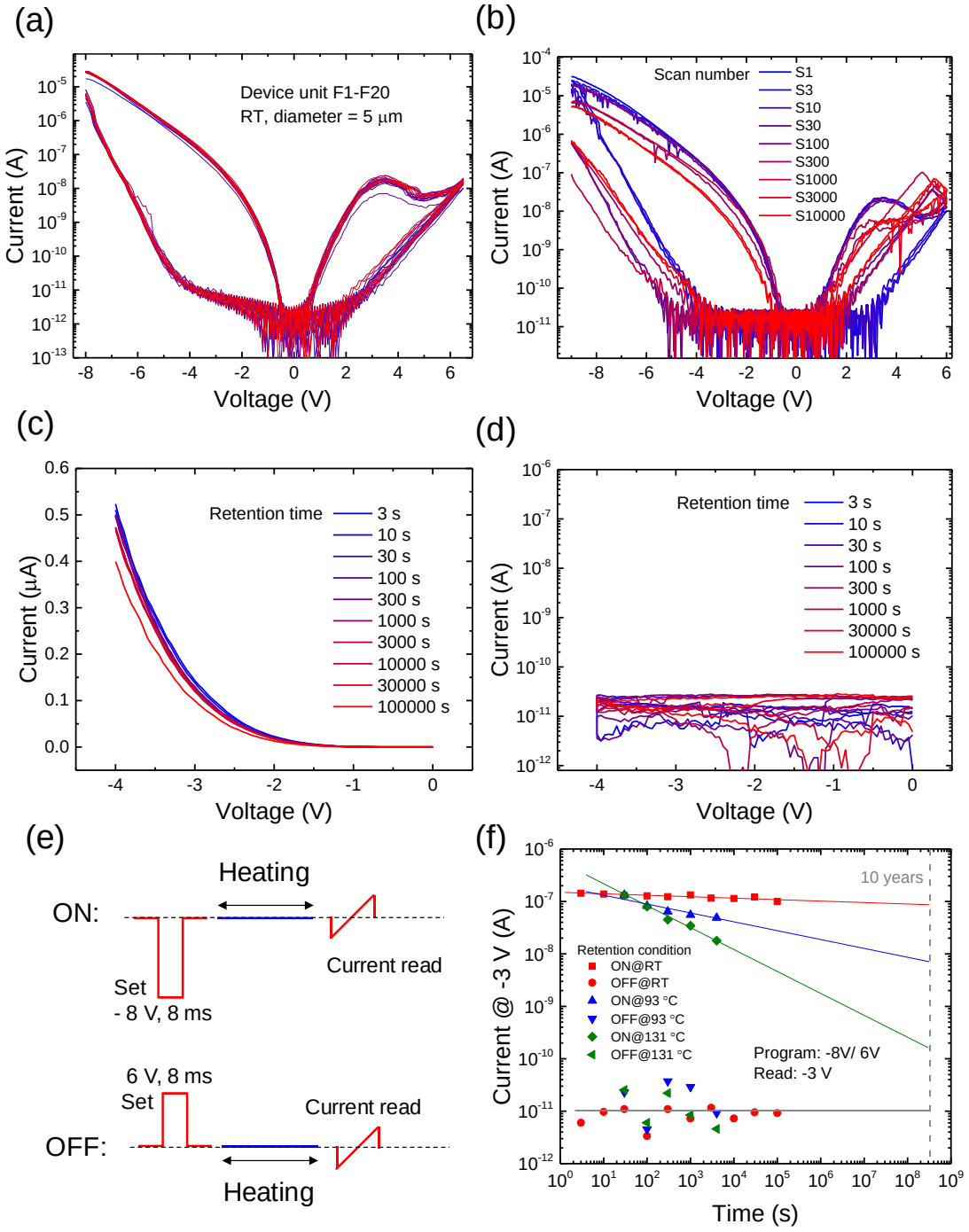


Figure S4. (a) I-V loops measured on 20 randomly distributed devices used to extract the data in Figure 2d. (b) I-V loops after different bipolar poling cycles with poling voltages of -8 V/ +6 V and pulse width of 8 ms. (c) (d) Retention characteristics of ON and OFF state current in the voltage range of 0 to -4 V. (e)(f) Retention characteristics at different temperatures.

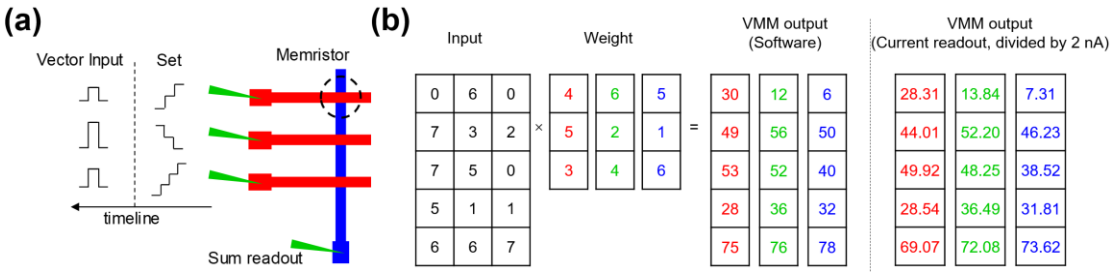
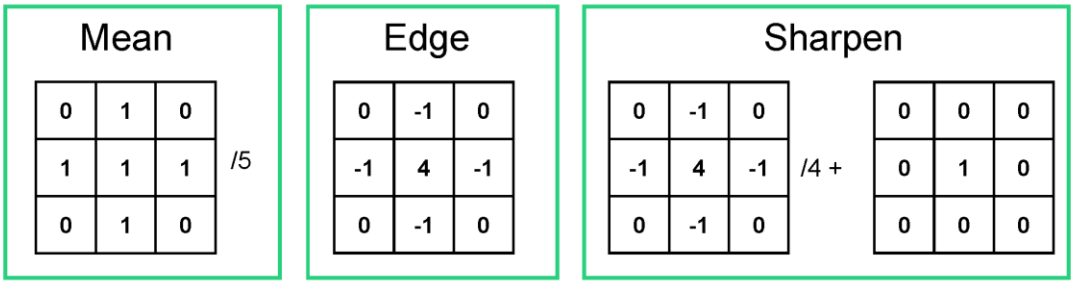


Figure S5. (a) Schematic of VMM operation using an array containing three devices and (b) VMM operation of randomly generated matrixes using an array with three different devices (diameter = 5 μm).

(a)



(b)

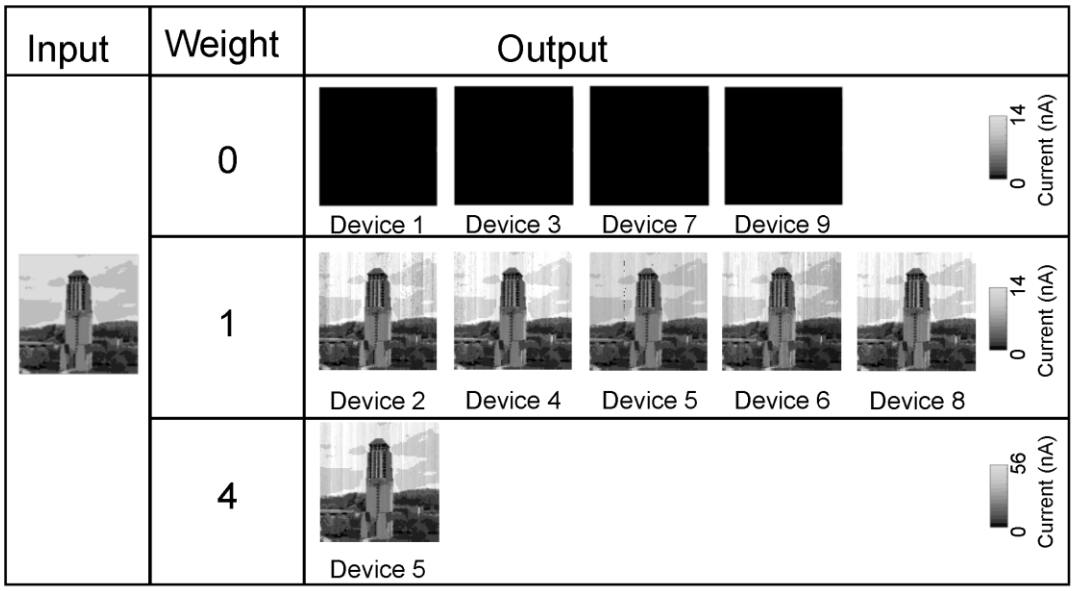


Figure S6. (a) Kernels used for image processing. (b) Weighted current output according to the kernels. Nine different devices were used.

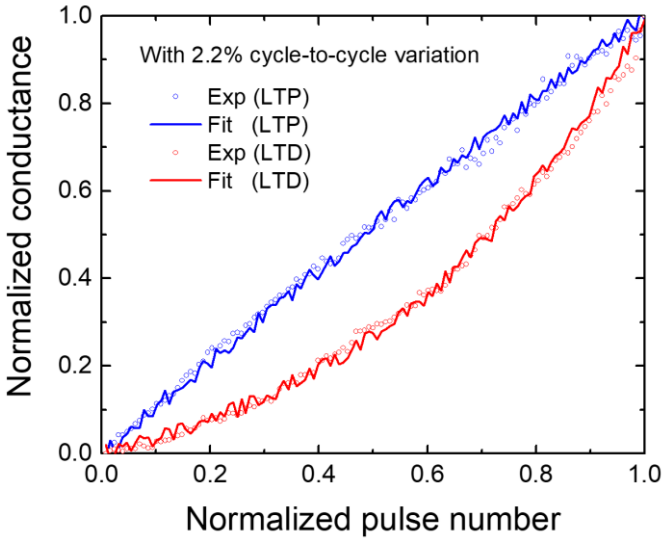


Figure S7. Fitting of the weight update data obtained in a ferroelectric nitride memristor. The extracted non-linearity factors were then transferred to NeuroSim V3.0 for real device simulation.

Table S1. Comparison of this work with some other types of synaptic devices reported in the literature.

Devices Type	Ag:a-Si [1]	TaOx/HfOx [2]	PCMO [3]	AlOx/HfOx [4]	GST PCM [5]	EpiRAM (Ag:SiGe) [6]	HZO FeFET [7]	This work
# of conductance states	97	128	50	40	100-120	64	32	**128**
Nonlinearity (LTP/LTD)	2.4/-4.88	0.04/-0.63	3.68/-6.76	1.94/-0.61	0.105/2.4	0.5/-0.5	1.75/1.46	**0.22/-1.69**
ON/OFF ratio	12.5	10	6.84	4.43	19.8	50.2	45	**> 100**
R_{ON}	26 MΩ	100 KΩ	23 MΩ	16.9 KΩ	4.71 KΩ	81 KΩ	559.28 KΩ	**~ 10 MΩ**
Set/reset voltage	3.2 V/-2.8 V	3 V/3 V	-2 V/2 V	0.9 V/-1 V	0.7 V/3 V	5 V/-3 V	3.65 V/-2.95 V	**-8 V/6 V**
Cycle-to-Cycle variation	3.5%	3.7%	<1%	5%	1.5%	2%	<0.5%	**2.2%**
Online learning accuracy	~ 72%	~ 80%	~ 33%	~ 20%	89%	92%	88%	**92.9%**

References:

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