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Ultrathin Nitride Ferroic Memory with Large ON/OFF Ratios for Analog In-Memory Computing

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Computing in the analog regime using nonlinear ferroelectric resistive memory arrays can potentially alleviate the energy constraints and complexity/footprint challenges imposed by digital von Neumann systems. Yet the current ferroelectric resistive memories suffer from either low ON/OFF ratios/imprint or limited compatibility with mainstream semiconductors. Here, for the first time, ferroelectric and analog resistive switching in an epitaxial nitride heterojunction comprising ultrathin (≈5 nm) nitride ferroelectrics, i.e., ScAlN, with potentiality to bridge the gap between performance and compatibility is demonstrated. High ON/OFF ratios (up to 10^5), high uniformity, good retention, (<20% variation after > 10^5 s) and cycling endurance (>10^4) are simultaneously demonstrated in a metal/oxide/nitride ferroelectric junction. It is further demonstrated that the memristor can provide programmability to enable multistate operation and linear analogue computing as well as image processing with high accuracy. Neural network simulations based on the weight update characteristics of the nitride memory yielded an image recognition accuracy of 92.9% (baseline 96.2%) on the images from Modified National Institute of Standards and Technology. The non-volatile multi-level programmability and analog computing capability provide first-hand and landmark evidence for constructing advanced memory/computing architectures based on emerging nitride ferroelectrics, and promote homo and hybrid integrated functional edge devices beyond silicon.

1. Introduction

To alleviate the performance constraints imposed by conventional von Neumann systems in an ocean of data, new architectures employing analogue in-memory computing techniques are being intensively investigated in pursuit of reducing energy consumption and latency.[1–4] Two-terminal memristors, owing to their dense device structure, ability to store and process data at the same location, simple weight update scheme, and straightforward vector-matrix multiplication (VMM) in a crossbar array fashion, have been widely explored for neuromorphic computing, machine learning, and edge computing applications.[5,6] To this end, various non-volatile memories (NVMs), including resistive memory, flash memory, phase-change memory, and magneto-resistive memory have been explored to carry out feature extraction, image processing, and neuro-inspired computing.[6–14] Ferroelectric resistive memory utilizes multi-domain polarization switching dynamics in a ferroelectric material, which has been shown to deliver fast potentiation and depression programming, symmetric and linear conductance response, and large ON/OFF conductance ratios.[15–19] To harness the well-established periphery circuitry and increase integration density, however, it is desired to integrate ferroelectric memory arrays with mainstream semiconductor technology, which significantly narrows down the materials available.[20–22] The discovery of ferroelectricity in HfO_2-based materials has rejuvenated the interest in ferroelectric memory with both front-end-of-line and back-end-of-line compatibility. To date, however, related two terminal resistive memories still suffer from low ON/OFF ratios, wake-up effect and significant imprint oscillations and retention loss.[19,21,23–27] Although recent studies have shown that HfO_2-based field effect transistors are much less affected by above limitations,[28] two-terminal memristors offer the advantages of significantly reduced device area and operation power and, therefore, have remained a subject of intensive study.

Those issues can potentially be addressed by exploiting a new class of ferroelectrics – nitride ferroelectrics.[29] Sc-alloyed III-nitrides, i.e., ScAlN and ScGaN, have been discovered with giant remnant polarization and superior thermal stability.[29–33] The wide processing temperature window and the approximation of the lattice with other nitride materials promise good compatibility and seamless integration with both GaN and silicon technology.[34–38] In addition, the wake-up effect and

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imprint are reported to be weak for epitaxial ScAlN films.[30,39] Those advantages not only enable the integration of nitride ferroelectrics based memristors with the mainstream technology to explore their potentiality in advanced computing architectures, but also allow for harnessing the well-established applications of nitrides, such as light emission/detection, high power and high speed devices, piezoelectric resonators, etc., to implement homo and hybrid integration and deliver computation and logic functionality in beyond silicon technology, further extending the landscape of edge computing.[40–48] In this regard, a few memristor demonstrations based on ScAlN have been reported, yet the ScAlN layer employed are thick (>20 nm) which causes high operation voltages and potentially scalability problems.[49–52] Moreover, the ferroelectric synaptic weight update as well as precise VMM operation and image processing in ultrathin ScAlN has remained elusive.

In this work, we demonstrate resistive switching and analog computing in a ferroic heterojunction memory comprising an ultrathin nitride ferroelectric, i.e., ScAlN as the barrier layer. First, ferroelectric switching is confirmed in sub-10-nm thick ScAlN via positive-up negative-down (PUND) and capacitance-voltage (*C*–*V*) measurements. Then, we demonstrated high ON/OFF ratios (10^4-10^5), high uniformity, good retention (>10^5 s) and good cycling endurance (>10^4) in the nitride ferroic junction by exploiting an oxide capping layer. Due to significant thickness-scaling-down, the read/write voltage was reduced to less than 3 V/8 V, which is already close to hafnia-based ferroelectric junctions in a similar structure.[53] Third, we demonstrated that this nitride memristor can provide programmability to enable multistate operation and linear weight updates as well as image processing with high accuracy. Finally, artificial neural network (ANN) simulations based on the weight update characteristics of the proposed nitride memory were performed to explore the potentiality of utilizing nitride memory for accurate analog in-memory computing. The demonstration of robust and programmable nitride ferroelectric memory and associated analog computing capability delineates a viable path to constructing next-generation memristors toward power-efficient data storage and advanced computing platforms.

2. Results and Discussions

Compared with sputter deposition, molecular beam epitaxy (MBE) provides significantly improved crystal quality and thickness control. Therefore, the ultrathin ScAlN layer in this work was grown by plasma-assisted MBE on n-GaN substrate with a nominal Sc composition of 30% and thickness of ≈9 nm. **Figure 1**a depicts the schematic of a metal/ScAlN/n-GaN capacitor used to explore the ferroelectricity in ultrathin ScAlN in this study. Due to the high oxygen affinity of Sc and Al, a thin oxide layer naturally formed at the surface, which appeared as the dark contrast region in the high-angle annular dark field scanning transmission electron microscope (HAADF-STEM) image (Figure 1b).[49] Highly ordered atomic stacking sequence with a wurtzite structure can be observed at the ScAlN/GaN interface, revealing the high-quality of the MBE-grown ScAlN film (Figure 1c). The single crystalline wurtzite structure of ScAlN and GaN as well as the non-crystalline structure of the oxide layer are further confirmed by nano-beam electron diffraction (NBED) patterns as shown in Figure 1d. HAADF-STEM image combined with corresponding elemental analysis (EDS mapping, Figure 1e) indicates the oxide layer has a thickness of ≈4 nm while the ScAlN layer is 5–6 nm. The oxidation process could be controlled by modulating the total exposure time using glove boxes with different gases or by controlled oxygen plasma treatment. Later we will show that this oxide layer can function as an extended barrier to enhance the rectifying ratio of the memristor. Figure 1f,g shows the PUND results using 10 µs short pulses performed on 10-µm-diameter capacitors. The contribution of the ferroelectric displacement current can be clearly observed. A saturated remnant polarization (P_r) of >16 µC cm^{-2} can be extracted. While giant ferroelectric polarization has been demonstrated previously,[54] this is the first demonstration of saturated switchable polarization in crystalline ScAlN in the sub-10 nm regime. The reduction in remnant polarization compared with thick ScAlN is mainly due to the oxide layer at the surface which forms a ferroelectric-dielectric bilayer structure and amplifies the effect of the depolarization field during thickness-scaling.[55] The butterfly-like hysteresis in the *C*–*V* loop, which is characteristic of ferroelectric capacitors,[56] is also successfully captured in Figure 1h. More information on the PUND and *C*–*V* measurements, as well as P-E loops can be found in the Supporting Information, Note S1 (Supporting Information). The extracted relative permittivity at zero bias is ≈10.4, which is smaller than bulk values due to increased contribution from surface oxide layer (Note S2, Supporting Information). We argue that with the oxide capping layer on top, the realistic thickness of the ScAlN layer showing ferroelectricity can be even smaller, implying high scaling-down capability of nitride ferroelectrics.

Memory cells with top electrode diameters ranging from 0.8 to 20 µm were fabricated. Otherwise mentioned, the measurement results are based on the devices with a diameter of 5 µm. **Figure 2**a displays a schematic of the device structure and the operation principle of the nitride memory. Due to the existence of an oxide layer, the ferroelectric polarization charge at the oxide/ScAlN interface causes a giant modulation effect on the total barrier height, significantly contributing to the large ON/OFF operations. More specifically, polarization pointing down leads to a higher total barrier and thus OFF operation, while polarization pointing up results in a lower barrier and ON operation. The depletion region in the semiconductor side is negligible as the doping concentration of the n-GaN bottom electrode is sufficiently high (>2×10^{19} cm^{-3}), implied by the small capacitance hysteresis near zero bias in Figure 1h. Besides, the trapped charge at the oxide/ferroelectric and ferroelectric/semiconductor electrode interface could also lead to a reduction of the depletion region. More details regarding the resistive switching mechanism can be found in the Supporting Information, Note S2 (Supporting Information). The nonvolatile conductance switching in the nitride memory is demonstrated by the clear hysteretic variation of the read current, as shown in Figure 2b. The pulse trains used are shown in the inset. Negative pulses set the polarity to upward direction, consequently the ON state, while positive pulses set the polarity to downward direction and corresponds to the OFF state, consistent with the band schematics in Figure 2a. By pre-programming the device

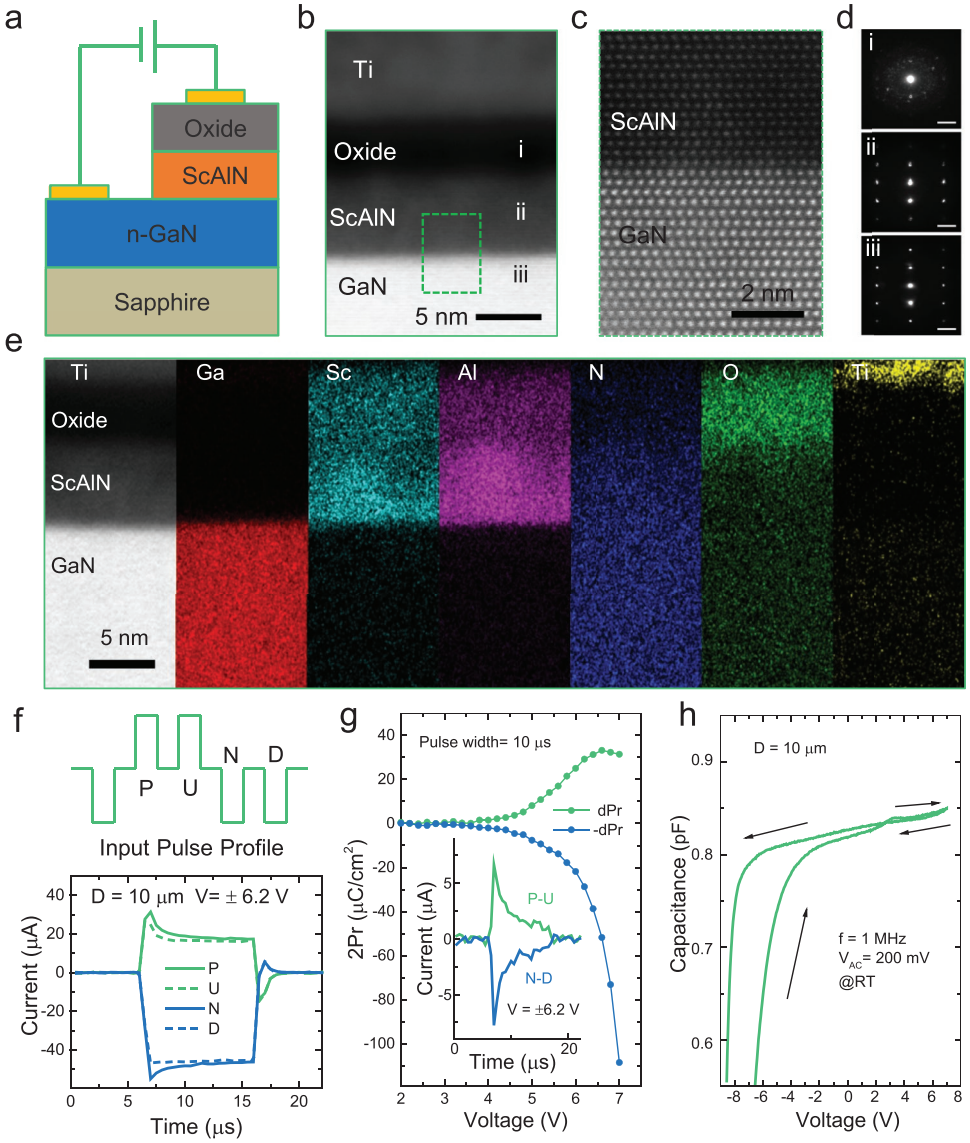

Figure 1. Ferroelectricity in ultrathin ScAlN films grown on GaN. a) Schematic illustration of the capacitor structure comprising ultrathin single-crystalline ScAlN and an oxide layer. Due to the high oxygen affinity of Sc and Al, a thin oxide layer is formed on the top of ScAlN. b) HAADF-STEM image of the heterostructure indicating an oxide layer of ≈4 nm and a ScAlN layer of 5–6 nm. c) Magnified STEM image at the ScAlN/GaN interface showing atomic sharp contrast. d) NBED patterns acquired from different regions in b): (i) the oxide layer, showing non-crystalline diffraction pattern, (ii) ScAlN layer and (iii) GaN layer, showing a wurtzite structure. The scale bar is 2 nm^{-1}. e) HAADF-STEM and corresponding EDS element maps of the heterostructure. Increased oxygen signal is detected near the surface. f) PUND pulse trains and corresponding current responses. g) Voltage-dependent PUND results with a pulse width and delay of 10 μs, revealing a saturated remnant polarization > 16 μC cm^{-2}. Inset shows the displacement current by subtracting non-switching current in f). h) Butter-fly shape capacitance-voltage curve of the heterostructure measured at 1 MHz with an AC voltage of 200 mV.

to OFF state and gradually switching to the ON state, a giant ON/OFF ratio approaching 10^5 is demonstrated, as shown in Figure 2c,d further shows the ON/OFF currents of 20 different devices with write pulses of −8 V and + 6 V read at −3 V. All measured devices exhibit high ON/OFF ratios larger than 10^4, suggesting good reproducibility and uniformity. Figure 2e,f depict the endurance and retention properties of the device. ON/OFF ratios > 10^3 can still be obtained after 10^4 bipolar switching cycles, with decreasing ON current possibly due to pinned domains parallel to the polarity of the substrate. The endurance obtained is somewhat lower than for fluorite-based ferroelectrics, yet it is already sufficient for applications such as an inference engine. Moreover, the device shows outstanding retention resistance, with only <20% degradation in ON current after 10^5 s (Note S3, Supporting Information), which outperforms its hafnia-based counterparts.[27] Retention tests at elevated temperatures were also performed and shown in the Supporting Information. Those reliability merits thus provide fundamental information for utilizing ferroelectric nitride memory toward reliable non-volatile memory and advanced computing applications. The *I*–*V* loops of different devices, *I*–*V* loops of devices with different diameters, after

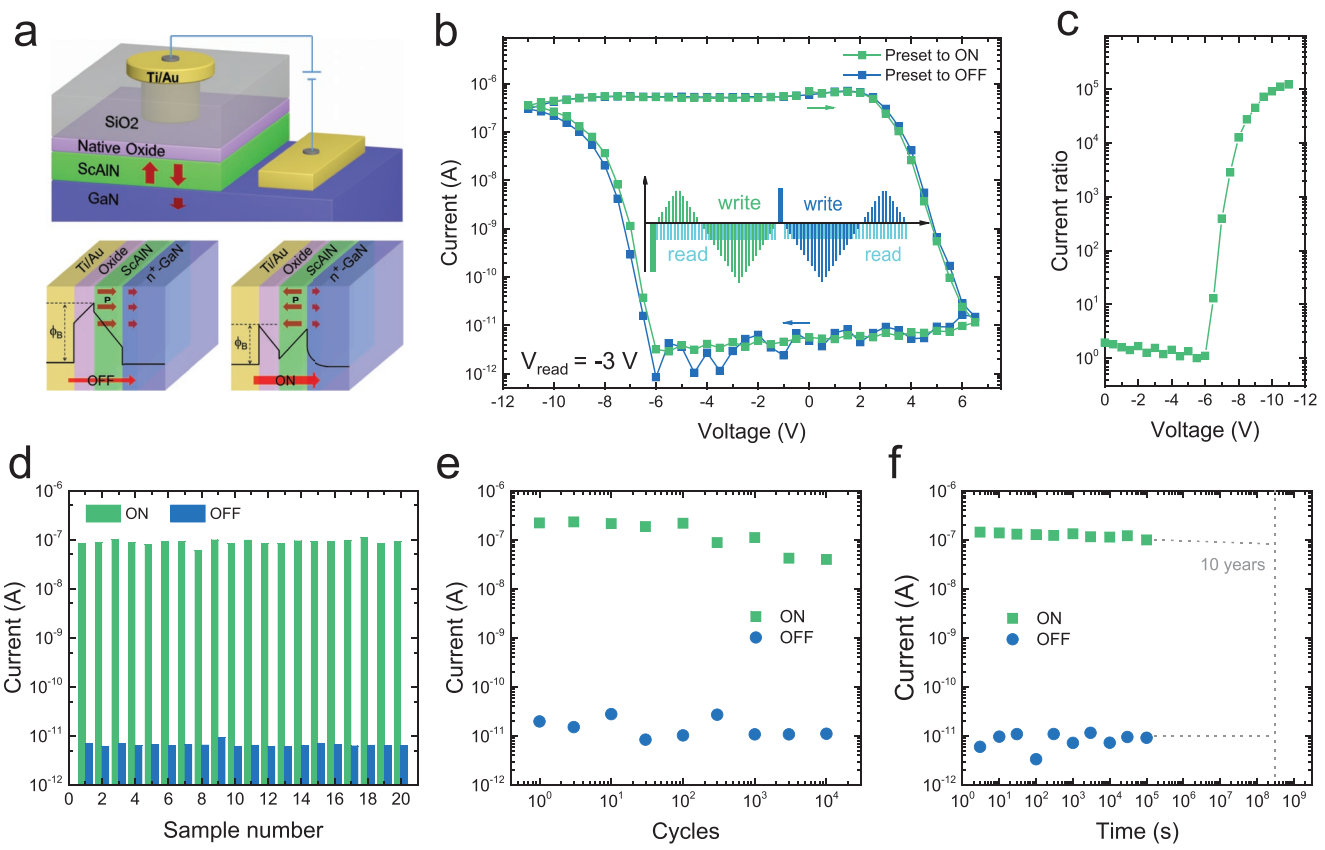

Figure 2. Electrical characterization of the nitride memory at room temperature. a) Schematic of the device structure and band profiles showing the ferroelectric polarization modulated potential energy barrier. b) Current hysteresis loops measured using pulse trains shown in the inset. The device is preset to the ON (OFF) state by a –11 V (+ 6.5 V) pulse, followed by staircase-like rectangular write pulses between –11 V and 6.5 V and read pulses of –3 V after each write pulse. c) Current rectifying ratio extracted from the negative branch in b). d) ON/OFF operation of 20 devices and e) endurance and f) retention properties of the memristor with rectangular write pulses of –8 and 6 V and read voltage of –3 V. The pulse width for pre-set, write and read pulses are 8 ms, 8 ms, and 0.16 s, respectively.

different cycling numbers and retention times can be found in Figure S4 (Supporting Information).

For ferroelectrics based memristors, multiple conductance levels can be established via partial polarization switching, which builds the key block for high-density data storage and advanced computing architectures.[15] The coupling between polarization and resistance in a ScAlN/GaN heterostructure has been studied previously, showing the feasibility to change the polarization thus the resistance gradually.[51] Using incremental voltage pulse scheme, eight clear, distinguishable conductance states are successfully demonstrated in the nitride memristor, as shown in **Figure 3**a. The conductance levels can be restored after multiple program/reset operations, and remain stable up to 200 s (Figure 3b). In addition to the reliability shown, the device exhibits a nonlinear *I*–*V* characteristic in all conductance states (Figure 3c), which is beneficial for suppressing sneak path currents and cross-talk in selector-free crossbar arrays.[57] Unlike redox or filament based resistive memory devices, we also note that the device can be switched to separate analog states without any initial forming or activation step, which not only reduces the overall operation voltage, but also means that the device and the circuits can be readily used in arrays without electrical pretreatment, a key issue for memory arrays that limits the stability and accuracy of the conductance state in certain memory devices.[58] The potential challenges of current work could be the high operation voltage and low current density,[59] which require the fine design of material and devices for further lateral scaling and integration, for example, through thickness scaling down or depolarization field design. These results, in combination with the good compatibility of nitride ferroelectrics with mainstream semiconductor technology, make the proposed structure a promising candidate for compact non-volatile memory architectures.

In convolution operations based on resistive crossbars, the output can be obtained from the current sums of the products of the input voltage vector and the device conductance, which requires electrical programmability and *I*–*V* linearity.[6] To demonstrate convolution operation using the nonlinear nitride memristor, a virtual logarithmic line driver is considered, which converts the linear input signal into nonlinear amplitude-programmed pulses to generate linear conductance outputs from the nonlinear nitride memristor.[14] Figure 3d,e show the fitting results of the *I*–*V* characteristics using an exponential function, which is typical for thermal and tunneling based conduction. Almost constant β and linear α values over each conductance level are obtained for all the conductance states in the

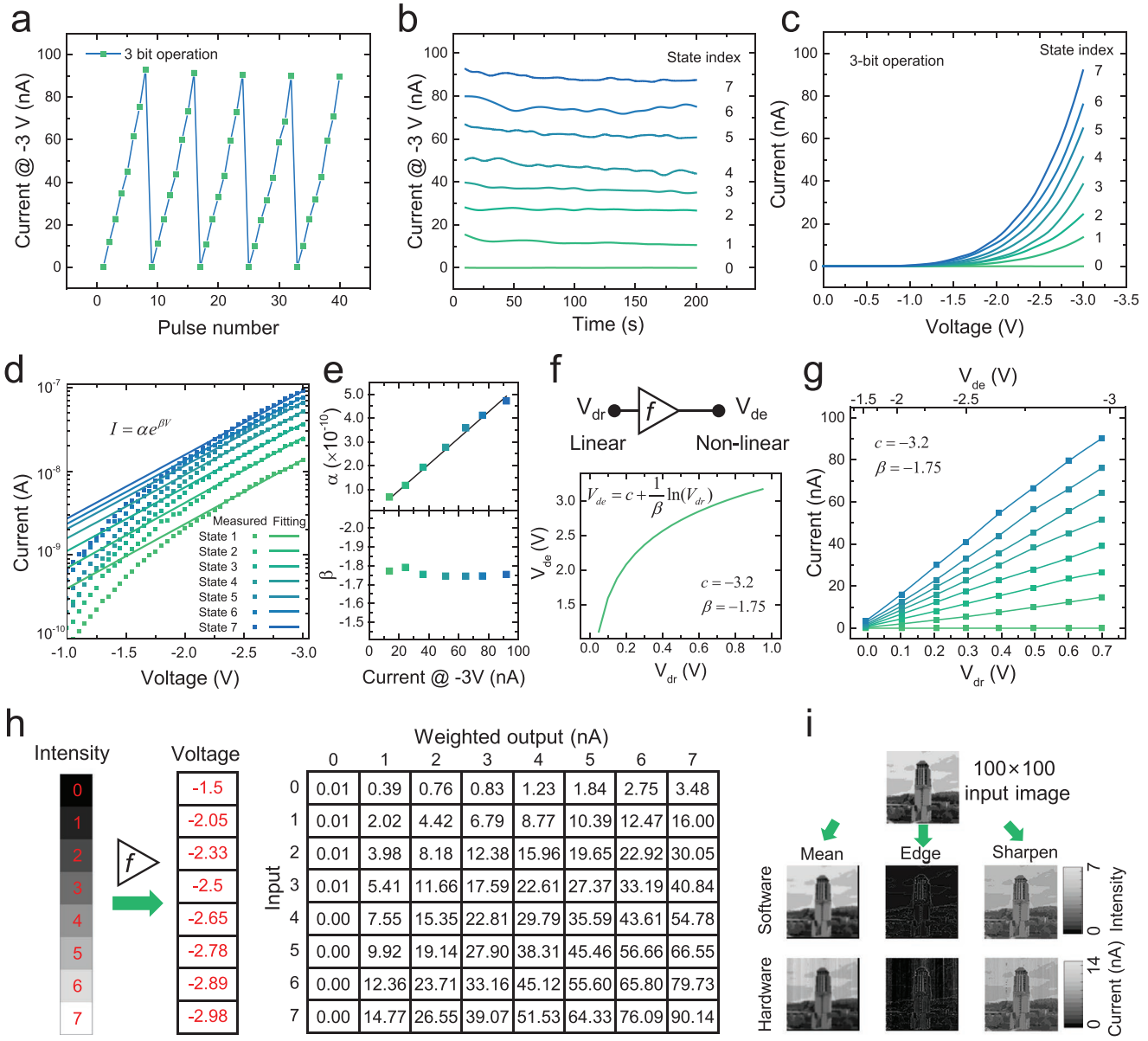

Figure 3. Demonstration of multi-state and convolution operation using nitride memristors. a) Multi-state operation by incremental pulses from –8 V to –8.35 V with a step of –50 mV and read voltage of –3 V. The pulse width is 8 ms. b) Retention of the 8 states up to 200 s. c) *I–V* curves of the 8 conductance states, showing non-linear *I–V* behavior. d) Fitting of the *I–V* curves in different states using an exponential function on the –2 to –3 V window and e) fitting parameters against the device state. f,g) Schematic of a logarithmic driver which maps linear input voltage to non-linear inputs for the non-linear nitride memristors. By properly choosing the fitting parameters, linear effective conductance can be established for analog computing. h) Gray-scale image inputs for convolution operations. The luminance of each pixel is encoded into voltage pulses from –2.05 V to –2.98 V according to g) and weighted outputs based on the 8 conductance states are shown accordingly. i) Basic image convolution operation using the ferroelectric nitride memory for three different kernels. A gray-scale image with 100 × 100 pixels is used as the input image. Three 3 × 3 kernel operations (mean, edge, and sharpen) are performed as examples.

[–2, –3.0] V and [2, 90] nA range, as shown in Figure 3e. A mapping function, as shown in Figure 3f, is utilized which scales non-linear device voltage V_{de} to linear drive voltage V_{dr} with β = –1.75 and c = 3.2 as an example. Figure 3g displays the mapping results, where linear effective conductance is achieved for all conductance levels. In reality, this logarithmic line driver can be essentially implemented with nonlinear drive circuits like p-n junctions or Schottky barrier diodes.[14]

To further demonstrate linear VMM operation and use the device for image convolution processing, 3-bit grayscale images are first converted into voltage pulses according to the mapping methodology in Figure 3g, and 3-bit conductance levels, i.e., 8 states, are then used as synaptic weights. Figure 3h shows the weighted output map for each input pixel intensity, which can be regarded as the multiplication results of 1-by-1 vectors with 1-by-1 matrixes (pixel intensity times weight). An error standard

deviation of 2.3% is extracted. Based on the scheme above, we performed convolution operations using three 3 × 3 kernels, i.e., mean, edge and sharpen, for a gray-scale input image with 100 × 100 pixels. Nine devices are first programmed to different conductance levels according to the kernel weights, and the voltage pulses converted from the intensity values of each pixel of the image are sequentially applied to every device. The weighted output currents from each device are collected separately as multiplication operation output while the accumulation operation is done on the software end. This ignores the inaccuracies introduced by the logarithmic driver and the differential readout circuits, but is sufficient for prototype demonstration. Figure 3i displays the convolution results from pure software calculation and from the current outputs of the nitride memristors, showing high convolution accuracy. High accuracy VMM operation based on an array containing three different devices, where current sums were read out directly from the hardware, can be found in Supporting Information, Note S4 (Supporting Information). These results provide first-hand and landmark evidence that ferroelectric nitride memristors can be used for convolution operations toward image processing and feature extraction. The exact form of the kernels and output current from different devices can be found in Figure S6 (Supporting Information).

In above demonstrations, only 8 conductance states are utilized. For ANNs computing in the analog regime, linear, symmetric potentiation and depression conductance response with tens of conductance states are required to accelerate the training process effectively.[2] In addition, the cycle-to-cycle and device-to-device variations should be minimal. In this work, two pulse schemes, namely identical pulse scheme and amplitude-incremental pulse scheme, are performed to test the symmetry and linearity during 128-state (7-bit) potentiation and depression operations. For identical pulse scheme, −7.8 V pulse is used for potentiation and 2.7 V pulse is used for depression. For incremental pulse scheme, the amplitude of the pulses is increased from −7.6 V to −8.24 V in a 5 mV step for potentiation, and from 1.9 V to 3.564 V in 13 mV step for depression, respectively. The read voltage is −3 V and read/write pulse widths are fixed at 8 ms for simplicity. As shown in **Figure 4**a, the second scheme delivers much more linear weight update characteristics, which is then adopted for ANN simulation. We note the current for each state is relatively low, which may cause increased latency for single-device readout, but will not matter much for large-scale computing arrays where current output from multiple devices are combined for accumulated readout. The cycle-to-cycle and device-to-device variation characteristics are further investigated in Figure 4b,c. No significant degradation is observed during repeated pulse operations (Figure 4b). The average cycle-to-cycle variation (standard error) is further estimated to be <2.2% based on 20 repeated cycles (Figure 4c). 10 different devices are measured to evaluate the device-to-device variation with results from the first 5 devices shown in Figure 4b. The device-to-device variation is found to be relatively larger than the cycle-to-cycle variation, with maximum variation < 6% and an average device-to-device variation of 3.1%. This relatively large device-to-device variation, however, is unlikely to cause significant performance degradation because the ANN model could have self-adaption to such static variation. Optimization of the processing steps and weight-update scheme is being done to improve the uniformity and reliability of the nitride memristors.

Based on above weight update results, we simulate the performance of the nitride memristors in a classic demonstration-purpose application where a trained two-layer multilayer perceptron (MLP) neural network is tasked to classify handwriting images from the Modified National Institute of Standards and Technology database (MNIST).[60] An illustration of the network is shown in the inset of Figure 4d, and more details can be found in previous publication.[60] While simulation results vary depending on the neural network structures employed, this simple yet complete tool allows us an easy comparison with other memory devices. During simulation, the nonlinearity factors are set to 0.22 and −1.69 (Figure S7, Supporting Information) for potentiation and depression with cycle-to-cycle variation of 2.2% and device-to-device variation of 3.1%. The weight values are mapped to the conductance range shown in Figure 4c. As shown in Figure 4d, even though the device is still in its infancy, a recognition accuracy of 92.9% (96.2% for ideal device) is achieved based on the realistic weight update characteristics of the nitride ferroelectric memristor, which already outperforms most analog synaptic devices and is comparable to those state-of-the-art ferroelectric transistors (Note S5, Supporting Information). Simulation without considering cycle-to-cycle and device-to-device variations is also performed and yields an increased recognition accuracy of 94.1%, implying that both the linearity of the weight update and the stability of the established states are to be optimized to further improve the overall accuracy. Nevertheless, the simulation of a MLP-based neural network confirmed that this new ferroelectric platform can be employed for accurate in-memory computing architectures.

3. Conclusion

In summary, we demonstrate ferroelectric and analog resistive switching in an ultrathin ferroelectric oxide/ScAlN/GaN heterojunction. PUND and *C*–*V* measurements were conducted to explore the ferroelectricity in the sub-10 nm ScAlN layer. With the help of a thin oxide capping layer, the heterostructure exhibited great potential for nonvolatile memory with superior ON/OFF ratios, high uniformity, good retention, and modest cycling endurance. In addition, we demonstrated that the nitride memristor can provide programmability to enable multistate operation and linear analogue computing as well as image processing with high accuracy, where the nonlinearity of the *I*–*V* characteristics and the low operation conductance could potentially benefit selector-free crossbars with high power efficiency. Neural network simulations based on the weight update characteristics of the ferroelectric nitride memory yield high image recognition accuracy. The robust ferroelectricity in the sub-10-nm ScAlN encourages further scaling down the thickness and operation voltage of nitride ferroelectrics for energy efficient applications. The non-volatile multi-level programmability and analog computing capability in this work can potentially bridge the gap between performance and compatibility in conventional ferroelectrics, and allow for constructing advanced

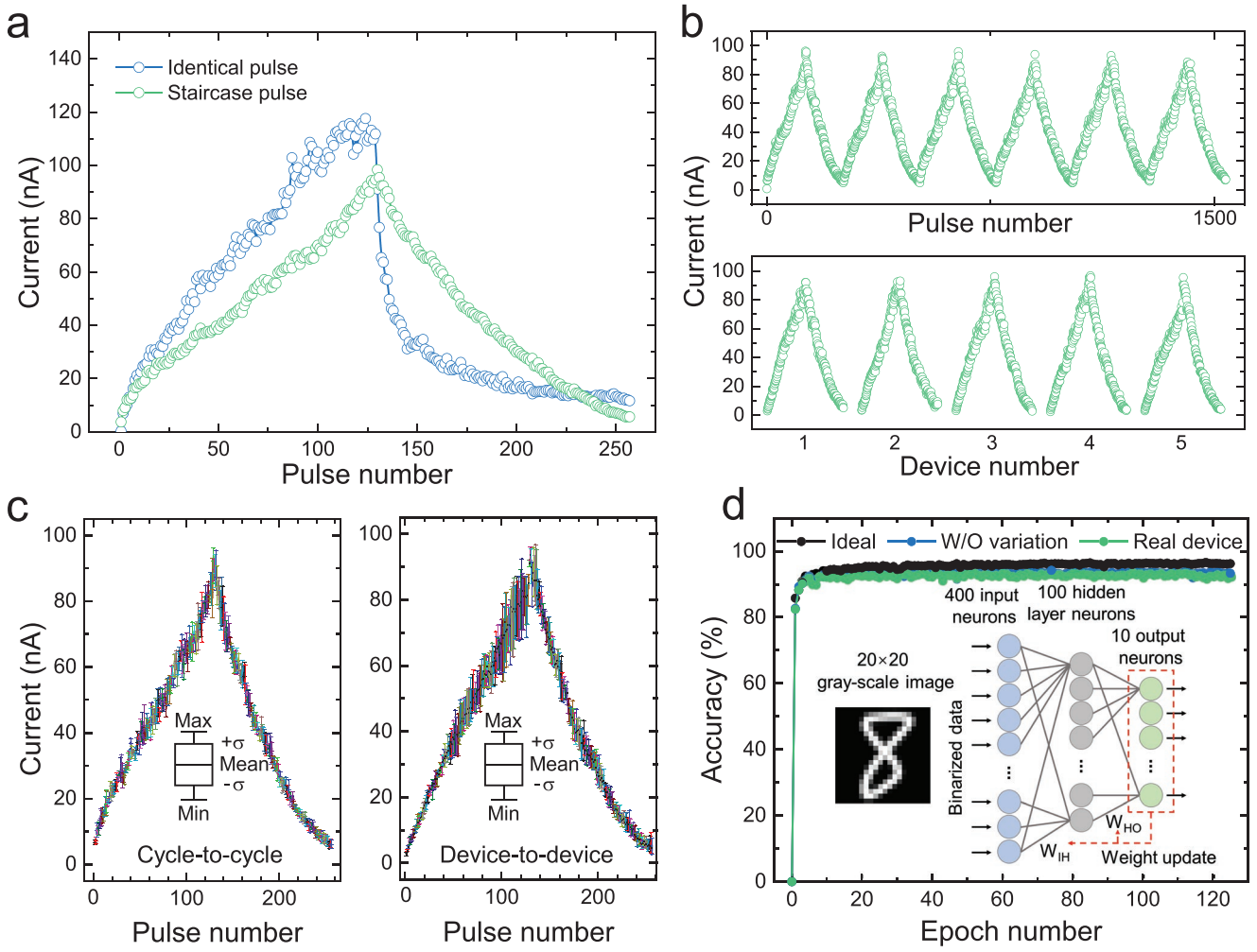

Figure 4. Weight update characteristics of the ferroelectric nitride memristor for neuromorphic computing and pattern recognition based on a two-layer MLP neural network. a) 7-bit potentiation and depression responses of the memristor to identical set/reset (blue, –7.8 V for potentiation and 2.7 V for depression) and staircase set/reset (green, from –7.6 V to –8.24 V in a 5 mV step for potentiation and from 1.9 V to 3.564 V in a 13 mV step for depression) pulse trains. The read pulse after each write pulse is –3 V and all pulse widths are 8 ms. b) Reproducible and uniform analog switching behavior over multiple cycles and on different devices under staircase pulse trains. c) Cycle-to-cycle variation and device-to-device variation characteristics of the memristor collected from 20 cycles and 10 devices. d) Comparison of simulated accuracies of the two-layer MLP based on ideal device (black, 128 states, on/off ratio of 50, perfect linearity), and based on nitride memristor with non-linearity property (blue) and further with cycle-to-cycle variation and device-to-device variation (green). The best recognition accuracy of 92.9% is achieved for ferroelectric nitride memristor with non-linearity and cycle-to-cycle/device-to-device variations.

memory/computing architecture based on nitride ferroelectrics, paving the way for homo and hybrid integrated functional edge devices beyond silicon.[61]

4. Experimental Section

Materials: The ScAlN/GaN heterostructure was grown by a Veeco GENxplor MBE system with a base chamber pressure of 10^{-11} Torr on commercial n-GaN templates. Active nitrogen (N^*, 6N purity) species were provided by a Vecco RF UNI-Bulb plasma source, while gallium (Ga, 7N purity), aluminum (Al, 6N5 purity), scandium (Sc, 5N purity, from American elements), and silicon (Si, 6N purity) sources were supplied using Knudsen effusion cells. 200-nm-thick Si-doped n^+-GaN was first grown as bottom contact layer after which ≈9 nm thick ScAlN with a nominal Sc content of 30% was grown under nitrogen rich condition. Some related growth conditions could be found in earlier reports.[30,34] Discussions on possible ways to integrate ScAlN with industrial CMOS technology could be found in Supporting Information, Note S6 (Supporting Information).

Device Fabrication: First, the ScAlN/GaN sample was cleaned in acetone, methanol, and deionized water with ultrasonic for 5 min in each step. Photolithography was first performed to pattern the sample surface after which 300-nm-thick SiO_2 was deposited by e-beam evaporation and windows for contacts were opened via lift-off. A second mask was used to define the top and bottom electrodes and the metal stack, comprising 50 nm Ti and 100 nm Au, was deposited by e-beam evaporation and released by lift-off in hot acetone.

Characterization: STEM specimens were prepared by a Thermo Fisher Scientific Helios G4 UXe focus ion beam (FIB) and STEM images were collected using a JEOL 3100R05 aberration-corrected STEM operated at 300 kV, with a collection range of 59–200 mrad for high-angle annular dark-field (HAADF) imaging. EDS maps were acquired with a Thermo

Fisher Scientific Talos F200X operated at 200 kV and equipped with the Super-X Detection System. The PUND transients were collected using a Radiant Precision Premier II ferroelectric tester driven from the top electrode. Current and capacitance were measured using B1500 semiconductor analyzer and Keithley 2400. The network simulations were performed using the open-source code "NeuroSim V3.0" in a Linux system and the optimization method "Adam" was selected with learning rate of 0.2 for weight update from input to hidden layer and learning rate of 0.1 for weight update from hidden to output layer, respectively. For baseline simulation, the conductance range was mapped to the real device while 128 states with ideal linearity and no cycle-to-cycle and device-to-device variation were considered.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Data available in article supplementary material or from the authors upon reasonable request.

Keywords

in-memory computing, large ON/OFF ratio, memory, nitride ferroelectrics, ScAlN, ultrathin

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