Power Processing Architectures for Sustainable Power and Energy

by

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DEDICATION

To my beloved parents for their endless love and support.

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ABSTRACT

Power processing transforms energy to be used for work, extracted from clean power generation, or stored effectively and sustainably. This thesis investigates (1) power processing architectures and methods to harvest power in solar photovoltaic (PV) systems efficiently, (2) power processing architectures and methods to employ second-use battery energy storage systems (2-BESS) optimally, and (3) temperature measurement of wide-bandgap power semiconductors, which are widely used in solar PV systems and battery energy storage systems (BESS).

The first part of this thesis focuses on architectures and methods for differential diffusion charge redistribution (dDCR) solar PV modules. These modules enable maximum power point tracking (MPPT) with cell-level granularity, which extracts nearly all the accessible power from each solar PV cell and is the best solution in terms of MPPT efficiency in solar PV systems. Since dDCR solar PV modules have two output ports, the conventional one-port hardware cannot be integrated with them. This thesis presents a new two-port up/down dc-dc MPPT converter and a new two-port hardware emulator for dDCR solar PV modules. Additionally, a new method for measuring diffusion capacitance in solar PV cells (an important parameter in dDCR modules) is introduced.

The second and third parts of this thesis investigate power processing architectures and methods in 2-BESSs for dc and ac applications. BESSs play important roles in grids, such as supporting renewable power systems like solar PV systems, voltage and frequency regulation for grid power quality improvement, and supporting electric vehicle (EV) fast charging. At the same time, second-use batteries from the exponential growth of EVs represent a challenge. Reusing the second-use EV batteries for stationary applications introduces a sustainable ap-

proach and adds economic value to these batteries. This thesis presents a new stochastic method for lite-sparse hierarchical partial power processing (LS-HiPPP) architecture to optimize 2-BESS power processing over the lifetime degradation of batteries. Additionally, a framework for optimizing multilevel ac battery energy storage systems (MAC-BESS) is introduced, which is particularly advantageous for 2-BESSs.

The fourth/last part of this thesis focuses on the accurate temperature measurement of the active area for wide-bandgap power semiconductors. High breakdown voltage, low on-resistance, and high speed have made wide-bandgap power semiconductors suitable for many applications, such as solar PV systems, BESSs, EVs, hybrid/electric aircraft, and wireless power transfer. However, the maximum power density of these devices is limited by the channel temperature rise. Thus, accurate temperature measurement of the active area is essential in research on wide-bandgap power semiconductors, often hampered by packaging and cooling methods.

CHAPTER I

Introduction

The sustainability of energy resources is one of the significant challenges for human beings. The shortage of conventional energy resources and the catastrophic results of their pollution, like the global warming crisis, escalates the problem. Therefore, we are looking for other resources like solar and wind energy to power our cities and industries, and for the same reasons, we are thinking of using electric vehicles (EV). Nevertheless, it is not that easy, and there are several challenges in using these clean energy resources. First of all, we need to spend energy to harvest renewable energy resources. The problem might be even more severe in using batteries to feed our cars. Secondly, we need specific and sometimes rare materials for these alternative solutions. Last but not least, using these alternative resources within the established infrastructures requires extra effort and adaptation. Power electronics is an essential part of the solution to these challenges. We can control and adapt the power and energy of these alternative resources by processing them through power electronics interfaces. Furthermore, we can make these alternative energy resources more efficient using power electronics, saving the energy and raw materials required to produce them. Therefore, it is not an exaggeration to say that power processing through power electronics is the central pillar of sustainable power and energy systems.

This thesis investigates (1) power processing architectures and methods to harvest power in solar photovoltaic (PV) systems efficiently, (2) power processing architectures and methods

to employ second-use battery energy storage systems (2-BESS) optimally, and (3) temperature measurement of wide-bandgap power semiconductors, which are widely used in solar PV systems and battery energy storage systems (BESS).

1.1 Solar Photovoltaic Systems

Solar power is one of the greatest alternative energy resources, with photovoltaics as the most prevalent harvesting platform. As an example, in the U.S., installation of the grid-connected distributed solar PV systems has increased from 800/year in 2000 to over 374000/year in 2019 [3]. One of the obstacles in solar PV systems is cell mismatch and partial shading. Reduction of accessible power, non-convexity in maximizing output power, and hotspots are some of the problems arising from mismatch and partial shading. In one example, 10% shading of a solar PV module can result in 30% total power loss [4]. Hence, addressing the partial shading and mismatch problems continue to be crucial research topics in solar PV systems—central maximum power point tracking (MPPT) [5], distributed MPPT [6, 7, 8], and differential power processing (DPP) [9, 10, 11, 12, 13, 14, 15, 16, 17, 18] are among those being investigated.

Diffusion charge redistribution (DCR) [19] is a switched-capacitor solution that enables one to perform MPPT with cell-level granularity using only a single module-level converter with differential diffusion charge redistribution (dDCR) as an architectural extension for DPP [20]. DCR and dDCR architectures rely on the intrinsic diffusion capacitance of the solar PV cells and do not require external energy storage elements. Note that most of the DPP methods require external energy storage components per PV element, including capacitors [9, 11, 12], inductors [13, 14], or transformers [10, 15, 16, 17, 18]. There have been efforts to use charge balancing of cells at the sub-module level, but not the cell level in [21, 22]. These methods use external capacitors for energy storage instead of the intrinsic diffusion capacitance of the solar PV cells. Recently, a modified DCR topology has been used to address cell and illumination mismatches in solar roofs for plug-in hybrid electric

vehicles (PHEVs) [4]. In comparison to dDCR, [4] does not perform DPP and has higher conduction losses than a comparable dDCR solar PV module.

Since the dDCR architecture is a two-port structure, it needs a two-port converter, and the conventional one-port converters, like boost converters, cannot be applied to dDCR solar PV modules. Similarly, the one-port PV emulators presented in the literature do not represent the behavior of the two-port dDCR solar PV modules; as an example, a one-port PV emulator cannot be used for evaluating and testing a two-port converter suitable for dDCR solar PV modules. It is worth noting that evaluating, validating, testing, and performing research on hardware components connected to actual solar PV systems can be challenging, and PV emulators are a common practical approach [23, 24, 25]. Thus, we need new hardware that can be integrated with dDCR solar PV modules to employ them and benefit from their advantages.

1.2 Second-Use Battery Energy Storage Systems

Battery energy storage systems play important roles in grids, such as supporting renewable energy systems like photovoltaics, voltage and frequency regulation for grid power quality improvement, and supporting EV fast charging [26, 27]. In 2019, 1.4 % of the small and 5 % of the large nonresidential solar PV systems in the U.S. employed BESSs, and this trend is increasing [3]. At the same time, the reduction of greenhouse gas (GHG) emissions by using electric vehicles and its impact on the transportation sector, as one of the largest contributors to GHG emissions (the largest in the U.S. [28]), has resulted in an exponential growth of EVs during recent years. As an example, electric delivery vehicles produce 25-38 % less GHG emissions than diesel delivery vehicles [28].

By 2030, there will be 200 GWh per year of used batteries from EVs [29]. When removed from the vehicle, these batteries still have approximately 80% capacity and power capability [30, 31] that could be used in grid storage or other stationary applications. Thus, reusing these batteries in 2-BESSs provides a sustainable solution that adds economic value to EV

batteries. However, reusing second-use batteries results in the challenge of a heterogeneous supply. Even with second-use batteries that are identical at the time of original manufacturing and installed in identical vehicles, these batteries, when removed, will exhibit a significant degree of variation. The conventional strategy for BESSs with heterogeneous batteries is to process all the power from every battery individually. This solution is expensive in terms of the enormous required power electronics and inefficient in terms of processed power. A typical strategy for BESSs using new batteries, which have a high degree of homogeneity, is partial power processing which reduces the cost of required power electronics and increases the system efficiency significantly. However, battery heterogeneity is a challenge in partial power processing structures for 2-BESSs. We recently introduced a new strategy for the partial power processing, lite-sparse hierarchical partial power processing (LS-HiPPP) [32, 33, 34] to overcome these challenges. However, we still need to address the heterogeneous degradation of batteries in 2-BESSs.

Note that although reusing retired batteries reduces the production-phase emissions from the production of new batteries for BESSs, the use-phase emissions of employing second-use batteries instead of new batteries need to be studied. Use-phase emissions depend on charging profiles of batteries [28], which can be different for new and second-use batteries based on the power processing architecture employed in the BESS. This topic is not covered in this research, but it is a rich subject for future work.

Multilevel converters with integrated batteries are perfect architectures for grid-connected BESSs. Directly producing multilevel ac from batteries reduces cost by eliminating the need for an explicit conventional inverter. Compared to conventional inverters with a high voltage dc bus, multilevel converters have better harmonic performance, which makes the required filters substantially smaller and cheaper [26], and are generally modular, which makes it possible to use smaller and faster switches. Additionally, by integrating batteries in multilevel converters, energy storage capacitors can be eliminated from the structure, which also reduces costs. Furthermore, multilevel converters provide a higher degree of freedom

for state-of-charge (SOC) balancing of the batteries, which is critical in BESSs [27]. Among multilevel ac battery energy storage systems (MAC-BESS), architectures based on cascaded H-bridges (CHB) and modular multilevel converters (MMC) are often used [26] with CHBs being among the best candidates [26, 27].

MMCs [35, 36] and CHBs [27, 37] with integrated batteries have been investigated in the literature. In [35], each sub-module includes one battery, one cell capacitor, one half-bridge, and one buck/boost indirect active interface (IAI), which connects the battery to the half-bridge. The sub-modules of [36] consist of one battery, one cell capacitor, one full-bridge, and one buck/boost IAI. These structures are suitable for applications with a common dc link and have more flexibility than CHB-based BESSs [26]. However, they need more active and passive components and have lower power efficiency than CHB-based BESSs [26]. In [37], each sub-module includes one battery and one full-bridge. In order to achieve SOC balancing, batteries are continuously sorted based on their SOCs, and then appropriate sub-modules are connected to the load. In [27], batteries rotate among different phases via a network of half-bridges and full-bridges in order to maintain SOC balancing for all three phases. These MMC-based and CHB-based methods need online SOC estimation, have relatively complicated control schemes that cannot be easily generalized to other multilevel converters, and sometimes rely on redundant batteries and auxiliary circuits. Furthermore, they do not address the challenges of heterogeneous second-use batteries.

1.3 Wide-Bandgap Power Semiconductors

Semiconductor devices are one of the key elements in power electronics that significantly affect the entire system's performance and efficiency. Power electronics used in sustainable energy resources like solar PV systems and BESSs or for sustainable energy consumption like EVs are not exempt from this fact. Therefore, using efficient and high-performance power semiconductors is critical in sustainable power and energy systems. Due to high breakdown voltage, low on-resistance, and high speed, wide-bandgap power semiconductors

are being used in many applications such as solar PV systems, BESSs, EVs, hybrid/electric aircraft, and wireless power transfer. However, the low thermal conductivity of the material and interfaces is typically one of the challenges in wide-bandgap power semiconductors like GaN-based [38] and β-Ga_2O_3-based [39] devices. Low thermal conductivity hinders heat transfer from the device, which leads to channel temperature rise and limits the maximum power density of such devices [40]. Particularly, GaN FETs utilize a two-dimensional electron gas (2DEG) as their channel, and the conduction loss within this thin layer is a highly concentrated heat source. Thus, accurate local temperature measurement of the active area is essential in research on wide-bandgap power semiconductors, such as cooling methods, packaging, and optimizing the partitioning of the switch modules. In the end, an accurate temperature measurement method for wide-bandgap power semiconductors will help to design more efficient and decent devices, which results in more efficient power electronics for various applications such as solar PV and battery energy storage systems.

1.4 Contributions and Organization of Thesis

The first research project of Chapter II studies a reconfigurable hardware emulator for dDCR solar modules. We employ charge transfer analysis to model the averaged behavior of switched-capacitor dDCR solar PV modules. We then use feedback and constraints to implement the obtained model in hardware. The second research project of Chapter II examines a two-port up/down dc-dc power converter capable of doing two-dimensional MPPT of dDCR solar modules. In addition to the novel topology, the control strategy for the converter is investigated, and its feasibility for performing MPPT is discussed. The dynamic parameters of solar PV cells, especially the intrinsic diffusion capacitance, are essential when connected to switched-mode converters [41] or used in switched-capacitor structures like dDCR structures [19, 20]. So, in the third research project of Chapter II, a new measurement method is investigated, which can measure the diffusion capacitance, the parasitic inductance, and the quality factor of the PV cells.

The first research project of Chapter III investigates a new stochastic optimization method for LS-HiPPP, which is an optimization over battery degradation. In other words, we want to optimize LS-HiPPP over the potential lifetime of the 2-BESS. In the second research project of Chapter III, a robust hierarchical system monitoring and control (SMC) is investigated, which consists of a central monitoring and control unit (CMCU) together with distributed monitoring and control agents (DMCA) for each battery and power conversion unit.

Chapter IV of this thesis presents a framework for optimizing a general class of multilevel ac battery energy storage systems, which is particularly advantageous for systems with heterogeneous (e.g., second-use) batteries. It is shown that, by adding partial power processing converters to a multilevel inverter, optimizing the power flow of these converters, and optimizing the switching sequence of the inverter's sub-modules, we could achieve perfect SOC balancing among the batteries while maximizing the output power of the BESS.

Chapter V of this thesis introduces an accurate temperature measurement method for wide-bandgap power semiconductors. We show that using a vector of three temperature sensitive electrical parameters, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, the temperature of the active area can be measured with high accuracy.

CHAPTER II

Maximum Power Point Tracking Converter for Differential Diffusion Charge Redistribution Solar Photovoltaic Modules [1]

2.1 Introduction

Solar power is one of the greatest alternative energy resources, with photovoltaics (PV) as the most prevalent harvesting platform. One of the obstacles in solar photovoltaic systems is cell mismatch and partial shading. Diffusion charge redistribution (DCR) [19] is a switched-capacitor solution that enables one to perform maximum power point tracking (MPPT) with cell-level granularity using only a single module-level converter with differential diffusion charge redistribution (dDCR) as an architectural extension for differential power processing (DPP) [20].

Since the dDCR architecture is a two-port structure, it needs a two-port converter, and the conventional one-port converters, like boost converters, cannot be applied to dDCR solar PV modules/panels. This thesis examines a two-port up/down dc-dc power converter capable of doing two-dimensional MPPT of dDCR solar panels. Similarly, the one-port PV emulators presented in the literature do not represent the behavior of the two-port dDCR solar PV modules; as an example, a one-port PV emulator cannot be used for evaluating

[1] This chapter is adapted from papers [42, 43, 44].

and testing a two-port converter suitable for dDCR solar PV modules. Thus, a two-port PV emulator and a two-port power converter for dDCR solar PV modules are investigated in this thesis. Furthermore, in switched-capacitor structures like dDCR solar configurations, the value of intrinsic diffusion capacitance of the cells limits the minimum appropriate switching frequency. Thus, a new measurement method for the diffusion capacitance of solar PV cells is studied.

2.2 Diffusion Charge Redistribution for Solar PV Systems

Diffusion charge redistribution balances all the average voltages of the cells in a solar PV module by using the large intrinsic capacitance of solar PV cells as energy storage while the charge is dynamically redistributed. Differential DCR is a method to extract the power so that only the mismatch power is processed by the dynamic charge redistribution.

2.2.1 PV Model

A commonly-used model for PV cells in PV emulator applications is the single-diode model [25]. The I-V relation of the single-diode model shown in Fig. 2.1(a) can be written [25] as

$$I = I_{\rm ph} - I_{\rm s}\left[\exp\left(\frac{V + IR_{\rm s}}{\alpha\frac{kT}{q}}\right) - 1\right] - \frac{V + IR_{\rm s}}{R_{\rm p}}, \tag{2.1}$$

where I is the PV cell current (A), V is the PV cell voltage (V), $I_{\rm ph}$ is the photo-generated current (A), $I_{\rm s}$ is the diode saturation current (A), $R_{\rm s}$ is the equivalent series resistance (Ω), $R_{\rm p}$ is the equivalent parallel resistance (Ω), α is the diode ideality factor, k is the Boltzmann constant (1.38×10^{-23} J/K), T is the absolute temperature of the junction (K), and q is the electron charge (1.6×10^{-19} C).

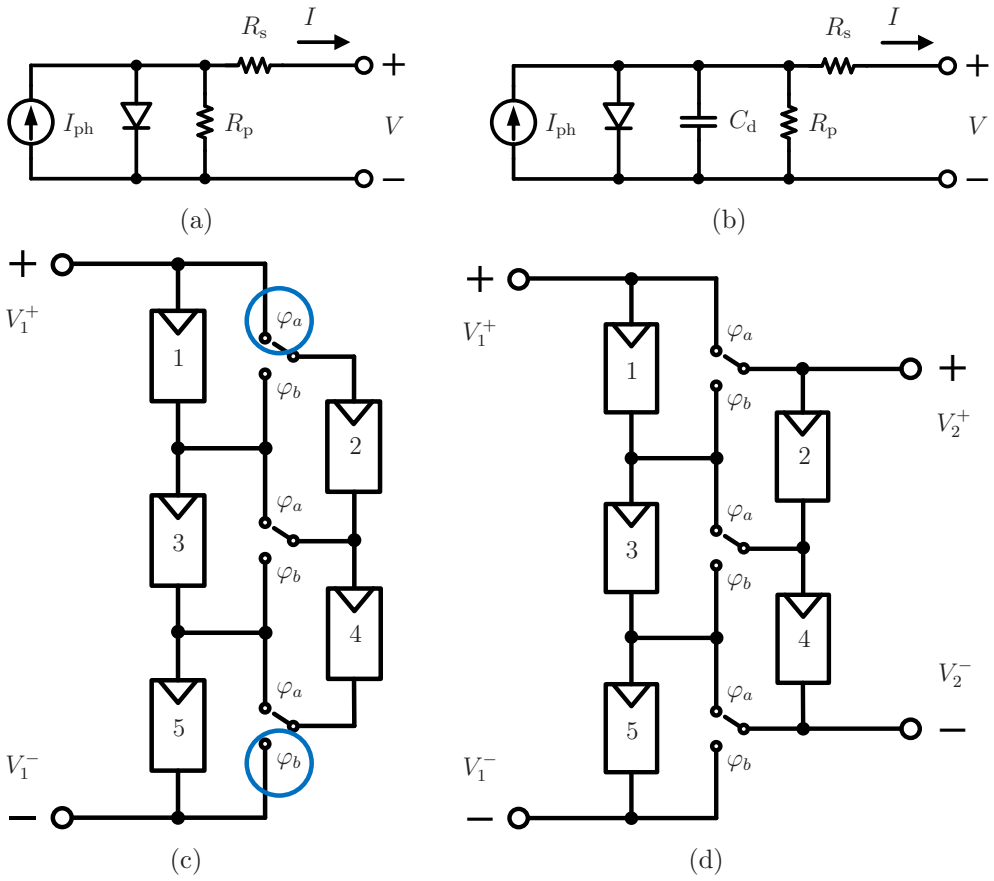


Figure 2.1: (a) Single-diode model of solar PV cells. (b) Modified single-diode model of solar PV cells. (c) 3×2 DCR structure. (d) 3×2 dDCR structure.

2.2.2 DCR and dDCR Modules

DCR is a switched-capacitor solution to the problems from cell mismatch and partial shading in PV systems by using the intrinsic diffusion capacitance of solar PV cells together with integrated semiconductor switches. This technique increases energy extraction and improves MPPT efficiency under mismatch and partial shading conditions [19]. In fact, it makes a solar PV module behave as a supercell [19] and enables us to perform MPPT with cell-level granularity using only a single module-level converter.

The diode capacitance C_{d} in the single-diode model in Fig. 2.1(b) represents a significant amount of capacitance [19]. The intrinsic diffusion capacitance C_{d} of a solar PV cell in [19] is as high as $10\,\mu$F. These intrinsic capacitances, together with semiconductor switches, form a switched-capacitor structure, which ultimately balances the average voltages among the solar PV cells. An example 3×2 DCR structure is shown in Fig. 2.1(c). However, this structure has one drawback in that all the power from the right string is necessarily processed through two switches, which are circled in Fig. 2.1(c); in other words, the current through these switches is not just the mismatch current as it for all the other switches, but rather the entire string current, hence causing a larger insertion loss.

To solve this problem, the dDCR architecture has been introduced [20] by adding a second port to the DCR architecture. An example 3×2 dDCR structure is shown in Fig. 2.1(d). The dDCR architecture preserves DPP by ensuring that only mismatch power is processed by the switches.

It should be noted that an important advantage of dDCR PV solar modules is that for practical implementations, where the losses from interconnects and switch resistances are small, the maximization of output power is convex with respect to (1) the sum of the output currents, and (2) the proportion of the current from each of the two strings, even under mismatched/partial shading conditions [20]. This makes it possible to perform a simple two-dimensional perturb-and-observe MPPT to find the maximum power point. As a result of this interesting property, the P-V curves of dDCR solar PV modules and also the

investigated emulator always have only one peak in contrast to the possible multi-peak P-V curves of conventional PV modules and emulators, even under mismatched/partial shading conditions. Note that, for the purposes of Chapter II, convexity is assumed homologous to concavity in that there is only one local optimum point, which is also the global optimum.

2.2.3 DCR and dDCR Principles of Operation

Solar PV modules that use DCR and dDCR in their simplest form consist of ladder structures that form two strings of solar PV cells in series. Cells of each string are individually shorted to particular cells of the adjacent string via semiconductor switches. A DCR or dDCR structure with $2N + 1$ solar PV cells consists of $2N + 2$ semiconductor switches. Figure 2.1 shows two examples: a 3×2 DCR and dDCR structure, each consisting of 5 PV solar cells and 6 semiconductor switches. The switches are denoted in Figs. 2.1(c) and 2.1(d) by their phases: the φ_a-switches alternately turn ON with the φ_b-switches at 50% duty cycle. To clarify the principle of operation in DCR and dDCR solar PV modules, the corresponding switched-capacitor structures of a 3×2 dDCR architecture during φ_a and φ_b are shown in Fig. 2.2(a) and Fig. 2.2(b), respectively. Figure 2.2 shows that during each phase, the diffusion capacitance C_{d} of each solar cell is shorted to the diffusion capacitance C_{d} of a particular solar cell from the adjacent string via two particular semiconductor switches. As a result, the average voltages of the cells become equal, even under partial shading and cell mismatch.

2.3 Reconfigurable Photovoltaic Emulator

Evaluating, validating, testing, and performing research on hardware components that are connected to actual PV systems can be challenging, and PV emulators are a common practical approach [23, 24, 25]. Temperature dependency along with cell variation and mismatch, which are time-dependent, often results in poor repeatability, and together with needing large physical space are among the obstacles to using actual solar PV panels [23, 24]. Fur-

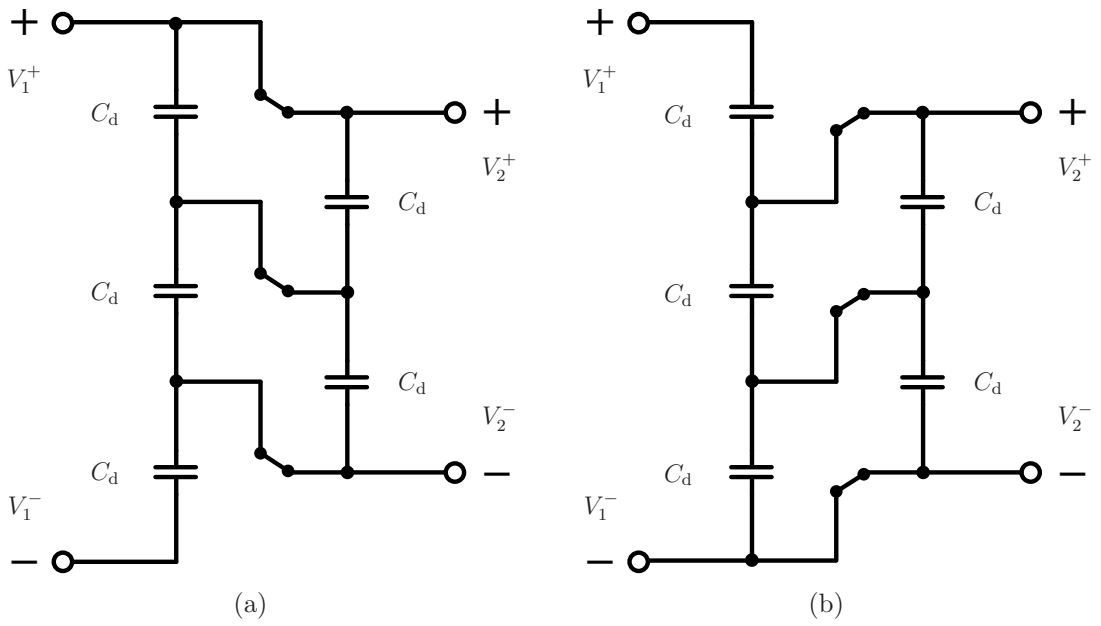


Figure 2.2: (a) The corresponding switched-capacitor structure of a 3×2 dDCR architecture during φ_a. (b) The corresponding switched-capacitor structure of a 3×2 dDCR architecture during φ_b.

thermore, to illuminate PV modules, a high-power controllable light source [24] is typically needed, making the required power supply bulky and expensive [25]; otherwise, one would struggle with the high variability of actual solar illumination [23].

In particular, there are additional challenges with DCR and dDCR solar PV modules because they contain integrated circuits (ICs). Preventing damage to prototype ICs is an additional concern that arises while performing actual-PV research on converters or inverters while connected to these modules or while trying different control algorithms; the risk is particularly great for the corner cases encountered in fault and failure testing. Generally, a PV emulator consists of two important parts: (1) the controller, which includes a PV model reference, and (2) the power stage. There are two types of controllers in the literature: analog and digital controllers; and two types of power stages: switching and linear [45].

Emulator controllers use analog or digital control loops together with analog representations, digital calculations, or digitally-stored tabulations of PV models as references [24]. Analog controllers are typically implemented with operational amplifiers (op-amps). Digital

controllers together with their references have been implemented on different computational platforms [24] including dSPACE [25, 46], DSPs [47, 48], microcontrollers [49], FPGAs [50], and ARM processors [51]. Examples of analog representations of PV models as a reference include using an actual PV cell [52, 53], a photosensor [54], an analog circuit [55], and a series-diode stack [53]. Digitally-implemented references are typically more flexible; for example, parameter changes to the PV model, like temperature and illumination level, can be imposed easily. However, digital implementations have a drawback in that current-voltage relationships are exponential, making quantization error a potential issue in either or both the analog-to-digital or digital-to-analog converter.

Switching-converter-based PV emulators use a switching power converter that is controlled to replicate the output characteristics of a solar PV module. Different dc-dc topologies are used including buck [25, 46, 48, 50], interleaved buck [52], buck-boost [49], forward [51], and full-bridge [47]. The disadvantages to switching-converter emulators include potential instability from interactions with other power electronics, such as MPPT converters, due to switching frequency and harmonic intermodulation and higher order converter dynamics.

Linear emulators [45, 56, 57, 58, 59, 60, 61, 62] do not have instability problems from switching intermodulation and higher order dynamics that are typical of switching-converters. Furthermore, quantization error is not an issue when analog controllers are used. However, analog implementations are not as flexible in setting model parameters (e.g. temperature, illumination, and shading) as emulators that use digital controllers.

As mentioned before, dDCR architecture is a two-port structure. Thus the one-port PV emulators presented in the literature do not represent the behavior of the two-port dDCR solar PV modules; as an example, a one-port PV emulator cannot be used for evaluating and testing a two-port converter suitable for dDCR solar PV modules. Thus, a two-port reconfigurable linear emulator with an analog controller is investigated in this thesis to replicate the averaged behavior of dDCR solar PV modules.

2.3.1 dDCR PV Emulator Concepts and Principles

Typical implementations of diffusion charge redistribution in a solar PV module have open-loop dynamics in that the behavior of the switches is dependent only on a fixed clock; intermodulation effects can be eliminated by synchronizing connected power converters to this clock. Under these conditions, a continuous-time PV emulator can represent the averaged behavior of the dDCR switched-system well.

2.3.1.1 Cell Mismatch and Partial Shading Equivalency

Partial shading or shading mismatch is when PV cells within a single module are under different levels of solar illumination. In other words, the cells, each represented by Fig. 2.1(b), have different corresponding photo-generated current I_{ph}. Cell mismatch, on the other hand, occurs when cells are physically different. In other words, the cells have different corresponding α, I_{s}, T, R_{s}, and/or R_{p} in (2.1). In this section, we show that these two phenomena manifest as electrical equivalents.

Assume that for a given mismatched solar PV cell α, I_{s}, T, R_{s}, and R_{p} have been changed to $(\alpha + \Delta\alpha)$, $(I_{\text{s}} + \Delta I_{\text{s}})$, $(T + \Delta T)$, $(R_{\text{s}} + \Delta R_{\text{s}})$, and $\left(R_{\text{p}} + \Delta R_{\text{p}}\right)$. For this cell, the mismatch appears as

$$I = I_{\text{ph}} - (I_{\text{s}} + \Delta I_{\text{s}}) \left[\exp\left(\frac{V + I\left(R_{\text{s}} + \Delta R_{\text{s}}\right)}{(\alpha + \Delta\alpha)\frac{k(T+\Delta T)}{q}} \right) - 1 \right] - \frac{V + I\left(R_{\text{s}} + \Delta R_{\text{s}}\right)}{R_{\text{p}} + \Delta R_{\text{p}}}. \tag{2.2}$$

This cell mismatch has a corresponding variation in photo-generated current ΔI_{ph} with the same voltage V and current I,

$$I = I_{\text{ph}} + \Delta I_{\text{ph}} - I_{\text{s}} \left[\exp\left(\frac{V + IR_{\text{s}}}{\alpha\frac{kT}{q}} \right) - 1 \right] - \frac{V + IR_{\text{s}}}{R_{\text{p}}}, \tag{2.3}$$

which results in

$$\begin{aligned}\Delta I_{\mathrm{ph}} = I_{\mathrm{s}} \left[\exp\left(\frac{V+IR_{\mathrm{s}}}{\alpha\frac{kT}{q}}\right)-1\right] + \frac{V+IR_{\mathrm{s}}}{R_{\mathrm{p}}} \\ -\left(I_{\mathrm{s}}+\Delta I_{\mathrm{s}}\right)\left[\exp\left(\frac{V+I\left(R_{\mathrm{s}}+\Delta R_{\mathrm{s}}\right)}{\left(\alpha+\Delta\alpha\right)\frac{k(T+\Delta T)}{q}}\right)-1\right] - \frac{V+I\left(R_{\mathrm{s}}+\Delta R_{\mathrm{s}}\right)}{R_{\mathrm{p}}+\Delta R_{\mathrm{p}}}.\end{aligned} \tag{2.4}$$

So, for each cell mismatch case $\left(\Delta\alpha, \Delta I_{\mathrm{s}}, \Delta T, \Delta R_{\mathrm{s}}, \Delta R_{\mathrm{p}}\right)$, there is an equivalent partial shading case $\left(\Delta I_{\mathrm{ph}}\right)$, which corresponds to the same cell terminal voltage V and current I.

2.3.1.2 Averaged Model for dDCR Solar PV Modules

In this section, the charge transfer model in [63] is used to model the time-averaged behavior of switched-capacitor dDCR solar PV modules. A dDCR solar PV module consisting of $2N+1$ cells is shown in Fig. 2.3(a). Replacing the cells in the dDCR structure with the modified single-diode model, neglecting the resistors, results in Fig. 2.3(b) and Fig. 2.3(c) for φ_a and φ_b, respectively.

In Figs. 2.3(b) and 2.3(c), $q^{\varphi}_{x,i}$ denotes the charge flow of the element x during phase φ, where i represents the PV cell number or output node. During φ_a, shown in Fig. 2.3(b), Kirchhoff's Current Law (KCL) for nodes $\mathcal{N}_i$ results in

$$\begin{aligned}q^a_{\mathrm{out},1} + q^a_{\mathrm{out},2} = q^a_{\mathrm{ph},2i-1} - q^a_{\mathrm{d},2i-1} - q^a_{\mathrm{c},2i-1} \\ + q^a_{\mathrm{ph},2i} - q^a_{\mathrm{d},2i} - q^a_{\mathrm{c},2i}\end{aligned} \tag{2.5}$$

for $i = 1, \ldots, N$. For node $\mathcal{N}_i$ during φ_a, photo-generated charges $q^a_{\mathrm{ph},2i-1}$ and $q^a_{\mathrm{ph},2i}$ enter the node; diode charges $q^a_{\mathrm{d},2i-1}$ and $q^a_{\mathrm{d},2i}$ exit the node; and capacitor charges $q^a_{\mathrm{c},2i-1}$ and $q^a_{\mathrm{c},2i}$ exit the node. Although (2.5) is clear for $\mathcal{N}_1$, it may not be obvious for other nodes unless one observes that for each node the sum of the intermediate charges, for example $\left(q^a_{\mathrm{int},1} + q^a_{\mathrm{int},2}\right)$ for node $\mathcal{N}_2$, is equal to $\left(q^a_{\mathrm{out},1} + q^a_{\mathrm{out},2}\right)$.

It is worth noting that KCL for node $\mathcal{N}_{N+1}$ leads to an equation that differs from (2.5),

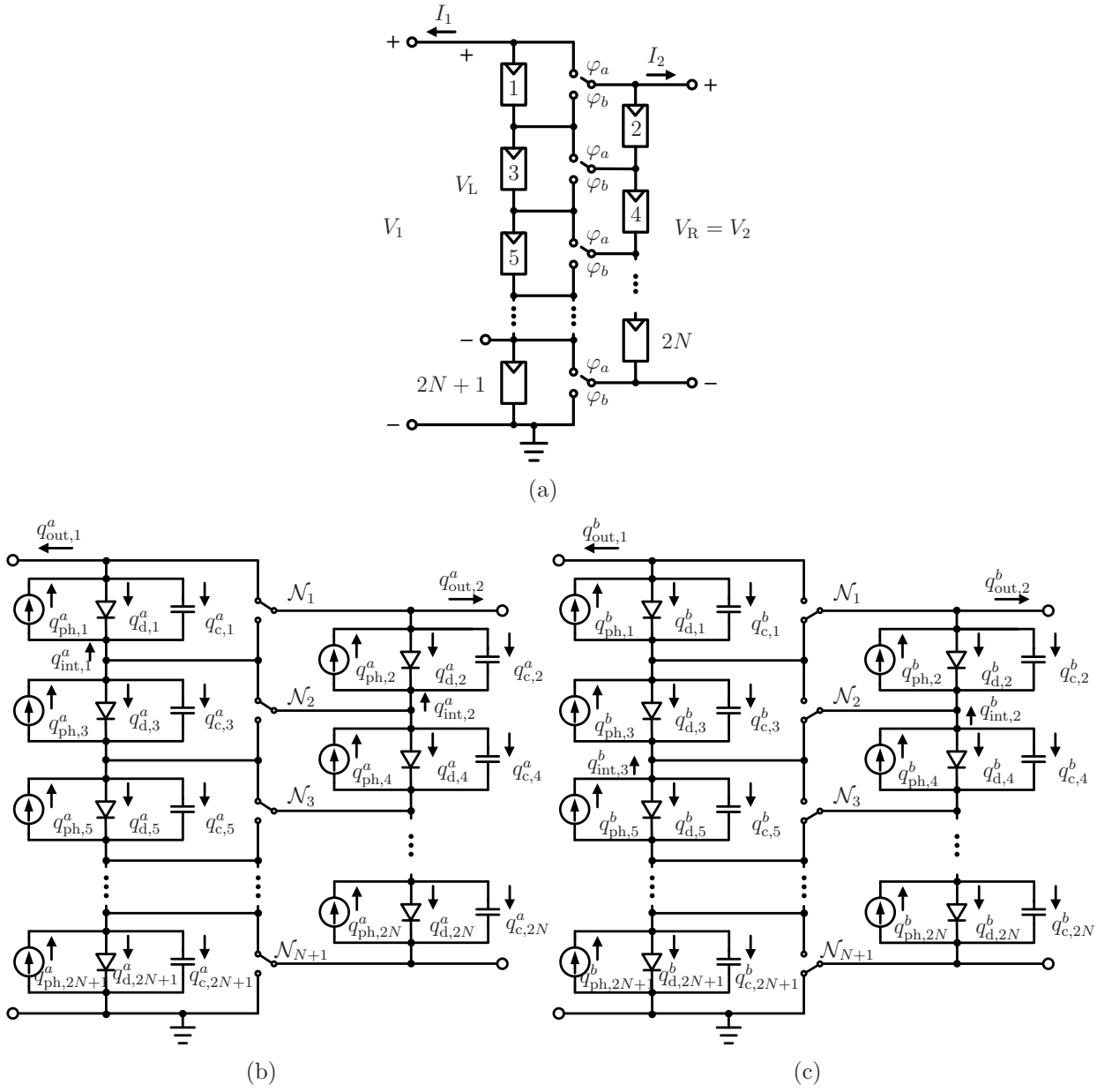


Figure 2.3: (a) dDCR structure with $2N + 1$ cells. (b) Charge flow during φ_a. (c) Charge flow during φ_b.

because there is no PV cell in the right string connected to this node from the top. KCL for this node gives

$$q^a_{\text{out},1} + q^a_{\text{out},2} = q^a_{\text{ph},2N+1} - q^a_{\text{d},2N+1} - q^a_{\text{c},2N+1} + q^a_{\text{out},2}. \tag{2.6}$$

For node $\mathcal{N}_i$ during φ_b, photo-generated charges $q^b_{\text{ph},2i-1}$ and $q^b_{\text{ph},2i-2}$ exit the node; diode charges $q^b_{\text{d},2i-1}$ and $q^b_{\text{d},2i-2}$ enter the node; and capacitor charges $q^b_{\text{c},2i-1}$ and $q^b_{\text{c},2i-2}$ enter the node. During φ_b, shown in Fig. 2.3(c), KCL for nodes $\mathcal{N}_i$ results in

$$\begin{aligned} q^b_{\text{out},1} + q^b_{\text{out},2} = q^b_{\text{ph},2i-1} - q^b_{\text{d},2i-1} - q^b_{\text{c},2i-1} \\ + q^b_{\text{ph},2i-2} - q^b_{\text{d},2i-2} - q^b_{\text{c},2i-2} \end{aligned} \tag{2.7}$$

for $i = 2, \ldots, N+1$. Again, for each node the sum of the intermediate charges, for example $\left(q^b_{\text{int},3} + q^b_{\text{int},2}\right)$ for node $\mathcal{N}_2$, is equal to $\left(q^b_{\text{out},1} + q^b_{\text{out},2}\right)$. During φ_b, KCL for node $\mathcal{N}_1$ leads to an equation that differs from (2.7), because there is no PV cell in the right string connected to this node from the bottom. KCL for this node gives

$$q^b_{\text{out},1} + q^b_{\text{out},2} = q^b_{\text{ph},1} - q^b_{\text{d},1} - q^b_{\text{c},1} + q^b_{\text{out},2}. \tag{2.8}$$

Summing the charge flows in each node from phases φ_a and φ_b, (2.5)–(2.8), results in

$$\begin{aligned} (N+1)\left(q^a_{\text{out},1} + q^b_{\text{out},1}\right) + N\left(q^a_{\text{out},2} + q^b_{\text{out},2}\right) = \\ + \sum_{i=1}^{2N+1}\left(q^a_{\text{ph},i} + q^b_{\text{ph},i}\right) - \sum_{i=1}^{2N+1}\left(q^a_{\text{d},i} + q^b_{\text{d},i}\right) \\ - \sum_{i=1}^{2N+1}\left(q^a_{\text{c},i} + q^b_{\text{c},i}\right). \end{aligned} \tag{2.9}$$

Note that capacitor charge balance in the steady state condition enforces

$$q^a_{\text{c},i} + q^b_{\text{c},i} = 0, \tag{2.10}$$

for $i = 1, \ldots, 2N+1$, which leads to

$$\begin{aligned}(N+1)\left(q^a_{\text{out},1} + q^b_{\text{out},1}\right) + N\left(q^a_{\text{out},2} + q^b_{\text{out},2}\right) = \\ \sum_{i=1}^{2N+1}\left(q^a_{\text{ph},i} + q^b_{\text{ph},i}\right) - \sum_{i=1}^{2N+1}\left(q^a_{\text{d},i} + q^b_{\text{d},i}\right).\end{aligned} \tag{2.11}$$

One observes that, $\left(q^a_{\text{out},1} + q^b_{\text{out},1}\right)$ and $\left(q^a_{\text{out},2} + q^b_{\text{out},2}\right)$ are the total charge of the first and second outputs V_1 and V_2, respectively, over a complete switching period. Also, $\left(q^a_{\text{ph},i} + q^b_{\text{ph},i}\right)$ and $\left(q^a_{\text{d},i} + q^b_{\text{d},i}\right)$ are the total charge of the i$^{\text{th}}$ current source and the i$^{\text{th}}$ diode, respectively, over a complete switching period. The time-averaged currents can be obtained by dividing the charge flows by the switching period T

$$(N+1)\,\bar{I}_1 + N\,\bar{I}_2 = \sum_{i=1}^{2N+1}\bar{I}_{\text{ph},i} - \sum_{i=1}^{2N+1}\bar{I}_{\text{d},i}, \tag{2.12}$$

where

$$\begin{aligned}\bar{I}_1 = \frac{q^a_{\text{out},1} + q^b_{\text{out},1}}{T}; \bar{I}_2 = \frac{q^a_{\text{out},2} + q^b_{\text{out},2}}{T}; \\ \bar{I}_{\text{ph},i} = \frac{q^a_{\text{ph},i} + q^b_{\text{ph},i}}{T}; \bar{I}_{\text{d},i} = \frac{q^a_{\text{d},i} + q^b_{\text{d},i}}{T}.\end{aligned} \tag{2.13}$$

Averaging the specific case of the charge transfer model in (2.11) resulted in (2.12), which agrees with the equation reported in [64].

dDCR enforces equal average cell voltages by transferring electrical charge among the cells. This can be represented by the following DCR constraint

$$\overline{V}_{\text{d},1} = \cdots = \overline{V}_{\text{d},2N+1} = \overline{V}_{\text{d}}, \tag{2.14}$$

where $\overline{V}_{\text{d},i}$ is the time-averaged voltage of the i$^{\text{th}}$ diode. In other words,

$$\overline{V}_{\text{d},i}(I_{\text{d},i}, I_{\text{ph},i}) = \overline{V}_{\text{d},j}(I_{\text{d},j}, I_{\text{ph},j}) = \overline{V}_{\text{d}} \tag{2.15}$$

even when there is a cell mismatch, which means

$$\bar{I}_{\mathrm{d},i} \neq \bar{I}_{\mathrm{d},j}, \tag{2.16}$$

or there is a shading mismatch, which means

$$\bar{I}_{\mathrm{ph},i} \neq \bar{I}_{\mathrm{ph},j}, \tag{2.17}$$

where $\overline{V}$ and $\bar{I}$ refer to time-averaged voltages and currents, respectively. However, because cell mismatch is equivalent to shading mismatch, equality of all $\overline{V}_{\mathrm{d},i}$ means that a variation in diode current can be transformed into a variation in photo-generated current

$$\Delta\bar{I}_{\mathrm{d}}(\Delta\alpha, \Delta T, \Delta I_{\mathrm{s}}, \Delta R_{\mathrm{s}}, \Delta R_{\mathrm{p}}) \mapsto \Delta\bar{I}_{\mathrm{ph}}. \tag{2.18}$$

Hence, we can make all $\bar{I}_{\mathrm{d},i}$ equal and encapsulate all the mismatches in $\bar{I}_{\mathrm{ph},i}$. Rewriting (2.12) gives

$$(N+1)\,\bar{I}_1 + N\,\bar{I}_2 = \sum_{i=1}^{2N+1} \bar{I}_{\mathrm{ph},i} - (2N+1)\,\bar{I}_{\mathrm{d}}. \tag{2.19}$$

2.3.1.3 Emulator Concept: Feedback and Constraints Approach

We take the time-averaged dDCR currents and voltages and map them to continuous-time currents and voltages in the analog emulator. Furthermore, we would like to simplify the dDCR structure by aggregating the current sources, separating the series-strings, and eliminating the switched-capacitor network while satisfying (2.14) and (2.19) using feedback and algebraic constraints. In this section, we show that the emulator in Fig. 2.4 is a correct simplification.

Observe that, for Fig. 2.3(a), (2.14) results in

$$V_{\mathrm{L}} = V_{\mathrm{R}} = N\,\overline{V}_{\mathrm{d}}. \tag{2.20}$$

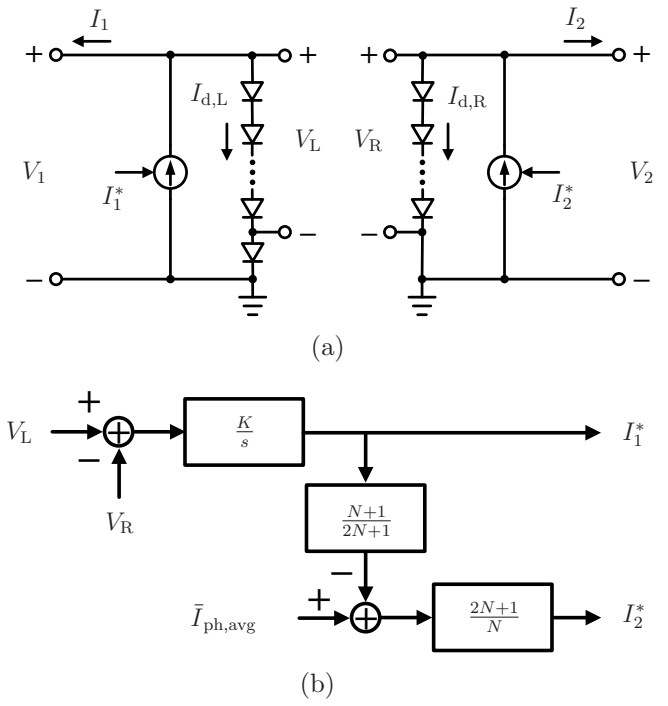


Figure 2.4: Emulator concept: (a) power stage, and (b) control stage.

This can be modeled by two series-diode stacks as shown in Fig. 2.4(a). It should be noted that the average voltage difference of two series-diode stacks is $\overline{V}_{\mathrm{d}}/2$. In other words, there is a small offset between V_1 and V_2, which can be approximately modeled by a single Schottky diode.

For the emulator in Fig. 2.4(a) we want

$$I_1^* - I_{\mathrm{d,L}} = I_1, \tag{2.21}$$

$$I_2^* - I_{\mathrm{d,R}} = I_2, \tag{2.22}$$

where

$$I_{\mathrm{d,L}} = I_{\mathrm{d,R}} = I_{\mathrm{d}}. \tag{2.23}$$

We use (2.21) and (2.22) to map the average currents in (2.19) to continuous-time currents

in the emulator and write

$$(N+1)\,I_1 + N\,I_2 = (N+1)\,I_1^* + N\,I_2^* - (2N+1)\,I_{\rm d}. \tag{2.24}$$

Now by comparing (2.19) and (2.24) one observes that

$$\sum_{i=1}^{2N+1} \bar{I}_{{\rm ph},i} = (N+1)\,I_1^* + N\,I_2^*, \tag{2.25}$$

which gives

$$\bar{I}_{\rm ph,avg} = \frac{\sum_{i=1}^{2N+1} \bar{I}_{{\rm ph},i}}{2N+1} = \frac{N+1}{2N+1} I_1^* + \frac{N}{2N+1} I_2^*, \tag{2.26}$$

where $\bar{I}_{\rm ph,avg}$ is the collective average of the time-averaged photo-generated current of all the cells. The control scheme that enforces (2.20) and (2.26) for Fig. 2.4(a) is shown in Fig. 2.4(b). In other words, the emulator in Fig. 2.4 replicates the time-averaged behavior of the dDCR structure in Fig. 2.3(a). The parameters needed to program the emulator are $\bar{I}_{\rm ph,avg}$ and N.

2.3.2 dDCR PV Emulator Hardware Implementation

The emulator elaborated in section 2.3.1 can be implemented using $v_{\rm be}$-multipliers [65], PFETs, op-amps, and difference amplifiers. A realization of the emulator shown in Fig. 2.4 is illustrated in Fig. 2.5.

2.3.2.1 Power Stage

The power stage of this emulator is linear and consists of closed-loop current sources and $v_{\rm be}$-multipliers.

- *Current Sources:* As shown in Fig. 2.5(a), each series-string uses a PFET in closed-loop as the current source. The current of the PFET is measured via a Hall-effect sensor, which outputs a voltage proportional to the current. An op-amp (A_1 or A_2) compares this

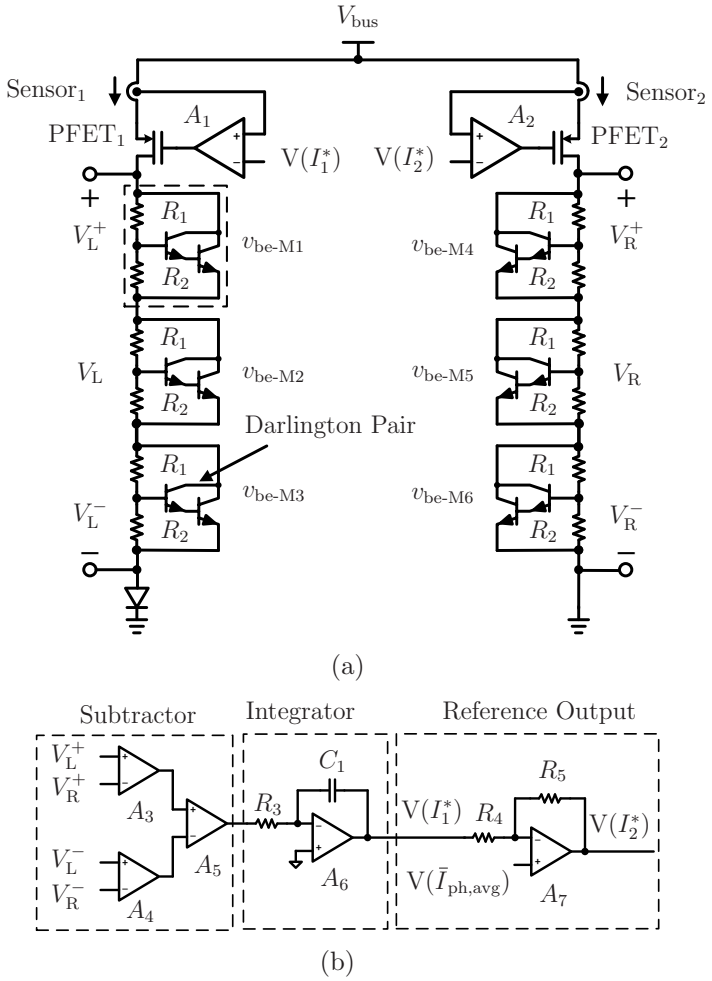


Figure 2.5: Emulator implementation: (a) power stage, and (b) control stage.

voltage to a reference voltage coming from the control circuit in Fig. 2.5(b), creating an appropriate gate voltage for the PFET. The currents of each PFET would be proportional to the respective reference voltages $\mathrm{V}(I_1^*)$ and $\mathrm{V}(I_2^*)$. It should be noted that level shifting is not shown in Fig. 2.5 for clarity.

• *v_{be}-multipliers:* To reduce the number of discrete power devices, two series-strings of v_{be}-multipliers denoted by $v_{\mathrm{be\text{-}M}}$ are used instead of two series-diode stacks. In this way, for each side in Fig. 2.5(a), three v_{be}-multipliers are used instead of 35 diodes (for a 70+1 cell module). It should be mentioned that the reason for using three v_{be}-multipliers instead of one is the limit on thermal dissipation.

Each v_{be}-multiplier consists of Darlington-connected BJTs and two resistors, which behave like a power diode with an approximate voltage drop of

$$V_{\mathrm{ON}} = 2 \times 0.7\,\mathrm{V} \times \frac{R_1 + R_2}{R_2}, \tag{2.27}$$

where 2 is the multiplicity of the Darlington pair and 0.7 V is the approximate voltage drop of a silicon diode. Using v_{be}-multipliers makes the emulator scalable, resizable, and easily reconfigurable by changing the values of R_1 and R_2. It will be discussed later how cell mismatch can also be easily implemented by changing these resistors. As mentioned previously, there is a small offset between the voltages of the two sides from the extra cell, which can be well-approximated by a single Schottky diode.

2.3.2.2 Control Stage

The control circuit in Fig. 2.5(b) realizes the controller in Fig. 2.4(b). This means that I_1^* and I_2^* are controlled in a way that (2.20) and (2.26) are satisfied.

• *Subtractor:* V_L and V_R are subtracted using unity-gain difference amplifiers ($A_3, A_4,$ and A_5), which corresponds to an error voltage. In fact, the positive $\left(V_L^+ \text{ and } V_R^+\right)$ and negative $\left(V_L^- \text{ and } V_R^-\right)$ ports of V_L and V_R are subtracted using A_3 and A_4, respectively. Then, the

outputs of A_3 and A_4 are subtracted via A_5.

• *Integrator:* After the subtractor stage, the error voltage is integrated by op-amp A_6, as shown in Fig. 2.5(b).

• *Reference Output:* The output of the integrator is the reference of the first current source $\mathrm{V}(I_1^*)$. Writing the equation for op-amp A_7 leads to

$$\mathrm{V}\left(\bar{I}_{\mathrm{ph,avg}}\right) = \frac{R_5}{R_4+R_5}\mathrm{V}\left(I_1^*\right) + \frac{R_4}{R_4+R_5}\mathrm{V}\left(I_2^*\right), \tag{2.28}$$

where $\mathrm{V}(I_2^*)$ is the reference of the second current source and $\mathrm{V}\left(\bar{I}_{\mathrm{ph,avg}}\right)$ is the reference of the average photo-generated current of the cells. Recall that the currents of the PFET current sources are proportional to the reference voltages, which can be written as

$$\mathrm{V}\left(I_1^*\right) = pI_1^*, \tag{2.29}$$

$$\mathrm{V}\left(I_2^*\right) = pI_2^*, \tag{2.30}$$

and

$$\mathrm{V}\left(\bar{I}_{\mathrm{ph,avg}}\right) = p\bar{I}_{\mathrm{ph,avg}} \tag{2.31}$$

where p is a proportionality factor. Substituting (2.29)–(2.31) into (2.28) results in

$$p\bar{I}_{\mathrm{ph,avg}} = \frac{R_5}{R_4+R_5}pI_1^* + \frac{R_4}{R_4+R_5}pI_2^*, \tag{2.32}$$

which leads to

$$\bar{I}_{\mathrm{ph,avg}} = \frac{R_5}{R_4+R_5}I_1^* + \frac{R_4}{R_4+R_5}I_2^*. \tag{2.33}$$

Now, by comparing (2.33) and (2.26) it can be easily obtained that to satisfy (2.26), it is sufficient to satisfy

$$\frac{R_4}{R_5} = \frac{N}{N+1}. \tag{2.34}$$

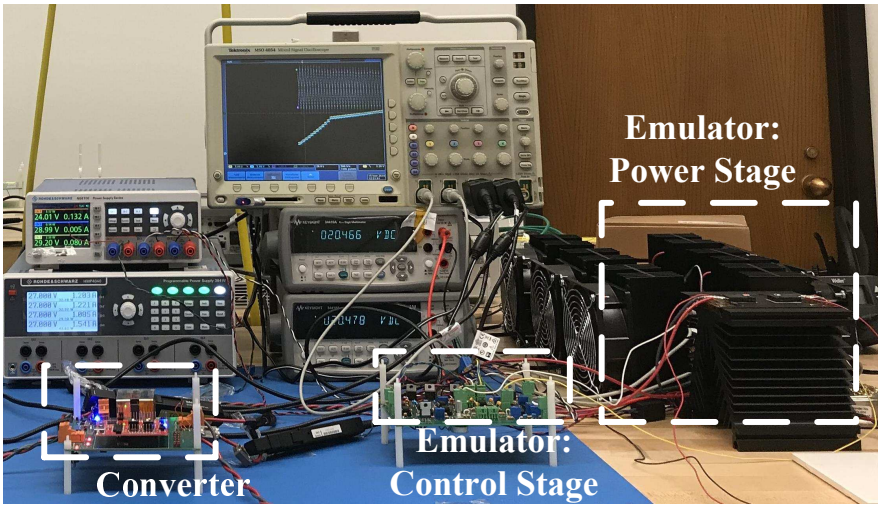


Figure 2.6: A photographs of the hardware setup.

Thus, R_4 and R_5 can be changed to emulate dDCR solar PV modules of different sizes. Also, $\bar{I}_{\text{ph,avg}}$, corresponding to the illumination level, can be set by changing $\text{V}\left(\bar{I}_{\text{ph,avg}}\right)$ via a potentiometer. This enables the emulator to be scalable, resizable, and easily reconfigurable.

2.3.3 Hardware Demonstration

A prototype of the dDCR emulator was constructed, evaluated, and tested in hardware. To vary output voltages and currents, the emulator was connected to the two-port converter discussed in Section 2.4. Figure 2.6 shows a photograph of the system.

2.3.3.1 Hardware Setup

In all the tests, the emulator was powered by a 27 V power supply (V_{bus} in Fig. 2.5(a)) and the load of the two-port converter was a constant 5 A current sink. Automated hardware experiments were performed to change I_1 and I_2, via the connected two-port converter. The output voltages and currents of the emulator were saved and maps of the emulator output characteristics under unshaded/matched conditions (Fig. 2.7(a) and Fig. 2.7(b)) and mismatched conditions (Fig. 2.7(c) and Fig. 2.7(d)) were obtained. It should be noted that the raw data is filtered and reduced in Fig. 2.7.

In the prototype, N is large (i.e. 35), so R_4 and R_5 are very nearly equal based on (2.34) and 10 kΩ resistors were used for R_4 and R_5. Also, the values of R_1 and R_2 were 127 Ω and 27 Ω, respectively. With these values, the voltage of each v_{be}-multiplier varied between 0 V and approximately 8 V. Therefore, the output voltages of the emulator, V_1 and V_2, varied between 0 V and approximately 24 V.

2.3.3.2 Hardware Results

• *Unshaded/Matched Conditions:* In this test, the behavior of the emulator under unshaded/matched conditions was evaluated. The experimental results are presented in Fig. 2.7(a) and Fig. 2.7(b). Figure 2.7(a) shows the experimental output contours of the emulator where the x-axis is the current ratio $\frac{I_1}{I_1+I_2}$ and the y-axis is the total current of the emulator $(I_1 + I_2)$. This result agrees with the simulation results for real switched-capacitor dDCR solar PV modules shown in [20] and shows the convexity of the total output power of the dDCR solar PV module with respect to $(I_1 + I_2)$ and $\frac{I_1}{I_1+I_2}$. Also, Trajectory 1 in Fig. 2.7(a), corresponding to a P-V curve slice at the power-optimal current ratio of 0.6, is plotted in Fig. 2.7(b). In this figure, the x-axis is V_1, and the y-axis is the total output power of the emulator. The P-V characteristic of the emulator is identical to that of a conventional solar P-V operating with a maximum power point of 100.3 W. Trajectory 2 in Fig. 2.7(a), corresponding to a P-V curve slice at the suboptimal current ratio of 0.3, is also plotted in Fig. 2.7(b). As shown, the maximum power point at this current ratio is 99.3 W, which is smaller than the one at the power-optimal current ratio.

• *Mismatched Conditions:* In this test, the behavior of the emulator under mismatched conditions was evaluated. To realize the mismatched condition, R_1 of $v_{\text{be-M5}}$ was changed from 127 Ω to 73 Ω and R_1 of $v_{\text{be-M2}}$ from 127 Ω to 102 Ω, which reduces the voltage and can, for example, represent partial shading. The experimental results are presented in Fig. 2.7(c) and Fig. 2.7(d). As shown, the experimental output contour has changed, and the maximum power occurs at a different current ratio; furthermore, the maximum power has been reduced.

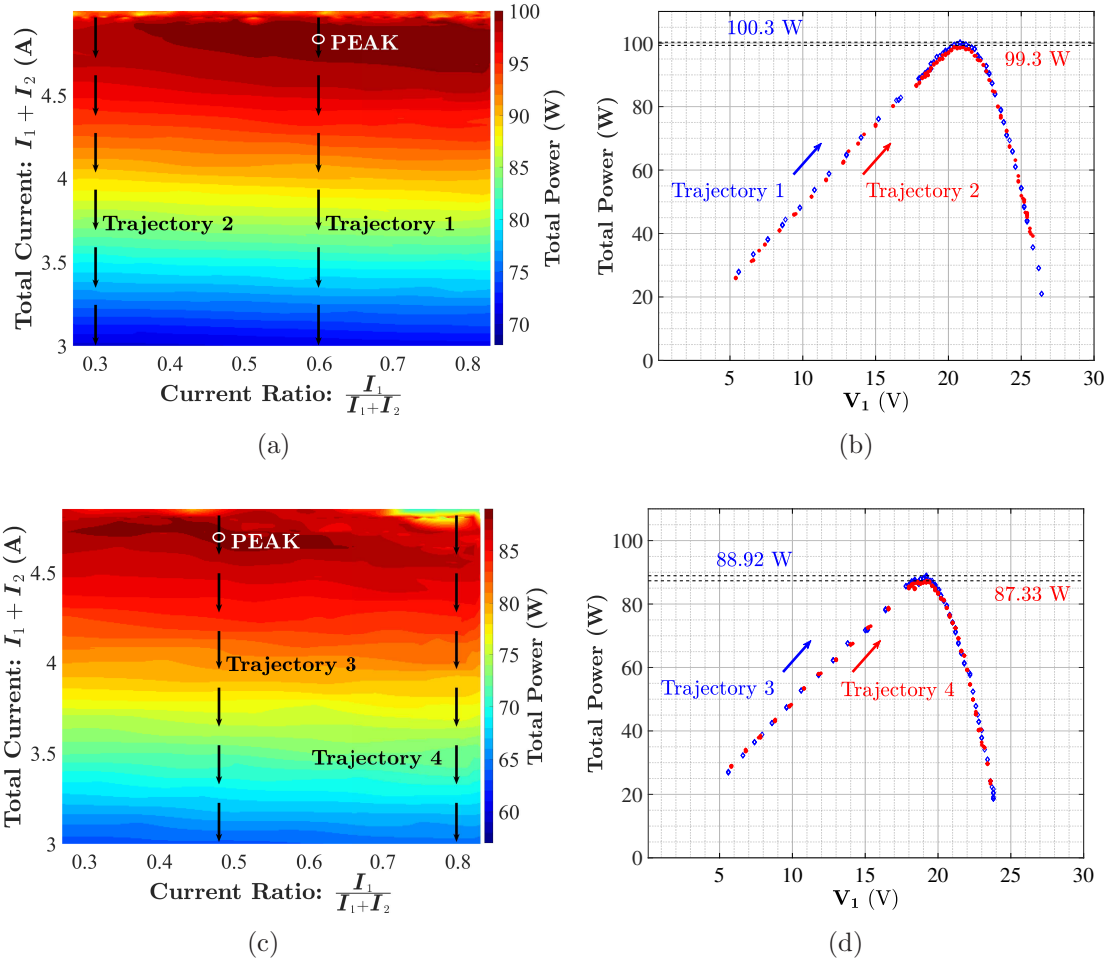


Figure 2.7: Hardware results: comparison of the emulator behavior under unshaded/matched and mismatched conditions. (a) The output contour under *Unshaded/Matched Conditions*. (b) The *P-V* curves for Trajectories 1 and 2, correspond to the power-optimal current ratio of 0.6 and the suboptimal current ratio of 0.3, respectively. (c) The output contour under *Mismatched Condition*. (d) The *P-V* curves for Trajectories 3 and 4, correspond to the power-optimal current ratio of 0.48 and the suboptimal current ratio of 0.8, respectively.

Trajectories 3 and 4, corresponding to a P-V curve slice at the power-optimal current ratio of 0.48 and a P-V curve slice at the suboptimal current ratio of 0.8, are plotted in Fig. 2.7(d). In this test, the P-V characteristic of the emulator at the power-optimal current ratio is identical to a uniformly-illuminated conventional solar P-V with a maximum power point of 88.92 W instead of 100.3 W. This demonstrates the result of an imposed mismatch on the emulator. Recall that cell mismatches are equivalent to shading mismatches, so this result could be interpreted as the behavior of the emulator under either cell or shading mismatched conditions. Note that this result agrees with the simulation results for real switched-capacitor dDCR solar PV modules shown in [20] and shows the convexity of the total output power of the dDCR solar PV module with respect to $(I_1 + I_2)$ and $\frac{I_1}{I_1+I_2}$, even under mismatched/shading conditions. Also, the maximum power point at the suboptimal current ratio of 0.8 is 87.33 W, which is smaller than that at the power-optimal current ratio.

2.4 Two-Port Up/Down DC-DC MPPT Converter

Since dDCR architecture is a two-port structure, it needs a two-port converter, and the conventional one-port converters, like boost converters, cannot be applied to dDCR solar PV modules. This thesis examines a two-port up/down dc-dc power converter capable of doing two-dimensional MPPT of dDCR solar panels. In addition to the novel topology, the control strategy for the converter is investigated, and its feasibility is discussed.

2.4.1 MPPT Converter Concepts

The converter presented here is a two-port up/down dc-dc converter that is capable of performing two-dimensional MPPT of dDCR solar panels. This converter has two modes of operation, boost mode, and buck mode. In the boost mode, the output voltage is higher than the average of the two input voltages, while in the buck mode, the output is less than the average input.

Because dDCR halves the voltage compared to a conventional panel with the same num-

ber of cells, the boost mode of operation is often a good choice for this application. By using the sum of the two input voltages as the output, cables with standard current-carrying capacities can be used for the same power level. In other words, the dDCR solar panel, together with the converter, behaves like a standard solar panel.

For the application in which the string is large, where the voltage is higher than the output dc bus, the buck mode can be utilized; for example, a residential panel configured for dDCR (22 V) can charge a 12 V battery.

A schematic view of the proposed converter is shown in Fig. 2.8(a). In Fig. 2.8(a), (V_1, I_1), (V_2, I_2), and (V_{out}, I_{out}) are the voltage current pairs of input 1, input 2, and the output of the converter, respectively. $V_{1,\text{measured}}$ and $V_{\text{out,measured}}$ are the measured voltages of input 1 and the output, respectively. It should be noted that no current sensors are used in the converter to reduce the costs and power losses. As a result, this converter cannot be used with a constant voltage load. However, with some modification in the control and using current sensors, it can be connected to a voltage sink as well.

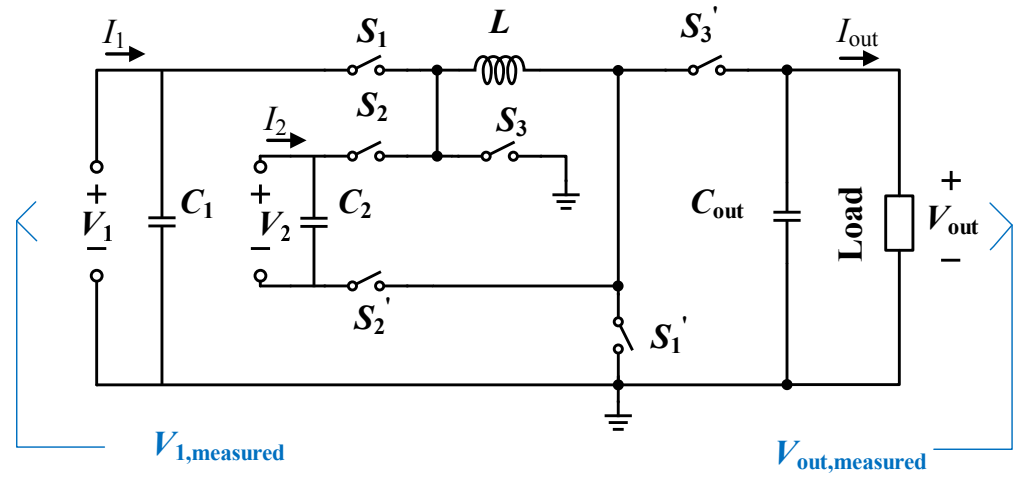
2.4.2 MPPT Converter Principles of Operation

The converter consists of one inductor, three capacitors, and six switches with a switching sequence shown in Fig. 2.8(b). When S_1 and S_1' are ON (Fig. 2.9(a)), the inductor is charged by the input 1. Similarly, when S_2 and S_2' are ON (Fig. 2.9(b)), the inductor is charged by the input 2. Finally, the inductor is discharged to the output capacitor and the load when S_3 and S_3' are ON (Fig. 2.9(c)). Invoking volt-second balance for the inductor gives

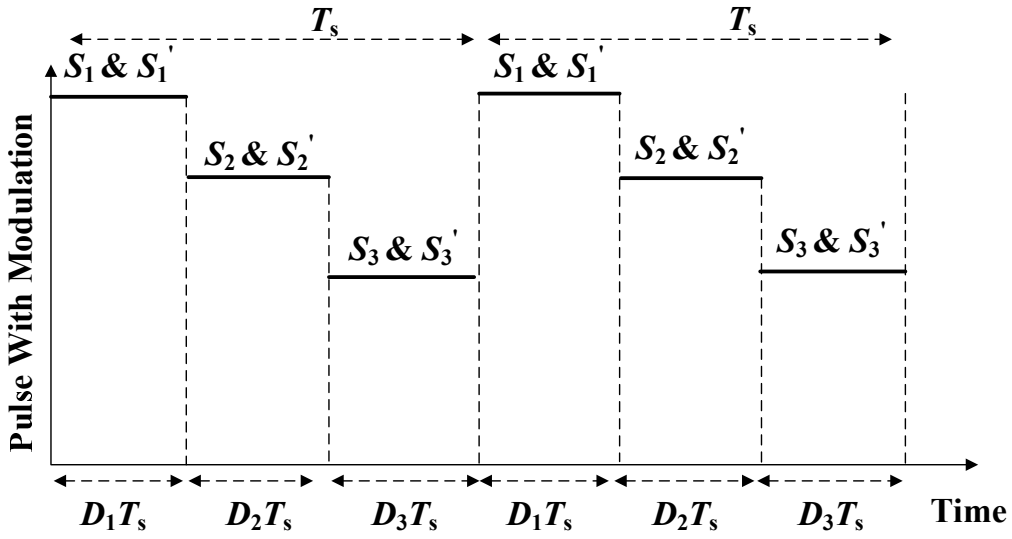
$$V_1 D_1 T_{\text{s}} + (-V_{\text{out}})\, D_3 T_{\text{s}} + V_2 D_2 T_{\text{s}} = 0, \tag{2.35}$$

which results in

$$V_{\text{out}} = \frac{V_1 D_1 + V_2 D_2}{D_3}, \tag{2.36}$$



(a)



(b)

Figure 2.8: (a) Schematic drawing of the converter. (b) Switching sequence of the converter.

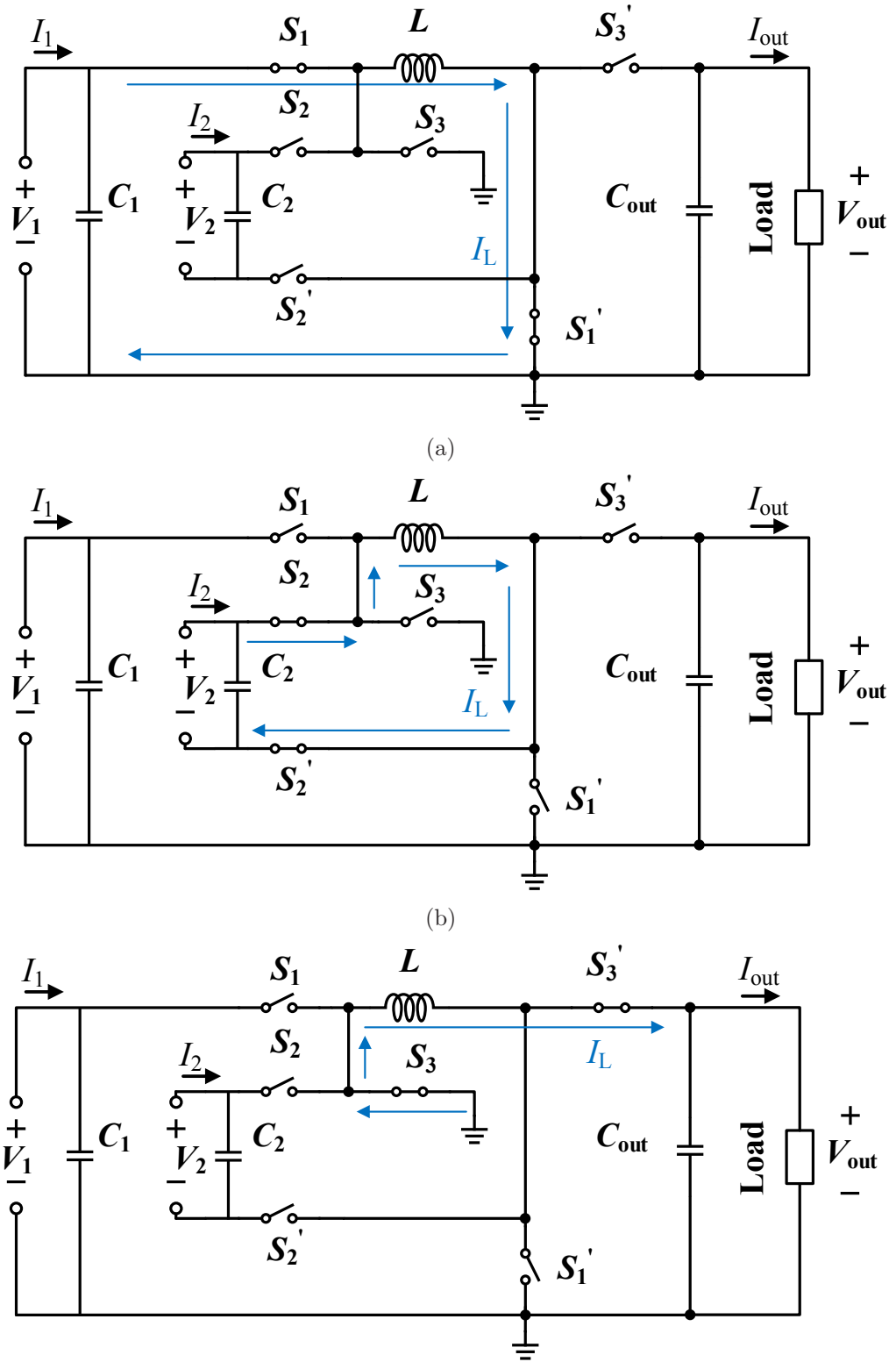


Figure 2.9: Path of I_{L} when: (a) S_1 and S_1' are ON, (b) S_2 and S_2' are ON, and (c) S_3 and S_3' are ON.

where D_1, D_2, and D_3 are the duty cycles of the switches (S_1 and S_1'), (S_2 and S_2'), and (S_3 and S_3'), respectively and T_s is the switching period. So, we have

$$D_1 + D_2 + D_3 = 1, \tag{2.37}$$

and (2.36) can be rewritten as

$$V_\mathrm{out} = \frac{V_1 D_1 + V_2 D_2}{1 - D_1 - D_2}. \tag{2.38}$$

Note that, switches S_3 and S_3' are unidirectional and can be replaced by diodes. However, we employed a synchronous architecture and used switches to lower the conduction losses. It is worth noting that based on the values of the duty cycles, V_out can be greater or smaller than $\frac{V_1+V_2}{2}$, and so the converter can work in either boost or buck modes. For a constant current load, invoking charge balance for C_1, C_2, and C_out gives

$$(I_\mathrm{L} - I_1)\, D_1 T_\mathrm{s} - I_1\, (1 - D_1)\, T_\mathrm{s} = 0, \tag{2.39}$$

$$(I_\mathrm{L} - I_2)\, D_2 T_\mathrm{s} - I_2\, (1 - D_2)\, T_\mathrm{s} = 0, \tag{2.40}$$

$$(I_\mathrm{L} - I_\mathrm{out})\, (1 - D_1 - D_2)\, T_\mathrm{s} - I_\mathrm{out}\, (D_1 + D_2)\, T_\mathrm{s} = 0, \tag{2.41}$$

respectively, which results in

$$I_\mathrm{L} = \frac{I_\mathrm{out}}{1 - D_1 - D_2} = \frac{I_1}{D_1} = \frac{I_2}{D_2}, \tag{2.42}$$

where I_L is the inductor current and I_out is the output current. For a constant resistive load, substituting

$$I_\mathrm{out} = \frac{V_\mathrm{out}}{R_\mathrm{out}}, \tag{2.43}$$

into (2.42) gives

$$I_\mathrm{L} = \frac{V_\mathrm{out}}{R_\mathrm{out}\, (1 - D_1 - D_2)} = \frac{I_1}{D_1} = \frac{I_2}{D_2}, \tag{2.44}$$

where R_{out} is the output resistive load.

2.4.3 MPPT Converter Controller Design

Generally, there are different choices for power converter variables to control; among them

- terminal variables such as input currents or voltages, output currents or voltages,
- internal states such as inductor currents,
- switch states such as average switch states (i.e. duty cycles), or cycle-by-cycle control of switches,

are some of the choices.

If the converter is an optimizing converter with an objective, such as MPPT of solar photovoltaic systems, the objective function should be a convex function of control variables. Furthermore, the valid area of operation in terms of control variables should be known to ensure that the optimum point is reachable via control variables. In other words, the feasibility of the control strategy ought to be proven.

In this thesis, two functions of terminal variables, i.e. voltage of input 1 and the ratio of input currents, are used as the control variables. It is shown that the total power is a convex function of the control variables when the source, i.e. the power of dDCR solar panels, is convex. In addition, it is shown that the converter can operate over the entire power range, and the control strategy is feasible.

2.4.3.1 Emulator Revisited

For the emulator in Fig. 2.4 we can write

$$I_1 = I_1^* - I_{0,1}\left(e^{\frac{V_1}{\alpha_1 V_{\text{t},1}}} - 1\right), \tag{2.45}$$

$$I_2 = I_2^* - I_{0,2}\left(e^{\frac{V_2}{\alpha_2 V_{\text{t},2}}} - 1\right), \tag{2.46}$$

$$\bar{I}_{\text{ph,avg}} = \frac{N+1}{2N+1} I_1^* + \frac{N}{2N+1} I_2^*. \tag{2.47}$$

where $I_{0,1}$, $V_{\text{t},1}$, and α_1 are the saturation current, thermal voltage, and ideality factor, respectively, of the equivalent diode of the left string in Fig. 2.4(a). Similarly, $I_{0,2}$, $V_{\text{t},2}$, and α_2 are the saturation current, thermal voltage, and ideality factor, respectively, of the equivalent diode of the right string in Fig. 2.4(a). For a large panel, i.e. large N, (2.47) can be rewritten as

$$\bar{I}_{\text{ph,tot}} = 2\bar{I}_{\text{ph,avg}} = I_1^* + I_2^*. \tag{2.48}$$

In addition, since $I_{0,1}$ and $I_{0,2}$ are very small (i.e. of order of 10^{-8} A [66]), we can approximate I_1 and I_2 as

$$I_1 = I_1^* - I_{0,1} e^{\frac{V_1}{\alpha_1 V_{\text{t},1}}}, \tag{2.49}$$

$$I_2 = I_2^* - I_{0,2} e^{\frac{V_2}{\alpha_2 V_{\text{t},2}}}. \tag{2.50}$$

Now, we encapsulate mismatches among the equivalent diodes of the two strings and also the length difference of the two strings in a positive variable termed β and rewrite (2.50) as

$$I_2 = I_2^* - I_{0,1} e^{\frac{\beta V_1}{\alpha_1 V_{\text{t},1}}}. \tag{2.51}$$

From (2.48), (2.49), and (2.51) we can write

$$I_1 + I_2 = \bar{I}_{\text{ph,tot}} - I_{0,1} \left(e^{\frac{V_1}{\alpha_1 V_{\text{t},1}}} + e^{\frac{\beta V_1}{\alpha_1 V_{\text{t},1}}} \right). \tag{2.52}$$

2.4.3.2 Controller Scheme

A block diagram of the controller is shown in Fig. 2.10, where $V_{1,\text{measured}}$ and $V_{\text{out,measured}}$ are the measured voltages in Fig. 2.8(a). Duty cycles for the switches are calculated from the compensator and MPPT controller. The MPPT block generates V_1^* and Cr^* based on the information from the previous cycle along with $V_{\text{out,measured}}$, where V_1^* is the reference

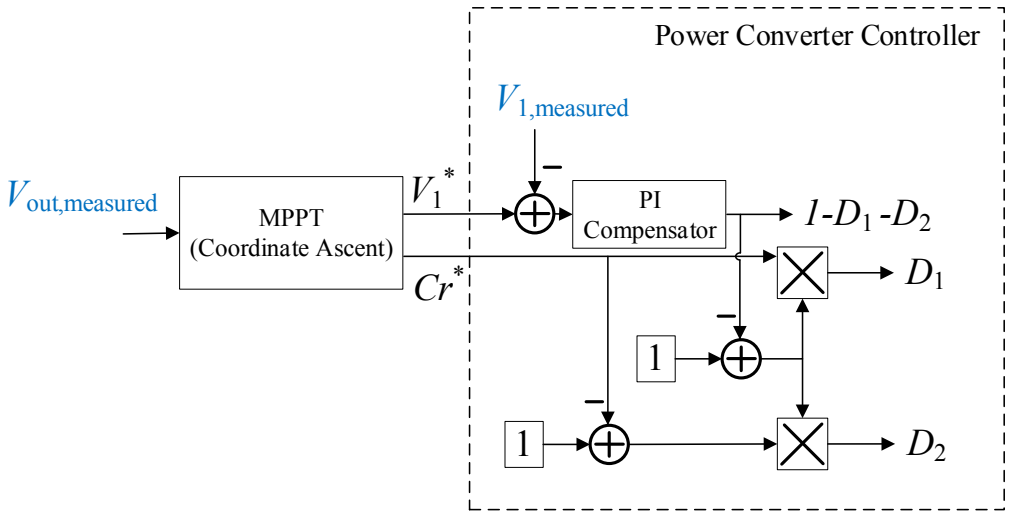


Figure 2.10: Block diagram of the digital controller.

voltage of the first input of the converter and Cr^* (i.e. current ratio) is defined as

$$Cr^* = \frac{D_1}{D_1 + D_2}. \tag{2.53}$$

V_1^* is then compared to $V_{1,\text{measured}}$ and the error goes to a PI compensator; the PI compensator then generates $1 - D_1 - D2$. Finally, D_1 and D_2 are calculated as

$$D_1 = Cr^* \left(D_1 + D_2\right), \tag{2.54}$$

$$D_2 = \left(1 - Cr^*\right)\left(D_1 + D_2\right). \tag{2.55}$$

2.4.3.3 Two-Dimensional MPPT

To perform two-dimensional MPPT, a simple coordinate ascent method is used [67]. The coordinate ascent method is an optimization algorithm that successively performs maximization along each coordinate direction (V_1^*, Cr^*) individually.

2.4.3.4 Feasibility of Control Strategy

The feasibility of finding the maximum power point is not immediately obvious. To perform MPPT, it is crucial that the chosen control variables are selected in a way that

- the output power is a convex function of the control variables,
- for every set of control variable values, there is a set of duty cycles with which the converter can operate,
- for every set of control variable values, there is a set of voltages and currents that satisfies the corresponding algebraic equations, and
- for every possible maximum power point, there is a set of control variable values that satisfies the corresponding algebraic equations.

To ensure feasibility, V_1^* and Cr^* are chosen as the control variables. The proof of convexity and feasibility follows.

- *Convexity:*

It had been shown in [20] that the total output power of the dDCR panel is convex with respect to $(I_1 + I_2)$ and Cr^*. Additionally, Fig. 2.7 shows that output power is convex with respect to V_1^*; like a huge normal PV cell in which the output power is convex with respect to the output voltage. Thus, we can claim that the total output power of the dDCR panel (or the emulator) is convex with respect to V_1^* and Cr^*.

- *Feasibility:*

Let's define the space of (V_1^*, Cr^*) as C, the space of (D_1, D_2) as D and the space of (V_1, I_1, V_2, I_2) as P. We want to prove that given $\bar{I}_{\text{ph,tot}}$ and I_{out} (for the constant current load case) or R_{out} (for constant resistive load):

1. for every vector $\vec{c} \in C$ there is a unique corresponding vector $\vec{p} \in P$,
2. for every vector $\vec{c} \in C$ there is a unique corresponding vector $\vec{d} \in C$,

3. for every vector $\vec{p} \in P$ there is a unique corresponding vector $\vec{c} \in C$.

◦ *Proof of Assertion 1: Given V_1^* and Cr^**

We simply can write

$$V_1 = V_1^*, \tag{2.56}$$

$$V_2 = \beta V_1^*. \tag{2.57}$$

Using (2.42) or (2.44), and (2.53) we can write

$$Cr^* = \frac{I_1}{I_1 + I_2}, \tag{2.58}$$

which results in

$$I_1 = Cr^* \left(I_1 + I_2\right), \tag{2.59}$$

$$I_2 = \left(1 - Cr^*\right)\left(I_1 + I_2\right). \tag{2.60}$$

Note that if

$$\bar{I}_{\text{ph,tot}} > I_{0,1}\left(e^{\frac{V_1}{\alpha_1 V_{\text{t},1}}} + e^{\frac{\beta V_1}{\alpha_1 V_{\text{t},1}}}\right), \tag{2.61}$$

substituting (2.56) and (2.57) into (2.52) gives

$$I_1 + I_2 = \bar{I}_{\text{ph,tot}} - I_{0,1}\left(e^{\frac{V_1^*}{\alpha_1 V_{\text{t},1}}} + e^{\frac{\beta V_1^*}{\alpha_1 V_{\text{t},1}}}\right). \tag{2.62}$$

Now, substituting (2.62) into (2.59) and (2.60) results in

$$I_1 = Cr^*\left(\bar{I}_{\text{ph,tot}} - I_{0,1}\left(e^{\frac{V_1^*}{\alpha_1 V_{\text{t},1}}} + e^{\frac{\beta V_1^*}{\alpha_1 V_{\text{t},1}}}\right)\right), \tag{2.63}$$

$$I_2 = \left(1 - Cr^*\right)\left(\bar{I}_{\text{ph,tot}} - I_{0,1}\left(e^{\frac{V_1^*}{\alpha_1 V_{\text{t},1}}} + e^{\frac{\beta V_1^*}{\alpha_1 V_{\text{t},1}}}\right)\right), \tag{2.64}$$

respectively. It is worth noting that (2.61) is the only necessary condition needed for calcu-

lating a set of (V_1, I_1, V_2, I_2), having V_1^* and Cr^*.

∘ *Proof of Assertion 2 for Constant Current Load: Given V_1^* and Cr^**

It had been proven that given V_1^* and Cr^* we can find a set of (V_1, I_1, V_2, I_2), if (2.61) is satisfied. Now, using (2.42) we can write

$$I_1 + I_2 = I_{\text{out}} \frac{D_1 + D_2}{1 - D_1 - D_2}, \tag{2.65}$$

which leads to

$$D_1 + D_2 = \frac{I_1 + I_2}{I_{\text{out}} + I_1 + I_2}. \tag{2.66}$$

Note that, if (2.61) is satisfied we have

$$I_1 + I_2 > 0, \tag{2.67}$$

which means that (2.66) satisfies $0 < D_1 + D_2 < 1$. Now, substituting (2.66) into (2.54) and (2.55) gives

$$D_1 = Cr^* \frac{I_1 + I_2}{I_{\text{out}} + I_1 + I_2}, \tag{2.68}$$

$$D_2 = (1 - Cr^*) \frac{I_1 + I_2}{I_{\text{out}} + I_1 + I_2}. \tag{2.69}$$

∘ *Proof of Assertion 2 for Constant Resistive Load: Given V_1^* and Cr^**

Similar to the constant current load case, given V_1^* and Cr^* we have a set of (V_1, I_1, V_2, I_2), if (2.61) is satisfied. Similar calculations lead to

$$\left(\frac{D_1 + D_2}{1 - D_1 - D_2} \right)^2 = \frac{R_{\text{out}} (I_1 + I_2)}{V_1 \left(Cr^* + \beta (1 - Cr^*) \right)}. \tag{2.70}$$

Again, as long as (2.61) is satisfied, (2.67) is satisfied, and since $0 < Cr^* < 1$ and $\beta > 0$, then

$$Cr^* + \beta (1 - Cr^*) > 0, \tag{2.71}$$

which means that

$$\frac{R_{\text{out}}\left(I_1+I_2\right)}{V_1\left(Cr^*+\beta\left(1-Cr^*\right)\right)}>0. \tag{2.72}$$

Now,

$$D_1+D_2=\frac{\sqrt{\frac{R_{\text{out}}(I_1+I_2)}{V_1\left(Cr^*+\beta(1-Cr^*)\right)}}}{1+\sqrt{\frac{R_{\text{out}}(I_1+I_2)}{V_1\left(Cr^*+\beta(1-Cr^*)\right)}}} \tag{2.73}$$

satisfies $0<D_1+D_2<1$. Note that the other solution for D_1+D_2 in (2.70) is not valid because it does not satisfy $0<D_1+D_2<1$. Finally, D_1 and D_2 can be calculated as

$$D_1=Cr^*\frac{\sqrt{\frac{R_{\text{out}}(I_1+I_2)}{V_1\left(Cr^*+\beta(1-Cr^*)\right)}}}{1+\sqrt{\frac{R_{\text{out}}(I_1+I_2)}{V_1\left(Cr^*+\beta(1-Cr^*)\right)}}}, \tag{2.74}$$

$$D_2=(1-Cr^*)\frac{\sqrt{\frac{R_{\text{out}}(I_1+I_2)}{V_1\left(Cr^*+\beta(1-Cr^*)\right)}}}{1+\sqrt{\frac{R_{\text{out}}(I_1+I_2)}{V_1\left(Cr^*+\beta(1-Cr^*)\right)}}}. \tag{2.75}$$

Again, (2.61) is the only necessary condition to have a set of (D_1, D_2), having V_1^* and Cr^*.

∘ *Proof of Assertion 3: Given V_1, I_1, V_2, I_2*

Given (V_1, I_1, V_2, I_2) satisfying (2.52), we can simply use (2.56) and (2.58) to calculate V_1^* and Cr^*, respectively.

2.4.4 Hardware Demonstration

To evaluate the capability of the converter in performing two-dimensional MPPT, prototypes of the converter and the emulator were constructed and tested. A photograph of the converter is shown in Fig. 2.11, and Fig. 2.6 shows a photograph of the system.

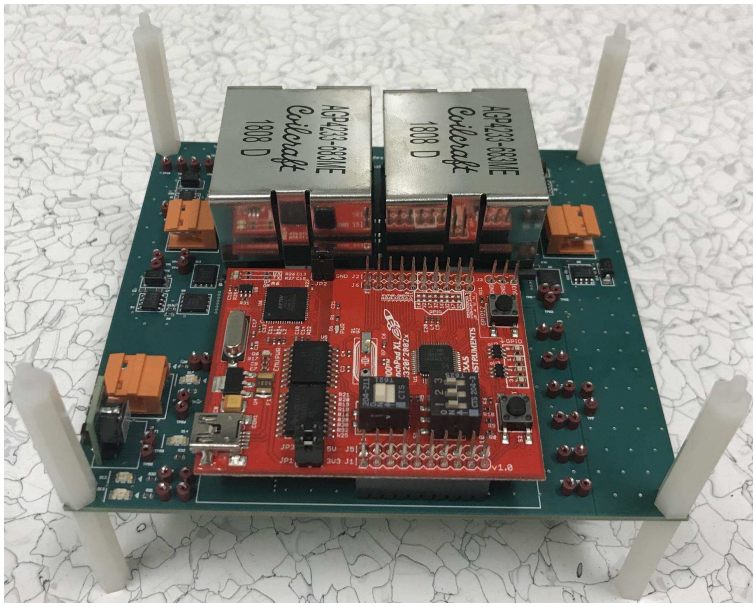


Figure 2.11: A photograph of the converter.

2.4.4.1 Hardware Setup

The components and the specifications of the converter are presented in Table 2.1 and Table 2.2, respectively. A Texas Instruments LAUNCHXL-F28027 kit is used for digital control. For digital control, a PI controller is used as the compensator. MPPT is performed every 50 ms and the perturbing step sizes are 0.2 V and 0.01 for V_1^* and Cr^*, respectively.

2.4.4.2 Hardware Results

In these tests, the emulator was supplied with 27 V at 8.5 A. The converter started-up in the closed-loop (i.e. without performing MPPT) from 6 different (V_1^*, Cr^*) starting points: (10 V, 0.3), (10 V, 0.5), (10 V, 0.7), (15 V, 0.3), (15 V, 0.5), and (15 V, 0.7), respectively. MPPT was then enabled after 1 s. In Fig. 2.12 and Fig. 2.13, trajectories 1, 2, 3, 4, 5, and 6 show the path toward the maximum power point when the starting (V_1^*, Cr^*) were (10 V, 0.3), (10 V, 0.5), (10 V, 0.7), (15 V, 0.3), (15 V, 0.5), and (15 V, 0.7), respectively.

- *Constant Current Load:*

  In this test, a constant current load of 4 A was used as the load. Fig. 2.12(a) and Fig.

Table 2.1: MPPT Converter Components

Parameter	Value
Input Capacitors	240 μF
Output Capacitor	200 μF
Inductor	34 μ H

Table 2.2: MPPT Converter Specifications

Parameter	Value
Nominal Input Voltages	20 V
Nominal Input Currents	10 A
Nominal Output Voltage	40 V
Nominal Output Current	10 V
Nominal Output Power	400 W
Switching Frequency	100 KHz

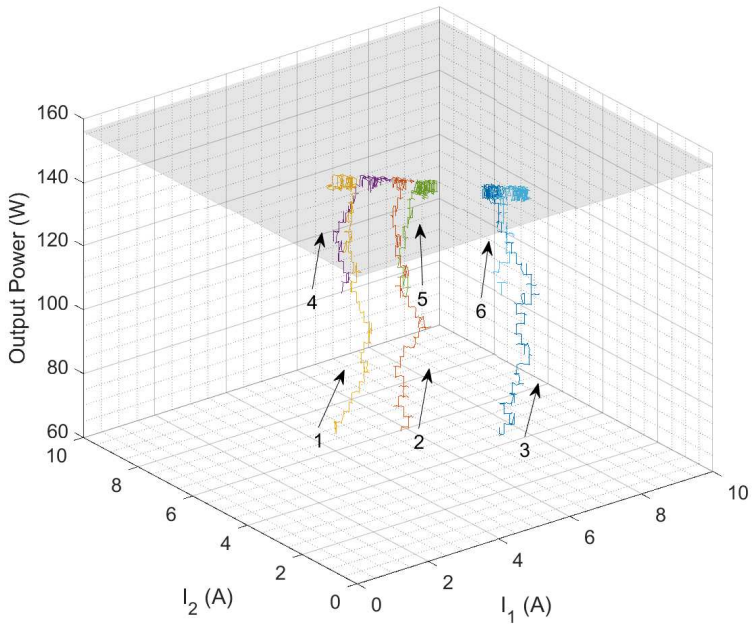
2.12(b) show that the maximum power point was consistently 156 W for the six cases. Fig. 2.14(a) shows I_1, I_2, V_{out}, and V_1 waveforms for the case with starting (V_1^*, Cr^*) set to (15 V, 0.3). It can be seen that in less than 2 s the maximum power point was reached.

• *Constant Resistive Load:*

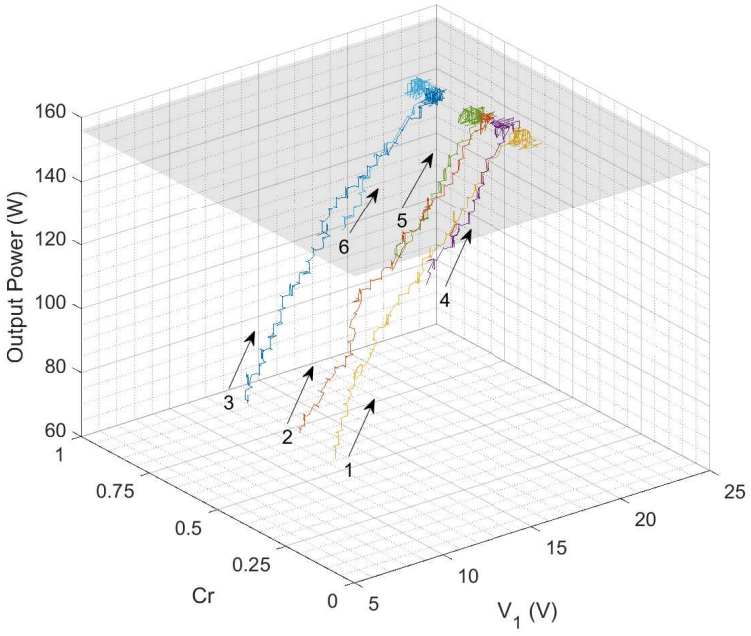
In this test, a constant resistive load of 10 Ω was used as the load. Similar to the constant current load case, Fig. 2.13(a) and Fig. 2.13(b) show that the maximum power point was consistently 156 W for the six cases. Fig. 2.14(b) shows I_1, I_2, V_{out}, and V_1 waveforms for the case with starting (V_1^*, Cr^*) set to (15 V, 0.3). Again, the maximum power point was reached in less than 2 s.

• *Discussion:*

As shown in Fig. 2.12(b) and Fig. 2.13(b), the value of V_1 at the maximum power point is about 21 V for all six cases. However, the final value of Cr^* appears different for different starting points. A possible explanation for this observation follows. Based on [20], although the total power of the dDCR panel is convex with respect to $(I_1 + I_2)$, it is not very sensitive to changes in Cr^* under uniform illumination and light shading conditions. Similarly, the total power of the dDCR panel is convex with respect to and strongly dependent on V_1.

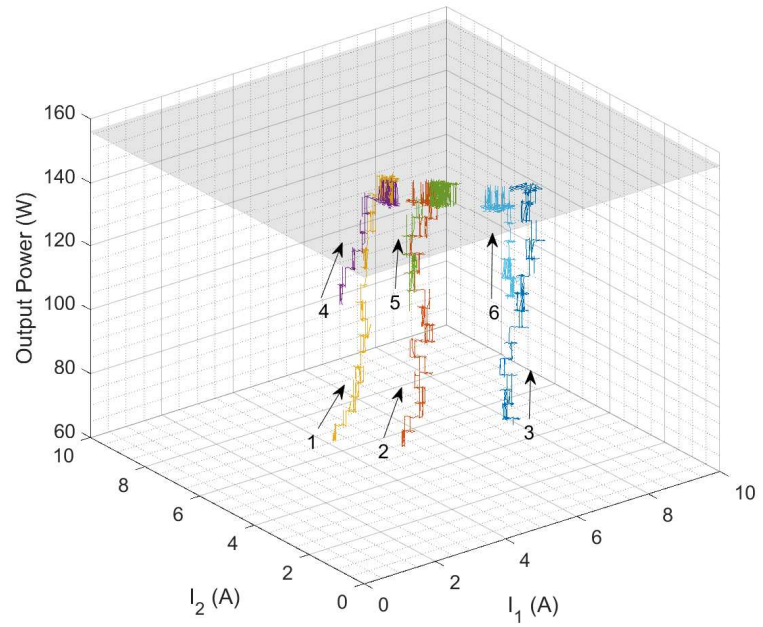


(a)

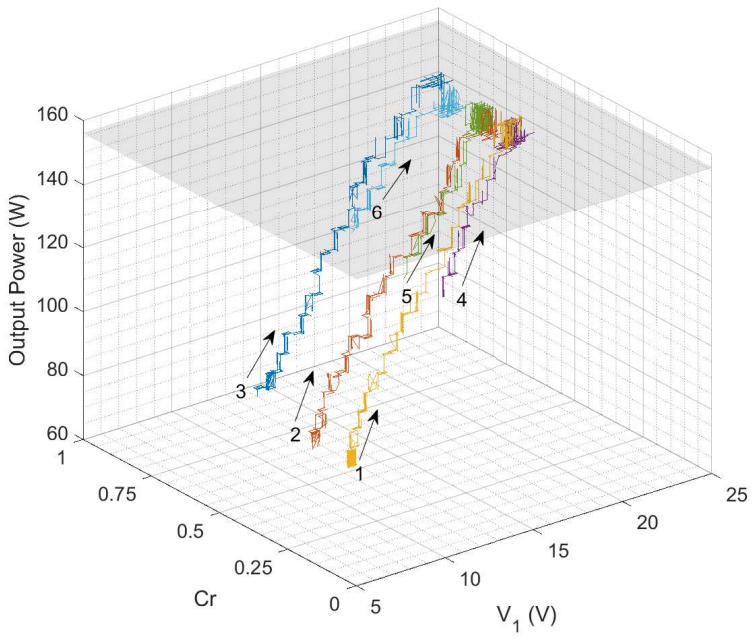


(b)

Figure 2.12: Hardware results for constant current load: (a) power versus I_1 and I_2, and (b) power versus V_1^* and Cr^*.

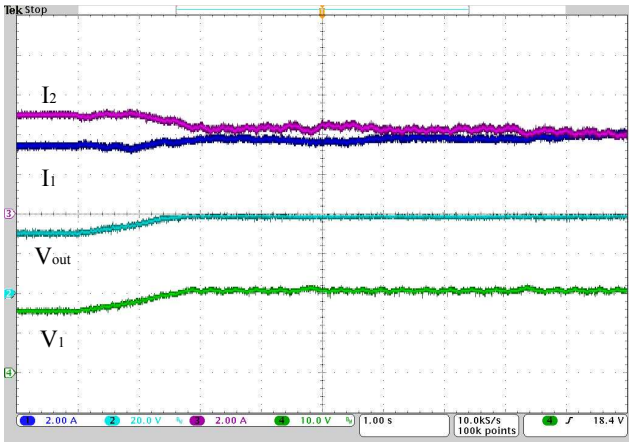


(a)

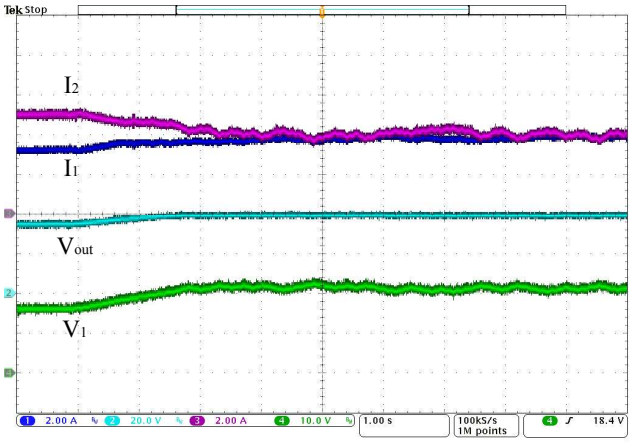


(b)

Figure 2.13: Hardware results for constant resistive load: (a) power versus I_1 and I_2, and (b) power versus V_1^* and Cr^*.



(a)



(b)

Figure 2.14: Hardware results: I_1, I_2, V_{out}, and V_1 waveforms for the case with starting (V_1^*, Cr^*) set to (15 V, 0.3) for: (a) constant current load, and (b) constant resistive load.

However, the power is relatively flat with respect to Cr^* near the maxima under uniform illumination and light shading conditions, which is the case for the above tests. Cr^* would be more important under severe partial shading conditions, e.g., when one side is drastically shaded.

2.5 Method for the Measurement of Diffusion Capacitance in Solar Photovoltaic Cells

To accurately model solar PV cells, we have to know their dynamic parameters and, in particular, the intrinsic diffusion capacitance. Solar PV systems are normally connected to switched-mode power converters, like maximum power point (MPP) tracking converters or inverters. The diffusion capacitance of solar PV cells is particularly important when they are connected to the switched-mode power converters [41]. In addition, in DCR solar configurations, the value of intrinsic diffusion capacitance of the cells limits the minimum appropriate switching frequency [19, 20]. Furthermore, the dynamic parameters of solar PV cells can be used to measure the minority carrier lifetime of solar PV cells.

Various small-signal methods have been introduced in the literature [4, 68, 69] to measure the diffusion capacitance of solar PV cells. The common disadvantage of these methods is that the solar PV cell is voltage-biased. Since diffusion capacitance is an exponential function of the diode voltage over the temperature, for a given voltage, diffusion capacitance varies greatly by temperature.

In contrast, diffusion capacitance is a linear function of the diode current over the temperature. In [19], a large-signal current-biased method has been introduced. Diffusion capacitance is measured ratiometrically by comparing the voltage slopes in two phases: when the cell is parallel to a known external capacitance and when it is disconnected from the external capacitance. The biasing point, however, can change based on the value of the external capacitance, as the results in [19] show. In [70], a small-signal current-biased method

has been introduced. Using a switch, a solar PV cell is periodically shorted to an external inductor and underdamped transient oscillation of the cell voltage is measured. Finally, the diffusion capacitance of the solar PV cell is calculated based on the measured voltage and the value of the external inductor. Adding an extra inductor helps to decrease the oscillation frequency and measure the capacitance at different test frequencies. However, the parasitic inductance of the solar PV cell has not been considered, which results in an error.

In this thesis, a new small-signal measurement method is investigated, in which the temperature dependency of the measurement is reduced by current-biasing the solar PV cell. By introducing a small sinusoidal perturbation and frequency sweeping, the minimum impedance frequency (ω_{min}) of the cell is determined, and the diffusion capacitance, the parasitic inductance, and the quality factor of the solar PV cell are calculated. This makes the method suitable for operando measurement of the parasitic inductance and the quality factor of a whole panel and all the interconnections. Furthermore, different external inductors are used to resonate the solar PV cells at different test frequencies. As a result, the diffusion capacitance, the parasitic inductance, and the quality factor can be measured at different frequencies.

2.5.1 Small-Signal Model of Solar Photovoltaic Cells

Figure 2.15 shows the small-signal model of solar PV cells [41] where C_{p} is the variable parallel capacitance, R_{ESR} models the dielectric losses, R_{s} is the equivalent series resistance, R_{p} is the variable parallel resistance, and L_{s} is the parasitic inductance of the cell. Note that C_{p} is the sum of the diffusion capacitance and the depletion layer capacitance. However, for positive voltages and near the MPP, the diffusion capacitance C_{d} dominates, and the depletion layer capacitance can be neglected [19, 41]. Here, the intended operating point range is positive and close to the MPP, and we focus on C_{d}. C_{d} varies by the diode voltage

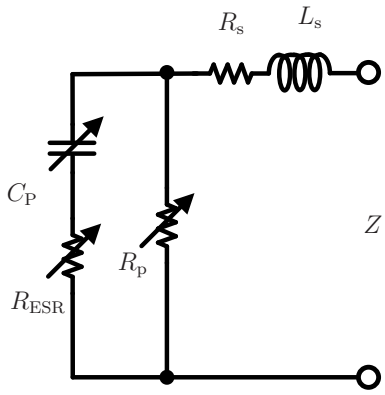


Figure 2.15: Small-signal ac model of solar PV cells.

and current as [19] shows:

$$C_d = \frac{\tau}{\alpha V_t} I_s \exp\left(\frac{V_d}{\alpha V_t}\right) = \frac{\tau}{\alpha V_t}\left(I_s + I_d\right) = \frac{\tau}{R_d}, \tag{2.76}$$

where V_d is the PV diode voltage (V), I_d is the PV diode current (A), R_d is the PV diode small-signal resistance (Ω), I_s is the PV diode saturation current (A), τ is the minority carrier lifetime (s), α is the PV diode ideality factor, and V_t is the thermal voltage. In Fig. 2.15, R_p is the equivalent parallel resistance of the static resistance, R_{sh}, and R_d. Note that R_d dominates at operation points near the MPP.

Figure 2.16 shows an example impedance plot of the small-signal model for a given operating point. At low frequencies, the impedance asymptotically goes toward $R_p + R_s$; at the middle frequencies, it looks like a capacitance; and at high frequency, it looks like an inductance [41].

2.5.2 Impedance Measurement Method

To measure the impedance of the small-signal model in Fig. 2.15, the solar PV cell is first current-biased by illuminating the cell. It is then connected to an ac current source, as shown in Fig. 2.17, to add a sinusoidal perturbation to the bias current.

It should be noted that R_o is required to prevent driving the current source directly

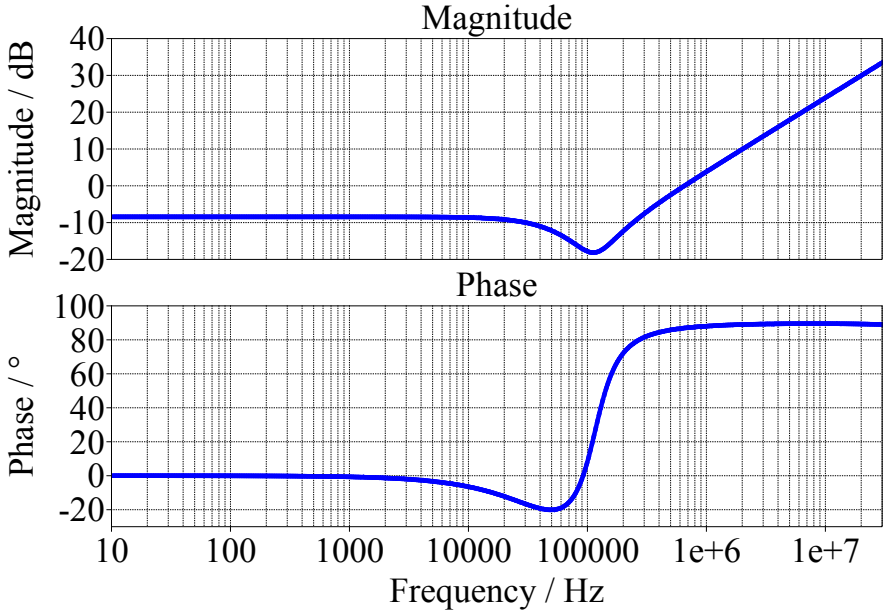


Figure 2.16: Example impedance plot of the small-signal ac model.

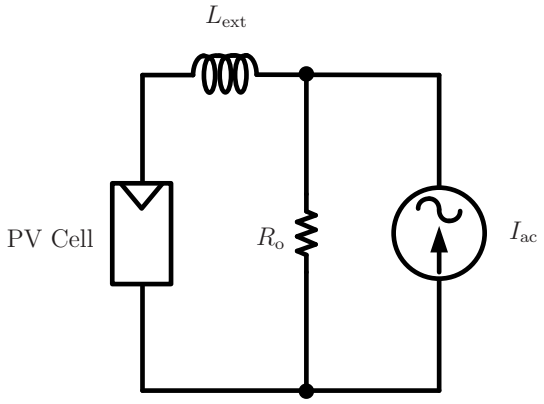


Figure 2.17: The schematic of the measurement setup.

into the inductor. As a result of adding R_{o}, the impedance magnitude in Fig. 2.16 is asymptotically pushed toward R_{o} at high frequencies. However, at low frequencies, R_{o} can be neglected as long as it is selected to be large enough, i.e. when $R_{\mathrm{o}} >> R_{\mathrm{p}} + R_{\mathrm{s}}$. As an interesting property of the RLC circuit in Fig. 2.17, there could be a dip even for low quality factors Q. This circuit has a different configuration in comparison to the conventional RLC filters, where you excite them with a source and measure the voltage or current of R, L, or C. Here, the pertinent impedance Z (in Fig. 2.15) in parallel to R_{o} is excited with a current source, and the voltage is measured across the entire pertinent impedance. As a result, the quality factor and asymptotic values of the impedance both take a part in the occurrence of a dip in the impedance curve.

An alternative approach for a sinusoidal perturbation is an ac voltage source. Because the solar PV cell is current-biased in the investigated method, a large resistor (R_{large}) would be needed in series with the ac voltage source to prevent shorting the bias current. As a result, the ac voltage source would necessarily be significantly large, i.e. $R_{\mathrm{large}} \times I_{\mathrm{pert}}$ for a sinusoidal perturbation of amplitude I_{pert}; a low voltage ac current source is easier and robust to implement over a wide range of frequencies.

Note that, as shown in Fig. 2.17, different external inductors can be added to the circuit to resonate the photovoltaic cells at different test frequencies; so the diffusion capacitance, the parasitic inductance, and the quality factor can be measured at these different frequencies.

2.5.3 Dynamic Parameters Calculations

After the measurement of the impedance, we need to calculate the parameters that determine the solar cell dynamics. The impedance of the small-signal model in Fig. 2.15 can be written

as

$$Z(j\omega) = \left[R_{\mathrm{s}} + \frac{R_{\mathrm{p}} + R_{\mathrm{p}} R_{\mathrm{ESR}} \left(R_{\mathrm{p}} + R_{\mathrm{ESR}} \right) C_{\mathrm{d}}^2 \omega^2}{1 + \left(R_{\mathrm{p}} + R_{\mathrm{ESR}} \right)^2 C_{\mathrm{d}}^2 \omega^2} \right] + j \left[L_{\mathrm{s}} \omega - \frac{R_{\mathrm{p}}^2 C_{\mathrm{d}} \omega}{1 + \left(R_{\mathrm{p}} + R_{\mathrm{ESR}} \right)^2 C_{\mathrm{d}}^2 \omega^2} \right]. \tag{2.77}$$

A possible approach to calculate the dynamic parameters is to resonate the circuit at different frequencies (using different external inductors), determine ω_{min} and measure the impedance magnitude at that frequency, and then solve for all the five unknowns. However, this approach is significantly complex, and the related fitting problem is usually not convex.

As shown in Fig. 2.16, near ω_{min}, the solar PV cell approximately behaves like an isolated series resonant circuit. This suggests that simplifying the model to a series resonant circuit near ω_{min} and collecting enough data near this point can yield useful information about the dynamic parameters of the solar PV cell. We may not be able to solve for all the unknowns, but we may be able to reliably calculate some pertinent ones.

2.5.3.1 Curve Fitting

If we encapsulate all the losses into one equivalent resistor, R_{tot}, and add L_{ext} to L_{s} to obtain the total inductance, L_{tot}, then the total impedance is

$$Z(j\omega) = R_{\mathrm{tot}} + j\omega L_{\mathrm{tot}} + \frac{1}{j\omega C_{\mathrm{d}}}. \tag{2.78}$$

As a series resonant circuit

$$R_{\mathrm{tot}} = \frac{Z_{0,\mathrm{tot}}}{Q_{\mathrm{tot}}}, \tag{2.79}$$

$$Z_{0,\mathrm{tot}} = \sqrt{\frac{L_{\mathrm{tot}}}{C_{\mathrm{d}}}}, \tag{2.80}$$

and

$$\omega_{0,\text{tot}} = \frac{1}{\sqrt{L_{\text{tot}} C_{\text{d}}}}. \tag{2.81}$$

Substituting (2.79), (2.80), and (2.81) into (2.78) leads to

$$Z\left(j\omega\right) = \frac{Z_{0,\text{tot}}}{Q_{\text{tot}}} + j\left(\frac{\omega Z_{0,\text{tot}}}{\omega_{0,\text{tot}}} - \frac{Z_{0,\text{tot}}\omega_{0,\text{tot}}}{\omega}\right), \tag{2.82}$$

and

$$\left|Z\left(j\omega\right)\right|^2 = \overbrace{\left(\frac{Z_{0,\text{tot}}}{\omega_{0,\text{tot}}}\right)^2}^{a}\omega^2 + \overbrace{\frac{\left(Z_{0,\text{tot}}\omega_{0,\text{tot}}\right)^2}{\omega^2}}^{b} + \overbrace{\left(\left(\frac{Z_{0,\text{tot}}}{Q_{\text{tot}}}\right)^2 - 2Z_{0,\text{tot}}^2\right)}^{c}. \tag{2.83}$$

On the other hand, by measuring the impedance at multiple points near ω_{min}, assuming $\omega_0 \approx \omega_{\text{min}}$, and fitting a second-order polynomial to the data like in Fig. 2.18, $\omega_{0,\text{tot}}$ can be calculated and the following equation constructed

$$\left|Z\left(j\omega\right)\right|^2 = q_1\omega^2 + q_2\omega + q_3. \tag{2.84}$$

Now by expanding the second-order Taylor Series of (2.83) around the calculated $\omega_{0,\text{tot}}$, we obtain

$$\left|Z\left(j\omega\right)\right|^2 = \overbrace{\left(a + \frac{3b}{\omega_{0,\text{tot}}^4}\right)}^{p_1}\omega^2 + \overbrace{\left(\frac{-8b}{\omega_{0,\text{tot}}^3}\right)}^{p_1}\omega + \overbrace{\left(c + \frac{6b}{\omega_{0,\text{tot}}^2}\right)}^{p_3}. \tag{2.85}$$

By comparing (2.84) and (2.85), the following system of equations can then be constructed

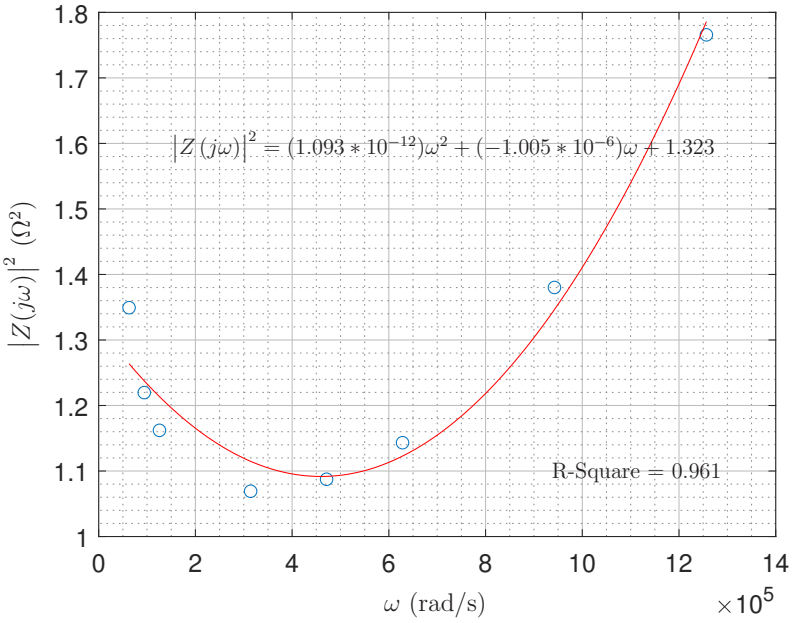


Figure 2.18: Example of the fitted curve to the measured data.

$$\begin{bmatrix} p_1 \\ p_2 \\ p_3 \end{bmatrix} = \begin{bmatrix} 1 & 3\omega_{0,\text{tot}}^{-4} & 0 \\ 0 & -8\omega_{0,\text{tot}}^{-3} & 0 \\ 0 & 6\omega_{0,\text{tot}}^{-2} & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} q_1 \\ q_2 \\ q_3 \end{bmatrix}. \tag{2.86}$$

If the system of equations (2.86) is solved for a, b, and c, we can then calculate C_d, L_tot, and Q_tot as

$$C_\text{d} = \frac{1}{\sqrt{b}}, \tag{2.87}$$

$$L_\text{tot} = \sqrt{a}, \tag{2.88}$$

and

$$Q_\text{tot} = \sqrt{\frac{1}{\frac{c}{\sqrt{ab}} + 2}}. \tag{2.89}$$

Finally L_{s}, and Q_{cell} can be calculated as

$$L_{\mathrm{s}} = L_{\mathrm{tot}} - L_{\mathrm{ext}}, \tag{2.90}$$

and

$$Q_{\mathrm{cell}} = \frac{\sqrt{\frac{L_{\mathrm{s}}}{C_{\mathrm{d}}}}}{\frac{Z_{0,\mathrm{tot}}}{Q_{\mathrm{total}}} - R_{\mathrm{ext}}} \tag{2.91}$$

where R_{ext} is the resistance of L_{ext}.

As expected, by simplifying the model to a series resonant circuit near ω_{min} and collecting enough data near this point, we are able to calculate three important parameters, i.e. the diffusion capacitance, the parasitic inductance, and the quality factor. Although, we are not able to solve for all the unknowns, and we cannot distinguish among different loss mechanisms.

As a summary, to calculate the dynamic parameters of the solar PV cell, the following is performed: (1) measure the impedance near ω_{min}; (2) fit a second-order polynomial to the data; (3) construct an analytical second-order function for the impedance through a Taylor Series approximation; (4) construct a system of equations using two equivalent second-order functions; and (5) solve for the dynamic parameters.

2.5.4 Measurement Circuits

Figure 2.19 shows a schematic of the ac current source and the measurement circuit designed for the investigated measurement method. A PNP transistor, in a feedback loop closed by op-amp A_1, acts as the ac current source where the ac current value is determined by $\frac{V_{\mathrm{ac}}}{R_{\mathrm{sense}}}$. Additionally, an NPN transistor biases the PNP transistor. Note that both of these current sources have the high output impedances of their collectors.

The common-mode voltage is rejected by a precision difference amplifier, A_4, of gain of 2 and bandwidth of 10 MHz. The difference amplifier is driven by two voltage followers, A_2 and A_3, so that the input impedance of the difference amplifier does not load the measured

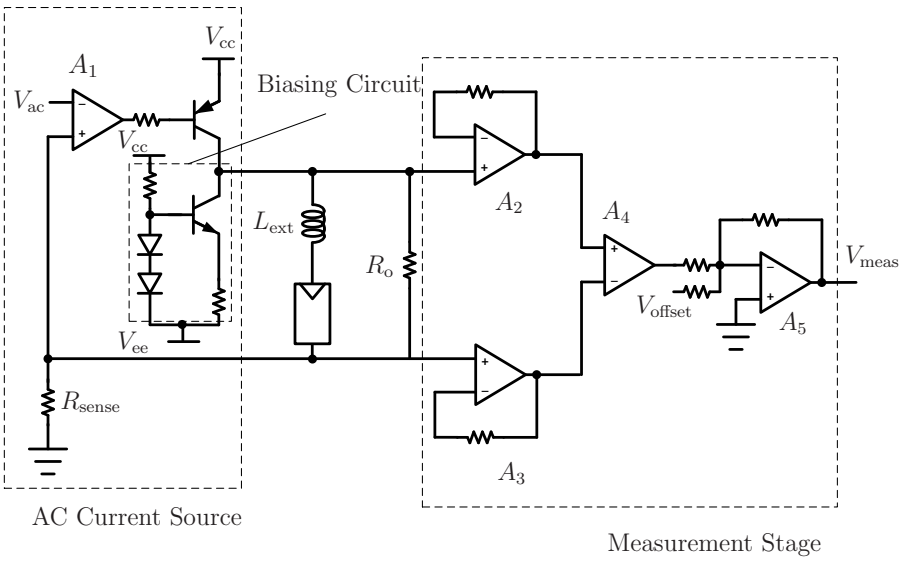


Figure 2.19: The schematic of the measurement circuit.

impedance. A dual channel CMOS op-amp is used for A_2 and A_3 so they are better matched and also so their input capacitance does not affect the measurement.

In the last stage of the measurement circuit, op-amp A_5 removes the voltage offset of the signal from the dc biasing of the cell and also amplifies the measured signal. A voltage follower driven by a potentiometer generates required V_{offset} so that A_5 does not saturate at different operating points.

2.5.5 Hardware Demonstration

To validate the investigated method, a prototype of the measurement circuit was built, and measurement was performed on a solar PV cell. Figure 2.20 shows a photograph of the hardware setup constructed for hardware evaluation of the investigated method.

2.5.5.1 Hardware Setup

The measurement was performed on a monocrystalline silicon solar PV cell (TDB125 model, VIKOCELL) with the parameters listed in Table 2.3. External inductors of 10, 36, 82, and 130 nH were used to resonate the solar PV cells at different test frequencies and measure the diffusion capacitance, the parasitic inductance, and the quality factor at different frequencies.

Figure 2.20: A photograph of the hardware setup.

Table 2.3: Solar PV Cell Parameters at Standard Test Conditions (STC)

Parameter	**Value**
Type	Monocrystalline Silicon PV Cell
Size (mm×mm)	125×125
Optical Efficiency (%)	18.29
MPP Power (W)	2.8
MPP Voltage (V)	0.524
MPP Current (A)	5.365
Open Circuit Voltage (V)	0.635
Short Circuit Current (A)	5.759
PV Diode Current at MPP (A)	0.394

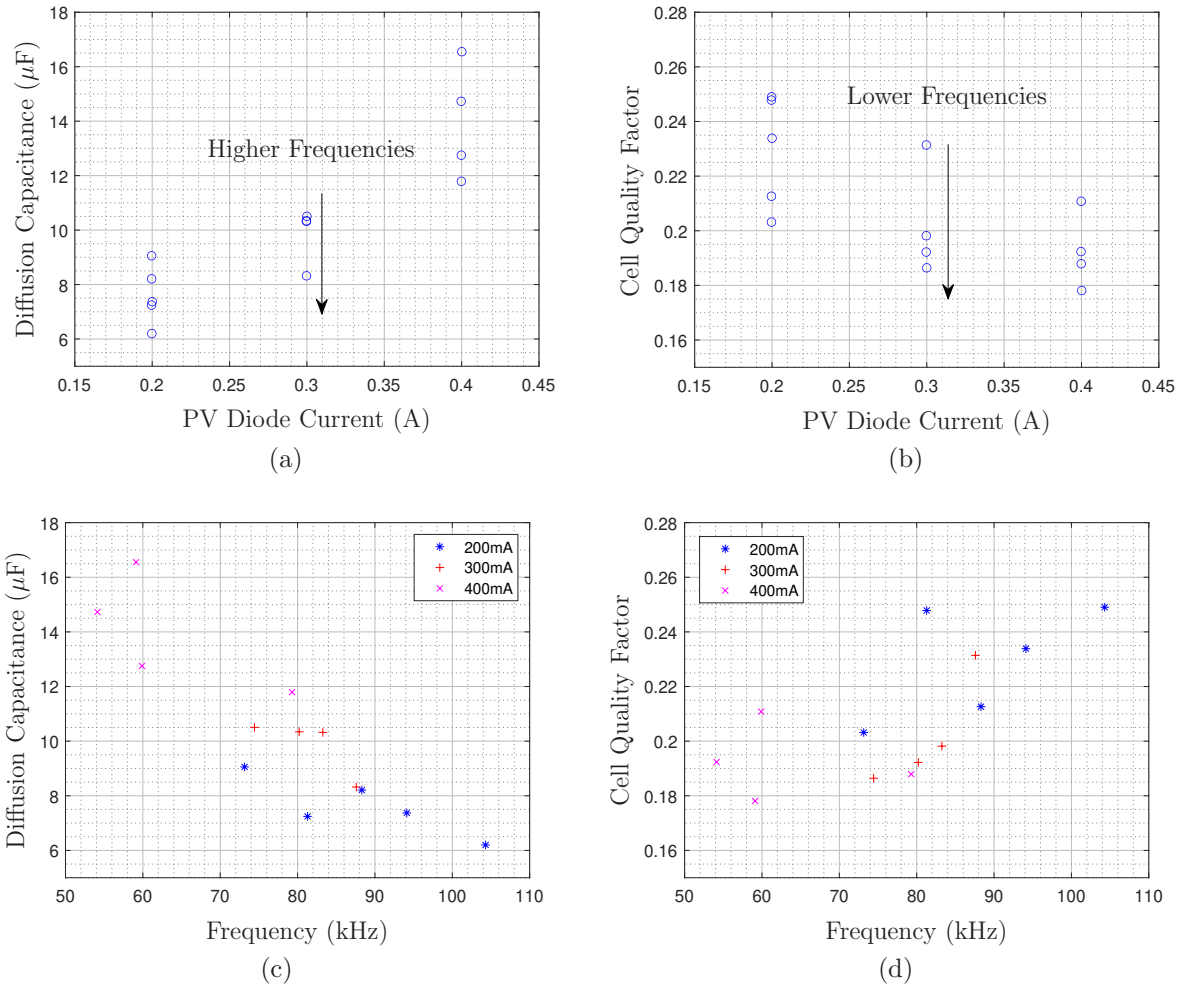


Figure 2.21: Hardware results: (a) diffusion capacitance versus PV diode current, (b) cell quality factor versus PV diode current, (c) diffusion capacitance versus frequency, and (d) cell quality factor versus frequency.

Additionally, the measurement was performed without any external inductors as well. The peak-peak amplitude of the ac current source was 9 % of the operating point. R_{sense} was 1 Ω and R_{o} was 1 kΩ. The total gain of the measurement stage was 100. A halogen lamp was controlled by a dc linear supply to change the illumination level.

2.5.5.2 Hardware Results

The dynamic parameters of the solar PV cell under the test were measured at 200, 300, and 400 mA at different frequencies. As listed in Table 2.3, for the solar PV cell under the test,

the PV diode current at the MPP is 394 mA, which is the intended operating point. In the measurements, 0.85 was considered the minimum acceptable R-Square for the goodness of the curve fittings.

Figure 2.21(a) shows the diffusion capacitance versus the PV diode current. The measured capacitance values around the MPP, i.e. 400 mA, agrees with 6-9 μF reported values in [19] for a 156 mm$\times$60 mm monocrystalline silicon solar PV cell at 50 kHz. As expected, the capacitance increases with the current. Figure 2.21(b) shows that the cell quality factor decreases with the PV diode current. Additionally, at each PV diode current, the diffusion capacitance decreases with frequency, as shown in Fig. 2.21(c), which agrees with the findings in [70]. Based on (2.79) and (2.80), it is expected that the cell quality factor increases with frequency at each PV diode current, which is confirmed in Fig. 2.21(d). The measured parasitic inductance of the cell, which is a 125 mm$\times$125 mm monocrystalline silicon solar PV cell, is 389.5 nH $\pm$ 44.5 nH.

2.6 Summary and Contributions

Alireza Ramyar and Lingsi Xu collaborated in the layout and fabrication of the control PCB of the hardware emulator in Section 2.3.3. Section 2.4.3 is worked by Alireza Ramyar and Xiaofan Cui. Alireza Ramyar and Yasir Altheyabi collaborated in the design and fabrication of the hardware setup and obtaining the hardware results in Section 2.5.5.

This chapter highlights the architectures and methods for dDCR solar PV panels. It was shown that the averaged behavior of switched-capacitor dDCR solar PV modules could be represented by two separate continuous-time circuits that are coupled by feedback and constraints. From this, a reconfigurable and scalable linear emulator for dDCR solar PV modules was investigated, which not only simulates mismatched conditions but is also easy to implement in hardware. We also investigated a two-port up/down dc-dc converter that performs two-dimensional MPPT for dDCR solar panels. In addition to the novel topology, the control strategy for the converter was studied, and its feasibility was discussed. Finally,

a current-biased small-signal measurement method for dynamic parameters of solar PV cells was investigated, which can measure the diffusion capacitance, the parasitic inductance, and the quality factor of the solar PV cells. All these architectures and methods were validated through hardware demonstration.

CHAPTER III

Optimizing Partial Power Processing for Heterogeneous Degradation of Batteries in Energy Storage Systems [1]

3.1 Introduction

Battery energy storage systems (BESS) are needed to stabilize the grid with a high penetration of renewables [73], support micro and nanogrids [74], and support electric vehicle (EV) fast charging and reduce the cost of grid upgrades from the high peak power [75]. At the same time, second-use batteries from the explosive growth of electric vehicles represent both a problem and an opportunity. By 2030, there will be 200 GWh per year of used batteries from EVs [29], and despite recycling, it will become overwhelmingly unsustainable. These batteries, when removed from the vehicle, still have approximately 80% capacity and power capability [30, 31]. Reusing these batteries in second-use battery energy storage systems (2-BESS) provides a sustainable solution that adds economic value to EV batteries [76, 77, 78].

There are several economic obstacles to the adoption and deployment of 2-BESS. The price competitiveness of 2-BESS relative to other storage technologies, including battery energy storage systems with new batteries, relies on lowering the added costs. These include

[1] This chapter is adapted from papers [32, 71, 72].

the cost of transportation [79], inventory, and power converters [80]. By using distributed production and a local supply together with just-in-time production, transportation, and inventory costs are minimized. However, this production strategy incurs the challenge of a heterogeneous supply. Even with second-use batteries that are identical at the time of original manufacturing and installed in identical vehicles, these batteries, when removed, will exhibit a significant degree of variation because of the different history of drive cycles and temperature cycling.

A typical strategy for BESSs using new batteries, which have a high degree of homogeneity, is to use conventional partial power processing (C-PPP) architectures [81] (shown in Fig. 3.1(a)). Partial power processing reduces the required converter ratings and hence the capital cost of converters [81]. Additionally, by reducing processed power, overall system efficiency increases, and the cost of thermal management decreases [82]. These architectures can have a pre-determined choice of power converters and power flow topology because of the high certainty and homogeneity among the batteries [83]. In a C-PPP structure, only mismatch power among the batteries and between the required load voltage and series voltage of the batteries is processed.

The conventional strategy for BESSs with heterogeneous batteries, e.g. 2-BESS, is to individually process all the power from every battery to adjust for the heterogeneity by individualizing each battery's power trajectory [84] (shown in Fig. 3.1(b)). The disadvantage to the full power processing (FPP) strategy is that the power ratings of the converters must be at least equal to the battery power ratings. Because power converter cost is nearly proportional to their power rating, FPP is the costliest option for power conversion. Additionally, the system efficiency will be less than the efficiency of the power converters [85]. For example, a system efficiency of 98% requires power converters with at least 98% efficiency, where the cost of the converters also increases with efficiency [86].

An appealing alternative to FPP for 2-BESS is partial power processing because of the lower cost of power converters, higher system efficiency, and lower cooling requirements.

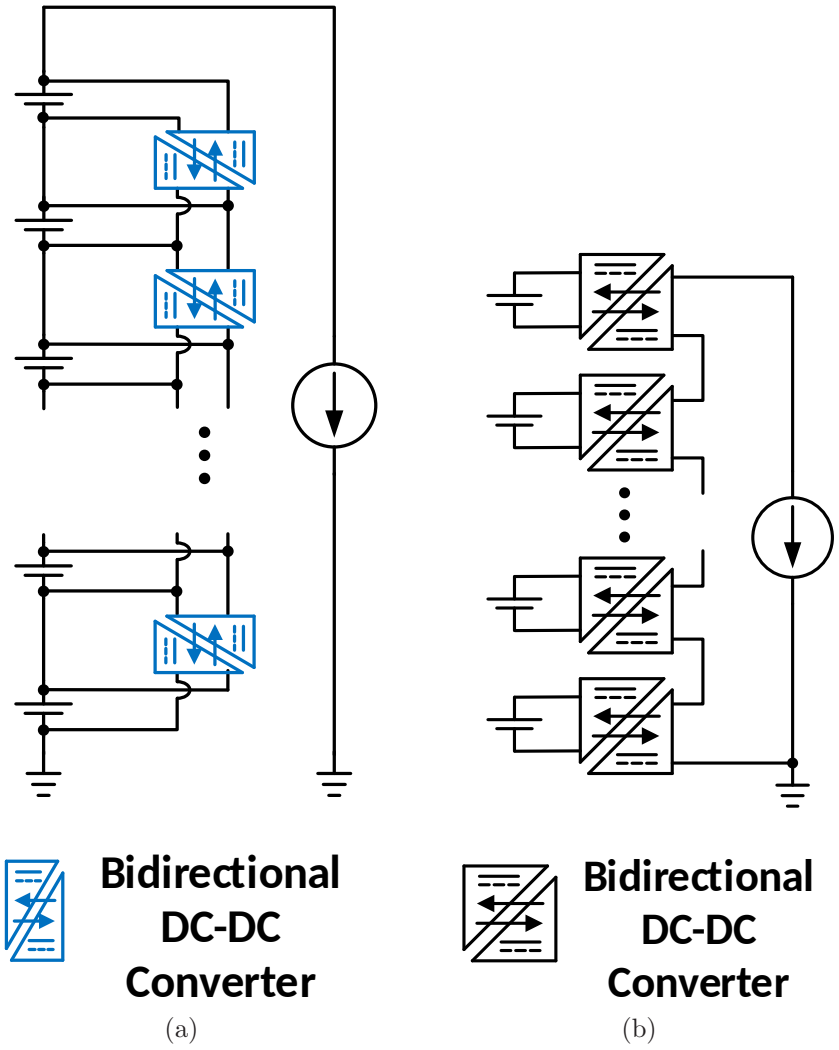


Figure 3.1: (a) Conventional partial power processing (C-PPP) in this particular topology cascades power from neighboring batteries and processes only the mismatch power. (b) Full power processing (FPP) uses a power converter for each battery to individually determine the charge and discharge current, voltage, and hence power trajectories.

However, heterogeneity among batteries is a challenge. We have previously introduced a new strategy for partial power processing, lite-sparse hierarchical partial power processing [32, 33, 34] to address the disadvantages of FPP and the challenges of C-PPP. This thesis investigates a new stochastic optimization method for LS-HiPPP, which is an optimization over battery degradation. In other words, we want to optimize LS-HiPPP over the potential lifetime of the 2-BESS. Additionally, a reliable hierarchical system monitoring and control (SMC) for power conversion in BESSs is investigated in this Chapter. The proposed SMC consists of a central monitoring and control unit together with distributed monitoring and control agents for each battery and power conversion unit.

3.2 Lite-Sparse Hierarchical Partial Power Processing for Heterogeneous Degradation of Batteries in Energy Storage Systems

3.2.1 Terminology

An objective often used for optimization in operations research over statistical uncertainties is the ensemble performance in the production of a large number of units, specifically the expected performance [87]. Expected performance metrics are used for optimization and evaluation in this Chapter.

The design targets for power processing in a 2-BESS are: (1) minimize the aggregate power rating of the power conversion; (2) minimize the number of power converters; (3) minimize the different types of converters; and (4) maximize the overall performance, specifically power capability. A goal of LS-HiPPP approach is to find the optimal tradeoff surface for (1) and (4) using optimization methods, with (2) and (3) as design choices that depend on the pricing structure of power converters. The choice of design point on the (1) and (4) tradeoff surface depends on the pricing structures of both batteries and power converters.

The battery utilization is the fraction that is available at the output of the combined individual capabilities of the batteries within a BESS. In LS-HiPPP approach, the expected

battery power/energy utilization is maximized given the statistics of the battery supply and choice of power converters. This more convenient optimization is a type of duality to minimizing the power processing for a given choice of battery utilization.

The aggregate power converter rating of a BESS is the sum of the ratings of the individual power converters within the energy storage system. The cost of power converters is known to be monotonic, with power rating with fewer types of converters being more advantageous for economies of scale.

System efficiency is the ratio of the output power of a BESS to the sum of the power delivered by the individual batteries. For full power processing, 100% of the individual power is processed by the power converters, which means system efficiency is determined by power converter efficiency. More efficient power converters are typically larger in size and more expensive. Lower system efficiency means higher losses, which means a larger cost in thermal management.

3.2.2 LS-HiPPP Concept

The approach to partial power processing in LS-HiPPP is circuit interconnection that is hierarchical, where most of the converters are "lite" in power with a "sparse" number of converters with more power. This results in a much lower processed power and hence aggregate converter rating for a particular 2-BESS performance. We use the hierarchy in the partial power processing to partition the power converters to take advantage of economies of scale by requiring only a minimal number of sets of identical power converters. This way, only a few types of power converters are needed, which can be purchased in larger volumes. The combination of numerous lower power converters together with a few higher power converters comprises the power processing for LS-HiPPP.

In contrast to FPP, where every battery requires its own power converter to process its power, the LS-HiPPP interconnection consists of two power converter layers. The first layer consists of a sparse number of power-heavy converters that is much fewer in number than

the batteries. The second layer consists of a more dense layer of lite-power converters.

The BESS shown in Fig. 3.2 with the Layer 1 sparse and Layer 2 lite converters includes a bus voltage regulator. The lite-sparse converters only process the mismatch power among the series connected batteries, but unlike conventional power processing, require lower overall power converter ratings. The bus voltage regulator processes the voltage mismatch between the series string of batteries and the voltage required by the current-sink load; in doing so, the voltage heterogeneity is also absorbed. LS-HiPPP approach applies not only to battery packs but also to battery modules (battery packs may be partitioned into modules) and individual battery cells.

3.2.3 Battery Distribution Flattening

The battery supply statistics can be mapped to the statistics of individual battery positions by a distribution flattening method. The method of distribution flattening generates a finite set of batteries that represent the expected performance. Fig. 3.3 shows a probability density function (PDF) for battery power capability $p(P)$. We would like to map this statistical distribution, which is a continuous function, to a finite expected set of batteries of size N.

This expected set is an ordered set. The elements of this set are a particular representation of the expected values for N batteries drawn from the supply distribution. The set is constructed in the following manner:

1. Divide the distribution into N intervals of equal probability: $[P_1, P_2]$, $[P_2, P_3]$, ..., $[P_N, P_{N+1}]$. P_1 and P_{N+1} are the lower and upper bounds of battery power capability, respectively. An example is shown in Fig. 3.3. The n^{th} interval satisfies

$$\int_{P_n}^{P_{n+1}} p(P)\, dP = \frac{1}{N}. \tag{3.1}$$

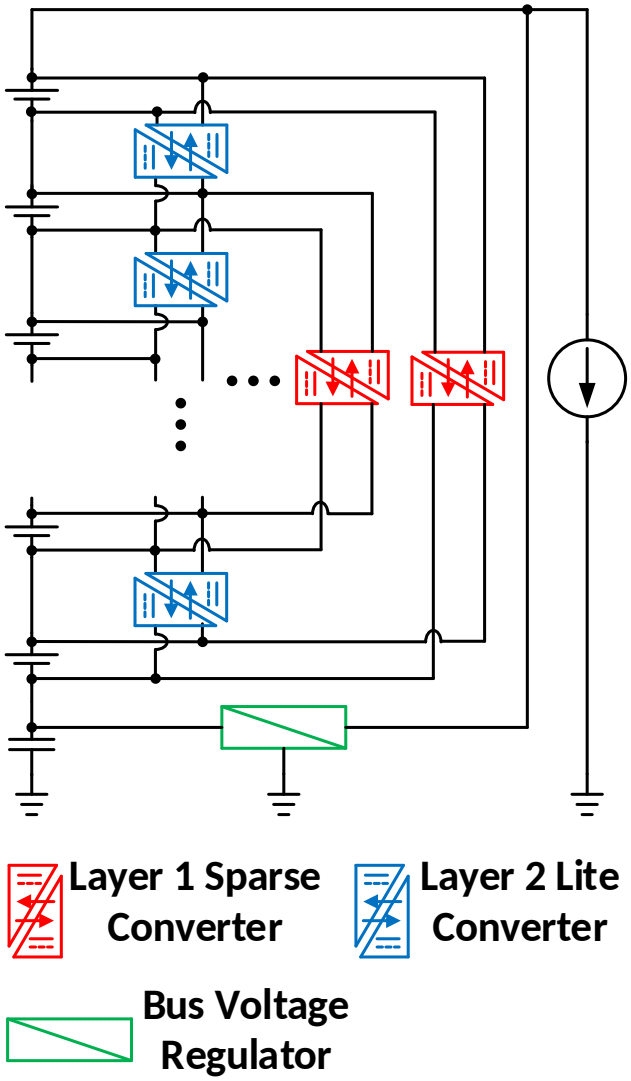


Figure 3.2: Lite-sparse hierarchical partial power processing (LS-HiPPP) for series connected 2-BESS. Layer 1 consists of a sparse set of higher power converters. Layer 2 consists of a dense set of lower power (lite) converters. A bus voltage regulator processes the mismatch between the battery series string and the required bus voltage. Only mismatch power is processed like C-PPP but with fewer power converters and lower converter ratings for the same performance using heterogeneous second-use batteries

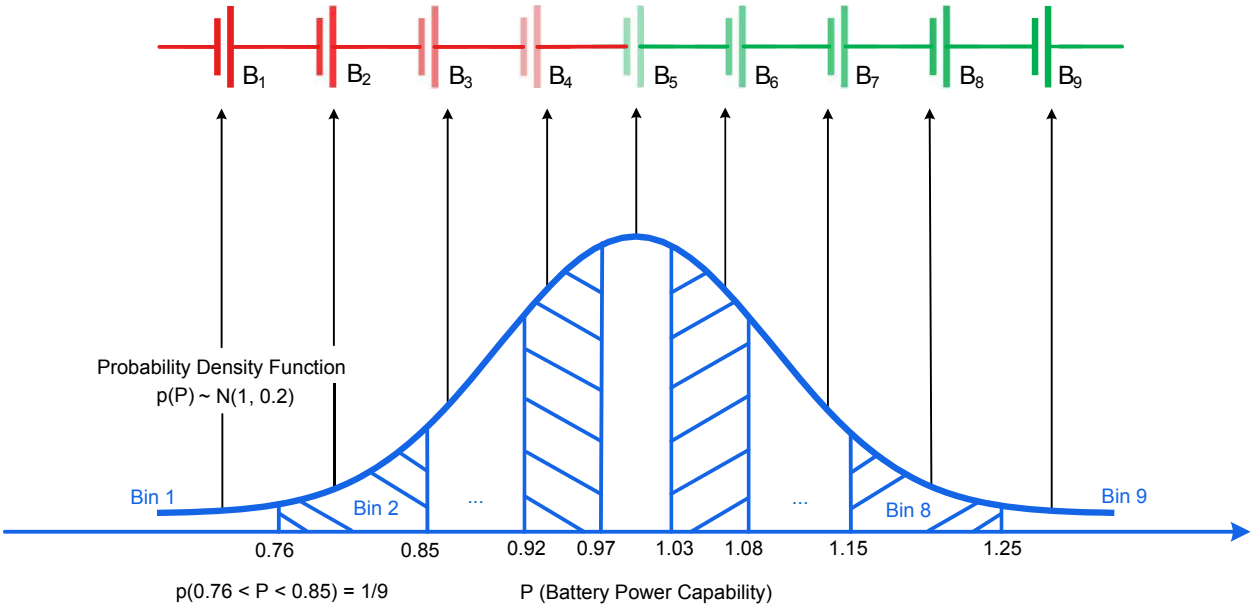


Figure 3.3: Distribution flattening method maps a statistical distribution to a series string of batteries that represents the expected behavior for that string.

2. Assign each interval its expected value (1st moment).

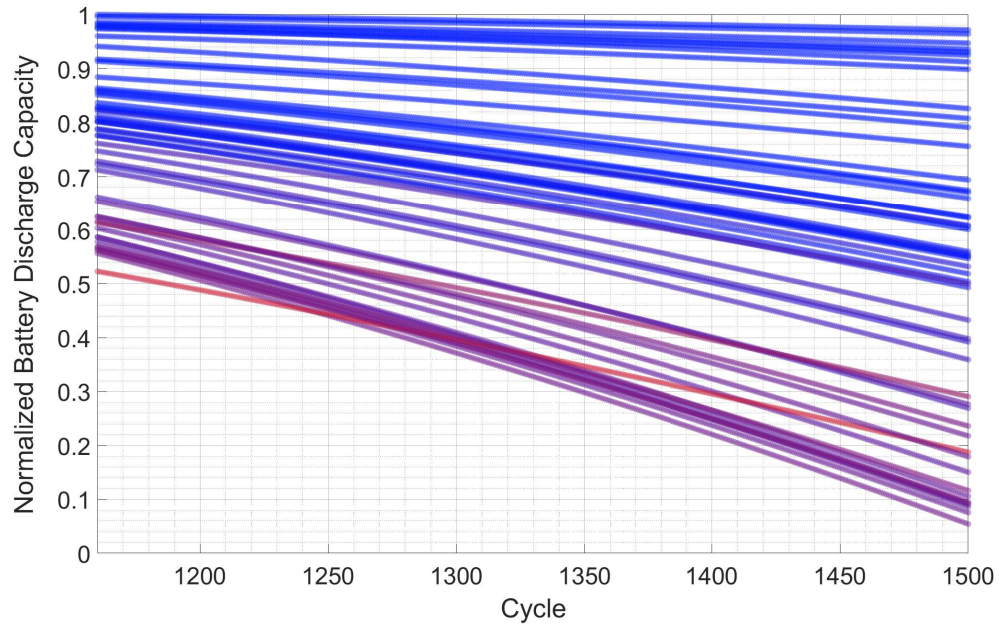
$$\bar{P}_n = N \int_{P_n}^{P_{n+1}} p(P) P \, \mathrm{d}P. \tag{3.2}$$

3. The finite expected set $\mathcal{B}$ is constructed as $\mathcal{B} = \{\bar{P}_1, \bar{P}_2, \ldots, \bar{P}_N\}$.

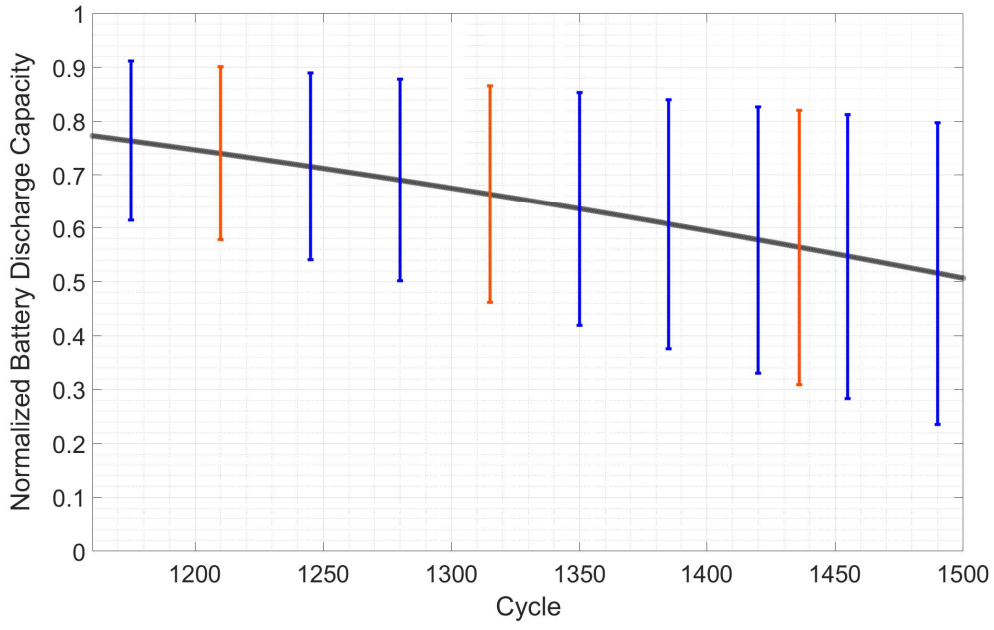
In general, each interval can be assigned any measure of central tendency, including those that are functions of the local shape of the interval. For example, one could use a function of the higher moments of the interval. Fig. 3.3 shows a realization of $\mathcal{B}$ as a series circuit of batteries. In general, $\mathcal{B}$ can be realized by any topology, including circuit topologies.

3.2.4 Modeling of Degradation

The data set by [1] is used in this thesis as a large public data set for the degradation of cycled Li-ion batteries. As shown in Fig. 3.4(a), the statistical characteristics of the batteries' capacity evolve over time. The capacity heterogeneity manifests as increasing deviations



(a)



(b)

Figure 3.4: Model data for battery degradation: (a) data extrapolated from [1] using quadratic models [2], and (b) expected value with heterogeneity (standard deviation) bars.

over charge/discharge cycles while the decreasing average discharge capacity is modeled as a decreasing expected value as illustrated in Fig. 3.4(b).

Note that although this data is for battery capacity degradation over time, we can use it to determine the battery power capability as it decreases from degradation. In this thesis, we choose the power capability so that the operational C-rate is relative to the battery's full capacity at the time of operation. For example, if the battery's capacity reduces by 20 % because of degradation, then its power capability also reduces by 20 %.

Discretization in time, which is a typical method for dynamic programming [88], is used in this thesis for the modeling of degradation. This procedure is illustrated in Fig. 3.5 and is described as follows. In the first step, the expected value of the battery capacity/power capability over time is discretized into three intervals of equal area, i.e., $S_1 = S_2 = S_3$. Then, in step 2, indicator cycles c_{d1}, c_{d2}, and c_{d3} are chosen such that $S_1 = S'_1$, $S_2 = S'_2$, and $S_3 = S'_3$. Finally, in step 3, the battery energy/power utilization for interval i is defined to be

$$U_i = \frac{S''_i}{S_i}, \tag{3.3}$$

where S''_i refers to the energy/power utilized by the 2-BESS during interval i, and S_i refers to the overall intrinsic energy/power of batteries during interval i in the 2-BESS. In Fig. 3.4(b), the red error bars correspond to the resulting c_{d1}, c_{d2}, and c_{d3} of the discretization procedure.

3.2.5 Optimizing Power Processing Design

The power processing design of a battery storage network (here a 2-BESS) can be defined by the following set, which comprises:

1. sets of power converters, which can be parameterized by a unique set of power converter ratings (e.g. power rating) and the number of power converters in the set,
2. interconnection of power converters to the batteries,
3. power flows among converters and batteries,

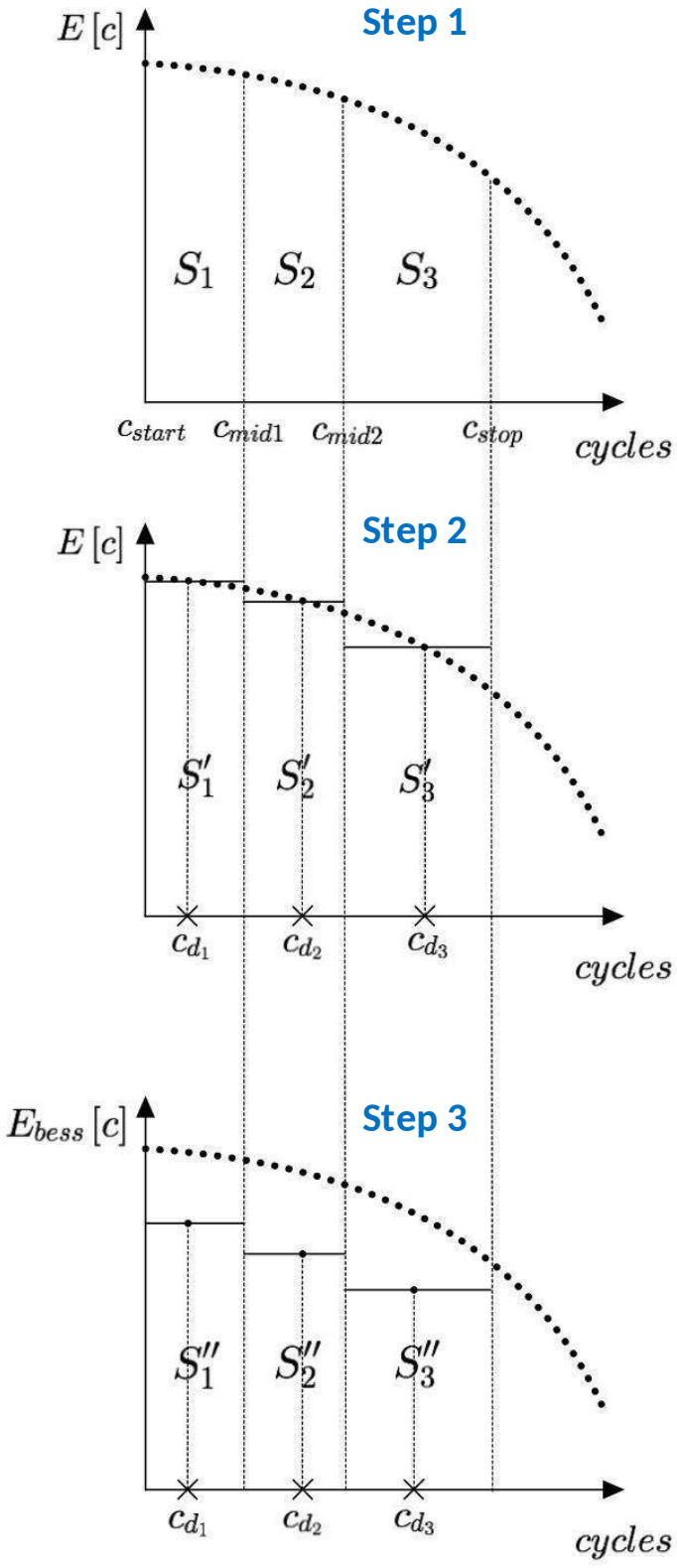


Figure 3.5: Procedure for time discretization of the degradation.

4. interconnections of input and output ports, and

5. variables of the input and output ports, e.g. voltage, current, and power.

In general, the power flows and the input and output port variables can be trajectories that change in continuous or discrete time or in a sampled data space that may or may not be uniform in continuous-time intervals.

The LS-HiPPP structure that we are investigating consists of two layers of bidirectional power converters. Layer 1 is a sparse layer of power converters that is optimized for the realization of an expected battery set from the supply population. Layer 2 is a dense layer of power converters, i.e. the number of converters is equal to one fewer than the number of batteries, with each converter's ports attached to a battery and its adjoining neighbor.

The power ratings of both Layer 1 and Layer 2 converters need to be determined. As previously discussed, the structure we choose for LS-HiPPP here has the interconnection of Layer 2 converters pre-determined. We also stipulate that the Layer 2 converters will be identical. For Layer 1, the number of converters and how they are partitioned into sets of identical converter ratings is determined as part of the optimization.

The cost of power converters scales approximately linearly with power rating (i.e. \$/kW). There is a penalty as the number of power converter sets increases. In other words, as the number of different types of converters that are needed for the design of a particular BESS product increases, the economy of scale gets worse because fewer converters of a particular type are purchased.

Here, the optimization goal is to maximize the overall battery power utilization,

$$U_{\mathrm{p}} = \frac{S_1'' + S_2'' + S_3''}{S_1 + S_2 + S_3}. \tag{3.4}$$

For each interval, a Weibull distribution is fit to the statistical data of the corresponding indicator cycle. The fitted Weibull distribution at the corresponding indicator cycle is then mapped to the batteries by performing the distribution flattening method, explained in

Section 3.2.3, to initiate the optimization.

3.2.5.1 Optimization Formulation

The design of Layer 1 can be formulated as a linear optimization problem over all the indicator cycles,

$$\max_{p_m^{(1),i}, p^i_{\text{utilized},j}} \sum_{1\le i\le I} \left(l_i \sum_{1\le j\le J} p^i_{\text{utilized},j} \right) \tag{3.5a}$$

$$\text{subject to :} \qquad -\bar{P}^i_j \le p^i_{\text{output},j} \le \bar{P}^i_j, \tag{3.5b}$$

$$p^i_{\text{output},j} = \sum_{k\in K^{(1)}_j} p^{(1),i}_k + p^i_{\text{utilized},j}, \tag{3.5c}$$

$$p^i_{\text{utilized},j} = I^i_{\text{string}} V^i_j, \tag{3.5d}$$

$$\text{for all} \quad 1 \le i \le I,\ 1 \le j \le J,\ 1 \le m \le M,$$

where J is the number of batteries, M is the number of Layer 1 converters (set by the user), I is the number of intervals (in our case $I = 3$), the decision variable $p^i_{\text{utilized},j}$ is the 2-BESS's output power contributed by the j^{th} terminal during the i^{th} interval, the decision variable $p^{(1),i}_m$ is the power processed by the m^{th} Layer 1 converter during the i^{th} interval, $p^i_{\text{output},j}$ is the output power of the j^{th} battery during the i^{th} interval, l_i denotes the length of the i^{th} interval, and $K^{(1)}_j$ is the j^{th} column of the interconnection matrix for Layer 1 converters that indicates the connections with the j^{th} battery in the architecture. Constraint (3.5b) enforces the battery input and output power limits, while constraint (3.5c) denotes the power conservation law for each battery. Constraint (3.5d) states that the power delivered at the j^{th} terminal during interval i is the product of the interval string current I^i_{string} and the individual battery's voltage; in other words, the battery determines the terminal voltage.

Note that the topology matrix $K^{(1)}$ is the same throughout the second-life of the batteries. After Layer 1 optimization, we obtain the optimal interconnection for Layer 1 converters, $K^{(1)*}$, and also the power processed by Layer 1 for each of the different time intervals. The

Layer 1 converter power rating $p^{(1)*}$ is chosen according to the highest required processed power for economies of scale.

Layer 2 converters that process the remaining battery mismatch are determined from a power flow optimization embedded in Monte Carlo. The design of Layer 2 can be formulated as a linear optimization problem over all the indicator cycles,

$$\max_{p_m^{(1),i}, p_n^{(2),i}, p^i_{\text{utilized},j}} \sum_{1\le i\le I} \left(l_i \sum_{1\le j\le J} p^i_{\text{utilized},j} \right) \tag{3.6a}$$

$$\text{subject to :} \qquad -(\bar{P}^i_j + \delta P^i_j) \le p^i_{\text{output},j} \le (\bar{P}^i_j + \delta P^i_j), \tag{3.6b}$$

$$p^i_{\text{output},j} = \sum_{k\in K_j^{(1)*}} p_k^{(1),i} + \sum_{k\in K_j^{(2)}} p_k^{(2),i} + p^i_{\text{utilized},j}, \tag{3.6c}$$

$$p^i_{\text{utilized},j} = I^i_{\text{string}} V^i_j, \tag{3.6d}$$

$$p_n^{(2),i} \le p^{(2)}_{\max}, \tag{3.6e}$$

$$p_m^{(1),i} \le p^{(1)*}, \tag{3.6f}$$

$$\text{for all} \quad 1 \le i \le I,\ 1 \le j \le J,\ 1 \le m \le M,\ 1 \le n \le N,$$

where N is the number of Layer 2 converters ($N = J - 1$), the decision variable $p_n^{(2),i}$ is the power processed by the n^{th} Layer 2 converter during the i^{th} interval, δP^i_j is the power uncertainty of the j^{th} battery during the i^{th} interval, $K_j^{(1)*}$ and $K_j^{(2)}$ are the j^{th} column of the interconnection matrices for Layer 1 and Layer 2, respectively. Note that constraint (3.6e) enforces that the power ratings for all Layer 2 converters are identically equal to $p^{(2)}_{\max}$. Also, constraint (3.6f) enforces the power rating of the Layer 1 converters, which was determined by the result of Layer 1 optimization.

3.2.6 Simulation Results

We use Monte Carlo methods to validate the performance of LS-HiPPP over optimal solutions on tradeoff curves. The average performance of 2-BESS over degradation is evaluated

through a large number of samples, and the results (for 9 batteries, 8 Layer 2 converters, and 3 Layer 1 converters) are illustrated in Fig. 3.6. In Fig. 3.6, the normalized aggregate converter rating is

$$\hat{\mathcal{R}}_{\mathrm{p}} = \frac{\sum\limits_{1\leq m\leq M} p^{(1)*} + \sum\limits_{1\leq n\leq N} p^{(2)}_{\max}}{\sum\limits_{1\leq j\leq J} \bar{P}_j}, \tag{3.7}$$

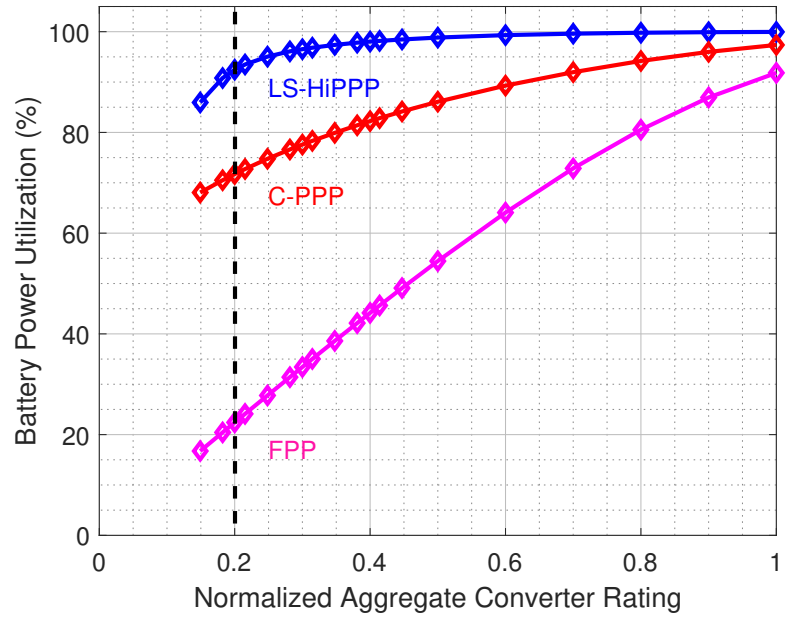
where $\bar{P}_j$ is the average intrinsic power capability of the j^{th} battery over degradation. Additionally, system efficiency is defined as

$$\begin{aligned} \eta_{\mathrm{system}} &= \frac{P_{\mathrm{output,BAT}} - P_{\mathrm{loss}}}{P_{\mathrm{output,BAT}}} \\ &= \frac{P_{\mathrm{output,BAT}} - (1-\eta_{\mathrm{converter}})P_{\mathrm{processed}}}{P_{\mathrm{output,BAT}}}, \end{aligned} \tag{3.8}$$

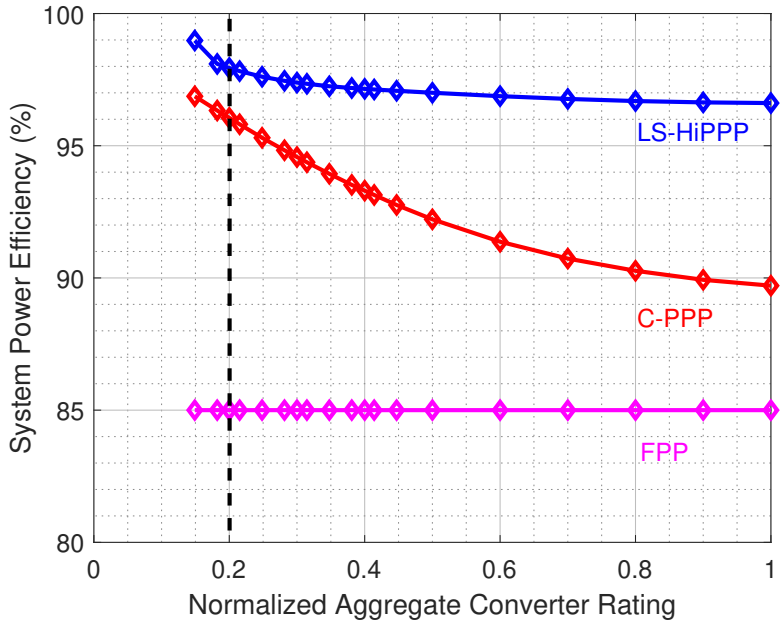
where all the converters are assumed to have individual efficiencies of $\eta_{\mathrm{converter}} = 85\,\%$.

When the aggregate power converter rating is 0.2 (marked by a dashed line), the average battery power utilization of LS-HiPPP over degradation is 92 %, as opposed to 72 % for C-PPP and 22 % for FPP, as shown in Fig. 3.6(a). LS-HiPPP utilizes approximately 20 % more battery power than C-PPP when using converters with a low aggregate power rating. The power utilization difference between LS-HiPPP and FPP is 60-70 % at low power converter ratings. LS-HiPPP is significantly more tolerant to lower aggregate power converter rating. As the converter rating decreases from 1 to 0.2, the power utilization reduces by less than 10 %, compared to approximately 25 % for C-PPP and 70 % for FPP.

High efficiency is essential in decreasing the cost of thermal management for 2-BESS. As shown in Fig. 3.6(b), LS-HiPPP has the best average efficiency over degradation among the three architectures for different converter ratings. Moreover, LS-HiPPP maintains system efficiency over the choice of converter ratings. The efficiency decreases by 1.4 % when the aggregate power converter rating increases from 0.2 to 1 for LS-HiPPP, as opposed to 6.4 % for C-PPP.



(a)



(b)

Figure 3.6: Comparison of LS-HiPPP, C-PPP, and FPP performance: (a) battery power utilization as a function of normalized aggregate converter rating, and (b) system power efficiency as a function of normalized aggregate converter rating.

3.2.7 Hardware Demonstration

A 1 kW energy storage testbed, as shown in Fig. 3.7(a), was used for hardware demonstration.

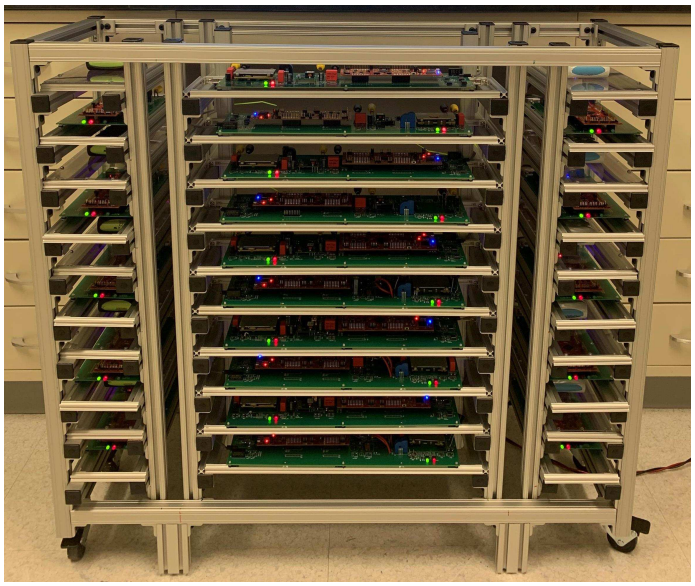
3.2.7.1 Hardware Setup

The testbed is universally configurable, consisting of nominally 5 Ah NMC and 2.5 Ah LFP batteries and isolated power converters for the Layer 1 and Layer 2 converters. All power converters and battery monitoring boards are controlled through Texas Instruments LAUNCHXL-F28379D kits and networked over a controlled area network (CAN) bus to a PC as a central controller. Both centralized and distributed fault handling and protection are implemented for scalability to megawatt-level systems.

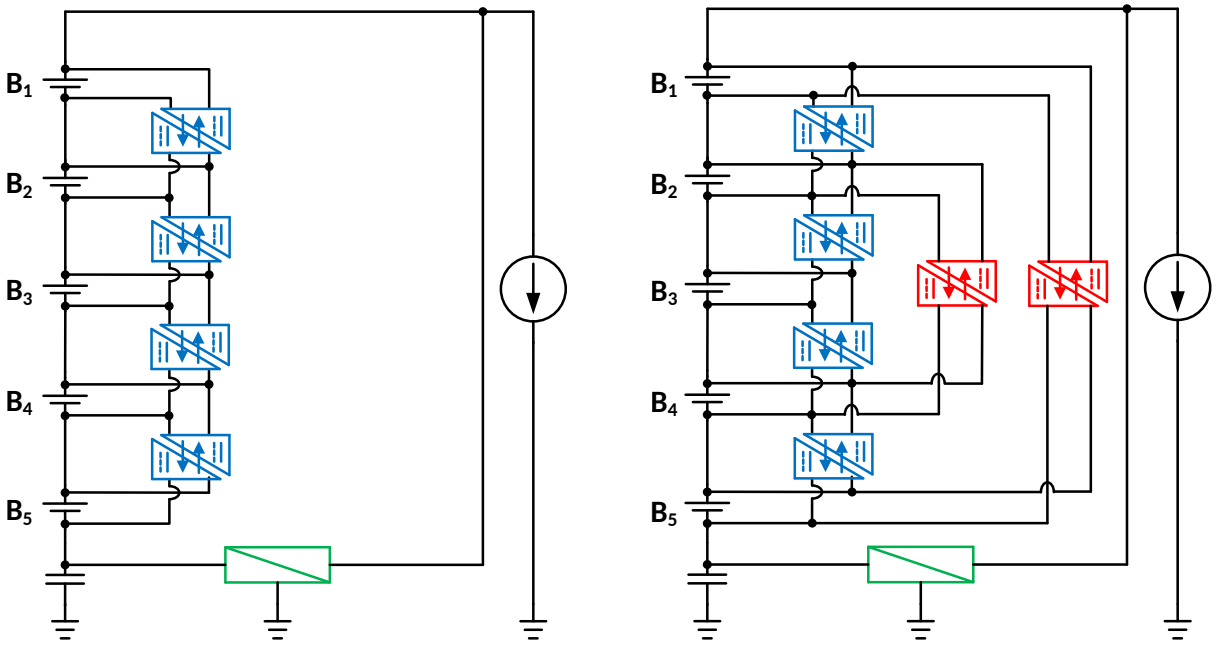
For the hardware demonstration, five 2.5 Ah LFP batteries, 4 Layer 2 converters, and 2 Layer 1 converters were used. The instantiation of the 2-BESS from the data of the first indicator cycle in Fig. 3.4, resulted in B_1, B_2, B_3, B_4, and B_5 modules with capacity of 2.500 Ah, 2.175 Ah, 1.975 Ah, 1.725 Ah, and 1.325 Ah, respectively. The placement and power flow of the Layer 1 converters and the power flow of the Layer 2 converters are optimized using the methods outlined in Section 3.2.5. For both LS-HiPPP and C-PPP, the load was a constant current sink of 1 A, and the load voltage was regulated with a bus voltage regulator converter to approximately 72 V. In other words, the performance of LS-HiPPP and C-PPP were compared using identical output power and power utilization. This means that the power processed by each converter and hence the aggregate converter ratings are the metrics of performance. The configurations of the energy storage testbed for hardware demonstration are shown in Fig. 3.7.

3.2.7.2 Hardware Results

The hardware demonstration shows a snapshot of the operation of a particular 2-BESS at the beginning of its second-life use when the power converter interconnection and ratings are optimized for the entire 2-BESS lifetime. The battery ratings for this 2-BESS are supplied



(a)



(b) (c)

Figure 3.7: (a) Battery energy storage testbed. (b) Testbed configuration for conventional partial power processing (C-PPP). (c) Testbed configuration for lite-sparse hierarchical partial power processing (LS-HiPPP).

from the family of evolving distributions described in Section 3.2.4.

In both LS-HiPPP and C-PPP, the processed power is much lower than the BESS output power because of partial power processing, as shown in Figs. 3.8(a) and 3.8(b), respectively. Because of identical output power, the bus voltage regulator, which maintains the bus voltage, also processes the same power in both. In Figs. 3.8(c) and 3.8(d), LS-HiPPP allows more power to be drawn from the battery with the largest capability (B_1) and less from the battery with the least capability (B_5); the power outputs from each battery in LS-HiPPP are better optimized. The charge distribution among batteries is narrower for LS-HiPPP than C-PPP as illustrated in Figs. 3.8(e) and 3.8(f), respectively.

Ultimately, the processed power using LS-HiPPP (16.3 %) is lower than C-PPP (25.3 %), which results in higher system efficiency and power converters with significantly lower power ratings, as illustrated in Fig. 3.9.

3.3 A Robust System Monitoring and Control for Battery Energy Storage Systems

BESSs consist of an enormous number of batteries, power converters, and power inverters, and safety is paramount in BESSs [89], especially for second-use partially degraded batteries. This urges the need for a reliable SMC in both scaled-down testbeds (1-10 kW/1-10 kWh) and full-scale (1-10 MW/100 kWh-100 MWh) BESSs. A robust SMC in BESSs helps to minimize catastrophic injuries to operators/researchers and damage to batteries and power conversion units. Additionally, it provides valuable data for diagnostics, maintenance, upgrading (software and hardware), and optimizing the control of power conversion and utilization of batteries.

Battery management systems (BMS) are the common SMC units in battery packs to ensure a safe and optimal operation [90, 91]. BMSs mainly monitor battery pack voltage, current, and temperature and maintain over-voltage (OV), under-voltage (UV), over-current

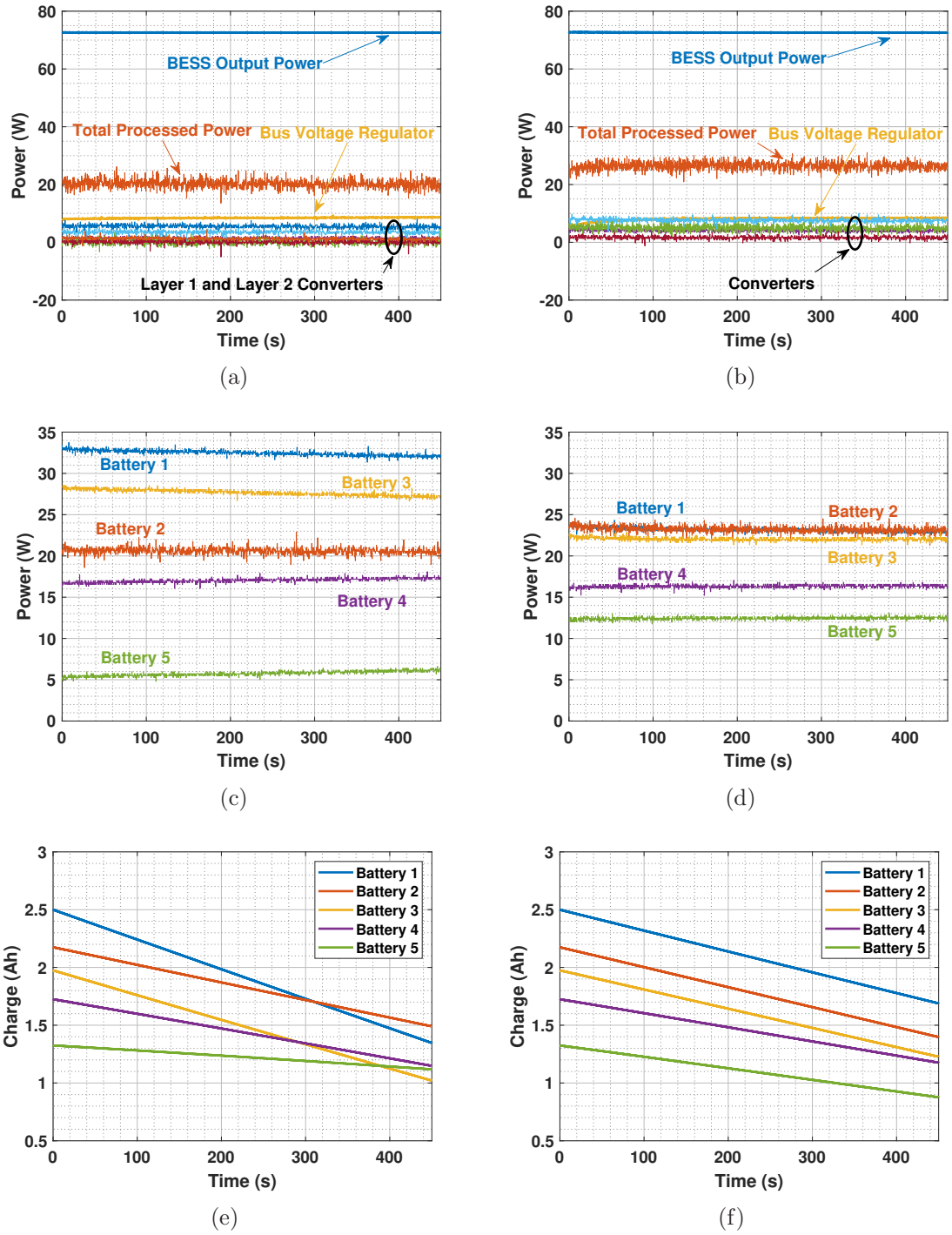


Figure 3.8: Hardware results: BESS output power, and total processed and individual converter power for: (a) LS-HiPPP, and (b) C-PPP. Power delivered by individual batteries for: (c) LS-HiPPP, and (d) C-PPP. Remaining charge of individual batteries for: (e) LS-HiPPP, and (f) C-PPP.

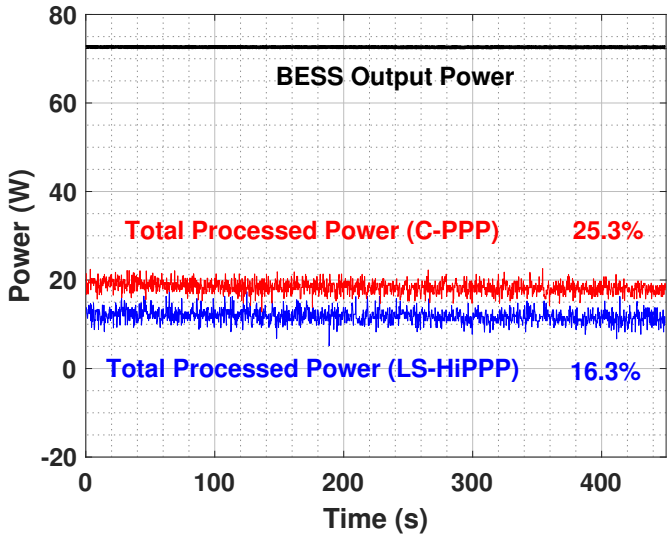
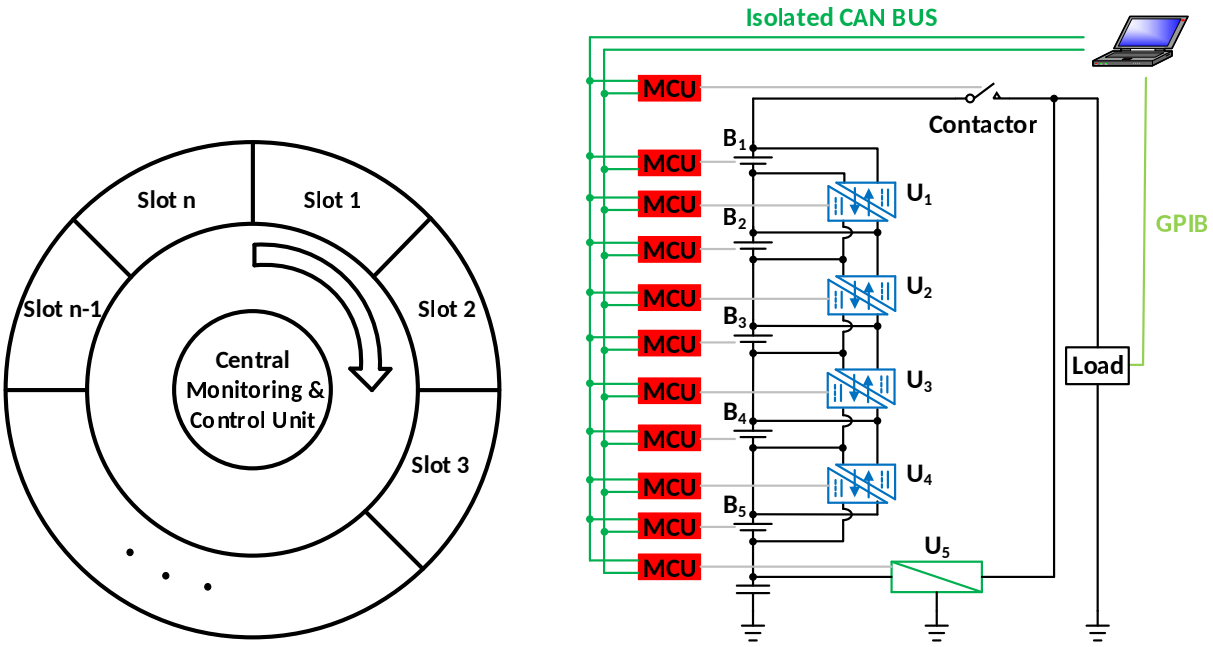


Figure 3.9: Hardware results: comparison of the processed power for LS-HiPPP and C-PPP, excluding the bus voltage regulator.

(OC), and thermal runaway protection [90]. However, in a BESS, the control of the power conversion units should be taken into account [91] to ensure their protection and battery safety. Furthermore, real-time response to control and safety commands is crucial to guarantee the safety of all the system's components. In this thesis, a robust hierarchical SMC is investigated, which consists of a central monitoring and control unit (CMCU) together with distributed monitoring and control agents (DMCA) for each battery and power conversion unit.

3.3.1 System Monitoring and Control Scheme

The proposed SMC has a hierarchical architecture. At a low level and for each node (i.e. battery and power conversion unit), a DMCA monitors and collects local data, executes control commands, and protects the corresponding node against local faults. Voltage, current, and temperature sensors are among many sensors that can be used for collecting data and monitoring purposes. Each DMCA reports its local fault to a high-level controller via a CAN bus. The CMCU logs everything in a database and then requests appropriate actions from other nodes. This way, the sequence of safety actions can be controlled in a hierarchical



(a) (b)

Figure 3.10: (a) The round-robin scheme. (b) An example of a BESS with SMC.

arrangement that prevents intractable events.

The round-robin scheme with bounded latency is used for communication, as shown in Fig. 3.10(a), and each node fulfills the assigned tasks in real-time, meaning there is an upper bound on the time a task is completed. The CMCU communicates with a single node at each time slot and assigns some tasks (including monitoring, protection, and control tasks) to that particular node. When the node completes the assigned tasks, the CMCU starts communicating with the next node and designates specific tasks for it.

3.3.1.1 System under Control

Figure 3.10(b) shows an example of a BESS consisting of five batteries, five converters, and a load. In this partial power processing architecture, converters U_1, U_2, U_3, and U_4 process the mismatch power among the batteries, and the bus voltage regulator (U_5) regulates the load voltage. The batteries, the converters, and the load must be real-time protected against potential faults. Also, the converters should be controlled in order to optimize the power

flows. Additionally, the data of each node (like the voltage, current, and faults) should be collected and logged for future purposes. The proposed SMC in this thesis accomplishes all these missions.

All battery management boards and converters are controlled through microcontroller units (MCU) networked over a CAN bus via isolated transceivers. The MCUs serve as the DMCAs for designated nodes. These agents communicate with a PC as the CMCU. Although the electrical load communicates with the CMCU via general purpose interface bus (GPIB), this communication can be implemented on the CAN bus, too.

3.3.1.2 Central and Distributed Monitoring and Control Flows

Figures 3.11(a) and 3.11(b) show the central and distributed monitoring and control flow charts, respectively. CMCU continuously communicates with DMCAs, sends control commands to the converters, and saves the data from all the nodes. If a DMCA reports a fault, the CMCU logs it and sends protection commands to the DMCAs. One of the advantages of the CAN communication protocol is the ability to broadcast a message to all the nodes, which enables synchronous protection actions from several nodes.

Each DMCA continuously monitors its designated node for potential faults like communication failure, OV, UV, OC, over-power OP (if the node is a load), and instability (if the node is a converter) while communicating with the CMCU on demand. After detecting a fault, the DMCA performs predefined protection actions and prepares a report for the CMCU.

3.3.2 Hardware Demonstration

The testbed shown in Fig. 3.7(a), was used for hardware demonstration, and the testbed was configured as the structure in Fig. 3.10(b). The load was a constant current sink of 1 A, and the load voltage was regulated with U_5 to approximately 70 V. Figure 3.12 shows a snapshot of four measured signals from the BESS. When the OV fault happens at the

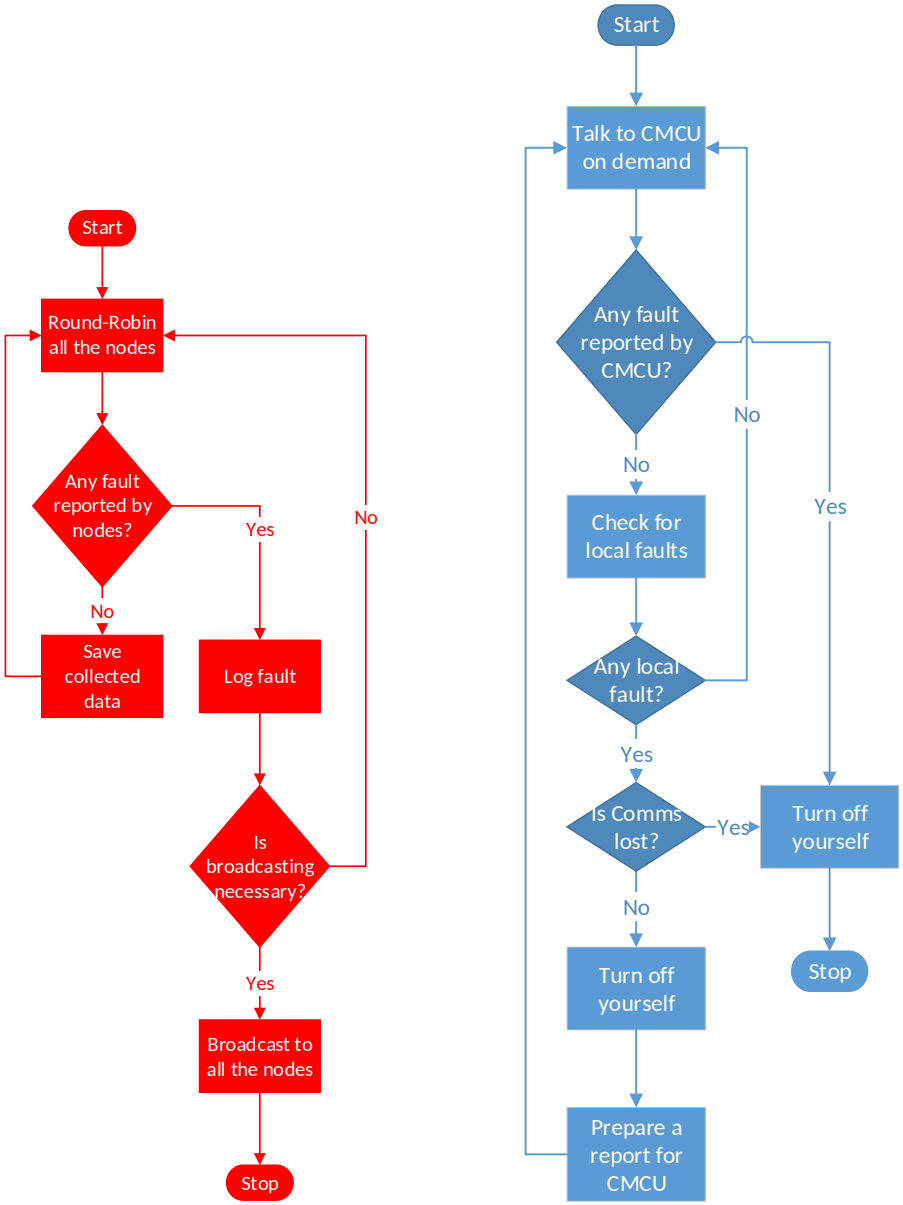


Figure 3.11: (a) Central monitoring and control flow chart. (b) Distributed monitoring and control flow chart.

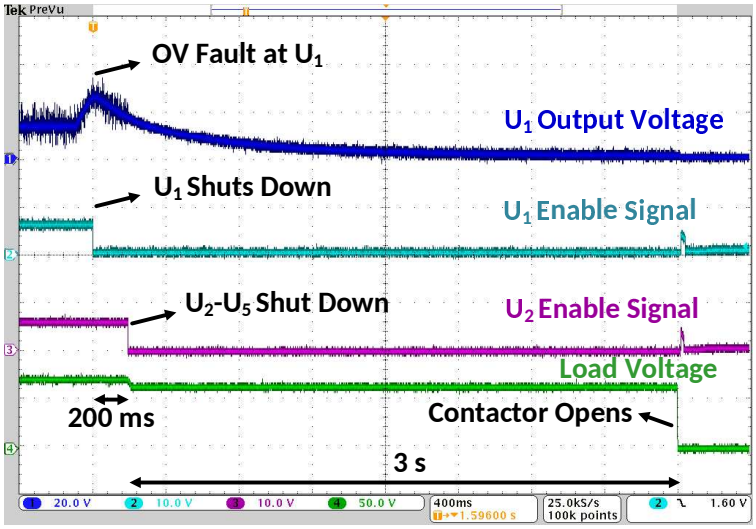


Figure 3.12: Hardware results: sequence of events triggered by SMC after the occurrence of an OV fault on one of the converters.

output of U_1, the designated DMCA detects it, pulls down the U_1 enable signal, and shuts U_1 down, promptly. After this local fault handling action, DMCA of U_1 reports this fault to the CMCU at the following communication (after 200 ms). The CMCU broadcasts a command to all the DMCAs, so U_2, U_3, U_4, and U_5 shut down. Finally, after a particular period (3 s), the contactor opens and separates the load from the batteries.

3.4 LS-HiPPP Challenges

Despite all the advantages of LS-HiPPP, some challenges need to be addressed. For Layer 1 optimization, an exhaustive search is performed to find the best interconnection, which can be computationally expensive for large systems. A similar problem shows up by adding complexity to the optimization. Rearranging batteries for Layer 2 optimization is one example. It will be shown that rearranging batteries improves the optimization objective while increasing the computational cost significantly. For a system with nine batteries, $\frac{9!}{2} = 181440$ valid permutations exist, which means the Monte Carlo simulations for Layer 2 optimization should be repeated 181440 times.

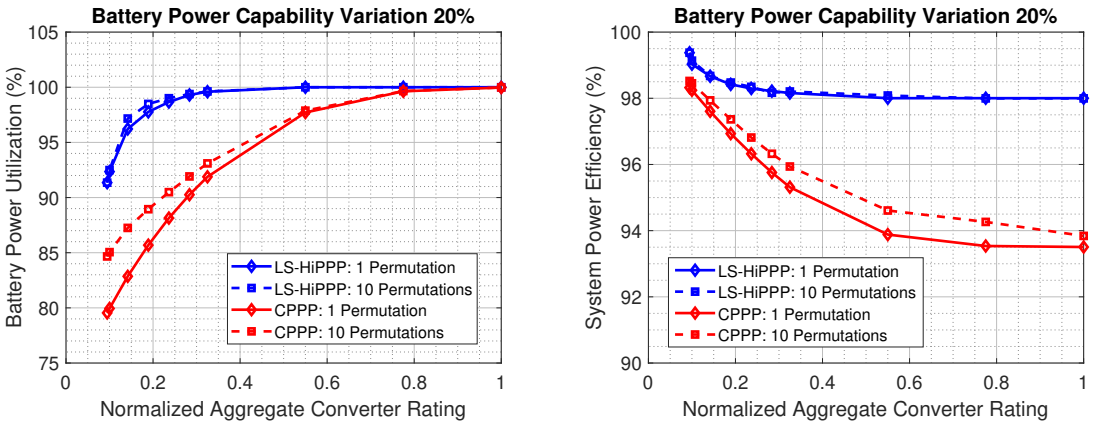
Another example is simultaneously optimizing a 2-BESS for charging and discharging a

set of second-use batteries. As shown in [31], charging and discharging resistances may degrade asymmetrically. So, we can anticipate that the statistical distribution among batteries may be different for charging than discharging states. It will be shown through a simulation demonstration that LS-HiPPP optimization is different for charging and discharging. So, the optimization problem should be modified and solved for the combination of charging and discharging states.

In the following two simulation demonstrations, the specific LS-HiPPP realization in Fig. 3.2 was used, which consists of nine heterogeneous batteries connected in series with three Layer 1 power converters and eight Layer 2 converters. Note that in the following demonstrations, battery degradation was not considered. In other words, only one indicator cycle was used in optimization formulated in Section 3.2.5.1. Considering battery degradation is another example of a complexity that makes the optimization computationally expensive.

3.4.1 Demonstration 1: Simulation Results Considering Battery Rearrangement

As mentioned before, in LS-HiPPP optimization, the interconnections of batteries are fixed. We can change the interconnections among the batteries and repeat the optimization, then select the best solution among all the battery permutations. However, for a system with nine batteries, 181440 valid permutations exist, and repeating the Monte Carlo simulations for all permutations is computationally expensive. To demonstrate the effect of the battery rearrangement on optimization results, the Monte Carlo simulations were repeated for ten random battery permutations, and the best solution was selected. As shown in Fig. 3.13, battery power utilization and system efficiency are higher for both LS-HiPPP and C-PPP when battery rearrangements are considered.



(a) (b)

Figure 3.13: Comparison of battery utilization and system efficiency with and without battery rearrangement for LS-HiPPP and C-PPP: (a) battery power utilization, and (b) system power efficiency.

3.4.2 Demonstration 2: Simulation Results Considering Charging and Discharging Difference

As mentioned before, charging and discharging resistances of the batteries may degrade asymmetrically [31]. For the Lithium Titanate ($Li_4Ti_5O_{12}$, LTO) batteries studied in [31], and after 2100 cycles, the discharging resistance (at full state-of-charge) has increased by 84 %, while the charging resistance has increased by 130 %. So, we can anticipate that the statistical distribution among batteries may be different for charging than discharging. To demonstrate the effect of different heterogeneity for charging and discharging states, the following simulation was performed. The battery power capability variation was set to 20 % for the discharging state and 30 % for the charging state to reflect the asymmetric degrading. As shown in Fig. 3.14, the results are different for charging and discharging states. This suggests that the optimization problem should be modified to consider both the charging and discharging states of the BESS.

The challenges in the optimization of the LS-HiPPP structure suggest that a new framework is needed. A framework that can limit the search spaces for optimization problems and effectively decrease their computational cost. The foundation of such a framework is

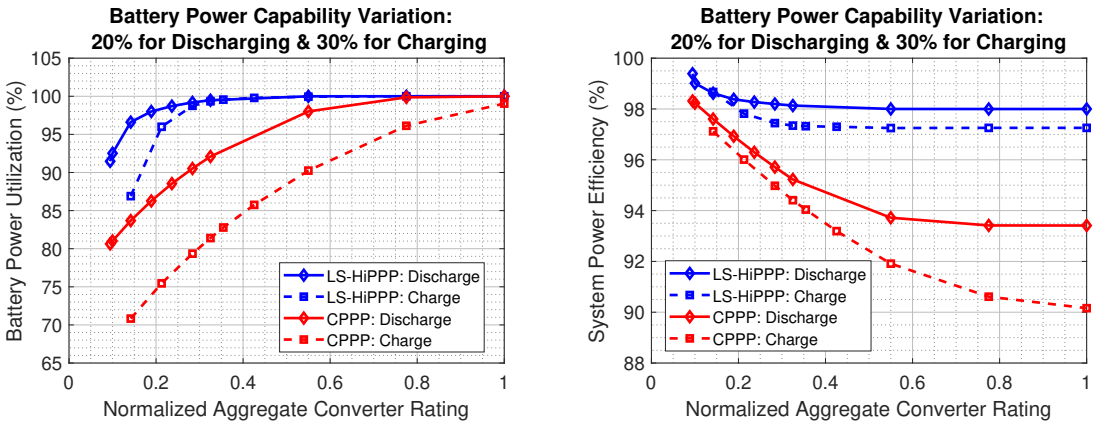


Figure 3.14: Comparison of battery utilization and system efficiency at charging and discharging states for LS-HiPPP and C-PPP: (a) battery power utilization, and (b) system power efficiency.

introduced in Appendix A.

3.5 Summary and Contributions

Section 3.2 is worked by Alireza Ramyar, Xiaofan Cui, and Wentao Xu. The testbed in Section 3.2.7 was designed and fabricated by Alireza Ramyar and Xiaofan Cui.

This chapter highlights power processing architectures and methods for 2-BESSs. We have presented a new stochastic method for lite-sparse hierarchical partial power processing architectures to optimize 2-BESS power processing over lifetime degradation. We optimize the power processing by determining the best tradeoff between converter ratings and battery power utilization by selecting the optimal power converter interconnections and power flow. We showed in simulation that LS-HiPPP over 2-BESS lifetime has an expected battery power utilization of 92 % using only 20 % aggregate converter power rating as opposed to conventional partial power processing at 72 %. When using low-cost power converters with individual efficiencies of 85 %, LS-HiPPP has an estimated system efficiency of 98 % as opposed to C-PPP at 96 %, which means half the thermal management is needed for LS-HiPPP. We demonstrated in hardware comparison between a 2-BESS using LS-HiPPP

versus C-PPP. Additionally, a reliable hierarchical system monitoring and control for power conversion in BESSs was investigated and demonstrated through a hardware testbed. The proposed SMC consists of a central monitoring and control unit together with distributed monitoring and control agents for each battery and power conversion unit. By utilizing a round-robin communication scheme with bounded latency, each node fulfills the assigned tasks in real-time. Finally, we demonstrated some of the challenges of LS-HiPPP that need to be addressed. These challenges suggest that a new framework is needed to limit the search spaces for optimization problems and effectively decrease the computational costs. The foundation of such a framework is introduced in Appendix A.

CHAPTER IV

A Framework for Optimizing Multilevel AC Battery Energy Storage Systems [1]

4.1 Introduction

Multilevel converters with integrated batteries are perfect architectures for grid-connected battery energy storage systems (BESS). Among multilevel ac battery energy storage systems (MAC-BESS), architectures based on cascaded H-bridges (CHB) and modular multilevel converters (MMC) are often used [26] with CHBs being among the best candidates [26, 27]. The MMC-based [35, 36] and CHB-based [27, 37] methods in the literature need online state-of-charge (SOC) estimation, have relatively complicated control schemes that cannot be easily generalized to other multilevel converters, and sometimes rely on redundant batteries and auxiliary circuits. Furthermore, they do not address the challenges of heterogeneous second-use batteries. This thesis presents a framework for optimizing a general class of multilevel ac battery energy storage systems, which is particularly advantageous for systems with heterogeneous (e.g., second-use) batteries. The investigated framework is validated through Matlab simulation and then demonstrated via PLECS simulation.

[1] This chapter is adapted from paper [92].

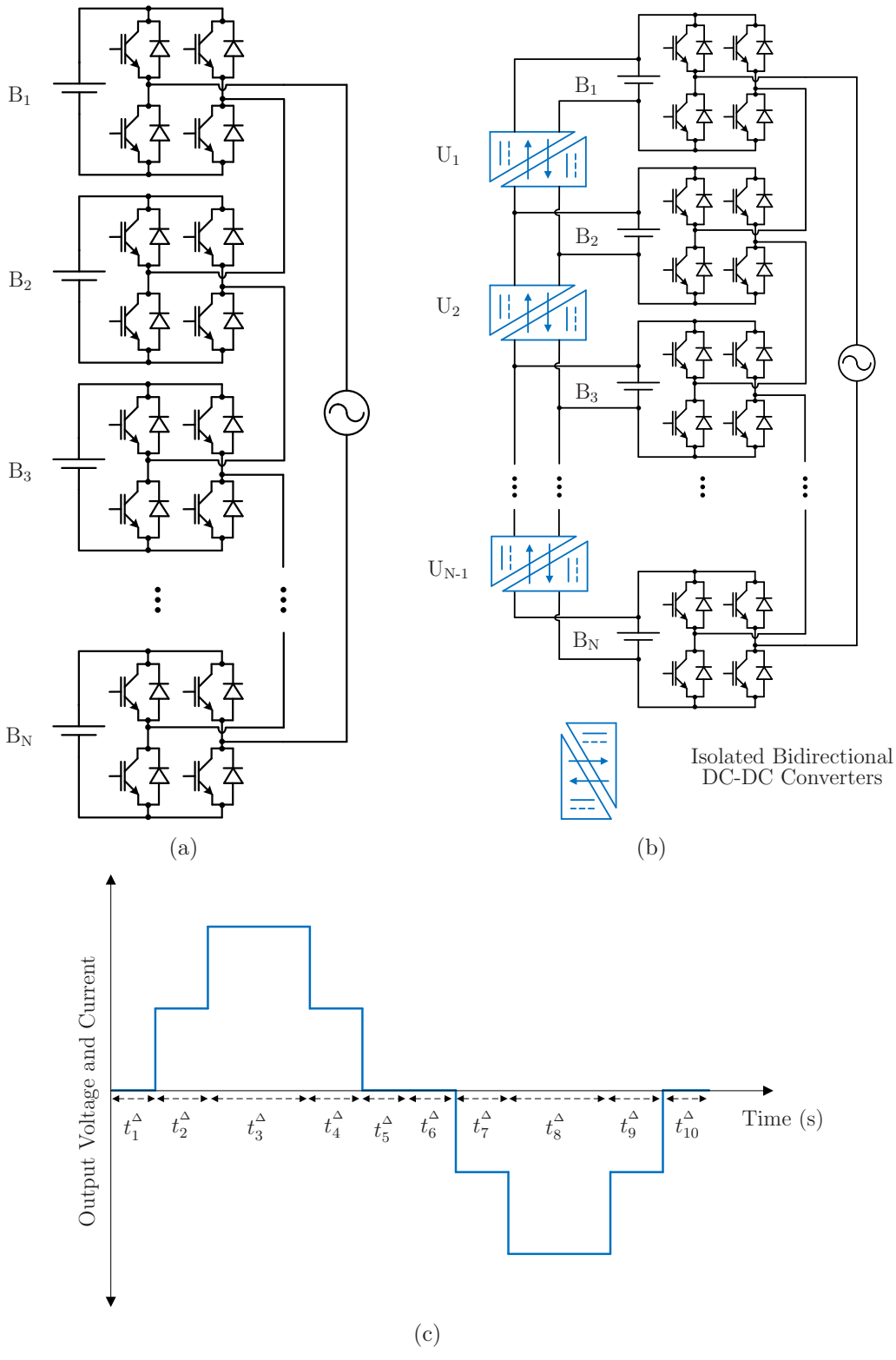


Figure 4.1: (a) Conventional CHB inverter with integrated batteries. (b) CHB inverter with partial power processing converters. (c) Output voltage and current (for a resistive load) of a 5-level CHB inverter with SHE modulation.

4.2 Framework for Optimization

We investigate the optimization framework for the conventional CHB inverter, shown in Fig. 4.1(a), and the CHB inverter with adjuvant partial power processing converters (PPPC), shown in Fig. 4.1(b). In the latter case, isolated bidirectional dc-dc converters are added ($N-1$ converters, i.e., U_1 to $U_{N\text{-}1}$, for N batteries, i.e., B_1 to B_N) to process the mismatch power/energy among the batteries and enhance the utilization of the batteries. Additionally, we use selective harmonic elimination (SHE) [93] as the modulation technique. SHE is a simple and fundamental frequency modulation scheme whose goal is to eliminate specific harmonics from the output voltage of the multilevel inverter and reduce its total harmonic distortion (THD). In principle, with N dc links and N H-bridges (HB), there are N degrees of freedom (switching angles) that can be utilized to eliminate $N-1$ harmonics and set the magnitude of the fundamental component. Figure 4.1(c) shows the output waveform (ac voltage and current) of a 5-level CHB inverter employing SHE modulation technique. In CHBs with SHE modulation and for N batteries, there exist N HBs, $2N+1$ voltage levels, and $4N+2$ time intervals (t_1^{Δ} to t_{4N+2}^{Δ}). For the case of Fig. 4.1(c), there are 2 batteries, 2 HBs, 5 voltage levels, 10 time intervals, and 1 PPPC (when used).

Although the framework is investigated for CHB inverters with SHE modulation, it can be generalized for other multilevel converters with various modulation techniques. Note that, in this thesis, a resistive load is chosen to simplify the analysis. Now we are ready to introduce the notions of Charge-Vector and Charge-Matrix as two key components of the investigated framework.

4.2.1 Charge-Vector and Charge-Matrix

The notions of Charge-Vector and Charge-Matrix presented here are built on the concepts introduced in Section 2.3.1.2. In the context of this investigation, a Battery Charge-Vector (BCV) is defined as an N-dimensional vector whose elements are the output charge of the batteries during the corresponding time intervals in the modulation. The Battery

Charge-Matrix (BCM) is then defined as a matrix $Q^{\mathrm{B}}_{N\times(4N+2)}$ consisting of $4N+2$ BCVs to designate the output charge of the batteries during a complete ac cycle. For the case of Fig. 4.1(c) with the configuration of Fig. 4.1(a) or Fig. 4.1(b)

$$Q^{\mathrm{B}} = \begin{bmatrix} q^b_{1,1} & q^b_{1,2} & q^b_{1,3} & q^b_{1,4} & q^b_{1,5} & q^b_{1,6} & q^b_{1,7} & q^b_{1,8} & q^b_{1,9} & q^b_{1,10} \\ q^b_{2,1} & q^b_{2,2} & q^b_{2,3} & q^b_{2,4} & q^b_{2,5} & q^b_{2,6} & q^b_{2,7} & q^b_{2,8} & q^b_{2,9} & q^b_{2,10} \end{bmatrix}, \tag{4.1}$$

where $q^b_{n,i}$ is the output charge of the n^{th} battery during the i^{th} time interval. Similarly, a Converter Charge-Vector (CCV) is defined as an $(N-1)$-dimensional vector, whose elements are the output charge of the converters during the corresponding time intervals, and the Converter-Charge-Matrix (CCM) is defined as a matrix $Q^{\mathrm{C}}_{(N-1)\times(4N+2)}$ consisting of $4N+2$ CCVs to designate the output charge of the converters during a complete ac cycle. For the case of Fig. 4.1(c) with the configuration of Fig. 4.1(b)

$$Q^{\mathrm{C}} = \begin{bmatrix} q^c_{1,1} & q^c_{1,2} & q^c_{1,3} & q^c_{1,4} & q^c_{1,5} & q^c_{1,6} & q^c_{1,7} & q^c_{1,8} & q^c_{1,9} & q^c_{1,10} \end{bmatrix}, \tag{4.2}$$

where $q^c_{m,i}$ is the output charge of the m^{th} converter during the i^{th} time interval.

As shown in Fig. 4.1(c), each time interval corresponds to a specific voltage level in the modulation. As an example, t^{Δ}_1, t^{Δ}_3, and t^{Δ}_7 correspond to voltage levels of 0, 2, and -1, respectively. At each time interval and based on the corresponding voltage level, specific numbers of sub-modules are required to be connected to the load. For example, 0, 2, and 1 sub-modules must be connected to the load during t^{Δ}_1, t^{Δ}_3, and t^{Δ}_7, respectively. In the context of this investigation, a Load Charge-Vector (LCV) is defined as an N-dimensional vector, which designates the connection of the sub-modules to the load during the corresponding time intervals. As an example, for t^{Δ}_1 the only possible LCV is $[0\ 0]^{\mathrm{T}}$; at t^{Δ}_3 the only possible LCV is $[q^l_3\ q^l_3]^{\mathrm{T}}$; and for t^{Δ}_7, $[q^l_7\ 0]^{\mathrm{T}}$ and $[0\ q^l_7]^{\mathrm{T}}$ are two possible LCVs, where q^l_3 and q^l_7 are the charges transferred to the load by each sub-module connected to the load during time intervals t^{Δ}_3 and t^{Δ}_7, respectively. A Load Charge-Matrix (LCM) is then defined as a matrix

$Q^{\mathrm{L}}_{N\times(4N+2)}$ consisting of $4N+2$ LCVs to designate the connection of the sub-modules to the load during a complete ac cycle, and the set of all the possible LCMs is called Load Charge-Matrix Space ($LCMS$). Note that all the LCMs in $LCMS$ comply with the shape and phase of the output current. For instance, $\begin{bmatrix} 0 & q_2^l & q_3^l & q_4^l & 0 & 0 & 0 & q_8^l & q_9^l & 0 \\ 0 & 0 & q_3^l & 0 & 0 & 0 & q_7^l & q_8^l & 0 & 0 \end{bmatrix}$ and $\begin{bmatrix} 0 & 0 & q_3^l & q_4^l & 0 & 0 & q_7^l & q_8^l & 0 & 0 \\ 0 & q_2^l & q_3^l & 0 & 0 & 0 & 0 & q_8^l & q_9^l & 0 \end{bmatrix}$ are two possible LCMs for Fig. 4.1(c), where q_2^l, q_3^l, q_4^l, q_7^l, q_8^l, and q_9^l are the charges transferred to the load by each sub-module connected to the load during time intervals $t_2^{\triangle}$, $t_3^{\triangle}$, $t_4^{\triangle}$, $t_7^{\triangle}$, $t_8^{\triangle}$, and $t_9^{\triangle}$, respectively. It is worth noting that KCL enforces

$$Q^{\mathrm{L}} = Q^{\mathrm{B}}, \tag{4.3}$$

and

$$Q^{\mathrm{L}} = Q^{\mathrm{B}} + \begin{bmatrix} Q^{\mathrm{C}} \\ 0 \end{bmatrix} - \begin{bmatrix} 0 \\ Q^{\mathrm{C}} \end{bmatrix}, \tag{4.4}$$

in Fig. 4.1(a) and Fig. 4.1(b), respectively.

4.3 Optimization Design

In this investigation, a Gaussian statistical distribution is used for the capacity of the batteries. Additionally, we choose the current capability of the batteries to be limited to a certain C-rate (i.e., 0.1) relative to the battery's capacity at the time of the operation to manage the degradation of the batteries. For simplicity, the voltages of the batteries are assumed to be homogeneous (equal), which, together with the current capability of the batteries, leads to the statistical distribution of the power capability of the batteries. The goal of the optimization is to maximize the power utilization (U_{p}) and energy utilization (U_{e}) of the BESS. For a

MAC-BESS, U_{p} is defined as the peak ac output power of the BESS normalized by the sum of the intrinsic power capability of the batteries. U_{e} is defined as the total extracted energy from the BESS prior to one of the batteries reaching its minimum allowed depth of discharge normalized by the sum of the available energy of the batteries. The decision variables are Q^{L}, Q^{B}, and Q^{C} (when used).

4.3.1 Without Partial Power Processing Converters

For a CHB inverter without PPPCs, shown in Fig. 4.1(a), U_{p} is the same for any given Q^{L}. In other words, the BESS output current is always limited by the current capability of the weakest battery, which is independent of Q^{L} (the connection of the sub-modules to the load). So, Monte Carlo simulations are performed to obtain the average U_{p} over the samples drawn from the power capability statistical distribution.

U_{e} can be optimized in a 2-step process as follows. Here, Q^{L} and Q^{B} are the decision variables. The goal is to minimize the deviation of individual SOCs from the average SOC, or in other words, make the battery SOCs closer to each other. All the batteries are assumed to have initial SOCs of 1 at the beginning of the first cycle, i.e., batteries are fully charged relative to their capacity at the time of the operation.

4.3.1.1 Optimization Formulation

$$\min_{Q^{\mathrm{L}},Q^{\mathrm{B}}} \sum_{n=1}^{N} \left(\mathrm{SOC}_n - \overline{\mathrm{SOC}}\right)^2 \tag{4.5a}$$

$$\text{subject to :} \qquad \overline{\mathrm{SOC}} = \frac{\sum_{n=1}^{N} \mathrm{SOC}_n}{N}, \tag{4.5b}$$

$$\mathrm{SOC}_n = \frac{C_n - \langle \vec{\mathbf{1}}, Q^{\mathrm{B}}_{n,:} \rangle}{C_n}, \quad n = 1, 2, \cdots, N, \tag{4.5c}$$

$$Q^{\mathrm{L}} = Q^{\mathrm{B}}, \quad Q^{\mathrm{L}} \in \mathit{LCMS}, \tag{4.5d}$$

where $\vec{\mathbf{1}}$ denotes the $(4N+2)$-dimensional all-ones vector, $\langle , \rangle$ denotes the inner product, N is the number of batteries, SOC_n is the SOC of the n^{th} battery at the end of one cycle (a scalar), $\overline{\mathrm{SOC}}$ is the average of $\mathrm{SOC}_1 \cdots \mathrm{SOC}_n$ (a scalar), C_n is the capacity of the n^{th} battery at the time of the operation (a scalar), and $Q^{\mathrm{B}}_{n,:}$ denotes the n^{th} row of Q^{B}. As mentioned in Section 4.2.1, constraint (4.5d) enforces KCL. Additionally, $Q^{\mathrm{L}} \in \mathit{LCMS}$ in constraint (4.5d) means that Q^{L} complies with the shape and phase of the output current. In the first step, we set the battery capacities to the expected values using the distribution flattening method described in Section 3.2.3 and find the Q^{L} that minimizes (4.5a). Note that, the objective function of (4.5a) is analogous to $-1 \times U_{\mathrm{e}}$. To make the optimization tractable, we first select the best Q^{L} from a random subset of *LCMS*. We then perform a coordinate ascent around this Q^{L} until it converges to the local optimum Q^{L^*}.

In the second step, the elements of Q^{L} are fixed to the elements of Q^{L^*}, meaning that for each time interval, the same sub-modules as in Q^{L^*} are selected for Q^{L} to be connected to the load. We then perform Monte Carlo simulations to obtain the average U_{e} over the samples drawn from the capacity statistical distribution.

4.3.2 With Adjuvant Partial Power Processing Converters

For a CHB inverter with PPPCs, shown in Fig. 4.1(b), U_{e} of 100% is enforced by introducing suitable constraints into the optimization that ensures SOC balancing at the end of each ac cycle. Note that having the same SOCs for all the batteries at the end of each cycle is analogous to U_{e} of 100% because all the batteries reach their minimum allowed depth of discharge simultaneously. Again, all the batteries are assumed to have initial SOCs of 1 at the beginning of the first cycle. U_{p} is optimized in a 2-step process as follows. Here, the decision variables are Q^{L}, Q^{B}, and Q^{C}.

4.3.2.1 Optimization Formulation

$$\max_{Q^{\mathrm{L}},Q^{\mathrm{B}},Q^{\mathrm{C}}} \sum_{n=1}^{N}\left(\sum_{i=1}^{4N+2} Q^{\mathrm{L}}_{n,i}\right) \tag{4.6a}$$

$$\text{subject to :} \quad -\left(\frac{P_n}{V}\right)T^{\Delta} \preceq Q^{\mathrm{B}}_{n,:} \preceq \left(\frac{P_n}{V}\right)T^{\Delta}, \tag{4.6b}$$

$$-\left(\frac{\mathcal{R}_{\mathrm{p}}}{V}\right)T^{\Delta} \preceq Q^{\mathrm{C}}_{m,:} \preceq \left(\frac{\mathcal{R}_{\mathrm{p}}}{V}\right)T^{\Delta}, \tag{4.6c}$$

$$\frac{\langle \vec{\mathbf{1}}, Q^{\mathrm{B}}_{n,:}\rangle}{C_n} = \frac{\langle \vec{\mathbf{1}}, Q^{\mathrm{B}}_{1,:}\rangle}{C_1}, \tag{4.6d}$$

$$Q^{\mathrm{L}} = Q^{\mathrm{B}} + \begin{bmatrix} Q^{\mathrm{C}} \\ 0 \end{bmatrix} - \begin{bmatrix} 0 \\ Q^{\mathrm{C}} \end{bmatrix}, \quad Q^{\mathrm{L}} \in LCMS, \tag{4.6e}$$

$$\frac{Q^{\mathrm{C}}_{m,i}}{t^{\Delta}_i} = \frac{Q^{\mathrm{C}}_{m,1}}{t^{\Delta}_1}, \tag{4.6f}$$

$$\text{for all} \quad 1 \le n \le N,\ 1 \le m \le N-1,\ 1 \le i \le 4N+2,$$

where $\vec{\mathbf{1}}$ denotes the $(4N+2)$-dimensional all-ones vector, V is the batteries' voltage (a scalar), $\mathcal{R}_{\mathrm{p}}$ is the upper bound for the power converter ratings (a scalar), and P_n is the power capability of the n^{th} battery (a scalar). T^{Δ} is a $(4N+2)$-dimensional vector containing all the time intervals defined as

$$T^{\Delta} = \begin{bmatrix} t^{\Delta}_1 & t^{\Delta}_2 & \cdots & t^{\Delta}_{4N+2} \end{bmatrix}. \tag{4.7}$$

Constraint (4.6b) limits the power capability of the batteries, and constraint (4.6c) limits the power converter ratings to an upper bound. Constraint (4.6d) enforces SOC balancing at the end of an ac cycle, and constraint (4.6e) enforces KCL. Again, $Q^{\mathrm{L}} \in LCMS$ means that Q^{L} complies with the shape and phase of the output current.

In the first step, we set the battery capacities and power capabilities to the expected values using the distribution flattening method described in Section 3.2.3 and find the Q^{L}

that maximizes (4.6a). Note that, the objective function of (4.6a) is analogous to U_{p}. Again, to make the optimization problems tractable, we select the best Q^{L} from a random subset of *LCMS*. For each Q^{L}, a Linear Programming (LP) problem is solved; then, the optimal Q^{L} is selected among the solutions of LP problems to obtain the best objective function value (i.e., U_{p}). At the end of the first step, we perform a coordinate ascent around this Q^{L} until it converges to Q^{L^*}.

In the second step, the elements of Q^{L} are fixed to the elements of Q^{L^*}, meaning that for each time interval, the same sub-modules as in Q^{L^*} are selected for Q^{L} to be connected to the load. We then perform Monte Carlo simulations on the same optimization problem, i.e., (4.6), to obtain the average U_{p} over the samples drawn from the capacity and power capability statistical distributions. It is worth noting that each Monte Carlo instance is an LP problem.

Note that we select the upper bound for the power converter ratings, i.e., $\mathcal{R}_{\mathrm{p}}$, for each optimization instance. We sweep this bound relative to the sum of the intrinsic power capability of the batteries and repeat the entire process to find the tradeoff between the power converter rating (determined by converter processed power) and U_{p} (battery power capability that is utilized). Additionally, the PPPCs can be chosen to have either constant or variable power flow during an ac cycle; thus, we consider CHB with both variable PPPCs (VPPPC) and constant PPPCs (CPPPC) and compare the results. Constraint (4.6f) enforces the power converters to have constant power flow during an ac cycle. Note that this constraint is not enforced when we use VPPPCs.

4.3.3 Effect of Output Current's Magnitude and Phase

It is worth noting that we solve the optimization to obtain the maximum U_{p} of the BESS, which gives us the maximum output current that BESS can provide. To maintain the BESS maximum output current, the PPPCs should have certain output current values obtained from optimization. When the magnitude of the BESS output current changes, the output

current of the PPPCs should follow the changes. Thus, in a BESS, the magnitude of the output current should be fed back to set the output currents of the PPPCs accordingly. The simulation results in the following Section demonstrate the effect of the output current's magnitude changes. Changing the output current's phase changes Q^{L} and consequently *LCMS*. However, the optimization formulations remain the same. We can solve the optimization for different phase values and make a lookup table. In a BESS, the output current's phase can be fed back to set the output current of the PPPCs to corresponding values from the lookup table.

4.4 Simulation Results

In order to evaluate the investigated framework, Monte Carlo simulations were performed in Matlab to compare the performance of CHB without PPPCs (with optimal Q^{L}), CHB with VPPPCs, and CHB with CPPPCs. Figures 4.1(a) and 4.1(b) show the schematics of the architectures for Monte Carlo simulations. Additionally, CHB with CPPPCs, shown in Fig. 4.1(b), was modeled and simulated in PLECS for full-load and half-load conditions. For all the Matlab and PLECS simulations, a 15-level (7 batteries) CHB inverter with SHE modulation and ac frequency of 60 Hz was used. For the batteries, we used the parameters of the battery modules in TESLA Model S EVs, i.e., 24 V and 250 Ah. Gaussian statistical distributions with μ_{capacity} of $1.00 \times 250\,\mathrm{Ah}$ and $\sigma_{\mathrm{capacity}}$ of $0.10 \times 250\,\mathrm{Ah}$, $0.15 \times 250\,\mathrm{Ah}$, $0.20 \times 250\,\mathrm{Ah}$, and $0.25 \times 250\,\mathrm{Ah}$ were used for the capacity of the batteries. The output voltage of the CHB is a 15-level ac waveform with a THD of 5.66 % and a fundamental component of 171 V peak (121 V rms). For simplicity, the load is assumed to be resistive, so the output voltage and current have the same shape and phase.

4.4.1 Optimization Results

In Fig. 4.2 and Fig. 4.3, normalized aggregate converter rating is defined as the sum of the ratings of the converters normalized by the sum of the intrinsic power capability of the

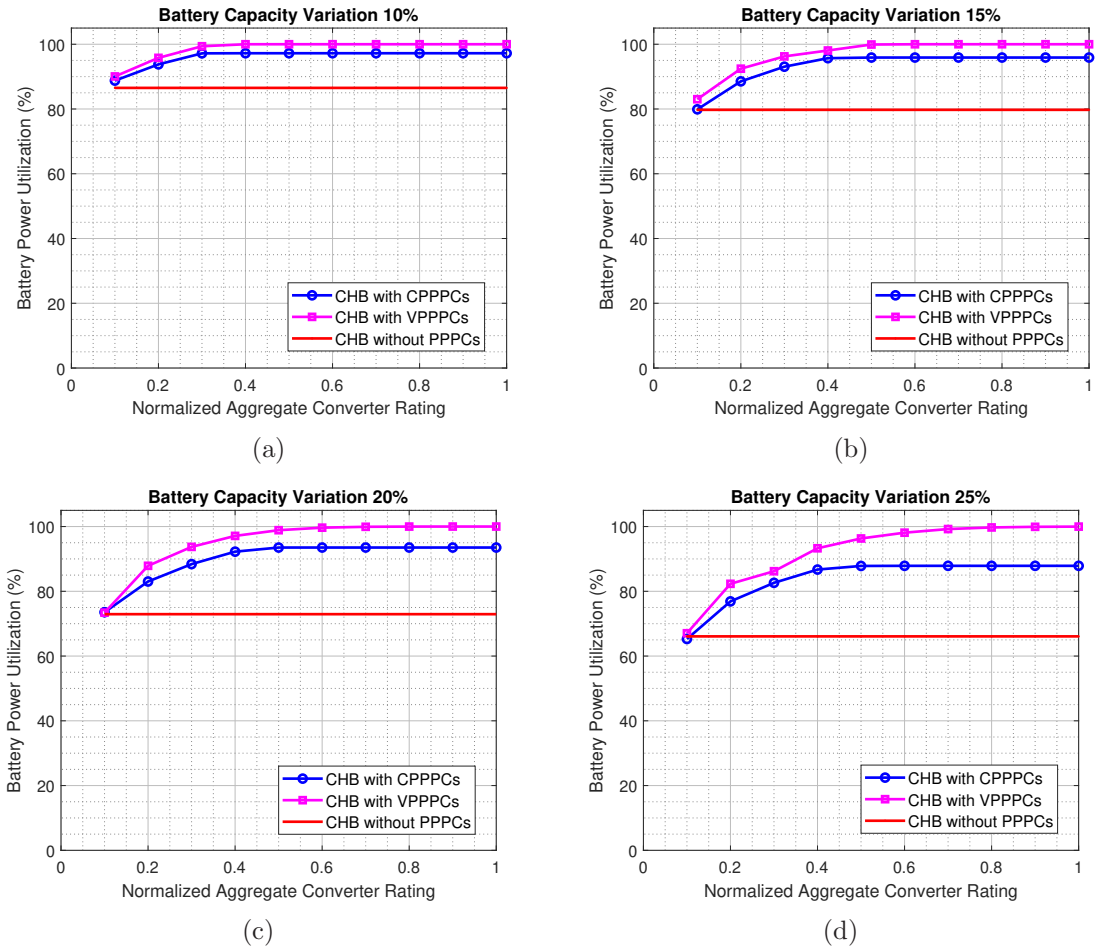


Figure 4.2: Comparison of battery power utilization for CHB without PPPCs (with optimal Q^{L}), CHB with VPPPCs, and CHB with CPPPCs when heterogeneity is: (a) 10 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.10\,\mathrm{p.u.}$), (b) 15 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.15\,\mathrm{p.u.}$), (c) 20 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.20\,\mathrm{p.u.}$), and (d) 25 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.25\,\mathrm{p.u.}$).

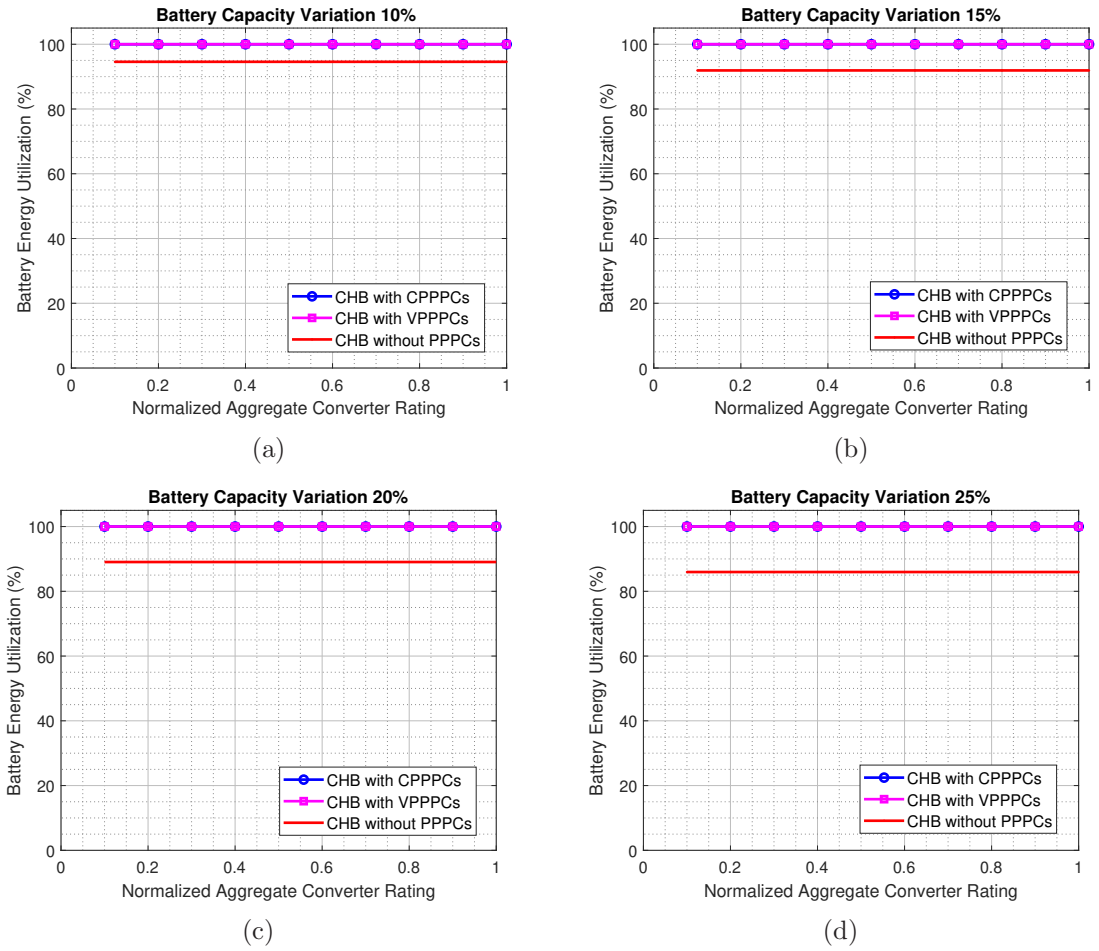


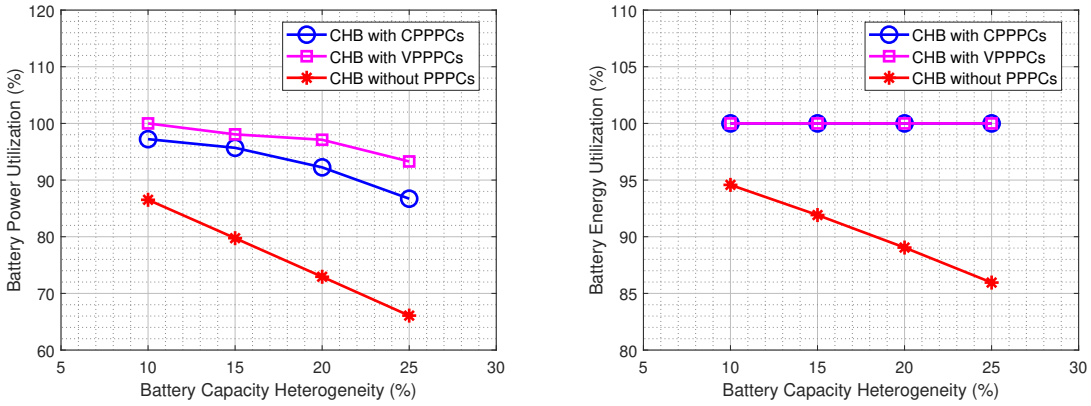
Figure 4.3: Comparison of battery energy utilization for CHB without PPPCs (with optimal Q^{L}), CHB with VPPPCs, and CHB with CPPPCs when heterogeneity is: (a) 10 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.10\,\mathrm{p.u.}$), (b) 15 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.15\,\mathrm{p.u.}$), (c) 20 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.20\,\mathrm{p.u.}$), and (d) 25 % ($\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.25\,\mathrm{p.u.}$).

batteries. Note that, for the economy of scale, all the converters are assumed to have the same rating, i.e., the highest rating among the converters.

As shown, CHB with CPPPCs and VPPPCs show a better U_{p} than CHB without PPPCs. This superiority increases when the batteries become more heterogeneous, i.e., when the battery capacity variation increases, as illustrated in Fig. 4.4. Furthermore, CHB with CPPPCs and VPPPCs have U_{e} of 100 % for all the normalized aggregate converter ratings and all the battery capacity variation values, which is expected because SOC balancing is enforced by the constraints of the optimization. Although having the same SOC for all the batteries is desirable in BESSs, especially for stochastic loads, we can relax the SOC balancing constraints to increase U_{p}. This way, we can compromise between U_{e} and U_{p} based on the cost of batteries and power converters.

Additionally, CHB with VPPPCs has a better U_{p} than CHB with CPPPCs. This observation is also not surprising because the feasibility region of the optimization problem for CHB with CPPPCs is a subset of the feasibility region of the optimization problem for CHB with VPPPCs. Thus, for a given U_{p}, a higher power converter rating is needed for CPPPCs compared to the required converter rating of VPPPCs. As an example, for battery capacity variation of 20 % and at U_{p} of 92 %, the normalized aggregate converter rating for VPPPC and CPPPC is 0.28 and 0.4, corresponding to PPPCs with power ratings of 196 W and 280 W, respectively. However, faster converters are required for the VPPPCs. So, the choice of CPPPCs or VPPPCs is a tradeoff between processed power and the switching frequency of the converters and depends on the dynamics of the load. As a reference, for a CHB with SHE modulation and 7 batteries in a grid with ac frequency of 60 Hz, the switching frequency of the VPPPCs should be at least 30 KHz, which is straightforward for such small converters.

As shown in Fig. 4.4, when the battery capacity heterogeneity increases from 10 % (i.e., $\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.10\,\mathrm{p.u.}$) to 25 % (i.e., $\mu_{\mathrm{capacity}} = 1\,\mathrm{p.u.}$, $\sigma_{\mathrm{capacity}} = 0.25\,\mathrm{p.u.}$), U_{p} decreases 7 %, 11 %, and 21 % for CHB with VPPPCs, CHB with CPPPCs, and CHB



(a) (b)

Figure 4.4: Comparison of: (a) battery power utilization, and (b) battery energy utilization as a function of battery capacity heterogeneity for CHB without PPPCs (with optimal Q^{L}), CHB with VPPPCs, and CHB with CPPPCs. Normalized aggregate converter rating is 0.4 for CHB with VPPPCs and CHB with CPPPCs.

without PPPCs, respectively. Additionally, U_{e} decreases 9 % for CHB without PPPCs, while it always equals 100 % for CHB with VPPPCs and CHB with CPPPCs. This shows that CHB with VPPPCs and CPPPCs are also less impacted by increasing battery heterogeneity compared to CHB without PPPCs.

4.4.2 PLECS Simulation Results

A sample battery set was instantiated from the battery capacity statistical distribution for a battery supply with 20 % capacity variation. Then, by using the results of Section 4.4.1, the power flow of the converters was optimized to obtain the maximum U_{p} for the case of CHB with CPPPCs at 0.4 normalized aggregate converter rating. The results were then used for the PLECS simulation to demonstrate the functionality of the structure. In the following simulations, the goal is to demonstrate that all the constraints (batteries' power limit, converters' power limit, batteries' SOC balancing constraints, and KCL constraints) are met in a circuit. C-Scripts were written in PLECS to generate the switching commands based on $Q^{\mathrm{L}*}$. PPPCs are bidirectional and need to operate as a current-controlled power converter in either direction; Fig 4.5 shows the model used for PPPCs in PLECS.

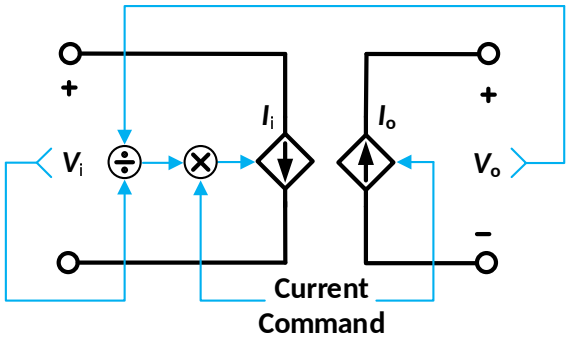
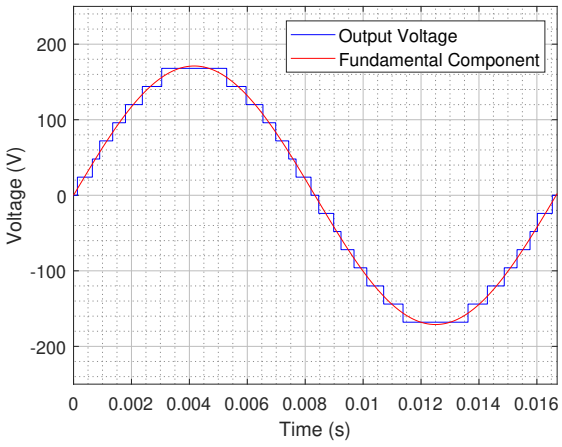


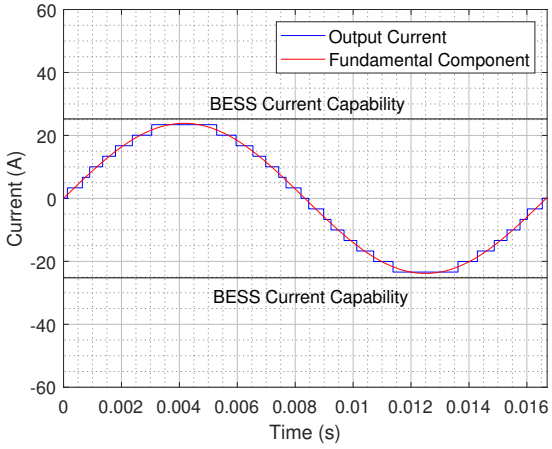
Figure 4.5: Model of a bidirectional current-controlled power converter for PLECS simulations.

4.4.2.1 Full Load

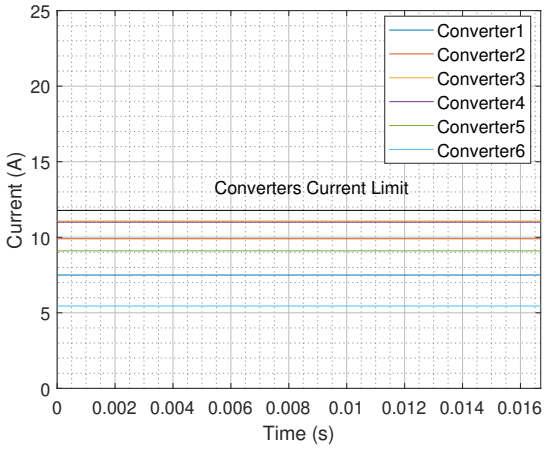
Figures 4.6 and 4.7 show the results of the PLECS simulation for the full load case. As shown, the output voltage of the CHB is a 15-level ac waveform with a fundamental component of 171 V peak (121 V rms). For the instantiated battery set, the BESS current capability is 25.24 A, which is approximately 0.1×250 A. Note that the C-rates of the batteries were set to 0.1 relative to the batteries' capacity at the time of the operation. For a MAC-BESS, the BESS current capability is defined as the sum of the intrinsic power capability of the batteries over the peak of the multilevel output voltage, i.e., $24\,\text{V} \times 7$. From Fig. 4.6(b), U_p equals $\frac{23.41\,\text{A}\times 24\,\text{V}\times 7}{25.24\,\text{A}\times 24\,\text{V}\times 7} = 92.75\%$, which approximately equals U_p in Fig. 4.2(c), i.e., 92.24 %. Recall that 92.24 % is the average U_p over Monte Carlo simulations. As shown in Figures 4.6(c) and 4.7, the currents of the PPPCs and batteries are always below their limits. Furthermore, all the batteries have the same SOC trajectory, which shows that the batteries will be discharged simultaneously, and U_e is 100 %.



(a)



(b)



(c)

Figure 4.6: PLECS simulation results for full load: (a) output voltage of the BESS, (b) output current of the BESS, and (c) output current of the converters.

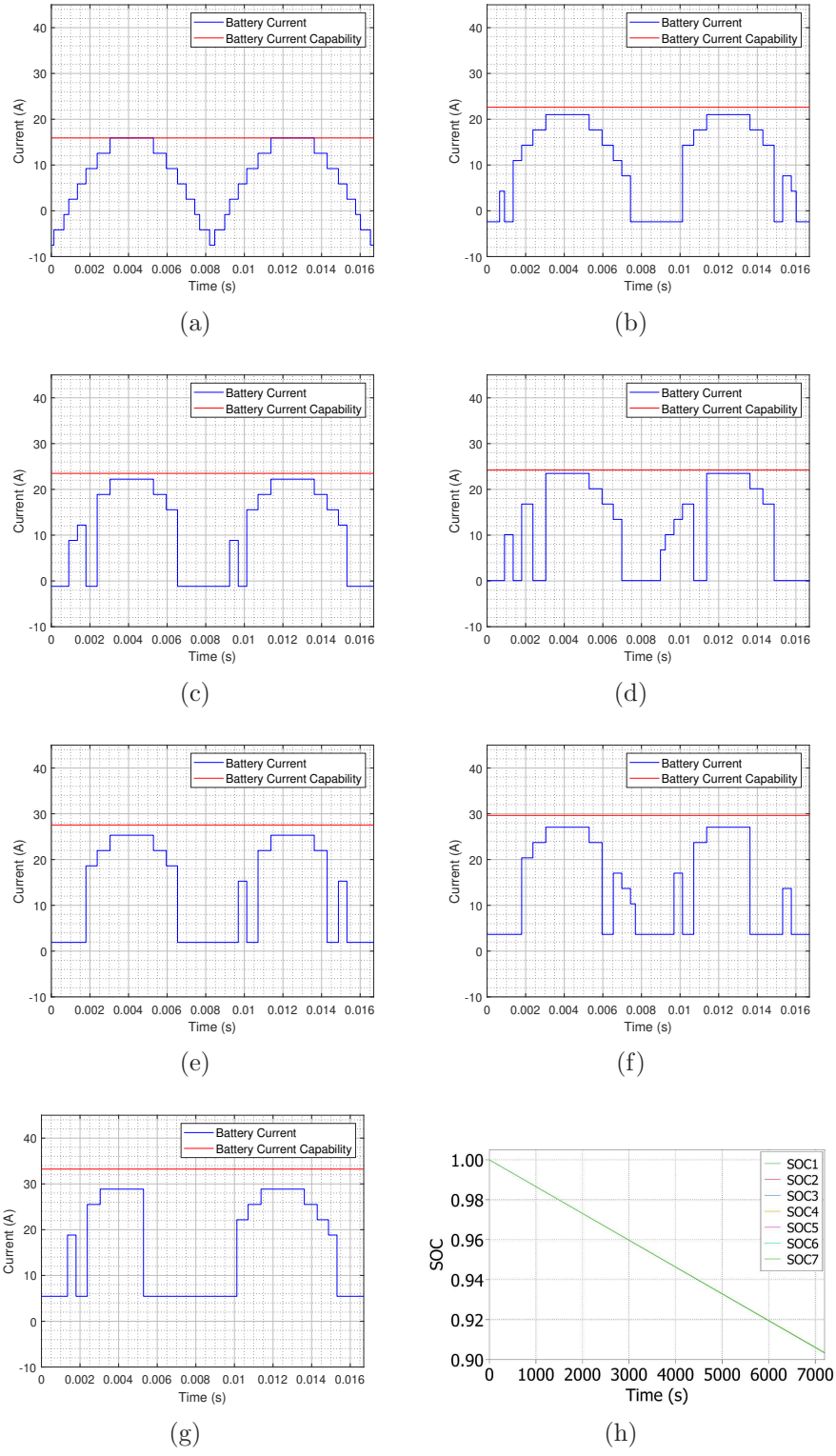
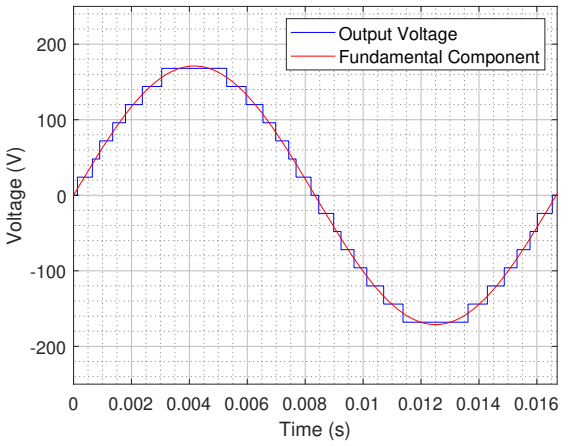


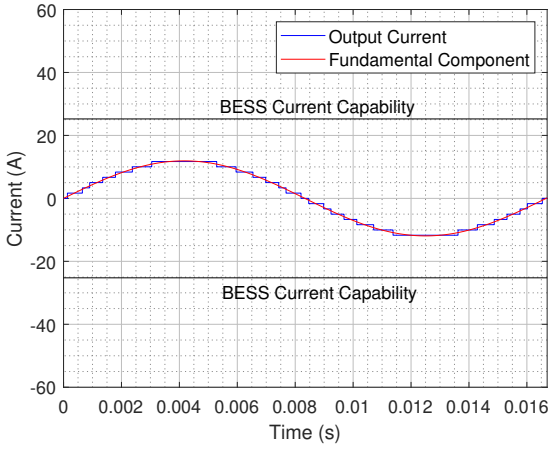
Figure 4.7: PLECS simulation results for full load: current of (a) battery 1 (the weakest battery), (b) battery 2, (c) battery 3, (d) battery 4, (e) battery 5, (f) battery 6, (g) battery 7 (the strongest battery), and (h) SOC of batteries.

4.4.2.2 Half Load

Figures 4.8 and 4.9 show the result of the PLECS simulation for the half load case. In this simulation, the BESS output current's peak value is set to half of the BESS output current's peak value of the previous simulation, i.e., the full load case; consequently, the PPPCs' output currents were halved. As shown, the output voltage of the CHB is a 15-level ac waveform with a fundamental component of 171 V peak (121 V rms). Additionally, the currents of the PPPCs and batteries are always below their limits, as illustrated in Figures 4.8(c) and 4.9. Furthermore, all the batteries have the same SOC trajectory, which shows that the batteries will be discharged simultaneously, and U_{e} is 100 %. Although the batteries discharge slower than the full load case, U_{e} does not change when the magnitude of the output current changes. In this case, U_{p} equals $\frac{11.70\,\mathrm{A}\times 24\,\mathrm{V}\times 7}{25.24\,\mathrm{A}\times 24\,\mathrm{V}\times 7} = 46.35\%$, which is half of U_{p} for the full load case, i.e., 92.75 %. As mentioned in Section 4.3.3, U_{p} obtained from optimization gives us the maximum output current that BESS can provide, which we termed full load. When the output current decreases from this maximum value, U_{p} drops.



(a)



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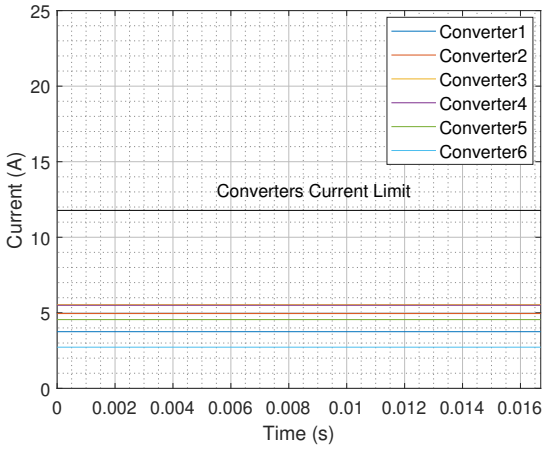


(c)

Figure 4.8: PLECS simulation results for half load: (a) output voltage of the BESS, (b) output current of the BESS, and (c) output current of the converters.

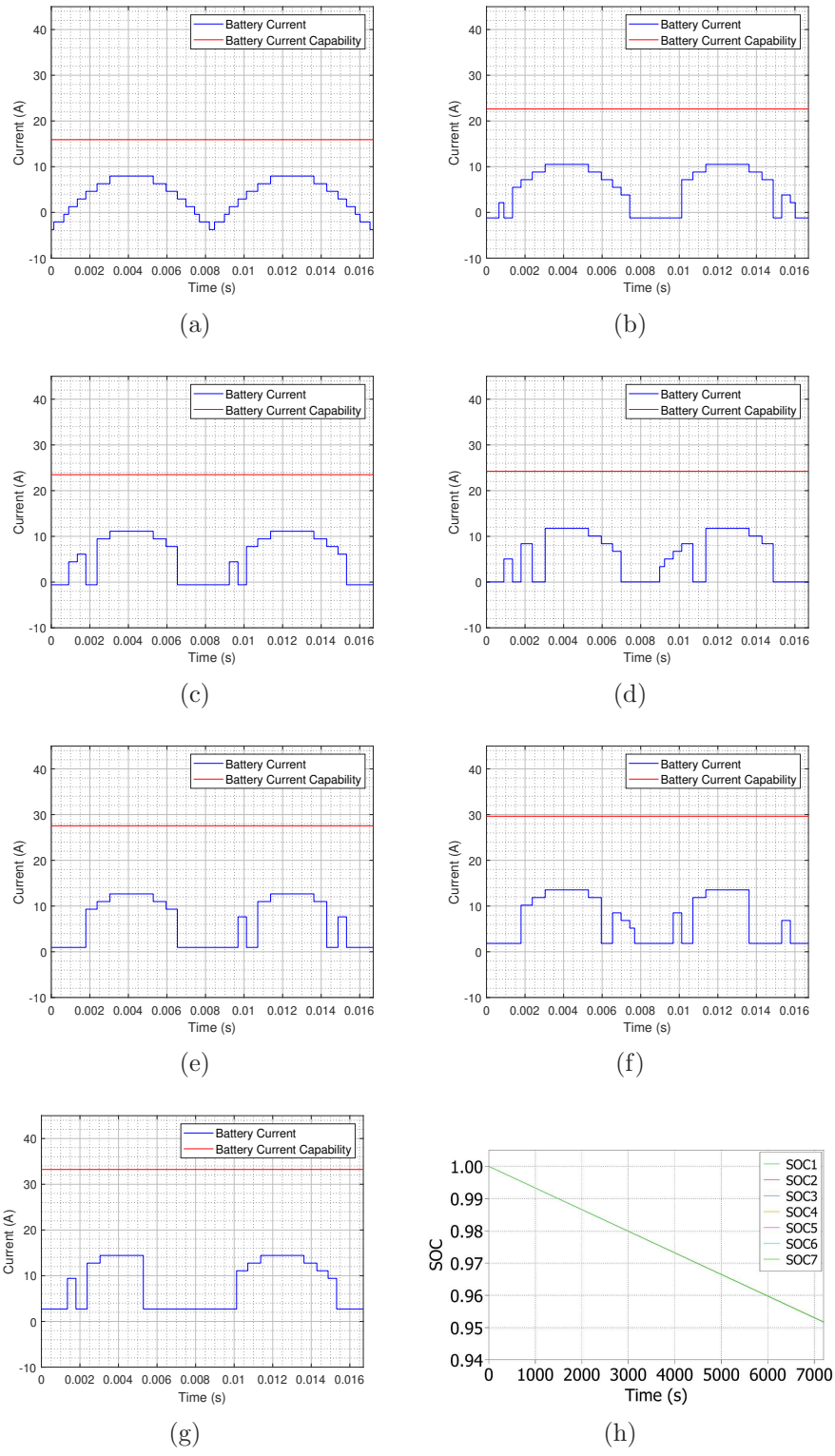


Figure 4.9: PLECS simulation results for half load: current of (a) battery 1 (the weakest battery), (b) battery 2, (c) battery 3, (d) battery 4, (e) battery 5, (f) battery 6, (g) battery 7 (the strongest battery), and (h) SOC of batteries.

4.5 Summary and Contributions

This chapter highlights a framework for optimizing multilevel ac BESSs. Through our simulation validation, we showed that by adding PPPCs to a multilevel inverter, optimizing the power flow of these converters, and optimizing the switching sequence of the inverter's sub-modules, we could achieve perfect SOC balancing among the batteries while maximizing the output power of the BESS. Furthermore, the functionality of the proposed structure and framework was demonstrated through PLECS simulation.

CHAPTER V

Accurate Temperature Measurement of Active Area for Wide-Bandgap Power Semiconductors [1]

5.1 Introduction

Due to high breakdown voltage, low on-resistance, and high speed [38, 95], wide-bandgap power semiconductors are being used in many applications such as wireless power transfer, EVs, hybrid and electric aircraft, and aerospace [38]. Particularly, GaN FETs are lateral power semiconductors with a high electric breakdown field (E_{crit}), low on-state resistance (R_{on}), and low gate width, which leads to low capacitance and gate charge (Q_{g}) [96]. As a comparison, $Q_{\text{g}} \times R_{\text{on}}$ of these devices, which is a figure of merit for switching frequency, is ten times smaller than Si-based FETs [96].

Table 5.1 lists the physical properties of different semiconductors [39, 96], where ε_{r} is the relative dielectric constant and μ_{e} is the electron mobility [96]. As listed, E_{crit} of wide-bandgap semiconductors is larger than Si, which enables them to handle large voltages with smaller sizes and makes them suitable for high-voltage applications. Note that the Baliga Figure of Merit (BFM_{Si}) is proportional to $\text{BV}^2/R_{\text{on}}$ [97], which reflects the resistive losses [96] and is the most commonly used merit for power semiconductors [98]. Additionally, Baliga High-Frequency Figure of Merit (BHFFM_{Si}) is proportional to $1/R_{\text{on}}C_{\text{in}}$ for the

[1] This chapter is adapted from paper [94].

Table 5.1: Physical Properties of Different Semiconductors

Parameter	**Si** [96]	**4H-SiC** [96]	**epi-GaN** [96]	**GaN** [96]	**β-Ga_2O_3** [39]
Bandgap E_g (eV)	1.1	3.26	3.42	3.42	4.8
Electric Breakdown Field E_{crit} (MV/cm)	0.3	2.2	2	3.3	8
Thermal Conductivity k (W/K.cm)	1.5	4.9	1.3	2.3	0.1-0.3
BFM_{Si}, $\varepsilon_r \mu_e E_{crit}^3$	1	223	190	850	3214
$BHFFM_{Si}$, $\mu_e E_{crit}^2$	1	45	36	98	NA

same breakdown voltage (BV) and gate voltage (V_g) [99] and reflects the switching losses [96]. Wide-bandgap semiconductors have high BFM_{Si} and $BHFFM_{Si}$, which means that they have smaller losses than Si and makes them suitable to be used as power switches.

However, the low thermal conductivity of the material and interfaces is typically one of the challenges in wide-bandgap semiconductors like GaN-based and β-Ga_2O_3-based [38, 39, 40, 100] deices. Power semiconductor devices have conduction and switching losses, which cause joule heating within the device [40]. Low thermal conductivity hinders heat transfer from the device, which leads to channel temperature rise and limits the maximum power density of such devices [40]. As listed in Table 5.1, the thermal conductivity of β-Ga_2O_3 is very low, and the situation is not perfect for GaN FETs. Particularly, GaN FETs utilize a two-dimensional electron gas (2DEG) as their channel, and the conduction loss within this thin layer is a highly intensive heat source.

GaN FETs, particularly in power applications, are fabricated on foreign substrates (epi-GaNs) such as Si due to the limitations of large-diameter freestanding GaN fabrication [96]. As listed in Table 5.1, this may aggregate the thermal conduction problem. Using high thermal conductivity materials like SiC and diamond as the foreign substrate for GaN and β-Ga_2O_3 devices is one of the promising solutions to enhance the thermal characteristics of these devices [39, 40, 96, 100].

Wide-bandgap power semiconductors with the highest power-density are chip-scale and do not have a package. Thus, conventional thermal management methods cannot be applied to these semiconductors. In addition to the aforementioned wafer-level approaches for improvement of the thermal characteristics of the high power-density wide-bandgap power semiconductors, various thermal management methods such as jumping-droplet hot-spot cooling [101, 102], liquid bridge confined boiling [103], and immersion cooling [104] have been proposed for chip-scale semiconductors.

Accurate local temperature measurement of the active area is essential in research on wide-bandgap power semiconductors. A common method for temperature measurement of the semiconductors is to attach a thermo-sensitive device like a thermocouple to the device under test (DUT) [101, 102, 104, 105]. However, the thermal resistance of the contact between the thermo-sensitive device and the DUT, as well as lack of proximity to the actual heat source, adds error to the measurement [104, 106]. In other words, a thermo-sensitive device measures the temperature at the outer surface of the DUT and does not accurately detect the temperature within the active area. Another approach uses optical methods like Raman thermometry [100, 106], which usually require expensive equipment and requires clear optical access to the active area.

Employing temperature sensitive electrical parameters (TSEP) is a promising approach to measuring the temperature of power semiconductors, eliminating the need for thermo-sensitive devices and optical equipment. The basic idea of TSEP-based methods is to map a TSEP of the DUT to temperature. Different TSEP-based methods have been proposed for different power semiconductors like FETs and IGBTs. On-state resistance [103, 107, 108], threshold voltage [109], sub-threshold voltage [110], and drain current [111] are among the TSEPs used in the literature for temperature measurement of power semiconductors.

This thesis uses a vector of three TSEPs, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, to extract more information for accurate temperature measurement of the active area in GaN FETs. The DUT is biased at three currents via

precision current sources, and then corresponding voltages are synchronously detected [112] and measured. Finally, the vector of the TSEPs, which we term temperature sensitive electrical vector (TSEV), is mapped to temperature.

5.2 Temperature Measurement Method

5.2.1 Temperature Sensitive Electrical Vector

A particular categorization identifies FETs having three different regions of operation: weak, moderate, and strong inversion regions. Figure 5.1 illustrates the I_{d}-V_{gs} curve of a diode-connected GaN FET with labeled regions of operation. In the strong inversion region $V_{\mathrm{gs}} \gg V_{\mathrm{th}}$, whereas in the weak inversion/sub-threshold region, $V_{\mathrm{gs}} < V_{\mathrm{th}}$. Additionally, the transition region between these two regions of operation is termed moderate inversion [113]. For a MOSFET, I_{d} has a quadratic relationship with V_{gs} in the strong inversion region (in saturation mode $V_{\mathrm{ds}} \geq V_{\mathrm{gs}} - V_{\mathrm{th}}$) [113],

$$I_{\mathrm{d}} \simeq \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}} W}{2L} \left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)^2, \tag{5.1}$$

while it has an exponential relationship with V_{gs} in the weak inversion region [113],

$$I_{\mathrm{d}} \simeq \frac{W I_{\mathrm{d0}}}{L} \exp\left(\frac{V_{\mathrm{gs}}}{n\left(kT/q\right)}\right), \tag{5.2}$$

where I_{d} is the drain current, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, W is the channel width, L is the channel length, μ_{n} is the mobility of electrons, C_{ox} is the oxide capacitance, n is the sub-threshold slope factor, k is the Boltzmann constant, T is the average temperature of the active area, q is the electron charge, and I_{d0} is a processed-dependent parameter that depends on V_{th} and source-bulk voltage V_{sb} [113]. Although the corresponding equations for different GaN FETs with different structures may differ from (5.1) and (5.2), the general temperature dependency remains the same [114, 115, 116]. From (5.1), and for a

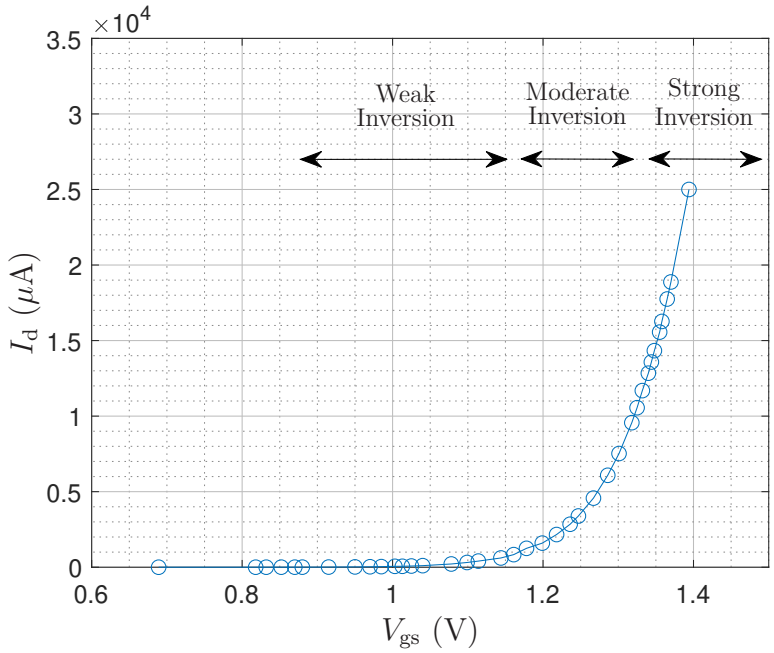


Figure 5.1: Experimental example I_d versus V_{gs} of a diode-connected GaN FET illustrating different regions of operation.

fixed I_d, V_{gs} is temperature-dependent because V_{th}, μ_n, and C_{ox} are temperature-dependent. Additionally, from (5.2) and for a fixed I_d, V_{gs} is directly proportional to the temperature, while I_{d0} is also temperature-dependent. This thesis uses a vector of V_{gs} at three biasing currents as a TSEV, i.e., ($V_{gs,wi}$, $V_{gs,mi}$, $V_{gs,si}$). $V_{gs,wi}$, $V_{gs,mi}$, and $V_{gs,si}$ are the gate-source voltage when the DUT is biased at weak, moderate, and strong inversion regions, respectively.

5.2.2 Measurement Circuits and Systems

We configure the DUT as a diode-connected FET [117] by shorting the gate and drain, as shown in Fig. 5.2. Note that a diode-connected FET with $V_{gs} \geq V_{th}$ is always in the saturation mode because $V_{ds} = V_{gs} \geq V_{gs} - V_{th}$. In order to bias the DUT at certain current values, three precision current sources (i.e., I_1, I_2, and I_3) are connected to the DUT via switches S_1, S_2, and S_3, respectively. This way, the current through the DUT alternates between these three current values. Note that switches S_1', S_2', and S_3' are complementary of

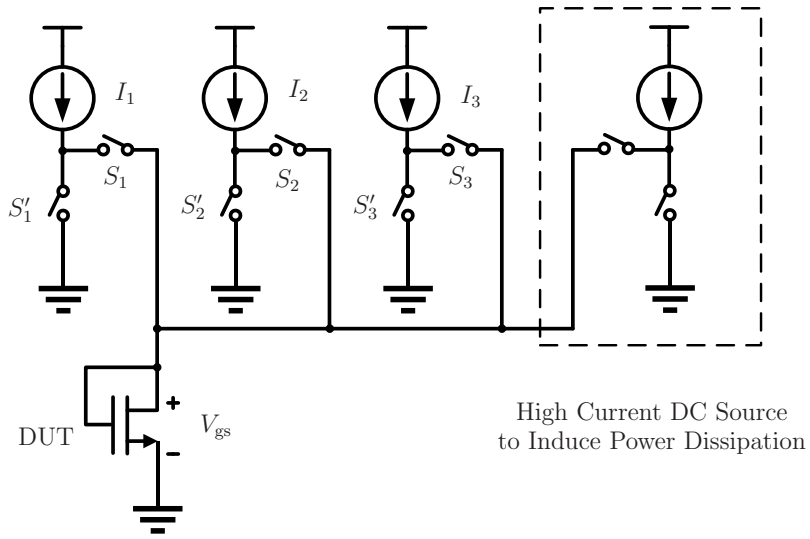


Figure 5.2: Schematic of the electrical setup with a method to induce device power dissipation.

switches S_1, S_2, and S_3, respectively, to short the corresponding current source to the ground while one of the other current sources is being pumped into the DUT. V_{gs} is sent to the precision voltage measurement board via a Kelvin connection. On the voltage measurement board, V_{gs} is then synchronously detected [112] and measured for each current source. It is worth noting that, DUT power dissipation can be induced by interleaving a high current dc source, which is also illustrated in Fig. 5.2.

5.2.2.1 Precision Current Sources

The precision current sources in Fig. 5.2 are designed as shown in Fig. 5.3. PNP transistors, in a feedback loop closed by op-amp A_2, act as the voltage-controlled current source. Note that, in order to have a good common-mode rejection in the measurement board, the load (DUT) is grounded. Thus the current sources are floated, and we need to provide level shifting by an instrumentation amplifier (A_1). The output current of the current sources is calculated as $I_{out} = \frac{V_{ref}}{R_{shunt}}$, where an accurate voltage reference provides V_{ref}. Having a high output resistance is essential for a precision current source, especially at low currents. So, PNP transistors are used because of their high output resistance. We cascoded [117]

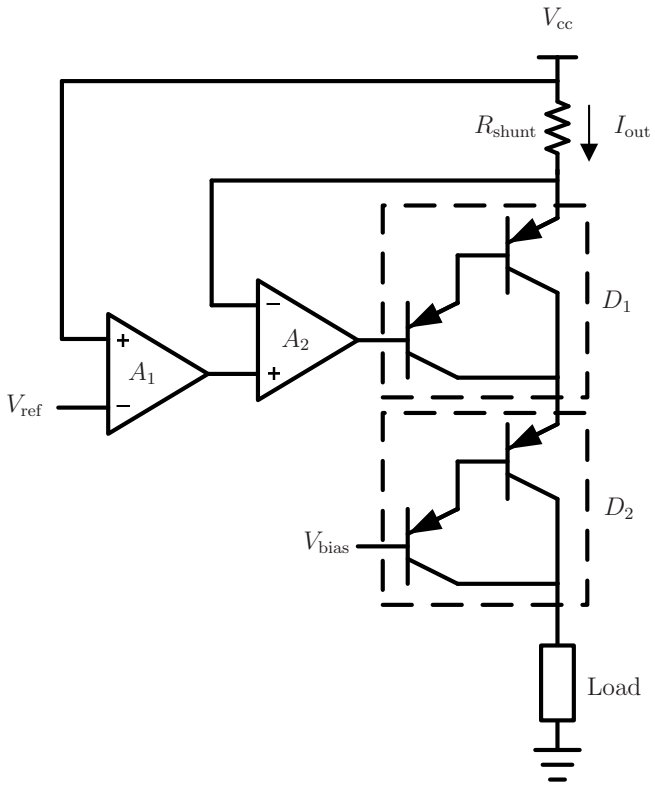


Figure 5.3: Schematic of the current sources.

two Darlington [65] structures (D_1 and D_2) to further enhance the output resistance of the current sources.

The current sources are carefully designed and precision components are cautiously chosen. A precision voltage reference generates the reference voltage for the current sources. Low leakage diodes and logic-level MOSFETs are used as switches S_1-S_3 and S_1'-S_3', respectively. The control signals for logic-level MOSFETs come from a microcontroller (MCU) through digital isolators. The selected amplifiers have low offset voltage, low input bias current, low noise, and low-temperature drift. The shunt residences and all resistances of the voltage dividers are also precision resistances with ultra-low temperature drift coefficients.

5.2.2.2 Precision Voltage Measurement

Figure 5.4(a) shows the schematic of the measurement board. Stage_1 is a buffer stage for the differential signals, V_{m}^{+} and V_{m}^{-}, which come from the DUT. In Stage_2, the phase

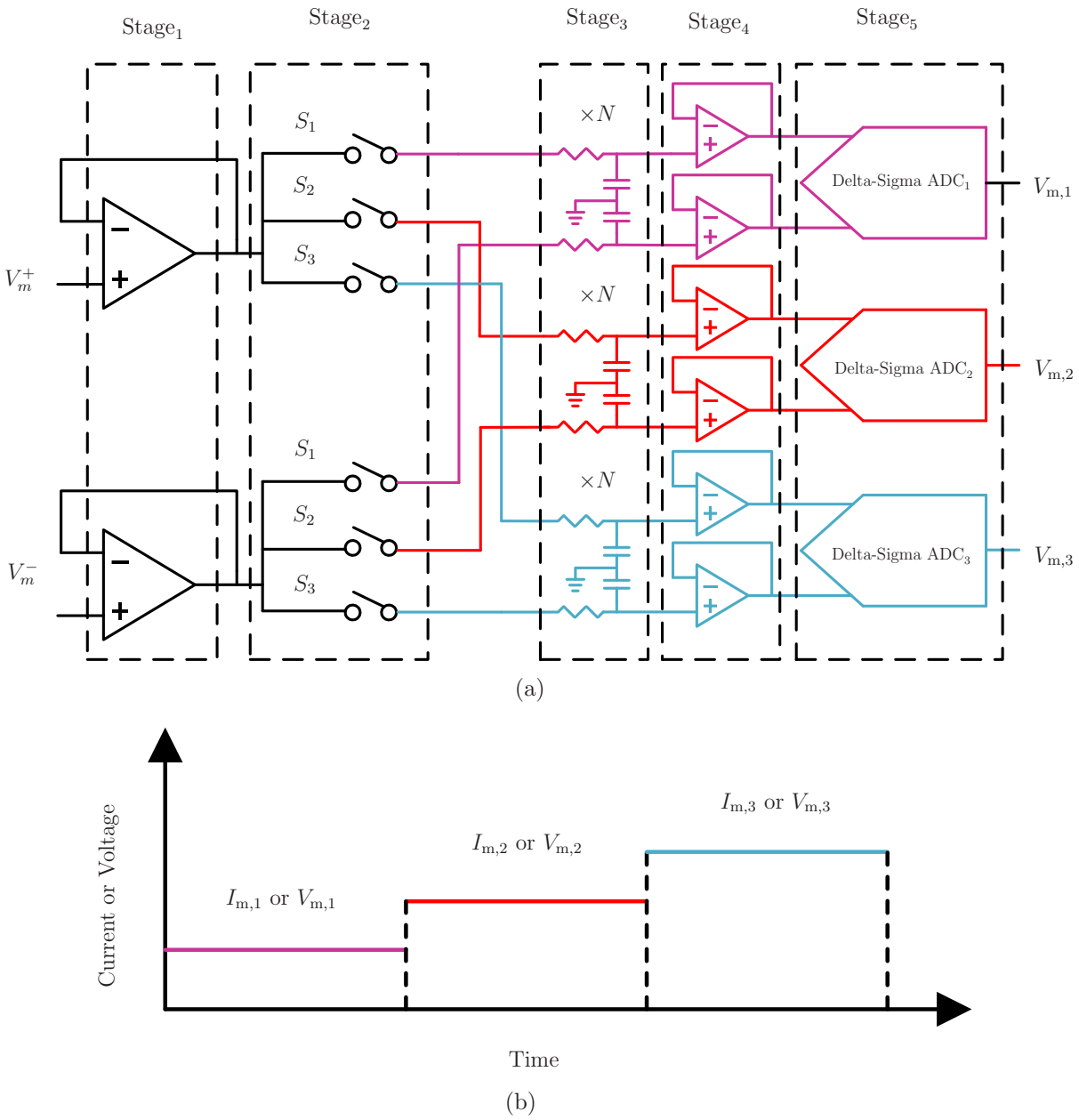


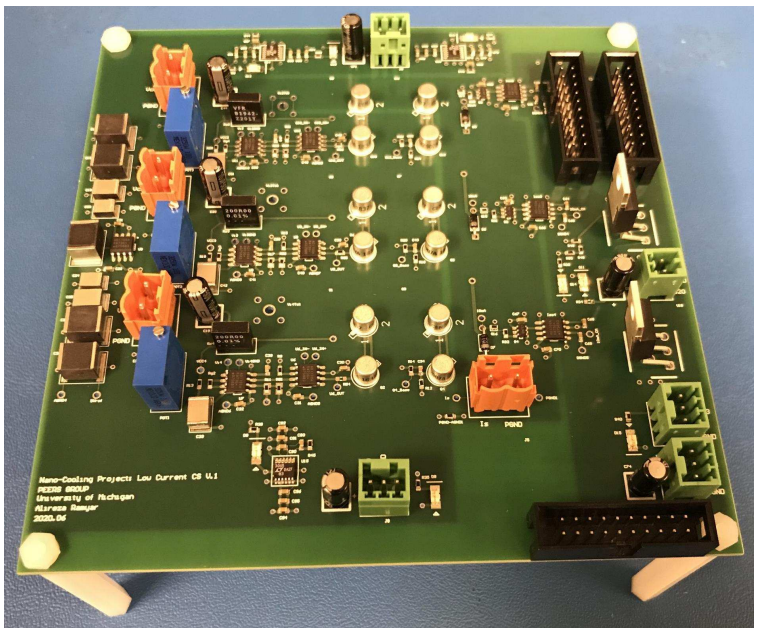
Figure 5.4: (a) Schematic of the measurement board. (b) Synchronous detection sequence.

of the measurement is selected via an analog switch. The control signals for the analog switch come from an MCU through digital isolators. After that, the signals are filtered by Stage_3 containing N cascaded RC filters. In Stage_4, voltage-followers are used to drive the analog-to-digital converters (ADC) of Stage_5. This structure acts as a sample and hold circuit where the analog switch samples the signal and the capacitors hold the signal to be converted by an ADC [118]. Note that the outputs of Stage_3 are dc signals, so we use delta-sigma ADCs, which are slow but highly accurate. A precision voltage reference generates the reference voltage for the ADCs. Finally, the ADCs send the measured values to the MCU through digital isolators using 3-wire serial peripheral interface (SPI) communication.

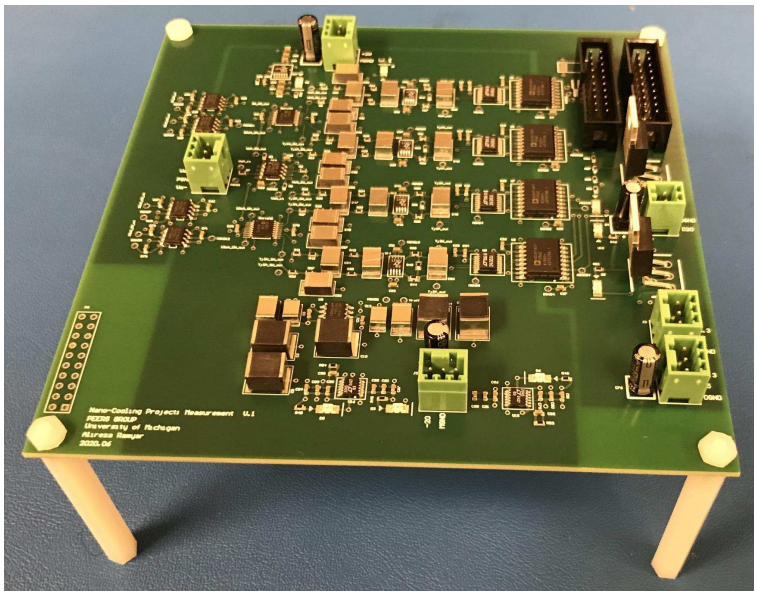
Note that switches S_1-S_3 in Fig. 5.4(a) are synchronous with switches S_1-S_3 in Fig. 5.2, respectively. As shown in Fig. 5.4(b), at each time interval, one of the current sources is pumping a certain amount of current into the DUT, which results in a specific voltage across the DUT. Using this circuitry and signal conditioning, the voltage across the DUT is synchronously detected for each current source [112]. Figure 5.5 shows photographs of the current source and the measurement boards.

5.2.3 Principal Component Analysis and Polynomial Regression

Since the features, i.e., $V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, and $V_{\text{gs,si}}$, are observed to be highly correlated, principal component analysis (PCA) is performed on the original data to reduce the multicollinearity while preserving as much information as possible. PCA is a method for dimensionality reduction that uses singular value decomposition to project the data onto a lower-dimensional space with uncorrelated variables known as principal components [119]. We then select the principal components we want to use based on their *explained variance ratio*. Explained variance ratio is a metric for selecting principal components based on their contribution to explaining the variance in the data [119]. Here, we select the first two principal components (i.e., PC_1 and PC_2) and find the projections of the original data onto them, i.e., $V_{\text{p,1}}$ and



(a)



(b)

Figure 5.5: Photographs of: (a) current source board, and (b) measurement board.

$V_{\mathrm{p,2}}$,

$$\left(V_{\mathrm{gs,wi}}, V_{\mathrm{gs,mi}}, V_{\mathrm{gs,si}}\right) \quad \longmapsto \quad \left(V_{\mathrm{p,1}}, V_{\mathrm{p,2}}\right). \tag{5.3}$$

We then apply a 2$^{\mathrm{nd}}$ order polynomial regression on ($V_{\mathrm{p,1}}$, $V_{\mathrm{p,2}}$), which results in the following equation for temperature

$$\begin{aligned} \mathrm{T}\left(V_{\mathrm{p,1}}, V_{\mathrm{p,2}}\right) &= C_1 + \left(C_2 \times V_{\mathrm{p,1}}\right) + \left(C_3 \times V_{\mathrm{p,2}}\right) \\ &+ \left(C_4 \times V_{\mathrm{p,1}}^2\right) + \left(C_5 \times V_{\mathrm{p,1}} \times V_{\mathrm{p,2}}\right) + \left(C_6 \times V_{\mathrm{p,2}}^2\right), \end{aligned} \tag{5.4}$$

where C_1 is the intercept term and C_2-C_6 are the coefficients of the regression model.

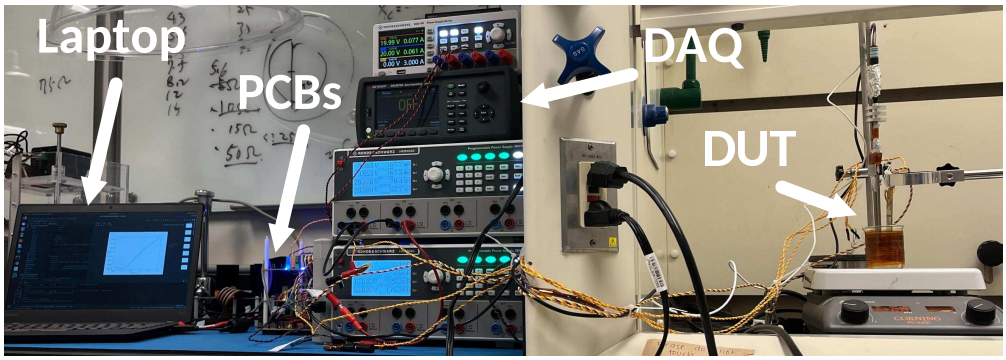
5.3 Hardware Demonstration

The hardware setup shown in Fig. 5.6(a) was used to demonstrate the measurement method. Current values of 25 μA, 2.5 mA, and 25 mA were selected as the biasing points of two DUTs (i.e., an EPC2019 GaN FET and an EPC2007C GaN FET) at weak, moderate, and strong inversion regions, respectively; it is worth noting that the choice of these currents need to reflect the current density and hence depend on the device size.

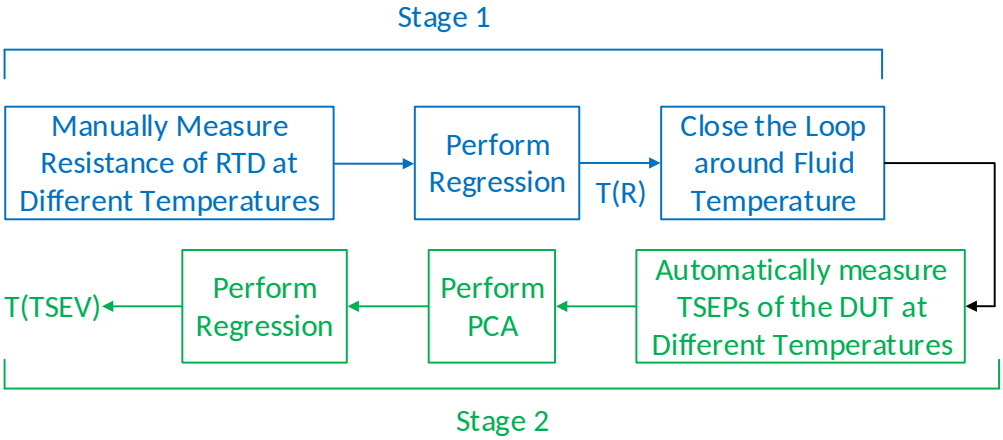
5.3.1 Hardware Setup

The DUT, a 4-wire resistance temperature detector (RTD) probe and an ultra-accurate digital thermometer were immersed in a beaker filled with mineral oil. The beaker was evenly surrounded with nichrome wires to symmetrically heat up the fluid and reduce the effects of thermal convection within the beaker. Additionally, a magnetic stirring bar was placed at the bottom of the beaker to rotate at 100 rpm using a magnetic stirrer. This way, we homogenize the fluid temperature, so the temperature of the GaN FET, including the temperature of the GaN FET's active area, equals the fluid temperature.

We employed a two-stage experimental procedure, as shown in Fig. 5.6(b). In Stage 1,



(a)



(b)

Figure 5.6: (a) A photograph of the hardware setup. (b) Diagram of the experimental procedure.

the RTD probe was calibrated against an ultra-accurate digital thermometer at temperatures in the range of 300-420 K. Then, a linear regression was applied to the data to obtain T(R), which reflects temperature as a function of the resistance of the RTD probe. Finally, we closed the loop around the fluid temperature. In Stage 2, we set the fluid temperature to different values in the range of 300-420 K and automatically measured the TSEV of the DUT. After performing PCA, a polynomial regression was applied to the data to obtain T(TSEV), which is the map of the GaN FET's TSEV to the temperature of the GaN FET's active area.

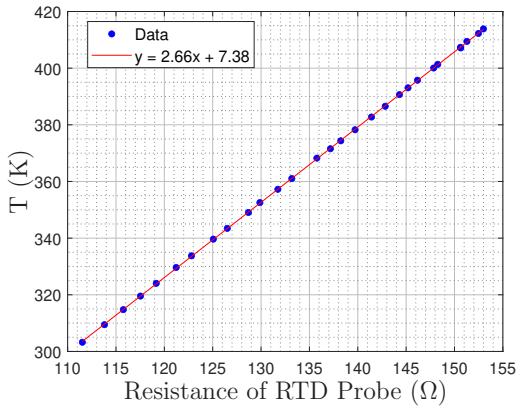
5.3.2 Hardware Results

5.3.2.1 Stage 1

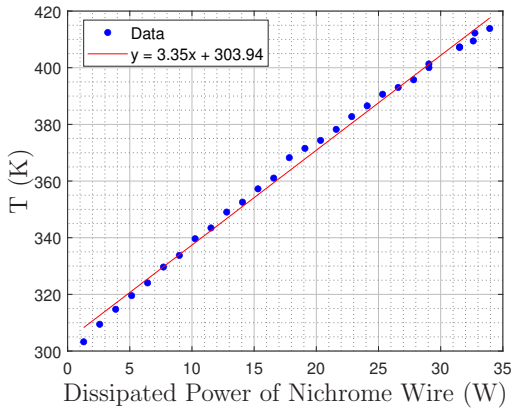
The results of Stage 1 are shown in Fig. 5.7. As shown in Fig. 5.7(a), the resistance of the RTD probe has a highly linear relationship with temperature, which is expected. Note that the slope of the plot shown in Fig. 5.7(b), i.e., 3.35, is the dc gain from the dissipated power of the nichrome wire to the fluid temperature. This information, together with the step response of the system (from the dissipated power of the nichrome wire to the fluid temperature), was used to model the plant and design a controller to track the fluid temperature with a reasonable speed. One of the challenges in designing the controller was the time delay due to the thermal diffusion, which was approximated by a pole and a non-minimum phase zero. The open-loop transfer function from the dissipated power of the nichrome wire to the fluid temperature is

$$\frac{T(s)}{P(s)} = \frac{K\left(\frac{2}{T_\mathrm{d}} - s\right)}{(s+p)\left(\frac{2}{T_\mathrm{d}} + s\right)}, \tag{5.5}$$

where p is the plant's pole, $\frac{K}{p}$ is the dc gain, and T_d is the time delay. A PI controller was then designed and tuned to enable tracking of the fluid temperature and automation of the Stage 2. Figure 5.7(c) shows the temperature of the fluid when we set the fluid temperature



(a)



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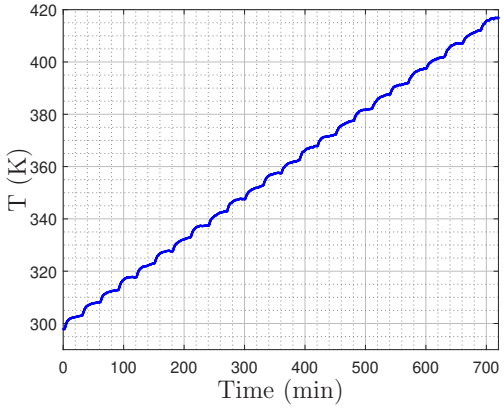


(c)

Figure 5.7: Hardware results of Stage 1: (a) fluid temperature versus resistance of RTD probe, (b) fluid temperature versus dissipated power of nichrome wire, and (c) example fluid temperature at different set points for closed-loop system.

to values in the range of 300-420 K with a step size of 5 K and let it settle in 30 min. As illustrated, the controller works properly, and we are ready for Stage 2. Figures 5.8 and 5.9 show the results of Stage 2 for two different DUTs, i.e., an EPC2019 GaN FET and an EPC2007C GaN FET, respectively.

5.3.2.2 Stage 2: EPC2019 GaN FET

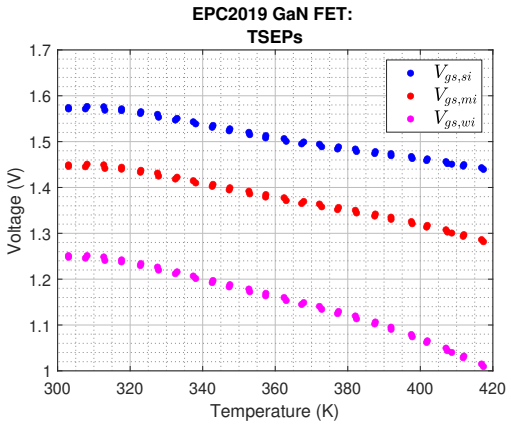
Figure 5.8(a) shows the measured $V_{\mathrm{gs,wi}}$, $V_{\mathrm{gs,mi}}$, and $V_{\mathrm{gs,si}}$ of the DUT at 49 data points. After performing PCA, we selected the first two principal components (i.e., PC_1 and PC_2) with explained variance ratios of 99.60 % and 0.39 %, respectively. We then applied a 2^{nd} order polynomial regression on ($V_{\mathrm{p,1}}$, $V_{\mathrm{p,2}}$), which results in the following equation for temperature

$$\begin{aligned} \mathrm{T}\left(V_{\mathrm{p,1}}, V_{\mathrm{p,2}}\right) &= 372.86 + \left(38.81 \times V_{\mathrm{p,1}}\right) + \left(10.33 \times V_{\mathrm{p,2}}\right) \\ &- \left(14.08 \times V_{\mathrm{p,1}}^2\right) - \left(2.50 \times V_{\mathrm{p,1}} \times V_{\mathrm{p,2}}\right) + \left(1.97 \times V_{\mathrm{p,2}}^2\right). \end{aligned} \tag{5.6}$$

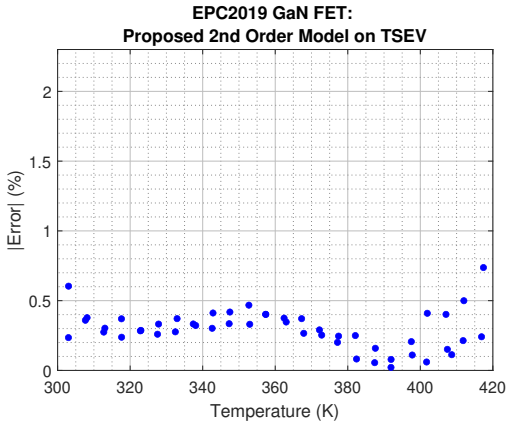
The temperature measurement error is determined using leave-one-out cross-validation (LOOCV) [120]. For each data point, all the other data points form the training dataset of the regression model, and the corresponding data point is used as the test data point. Figure 5.8(b) shows the values of the error, which were calculated from

$$|\mathrm{Error}| = \left| \frac{T_{\mathrm{actual}} - T_{\mathrm{predicted}}}{T_{\mathrm{actual}}} \right| \times 100, \tag{5.7}$$

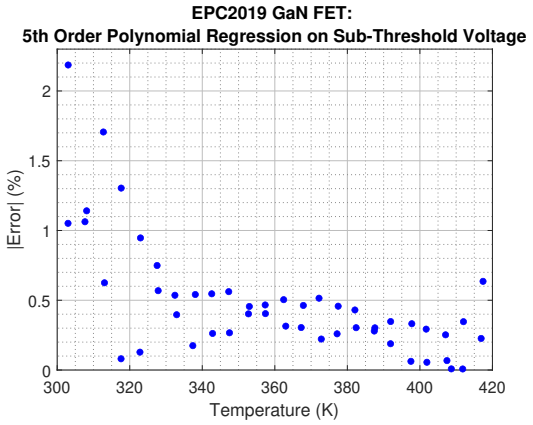
where T_{actual} is the measured temperature and $T_{\mathrm{predicted}}$ is the predicted temperature by the model. As the results show, the measurement method has an accuracy of better than 99 %. For comparison, the results of a 5^{th} order polynomial regression applied on the sub-threshold voltage (i.e., $V_{\mathrm{gs,wi}}$) is shown in Fig. 5.8(c). Note that both models have one intercept term and five coefficients and hence, have similar complexities. As illustrated, using three voltages at different operation regions results in a more accurate temperature measurement than the case in which we only use sub-threshold voltage.



(a)

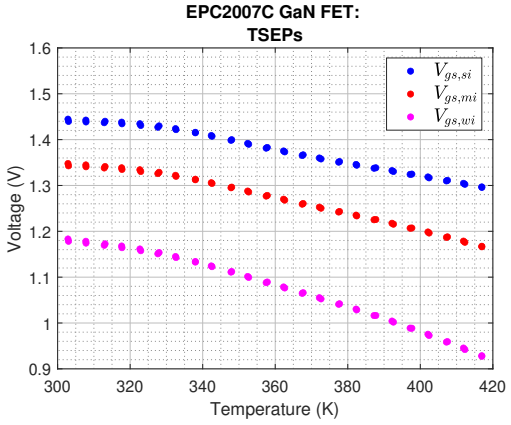


(b)

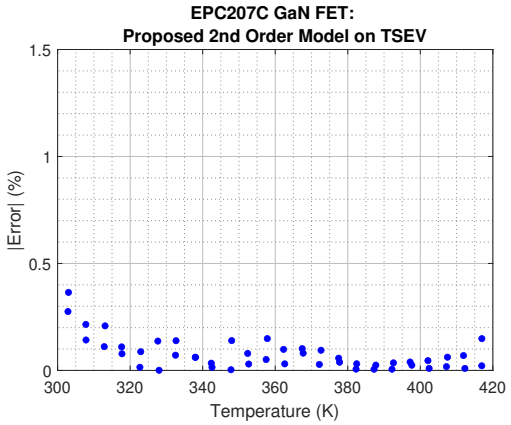


(c)

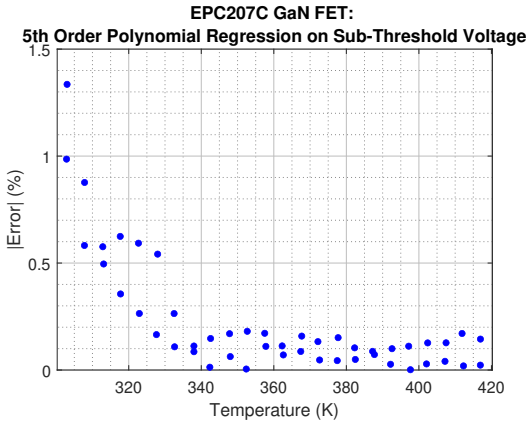
Figure 5.8: Hardware results for Stage 2 (EPC2019 GaN FET): (a) $V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, and $V_{\text{gs,si}}$ at different temperatures, (b) error at different temperatures for proposed 2^{nd} order model on TSEV, i.e., ($V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, $V_{\text{gs,si}}$), and (c) error at different temperatures for 5^{th} order polynomial regression on sub-threshold voltage, i.e., $V_{\text{gs,wi}}$.



(a)



(b)



(c)

Figure 5.9: Hardware results for Stage 2 (EPC2007C GaN FET): (a) $V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, and $V_{\text{gs,si}}$ at different temperatures, (b) error at different temperatures for proposed 2^{nd} order model on TSEV, i.e., ($V_{\text{gs,wi}}$, $V_{\text{gs,mi}}$, $V_{\text{gs,si}}$), and (c) error at different temperatures for 5^{th} order polynomial regression on sub-threshold voltage, i.e., $V_{\text{gs,wi}}$.

5.3.2.3 Stage 2: EPC2007C GaN FET

Figure 5.9(a) shows the measured $V_{\mathrm{gs,wi}}$, $V_{\mathrm{gs,mi}}$, and $V_{\mathrm{gs,si}}$ of the DUT at 48 data points. Again, we selected the first two principal components (i.e., PC_1 and PC_2) with explained variance ratios of 99.90 % and 0.09 %, respectively. We then applied a 2^{nd} order polynomial regression on ($V_{\mathrm{p,1}}$, $V_{\mathrm{p,2}}$), which results in the following equation for temperature

$$\begin{aligned} \mathrm{T}\left(V_{\mathrm{p,1}}, V_{\mathrm{p,2}}\right) &= 367.70 + \left(36.93 \times V_{\mathrm{p,1}}\right) + \left(4.98 \times V_{\mathrm{p,2}}\right) \\ &- \left(8.47 \times V_{\mathrm{p,1}}^2\right) - \left(0.92 \times V_{\mathrm{p,1}} \times V_{\mathrm{p,2}}\right) + \left(0.67 \times V_{\mathrm{p,2}}^2\right). \end{aligned} \tag{5.8}$$

Figure 5.9(b) shows the values of the error at different data points. Similar to the case of the EPC2019 GaN FET, the measurement method has an accuracy of better than 99 %. As shown, using three voltages at different operation regions results in a more accurate temperature measurement than the case in which we only use sub-threshold voltage, i.e., Fig. 5.9(c).

5.4 Summary and Contributions

Alireza Ramyar and Yukun Lou collaborated in obtaining the hardware results in Section 5.3. The circuits were adapted from the design by Xin Zan and Yanqiao Li.

This chapter highlights an accurate temperature measurement method for characterizing the thermal performance of practical wide-bandgap power devices in-situ. Through the hardware results, we showed that using a vector of three TSEPs, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, the temperature of the active area can be measured with high accuracy.

CHAPTER VI

Conclusions, Contributions, and Future Work

The sustainability of energy resources is one of the major challenges for human beings. The shortage of conventional energy resources and their pollution escalates the problem, and we are looking for other resources like solar energy to power our cities and industries, and for the same reasons, we are thinking of using electric vehicles. However, it is not that easy, and there are several challenges in using these clean energy resources. We need to spend energy to harvest renewable energy resources; we need specific and sometimes rare materials for these alternative solutions; using these alternative resources within the established infrastructures requires extra effort and adaptation. Power electronics is an essential part of the solution to these challenges. By processing the power through power electronics interfaces, we can control and adapt the power and energy of these alternative resources and also make these alternative energy resources more efficient, saving the energy and raw materials required to produce them.

This thesis investigated (1) power processing architectures and methods to harvest power in solar photovoltaic systems efficiently, (2) power processing architectures and methods to employ second-use battery energy storage systems optimally, and (3) temperature measurement of wide-bandgap power semiconductors, which are widely used in solar photovoltaic systems and battery energy storage systems.

6.1 Conclusions

Solar power is one of the greatest alternative energy resources, with photovoltaics as the most prevalent harvesting platform. As an example, in the U.S., installation of the grid-connected distributed solar photovoltaic systems has increased from 800/year in 2000 to over 374000/year in 2019 [3]. One of the challenges in solar photovoltaic systems is cell mismatch and partial shading. Reduction of accessible power, non-convexity in maximizing output power, and hotspots are some of the problems arising from mismatch and partial shading. Differential diffusion charge redistribution structure is a solution to the shading problem. However, this architecture is a two-port structure, and we need new hardware that can be integrated with it to benefit from its advantages. We addressed this issue and investigated novel power processing architectures and methods for differential diffusion charge redistribution solar photovoltaic modules.

On the other hand, the utilization of battery energy storage systems for supporting solar photovoltaic systems has increased recently. In 2019, 1.4 % of the small and 5 % of the large nonresidential solar photovoltaic systems in the U.S. employed battery energy storage systems, and this trend is increasing [3]. However, producing new batteries for these systems results in a huge amount of emissions. A possible solution to this issue is to reuse retired electric vehicles' batteries in battery energy storage systems. When removed from the vehicle, these batteries still have approximately 80% capacity and power capability [30, 31]. Reusing these batteries in second-use battery energy storage systems provides a sustainable solution that adds economic value to the batteries. Nonetheless, reusing second-use batteries results in the challenge of a heterogeneous supply. Even with second-use batteries that are identical at the time of original manufacturing and installed in identical vehicles, these batteries, when removed, will exhibit a significant degree of variation. We addressed this issue and investigated new power processing architectures and methods for second-use battery energy storage systems for DC and AC applications.

Semiconductor devices are one of the key elements in power electronics that significantly

affect the entire system's performance and efficiency. Power electronics used in sustainable energy resources like solar photovoltaic battery energy storage systems are not exempt. Due to high breakdown voltage, low on-resistance, and high speed, wide-bandgap power semiconductors are being used in many applications. However, the low thermal conductivity of the material and interfaces is typically one of the challenges in wide-bandgap power semiconductors. Thus, accurate local temperature measurement of the active area is essential in research on wide-bandgap power semiconductors, such as cooling methods, packaging, and optimizing the partitioning of the switch modules. In the end, an accurate temperature measurement method for wide-bandgap power semiconductors will help to design more efficient and decent devices, which results in more efficient power electronics for various applications such as solar photovoltaic and battery energy storage systems. We addressed this issue and investigated temperature measurement of the active area for wide-bandgap power semiconductors.

6.2 Contributions

Chapter II investigated a reconfigurable and scalable hardware emulator for differential diffusion charge redistribution solar photovoltaic modules. We introduced a two-port up/down dc-dc converter that performs two-dimensional maximum power point tracking for differential diffusion charge redistribution solar photovoltaic modules. We discussed the converter's control strategy and proved the feasibility of the control scheme for maximum power point tracking. We also introduced a new measurement method for dynamic parameters of solar photovoltaic cells, which can measure the diffusion capacitance, the parasitic inductance, and the quality factor of the solar photovoltaic cells. All these architectures and methods were validated via hardware demonstration.

In Chapter III, we introduced a new stochastic method for lite-sparse hierarchical partial power processing architecture to optimize power processing of second-use battery energy storage systems over the potential lifetime of batteries. Through simulation and hardware demonstration, we showed that lite-sparse hierarchical partial power processing architecture

has a better performance compared to conventional partial power processing and full power processing architectures over the lifetime of the second-use batteries. Additionally, a reliable hierarchical system monitoring and control for power conversion in battery energy storage systems was investigated and demonstrated through a hardware testbed. The proposed system monitoring and control consists of a central monitoring and control unit together with distributed monitoring and control agents for each battery and power conversion unit. Finally, we demonstrated some of the challenges of lite-sparse hierarchical partial power processing architecture that need to be addressed. These challenges suggest that a new framework is needed to limit the search spaces for optimization problems and effectively decrease the computational costs. The foundation of such a framework was introduced in Appendix A.

Chapter IV investigated a framework for optimizing multilevel ac battery energy storage systems. Through the simulation validation, we showed that by adding partial power processing converters to a multilevel inverter, optimizing the power flow of these converters, and optimizing the switching sequence of the inverter's sub-modules, we could achieve perfect state-of-charge balancing among the batteries while maximizing the output power of the battery energy storage system. Furthermore, the functionality of the proposed structure and framework was demonstrated through PLECS simulation.

In Chapter V, we introduced an accurate temperature measurement method for wide-bandgap power semiconductors. These devices are suitable for many applications, such as solar photovoltaic systems and battery energy storage systems. Through the hardware results, we showed that using a vector of three temperature sensitive electrical parameters, i.e., the gate-source voltage biased at weak, moderate, and strong inversion regions, the temperature of the active area can be measured with high accuracy.

6.3 Future Work

We can finalize the framework introduced in Appendix A and utilize it for optimization of power processing architectures like second-use battery energy storage systems when the computational cost is high; like interconnection selection in optimization of Chapter III or Charge-Matrix selection in optimization of Chapter IV. One can also take into account the actual cost of batteries and power electronics in the optimization designs discussed in Chapter III and Chapter IV. Particularly, for the framework introduced in Chapter IV, we may relax the state-of-charge balancing constraints and compromise between energy and power utilization based on the cost of batteries and power converters. Additionally, emissions from using second-use batteries should be addressed. Although reusing retired batteries reduces the production-phase emissions from the production of new batteries for battery energy storage systems, the use-phase emissions of employing second-use batteries instead of new batteries need to be studied. Charging profiles of batteries can be different for new and second-use batteries based on the power processing architecture employed in the battery energy storage system, which means that the use-phase emissions can be different for battery energy storage systems and second-use battery energy storage systems.

APPENDIX

APPENDIX A

An Energy Network for Modeling of Power Processing Architectures

We aim to investigate a graph-based representation of power processing architectures like battery energy storage systems (BESS). Graph theory has been widely used for modeling, design, control, and optimization in the power electronics field. A comprehensive categorization of the graph theory applications in the power electronics area has been delineated in [121]:

- component-level applications, including filter design [122] and PCB layout automation [123],
- converter-level applications, including power converter synthesis using algebraic graph-theory [124], power converter derivation using circuit duality [125] and graphical isomorphism [126], and
- system-level applications including, decentralized [127] and centralized [128] power flow management in multi-agent power systems.

As one of the essential applications of graph theory, network flows have been widely used for communication, transportation, and the study of power flows [121, 129]. However, their

application for power processing architectures, like modular dual active bridges (DAB) [129], is an emerging research topic [121]. Here, we investigate an architecture-level network flow framework, somewhere in between converter-level and system-level, for power processing architectures like BESSs. Before analyzing our framework, we need to introduce basic terminology, and for this purpose, the definitions in [130] have been used as follows.

A.1 Basic Graph Theory Terminology

- A *graph* $G = (N, E)$ is a pair of two sets where the elements of E are 2-element subsets of N.
- N is the set of graph's *nodes/vertices*.
- E is the set of graph's *edges*.
- Two nodes (n_1 and n_2) are *adjacent*, if $\{n_1, n_2\} \in E$.
- A *direct graph* (*digraph*) is a graph together with two maps assigning to each edge $e \in E$ an *initial node* $\text{init}(e)$ and a *terminal node* $\text{ter}(e)$, respectively. Then, e is a *directed edge* from $\text{init}(e)$ to $\text{ter}(e)$. Note that in a digraph, there can be more than one edge between two nodes.
- A *loop* is an edge e for which the initial and terminal nodes are the same, i.e. $\text{init}(e) = \text{ter}(e)$.
- A *network/weighted graph* is a graph whose edges are weighted and carry a flow.
- A map (M) from a graph (G_1) to another graph (G_2) is a *homomorphism* if it preserves the adjacency of the nodes.
- If a homomorphic map (M) from a graph (G_1) to another graph (G_2) is bijective and its inverse is also a homomorphism, we call M an *isomorphism* and say that G_1 and G_2 are *isomorphic*, i.e., $G_1 \simeq G_2$.

- If a class of graphs is closed under isomorphism, we call it a *graph property*.

A.2 Energy Network Principles

Here, we investigate a *directed network* for modeling of power processing architectures which we call an *energy network*. The general rules of the energy networks are as follows:

- The nodes are the components of the power processing architecture like batteries (B), electrical loads (L), power converters (U), or solar photovoltaic components (PV).

- If there is a power path from n_1 to n_2, then there is a directed edge e where $\text{init}(e) = n_1$ and $\text{ter}(e) = n_2$.

- The weight of an edge is an ordered n-tuple [131] of positive or zero values to capture the pertinent parameters like voltage, current, power, energy, or charge. As an example, an interesting ordered n-tuple weight for an edge is the ordered pair of (voltage, current).

- The ordered n-tuple weight of the edge e is annotated by:

$$W(e) = \left(w_1(e), w_2(e), ..., w_n(e)\right). \tag{A.1}$$

- For each element of the ordered n-tuple weights, a *weighted adjacency matrix* $A_{w_m} = (a_{ij})_{k\times k}$ is defined as follows:

$$a_{ij} = \begin{cases} w_m(e) & \text{if } \exists e : \text{init}(e) = n_i \text{ and } \text{ter}(e) = n_j, \\ 0 & \text{otherwise,} \end{cases} \tag{A.2}$$

  where $m \in \{1, 2, ..., n\}$ and k is the number of nodes.

- A loop does not represent a power path. Loops capture parameters like the remaining charge of a battery.

- Losses can be modeled as a directed edge from the loss source, like a converter or a battery, to a virtual load.

A.3 Energy Network Examples

Using the notion of the energy networks introduced above, some of the basic power processing architectures are modeled as in Fig. A.1 and Fig. A.2. It should be noted that the concept of the energy networks introduced here is still evolving and yet to be completed. Note that in Fig. 1.1(a), Fig. 1.1(c), Fig. 1.1(e), and Fig. 1.1(g), all the converters are bidirectional isolated dc-cd power converters. A dual active bridge [132] is a common realization of such converters. In Fig. A.2, the switched-capacitor structure of diffusion charge redistribution (DCR) and differential diffusion charge redistribution (dDCR) solar PV modules is modeled as a multiple-input multiple-output dc-dc power converter. The virtual-bus structure in Fig. 1.1(g) is a partial power processing architecture being used for wide applications like in BESSs [132] and solar PV systems [18]. As shown in Fig. A.1 and Fig. A.2, the interconnections of the nodes within the graphs do not replicate the actual electrical interconnections. For example, a one-to-one bidirectional converter has been modeled as a node with two inputs and one output to express the genuine power paths from the sources to the loads. In other words, in the investigated energy networks, the electrical circuits are abstracted into power flows among the nodes.

One of the basic functionalities of the energy network investigated here is its representation capability for analysis of the partial power processing architectures. One can distinctly observe that the energy network in Fig. 1.1(f) processes all the power from the batteries. Similarly, it can be seen that in the energy network of Fig. 1.2(b), all the power from PV_2 is processed through U_1, while in Fig. 1.2(d), there is a direct path from PV_2 to L_2, making the differential power processing doable. Additionally, it can be noticed that the energy network in Fig. 1.1(h) is reducible to an energy network in Fig. 1.1(b). Furthermore, the

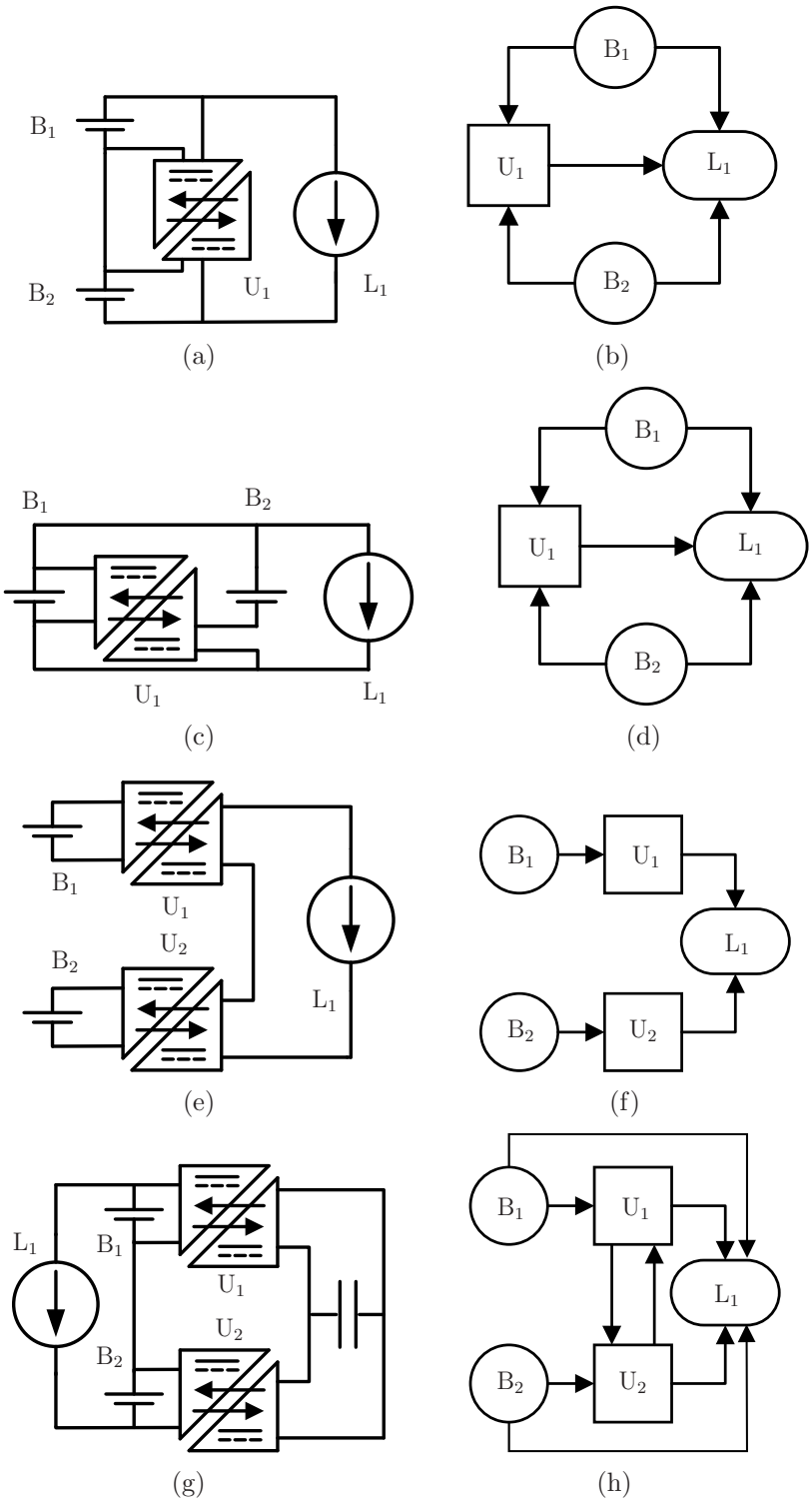


Figure A.1: Circuits and corresponding energy networks for BESSs: (a),(b) series partial power processing, (c),(d) parallel partial power processing, (e),(f) full power processing, and (g),(h) virtual-bus.

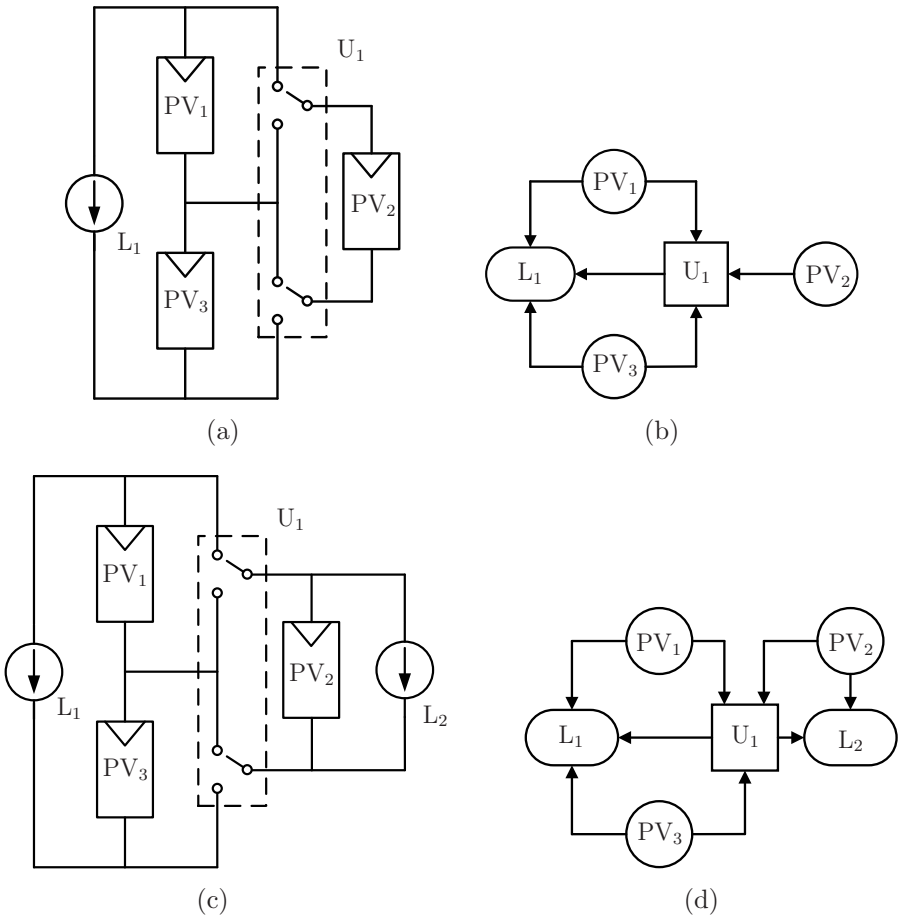


Figure A.2: Circuits and corresponding energy networks for DCR and dDCR solar PV structures: (a),(b) DCR structure, and (c),(d) dDCR structure.

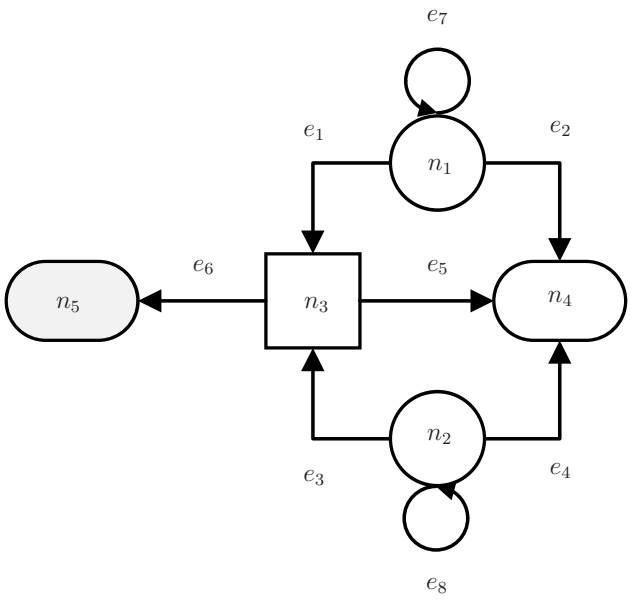


Figure A.3: Energy network for a simple series LS-HiPPP.

energy networks in Fig. 1.1(b) and Fig. 1.1(d) are isomorphic. So, one can expect that the optimization problems for such networks are analogous.

A.3.1 Energy Network for Series Lite-Sparse Hierarchical Partial Power Processing Architecture

As an example, the energy network of a simple series lite-sparse hierarchical partial power processing (LS-HiPPP) architecture (Fig. A.3) is further discussed in detail. This graph $G = (N, E)$ has 5 nodes and 8 directed edges (including 2 loops). Based on the definitions discussed before, for G, we have:

- $N = \{n_1, n_2, n_3, n_4, n_5\}$,
- $E = \big\{\{n_1, n_3\}, \{n_1, n_4\}, \{n_2, n_3\}, \{n_2, n_4\}, \{n_3, n_4\}, \{n_3, n_5\}, \{n_1, n_1\}, \{n_2, n_2\}\big\}$,
- Map 1 for the initial nodes of the edges: $\text{init}(e_1) = n_1$, $\text{init}(e_2) = n_1$, $\text{init}(e_3) = n_2$, $\text{init}(e_4) = n_2$, $\text{init}(e_5) = n_3$, $\text{init}(e_6) = n_3$, $\text{init}(e_7) = n_1$, $\text{init}(e_8) = n_2$,
- Map 2 for the terminal nodes of the edges: $\text{ter}(e_1) = n_3$, $\text{ter}(e_2) = n_4$, $\text{ter}(e_3) = n_3$, $\text{ter}(e_4) = n_4$, $\text{ter}(e_5) = n_4$, $\text{ter}(e_6) = n_5$, $\text{ter}(e_7) = n_1$, $\text{ter}(e_8) = n_2$,

- $W(e_1) = (v_1, i_1, 0)$,
- $W(e_2) = (v_1, i_2, 0)$,
- $W(e_3) = (v_2, i_3, 0)$,
- $W(e_4) = (v_2, i_4, 0)$,
- $W(e_5) = \left(v_1 + v_2, \frac{v_1}{v_1+v_2} i_1 + \frac{v_2}{v_1+v_2} i_3, 0\right)$,
- $W(e_6) = (v_1 + v_2, i_5, 0)$,
- $W(e_7) = (0, 0, c_1)$,
- $W(e_8) = (0, 0, c_2)$,
- $A_{w_1} = A_v = \begin{bmatrix} 0 & 0 & v_1 & v_1 & 0 \\ 0 & 0 & v_2 & v_2 & 0 \\ 0 & 0 & 0 & v_1 + v_2 & v_1 + v_2 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$,
- $A_{w_2} = A_i = \begin{bmatrix} 0 & 0 & i_1 & i_2 & 0 \\ 0 & 0 & i_3 & i_4 & 0 \\ 0 & 0 & 0 & \frac{v_1}{v_1+v_2} i_1 + \frac{v_2}{v_1+v_2} i_3 & i_5 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$,
- $A_{w_3} = A_c = \begin{bmatrix} c_1 & 0 & 0 & 0 & 0 \\ 0 & c_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$.

Note that the intuitive way of defining weights for this network is assigning battery voltages (v_1 and v_2) to the power paths from the corresponding batteries towards loads or converters. Additionally, the voltage contribution of the converter to the load is the summation of the voltage batteries, i.e., $v_1 + v_2$, which leads to a weighted current contribution, i.e., $\frac{v_1}{v_1+v_2} i_1 + \frac{v_2}{v_1+v_2} i_3$. In this graph, e_7 and e_8 capture the remaining charge of n_1 and n_2, i.e., c_1 and c_2, respectively. Also, e_6 going from n_3 to the virtual load n_5 models the loss of n_3. As mentioned earlier, the concept of the energy networks introduced here is still evolving and is yet to be completed.

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