Narrowband RF Localization Circuits and Systems

by

Chien-Wei Tseng

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Doctoral Committee:

Professor David Blaauw, Chair
Associate Professor Hun-Seok Kim
Associate Professor Alanson Sample
Professor Dennis Sylvester

Chien-Wei Tseng

cwtseng@umich.edu

ORCID iD: 0009-0007-4280-2676

To my family and Kuan-Ting Lai.

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ABSTRACT

This dissertation focuses on the design and implementation of wireless communication circuits and systems for IoT applications, aiming to build a miniaturized IoT device with low power consumption and advanced features. Several challenges need to be addressed. First, the increasing number of devices operating in the limited radio spectrum resources drives the need for improving out-of-band filtering to eliminate interference. Second, the limited battery capacity and driving power restrict the functionality of IoT devices, necessitating new circuits and systems co-design to enhance performance. Third, the power-hungry and bulky off-chip components challenge the system's power and form-factor constraints. This dissertation proposes three works in circuits and systems, especially localization systems, to address those issues. The first work introduces a highly reconfigurable analog-FIR filter with a sharp transition and high rejection to address the IoT device spectrum congestion issue. The second work proposes a long-range narrowband RF localization system featuring a PLL-less frequency hopping receiver front-end with a novel signal processing technique, enabling an unprecedented long-range localization service with a small form factor of the tag device. Lastly, a more comprehensive version of a PLL-less and crystal-less frequency hopping receiver is proposed. We introduce a novel signal processing technique to resolve the unstable sampling clock issue, enabling a compact and fully integrated receiver. The three works present in this dissertation provide solutions to IoT challenges and broaden IoT applications.

CHAPTER I

Introduction

The Internet of Things (IoT) has been advocated for decades with a long history. It refers to a network of connected devices and technology that facilitates communication and provides functionality between devices and the cloud or devices themselves. This concept has been pervasive across industries and academia, and we are witnessing many areas dedicated to driving the service and accelerating the technology, thereby contributing to the ever-growing worldwide market. Forecasting by the market analysis report [1], the worldwide total revenue will reach 600 billion US dollars by 2030, tripling the revenue every ten years. The revenue and the number of IoT-connected devices are forecast to reach 125 billion in 2030 [2]. Moreover, there has been a significant increase in the demand for edge AI, and it is expected to be a significant factor in the exponential growth of the IoT market [3] (Figure 1.1).

The rapidly growing market also enables numerous application services, holding the potential to impact people's daily lives profoundly. Edge AI uses artificial intelligence (AI) technologies at the edge of the networks, enabling smarter, faster, and more efficient systems and devices that can respond in real-time without constant cloud connectivity. Augmented and virtual reality (AR/VR) devices with low latency and reliable links provide broad benefits across various domains, ranging from industrial and manufacturing applications to entertainment and social services.

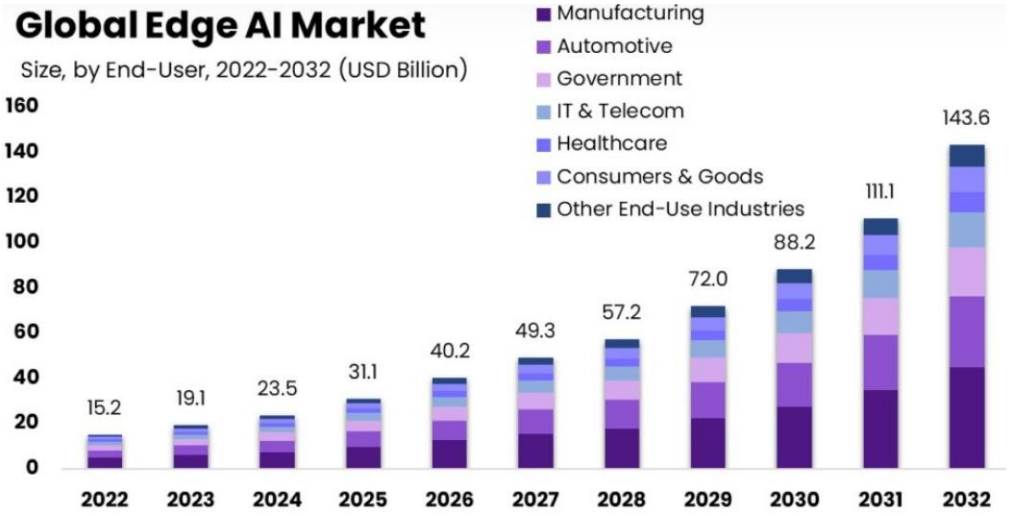


Figure 1.1: Global edge AI revenue; source: market.us, Edege AI Market, Jan 2024

The ability to monitor assets and individuals across vast areas, including applications like tracking people's movement and tracking goods in transit, significantly enhances manufacturing efficiency. Smart agriculture, driven by connected sensor technologies, allows for the real-time monitoring of moisture levels and chemical compositions and the automation of feeding and watering schedules. For smart cities, the widespread deployment of sensors can be harnessed for public safety infrastructure and energy/utilities monitoring. Autonomous vehicles equipped with intelligent sensors offer various advantages, from enhancing roadway safety to providing collision warnings and optimizing vehicle operations.

Entering the 5G era, the intelligent wireless edge is essential for the IoT expansion. 5G New Radio (NR) begins with enhanced mobile broadband (eMBB) and ultra-reliable, low-latency communication (URLLC). Still, it has scaled down to support broader IoT devices and services. In 3GPP Release 13, it introduced narrowband Internet of Things (NB-IoT) and enhanced machine-type communication (eMTC) to deliver a scalable, efficient, and cost-effective platform for connecting wide-range low power devices.

In addition to advancing wireless systems and infrastructure, expanding IoT services also necessitates progress in the evolution of end devices. These end devices are envisioned to be characterized by a small form factor, low power consumption, low cost, and computational capability. Over several decades, various technologies have been developed to unlock the potential of IoT devices and services.

One of the fundamental technologies driving device miniaturization is fully integrated systems in the silicon process, resulting in benefits such as smaller die areas, lower production costs, and low power consumption. However, recent process technology scaling tends to favor high-performance computing (HPC), which can lead to higher costs per wafer/die and increased device leakage. Therefore, the advantages of advanced process nodes are diminishing. Another critical factor is battery technology. The trade-off between energy density, power density, and volume [4] [5] directly impacts IoT devices' lifetime, functionality, and physical size. Additionally, the potential for IoT devices to operate without batteries, thereby achieving independence and sustainability, is a promising approach. Techniques such as energy harvesting [6], backscattering [7], or utilizing photovoltaic cells can enable battery-less operation. However, the increasing demands for edge computing capabilities necessitate a breakthrough in power delivery methods.

Therefore, ongoing efforts in circuit- and system-level techniques are pivotal to realizing IoT devices that are both small in size, low in power consumption, and highly efficient. These efforts are poised to usher in a new era of the IoT ecosystem, characterized by millimeter-scale devices and a proliferation of trillions of connected devices.

This chapter introduces a brief history of the end device evolution focusing on the wireless sensor node and describes challenges to power the IoT application.

1.1 Smart Sensing Devices and Services

1.1.1 Millimeter-scale Sensing Devices

Millimeter-scale computing devices concept was introduced by researchers at UC Berkeley [8]. They pioneered the creation of these devices, also known as 'smart dust' or 'smart motes,' which were remarkably compact (5.8mm x 5.8mm x 2.4mm) and cost-effective. Furthermore, it can establish the communication link and simulate basic functionality with a lower power consumption of 17 uW. Since then, such miniaturized and functional systems have shed light on the potential for large-scale wireless sensor networks comprising large quantities of small devices. Subsequently, several miniaturizations of wireless sensor nodes emerged, including the Eco node [9] proposed by researchers at UC Irvine and small autonomous network devices (SAND) [10] proposed by Philips Research. Both the Eco and SAND systems relied on commercial off-the-shelf components, which limits the power efficiency and lifespan of small devices. In addition to focusing on miniaturization, research attention also shifted toward low-power circuit techniques, such as low-leakage design, subthreshold operations, and battery-less or energy-harvesting circuits. Michigan Micro-Mote (M^3) [11], a millimeter-scale sensing platform was proposed by researchers at the University of Michigan. This innovative platform adopted a modular design approach, akin to the chiplet concept, with various functional layers stacked together, ushering in a new era for millimeter-scale sensing platforms [12][13][14][15]. The modular design featured a customizable application layer with a universal protocol for communication between these layers.

1.1.2 Sensing Device For Location-as-a-service

With the continuous expansion of IoT applications and efforts to enhance device functionality, these devices are becoming increasingly intelligent. They can now

provide communication services and their location information to the host. Applications such as warehouse asset tracking, smart home devices, and livestock tracking have gained popularity and experienced rapid growth. Various trade-offs must be considered; the optimal solution often hinges on the specific use case.

Location services have a rich history with many variations. Starting from satellite-based navigation, the Global Positioning System (GPS) is the most widely used system for outdoor localization. The technique compares the time difference between signals transmitted by the transmitters from satellites with signals received by the GPS receiver on Earth. Following GPS, several similar satellite positioning services, such as Galileo, Glonass, or Beidou, have emerged, collectively known as the Global Navigation Satellite System (GNSS). However, GPS/GNSS systems require line-of-sight (LOS) between satellites and devices.

Location services saw a resurgence with the rise of the smartphone and the introduction of cellular broadband services. While the GPS service can seamlessly integrate into smartphones, providing users with accurate outdoor positioning, indoor is where the GPS system struggles to provide precise precision or fails. This gap in indoor location precision necessitates the development of a new type of location service known as indoor positioning systems. Numerous technologies have been developed for decades for Cellular/WiFi/Bluetooth/Ultra-Wide Band (UWB)/ZigBee, with popular techniques including time-of-arrival (ToA), angle-of-arrival (AoA), received signal strength indicator (RSSI). The performance overview and comparison of different technologies [16] [17] is shown in Figure 1.2. However, as we enter the IoT era, battery-operated IoT devices require more stringent power constraints with a compact form factor. This challenges conventional positioning systems due to their power-hungry transceivers and strict wireless system requirements.

Technology	Technique	Method	Accuracy (m)	Cost	Coverage	Pros	Cons
Satellite	Trilateration	TOA TDOA	3–5		Floor level	Low power consumption	
Inertial	Dead Reckoning	–	2	Low	Floor level	Cheap	Accumulative errors
Magnetic Based	Trilateration Fingerprinting	–	2	Low	Floor level	Cheap	Requires mapping
Ultrasonic Based	Trilateration	TOA TDOA	0.01–1	Medium–High	Room level	Good accuracy No effect of multipath	Interference Cost for hardware
Acoustic	Trilateration	TOA	meters	Low	Room level	Cheap	Poor accuracy
Infrared	Proximity Trilateration	TOA	1–2	Medium	Room level (few meters)	Cheap No effect of multipath Low power consumption	Sunlight interference Short-range Cost for hardware
Visible light	Angulation	AOA	0.1	Medium	Floor level	No interfering	Expensive construction
Wi-Fi	Proximity	AP ID	10 (proximity)	Low	Floor level (around 35)	Good accuracy	RF interference with devices operating at 2.4 GHz
	Trilateration	RSS	1–5			Low cost	
	Angulation	TOA				Wi-Fi signals can penetrate walls/	Fingerprinting requires a huge effort
	Fingerprinting	TDOA				No need for additional infrastructure	
	RSS-Propagation model	AOA					
ZigBee	Proximity	AP ID	3–5	Medium	Floor level	Low cost	Requires special equipment
	Trilateration	RSS				Low power consumption	
	Fingerprinting						
	RSS-Propagation model						
Bluetooth	Proximity	AP ID	2–5	Low-Medium	around 10	Good accuracy	RF interference
	Trilateration	RSS				No need for additional infrastructure	Limited coverage and mobility
	Fingerprinting	TOA				Low power consumption	
UWB	Trilateration	TOA	0.01–1	High	Few meters	Accurate	Expensive
	Angulation	TDOA					Coverage is limited
		RSS					Performance degrades in NLOS
		AOA					
RFID	Proximity	AP ID	1–5	Low	Room level	Cheap	Low accuracy
	Trilateration	RSS				Real-time localization	Response time is high
	Fingerprinting						
	RSS-Propagation model						
FM	Fingerprinting	RSS	2–4	Low	100 km	Low sensitivity to objects	Vast change of signal over a small distance
Cellular network	Fingerprinting	RSS	2.5–25	Low	80 km	Networks available all over areas	Low accuracy
	Proximity	TOA					
	Trilateration						

Figure 1.2: Localization technologies performance overview

1.2 Next Generation IoT Challenges

IoT applications have opened the door to many new possibilities. They have captured researchers' attention, leading them to make devices small, compatible, low power, and highly integrated. In this dissertation, we focus on addressing the challenges of IoT end devices and exploring unprecedented applications of wireless sensors in long-range localization services.

1.2.1 Available Bandwidth and Interference

The radio spectrum is a finite resource shared with the entire world. Enabling billions of connected devices to share the limited frequency band makes the already crowded spectrum even worse. Fortunately, emerging IoT technologies in networking have found efficient ways to use the bandwidth. NB-IoT or eMTC, for example, have developed ways to allocate the recourse to IoT devices. However, thousands of devices usually appear nearby and use similar frequency bands, creating significant interference and thus degrading the signal-to-noise ratio (SNR). As the number of devices keeps growing, interference eventually dominates the validity of IoT device usage, exposing challenges to the growing number of devices.

1.2.2 Limited Battery Power and Small Form Factor

While most devices aim to be compact and self-sustaining, limitations in silicon physics and the increasing demand for functionality make using batteries unavoidable. As illustrated in Figure 1.3 [5], the battery's size and capacity restrict the system form factor, using scenario, and how it can be installed. Moreover, a significant portion of the device lifespan is spent in idle mode, awaiting the next trigger event. This idle time poses a considerable challenge in terms of leakage considerations.

In wireless sensor nodes, the power-hungry and large-size components are typically the crystal oscillator and high-frequency clock generation circuits. These components

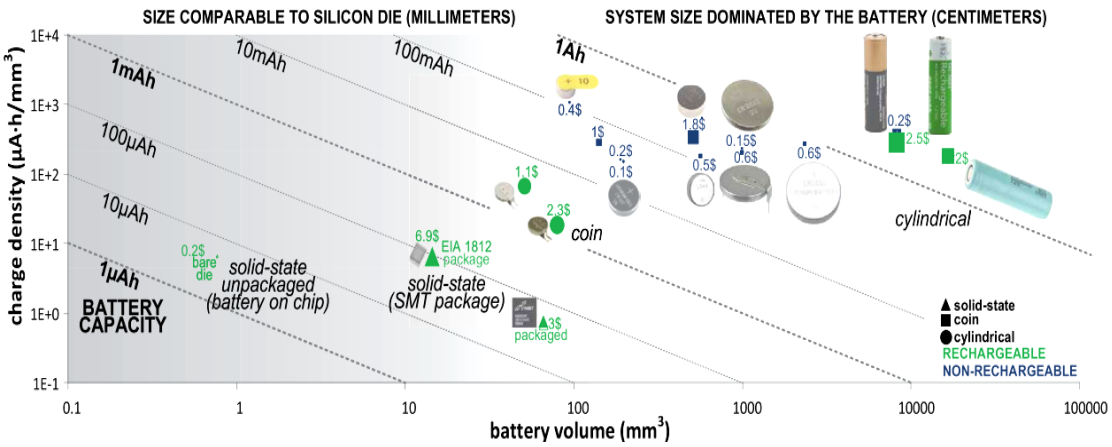


Figure 1.3: Battery for self-powered IoT systems

are critical for wireless communication since accurate data exchange depends on precise frequency, phase, and timing alignment. Nevertheless, there are instances [18] [19] [20] to remove them to minimize the power consumption. However, it can result in unstable transmitted signals with large frequency and phase drift, posing challenges for detection, synchronization, and demodulation on the receiver side.

Reducing power consumption can also be minimized by reducing tasks on edge devices. As a result, the system is forced to employ low-complexity algorithms on IoT devices and shift the heavy workloads to the gateway [18] [19] [20]. Hence, the collaboration between IoT devices and the gateway becomes crucial.

1.2.3 Long-Range Location-based Service Challenges

Asset tracking is one of the fast-growing IoT markets. It requires most connected devices to be location-aware. Such tracking service demands even long-range operations for emerging applications like autonomous micro-robots navigating large warehouse or factory spaces. Achieving long-distance positioning relies heavily on radio frequency circuit technologies and network infrastructure advancements. For example, while conventional GPS systems offer long-range positioning, they fail to operate in indoor environments and require a power-hungry receiver, impractical to the IoT

device. Alternative technologies such as UWB/WiFi/Bluetooth-based technologies provide indoor positioning but suffer from relatively high power consumption, limited ranging distances (typically $\leq$ 100m [21]), and integration challenges with external crystal oscillators that do not align with the form factor requirements of mm-scale IoT systems. Radio-frequency identification (RFID) is another form of asset tracking characterized by low power consumption, but the range distance is typically short. Clearly, there is a demand for new solutions for IoT devices providing long-range location service.

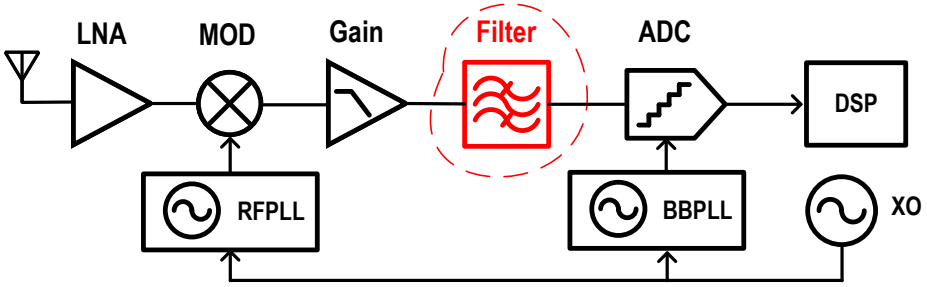
1.3 Dissertation Outline

This dissertation presents three works that contribute to resolving different challenges described in Section 1.2. These works focus on circuit and system design solutions to address challenges.

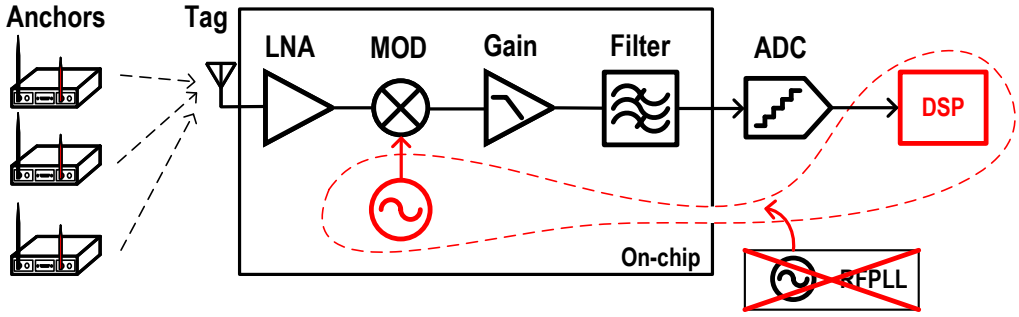
In Chapter II, we propose a novel highly reconfigurable charge-domain analog-FIR (AFIR) filter for high channel-selectivity receivers. This architecture demonstrates excellent power scaling with reconfigurability to different bandwidths and desired stopband rejection. We fabricated a chip in 28nm CMOS, showing the filter achieving -70 dB stopband rejection with a sharp transition and low power consumption of 0.356 mW.

In Chapter III, we propose a narrowband long-range localization system with a low-power tag receiver. The system utilizes the narrowband frequency hopping mechanism to traverse the available bandwidth and localize the tag. The localization system allows for a simplified receiver front-end design without the conventional PLL, resulting in an overall low-cost and low-power system. Instead, it introduces novel digital-assisted signal processing techniques to resolve system impairments. We fabricated an ASIC tag chip using a 55nm CMOS process, demonstrating the feasibility of the proposed signal-processing technique. Ultimately, we achieved a long-range,

- **Chapter II: A Reconfigurable Analog FIR Filter Achieving -70dB Rejection With Sharp Transition For Narrowband Receivers**



- **Chapter III: A Long Range Narrowband RF Localization System With a PLL-Less Frequency-Hopping Receiver Frond-End**



- **Chapter IV: A Compact, PLL-Less, Crystal-Less Receiver with 10-bit ADC For Narrowband Localization System**

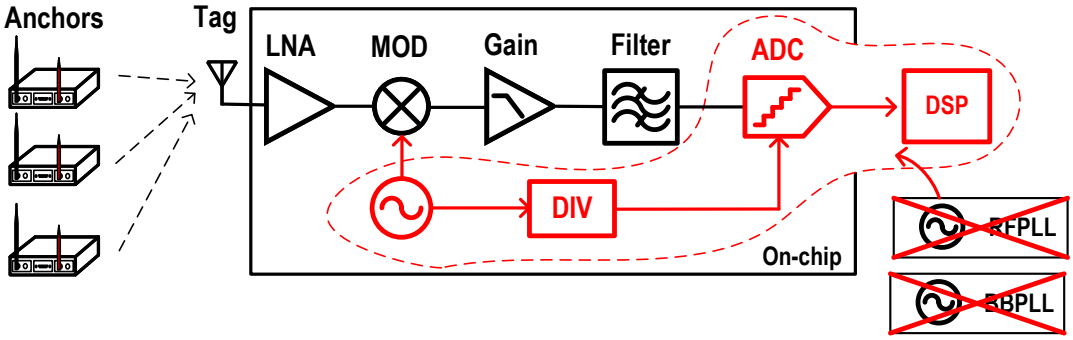


Figure 1.4: Three works address different challenges in this dissertation

low-power tag receiver RFFE for IoT applications.

In Chapter IV, following Chapter III, we aim to build a millimeter-scale fully-

integrated receiver, enabling the entire receiver to operate independently with a small form factor. Unlike conventional receivers using PLL for accurate sampling clock generation, the ADC sampling clock in the proposed system utilizes the divided-down clock from a free-running oscillator, simplifying the clock generation circuits. Accordingly, a novel signal processing technique is present to tackle the simplified receiver with a non-uniform sampling clock issue. The fully-integrated receiver demonstrates -115 dBm sensitivity with an 86 dB dynamic range.

Finally, Chapter V concludes the contributions of each work in this dissertation and discusses some future directions for the research.

CHAPTER II

A Reconfigurable Analog FIR Filter Achieving -70dB Rejection With Sharp Transition For Narrowband Receivers

2.1 Introduction

The need to adapt to various wireless standards has increased with the expansion of programmable receiver front-ends, making a reconfigurable baseband filter a critical component. For multi-channel narrowband applications, these systems require high channel selectivity, narrow bandwidth with tunability, low power consumption, and good linearity.

Figure 2.1 shows a typical zero-IF receiver chain. The baseband circuits commonly realize with one gain stage followed by a high selectivity low-pass filter (LPF). The gain stage is usually realized with a trans-impedance amplifier (TIA). It is commonly embedded with at least 1st-order low-pass filtering to filter out out-of-band (OOB) high-frequency signals. When the following LPF stage is chosen with an analog finite-impulse-response (AFIR), the gain stage is also responsible for filtering out the clock aliasing frequencies as they are only suppressed by the AFIR embedded sinc function, which is typically much lower than the average AFIR rejection. Therefore, the primary OOB frequency rejection contributing from AFIR is within the 1st aliasing clock

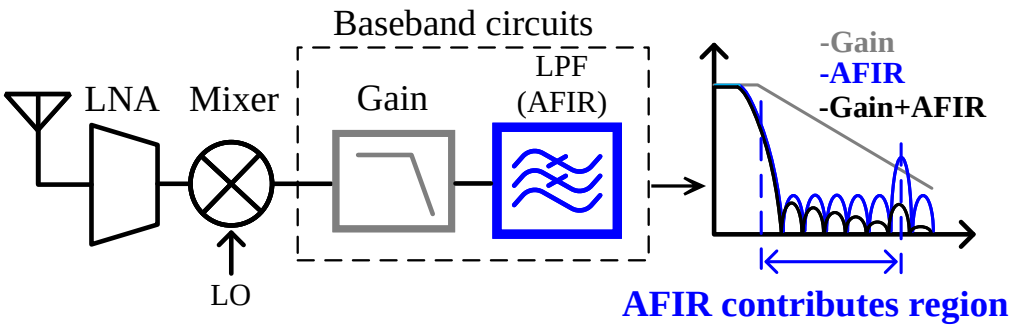


Figure 2.1: High channel selectivity receiver with analog FIR filter

frequency. Moreover, as the AFIR is typically located in the last stage of the receiver chain, the input-referred noise is much suppressed by the total receiver gain, making the noise requirement less critical. Therefore, AFIR focuses on providing maximal flexibility in terms of bandwidth, stopband rejection, and transition sharpness while maintaining good linearity.

This work has already been published in [22] [23]. A comprehensive explanation will be provided in this chapter.

2.2 Prior Works

Recently, several high selectivity LPF techniques have been proposed [24–32].

Techniques based on transconductance (Gm-C) and source-followers are described in [24] [25] [26], achieving low power consumption and the capability to implement high-order filter. However, they suffer from poor bandwidth tunability as it is typically fixed by the combination of transconductance and capacitance. [24] also utilizes a two-stage cascade to achieve a 5th-order filter.

Charge-sharing infinite-impulse-response (CS-IIR) techniques [27] [28] [29] are known for their ability to create high-order filters featuring a straightforward design and less affected by process, voltage, and temperature (PVT) variations. However,

these techniques cannot achieve the sharp transition needed for high-selectivity applications and demand a significant capacitance area to allow for adjustable bandwidth.

For FIR architecture, a full-rate cascaded-AFIR filter [30] achieves a sharper transition but at the cost of substantially high power consumption and incorporates a multi-stage design to facilitate a high-order filter. Filtering-by-aliasing [31] and low-power AFIR [32] are based on similar principles. They use either a time-varying resistor R(t) or transconductor G_m(t) to generate FIR coefficients and integrate the signals in the integrator. However, [31] requires significant power consumption, making it impractical for low-power applications. Additionally, varying the resistor value generates significant kick-back signals to the previous stage. [32] achieves low power consumption but suffers from substantial parasitic caps and finite-impedance charge leakage due to the large transconductor implemented as a digital-to-analog converter (DAC). Therefore, it requires complicated charge leakage calibration and implementation in the Fully Depleted Silicon On Insulator (FD-SOI) process.

Time-domain signal processing is historically prevalent in various fields, including phase-lock loop (PLL) [33], analog-to-digital converter (ADC) [34], and digital computing [35]. For filter design, the first filtering technique in which the transfer function coefficients are determined by timing is introduced in [36] [37]. A continuous-time filter version without sample/hold delay elements is proposed in [38]. Recently, a time-domain filter that embeds a bandpass function during the up-conversion for direct RF transmitter is proposed in [39] [40], featuring suppress OOB noise with high tunability and stopband attenuation. A similar approach for the receiver is proposed in [41], featuring high OOB blocker resilience. However, these techniques have not concentrated on developing high-resolution FIR filters that could further enhance OOB rejection.

2.3 Proposed Solutions

A novel compact, highly reconfigurable charge-domain AFIR for high channel selectivity receivers is presented. For FIR architecture, high rejection requires a high-resolution DAC to quantize the FIR coefficients. Therefore, we proposed a novel 11-bit charge-domain DAC, which is realized with the multiplication of the dual-path gm-DAC and the programmable time-DAC to quantize the FIR coefficients. It demonstrates excellent power scaling with reconfigurability to different bandwidths and desired stopband rejection. The proposed FIR filter realizes the coefficients in the charged domain with time-varying pulse width controlling the on-time transconductance and integrator capacitor. The charge-domain FIR principle is derived step-by-step in the following sections. This filter, manufactured in 28 nm CMOS, occupies an area of 0.05 mm^2. Its bandwidth can be reconfigured from 0.37 MHz to 4.6 MHz. It achieves -70 dB stopband rejection with a sharp transition (f_{-60dB}/f_{-3dB}=4.5) and a low power consumption of 0.356 mW in the CMOS process. Moreover, it can customize the configuration to different power, rejection, and clock frequencies with specific filter parameters.

2.4 Charge-Domain FIR Approximation

2.4.1 Operation Principle

The proposed AFIR filter structure leverages similar principles as in [31] [32]. Figure 2.2 illustrates the operation principle. The analog input signal X is first multiplied by the pre-determined discrete time-varying coefficient h and accumulates in the integrator. Then, the output Y samples the accumulated signal at every N sample, where N is the number of FIR coefficients. The coefficient h represents the FIR impulse response and is transmitted at the f_{clk} rate, while the output samples the accumulated signals at the down-sample f_{clk}/N rate. However, down-sampling

can lead to high-frequency signals aliasing to the in-band regions, resulting in the distortion of the in-band signals. This issue can be mitigated by ensuring the FIR response sufficiently suppresses the aliasing signals, making them much lower than the in-band signals before folding to the in-band regions. Therefore, this work focuses on implementing a high stopband and sharp transition FIR filter.

High OOB rejection requires a high-resolution 11-bit DAC for quantizing the FIR coefficients. We propose a *hybrid* gm- and time-domain DAC to realize a combined 11-bit charge-domain DAC resolution with a small area and low power consumption, as shown in Figure 2.3. The 11-bit resolution is divided into a fine-grain 4-bit DAC and a coarse 7-bit DAC using two paths (G_{m1} and G_{m2}) whose currents are summed together and integrated on the capacitor C_i with a total charge Q_{total}. Each path consists of a pulse-modulated G_m stage, where the coarse G_{m2} stage is 16 times larger than the fine-grain G_{m1} stage. Each stage is modulated by a pulse (T_1/ T_2 or h_1[n]t_u/ h_2[n]t_u). The pulse widths encode the n-th coefficient code h[n] where h[n] = h_1[n]+16*h_2[n]. T_1 and T_2 have maximum pulse widths of up to 15 and 127 time units (t_u) within one clock cycle T_{clk} for the 4-bit and 7-bit time-DAC, respectively. This dual-path implementation balances the gm/time dimensions, enabling higher bit-resolution implementation.

Figure 2.4 shows how the fine-grain and coarse DACs combine to form a single 11-bit DAC. During each clock period T_{clk}, both T_1 and T_2 fire their pre-programmed pulse widths. The charge on C_i is integrated across multiple clock cycles, representing the number of taps. Charge integration is performed during ϕ_1 ($\overline{\phi_1}$), and the resulting value is then sampled at the output during ϕ_2 ($\overline{\phi_2}$). The capacitor C_i is reset during ϕ_3 ($\overline{\phi_3}$). Time interleaving allows the output to be sampled continuously, avoiding dead time during the reset phase.

Figure 2.5 shows an example of simple 8-tap FIR coefficient mapping with the proposed charge-domain DAC. Each tap is implemented with discrete-time charge

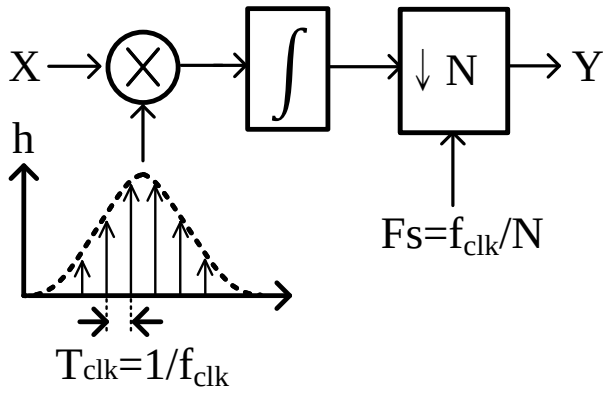


Figure 2.2: Energy-efficienct analog-FIR operation principle

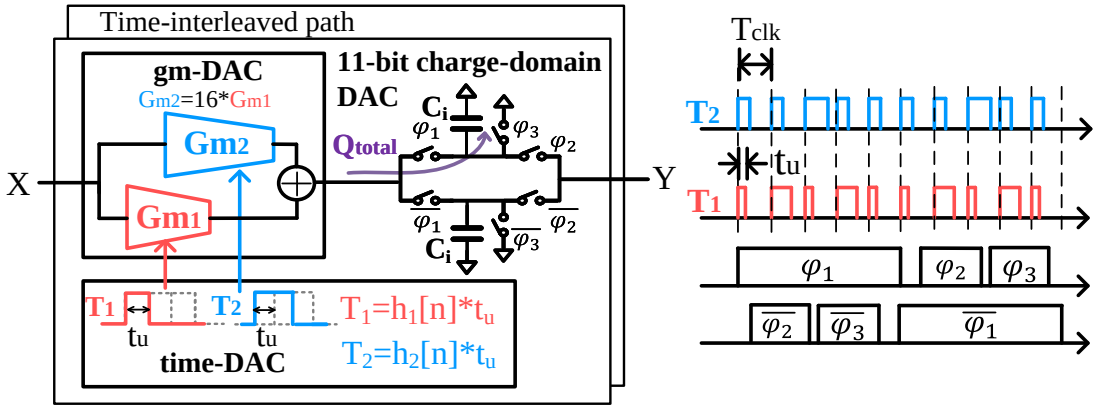


Figure 2.3: Proposed 11-bit charge-domain DAC architecture

accumulation through the two paths. Figure 2.5 illustrates the time-varying G_m value resulting from the differing on-times of the two G_m stages. The pulse-modulated approach yields a "return-to-zero" (RZ) transconductance waveform (solid-black RZ line in the bottom of Figure 2.5). The G_m value returns to zero at the end of every clock cycle when both G_m stages finish the clock cycle in their off states. This contrasts with the conventional approach where the transconductance strength is modulated but the G_m stage remains on continuously (dashed-black NRZ line in the bottom of Figure 2.5). The proposed approach activates the gm-DAC only when necessary, re-

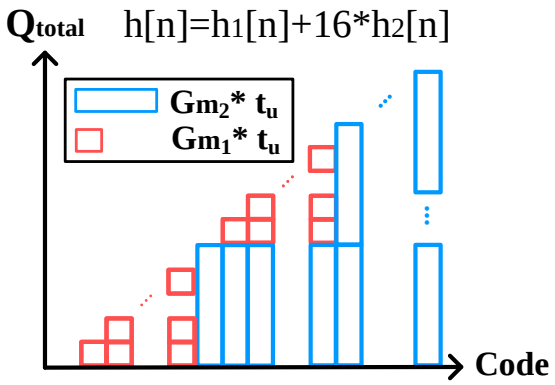


Figure 2.4: Q_{total} versus input digital code

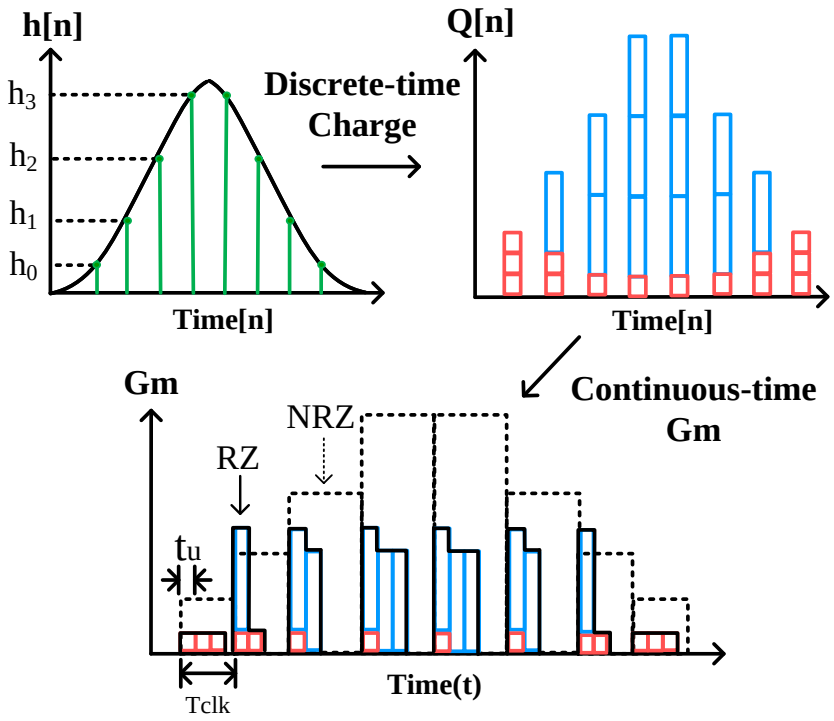


Figure 2.5: Example of 8-tap FIR coefficient mapping with the proposed DAC

sulting in power savings for the transconductor. Additionally, this approach mitigates excessive charge accumulation on the integrator, reducing the capacitor area.

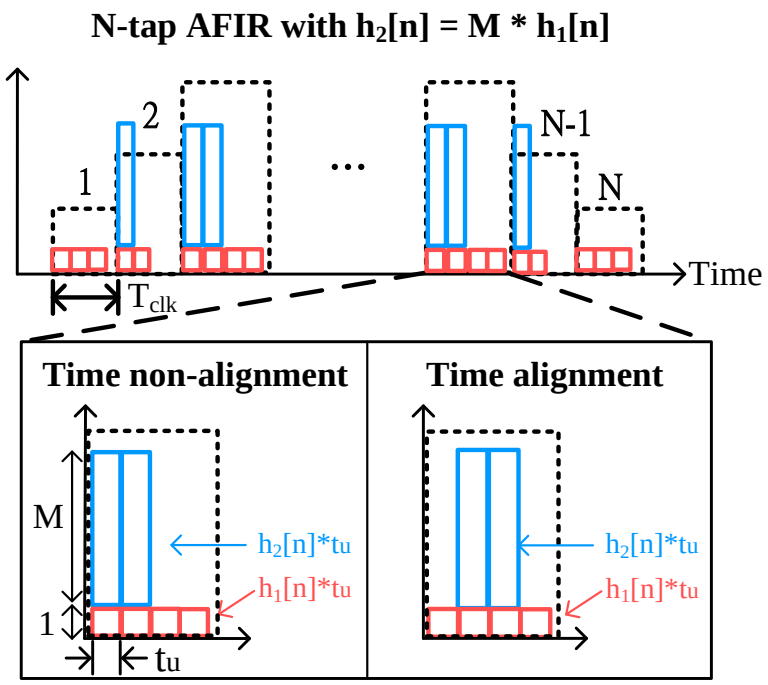


Figure 2.6: Time-domin illustration of the proposed AFIR

2.4.2 Transfer Function Analysis

Figure 2.6 presents the general time-domain illustration of the proposed AFIR. The filter is designed with N-tap FIR, each tap operating with T_{clk} period. Within each tap, two paths produce the accumulated charge stored on the C_i, as shown in blue and red. Each path operates with distinct pulse widths ($h_2[\mathrm{n}]t_u/h_1[\mathrm{n}]t_u$, where t_u is the unit time of the time-DAC) and transconductance ($M:1$ ratio). Therefore, if the input is $x(t)$, the total accumulated charge $y_n(t)$ at the n-th tap can be described as

$$\begin{aligned} y_n(t) = \frac{g_m}{C_i} x(t) \{ & M \left[u\left(t\right) - u\left(t - h_2[n]t_u\right) \right] \\ & + \left[u\left(t\right) - u\left(t - h_1[n]t_u\right) \right] \} \end{aligned} \tag{2.1}$$

The above equation is a straightforward implementation. In practice, there are

two physical implementation methods: time alignment and time non-alignment, as illustrated in Figure 2.6. Because the two paths operate with different lengths of pulse widths, capturing different segments of the signal results in a summation of different delays of the input signal. Therefore, ensuring timing alignment is crucial to equalize the delay of $h_1[n]$ and $h_2[n]$. However, considering hardware complexity, time non-alignment is preferred as it is much easier to implement. Both start times can be easily aligned with the rising edge of the clock, and the stop time can be adjusted to reflect the target pulse width. The time-domain transfer function of k-th sampled output $h_k(t)$ can be described as

$$\begin{aligned} h_k(t) = \frac{g_m}{C_i} \sum_{n=0}^{N-1} \{ & M \left[u\left(t - nT_{clk}\right) - u\left(t - nT_{clk} - h_2[n]t_u\right) \right] \\ & + \left[u\left(t - nT_{clk}\right) - u\left(t - nT_{clk} - h_1[n]t_u\right) \right] \end{aligned} \tag{2.2}$$

After obtaining the time-domain response, we can also derive the frequency response by converting it to the s-domain. The frequency-domain transfer function can be described as

$$\begin{aligned} H(s) &= \frac{g_m}{C_i} \sum_{n=0}^{N-1} \left\{ M \cdot e^{-nT_{clk}s} \left(\frac{1 - e^{-h_2[n]t_u s}}{s} \right) + e^{-nT_{clk}s} \left(\frac{1 - e^{-h_1[n]t_u s}}{s} \right) \right\} \\ &= \frac{g_m}{C_i} \sum_{n=0}^{N-1} \big\{ \big(M \cdot h_2[n]t_u \cdot \mathrm{sinc}(h_2[n]t_u f) \cdot e^{-h_2[n]t_u \cdot s} \\ &\quad + h_1[n]t_u \cdot \mathrm{sinc}(h_1[n]t_u f) \cdot e^{-h_1[n]t_u \cdot s} \big\} \cdot e^{-nT_{\mathrm{clk}} \cdot s} \end{aligned} \tag{2.3}$$

In summary, the general transfer function of the proposed charge-domain AFIR can be written as

$$\begin{aligned} H(f) = \frac{g_m}{C_i} \sum_{n=0}^{N-1} \big\{ & \big(M \cdot h_2[n]t_u \cdot \mathrm{sinc}(h_2[n]t_u f) \cdot e^{-h_2[n]t_u \cdot j2\pi f} \\ & + h_1[n]t_u \cdot \mathrm{sinc}(h_1[n]t_u f) \cdot e^{-h_1[n]t_u \cdot j2\pi f} \big\} \cdot e^{-nT_{\mathrm{clk}} \cdot j2\pi f} \end{aligned} \tag{2.4}$$

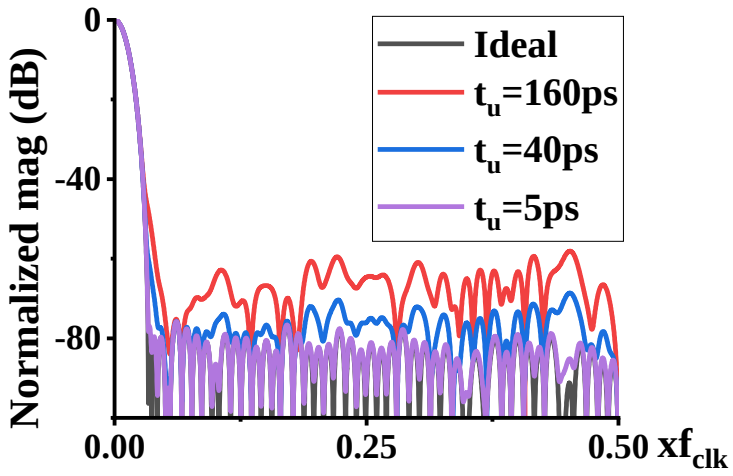


Figure 2.7: Simulation of frequency response with different t_u

where g_m is the transconductance of the fine-grain stage (G_{m1}), M is the ratio of G_{m2} to G_{m1}, and C_i is the integrator capacitance.

There are two major differences compared to the conventional FIR transfer function [42]. First, the sinc function contains the time-varying coefficients h_1[n] and h_2[n]. Second, there are two paths (G_{m2} and G_{m1}), each characterized by distinct complex values in the frequency domain. Improper handling of these two complex values may result in a non-ideal overall FIR frequency response.

However, if t_u is much shorter than T_{clk} ($t_u \ll T_{clk}$) and focuses on the low frequency, the sinc function can be simplified to

$$sinc(h_k[n]t_u f) \approx 1 \tag{2.5}$$

where h_k[n] is the coefficient of either h_1[n] or h_2[n]. Combining Equation 2.4 and Equation 2.5, the transfer function with a short t_u at low frequency can be approximated to

$$H(f) = \frac{g_m \cdot t_u}{C_i} \sum_{n=0}^{N-1} (M \cdot h_2[n] + h_1[n]))e^{-nT_{clk}s} \tag{2.6}$$

$$= \frac{g_m \cdot t_u}{C_i} \sum_{n=0}^{N-1} (h[n])e^{-nT_{clk}s} \tag{2.7}$$

The result is similar to the low-frequency approximation of conventional FIR response [42]. Applying different implementation methods (time alignment/ time non-alignment) would change the phase of the two complex values. Ideally, making two paths with equal phases would result in more accurate charge summation. However, implementing this in actual hardware requires additional timing controls of the pulses, increasing design complexity. Consequently, we accept such non-ideality and decrease the unit pulse width (t_u) to minimize the phase difference.

Figure 2.7 shows the simulation of the filter's frequency response of 96-tap/11-bit configuration with different lengths of t_u. As expected from the derivations in Equation 2.4 - 2.7, shortening t_u brings the filter response close to the ideal 11-bit quantization response (black line in Figure 2.7).

2.4.3 Noise Analysis

This section will analyze three primary noise sources: clock jitter, transconductance noise, and switch noise.

2.4.3.1 Clock Jitter

The proposed *hybrid* filter consists of two paths for accumulating charge over N clock cycles, where N represents the number of taps and T represents the clock period. Each path is modulated with a specific pulse width (h_1[n]t_u/ h_2[n]t_u) to control the on-time of transconductance (G_{m1}/ G_{m2}) and finally accumulates charge on the capacitor (C_i). While the filter integrates across multiple taps, the clock jitter disturbs the integration time of each cycle in each path. With the input $x(t)$ and the

k-th sampled output $y_k(t)$, where

$$y_k(t) = \frac{g_m}{C_i} \sum_{n=0}^{N-1} \int_{t+nT+t_{j,2,r}(t-nT)}^{t+nT+h_2[n]t_u+t_{j,2,f}(t-nT)} M \cdot x(\tau)\, d\tau \; + \int_{t+nT+t_{j,1,r}(t-nT)}^{t+nT+h_1[n]t_u+t_{j,1,f}(t-nT)} 1 \cdot x(\tau)\, d\tau \tag{2.8}$$

in which M represents the g_m ratio of G_{m2}/G_{m1}, $t_{j,2,r}$(t) and $t_{j,2,f}$(t) represent the rising/falling clock jitter of G_{m2} as a function of time, and $t_{j,1,r}$(t) and $t_{j,1,f}$(t) represent the rising/falling clock jitter of G_{m1} as a function of time. This integral can be approximated using Taylor's series expansion [43] to

$$\begin{aligned} y_k(t) \approx \frac{g_m}{C_i} \sum_{n=0}^{N-1} \{ & \\ & M\,[x(t)(u\,(t-nT) - u\,(t-nT-h_2[n]t_u)) - x(nT)t_{j,2,r}(nT) \\ & + x(nT+h_2[n]t_u)t_{j,2,f}(nT+h_1[n]t_u)] \\ & + [x(t)(u\,(t-nT) - u\,(t-nT-h_1[n]t_u)) - x(nT)t_{j,1,r}(nT) \\ & + x(nT+h_1[n]t_u)t_{j,1,f}(nT+h_1[n]t_u)]\} \end{aligned} \tag{2.9}$$

When operating with short t_u, as shown in Equation 2.5, and assuming the rising/falling time clock jitter are equal, the power spectral density (PDF) can be written as

$$\begin{aligned} S_{y_k}(f) = \frac{g_m^2}{C_i^2} \sum_{n=0}^{N-1} \{ & \left[(M \cdot h_2[n]t_u)^2 + (h_1[n]t_u)^2 \right] S_x(f) \\ & + 4(S_x(f) * S_{j,2,n}(f)) sin^2(\pi h_2[n]t_u f) + 4(S_x(f) * S_{j,1,n}(f)) sin^2(\pi h_1[n]t_u f) \} \end{aligned} \tag{2.10}$$

The input signal transfer function remains the same as the previous derivation result. The clock jitter will convolute with the input signal and accumulate over multiple taps. This convolution of the input signal and clock jitter is shaped by the sine

function. Given that t_u is a small number, it results in very small values.

2.4.3.2 Switch Noise

During the reset phase, the reset switch introduces a voltage noise of kT/C stored on the accumulation capacitor C_i. Following the reset, the sampling switch turns on, connecting the accumulation capacitor to the gm-DAC. In the proposed structure, we utilize a small number of g_m units to implement the gm-DAC. Therefore, the parasitics of gm-DAC are negligible compared to the accumulation capacitor, allowing us to neglect the charge-sharing effect. Since the kT/C noise is white and spreads over the output sampling clock F_s, the output-referred power spectral density can be written as

$$S_y(f) = \frac{kT}{C_i}\frac{1}{F_s} \tag{2.11}$$

2.4.3.3 Transconductance Noise

Transconductance generates white noise of $4\mathrm{kT}\gamma/g_m$ at the filter input. The filter integrates over multiple short time intervals from two paths: [0, h_1[n]t_u] for path-1, [0, h_2[n]t_u] for path-2, where n ranges from 0 to $N-1$, and N represents the number of taps. Despite some overlap in integration time between the two paths, they originate from distinct transconductance sources, each with high output impedance. This effectively isolates them as discrete events. The integration time is over time-limited signals, and the total integration time is shorter than the output sampling clock period, allowing for applying a general theorem described in [43]. According to this theorem, integrating the transfer function frequency response across an infinite frequency range is equivalent to integrating such time-limited signals. Consequently, the integration result is independent of frequency and remains a constant value, making the transconductance's output noise remain white noise.

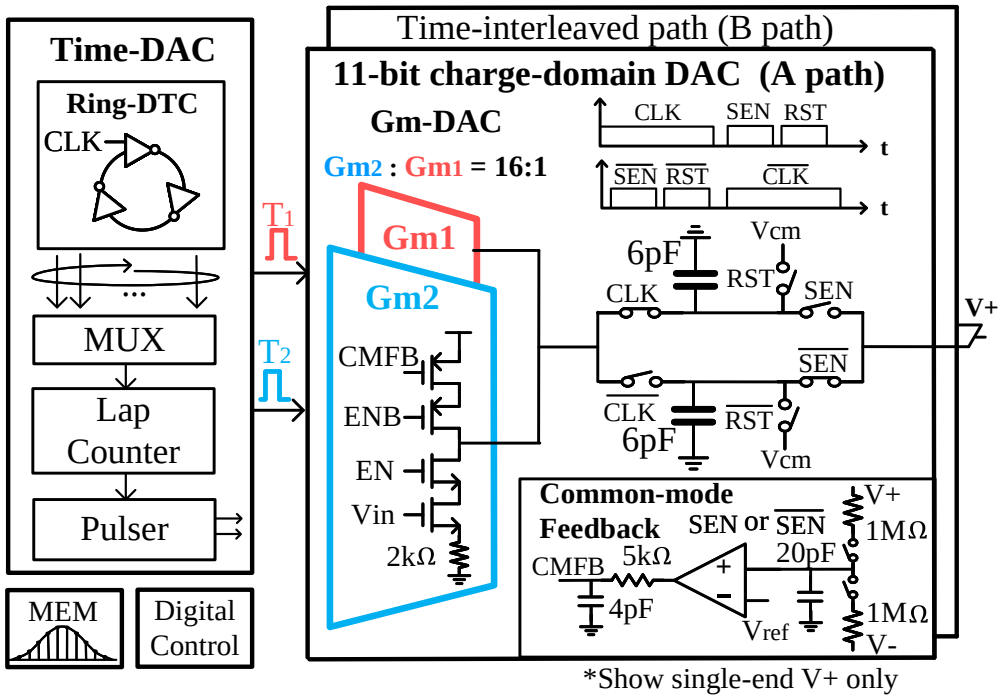


Figure 2.8: Proposed time-interleaved AFIR with a 11-bit charge-domain DAC

2.5 Circuit Implementation

2.5.1 Circuit Architecture Overview

Figure 2.8 shows the proposed AFIR filter circuit architecture. We implemented the 11-bit charge-domain DAC with a 7-bit time-DAC and a 4-bit gm-DAC. Dedicated common-mode feedback circuits are used to set individual paths' output common-mode to resolve the common-mode mismatch. The time-DAC is realized with a digital-to-time converter (DTC) structure to generate different pulse widths to control the on-time of the gm-DAC. An inverter-based DTC is used for its high linearity. The unit time delay is set to $\sim$ 60 ps to cover the gm-DAC rise and fall settling time ($\sim$20% of total pulse width). The unit time delay affects the DNL transition between G_{m1} and G_{m2}. Double-edge pulses at the rising/falling of the clock edge provide odd-order f_{clk} aliasing frequency cancellation. Two single-port SRAMs with 64 13-bit words are

utilized to store the weight coefficients. This can support a maximum of 128 taps, assuming taps are symmetrical. This is a valid assumption as this architecture suffers less charge leakage due to finite output impedance. The flexibility of FIR filtering is controlled by programming different numbers of FIR taps and bits via the digital controller.

2.5.2 Gm-DAC Implementation

Figure 2.8 shows the gm-DAC implementation. The gm-DAC physically uses only 16 (G_{m2}) + 1 (G_{m1}) g_m units to generate the current to the integration capacitors, significantly reducing parasitic caps and charge leakage due to finite output impedance. For G_{m2}, transistors M_{0-2} are 6.4u/120n, while M_3 is 10u/120n. To enhance the g_m device linearity, the resistor is placed on the source side of the common-source g_m device. The equal size of M_1 and M_2 balances the charge pushing from the P/NMOS switch parasitic caps to the output. Moreover, a differential structure is implemented to cancel out the residue charge pushing on both the V+ and V- sides. The ping-pong structure of the integration capacitors in the A path hides the reset delay and allows sampling at SEN ($\overline{SEN}$) duration. Hence, the sampling rate is already equal to the clock rate with one path, and with two paths (A/B path), it would double. Each path has dedicated common-mode feedback circuits to set individual path output common-mode voltage. The output common-mode signal is sampled with an around 10 kHz RC network (1MΩ/15pF). This sampled signal is then compared with the desired common-mode voltage to adjust the bias voltage of the PMOS.

2.5.3 Reconfigurable Time-DAC Implementation

Figure 2.9 shows the time-interleaved time-DAC implemented with a ring-DTC structure, including a 33-stage inverter ring, a 33-to-1 multiplexer (MUX), a 3-bit lap counter, and a pulser. The time-interleaved paths share the same ring-DTC to

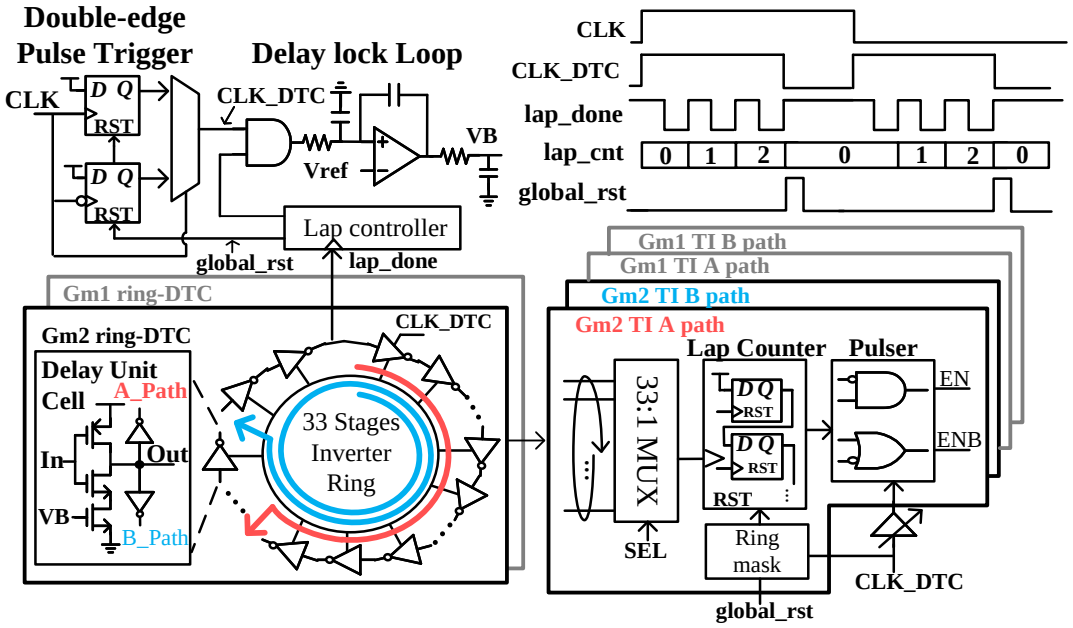


Figure 2.9: Implementation of the reconfigurable 7-bit time-DAC

minimize the path mismatch. The MUX selects an output inverter stage and sends the rising edge to the lap counter, which tracks the number of laps completed by the ring and outputs the delay edge. The final pulse is generated by the pulser using the time difference between the reference edge and the delay edge. The digital controller controls the MUX and the lap counter to generate different pulse widths representing the FIR coefficients. Another lap counter with a fixed lap setting determines the maximum laps of the time-DAC, allowing the programmability between 5 to 7 bits. The lap counter's output edge is sent to the delay-lock loop (DLL), which controls the total delay between the reference edge and the delay edge by adjusting the inverter's bias voltage (VB).

The time-DAC's unit pulse width is adjusted to ~60 ps to accommodate the rise and fall settling time of the g_m unit, and the DLL regulates the unit pulse width variation over PVT between 49 ps to 68 ps. The time-DAC achieves DNL/INL $\leq$ 0.15/0.3 LSB over 200 Monte Carlo simulations. Finally, double-edge pulses are

generated at the clock's rising and falling edge for odd-order aliasing clock frequency cancellation.

2.5.4 Mismatch and PVT Sensitivity Analysis

2.5.4.1 PVT Sensitivity

For the PVT variation, the ring-DTC (time-DAC) is robust against process and temperature variation since the DLL dynamically tracks the total delay and sets the unit delay of each stage. However, the time-DAC is sensitive to supply variation as the DLL's reference voltage is provided externally for a wide tuning range. Therefore, there is no reference voltage scaling with supply variation (the delay path's average DC value would scale with supply variation). The effect of supply variation would reflect on the variation of the unit pulse width of the time-DAC. The simulation of time-DAC unit pulse width over PVT is shown in Figure 2.10. The nominal unit pulse width is ∼60 ps, with process and temperate variation around +/-1.5 ps and supply variation around +/-8 ps.

Considering the unit pulse width varying +/-10 ps, the frequency response simulation is illustrated in Figure 2.11. The simulation result reveals that the unit pulse width variation over PVT slightly impacts the overall response (minimum stopband rejection variation ≤1.9dB). During the measurement, we fixed the supply voltage of the time-DAC to avoid supply variation and set the reference voltage externally for high tuning resolution.

2.5.4.2 Mismatch Sensitivity

We implemented the unit delay with an inverter-based delay cell for the time-DAC linearity. The delay increase is achieved by increasing the delay stages, ensuring high linearity. The 200 Monte Carlo simulations of "one" stage variation show a 1σ variation of 1.8 ps from the nominal 60 ps. Then, the 200 Monte Carlo simulation of

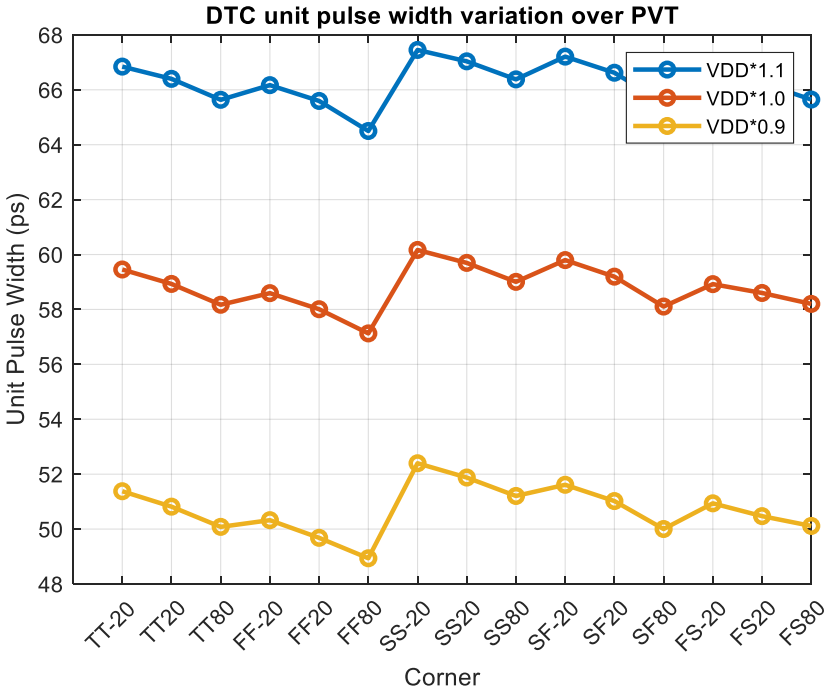


Figure 2.10: Simulation of ring-DTC unit pulse width variation over PVT

7-bit time-DAC's DNL/INL is shown in Figure 2.12.

The mismatch of the time-DAC and gm-DAC affects the filter transfer function. The OOB rejection is guaranteed to achieve worse case $\leq$ -65 dBc in simulation. In our design, the 7-bit time-DAC achieves DNL/INL $\leq$ 0.15/0.3 LSB. Additionally, the gm-DAC achieves 1σ $\sim$1.5% of its nominal value (G_{m2}) and 1σ $\sim$8% of its nominal value (G_{m1}). We run the Monte Carlo simulation of 87 frequency points within $1^{*}f_{clk}$ frequency, each point with 100 runs. The simulation result is shown in Figure 2.13. The black circle line is the median of 100 Monte Carlo runs of each frequency point. The worst case of OOB rejection is $\leq$-65 dBc.

During the measurement, we fine-tuned the FIR coefficients to achieve the out-of-band rejection $\leq$ -70 dBc. We measured the filter response and applied the MATLAB optimizer to adjust the FIR coefficients iteratively.

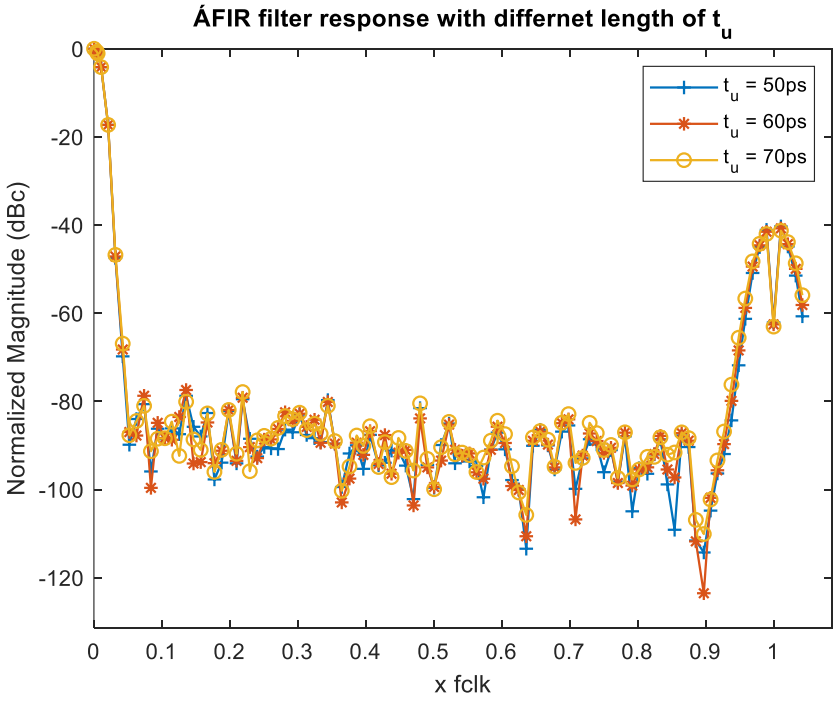


Figure 2.11: Simulation of AFIR filter response to unit pulse width variation sensitivity

2.5.4.3 Noise Analysis

The primary noise source in the time-DAC is from the ring-DTC. It is made up of 33-stage inverters connected in the ring style. The clock's rising/falling edge controls the start time, while the lap counter controls the stop time. The noise in each stage originates from a single inverter, and the noise variance can be described as [44]:

$$\sigma_{j,inv}^2 = \frac{4kT\gamma CV_{DD}}{2I^2(V_{DD} - V_t)} + \frac{kTC}{I^2} \tag{2.12}$$

where C is the inverter output capacitor, and I is the inverter current strength.

When it comes to a multi-stage and multi-lap ring-DTC, the noise generated by a single inverter will propagate and accumulate across multiple stages and laps. The

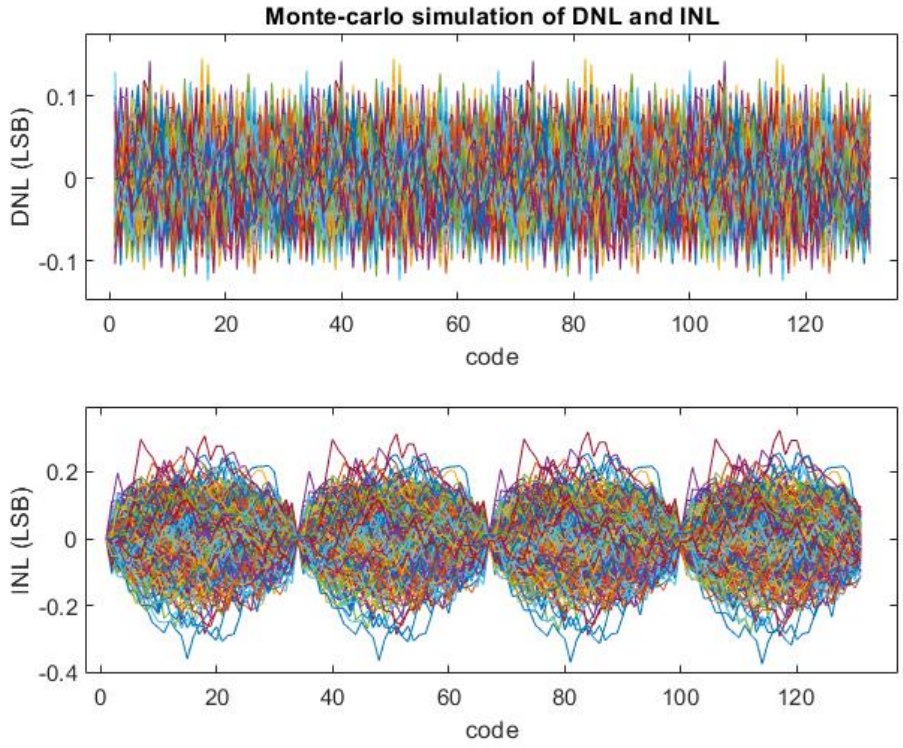


Figure 2.12: Simulation of ring-DTC DNL/INL

noise variance of ring-DTC can be written as

$$\sigma_j^2(n,l,N) = \begin{cases} n\sigma_{j,inv}^2 & \text{, l=0} \\ n\sigma_{j,inv}^2 + 2\sigma_{j,inv}^2(n - l\cdot N) & \text{, l=1} \\ n\sigma_{j,inv}^2 + 2\sigma_{j,inv}^2(n\cdot l - 0.5\cdot l\cdot N - 0.5\cdot l^2\cdot N) & \text{, l}\geq 2 \end{cases}$$

Here, n represents the input digital code, N denotes the total number of stages, and l denotes the number of completed laps. While N is a fixed value in physical implementation, l varies based on the input digital code n. The relationship between n and other parameters can be written as

$$l = \lfloor n/N \rfloor \tag{2.13}$$

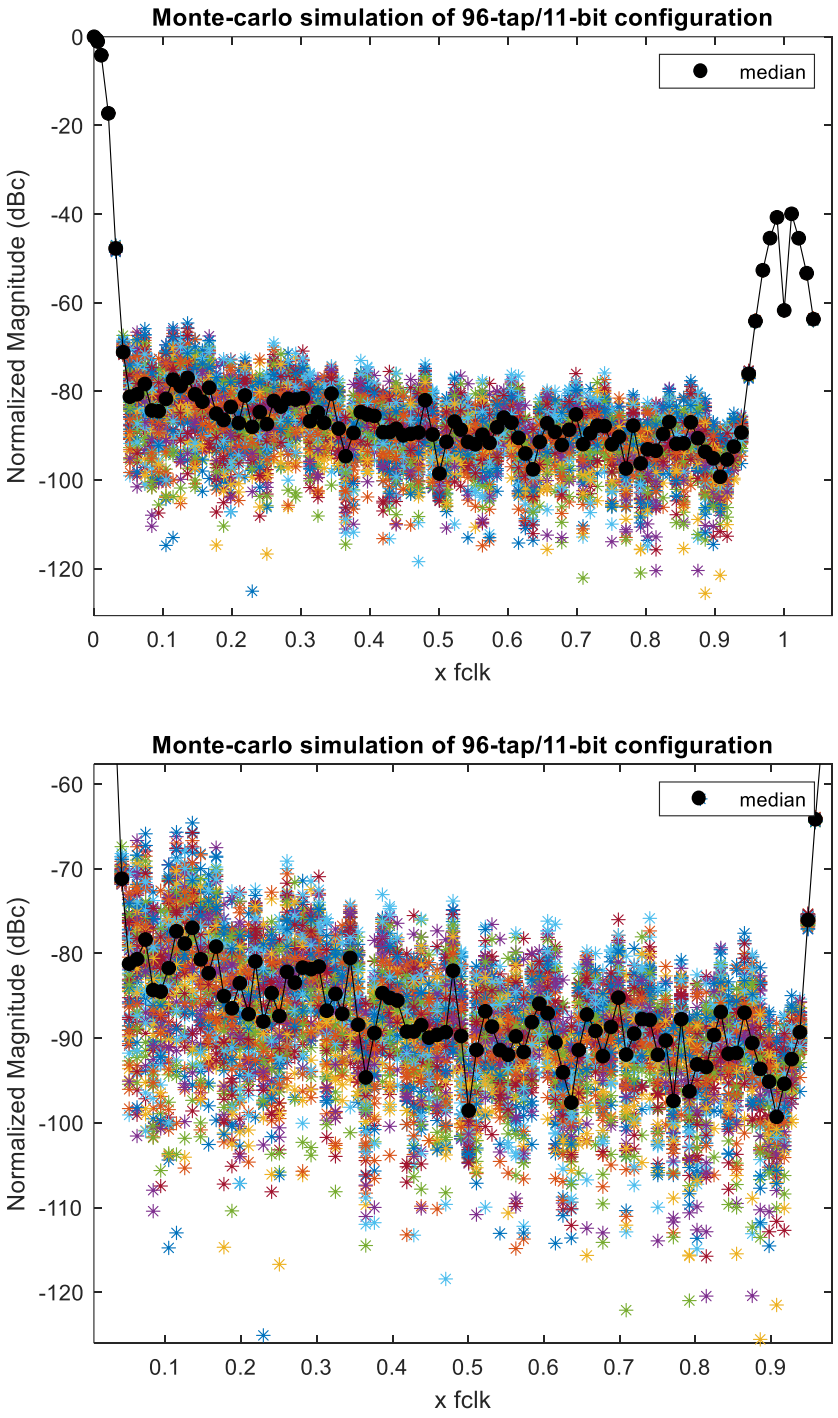


Figure 2.13: Simulation of AFIR mismatch sensitivity to time- and gm-DAC

With the number of stages N fixed, the noise variance becomes a function of n and l, increasing with large delays. Given the noise variance and assuming it to be white noise, the single-side-band power spectral density $L(f)$ can be derived as

$$L(f) = \sigma_j^2 \frac{f_0^2}{f^2} \tag{2.14}$$

where the σ_j^2 represents the noise variance, f_0 denotes the clock frequency, and f represents the frequency of interest.

In Section 2.4.3.1, we derive a noise analysis considering the clock jitter. Here, we take into account the clock jitter behavior of the ring-DTC. The noise in the rising/falling edge originates from different noise sources. The jitter on the rising edge is produced by the clock source. In contrast, the jitter on the falling edge results from the ring-DTC, which introduces more significant noise due to the accumulated jitter. Consequently, the time-domain response shown in Equation 2.9 can be simplified by excluding the rising edge clock jitter. The simplified expression is presented below

$$\begin{aligned} y(t) \approx \frac{g_m}{C_i} \sum_{n=0}^{N-1} \{ & M \left[x(t)(u\left(t - nT\right) - u\left(t - nT - h_2[n]t_u\right)) \right. \\ & + x(nT + h_2[n]t_u) t_{j,2,f}(nT + h_1[n]t_u)] \\ & + x(t)[u\left(t - nT\right) - u\left(t - nT - h_1[n]t_u\right)] \\ & \left. + x(nT + h_1[n]t_u) t_{j,1,f}(nT + h_1[n]t_u) \right\} \end{aligned} \tag{2.15}$$

The corresponding power spectral density can be expressed as:

$$\begin{aligned} S_y(f) = \frac{g_m^2}{C_i^2} \sum_{n=0}^{N-1} \{ & \left[(M \cdot h_2[n]t_u)^2 + (h_1[n]t_u)^2 \right] S_x(f) \\ & + S_x(f) * S_{j,2,n}(f) + S_x(f) * S_{j,1,n}(f) \} \end{aligned} \tag{2.16}$$

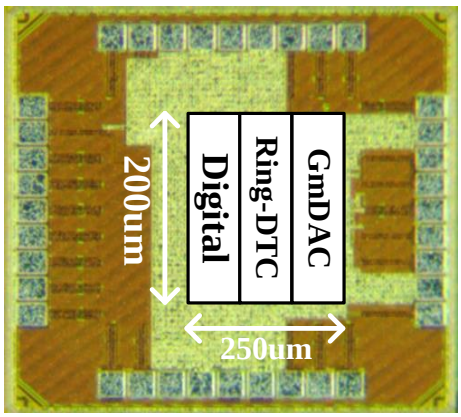


Figure 2.14: Die micrograph

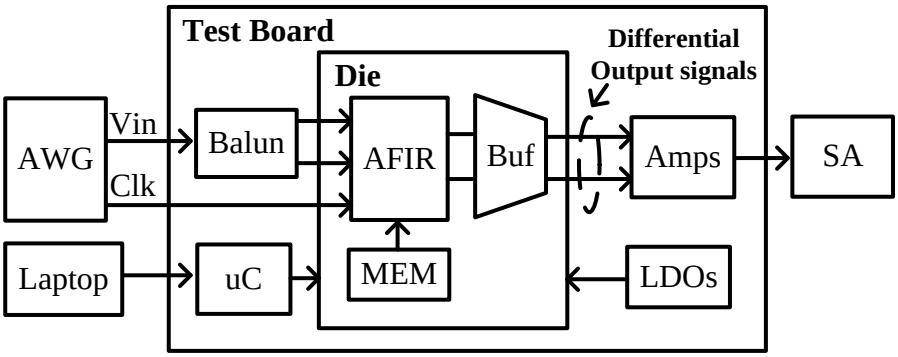
2.6 Measurement

2.6.1 Measurement Setup

The prototype of the proposed AFIR filter was fabricated in the 28nm CMOS process with a compact area of $0.05mm^2$. Die micrograph is shown in Figure 2.14.

Figure 2.15 shows the measurement setup for the test chip. The test chip is attached to the PCB through chip-on-board. An arbitrary waveform generator (Keysight 33612A) provides synchronous single-end input and clock signals. An on-board balun (ADT1-6T+) converts the single-end input signal to differential signals and provides the common-mode voltage. The AFIR output signals are connected to the on-chip buffer, which isolates the internal sampling nodes and drives the external amplifier connected to the spectrum analyzer (Keysight N9010B). The laptop generates the synthesis FIR coefficients and sends them to the microcontroller. The microcontroller, in turn, relays these coefficients to the on-chip digital controller, which stores them in the on-chip memory.

An internal bypass path is implemented to calibrate the frequency response and noise of the on-chip buffer to the spectrum analyzer path. In frequency response



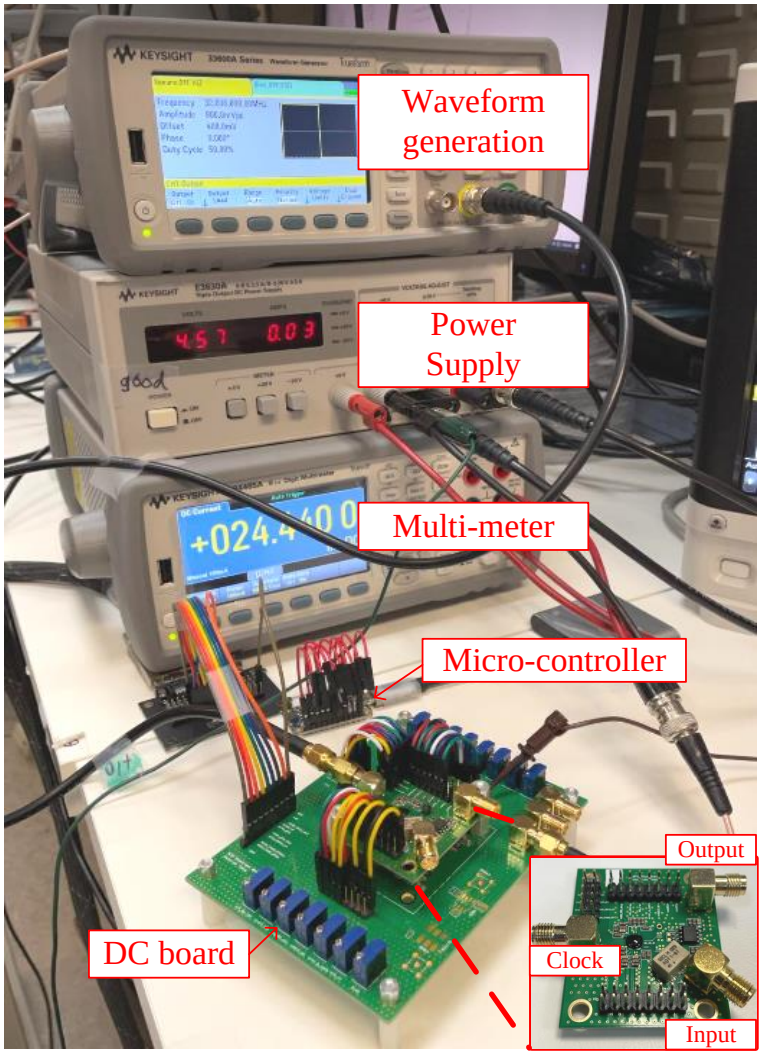


Figure 2.15: Measurement setup

calibration, the bypass path's measured response is normalized and inversely applied to compensate for the main path result. Similarly, for the noise calibration, the bypass path's noise is first measured and subtracted from the main path's noise result.

2.6.2 FIR Coefficients Optimization

In this work, FIR coefficients are synthesized using MATLAB's Filter Design Toolbox. Due to the circuit mismatches and other non-idealities, it is necessary to optimize the coefficients to enhance the filter performance. To facilitate this, we developed a closed-loop measurement setup. In our setup, MATLAB software serves as the host, generating the coefficients and sending the configuration to the chip via a microcontroller. The system then evaluates the frequency response by measuring the rejection at designated frequency points and uses this data to refine the coefficients iteratively.

The optimization problem is structured as a Mixed-integer Nonlinear Programming (MINLP) [45] optimization because it involves discrete integer variables with bound constraints. The objective function is to minimize the difference between measured out-of-band rejection and desired rejection. The number of integer variables correlates with the number of taps, while each variable is bound by the constraint linked to the bit resolution. To limit the search space, we specified the space that reflected the typical bell-shaped curve of a low-pass FIR filter. In the measurement, we selected 40 frequency points uniformly distributed from the filter's passband to the first aliasing clock frequency ($1*f_{clk}$). The target rejection level is pre-evaluated using an ideal quantized filter response. The OOB rejection after optimization is close to the ideal quantization result with $\leq$ 3 dB error.

The optimization equation can be described as

$$\begin{aligned} \mathrm{x} = \underset{\mathbf{x}\in\mathcal{Z}^N}{\operatorname{argmin}} \sum_{k=1}^{K} \|f^*(f_k) - f_{meas}(\mathbf{x}, f_k)\|_2^2, \\ s.t\ \{x_i : x_i \in \mathcal{Z}\ and\ 0 \leq x_i \leq 2^B - 1\} \end{aligned} \tag{2.17}$$

where x represents the FIR coefficients, N represents the number of taps, B represents the bit resolution, K represents the number of frequency points to be evaluated, f_k represents the selected frequency, f^* represents the desired rejection level, and f_{meas} represents the evaluated rejection level. Figure 2.16 shows the filter optimization flow. Optimization begins by assessing the ideal frequency response according to the specified frequency requirements. This initial evaluation determines the necessary number of taps and the bit resolution required for the filter. Following the initial evaluation, MATLAB's optimization tool proceeds the remaining optimization process.

2.6.3 Frequency Response and Out-of-band Rejection

Figure 2.17 shows the measured normalized frequency response of the filter. When the clock frequency is set at 48 MHz, the result indicates that the filter achieves a tunable bandwidth ratio of 6.8 with varying the number of taps from 16 to 128. Moreover, if the clock frequency is increased to 80 MHz while maintaining the 16 taps, the bandwidth ratio can increase to 12.4. The overall bandwidth can be adjusted from 0.37 to 4.6 MHz.

Figure 2.18 shows the measured reconfigurability of stopband attenuation while maintaining a similar filter bandwidth. Operating at clock frequency 48 MHz and using 96 taps, the filter allows for adjustment of the bit resolution from 11 to 9 bits, corresponding to a change in stopband attenuation from -70 dB to -50 dB. Concurrently, this resolution scaling also results in a proportional reduction in power consumption, from 356 uW to 225 uW, demonstrating the efficiency of the power

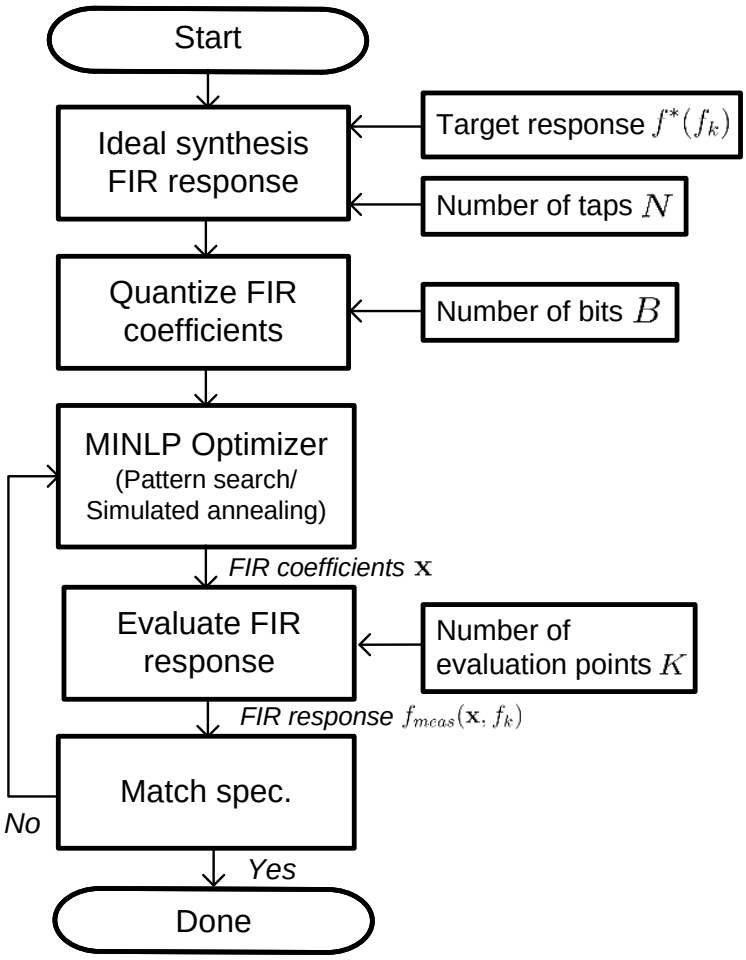


Figure 2.16: FIR coefficients optimization flow

scaling with bit resolution. Figure 2.24 shows the maximum rejection across five experiment chips, all configured with 96-tap/11-bit/48MHz. Each chip has undergone the FIR coefficient optimization process and achieves a minimum stopband rejection of -69 dB.

Figure 2.19 shows the double-edge cancellation for odd-order aliasing clock frequencies. The filter is intentionally configured to 32-tap/10-bit to see the 1st and 2nd aliasing clock frequencies. The double-edge cancellation achieves -40 dBc rejection at the first aliasing clock frequency, complemented by an additional 10dB rejection at frequencies close to the clock frequency. It also shows there is no even-order aliasing

clock frequency rejection. Such high-order clock frequencies are typically suppressed by the previous stages in front of the AFIR in the receiver chain.

2.6.4 Linearity

Figure 2.20 illustrates the out-of-band OIP2 and OIP3 measurement. For the OIP3 measurement, an intermodulation signal was fixed at 50kHz, and two signal tones were applied at frequencies of 4.01 MHz and 7.97 MHz. Meanwhile, tones at 4.01 MHz and 4.06 MHz were selected for the OIP2 measurement. The result shows that the filter can achieve 42 dBm OIP3 and 60 dBm OIP2.

Figure 2.21 shows the result of sweeping the frequency offset from 2 MHz to 40 MHz for both OIP2 and OIP3 measurements. These results show that the out-of-band performance of the filter remains stable across various bandwidths.

2.6.5 Efficient Power Scaling and Rejection Optimization

Figure 2.22 shows the measured power distribution among various blocks in the 96-tap/11-bit/48MHz configuration. The data reveals that high-speed digital blocks account for most power consumption (the ring-DTC consumes 280 uW, and the digital controller consumes 66.5 uW). These findings suggest that adopting a more advanced process node could potentially reduce power consumption.

Figure 2.23 shows the power consumption of the AFIR filter with different numbers of taps and bit resolution under similar bandwidth. The graph shows a highly linear relationship between power consumption and the number of taps and bits, indicating efficient power scaling characteristics. To keep a similar bandwidth, the tap, consequently the clock frequency, is well-known as having an approximate linear relationship with the power consumption. In our approach, we further adjust the bit resolution by setting the ring-DTC lap counter, which similarly exhibits a linear relationship with the power consumption. Thus, the observed results align with our

expectations.

Figures 2.25 and 2.26 detail the power consumption and rejection of the AFIR filter related to the reconfigurable parameters while maintaining a 0.46 MHz bandwidth. These figures emphasize the capability to optimize between power consumption, stopband attenuation, and the frequency of aliasing clock according to different target applications.

2.6.6 Performance Summary

Table 1 summarizes the chip performance measured under 800 mV supply voltage. All measurements under a clock frequency of 48 MHz with 96-tap/11-bit unless specified. The proposed AFIR shows its reconfiguration ability with two FIR coefficient configurations: 1) high stopband rejection achieving -70 dB with sharp transition f_{-60dB}/f_{-3dB} ratio 4.5 and 2) low power consumption of 90 uW achieving -60 dB rejection under 16 MHz clock frequency and 32-tap/10-bit. Compared with similar FIR works, it also demonstrates better OIP3 43.7 dBm with the help of small and linearized gm-DAC. Compared with analog-IIR works, the proposed AFIR provides more programmability while using less area.

2.7 Summary

This work demonstrates a highly reconfigurable low-power AFIR filter with a novel 11-bit charge-domain DAC implementation. A power-efficient change-domain approximation signal processing technique is proposed, analyzed, and implemented. The proposed charge-domain DAC features a compact gm-DAC and a highly programmable time-DAC. It first demonstrates that the AFIR can achieve -70 dB rejection with a sharp transition and low power consumption of 356 uW in the CMOS process. The study further examines the use of the AFIR filter in the standard zero-IF receiver, illustrating that the proposed AFIR filter offers significant flexibility. It

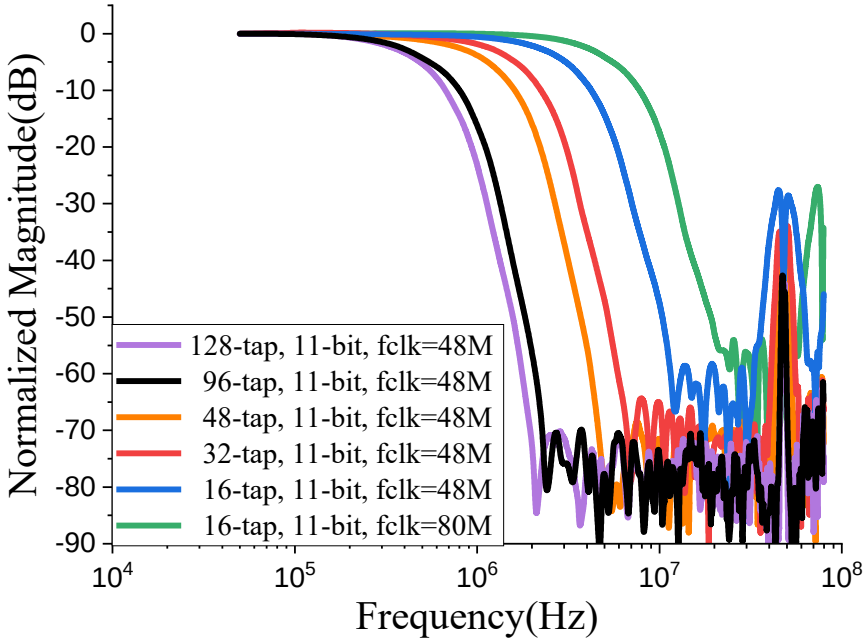


Figure 2.17: Measured reconfigurable bandwidth with different setting

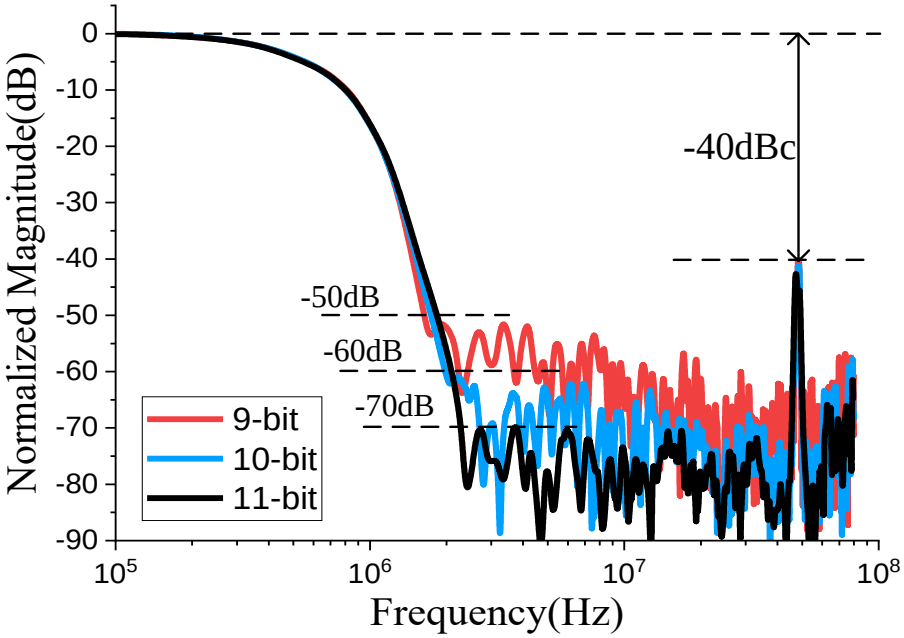


Figure 2.18: Measured reconfigurable stopband rejection with different setting

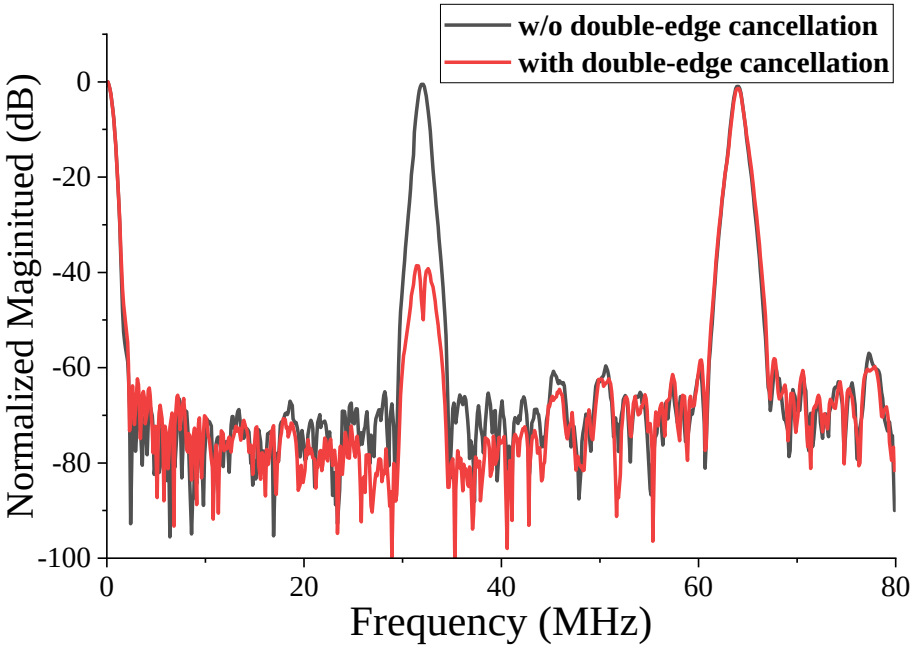


Figure 2.19: Measured double-edge cancellation at f_{clk} frequency

enables customization of power consumption, bandwidth, and stopband rejection to meet the needs of programmable receivers. Consequently, the proposed circuit can effectively tackle the growing issues of RF spectrum congestion that arise from the proliferation of connected devices in dense environments.

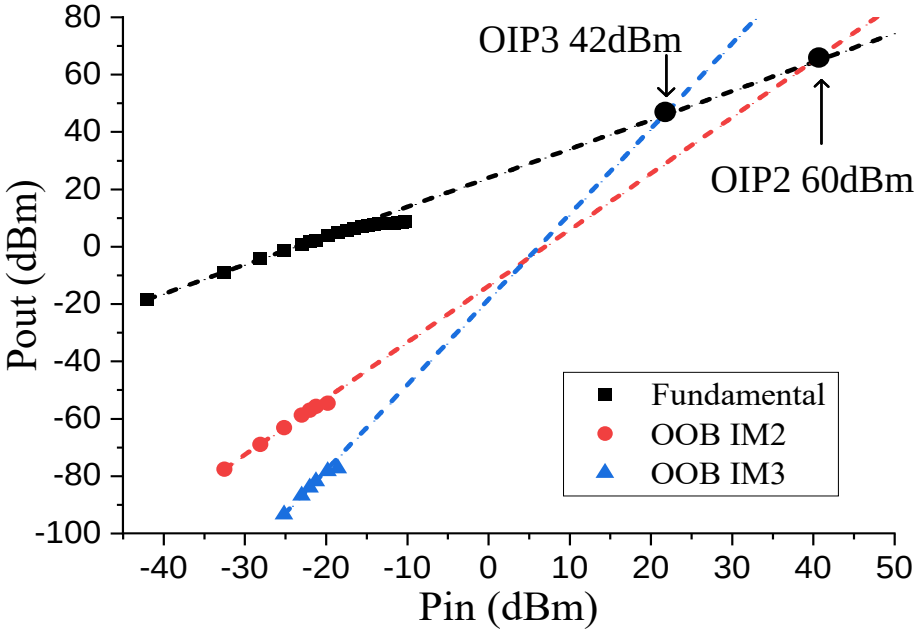


Figure 2.20: Measured OIP2/OIP3 versus input power

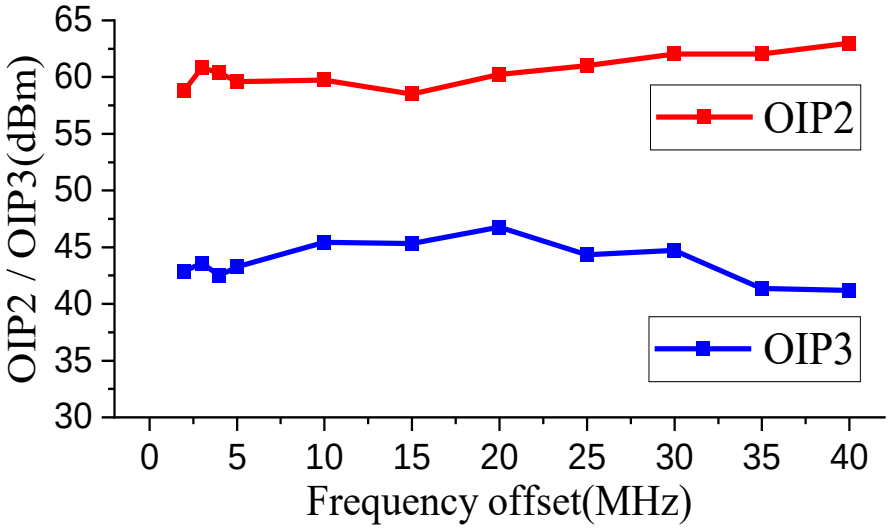


Figure 2.21: Measured OIP2/OIP3 versus frequency offset

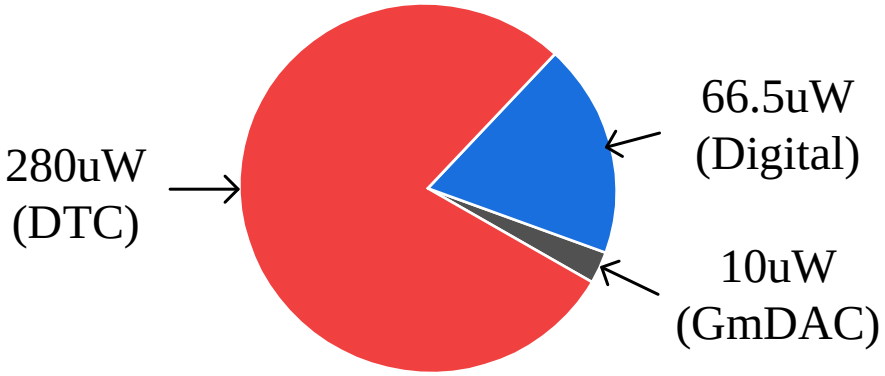


Figure 2.22: Measured power distribution

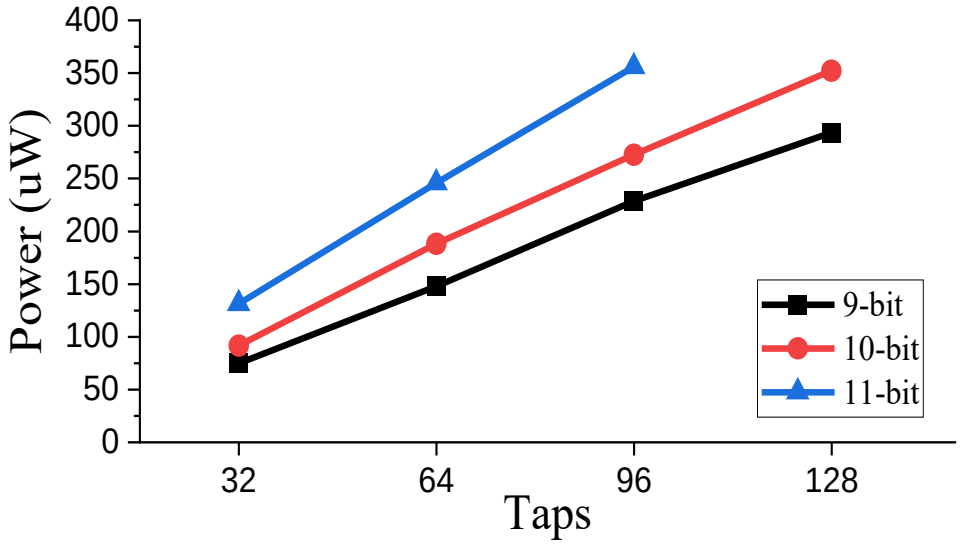


Figure 2.23: Measured power consumption with different numbers of taps and bits

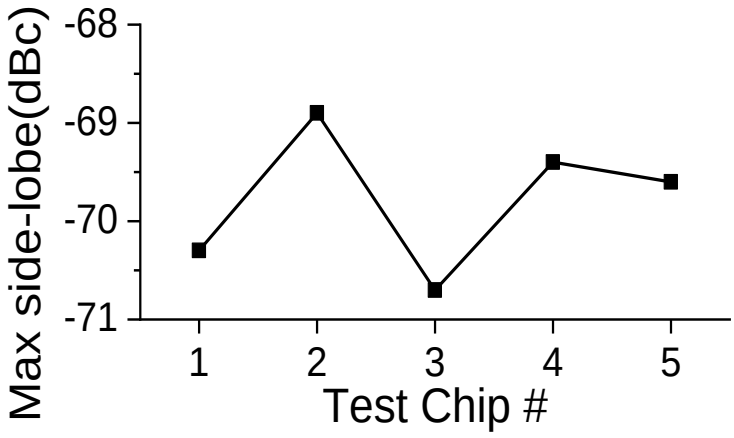


Figure 2.24: Measured OOB rejection of five different chips

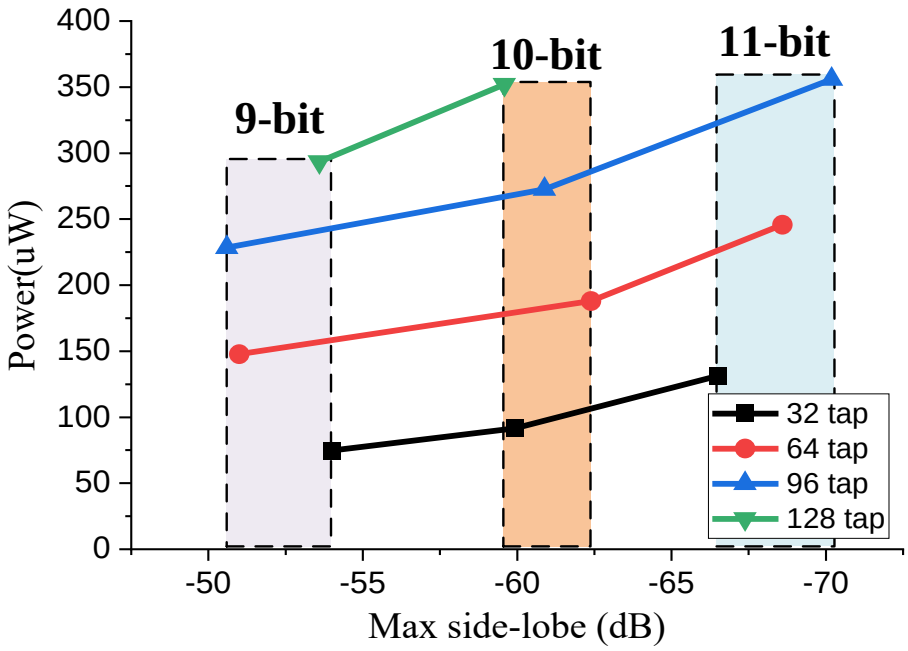


Figure 2.25: Rejection optimization with different numbers of taps and bits

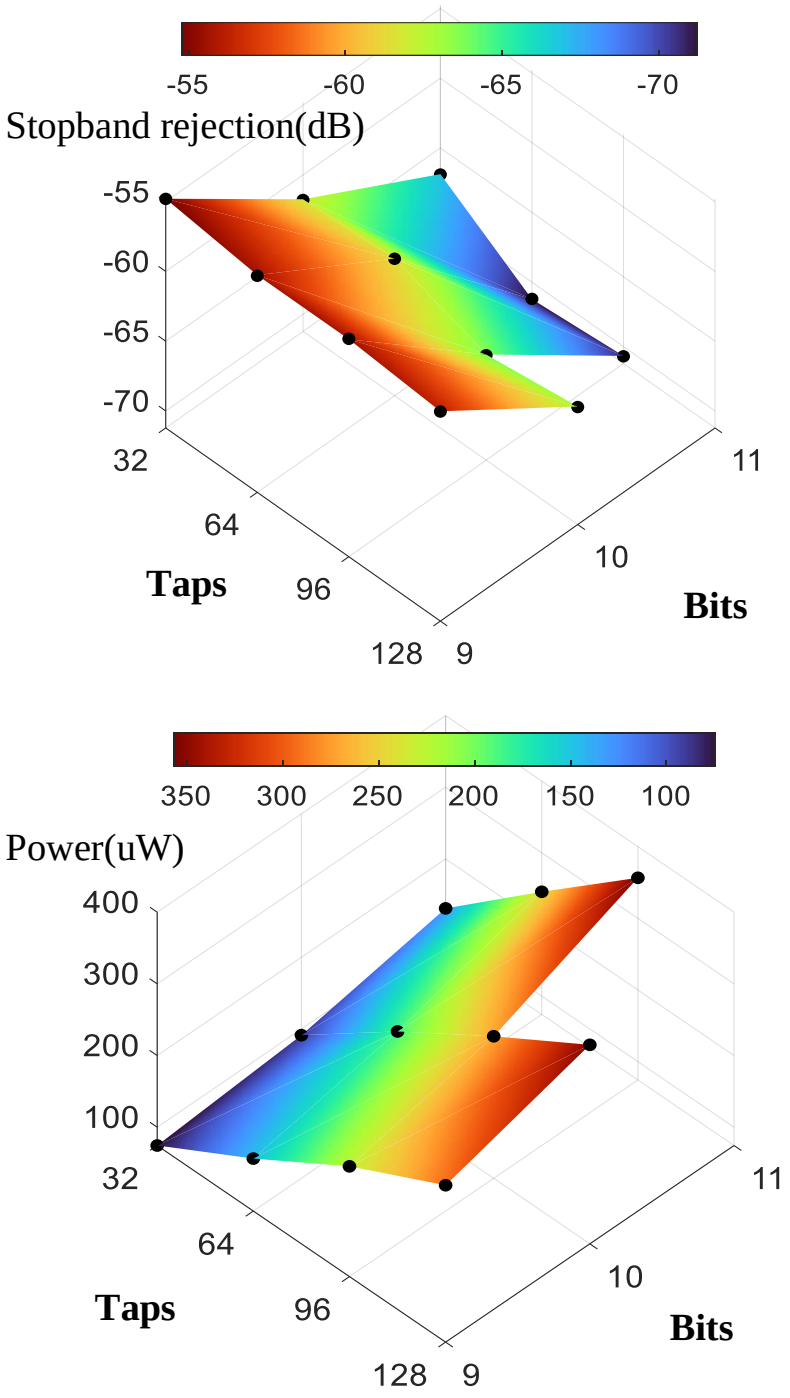


Figure 2.26: Rejection optimization with different numbers of taps and bits

Table I : State-of-the-art Comparison

	This work		JSSC'20[7]	JSSC'13[5]	JSSC'18[6]	JSSC'14[2]	TCAS'18[3]	JSSC'22[4]
Topology	CD-AFIR		AFIR	Cascade-AFIR	FA	CS-IIR	CS-IIR	CS-IIR
Reconfigurability[#]	9/10/11-bit + 16~128-tap		10-bit + 16[†]~128-tap	3-bit delay D_T	13-bit with varying Ts	0.25~64pF C_H + 0.4~2.2pF C_S	1~68.5pF C_H + 0.5~4pF C_S	1~19pF C_H + 0.5~4pF C_S + 1~6pF C_{IH}
Technology	28nm CMOS		22nm FDSOI	65nm CMOS	65nm CMOS	65nm CMOS	180nm CMOS	28nm CMOS
Supply (V)	0.8		0.7	1.2	1.2	1.2	1.8	0.9
Tunable BW (MHz)	0.37-4.6		0.06-3.4	5-26	1.25-20[+]	0.4-30	0.49-13	1-9.9
Min.Stopband Rejection (dB)	Low power (32-tap/ 10-bit)	Max rejection (96-tap/ 11-bit)	-60 (128-tap/ 10-bit)	-65.3	-70	-83[†]	-90[†]	-98[†]
	-60*	-70						
f_{-60dB}/f_{-3dB}	4.15*	4.5	3.8	1.5	3.3[†]	7.8[†]	7.5[†]	14[†]
Power(mW)	0.09*	0.356	0.092	8.4	75~99	1.98	4.3	0.92
IB OIP3[‡] (dBm)	25		-	13	31	31	28.7	32.4
OB OIP3[‡] (dBm)	43.7		28	-	44	21	32.63	41.3
OB OIP2[‡] (dBm)	60.5		-	-	87	69.3	73.48	-
Gain (dB)	23.5		31.5	41	23	9.3	17.6	14.7
IRN (nV/√Hz)	26[§]		12	12.3	-	4.57	6.54	3.5
Area (mm^2)	0.05		0.09	0.52	2.3	0.42	2.9	0.192

[#]Fix clock frequency; *fclk=16MHz; [†]Estimate from figure; [§]Integrated over 50k-460kHz; [+]Baseband BW; [‡]OIPn=IIPn+Gain;

Figure 2.27: Table 1: State-of-the-art comparison

CHAPTER III

A Long-Range Narrowband RF Localization System with a PLL-Less Frequency-Hopping Receiver Front-End

3.1 Introduction

3.1.1 Background

Emerging internet-of-thing (IoT) applications, such as asset tracking and first responder rescue operation, require a new localization solution that achieves decimeter-level accuracy for long-range (km) in GPS-denied indoor non-line-of-sight (NLOS) scenarios [46]. Accurate and long-range localization service in intelligent warehouses and factories enhances efficiency and effectiveness. These services involve precisely determining the real-time positions of assets [47], inventory, and personnel within such environments. Application of such service enables greater operational control, optimizes resource allocation, improves safety, and streamlines various processes. This type of localization service also has numerous applications in public safety, offering advanced solutions for enhancing emergency response, situation awareness, potential threat surveillance, and public health monitoring. We envision a new localization technology with the following characteristics: 1) Operable in LOS/NLOS environ-

ments. 2) Low power, low cost, and small form factor of tag device. 3) Rapidly deployable with low-cost commercial components as anchor infrastructure. 4) Multiple-access, concurrent localization service to multiple tag devices.

This work has already been published in [19]. A comprehensive explanation will be provided in this chapter.

3.1.2 Prior Works

There are several existing wireless localization solutions.

Conventional long-range localization relies on the Global Navigation Satellite System (GNSS). GNSS technology requires a LOS condition between the receiver and the satellites to determine positioning. However, this requirement poses a constraint that reduces its effectiveness in environments with abundant signal reflection, like indoor areas, areas with geographical features such as valleys or tall buildings, and underground positioning [48]. In addition to accuracy impairments due to the NLOS condition, the high power consumption and huge integration form factor of GNSS receiver make it challenging to fit power-constrained and miniaturized devices for IoT applications [49].

Impulse response ultra-wideband radar (IR-UWB) is another popular approach. IR-UWB localization leverages the unique properties of short-pulse wide-bandwidth signals to provide highly accurate and reliable positioning information [50–52]. It can achieve high precision in the order of centimeters but cannot operate in long-distance NLOS conditions due to FCC-regulated transmit power limits and severe path loss through walls. Moreover, IR-UWB requires high instantaneous power ($\geq$ 70mW [2]), rendering it impractical for energy-constrained IoT with small batteries and high internal resistance. Also, the conventional signal process approach requires a high sampling rate (in the order of GS/s) ADC to sample the short pulses, making the high-speed ADC power-hungry and high cost for IoT applications.

Many localization applications have been explored to fit WiFi/BLE systems as they have widely deployed infrastructure. Several localization technologies can demonstrate decimeter accuracy by using either the received signal strength indicator (RSSI), time-of-flight (ToF), or multi-carrier phase base ranging (MCPD). However, they typically have a limited range of $\leq$100m or are not operable in NLOS condition [53–62]. In addition to the limited localization range and condition, the high power consumption of the system makes it impractical to fit the IoT application. In a proprietary 80MHz [63–65], the Bluetooth-based MCPD localization method shows a tag receiver power consumption of 5.3 mW, but it has a limited range of only 20 meters. In a proprietary 80 MHz OFDM-based solution [61], it uses an active reflection IC to achieve decimeter-level accuracy in NLOS conditions. However, it requires relatively high power consumption ($\sim$62.8 mW) with a limited range of up to 100 meters.

Low Power Wide Area Networks (LP-WANs) can cover long ranges on the order of hundreds of meters to kilometers; their accuracy is relatively poor, especially in multi-path rich environments at about tens of centimeters to tens of meters [66–68].

3.1.3 Proposed Solutions

Addressing this technological gap, we propose a novel localization system to achieve long-distance operation and low-power tag receivers with narrowband subcarriers communicating between anchors and tag devices while maintaining high accuracy in a multi-path rich environment. The system can operate at the free-licensed ISM band, 900 MHz/2.4 GHz/5.8 GHz, to be compatible with existing mobile infrastructure. It hops through the available bandwidth utilizing narrowband frequency-orthogonal subcarrier signals. Multiple anchors are used in the system, each communicating with narrowband signals to have better signal-to-noise (SNR) ratio. The tag receives the concurrent narrowband signals from multiple anchors and hops harmoniously across the pre-determined frequency pattern agreed upon in the system.

Anchors and tag devices communicate in frequency-orthogonal signals, making it work as an orthogonal frequency multiple access (OFDMA) scheme. The narrowband subcarrier signals are combined and then used to estimate the channel impulse response (CIR) as it is operating in full bandwidth. The time-of-arrival (ToA) is used to calculate the distance between the tag and anchors, and the precise tag localization can be estimated with time-difference-of-arrival (TDoA) with multilateraion TDoA information. The accuracy of ToA can be improved with a neural network, which is trained to learn the shape of the first arrival of CIR response in a multi-path rich environment.

To further advance the system performance regarding the tag device's localization range, power consumption, and form factor, we implemented the tag receiver by fabricating a new custom ASIC receiver in the 55nm CMOS process. The proposed ASIC tag receiver features a PLL-less receiver while operating in a frequency-hopping fashion. The RF impairments due to the lack of precise frequency reference were then resolved by an innovative digital signal processing approach. The tag receiver achieves a narrow bandwidth of around 1.6 MHz, a high sensitivity of -115 dBm, low power consumption of 3.9 mW, and a small form factor $2mm^2$ die area, enabling the system to operate in long-range 621 meters with decimeter accuracy 0.6 meters in relatively wide bandwidth 100 MHz of 2.4 GHz band.

The system introduces a novel approach in which the tag receiver does not rely on strict frequency and phase information, enabling the low power and small form factor tag device. The absolute distance information can be calculated by observing concurrently multiple tags to anchor ToA information, then making it to TDoA with multilateral processing to localize the tag precisely. The ToA from each tag to anchor is estimated by observing the *relative amplitude and phase difference* of narrowband symbols across multiple hopping subcarrier symbols. The use of relative amplitude and phase in the proposed system mitigates the strict frequency/phase requirements,

allowing the tag to operate in PLL-less operation. To address the relative amplitude and phase ToA scheme and PLL-less receiver, we proposed a novel signal processing algorithm to correct the receiver impairments, i.e., frequency offsets, phase noise, and phase uncertainties between narrowband frequency hops, showing the feasibility of digitally enhanced low power RF systems where the requirement of analog/RF circuit is relaxed to save power and form factor. In contrast, advanced digital signal processing algorithms compensate for impairments.

The anchors in the proposed system are implemented with Universal Radio Software Peripheral (USRP) X310 software-defined radio. We customize the FPGA fabric RTL design to enable a real-time frequency hopping system and process the tag-received information on the fly. The system was evaluated in an indoor multi-path rich environment of distance ≤ 60 meters and outdoor LOS environment ≤ 621 meters 1-D TDoA performance. We were able to achieve decimeter-scale accuracy in both environments.

3.2 Narrowband RF Localization System Overview

3.2.1 Main and Reflection Anchors

The localization system involves a primary/main broadcast anchor and multiple (≥ 3) reflecting anchors at known positions. Tags (receivers) can self-localize based on the received symbols from the anchors and the known positions of the anchors. The narrowband symbols are transmitted in a pre-determined pattern understood by the receiving tags and the reflecting anchors. The main anchor initiates transmission through a synchronization signal followed by the transmission of the narrowband symbols. After detecting the synchronization signal, the reflecting anchors re-transmit received symbols from the main anchor to the tags with a constant frequency shift. Reflected symbols from multiple reflecting anchors and the original symbol from the

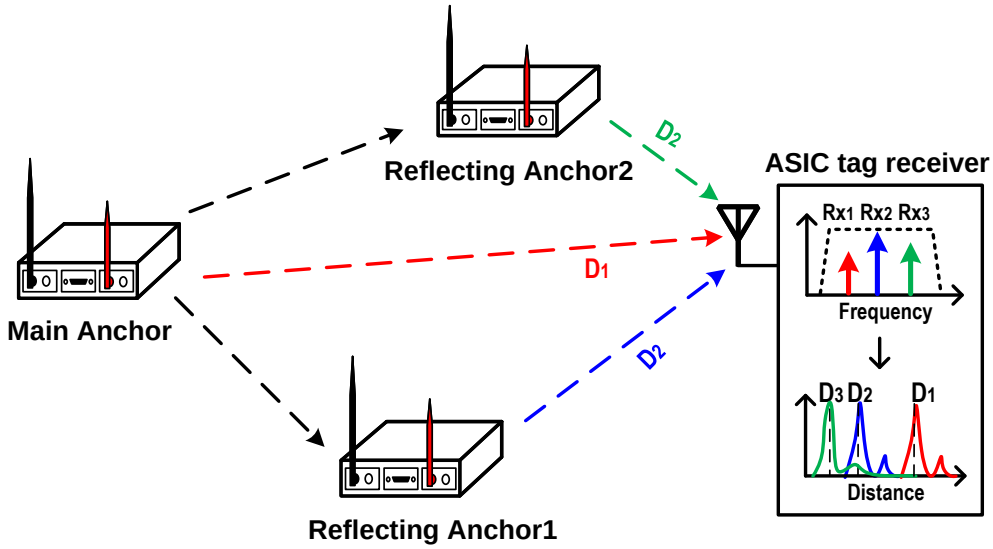


Figure 3.1: Narrowband RF localization system overview

main anchor are transmitted on orthogonal subcarrier channels as in an OFDMA scheme. The proposed signal reflection scheme with OFDMA transmission using multiple anchors is shown in Figure 3.1.

This localization system operates within a 100 MHz bandwidth available in the 2.4 GHz ISM band. This bandwidth is divided into 512 × 16 subcarriers, where 512 is used for symbol transmission by a single anchor, and 16 is the maximum number of anchors. The symbols are akin to single-frequency tones with a bandwidth given by the subcarrier frequency spacing of ∼12 kHz. The symbol length is given by 1/ (subcarrier frequency spacing). Symbols are transmitted on subcarriers sequentially spaced from one another across the bandwidth at a frequency interval of 16 subcarriers (∼195 kHz). This arrangement enhances frequency diversity, making the system resilient to wireless channel interference [69]. Each symbol transmission is preceded by a cyclic prefix guard interval, similar to OFDM systems, to counter channel dispersion and inter-symbol interference [70, 71].

A reflecting anchor receives a symbol from the main anchor and simultaneously

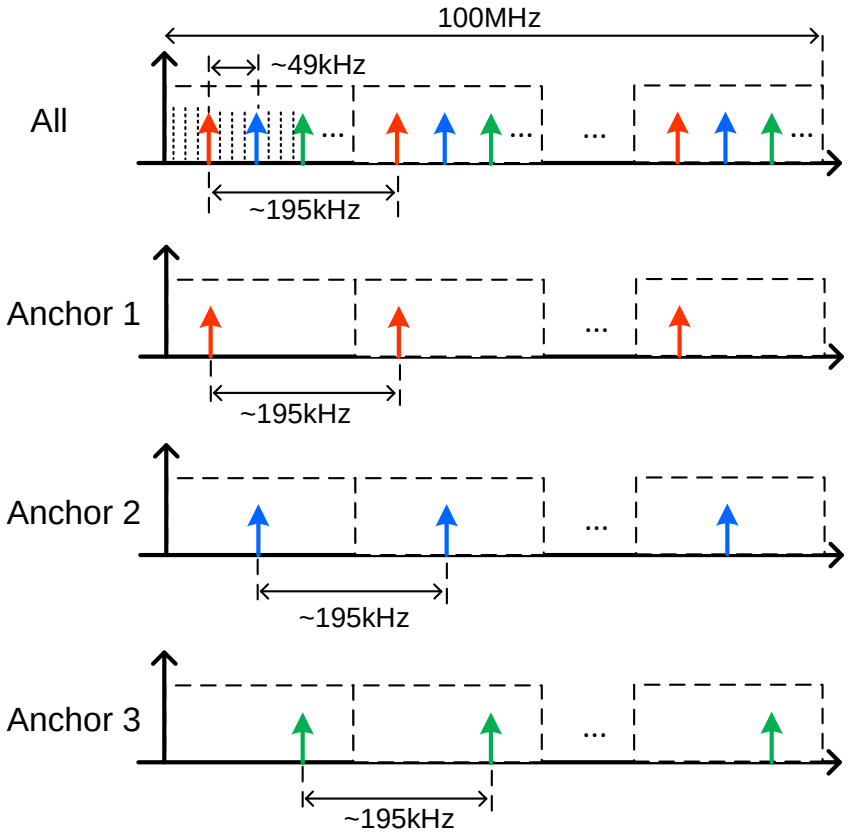


Figure 3.2: System frequency plan and subcarriers hopping in different anchors

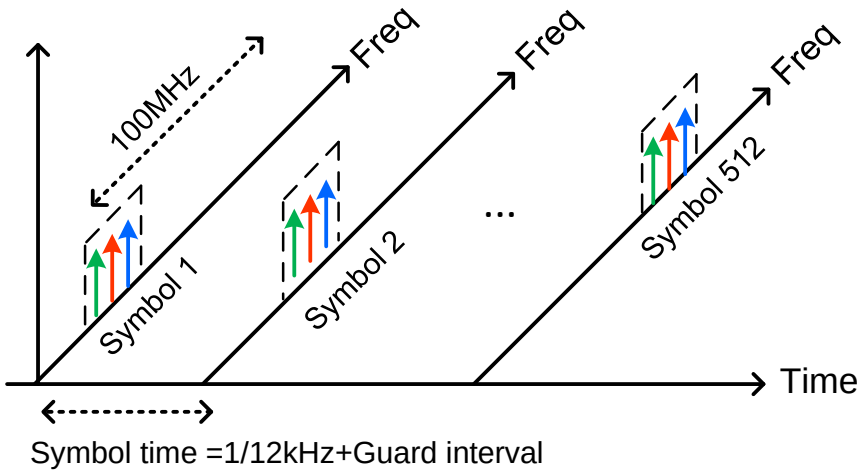


Figure 3.3: Localization system subcarrier frequency hopping versus time

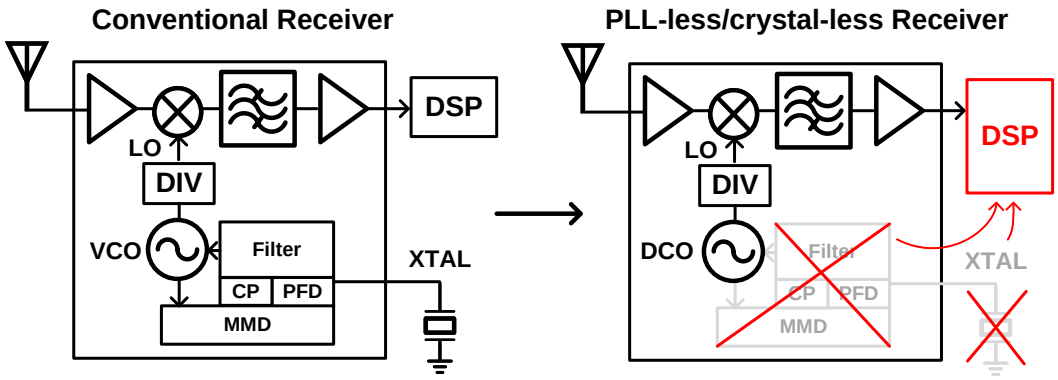


Figure 3.4: Proposed PLL-less receiver with digital-assisted signal processing for localization system

re-transmit the same symbol on a different subcarrier. It receives a symbol from the main anchor, corrects its phase and frequency offsets, and re-transmits the offset-corrected symbol with a distinct frequency shift on a dedicated subcarrier for reception by the tags. With three reflecting anchors in the system, for example, each has a unique frequency shift equivalent to multiples of 4-subcarrier frequency spacing (approximately 49 kHz, 98 kHz, and 146 kHz) to ensure orthogonality among symbols transmitted by the main anchor and the other reflecting anchors as shown in Figure 3.2 and Figure 3.3. This system resembles OFDMA [72], as the main and reflecting anchors transmit simultaneously on different orthogonal subcarriers.

3.2.2 Tag Receiver

The proposed localization system introduces an innovative approach in which the RF receivers on the tags do not require strict phase and frequency synchronization with anchors. This eliminates the need for a power-demanding and expensive conventional phase-lock loop (PLL) that relies on a high-frequency crystal reference [73] as shown in Figure 3.4. Instead, the system employs a PLL-less, low-power RF receiver with a superb sensitivity of -115 dBm and a digitally controlled free-running oscillator (without a high-frequency crystal) for signal reception. We built and evaluated our

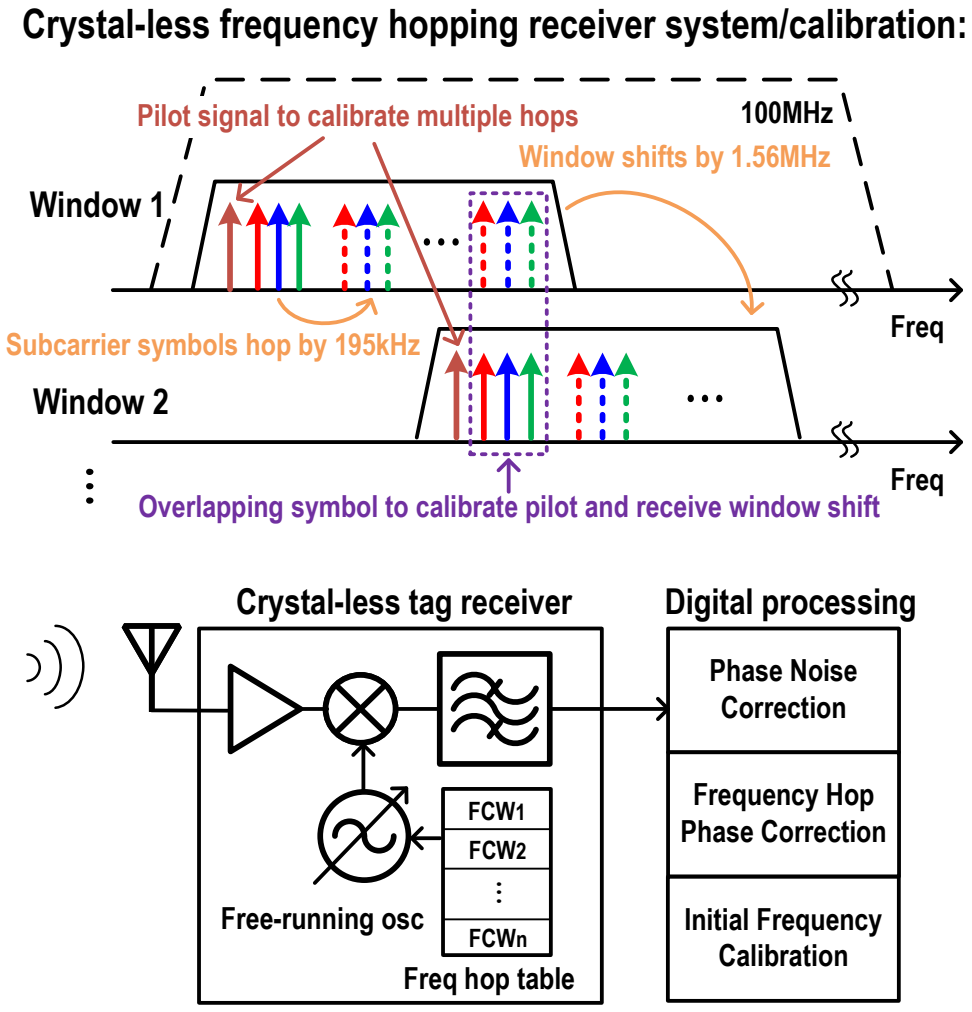


Figure 3.5: Proposed digital signal processing techniques to mitigate receiver impairments

system using a PLL-less, low-power ASIC RF receiver chip. The receiver features a programmable intermediate frequency (IF) and a bandwidth of approximately 1.6 MHz for a given IF in the 2.4 GHz ISM band. This architecture enables the tag to capture narrowband frequency hopping symbols transmitted across a 100 MHz bandwidth by dynamically adjusting its IF center frequency (similar to a typical BLE receiver) according to a pre-determined hopping pattern.

The emphasis on low-power and cost-effective design influences the localization system's configuration. To accommodate the available bandwidth for frequency hop-

ping, the bandwidth is divided into 64 tag-receiving windows, each spaced by 1.56 MHz (equivalent to 8 frequency hopping symbols). The PLL-less receiver's center frequency is tuned using a calibrated control word for each window, allowing it to receive the localization symbols within that specific band. The tag systematically moves across the entire bandwidth by transitioning from one window to another for symbol reception. However, due to the absence of a PLL, the receiver introduces impairments such as frequency and phase offsets, necessitating correction for accurate CIR estimation. To address these challenges via digital signal processing, the system introduces constant pilot symbols sent by the main anchor alongside each narrowband symbol received at the tag. These pilot tones maintain a consistent frequency and phase throughout the receiving window. The issue of phase inconsistency between tag-received symbols from different windows is tackled by transmitting the first symbol of each window to be phase-continuous with the last symbol in the preceding window, facilitating the estimation and rectification of phase shifts across windows. The two mechanisms can be illustrated in Figure 3.5. The tags, provided with sufficient information about the frequency- and phase-shift between pilots and symbols for each receiving window, correct for introduced impairments using the algorithm discussed in the following section.

3.2.3 Summary

In summary, the tag traverses the entire bandwidth with frequency hopping in 64 iterations, receiving 9 symbols during each receiver window hop, resulting in a cumulative reception of 64×9 symbols. The anchors transmit 512 distinct localization symbols together with the 64 pilot tones for the receiving windows. A localization symbol is repeated for adjacent receiving windows for frequency and phase offset corrections. With a subcarrier bandwidth of around 12 kHz and guard interval matching the symbol length and extension of symbol duration to enhance SNR, each symbol

has a duration of 330 us. The time required to transmit all the necessary 64×9 symbols for localization amounts to roughly 181.5 ms, which is within the coherence time of our wireless channel [74, 75].

Upon successful reception, the tag computes each received symbol's channel frequency response (CFR). These CFRs serve as the basis for inferring the CIR corresponding to each anchor-to-tag pathway. Subsequently, ToA is determined from the CIRs through a trained neural network, enabling the calculation of TDoA between anchors. Leveraging this TDoA information alongside the known positions of the anchors, multilateration methods are employed to estimate the tag's location accurately.

3.3 Narrowband Localization System Design

3.3.1 Main and Reflection Anchors

Figure 3.6 shows the main and refecting anchor operation.

The main anchor controls the start of localization in the system. It initiates the process by broadcasting a synchronization signal to both the reflecting anchors and the tag, which serves as a signal to commence transmission. The hopping sequence from one symbol to the next is pre-established and known to the reflecting anchors and the tag, thus eliminating the necessity for communication on this aspect during localization. The main anchor hops sequentially through the localization bandwidth, transmitting the essential localization pilots and symbols for each hop. Each hop involves the transmission of narrowband localization symbols/pilots, achieved by transmitting tones with frequencies corresponding to the subcarrier frequencies designated for that specific hop's pilot and symbol. This mechanism leads to the composition of OFDMA symbols in which active subcarriers correspond to the pilots and symbols of the given hop.

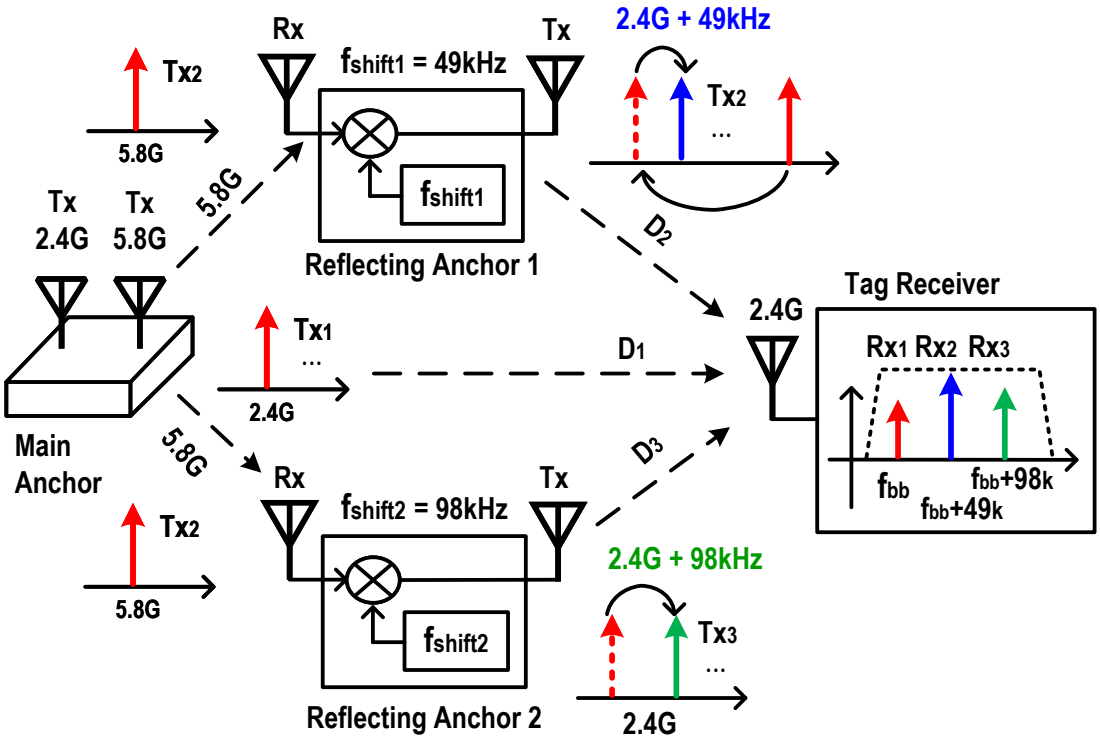


Figure 3.6: Main and reflection anchor perform anchor-specific frequency shift

The main anchor transmits these symbols concurrently utilizing two distinct carrier frequencies, necessitating the presence of two RF transmitters operating with different carrier frequencies: 2.4 GHz and 5.8 GHz. This concurrent transmission is necessary because each reflecting anchor performs reception using the 5.8 GHz carrier and simultaneously re-transmit the reflected symbols using the 2.4 GHz carrier. Concurrent reception and transmission are only possible because they are performed on different carrier frequencies in the reflecting anchor (otherwise, the receiver is interfered with by the transmitter using the same/similar frequency). The tag operates only in the 2.4 GHz to receive the original symbol from the main anchor and reflected symbols from reflecting anchors.

The reflecting anchor comprises a receiver in 2.4 GHz and a transmitter in 5.8 GHz. The receiver captures signals sent by the main anchor in 5.8 GHz. At the

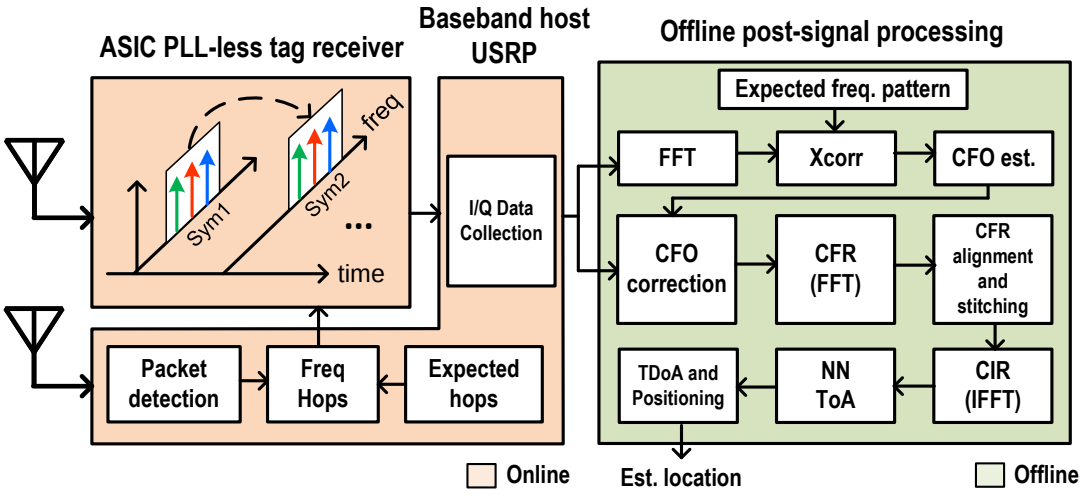


Figure 3.7: Tag receiver system design and post-signal processing flow

same time, the transmitter serves to retransmit the received symbols after applying a distinct frequency shift to a subcarrier in the 2.4 GHz band for each reflecting anchor. The use of separate 2.4 and 5.8 GHz bands for reception and transmission is guided by the need to avoid crosstalk, given that active reflection in the reflecting anchor requires concurrent reception and transmission. This active reflection is initiated upon detecting a synchronization signal from the main anchor. Leveraging the known hopping pattern and presence of designated pilots, the reflecting anchor also corrects the introduced phase and frequency offsets itself.

3.3.2 Tag Receiver

The tag's operation commences by detecting the synchronization signal from the main anchor, initiating the reception of localization symbols from both the main and reflecting anchors. The signal processing datapath at the tag for localization is illustrated in Figure 3.7.

A novel feature of the system is the innovative tag design that permits a low-power receiver without a PLL, as the approach eliminates the need for accurate

phase, frequency, or time synchronization between the tag and anchors. In the tag implementation, we remove a conventional PLL as well as a high-frequency crystal reference, which are power-demanding and cost-elevating [73]. This ASIC receiver employs a free-running RF oscillator without a PLL or a crystal, and it has an intermediate frequency (IF) bandwidth of around 1.6 MHz. The local oscillator (LO) center frequency is programmable for frequency hopping by a digital control word across the 2.4 GHz ISM band. The design empowers the tag to receive narrowband symbols transmitted across the 100 MHz localization bandwidth by hopping the IF center frequency in alignment with the pre-determined hopping pattern.

The tag's signal acquisition mechanism involves dividing the localization bandwidth into 64 receiving windows. The PLL-less receiver's center frequency is configured for each window using the pre-programmed control word, a process quick enough (approximately 0.3us) to fit within the symbol's guard interval (GI). The tag traverses the entire localization bandwidth methodically, transitioning from one window to the next by tuning to the proper IF center frequency for each receiving window to collect the stream of localization symbols from the anchors.

The absence of a PLL in the receiver introduces impairments that impact the received signal quality for localization. As the receiver's phase noise accumulates, it causes carrier frequency fluctuations, leading to a carrier frequency offset (CFO) during a given receiving window. This frequency offset is particularly critical for our system using narrowband symbols because the offset can be significantly larger than the symbol bandwidth or subcarrier spacing. Furthermore, tuning the IF center frequency for each receiving window introduces frequency and phase offsets into the received signal. If left unaddressed, the impairments introduced by the tag's receiver would cause inter-symbol and inter-carrier interference [76], which can significantly disrupt the coherent reception of the OFDMA symbols. However, the system has been thoughtfully designed to account for these challenges. Incorporating pilot symbols

and repeated symbols across the adjacent receiving windows plays a pivotal role in mitigating the introduced impairments, ensuring a successful localization process.

3.3.3 Tag Post Signal Processing

3.3.3.1 CFO Estimation and Phase Noise Correction

The estimation and correction of the carrier frequency offset are executed using pilot tones on a per-window basis. This correction procedure, specific to each reception window, utilizes all anchor symbols obtained by the tag at the reception window that uses a fixed carrier/intermediate frequency. These symbols consist of the eight localization symbols and the repeated first symbol, which is the same as the last symbol of the previous window. An anchor pilot symbol persists throughout the entire reception window, preserving a constant frequency spacing equivalent to the sub-carrier separation of the anchors. Figure 3.8 shows the pilot and data symbols. Armed with a prior understanding of the anticipated frequency and subcarrier shifts for capturing these pilot and other anchor symbols in relation to the center frequency of the reception window, the tag initiates a correction mechanism to cancel the frequency offset for that receiving window.

The CFO correction procedure, which is done in the frequency domain, involves performing a fast Fourier transform (FFT) of the received signal and evaluating cross-correlation by shifting the carrier frequency gradually with the expected pattern for the pilot and other anchor symbols. Given the fixed subcarrier allocation of these pilot and non-pilot symbols, the frequency shift that results in maximal cross-correlation is used to estimate the frequency offset of the receiving window [77]. The CFO of the received signal window is then rectified by shifting the signal by the estimated frequency offset.

In addition, the correction of frequency/phase drift resulting from phase noise throughout the reception window for each anchor is accomplished by comparing the

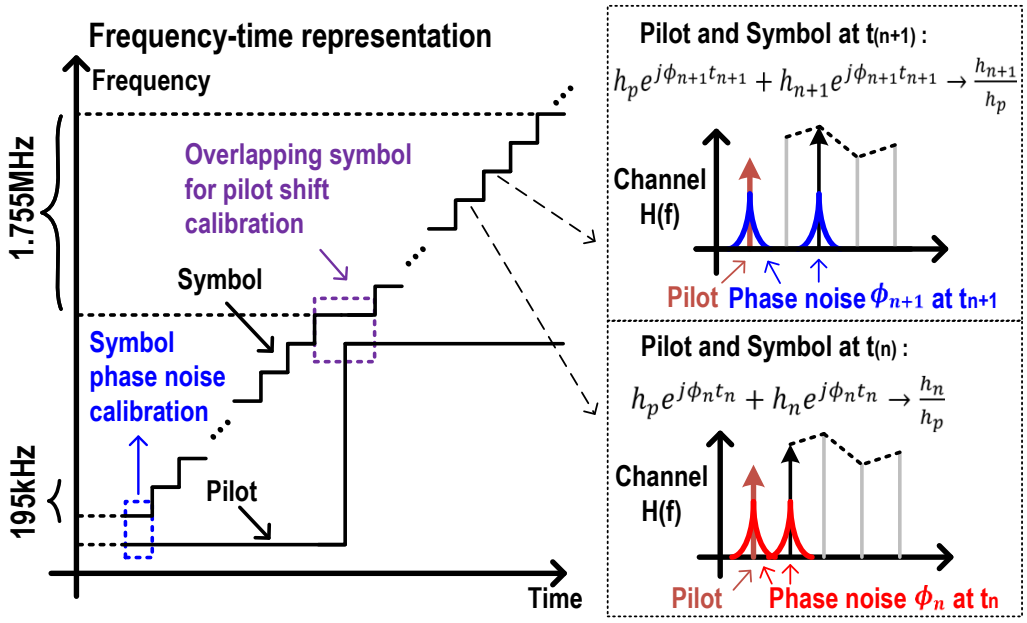


Figure 3.8: Pilot and data symbol hopping profile and phase noise tracking

drift on the received pilot symbol with other data symbols, as illustrated in Figure 3.8. The data symbol is adjusted by the observed pilot symbol drift amount over the reception window's duration, effectively counteracting the impact of phase noise of the PLL-less tag. Therefore, the *relative* phase of the data symbol to the pilot symbol is employed in the system to acquire the CFR/CIR result.

3.3.3.2 Window Stitching and CFR/CIR Estimation

Following the rectification of CFO and phase noise, the computation of the CFR for each anchor's localization symbols is initiated. This calculation transpires on a symbol-by-symbol basis and involves applying FFT to the received symbols during each localization hop. Subsequently, the CFR estimation for the received localization symbols from each anchor is derived by collecting the response at the assigned sub-carrier within the FFT output.

In deriving the CFR for the entire localization bandwidth, the computed CFR

symbols are combined to emulate the response obtained from a wideband signal. Nevertheless, a challenge arises due to a phase offset introduced by the free-running oscillator, which is distinct for each receiving window. While the oscillator frequency changes by increasing (or decreasing) the capacitor code, the phase would decelerate (or accelerate) instantaneously. Since the oscillator is free-running, the phase would not maintain coherence. However, maintaining phase coherence across all received tag symbols is crucial for effective CIR and T(D)oA estimation. To address this phase mismatch/offset issue, the system employs a strategy where the main anchor transmits the initial symbol of each receiving window by duplicating the last symbol in the preceding window without phase disruption. Figure 3.9 illustrates that a symbol is added as a repeated (overlapping) symbol at the end of every tag window. The phase difference between windows can be calculated by observing the overlapping symbol phase difference.

Integrating duplicated symbols and known pilot symbols across both windows enables estimating and correcting phase changes/offsets between consecutive receiving windows. This approach proves to be straightforward in terms of implementation and solution compared to conventional methods like phase retrieval algorithms [78, 79], which often necessitate complex numerical techniques and convergence assurances, along with a sufficiently high signal-to-noise ratio (SNR) for successful retrieval.

Figure 3.10 shows the before and after data symbol correction with phase noise correction and window switching. Subsequently, the CIR for each anchor-to-tag channel is estimated from the merged, phase-offset corrected CFR symbols via computation of the inverse FFT (IFFT). These derived CIRs for each anchor are then utilized to determine the ToA and TDoA for the anchors, a process pivotal for localization.

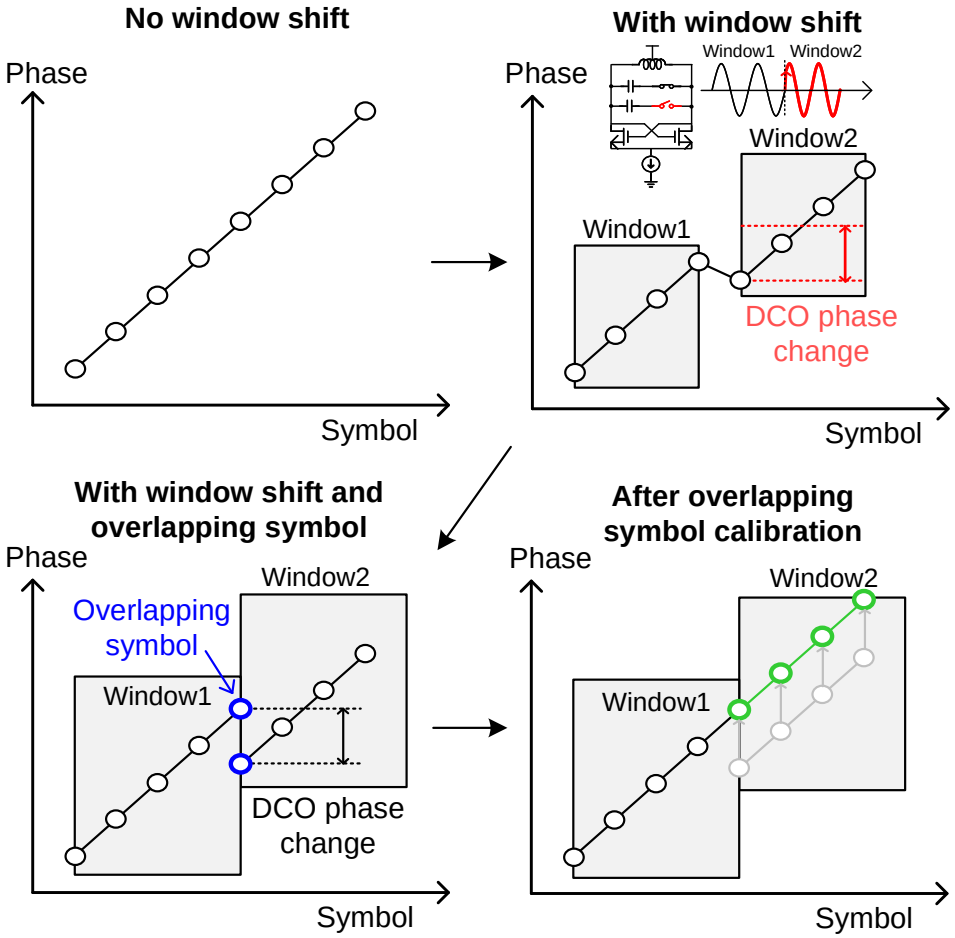


Figure 3.9: Window stitching and overlapping symbols

3.3.3.3 Neural Network ToA Estimation

The available RF bandwidth limits the localization distance resolution, as discussed in [80]. In a 100 MHz bandwidth context, the achievable resolution based on the CIR is approximately 3 meters. To enhance both the resolution and the precision of localization, a neural network is employed to estimate the ToA using an upsampled version of the computed CIR. The original CIR is subjected to a 10-fold upsampling, resulting in a potential enhancement of distance resolution, now reaching 0.3 meters when followed by a proper post-processing algorithm. In estimating ToA from the up-

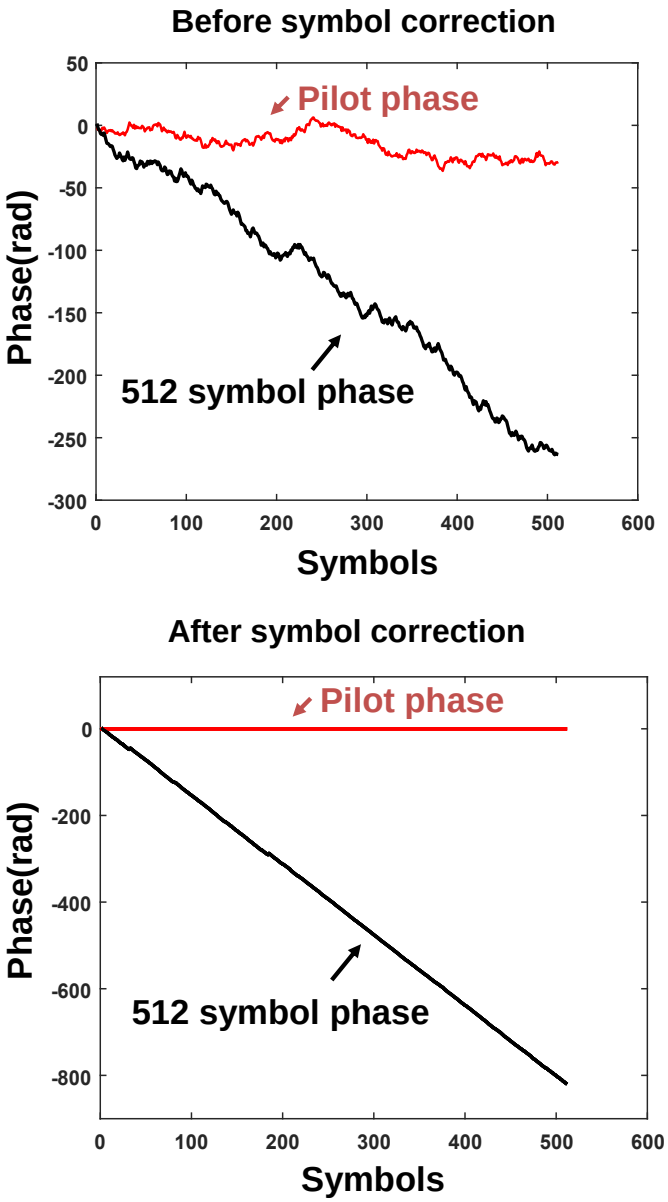


Figure 3.10: Before and after data symbol correction

sampled CIR of each anchor, a pattern-matching neural network with bootstrapping aggregation, initially introduced in RF-Echo [61, 62], is leveraged.

The neural network is trained to identify the characteristic pattern of the initial arrival path within the CIR. This strategy is grounded on the assumption that the first arrival path within the CIR aligns with the shortest direct trajectory (which is

through blocking objects in NLOS conditions), thus enabling accurate detection of the ToA. The neural network's training uses an exponential decaying channel model, detailed in [62], which spans various SNR scenarios and channel delay profiles. The neural network's performance surpasses that of classic super-resolution algorithms [62], achieving localization accuracy in the decimeter range. The TDoA is estimated by the ToA differences between anchors, which are then used for the 1D/2D localization process by multilateration.

3.4 Tag ASIC Chip Implementation

This section will go through the narrowband ASIC tag receiver design. The tag receiver is purposely designed to accommodate the proposed localization system. It features a narrowband, PLL-less, crystal-less, low-IF I/Q receiver with a digitally controlled oscillator (DCO) executing frequency hopping. Unlike conventional fully-armed receivers, the receiver is exposed to significant RF impairments, like CFO, SFO, phase noise, etc. However, those impairments are tackled by a novel signal processing technique along with a custom communication protocol. In return, the tag receiver, fabricated in a 55nm CMOS process, can achieve a low power consumption of 3.9 mW and a small form factor (single RFFE chip) with a high sensitivity of -115 dBm. It boosts the localization system performance to achieve long-range operation of 621 meters (LOS) with a decimeter accuracy of 0.6 meters.

3.4.1 Receiver Architecture

With the emphasis on a low power and simple structure receiver front-end for the tag, the receiver building blocks are designed with the power-optimized structure to convert the RF signals to baseband signals. The receiver consists of a narrowband input matching network, a single-end low-noise amplifier (LNA), an I/Q passive mixer, a trans-impedance amplifier (TIA), and a band-pass filter (BPF). The LO frequency

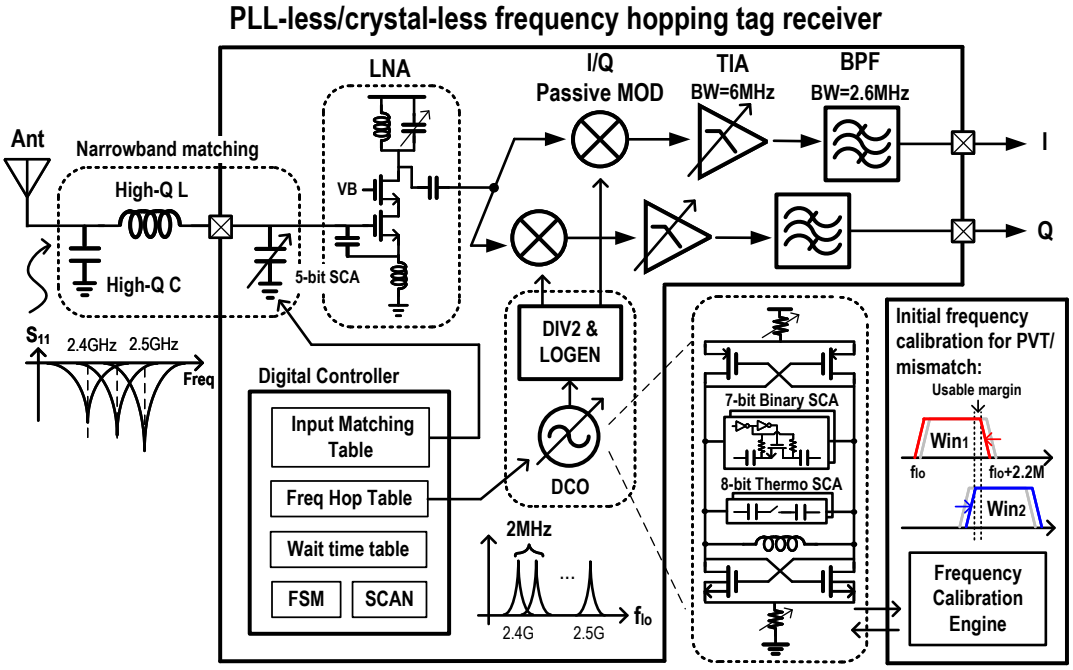


Figure 3.11: Receiver structure overview

is generated through the free-running digitally-controlled oscillator (DCO) followed by a divide-by-2 divider (DIV2) and a 25% duty-cycle LOGEN I/Q waveform. Figure 3.11 shows the overall structure of the receiver.

The receiver will perform 64 window frequency hopping between 2.4 and 2.5 GHz with a baseband window bandwidth ∼1.6 MHz. The digital controller executes the frequency hopping to march through frequency codes stored on on-chip memory. The frequency table and the wait time table determine the frequency hopping time and frequency. The frequency hop table stores the information about the calibrated frequency code, while the wait time table stores the information about fine-tuning the absolute hopping time. The frequency code is well-calibrated through the off-chip measurement path with post-processing to select the target frequency. While changing the LO frequencies, the digital controller also tunes the input matching network center frequency to further narrow the bandwidth and the matching power loss. The baseband bandwidth is calibrated to cover the overlapping symbol between two

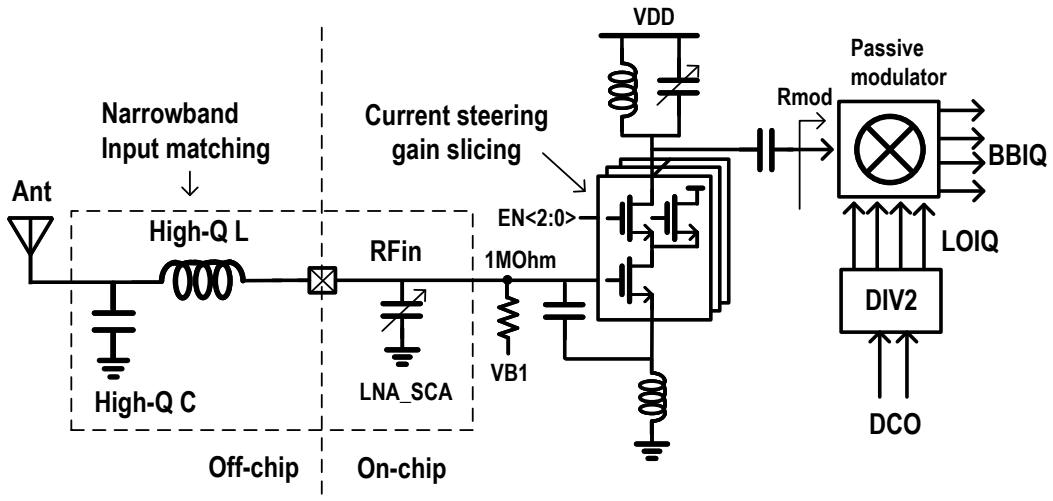


Figure 3.12: Narrowband RFFE circuits with high-Q input matching network

windows and reserved bandwidth margin to overcome process-voltage-temperature variation (PVT).

3.4.2 Receiver Front-end Circuits

Narrowband LNA consists of a narrowband input matching network, inductive-degenerative LNA, current-steering gain slicing, and the output LC network. The overall schematic is shown in Figure 3.12.

The input matching network uses off-chip high-quality L and C to minimize the matching power loss and boost the voltage gain to g_m device. The input matching also works with a tunable on-chip capacitor, which can be used as coarse channel selectivity for a narrowband receiver. The source inductance degenerates the common-source thermal noise, making the noise primarily dominated by gate inductance's resistance. With the off-chip high-Q (50) gate inductance, the overall noise figure of the LNA can be enhanced to around 3 dB in pre-simulation. The current steering with a cascade device can control the LNA gain, maintaining the input matching condition while effectively implementing the binary current/g_m slicing. The LNA gain is implemented

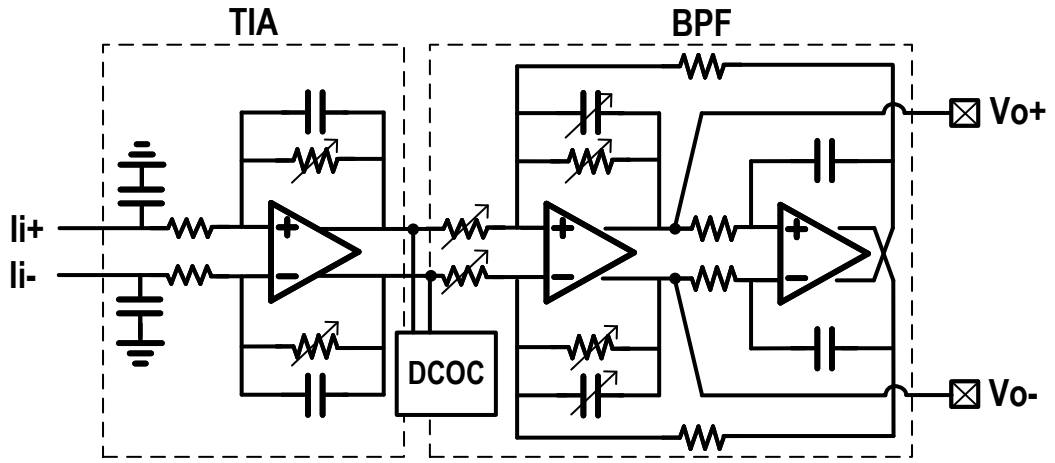


Figure 3.13: Receiver baseband circuits schematic

with three gain gears for high/mid/low gain. The output network is co-designed with the modulator (MOD) to optimize the current gain efficiency [81] [82]. Due to the low-quality factor of the output matching network, the tunable capacitor is calibrated to center frequency once and maintains the same value across the frequency hopping range.

The modulator is designed with a passive mixer structure with low power consumption and low flicker noise at low-frequency offset. The passive mixer fits the narrowband application as flicker noise is critical to narrowband low-IF receivers.

3.4.3 Receiver Baseband Circuits

The receiver baseband circuits consist of a trans-impedance amplifier (TIA), a band-pass filter amplifier (BPF), and a DC-offset cancellation circuit (DCOC), as illustrated in Figure 3.13

The TIA is essential to convert the input current from the MOD to the output voltage for BPF. It also provides 1st-order low-pass filtering to suppress out-of-band interference. The TIA bandwidth is intentionally set to be wider than the subsequent

BPF stage to prevent band-edge frequency drooping and reduce the sensitivity to bandwidth variation. The TIA is designed with multiple gain gears, which is achieved by adjusting the resistor values. It offers a range of 47 dBΩ to 65 dBΩ with 6 dB/step.

The local oscillator noise could down-convert to the baseband, exhibiting $1/f^3$ and $1/f^2$ noise response. Unlike the conventional receiver equipped with a PLL to suppress the oscillator noise, the free-running oscillator in our structure is more susceptible to low-frequency noise. Therefore, following the TIA, we must apply BPF to provide high-pass filtering at low frequency. The high-pass response eliminates the low-frequency noise, such as the flicker noise of the MOD/TIA, and the flicker and thermal noise of the free-running oscillator.

The BPF is implemented with a Tow-thomas-biquad structure. The biquad structure has more flexibility in adjusting the resistor and capacitor values, allowing the bandwidth and damping factor to be adjusted independently according to different settings. The BPF can provide additional gain gears with 12/18/24 dB. The biquad structure has both low-pass and band-pass signals. The band-pass signals are output signals, while the low-pass signals are used for DC offset correction. The DCOC comprises a 5-bit resistor array to adjust the differential current to correct the DC offset error.

3.4.4 Digitally-Controlled Oscillator

The digitally-controlled oscillator (DCO) is designed with a class-B push-pull LC oscillator structure, as illustrated in 3.14. We utilize a 7-bit binary switch-cap array (SCA) for coarse frequency tuning and an 8-bit thermometer SCA for fine frequency tuning. We also integrate an on-chip low-dropout regulator (LDO) to mitigate the supply sensitivity.

The coarse frequency tuning is used for initial frequency acquisition, which centers the discrete frequency. The fine frequency tuning is used for enhancing the linearity

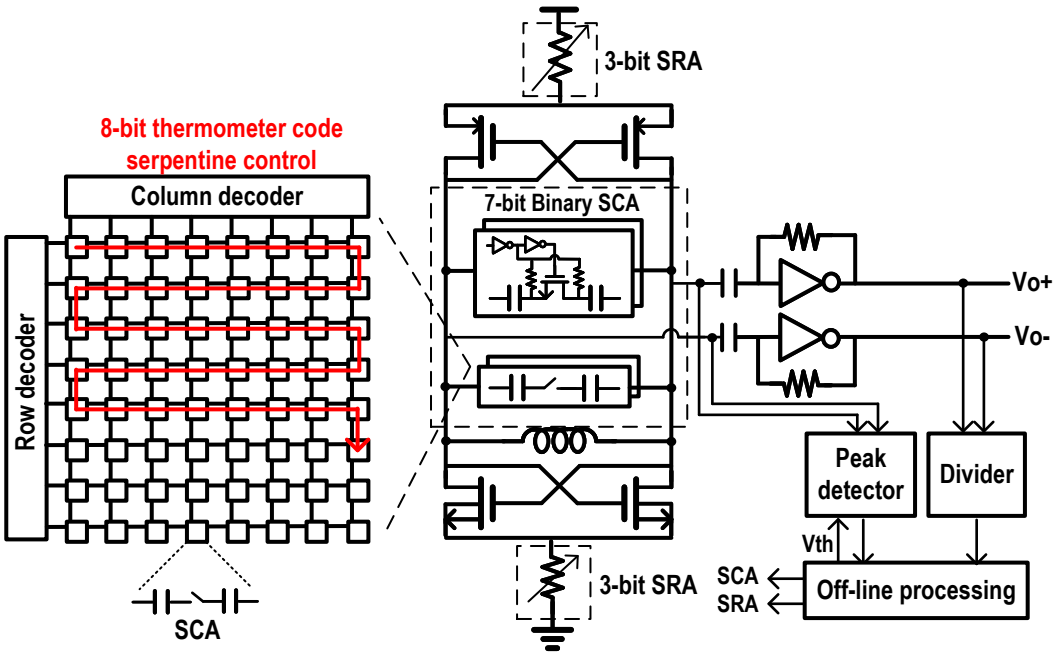


Figure 3.14: Digital-controlled oscillator

of the SCA. It is implemented with a thermometer code combined with a serpentine layout style. Frequency calibration is performed by measuring the divided-down clock frequency with frequency-counting equipment. The coarse frequency resolution is around 5 MHz/step, while the fine frequency resolution is about 200 kHz/step. The overall DCO tuning range can cover PVT from 4850 MHz to 5200 MHz, which is wide enough for the target frequency range.

The DCO current is controlled by a 4-bit switch-resistor array (SRA). The resistor control method can reduce the flicker noise contribution compared to the current-source control method. The output amplitude of the DCO is well-calibrated. The calibration is completed by monitoring the output amplitude through the peak detector with a threshold value and then adjusting the SRA settings.

3.5 Narrowband Localization System Integration

3.5.1 Main and Reflection Anchors

The localization system anchors were implemented using the Universal Software Radio Peripheral (USRP) X310. The USRP X310 features two extendable wide-bandwidth RF daughtercard slots covering a frequency range from DC - 6 GHz and a customizable Kintex-7 FPGA [83]. Each of the two channels on the USRP X310 was configured for full duplex operation at separate transmitting and receiving carrier frequencies, covering up to 160 MHz baseband wideband when used with the UBX-160 daughterboards [83]. The UHD software C/C++ API controls the parameters of the USRP hardware and can also be used to build custom applications from a host computer. Still, there are sampling rate, hopping rate, and latency limitations [83] with such software-based applications. The system has strict real-time deterministic-latency control requirements on the transmission and processing of symbols on the (reflecting) anchors for a successful localization since it hops from one frequency to another across a wide bandwidth. As a result, the anchors were implemented using Verilog, and the modules were ported to the FPGA of the USRP for hardware execution. With this design, the anchor modules have direct access to the digitizers on the USRP X310 and run at the FPGA clock rate of 200 MHz.

3.5.2 Tag Receiver

The tag implementation is based on the low-power RF receiver ASIC chip, and it is controlled by the USRP X310, which is equipped with the UBX-160 daughterboard on one of the channels and the LFRX daughterboard on the other channel. The LFRX daughterboard can prodive from DC to 30 MHz [84] bandwidth and it is used to buffer baseband signals from the ASIC receiver, which only contains the RF analog front-end, to 14-bit ADC inside USRP X310. The channel with the UBX-160

daughterboard is tuned to the 2.4 GHz band to detect the synchronization signal from the main anchor using the real-time detection module implemented on the FPGA. The USRP controls the hopping of the receiver carrier frequency after detecting the synchronization signal by sending the control word to the ASIC receiver. The baseband I/Q samples from the ASIC receiver are captured by the USRP and streamed to a host computer at a 12.5 MHz rate. These samples are processed offline for localization of the tags. The datapath of the signal processing on the tag is shown in Figure 3.7.

3.5.3 Synchronization

The localization system requires time synchronization between the anchors and the tags to signal the start of the localization. Since the hopping pattern is known to both the tags and the reflecting anchors, successful detection of the synchronization within appropriate timing bounds (e.g., cyclic prefix length) is necessary for proper hopping control for successful localization. The synchronization packet was designed using a repeated pseudo-noise (PN) sequence due to the good autocorrelation properties for detection in the presence of noise [85]. The PN sequence bits are modulated using BPSK, which provides a better performance for detection than other non-coherent modulations in noisy multi-path rich environments [86], and its length is determined to guarantee that the limitation of the system is not from the synchronization. The synchronization signal is detected by autocorrelating throughout the PN sequence. An algorithm that computes the autocorrelation metric using reduced multipliers [87] is used since the FPGA does not have enough multiplier resources for a full autocorrelation implementation that allocates one multiplier per autocorrelation sample.

3.5.4 Sampling Frequency Offset Correction

The clocks used in USRPs are derived from independent oscillators, and they may introduce sampling time offsets during data processing due to inherent deviations. These offsets can lead to symbol phase rotations affecting the accuracy of the localization system. Since the clocks are responsible for sampling the received symbols and processing the data in both the anchors and the tags, any discrepancies in the sampling clock frequencies can result in timing and symbol phase misalignment. The localization symbols would be transmitted from different sampling domains in the system, which involves the main anchor, reflecting anchors, and tag anchor. To mitigate the impact of sampling offsets on localization accuracy, aligning these symbols to a single sampling domain as closely as possible is crucial. Correcting the sampling offsets involves estimating the timing discrepancies between the different sampling domains and applying adjustments. This correction is typically performed by aligning the timing of the reflecting anchors to the main anchor's domain.

There are various methods to correct sampling time offsets. A typical method involves estimating the sampling offset and resampling the signals to the desired sampling clock domain [88]. However, in the case of the direct digital synthesis (DDS) system used in our implementation, the resolution of the phase and memory limitations of the FPGA makes it practically infeasible to implement the lookup table (LUT) required to compensate for subtle timing deviations accurately. To overcome these limitations, we developed a simple fractional resampling algorithm specifically for the reflecting anchors in the data path. This algorithm ensures that the symbols transmitted by the reflecting anchors align with the timing of the main anchor's symbols during the processing stage, as described below.

To compensate for the sampling clock deviation between the main anchor and the reflecting anchor, we estimate the deviation as $\pm\Delta t$, which is different for each sample. This deviation represents the difference in sampling time between the two

anchors, where the sampling time for the main anchor is denoted as T_s and the sampling time for the reflector is $(T_s \pm \Delta t_s)$. To maintain alignment in the reflecting anchor's processing path, we approximate the fractional (non-integer) sample index offset using the parameter R, which is a constant regardless of the sampling time. The relationship between the sampling time deviation and R is given by the equation

$$\frac{\Delta t_s}{T_s} = \frac{1}{R}. \tag{3.1}$$

To estimate the sampling deviation between two anchors in the system, a pure tone is transmitted during the calibration phase from the main anchor and received at the reflecting anchor. The carrier frequency offset calculated in the reflecting anchors is directly proportional to the sampling clock deviation. This is because the same crystal reference on the USRP drives carrier frequency and the FPGA clock. While this estimation provides a reasonable estimate of the sampling deviation, further calibration is performed to refine the accuracy. The calibration involves sweeping the value of R, which was computed based on the frequency offset estimation, and evaluating the resulting phase shift of the received tone. The calibration process aims to identify the R value that minimizes the phase shift throughout the duration of the localization symbol received at the tag. By iteratively adjusting the R value and observing the phase shift, the calibration process aims to find the best approximation that minimizes the deviation in the timing alignment between the main anchor and the reflecting anchor.

Once R is determined, the compensation process involves repeating the mixing at the sampling instance once for every R samples when the reflector clock is faster than the main anchor clock. Conversely, when the main anchor clock is faster than the reflector clock, a digital mixing step is skipped after every R samples. The fine calibration process is necessary to refine the residue error. This is done by inserting

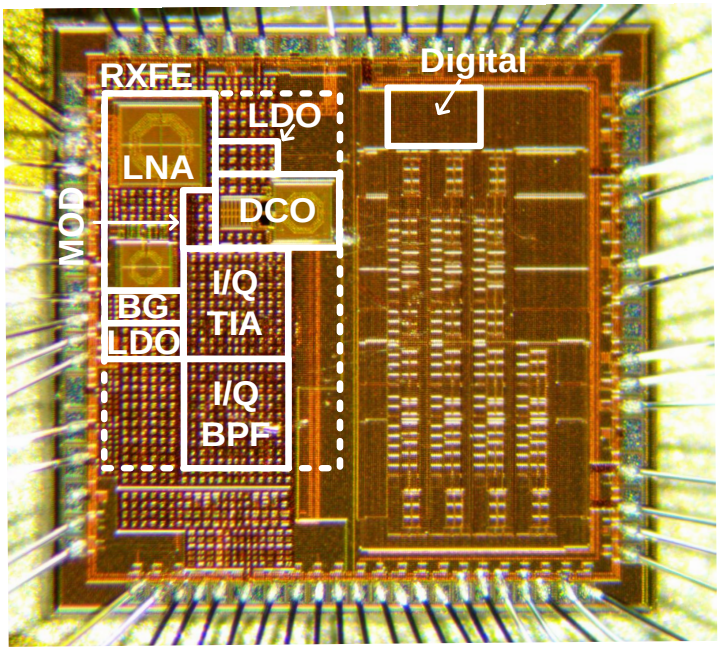


Figure 3.15: Die micrograph of the $0.7\times1.2mm^2$ 55nm CMOS tag receiver front-end

skipped samples while generating DDS signals.

3.6 Narrowband Localization System Measurement

3.6.1 ASIC Chip Measurement

The proposed tag receiver is fabricated using the 55 nm DDC process technology provided by United Semiconductor Japan CO., Ltd. The die micrograph is shown in Figure 3.15 and occupies 0.85 mm^2. The receiver signal path is shown on the left-hand side of the chip. The total receiver front-end consumes 3.9 mW under supply 0.9V. A thorough test is measured in the lab.

Figure 3.16 shows the receiver input matching, S_{11}, with external high-quality L and C, and it shows how varying the capacitance value adjusts the input matching's center frequency. The input matching is deliberately detuned at the band edges, specifically at 2.4 GHz and 2.5 GHz, to reduce interference from out-of-band signals.

Figure 3.17 shows the measurement of the receiver's noise figure performance at the different gain levels. The noise figure is around 6.5 dB at the maximum gain; while lowering the gain, the noise figure increases up to about 25 dB. The noise figure remains relatively stable across the 2.4 to 2.5 GHz frequency range.

Figure 3.18 shows the free-running oscillator phase noise at 4.9 GHz. The resistance has been fine-tuned to maintain an adequate signal amplitude while minimizing power consumption as much as possible. It shows a phase noise of -85 dBc/Hz at a 100 kHz offset with a current of 800 uA.

Figure 3.19 shows the DCO frequency hopping profile from 2.4 to 2.5 GHz. It achieves ∼0.3 us settling time for the required ∼3.2 MHz frequency hop (∼1.6 MHz in LO frequency). This simple structure significantly reduces design complexity compared to more complex PLL designs that accomplish fast frequency hopping.

3.6.2 Distance Measurement

3.6.2.1 Measurement Setup

A 1-D localization system was evaluated in various LOS and NLOS conditions. Three distinct tests were carried out: indoor, outdoor, and indoor-outdoor.

The known locations of the main and reflecting anchors serve as reference points for the localization system to enable the estimation of the 1-D location of the mobile tag. To measure the distance, we move the reflecting anchor position while fixing the tag and main anchor positions. This particular setup is intended to stress the system in two ways. First, the main-to-reflection anchor link experiences the longest distance, exposing the anchor-to-anchor radio performance. Second, the link from the reflecting point to the tag encounters the worst signal-to-noise ratio (SNR) as the signal travels through the round-trip channel, resulting in significant degradation.

For anchors, Vert2450 / RO5810NF antennas [89] were employed for the 900 MHz/ 2.4 GHz/ 5.8 GHz band. To mitigate ground reflections [90, 91], the antennas

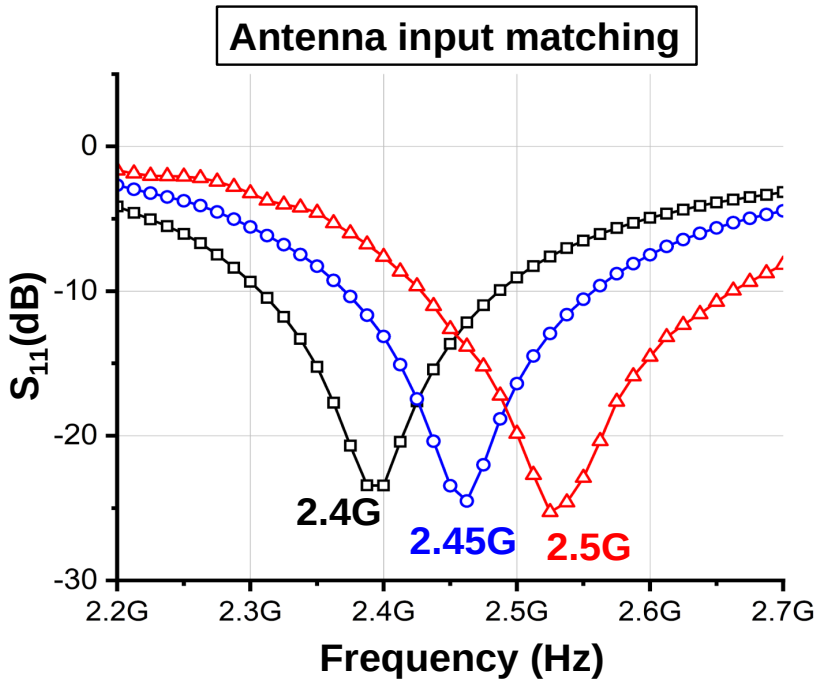


Figure 3.16: Measured S_{11} with different input matching settings

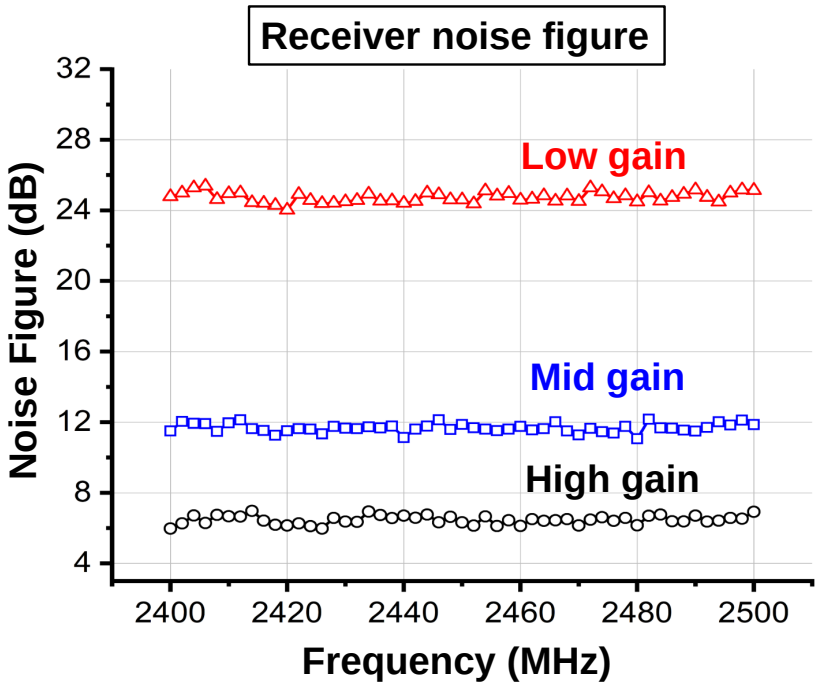


Figure 3.17: Measured noise figure with different gain settings

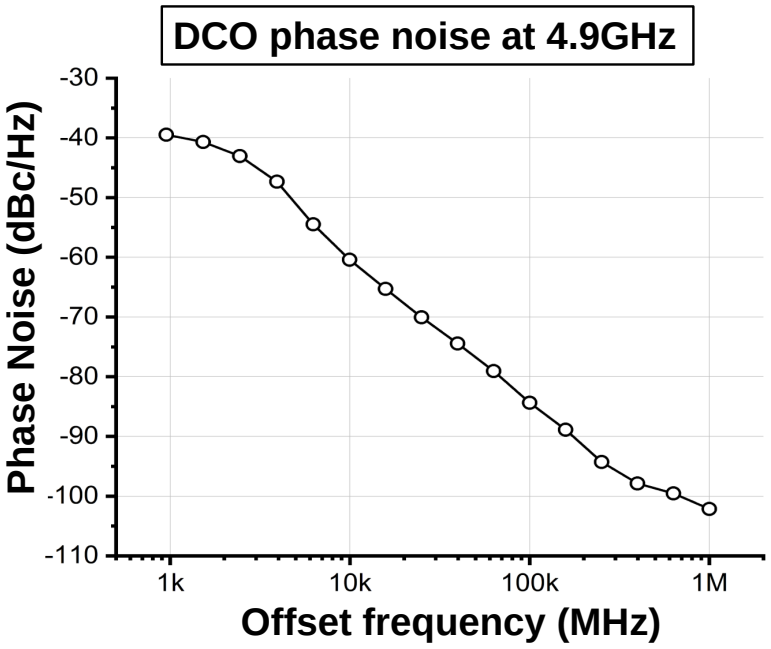


Figure 3.18: Measured free-running DCO phase noise

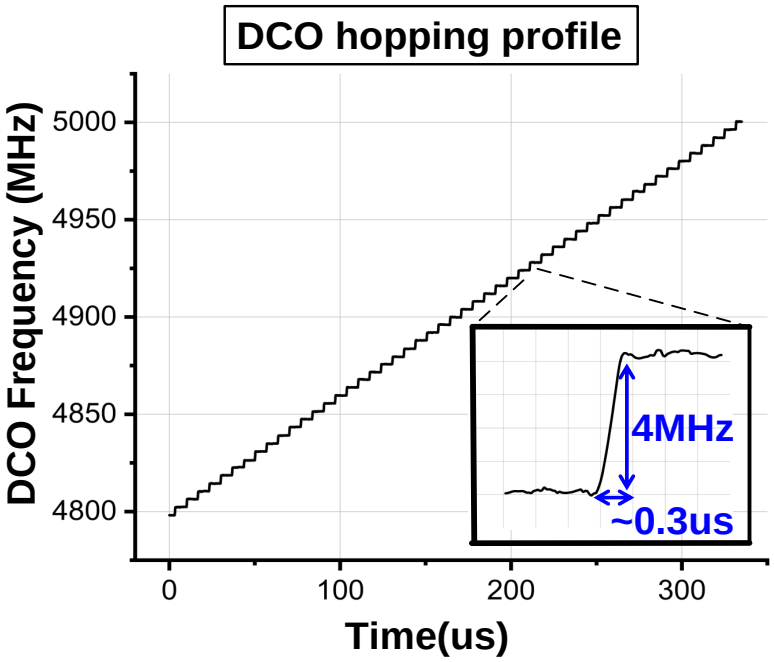


Figure 3.19: Measured DCO hopping profile

were positioned on tripods with 1.5 meters height. External power amplifiers [92] were used to amplify the transmit signals from the anchors (main and reflecting anchors). The USRP with an external power amplifier can provide ∼15 dBm output power. The reflecting anchors utilized an additional low-noise amplifier [93] for the reception of the main anchor signals. Figure 3.20 shows the overall setup. The ground truth locations were measured using a Leica E7500i laser distance meter [94]. The localization error was measured by the distance from the estimated position to the ground truth position.

Figure 3.21 presents the measured spectrogram of the one anchor and tag scenario. In this scenario, each window includes a pilot symbol that remains constant and data symbols that undergo frequency hopping across nine different symbols.

Figure 3.22 presents the measured spectrum of the two anchors and one tag receiver scenario. In this scenario, each window would observe pilot and data symbols from the main and reflecting anchors. Because the main anchor is closer to the tag receiver than the reflecting anchor, its signal shows a greater strength in the spectrum. The pilot tone, which remains constant throughout the window's duration, exhibits a higher signal strength than other data symbols. In this setup, the reflecting anchor introduces a frequency shift of ∼50 kHz.

Figure 3.23 illustrates CIR measurements from the main and reflecting anchors at a specific location. The blue line represents the path from the main anchor to the tag receiver, while the red line represents the path from the reflecting anchor to the tag receiver. The tag's location can be determined using the TDoA information with the known positions of the main and reflecting anchors.

3.6.2.2 Indoor-Outdoor Test

The indoor-outdoor test was designed to evaluate the system's performance in scenarios where the reflecting anchors are positioned outside the building while the

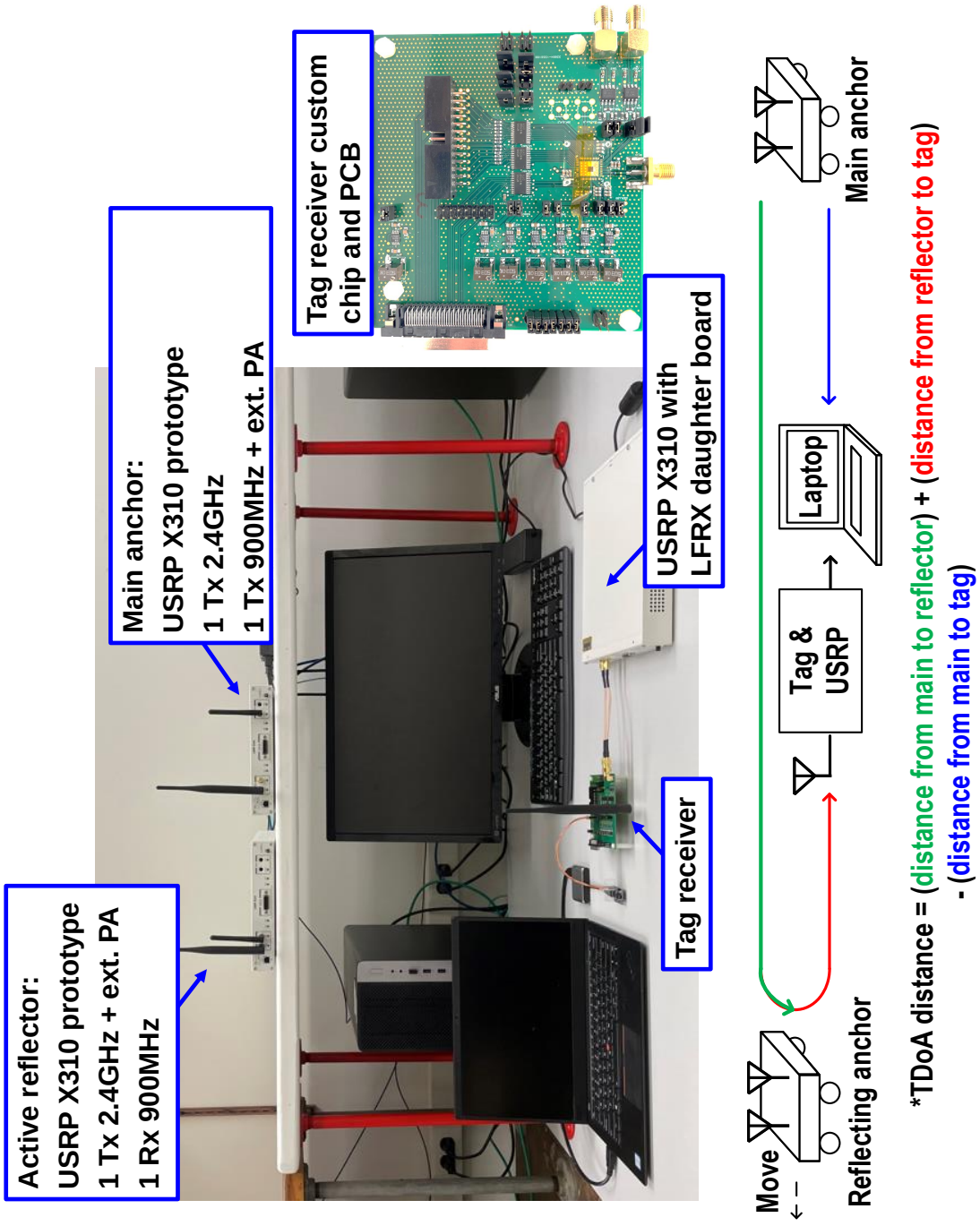


Figure 3.20: Localization system measurement setup

tag and main anchor are inside. This test scenario is particularly relevant for public safety applications, such as firefighter operations, where it is crucial to track the positions of individuals inside a building while the anchors remain outside.

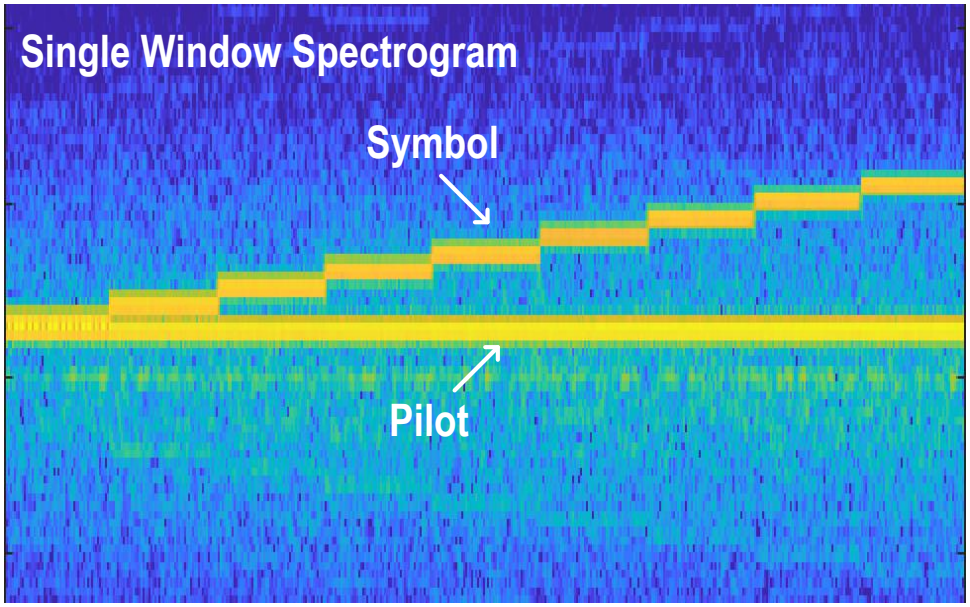


Figure 3.21: Measured one anchor per window spectrogram

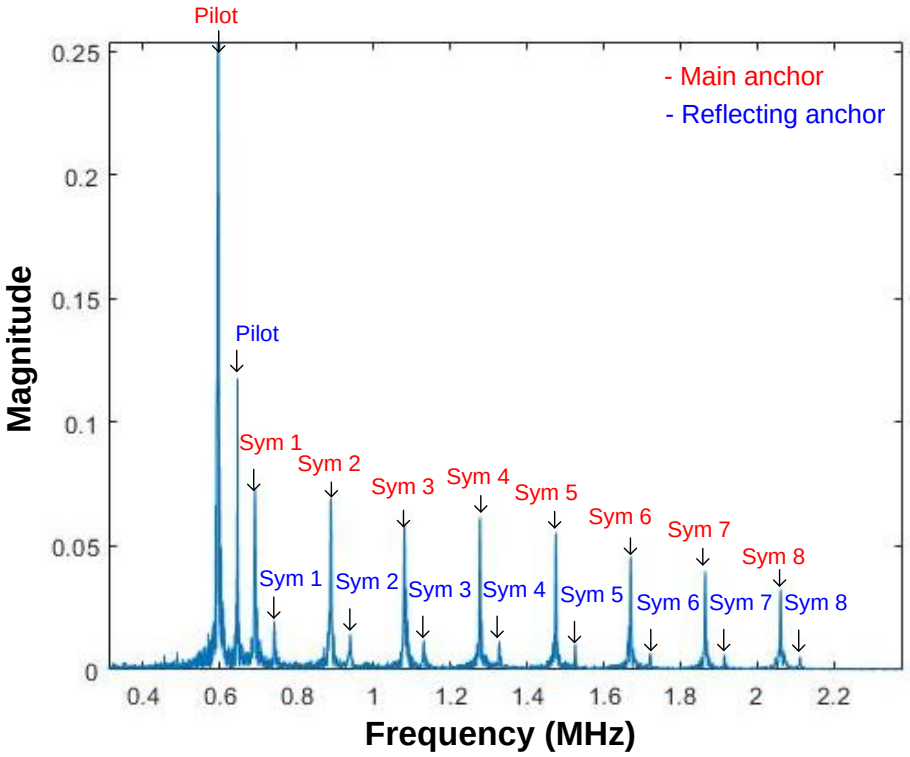


Figure 3.22: Measured two anchors per window spectrum

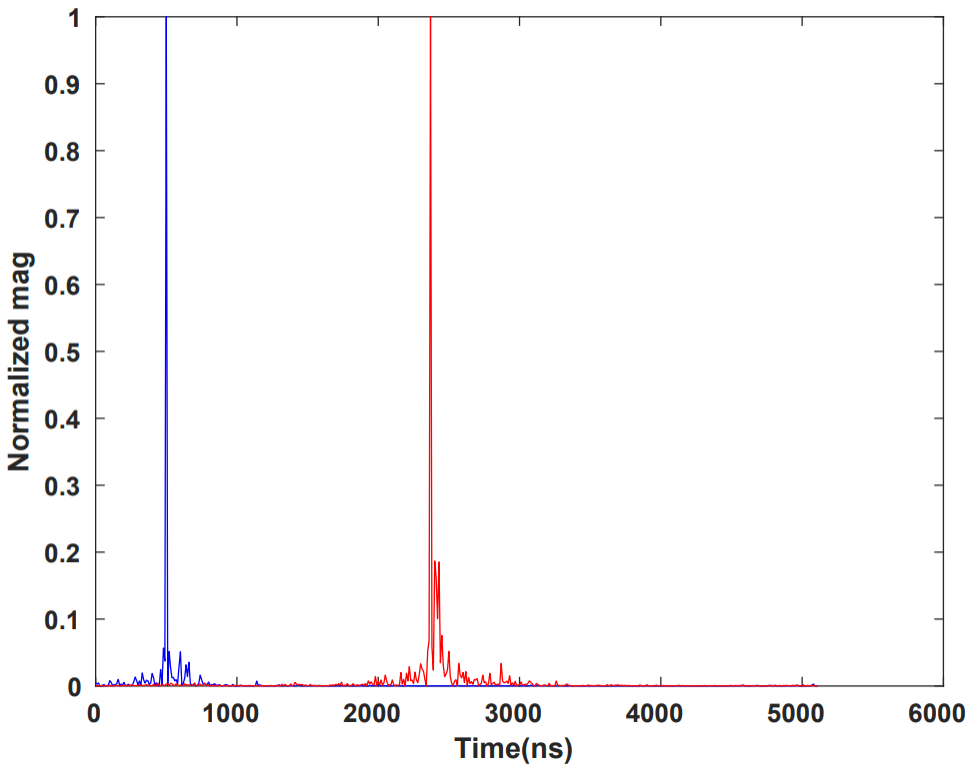


Figure 3.23: Measured two anchors CIR responses

Figure 3.24 shows the measurement setup. We moved the reflecting anchor position while fixing the tag and main anchor inside the building. The main anchor is indoors on the 1st floor of the building, 60 meters behind the front door, and the tag is 48 meters behind the front door. The reflecting anchor was moved from 22 to 309 meters to demonstrate the NLOS scenario.

Figure 3.25 displays the tag's estimated positions and ground truth locations and illustrates the localization errors performed at each position, providing insights into the accuracy of the system's estimates. We measured 7 locations, each with 100 samples, to get the statistical result. The system can achieve a maximum of 309 meters NLOS localization distance. The worst median error was observed at location 5, with a value of 1.74 meters. On the other hand, location 6 exhibited the best median error, with a value of 0.6 meters. These results highlight the feasibility and

effectiveness of the system in environments where the anchors are positioned outside while the tags can self-localize indoors. This capability suits a wide range of public safety applications where accurate localization within buildings is essential.

3.6.2.3 Indoor Test

The indoor test aims to evaluate the performance in indoor environments characterized by multipath effects and signal attenuation. These conditions pose additional challenges for accurate localization. The test was conducted on the 1st floor atrium of the school building with $60 \times 37\ m^2$, as illustrated in Figure 3.26. The indoor area featured concrete walls, glass windows, and wooden doors for the large rooms (classrooms, labs, and offices). This configuration introduced much multipath interference and blocked LOS paths between the anchors and the tag.

Figure 3.27 shows the tag's estimated positions and ground truth locations and illustrates localization errors performed at each position, providing insights into the accuracy of the system's estimates. We measured 6 locations, each with 100 samples, to get statistical results. The worst median error was observed at location 3, with a value of 0.57 meters. On the other hand, location 1 exhibited the best median error, with 0.31 meters.

3.6.2.4 Outdoor Test

The outdoor test was designed to evaluate the performance in an open-air environment, where the LOS between the anchors and the tag was mostly unobstructed. Figure 3.28 illustrates the positions of the anchors and tag testing at the school campus. We fixed the tag and main anchor locations while moving the reflecting anchor from 181 to 621 meters. The outdoor LOS environment still experiences terrain fluctuations a little.

Figure 3.29 shows the tag's estimated positions and ground truth locations and

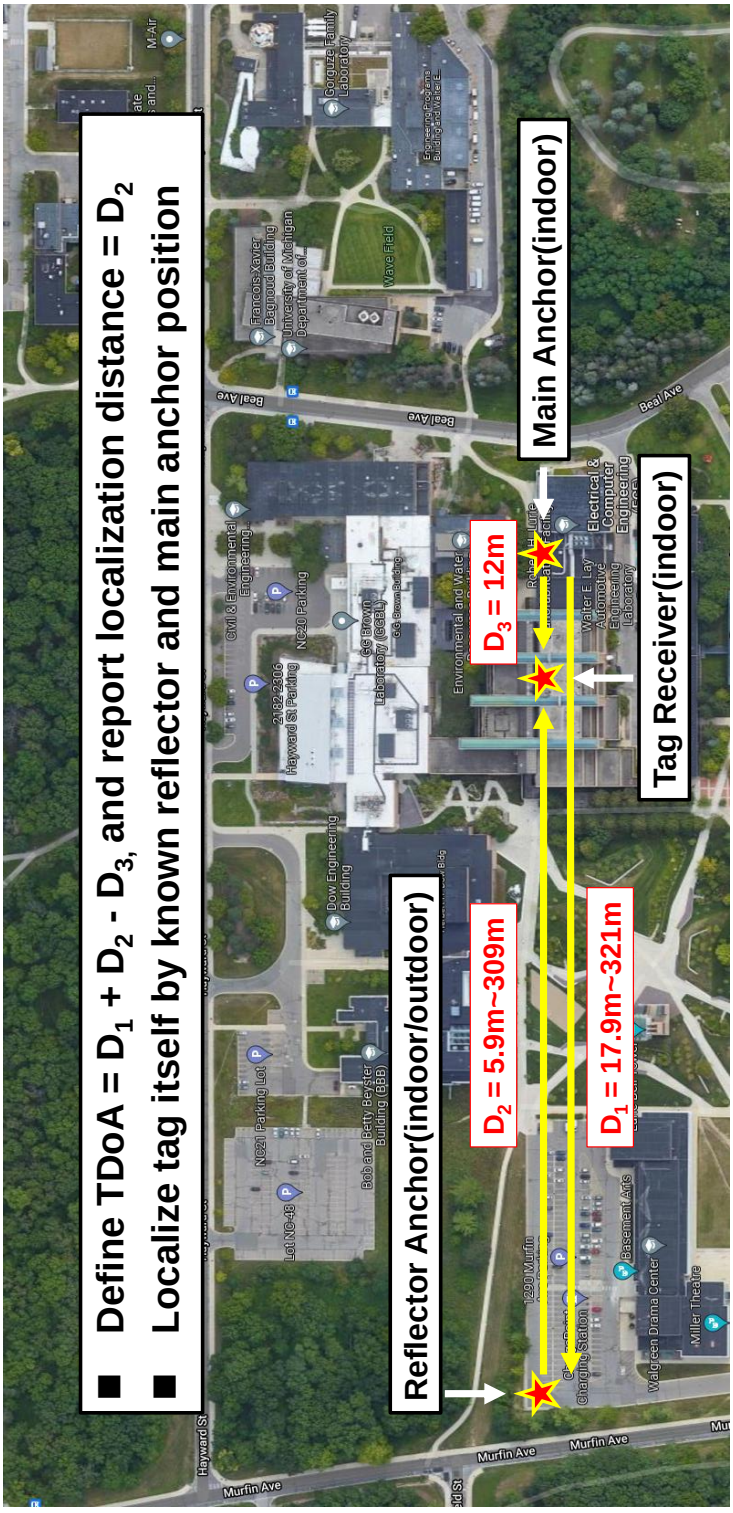
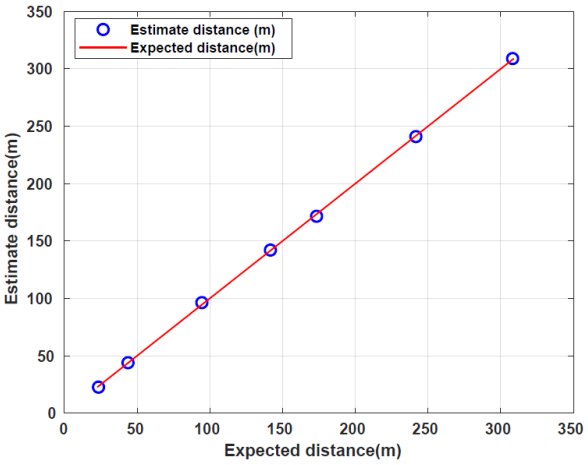


Figure 3.24: Indoor-outdoor NLOS measurement setup



- Tag and main indoor, reflector outdoor
- Each location : 100 samples
- Each distance result is median of 10 CIRs
- Max. reflector to tag ~309m

Distance (m)	Median abs. error over 10 results (m)
22.6	0.76
43.9	0.29
96.3	1.7
142.1	0.48
171.6	***1.74***
241	0.6
309.0	1.24

Figure 3.25: Indoor-outdoor NLOS measurement result

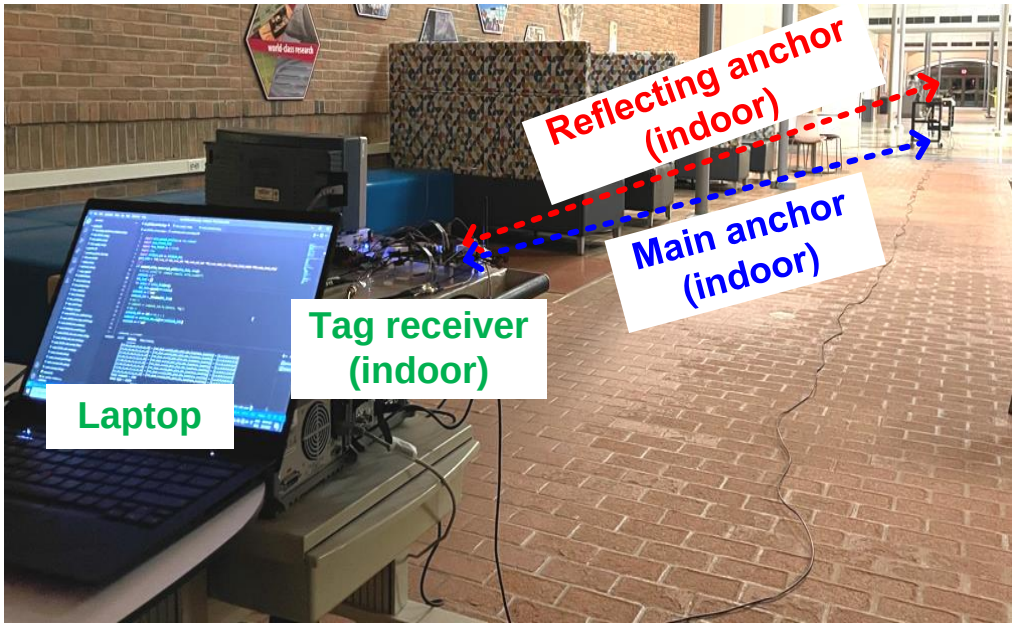
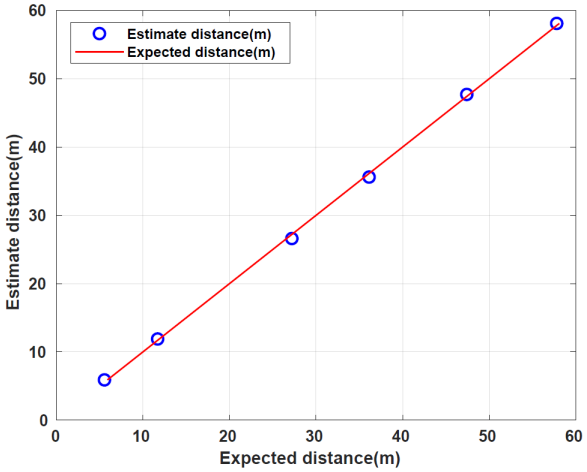


Figure 3.26: Indoor multi-path rich environment measurement setup

illustrates localization errors performed at each position, providing insights into the accuracy of the system's estimates. We measured 7 locations, each with 100 samples, to get statistical results. The system can give a maximum of a 621 meters LOS localization distance. The worst median error was observed at location 3, with a



- **Tag, main, reflector all indoor**
- **Each location : 100 samples**
- **Each distance result is median of 10 CIRs**
- **Max distance limited by setup**

Distance (m)	Median abs. error over 10 results (m)
5.9	0.31
11.9	0.37
26.6	**0.57**
35.6	0.56
47.7	0.38
58.1	0.36

Figure 3.27: Indoor multi-path rich environment measurement reuslt

value of 0.67 meters. On the other hand, location 5 exhibited the best median error, with a value of 0.26 meters. The maximum distance is limited by the available received signal power and the availability of LOS distance near the school campus. The reflecting anchor to the tag link suffers severe power attenuation on both sides.

3.6.3 Performance Comparison

The system performance is summarized in Figure 3.30. Compared with other ASIC chips used for localization application [95–98], the proposed system achieves a much longer range, a maximum of 621 meters for LOS condition and 309 meters for NLOS condition, with a low power consumption of 3.9 mW in tag receiver. [95] uses IR-UWB technology with a transceiver chip to achieve high accuracy of 1.2 mm at 4 meters distance and support a maximum 9 meters distance with 118 mW. Such high power consumption and short distances do not fit long-range IoT location services. [97] demonstrates that multi-tone technique [99] with wide bandwidth can be used for localization, but the power consumption and localization range still fail to reach our targets. WiFi and BLE-based localization systems usually demonstrate system-level solutions to achieve backward compatibility with the existing devices and

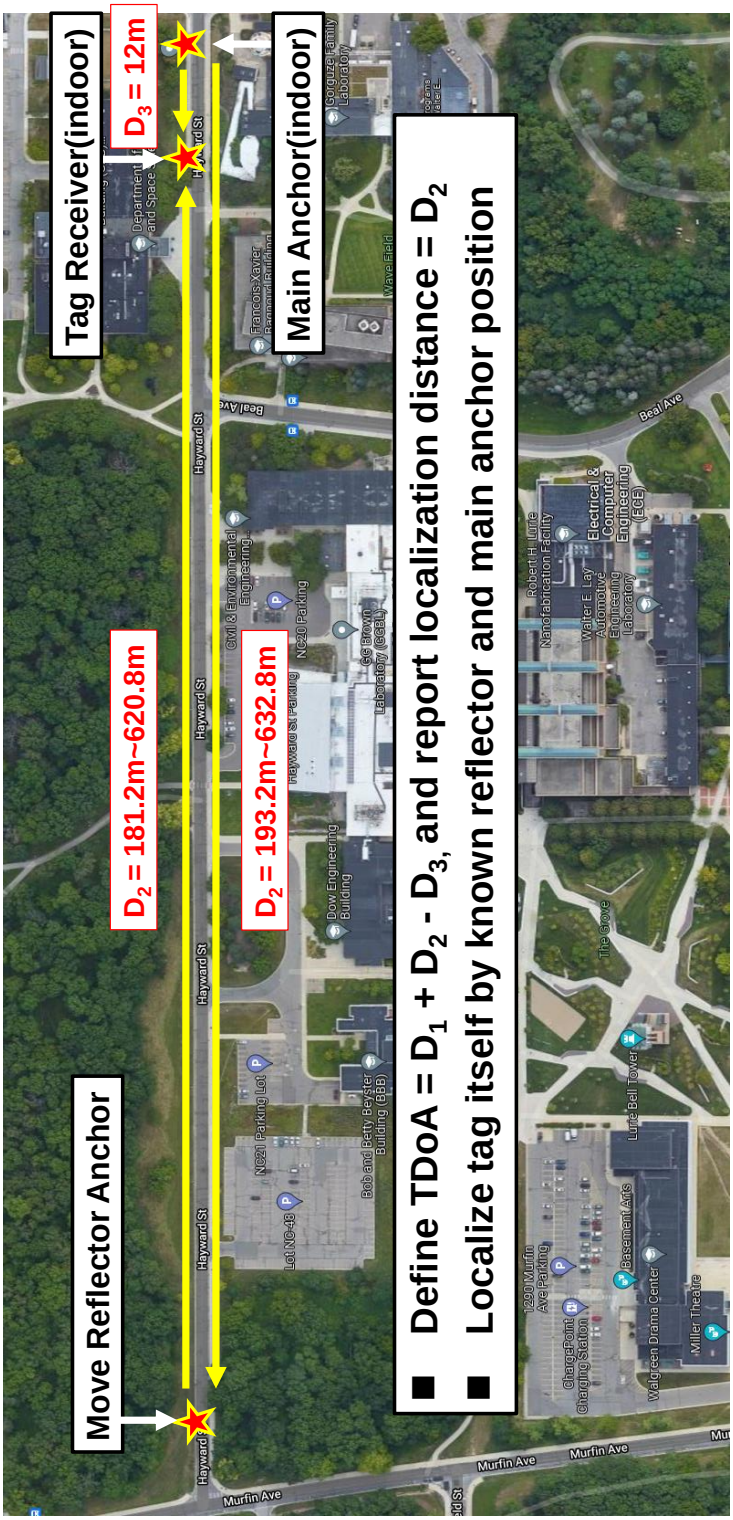
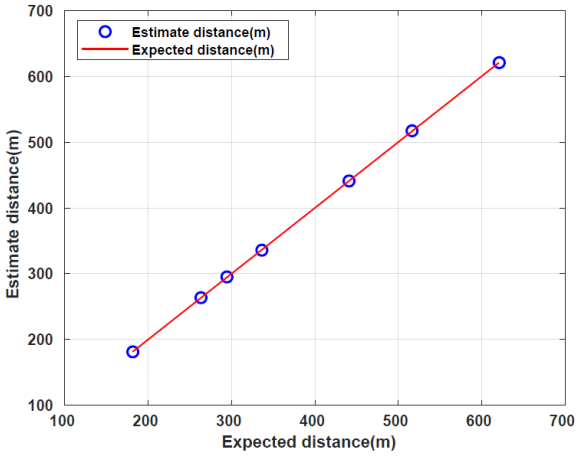


Figure 3.28: LOS distance measurement setup



- **Tag, main, reflector all outdoor**
- **Each location : 100 samples**
- **Each distance result is median of 10 CIRs**
- **Max. reflector to tag ~621m**

Distance (m)	Median abs. error over 10 results (m)
181.2	0.44
263.5	0.28
295.1	***0.67***
335.7	0.65
440.9	0.26
517.2	0.48
620.8	0.47

Figure 3.29: Outdoor LOS measurement result

infrastructure. [97] uses ASIC tag with phase-based rangeing to show the backward compatibility to the BLE system. Although it demonstrates a low power of 5.3 mW with 20 meters ranging distance in a low bandwidth of 80 MHz, the ranging distance is still far behind our target. Compared with the state-of-the-art narrowband receiver only designed for the NB-IoT application, [98, 100], the proposed tag receiver demonstrates a similar power consumption level.

3.7 Summary

A novel narrowband RF localization system has been proposed, designed, implemented, and evaluated. It has demonstrated that the proposed system can achieve long-range operation, covering distances of up to 621 meters in an LOS outdoor environment and 309 meters in an NLOS indoor-outdoor environment, with an accuracy of less than 0.67 meters (LOS) or 1.74 meters (NLOS). Furthermore, it demonstrates that the system can operate with a low power consumption of 3.9 mW tag receiver without requiring strict frequency and phase generation circuits (PLL). A novel signal processing technique has been proposed to address the issue of unstable frequency/phase in the absence of a PLL. Consequently, this innovative system

can be applied effectively for large-scale asset or people tracking in industrial IoT applications.

	This work	[1]	[2]	[3]	[5]	[7]	[8]
Standard/Modulation	TDoA/OFDMA	IR-UWB	IR-UWB	Multi-tone	BLE/GMSK	NB-IoT/OFDM	NB-IoT/OFDM
Architecture	Low-IF I/Q	Direct-sampling	Direct-sampling	Sub-sampling	Zero-IF I/Q	Zero-IF I/Q	Zero-IF I/Q
Integration Level	RXFE	TRX	RX	RX	TRX	WuRXFE	TRX
Technology	55nm CMOS	55nm CMOS	65nm CMOS	40nm CMOS	40nm CMOS	28nm CMOS	55nm CMOS
Area	0.85mm^2	8.6mm^2	6mm^2	2.93mm^2	0.89mm^2(RF)	1.08mm^2	2.23mm^2
Operation frequency	2.4-2.5GHz	7.3G/8.7GHz	4GHz	60GHz	2.4GHz	750-960MHz	450-2220MHz
Noise figure	6.5dB	6.3dB	-	-	-	5~7dB	3.5~4.5dB
Sensitivity	-115dBm (ranging)	-	-	-	-94dBm	-109dBm	-140dBm (With repetition)
Supply voltage	0.9V	1.8/3.3V	-	-	-	0.9V	0.9V/1.1V
Rx power	3.9mW	118mW(total)	70mW(<1m)/ 320mW(2m)	195mW	5.3mW	2.1mW	11.8mW
Off-Chip matching	Yes	No	No	Yes	No	Yes	Yes
Off-chip reference	No	Yes	Yes	Yes	Yes	Yes	Yes
Ranging BW	100MHz	1.4G/1.5GHz	500MHz	2GHz	80MHz	-	-
Ranging time	181.5ms	100us	100us	20us	5.3ms	-	-
Max. range	621m(LOS)* 309m(NLOS)*	9m	2.1m	5m	20m	-	-
Accuracy	<0.67m(LOS)* <1.74m(NLOS)*	1.2mm(4m)	1.9mm(47-50cm)	4mm(3.6m)	22cm	-	-

*Numbers are updated for longer max distance measurements since conference proceddings publication

Figure 3.30: Performance comparison table

CHAPTER IV

A Millimeter-Scale, PLL-Less, Crystal-Less Receiver with a 10-bit 20MS/s ADC For Narrowband RF Localization System

4.1 Introduction

4.1.1 Backgrounds

In Chapter III, we propose a novel narrowband RF localization system to achieve long-distance operation and a low-power tag receiver that performs narrowband sub-carrier frequency hopping to traverse the entire radio frequency (RF) bandwidth (described in Section 3.2). The narrow bandwidth tag receiver hops harmoniously across the pre-determined frequency pattern and collects the transmitted symbols from anchors. The received signals are then used to estimate the channel impulse response (CIR) as it is operating at full bandwidth. The time-of-arrival (ToA) getting from CIR calculates the distance between a pair of a tag and an anchor. Multiple anchors' estimated ToAs, together with the known position of anchors, can localize the tag itself with the localization process described in Section 3.3.3.

To further simplify the tag receiver front-end, in Section 3.3.2, we have described an innovative tag receiver signal processing algorithm to not rely on strict frequency

and phase information. Therefore, the tag receiver can operate without the need for a phase-lock loop (PLL), and thus a crystal oscillator, to provide accurate frequency and phase reference, enabling a small form factor and low-cost receiver. Correction of RF impairments, i.e., frequency offsets and phase uncertainties, have been described in Section 3.3.3.1. Then, we fabricated an RF front-end ASIC chip in a 55nm CMOS process to demonstrate the concept's feasibility, described in Section 3.4. Finally, a thorough system-level evaluation with Universal Software Radio Peripheral (USRP) is conducted and reported in Section 3.6.

4.1.2 Challenges

As the measurement setup shown in Section 3.5.2, the tag USRP is used to communicate with the ASIC tag receiver, performing frequency hopping and sampling the baseband I/Q analog signal. The synchronization (time/ frequency) between the tag and anchors relies on an accurate sampling frequency at the baseband, achieved through high-precision temperature-compensated crystal oscillators (TCXO) within the USRP. For long packet time scenarios, a detailed method for enhancing synchronization is described in Section 3.5.3 and 3.5.4. Moreover, the USRP utilizes a high-resolution 14-bit analog-to-digital converter (ADC) to convert the baseband analog signal. The high-resolution ADC significantly reduces the quantization noise, resulting in the overall receiver achieving heightened sensitivity.

Nevertheless, integrating such high-standard system requirements into the IoT system is often impractical due to substantial power consumption, large physical footprint, and high system costs. On the other hand, replacing the USRP with a fully integrated ASIC implementation presents several challenges, especially the indispensability of a precise sampling clock. If the baseband sampling clock lacks accurate synchronization, the tag cannot effectively process symbol information or combine multiple symbols while maintaining the correct phase relationship, which is

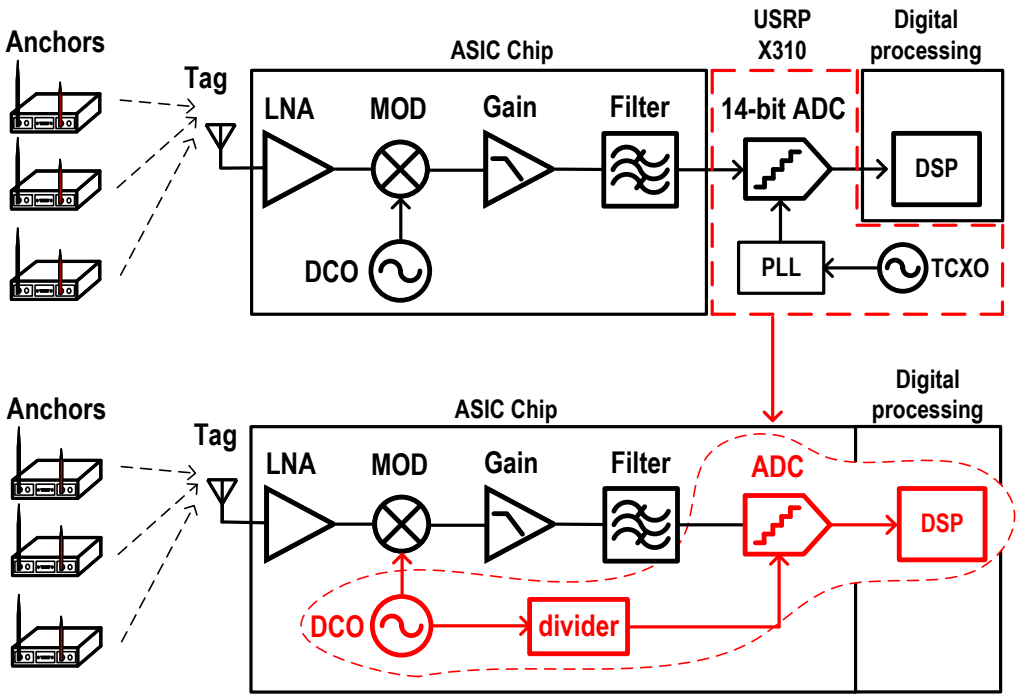


Figure 4.1: Difference between Chapter III (top) and Chapter IV (bottom)

essential for obtaining accurate channel frequency response (CFR) information.

4.1.3 Proposed Solutions

To enable a fully integrated millimeter-scale tag receiver for the localization system, we propose a novel signal-processing technique that works with a sampling clock generated by the free-running oscillator. The technique enables a system to operate without requiring a strict sampling frequency at the baseband. Moreover, the receiver utilizes the divided-down clock from the free-running oscillator as the ADC sampling clock. This eliminates the need for external crystal oscillators or power-consuming PLL circuits, making the receiver self-contained in clock generation. The difference between Chapter III and Chapter IV is shown in Figure 4.1

Without the PLL, the free-running oscillator introduces an unknown carrier frequency offset (CFO). In the proposed scheme, the receiver uses the clock derived

from the local oscillator (scaled down in frequency) as its sampling clock. This arrangement indicates that the CFO is directly linked to the sampling frequency offset (SFO). The division process reduces the frequency of the local oscillator to a lower level but preserves the original frequency error, which is proportional to the value set by the divider. As a result, with the known divider ratio N_{DIV}, this relationship can be described as

$$SFO = \frac{CFO}{N_{DIV}} \tag{4.1}$$

As described in Section 3.3.3.1, the CFO value can be estimated by the known pilot signal frequency. Following the above equation, we can acquire the estimated SFO (or estimated sampling frequency). Given the estimated sampling frequency, the data symbols within a window can undergo a resampling process. The resampling process adjusts the estimated sampling frequency to match the system's sampling frequency, which is aligned to the main and reflecting anchors. It adjusts the signal sampling frequency and corrects the symbol's magnitude and phase. This correction is tailored for each reception window and is on a per-window basis during the offline post-signal processing. Between frequency hopping windows, the receiver changes the oscillator frequency, which in turn changes the sampling frequency. This leads to window length errors on a per-window basis and cumulative window start time errors over multiple windows. The window start time error introduces an undesired phase delay, which causes problems in aligning multiple windows. However, these errors can be estimated and compensated in the proposed signal processing with the known SFO. SFO correction is crucial to correct the symbol's magnitude and phase information, and it also ensures precise timing between different windows, effectively achieving window-to-window synchronization. Equipped with the novel CFO and SFO correction to the baseband signals, it becomes possible to completely restore the

original signal's magnitude, phase, and sampling frequency. This restoration is vital for precise CFR or CIR estimation.

4.2 Tag Receiver System Overview

4.2.1 ASIC Tag Receiver

The proposed tag receiver is implemented with coherent receiver architecture and integrated 10-bit ADC to produce the digital output signals. The receiver operates in the 2.4-2.5GHz ISM band and performs frequency hopping across 100 MHz bandwidth. It hops across 64 windows, each with a bandwidth of 3 MHz. The frequency hopping is controlled by a digital controller, which configures the frequency code of the free-running oscillator. Each pre-determined frequency code undergoes precise calibration using external frequency counting equipment before being stored in the on-chip memory. Measurement result reveals that the frequency range can cover 100 MHz with a frequency resolution between 0.35-0.4 MHz.

The tag receiver is designed to function in indoor, multi-path rich environments and outdoor, long-range environments. This requires a wide dynamic range as well as high sensitivity. In the high-sensitivity scenario, the receiver naturally benefits from a low noise bandwidth through receiving narrowband subcarriers. Nonetheless, a significant receiver gain is necessary to suppress quantization noise produced by the ADC. With a 10-bit ADC and noise figure of 7.5 dB, a minimum gain of 70 dB is required to suppress the quantization noise if targeting the -115 dBm sensitivity level. For wide dynamic range, the receiver includes multiple gain stages across different blocks, including the low-noise amplifier (LNA), the trans-impedance amplifier (TIA), the band-pass filter (BPF), and the programmable gain amplifier (PGA). The receiver provides ten gain gears, achieving a wide gain range of 72 dB. The first seven gain gears increase by 6 dB/step, while the subsequent three gain gears increase by 10

dB/step. Measurement results reveal that the receiver can achieve a sensitivity of -115 dBm with a wide dynamic range of 86 dB.

To make a complete millimeter-scale low-power tag receiver, we simplify the ADC sampling clock generation without the need for a PLL and an external crystal oscillator. Instead, the free-running oscillator generates the ADC sampling clock with a downscaling ratio. The ratio is designed with a fixed integer value of 256. Consequently, while the receiver performs frequency hopping across 2.4 to 2.5 GHz, the ADC sampling clock varies from 18.75 MHz to 19.53125 MHz. This results in a sampling frequency that differs from window to window and is asynchronous with the transmitter's sampling frequency. Without adequately handling the received data, it can fail to extract actual data symbol information needed for CFR/CIR estimation. To address this issue, we propose a novel signal processing technique to effectively process the asynchronous sampling data.

4.2.2 Tag Post Signal Processing

The entire receiver operates primarily based on the free-running oscillator to generate the local oscillator clock and ADC sampling clock. Therefore, while the receiver performs frequency hopping, the ADC sampling frequency varies along with the local oscillator frequency. This poses significant challenges for post-signal processing- in particular, it complicates the synchronization of individual and consecutive windows. These challenges include 1) loss of precise time and phase information within each reception window. 2) Inability to achieve coherent stitching of data symbols between windows because of different sampling frequencies. 3) loss of precise timing for the timing control of frequency hopping, which in turn creates multi-window synchronization issues. Consequently, managing a wide range of unknown sampling frequencies and asynchronous timing presents significant challenges in our scenario.

Figure 4.2 shows the proposed tag receiver signal processing overview. The tag

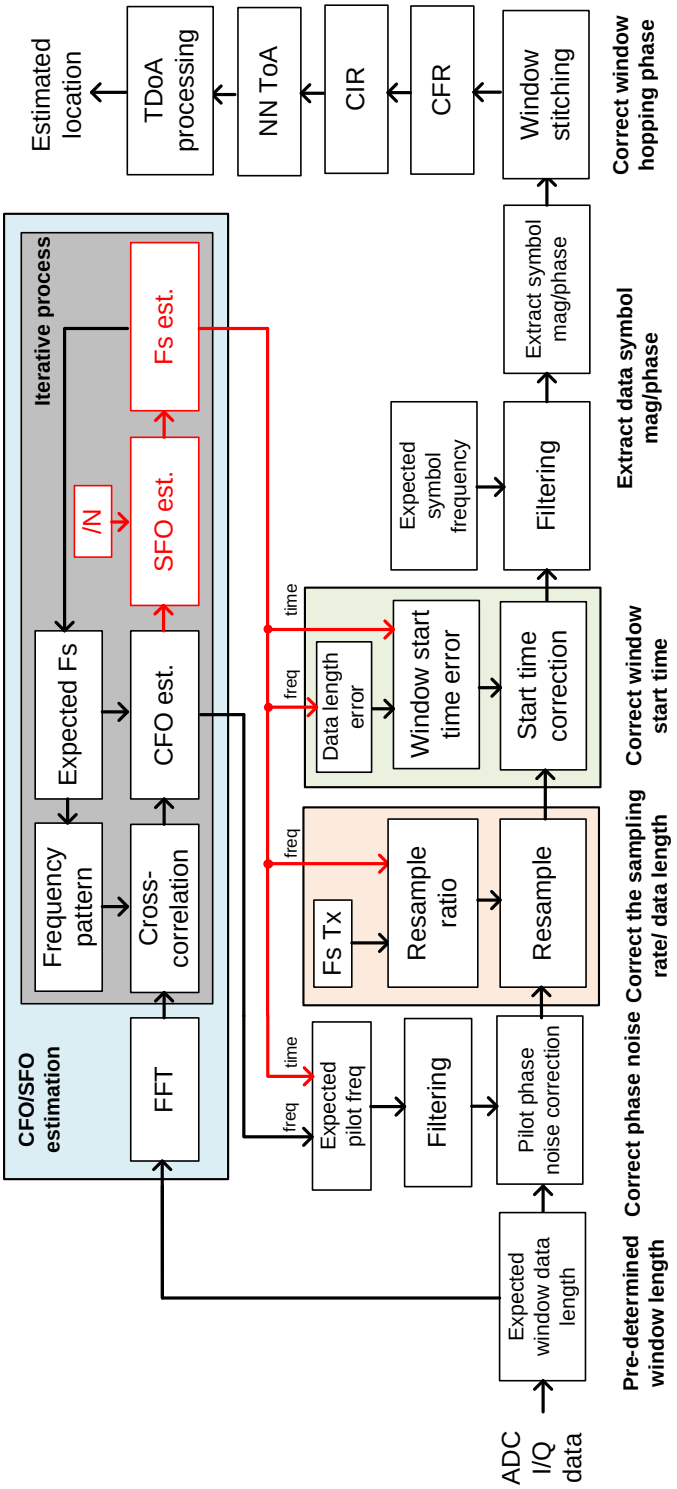


Figure 4.2: Tag receiver post signal processing overview

post-signal processing contains several stages. The CFO and phase noise correction and window stitching processes have been covered in Section 3.3.3.1 and Section 3.3.3.2. Three new processes are introduced in the section to address the unknown sampling clock issues.

4.2.2.1 CFO and SFO Estimation

The window hopping time is pre-determined and agreed upon in the system. In our design, the receiver calculates the window hopping time by counting the number of samples with its current sampling frequency. The number of data samples per window is also pre-determined and calculated based on the window hopping time and the expected sampling frequency. The expected sampling frequency (expected Fs in Figure 4.2) can be estimated by observing the divided-down clock from a local oscillator, which ranges from 18.75MHz to 19.53125MHz. Distinct windows would require counting a different number of data samples, and that information is stored in the memory as the estimated window hopping time.

Once each window's expected number of data samples (data length) is known, we extract the target data length for post-signal processing. Following the data extraction, we perform the FFT and cross-correlate it with the expected frequency pattern to find the initial CFO. The initial CFO combined with the known divider ratio yields the SFO (as shown in Equation 4.1). The initial CFO is a coarse estimation based on the assumption of the expected Fs (and the frequency pattern). To further enhance accuracy, an iterative process is required. We update new Fs (and the frequency pattern) with the expected Fs and an estimated SFO and perform the next iteration of CFO and SFO estimations. The CFO error would result in the SFO error.

4.2.2.2 Resample Process

The free-running oscillator with a known dividing ratio determines the tag receiver sampling frequency. The sampling frequency can be estimated by the SFO estimation process, as shown in Section 4.2.2.1. However, it is still not aligned with the transmitter sampling frequency (Fs Tx in Figure 4.2), which is determined by the system configuration. The sampling frequency difference between the transmitter and receiver poses challenges to demodulating the data symbol information and timing synchronization.

The simple way to re-align distinct sampling frequencies is through resampling. The resampling process performs rate conversion by upsampling the original sequence by an integral factor, k, and subsequently decimating it by another integral factor, j. In this way, the original sequence can resample to a rational multiple (k/j) of its original sample rate, which, in the end, aligns with the transmitter sampling rate. The resampling process involves nonlinear operations through interpolation and decimation. Thus, it should be performed after CFO and pilot phase noise correction to preserve the original CFO/phase noise information. In this process, the data length must be updated with the estimated Fs to acquire the correct number of samples (data length).

4.2.2.3 Window Timing Correction

To this point, each window's data symbol information has been successfully demodulated. The sampling frequency estimation and data length correction process described above have successfully synchronized the captured data with the system's sampling frequency and window data length. The synchronization allows an accurate reconstruction of the original waveform.

However, in the pre-processing stage, we choose a pre-defined data length for post-processing, and the subsequent window start time is based on the assumption

of counting the correct number of samples in the previous window. Capturing a pre-determined data length approach produces cumulative start time errors across multiple windows. If this cumulative start time error is not addressed, it can lead to incorrect time or phase information while stitching multiple windows. Therefore, to compensate for such time error, we measure the time difference (time error) between the expected and actual data length based on the estimated sampling frequency. Then, we correct the time error per window and calculate the cumulative errors across multiple windows. Figure 4.3 shows the window start time correction with different sampling frequencies (SFO) between windows.

4.2.3 Impact of Sampling Frequency Offset in the System

The proposed PLL-less and crystal-less tag receiver utilizes the free-running oscillator to generate the sampling clock. This arrangement produces the sampling frequency mismatch between the transmitter and receiver. Furthermore, the frequency hopping scheme causes the sampling frequency to vary across multiple windows. Therefore, this section delves into analyzing the system's behavior under the influence of SFO.

4.2.3.1 Symbol Distortion Due to SFO

To align the sampling frequency mismatch between the transmitter and receiver, Section 4.2.2.1 introduces a method to estimate the SFO using the estimated CFO and a known divider ratio. An iterative process is utilized to achieve an accurate estimation of SFO. Following the SFO estimation, a resampling process is conducted to adjust the receiver's sampling frequency to match the transmitter's sampling frequency. Nevertheless, any CFO estimation error would result in an SFO estimation error. Considering the SFO, the received signal $y(t)$, which should be sampled at intervals of T_s, is instead sampled with an interval of T_s plus a timing offset ΔT.

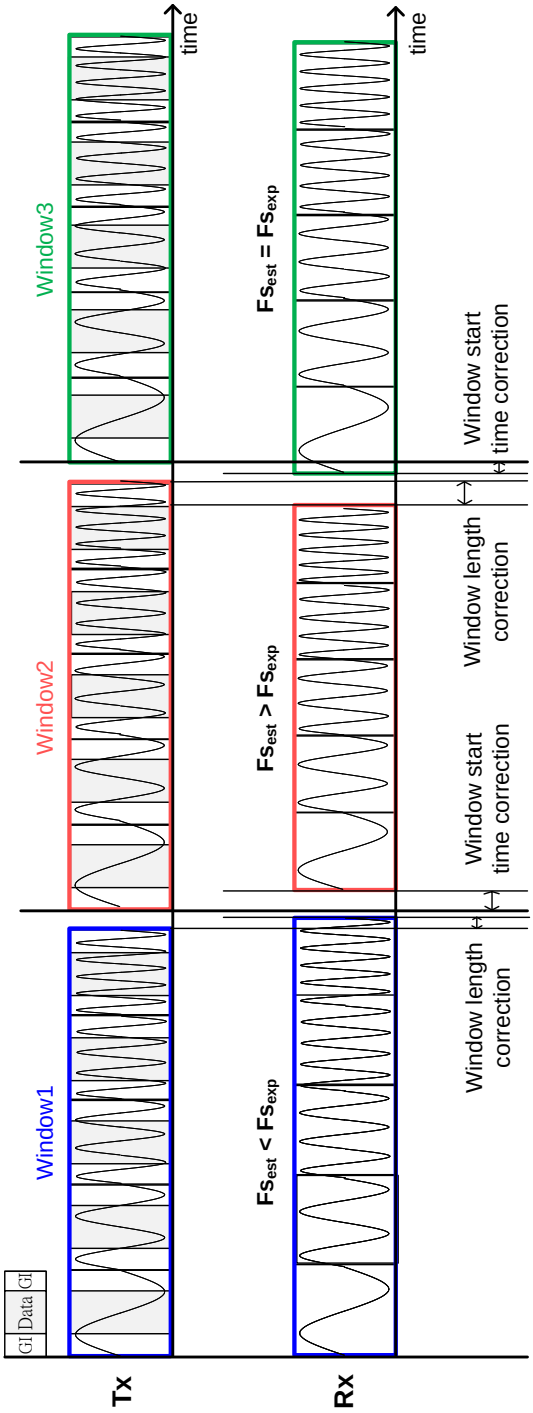


Figure 4.3: Window length and start time correction

This can be mathematically written as

$$y(nT_s) \rightarrow y(n(T_s + \Delta T)) \tag{4.2}$$

Thus, we can express the SFO mathematically as

$$\begin{aligned} SFO &= \frac{1}{T_s} - \frac{1}{T_s + \Delta T} \\ &\approx F_s \frac{\Delta T}{T_s} \\ &= F_s \delta \end{aligned} \tag{4.3}$$

Here, F_s denotes the desired sampling frequency, and δ is the normalized sampling period offset. In practice, the SFO can be quantified by δ.

Let's assume that the receiver sampling clock has an SFO error, and this SFO remains constant during symbol evaluation time. If there are K subcarriers, each with modulation data symbol S_k, the received signal $y[n]$ can be written as

$$y[n] = x(nT_s(1+\delta)) = \sum_{k=0}^{K-1} S_k e^{j\frac{2\pi}{N}kn(1+\delta)} \tag{4.4}$$

In this equation, n represents the discrete-time index, T_s is the ideal sampling period, δ is the SFO error, and N is the total number of samples.

Moving to the frequency domain $Y[m]$, where m is the subcarrier index, we can derive the signal from N samples using the FFT

$$\begin{aligned} Y[m] &= \frac{1}{N} \sum_{n=0}^{N-1} y[n] e^{-j\frac{2\pi}{N}mn} \\ &= \frac{1}{N} \sum_{n=0}^{N-1} \sum_{k=0}^{N-1} S_k e^{j\frac{2\pi}{N}kn(1+\delta)} e^{-j\frac{2\pi}{N}mn} \\ &= \frac{1}{N} \sum_{k=0}^{K-1} S_k \Big(\sum_{n=0}^{N-1} e^{-j\frac{2\pi}{N}[m-k(1+\delta)]n} \Big) \end{aligned} \tag{4.5}$$

To simplify this equation, we leverage the properties of the geometric series [101]

$$\sum_{n=0}^{N-1} e^{-j\frac{2\pi}{N}[m-k(1+\delta)]n} = \frac{sin(\pi[m-k(1+\delta)])}{Nsin(\frac{\pi}{N}[m-k(1+\delta)])} e^{-j\pi\frac{N-1}{N}[m-k(1+\delta)]} \tag{4.6}$$

Finally, combining the Equation 4.5 and Equation 4.6, we can simplify the frequency response to

$$Y[m] = \frac{1}{N}\sum_{k=0}^{K-1} S_k \frac{sin(\pi[m-k(1+\delta)])}{Nsin(\frac{\pi}{N}[m-k(1+\delta)])} e^{-j\pi\frac{N-1}{N}[m-k(1+\delta)]} \tag{4.7}$$

From the above equation, the received subcarrier $Y[m]$ is the sum of multiple subcarriers S_k. Each S_k is subject to the amplitude and phase distortion due to SFO. It is important to note that each subcarrier also has a different level of distortion; subcarriers with high-frequency experience more severe distortion. Notably, this effect undermines the orthogonal relationship between subcarriers, causing intercarrier interference (ICI).

Instead of transmitting all subcarriers simultaneously in the proposed system, we transmit one subcarrier per symbol time. This approach largely reduces the ICI effect. Let's assume that we receive one symbol ($m = k$) in each symbol time and $N \gg 1$; the received subcarrier can be described as

$$Y[k] \approx \frac{1}{N} S_k \frac{sin(\pi k\delta)}{Nsin(\frac{\pi}{N}k\delta)} e^{j\pi k\delta} \tag{4.8}$$

$$\Delta A[k] = \frac{sin(\pi k\delta)}{Nsin(\frac{\pi}{N}k\delta)} \tag{4.9}$$

$$\Delta\phi[k] = \pi k\delta \tag{4.10}$$

The symbol amplitude distortion (ΔA) and phase distortion ($\Delta\phi$) are still affected by the SFO error but without the ICI. The phase shift is more critical for localization accuracy and linearly increases with $\pi\delta$ between two consecutive subcarriers. Therefore, accurate SFO estimation is critical to restore the original magnitude and phase information.

4.2.3.2 Symbol Start Time Error with SFO

In our system, only one symbol is transmitted per symbol time to mitigate the ICI effect caused by the SFO. However, when multiple symbols need to be transmitted, the reception time increases linearly over time. During the post-processing, symbol-by-symbol processing is applied to demodulate the data, and it requires the exact knowledge of the start time of each symbol. Consequently, considering the SFO, subsequent symbols/windows are more likely to experience inaccurate start time errors. In other words, SFO leads to the accumulation of start time errors over multiple symbols. Similar to Equation 4.2, assuming a non-ideal delay t_l due to the start time error, the received data $y[n]$ can be written as

$$y[n] = x(nT_s(1+\delta) - t_l) = x(nT_s(1+\delta) - l \cdot T_s) = \sum_{k=0}^{N-1} S_k e^{j\frac{2\pi}{N}kn(1+\delta)} e^{-j\frac{2\pi}{N}kl} \quad (4.11)$$

where l is the delay normalized to the sampling period T_s.

Considering the k_{th} symbol in the window, where each symbol has N samples, the accumulated start time error due to SFO is $kN\delta T_s$. With Equation 4.11 and following the procedure mentioned in Equation 4.5 - 4.8, the k_{th} subcarrier can be written as

$$Y[k] \approx \frac{1}{N} S_k e^{-j2\pi k^2\delta} \frac{sin(\pi k\delta)}{Nsin(\frac{\pi}{N}k\delta)} e^{j\pi k\delta} \quad (4.12)$$

$$\Delta A[k] = \frac{sin(\pi k\delta)}{Nsin(\frac{\pi}{N}k\delta)} \quad (4.13)$$

$$\Delta\phi[k] = \pi\delta(2k^2 + k) \quad (4.14)$$

The above equation illustrates two phenomena due to SFO: 1) symbol itself amplitude and phase distortion. 2) accumulated start time error causes phase rotation. It's worth noting that SFO increases the symbol phase linearly with the subcarrier frequency, while the start time error causes the symbol phase to increase quadratically.

Section 4.2.2.3 discusses the window timing correction. Because of the frequency hopping in the system, each window operates with a different sampling clock, resulting in different SFO. Hence, we must consider the accumulated start time error between windows to align window-to-window timing properly. Given the total of W windows, where each window has K symbols and each symbol has N samples, the frequency response of k_{th} subcarrier in w_{th} window can be written as

$$Y_w[k] \approx e^{-j2\pi \frac{k(wNK\delta_w)}{N}} \frac{1}{N} S_k e^{-j2\pi k^2 \delta_w} \frac{sin(\pi k \delta_w)}{N sin(\frac{\pi}{N} k \delta_w)} e^{j\pi k \delta_w} \tag{4.15}$$

$$\Delta A[k] = \frac{sin(\pi k \delta_w)}{N sin(\frac{\pi}{N} k \delta_w)} \tag{4.16}$$

$$\Delta \phi_w[k] = \pi \delta_w (2k^2 + wK + k) \tag{4.17}$$

Equation 4.16 and 4.17 show the amplitude distortion and phase distortion due to the SFO. Within the window, the phase increases quadratically with subcarrier frequency k. Across windows, the phase is growing linearly with window time wK. The result indicates the bandwidth limitation for our SFO-sensitive systems.

Finally, to compute the CIR, we can apply IFFT to the CFR

$$\begin{aligned} y[n] &= \sum_{k=0}^{N-1} Y[k] e^{j2\pi \frac{kn}{N}} \\ &= \sum_{w=0}^{W-1} \sum_{k=0}^{K-1} Y_w[k] e^{j2\pi \frac{kn}{N}} \end{aligned} \tag{4.18}$$

4.3 Tag Receiver Chip Implementation

Figure 4.4 shows the tag receiver system structure. The tag receiver is designed with a coherent receiver structure with input RF signal and output I/Q baseband digital signals. The receiver operates under a single power domain, 1.1V, with several low-dropout regulators (LDO) providing 0.9V for internal circuits. The RF signal is

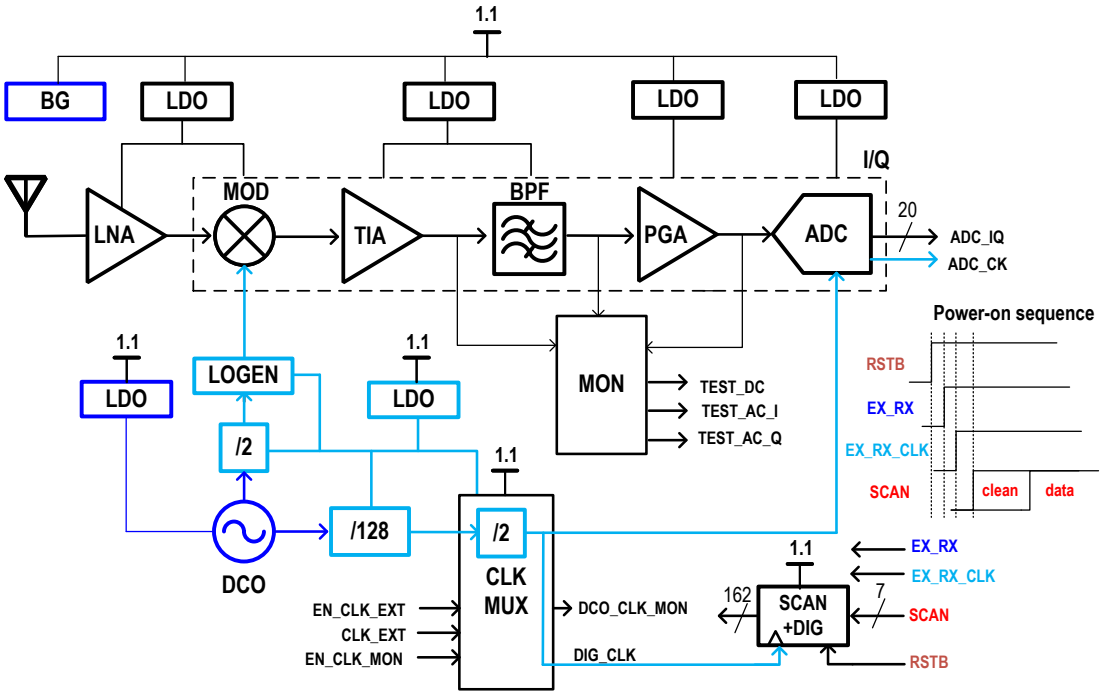


Figure 4.4: Block diagram of the fully-integrated tag receiver

down-converted to the baseband signals by the free-running oscillator with a divide-by-2 ratio. Simultaneously, the ADC sampling clock uses the divided-down clock from the free-running oscillator with a divide-by-256 ratio. The digital controller clock shares the same clock as the ADC sampling clock. This arrangement makes the entire receiver self-contained in the clock generation, without any other clock generation circuits and external components (crystal oscillator). The chip can power on through three GPIO pins, including the RSTB pin, EN_RX pin, and EN_RX_CLK pin. The RSTB pin resets the digital block. The EN_RX pin activates the bandgap and LDO circuits. The EN_RX_CLK pin enables the internal clock divider circuits. The power-on sequence is shown in Figure 4.4. The chip can program through the scan digital interface with an internal decoder in the digital controller to decode the scan commands.

4.3.1 A Low Noise Amplifier with Transformer Input Matching

The low noise amplifier is required to have high RF gain (to suppress quantization noise), low noise, and low footprint on both chip- and board-level to enable a millimeter-scale tag receiver. The low noise amplifier is designed with transformer-based input matching LNA structure [102] [103] [104]. In the conventional design, a gate inductor (Lg) and a source inductor (Ls) are required to generate a real part impedance at the resonant frequency. The transformer structure couples both the gate and source inductor to save the footprint of the magnetic devices. The mutual inductance, M, due to the coupling between the gate and source inductor, increases both the inductive and real parts. As a result, a small winding area can be used to achieve a target inductance. The input matching condition for the transformer-based input LNA can be described as

$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_s + L_g + 2M) + \frac{g_m}{C_{gs}}(L_s + M) \tag{4.19}$$

where g_m is the common-source transconductance, C_{gs} is the common-source gate to source capacitance.

For the transformer layout, we implement a stack layout style. This arrangement allows a large magnetic coupling to be obtained (k=0.85). However, it introduces more inter-winding parasitic capacitance (C_{p3}/C_{p4}) between the primary and secondary coil. We have two top metals with same thickness in our particular process. Therefore, there is no significant difference in quality factor regarding which inductor should be on top, except the parasitic capacitance to ground. The top metal is used for Lg, while the bottom layer is used for Ls. The extraction model of the transformer is shown in Figure 4.6.

The complete LNA structure is implemented with 3-stage LNA to provide high RF gain, as illustrated in Figure 4.7. The first stage aims to achieve both input match

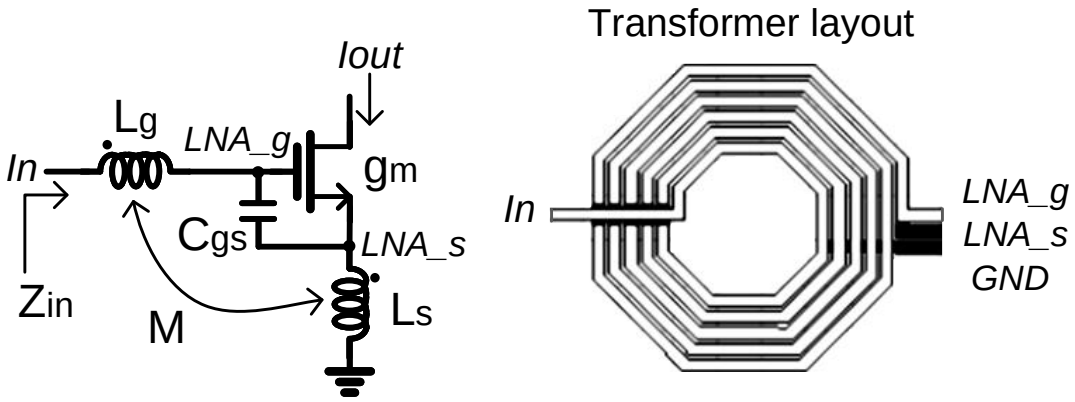
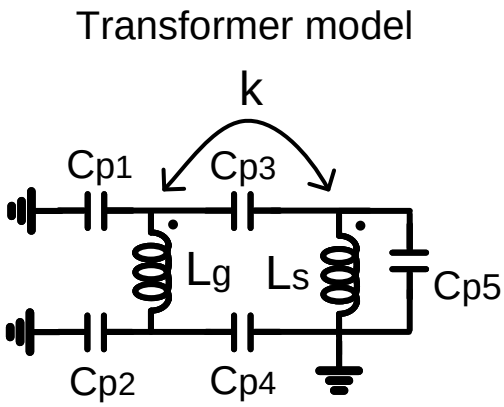


Figure 4.5: Transformer input matching and layout



Model parameters

Lg	3.3n
Ls	3n
k	0.85
Cp1	60f
Cp2	70f
Cp3	100f
Cp4	100f
Cp5	90f

Figure 4.6: Transformer model and parameters

($S_{11} < -15$ dB) and low noise figure ($NF < 4$ dB), while the second and third stages are used for RF gain boosting. The second and third-stage RF gain amplifiers are designed with an inductor-less complementary amplifier to save the inductor areas and avoid on-chip coupling. Simulation shows the LNA can provide a maximum of 40 dB gain, 4.2 dB noise figure, and 2.8 mW power consumption. The first stage can

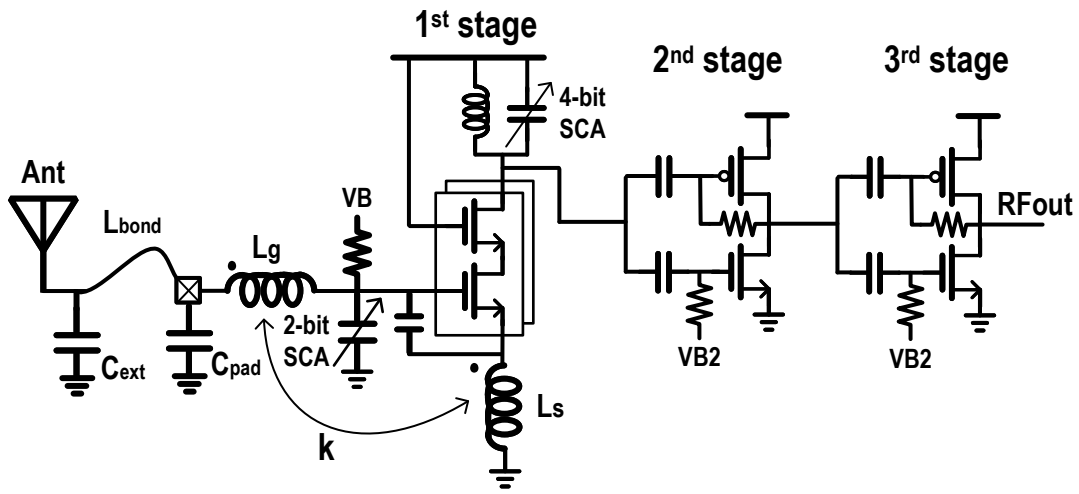


Figure 4.7: Complete 3-stage LNA schematic

provide additional 6 dB gain tuning.

Due to the wire-bonding inductor, we need an external capacitor with 1.5 pF on the PCB board for external input matching. The overall design structure requires only one external component and two inductor areas (one transformer and one drain-side inductor), achieving a very compact area.

4.3.2 A 10-bit, 20MS/s SAR ADC with Digital Error Correction

To achieve low power, high reliability, and high-resolution ADC, we implement a 10-bit ADC with asynchronous successive-approximation-register (SAR) and digital error correction [105] [106] [107] [108]. The implementation structure is shown in Figure 4.8. The basic principle of digital error correction is that if a comparator misjudges in a step due to the comparator dynamic offset or incomplete settling time effects (especially during the MSB bits process), the following steps have redundancy to correct such error. This technique has been widely used for different purposes. It can be used for increasing the yield of ADC across different process corners [107], relaxing the incomplete settling time, thus increasing the speed [105], or eliminating

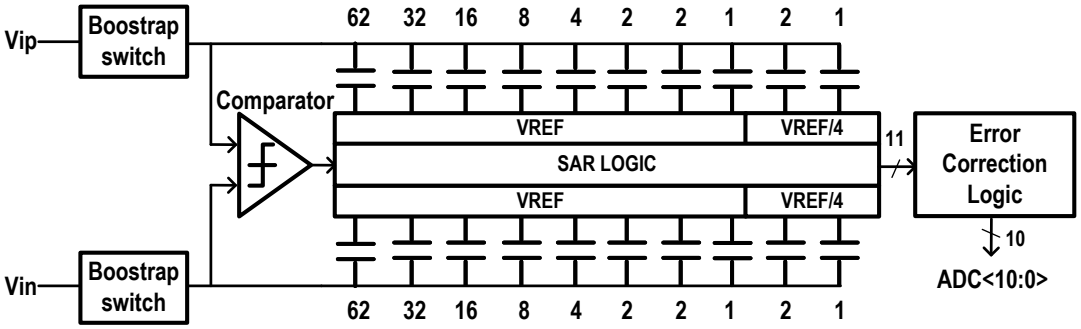


Figure 4.8: Block diagram of a 10-bit, 20MS/s SAR ADC with digital error correction

Cycle	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11
Non-Binary	496	256	128	64	32	16	16	8	4	2	1
ECC range	32	16	16	16	16	16	0	0	0	0	
Cap value	62	32	16	8	4	2	2	1	2	1	
with Vdac	Vref	Vref	Vref	Vref	Vref	Vref	Vref	Vref	Vref/4	Vref/4	

Cycle\ Decimal		512	256	128	64	32	16	8	4	2	1
#1	496		B10	B10	B10	B10	B10				
#2	256		B9								
#3	128			B8							
#4	64				B7						
#5	32					B6					
#6	16						B5				
#7	16						B4				
#8	8							B3			
#9	4								B2		
#10	2									B1	
#11	1										B0
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Figure 4.9: Non-binary DAC implementation with redundancy

$$D_{out} = 256*(B_{10}+B_9) + 128*(B_{10}+B_8) + 64*(B_{10}+B_7) + 32*(B_{10}+B_6) + 16*(B_{10}+B_5+B_4) + 8*B_3 + 4*B_2 + 2*B_1 + 1*B_0$$

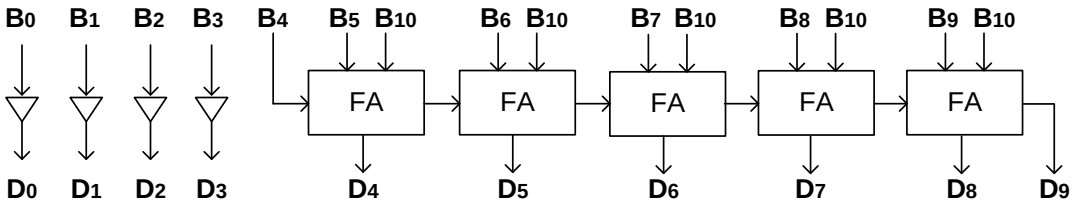


Figure 4.10: Error correction logic and its implementation

the need for analog calibration.

Digital error correction employs a non-binary search algorithm and requires more capacitors and conversion cycles (for redundancy) in the SAR operations. Figure 4.9 shows the redundancy implementation. We introduce one extra conversion cycle (total of 11 cycles) and an additional 3% redundancy capacitance in the capacitor-DAC (CDAC). If the CDAC voltage settling time error is within the redundancy range, any erroneous decision can be corrected in the subsequent conversion cycles. This arrangement results in an effective error tolerance range of 32 for the MSB bit and 16 for the next 5 bits. An error in the subsequent conversion cycles will result in performance degradation as there are no subsequent conversion cycles to correct it.

Figure 4.10 shows the implementation of the error correction logic. The proposed logic is implemented by a ripple-carry adder circuit consisting of a five-stage full adder to decode the first six MSB bits (D9 - D4). The propagation delay for the error correction logic is negligible regarding the sampling frequency (20 MHz).

The CDAC switching scheme is essential in determining the total energy consumption. We implement the monotonic switching scheme [109] with reference voltage scaling to save switching energy and reduce the total capacitance value. The voltage scaling is used in the last 2 bits with a voltage ratio of 4:1. The unit cap in the implementation is 5 fF with a total cap of 650 fF.

The total ADC noise includes three components: thermal noise (kT/C) of 79 uV_{rms}, comparator noise of 404 uV_{rms}, and quantization noise of 310 uV_{rms}. The total ADC noise will be suppressed by the receiver gain. According to the link budget analysis, the receiver gain requires a minimum 70 dB gain to achieve $\sim$-115 dBm sensitivity level.

4.4 Tag Receiver Measuremnt

The proposed tag receiver is fabricated in the 40nm CMOS process. The die micrograph is shown in Figure 4.11 and occupied 1.6 x 2.6 mm^2 area. The receiver chip consumes 10 mW of power under a single supply voltage of 1.1V.

4.4.1 Measurement Setup

The measurement setup is shown in Figure 4.12. The tag receiver is evaluated with chip-on-board (CoB). The chip is covered with black encapsulation. The free-running oscillator is a sensitive circuit that can experience noise caused by photons interacting with the oscillator. Therefore, the use of black encapsulation is necessary to block the light. The tag receiver converts the RF signal to baseband I/Q digital signals on the RF board. Then, the digital signals pass through a board located beneath the RF board, with level shifters to convert to the 3.3V voltage domain. The output digital signals are eventually captured by the digital oscilloscope (Saleae, Logic Pro 16) and stored on the desktop for signal processing. The clock monitor port outputs a divided-down clock from the free-running oscillator with a divide-by-256 ratio. It connects to the frequency counting equipment (Keysight 53220A) for characterizing the DCO frequencies. The microcontroller (Adafruit FT232H) is used to program the chip with scan commands.

4.4.2 Frequency Window Characterization

Figure 4.12 shows the sweeping of 7-bit fine cap code in DCO at both high (2.5 GHz) and low (2.4 GHz) frequency bands. The fine capacitor bank is implemented with a thermometer code structure. It achieves an average of 0.35 MHz frequency resolution with DNL 0.14 LSB at the low-frequency band and 0.4 MHz frequency resolution with DNL 0.19 LSB at the high-frequency band. Figure 4.14 shows the sweeping of 8-bit coarse code in DCO for the full operation bandwidth. The coarse

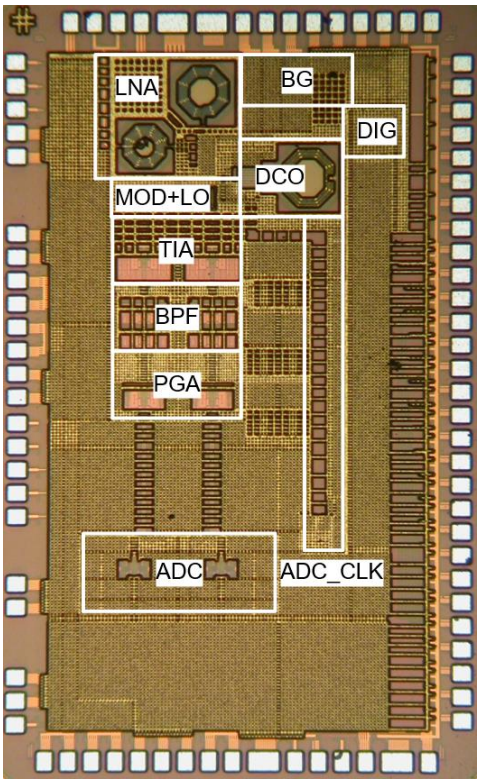


Figure 4.11: Die micrograph of the proposed tag receiver in 40nnm CMOS process

capacitor bank is implemented with a binary code structure, offering a maximum frequency step of 4.24 MHz.

Figure 4.15 shows the calibration result of 64 window frequencies. The allocated frequency hopping bandwidth is 100 MHz with a pre-determined window frequency step of 1.56 MHz. Initially, the fine code is configured to approximate the maximum allowable code during the calibration. Then, we adjust the coarse capacitor code to the minimum operation frequency. Subsequently, the fine code is incrementally decreased until the fine code approaches its lower limit. Upon nearing the boundary, the system recalibrates the coarse code, followed by the fine code set to its maximum value, to align the next target frequency. The iterative process of adjusting the fine code and, when necessary, the coarse code persisting until the operation frequency's upper limit is reached. The calibration result achieves a maximum 0.32 MHz error

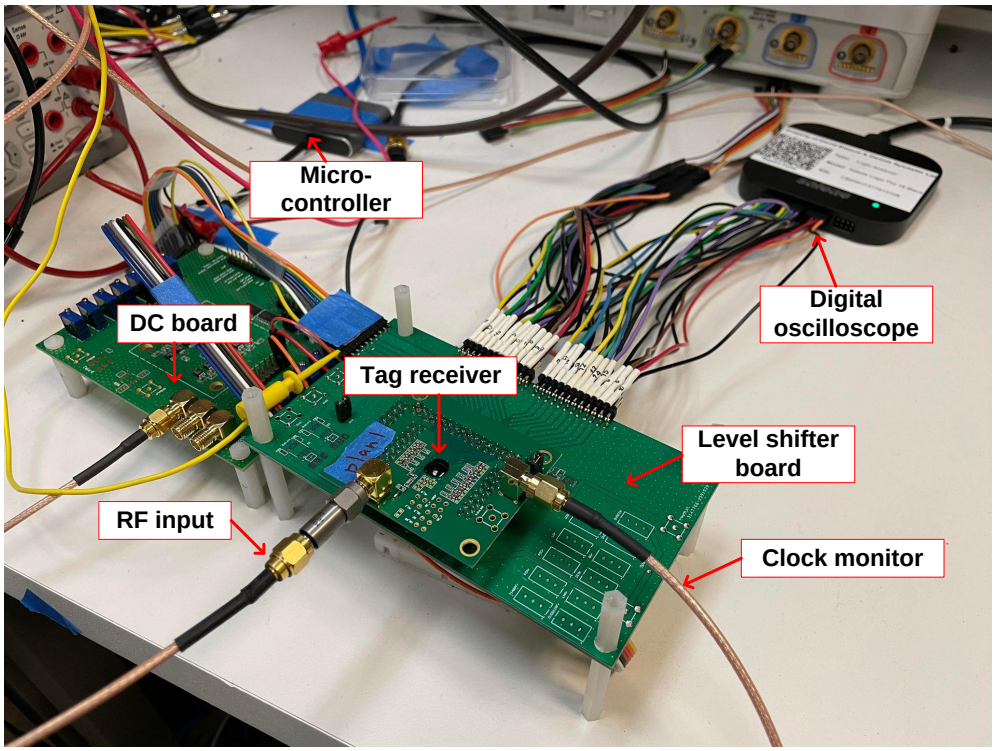


Figure 4.12: Measurement setup

across 64 window frequencies.

4.4.3 Receiver Measurement

Figure 4.16 shows the noise figure and sensitivity measurement of 64 frequency hopping windows. The noise figure measurement characterizes the entire receiver chain, from RF signal input to ADC digital output. The signal/noise integration bandwidth is ∼10 kHz, and each result undergoes averaging over 10 times. The receiver demonstrates an average 7.6 dB noise figure across 64 frequency hopping windows. For sensitivity measurement, the sensitivity level is characterized at 10 dB SNR and achieves ∼-115 dBm sensitivity level across 64 frequency hopping windows.

Figure 4.17 shows the dynamic range measurement of the receiver with three distinct frequencies (low/mid/high frequency). The receiver provides a total of 10 gain gears. The initial seven gain gears operate with 6 dB/step, while the final three

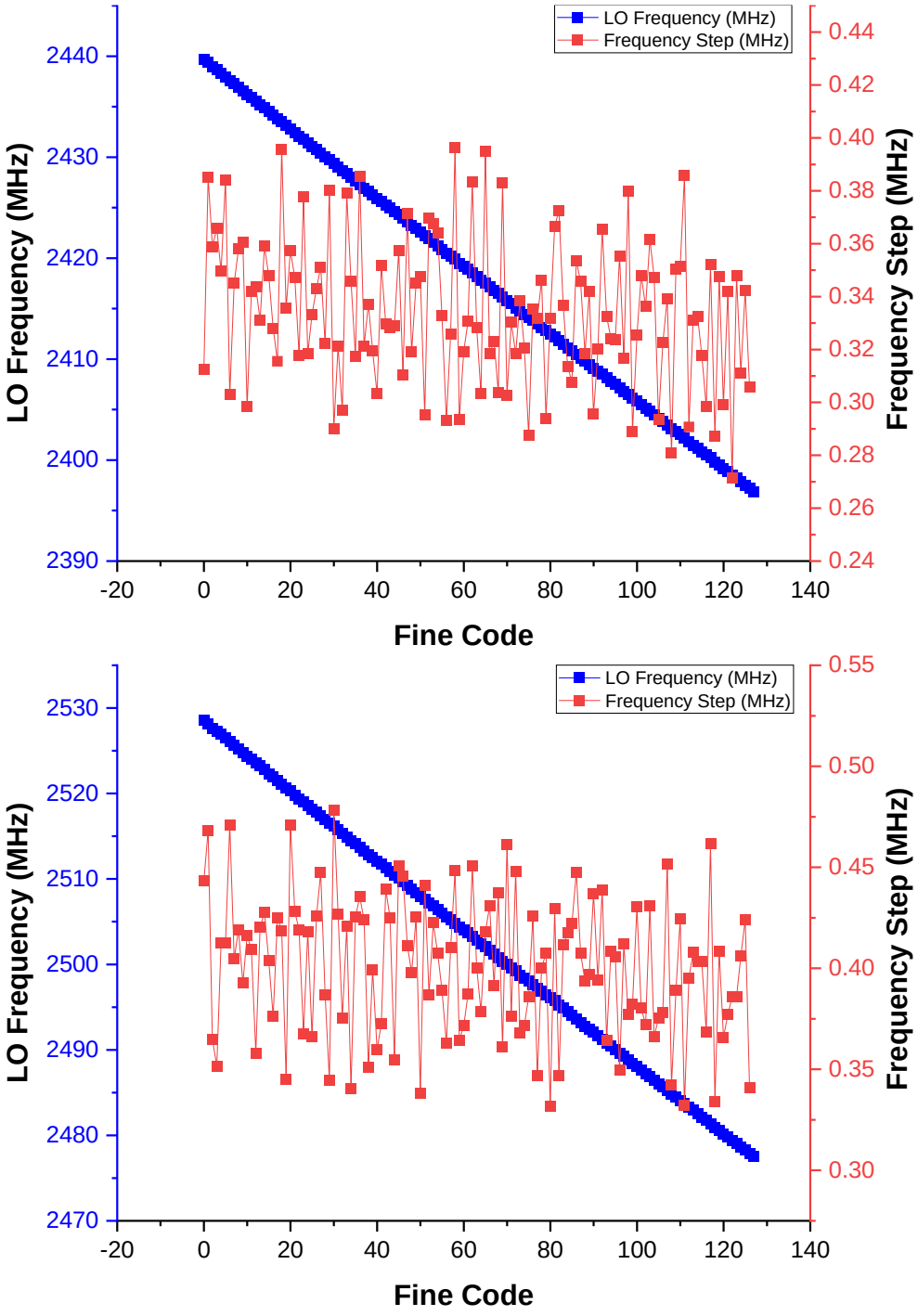


Figure 4.13: Sweeping of 7-bit fine capacitor code in DCO

gain gears operate with 10 dB/step. The transition of the highest gain setting is at ∼-92 dBm input power, after which each subsequent gain reduces 6 dB gain when

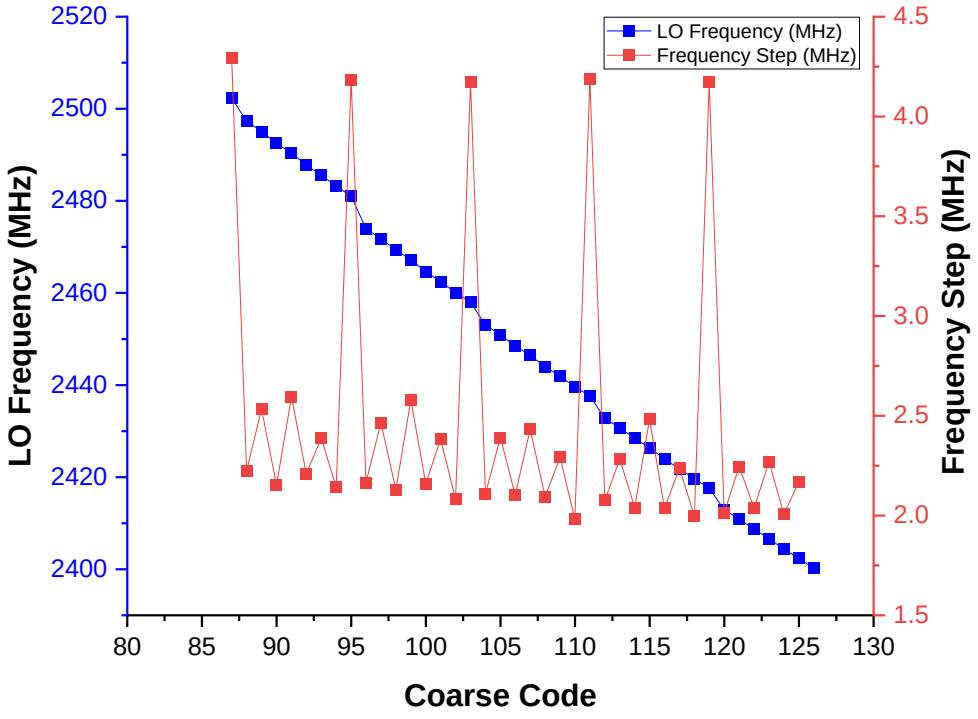


Figure 4.14: Sweeping of coarse capacitor code in DCO across the operating frequency band

the input power increases 6 dB. The measurement result reveals that the receiver can detect the signal as low as -115 dBm and achieves the 1 dB input compression point (P_{1dB}) of -29 dBm, resulting in the total dynamic range of $\sim$ 86 dB.

Figure 4.18 shows the receiver bandwidth measurement. This measurement characterizes the entire receiver chain baseband frequency response, revealing a bandpass frequency response with -3 dB from 80 kHz to 3 MHz.

Figure 4.19 shows the necessary external components for the input matching. It requires one shunt capacitor to match 50 Ohm, and an additional cap in series acts as an AC coupling component. This configuration effectively reduces the footprint on the PCB board. The input matching is characterized by the network analyzer (Keysight E5062A). As illustrated in Figure 4.20, the measured S_{11} is $\leq$ -20 dB across the entire operation bandwidth.

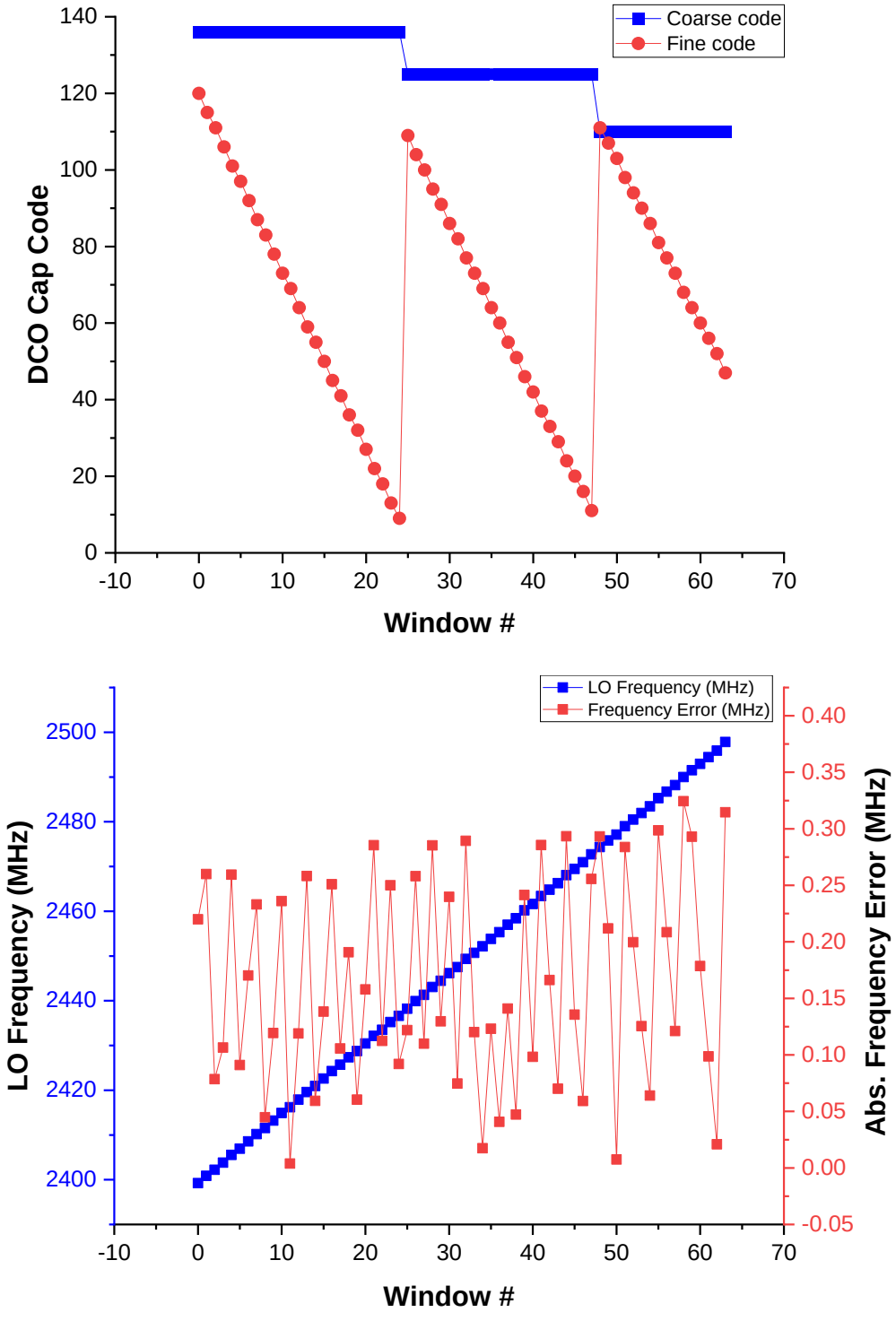


Figure 4.15: Calibration of frequency hopping windows

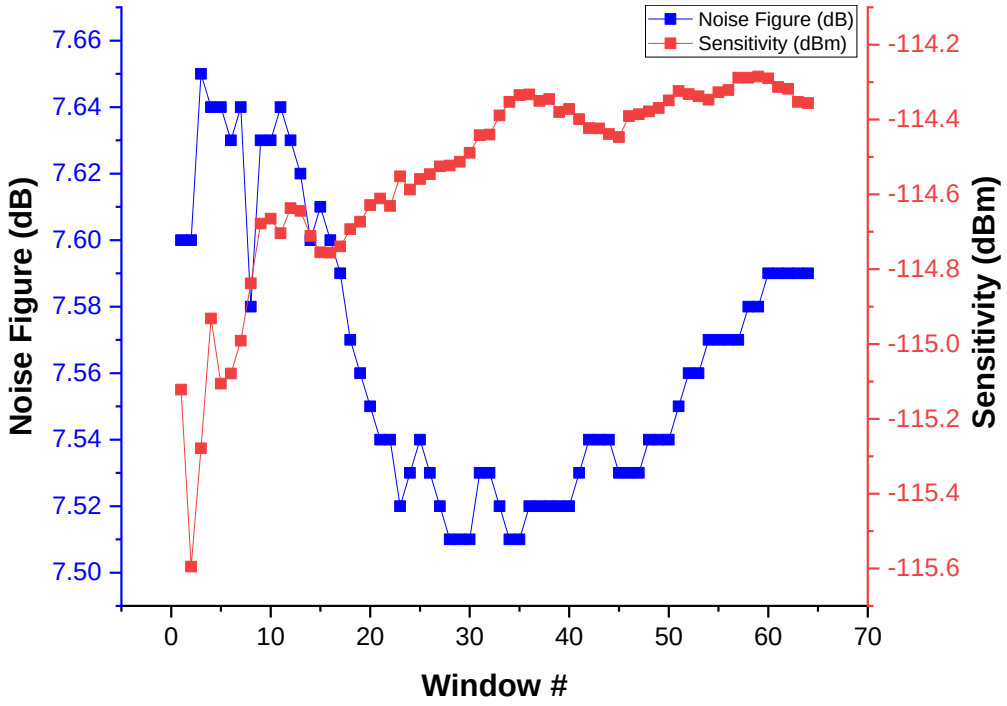


Figure 4.16: Noise figure and sensitivity measurement of 64 frequency hopping windows

4.4.4 Impact of Free-running Oscillator in the Receiver

Figure 4.21 presents the measured spectrum at the sensitivity level. The ADC output captures this spectrum while the input power is around -115 dBm and the SNR is around 10 dB. A notable system characteristic is the frequency spread of the primary signal caused by the free-running oscillator, which extends roughly +/-40 kHz throughout 450 us duration. Figure 4.22 illustrates this behavior more comprehensively. We conducted five separate data captures and showed their magnitude and phase response. The free-running oscillator presents frequency and phase drift over the symbol/window duration. From the system point of view, this frequency spread would restrict the number/length of symbols per reception window. Moreover, allocating appropriate frequency space between symbols must also be considered in the frequency plan. The impact of frequency spread to the system includes 1) CFO/SFO

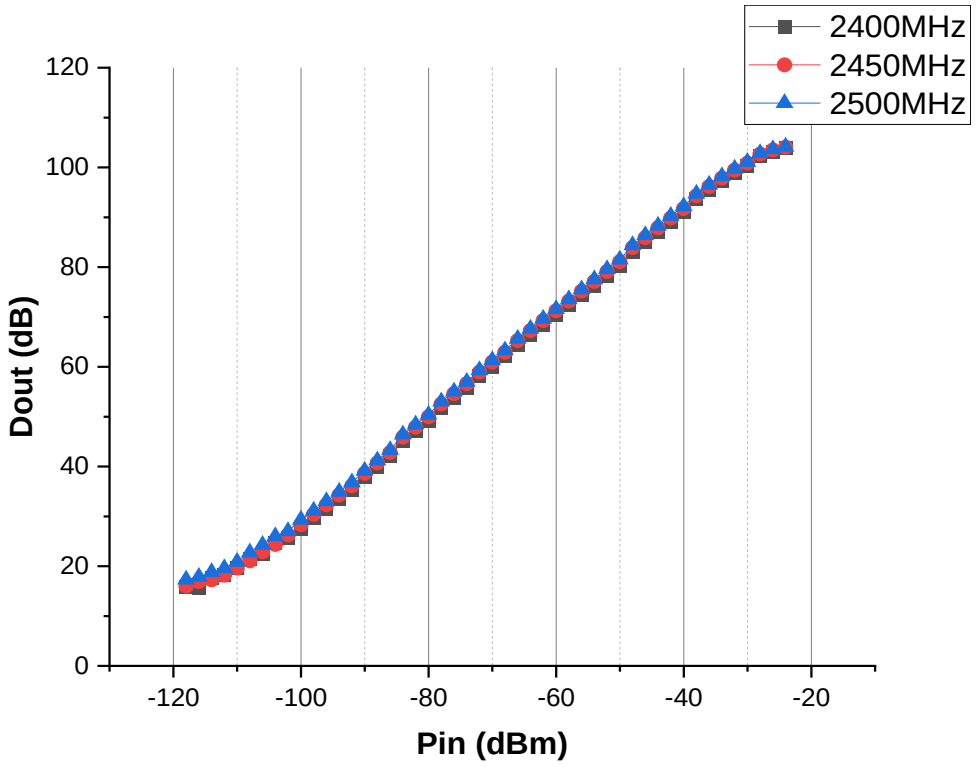


Figure 4.17: Dynamic range measurement of the receiver

estimation accuracy. 2) the necessity of pilot frequency correction.

The observed frequency spread phenomenon impacts the allocation of symbol frequencies within the system. The CFO estimation requires a clear frequency pattern for the cross-correlation process in the proposed signal processing flow (Section 4.2.2). However, frequency spreading obscures these patterns and reduces the CFO accuracy. Accordingly, the symbol frequency allocation strategy must consider the implications of frequency spread. This ensures adequate frequency spacing between symbols, thereby mitigating the CFO estimation error and enhancing the CFO/SFO robustness.

In our proposed system, correction for free-running oscillator phase noise behavior is achievable via an assisted pilot tone transmitted concurrently with the data symbols. Each data symbol is subject to unique phase fluctuation caused by the

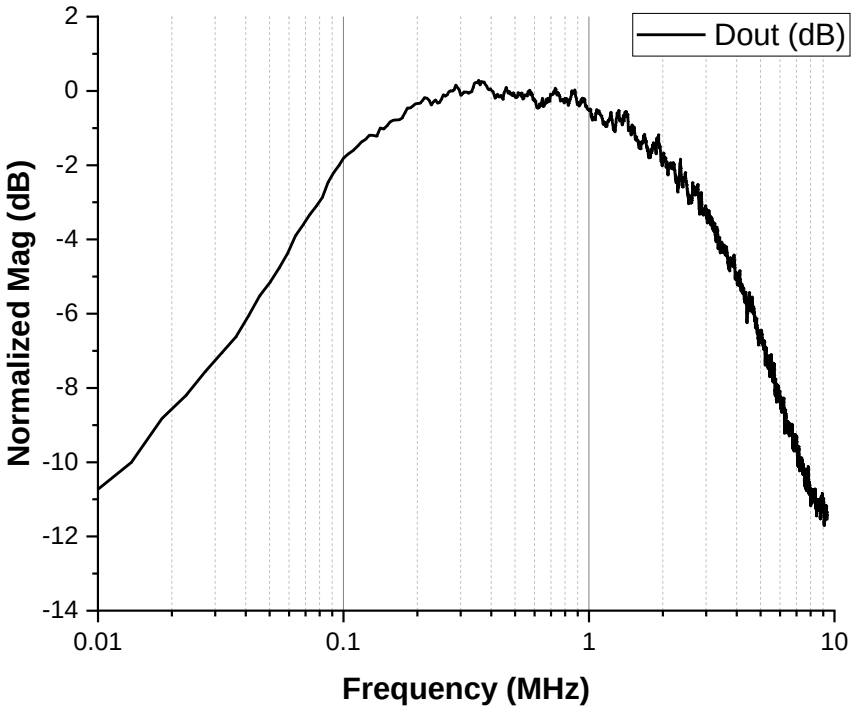


Figure 4.18: Receiver frequency response measurement

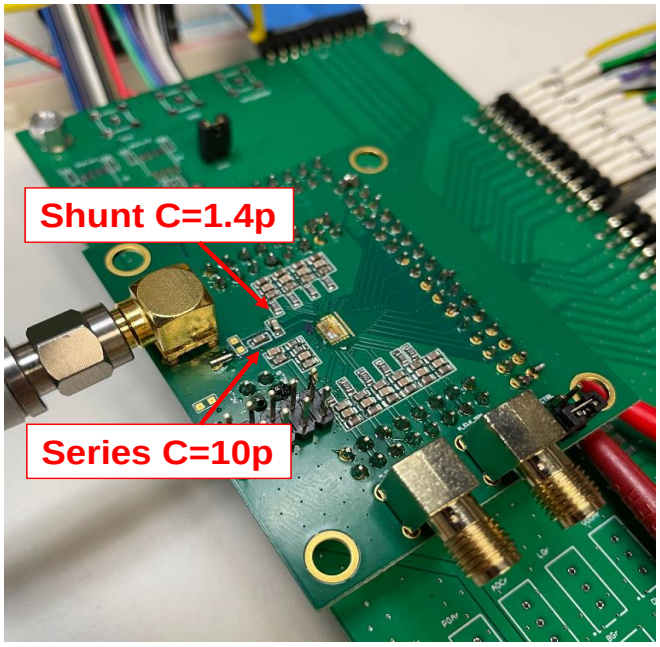
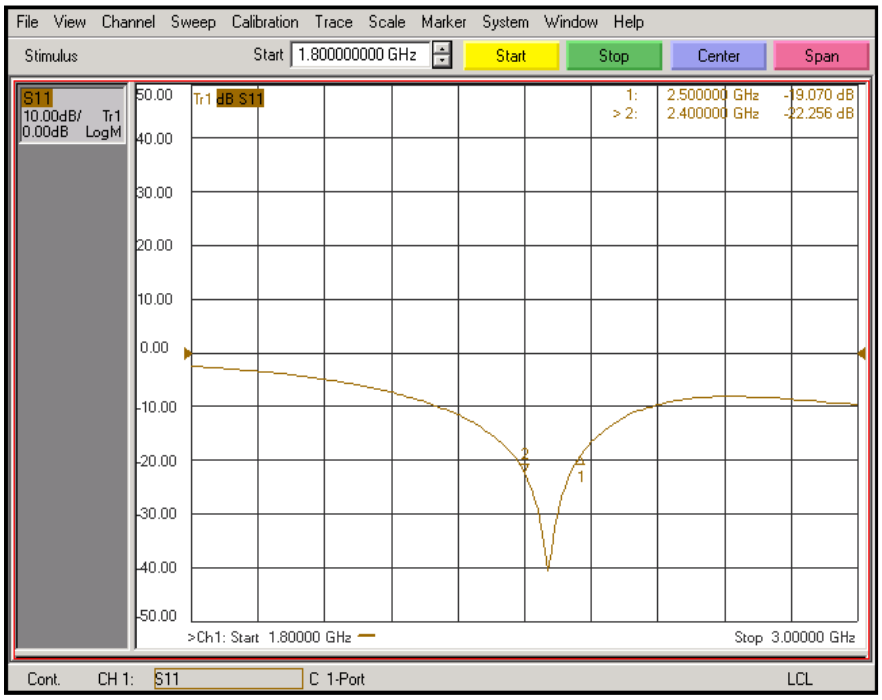


Figure 4.19: External input matching measurement setup



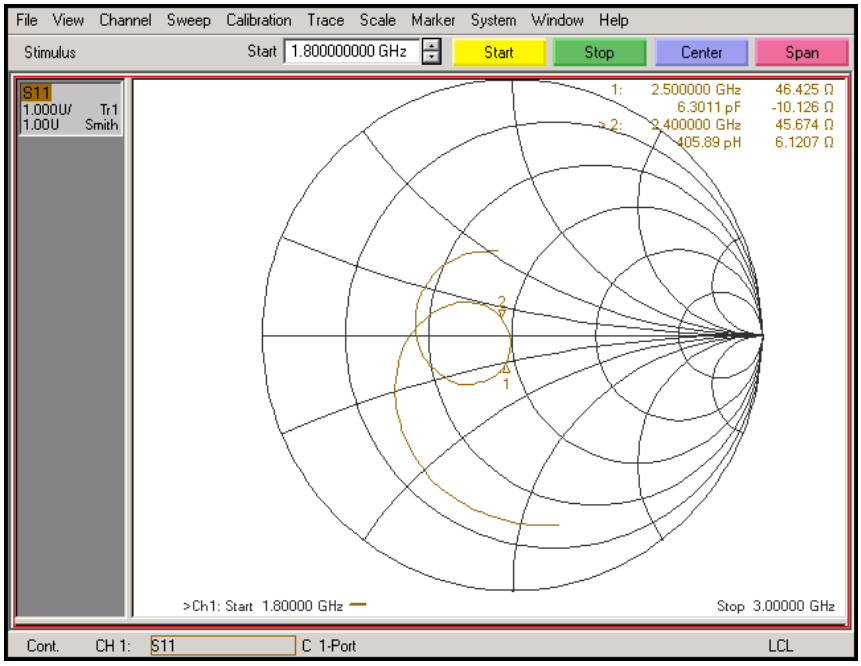


Figure 4.20: Measured S_{11} frequency response and its Smich Chart

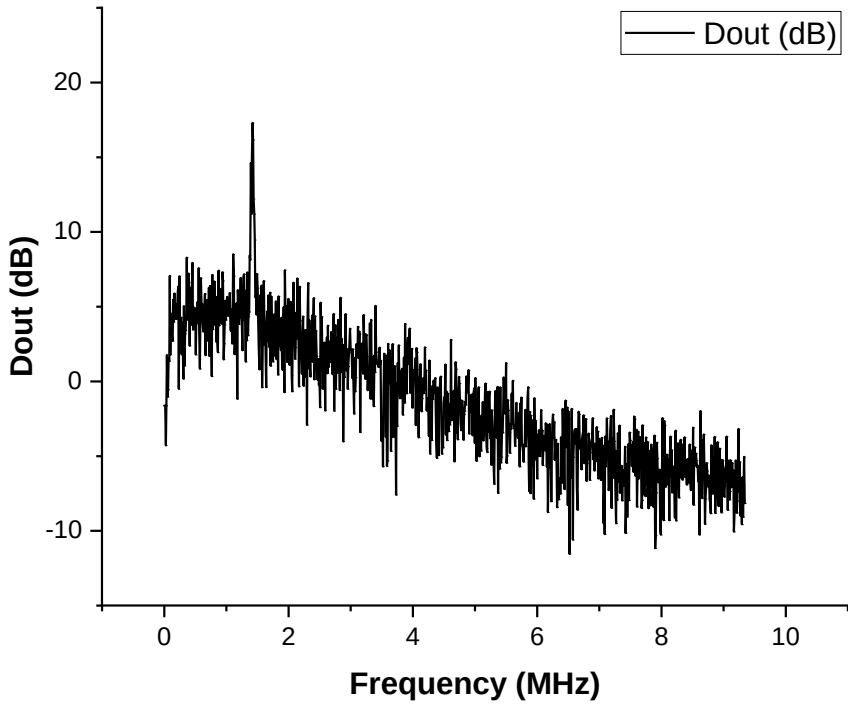


Figure 4.21: Measured sensitivity spectrum

free-running oscillator, which is continuously tracked by the pilot symbol. Therefore, it is crucial to correct the phase noise before analyzing the data symbol's magnitude and phase information. This process ensures the integrity and accuracy of the signal interpretation in the presence of oscillator phase noise.

Figure 4.23 shows the measured per window spectrum of two anchors and one tag scenario. We observed the frequency spread from the raw spectrum due to the free-running oscillator. It reveals that the frequency spread occupies +/- 40kHz. After pilot correction, referring all signals to the main pilot tone, the frequency speed is much suppressed, and the original pilot and data symbols can be recovered.

4.5 Summary and Future Work

A millimeter-scale, PLL-less, crystal-less receiver incorporating a novel signal processing technique is presented. To realize a miniaturized radio system, we employ a

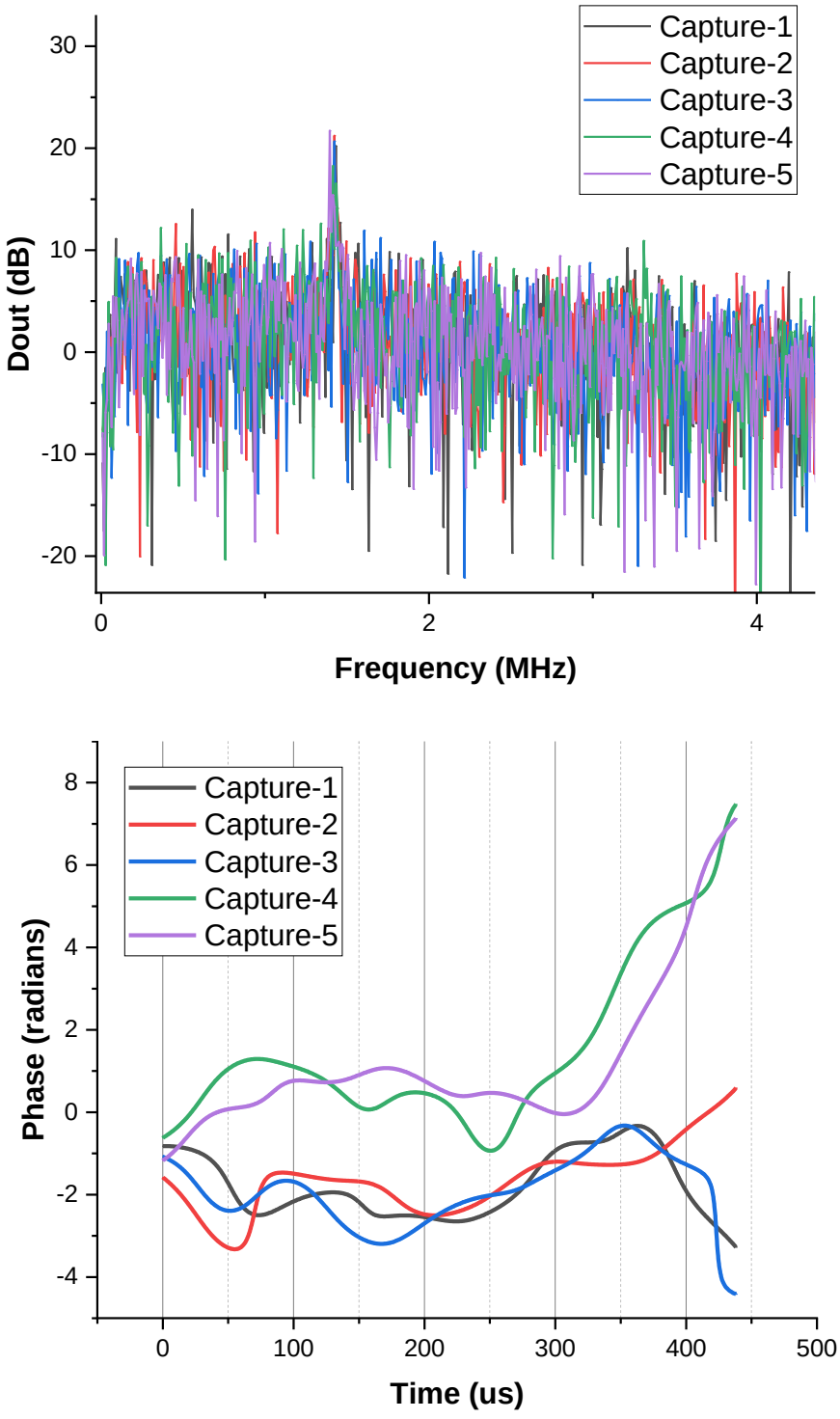


Figure 4.22: Measured frequency speed and phase response

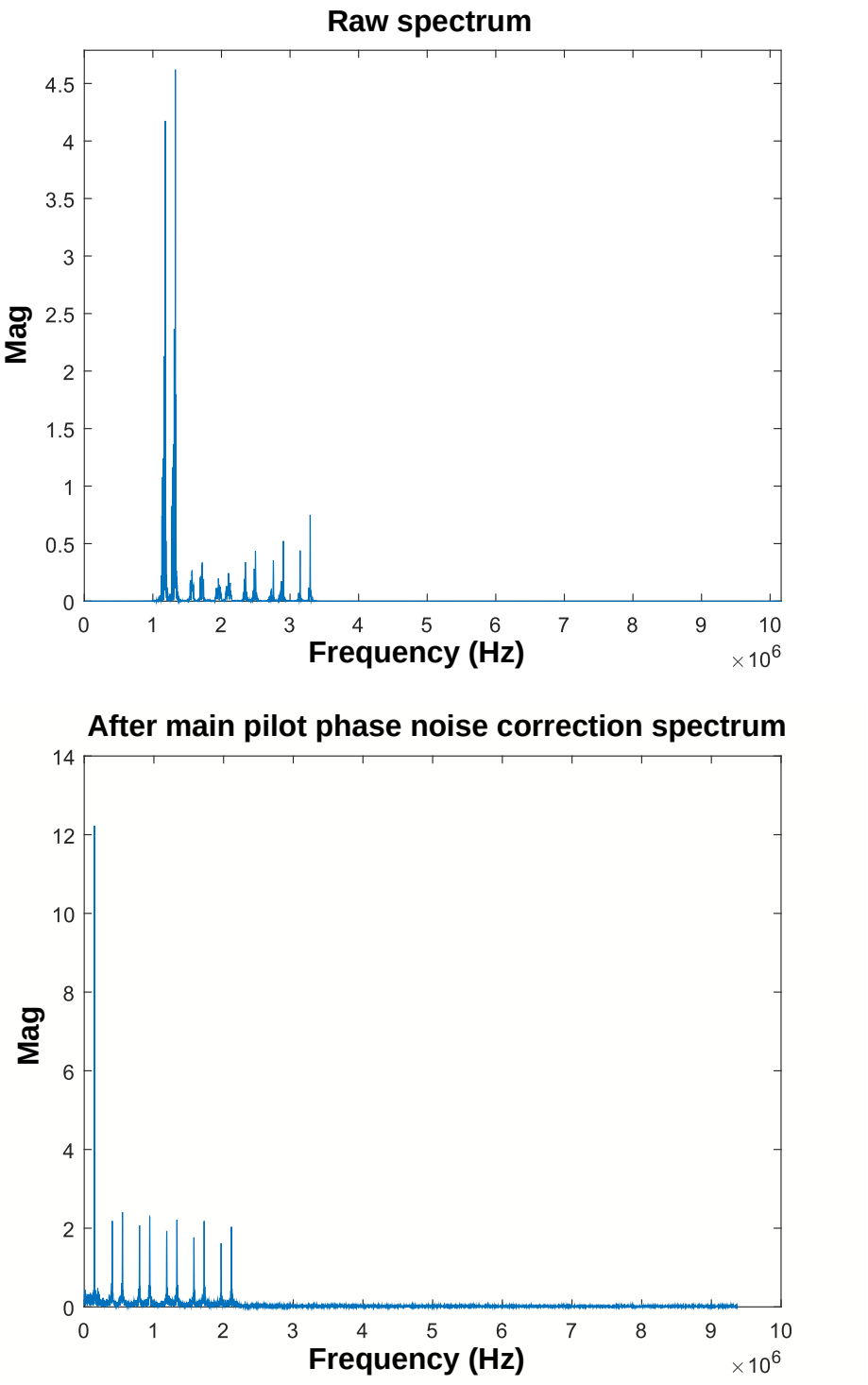


Figure 4.23: Per window spectrum and pilot correction

novel receiver architecture that utilizes a free-running oscillator to serve dually as the source of the local oscillator and the ADC sampling clock. This design allows the receiver to generate its clock internally without the need for any external components and circuits for clock generation. The tag receiver front-end chip is implemented and evaluated. It successfully demonstrates a sensitivity level of -115 dBm with 86 dB dynamic range while consuming 10 mW and occupying 4.16 mm^2 area.

This work also introduces a novel signal processing flow to address the CFO and SFO caused by utilizing a free-running oscillator as a down-conversion clock and sampling clock. A thorough simulation and real measured data have been used to verify the proposed signal processing. An ASIC digital chip will be designed and implemented to validate this new RF localization system to accelerate the signal processing flow and reduce the data footprint. We envision a complete tag receiver system that integrates the RF and digital chip into a millimeter-scale size device, enabling the potential for effective deployment in IoT applications.

CHAPTER V

Conclusion and Future Directions

5.1 Summary of Contributions

This dissertation focuses on the challenges of IoT end devices, particularly in their use for localization systems. It outlines three primary challenges: 1) managing limited bandwidth and substantial interference; 2) pursuing an energy-efficient, cost-effective, and compact device; and 3) overcoming the limited communication and localization range. IoT device development has consistently aimed to achieve low power consumption, low cost, and small size. This pursuit remains critical for circuit design, demanding a continued call for circuit innovation. As the number of devices grows and continues to share the finite spectrum resource, balancing bandwidth and interference becomes a significant challenge in communication system design, signaling the need for technological breakthroughs. When applying IoT devices for localization service, the performance is limited by the available power provided by the battery sources, restricting communication and localization range. This dissertation investigates the potential of unprecedented circuits and systems to address those challenges.

Chapter II proposes a novel reconfigurable analog-FIR filter with an 11-bit charge-domain DAC, implemented with hybrid time- and gm-DAC. This work enables unprecedented flexibility in bandwidth and out-of-band rejection adjustment for the narrowband receiver to accommodate various wireless standards. The major contri-

butions of this work include: 1) Achieving an unprecedented -70 dB rejection and sharp transition in FIR filter structure; 2) Demonstrating a highly programmable bandwidth (0.37 to 4.6 MHz) and out-of-band rejection (-50 dB to -70 dB); 3) Low power consumption of a maximum of 356 uW with efficient power scaling across various configuration settings.

Chapter III proposes a novel narrowband RF localization system with a PLL-less tag receiver and a novel post-signal processing. This work demonstrates using a narrowband frequency hopping scheme for long-range localization while removing the need for PLL, thus a crystal oscillator, for clock generation in the tag receiver. The major contributions of this work include: 1) Demonstrating a long-range localization system with an LOS capability of 621 meters and a decimeter accuracy of 0.6 meters. 2) Showing the PLL-less tag receiver that operates using a novel post-signal processing technique to correct RF impairments; 3) Achieving a low power (3.9 mW) and compact (0.85 mm^2) tag receiver front-end that operates without the need for a crystal oscillator.

Chapter IV presents a fully integrated tag receiver with 10-bit ADC that features all necessary clocks generated internally. This work demonstrates the idea of using the divided-down local oscillator clock as an ADC sampling clock and introducing a novel signal processing technique to compensate for the non-ideal SFO and demodulation of data symbols. The major contributions of this work include: 1) A novel signal processing technique for correcting the CFO and SFO in the PLL-less and crystal-less frequency hopping receiver; 2) Demonstrating a fully integrated tag receiver with -115 dBm sensitivity and 86 dB dynamic range; 3) Enabling a fully integrated millimeter-scale radio system for long-range localization.

5.2 Future Directions

This dissertation presented several critical technological advancements for future IoT circuits and systems. Each work has proven successful at every stage—from algorithm development, system design, practical implementation, and final validation. Moving forward, multiple directions could be explored to unleash the system's capabilities.

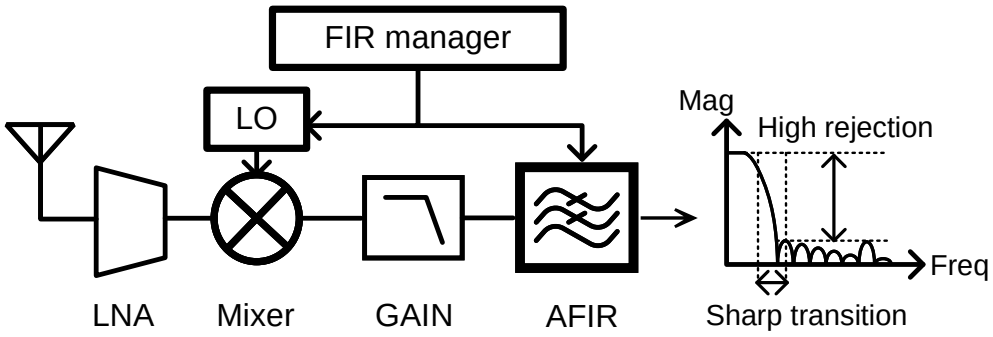


Figure 5.1: High channel selectivity and low power recevier

First, time-domain processing with different physical domains shows great promise in achieving high-resolution quantization. Our research primarily focused on the baseband filter. We quantize the coefficients and allocate part of the coefficients to process in time. Such time-related information can be further applied to the down-conversion LO signal, which is easier to quantify due to its naturally high frequency. Therefore, co-designing and strategically deploying the FIR coefficients across LO, baseband time-DAC, and baseband gm-DAC can be a valuable research topic. Figure 5.1 shows the proposed concept. We envision this receiver architecture can demonstrate exceptional channel selectivity. This could revolutionize the standard requirements for narrowband communication systems, paving the way for more advanced and capable IoT devices.

Second, we aim to create a self-contained millimeter-scale tag receiver system that

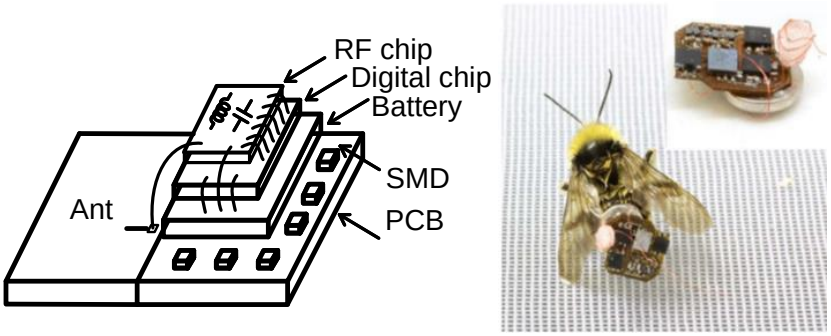


Figure 5.2: Fully integrated mm-scale tag receiver system for insets tracking

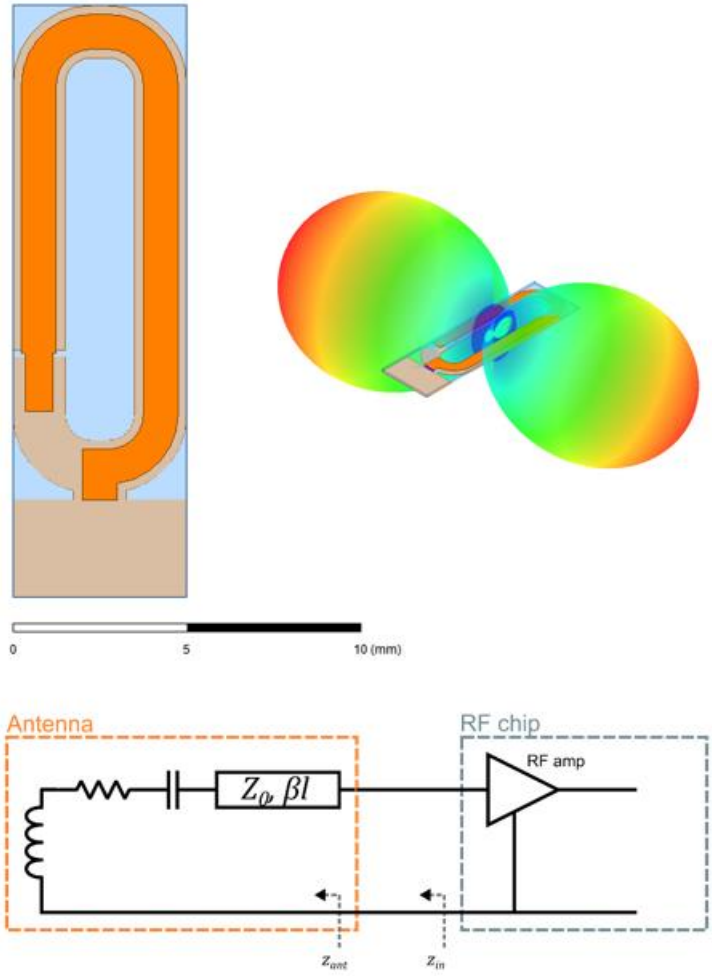


Figure 5.3: Skinny loop antenna

integrates the front-end chip, digital chip, antenna, and battery. Our research already demonstrates a tag receiver with all required clock signals generated internally. This receiver works alongside a novel signal processing to correct the RF and baseband impairments. Its next development phase involves implementing a specialized digital chip, accelerating the processing time, and reducing the data footprint that needs to be communicated externally. Figure 5.2 shows the proposed concept. The digital chip is also designed to store localization information on-chip, allowing the tag to record its spatial trajectory and effectively capture its movement over time. Figure 5.3 shows the resonant planar shielded microstrip loop antenna [110–113], which could integrate into the system. This long-range, mm-scale tag device opens up possibilities for applications such as tracking data assets or insects [114] across extensive areas.

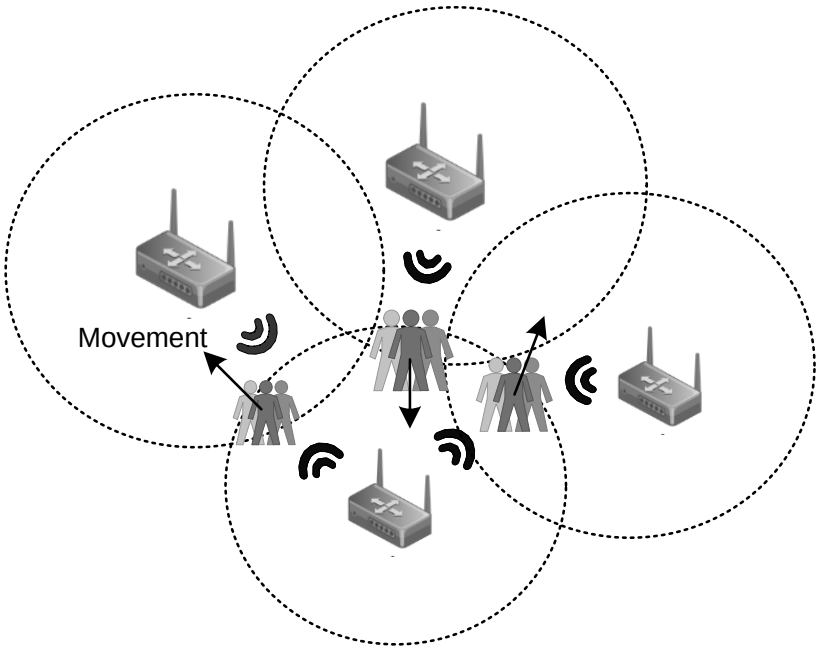


Figure 5.4: Multi-anchor and multi-user tracking system

Third, we propose to expand the setup to include more anchors and tags to facilitate localization in higher dimensions with numerous users. Our research demon-

strates an example of two anchors and a single tag receiver working together, using TDoA to pinpoint a location within 1-D space. By introducing additional anchors whose positions are predetermined, we can extend our approach to achieve localization in 2-D or 3-D space. Moreover, including extra anchors can improve the precision of the localization, which can be achieved by disregarding weaker signals or collectively estimating the position based on multiple data points. Ideally, the system can simultaneously determine the positions of an infinite number of tags. The tag receivers only collect data from the anchors; they operate without causing any interference with others. Figure 5.4 shows the proposed concept. The ability of concurrent localization is extremely valuable as it allows for the monitoring and recording of the movement of large-volume tags over a long period in a large area.

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