Simultaneous Switching Noise in Printed Circuit Boards: Electromagnetic Modeling/Simulation

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Simultaneous Switching Noise in Printed Circuit Boards : Electromagnetic Modeling / Simulation

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1 Parasitic Extraction

This document describes the progress in our study from October 1994 to October 1995. The developed program can analyze a given circuit board and compute switching noise at different locations. The procedure is based on a powerful tiling approach which will be described in detail in the following sections.

For the sake of clarity, the progress report will start with a description of the tiling procedure as it has been applied to a simple PCB geometry made only of a power and a ground plane. Following this, a detailed discussion will be given on the computation of equivalent circuits for the various resulting tiles and the development of a HSPICE file by appropriate combinations between the derived electrical circuits. After the completion of this discussion, a description of the tiling process on a multilayer printed circuit board will be given along with schematic pictures to help in the understanding of the approach. Finally, the presented approach will be applied to a variety of examples and accuracy along with computational efficiency will be discussed. The report will conclude with a presentation of data showing switching noise at various points on the power and ground planes of some example PCBs, a discussion of the findings and description future work.

The parasitic extraction technique of the printed circuit boards (PCBs) may be divided into three categories, which are packaging modeling, power/ground/signal plane modeling, and chip driver modeling (see Figure 1). In this section of the report, we summarize some of the basic concept of the electromagnetic (EM) aspect of the packaging and power/ground/signal plane modeling procedures. The modeling procedure is based on a *tiling* approach, aims at the understanding of possible sources of ground bounce and attempts an effort to visualize the potential distribution on the power and ground planes. In the following subsections, we will describe in detail the basic step of EM modeling including the underlying assumptions and modeling procedures.

1.1 Equivalent circuit for power and ground plane

Power and ground planes are the basic components of the PCBs. In our approach, these planes can be considered as sections of a parallel plate waveguide. For our problems of interest, due to geometrically small dimensions of the separation between the planar conductors and the clock rates which do not exceed 1 GHz, the parallel plate waveguide supports only a transverse electromagnetic (TEM) wave while evanescent higher modes are so weakly excited that can be practically considered non-existent. Under these assumptions such a line can be represented very effectively a simple N-port network. In our case, it is modeled as a 4-port RLC network as shown in Figure 2.

For the measurement of power and ground plane potential fluctuation, especially for the measurement of the ground bounce, we adapted special type of equivalent circuit representation. The vertical capacitor takes into account the capacitive effect of the two conductor planes. The eight series inductor and resistor pairs take into account the effect of the two orthogonal current components flowing on top and bottom walls. A detailed description of the derivations followed for the computation of the inductive, capacitive and resistive elements of this equivalent circuit is given in the next section. The appropriate values of the equivalent network parameters can be easily found assuming the dominant mode (TEM) operation condition.

1.2 Equivalent circuit for power and ground pins

To model power and ground pins, appropriate inductance and capacitance values are computed from the finite element method (FEM). The inductance of the pin is dependent on the length and diameter of each pin and the capacitive effect between pin and hole in the power plane is mainly function of diameter of pin and hole. The inductance values of specific size vertical pins are computed from the one-port via grounding structures (refer last year report). The equivalent circuit for the power and ground pins connecting a current source to power and ground planes is shown in Figure 3. For the effective modeling of this kind of structure, we have applied

the Finite Element Method and we have used the data to develop an appropriate macro-model which will provide very effectively the equivalent circuit for a driver pin as a function of geometrical characteristics.

1.3 Equivalent circuit for signal lines

The signal line between two conducting planes is modeled as a stripline placed halfway between the two planes (see Figure 4). As with the simple power/ground plane tiles, in the case of a stripline tile, an equivalent circuit is developed which can take into account the potential fluctuations on the power and ground planes through inductances placed as shown as shown on the figure. In addition to inductive elements, capacitive and resistive elements are added to the equivalent circuit to take into account the necessary capacitive effects in addition to ohmic loss.

1.4 Equivalent circuit model extraction procedure

An appropriate discretization procedure is performed under the given geometrical and electrical data such as the size of printed circuit board (PCB), material constant, thickness, via dimension, and frequency components in the input signal. After discretizing the PCB, the equivalent circuit for each small tile is found using various methods including 3-dimensional FEM and these equivalent circuits are electrically connected to each other for circuit simulation. In addition to these equivalent circuits for the tile structures we discussed, equivalent circuits for the input sources, connectors, and power/ground pins are also included.

The information of all of theses equivalent circuits are recorded in a HSPICE input file and circuit simulation is performed in time or frequency domains. ¿From the circuit simulation step, the potential distribution on the power and ground planes is computed. Also, the input impedance at the driving port can be easily extracted from the voltage and current information.

The overall procedure is summarized in Figure 5. The dotted box in the figure shows the part of the program which divides the structure into tiles and derives the

appropriate equivalent circuits. Various geometries require different modeling techniques depending on the structural complexity of the of the tile For examples tiles including only power and ground planes or signal lines were treated through transmission line theory. Vias connecting various planes and source pins were characterized through FEM.

2 Derived Formulas of the Equivalent Circuit Models for Several Different Geometries

In this section, we will present more detailed expressions for each of the equivalent circuits in the previous section.

2.1 Parallel Plate : Power and Ground Planes

To derive an equivalent circuit model for parallel plate waveguide and take into account the floating potentials on power and ground planes, special type of equivalent circuit shown in Figure 2 is devised. Since an arbitrary surface current can be decomposed into two orthogonal components, we can determine two two-port networks one for each direction. The equivalent inductances and capacitances for each two-port network is found by matching the scattering parameters between the corresponding two-port transmission line and the equivalent circuit shown in Figure 2:

$$\omega L = \frac{60\pi h}{W\sqrt{\epsilon_r}} \sin\left(\frac{2\pi\sqrt{\epsilon_r}}{\lambda_o} D_1\right) \tag{1}$$

$$\omega C = \frac{W\sqrt{\epsilon_r}}{120\pi h} \tan\left(\frac{\pi\sqrt{\epsilon_r}}{\lambda_o} D_2\right) \tag{2}$$

where the geometrical factors, D_1, D_2, and W are defined in Figure 6. In equation (2), h and ϵ_r are the thickness and dielectric constant of the PCB, respectively. As we can recognize from the above expressions, the inductance and capacitance are frequency dependent quantities. However, these are almost constants when the size of each tile is relatively small compared to the guided wavelength. As frequency

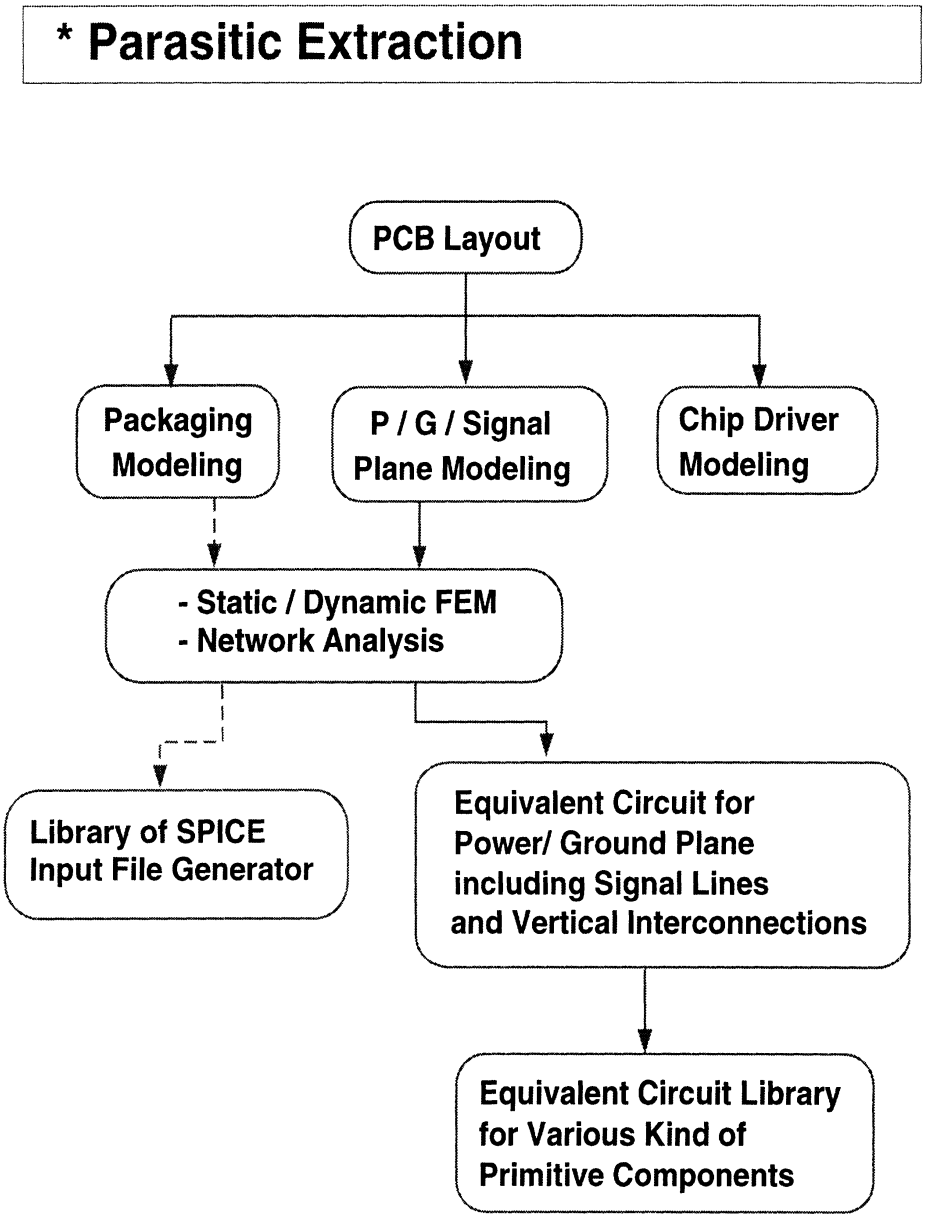


Figure 1: Parasitic extraction procedure

*** Equivalent Circuit for Power / Ground Planes**

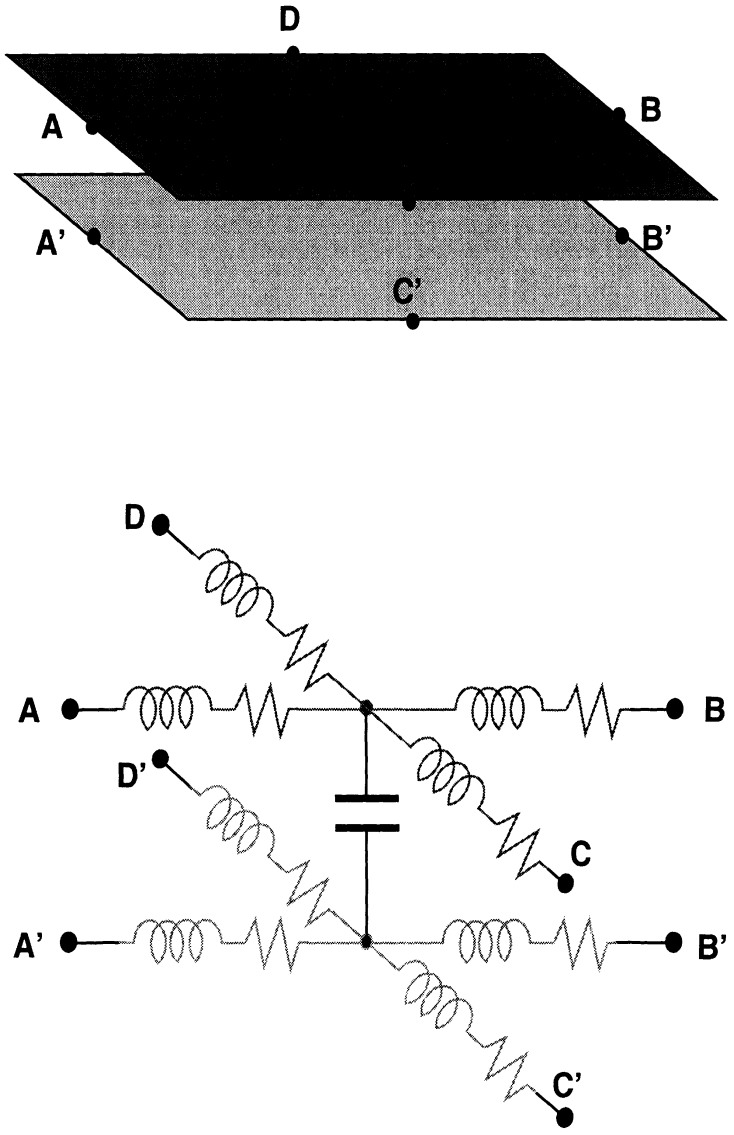


Figure 2: Equivalent circuit for power and ground plane

*** Equivalent Circuit for Power and Ground Pins**

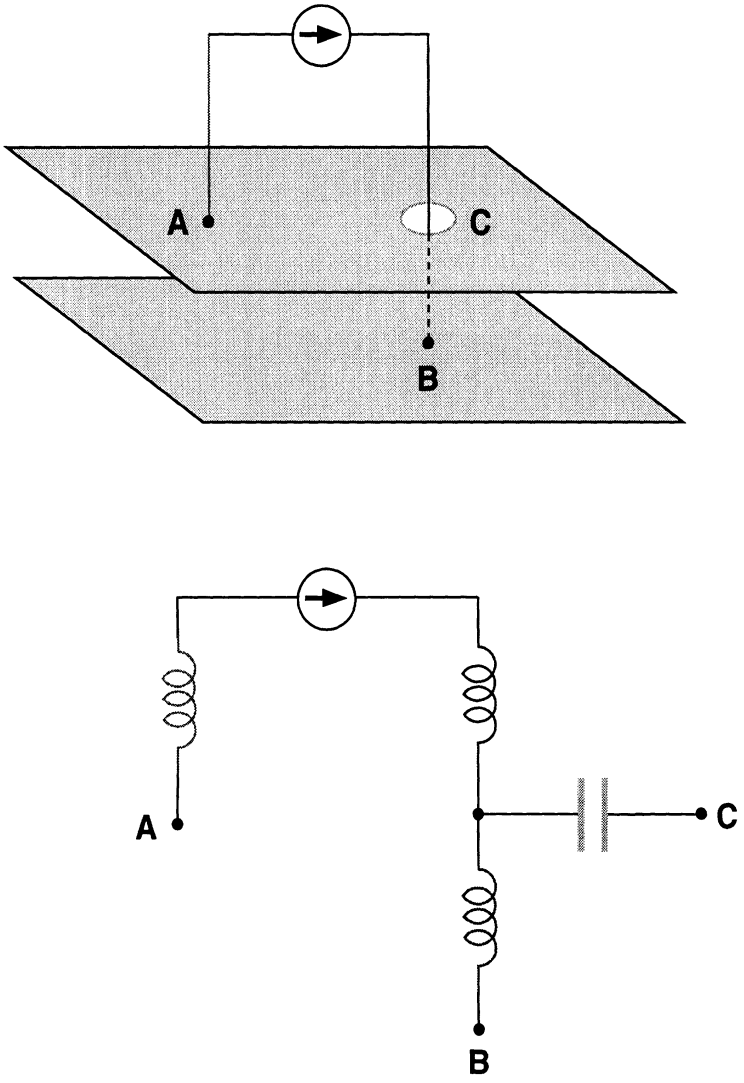


Figure 3: Equivalent circuit for power and ground pins

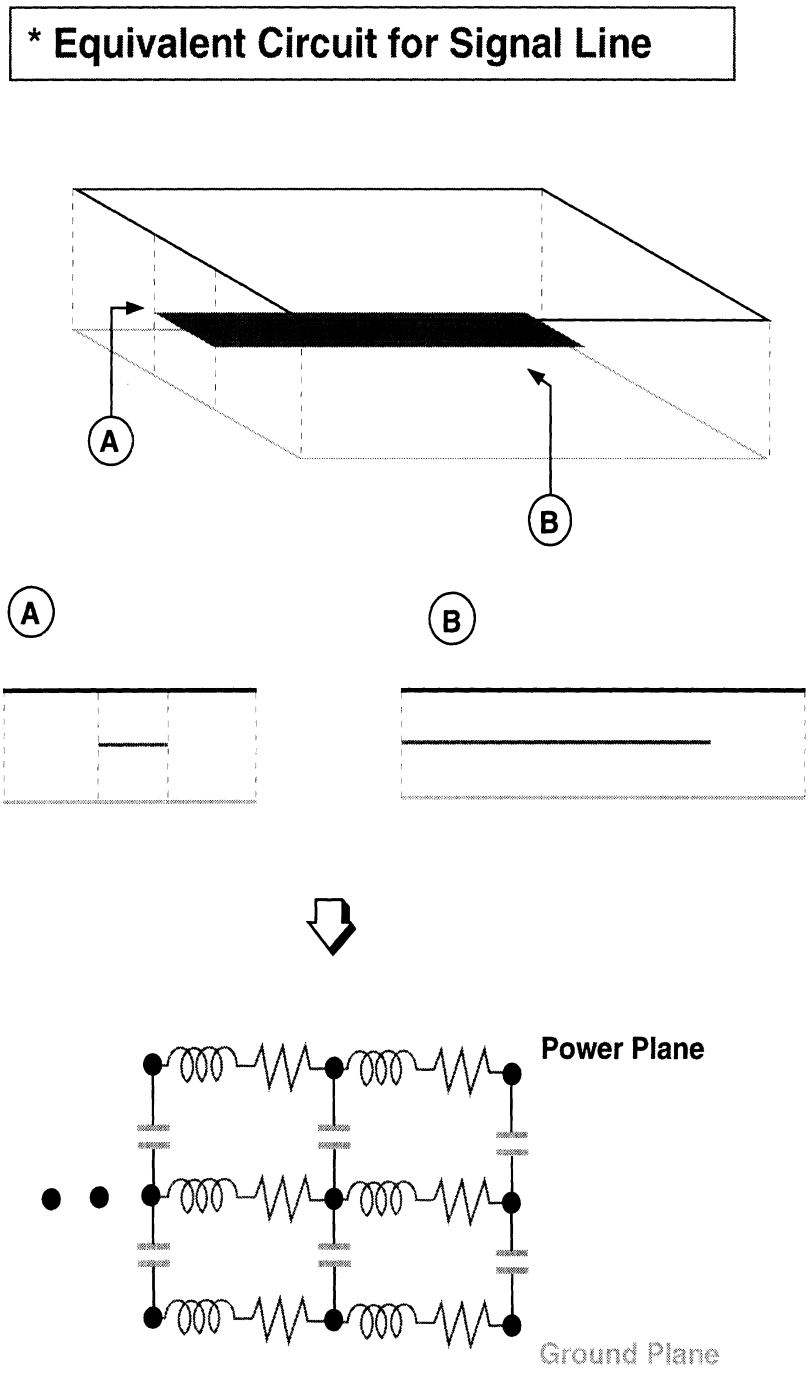


Figure 4: Equivalent circuit for signal lines

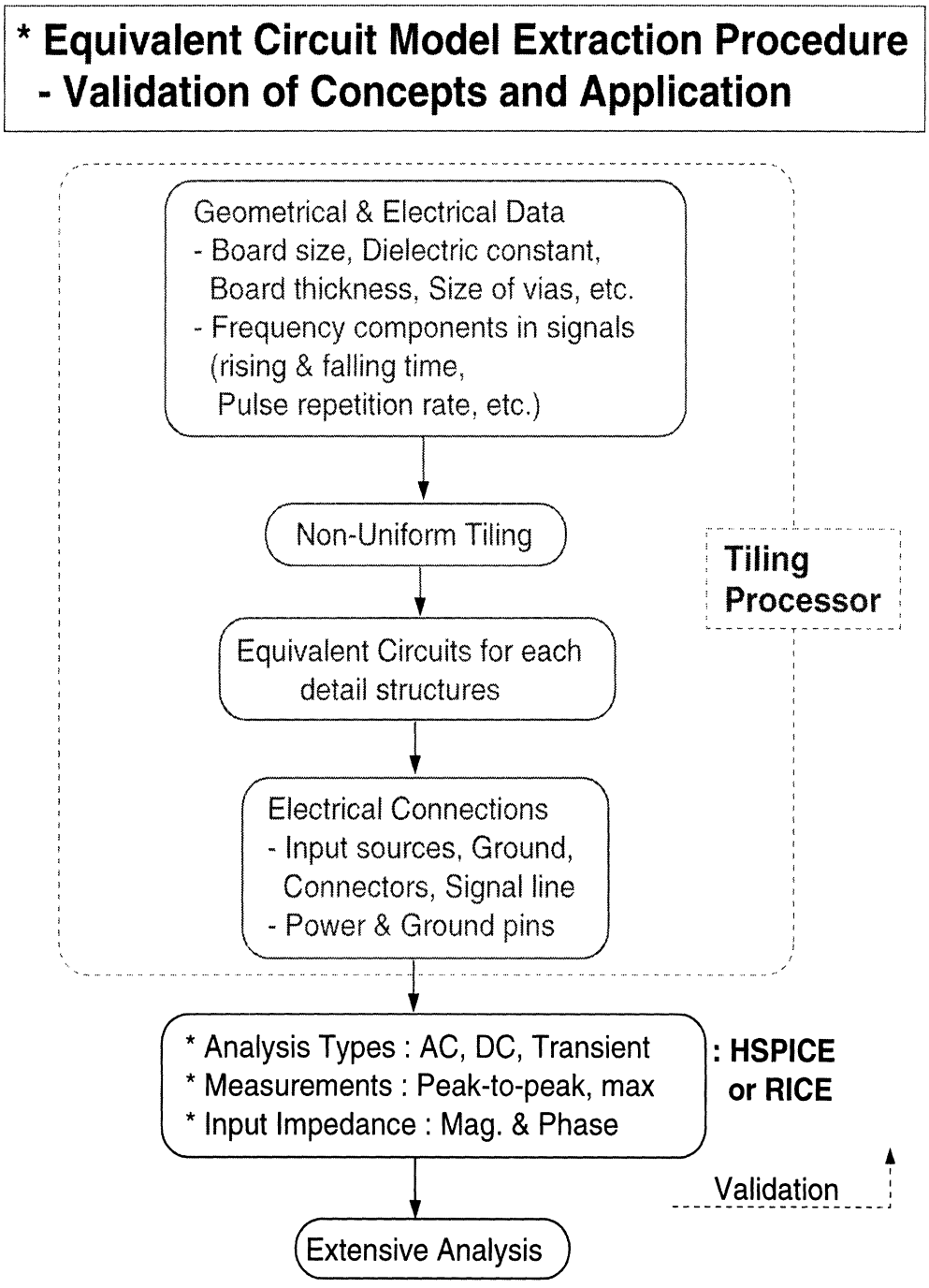


Figure 5: Equivalent circuit model extraction procedure

increases, however, the inductance and capacitance values can vary according to the geometrical factors. If we consider TEM mode operation, then we have to keep the size of tile smaller than a fraction of guided wavelength.

Under the assumption that the tile size is much smaller than the wave length of the operating frequency, that is, $\beta_g D_1$ and $\beta_g D_2 << 1$, the above equations can be reduced to more compact form.

$$L = \frac{60\pi h}{c}(\frac{D_1}{W}) \tag{3}$$

$$C = \frac{W D_2 \epsilon_r}{240\pi h c} \tag{4}$$

where c is the speed of light in vacuum. From the above equations, we can recognize that the inductance of the network is directly proportional to the path length and inversely proportional to the width of the current path. Similarly, the capacitance is proportional to the tile area, WD_2, and material constant, ϵ_r, and inversely proportional to the thickness of the PCB.

2.2 Signal Line Between Power and Ground Planes

To derive equivalent circuit for a signal line residing halfway between the two conducting planes, we considered the structure as a stripline. First of all, the characteristic impedance of the stripline is evaluated from the empirical formula. Second, an equivalent T-network is constructed for a transmission line of length l and width W as shown in Figure 7. The effect of the width of the transmission line and the fringing fields are included in the characteristic impedance Z_o as shown below. After the characteristic impedance and propagation constant are determined (step I), an equivalent T-network, with a series inductance and shunt capacitance, may be derived. From this equivalent circuit, we can extracted the values of capacitance and inductance in Figure 7 (step II).

- Step I : Characteristic Impedance

$$Z_o = \frac{30\pi}{\sqrt{\epsilon_r}} \cdot \frac{1}{(W_e/H) + 0.441} \tag{5}$$

$$\frac{W_e}{b} = \frac{W}{H} - \begin{cases} 0 & \text{if } W/H > 0.35 \\ (0.35 - \frac{W}{H})^2 & \text{if } W/H < 0.35 \end{cases} \quad (6)$$

- Step II : Capacitance and Inductance

$$\omega L = Z_o \cdot \frac{1 - \cos(\beta l)}{\sin(\beta l)} \quad (7)$$

$$\omega C = \frac{\sin(\beta l)}{Z_o} \quad (8)$$

The equivalent inductance and capacitance are not frequency dependent as it happens in the the parallel plate waveguide model. This is easily seen from equation (7) and (8) if we observe that for βl much smaller than 1.0, as it happens in the given problem, the above formulas simplify to the following:

$$L = \frac{Z_o l \sqrt{\epsilon_r}}{2c} \quad (9)$$

$$C = \frac{l\sqrt{\epsilon_r}}{Z_o c}. \quad (10)$$

At the first glance, the inductance of the equation (9) looks like dependent upon the dielectric material in contrast to general concept. However, after combining the equation (5) for characteristic impedance, it becomes clear that the inductance is independent on the dielectric material.

2.3 Power and Ground Pins : Vertical Via Holes

For a given geometry, the equivalent inductance and capacitance are evaluated from the finite element method (FEM) or simplified analytic expressions. As shown in Figure 8, the radii of the vertical conductor and hole in the power plane and the length of the conductors are important factors to determine the values of the inductance and capacitance. The inductance of the vertical via hole is proportional to the length of the line and insensitive to frequency. Moreover, as diameter of the vertical via or pin increases, the inductance of the structure is decreased due to the increased possible current path. For more efficient computation, an appropriate macro-model function will be developed as a function of geometrical factors (a, b, and H) and material properties (ϵ_r).

2.4 Sample PCB Layout and Modeling Example

To show the concept of the tiling approach used herein and its effectiveness, a test PCB geometry is discretized into smaller pieces (*tiles*) and substituted with appropriate equivalent circuits (see Figure 9). All of these equivalent circuits of the each fine structures of the PCB are interconnected for the HSPICE input network. The tiling processor can discretize into uniform or non-uniform tiles and has the capability to model multiple layer PCBs with arbitrary number of signal lines as shown in Figure 10.

2.5 Discretization of Multi-layer PCB

Figure 10shows the discretization of a multi-layer PCB. First, the important features of all the layers are projected onto the top plane. After that projection, discretization procedure can be applied while keeping the position of all the important features, such as, nodes and direction of signal lines. After the discretization has been performed, the tiles are unfolded and N layers of nodes are introduced. The equivalent circuits of the n-layered tiles are then computed by appropriate combination of the equivalent circuits of the 2-layered tiles described earlier. The resulting HSPICE file is then run to compute the switching noise at any point of the N layers of the printed circuit board.

3 Numerical Example : Preliminary Verification

In this section, we chose a simple but practical example to verify the tiling approach described in the previous sections. As shown in Figure 11, the test PCB has two conducting planes, power and ground, and one current source connected to the two planes through pins. The one end of the current source is connected to the power plane and the other end is connected to the ground plane passing through a hole in the power plane. The overall size of the PCB is 50 mm by 50 mm and the positions of power and ground pins are given in the figure ($a1 = a2 = b1 = b2 = 5.0$ mm). The

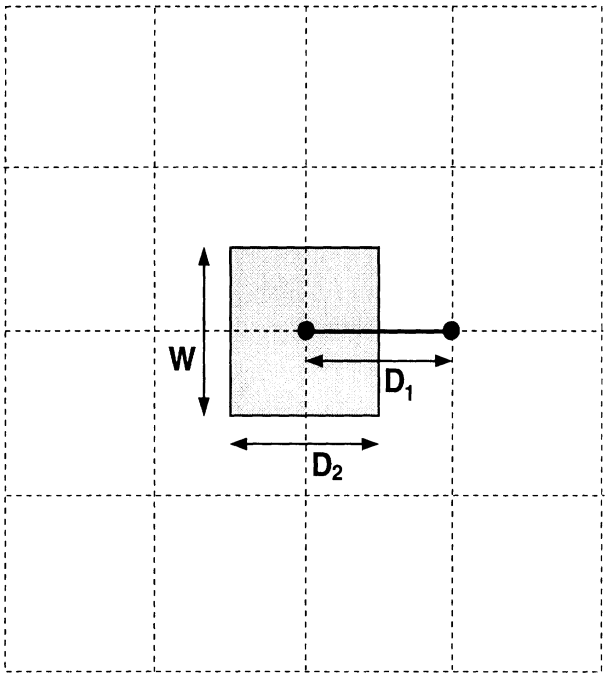


Figure 6: Parallel Plate : Top view of the power and Ground Planes

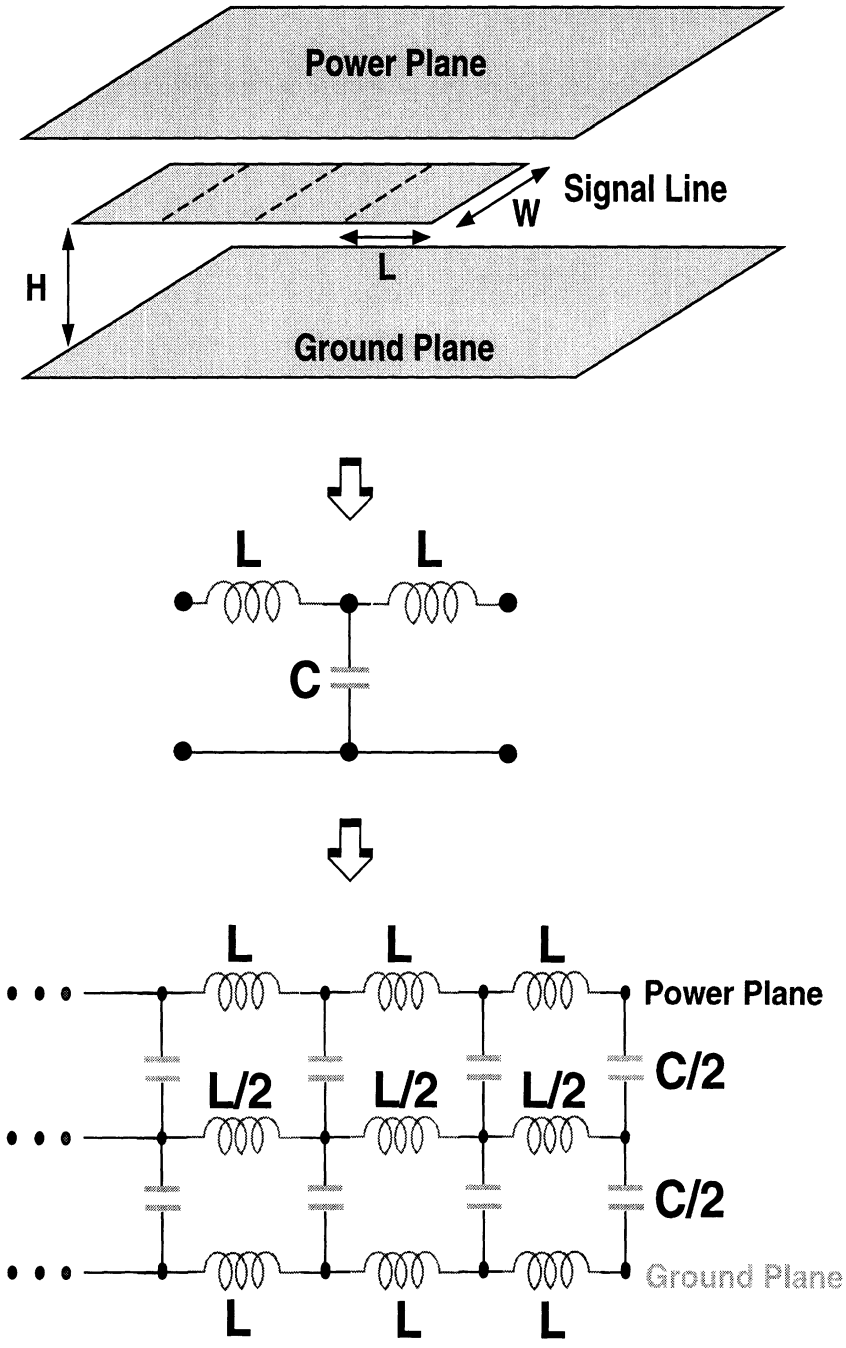


Figure 7: Signal Line Between Power and Ground Planes

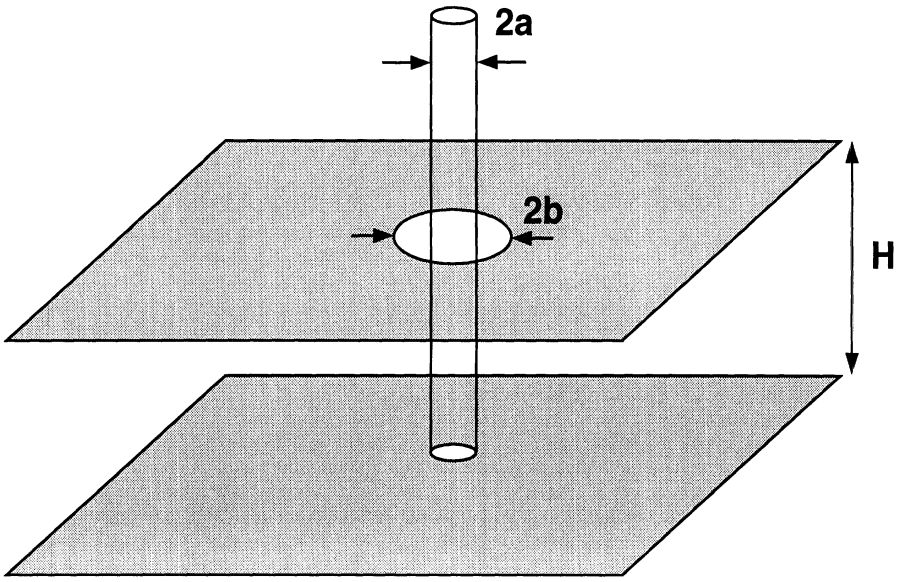


Figure 8: Power and Ground Pins : Vertical Via Holes

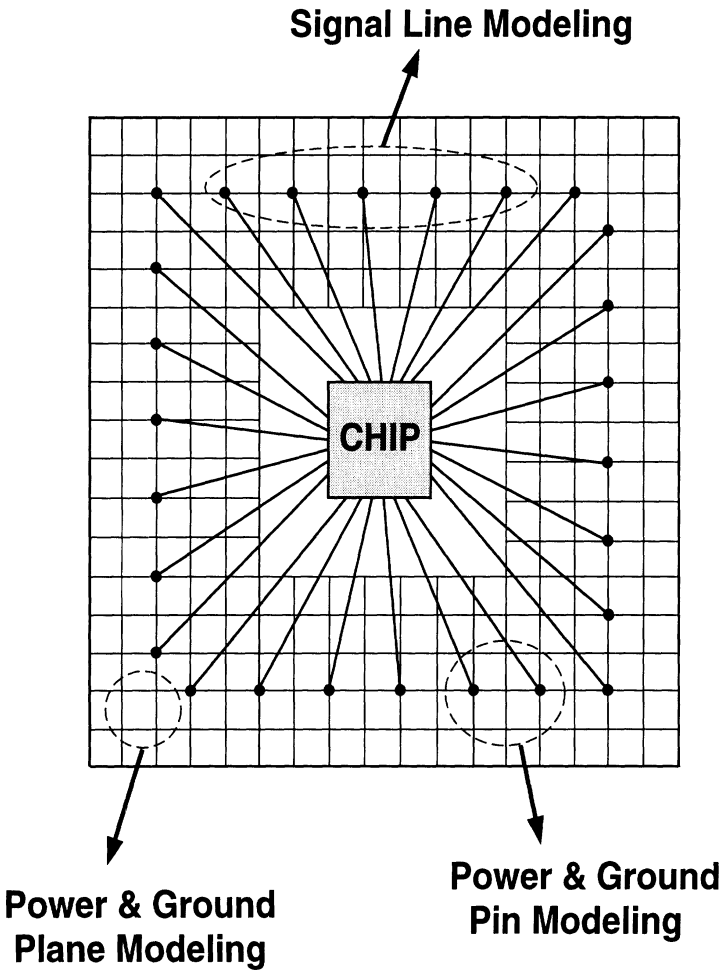


Figure 9: Sample PCB Layout and Modeling Example

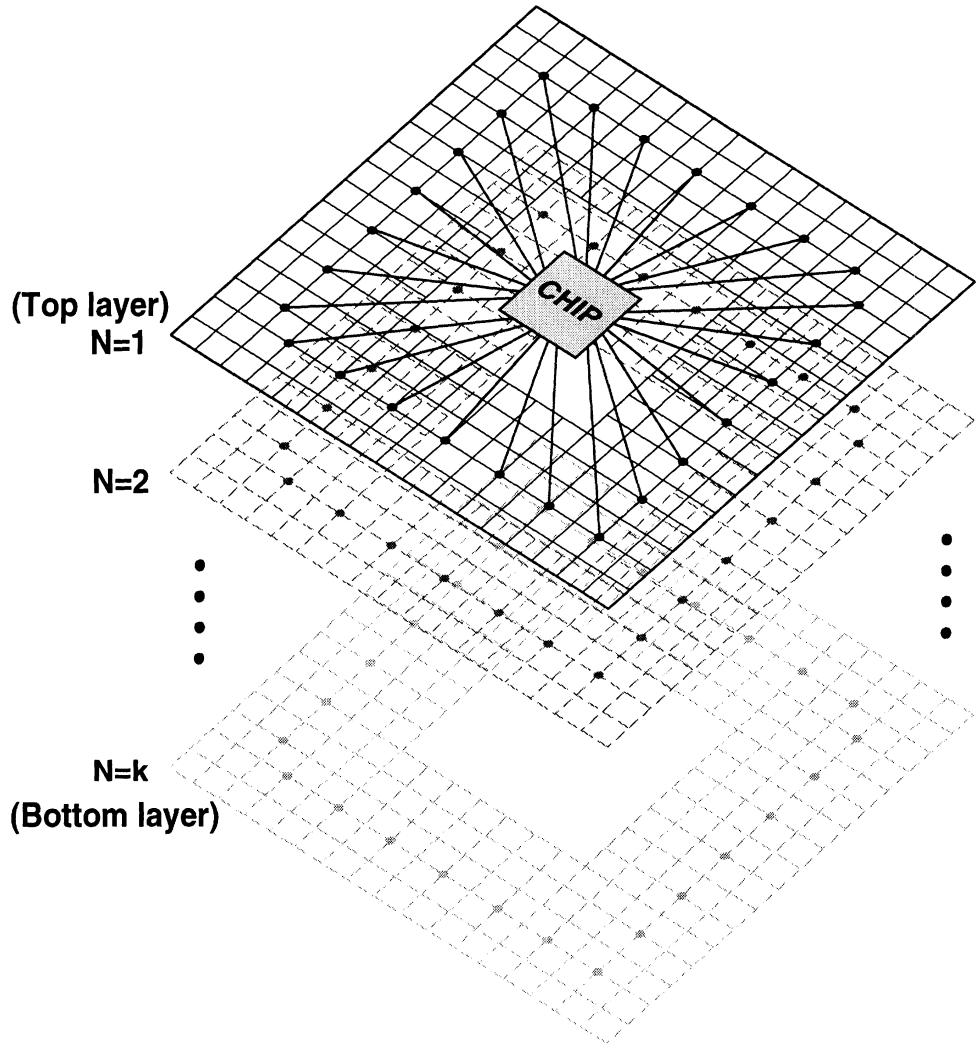


Figure 10: Discretization of Multi-layer PCB

size of hole in the power plane is set to have $d = 0.5$ mm and the length of the power and ground pins is 1.0 mm. We also connected the connector at one of the four sides and the potential at the connector position is fixed t 3.3 V and 0.0 V for the power and ground planes, respectively.

As an input current excitation, a trapezoidal pulse is used as shown in Figure 12. The rising and falling times of the pulse are set to have 0.1 nsec, pulse duration is 1.0 nsec and the magnitude is 1.0 mA. Also, the pulse period is set to 2.0 nsec. The frequency components contained in the pulse are also shown. As we can see from this figure, the trapezoidal pulse contains high as well as low frequency components. According to the frequency spectrum of the pulse, 500 MHz is used as an extraction frequency.

The size of discretization is varied from a coarse mesh to dense mesh to check convergence and accuracy. The memory requirements and computation time is also studied carefully to find optimum discretization rate. After the circuits are excited with trapezoidal pulses, the maximum potential distribution is computed on the power and ground planes.

3.1 Convergence Test

As a validation of the *tiling* procedure, convergence tests are performed for different types of discretizations. The relevant geometrical and electrical factors are summarized in the following :

- Current source : trapezoidal pulse
  - rising and falling time = 0.1 nsec
  - pulse duration = 1.0 nsec
  - pulse period = 2.0 nsec
  - magnitude = 1.0 mA
- PCB

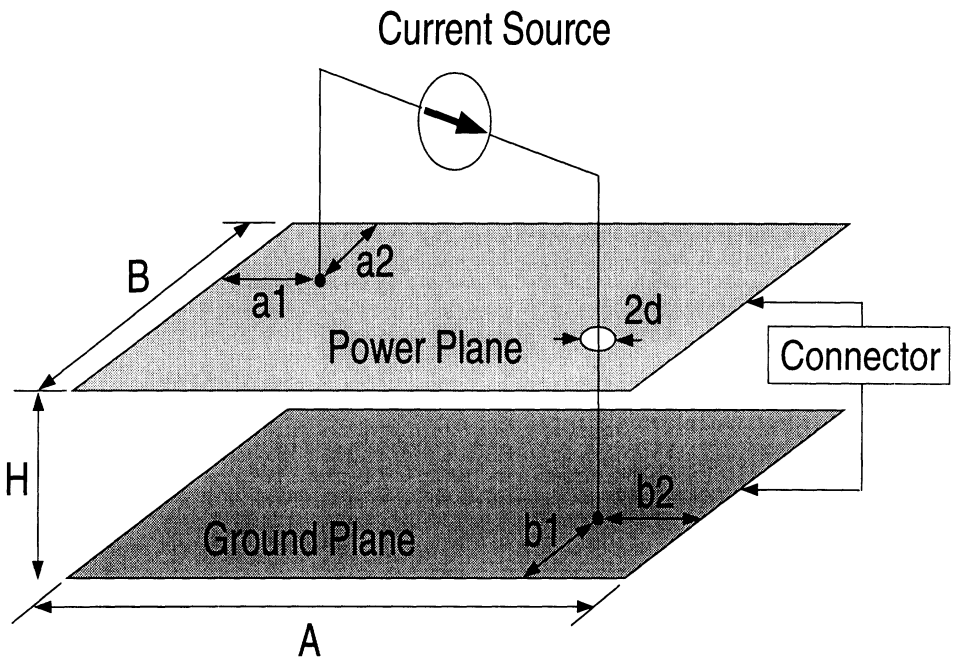


Figure 11: Test PCB with current source. Power and ground pin length = 1.0 mm. Connector is connected on the right side : Power plane = 3.3 V and Ground plane = 0.0 V. Geometrical factors : A = 50 mm, B = 50 mm, H = 0.3 mm, a1 = 5.0 mm, a2 = 5.0 mm, b1 = 5.0 mm, b2 = 5.0 mm, and d = 0.5 mm.

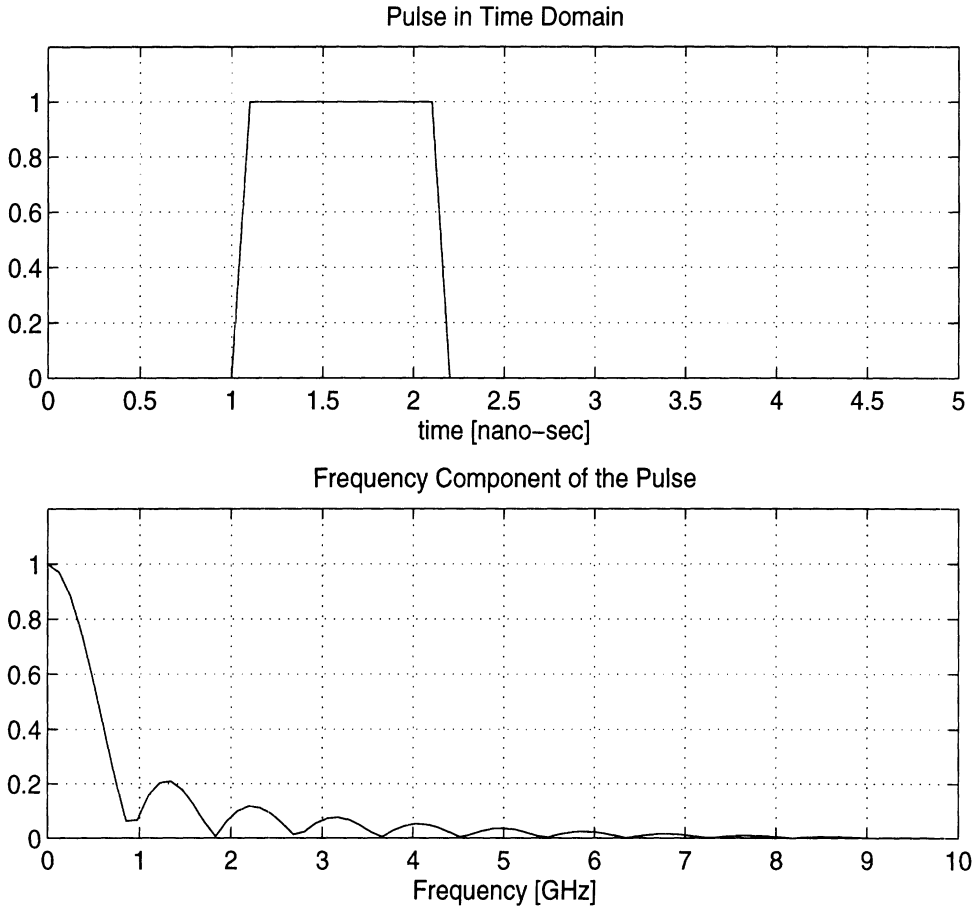


Figure 12: Input Current source and its frequency spectrum

- size = 50 × 50 mm, Thickness (H) = 0.3 mm.
- a1 = a2 = b1 = b2 = 5.0 mm
- d = 0.5 mm

- Extraction frequency = 500 MHz.
- Connector
  - Connector on the right side
  - Power plane = 3.3 V, Ground plane = 0.0 V.
- Measurement : maximum voltages on the power and ground planes.
- Fix power and ground pin positions and vary tile sizes :
  tile size = 10.0 mm to 2.0 mm

3.1.1 Convergence Test 1 : 5 x 5 tiles

In this section, we choose a coarse grid which has 10 × 10 mm tile size resulting in 25 tiles on the power and ground planes, separately. The maximum voltage on the two planes are measured in a given time interval. Figure 13 shows the maximum potential distribution on both planes. As expected, the potential on the right hand side of the two planes is fixed due to the connector. The potential distribution on the power plane shows a peak at the position of the power pin and a similar peak is shown on the ground plane. The slight potential variation on the power plane at the position of the ground pin is caused by the capacitive effect between ground pin and the hole in the power plane.

The computational time and peak potential on two plane are as follows:

- Computation time ⇒ 3.9 sec
- $V_{max}^{power} = 3.30141$ V,
  $V_{max}^{ground} = 1.03$ mV.

Note that for this numerical experiment, HP 9000/715 workstation is used.

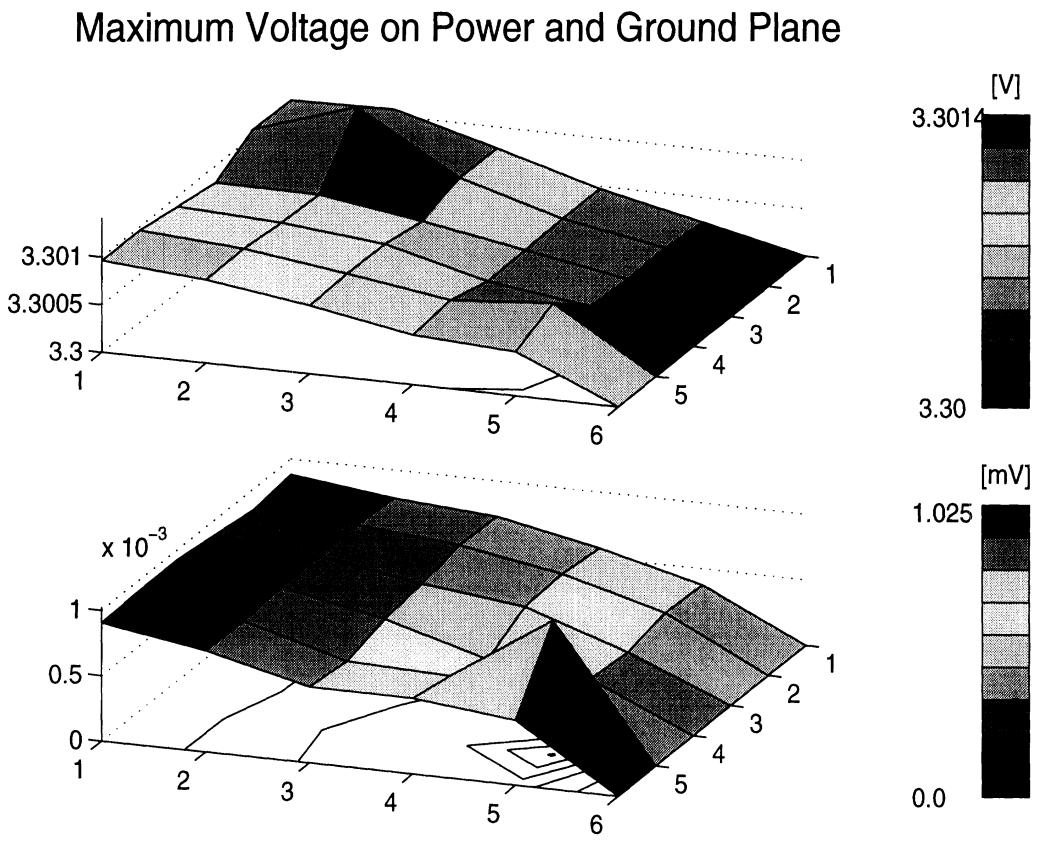


Figure 13: Convergence Test 1 : 5 x 5 tiles

3.1.2 Convergence Test 2 : 10 x 10 tiles

In this section, we increased the tile density for the given structure. The tile size is chosen to be 5 × 5 mm and as a result there are 100 tiles in each plane. Figure 14 shows the potential distribution and reveals more detail information than the previous case.

The computational time and peak potential on two plane are as follows:

- Computation time ⇒ 38 sec
- $V_{max}^{power} = 3.30177$ V,
  $V_{max}^{ground} = 1.41$ mV.

While the peak values are increased slightly, the CPU time is increased about 10 times due to the increased number of electrical nodes. The overall problem size is approximately four times that of the previous discretization.

3.1.3 Convergence Test 3 : 15 x 15 tiles

The tile density is further increased in this section and the resulting potential distribution is plotted in Figure 15. The general shape of the potential distribution is very similar, though it has more detail information. The computational time and the maximum potentials are summarized below.

- Computation time ⇒ 199.3 sec
- $V_{max}^{power} = 3.30184$ V,
  $V_{max}^{ground} = 1.52$ mV.

The maximum voltage on the power and ground planes is slightly increased and the relative deviation remains within a few percent.

3.1.4 Convergence Test 4 : 20 x 20 tiles

The tile size is further reduced to have 2.5 × 2.5 mm and the resulting sub-circuit density reaches 400 per PCB. The number of electrical nodes are much larger than

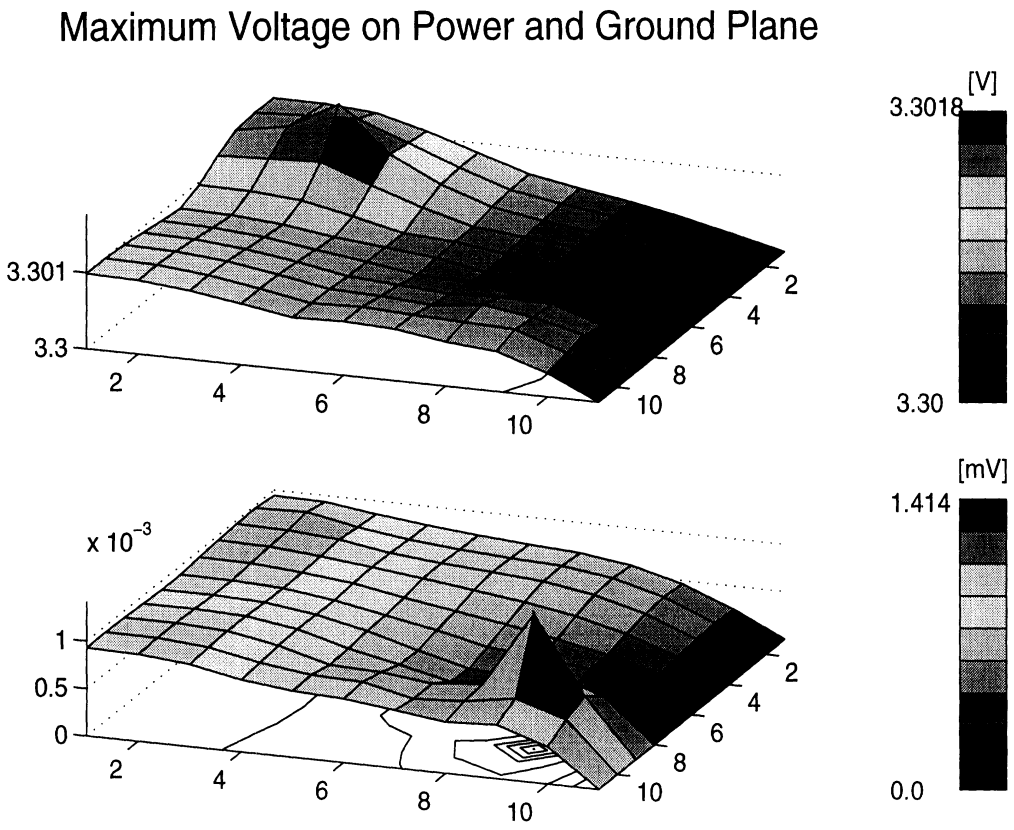


Figure 14: Convergence Test 2 : 10 x 10 tiles

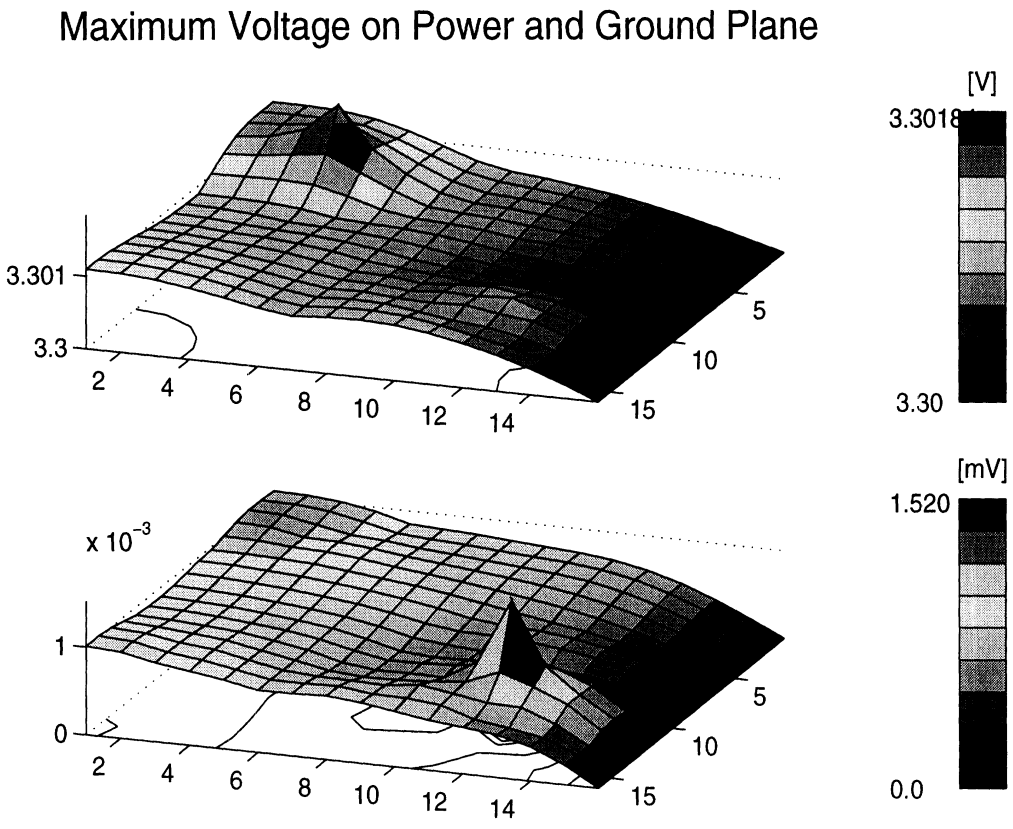


Figure 15: Convergence Test 3 : 15 x 15 tiles

that of the sub-circuit, since each sub-circuit contains 18 electrical nodes. Figure 16 shows potential fluctuations on the power and ground planes. The computational cost and derived results are follows :

- Computation time $\Rightarrow$ 1017 sec
- $V_{max}^{power} = 3.30195$ V,
  $V_{max}^{ground} = 1.52$ mV.

The maximum voltages are almost the same as in the previous case, even though the computational cost increases more than 5 times.

3.1.5 Convergence Test 5 : 25 x 25 tiles

As a last test case, we choose 2.0×2.0 mm tile size resulting in an further increased tile density. As we can see in Figure 17, the HSPICE result has finer details compare to the previous case, but the overall shape is almost same. Slight increase of tile density causes exponential increase in computing time and required memory, even though the result is marginally improved.

- Computation time $\Rightarrow$ 3010.7 sec
- $V_{max}^{power} = 3.30201$ V,
  $V_{max}^{ground} = 1.57$ mV.

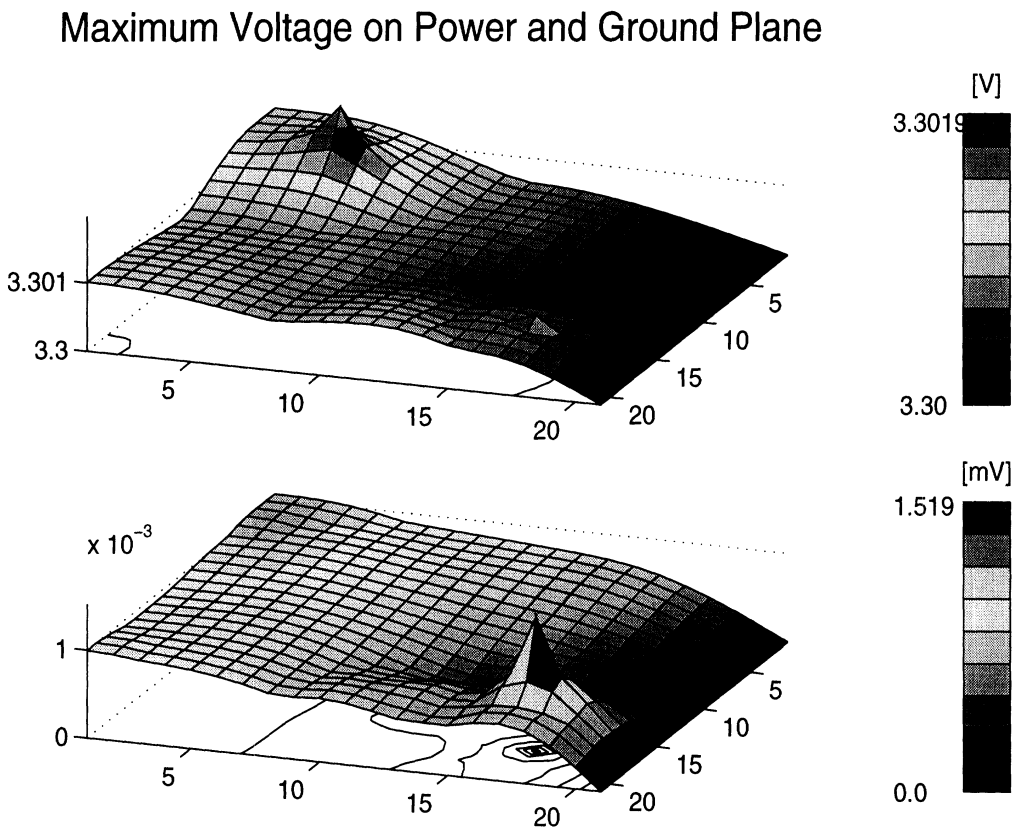


Figure 16: Convergence Test 4 : 20 x 20 tiles

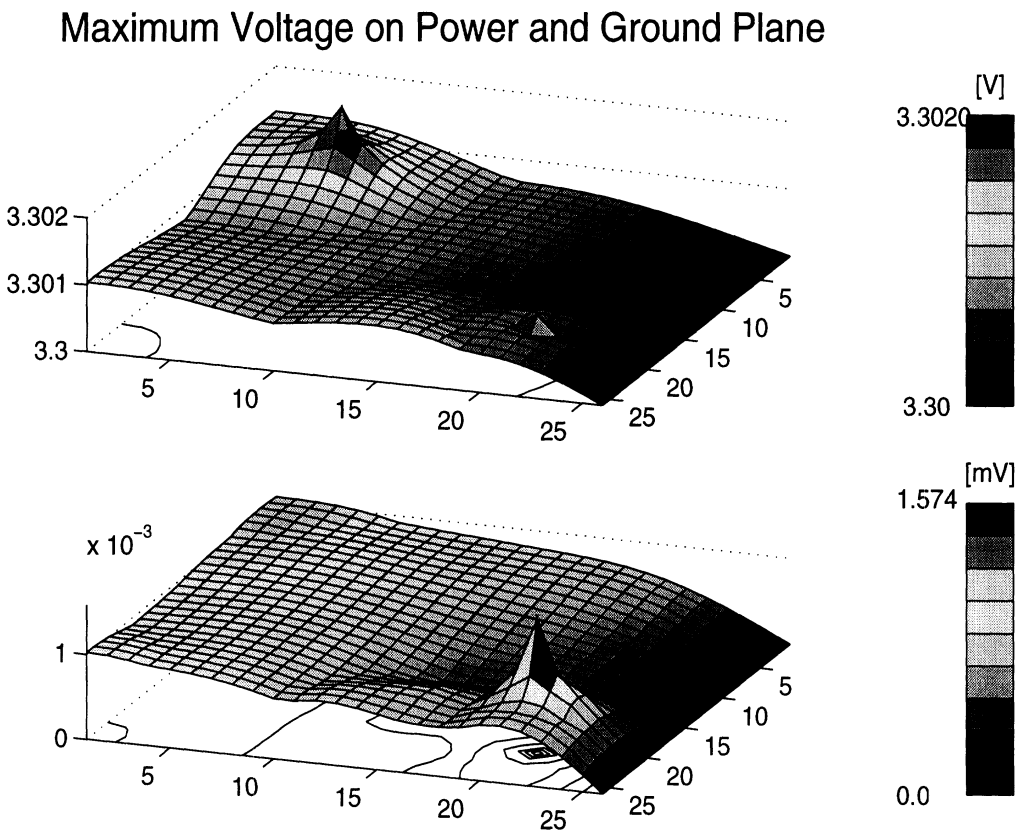


Figure 17: Convergence Test 5 : 25 x 25 tiles

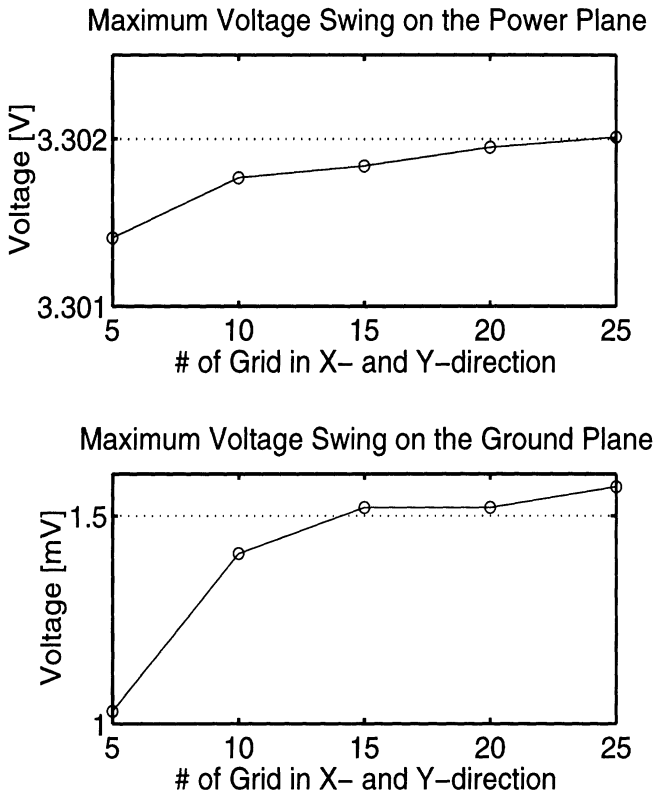


Figure 18: Convergence of the Maximum potentials on the power and ground planes as a function of grid(mesh) density.

3.1.6 Convergence of the Maximum potentials

Figure 18 shows the result of the convergence test for maximum potential on the power and ground planes and can be summarized in the following:

- Potentials on the power and ground planes reach steady state values quickly as we decrease the tile size.
- The relative error of the potential on the power plane remains very small values.

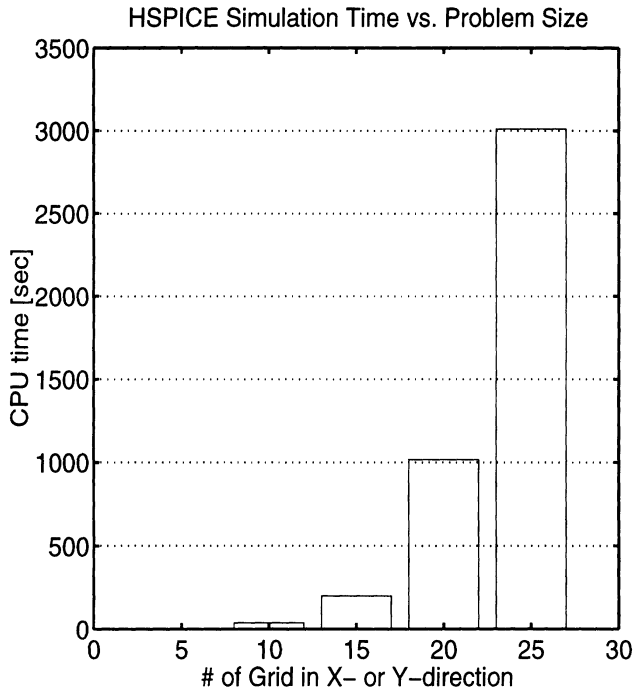


Figure 19: Summary of the Computation Time

3.2 Summary of the Computation Time

After the convergence tests, we observe following facts :

- As we increase the number of tiles in both directions, the number of electrical nodes in HSPICE network also increases in the same manner.
- Total CPU time $\propto N^{\alpha}$, $\alpha > 2$.
- Depending on the desired accuracy of the solution and the available computing facility, it is possible to further to optimize the tile size or tile density.
- Coarse tiling gives fast but less detail information and dense tiling has opposite effect.

4 Simulation approach

In the second part of the report we will discuss the circuit simulation performed using the netlist generated earlier. We will first show how we determined the number of grids for creating the equivalent circuit. Based on the simulations done for this purpose, we will plot the runtime and the memory usage versus the number of grids used. This will be followed by a description of how we modeled the transistor with a current source to run some preliminary experiments. Finally, we will describe the results of simulations using realistic transistor drivers.

An HSPICE netlist was generated using the programs described earlier. This netlist was modified to remove inductive loops (i.e. loops consisting of pure inductances only) by adding a 0.1 ohm series resistor with each inductance. This was necessary since HSPICE does not accept a netlist with inductive loops.

A current source was used to model the transistor driver and simulated using HSPICE. Details of this are shown later. A program was written in C to convert the HSPICE output into a form suitable for MATLAB and a 3-D plot of the switching noise was generated.

5 Modeling the current through an inverter

The preliminary simulations were done using a current source that modeled the driver. This was done in order to remove any non-linear elements (such as transistors) from the netlist. At that time it was not clear how much time HSPICE would take and we wanted to keep the option of using a linear circuit simulator like RICE open.

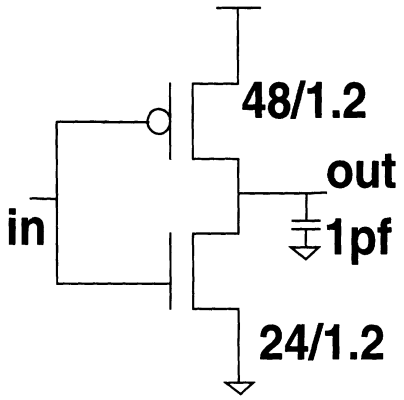


FIGURE 20. An inverter

We first simulated the circuit shown in Figure 20. The resulting currents through the n and the p transistors are shown in Figure 21.

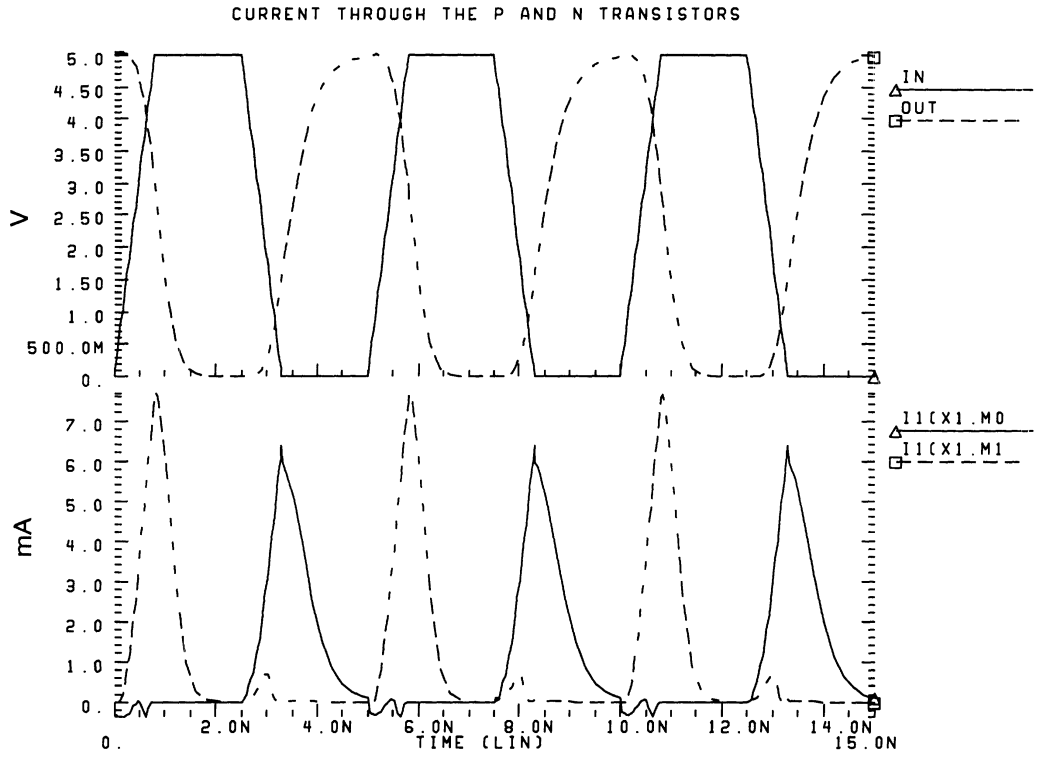


FIGURE 21. Currents through the n and p transistors

The dashed line shows the current through the n transistor and the solid line shows the current through the p transistor. The input to the inverter was a periodic waveform of period 5ns and rise and fall times of 0.8ns. Based on this, the current source was specified as having the shape shown in Figure 21 with a peak value of 10mA and rise and fall times equal to 0.5ns.

The following board parameters were fixed for the rest of the simulations described in this report:

- Board size was fixed at 50mm X 50mm.
- The relative dielectric constant of the material of the board was assumed to be 3.4.
- The board inductances and capacitances were extracted for a frequency of 500 MHz.
- The board was assumed to have one power and one ground plane.
- One side of the board was fixed to the connector, which was the DC bias. A bias value of 5 V was chosen.

In the reminder of the report, the term source is used to mean a connection to the power plane and the term sink is used to mean a connection to the ground plane.

6 Determining the number of grids

The board layout used in the next series of experiments is shown in Figure 22.

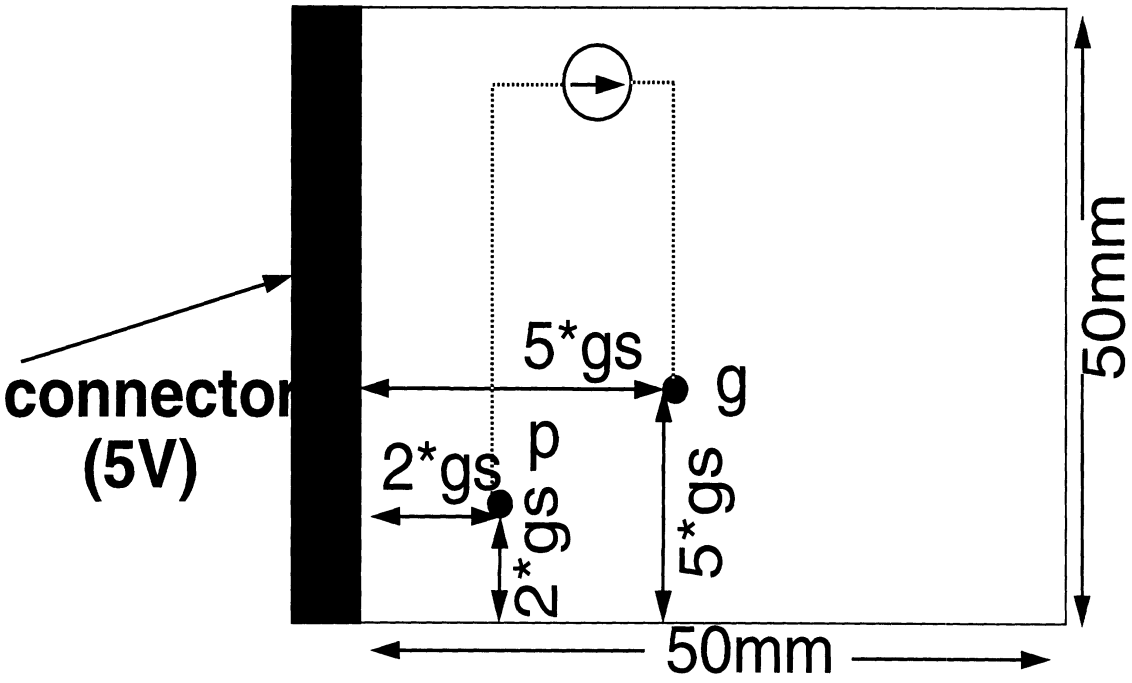


FIGURE 22. Board layout for determining the number of grids

The term "gs" in the figure refers to the distance between the center of one grid to the center of the other grid. This varies with the number of grids since the board size is fixed. The term "p" refers to the source and the term "g" refers to the sink.

The simulation results for N (the number of grids) = 20, 25 and 32 are shown in Figures 23-25. In all the simulations described in this part of the report, the peak to peak voltage swing is plotted. The peaks correspond to the position of the source and the sink points. As can be seen from the plots, the essential features of the output are the same for the three. Only the minor details become more clear as the gridding is made finer. We also plotted

the simulation time (in CPU seconds) and the memory used (in Mbytes) and the results are shown in Figure 26.

The gridding was chosen to be 25 as a compromise between simulation time and accuracy. This is the value used in the remainder of this report.

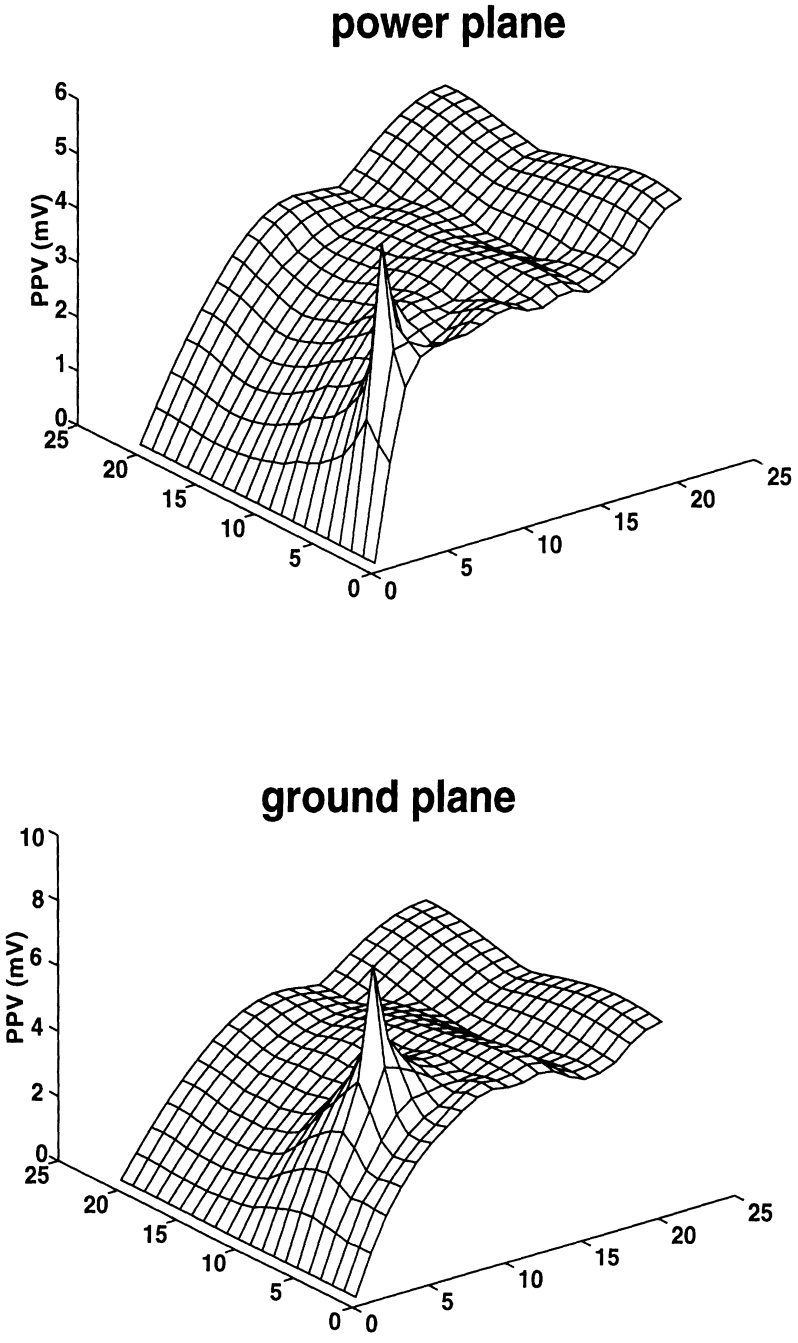


FIGURE 23. Simulation results for N=20

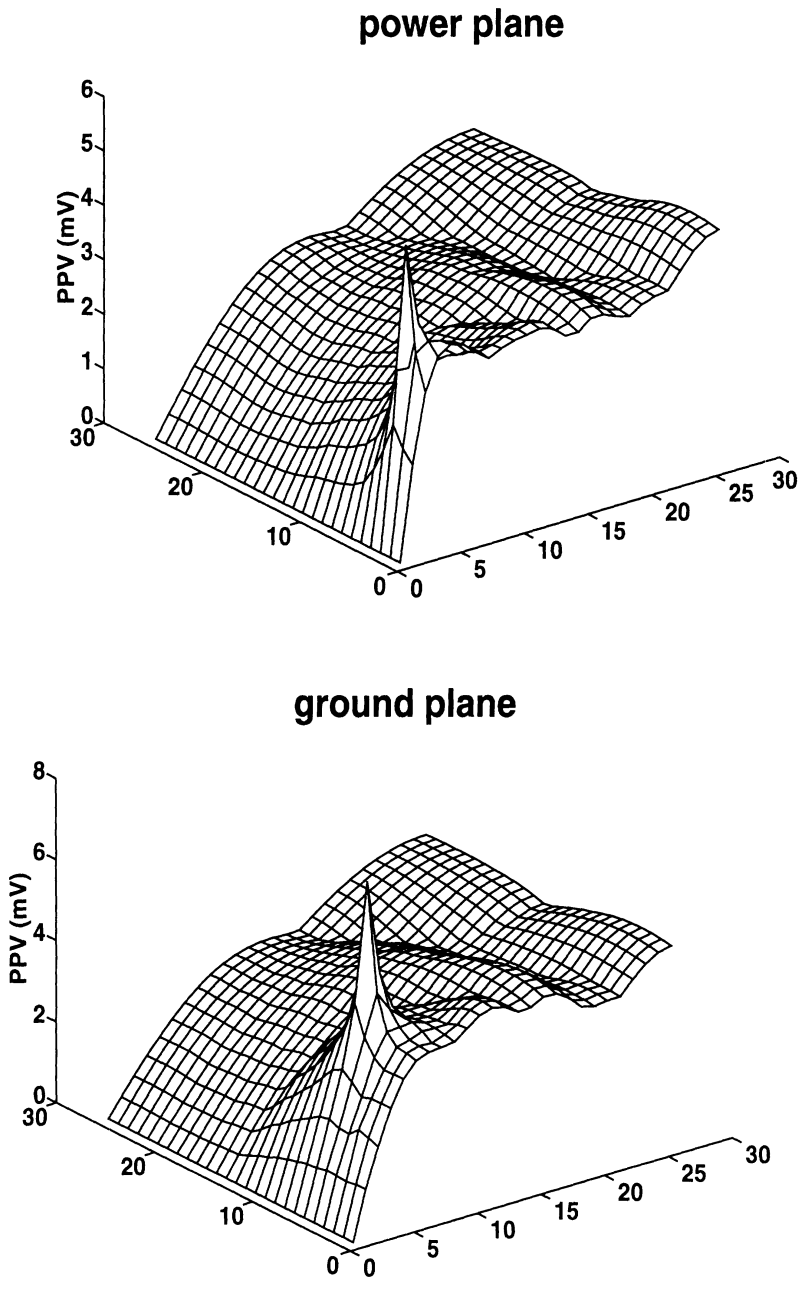


FIGURE 24. Simulation results for N=25

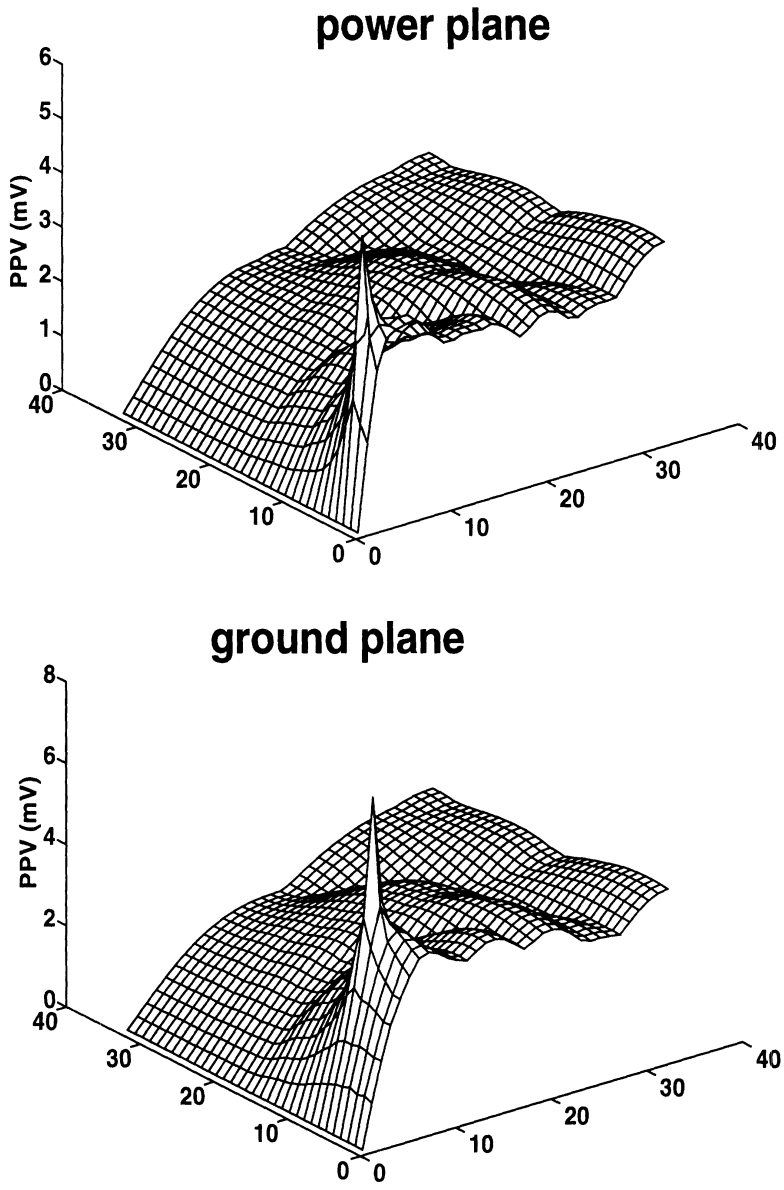
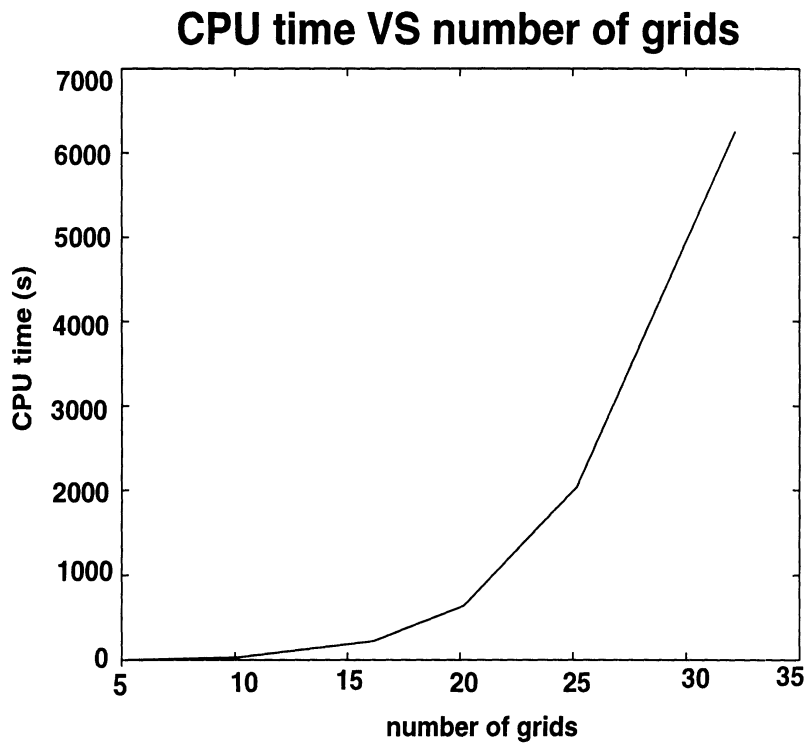


FIGURE 25. Simulation results for N = 32



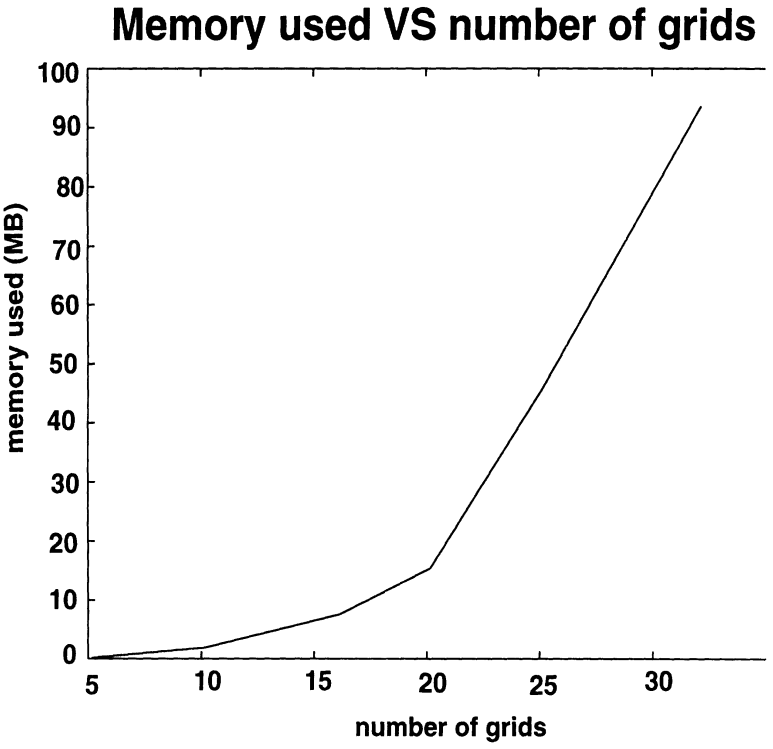


FIGURE 26. CPU and memory used versus number of grids

7 Simulations with different positions of the connector

Figure 24 shows the simulation result with the connector on the left side of the board. The board layout is the same as shown in Figure 22. The maximum value of the peak-to-peak (PP) voltage on the power plane was 5.5mV and that on the ground plane was 7.8mV.

Next, the simulation was repeated with the connector on the top of the board but with the source and sink positions same as before. The maximum PP voltage on the power plane was 23mV and that on the ground plane 21mV. For the connector on the right side of the board the maximum PP value on the power plane was 23mV and on the ground plane was 21mV. For the connector on the bottom of the board, the maximum PP value had reduced to 5.5mV on the power plane and 7.8mV on the ground plane.

In each simulation, the maximum PP voltage corresponded to the position of the source and the sink points. These results shown an interesting trend. As the source and sink points are moved away from the connector, the switching noise increases. Referring to Figure 22, when the connector was placed on the top and on the right, its distance to the source and sink points is increased whereas when the connector is placed on the left and the bottom its distance to the source and sink points is reduced. Next, the connector was fixed to the left side of the board and the distance between the source and sink was increased. The new board layout is shown in Figure 27

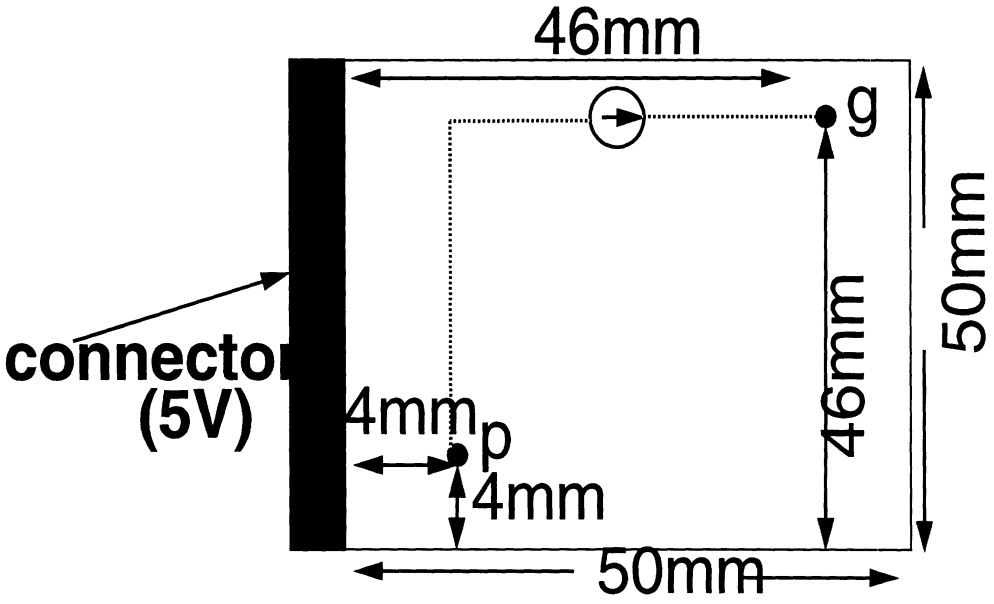


FIGURE 27. Board layout with source and sink far apart

The maximum PP voltage on the power plane increased to 11mV and on the ground plane increased to 18.6mV. Interestingly, the value of 11mV was due to the coupling capacitor between the ground lead and the power plane. This is consistent with our earlier simulations since the coupling capacitor is at a greater distance from the connector.

8 Simulations with actual transistor drivers

We next simulated with actual transistor drivers replacing the current sources. The board layout is shown in Figure 28 which corresponds to the test vehicle given by INTEL.

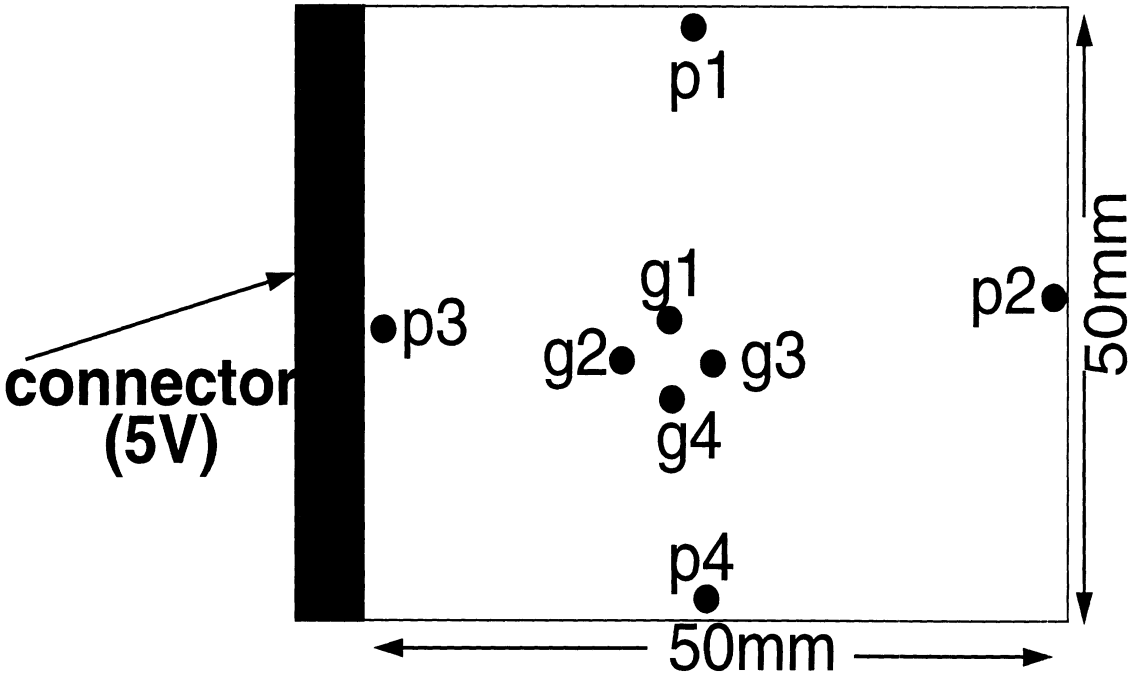


FIGURE 28. Board layout for the drivers

First, we used only small transistor drivers with W/L = 48μ/1.2μ for the p transistor and W/L = 24μ/1.2μ for the n transistor. Each driver had a load of 100fF and was driven by a periodic pulse train of period 5ns and rise and fall times equal to 0.8ns. All four drivers were assumed to switch simultaneously. The simulation results are shown in Figure 29. The maximum PP voltage was 29mV on the power plane and 22 mV on the ground plane. Again, the coupling capacitors contributed to the maximum noise on the power plane.

Next, we replaced the small drivers with large drivers, such as the ones that are present in the output pads. The W/Lfor the p transistor was 1400μ/1.2μ and W/L for the n transistor was 800μ/1.2μ. The output load on each driver was 25pF and each driver was excited by a pulse train same as before. The simulation results are shown in Figure 30. The maximum PP voltage on the power plane was 0.42V and on the ground plane was 0.67V. As can be seen from Figure 30, the effects of the source points overshadow the effects of the coupling capacitors.

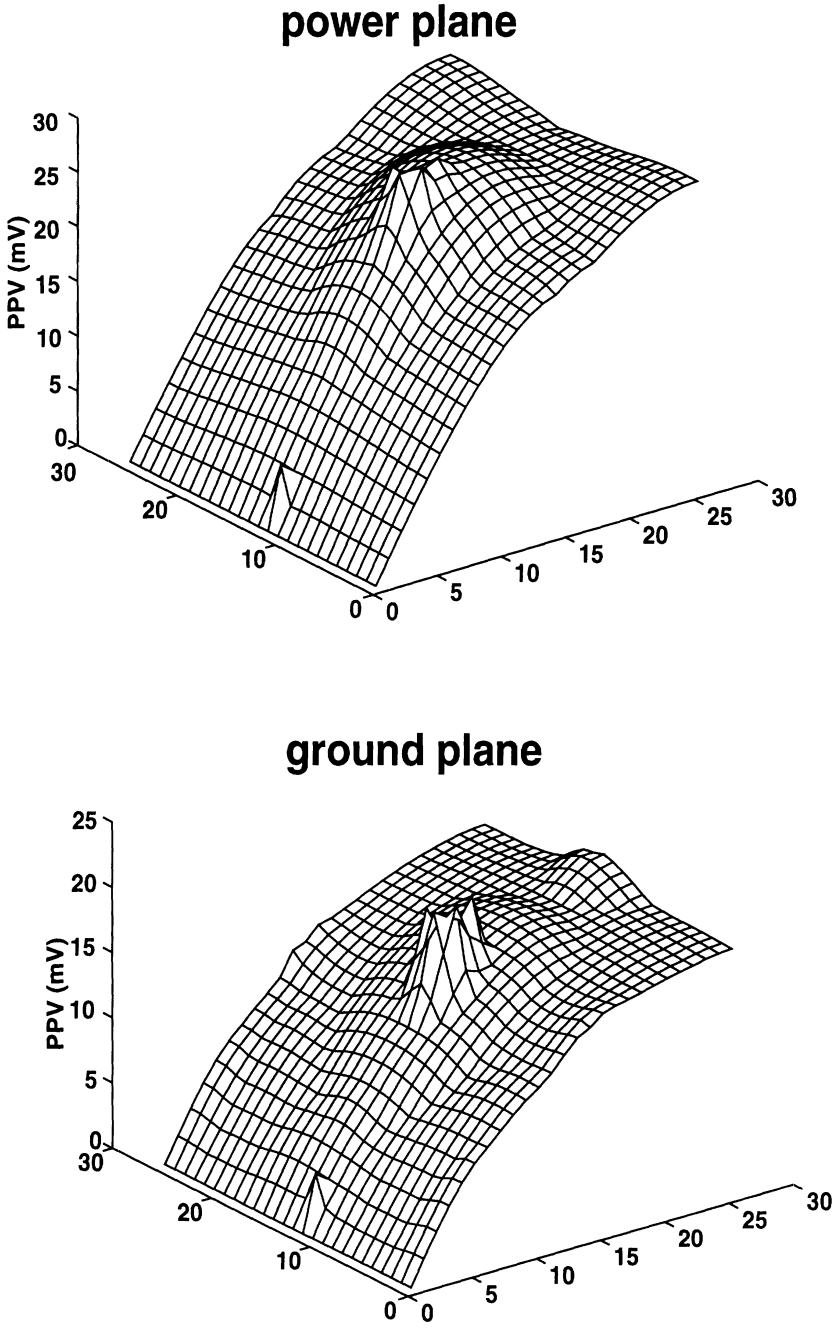


FIGURE 29. Simulation results with 4 small drivers

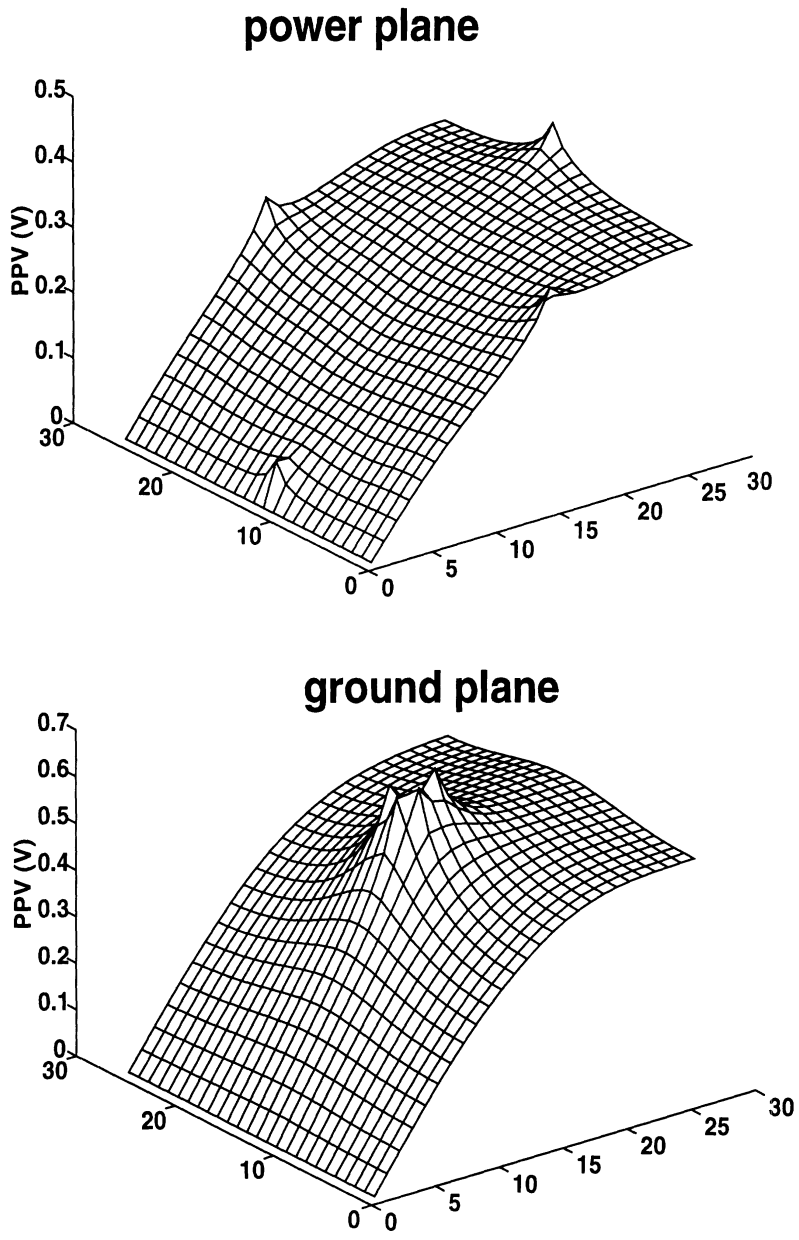


FIGURE 30. Simulation results with 4 large drivers

Next, instead of switching all 4 drivers simultaneously, only two were switched on at a given time. Referring to Figure 28, first drivers 1 and 3 were turned on followed by drivers 2 and 4. As expected, the maximum PP voltage on the power plane decreased to 0.2V and on the ground plane decreased to 0.42V.

9 Simulation with stripline

So far the effect of signal traces was ignored. Next we simulated a single large transistor driver with effect of signal trace included. The board layout is shown in Figure 31.

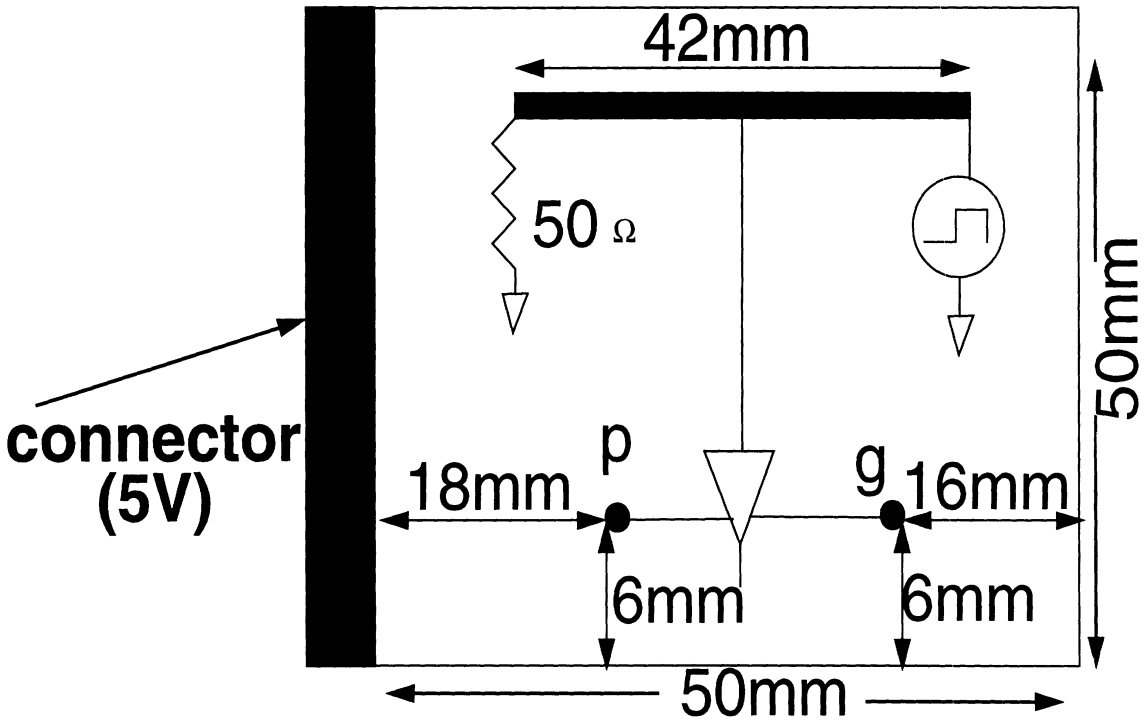


FIGURE 31. Board layout showing signal trace

The signal trace was modeled as a stripline, shown by the thick line. One end was terminated with a 50 ohm load impedance while the other end was driven by a square wave. The transistor sizes were the same as before. The maximum PP voltage on the power plane was 0.23V and 0.52V on the ground plane. These corresponded to the source and sink points on the board.

10 The Summary of the Work

As a summary of the presented study, the following should be mentioned:

- Combination of micro- and macroscopic analysis has been implemented for the analysis of the switching noise in printed circuit boards (PCB).
- Uniform/Non-uniform structured tiling processor has been developed for the tiling of the multilayer PCB with multiple signal lines and a connector placed at various locations.
- Frequency independent equivalent circuits have been developed for power/ground planes, signal lines, and vertical vias.
- The tiling processor can deal with multiple power and ground planes, signal lines, pins and drivers.
- From the tiling procedure, a HSPICE netlist input file is generated which can be used in HSPICE to provide frequency and time-domain data.

11 Future Work

This project is expected to be completed in 1996. The following are necessary for its completion

- Comparison between computed values of switching noise and measurements. The measurements will be provided to us by J.C. Liao at INTEL Chandler, Arizona.
- Development of macro-model functions for geometries, such as, multilayer vias to replace the FEM based codes.
- Extension and verification of the tiling processor for the multilayer PCB with multiple signal lines.
- Optimization of tiling procedure to reduce the number of electrical nodes and improve efficiency.
- Introduction of decoupling capacitors.
- Development of an automated procedure to insert the capacitors.
- Transfer of programs to INTEL
- Final Report.