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COMPUTATION OF SWITCHING NOISE IN PRINTED CIRCUIT BOARDS

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Abstract

Simultaneous switching noise (SSN) is a phenomenon with adverse and severe effects when a large number of high speed chip drivers switch simultaneously causing a large amount of current to be injected into the power distribution grid. The effects of SSN are manifested in a variety of transient and permanent system malfunctions including the appearance of undesirable glitches on what should otherwise be quiet signal lines and the flipping of state bits in registers and memories. Current approaches for dealing with SSN are largely ad hoc, relying primarily on the ability of expert designers to postulate worst-case scenarios for the occurrence of SSN-related errors and to analyze these scenarios using pessimistic estimates of packaging parasitics. This paper takes a first step towards evolving a systematic methodology for modeling and analysis of SSN in printed circuit boards (PCBs). This methodology adopts a combination of macro- and micro-models which allow for a system level treatment of the problem without losing the necessary detailed descriptions of the power/ground planes, the signal traces and the vertical interconnections through vias or plated holes. This approach has been applied to a variety of PCB structures and has allowed for an effective characterization of switching noise and a comprehensive understanding of its effects on PCB performance.

Keywords

Simultaneous switching noise, printed circuit board, decoupling capacitors, ground bounce, tiling, electromagnetic modeling, circuit simulation.

1 Introduction

Inductively induced voltage fluctuations in the power and ground lines of digital systems are a source of performance degradation and may pose serious reliability problems. Variously termed *simultaneous switching noise* (SSN), *inductive noise*, $\frac{di}{dt}$ *noise*, *delta-I noise*, and *ground bounce*, this phenomenon is most severe when a large number of high frequency chip drivers switch simultaneously causing a large amount of current to be injected into the power distribution grid. The adverse effects of SSN are manifested in a variety of transient and permanent system malfunctions including the appearance of undesirable glitches on what should otherwise be quiet signal lines and the flipping of state bits in registers and memories. Because of their unpredictability, SSN-related bugs have been reported to be among the most difficult to track down and correct [1].

While the fundamental mechanism underlying SSN, namely current switching, has been widely recognized for many years [2]-[6], the computer-aided design (CAD) tool kits available to a digital system designer today still lack adequate SSN modeling, analysis, and design capabilities. This lack can be partially attributed to the complexity of the EM modeling required to obtain accurate estimates of the inductive parasitics responsible for SSN coupled with the need for system-wide global analysis of this effect. Current approaches for dealing with SSN are largely ad hoc, relying primarily on the ability of expert designers to postulate worst-case scenarios for the occurrence of SSN-related errors and to analyze these scenarios using pessimistic estimates of packaging parasitics.

Our goal in this paper is to take a first step towards evolving a systematic methodology for modeling and analysis of SSN in printed circuit boards (PCBs). In this methodology the seemingly contradictory goals of modeling accuracy and global analysis efficiency are reconciled through a divide-and-conquer process. Accuracy is insured by performing detailed EM field analysis on appropriately chosen small sections of the PCB, referred to as *tiles*, to create lumped electrical equivalent circuit models. PCB tile models are subsequently combined with models for chip current drivers and package leads to produce an electrical simulation model for the PCB power distribution subsystem. A circuit simulator such as SPICE [7] is then used to exercise this model under a variety of current excitation conditions to yield *noise maps* that indicate the variation in power and ground potential as a function of location on the PCB.

It is instructive to note that this approach is similar, at least in spirit, to the approach routinely employed in modeling and simulation of very large scale integrated (VLSI) chips. Accurate circuit simulation of VLSI chips containing tens of thousands of transistors is made possible by separating the detailed physical modeling of 3-D transistor structures from the global chip-wide electrical analysis. Device modeling involves creating lumped electrical equivalent circuits that are obtained by solving the partial differential semiconductor equations governing the movement of charge carriers within the semiconducting material. These equivalent circuits, appropriately parameterized by material, geometric and environmental factors, are then combined to produce a complete electrical model for a chip that is amenable to analysis by fast circuit simulators.

The rest of this paper is organized in four sections. Section 2 reviews current approaches for modeling and analysis of SSN and motivates our approach to the problem. The tiling procedure central to our method is described in Section 3 along with the equivalent circuits for a sampling of tile types. In Section 4 we present simulation results for a number of PCB configurations that are aimed at enhancing our understanding of the SSN phenomenon. The paper contributions and directions for future work are summarized in Section 5.

2 Problem Statement and Previous Work

A simplified model of the current path through a PCB-mounted IC chip is shown in Figure 2-1 [2]-[4],[8]. Current enters the PCB through a metal connector to an external power supply (denoted as V_{DD}) and flows through the conducting material of the board's power plane and the chip's package leads and bonding wires to a V_{DD} pad (point A) connected to the chip's internal power distribution network. Current then flows through one or more output pad drivers C and returns through a V_{SS} pad (point B), bonding wires and package leads, to the board's ground plane and ground connector to the external power supply. In this simplified model the PCB power and ground planes and the package leads are represented by lumped inductances. In this treatment it is assumed that the internal chip power distribution network is mostly resistive and does not significantly contribute to the overall inductance responsible for SSN. Techniques for efficient design of chip power distribution are discussed in [9]. When a pad driver C changes

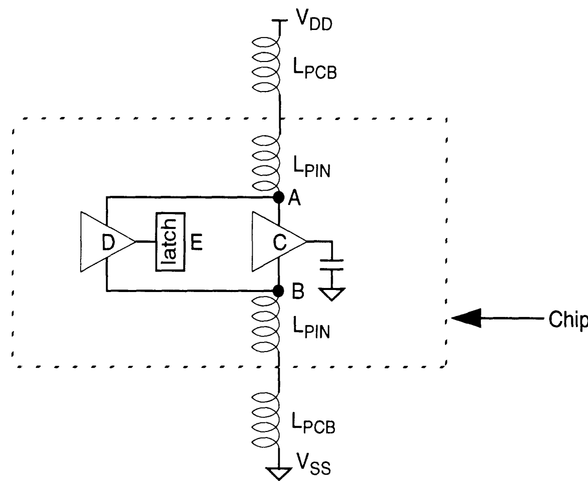

Figure 2-1: Traditional way of modeling the inductances of the PCB and the package bonding wires

state to charge or discharge its load capacitance, the resulting current surge through the power distribution network produces inductive voltage drops that lower the potential at point A below V_{DD} and raise the potential at point B above V_{SS}. Such glitching, or noise, in what should otherwise be quiescent power and ground rails leads to two harmful effects on the chip circuitry: increased driver delay and loss of data integrity [2][3]. The increase in driver delay is directly attributable to the temporary lowering (raising) of potential at point A (point B) causing a reduction in the current drive available for charging (discharging) the load capacitance to V_{DD} (V_{SS}). The second effect is more insidious as it may lead to logic errors. Since the power and ground lines establish the reference levels for all other signals, fluctuations in these levels may be misinterpreted as logic transitions in data and clock lines. If these transitions are inadvertently latched, the circuit may end up in an incorrect logic state. For example, a dip in potential at point A may be seen as a spurious glitch at the output of quiet driver D that flips the state of latch E. These problems are compounded when a large number of output drivers switch simultaneously on a PCB with many chips.

Much of the previous work on SSN can be characterized as seeking the determination of an aggregate effective inductance L_{eff} that accounts for the power and ground leads, the board itself, and the mutual inductances between the chip packaging and the PCB, and the development of design guidelines to reduce SSN effects. Some of the early work in this area was done in [3] where a detailed electrical model of the package is simulated using ASTAP [10] and a gross value of L_{eff} is determined using:

$$L_{eff} = \frac{V_n}{N\frac{di}{dt}} \qquad (2.1)$$

where V_n is the noise magnitude, N is the number of simultaneously switching drivers and di/dt is the rate of change of driver current. In this study only a single chip is considered and the computed L_{eff} is used to explain the noise effects. In a similar way, Rainal [5] gives detailed formulas for calculating the self- and mutual-inductances assuming that the pin inductances are the principal sources of switching noise on a chip. Using detailed electrical models of the package and the noise tolerance level of a logic family, Katopis [4] applies statistical design rules to determine the maximum number of drivers that may switch simultaneously. Furthermore, EDN's Advanced CMOS Logic ground bounce tests [11] conclude that centrally placed ground pins or surface mounted packages reduce the ground bounce effects. In all these treatments, the parasitic inductance of the PCB is ignored and the lead inductances of the package pins are considered to be the primary contributors to SSN.

Recently, attempts are made to account for the effect of the PCB power and ground plane inductances. Specifically, in the current distribution in the power and ground planes is computed by solving the field equations using source and sink points. In another approach [16], switching noise due to inductances in the board as well as the vias is computed using an appropriate SPICE model. The board is assumed to have four layers: a signal layer, a power layer, a ground layer and a reference layer for the measurements. The model is created by appropriately discretizing the power and ground planes and finding the equivalent circuit for each mesh. More recent work [6] has shown that the induced noise voltage is, in fact, sub-linear in the number of switching drivers; this phenomenon is due to the reduced drive of CMOS transistors which in turn is caused by ground bounce, and is a form of negative feedback. In this work L_{eff} is calculated by placing centralized point sources and distributed sinks on the power planes. The static field equations are then solved for the power planes and the L_{eff} is computed in a modified form of (2.1) to take into account the negative feedback effect. The level 1 SPICE model of the CMOS transistors used in deriving the noise equations limits the accuracy of the model when it is applied to sub-micron technologies. Moreover, the computed value of L_{eff} varies with location when many chips are placed on a PCB. A detailed EM analysis of the interconnect structure in a computer package is performed in [13], [14] using finite-difference-time-domain (FDTD) and transmission line

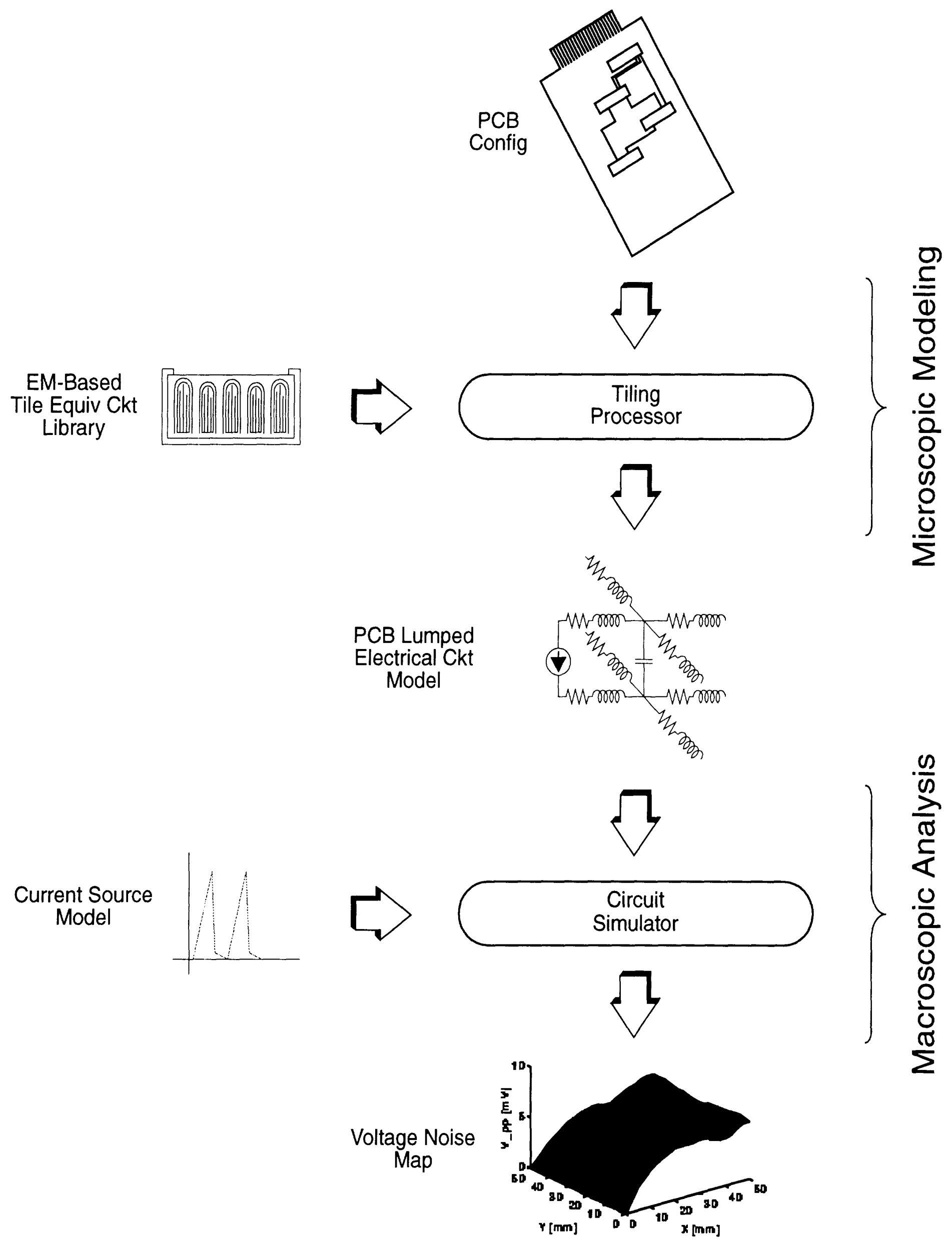

Figure 2-2: SSN Modeling and Simulation Methodology

matrix (TLM) methods. While being accurate, this approach becomes infeasible for realistic systems where a PCB may contain several hundred ICs.

An accurate SSN simulator must consider the inductances due to both the PCB and the pins themselves. The technique developed during the study presented in this paper uses a combination of both macroscopic and micro-

scopic modeling (see Figure 2-2). The macroscopic model considers the SSN at the system level and accounts for its variations across the PCB due to the flow of current along the conducting paths on all planes. At this level, the approach provides for an accurate electrical representation of the board as an interconnection of *N*-port networks. These networks, generated by microscopic modeling, are three-dimensional ladders of *RLC* elements and represent the electrical equivalents of subsections of the board, referred to as *tiles*. Tile equivalent circuits are defined according to the expected electric field signatures inside the board. High accuracy is achieved by taking into account the dynamic nature of the electromagnetic fields. Depending on the substructure, these models may be based on quasi-static or full-wave solutions. The resulting board equivalent circuit is augmented with models for chip current drivers and simulated using HSPICE [15] . A "noise-map" of the power and ground planes is obtained and the regions where the effect of noise is maximum are identified for possible insertion of bypass capacitors.

While this approach is similar to [16], it has the advantage of combining the accuracy of full-wave field solvers with the large-scale capacity of SPICE electrical simulation, and can be easily generalized to handle any number of power, ground and signal layers. Moreover, since the equivalent circuits resulting from the full-wave analysis consist of lumped *R*, *L* and *C* elements, we can potentially use the AWE [17] based simulators which are 3-4 times faster than SPICE, provided that the drivers are linearized appropriately.

3 PCB Tiles and their Lumped Equivalent Circuits

In the following, we present our hybrid modeling methodology starting with the tiling procedure and concluding with a summary of the primitive equivalent circuits structures which are the main building blocks of the printed circuit board geometry.

3.1 Tiling Procedure

The board is partitioned into a set of tiles, *primitive structures*, using a systematic mesh generation procedure (see Figure 2-2). In this procedure, grid points (nodes) are introduced for all the physical details of the structure.

These *physical nodes* correspond to crossings and bends of traces, via connections to planes, corners of the printed circuit boards, connections to connectors and drivers, apertures on the planes and connections to loads, decoupling capacitors, etc. These nodes exist on all planes of the PCB and may vary in number from plane to plane. The intent of the tiling approach is to construct a three-dimensional grid that preserves all the geometrical details of the printed circuit board. The resulting mesh is rectangular and nonuniform and its grid points provide the electric nodes for the three-dimensional SPICE model which is generated at the end of the tiling process.

A simple example of the tiling procedure is shown in Figure 3-1. During this tiling process we define three different types of tiles: interior, edge, and corner. The interior tiles can be represented by a cross-shaped equivalent circuit. This equivalent circuit also provides an electrical representation of the edge and corner tiles by use of appropriate terminations. For the sake of simplicity, three different primitive structures are considered: a power/ground plane tile (see Figure 3-1(a)), a power/signal/ground tile (see Figure 3-1(b)) and a power/ground pin tile (see Figure 3-1(c)). The equivalent circuits for these primitives are derived by using appropriate electromagnetic simulation tools as it will be discussed below. In addition, equivalent circuit representations for the input sources and connectors are also considered. Throughout the presented study we have assumed that the connectors are attached to one side of the PCB and maintain constant potentials for power and ground planes.

The information of all of these equivalent circuits are recorded in a HSPICE input file and circuit simulation is performed in time or frequency domain. From the circuit simulation, the potential distribution on the power and ground planes is computed and from this information the switching noise is extracted. Also, the input impedance at the driving port can be easily computed from the voltage and current information at a given branch.

3.2 Equivalent Circuits

As was mentioned above, a variety of modeling approaches are followed in order to identify the equivalent circuits for the primitives defined during the tiling procedure. A description of these approaches is given below.

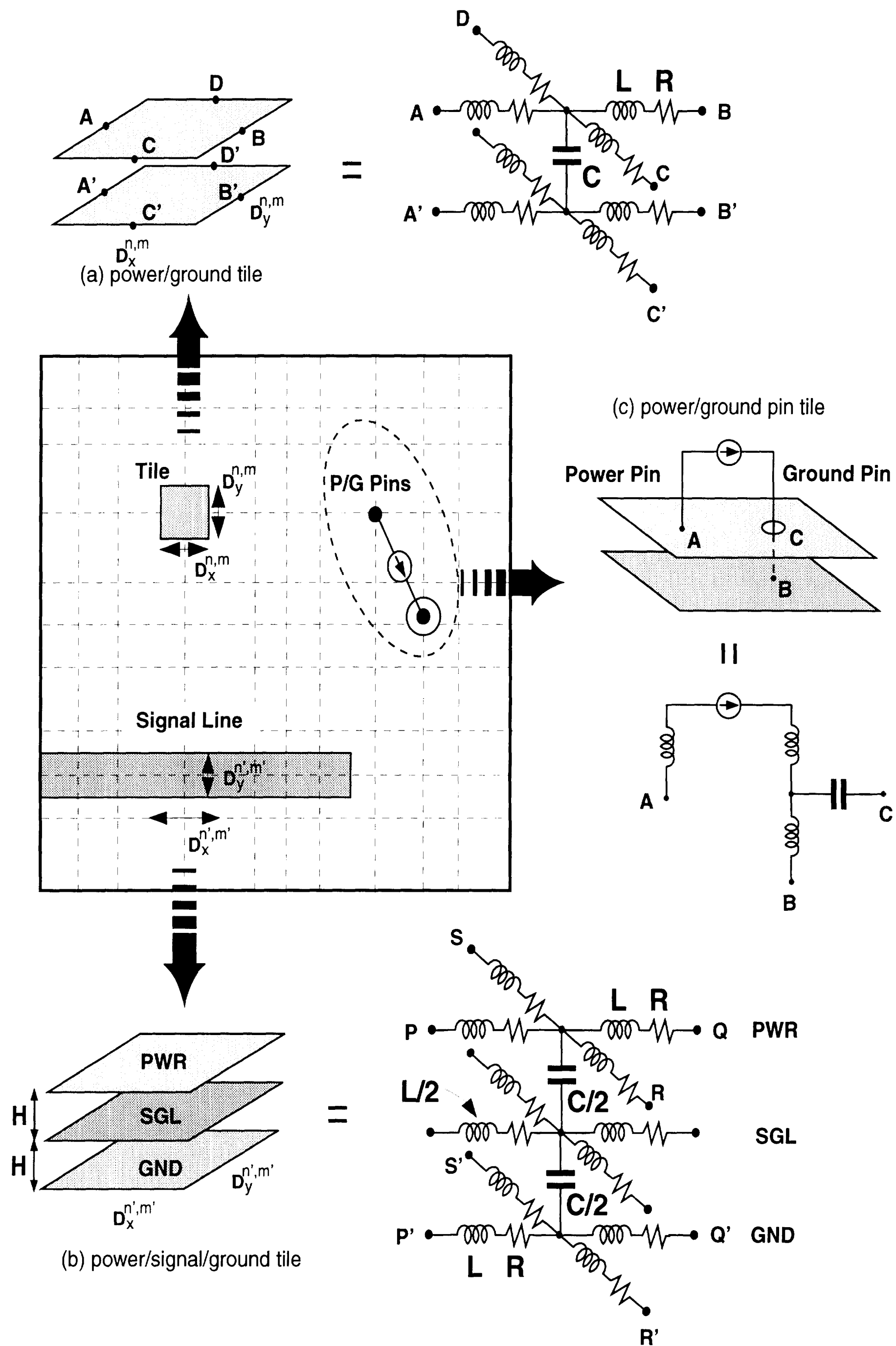

Figure 3-1: Tile equivalent circuits.

3.2.1 Power and ground (P/G) plane tiles

A power/ground plane primitive is considered as a section of a parallel plate waveguide. From microwave circuit

theory, the equivalent circuit for a such a structure is a 4-port network as shown in Figure 3-1(a). Under the assumption that the parallel plate waveguide supports only a TEM wave while evanescent higher order modes are weakly excited and can be practically considered non-existent, the equivalent circuits can be easily computed using an ideal transmission line theory. The above underlying assumptions are in general valid for clock frequencies in the GHz range. Moreover, to take into account the floating potentials on the power and ground planes, a special form of an equivalent circuit is devised as shown in Figure 3-1(a). Since an arbitrary surface current can be decomposed into two orthogonal components, we can specify two equivalent 2-port networks, one for each direction of the current. The appropriate equivalent inductances and capacitances for each two-port network are found by matching the scattering parameters between the corresponding four-port transmission line combination and the equivalent circuit. In addition to the inductive and capacitive elements, resistive elements are also added to account for ohmic losses and to prevent pure inductive loops in the equivalent circuits. The derived equations for the P/G plane equivalent circuits are as follows;

$$\omega L^{n,m} = \frac{60\pi h}{D_y^{n,m}\sqrt{\varepsilon_r}}\sin\left(\frac{2\pi\sqrt{\varepsilon_r}}{\lambda_o}D_1\right) \tag{3.1}$$

$$\omega C^{n,m} = \frac{D_y^{n,m}\sqrt{\varepsilon_r}}{120\pi h}\tan\left(\frac{\pi\sqrt{\varepsilon_r}}{\lambda_o}D^{n,m}{}_x\right) \tag{3.2}$$

$$R = \sqrt{\frac{\pi f \mu_o}{\sigma}} \tag{3.3}$$

where $D_x^{n,m}$, $D_y^{n,m}$ are the x and y dimensions of the n, m tile and $D_1 = \frac{D_x^{n,m} + D_x^{n-1,m}}{2}$ as shown in Figure 3-1. Furthermore, h and ε_r are the thickness and relative dielectric constant of the dielectric material separating the conducting layers of the printed circuit board and λ_o is the wavelength at the frequency of equivalent circuit extraction. As we can recognize from the above expressions, the inductance and capacitance are frequency independent quantities when the size of each tile and the distance between the power and ground planes are relatively small compared to the smallest wavelength of interest in the propagation signals. As frequency increases, however, the inductance and capacitance values may vary accordingly thus giving rise to high-frequency effects. For the examples

presented in this study, we assumed that the inductances and capacitances in all equivalent circuits are independent of frequency.

Under the assumption that the electrical dimensions of the tile are much smaller than the wavelength of the operating frequency, that is, $\beta_g D_x^{n,m}$ and $\beta_g D_y^{n,m} \ll 1$ where β_g is the propagation constant, the above equations can be reduced to a more compact form using the small argument approximation of the trigonometric functions.

3.2.2 Power/Signal/Ground Tiles

The signal line between two conducting planes is modeled as a stripline placed halfway between the two planes (Figure 3-1(b)). As with the single power/ground plane tile, in the case of a stripline tile, an equivalent circuit is developed which can take into account the potential fluctuations on the power and ground planes through series inductances and shunt capacitances placed as shown in the figure. Derivation of the equivalent circuit is completed in two steps. First, the characteristic impedance of the stripline is evaluated from an empirical formula [19] which takes into account the fringing fields. Second, an equivalent T-network is constructed for a transmission line of length $D_x^{n',m'}$ and width $D_y^{n',m'}$ as shown in the bottom of the figure and the values of capacitance and inductance in the equivalent circuit are determined after following a similar procedure as in the previous subsection. The values of the inductances and capacitances for this primitive are given by the following formulas:

$$\omega L^{n',m'} = Z_o^{n',m'} \times \frac{1-\cos(\beta_g D_x^{n',m'})}{\sin(\beta_g D_x^{n',m'})} \tag{3.4}$$

and

$$\omega C^{n',m'} = \frac{\sin(\beta_g D_x^{n',m'})}{Z_o^{n',m'}} \tag{3.5}$$

where

$$Z_o^{n',m'} = \frac{30\pi}{\sqrt{\varepsilon_r}} \times \frac{1}{(W_e/H) + 0.441} \tag{3.6}$$

and

$$\frac{W_e}{H} = \frac{D_y^{n',m'}}{H} - \begin{pmatrix} 0, & D_y^{n',m'}/H > 0.35 \\ \left(0.35 - \frac{D_y^{n',m'}}{H}\right)^2, & D_y^{n',m'}/H \le 0.35 \end{pmatrix} \tag{3.7}$$

In general, the equivalent inductance and capacitance are functions of frequency. However, if the length of the transmission line tile is less than 1/00 of the wavelength corresponding to the clock frequency, then $\beta_g D_x^{n',m'} \ll 1$ and thus leading into frequency independent circuit components. As a result, the above equations are simplified to the following:

$$L^{n',m'} = \frac{Z_o^{n',m'} D_x^{n',m'} \sqrt{\mu_r}}{2c\eta_o} \tag{3.8}$$

$$C^{n',m'} = \frac{d\sqrt{\varepsilon_r}}{Z_o^{n',m'} c} \tag{3.9}$$

where η_o is the intrinsic impedance of the medium.

3.2.3 Power/Ground Pin Tiles

To model the power and ground pins connected to a current source or driver, as shown schematically in Figure 3-1(c), the equivalent circuit shown in the same figure is employed. The power pin, directly connected to the power plane, is modeled as a simple vertical inductance element and the ground pin, which is connected to the ground plane through a via hole on the power plane, is replaced by two inductances, one for the line above the power plane and one for the line below. To increase accuracy, one capacitor is added between the ground pin and the power plane, as shown in the figure, to account for the parasitic capacitive effect between the pin and the plane.

The appropriate inductance and capacitance values are computed for a given geometry from a finite element

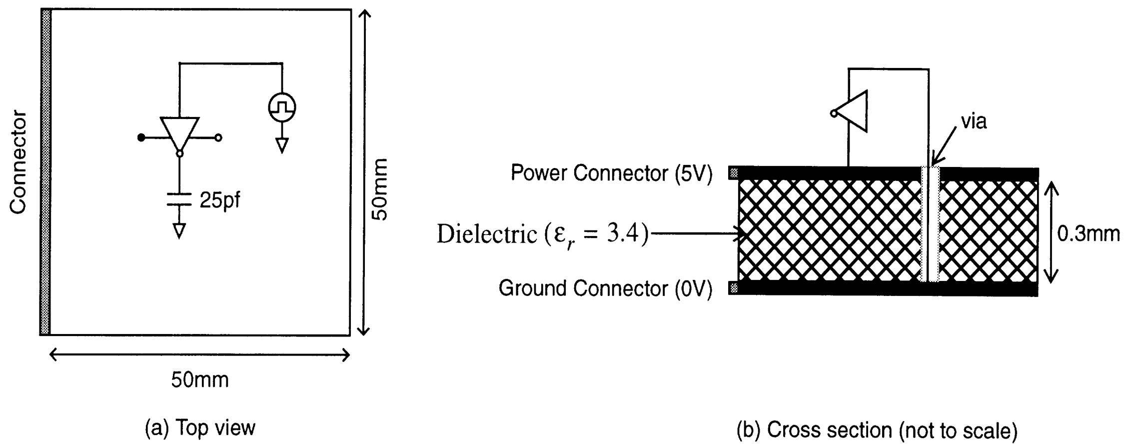

Figure 4-1: Example PCB used in the validation experiments (with signal trace included)

method (FEM) electromagnetic simulator developed at the University of Michigan [20][21]. This FEM code is based on tetrahedral edge basis functions and provides a highly accurate modeling of the fields including their dynamic effects. The values of the elements of these equivalent circuit are extracted by matching the scattering parameters derived from the FEM numerical data with the scattering parameters of the equivalent circuit representing the power/ ground pin tiles. Similar type of equivalent circuit could be derived from a simplified analytic expressions as presented in [22]. It has been found that the inductance of the pin depends on the length and diameter of each pin, but it is frequency independent. The amount of the capacitive effect between the pin and the via hole in the power plane is mainly determined by the diameters of the pin and the surrounding hole. Moreover, as the diameter of the vertical via or pin increases, the inductance of the structure is decreased due to the increased width of the current path. Similar macro-model functions can be derived for the elements of the equivalent circuits of the more complex primitives and can be stored in a library inside the tiling processor. This will make the analysis of the whole printed circuit board accurate and computationally efficient.

4 Simulation Results

The modeling and simulation methodology described above was used to analyze SSN for a number of configura-

tions of an example PCB whose physical characteristics are shown in Figure 4-1. These configurations differed in the locations of the power/ground connectors, the number and placement of the current sources and sinks, the amount of current injected by each driver, and the size and location of decoupling capacitors. We also examined, in one of the experiments, the effect of a signal trace modeled as a stripline.

Using the flow outlined in Figure 2-2, a PCB configuration was tiled and simulated in the time domain using HSPICE. Transient simulation results, in the form of voltage waveforms at the power and ground grid points, were subsequently converted to produce 3-D noise maps. In these maps, the maximum drop in voltage at each grid point on the power plane and the maximum increase in voltage at each grid point on the ground plane was plotted. All the simulations were performed on an HP 735 workstation.

Our first task was to determine how changing the number of tiles used to model the power and ground planes affected the noise map. The experimental setup is shown in Figure 4-2(a). The connectors were placed on the left side and a current source was connected between the power and the ground planes as shown. The point "p" denotes the connection to the power plane and the point "g" denotes the connection to the ground plane through a via hole. The current waveform, shown in Figure 4-2(b), was a triangular pulse with rise/fall time of 500ps and a peak value of 10mA. This waveshape was chosen to model the actual current flowing through the n- and p- transistors of a switching CMOS inverter. The noise maps for the various tiling cases are shown in Figure 4-2(c) and (d) for power and ground plane, respectively. These maps indicate a maximum voltage drop of 2.73mV on the power plane (corresponding to point "p") and a maximum voltage increase of 3.69mV on the ground plane (corresponding to "g") regardless of the number of tiles. As can be seen from the plots, the essential features of the noise maps are also the same, with maps corresponding to finer grids showing better resolution of the noise magnitude.

Figure 4-3 shows the CPU and memory usage as a function of the number of tiles for this configuration. As a reasonable compromise between accuracy and simulation time, we decided to partition the PCB into 625 tiles for all other experiments described in this section.

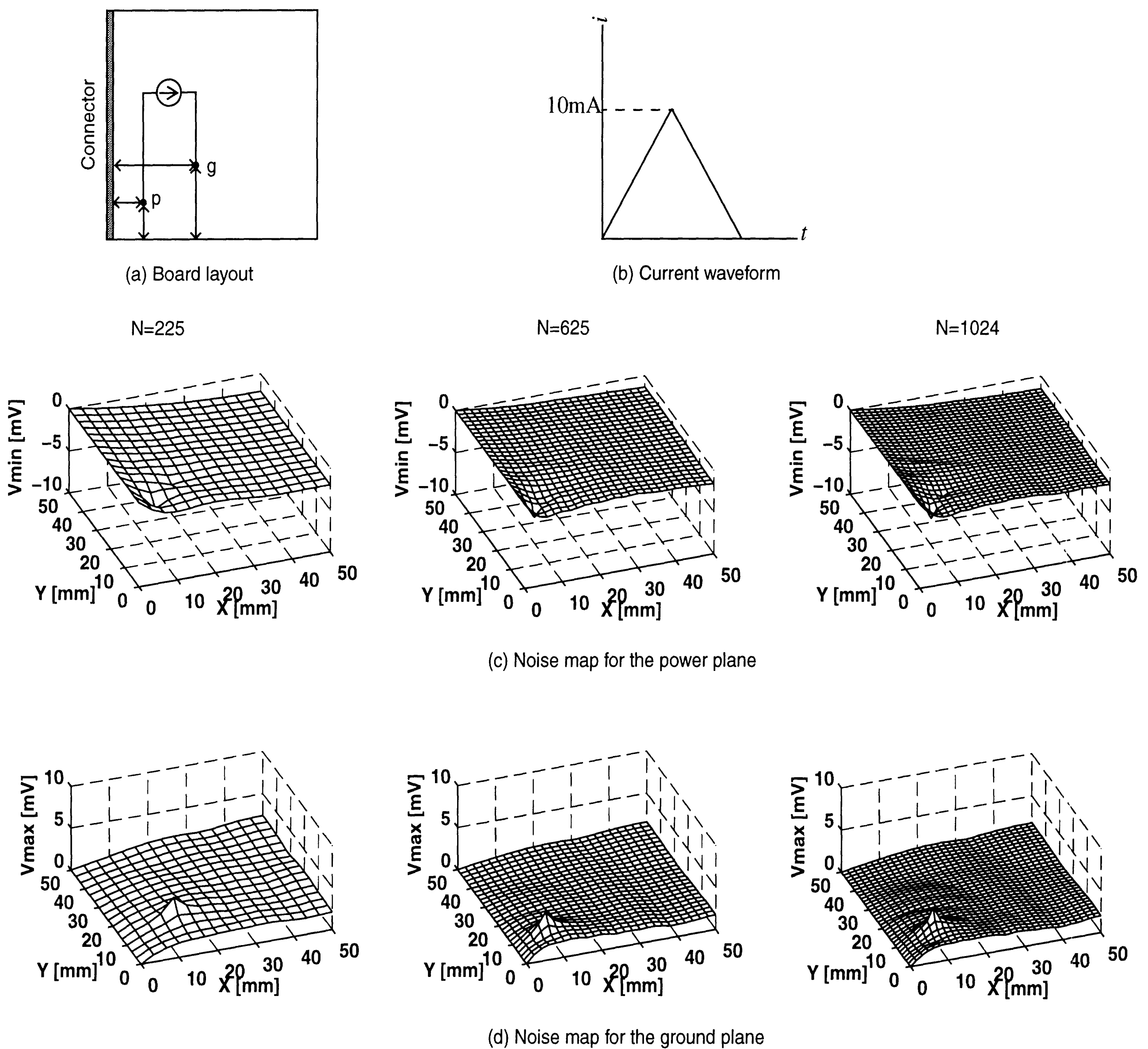

Figure 4-2: Simulation results for different number of tiles

We next varied the position of the connectors keeping the coordinates of the current injection points on the PCB the same as in Figure 4-2(a). The connectors were alternately placed on the left, top, right and bottom edges of the PCB (see Figure 4-4). We found that variation of potential on the power and ground planes was maximum when the connectors were placed on the top and right edges. This is readily explained by noting that the current injection points for these two configurations are farther away from the DC power supply than in the other two configurations, making them more susceptible to noise.

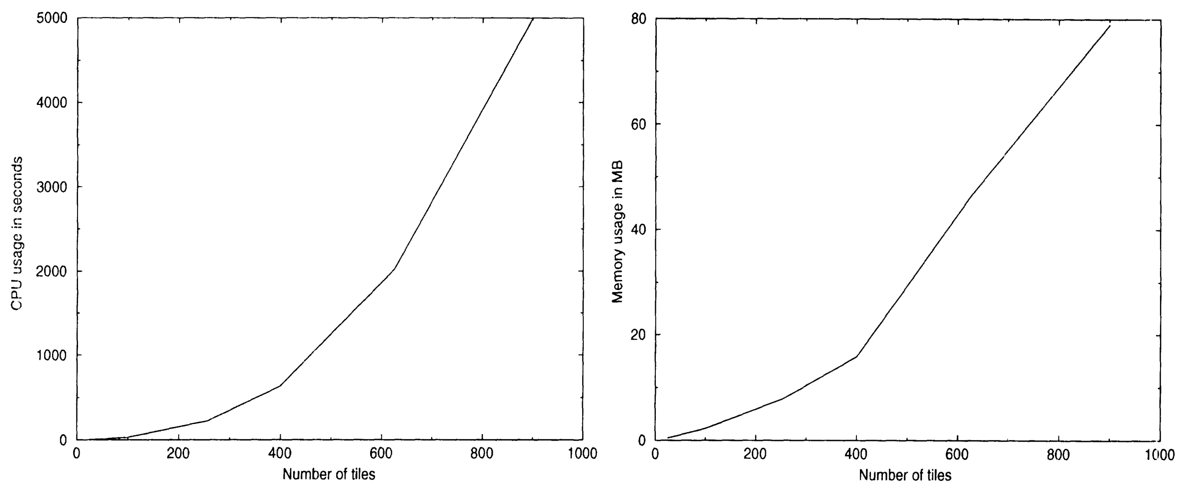

Figure 4-3: CPU and Memory usage versus the number of tiles

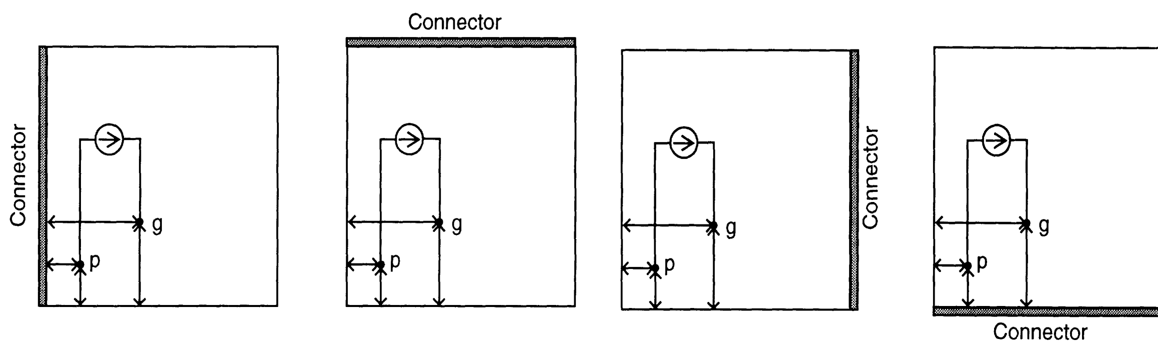

Figure 4-4: Variation in the position of the connector

In order to get more realistic values of the noise voltages, we next simulated the PCB with actual transistor drivers replacing the ideal piecewise linear current source. Seven large CMOS inverters were connected to different points on the power and ground planes. Transistor sizes and capacitive loads were chosen to represent realistic VLSI chip pad drivers: 1400μ/1.2μ for p-channel MOSFETs, 800μ/1.2μ for n-channel MOSFETs, and $25pF$ load capacitance. Each driver was excited by a 1.7ns wide voltage pulse with 0.8ns rise/fall times. The resulting noise maps are shown in Figure 4-5(a) and indicate that the maximum power and ground plane noise levels were 439.26mV and 560.93mV, respectively. In order to see the effect of decoupling capacitors, $0.1\mu F$ ideal capacitances (i.e. with no lead inductance) were connected across the power and ground leads of the seven drivers. The corresponding noise maps are shown in Figure 4-5(b) and indicate a reduction in the switching noise to 149.4mV and 98.43mV, respectively, on

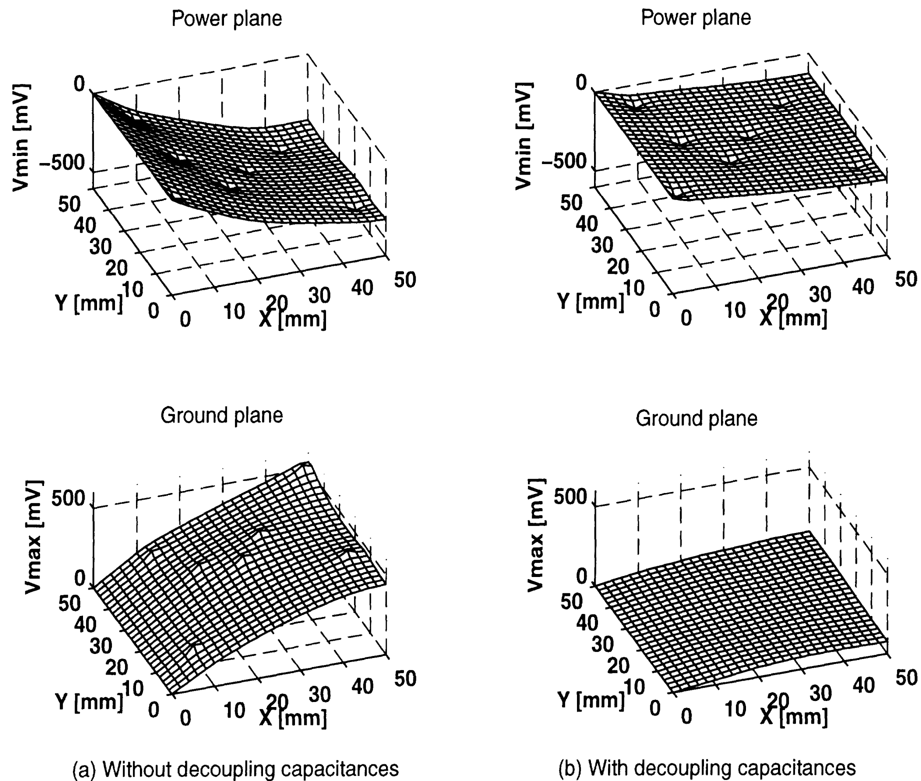

Figure 4-5: Noise maps with and without decoupling capacitors for the seven drivers case

Variation in noise levels as a function of decoupling capacitance magnitude is shown in Figure 4-6. In general, larger values of decoupling capacitance reduce the noise level. However, switching noise cannot be reduced to zero regardless of the amount of decoupling capacitance used. Instead, noise tends to a constant level beyond a certain *critical* decoupling capacitance value (the "knee" of the curves). In these experiments, this critical value was roughly $1nF$.

In the final experiment we examined the effect of a signal trace on switching noise. The PCB configuration used in this experiment and the resulting noise maps are shown in Figure 4-7. The driver and its excitation were identical to those used in the previous experiment. The noise levels in this case were 93.48mV on the power plane and 140.98mV on the ground plane and, as expected, corresponded to the locations of the driver power/ground pins. In addition, the presence of the stripline caused a slight perturbation to the potential distribution on the power plane.

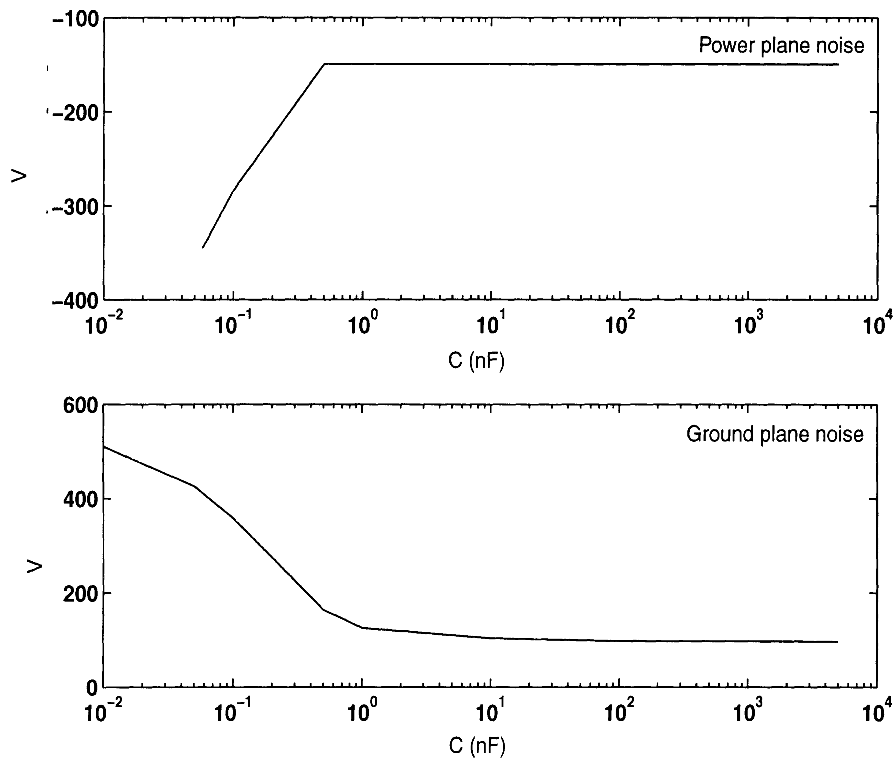

Figure 4-6: Noise variation on power and ground planes with decoupling capacitance

From these experiments, the following observations can be made:

- For a given amount of current injection, SSN increases when the current drivers are placed farther away from the equipotential connectors that supply DC power to the board.
- Maximum reduction in SSN occurs when decoupling capacitors are placed in the vicinity of the current injection points (i.e. the power and ground driver pins).
- Increasing the value of decoupling capacitance tends to reduce the magnitude of SSN. Beyond a critical value, however, further increases in capacitance have no effect on SSN. This critical value depends on the PCB configuration and the amount of current injected by the drivers.
- The presence of signal traces contributes to noise. However, limited evidence suggests that this contribution is dwarfed by that due to current injection from the drivers.

characterization of switching noise and a comprehensive understanding of its effects on PCB performance

Keywords

simultaneous switching noise, printed circuit board, decoupling capacitors,

This paper takes a first step towards evolving a systematic

analysis of SSN in printed circuit board

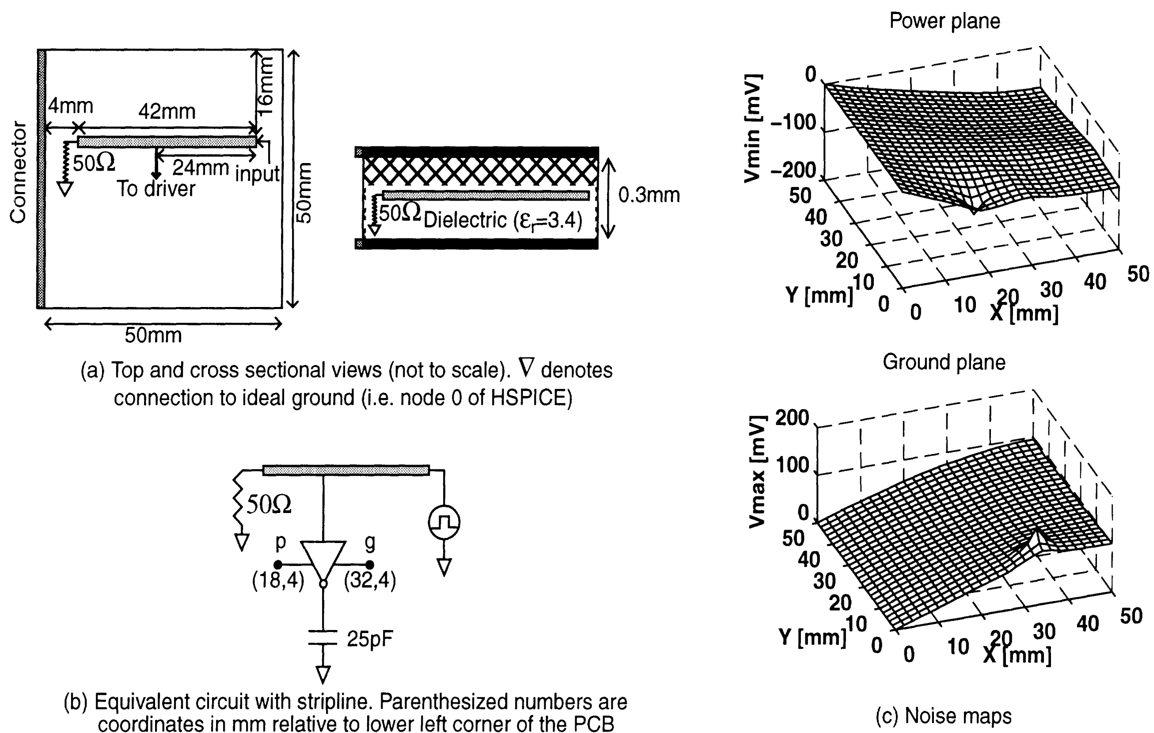

Figure 4-7: Signal trace modeled as a stripline

Additional experiments also suggested that significant lead inductances introduced by the decoupling capacitors may in some cases nullify the noise reduction benefits of these capacitors.

5 Conclusions and Future Research

This paper has presented a systematic methodology for the modeling and analysis of SSN in printed circuit boards. In this methodology the seemingly contradictory goals of modeling accuracy and global analysis efficiency are reconciled through a divide-and-conquer process. Accuracy is insured by performing detailed EM field analysis on appropriately chosen small sections of the PCB, referred to as tiles, to create lumped electrical equivalent circuit models. PCB tile models are subsequently combined with models for chip current drivers and package leads to produce an electrical simulation model for the PCB power distribution subsystem. A circuit simulator is then used to exercise this model under a variety of current excitation conditions to yield noise maps that indicate the variation in power and ground potential as a function of location on the PCB. Our future research will focus on using this model-

ing and analysis framework in a realistic design environment to optimize the placement and value of decoupling capacitors to achieve a user-specified level of noise immunity.

Acknowledgment

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