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Silicon-Based Micromachined Packaging Techniques for High Frequency Applications

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SILICON-BASED MICROMACHINED PACKAGING TECHNIQUES FOR HIGH FRQUENCY APPLICATIONS

by

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To my family.

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TABLE OF CONTENTS

DEDICATION ii

ACKNOWLEDGMENTS iii

LIST OF FIGURES vii

LIST OF TABLES xvi

LIST OF APPENDICES xviii

CHAPTER

I. INTRODUCTION 1

1.1 Motivation 1
1.2 Dissertation Overview 3

II. BACKGROUND 5

2.1 Why Silicon for Packaging? 5
2.1.1 Silicon Properties 6
2.1.2 Other Packaging Materials 7
2.1.3 Ceramics 7
2.2 The Design Cycle 9
2.2.1 Anisotropic Etchants 12
2.3 Summary 14

III. **DEVELOPMENT OF CONFORMAL PACKAGES FOR MONOLITHIC APPLICATIONS** 15

3.1 Introduction 15
3.2 Design 18
3.2.1 Transmission Lines 21
3.2.2 Microstrip Patch Antenna 26
3.3 Fabrication 29
3.3.1 Substrate Thinning 29
3.3.2 Convex Corner Compensation 32
3.4 Measurements 40
3.4.1 Transmission Line Characteristics 40
3.4.2 Noise Floor/Coupling 45
3.4.3 Cross Coupling and Isolation 46
3.4.4 Antenna Feed Performance 49
3.5 Summary 53

IV. **DESIGN OF A SI-BASED CHIP CARRIER FOR DISCRETE COMPONENTS** 54

4.1 Introduction 54
4.2 Chip Carrier Design 56
4.3 Fabrication and Assembly 63
4.4 Measurements 65
4.5 Summary 74

V. **HYBRID TECHNIQUES INTEGRATING CONFORMAL PACKAGING WITH FLIP-CHIP TECHNOLOGY** 75

5.1 Introduction 75
5.2 Circuit and Package Design 78
5.3 Fabrication and Assembly 82
5.4 Measurements 84
5.4.1 Transmission Line Characteristics 84
5.4.2 RF Components 88
5.4.3 DC Bias Components 92
5.4.4 Single Transistor Measurements 96
5.4.5 LNA Measurements 100
5.5 Summary 104

VI. PACKAGING FOR THREE-DIMENSIONAL INTEGRATION 108

6.1 Introduction 108
6.2 FGC Lines in Multiconductor Environments 112
6.3 Initial Design 115
6.4 Optimization of CPW Distribution Network 117
6.4.1 Fabrication Improvements 118
6.5 Multiconductor Circuit Performance 121
6.5.1 Impact on Distribution Network 133
6.5.2 Impact on Cross Coupling 135
6.6 Summary 137

VII. CONCLUSIONS 139

7.1 Conclusions 139
7.2 Recommendations 140

APPENDICES 143

BIBLIOGRAPHY 183

LIST OF FIGURES

Figure

Fig. 2.1:Basic design cycle for microwave circuit. 10

Fig. 2.2:Microstrip and coplanar waveguide transmission lines. 11

Fig. 2.3:Cross-section of <100> Si wafer. 13

Fig. 3.1:Concept of cavity widths needed to shield a bending line. The package width on the left is larger than the one on the right by the bend length, Lbend. 17

Fig. 3.2:Conceptual drawing of packaged microstrip line. 19

Fig. 3.3:Circuit topology: (a) Conventional microstrip on full thickness Si. (b) Packaged microstrip on reduced thickness wafer. Dimensions: h=500, W=420, w=210, t=690, L=2300, c=400, d=165, f=140, H=180, g=380, U=1250, T=1300 μm. 20

Fig. 3.4:Layout configurations. (a) Design Layout A: a through line and back-to-back right angle bend. (b) Design Layout B: two back-to-back right angle bends.. 20

Fig. 3.5:Dimensions for 50 Ω CPW structure analyzed using the point-matching method. 23

Fig. 3.6:Structures compared in LineCalc for initial packaged microstrip dimensions.(a) Conventional microstrip, and (b) conductor-backed CPW.. 23

Fig. 3.7:Layout of CPW-to-microstrip transition for probe measurements: a=500, b=985, c=285, d=200, e=1970, f=378<8°, g=385, h=420, i=375, j=385, k=350, l=150, m=150, n=100, o=p=220, q=132<229°, r=78<320°, s=60, t=100 μm.. 25

Fig. 3.8:Layout of CPW-to-packaged microstrip transition: a=165, b=220, c=435, d=250, e=2470, f=388<15°, g=150, h=210, i=540, j=120, k =114<299°, l=150 μm. 25

Fig. 3.9:The input match (S_{11}) for a patch (W=2.9 mm and L=2 mm) with bending feedline (with and without mitering) compared to a patch with a straight feedline. The patch length was increased to incorporate the frequency shift caused by mitering. See Fig. 3.21 for feedline dimensions. 28

Fig. 3.10:Fabrication process for lower wafer development. 31

Fig. 3.11:Front view drawing of a microstrip line printed on an inverted lower package with dimensions, A=850, B=100, C=400, D=150, E=210, F=380, G=750, H=148 μm. The conductors are indicated with hashed lines. This is a SEM photo of the inverted lower package developed during the two-step etch procedure. 32

Fig. 3.12:Micromachined packaged back-to-back right-angle bends. (a) The upper cavity package with probe windows for on-wafer testing. (b) Circuit layout of microstrip line which is printed on the frontside of (c) the lower cavity, which shows the reduced thickness regions in the center with the lower package channels seen as white regions. 33

Fig. 3.13:Illustration of convex and concave corners in a right-angle bend. 34

Fig. 3.14:Underetching of a convex corner is caused by the fastest etching plane {211} according to Lee [43]. 35

Fig. 3.15:Layout masks showing compensations at convex corners. (a) Lower cavity wafer. (b) Upper cavity wafer. The large squares form the package channels and the small squares form the reduced thickness regions.. 36

Fig. 3.16:Corner compensation marks: (a) CAD drawing of the mask layout, showing the corner compensation required for the formation of the lower cavity package (a=400, b=850, c=1286.5, d=2536.5, e=2351.5, f=400, g=800, h=4687, i=3437 ,j=100, k=2393.5, l=2098.5, m=1178, n=800,o=210, p=2068,q=2478,r=4978,s=2098.5) mm. (b) Good compensation from the etch. (c) Poor compensation due to the extended amount of time for the etch.. 38

Fig. 3.17:Effect of etching on square compensation for a right angle bend.39

Fig. 3.18:HFSS simulation of 7 mm microstrip line in open and lower shielded configuration. 41

Fig. 3.19:Measurement of 8 mm microstrip line in open and lower shield configuration. 41

Fig. 3.20:Microstrip effective dielectric constant. 42

Fig. 3.21:Electrical response of open microstrip circuits for a delay line and right angle bend (L=13.392 mm).. 43

Fig. 3.22:Electrical response of a packaged back-to-back right angle bend and microstrip delay line of similar length (L=13.392 mm). 43

Fig. 3.23:(a) Dimensions of open and packaged back-to-back right angle bends: (a=1970, b=2468.5, c=2078.5, d=1898.5, e=2258.5, f=848<31.5, h=5148, I=3648, j=2498.5, k= 2470, l=4464, m=1709, n=2198.5, o=424<315, p=3163.5, q=2194, r=2288, w=2483.5) µm. (b) Electrical response of an open and packaged back-to-back right angle bend (L=13.392 mm). The total loss of each line is compared to a delay line of equal physical length (13.392 mm). 44

Fig. 3.24:Layout for contact noise characterization. The boxes represent probe windows in Design Layout B (Figure 3.4) for the bend-to-bend arrangement. Probing points in the contact noise measurement are indicated by starts at Port 1 for the input signal onto the conducting line at Port 2. 45

Fig. 3.25:Noise data from contact and non-contact measurements. 46

Fig. 3.26:Comparison of cross-coupling effects in open microstrip structures for design Layout A and B (See Fig. 3.3). 47

Fig. 3.27:Cross -coupling effects in Design Layout B for two back-to-back right angle bends in open, lower half packaged, and full packaged designs.(See Fig. 3.3) 48

Fig. 3.28:Comparison of coupling between two packaged back-to-back right angle bends and the contact noise measurement of the packaged system. 48

Fig. 3.29:HFSS simulation of cross coupling between two straight microstrip lines in the conventional and packaged configurations where l=7 mm. . 49

Fig. 3.30:Conceptual drawing of packaged antenna configuration. 51

Fig. 3.31:Layout of antennas: (a=1140, b=789, c=2900, d=2200, e=105, f=8135.5, g=2673, h=750, I=970, j=210, K=8835.5, l=2470, m=183<55,

n=7123.5, o=6900, p=2000) μm. 52

Fig. 3.32:Return loss for a patch antenna with open and packaged microstrip feedlines. 52

Fig. 4.1:Actual photograph of K/Ka-Band ceramic package for phase shifter chip. 57

Fig. 4.2:Schematic drawing of K/Ka-Band package for phase shifter chip. Courtesy of Yook [58]. 58

Fig. 4.3:Transmission lines used in RF input/output interconnects: microstrip, stripline, and shielded microstrip.. 58

Fig. 4.4:3-Dimensional rendering of Si package. 61

Fig. 4.5:Process layers superimposed. 62

Fig. 4.6:Pyramidal via micromachined with anisotropic etchant and Cr/Au overlay pad. 63

Fig. 4.7:Designs for Si package: Design #1-Shifted vias and I/O line, Design #2-Shifted vias and centered I/O line, Design #3-Aligned vias and centered I/O line. 64

Fig. 4.8:Cross-section A'-A of package layers. 65

Fig. 4.9:Cross section B-B' shows the assembly of the IC into the package. . 66

Fig. 4.10:Top view of Si package without metal layer or vias filled.. 67

Fig. 4.11:Block diagram of the package interconnects used in the Libra simulation. 68

Fig. 4.12:RF input feedthrough with CPW-to-microstrip transition for on-wafer measurements. 68

Fig. 4.13:S-Parameters for Libra interconnect simulation, alumina package (within test fixture), and shielded Si package. 70

Fig. 4.14:Computed vertical electric field distribution (dB scale) in the asymmetric alumina package at 29.5 GHz. Courtesy of Yook [60]. 71

Fig. 4.15:Cross-section (A'-A) of the alumina and Si package illustrating the cavity side wall created by the vias. (Units in microns.) 71

Fig. 4.16:Comparison of attenuation for two metal thicknesses for an 8 mm long microstrip line. the typical length with two metal thicknesses. . 73

Fig. 4.17:S-Parameters for a symmetrical package with and without lid added. 74

Fig. 4.18:S-Parameters for different package designs: Completely symmetric (Design #3), shifted vias (Design #2), asymmetric (Design #1). 75

Fig. 5.1:Substrate area for MCM versus substrate area for 3-D technology [68]. 77

Fig. 5.2:Si micromachined two-layer packaged circuit. The upper wafer shields conductors and provides support for vertical integration. 78

Fig. 5.3:Cross-section of packaged FGC line and upper shielding cavity (with or without metallization) of height hc=275, wg=500, w=53, s=94, h1=500, h2=400, d=385, g=200, wc=800 μm. 79

Fig. 5.4:Schematic diagram of microstrip and FGC 3-stage LNA. 81

Fig. 5.5:Libra simulated insertion gain for original design (Libra_Ideal) and corrected design (Libra_corrected) for fabrication. 82

Fig. 5.6:FGC mask layers for LNA. 83

Fig. 5.7:Photograph of 1/4 of a 4 inch wafer used for fabricating LNA circuit. Notice two circuits in the center with test devices and cal standards on the edges. 84

Fig. 5.8:Attenuation for different packaging environments. 86

Fig. 5.9:Cross-section for conventional, dielectric shielded, and metal shielded FGC lines. 87

Fig. 5.10:Effective dielectric constant for different packaging environments. 87

Fig. 5.11:Cross coupling measurements for different two planar FGC lines (Dimensions in microns). 88

Fig. 5.12:HFSS simulation of similar FGC layout where the ground planes edges are separated by 871 microns. 88

Fig. 5.13:Cross coupling between planar lines separated 774 microns edge-to-edge. 89

Fig. 5.14:Open balanced stub with dimensions: L1=753, L2=1752, L3=2485, L4=630, L5=698. Units are in microns. 90

Fig. 5.15:Photograph of shunt stub and corresponding shielding cavity inverted to show etching and convex corners. 90

Fig. 5.16:Comparison between measured and simulated S-parameters for balanced open shunt stubs. The simulation considers air bridges and T-junctions. 91

Fig. 5.17:Comparison of S-parameters for the balanced open shunt stubs for the fabricated cases (no shield, dielectric shield, metal shield) versus the simulated case. 91

Fig. 5.18:Open series stub resonator used for DC block. The stub length is 1568 microns for the design frequency of 23 GHz. 92

Fig. 5.19:Comparison of reflection and transmission coefficients of the open series stub for calculated (Momentum), open (no shield), metal shield, and dielectric shield environments. 92

Fig. 5.20:Loss comparisons between measured open-end series stubs. . . . 93

Fig. 5.21:Layout of resistors in parallel and series. 94

Fig. 5.22:Cross-section and top view of capacitor structure used in LNA circuits with dimensions: a=500, b=200, c=226, d=160, e=2640, f=220, g=627, h=94 μm. 96

Fig. 5.23:Equivalent circuit for capacitors across FGC line. 97

Fig. 5.24:RF capacitance measurements before and after adding airbridges. 97

Fig. 5.25:Insertion gain for single transistor. Measured on InP wafer (transistor only), mounted without shielding (No shield), and mounted with metal shield covering transmission lines. 98

Fig. 5.26:Layout for solder well and flip-chip device (a=1000, b=1000, c=1200, d=200, e=500, f=500: All units in microns). 99

Fig. 5.27:Device and pad after bonding to the Si substrate. 100

Fig. 5.28:The SEC model 410 aligns and attached the flip chip die onto the machine. 100

Fig. 5.29:Measured insertion gain of amplifier using two calibrations with VDS(123)=3 V, VGS(123)=-1.1 V, IDS(TRL)=145 mA, IDS(SOLT)=143 mA.. . . . 102

Fig. 5.30:Comparison of insertion gain for Libra_corrected and Libra_IE3D simulations . . . 106

Fig. 5.31:Comparison of measured LNA performance with Libra_IE3D simulation. . . . 107

Fig. 5.32:Comparison of measured LNA with Libra_Physical simulation. . . 108

Fig. 6.1:Conceptual 3-D view of the W-Band power cube showing the micromachined wafers and metal layers. . . . 110

Fig. 6.2:Layout of initial design of distribution network with antenna feed and patch shown. The vertical interconnect is on the bottom side of the MMIC layer while the slots and patch antenna are on the feed and antenna layer, respectively. . . . 112

Fig. 6.3:3-D environment geometries for the transmission lines. . . . 114

Fig. 6.4:Attenuation for line architectures. . . . 115

Fig. 6.5:Effective dielectric constant for line architectures. . . . 115

Fig. 6.6:Single 1 x 4 distribution network: (a) CPW-based Wilkinson distribution network design, (b) Coupled CPW Wilkinson distribution network design. . . . 117

Fig. 6.7:Performance of first iteration distribution networks where (a) is the CPW-based design and (b) is the CPW/slotline design. . . . 117

Fig. 6.8:Layout of distribution network and coupling between adjacent ground planes separated by 300 μm. . . . 118

Fig. 6.9:Layout of two 100 Ω resistors in parallel to create the 50 Ω termination impedance used in the distribution network. a) Poor alignment, b) additional FGC circuit metal to keep pad dimensions. (Not drawn to scale) . . . 120

Fig. 6.10:Airbridge arrangement for CPW-based power divider. . . . 121

Fig. 6.11:Photograph of individual dividers. The ground planes in (a) have been truncated (b) to reduce parasitic effects in the return loss of the in-

dividual device. 122

Fig. 6.12:Cross-section of FGC lines used for distribution network design. The wafer thickness if 100 mm and the metal thickness is approximately 1 mm. 123

Fig. 6.13:Layout of final distribution network design. 124

Fig. 6.14:S-Parameter measurements of the distribution network in a conductor backed environment.. 125

Fig. 6.15:Four architectures for individual component measurements.. . 126

Fig. 6.16:Single divider isolation, input port matched. 126

Fig. 6.17:Single divider isolation measurements for four architectures. . 127

Fig. 6.18:Tee junction isolation with input port terminated. 127

Fig. 6.19:Tee junction isolation measurements for four architectures. . . 128

Fig. 6.20:Tee junction input match for four architectures. 129

Fig. 6.21:Insertion loss for tee plus bend circuit in four architectures. . . 129

Fig. 6.22:Tee with bend S parameters for conductor backed and packaged environments. 130

Fig. 6.23:Measured insertion loss of back-to-back dividers for four architectures. 131

Fig. 6.24:Measured S parameters of back-to-back divider for packaged and conductor backed environments. 131

Fig. 6.25:Measured insertion loss of double bend circuit for four architectures. 132

Fig. 6.26:Measured S parameters of double bend in packaged and conductor backed environments.. 132

Fig. 6.27:Insertion loss of single divider in four architectures.. 133

Fig. 6.28:S Parameters of single divider for packaged and conductor backed environment. 133

Fig. 6.29:Measured S parameters for distribution network in conductor

backed and packaged environments. 134

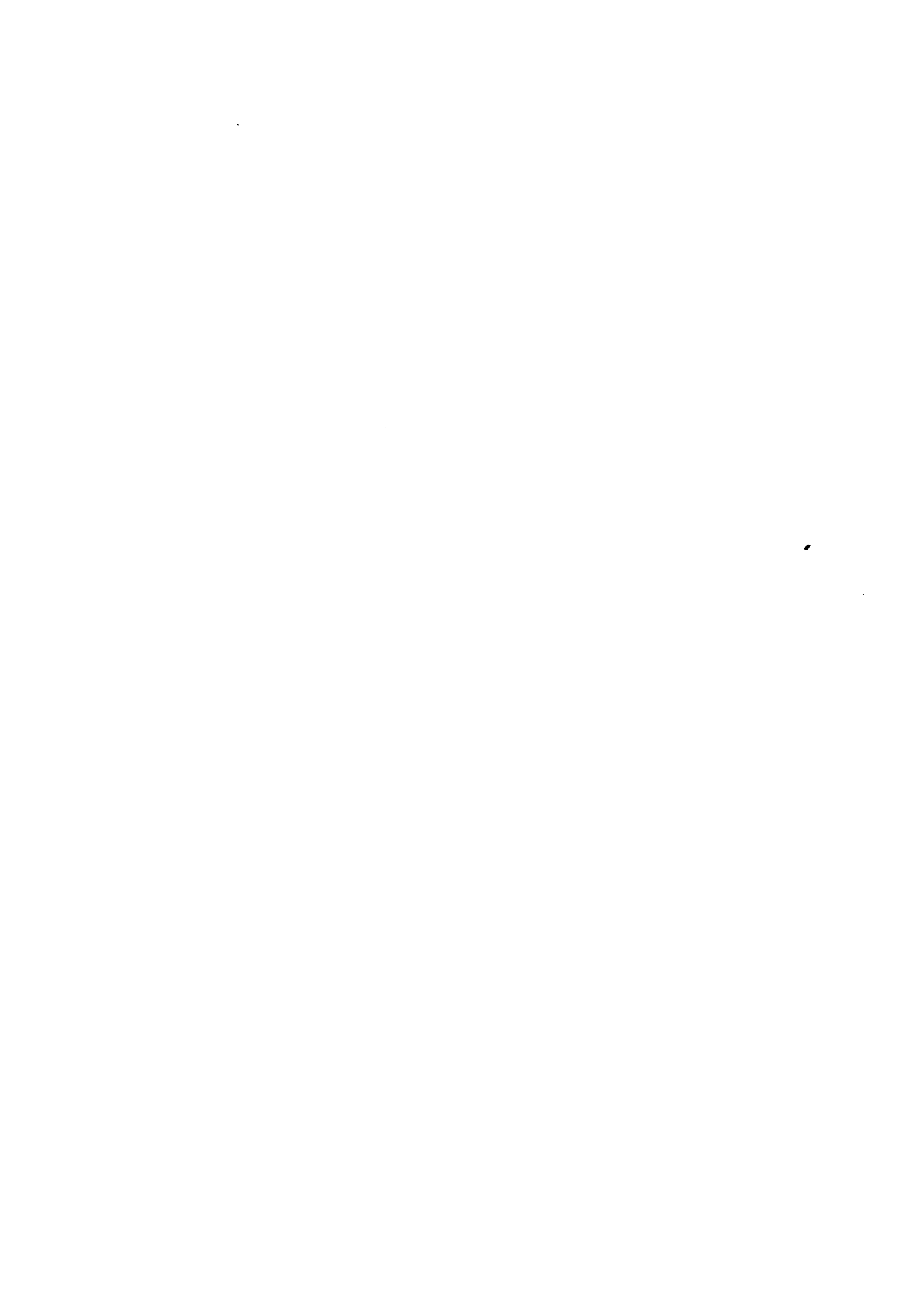
Fig. 6.30:Distribution loss for all four outputs is approximately -1.5 +/- 0.3 dB and phase balance is +/- 2 degrees. 135

Fig. 6.31:Cross-coupling measurements of layout with metal backed structure and no upper shielding cavity. 136

Fig. 6.32:Cross-coupling measurements of layout with upper shielding cavity and Si carrier. 137

Fig. 7.1:Simulated response of coupling between 50 Ω microstrip lines separated by the distances of 1.58, 2.58, and 4.58 mm. 142

Fig. 7.2:Simulated response of coupling between 50 Ω FGC lines separated by no distance, 0.87 mm, and 1.6 mm. 142



LIST OF APPENDICES

Appendix

A. HOW MMIC PROCESSING AFFECTS THE ATTENUATION OF FGC LINES AT W-BAND 144

A.1 Introduction 144
A.2 Methods 145
A.3 Results 146
A.4 Summary 149

B. FABRICATION OF PACKAGED MICROSTRIP 150

B.1 Introduction 150
B.2 Circuit Wafer with Lower Cavity 150
B.3 Shielding Cavity Fabrication. 156

C. FABRICATION OF SILICON CHIP CARRIER 160

C.1 Introduction 160
C.2 Fabrication Steps 160

D. FABRICATION OF A 3-STAGE LNA CIRCUIT 165

D.1 Introduction 165
D.2 Circuit Wafer Fabrication 165
D.3 Shielding Cavity Fabrication. 171

E. FABRICATION OF W-BAND OUTPUT DISTRIBUTION NETWORK 175

E.1 Introduction 175
E.2 Circuit Wafer Fabrication 175
E.3 Shielding Cavity Fabrication. 179

CHAPTER I

INTRODUCTION

1.1 Motivation

Once used exclusively by the defense industry, the technology for radio frequency (RF), microwave, and millimeter-wave systems is now becoming more important to the commercial sectors, automotive, medical, and communications (ground- and space-based) industries [1]. Performance, cost, and reliability of the product are three factors which govern the type of technology used in production. Space communications and medical industries desire reliable high performance components. The ground-based communications sector emphasizes a low-cost solution. It is estimated that by the year 2003, approximately one-third of the U.S. population will use wireless phone services. Therefore, the development of high-performance, low-cost circuits is important.

Circuit design and integrated circuit (IC) fabrication techniques have become so advanced that components are being developed that meet single circuit specifications, but limit overall performance when incorporated into a system. In recent years, however, it has been shown that the electronic packaging for many of these components is a primary source of system degradation [2]. Thus, poor design and fabrication of packages have led to increased cavity resonances and cross-talk between neighboring circuits.

Everyone in the semiconductor industry will admit to neglecting package design to improve circuit performance and to considering the package after the component has been optimized [3], [4], [5]. Now that the package has become a limiting factor in high-frequency system development, it is very important to include package development within the circuit design cycle.

An electronic package must provide electrical, mechanical, and thermal support for a circuit. The package design must also be amenable to the circuit it is protecting by providing low loss interconnects. The mechanical structure of the package should provide stability for the circuit and protect it from harsh environmental conditions. Because electrical circuits dissipate energy in the form of heat, thermal properties of the packaging material are important. Materials which function as heat sinks are desired for high-frequency high-power applications. These characteristics have been quantified as material properties and ultimately are useful if the material can be machined to protect the electronic device.

Given these basic requirements in addition to the fact that the circuits are operating at high frequencies, novel packaging schemes are needed. Not until industry decides on a standard technology, will batch fabrication be used to realize low-cost packages for millimeter-wave applications. Plastic packages are low in cost but offer high electrical protection only up to 5 GHz [6]. Despite the fact that alumina package performance is better, it begins to degrade beyond 10 GHz and provides inadequate thermal protection [7],[8]. The research question this dissertation addresses is: ***Can silicon (Si) be used as an electronic packaging material for high-frequency circuits?***

Although the electrical properties of Si have resulted in it being the choice as the standard for very large scale integration (VLSI) design, microelectro-mechanical systems (MEMs) research has taken advantage of the mechanical

properties and developed low-cost, high-performance sensors and actuators [9], [10].

Within the last 10 years, Si micromachining techniques have been used to improve high-frequency circuit performance and to develop monolithic packages that mechanically protect circuits [11], [12]. The excellent electrical results obtained from these efforts have been the stimulus for continued exploration of Si as a packaging material for high-frequency applications. This research is important because it will show the feasibility of using packaged Si circuits for millimeter wave three-dimensional on-wafer systems.

1.2 Dissertation Overview

The experimental characterization of Si-based packages for high-frequency applications is presented in this dissertation. Designs have been developed using simulation tools and low-frequency models. Prototype packaged circuits have been fabricated and tested for electrical performance. Results for transmission line characteristics and cross-coupling are used to extend the designs to high-frequency microwave and millimeter-wave systems. Following is an overview of the organization of the dissertation.

Chapter 2 explains the evolution of Si from an electrical material to a mechanical material in microwave circuit design. The properties of Si are presented and compared to currently used packaging materials.

Chapter 3 presents the characterization of an integrated conformal package for monolithic applications. Parasitic radiation typical in microstrip and due to bending geometries is reduced by incorporating the package design with the circuit. Cross-talk between neighboring microstrip lines is eliminated and allows for increased circuit density on the substrate. Variable substrate thick-

ness wafers are developed which offer an additional degree of freedom for the circuit designer, when posed with the challenge of incorporating circuits and antennas on one substrate for optimal performance.

Chapter 4 presents the development of a Si-based package for discrete components. This effort is intended to show that Si micromachining techniques can be used to realize single-chip as well as on-wafer packages that offer high-performance capability up to 40 GHz. The package can be scaled to higher frequency applications and if batch-fabricated, cost an order of magnitude less than it's conventional alumina counterpart.

Chapter 5 presents a study of on-wafer packaging for K-Band circuits. The influence of metal and dielectric shielding on finite ground coplanar (FGC) lines is compared to a conventional unshielded line. Si micromachining is incorporated with flip chip bonding techniques to realize a three-stage low-noise amplifier (LNA) circuit with monolithic packaging.

Chapter 6 reports on an extensive study of three-dimensional environment effects on high-frequency planar circuits. The development of on-wafer packaging for a 94 GHz multi-level antenna array system is demonstrated with detailed characterization on the performance of four (1 x 4) output distribution networks in various packaging architectures.

Chapter 7 summarizes the work presented in the dissertation with concluding remarks and recommendations for future research.

CHAPTER II

BACKGROUND

2.1 Why Silicon for Packaging?

Silicon (Si) has been the material of choice for ICs in the semiconductor industry since the late 1950s. It surpassed germanium in the area of electrical performance and high-temperature processing for transistors. The first planar IC process with a monolithic transistor was demonstrated by Noyce in 1959 at Fairchild Semiconductor [13] and started the microelectronics revolution. Because Si is used for 90% of all ICs today, characterization and development of the material have resulted in low-cost wafer processes which produce excellent individual circuit performance.

With the advent of World War II and the use of radar (Radio Detection and Ranging), an extensive amount of research was conducted in the area of microwave engineering. In the 1940s the Radiation Laboratory was established at MIT where microwave network theory and experimental and theoretical studies of waveguides were developed by top physicists [14]. Although the introduction of the waveguide revolutionized the microwave industry, this transmission line was large, expensive, and limited in bandwidth. The development of planar transmission lines began as far back as the 1930s but research in earnest came in the 1950s with the invention of the stripline by R. M. Barrett [15]. With the advances seen in the semiconductor industry, micro-

wave engineers decided to incorporate those techniques to develop miniaturized microwave integrated circuits for communication and radar applications in the early 1960s. Because the processing techniques in the semiconductor industry were automated, performance of microwave circuits improved tremendously. These microwave integrated circuits (MICs) offered a reduction in size, volume, and cost.

While extensive Si research was taking place in the electronics industry, the transducers industry was investigating Si for various reasons as well. Micromachining techniques were used to create low-cost, high volume, miniaturized visible image sensors (1960s), pressure sensors (1970s), and microsystems (1980s), devices which integrate mechanical and signal-processing electronics.

In the late 1980s, microwave engineers became aware of how micromachining techniques could be useful in removing material in Si circuits and thereby reducing parasitic effects observed at high frequencies. Efforts were begun at California Institute of Technology [16] and the University of Michigan [17] [18], [19] to incorporate micromachining techniques to develop high-performance interconnects, antennas, and passive circuits. To reduce high-frequency measurement errors, Drayton and Katehi proposed a micromachined package circuit for Si-based circuits [20]. By incorporating an upper shielding cavity, Drayton and Katehi reduced radiation loss and could measure the true effects of the circuit within a packaged environment. Since that time, efforts have been made to develop Si-based packages for high-frequency circuits and antennas.

2.1.1 Silicon Properties

Materials for electronic packages are very important to the microwave engineer. In addition to providing the electronic circuit with physical support and thermal protection, the package transfers energy from the rest of the system to the individual circuit. In high-frequency applications where it has been proven that the package limits performance of the circuits, it is very important to incorporate the electrical characteristics of the packaging material when designing a microwave system.

The electrical properties of Si have enabled the semiconductor industry to use it as the primary dielectric material in developing ICs [21] while the mechanical properties of Si have been utilized to develop high performance MEMs structures. These two properties in addition to the thermal characteristics of Si make it a potential candidate for packaging high-frequency circuits.

2.1.2 Other Packaging Materials

The most commonly used packaging materials are plastics and ceramics. Thermoplastic and thermoset plastics are the least expensive packaging materials and work well at low frequencies. As the frequency increases to approximately 3 GHz, this material is no longer useful because of performance limitations. In addition, defense-related applications require extensive testing and long-lifetime capabilities, while most plastic packages experience early failure in adverse environment conditions.

2.1.3 Ceramics

Ceramics are more popular for applications up to 20 GHz, with aluminum oxide, beryllium oxide, and aluminum nitride (AlN) the materials ordinarily used. Aluminum oxide (alumina) is by far the most characterized of these materials and provides excellent insulation and mechanical support for low power circuits. High-power applications require packaging materials with thermal conductivity values that allow it to function as a heat sink for the circuit. Beryllium oxide (beryllia) is the material of choice for high power specifications because its thermal conductivity is ten times greater than that of alumina. The cost of beryllia and toxicity of the material limit its use to extreme situations where high-power efficiency is very important. The thermal coefficient of expansion (TCE) for alumina is another limiting factor of this packaging material, especially when varying temperature conditions exist for circuit applications. The TCE of AlN is very close to that of Si and other semiconductor materials, while the TCE of alumina is greater, which implies the packaging material will expand more easily due to temperature changes. AlN is an expensive and relatively new material which is being used for specific applications but has still not been firmly adopted by industry.

No one ceramic material can satisfy all the requirements for high-frequency circuit packages and the introduction of another potential substrate will provide the industry with more design options. Table 2.1 lists mechanical and thermal properties of alumina (Al_20_3) and Si.

Properties	Si	Al_2O_3
Thermal conductivity, W/m°K	150	20
CTE from 25-400 °C	3.5	7.1
Density, g/cm^3	2.33	3.75
Grain size, μm	single crystal	5.0
Yield Strength, 10^{10} dyne/cm^2	7.0	15.4
Bonding strength, kg/mm^2	10-50	25-35
Young's modulus, 10^{12} dyne/cm^2	1.9	5.3
Poisson ratio	0.2782	0.22
Sintering temperature, °C	1412 (MP)	1300
Knoop Hardness, kg/mm^2	850	2100
Max. use temp. (nonoxidizing atmosphere), °C	1400	1500
Dielectric constant	11.7	8.9-10.2

Table 2.1: Mechanical and thermal properties of alumina and Si.

2.2 The Design Cycle

The design cycle for conventional high-frequency circuits typically incorporates packaging requirements after circuit performance optimization. Low-frequency cavity resonances and incompatible thermal characteristics are two common problems which limit the performance of the circuits.

By including package requirements along with circuit specifications in the initial design, the chances of developing a component which will perform as expected is much higher. Figure 2.1 shows the design cycle used in developing the packaged circuits presented in this dissertation.

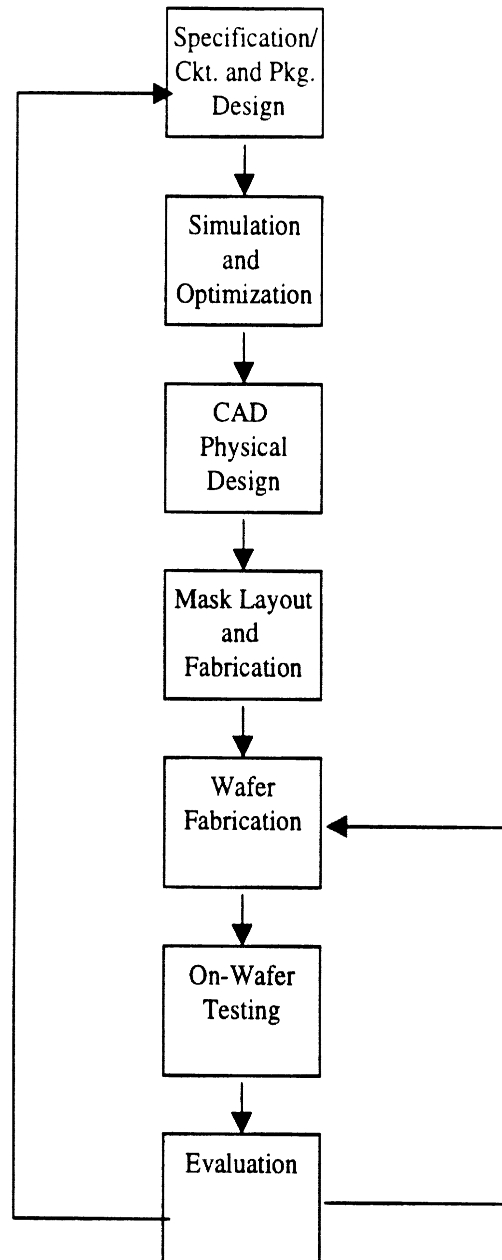


Fig. 2.1: Basic design cycle for microwave circuit.

Design specifications typically include a proposed budget, time-line, and performance requirements. Depending on the application, a designer may be

limited in the line architecture which can be used. The two transmission lines most commonly used for circuit design in this dissertation are microstrip and coplanar waveguide (CPW).

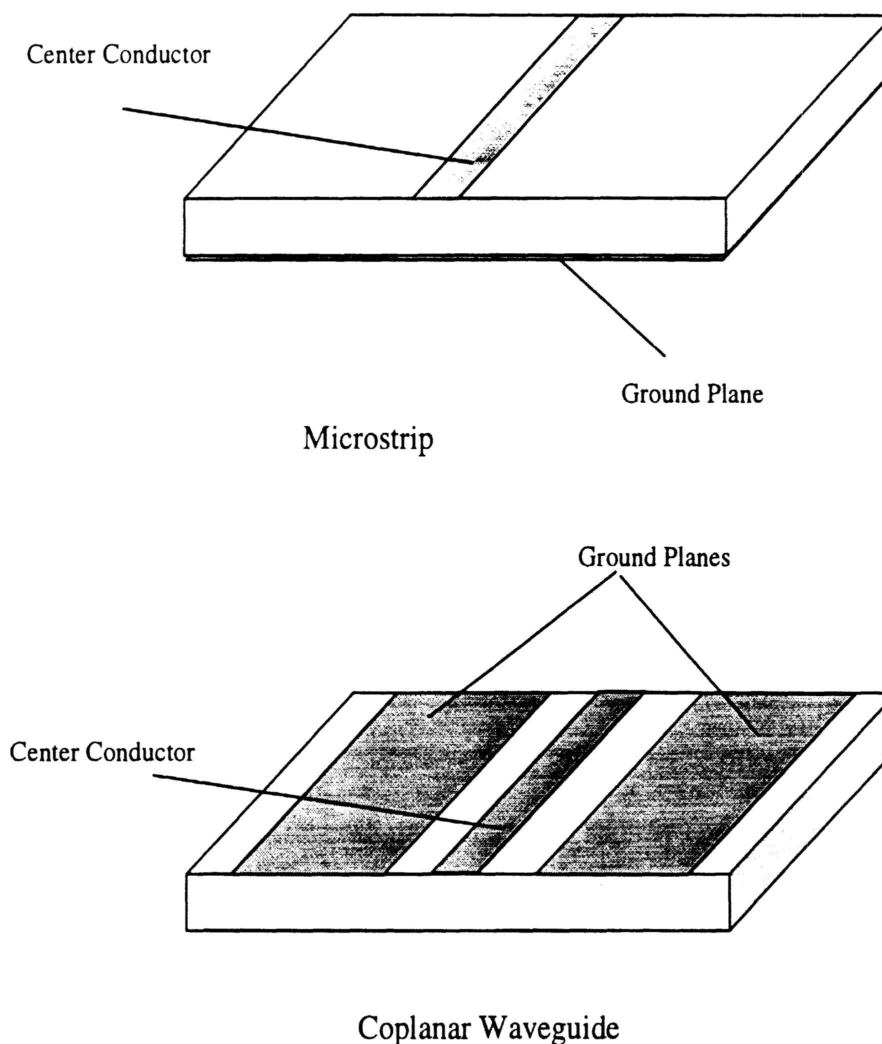


Fig. 2.2: Microstrip and coplanar waveguide transmission lines.

Both lines can be easily fabricated using photolithographic techniques and propagate a single mode. A large library of closed form expressions have been derived for microstrip and make it easier to simulate and optimize the line for circuit design. Higher order modes, parasitic radiation, and losses are introduced when discontinuities exist along the line, or it is operating near the cut-

off frequency which is dictated by the line geometry and substrate thickness. Variations of the microstrip line have been introduced to accommodate for the wide range of design needs. With CPW transmission lines the conductors are printed on the top side of the substrate material and mounting devices in shunt or series arrangements can be easily done.

Micromachining techniques can be combined with standard planar transmission line processing to develop on-wafer shielding cavities for circuits and interconnects. These cavities provide a packaged environment which helps reduce the parasitics most commonly found in these structures. This technique increases the number of options for the designer when low loss and high isolation may be major design concerns.

2.2.1 Anisotropic Etchants

The anisotropic etchants used to micromachine Si are listed in Table 2.2:. The fastest and most toxic etchant is ethylene diamine pyracathecol (EDP_f) with an etch rate of 80 μm/hr on the <100> crystal plane [22], [23]. By adjusting the chemical composition and reducing the temperature, the etch rate can be reduced to 40 μm/hr a more controllable rate for etching very thin Si (<200 μm). Potassium hydroxide (KOH) is a safer etchant with a slower etch rate (30 μm/hr) but etches silicon dioxide (SiO_2) a common masking film [24]. Tetramethyl ammonium hydroxide (TMAH) is also very safe and etches Si at a rate of 35 μm/hr [25]. The etch rate can be increased by adding deionized water (DI water) but hillocks can be formed and ruin the smooth sidewall profile. The <111> crystal plane acts as an etch stop and realizes the pyramidal shape shown in Fig. 2.3.

Etchant	Composition	Temp. °C	Etch Rate (μm/hr)	Masking Films	Safety
EDP_f	Ethylene Diamine 150mL Pyrazine 0.9 g Catechol 48 g DI Water 48 mL	110	80	$Si0_2$, Si_3N_4	Toxic
EDP_s	Ethylene Diamine 150mL Pyrazine 0.9 g Catechol 32 g DI Water 48 mL	100	40	$Si0_2$, Si_3N_4	Toxic
KOH	KOH 80 g DI Water 80 mL	65	30	Si_3N_4	Safe
TMAH	TMAH, 25 wt.%	100	35	$Si0_2$, Si_3N_4	Safe

Table 2.2: Anisotropic etchants.

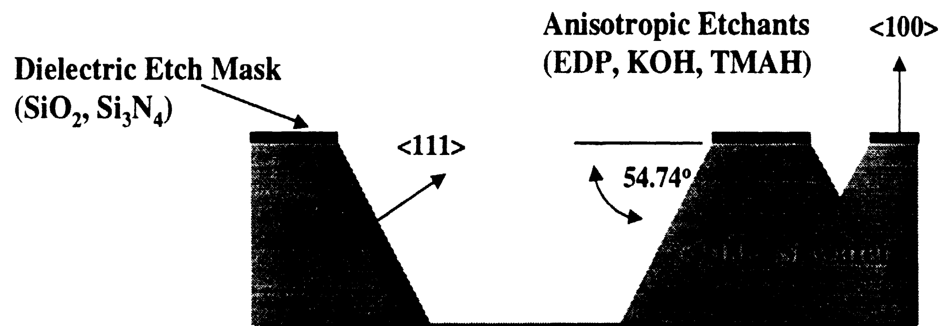


Fig. 2.3: Cross-section of <100> Si wafer.

2.3 Summary

The following four chapters give technical detail about the design, fabrication, and testing of micromachined Si packaged circuits and interconnects K- to W-Band applications. Electronic packages for discrete, monolithic, and hybrid applications will be presented. The common theme in each design is the integration of standard IC processing with Si micromachining techniques to produce a high performance package for circuits which can be batch-fabricated to reduce manufacturing costs.

CHAPTER III

DEVELOPMENT OF CONFORMAL PACKAGES FOR MONOLITHIC APPLICATIONS

3.1 Introduction

Dense circuit and antenna layouts in many high-frequency applications suffer from poor performance due to cross-talk between neighboring elements. In fact, as the criteria for high-performance circuits require better cost-effective solutions that are small, lightweight, and compact, techniques to reduce cross-talk will have an even larger impact on improving the overall performance of circuits implemented in on-chip configurations. Low-cost solutions that produce compact circuit designs heavily depend on the ability to utilize existing circuit space.

Unfortunately, as more circuits are located in close proximity to each other, cross-talk effects become more pronounced, especially as the operating frequency increases. In the past, design solutions focused on reducing system size and weight, but were limited in overall success because of failure to achieve high electronic circuit isolation. Using advanced computational methods and high-speed computer resources, simulations were employed to predict individual circuit performance. Complex layouts were implemented using CAD tools for system realization, however, the measured electrical perfor-

mance was degraded because the simulations did typically consider electromagnetic interactions between closely spaced components. Cross-talk occurred from unwanted signal propagation within the circuit environment either in air or through the substrate and reduced the system performance.

Several design approaches have been investigated to reduce the interactions between elements placed in close proximity within a given circuit layout. One approach uses sophisticated numerical models to determine the appropriate component placement for a variety of planar geometries [26]. While the results offered layout solutions which address performance requirements, space and size criteria were not met by these designs. Another approach separates large systems into smaller units with comparable circuit functions (similar to multi-chip-modules) [27] to minimize the interactions. Although effective for large scale integrated (LSI) circuits, this approach does not address the issues associated with electromagnetic field interactions due to the excitation of waves in the substrate. In addition to the above, conventional packaging in high-frequency circuit designs, however, suffer from parasitic coupling between the circuit and package due to low-frequency resonances created by the large package housing.

With the advances in semiconductor integrated circuit (IC) and monolithic microwave IC (MMIC) processing today, novel solutions can be implemented so that both the design specifications and electrical performance requirements can be met. In the early eighties, Petersen [21] predicted that Si as a mechanical material could be used to develop high-precision, miniaturized structures that offer high performance. Since then, RF micromachining of Si has become an enabling technology to high-frequency circuit design [28].

Si micromachined packages for CPW circuits have been characterized with miniature upper and/or lower cavities that shield the circuit conductor and

dielectric to reduce parasitic radiation and substrate modes [20]. In this study, micromachined conformal packages are designed to shield meander microstrip lines commonly found in high density layouts. These monolithic housings offer a shielded environment to each transmission line, and have package resonances at much higher frequencies than rectangular packages (Fig. 3.1) [29].

In an effort to explore the effectiveness of packaging individual lines to reduce cross-talk and improve high-frequency propagation, performance comparisons are made between conventional and packaged microstrip. Two meander lines are placed less than an inch away from each other to study how cross coupling is reduced with upper and lower shielding cavities.

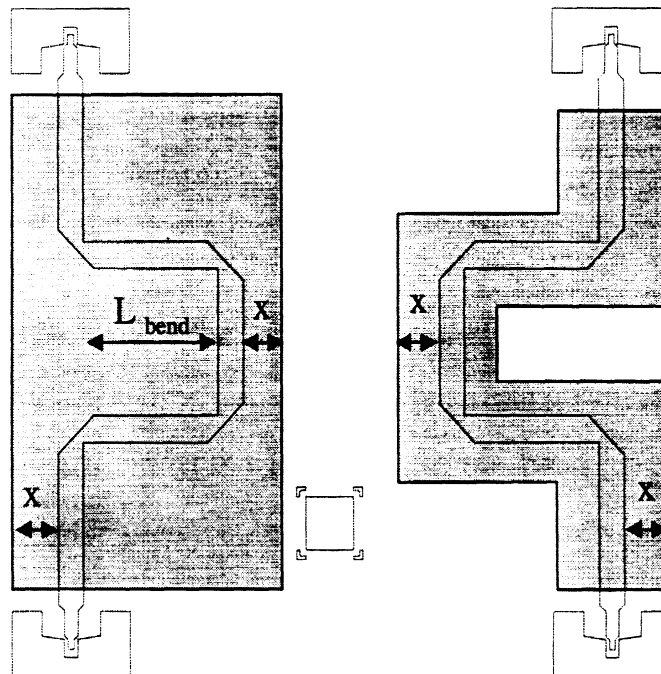


Fig. 3.1: Concept of cavity widths needed to shield a bending line. The package width on the left is larger than the one on the right by the bend length, L_{bend}.

3.2 Design

This section presents the development of a conformal package for microstrip-based circuits. Microstrip is one of the most commonly used transmission line media in high-frequency planar circuits and antennas due to its small size, low profile, and ease in formability, as well as the benefits offered by the availability of circuit design models and simulation tools. Although this line is one of the most popular, it is highly susceptible to radiation loss caused by discontinuities and substrate mode leakage [39]. Radiation loss can be eliminated by adding a miniaturized shield to the line when micromachined packages are included.

A packaged microstrip transmission line consists of an air-filled upper cavity and a Si-filled lower cavity (Fig. 3.2). The microstrip signal line and ground plane are printed on the front- and backside of the lower cavity wafer, respectively. The upper cavity is metallized and the two wafers are placed into direct metal contact by printing ground pads and etching vias in the lower cavity. For alignment purposes metal crosses are printed on the lower cavity and appropriately sized windows are etched in the upper cavity to align the two wafers with 20 ± 5 μm accuracy. Silver epoxy is placed on the lower cavity wafer for adhesion to the upper cavity.

The transmission line layout is classified either by topology and/or layout configuration. The two topologies (Fig. 3.3) considered are: (1) conventional microstrip, referred to as "open," or (2) micromachined shielded microstrip, referred to as "packaged." The description of transmission line cross-coupling can be distinguished by the layout configurations (Fig. 3.4), A and B, where (A) includes an adjacent straight through line and back-to-back (B-B) right-

angle bend referred to as "through-to-bend", and (B) includes two adjacent back-to-back right-angle bend geometries referred to as "bend-to-bend".

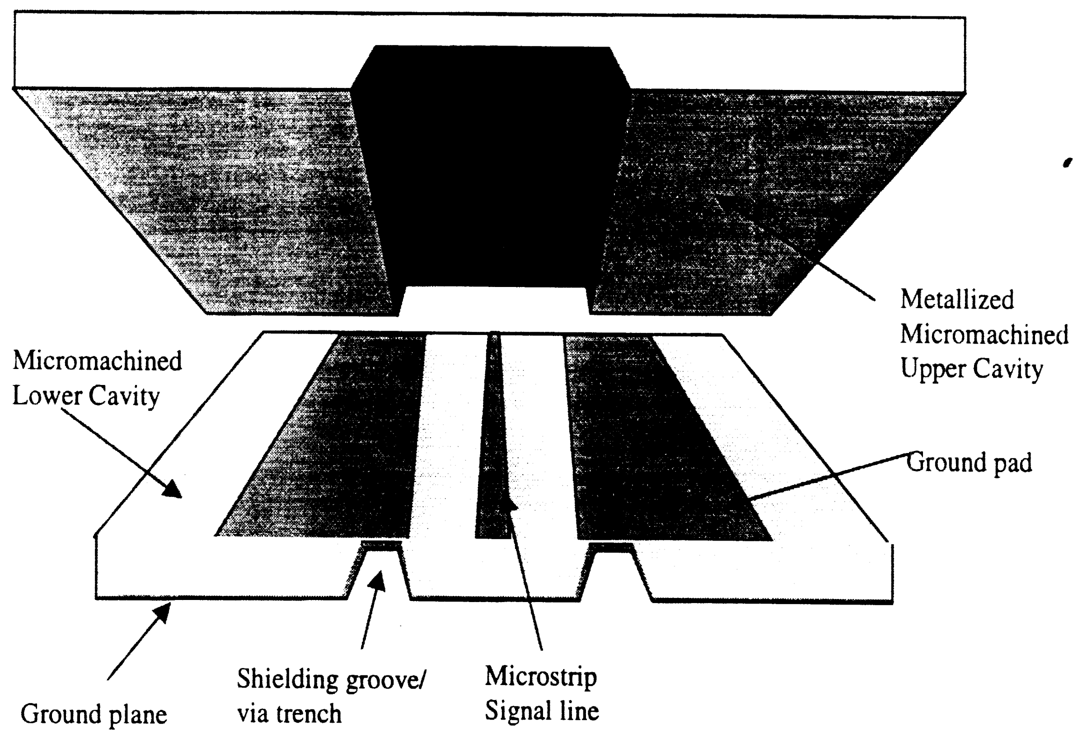


Fig. 3.2: Conceptual drawing of packaged microstrip line.

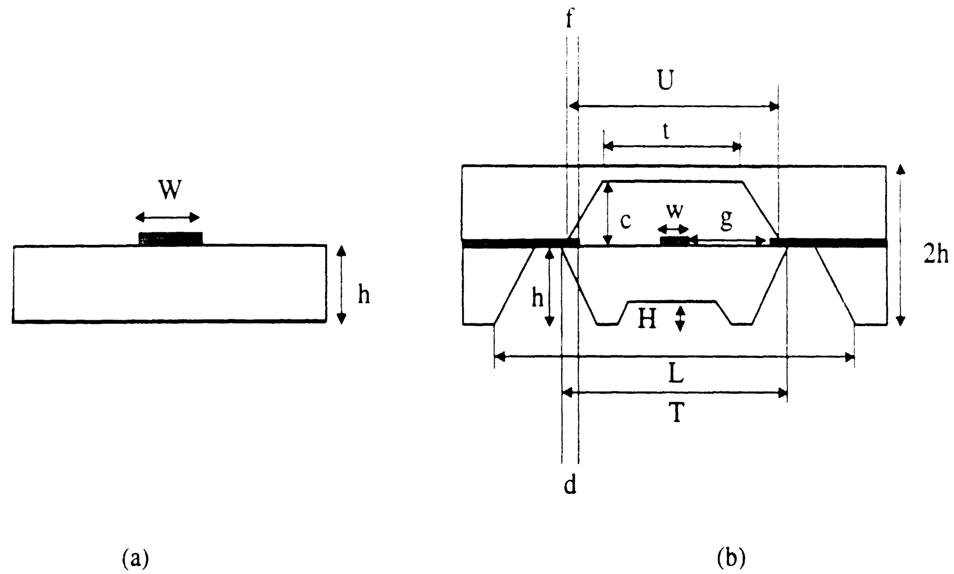


Fig. 3.3: Circuit topology: (a) Conventional microstrip on full thickness Si. (b) Packaged microstrip on reduced thickness wafer. Dimensions: h=500, W=420, w=210, t=690, L=2300, c=400, d=165, f=140, H=180, g=380, U=1250, T=1300 μm.

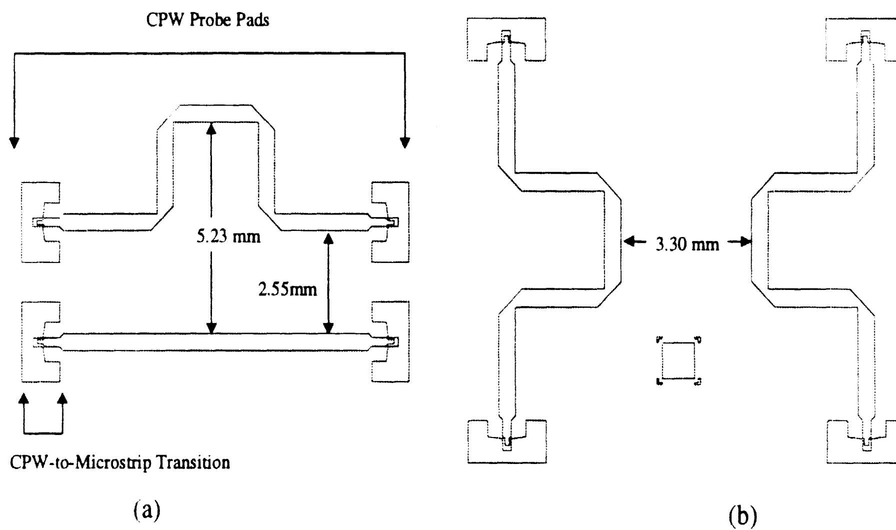


Fig. 3.4: Layout configurations. (a) Design Layout A: a through line and back-to-back right angle bend. (b) Design Layout B: two back-to-back right angle bends.

3.2.1 Transmission Lines

The dimensions of the conventional microstrip have been calculated from the following closed-form expression developed by Hammerstad and Jensen [32] for the characteristic impedance (Z_{0air}) as a function of substrate thickness and conductor width:

$$Z_{0air}(u) = \frac{\eta}{2\pi}\ln\left[\frac{f(u)}{u} + \sqrt{1 + \left(\frac{2}{u}\right)^2}\right] \tag{3.1}$$

where

$$f(u) = 6 + (2\pi - 6)\exp\left[-\left(\frac{30.666}{u}\right)^{0.7528}\right] \tag{3.2}$$

and $u = W/h$ *and* $\eta = 120\pi\ \Omega$.

The effective dielectric constant (ε_{re}) is expressed as:

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{10}{u}\right)^{-a(u)b(\varepsilon_r)} \tag{3.3}$$

where

$$a(u) = 1 + \frac{1}{49}\ln\left(\frac{u^4 + (u/52)^2}{u^4 + 0.432}\right) + \frac{1}{18.7}\ln\left[1 + \left(\frac{u}{18.1}\right)^3\right] \tag{3.4}$$

and,

$$b(\varepsilon_r) = 0.564\left(\frac{\varepsilon_r - 0.9}{\varepsilon_r + 3}\right)^{0.053} \tag{3.5}$$

The characteristic impedance for the line printed on a dielectric material, Z_{0m} is:

$$Z_{0m} = \frac{Z^a_{0air}}{\sqrt{\varepsilon_{re}}} \tag{3.6}$$

Given these expressions, the width and ε_{re} for a 50 Ω line on 500 μm-thick Si is found using HP Libra [30] to be, W=420 μm, ε_{re}=8.42 at 20 GHz.

The bottom wafer of the packaged microstrip cross-section looks similar to conductor-backed CPW because ground pads are printed to make contact between the lower ground plane and metallized upper shielding cavity wafer (Fig. 3.2). A code developed by Dib using the point matching method is used to determine the line geometry for the packaged circuit [31].

For a 500 μm thick Si wafer, the packaged line geometry would require a 420 μm microstrip conductor width and ground pads placed 1150 μm away. This cavity width for such a structure would be 3 mm wide and would reduce the high frequency performance of the line. By reducing the substrate thickness to 350 μm a narrower 50 Ω line and package can be fabricated. Using the point-matching method a 50 Ω CPW structure was realized with the predicted dimensions shown in Fig. 3.5. Closed form expressions in HP Libra for open conductor-backed CPW [34] and shielded microstrip confirm the predicted will produce a 50 Ω line. Table 3.1 lists the impedance and effective dielectric con-

stant values obtained with the new geometry. The CPWG and microstrip expressions produced a line with an impedances between 53 and 55 Ω and after adding a cover and sidewalls, the microstrip line impedance approached 50 Ω exactly.

To ease on-wafer measurements, CPW probe pads have been fabricated at the feed point and transitioned to the 50 Ω microstrip line geometry to minimize mismatch [35]. The vias and shielding grooves required for ground plane equalization in each structure are identified in Fig. 3.7 by the shaded regions.

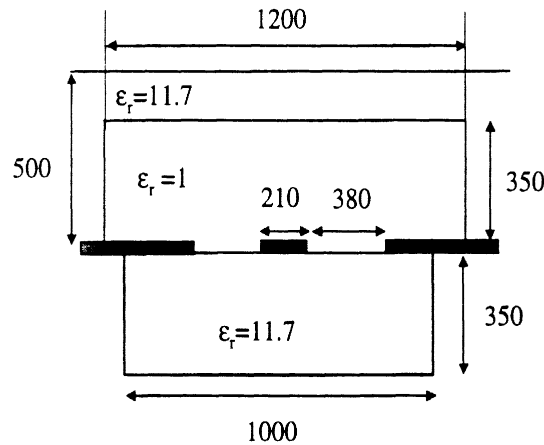


Fig. 3.5: Dimensions for 50 Ω CPW structure analyzed using the point-matching method.

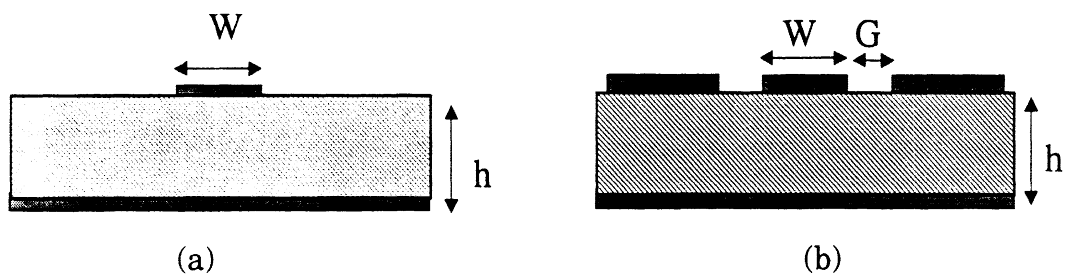


Fig. 3.6: Structures compared in LineCalc for initial packaged microstrip dimensions.(a) Conventional microstrip, and (b) conductor-backed CPW.

Line Type	Zo(Ω)	ε_{eff}	W(μm)	G(μm)	h(μm)	Package Width (mm)
Microstrip	50	8.42	420	n/a	500	n/a
CPWG	50	7.80	420	1150	500	3
Microstrip	57	7.86	210	n/a	350	n/a
CPWG	54.6	7.14	210	380	350	1.3
Microstrip w/ 350 μm cover and 380 μm wall	51	6.84	210	n/a	350	1.3
Microstrip	55	7.87	210	n/a	320	n/a
CPWG	53	7.234	210	380	320	1.3
Microstrip w/ 400 μm cover and 380 μm wall	49.6	6.93	210	n/a	320	1.3

Table 3.1: Dimensions for lines developed using LineCalc on Si at 20 GHz.

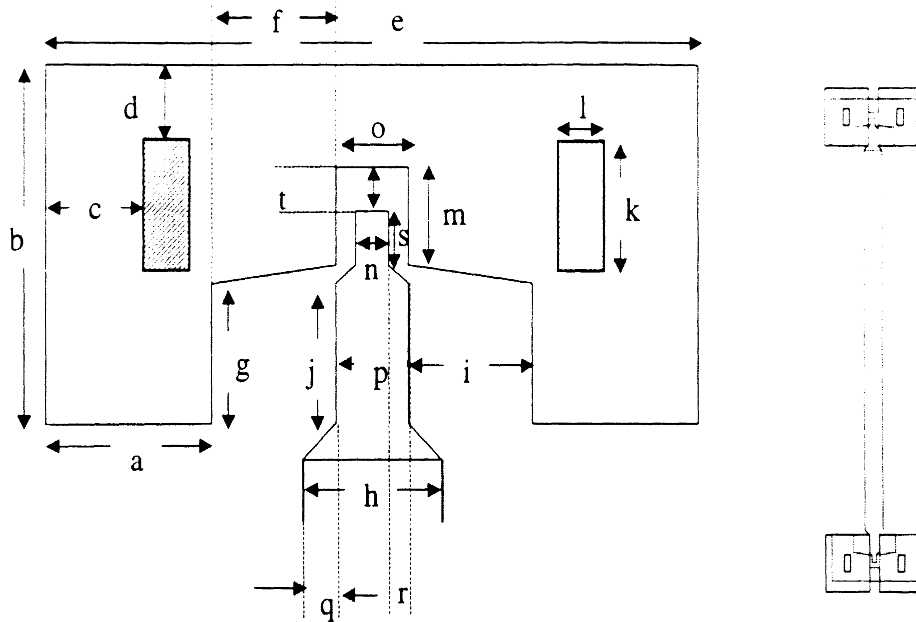


Fig. 3.7: Layout of CPW-to-microstrip transition for probe measurements: a=500, b=985, c=285, d=200, e=1970, f=378<8°, g=385, h=420, i=375, j=385, k=350, l=150, m=150, n=100, o=p=220, q=132<229°, r=78<320°, s=60, t=100 μm.

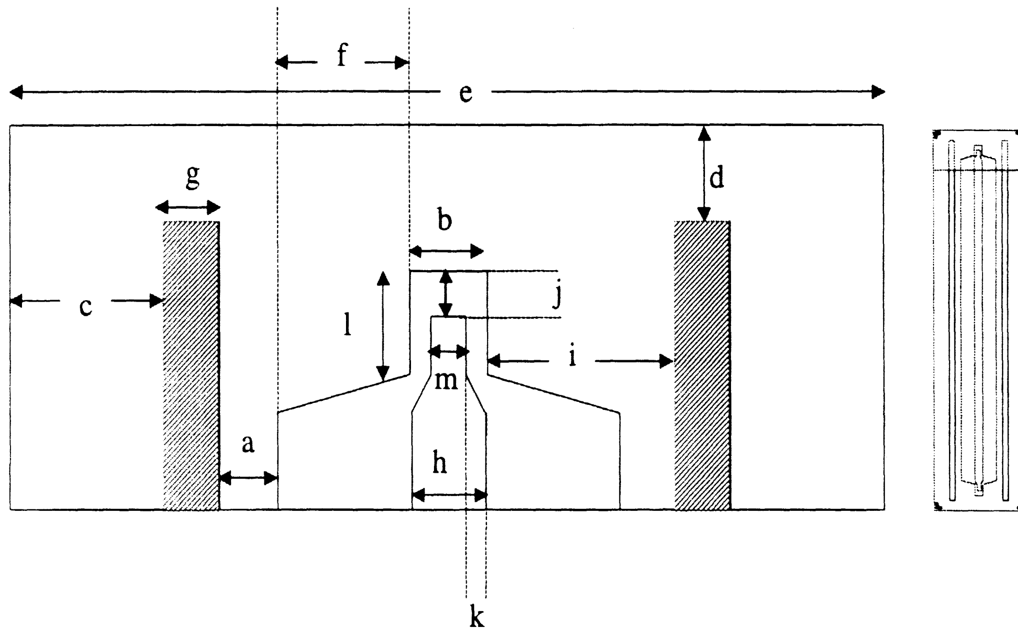


Fig. 3.8: Layout of CPW-to-packaged microstrip transition: a=165, b=220, c=435, d=250, e=2470, f=388<15°, g=150, h=210, i=540, j=120, k =114<299°, l=150 μm.

As shown by Wadell [36], the cutoff frequency, f_c, for microstrip lines is based on the following equation:

$$f_c = \frac{c}{4h \cdot \sqrt{\varepsilon_r - 1}} \tag{3.7}$$

which indicates for full thickness Si (h=500 μm, ε_r=11.7), f_c = 45.96 GHz, while for a thinner substrate (h=350 μm) f_c = 65.6 GHz.

3.2.2 Microstrip Patch Antenna

The microstrip patch antenna is popular for low profile antenna applications where size, weight, and cost are important parameters. Narrow bandwidth and poor efficiency limit the performance of the antenna but can be overcome by using thicker substrates and implementing an array of elements, respectively. Thinning the substrate increases the frequency of operation of the line, however, printing a patch antenna on a thinner substrate reduces the bandwidth of the antenna. [37]. Narrow bandwidth and poor efficiency limit the performance of the antenna but can be overcome by using thicker substrates and implementing an array of elements, respectively. The designer is forced to make a choice to either limit the performance of the feedline or the antenna.

Six microstrip antenna designs (four with quarter wavelength ($\lambda_d/4$) feeds and two with inset feeds) have been developed using PCAAD [38] as listed in Table 3.2. Photolithography limitations prevent the $\lambda_d/4$ fed patches from being used because the widths of those sections were between 10 and 20 μm while the feedline width was 420 μm. At that time, the layout masks were processed using rubylith and the resolution of the system using a one times exposure would not realize such a contrast in widths. Consequently, the inset fed

patch, with slot widths of 105 μm, was chosen for the design. To better predict the performance and make adjustments to the design of the patch with right-angle bend feedlines, a 3 GHz microwave model has been developed using stycast and copper tape. The measured input match on one straight and two bending patch antennas is shown in Fig. 3.9. Notice the additional low-frequency resonance due to the local reflections at the bends with no miters. Mitering the corner removes the parasitic resonance and shifts the resonant frequency from 3.12 GHz to 2.96 GHz [39]. The length in the straight feed patch has been increased by 200 μm to shift the resonance of the antenna to 2.95 GHz.

To increase design flexibility, the patch is fabricated on full thickness Si while the feedline is printed on an area of the wafer which has been thinned locally to 320 μm.

Design	W (μm)	L (μm)	Z_{in} (Ω)	f_d (GHz)	Inset (μm)	Z_{trans}, (Ω)/ ε_{eff}	W_{trans} (μm)	Type
W=1.5L	4000	1940	49.3+j5.5	20.03	715	n/a	n/a	Inset
*W=2L	2900	2000	49.4+j5.5	20.01	775	n/a	n/a	Inset
W=1.5L	3070	1990	391+j5.5	20.01	n/a	140/ 6.6	10	λ/4
W=2L	4100	1940	300+j5.5	19.99	n/a	122/ 6.7	20	λ/4
W=1.5L(oe)	3070	1593	391+j5.5	20.01	n/a	140/ 6.6	10	λ/4
W=2L(oe)	4100	1535	300+j5.5	19.99	n/a	122/ 6.7	20	λ/4

Table 3.2: Proposed microstrip patch antenna designs for Si (ε_r=11.7) on 500 μm thick substrate with a design frequency of 20 GHz. The design used for the project is shaded.

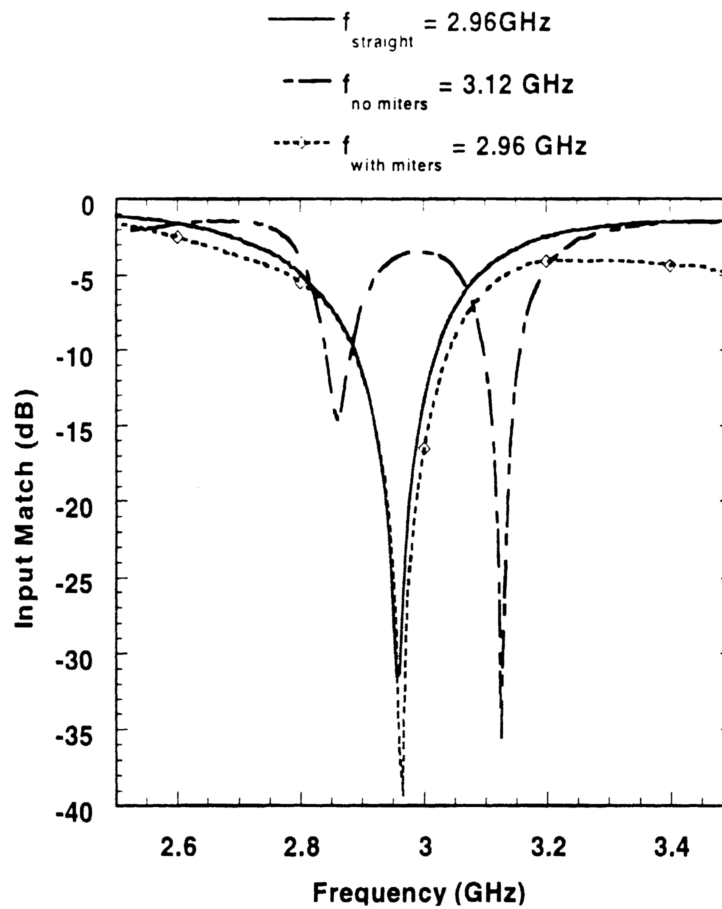


Fig. 3.9: The input match (S11) for a patch (W=2.9 mm and L=2 mm) with bending feedline (with and without mitering) compared to a patch with a straight feedline. The patch length was increased to incorporate the frequency shift caused by mitering. See Fig. 3.21 for feedline dimensions.

Material	ε_r	W (mm)	L (mm)	f_d (GHz)	Inset L (mm)	Inset W (mm)	Feed W (mm)	Thickness (mm)
Stycast	10	19.14	14.53	3.03	52.07	6.909	2.77	33
Silicon	11.7	0.29	0.22	20	7.89	0.105	0.42	0.5

Table 3.3: Microwave model and actual patch dimensions.

3.3 Fabrication

The approach for the packaged microstrip architecture incorporates the two-wafer fabrication technique described in [20]. Grounding pads are printed 380 μm away from the microstrip line for bonding and ground plane equalization of the package. The substrate beneath the lines is locally thinned to 320 μm while the remaining substrate thickness is 500 μm. The conventional microstrip line and circuit/lower cavity of the packaged line (Fig. 3.3) are fabricated on high-resistivity 500 μm-thick Si, while the upper cavity is developed on low-resistivity 500 μm-thick Si. The masking dielectrics on the circuit wafer are a tri-layer of $SiO_2/Si_3N_4/SiO_2$ with a total thickness of 1.5 μm, while the upper cavity substrate uses a thermal SiO_2 mask of 7500Å. In the fabrication process, standard lift-off, and electroplating techniques are used for Au circuit metal definition of 3 μm. The shielding cavities and vias are defined by removing the masking dielectrics with reactive ion etching (RIE) and wet etching techniques while they are etched using bulk micromachining processes with EDP water solution that has an etch rate of 1.2 μm per minute. Details of the process can be found in Appendix C.

3.3.1 Substrate Thinning

In order to realize a locally thinned region of Si on a full thickness wafer and create packages which conform to bending transmission lines, processing steps have been developed to: (1) reduce the wafer thickness under the conducting line, and (2) realize convex corners around bends in the upper and lower cavity regions.

One way to realize a thinned area is by etching the shielding grooves/ trenched vias completely in one step and then etching the thinned area in a

second step. Currently this is only possible if the shielding grooves are 100 μm-thick or less due to limitations of the photolithography techniques available. When using a wet etchant such as EDP, the sample must be thoroughly recleaned using a piranha etch[1] before it can be taken back into the lab. After vias are etched in a wafer, it is sometimes difficult to post-process and achieve a vacuum on the sample. It must be mounted on a carrier to complete the fabrication. These additional steps add time and money to the processing of the packaged microstrip. The method used in this work involves a two-step etching process using multiple masking dielectrics where the material in the deeper etched area (shielding grooves/trenched vias) is removed "enough" so that when the thinner etched area is exposed with a specific time constraint, both areas are etched for the desired thicknesses.

As mentioned in Chapter 2, pyramidal vias in Si are realized by defining an etch aperture width based on the substrate thickness and the size of the final width desired. The via is etched from the bottom of the wafer and bounded by the <111> crystal planes. The lower cavity wafer is shown in Fig. 3.12 where the aperture needed to realize a 100 μm (narrowest width) shielding groove is 850 μm. For the lower cavity three adjacent regions are defined on the bottom of the circuit wafer. The two outer areas create the shielding grooves and must be etched completely (H=500 μm) while the inner area defines the locally thinned substrate and h=180 μm will be removed.

With one mask the first two dielectric layers are removed on all three regions, and with a second mask the third dielectric is removed from the shielding groove regions only (Fig. 3.11). After 70% (5 hours, 360 μm) of the shielding groove Si has been etched, the remaining feedline dielectric (SiO_2) is

---

1. Piranha etch: 1: 1.2 H_2O_2: H_2SO_4

removed and the sample is etched for an additional 2 hours (180 μm) to realize the thinned area and complete the shielding grooves.

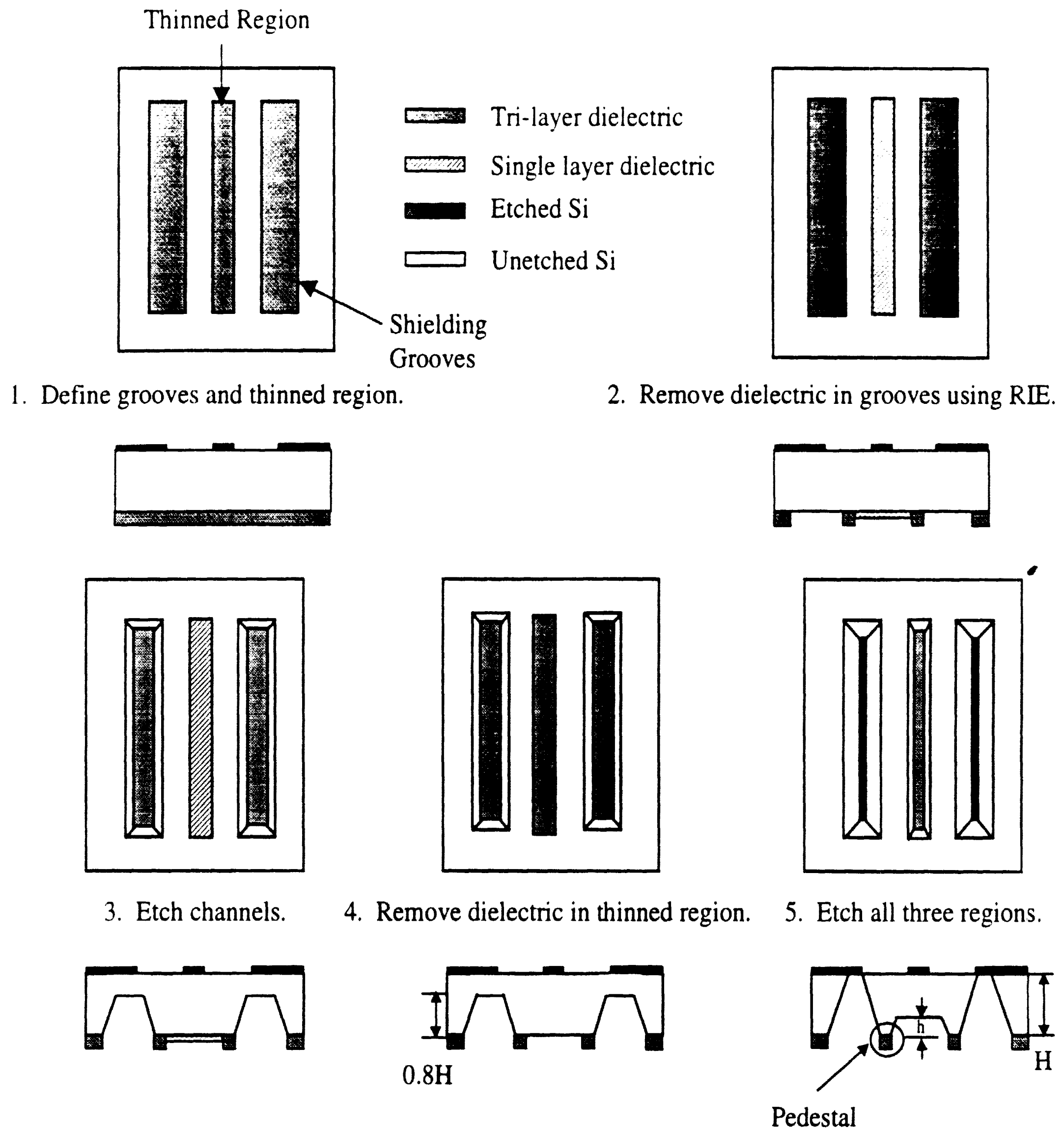


Fig. 3.10: Fabrication process for lower wafer development.

In the scanning electron microscope (SEM) photo of the fabricated lower package (shown in Fig. 3.11), the shielding grooves and thinned substrate are shown with 100 μm wide pedestals necessary to overcome the limitations of the wet anisotropic etchant and realize a flat, smooth etched surface. Fabrication tests have been performed with pedestal widths equal to 10, 20, 30, and

100 μm. If a pedestal is smaller than 100 μm, the Si surface directly beneath the microstrip conductor is very rough after etching.

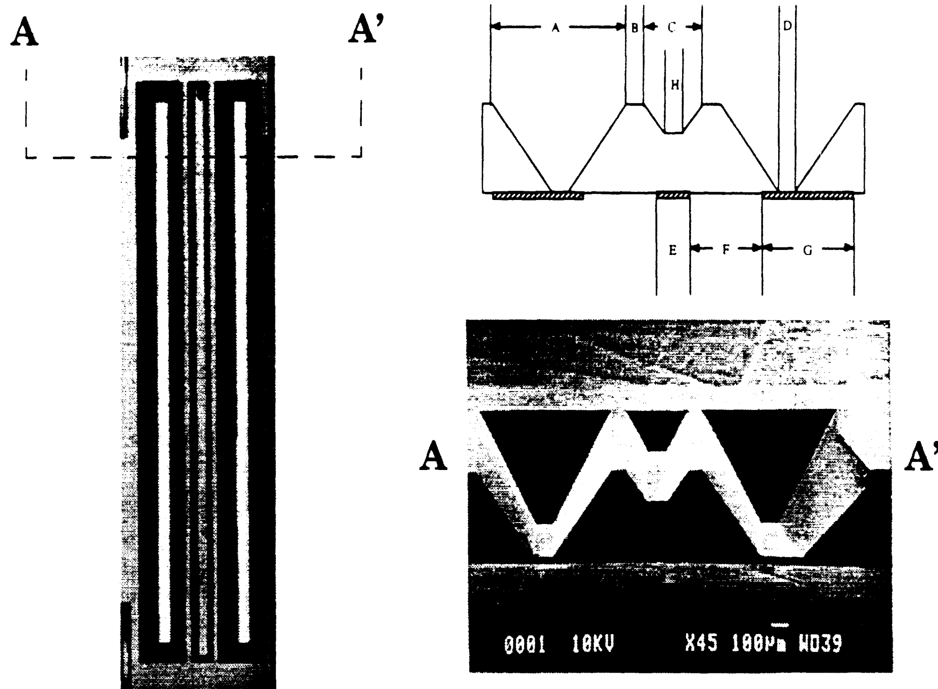


Fig. 3.11: Front view drawing of a microstrip line printed on an inverted lower package with dimensions, A=850, B=100, C=400, D=150, E=210, F=380, G=750, H=148 μm. The conductors are indicated with hashed lines. This is a SEM photo of the inverted lower package developed during the two-step etch procedure.

3.3.2 Convex Corner Compensation

The fabrication of locally thinned straight packages has been achieved using the aforementioned procedure, however, several problems arise when developing structures with bends (Fig. 3.13). The etch rate along the (100) crystal plane versus the (111) plane allows for the realization of grooves/vias in (100) Si. Higher order crystal planes (found in convex corners) have higher etch rates and become overetched very quickly. Fig. 3.12 shows a photograph of Layout B "bend-to-bend" for the packaged microstrip with a top view of the lower cavity (circuit metal) and bottom views of the upper and lower cavities.

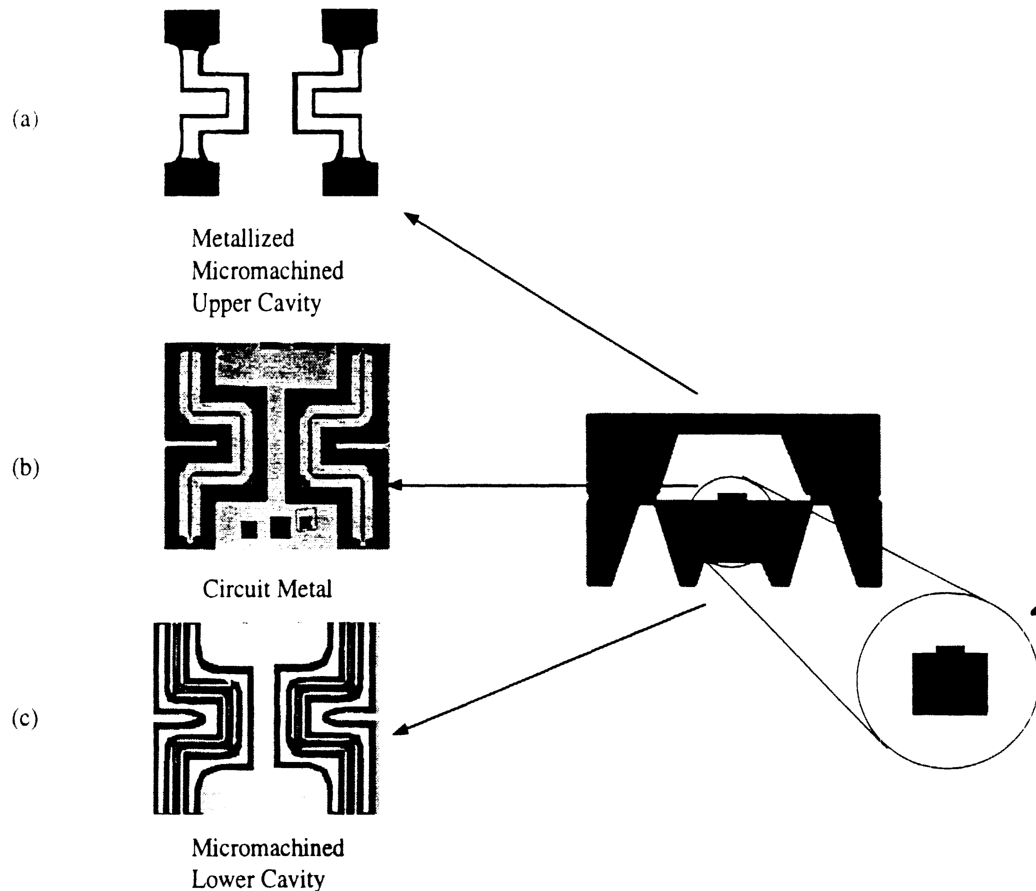


Fig. 3.12: Micromachined packaged back-to-back right-angle bends. (a) The upper cavity package with probe windows for on-wafer testing. (b) Circuit layout of microstrip line which is printed on the frontside of (c) the lower cavity, which shows the reduced thickness regions in the center with the lower package channels seen as white regions.

Notice that certain corners in the lower cavity wafer suffer from rounding known as undercutting. Figure 3.13 illustrates the convex and concave corners found in a right angle bend. Wu [42] defines a concave corner as one bounded by the slowest etching planes (111) while a convex corner is one bounded by the fastest etching planes. The planes have been defined by Bean as {211} [40], by Abu-Zeid as {331} [41], and Wu as {212} [42]. An example of

the higher order plane {212} being undercut is shown in Fig. 3.14 for a mesa as proposed by Lee [43].

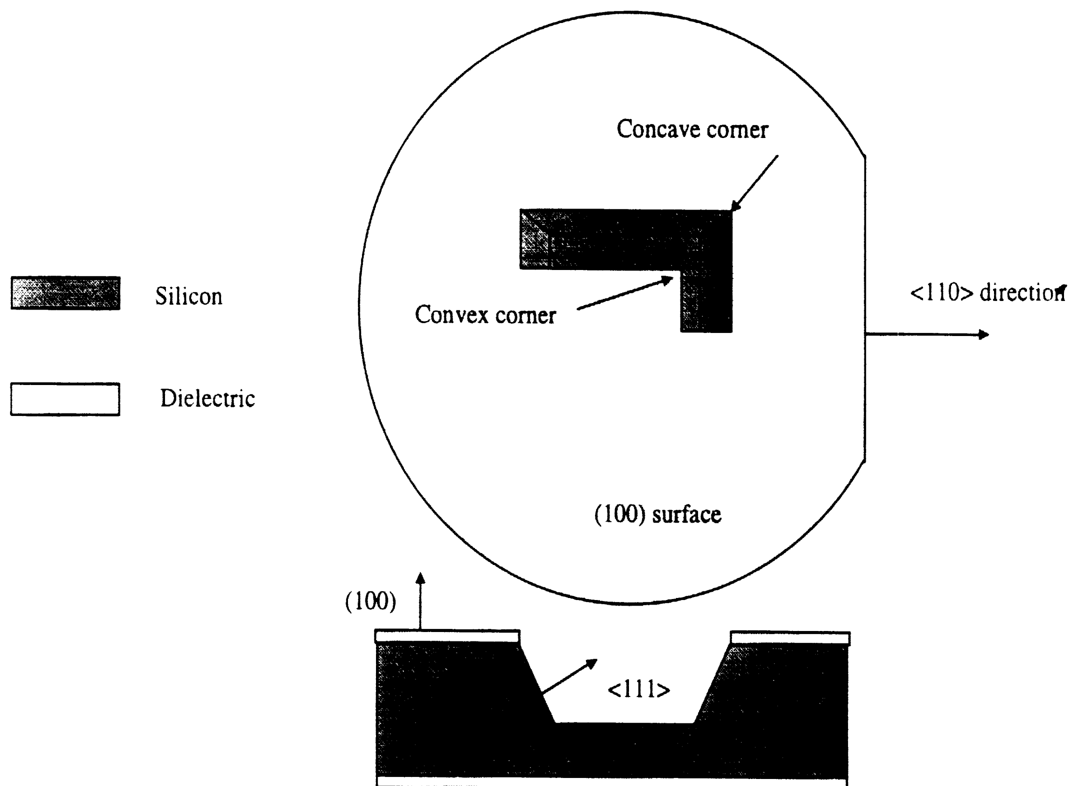


Fig. 3.13: Illustration of convex and concave corners in a right-angle bend.

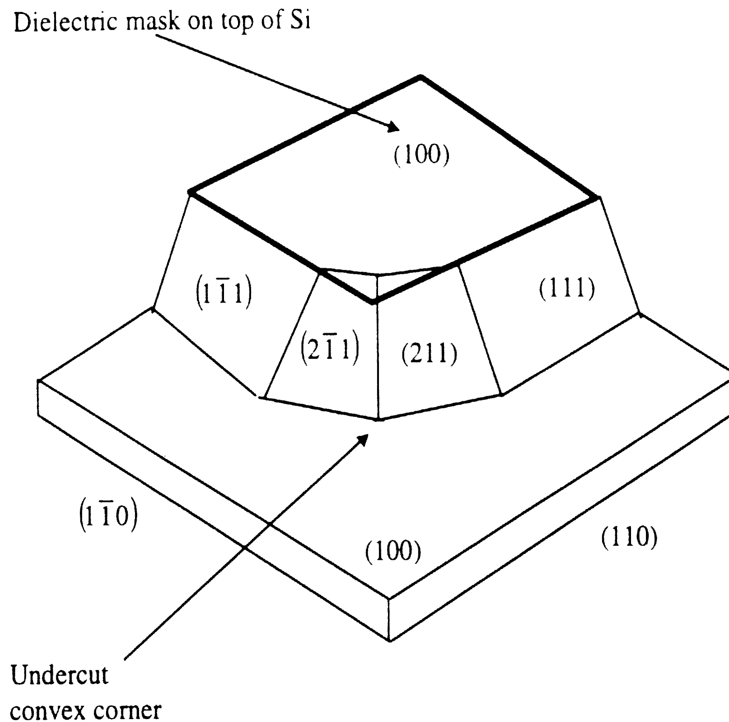


Fig. 3.14: Underetching of a convex corner is caused by the fastest etching plane {211} according to Lee [43].

One method to reduce the excessive undercut of convex corners is to add chemical additives to the etchant [44]. While this technique reduces the undercut rate, it also reduces the anisotropy ratio between crystal planes and may ultimately create problems in the structure development. A more common method is to incorporate compensations in the mask to protect the convex corner [42]. Although sophisticated algorithms and techniques have been developed to predict the best compensation geometry for a given problem ([45], [46], [47], [48], [49], [50]), simple square compensations have been used and are centered at the endpoint of each expected convex corner found in the original mask (Fig. 3.15) [41]. The compensations protect the corners by providing the etchant with excess material to attack until the desired depth has been achieved.

The design rules in the literature indicate that compensation squares of approximately 1.2 times the etched depth are sufficient to produce the quality of corners seen in Fig. 3.12a for the upper cavity package. For cases where the sample must be etched for a longer period of time, the simple compensation techniques break down as shown in Fig. 3.16b. In the initial fabrication, the upper cavity compensation has been designed as described above, however, the lower cavity wafer suffers from noticeable undercutting in the shielding grooves region and beneath the microstrip line. Since high-frequency planar circuits are highly geometry dependent, a structure as seen in Fig. 3.16b produces non-uniform field distribution under the microstrip feedline and contributes to higher-order moding as well as higher circuit loss [51]. Therefore, in the lower package additional geometrical and etching considerations are required to optimize the etch process.

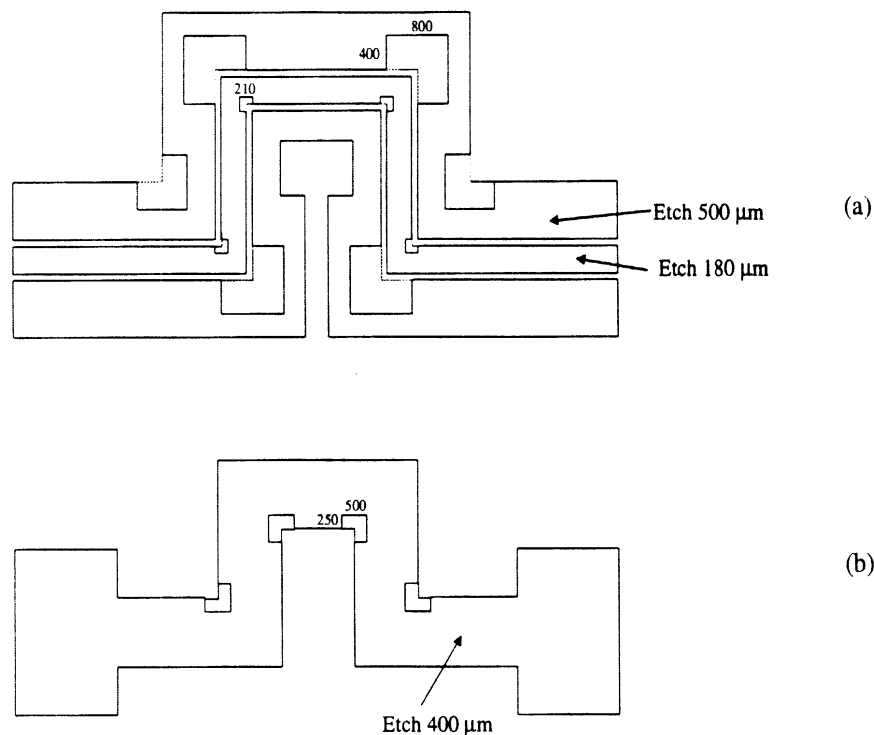


Fig. 3.15: Layout masks showing compensations at convex corners. (a) Lower cavity wafer. (b) Upper cavity wafer. The large squares form the package channels and the small squares form the reduced thickness regions.

Separate compensation corners are required to develop the shielding grooves/trenched vias (500 μm) and locally thinned regions (180 μm) with, square sizes of 800 μm an 210 μm, respectively. Table 3.4 lists the estimated etching schedule for the lower cavity wafer. In order to preserve the compensation in the shielding grooves area, the total etch time must be considered. In general it takes 7 hours to etch an entire 500 μm wafer from one side.

Process Step	Process Time (hour)
Begin etching (Step 1)	0
Monitor sample	1-4
Remove samples, rinse, measure etched depth in grooves, remove dielectric	5.5
Begin etching thinned region (Step 2)	0
Monitor sample	6.5
Remove samples, measure etched depth in local thinned area	7.5

Table 3.4: Etching schedule for lower cavity.

Fig. 3.17 shows the effect etching has on the mask compensations for a right angle bend in the lower package. The CAD mask and photographs of the etched sample after 5 hours and 7.5 hours are shown. After the first 5 hours of etching one compensation square has been completely etched while some material still remains on the other two.

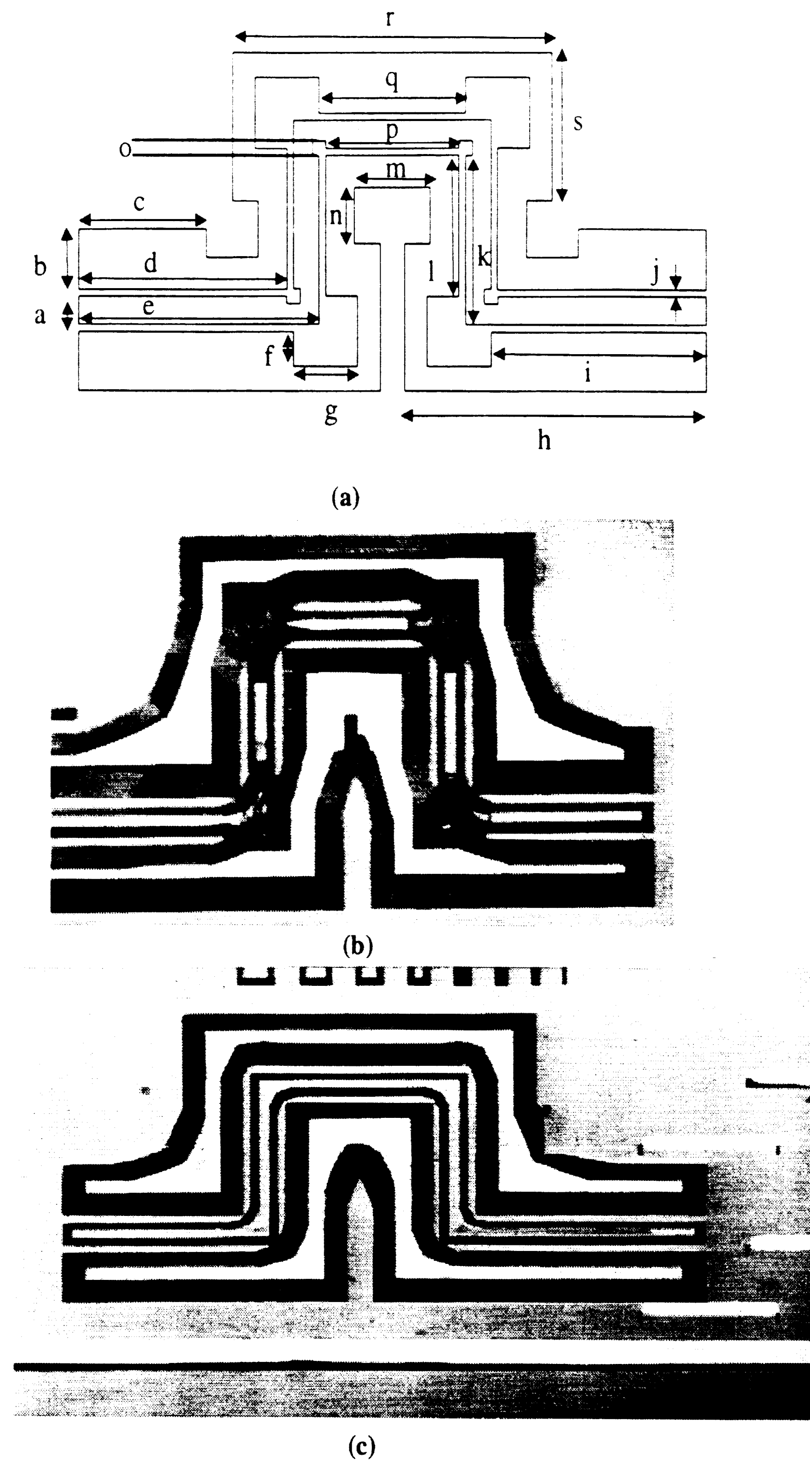


Fig. 3.16: Corner compensation marks: (a) CAD drawing of the mask layout, showing the corner compensation required for the formation of the lower cavity package (a=400,b=850,c=1286.5,d=2536.5,e=2351.5,f=400,g=800,h=4687,i=3437,j=100,k=2393.5,l=2098.5m =1178,n=800,o=210,p=2068,q=2478,r=4978,s=2098.5) μm. (b) Good compensation from the etch. (c) Poor compensation due to the extended amount of time for the etch.

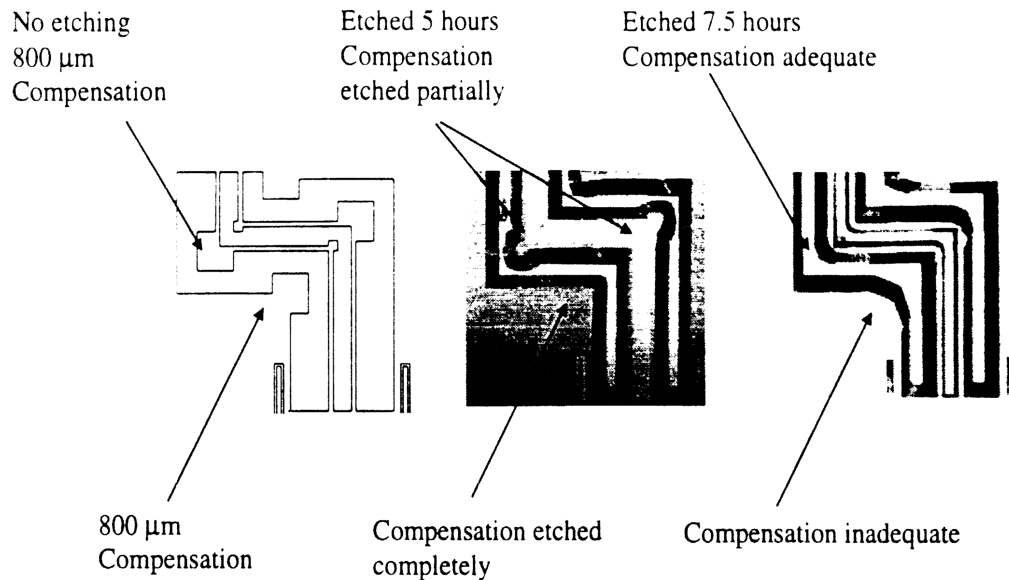


Fig. 3.17: Effect of etching on square compensation for a right angle bend.

Identification and design of the compensation corners must account for the depth that the convex corner will be etched (as in the case of the upper cavity wafer and reduced thickness region area in lower wafer), but also the total etch time to preserve corners if a longer etch is required. A quantitative expression for a simple (one-step etch) square compensation, c, is

$$c = 1.2 \cdot d \tag{3.8}$$

and the complex compensation square, C, for a two-step etch is defined by:

$$C = 1.2 \cdot d + 26 \cdot h \tag{3.9}$$

where d is the etched depth, h is the total etch time in hours and 26 is the linear approximation of the time dependence factor in units of microns per hour.

3.4 Measurements

To RF characterize the micromachined circuits accurately, the following test equipment has been used: (1) two coplanar waveguide based GGB PicoProbes (150 μm pitch), (2) an Alessi High Frequency Probe Station, and (3) an HP 8510C Network Analyzer. All circuits were measured after performing a Short-Open-Load-Through (SOLT) calibration method in which the test probes were de-embedded from the circuit. The measured performance of the open and packaged circuits will be shown in the following sections describing the electrical characteristics of each line. Coupling mechanisms associated with different circuit layouts are evaluated and compared to a "reference" minimum noise value for the packaged system.

3.4.1 Transmission Line Characteristics

Hewlett Packard's high frequency structure simulator (HFSS) has been used to simulate the performance of the microstrip lines [33]. The S-parameters for a 7 mm-long line are shown in Fig. 3.18 and the measured response for a 9.4 mm-long line (including transitions) is shown in Fig. 3.19. The measured return loss is 10 dB worse due to the mismatch caused by the CPW- to-microstrip transition and system calibration.

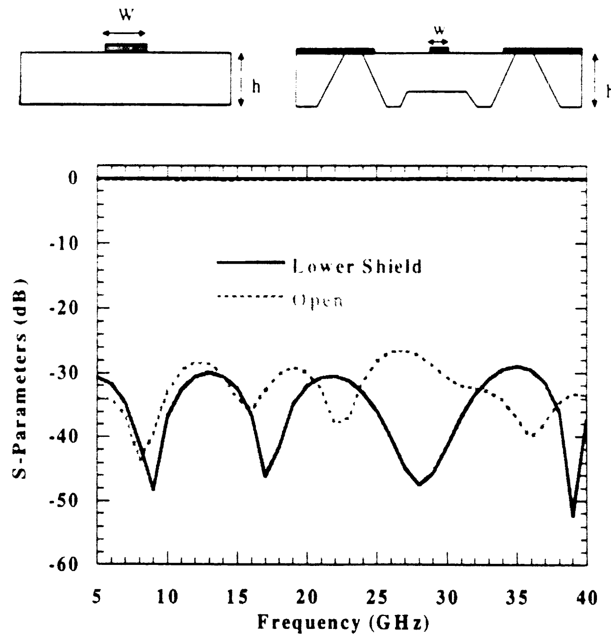


Fig. 3.18: HFSS simulation of 7 mm microstrip line in open and lower shielded configuration.

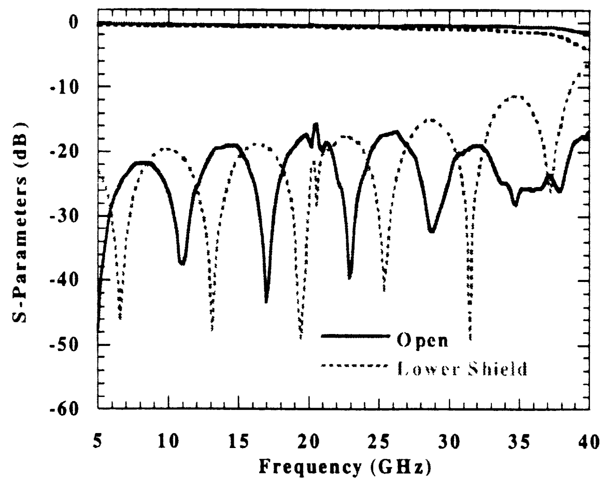


Fig. 3.19: Measurement of 8 mm microstrip line in open and lower shield configuration.

The effective dielectric constant (ε_{re}) predicted by Libra and the code based on the point matching technique for the conventional and packaged microstrip structures is 8.42 and 6.3, respectively. Fig. 3.20 compares the ε_{re} for a through line in the open and packaged configuration based on a Libra simula-

tion and the measured data. Notice that when the line becomes packaged, the slope of ε_{re} reduces indicating less frequency dependence. The effect of the lower shielding and complete shielding are indicated by the reduction in ε_{re}.

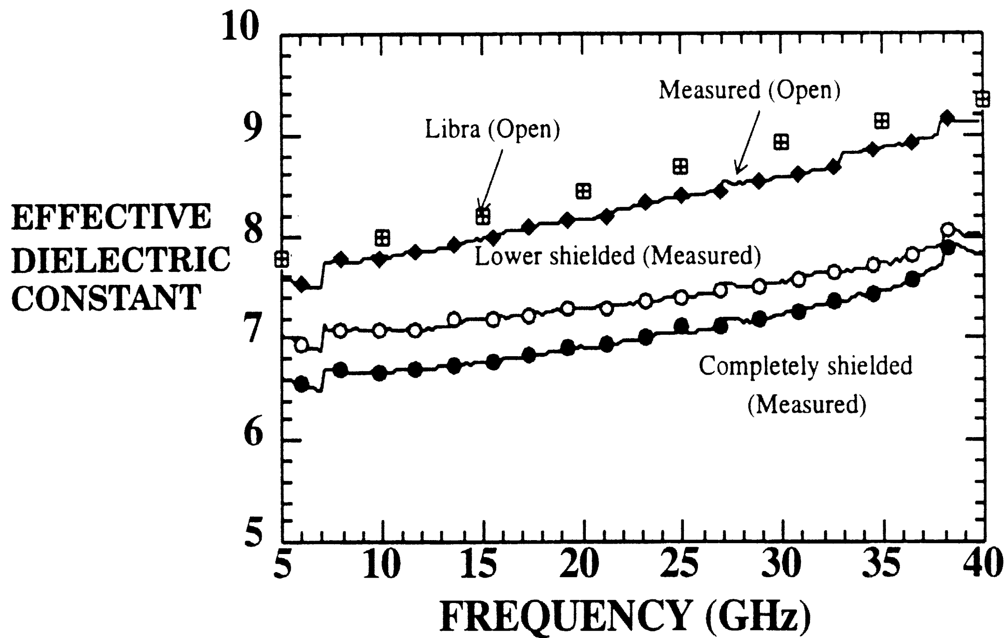


Fig. 3.20: Microstrip effective dielectric constant.

The electrical response of the interconnects for Layout A and B in the conventional and packaged microstrip configurations will be presented herein. Measurements for the insertion loss are shown illustrating the transmission properties in the various circuits.

The performance of a right-angle bend (L=13.392 mm) and a straight delay line (L=13.392 mm) for a conventional microstrip design is shown in Fig. 3.21. The insertion loss is similar for both lines at lower frequencies, however, above 15 GHz the corners in the bending line radiate and excite substrate modes. The bending line oscillates above 30 GHz with total loss ($1-|S_{11}|^2-|S_{12}|^2$) as high as 65%.

Figure 3.22 shows that the total loss of a packaged bend and delay line of equal length is very similar. Although the packaged bend exhibits higher losses due to the metallization of upper cavity, the parasitic radiation associated with the open bend is eliminated by the shielding cavities. A comparison between the open and packaged bend is shown in Fig. 3.23.

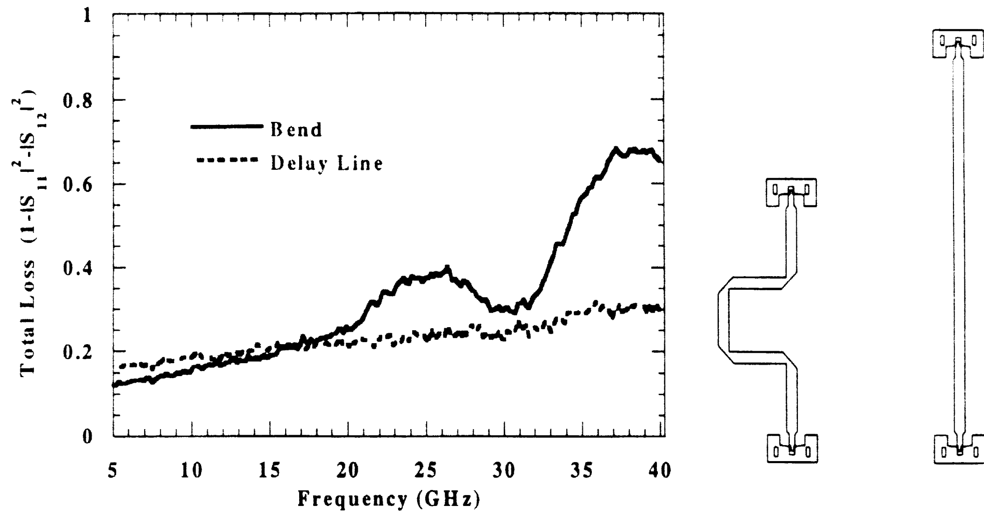


Fig. 3.21: Electrical response of open microstrip circuits for a delay line and right angle bend (L=13.392 mm).

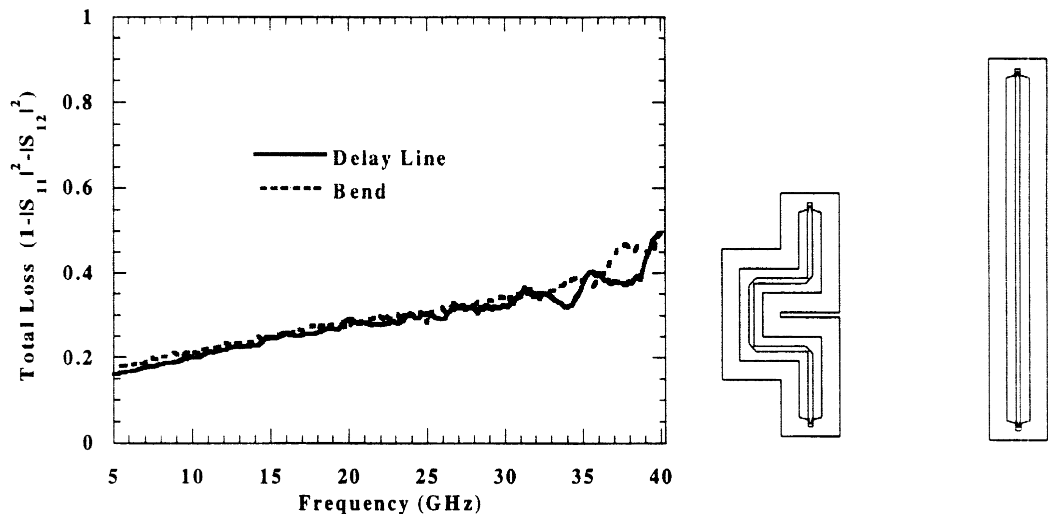
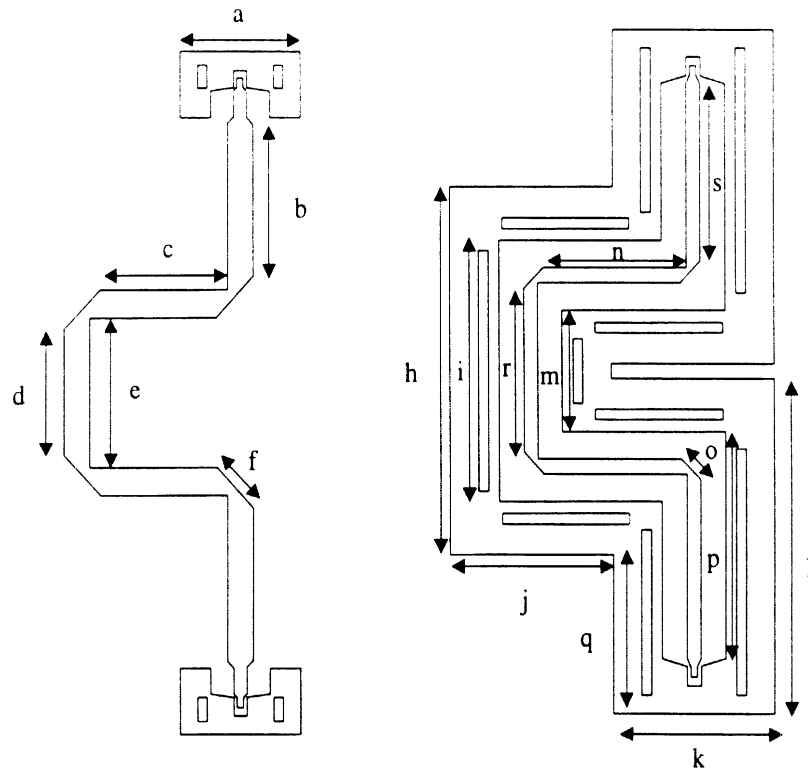


Fig. 3.22: Electrical response of a packaged back-to-back right angle bend and microstrip delay line of similar length (L=13.392 mm).



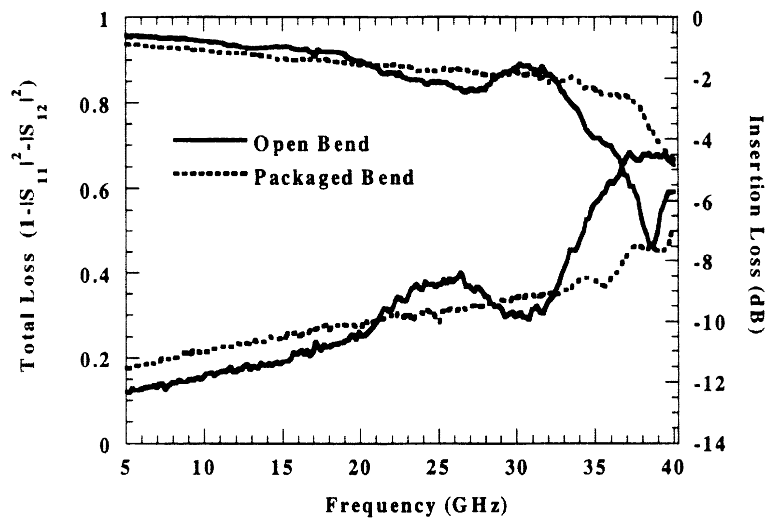


Fig. 3.23: (a) Dimensions of open and packaged back-to-back right angle bends: (a=1970, b=2468.5, c=2078.5, d=1898.5, e=2258.5, f=848<31.5, h=5148, I=3648, j=2498.5, k= 2470, l=4464, m=1709, n=2198.5, o=424<315, p=3163.5, q=2194, r=2288, w=2483.5) mm. (b) Electrical response of an open and packaged back-to-back right angle bend (L=13.392 mm). The total loss of each line is compared to a delay line of equal physical length (13.392 mm).

3.4.2 Noise Floor/Coupling

Two types of noise measurements are defined: (1) "non-contact": probe-to-probe in air and (2) "contact": packaged system noise floor. The non-contact noise is measured when the probes are elevated 20 mm above the package surface and separated by 8.3 mm in the x-y plane (Fig. 3.24). This distance is equal to the separation found in the bend-to-bend layout (Fig. 3.4). The contact noise measurement is an average of different measurements obtained when the transmission line is excited at one port and the propagating signal is measured at different locations on top of the circuit package environment, as indicated in Fig. 3.24 [29]. Figure 3.25 compares the two noise measurements and shows good agreement between them.

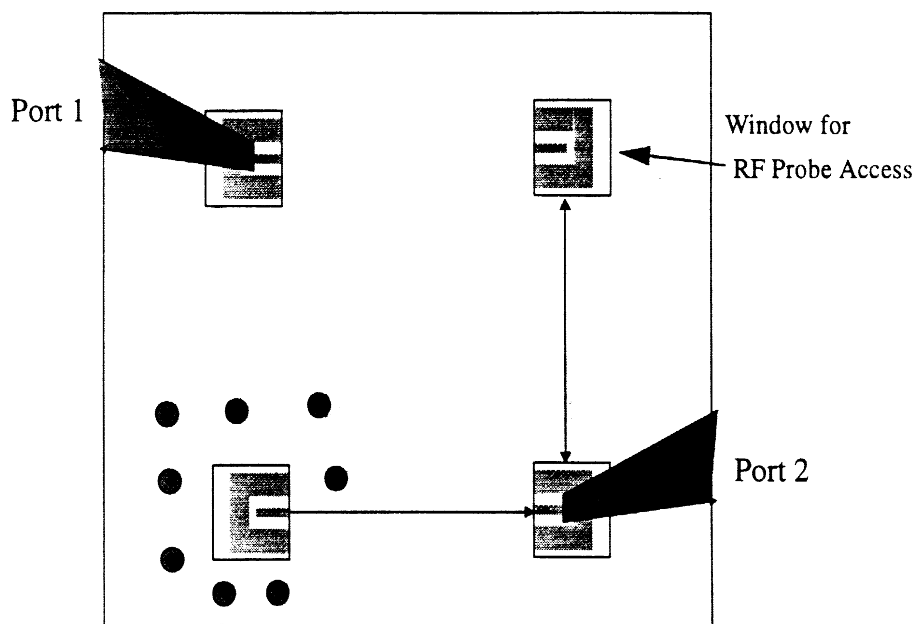


Fig. 3.24: Layout for contact noise characterization. The boxes represent probe windows in Design Layout B (Figure 3.4) for the bend-to-bend arrangement. Probing points in the contact noise measurement are indicated by starts at Port 1 for the input signal onto the conducting line at Port 2.

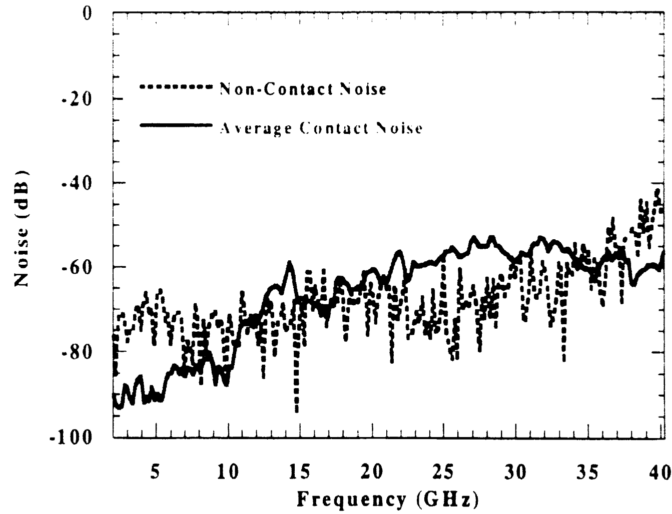


Fig. 3.25: Noise data from contact and non-contact measurements.

3.4.3 Cross Coupling and Isolation

This section focuses on the measured cross coupling in the two layouts presented earlier (see Figure 3.4). Figure 3.26 shows a comparison of cross coupling between Layout A and B for conventional microstrip. Coupling is as high as -20 dB for the through-to-bend arrangement (Layout A) while it is even higher (-10 dB) for the bend-to-bend arrangement (Layout B). These results indicate that the amount of coupling seen in open structures is highly dependent upon the layout configuration. Figure 3.27 shows that the addition of the integrated lower cavity reduces the coupling by approximately 20 dB for the bend-to-bend arrangement. Inclusion of the upper cavity achieves an additional 10 dB reduction. These results demonstrate that advanced monolithic packaging can reduce coupling between elements to the noise level.

The contact noise and cross coupling response of the completely packaged bend-to-bend arrangement are compared in Fig. 3.28 and show very good

agreement up to 33 GHz. The increased coupling in the packaged bends is associated with leakage that occurs at the input and output ports of the packaged line, which are left open (Fig. 3.25).

A HFSS simulation of two parallel microstrip lines in an open lower shielded and completely shielded topologies (Fig. 3.3) are shown in Fig. 3.29. The edge-to-edge spacing for the packaged microstrip is 2.82 mm and 2.58 mm for the conventional line. The coupling levels differ by approximately 20 dB across the band. The measured coupling levels increase with frequency and the simulated levels decrease. This is due to the complexity of the measured layout (bend-to-bend arrangement) in comparison to parallel lines in the simulation. Fewer frequency points are used in the packaged line simulations and are not as smooth as the conventional results.

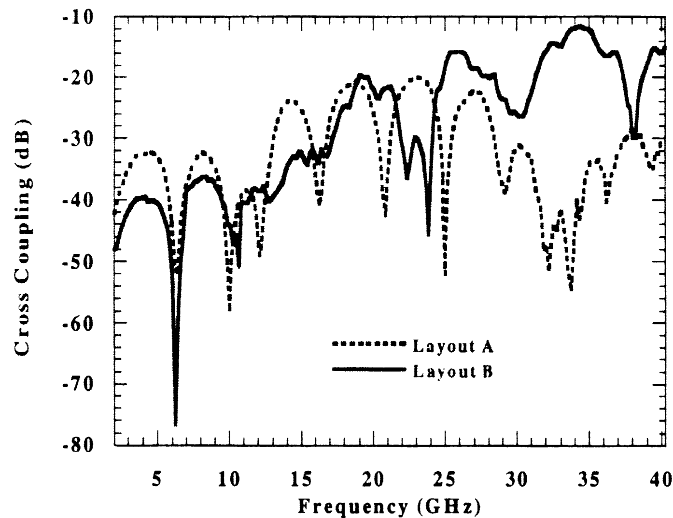


Fig. 3.26: Comparison of cross-coupling effects in open microstrip structures for design Layout A and B (See Fig. 3.3).

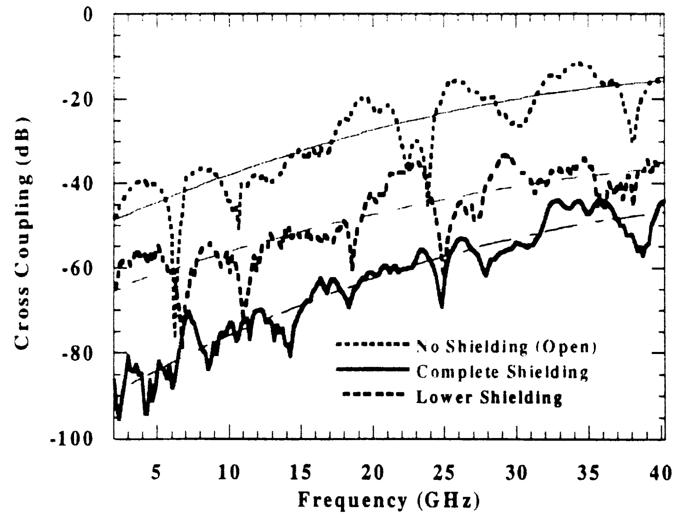


Fig. 3.27: Cross -coupling effects in Design Layout B for two back-to-back right angle bends in open, lower half packaged, and full packaged designs.(See Fig. 3.3)

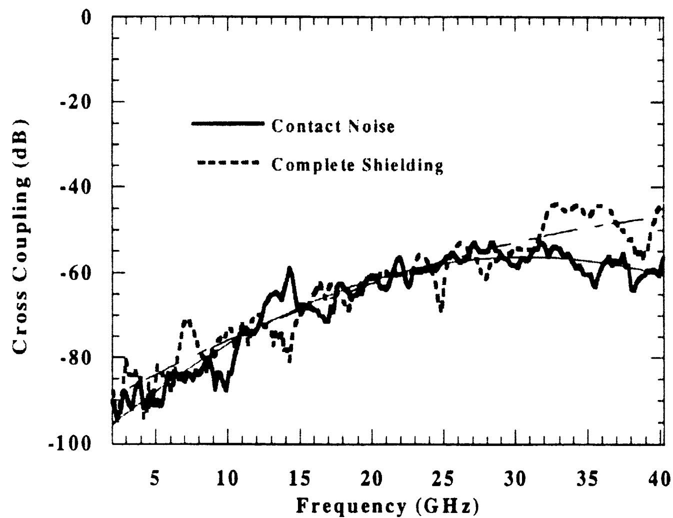


Fig. 3.28: Comparison of coupling between two packaged back-to-back right angle bends and the contact noise measurement of the packaged system.

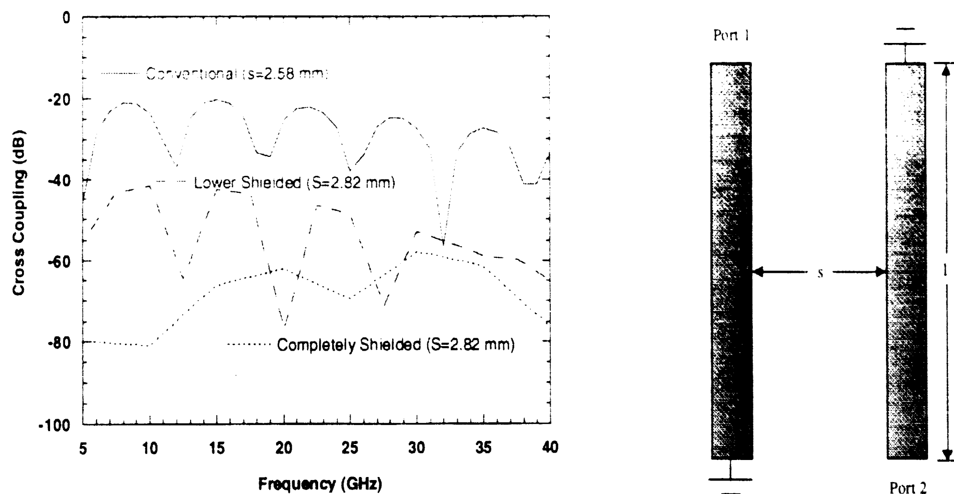


Fig. 3.29: HFSS simulation of cross coupling between two straight microstrip lines in the conventional and packaged configurations where l=7 mm.

3.4.4 Antenna Feed Performance

To illustrate the packaging approach for an antenna element, a shielding cavity has been developed around the feedline of a microstrip patch antenna (Fig. 3.30). The antenna window has dimensions of 7.1 mm x 6.9 mm, including a distance separation of 2 mm (Fig. 3.31). By separating the antenna edges from the package by 4 times the substrate height, the interactions between the feedline shielding cavity wafer and antenna element are reduced [52].

The packaged feedline is printed on a thinner substrate (320 μm) to ensure a dominant microstrip mode and the patch is printed on a thicker substrate (500 μm) to increase the frequency bandwidth [37]. As observed from the data in Fig. 3.31, the 3 dB bandwidth of the packaged antenna is approximately

12.8% while the bandwidth of the open antenna is approximately 6.4%, an increase of 200%.

$$3dBBandwidth = \frac{Freq_{upper} - Freq_{lower}}{Freq_{center}} \tag{3.10}$$

Since the two antennas only differ in feeding structures, the antenna with a better input match will achieve higher antenna efficiency as shown in Equation 3.11 where the total antenna efficiency, e_t, is:

$$e_t = e_{cd}(1 - |\Gamma|^2) \tag{3.11}$$

where e_{cd} is the antenna radiation efficiency due to conduction and dielectric losses and Γ accounts for reflections between the feedline and antenna. The magnitude of the reflection coefficients of the patch input are 0.058 and 0.0186 for the conventional and packaged feedlines, respectively. A higher antenna efficiency for the packaged feedline can be attributed to the fact that the propagation characteristics (β) and characteristic impedance (Z_0) are less sensitive to frequency due to the improved TEM propagation on the line as shown in previous transmission line measurements. In the case of high density antenna arrays where feedline cross coupling limits performance, this packaging scheme can improve feedline isolation and propagation.

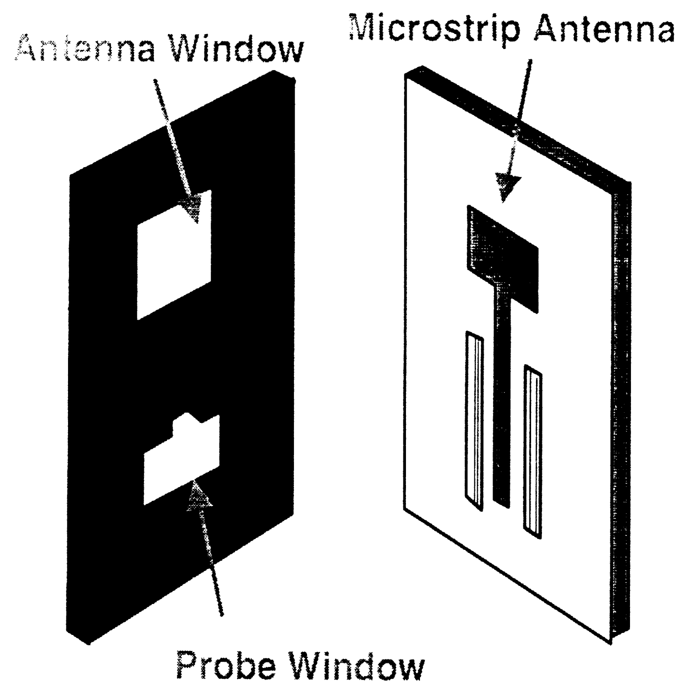


Fig. 3.30: Conceptual drawing of packaged antenna configuration.

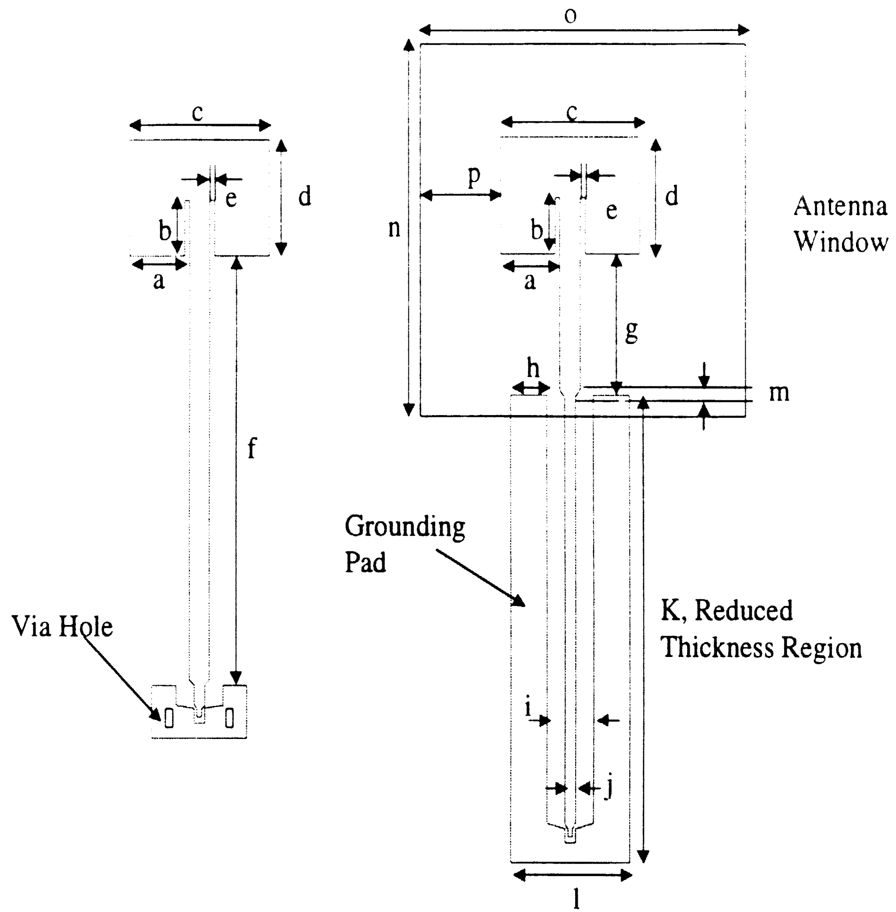


Fig. 3.31: Layout of antennas: (a=1140, b=789, c=2900, d=2200, e=105, f=8135.5, g=2673, h=750, I=970, j=210, K=8835.5, l=2470, m=183<55, n=7123.5, o=6900, p=2000) μm.

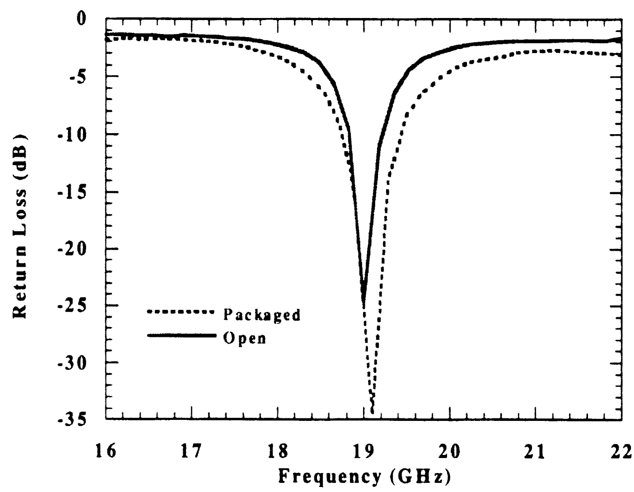


Fig. 3.32: Return loss for a patch antenna with open and packaged microstrip feedlines.

3.5 Summary

The work presented in this chapter has demonstrated the substantial benefits of advanced monolithic packaging concepts in high density planar circuit and antenna design. Specifically, cross-talk and parasitic radiation in circuit components and antenna feed networks can be eliminated through selectively packaging sections of planar circuits. The packaging technology is based on integrating Si micromachining techniques with standard IC processing techniques. Circuit performance for components generally demonstrating high radiation is improved substantially with the inclusion of a package environment. This packaging scheme also reduces interactions between neighboring elements in dense layouts and creates an environment similar to the package system noise. The findings from the circuit interconnect problem make the inclusion of such packages into antenna array applications beneficial by isolating the functions of the feeding networks and antenna element. In addition to the aforementioned benefit of improved performance, monolithic micromachined packages for high-frequency circuit designs are lightweight and small, as well as low in volume and cost.

Novel micromachining techniques have been used to develop low-cost package solutions for microstrip lines; to further study cross-talk behavior in open and packaged geometries; to characterize the noise associated with monolithic packages; and to demonstrate the integration of a package with planar elements common in array applications.

CHAPTER IV

DESIGN OF A SI-BASED CHIP CARRIER FOR DISCRETE COMPONENTS

4.1 Introduction

This chapter presents an approach to discrete component package design that uses processes compatible with IC fabrication techniques to develop high-precision, miniaturized, high-frequency housings which do not limit device performance. With low cost Si as the packaging material and anisotropic etching as the technique for machining the packages, this design can be easily scaled to millimeter-wave frequencies, an option not available for conventional packaging materials. The excellent mechanical and thermal properties of Si lead to a very competitive packaging technology which offers improvements in high-frequency performance and reductions in long-range production costs.

In the early eighties, Petersen extensively reported on the properties of Si and emphasized that its mechanical strength is comparable to the strength of many metals [21]. Although Si is a brittle material, wafer chips on the order of 6 mm x 6 mm are quite rugged under normal handling conditions. The excellent properties of Si along with the numerous micromachining techniques available have allowed engineers to develop high-performance miniature elec-

tromechanical devices [53], and membrane-type transmission lines which can operate at frequencies as high as 1000 GHz [54]. GigaBit Logic developed a Si-based package for GaAs circuits and compared the performance to a multi-layer ceramic one [55]. The Si-chip carrier provided shielding for signal lines, lower cross-talk, and lower thermal resistance when compared to the ceramic package. While chip capacitors were mounted on the ceramic substrate to reduce power supply disturbs, they were monolithically integrated in the Si substrate. This capability gives an engineer more design options and reduces the amount of potential loss associated with hybrid circuits.

Si technology has been implemented in a high density, 3-dimensional card-on-board package for a Josephson technology experiment [56]. The substrates for the thin film-circuits, circuit boards, and structural supports were all made from Si and eliminated thermal mismatch problems. Table 4.1 lists the thermal conductivity values for common III-V materials compared to Si [57]. The thermal properties of Si are very good compared to those of ceramic materials and allow for excellent heat transfer between the semiconductor and package, thus making Si an excellent candidate for high-frequency MMICs.

Material	Thermal conductivity (W/(m °K))
GaAs	80
InP	65
Ge	68
Si	135

Table 4.1: Thermal conductivity for MMIC substrates [57].

In the following sections, the design, fabrication, assembly, and testing of a Si package that can provide on-wafer or discrete shielding to ICs is described. The package performance is evaluated and compared to a Ka-Band ceramic package for a MMIC phase shifter chip.

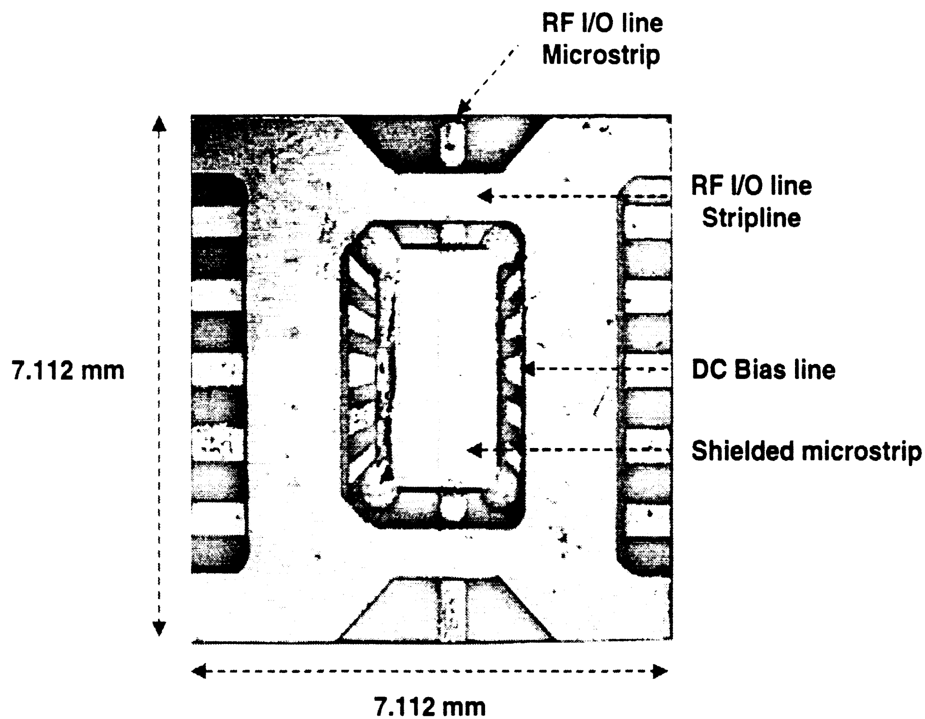


Fig. 4.1: Actual photograph of K/Ka-Band ceramic package for phase shifter chip.

4.2 Chip Carrier Design

The Si-based single-chip carrier layout (Fig. 4.1) originated from a design fabricated by Hughes Aircraft Company for NASA Lewis Research Center using high temperature co-fired ceramic (HTCC) techniques with 92% alumina [58]. The package is designed around a K/Ka-Band MMIC phase shifter chip with ten bias lines perpendicular to the RF input/output line. The width and length of the package is 7.112 mm and 7.112 mm, respectively, and the

multi-layer assembly includes a seal frame, RF substrate, base, and top metal lid which create a microstrip-stripline-shielded microstrip interconnect for the MMIC device (Fig. 4.2).

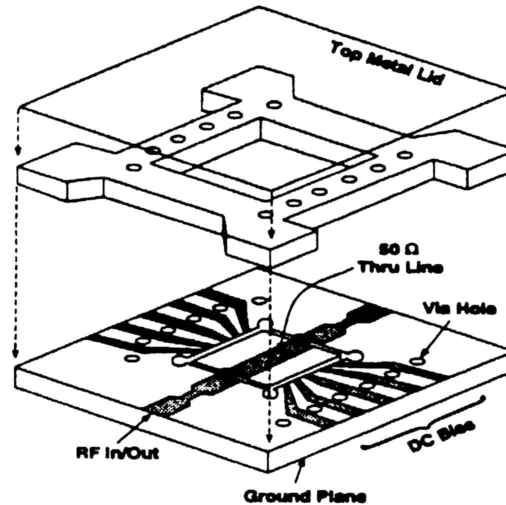


Fig. 4.2: Schematic drawing of K/Ka-Band package for phase shifter chip. Courtesy of Yook [58].

The characteristic impedance of the transmission lines is 50 Ω and the dimensions of the lines were obtained using LineCalc (Fig. 4.3). The impedance for the microstrip is based on the Hammerstad and Jensen formulas (see Chapter 3) while the impedance for the stripline is based on Wheeler's approximate formula [59]. For the design frequency of 29 GHz the cross-section dimensions and lengths of the interconnect at the input are shown in Table 4.2.

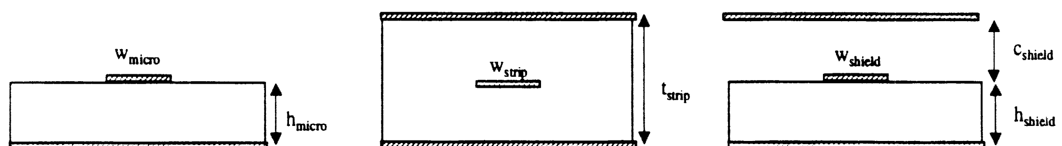


Fig. 4.3: Transmission lines used in RF input/output interconnects: microstrip, stripline, and shielded microstrip.

$$Z_0 = \frac{\eta_0}{4.0\pi\sqrt{\varepsilon_r}} \ln\left\{1.0 + \frac{4.0(b-t)}{\pi w'}\left[\frac{8.0(b-t)}{\pi w'} + \sqrt{\left(\frac{8.0(b-t)}{\pi w'}\right)^2 + 6.27}\right]\right\} \quad (4.0)$$

where

$$w' = w + \frac{\Delta w}{t} t \quad (4.1)$$

and

$$\frac{\Delta w}{t} = \frac{1.0}{\pi}\left\{1.0 - 0.5\ln\left[\left(\frac{1.0}{2.0(b-t)/(t+1.0)}\right)^2 + \left(\frac{1.0/(4\pi)}{w/t+1.1}\right)^m\right]\right\} \quad (4.2)$$

$$m = \frac{6.0}{3.0 + \frac{2.0t}{(b-t)}} \quad (4.3)$$

Transmission Line	$\varepsilon_r/\varepsilon_{ff}$	Material Thickness (μm)	Conductor width (μm)	$Length_{phy}/Length_{ele}$ (μm/°)	Z_o (Ω)
Microstrip	11.7/8.49	350	320	469/48	48.93
Shielded Micros-trip	11.7/7.33	350	250	305/29	50.06
Balanced Strip-line	11.7	700	100	559/67	49.12

Table 4.2: Dimensions for interconnects used in Si package, obtained from Linecalc where f_d=29GHz.

To compare electrical performance between the different materials (Si and alumina), the micromachined package design is kept the same with the ceramic one. The thickness of the substrate and seal frame layers for the alumina package is 381 μm while the Si wafer thicknesses are 350 ±25 μm. Table 4.3 lists the redesign parameters for the Si chip carrier.

PARAMETER	92% ALUMINA	MICROMACHINED Si
Permittivity	9.5	11.7
Wafer Thickness (μm)	381	350
Metal Thickness (μm)	4	3
Vias (μm)	203.2 diameter (circular)	150/side (square)
Process	HTCC	Si micromachining
Bias Line width (μm)	457	350
Wirebonds (number)	4	3

Table 4.3: Redesign parameters for discrete package.

The Si-based package is comprised of six layers (4 dielectric and 2 metal): the carrier (1), the substrate (2), the seal frame (3), and the top cover (4) as shown in Fig. 4.4 and Fig. 4.5. The carrier wafer has a metal layer on the top side (Metal 1, Fig. 4.4) which provides the ground for the package. The substrate wafer supports the input and output RF lines, the DC bias lines, and the lower part of the shielding vias. The seal frame includes the upper part of the shielding vias and two probe windows which allow access to the input and output RF lines for on-wafer measurements. In addition, the seal frame supports a metal layer which provides the upper ground plane for electromagnetic (E-M) shielding (Metal 2, Fig. 4.4).

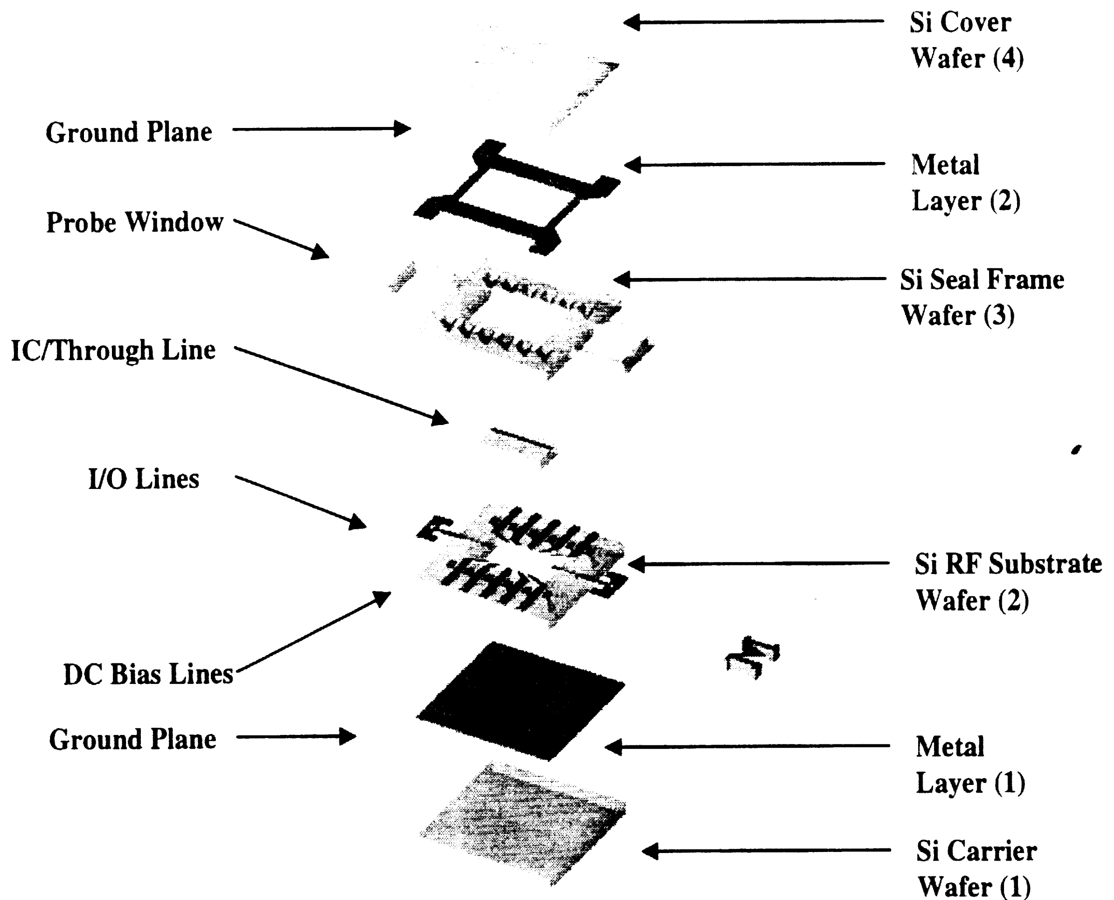


Fig. 4.4: 3-Dimensional rendering of Si package.

The package layout has been developed using AUTOCAD and Fig. 4.5 shows the process layers superimposed. To provide mechanical support and connect the two metal layers, a set of 12 vias are processed in the substrate and seal frame wafers on the Si package (Fig. 4.5 and Fig. 4.6).

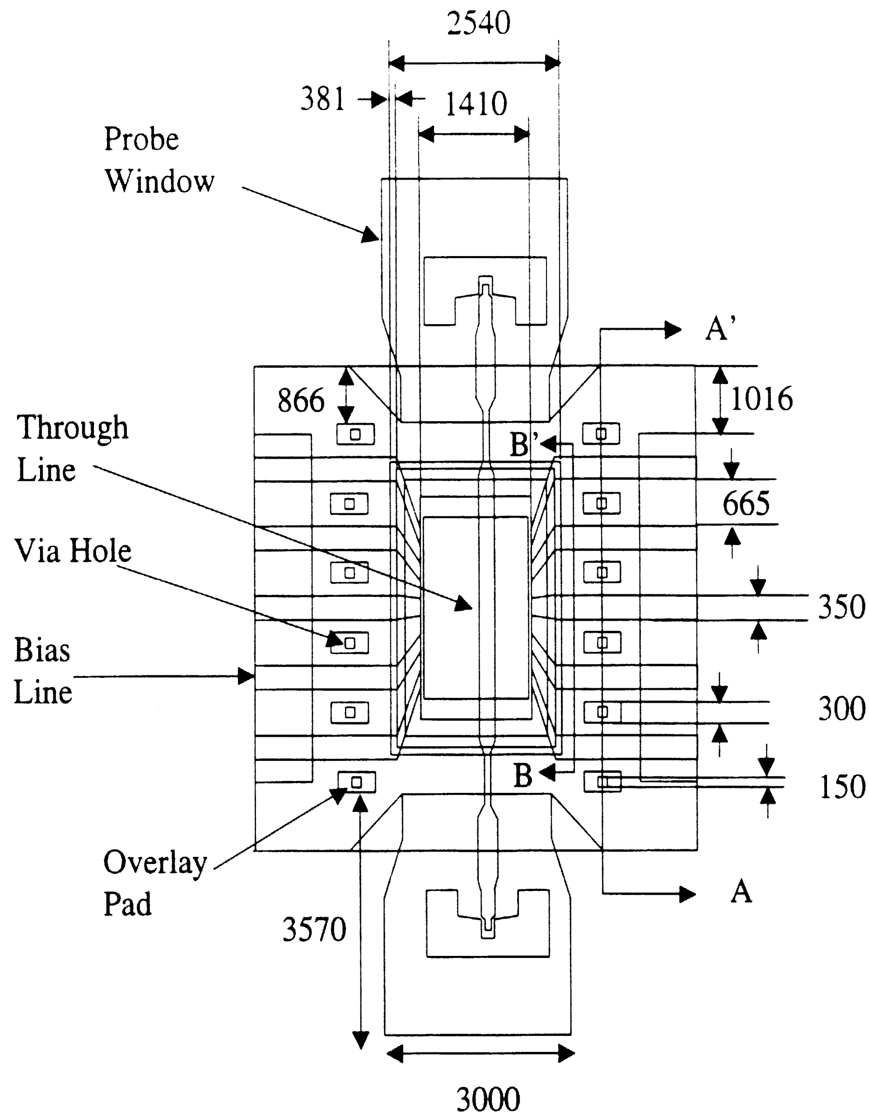


Fig. 4.5: Process layers superimposed.

In normal HTCC processing, the interconnecting vias are stamped and then filled with a conductive paste by screen printing. In the Si-based approach, selective etching along the <111> crystal plane in a <100> Si wafer is used to create vias with a pyramidal shape, as shown in Fig. 4.6. The wide square aperture of each via is equal to 640 x 640 μm^2, which results in a narrow aperture of 150 x 150 μm^2 on the other side of the wafer after etching. Metal over-

lay pads are electroplated over the narrow via aperture to provide electrical contact between the conducting layers [61].

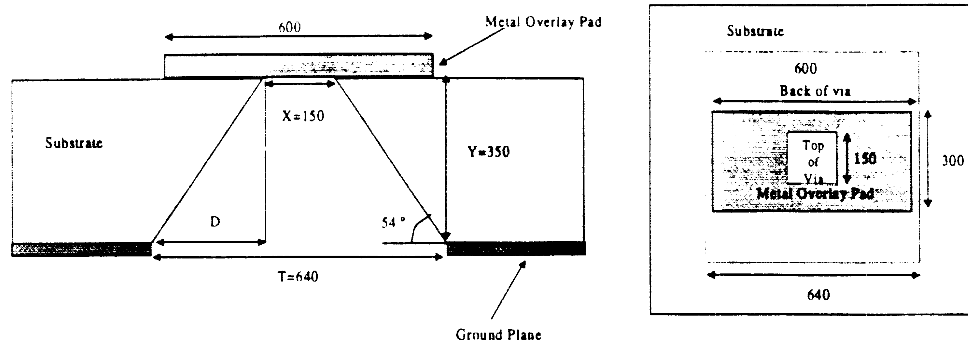


Fig. 4.6: Pyramidal via micromachined with anisotropic etchant and Cr/Au overlay pad.

The wide via aperture width, T, is related to the narrow width, X, and depth of the via, Y, by the following equation,

$$T = X + 2 \cdot D \tag{4.4}$$

and,

$$D = 0.7 \cdot Y \tag{4.5}$$

The original HTCC package design is asymmetric to accommodate the layout of the MMIC phase shifter, with the I/O feedlines displaced 178 μm from the center axis of the cavity while the two outer vias on the left side of the package are displaced 105 μm from the others, as shown in Fig. 4.7. In addition to the original design, two more variations have been fabricated and measured to determine the sensitivity of the electrical performance to layout asymmetries. In design #2, I/O lines have been placed along the center axis of the package to study the effects of feedline symmetry while the vias have been

left at their original location as in the ceramic package. In design #3, both I/O lines and shielding vias have been symmetrically placed with respect to the center axis.

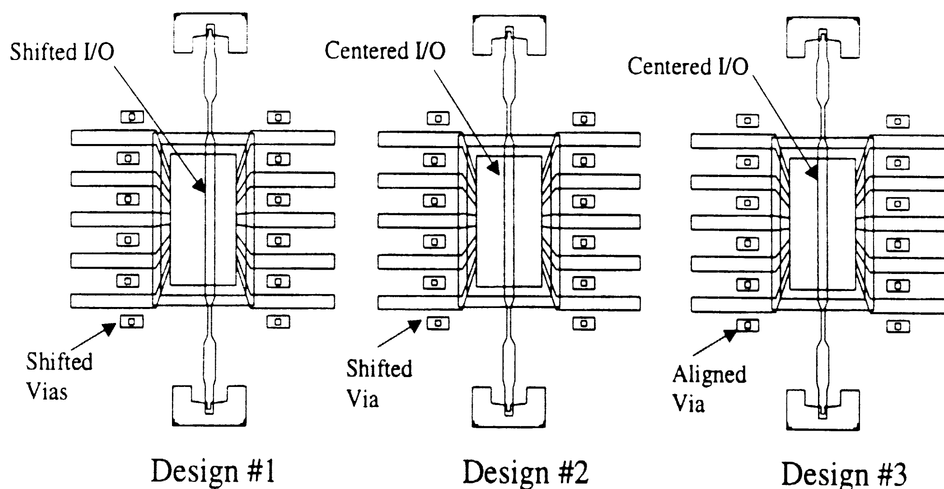


Fig. 4.7: Designs for Si package: Design #1-Shifted vias and I/O line, Design #2-Shifted vias and centered I/O line, Design #3-Aligned vias and centered I/O line.

4.3 Fabrication and Assembly

A 500-μm, high-resistivity, <100>, Si wafer with 7500Å of thermal SiO_2 is used to fabricate the package. The process flow consisted of wafer preparation, circuit metallization, and via formation (etching), and metallization as detailed in Appendix D. The wafers were assembled using Epotek silver epoxy as detailed in the following steps. Figures 4.8 and 4.9 and show the cross-sections of the package assembly.

Step	Process
1. Attach RF wafer to carrier.	Fill the vias in the RF wafer with silver epoxy. Place the RF wafer on the metallized carrier. Cure epoxy for 15 minutes at 120°C.
2. Attach microstrip through line.	Place epoxy on backside of through line. Place it within the IC aperture on RF wafer onto the carrier wafer. Align interconnect and through line and cure epoxy for 15 minutes at 120°C.
3. Wirebond	Attach Au bondwires between the interconnect and through line.
4. Align and attach seal frame wafer.	Place epoxy on the RF wafer metal overlay pads. Align seal frame and RF wafers. Cure epoxy for 15 minutes at 120°C.
5. Attach top cover	Fill vias in the seal frame wafer and add the top cover to the assembly. Cure epoxy for 15 minutes at 120°C.

Table 4.4: Assembly of micromachined package.

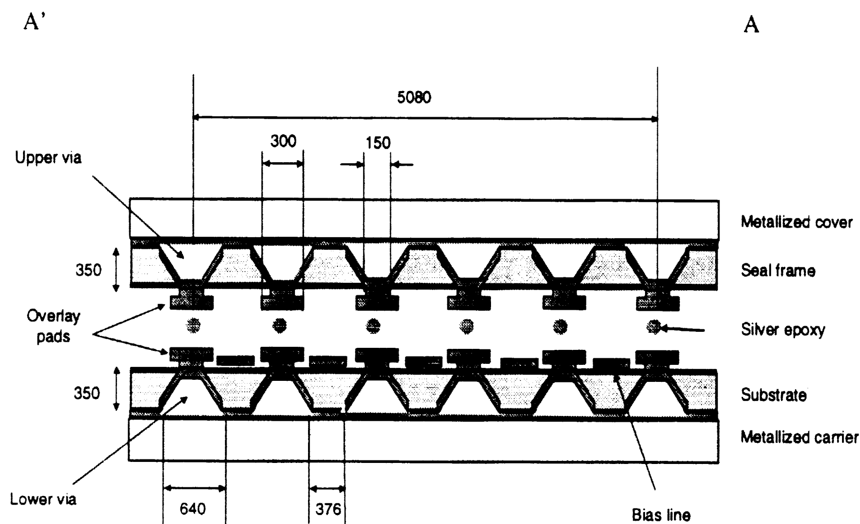


Fig. 4.8: Cross-section A'-A of package layers.

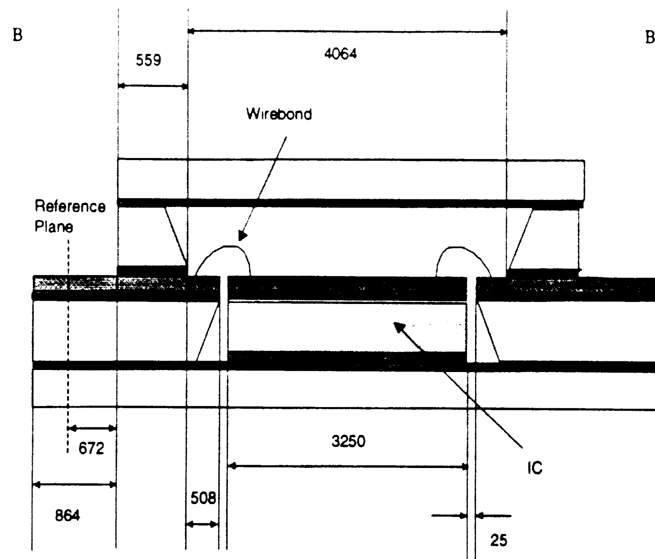


Fig. 4.9: Cross section B-B' shows the assembly of the IC into the package.

4.4 Measurements

The micromachined packages have been evaluated for electrical performance and are compared to the ceramic package. Figure 4.10 shows the top view of an assembled Si package without the top metal layer and cover attached [62].

Measurements have been performed on a microstrip through line representing the phase shifter integrated circuit. On-wafer high-frequency measurements have been conducted using a HP 8510C network analyzer with an Alessi Probe Station and 150-μm pitch ground-signal-ground (GSG) GGB Picoprobes. The network analyzer is calibrated with microstrip TRL standards which shift the reference plane location, thereby eliminating the effect of the GCPW-to-microstrip transition (Fig. 4.12). For on-wafer characterization, the CPW-to-microstrip transition presented in Chapter 3 is used with the microstrip width equal to 320 μm. Probe windows are etched in the seal-frame wafer to access the transmission lines (Fig. 4.10).

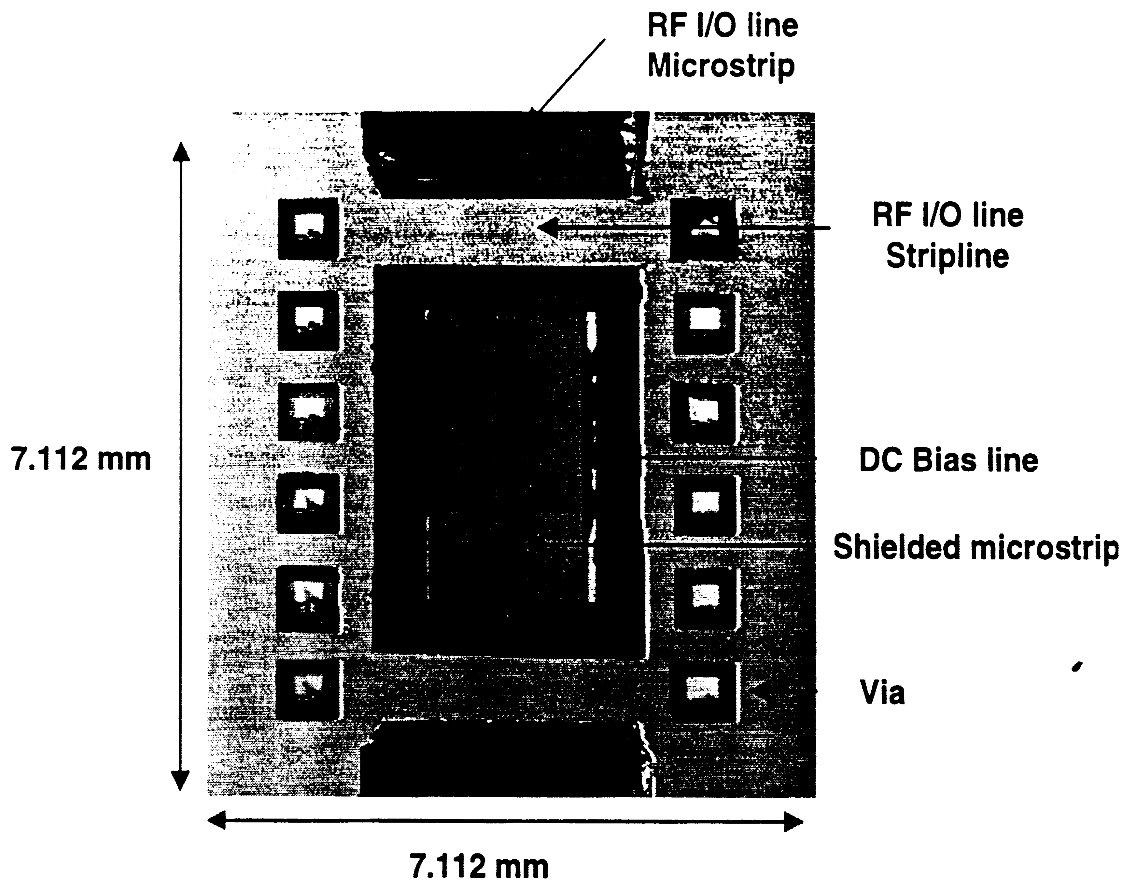


Fig. 4.10: Top view of Si package without metal layer or vias filled.

The feedthrough transitions between microstrip, stripline, and shielded microstrip including steps in width that taper to reduce the effects of the discontinuities. As the wave propagates along the feedthrough, the field lines must transition as well.

Figure 4.13 compares the insertion loss and return loss for the Si (best performing) and alumina package (within a test fixture) along with a Libra simulation of the package interconnects using Si as the substrate material. The physical dimensions of the package interconnect were used to model the effect of the interconnects (Fig. 4.11).

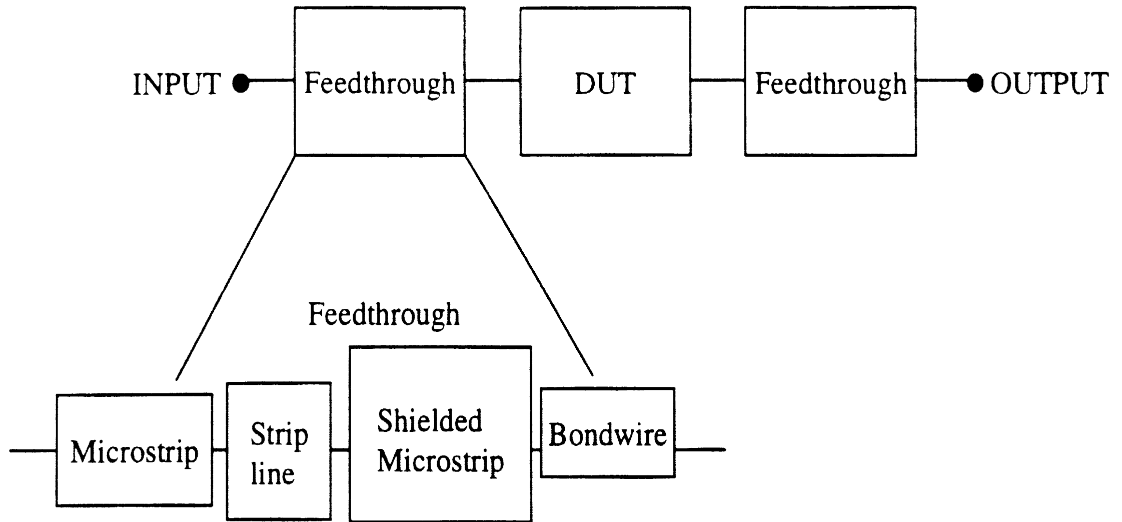


Fig. 4.11: Block diagram of the package interconnects used in the Libra simulation.

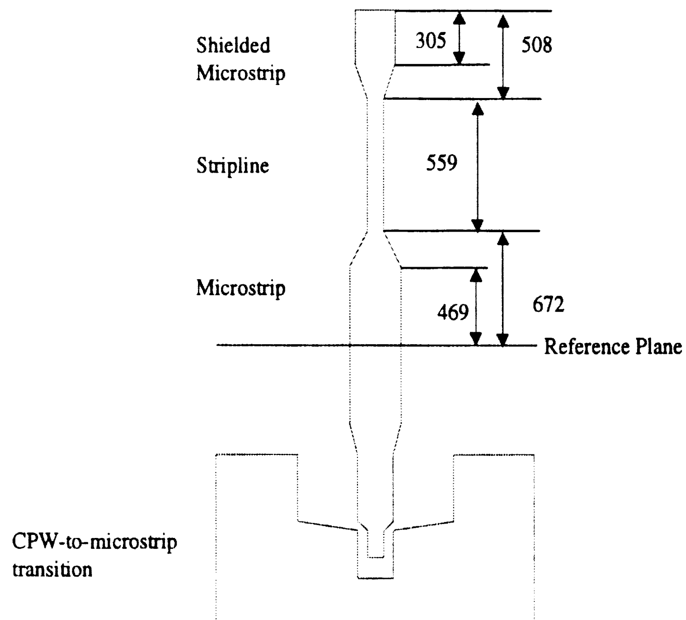


Fig. 4.12: RF input feedthrough with CPW-to-microstrip transition for on-wafer measurements.

The lossless discontinuity effects are shown in the Libra data and indicate that the return loss for the interconnect design can be as high as -20 dB at certain frequencies. The two resonances in the simulated return loss at 30 and 37 GHz imply correlation to the two resonances in the measured Si package at 28 and 34 GHz despite the frequency shift.

The alumina package has been modeled by Yook [60] using a finite element method (FEM) technique where the package detail geometry including bias lines, bondwires, geometrical asymmetries, and vias are considered in modeling. The vertical electrical field of the package is calculated to locate EM field leakage and spurious resonances (Fig. 4.14). Although the vias within the package do not provide total EM shielding for the MMIC, the leakage in the 12 vias suppresses the cavity resonances in the package as shown at 29.5 GHz. Notice the voltage standing wave pattern of the EM field along the I/O line.

In Fig. 4.15 the cross-section of the vias indicates the exposed substrate width where EM field leakage occurs. In the alumina package, the width is 1016 μm and in the Si package that width is 376 μm. This implies more isolation can be achieved in the Si package as a result of wet anisotropic etching.

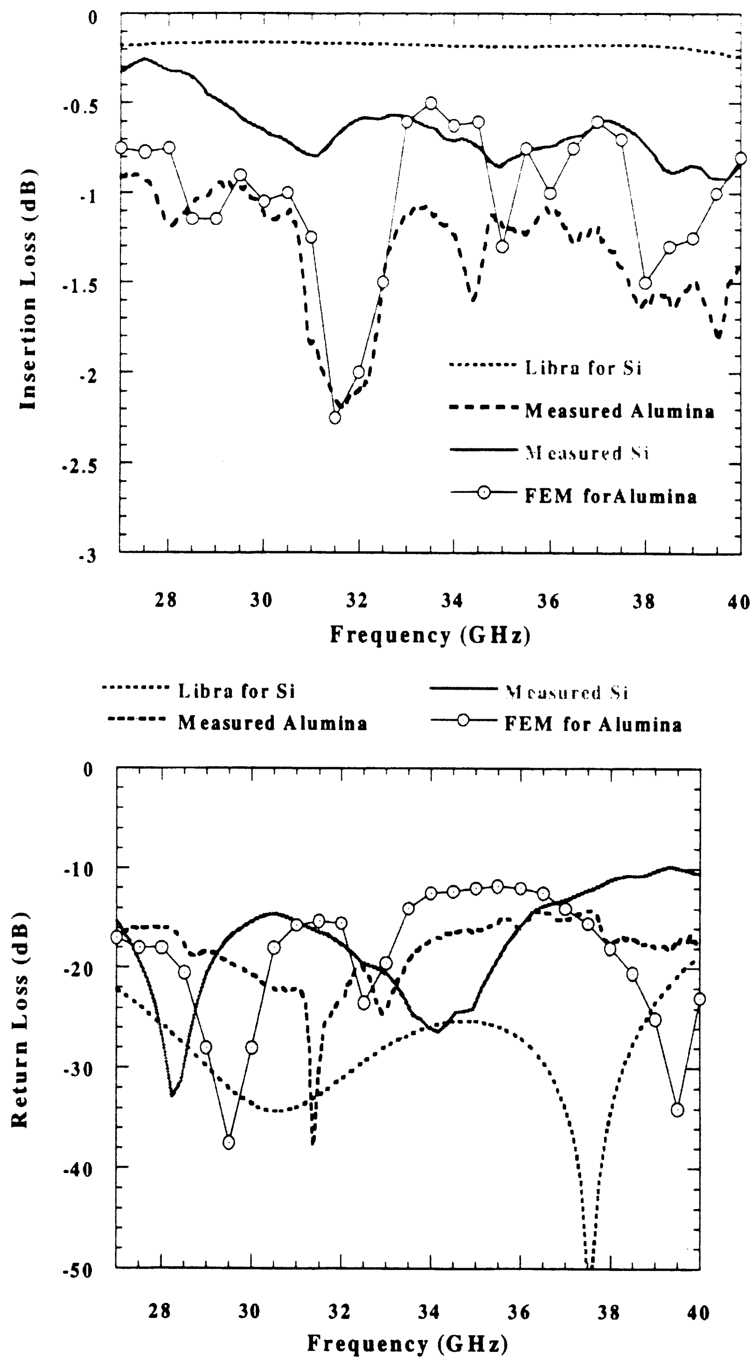


Fig. 4.13: S-Parameters for Libra interconnect simulation, alumina package (within test fixture), and shielded Si package.

Electric Field Distribution in Package at 29.5 GHz

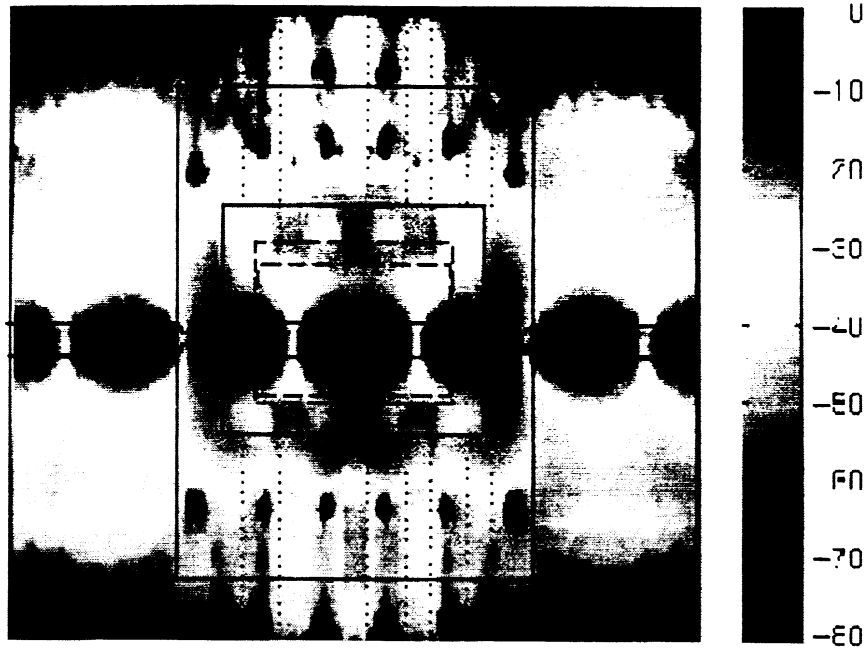


Fig. 4.14: Computed vertical electric field distribution (dB scale) in the asymmetric alumina package at 29.5 GHz. Courtesy of Yook [60].

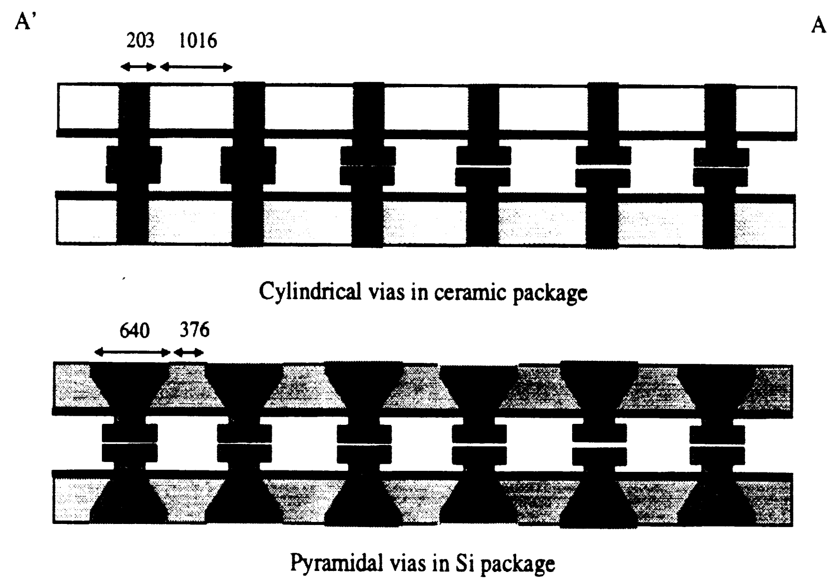


Fig. 4.15: Cross-section (A'-A) of the alumina and Si package illustrating the cavity side wall created by the vias. (Units in microns.)

As listed in Table 4.5, the process steps for ceramic packages require high-temperature firing which alters the surface of the conducting materials and increases RF interconnect losses. A post-firing metallization step can be added to HTCC processing to reduce conductor loss, but it increases production costs. Figure 4.16 shows the attenuation as a function of frequency for a 8 mm-long 50 Ω Au electroplated microstrip line (typical package length). Attenuation is calculated as,

$$Attenuation = -\frac{S_{21}}{LineLength} \tag{4.6}$$

It can be seen from the measurements that conductor loss can be reduced by increasing circuit metal thickness during electroplating [55]. The skin depth, δ, is defined as,

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{4.7}$$

where ω is the angular frequency, μ is the permeability, and σ is the conductivity of the metal. For Au at 20 GHz, δ is equal to 0.55 μm and the two metal thicknesses represent 14.5 and 5.4 skin depths for 8 and 3 μm of plated Au, respectively. Notice that the additional 5 μm of Au reduces the attenuation by a factor of two up to 26 GHz.

By virtue of the processing capabilities alone, thin-film techniques are the best alternative for low-cost mm-wave packages. The use of micromachining techniques not only improves electrical performance but also provides a simplified method of fabrication.

PROCESS	THIN FILM	THICK FILM
Circuit Metal	Electroplating	Screen Printing
Via Formation	Micromachining	Punching
Package Assembly	Bonding	High Temp Stacking and Firing
Via Metallization	Evaporting/Epoxy	Epoxy before Firing
Chip Insertion	Micromachining	Pedestal/Solder Preform
Metal Cover	Bonding	Low Melting Point Solder

Table 4.5: Process steps for thick and thin film packages.

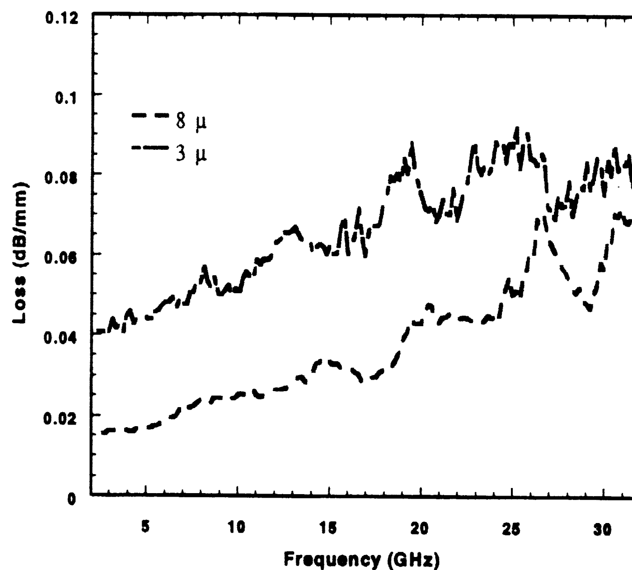


Fig. 4.16: Comparison of attenuation for two metal thicknesses for an 8 mm long microstrip line. the typical length with two metal thicknesses.

The following measurements compare Si structures and are more lossy than the best performing Si package due to misalignment of the through line and interconnects. Figure 4.17 shows how placement of the top lid affects performance of the package. Slight frequency shifts and more loss are due to the

conductor metal on the backside of the cover. Finally, the three designs are compared in Fig. 4.18. There is fairly good agreement between the three measurements in S_{21} which shows the design asymmetries do not significantly impact performance.

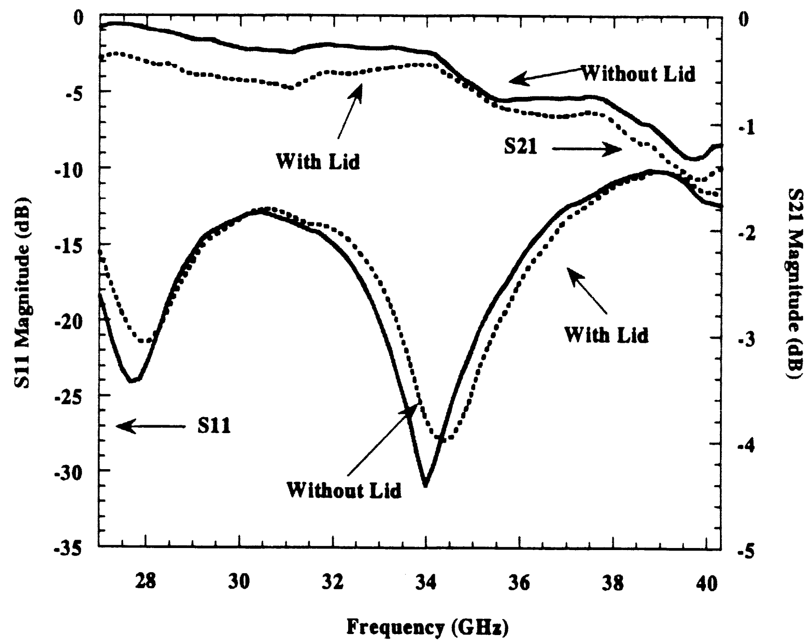


Fig. 4.17: S-Parameters for a symmetrical package with and without lid added.

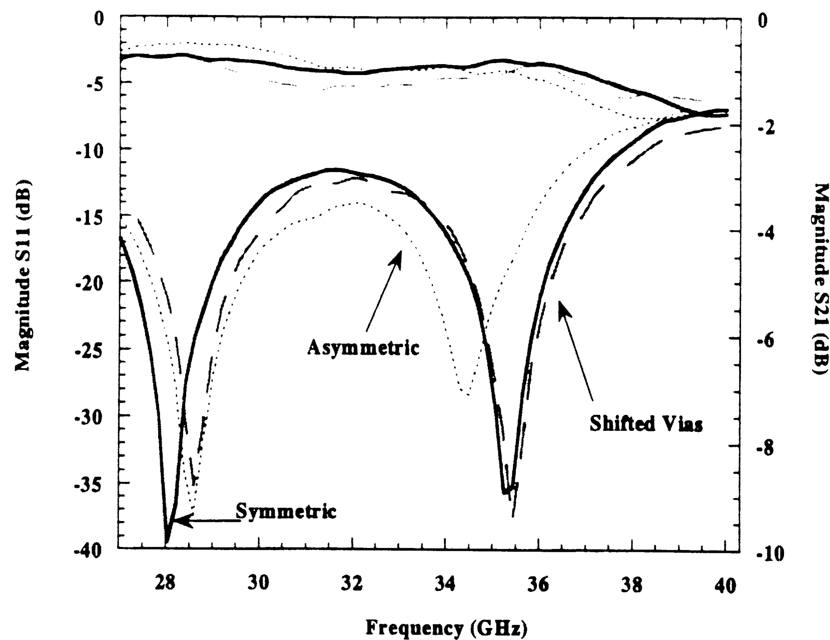


Fig. 4.18: S-Parameters for different package designs: Completely symmetric (Design #3), shifted vias (Design #2), asymmetric (Design #1).

4.5 Summary

It has been shown that a Si-based package for Ka-Band discrete circuits can offer improved electrical performance as compared to its ceramic counterpart, when thin-film and micromachining techniques are applied to develop the housing for the electronic device.

The proposed packaging concept involves the same processing techniques used to realize the electronic devices they are protecting. Performance degradation associated with package and circuit incompatibilities can be reduced when both are manufactured simultaneously and eliminated when the package and circuit are the same material. Batch-fabrication of the Si-based packages can reduce production costs by as much as a factor of 30. These advances can significantly impact the wireless industry as it strives to produce low-cost, high-performance, microwave communication systems.

CHAPTER V

HYBRID TECHNIQUES INTEGRATING CONFORMAL PACKAGING WITH FLIP-CHIP TECHNOLOGY

5.1 Introduction

For the commercial industry to take advantage of the recent reallocation of bandwidth at mm-wave frequencies [63], high performance systems at extremely low costs must be realized. Currently mm-wave MMICs are quite expensive due to low yield in performance and the high cost of III-V material. Passive components and active devices are fabricated on the same wafer resulting in inefficient use of the active substrate. This costly process results in even lower circuit yield when multiple devices are incorporated.

An alternative to developing monolithic ICs at microwave frequencies is using hybrid techniques where the active device is wire bonded to a low-cost substrate. At mm-wave frequencies however, the parasitics associated with bondwires inhibit circuit performance due to uncontrollable inductance. Consequently, flip-chip mounting of active devices onto low-cost substrates with coplanar transmission lines has become a promising solution producing high yield connections with low parasitics [64], [65].

Along with a cost-effective fabrication methodology for high performance commercial MMICs, there must be an equally developed packaging technique in place to transfer the performance to the system in which it was designed. For most hybrid or monolithic designs, packaging is still being considered at the end of the design cycle and results in low overall system performance due to package resonances and parasitics. By designing monolithic integrated circuits with integrated packages, performance yields will ultimately increase. The concept of packaged circuits based on Si micromachining techniques have been demonstrated by Robertson [66], and Drayton [20] and is extended here to more complex designs.

As reported by Al-sarawi three-dimensional (3-D) packaging is the future technology for VLSI applications because it offers significant reductions in weight and volume over multi-chip module and discrete packaging technologies [67]. The development of a mature 3-D packaging technology provides great promise for high frequency applications where low power consumption, low weight, and compactness are high priorities. As mentioned previously, vertical integration is a way in which wafer real estate can be increased by reducing the total substrate area needed for a circuit layout. Figure 5.1 shows a schematic indicating how Si circuit density is increased by implementing 3-D packaging technology.

Fig. 5.1: Substrate area for MCM versus substrate area for 3-D technology [68].

In most high-frequency applications, planar circuits are designed and fabricated using standard IC (thin-film) processing techniques. With the requirement for increased density in planar circuits, the need to develop vertical integration for thin-film circuits technology is becoming more important. In multi-layer circuits, conductor metal strips are separated by dielectric layers. Si micromachining can be used to isolate and shield conductors while providing a support for additional interconnect circuits printed on vertically stacked substrates as shown in Fig. 5.2. The two-wafer packaged circuit with shielding cavity is a fundamental element which can be used in a Si multi-layer circuit technology.

Fig. 5.2: Si micromachined two-layer packaged circuit. The upper wafer shields conductors and provides support for vertical integration.

The objectives of this chapter are to study the effects of on-wafer shielding of interconnects and circuits appropriate for 3-D integration in an effort to demonstrate the cost-effective option of integrating Si packaged circuits with flip chip mounting for mm-wave applications. The performance of transmission lines and circuits using two different shields (dielectric and metal) is studied to determine the usefulness of the additional metal layer for packaged circuits [68]. As an application example for this concept, a low noise amplifier (LNA) circuit is designed and fabricated.

5.2 Circuit and Package Design

An integrated packaged circuit consists of two Si wafers bonded together as shown in Fig. 5.3. The interconnecting geometry is a finite ground coplanar waveguide (FGC) because of the excellent propagation characteristics [69]. Si micromachining techniques is used to develop the air cavity wafer. The air cavity is 275 μm away from the circuits and the two wafers are bonded together with silver epoxy. The cavity width is 800 μm and the total transmission line width is 1200 μm.

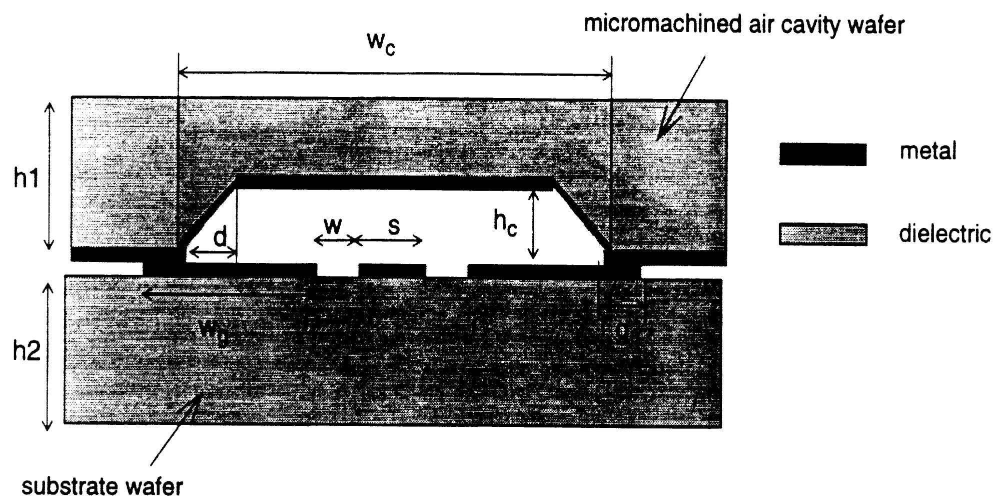


Fig. 5.3: Cross-section of packaged FGC line and upper shielding cavity (with or without metallization) of height h_c=275, w_g=500, w=53, s=94, h1=500, h2=400, d=385, g=200, wc=800 μm.

Excellent noise figure measurements and the highest possible cutoff frequencies for useful gain at frequencies above 100 GHz are performance traits which have identified Indium Phosphide high electron mobility transistors (InP HEMTs) as the best device for mm-wave low-noise applications [70]. Herein a 3-stage LNA circuit has been designed using discrete devices which are bonded onto the substrate using flip-chip attachment with tin/lead solder bumps. The InP HEMT device has been developed at HRL Laboratories, and the structure consists of a 250 nm undoped AlInAs buffer with a 40 nm

GaInAs channel, a 1.5 nm undoped spacer, an 8 nm AlInAs donor layer, and a 7 nm GaInAs doped cap. The gate length and total gate width are 0.15 μm and 300 μm, respectively, and a 100 nm Si nitride layer protects the device from particulates and moisture [71]. Tin/lead (Sn/Pb) solder bumps make contact between the chip and the substrate.

In the original microstrip-based design developed at HRL [73] (ε_r=3, t=250 μm), radial stubs and 20 pF lumped element capacitors isolate the DC from the RF along the bias paths. Coupled line filters block the DC and radial stubs provide matching for the gate and drain (Fig. 5.4). The stub lengths in each stage have been optimized using Libra to produce maximum gain given for low noise matching conditions.

High and low impedance sections (125 Ω and 50 Ω) are designed on a low dielectric constant material (ε_r=3). When implemented in Si (ε_r=11.7) the high impedance line widths are difficult to realize with contact photolithography. In addition, changing from high to low impedance sections (change in width) increases the number of discontinuities and limits overall circuit performance. For these two reasons in addition to the advantage of flip-chip bonding onto coplanar lines, the design has been converted to 50 Ω finite ground coplanar waveguide (FGC) on high resistivity Si (ε_r=11.7, t=400 μm) and the lumped elements are replaced with monolithic components [73]. The radial stubs are replaced with balanced shunt open stubs [74] and the coupled line filters are replaced with series open-end stubs. Libra has been used to optimize the transmission line lengths for high bandwidth. Figure 5.4 shows the schematic diagram for both designs and Fig. 5.5 compares the expected performance based on Libra simulations for the original design and the "corrected" design which includes the new layout dimensions.

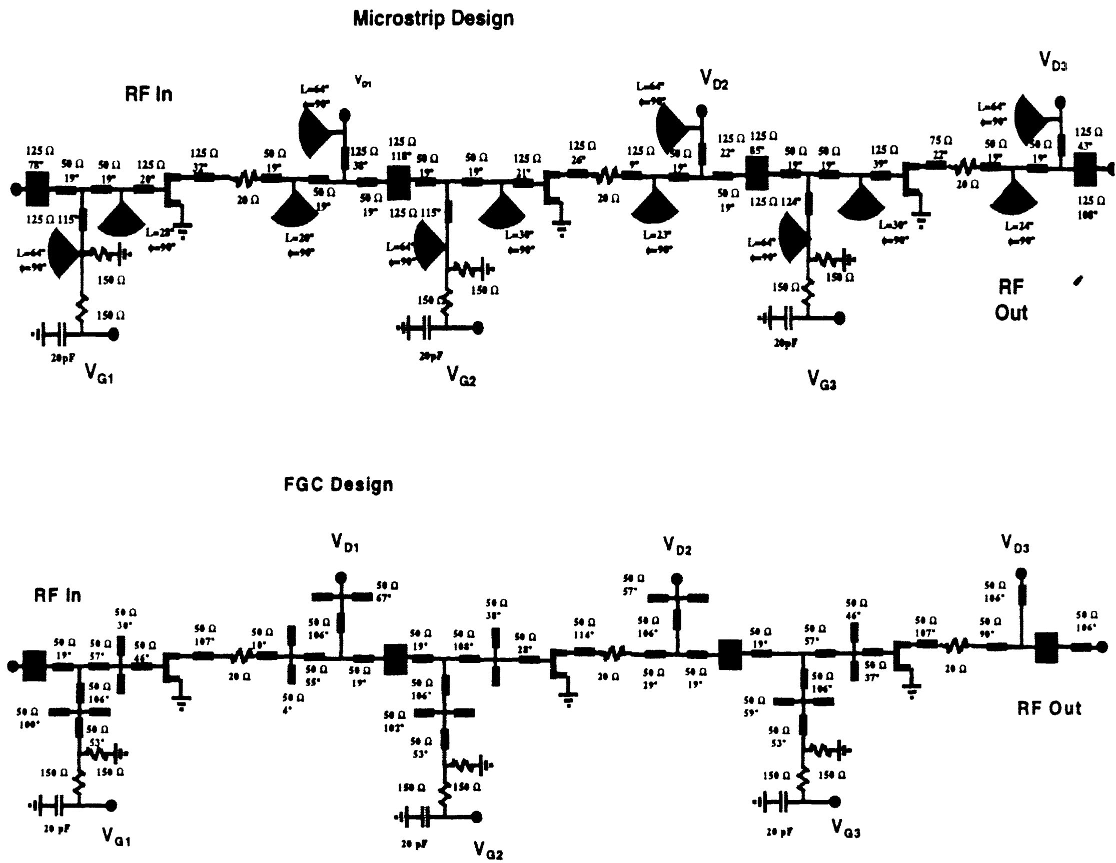


Fig. 5.4: Schematic diagram of microstrip and FGC 3-stage LNA.

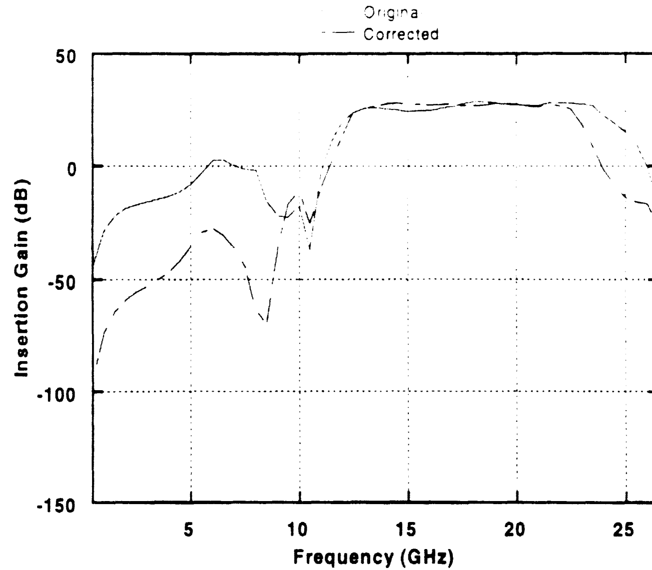


Fig. 5.5: Libra simulated insertion gain for original design (Libra_Ideal) and corrected design (Libra_corrected) for fabrication.

To prevent circuit crowding in the layout, additional transmission line lengths have been added in the RF and bias paths of the FGC design (Fig. 5.6). The transmission line extending from each bias circuit tee has been set to a fixed length of 2845 μm to isolate the ground planes. An additional $\lambda_g/2$=3062 μm has been included along the RF path to accommodate for the shunt stub lengths in the DC bias network. On-wafer biasing is included with the gate and drain DC lines routed to one location onto the substrate (see Fig. 5.6). A customized six-lead DC bias probe has been designed so that all devices can be probed at one time. Libra was used to optimize the transmission line lengths to improve the bandwidth of the circuit. The overall size of the on-wafer packaged structure including bias routing is 33.4 x 12.6 mm^2 while the estimated size of the microstrip circuit without packaging is 23 x 4.5 mm^2. The microstrip circuit would have a size of 34 x 10 mm^2 when packaged in a discrete chip carrier without bias routing included.

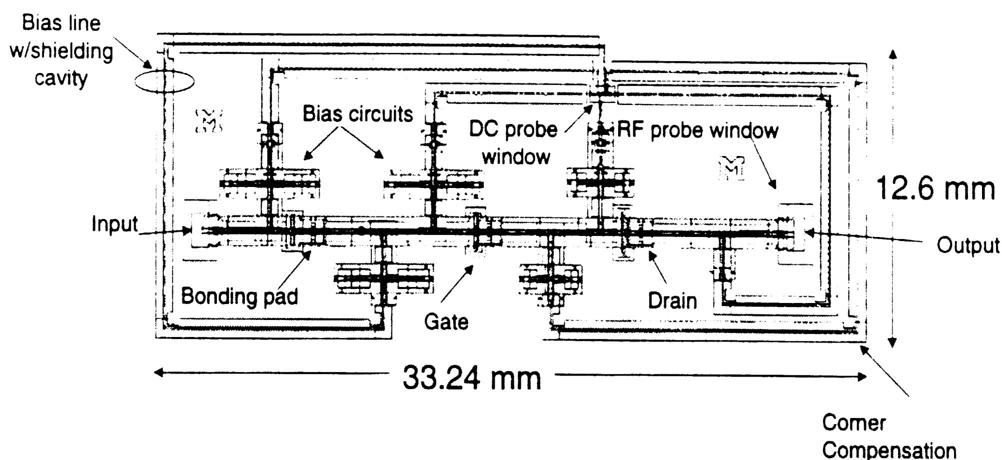


Fig. 5.6: FGC mask layers for LNA.

5.3 Fabrication and Assembly

The process steps for the circuit wafer include the development of tantalum nitride (TaN) resistors, gold (Au) electroplated circuit metal, nickel (Ni) solderable pads, polyimide solder wells, alumina (Al_2O_3) metal-insulator-metal (MIM) capacitors, and Au electroplated airbridges. The interconnects and circuits are fabricated on 400 μm-thick high-resistivity Si using standard lithographic steps detailed in Appendix D.

The upper shield is fabricated on 500 μm-thick low-resistivity Si with an 8500 Å thermal SiO_2 masking layer. Since right-angle bends are used in the mask layout (Fig. 5.5), compensation squares (500 μm) have been added at each convex corner. The air cavities and access windows for alignment, RF probing, DC biasing, and flip-chip mounting, are etched using (EDP) water solution. Th wafer is etched from both sides simultaneously so the access windows (500 μm) and cavity (275 μm) can be realized at the same time and reduce the total etch time from 6.25 to 3.5 hours.

A photograph of the fabricated circuit wafer is shown in Fig. 5.7. There are two circuits, a set of TRL calibration standards, and individual passive components including capacitors, shunt stubs, series stubs, and resistors. After fabricating the circuit wafer, the individual passive components are tested for DC and RF performance. It is necessary to verify that the airbridges and capacitors have not been damaged in processing. Using a multimeter, airbridge locations are tested for short circuits. Using a HP LCR meter, the capacitance values are measured within the circuit. RF performance of the capacitors and stubs is recorded as well.

The SiO_2 layer is removed from the micromachined wafer using BHF (dielectric shield) and Au electroplated (metal shield) for bonding. Silver epoxy is placed along the cavity wafer and it is inverted and aligned over the circuit wafer with a hotplate, micrometer, and microscope vacuum system typically used for wafer-to-wafer bonding [75]. The wafers are cured at 120°C for 15 minutes and the flip-chip HEMT devices are mounted off-site at HRL Laboratories with a bonding machine manufactured by Semiconductor Equipment Corporation [76].

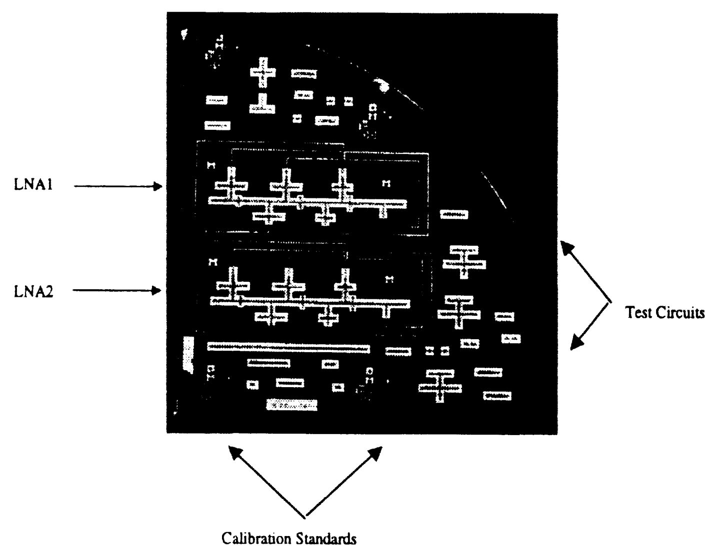


Fig. 5.7: Photograph of 1/4 of a 4 inch wafer used for fabricating LNA circuit. Notice two circuits in the center with test devices and cal standards on the edges.

5.4 Measurements

The S-parameters of the circuits are measured on a HP8510C Network Analyzer, using 150 μm pitch GGB Picoprobes from 2 to 40 GHz. A TRL calibration method using NIST's Multical program is performed to shift the reference plane directly to the packaged circuit [77]. The following sections detail the design and performance of the individual components and conclude with the measurement of the LNA.

5.4.1 Transmission Line Characteristics

Line losses due to parasitic radiation can be eliminated by adding shielding cavities, leaving ohmic loss and dielectric loss as the contributors to line attenuation. FGC input lines for the amplifier circuits have been designed for a characteristic impedance (Z_0) of 50 Ω (s = 94 μm, w = 53 μm, wg = 500 μm). These lines are intrinsically lower in loss because the field lines propagate within the slot apertures, offer higher isolation, and provide better compactness when compared to conventional CPW. Although there is no need for via hole processing, airbridge technology is needed to equalize the ground planes of such a complex layout (Fig. 5.6).

The effective dielectric constant (ε_{eff}) and attenuation (α) of FGC lines used in this circuit design have been extracted using the Multical program. Figure 5.8 compares the attenuation for the "conventional" (unshielded) line with the dielectric and metal shield lines. Results show that the attenuation is greater in the metal shield due to the additional conductor metal on the package walls (Fig. 5.9). The ε_{eff} for FGC line when operating in an open and shielded by a dielectric cavity is very similar, however, the FGC line shielded

by a metallic cavity exhibits higher dielectric constant due to increased line capacitance.

The cross coupling between two parallel lines separated 774 μm edge-to-edge is shown in Figures 5.11 and 5.13. The longer line is excited at Port 1 and the induced standing wave on the coupled line is measured from Port 4. The other two ports (2, 3) are left open [29].

HFSS simulated a similar response for two parallel FGC lines of the same cross-sections (Fig. 5.12). To reduce processing time, the longer line length is reduced to of 4.55 mm and the shorter line length is reduced to 1.8 mm and placed 2.75 mm away from the longer line (similar to the layout in Fig. 5.11). Port 2 is shorted and port 3 is left open. The coupling for all three architectures is comparable with the best performance within the design bandwidth from the conventional line.

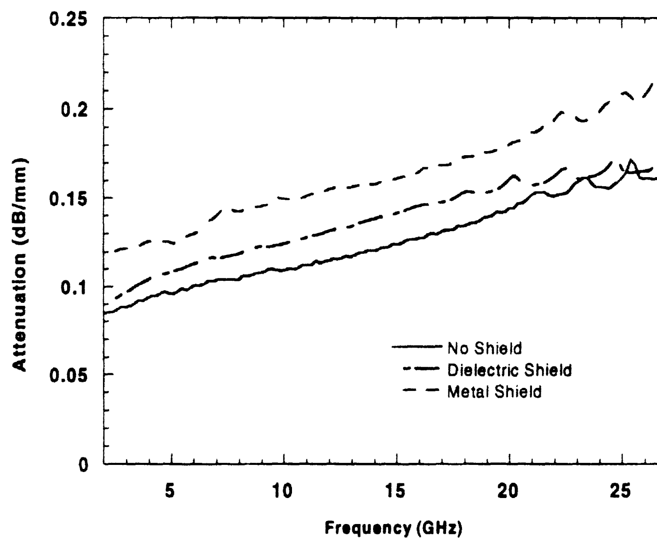


Fig. 5.8: Attenuation for different packaging environments.

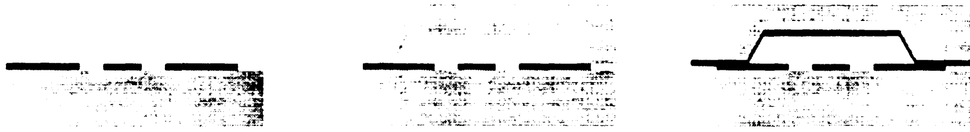


Fig. 5.9: Cross-section for conventional, dielectric shielded, and metal shielded FGC lines.

The increase in coupling observed in the lines with metal shielding is due to the continuous ground between the lines, provided by the shield. Figure 5.13 shows that shielding by dielectric cavities can reduce coupling at the lower frequencies by as much as 5-10 dB to provide isolation as high as -60 dB [29]. The coupling measured is 6 dB higher than that expressed when the lines are matched.

Figure 5.13 shows the measured and average level of coupling for each case separately. Notice the increase in coupling above 25 GHz for the lines covered with the metal shield.

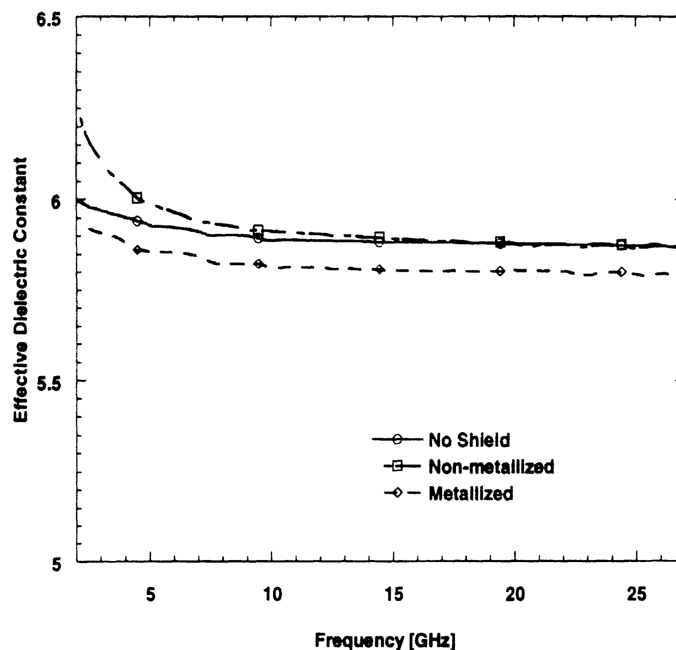


Fig. 5.10: Effective dielectric constant for different packaging environments.

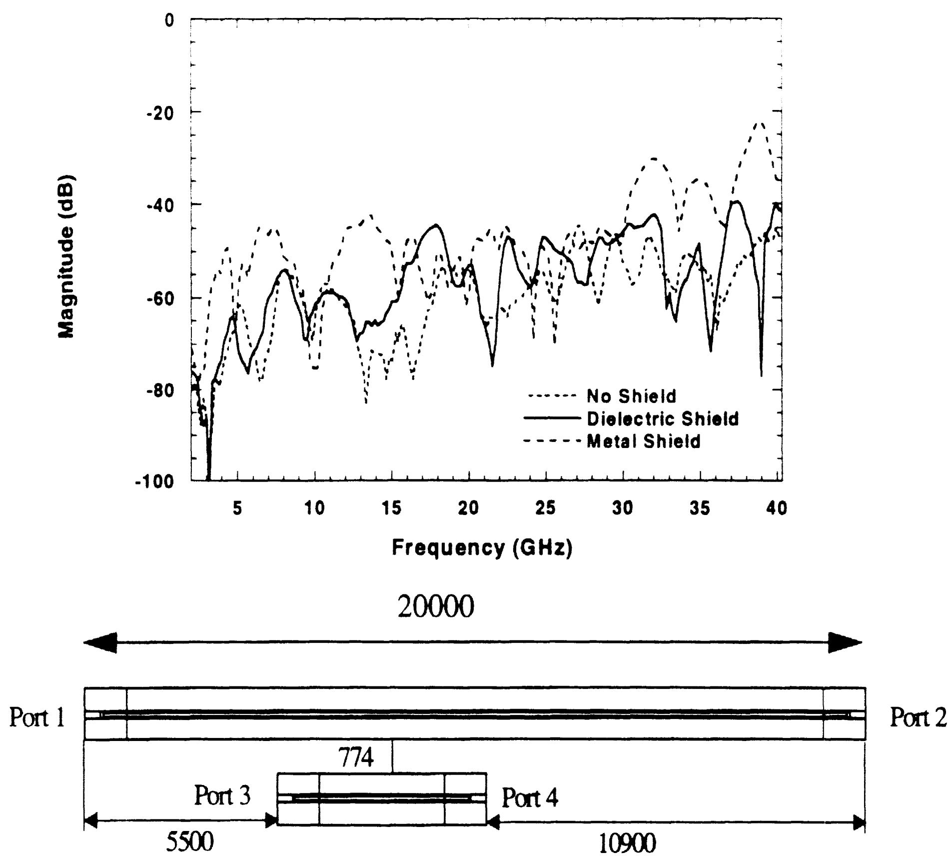


Fig. 5.11: Cross coupling measurements for different two planar FGC lines (Dimensions in microns).

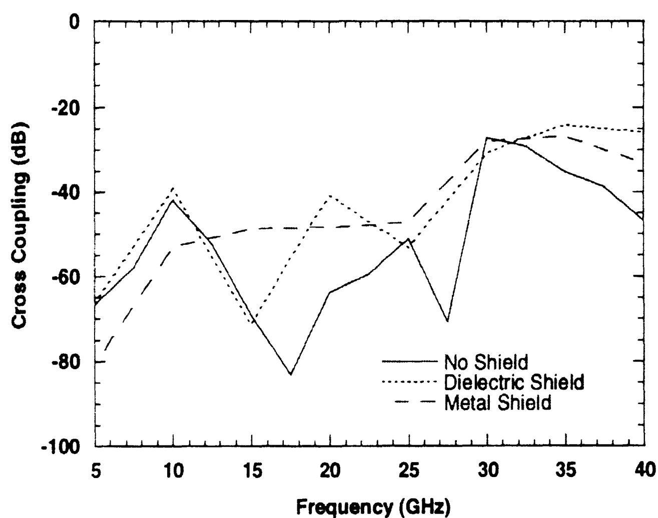


Fig. 5.12: HFSS simulation of similar FGC layout where the ground planes edges are separated by 871 microns.

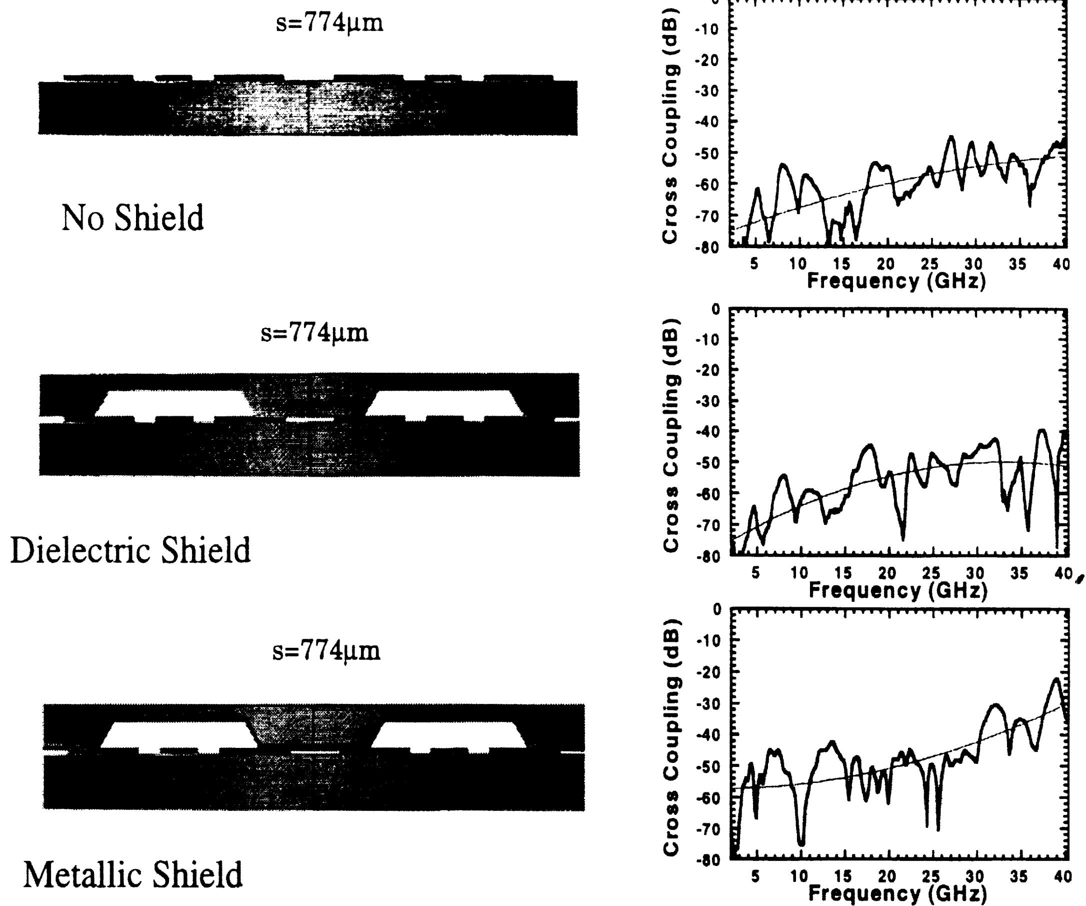


Fig. 5.13: Cross coupling between planar lines separated 774 microns edge-to-edge.

5.4.2 RF Components

In addition to studying the transmission lines characteristics, individual components incorporated in the circuit have been characterized. When converting the design from microstrip to FGC, radial stubs are replaced by balanced open shunt stubs for matching and biasing. In order to predict the performance of the biasing stubs in the presence of the FGC tee and air-bridges, a stub design for 14 GHz has been modeled using a full wave simula-

tor (IE3D) [78] (Fig. 5.14). The IE3D modeling considers the stub in an open environment but does not take into account ohmic losses. A photograph of the stub and corresponding shielding cavity (inverted) is shown in Fig. 5.15. There is good agreement between the simulated and measured results in Fig. 5.16. The effects of the metal shield on the stub performance in Fig. 5.17 indicate a resonant shift of 1 GHz.

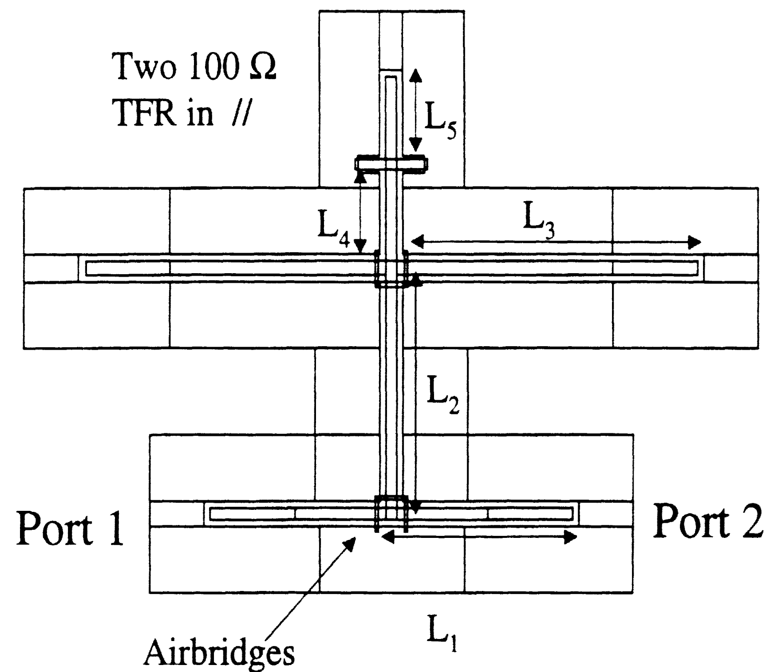


Fig. 5.14: Open balanced stub with dimensions: L_1=753, L_2=1752, L_3=2485, L_4=630, L_5=698. Units are in microns.

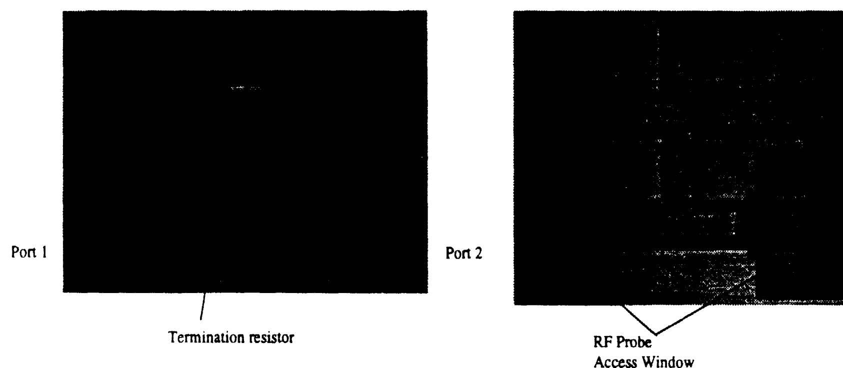


Fig. 5.15: Photograph of shunt stub and corresponding shielding cavity inverted to show etching and convex corners.

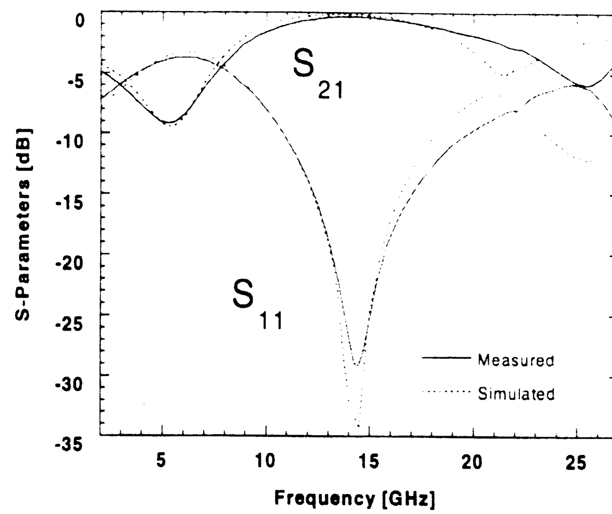


Fig. 5.16: Comparison between measured and simulated S-parameters for balanced open shunt stubs. The simulation considers air bridges and T-junctions.

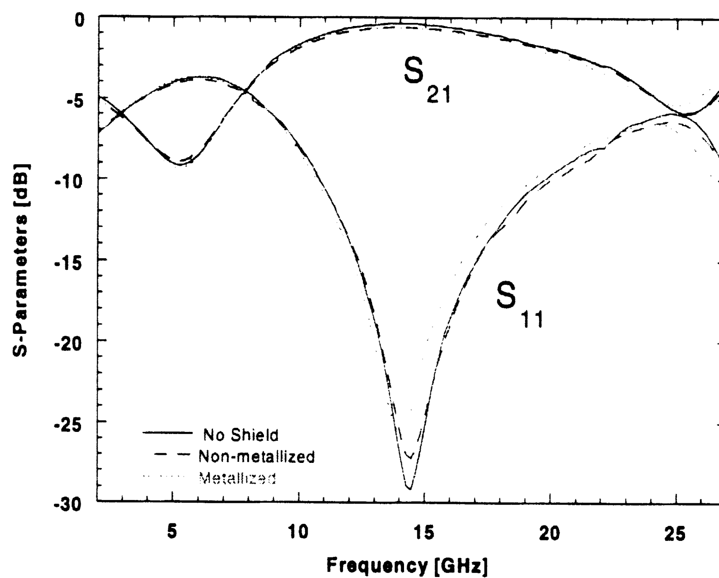


Fig. 5.17: Comparison of S-parameters for the balanced open shunt stubs for the fabricated cases (no shield, dielectric shield, metal shield) versus the simulated case.

The microstrip DC block is replaced by a series open-end stub series open-end stub The stub (Fig. 5.18) is modeled using HP Momentum [79] at a design frequency of 23 GHz. A plot of measured and modeled performance is shown in Fig. 5.19 with good agreement. Figure 5.20 shows there is more loss in the circuit with the metal shield due to the continuous ground plane.

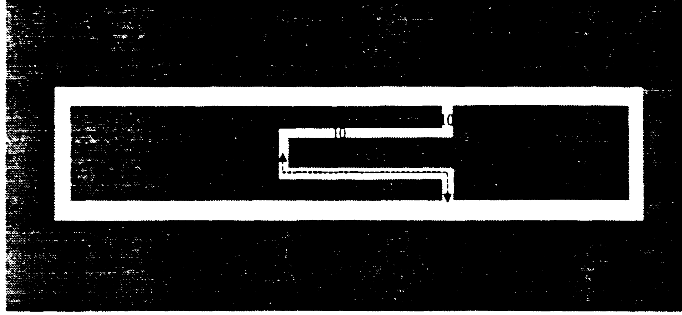


Fig. 5.18: Open series stub resonator used for DC block. The stub length is 1568 microns for the design frequency of 23 GHz.

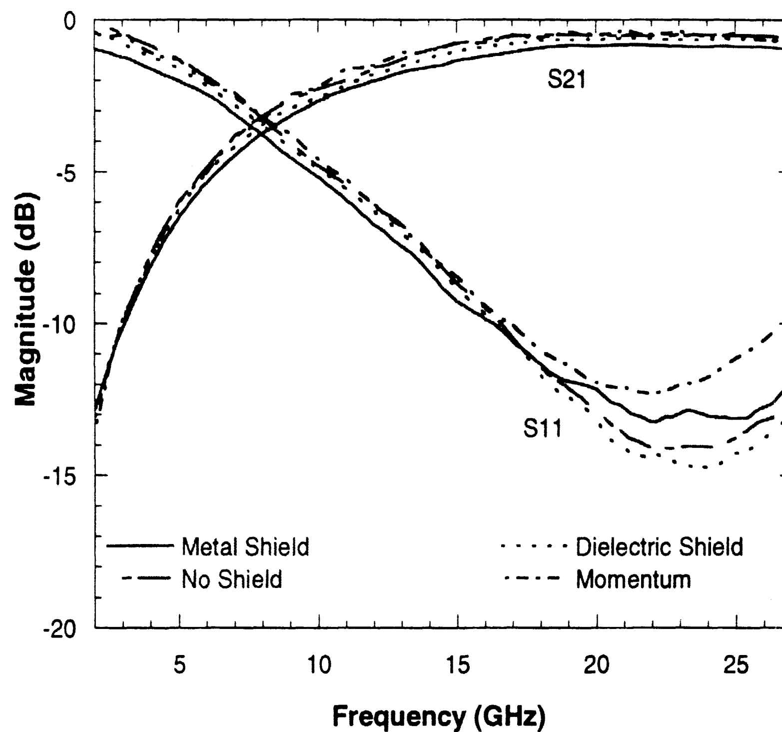


Fig. 5.19: Comparison of reflection and transmission coefficients of the open series stub for calculated (Momentum), open (no shield), metal shield, and dielectric shield environments.

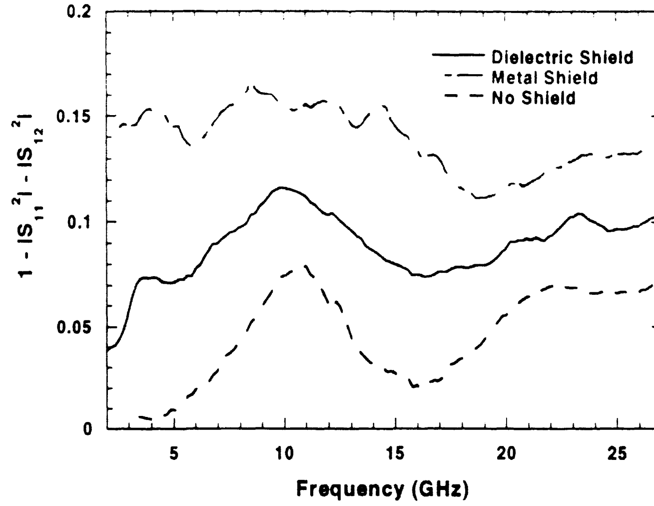


Fig. 5.20: Loss comparisons between measured open-end series stubs.

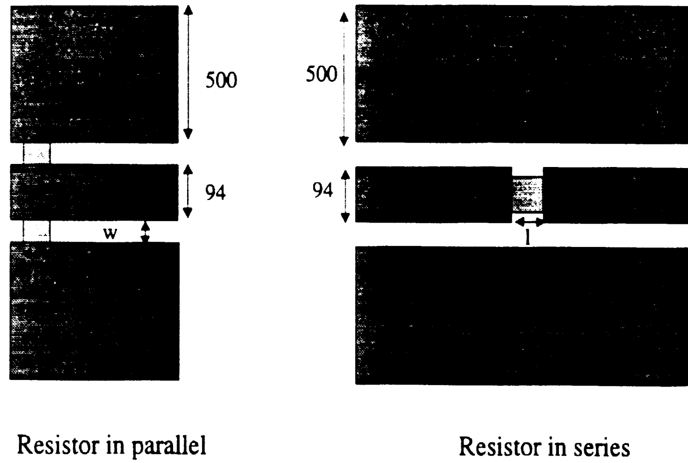
5.4.3 DC Bias Components

RF shunt stubs along with thin-film resistors and MIM capacitors have been used for matching and biasing the gate and drain of the transistors. The thin film resistor is realized when TaN is deposited onto the substrate and the circuit metal provides metal contact as shown in Fig. 5.21. The resistance value R of a rectangular pattern is defined as:

$$R = \frac{R_s L}{W} \tag{5.1}$$

where R_S is the sheet resistivity of the resistor ($R_S=\rho/t$) in Ω/sq, L is the length of the film, W is the width of the film, and L/W is the aspect ratio of the resistor which defines the number of squares needed to realize a certain resistance value [80]. Figure 5.21 shows the layout of a resistor in a parallel or

series configuration with the square defined by the FGC aperture width. Table 5.1 gives the dimensions of the resistors which exhibit a sheet resistivity of 33 Ω/sq.



Resistor in parallel Resistor in series

Fig. 5.21: Layout of resistors in parallel and series.

Resistance (Ω)	Function	Length (μm)	Width (μm)	# of squares
50=Two 100 in //	Termination	228	75	3.03
150=Two 300 in //	DC Bias	227	25	9.09
20	RF	50	82	0.606
150	DC Bias	225	50	4.5

Table 5.1: Dimensions for resistors used in LNA circuits.

MIM capacitors are fabricated by sandwiching a thin alumina layer between two conductive layers. The capacitance value C is defined by

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{5.2}$$

where d is the thickness of the dielectric, A is the area of the overlapping electrodes, and ε_0 and ε_r are the permittivity values for free space and the dielectric material, respectively.

The capacitor dielectric constant ranges from 8 to 10 and the thickness of deposited alumina to realize 20 pF shunt capacitors is 1500Å. Based on the fabrication process described by Robertson [68], three individual capacitors are realized, two across the ground planes (C_g) and one across the center conductor (C_c) (Fig. 5.22). According to the equivalent capacitance formula for the circuit (Fig. 5.23) the overall capacitance value is a function of the center conductor capacitance as long as the ground capacitances are at least twice as large as the center conductor capacitance. The measured RF performance of the capacitor is shown in Fig. 5.24.

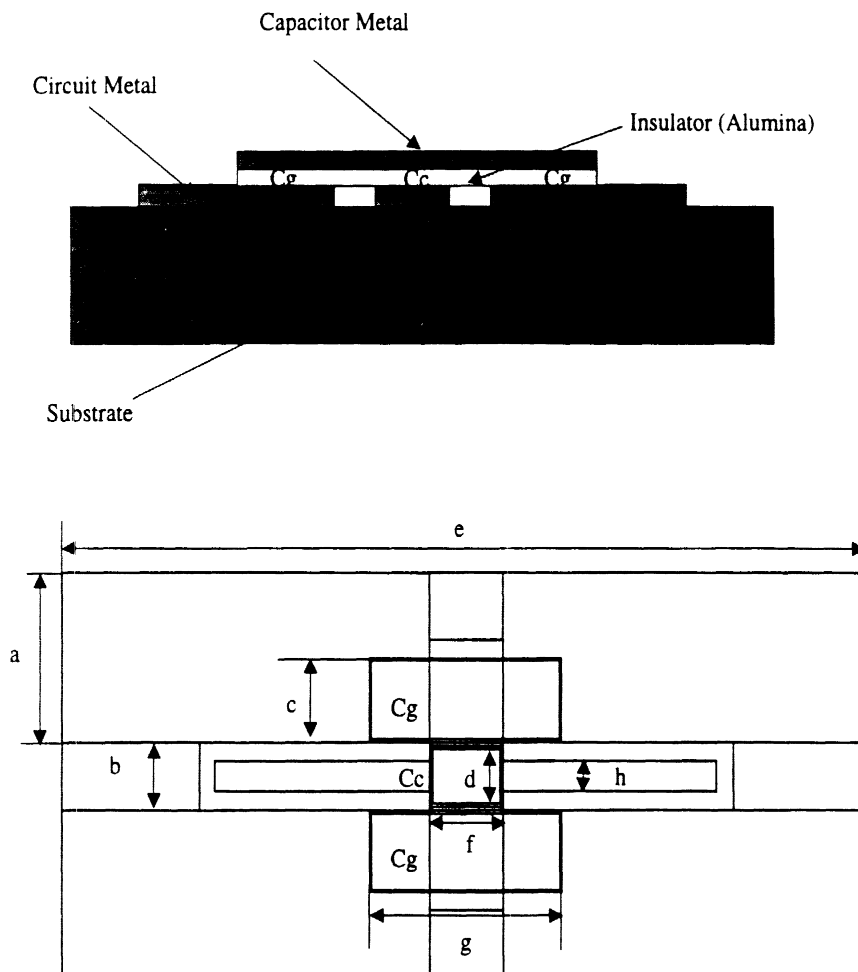
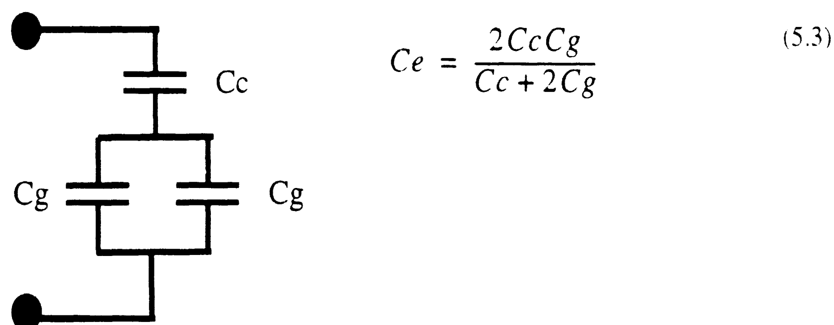


Fig. 5.22: Cross-section and top view of capacitor structure used in LNA circuits with dimensions: a=500, b=200, c=226, d=160, e=2640, f=220, g=627, h=94 μm.



$$Ce = \frac{2CcCg}{Cc + 2Cg} \tag{5.3}$$

Fig. 5.23: Equivalent circuit for capacitors across FGC line.

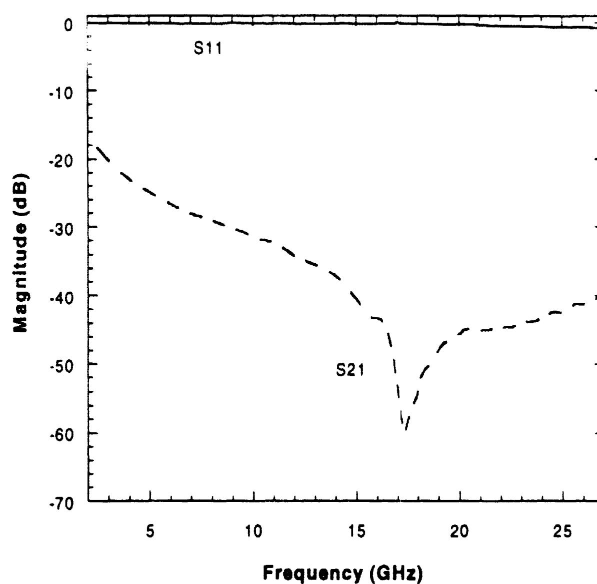
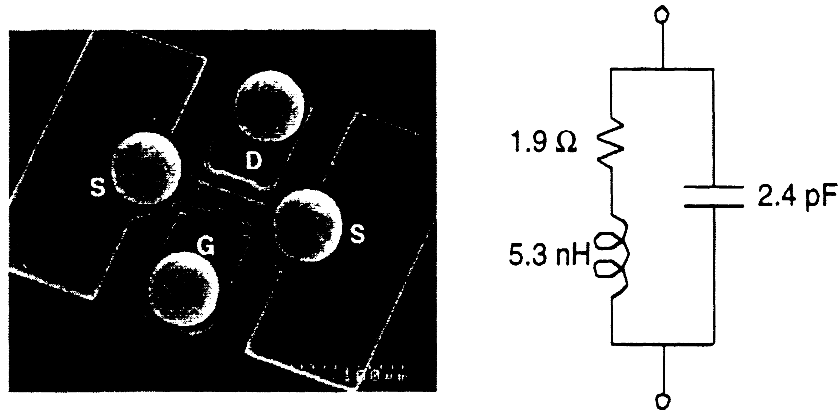


Fig. 5.24: RF capacitance measurements before and after adding airbridges.

5.4.4 Single Transistor Measurements

In Fig. 5.25 there is a photograph of the flip-chip high electron mobility transistor (HEMT) developed at HRL Labs. Sn/Pb solder bumps which are 25 μm high and 50 μm in diameter have been used to mount the transistor on the Si substrate. The gain of a single transistor measured on-wafer (InP) com-

pares well to the gain of a similar device after it has been flip-chip bonded onto the Si substrate. The reduction in gain for the unmounted and mounted case can be attributed to the effects of the solder bumps and the transition to the device when measuring it in a bumped configuration [81]. Introducing a series resistance and inductance in parallel with a capacitor models the loss due to the solder bumps. Table 5.2 lists the bias point conditions and associated gain for the device on InP and the Si substrate with a dielectric shield.



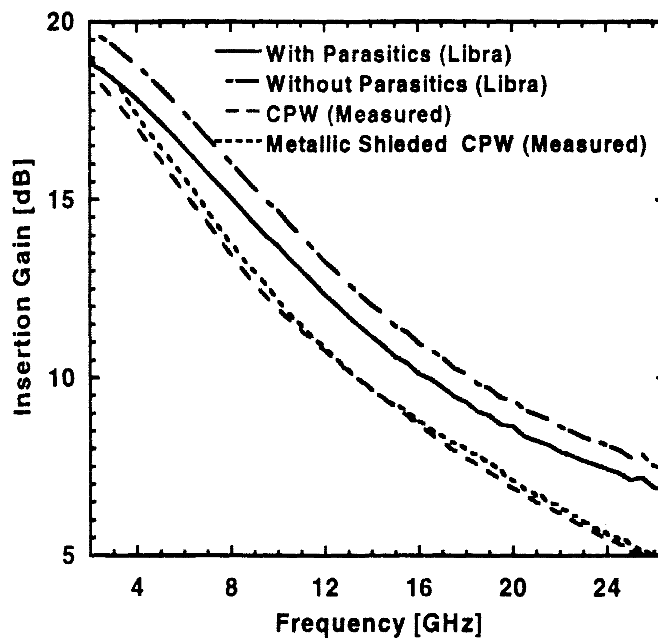


Fig. 5.25: Insertion gain for single transistor. Measured on InP wafer (transistor only), mounted without shielding (No shield), and mounted with metal shield covering transmission lines.

Parameter	InP	Dielectric Shield Si
Gate Voltage (V)	-0.388	-0.7
Drain Voltage (V)	1	1
Gate Current (mA)	-.009	-0.5
Drain Current (mA)	45.04	42.3
Insertion Gain at 20 GHz (dB)	9.4	7.86

Table 5.2: Bias conditions for maximum gain of individual transistor.

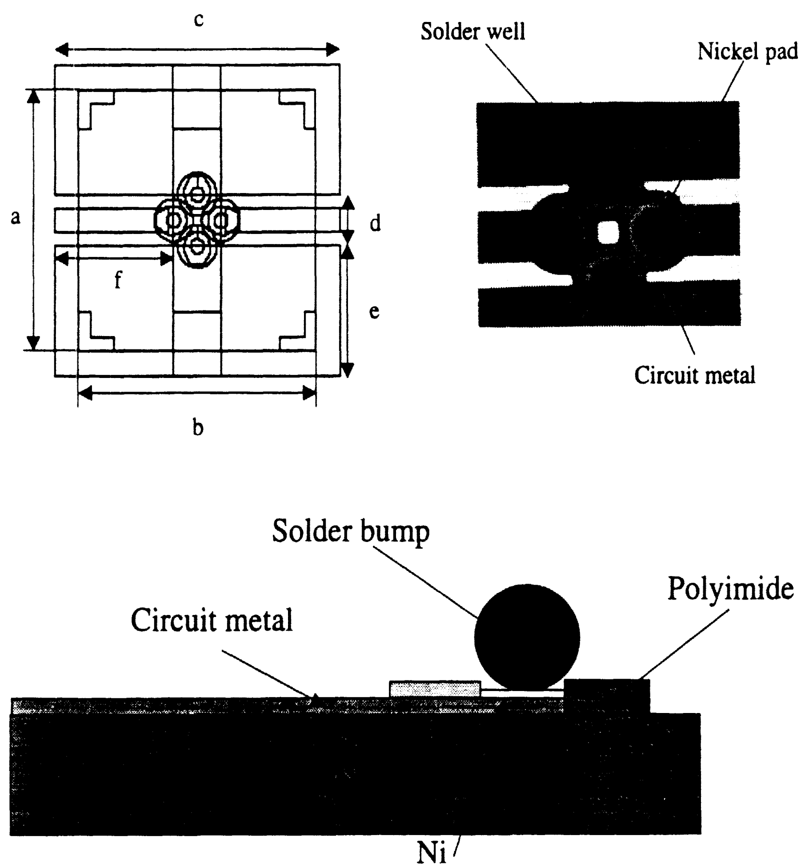


Fig. 5.26: Layout for solder well and flip-chip device (a=1000, b=1000, c=1200, d=200, e=500, f=500: All units in microns).

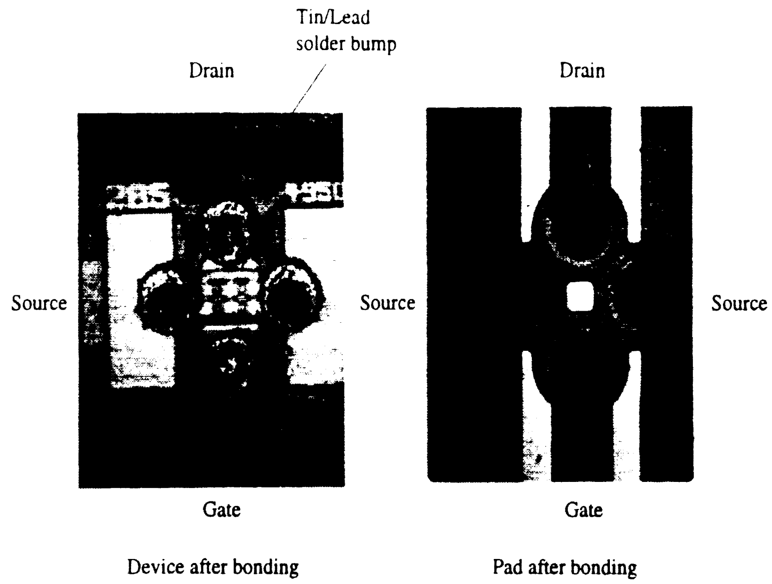


Fig. 5.27: Device and pad after bonding to the Si substrate.

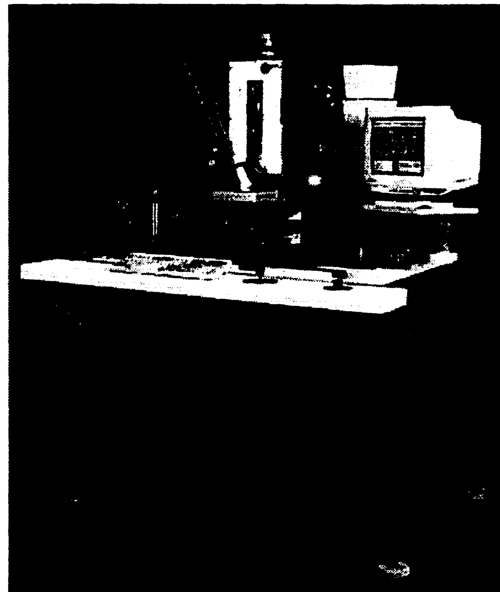


Fig. 5.28: The SEC model 410 aligns and attached the flip chip die onto the machine.

5.4.5 LNA Measurements

The LNA circuit has been measured at HRL laboratories using two calibrations (SOLT and TRL). Using a SOLT calibration up to the probe tips, the gates and drains of each stage are tied together and biased at different conditions to obtain maximum gain. The recorded gain values and the corresponding frequencies are listed in Table 5.3. The maximum gain (S_{21}=12.9 dB at 17.5 GHz) is achieved when the $V_{DS1}=V_{DS2}=V_{DS3}=3$ V and $V_{GS1}=V_{GS2}=V_{GS3}$ = -1.1 V. The corresponding total drain current, I_{DS}=143 mA and corresponds to a value of 47 mA for each device. Using the same bias conditions with a TRL on-wafer calibration, the measured insertion gain increases to 15.7 dB at 17.9 GHz as shown in Fig. 5.29.

Name	V_{DS} (V)	V_{GS} (V)	Total I_{GS} (mA)	Total I_{DS} (mA)	F (GHz)	Cal type	S_{21} (dB)
AB	2	-1	-10	89	18.5	SOLT	7.5
AC	2.5	-1	-10	11.7	18.5	SOLT	9.7
AD1	2.5	-0.7	-7	129	17.5	SOLT	6.2
AD2	2.5	-1.2	-12	110	n/a	SOLT	10.5
AD3	2.5	-1.4	-14	102	n/a	SOLT	8.6
AE	3	-1.2	-12	137	18.5	SOLT	12.6
AF	3	-1	-10	147	17.5	SOLT	12.1
AG	3	-1.1	-11	143	17.5	SOLT	12.9
BA	3	-1.1	-11.2	145	17.91	TRL	15.7

Table 5.3: Bias conditions and associated gain of amplifier when all transistors are biased together.

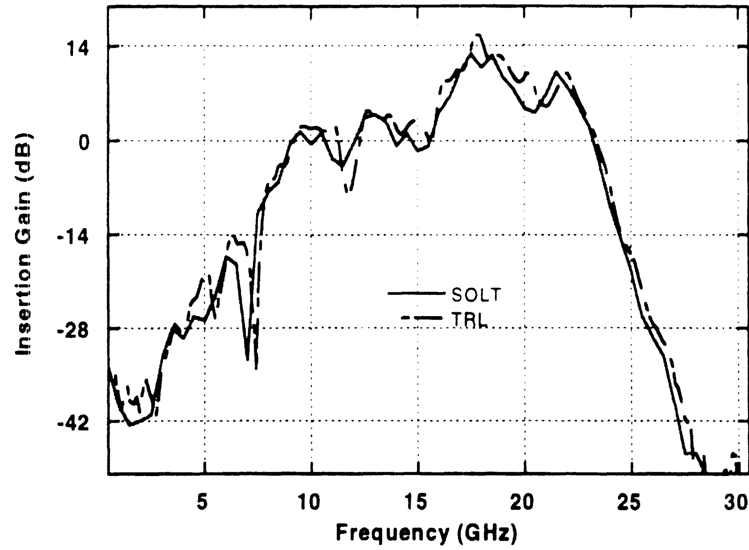


Fig. 5.29: Measured insertion gain of amplifier using two calibrations with $V_{DS(123)}$=3 V, $V_{GS(123)}$=-1.1 V, $I_{DS(TRL)}$=145 mA, $I_{DS(SOLT)}$=143 mA.

To realize more gain, the gate of each stage has been individually biased and the drain voltage is fixed to 3 V. Table 5.4 shows the insertion gain, total currents, for varying gate bias points. The optimum gate bias voltages resulting in S_{21} > 16 dB are V_{GS1}=-1.3 V, V_{GS2}=-1.3 V, and V_{GS3}=-1.0V at approximately 17.9 GHz.

Freq. (GHz)	V_{G1} (V)	V_{G2} (V)	V_{G3} (V)	I_{GT} (mA)	I_{DT} (mA)	S_{21} (dB)
17.757	-1.1	-1.1	-1.1	-11.2	145	15.795
17.757	-1.2	-1.1	-1.1	-11.5	143	16.1
17.757	**-1.3**	**-1.1**	**-1.1**	**-11.8**	**142**	**16.39**
17.757	-1.4	-1.1	-1.1	-12.2	144	16.30
17.757	-1.0	-1.1	-1.1	-10.9	146	15.12
17.905	-1.1	-1.0	-1.1	-10.9	147	15.73
17.905	-1.1	-1.1	-1.1	-11.2	148	16.03
17.905	-1.1	-1.2	-1.1	-11.6	144	16.40
17.905	**-1.1**	**-1.3**	**-1.1**	**-11.9**	**144**	**16.48**
17.905	-1.1	-1.4	-1.1	-12.2	142	16.42
17.905	-1.1	-1.5	-1.1	-12.5	140	16.24
17.757	-1.1	-1.1	-1.1	-11.2	148	15.9
17.757	-1.1	-1.1	-1.2	-11.6	145	15.85
17.905	-1.1	-1.1	-1.2	-11.6	143	15.98
17.905	-1.1	-1.1	-1.3	-11.9	140	15.84
17.905	-1.1	-1.1	-1.4	-12.2	137	15.71
17.905	**-1.1**	**-1.1**	**-1.0**	**-10.9**	**147**	**16.07**
17.757	-1.1	-1.1	-0.9	-10.6	151	15.92
17.757	-1.1	-1.1	-0.8	-10.2	152	15.43

Table 5.4: Gain at different bias points for amplifier.

The flip-chip devices are incorporated in a 3-stage LNA design which uses the interconnects and stubs presented earlier. Figure 5.30 shows the measured and simulated gain results. On this figure three different sets of data derived by Libra [30] and IE3D [78] are compared. The bias conditions are V_{GS}=-0.388 V, V_{DS}=1 V, I_{GS}=-0.009 mA, and I_{DS}=45 mA. The Libra_Ideal sim-

ulation treats the passive components as ideal and models the original design on substrate material ε_r=3 using microstrip. The Libra_Corrected simulation, ε_r=3 on microstrip, converts the electrical lengths and passive components converted to that of the FGC layout. With Libra_IE3D the transmission line is FGC with airbridges included on Si (ε_r=11.7). The results are based on a Libra harmonic simulation where all the passive components have been replaced by the S-Parameters modeled using IE3D and do not consider ohmic loss. The Libra_Physical simulation considers the physical dimensions, effective dielectric constant ε_{eff}=5.7, and attenuation constant, α=0.104 dB/mm (the true loss on a FGC line) at 20 GHz (see Table 5.3).

Simulation	Transmission Line	Airbridges	ε_r	Losses
Libra_Ideal	Microstrip	No	3	No
Libra_Converted	Microstrip	No	3	No
Libra_IE3D	FGC	Yes	11.7	No
Libra_Physical	Physical Transmission Line	No	ε_{eff}=5.7	Yes

Table 5.5: Libra simulations for low noise amplifier circuit.

The three simulations predict a maximum gain of approximately 28 dB centered at 20 GHz. Figures 5.29, 5.30 and 5.31 show comparisons of simulations with the measured LNA. In comparing Libra_IE3D with Libra_Corrected, there is a decrease in gain at the lower frequencies. This can be attributed to the effects of the airbridges and FGC line geometry which have been accounted for in the Libra_IE3D simulation. The predicted low frequency decrease in loss is confirmed in the measured LNA (Fig. 5.31). Although 7 dB

lower in insertion gain, the shape of the two curves agree very well. To account for the overall reduction in insertion gain for the measured circuit, the Libra_Physical simulation is compared with the measured response. When the normal loss for a FGC line on high resistivity is included in the Libra model (0.1 db/mm at 20 GHz), the maximum gain achievable for this layout is approximately 19 dB at 19 GHz.

The continuous masking dielectric SiO_2 is not removed from the circuit and contributes to a reduction in insertion gain. In addition, the suggested biasing conditions for the transistor (Table 5.3) have been changed for the actual circuit because a 20 Ω resistor is in series with a drain and source. This changes the drain voltage from 1 V to 3 V. We believe this also affects the maximum gain which can be measured for the circuit.

5.5 Summary

Si-micromachined, on-wafer shielded circuits have been fabricated for K-band operation and the performance in various shielding environments has been studied. The shielding cavity is a primary component in vertically integrated circuits and its effect on the performance of these circuits has been analyzed. Dielectric shields outperform metal shields with continuous ground planes in loss and cross coupling. Active devices can be flip-chip mounted onto a Si substrate to create low-cost alternatives to MMICs but the parasitics of the solder bumps and the substrate can reduce the expected performance of a large size circuit. Alternatives to reducing line attenuation are presented in Appendix A.

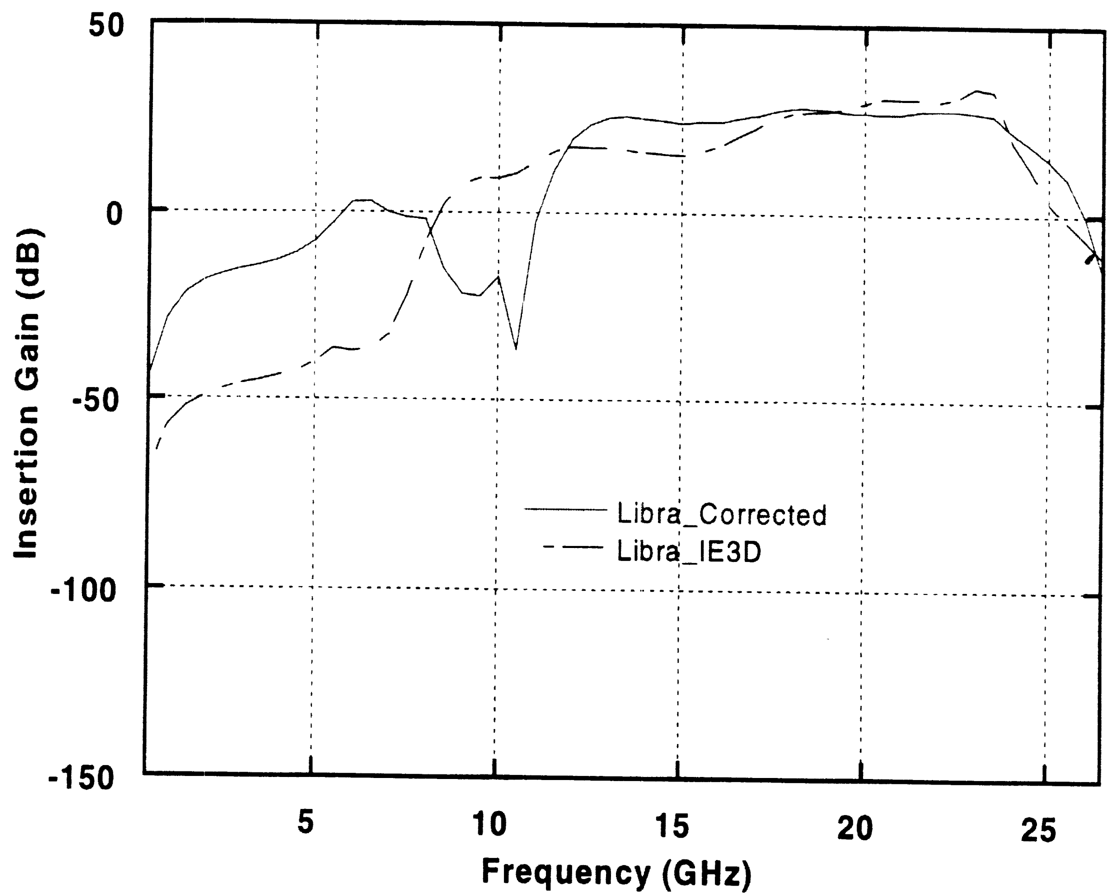


Fig. 5.30: Comparison of insertion gain for Libra_corrected and Libra_IE3D simulations

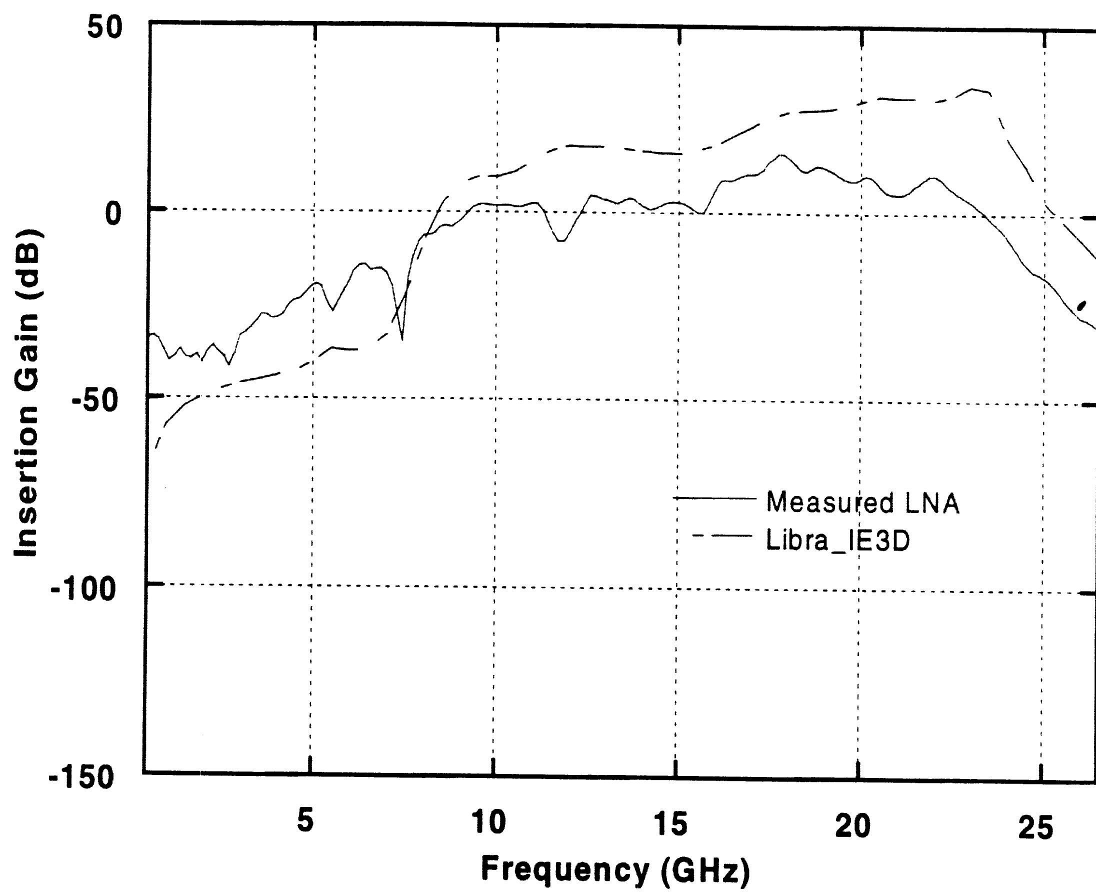


Fig. 5.31: Comparison of measured LNA performance with Libra_IE3D simulation.

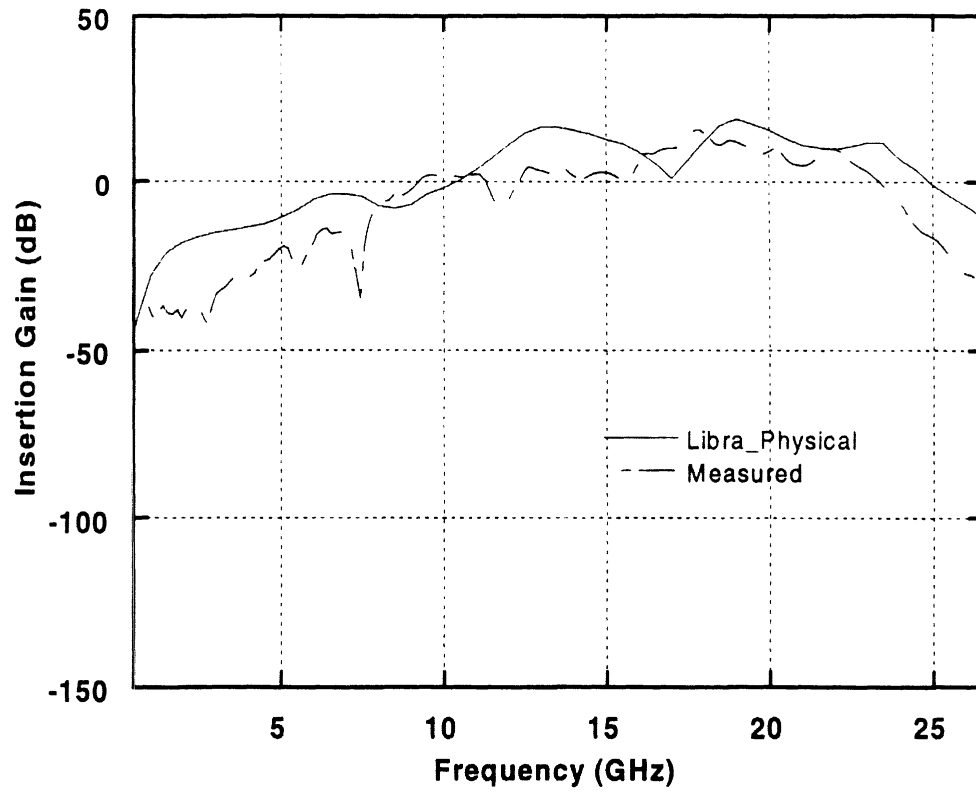


Fig. 5.32: Comparison of measured LNA with Libra_Physical simulation.

CHAPTER VI

PACKAGING FOR THREE-DIMENSIONAL INTEGRATION

6.1 Introduction

In order to develop high-frequency solid-state transmitters with moderate output power levels, multiple transistors and power combining techniques have been proposed. There are two types of combining techniques, commonly used, spatial combining and circuit combining methods. With the desire to reduce front-end size and volume, it is necessary to develop miniaturized three-dimensional transmitter systems which use planar circuits for power combining. Not only does circuit power combining offer size reductions and more flexibility in system design, but it provides more ability to obtain uniform amplitude and phase at each element [82]. However, the loss found in combining stages and sensitivity to matching networks are two important factors which have led to designs using other combining methods [83].

This research focuses on the development of a conformally packaged distribution network to be used in a three-dimensional (3-D) planar power cube linear array transmit tile module (Fig.6.1) appropriate for spatial power combining. We seek to reduce size and volume using this method and minimize loss by integrating on-wafer packaging while developing the 3-D structure.

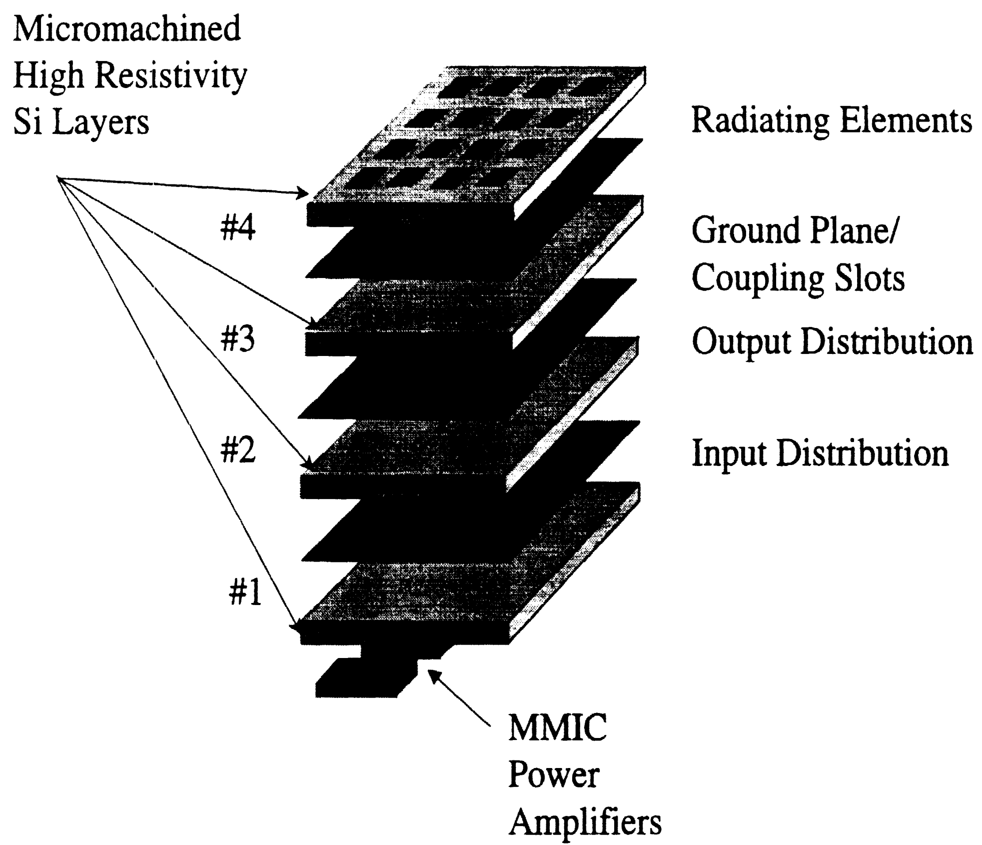


Fig. 6.1: Conceptual 3-D view of the W-Band power cube showing the micromachined wafers and metal layers.

The power cube is made of separate Si wafers each (Fig.6.1) one responsible for separate functions as listed in Table 6.1 The W-Band signal is amplified by four MMICs flip chip bonded at the lower part of the vertical structure and then distributed vertically to 16 radiating elements via four 1 x 4 distribution networks using novel vertical interconnects and low loss CPW-to-microstrip transitions (Fig.6.2). Each microstrip antenna element is 750 μm x 750 μm and separated 850 μm from an adjacent one. The total area available for distributing power to the antenna feed layer is 6 mm x 6 mm. For this reason high performance FGC lines are used to develop the network. Airbridges have been included to suppress unwanted mode excitation at discontinuities [84]. To preserve the integrity of the airbridges when bonding layers, micromachined packages are monolithically developed along with the circuits.

Layer	Si	Metal
1	Heat sink/MMIC access	Input distribution
2	Si micromachined layer/on-wafer packaging cavities	Output distribution
3	Si micromachined layer/on-wafer packaging cavities	Antenna feed
4	Antenna/micromachined layer for reduction of surface waves	Patch antenna array

Table 6.1 :Function of power cube layers.

Presented herein are details involving the design, fabrication, and testing of the output distribution network. Along with the development of the network on FGC, we investigate the effects of packaging on transmission line propagation, individual circuit, and sub-system performance.

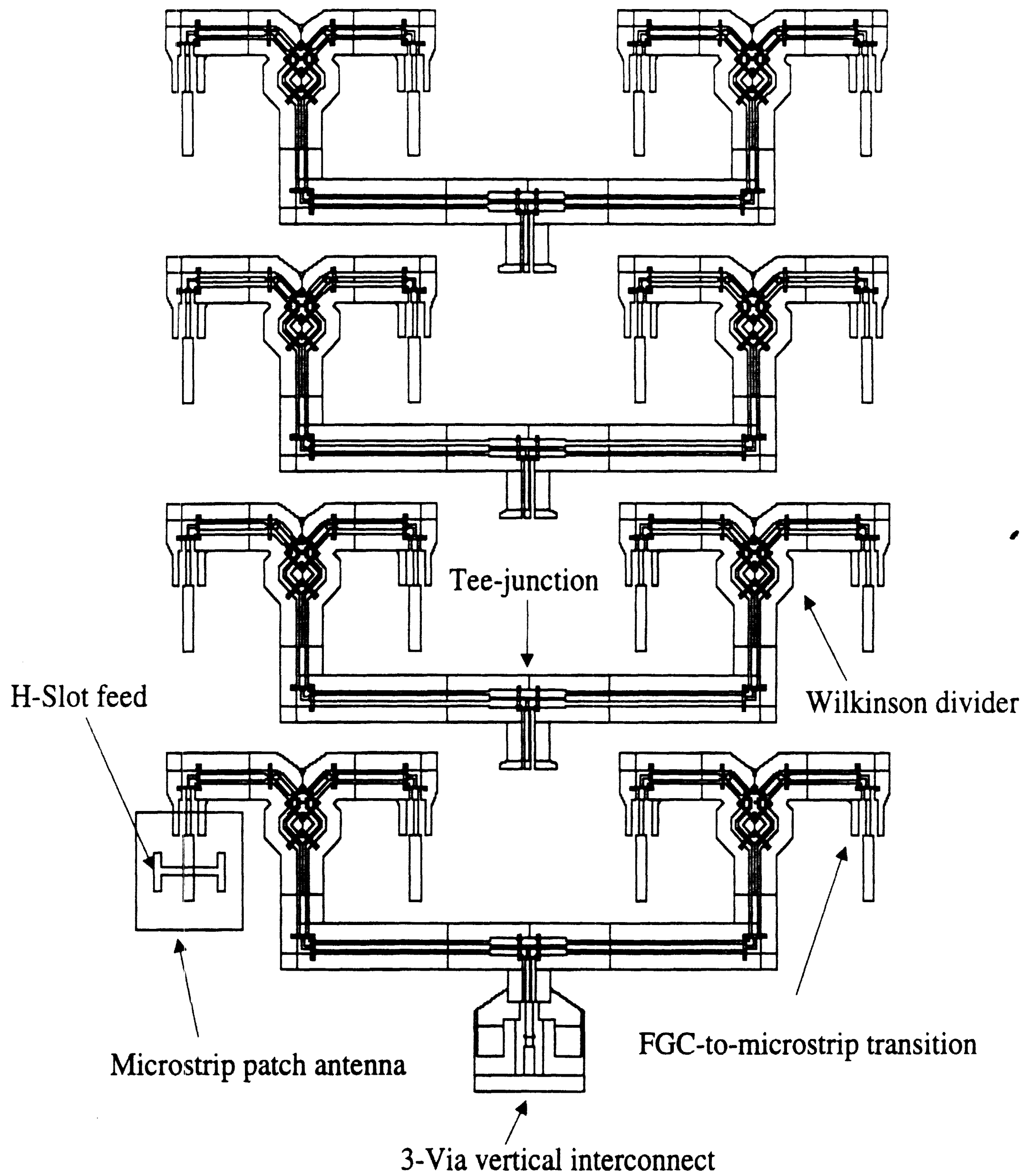


Fig. 6.2: Layout of initial design of distribution network with antenna feed and patch shown. The vertical interconnect is on the bottom side of the MMIC layer while the slots and patch antenna are on the feed and antenna layer, respectively.

To the best of my knowledge, this is the first uniplanar design of a W-Band 4, 1 x 4 distribution network. The next section presents the study of the FGC line performance in a 3-D environment.

6.2 FGC Lines in Multiconductor Environments

The FGC line dimensions are chosen using design rules established by Herrick [85]. Limited to a total line width of 300 μm, the aspect ratio necessary to realize 50 Ω is,

$$\frac{s}{s+2w} = 0.45 \tag{6.1}$$

where s is the center conductor width and w is the aperture width. This aspect ratio generates an ε_{eff} of approximately 6.34. The dimensions chosen for the line are s=40, w=24, wg=106, and t=100 μm. In order not to excite higher order modes the total line width has to be less than $\lambda_g/2$ where λ_g corresponds to a wavelength well above the maximum operating frequency,

$$2Wg + 2w + s \leq \lambda_g/2 \tag{6.2}$$

For the center frequency, f_c=94 GHz, $\lambda_g/2$= 632 μm, a value much greater than the total line width of 300 μm.

$$\lambda_g/2 = \frac{c}{2f\sqrt{\varepsilon_{eff}}} = 632\mu m$$

Because the network is placed in a 3-D environment where metal layers can be placed above and/or below the circuit metal layer, the impact of conductor metal on line characteristics must be considered.

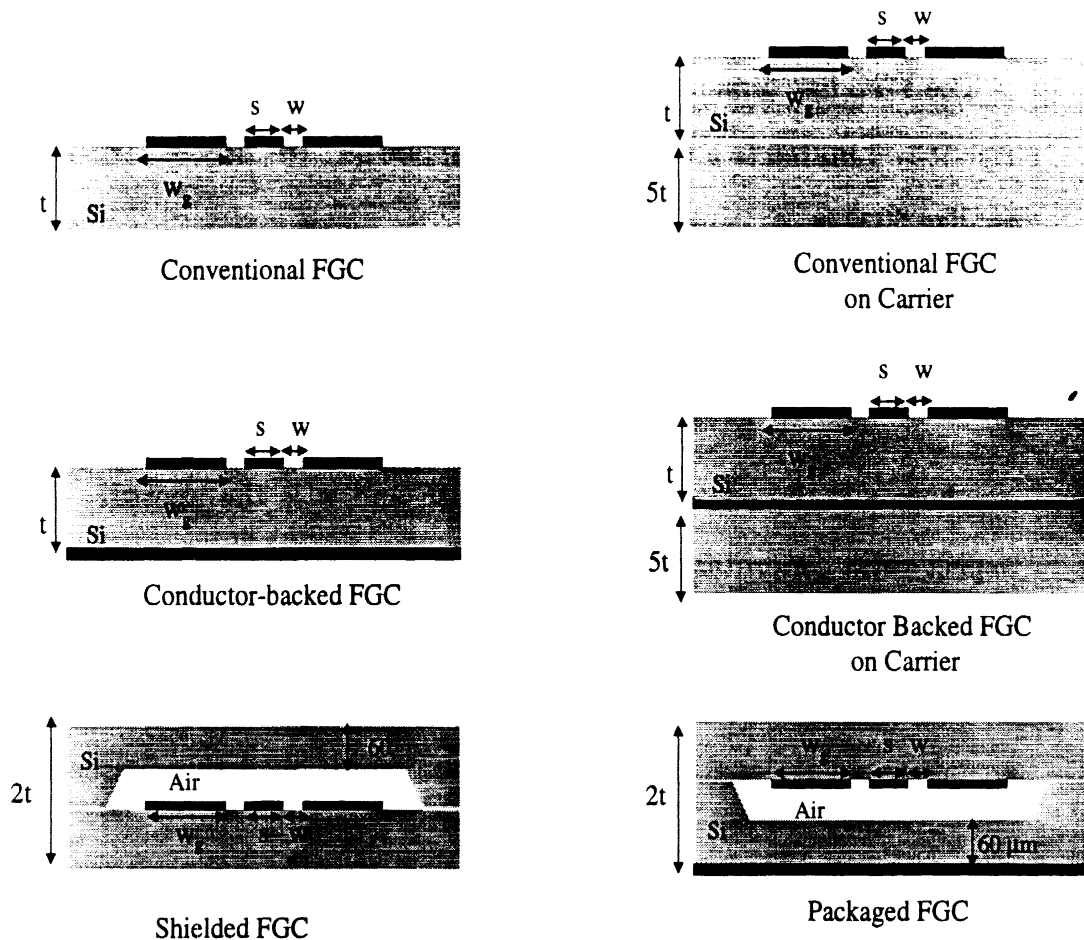


Fig. 6.3: 3-D environment geometries for the transmission lines.

Figure 6.3 shows six line architectures in which an FGC line may be placed. Conventional FGC represents a line isolated from vertical metal layers. Conductor backed FGC lines have two metal layers separated by 100 μm of pure Si. The conventional and conductor backed FGC lines are placed on a carrier to represent structures which have substrate thicknesses greater than 100 μm. Shielded FGC represents isolated lines with a micromachined cavity 40

mm away from the circuit metal. Packaged FGC lines have two metal layers separated by a 40 μm micromachined air cavity.

All data is measured using a HP8510C Network Analyzer with 100 μm-pitch GGB Picoprobes on an Alessi probe station. Attenuation and effective dielectric constant are extracted from the on-wafer calibration using Multical. Notice that the attenuation constant for lines on the left have a periodic ripple in Fig.6.4 That ripple is suppressed in thicker substrates and packaged lines.

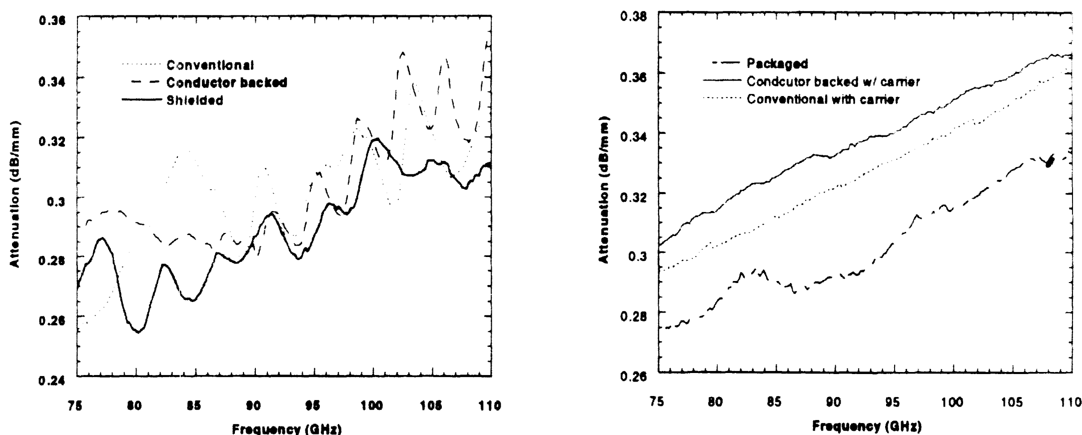


Fig. 6.4: Attenuation for line architectures.

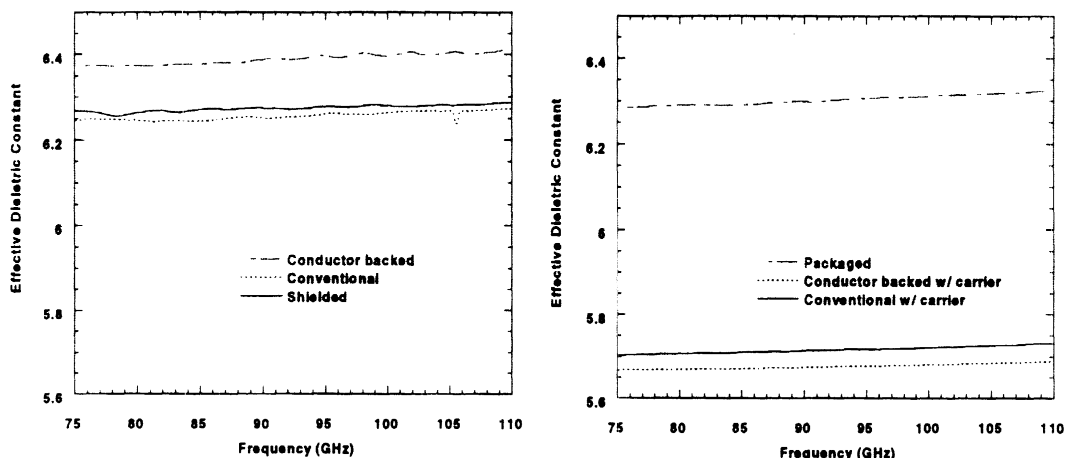


Fig. 6.5: Effective dielectric constant for line architectures.

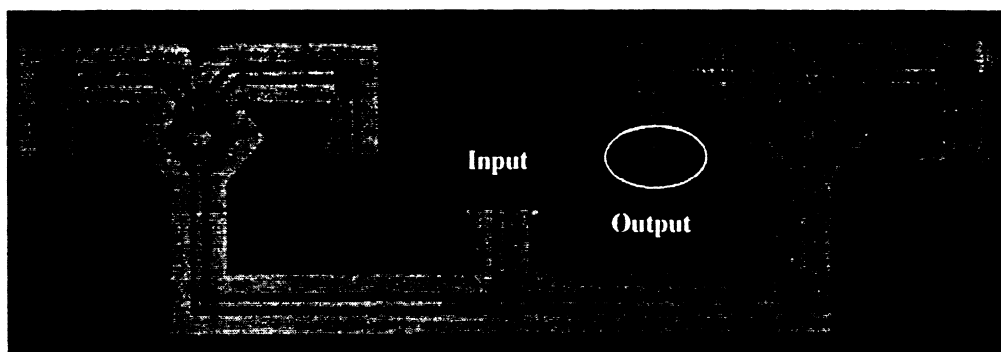
Measurements show that lines with thinner substrates have an effective dielectric constant value closer to the value predicted by Herrick (ε_{eff}=6.34). Lines with air cavities have propagation characteristics similar to the thinner substrate lines while thicker substrates have lower dielectric constant values (see Fig.6.5).

From the transmission line data, a packaged FGC line with metal conductors separated by an air/dielectric cavity has propagation and loss values which agree very well to a conventional FGC line completely isolated from metal conductors. A packaged FGC line is less sensitive to environmental conditions (metal layer location) than a conductor backed line. The next two sections focus on the design and fabrication of the distribution network.

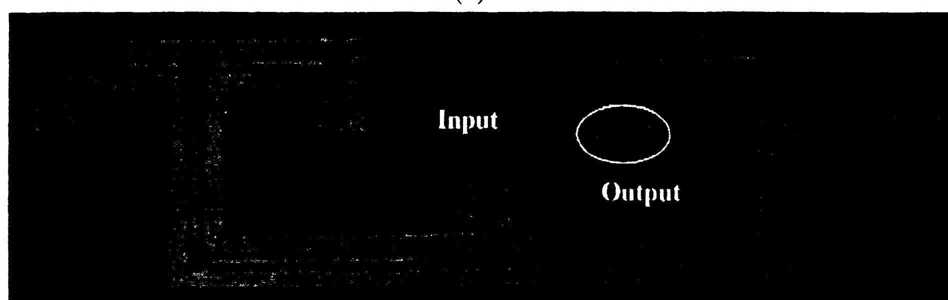
6.3 Initial Design

Two 50 Ω Wilkinson power divider geometries have been considered for use in the distribution network: a coupled CPW/slotline (Fig.6.6a) and a FGC design (Fig.6.6b). In the coupled CPW/slotline Wilkinson design, fewer discontinuities are needed and the total width is 300 μm. The CPW-based Wilkinson is larger in width by approximately 200 μm and requires five additional air-bridges to suppress higher order mode excitation at the discontinuities.

Both designs are measured in the conventional FGC with carrier environment (see Fig.6.3). Figure 6.7 shows the insertion and return loss for the network with the three output ports terminated with 50 Ω thin-film resistors. At the design frequency (94 GHz), the insertion loss is approximately -7.5 dB for both designs. Lateral/horizontal coupling for the two designs is measured in the layout and results in levels as high as -26 dB for the CPW-based design shown in Fig.6.8. The distance between adjacent networks is 1600 μm, although ground-to-ground spacing is 300 μm.

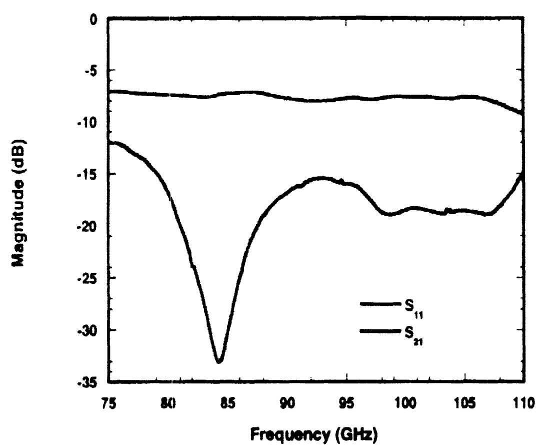


(b)

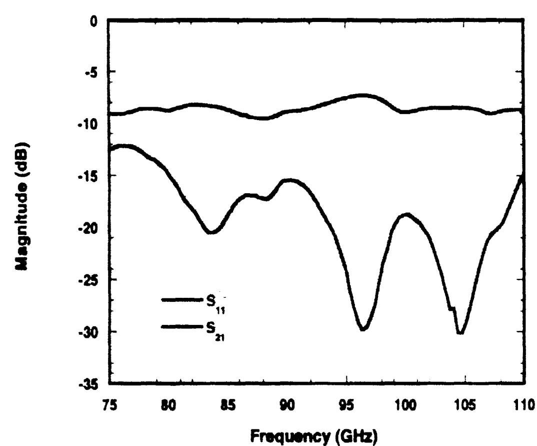


(a)

Fig. 6.6: Single 1 x 4 distribution network: (a) CPW-based Wilkinson distribution network design, (b) Coupled CPW Wilkinson distribution network design.



(a)



(b)

Fig. 6.7: Performance of first iteration distribution networks where (a) is the CPW-based design and (b) is the CPW/slotline design.

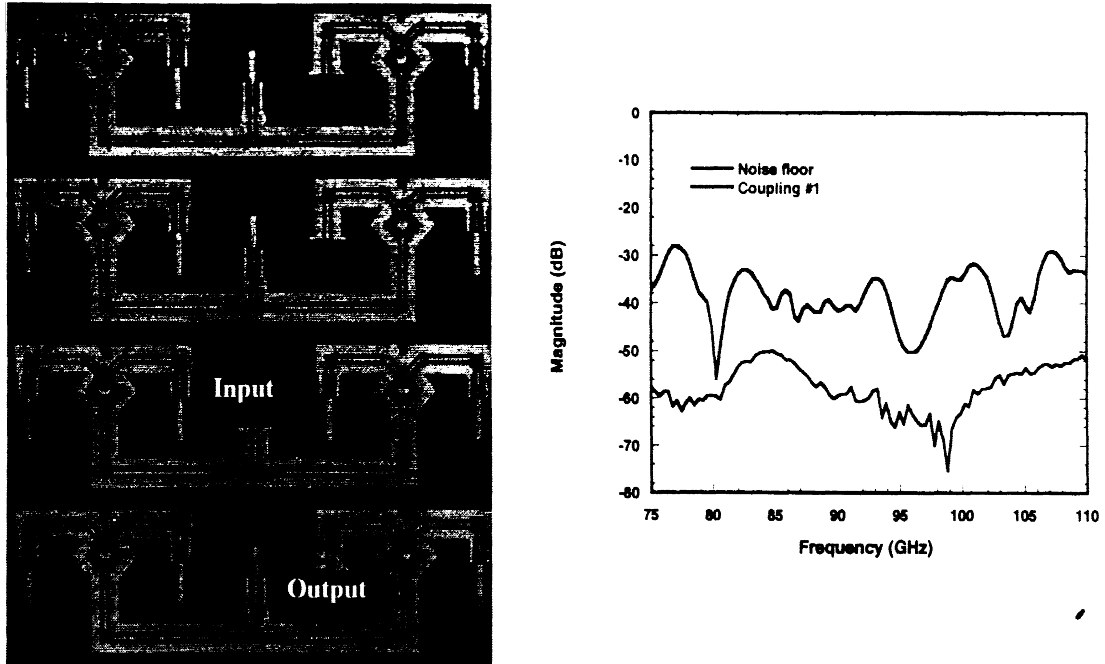


Fig. 6.8: Layout of distribution network and coupling between adjacent ground planes separated by 300 μm.

After it was proven that distribution networks with good performance could be developed for W-Band applications, a second design effort was implemented to further improve performance of the CPW-based design by shift the resonant frequency to 94 GHz.

6.4 Optimization of CPW Distribution Network

The tee junction and Wilkinson dividers are standard equal division 50 Ω designs with airbridge step compensations to improve circuit response. TaN thin-film resistors are used in the Wilkinson design (100 Ω) and 50 Ω resistors are used to terminate three of the four output ports in the distribution network.

The distribution network is fabricated on high-resistivity bare Si (>2000 Ω-cm). 700 Å of TaN (Rs=45 Ω/sq) is sputtered onto the substrate and selectively

etched using reactive ion etching for the resistor metal. 9500 Å of Au is evaporated for the circuit metal and 3 μm Au airbridges are electroplated to equalize the ground plane potential.

The shielding cavity is fabricated on a 100 μm-thick Si substrate with 8500 Å SiO_2 masking layer. Probe access windows are etched into the substrate for on-wafer measurements. The 40 μm cavity and access windows are defined using photolithography and etched using EDP water solution. The metal conductor evaporated on the cavity is 2000 Å Au. The two wafers are aligned using a bonding station with 10 ± 5 μm accuracy. Details of the process are found in Appendix F.

6.4.1 Fabrication Improvements

The two most sensitive steps of the process are the airbridges and thin-film resistors. For the FGC line dimensions used in the distribution network (w_g=106 μm, w=24 μm, s=40 μm), 50 Ω termination resistors are formed by placing two 100 Ω resistors in parallel (Fig.6.9).

The resistance, R is related to the dimensions of the resistor and sheet resistance, R_s by the following formula:

$$R = R_s\left(\frac{L}{W}\right) \tag{6.3}$$

where R_s = 50 Ω/so, W = 12 μm and L = 24 μm.

A variation in circuit metal or resistor pad dimensions can affect the return loss of a terminated line or the performance of the Wilkinson. The original resistor and circuit metal masks did not include compensations for misalign-

ment and a 3-5 μm shift can result in the structure shown in Fig.6.9a which effectively has a larger resistor pad area and therefore a smaller resistor value. By adding a 5 μm overlap on the FGC circuit metal and an edge bead removal process step [68] this problem is eliminated. When one typically spins photoresist on a sample, thick beads of resist gather near the edge of the wafer and preclude the best contact lithography step. Removing the beads of resist at the edge of the sample ensure better transfer of the resistor pattern from the mask to the wafer.

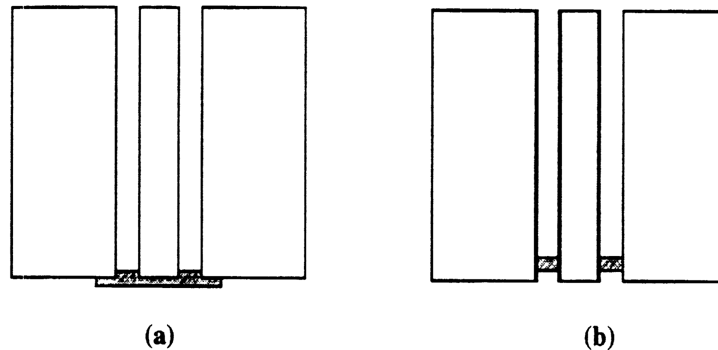


Fig. 6.9: Layout of two 100 Ω resistors in parallel to create the 50 Ω termination impedance used in the distribution network. a) Poor alignment, b) additional FGC circuit metal to keep pad dimensions. (Not drawn to scale)

In addition to improving the reliability of the resistor process, efforts are made to develop repeatable airbridges. As mentioned earlier, airbridges, due to capacitive loading, affect the attenuation and phase velocity in coplanar lines. Figure 6.10 shows a SEM of the airbridges used in the power divider.

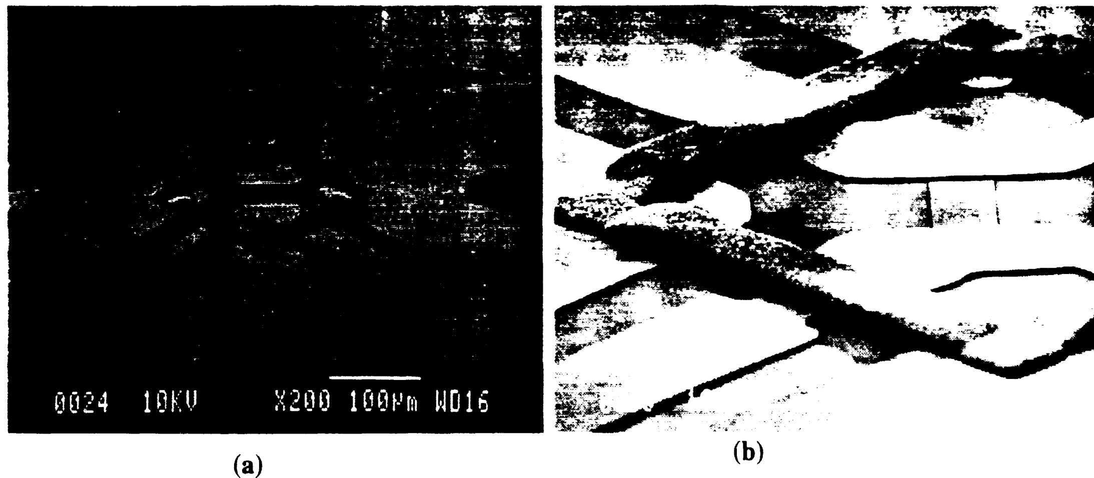


Fig. 6.10: Airbridge arrangement for CPW-based power divider.

The integrity of the airbridges is very good as seen from the SEM photo. The bridge width is designed to be 20 μm wide but measures 25 μm due to processing. In order to compensate for the additional airbridge capacitance, adjustments are made to the circuit metal mask. Given the height and width of the airbridge, the compensation width and length on the center conductor of the T-junction and right-angle bend are reduced to shift the resonance to the center frequency of 94 GHz.

In the second design iteration, the ground plane widths in the vicinity of the divider are truncated to reduce parasitic effects (Fig.6.11). Improvements in the return loss for a single divider resulted from this adjustment.

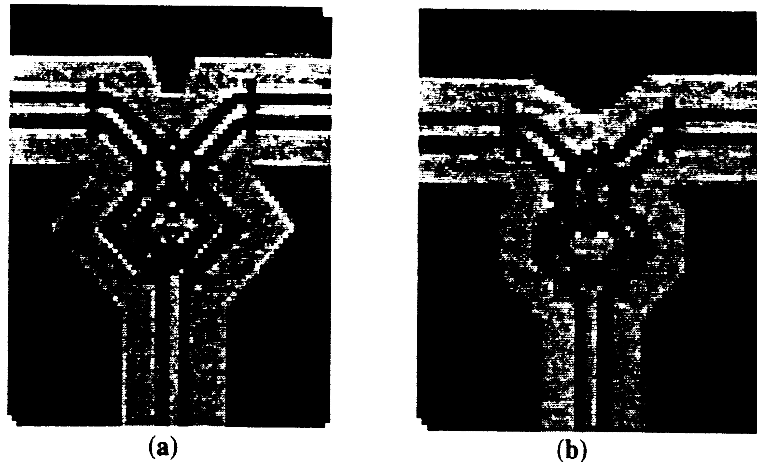
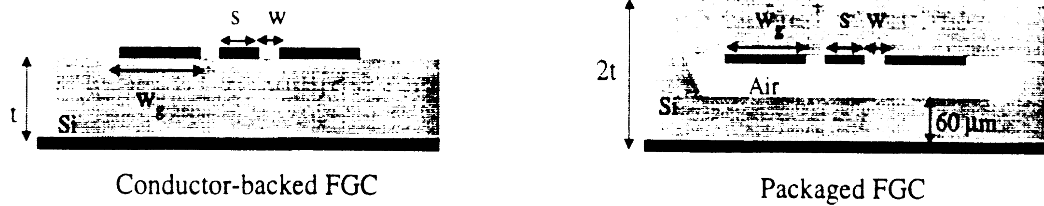


Fig. 6.11: Photograph of individual dividers. The ground planes in (a) have been truncated (b) to reduce parasitic effects in the return loss of the individual device.

6.5 Multiconductor Circuit Performance

According to Ponchak [69], the propagation characteristics of FGC lines are not subject to the substrate thickness or location of a ground plane. With that in mind the vertical layout of the distribution network or location of ground planes should not be a large concern. According to the layout shown in Figure 6.1 the power combining network distributes power to the antenna with a microstrip line through an H-shape slot which requires a continuous conductor plane. The true environment in which the distribution network resides is similar to the conductor backed architecture shown in Fig.6.12. A 40 μm cavity has been etched into the next layer Si wafer which supports the feeds to the antenna (Fig.6.12).



Conductor-backed FGC

Packaged FGC

Fig. 6.12: Cross-section of FGC lines used for distribution network design. The wafer thickness if 100 µm and the metal thickness is approximately 1 µm.

In the second design iteration of the distribution network using CPW-based Wilkinson dividers, Cr/Au metal is evaporated on the backside of the sample to simulate the conductor backed environment. Distribution network results (Fig.6.14) show the same parasitic effect demonstrated in the FGC line attenuation measurements (Fig.6.4). The continuous ground plane attracts the fields of the FGC line into the substrate and increases the parasitic capacitance of the network. Presented herein are measurements of the individual circuit components in four different line architectures. The sensitivity of the individual elements to circuit environment is clearly shown with performance degradation caused by the presence of neighboring circuit metal.

Table 6.2 lists the components which will be shown in the next several pages. The Wilkinson divider is characterized by isolation, back-to-back, and single divider response. The tee-junction is characterized by isolation, input match, and a tee with bend circuit. The right-angle bend is characterized by a double bend circuit. The tee with bend represents the input of the distribution network and the Wilkinson with bend represents the output (Fig.6.13).

Comparisons are made between the conductor backed, packaged, conventional, and shielded circuits (Fig.6.15). In the conventional architecture circuit metal lines are isolated from additional conducting layers and produce a reference measurement. The shielded architecture represents the conventional circuits in an on-wafer packaging environment without additional conducting

layers and simulates the effects of the shielding cavity on performance. The conductor backed architecture represents a circuit in a multiconductor unpackaged environment. The packaged architecture represents a circuit in a multiconductor environment with on-wafer packaging integrated into the 3-D system.

Circuit components
Divider isolation
Tee-junction isolation
Tee input match
Tee plus bend
Back-to-back dividers
Double bend
Single divider

Table 6.2 :Individual circuit components.

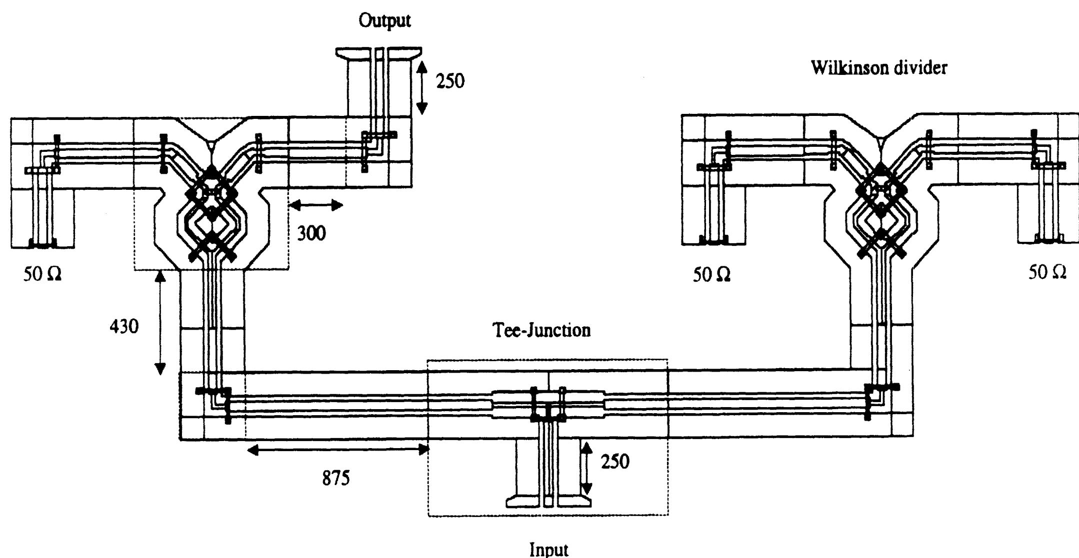


Fig. 6.13: Layout of final distribution network design.

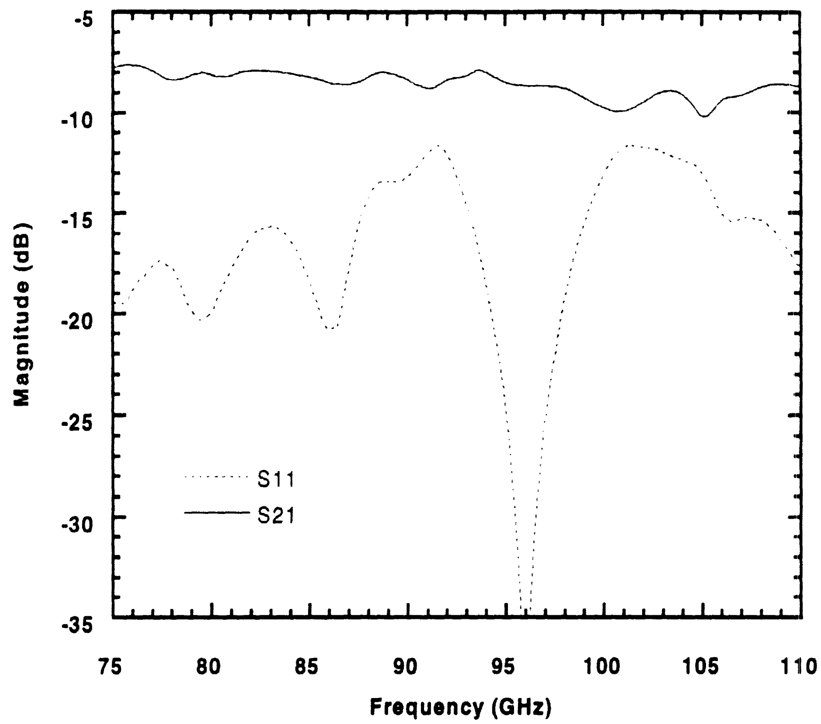


Fig. 6.14: S-Parameter measurements of the distribution network in a conductor backed environment.

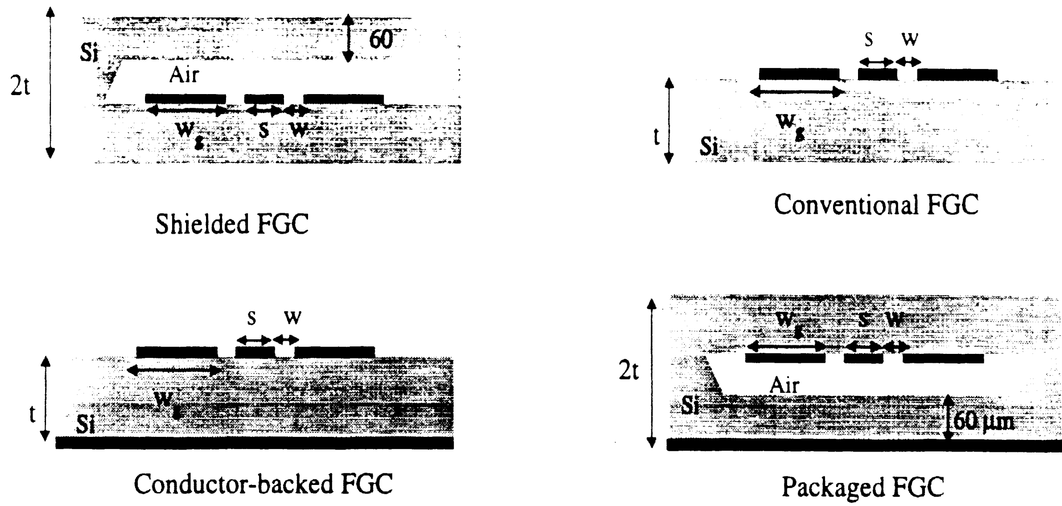


Fig. 6.15: Four architectures for individual component measurements.

Figure 6.16 shows the single divider circuit with input ports matched. The measured response for each architecture is shown in Figure 6.17. An unwanted resonance occurs at 96 GHz which increases the coupling to -10 dB in the conductor backed circuit. In the other environments the coupling is -20 dB and below for the entire bandwidth.

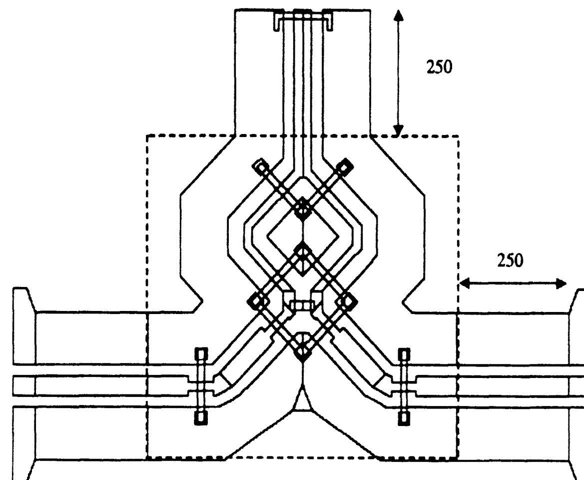


Fig. 6.16: Single divider isolation, input port matched.

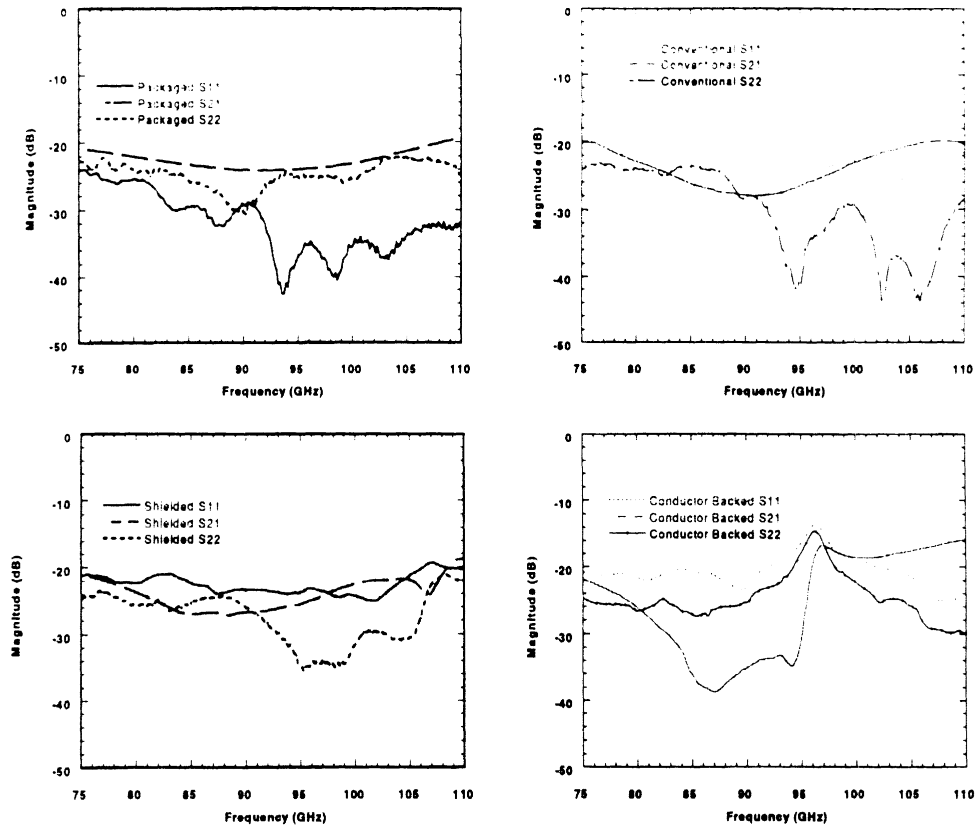


Fig. 6.17: Single divider isolation measurements for four architectures.

Figure 6.18 shows the layout for the tee-junction isolation measurement. The coupling levels are consistent for each architecture although a ripple is seen in the conductor-backed circuit (Figure 6.18).

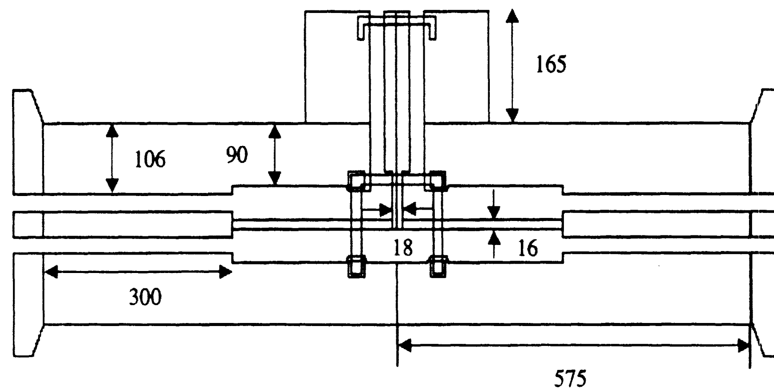


Fig. 6.18: Tee junction isolation with input port terminated.

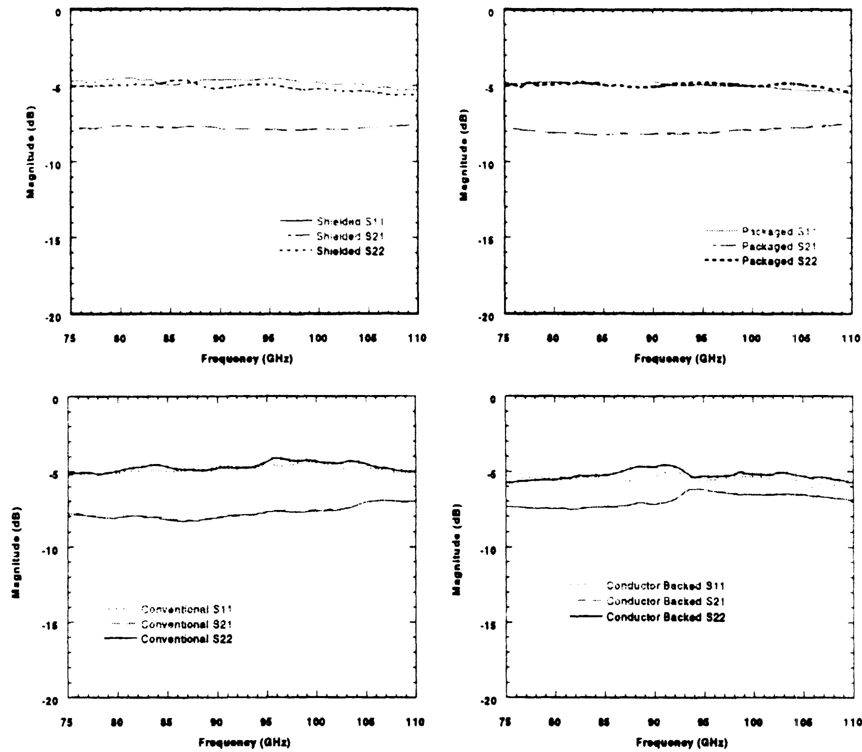


Fig. 6.19: Tee junction isolation measurements for four architectures.

The input match for the tee-junction is shown in Figure 6.20. The packaged circuit has the best performance in the frequency band. The shielded circuit measurement corresponds and the conventional circuit appears to perform best outside of the measurement spectrum. The conductor backed circuit has a high frequency resonance and is more noisy.

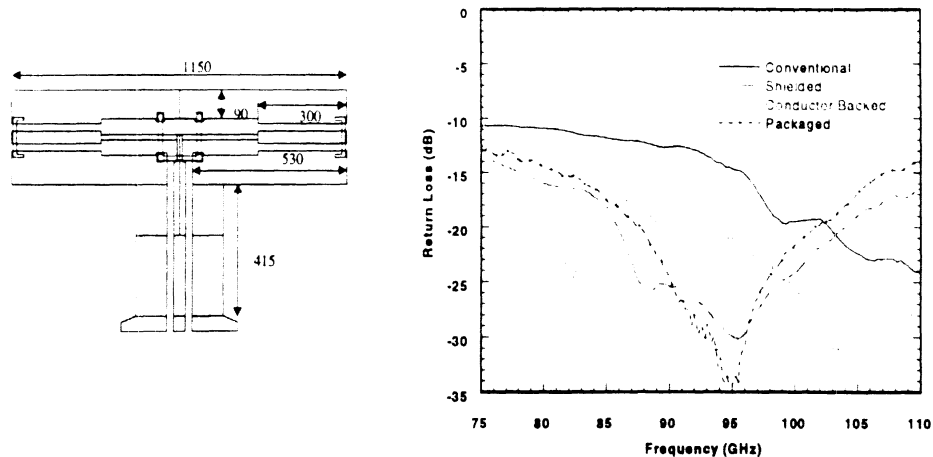


Fig. 6.20: Tee junction input match for four architectures.

Figure 6.21 shows the insertion loss for the tee with bend. The conventional circuit is best performing followed by close agreement between the packaged and shielded architectures. The ripple in the conductor backed circuit introduces an additional 2 dB of insertion loss within the operating frequency. A comparison of the two multiconductor environments clearly indicates the effectiveness of the package in removing the parasitic ripple (Figure 6.22).

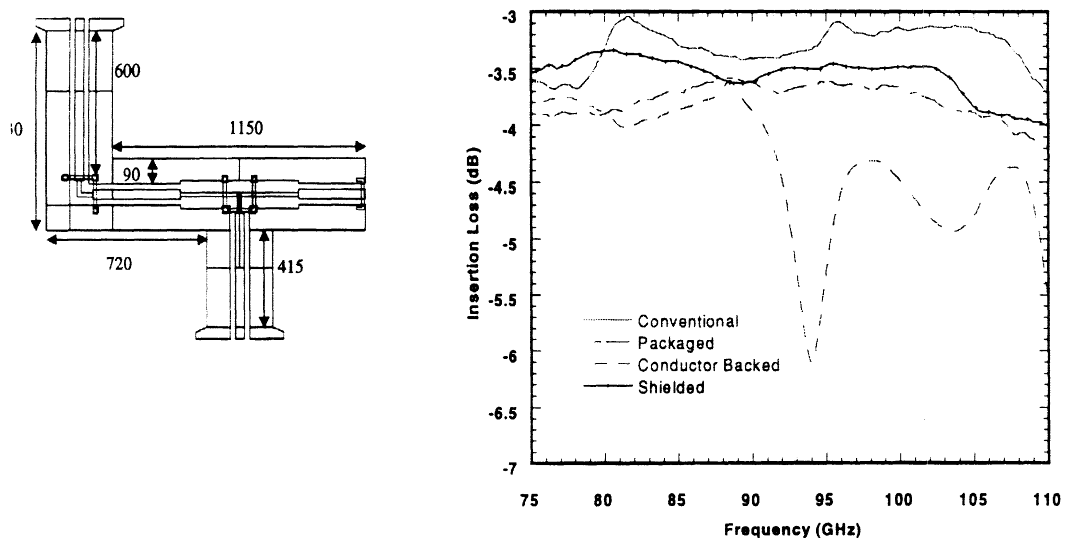


Fig. 6.21: Insertion loss for tee plus bend circuit in four architectures.

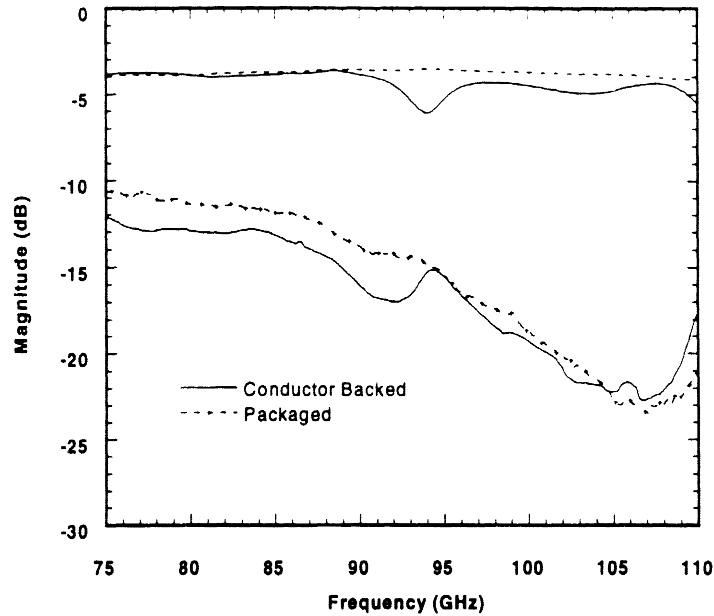


Fig. 6.22: Tee with bend S parameters for conductor backed and packaged environments.

Measurements of the back-to-back bend show similar performance with the conventional and shielded lines agreeing very well and a small amount of loss in the packaged circuit (Figure 6.23). An additional 3 dB of insertion loss is caused by the ripple in the conductor backed circuit. A frequency shift is introduced in the conductor backed-circuit in addition to the reduction in insertion loss (Figure 6.24).

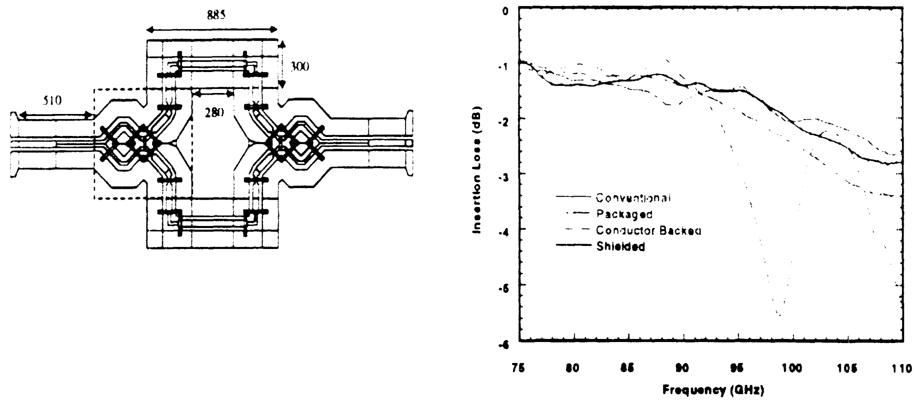


Fig. 6.23: Measured insertion loss of back-to-back dividers for four architectures.

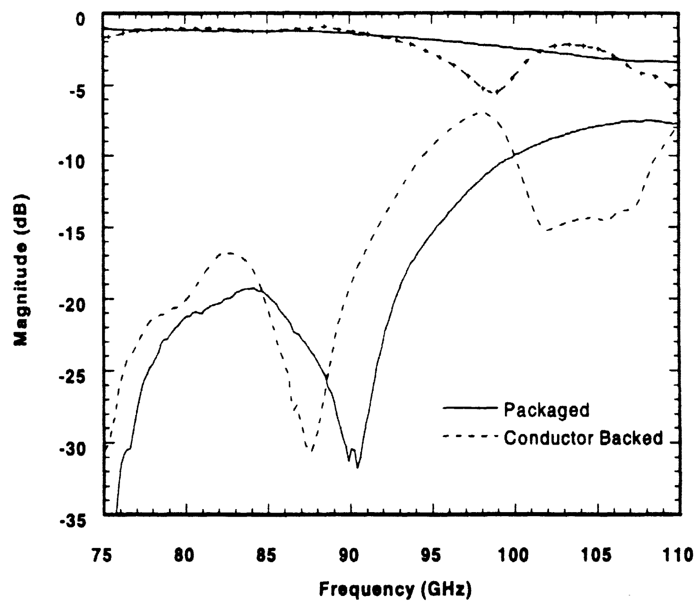


Fig. 6.24: Measured S parameters of back-to-back divider for packaged and conductor backed environments.

The double bend circuit in Figure 6.25 shows good agreement between the conventional and packaged circuits, with 0.01-0.03 dB reduction in insertion loss for the packaged bends. Additional insertion loss of 1 dB is indicated by

the conductor backed circuit. The return loss for the bends is more uniform in the packaged circuit than the conductor backed (Figure 6.26).

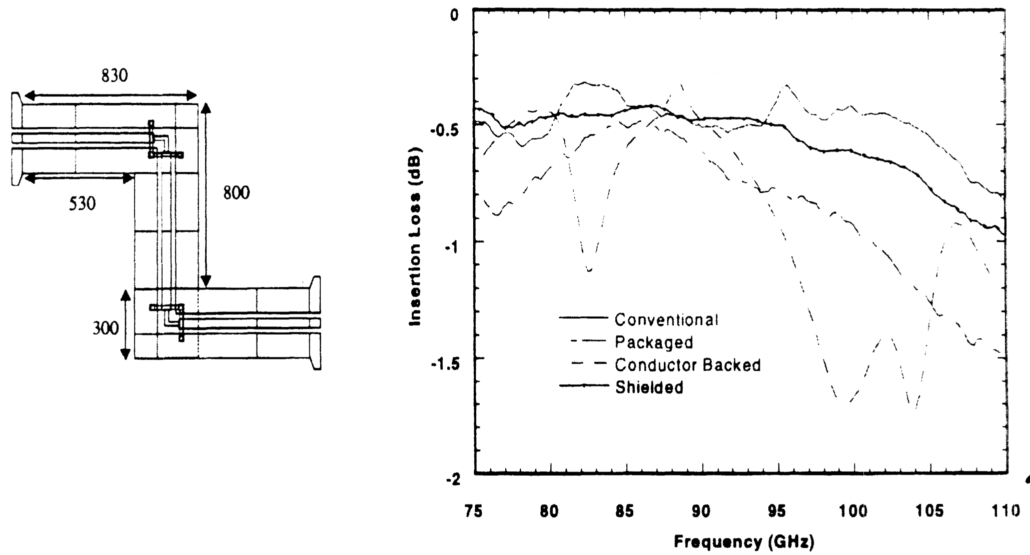


Fig. 6.25: Measured insertion loss of double bend circuit for four architectures.

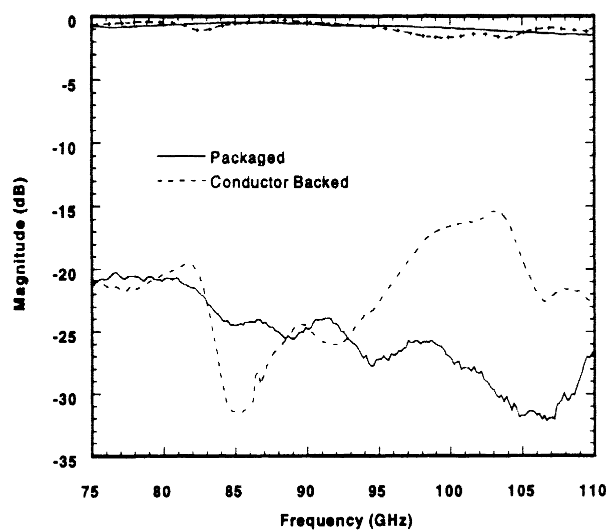


Fig. 6.26: Measured S parameters of double bend in packaged and conductor backed environments.

Single divider insertion loss is shown in Figure 6.27. The package response, although higher in insertion loss compared to the shielded and conventional circuits, is more flat and less sensitive. The ripple in the conductor backed circuit affects performance at 100 GHz with this circuit. A resonance occurs in the conductor backed circuit but the return loss is more reasonable for this component (Figure 6.28).

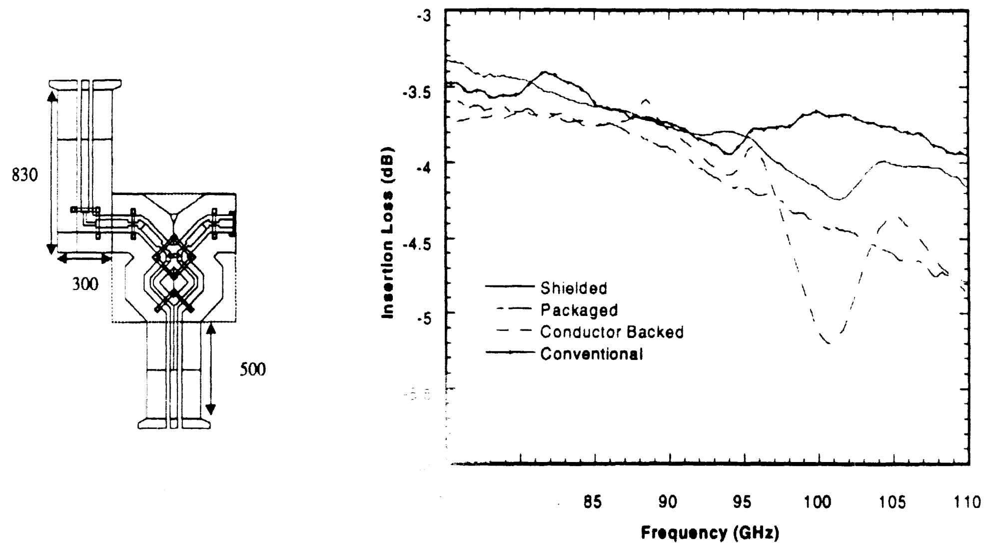


Fig. 6.27: Insertion loss of single d[illegible] [illegible]r architectures.

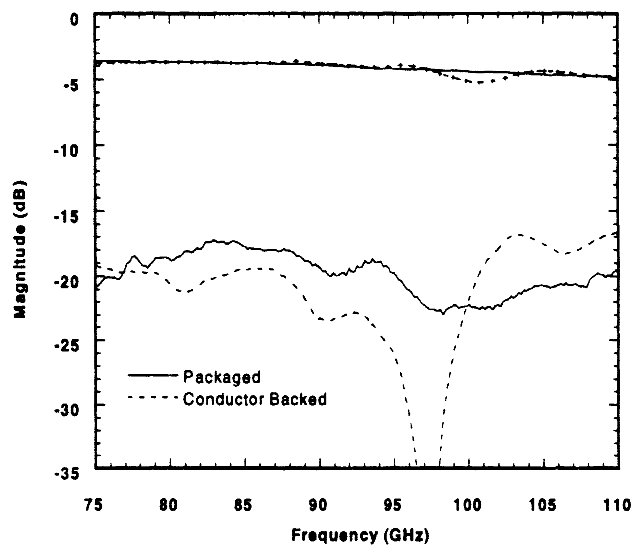


Fig. 6.28: S Parameters of single divider for packaged and conductor backed environment.

From observing the measurements, some components are more sensitive to the conductor backed environment than others. In each case the insertion loss was worsened by the presence of the ground plane. Non-packaged circuits demonstrate a varying performance due to parasitic effects that are sensitive to circuit environment. By placing an air/dielectric cavity between the two conducting planes, the parasitic effects are eliminated.

6.5.1 Impact on Distribution Network

Individual component performance is critical to feed network efficiency and warrants the extensive measurements for different line architectures. Figure 6.29 shows a comparison between two distribution networks in a conductor backed and packaged environment. The individual component parasitics combine to produce the measured response with insertion loss as low as -11 dB within the frequency of operation. The response of the packaged circuit is less dependent on frequency (smooth response) and produces an insertion loss of approximately -6.9 dB across the band of interest.

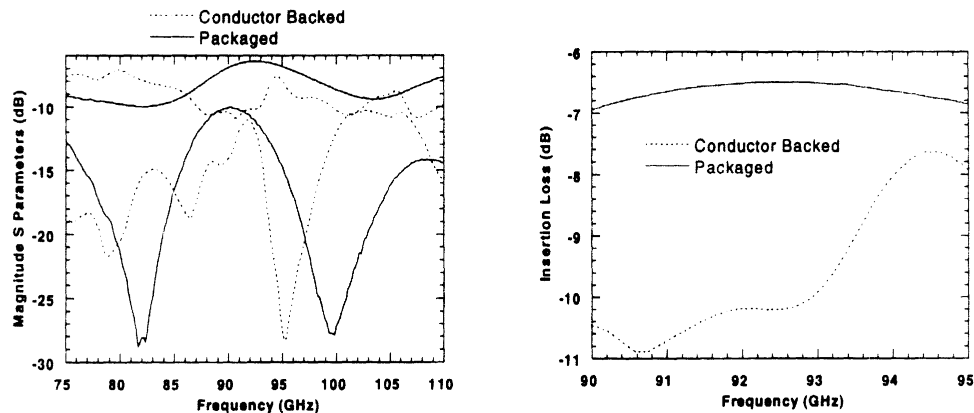


Fig. 6.29: Measured S parameters for distribution network in conductor backed and packaged environments.

The insertion loss for each output of the distribution network in the conventional architecture is shown in Figure 6.30. The loss of the circuits is -1.5 ± 0.3 dB with phase balance of ±2° from 90 to 95 GHz. The best results for the distribution network occurs when it is placed in the packaged environment. An insertion loss value of -0.7 dB can be achieved which is equivalent to approximately 85% efficiency.

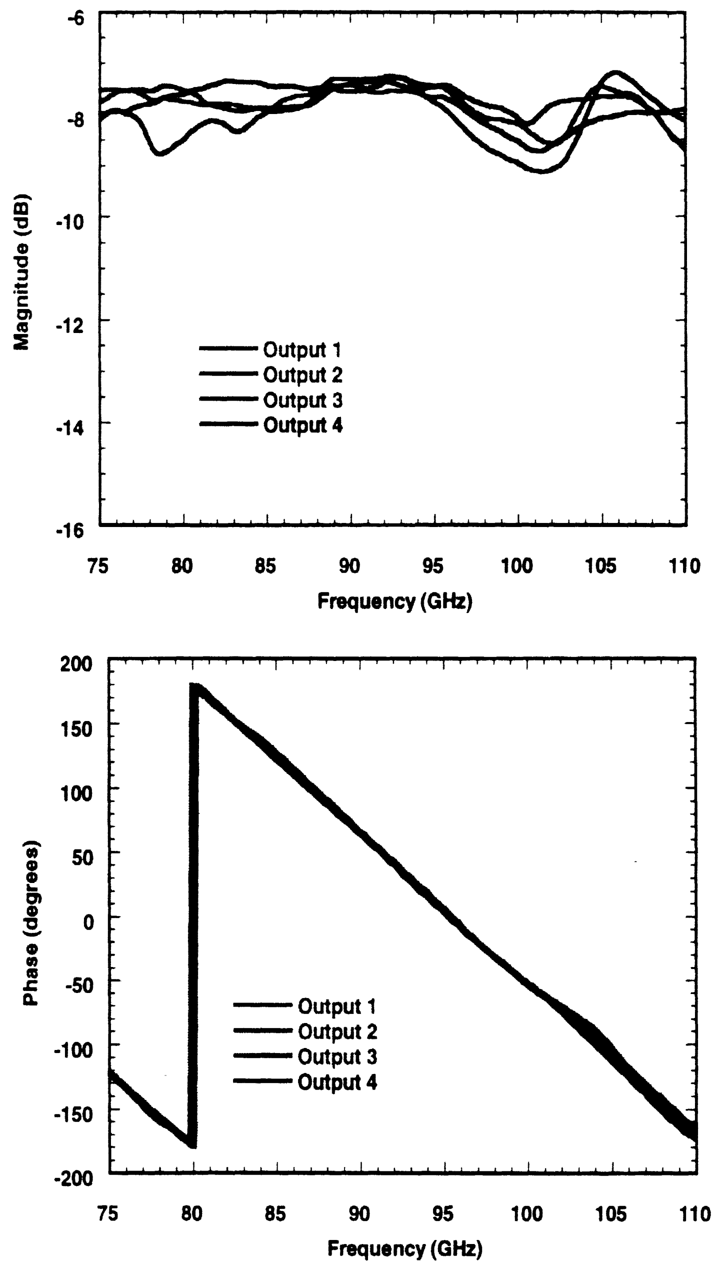


Fig. 6.30: Distribution loss for all four outputs is approximately -1.5 +/ 0.3 dB and phase balance is +/ 2 degrees.

6.5.2 Impact on Cross Coupling

Figure 6.31 shows the cross-coupling between unshielded transmission lines in the 4 x 4 array as shown in Figure 6.32. Arrangement A and B refer to nearest neighbor coupling where the lines are separated from the input by approximately 1.5 mm, but in opposite directions. In Arrangement C, the lines are separated by 2.1 mm.

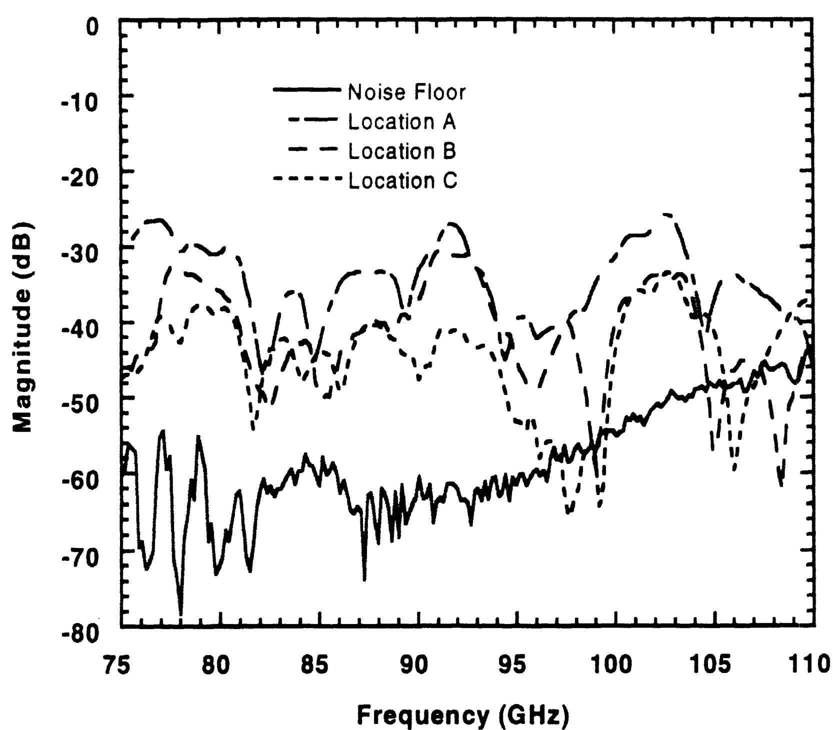


Fig. 6.31: Cross-coupling measurements of layout with metal backed structure and no upper shielding cavity.

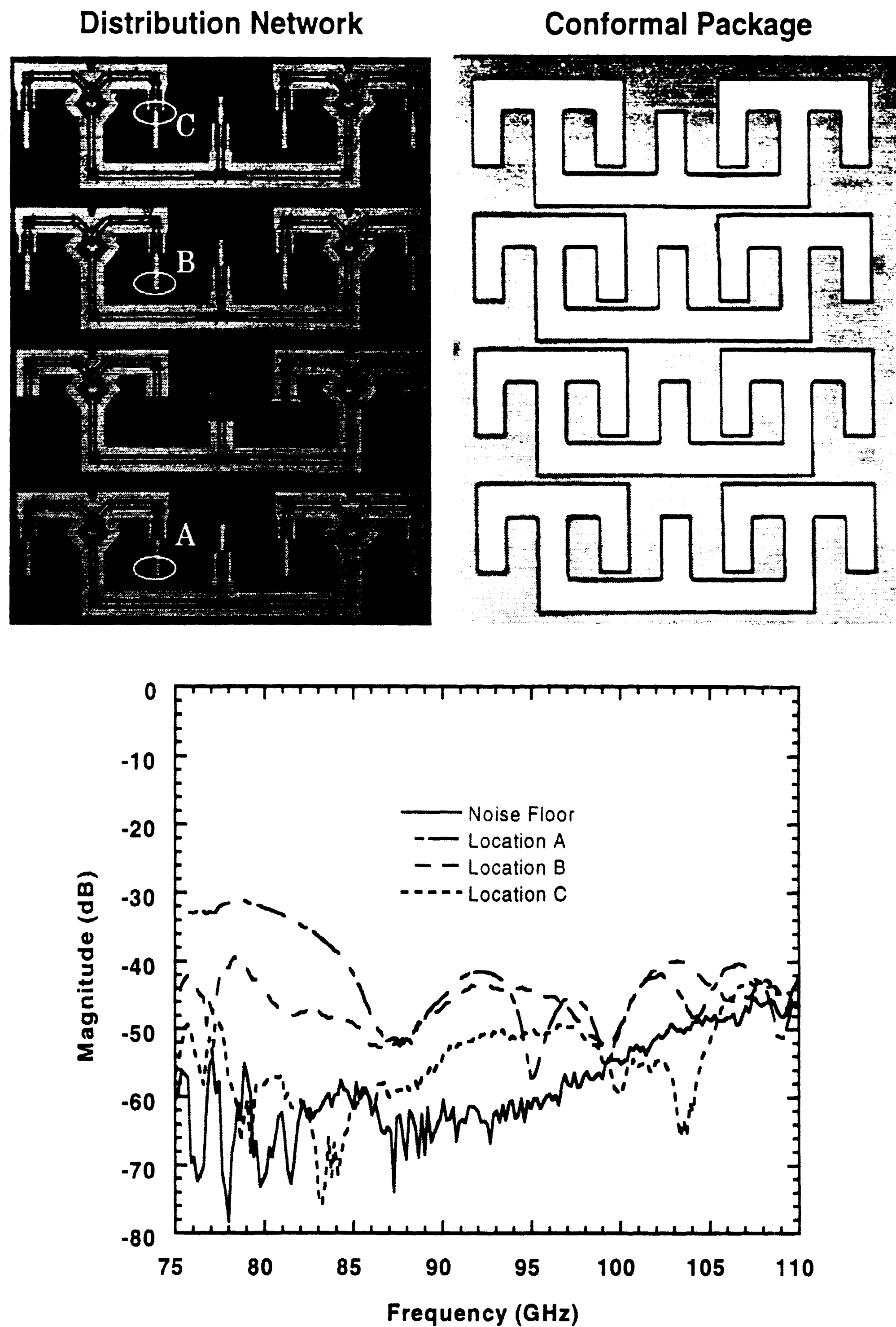


Fig. 6.32: Cross-coupling measurements of layout with upper shielding cavity and Si carrier.

6.6 Summary

The technology presented in this chapter can be used to realize high performance low loss W-Band distribution networks using FGC lines. On-wafer packaging provides excellent integration options for 3-D circuits. It is not only useful in providing high isolation between laterally coupled circuits, but it provides excellent solutions for vertical parasitic coupling.These results demonstrate the capability of this technology to provide superior integration options in addition to excellent performance compared to any other planar technology.

CHAPTER VII

CONCLUSIONS

7.1 Conclusions

A novel concept of Si micromachined electronic packages for microwave and millimeter-wave applications has been presented in this thesis. The processing techniques are compatible with standard IC technology and help realize low cost, high-precision, integrated on-wafer housings for circuits and interconnects.

Conformal shielding cavities have been fabricated around microstrip transmission lines (packaged microstrip) to provide high isolation and reduce coupling levels between neighboring lines to the system noise level. Procedures to thin a standard 500 μm Si wafer in local regions to increase high frequency microstrip performance have been developed. These custom lines compare well with conventional microstrip impedance values and show a reduction in parasitic radiation due to discontinuities.

A micromachined Ka-Band Si chip carrier for discrete component packaging has been fabricated and demonstrates superior performance in comparison to its alumina counterpart. The capability of scaling this package to W-Band or higher and using it for discrete or on-wafer applications is possible using Si micromachining techniques. Batch-fabrication of the Si-based package can reduce production costly by as much as 30 times the current amount.

In conjunction with conformal packaging techniques, a comparative study of on-wafer packaging with metal and dielectric shields has been presented. The performance of lines and circuits is compared and indicates that dielectric shielding is sufficient for FGC based circuits. The integration of on-wafer packaging with another enabling technology, flip-chip bonding has been demonstrated in the realization of a 3-stage low noise amplifier circuit. Measurements show that additional FGC line loss caused by the masking dielectric can significantly reduce the expected performance and should be taken into account during the circuit design when a large substrate area is employed.

Finally on-wafer packaging has been extended to three-dimensional integration. An extensive study of FGC line performance as a circuit is placed in multiconductor packaging environments is presented. Novel micromachining techniques have been presented to reduce parasitic vertical coupling affects caused by metal layers. The success of this technique is demonstrated in the performance of a complex distribution network for a Si micromachined W-Band linear transmitter tile array.

7.2 Recommendations

High density circuits and multi-level integration is an important area of research which will greatly benefit from the packaging technology developed within this research. The work presented has been very useful in advancing the RF Si micromachining technology. Fabrication techniques for vertical integration are currently underway in order to make on-wafer packaging a real option for high performing 3-D systems. No standard bonding process exists for this technology and it must be put in place to realize the proposed vertically stacked structures.

More characterization of the mechanical and thermal strength of the packaged circuits should be investigated to give a better comparison to the currently available technologies.

It has been shown in Chapter 6 that coupling (vertical and horizontal) can have adverse affects on the performance of circuits. It is important to take advantage of simulation tools to predict coupling trends for simple lines and extend that information to circuit and system design. Figures 7.1 and 7.2 show simulated coupling responses for conventional microstrip and FGC lines. The microstrip line dimensions are obtained from the circuit in Chapter 3 and the FGC dimensions are obtained from the circuit in Chapter 5. HFSS is used to simulate the response with the layouts and methods similar to those described earlier. In Fig. 7.1, the microstrip line coupling level is fairly constant over the frequency band for edge separations up to 2.6 mm (0.42 λ_g at 20 GHz). A more pronounced reduction is observed at the higher frequency range when the lines is separated by 4.58 mm (0.75 λ_g at 20 GHz).

Coupling for the FGC lines is much lower and less sensitive to separation distance. The highest coupling occurs when the ground planes have no separation space and varies with separation distances of 0.87 mm and 1.6 mm (0.25 λ_g at 20 GHz) by as much as 20 dB at the design frequency (Fig. 7.2). Modeling of vertical coupling can be used to improve single- and multi-layer circuit and designs in multiconductor environments [86].

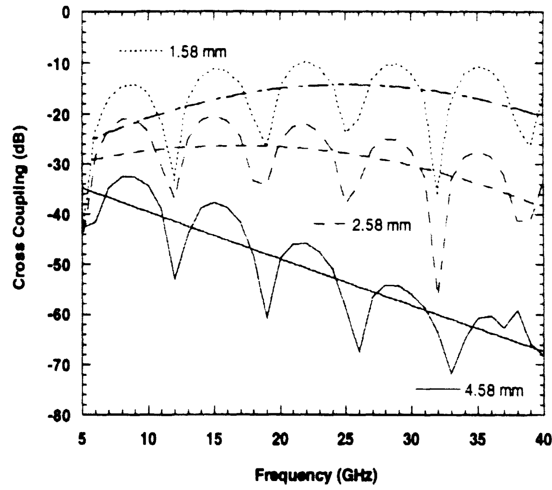


Fig. 7.1: Simulated response of coupling between 50 Ω microstrip lines separated by the distances of 1.58, 2.58, and 4.58 mm.

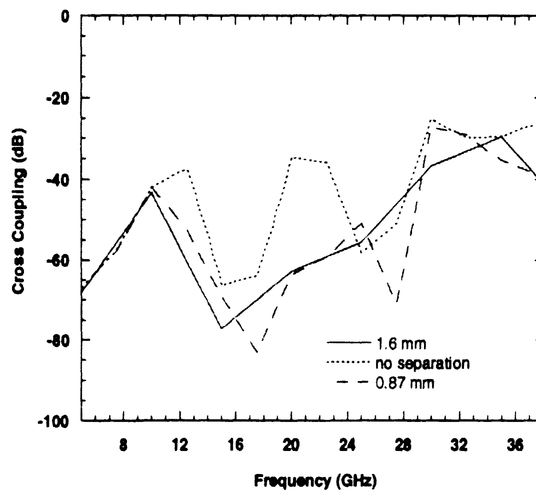


Fig. 7.2: Simulated response of coupling between 50 Ω FGC lines separated by no distance, 0.87 mm, and 1.6 mm.

APPENDICES

APPENDIX A

How MMIC Processing Affects the Attenuation of FGC Lines at W-Band

A.1 Introduction

This section presents a study of the change in loss of finite ground coplanar (FGC) lines on high resistivity Si (HRS), as a result of various MMIC processing steps. Because coplanar lines are becoming more popular for millimeter-wave applications and being used in MMIC fabrication, it is important to determine if any of these steps actually increase the attenuation of the transmission line. We present how metal thickness, high temperature exposure, and masking dielectric presence affect the attenuation of FGC lines at W-Band.

The cross section of the 50 Ω FGC line is shown in Fig. A.1 where w_g=106, w=24, s=40 μm. The height, h, of the substrate is either 500 μm or 600 μm and the skin depth of gold (Au) at f_C=94 GHz is 0.25 μm. Lines are indicated as having no dielectric (no dieletric on wafer prior to processing), a discontinuous dielectric (dielectric removed after metal deposition), or a continuous dielectric (dielectric remains after processing).

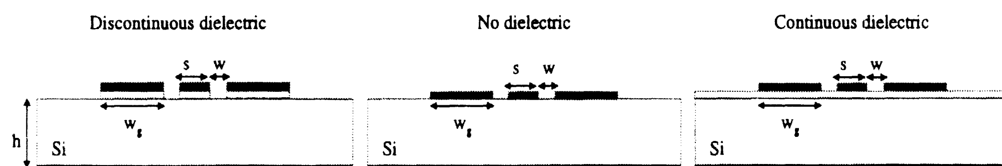


Fig. A.1: FGC lines with dimensions w_g=106, w=24, s=40 μm.

A.2 Methods

A set of TRL calibration standards is printed on two thicknesses (500 μm and 100 μm) of HRS (greater than 2000 ohm-cm). Three different metal thicknesses are printed on the 500 μm-thick wafers with an 8500Å thermally grown silicon dioxide (SiO_2) etch masking layer. Three micron lines are Au electroplated while lines with one micron or less metallization (0.95 and 0.83 μm) are evaporated using a lift-off technique. In each case, chromium (Cr) is used as the adhesion layer. The 100 μm-thick wafer had no dielectric material (Pure Si) and after processing it is attached to a full thickness (500 μm) Si carrier using photoresist. Finally, wafers are placed in an oven at 300℃ for 30 minutes to simulate a wafer-to-wafer bonding process. Table A.1 summarizes the various process environments that might impact the line attenuation.

Substrate thickness (μm)	Metal thickness (μm)	SiO_2	Heated
500	3	yes	no
500	3	no	no
500	0.95	yes	yes
500	0.95	no	yes
600	1	no	yes
600	1	no	yes
500	0.83	yes	yes
500	0.83	no	yes

Table A.1: Different processing environments for the transmission line.

A.3 Results

The standards are measured from 75-110 GHz with an HP 8510C Network Analyzer using 150 μm pitch G.G.B. Picoprobes on an Alessi Probe Station at room temperature and the attenuation is extracted using NIST's MultiCal program.

Figure A.2 shows the loss difference between 3 μm of electroplated Au, with and without SiO_2, continuous and discontinuous dielectric, respectively. Because the field lines are primarily confined within the thick metal layer, there is only a small variation (0.3 dB/mm) in attenuation when the oxide is removed.

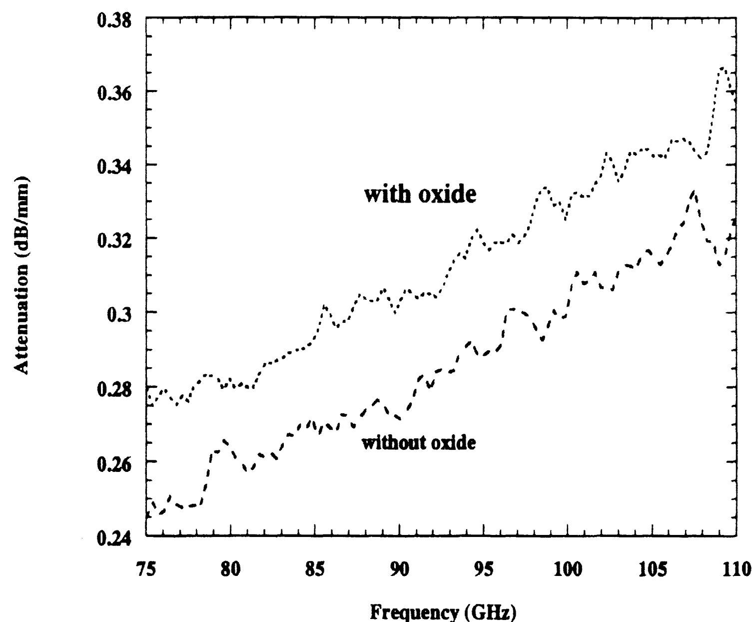


Fig. A.2: The attenuation of 3 micron thick Au electroplated lines with and without 8500 Å of SiO_2.

In the line where less metal is printed, the difference in attenuation is more pronounced and in agreement with results for 1.46 μm-thick Al lines [87]. Figure A.3 shows the loss for a 0.95 μm-thick metal layer, with and without SiO_2.

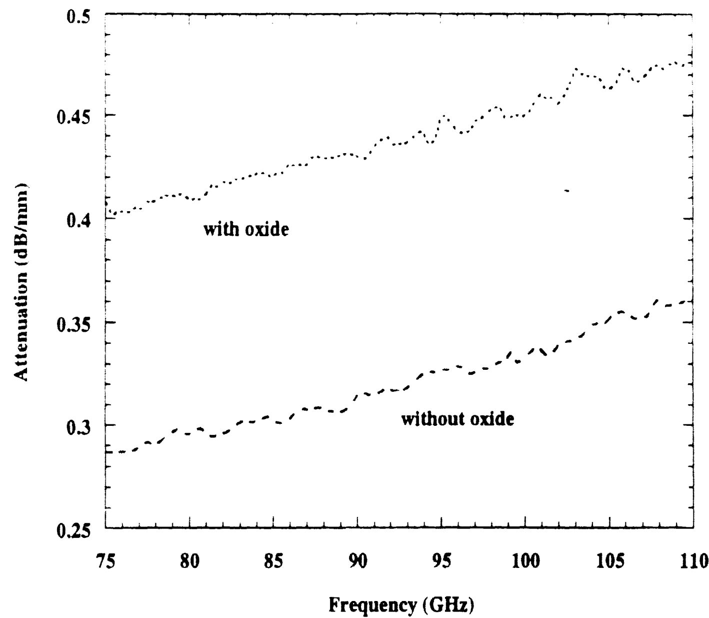


Fig. A.3: The attenuation of 0.95 micron thick Au evaporated lines with and without 8500 Å of SiO_2.

In addition to determining the effects caused by oxide removal, we show how thicker circuit metal affects the line performance at W-Band. Figure A.4 shows attenuation for varying metal thicknesses with a discontinuous dielectric. The thicker metal circuit (12 skin depths) is lowest in loss while the thinner metals have comparable values. Although the 0.83 μm (3.3 skin depths) lines have lower loss than the 0.95 μm (3.8 skin depths) line, it is believed to be due to excessive probing and the measurement error of the system.

Figure A.5 shows the attenuation for substrates before and after heating in an oven at 300℃ for 30 minutes. Measurements presented herein show that a decrease in attenuation on the order of 0.1 dB/mm occurs for heated wafers (during processing) with $Si0_2$ not yet removed, while wafers without $Si0_2$ removed have only a minor reduction in attenuation.

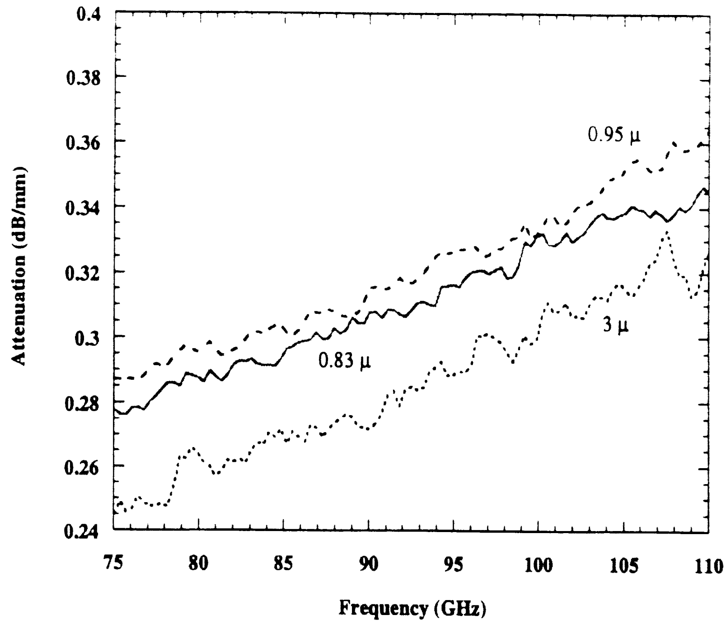


Fig. A.4: Attenuation for three different metal thicknesses on 500 μm-thick HRS.

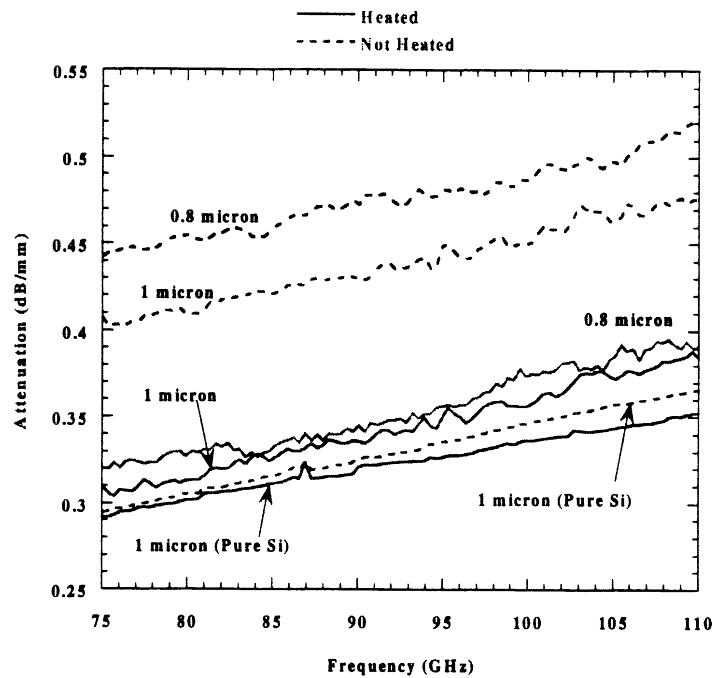


Fig. A.5: Attenuation for thicknesses 1 μm or less after being heated for 30 minutes at 300 °C. Unless noted, the lines still have a continuous dielectric.

A.4 Summary

It has been shown that certain IC processing steps can affect the attenuation of FGC lines on HRS at W-Band. Removing the masking layer after Si micromachining realizes a discontinuous dielectric between the conductor metal and substrate and reduces the attenuation by approximately 0.1 dB/mm at f_C for one micron thick lines. Placing a sample with continuous SiO_2 in a 300 °C oven for approximately 30 minutes can reduce loss by as much as 0.1 dB/mm as well. Finally, adding thicker conductor metal by electroplating, a more costly option, can reduce attenuation only by approximately 0.03 dB/mm. This measurement confirms the design rule that only 3-5 skin depths is necessary to obtain low-loss results [88]. The information presented herein can be useful to a designer when presented with the dilemma of reducing transmission line loss to obtain better circuit performance.

APPENDIX B

FABRICATION OF PACKAGED MICROSTRIP

B.1 Introduction

The fabrication steps of the K-Band conformal package for microstrip transmission lines are presented in this appendix. Two 500 μm, double-side polished Si wafers, one high resistivity for the circuit and lower cavity and another low resistivity for the upper shielding cavity are used. All processing steps except etching are conducted in a clean room environment with deionized water (DI H_20) for rinsing. At the time of this fabrication, the dielectric masking layers consisted of a membrane tri-layer ($SiO_2/Si_3N_4/SiO_2$), (8500Å/3500Å/4500Å). The photoresist used during that time, PR1400-37 manufactured by Shipley, Inc., has been discontinued. The recommended replacement is PR1827. Unless otherwise indicated, all baking is done using a hotplate.

B.2 Circuit Wafer With Lower Cavity

ALIGNMENT MARKS DEFINITION

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Spin HMDS, PR AZ5214 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose alignment mark mask for 6.5 seconds.

4. Hardbake resist in for 1 minute at 130°C.

5. Image reversal flood expose wafer for 90 seconds.

6. Develop wafer in AZ 327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

7. Inspect lithography using light filtered microscope. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

8. Evaporate Ti/Au (500Å/2000Å) on wafer.

9. Lift-off unwanted metal in warmed ACE for approximately 2 hours.

10. Rinse in IPA. Dehydrate bake at 130°C for 2 minutes.

DC CONTACT (DIELECTRIC REMOVAL) FABRICATION

To provide DC contact between the front and back side of Si wafers.

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Protect the dielectric on the backside of the wafer by spinning HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes.

3. Flip wafer over and spin HMDS and PR 1400-37 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

4. Align and expose dielectric removal mask for 15 seconds.

5. Develop wafer in MF351 for 40-70 seconds. Rinse for 2 minutes and dry with N_2.

6. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.

7. Etch 4500Å SiO_2 with BHF (etch rate 1000Å/min) for 5-6 minutes. Rinse for 3 minutes and dry with N_2.

8. Etch nitride with plasma etcher using O_2 (0.5 sccm) and CF_4 (20 sccm) at 250 mT with RF power of 100W for 8 minutes.

9. Etch SiO_2 with BHF (etch rate 1000Å/min) for 8-9 minutes. Rinse for 3 minutes and dry with N_2.

10. Remove excess resist with ACE/IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

CIRCUIT METAL FABRICATION (PLATING 3 μm)

This mask also covers the areas exposed for DC contact.

1. Descum wafer for 0.6 minutes at 80 W, of O_2 at 250 mT.

2. Evaporate Ti/Au/Ti (500Å/1000Å/500Å) seed layer on wafer.

3. Spin PR1400-37 at 3.5 krpm for 30 seconds. Softbake at 105 °C for 1 minute.

4. Align and expose circuit metal mask for 15 seconds.

5. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

6. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute. Using an ACE dipped swab, expose a small corner of Ti to provide contact when placing sample in the plating station set-up.

7. Dektak to measure height of resist. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

8. Plate circuit metal 3 μm thick. Dektak to measure height of plated Au. Continue plating until the difference between plated Au and PR height is < 5000Å.

9. Remove resist in ACE/IPA. Dry with N_2.

10. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2. Etch Au seed layer in TFA Gold etchant for 30-45 seconds. Rinse for 2 minutes and dry with N_2.Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

CAVITY DEFINITION FOR CIRCUIT WAFER

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Protect the frontside of the wafer by spinning HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes on hotplate.

3. Flip wafer over and spin HMDS and PR 1400-37 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

4. Align and expose cavity mask (1) for 15 seconds.

5. Develop wafer in MF351 for 40-70 seconds. Rinse for 2 minutes and dry with N_2.

6. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.

7. Etch SiO_2 with BHF (etch rate 1000A/min) for 5-6 minutes. Rinse for 3 minutes and dry with N_2.

8. Etch nitride with plasma etcher using O_2 (0.5 sccm) and CF_4 (20 sccm) at 250 mT with RF power of 100W for 8 minutes. The single layer of oxide will be left on the wafer to protect the locally thinned regions.

9. Remove excess resist with ACE, IPA. Dry with N_2. Remove excess solvents by baking at 130°C for 2 minutes.

THINNED REGION PROTECTION

1. Protect the frontside of the wafer by spinning HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes on hotplate.
2. Flip wafer over and spin HMDS and PR 1400-37 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.
3. Align and expose dielectric removal (1) mask for 15 seconds.
4. Develop wafer in MF351 for 40-70 seconds. Rinse for 2 minutes and dry with N_2.
5. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.
6. Etch 8500Å SiO_2 with BHF (etch rate 1000Å/min) for 8-9 minutes. Rinse for 3 minutes and dry with N_2. At this point, the shielding grooves are completely exposed while the locally thinned areas are protected with the final layer of SiO_2.

WAFER ETCHING (USING EDP)

1. Solution recipe for 1 X batch: 48mL of DI water, 48g of catechol, 0.9g of pyrazine, and 150mL of ethylenediamine. Heat the solution to 110°C and let stabilize for 30 minutes. The solution color should be a golden honey color. The etch rate is 72μm/hour.
2. Place the samples in BHF for 20 seconds to remove the native oxide layer and rinse for 3 minutes. Immediately place the samples in the solution and cover with aluminum foil. After five hours, at least 350μm

of Si should be removed in the cavity areas. Remove the samples from the solution and rinse in DI water for 5 minutes. Re-cover the solution with foil.

3. Inspect cavity depth with a microscope in a dirty (non-clean room environment) room and calculate the true etch rate. If the cavities have etched the estimated thickness, place the samples in BHF to remove the locally thinned regions.

4. Rinse for 5 minutes and immediately place the samples back in the EDP solution to etch the locally thinned regions and complete the cavity etch. For this case the desired thinned region is between 150 and 180 μm, which implies an additional etch time of 2 hours if the estimated etch rate is 72μm/hr.

5. After etching, remove the samples from the solution and rinse in DI water for 5 minutes.

6. Inspect the thinned region depth with a microscope in a dirty (non-clean room environment) room. At this point the samples are contaminated and can not be taken back into the clean room until after a 6 hour cleansing process which removes EDP residue. The total etch time for this process is in excess of 8 hours if the inspection and rinse times are included. It is important to cover the EDP with foil because O_2 exposure can alter the solution etch rate. The longer one etches, the dirtier the solution becomes and the more residue will be left on the wafer.

7. Place the samples in methanol for at least six hours. Rinse with ACE, IPA and then dry with N_2.

CAVITY METALLIZATION

Mount circuit wafer on a Si carrier with circuit metal facing down to expose

cavities for deposition.

1. Obtain Si carrier wafer (larger than circuit wafer) and small pieces of Si for standoff purposes.
2. Place small drops PR on the bottom of the standoff pieces and mount them to the carrier wafer. Hardbake at 130°C for 3 minutes. Using tweezers, try to move standoff. If secure move on, if not, add more resist and reheat.
3. Place PR on top of standoff pieces and mount inverted circuit wafer onto carrier. Hardbake at 130°C for 3 minutes. Test for movement.
4. Evaporate Ti/Al/Ti/Au (500Å/12000Å/500Å/3000Å) on backside of wafer.
5. Place sample in ACE for 20-30 minutes for dismounting. Rinse with IPA and dry with N_2.

B.3 Shielding Cavity Fabrication

ALIGNMENT MARKS

1. Spin HMDS, PR AZ5214 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.
2. Align and expose alignment mark mask for 6.5 seconds at 20 mW/cm^2.
3. Hardbake resist in for 1 minute at 130°C.
4. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.
5. Develop wafer in AZ 327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

6. Inspect lithography using light filtered microscope. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

7. Evaporate Ti/Au (500Å/2000Å) on wafer.

8. Lift-off unwanted metal in warmed ACE for approximately 2 hours.

9. Rinse in IPA. Dehydrate bake at 130°C for 2 minutes.

PROBE WINDOW DEFINITION (BACKSIDE)

1. Protect the frontside of the wafer by spinning HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes.

2. Flip wafer over and spin HMDS and PR 1400-37 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose probe window (1) mask for 15 seconds at 20 mW/cm^2 using the infrared option on the mask aligner. The marks deposited earlier will be used for alignment.

4. Develop wafer in MF351 for 40-70 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.

6. Etch SiO_2 with BHF (etch rate 1000Å/min) for 5-6 minutes. Rinse for 3 minutes and dry with N_2.

7. Etch nitride with plasma etcher using O_2 (0.5 sccm) and CF_4 (20 sccm) at 250 mT with RF power of 100W for 8 minutes.

8. Etch SiO_2 with BHF (etch rate 1000Å/min) for 7-8 minutes. Rinse for 3 minutes and dry with N_2.

9. Remove excess resist with ACE/IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

CAVITY DEFINITION (FRONTSIDE PROCESSING)

1. Protect the backside of the wafer by spinning HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes.

2. Flip wafer over and spin HMDS and PR 1400-37 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose probe window/cavity (2) mask for 15 seconds at 20 mW/cm^2.

4. Develop wafer in MF351 for 40-70 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.

6. Etch SiO_2 with BHF (etch rate 1000Å/min) for 5-6 minutes. Rinse for 3 minutes and dry with N_2.

7. Etch nitride with plasma etcher using O_2 (0.5 sccm) and CF_4 (20 sccm) at 250 mT with RF power of 100W for 8 minutes.

8. Etch SiO_2 with BHF (etch rate 1000Å/min) for 7-8 minutes. Rinse for 3 minutes and dry with N_2.

9. Remove excess resist with ACE/IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

WAFER ETCHING (USING EDP)

1. Use same solution recipe as described in earlier section.

2. Place the samples in BHF for 20 seconds to remove the native oxide layer and rinse for 3 minutes. Immediately place the samples in the solution and cover with aluminum foil. After 3.5 hours, the probe windows should be exposed and the cavities should be etched the appropriate depth of approximately 400 μm. Remove the samples from the solution and rinse in DI water for 5 minutes. Re-cover the solution with foil.

3. Inspect the cavity regions using a microscope in a dirty (non-clean room environment) room. If the cavity depth is correct and the probe windows are open, the wafer is done. At this point the samples are contaminated and can not be taken back into the clean room until after a 6 hour cleansing process which removes EDP residue.

4. Place the samples in methanol for at least six hours. Rinse with ACE, IPA and then dry with N_2.

CAVITY METALLIZATION

1. Evaporate Ti/Al/Ti/Au (500Å/12000Å/500Å/3000Å) on backside of wafer.

APPENDIX C

FABRICATION OF SILICON CHIP CARRIER

C.1 Introduction

This section contains the fabrication steps for the Ka-Band Si chip carrier and test circuit. Four wafers are used to fabricate the chip carrier. The masking dielectric on the wafers is SiO_2. Three hundred fifty micron-thick, double-side polished high resistivity Si wafers are used for the RF substrate wafer and seal frame wafer. The carrier and top cover can be fabricated using low resistivity Si. All processing steps except etching are done in a clean room environment with deionized water (DI H_20) for rinsing. Unless otherwise indicated, all baking is done using a hotplate. In order to process one on-wafer package, five individual wafers must be fabricated and then assembled. The microstrip through line wafer (for package characterization) needs circuit metal and ground plane definition in addition to alignment marks for dicing.

C.2 Fabrication Steps

WAFER PREPARATION

1. Measure the wafer thickness using Mituyoto gauge and the dielectric thickness with the SP.

2. Scribe wafer into appropriate pieces for processing.

3. Clean the samples with hydrogen peroxide: sulfuric acid (1:1.2) for 15 minutes. Rinse in DI water. Dry with nitrogen (N_2).

DC CONTACT (UPPER VIA APERTURE) FABRICATION

1. Spin HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Softbake at 105°C for 1 minute.

2. Align and expose dielectric removal mask for 15 seconds at 20 mW/ cm^2.

3. Develop wafer in MF351 for 40-70 seconds. Rinse for 2 minutes and dry with N_2.

4. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.

5. Etch SiO_2 with BHF (etch rate 1000Å/min) for 7-8 minutes. Rinse for 3 minutes and dry with N2.

6. Remove excess resist with ACE/IPA. Dry with N_2. Remove excess solvents by baking at 130°C for 2 minutes.

CIRCUIT METAL AND OVERLAY PADS

1. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

2. Evaporate Ti/Au/Ti (500Å/1000Å/500Å) on wafer.

3. Spin PR1400-37 at 3.5 krpm for 30 seconds. Softbake at 105 °C for 1 minute.

4. Align and expose circuit metal mask for 15 seconds at 20 mW/cm^2.

5. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

6. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute.

7. Dektak to measure height of resist. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

8. Plate circuit metal 3 μm-thick. Dektak to measure height of plated Au.

9. Remove resist in ACE/IPA. Dry with N_2.

10. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2. Etch Au seed layer in TFA Gold etchant for 30-45 seconds. Rinse for 2 minutes and dry with N_2. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

IC APERTURE DEFINITION

1. Protect the frontside of the wafer by spinning HMDS and PR 1400-37 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes on hotplate.

2. Flip wafer over and spin HMDS, AZ5214 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose IC aperture mask for 4 seconds at 20 mW/cm^2.

4. Hardbake resist in oven for 1 minute at 130°C.

5. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.

6. Develop wafer in AZ 327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

7. Inspect lithography using light filtered microscope. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

8. Evaporate Cr/Au (500Å/2500Å) on wafer.

9. Lift-off circuit metal in warmed ACE for approximately 2 hours.

WAFER ETCHING

1. Solution recipe for 1 X batch: 48mL of DI water, 48g of catechol, 0.9g of pyrazine, and 150mL of ethylenediamine. Heat the solution to 110°C and let stabilize for 30 minutes. The etch rate for this recipe and temperature is 72μm/hour.
2. Place the samples in BHF for 20 seconds to remove the native oxide layer and rinse for 3 minutes. Immediately place the samples in the solution and cover with aluminum foil.
3. After etching, remove the samples from the solution and rinse in DI water for 5 minutes.
4. Inspect cavity depth with a microscope in a dirty (non-clean room environment) room. At this point the samples are contaminated and can not be taken back into the clean room until after a 6 hour cleansing process which removes EDP residue.
5. Place the samples in methanol for at least six hours. Rinse with ACE, IPA and then dry with N_2.

VIA METALLIZATION

1. Obtain carrier Si wafer and standoff pieces. Spin PR AZ4620 at 2krpm for 30 seconds.
2. Place standoffs in strategic locations near the edge of where inverted circuit wafer will lay.
3. Place small drops of photoresist on standoffs and add inverted circuit. Bake carrier on hotplates of temperatures, 80 and 130°C for 2 minutes each.
4. Evaporate 1.55 mm Ti/Al/Ti/Au (0.05/1.2/0.05/0.3) for DC contact.

CARRIER AND TOP COVER METALLIZATION

1. Metallize the top cover and carrier with 1.55 μm Ti/Al/Ti/Au (0.05/1.2/ 0.05/0.3).

2. Dice the top cover wafer into 7.112 mm x 7.112 mm square pieces.

MICROSTRIP THROUGH LINE

1. The through line can be defined with two masks, one for microstrip and the other for dicing alignment marks. Three microns of electroplated Au can be deposited on the upper ground while the backside ground is formed by evaporating 1.55 μm Ti/Al/Ti/Au.

APPENDIX D

FABRICATION OF A 3-STAGE LOW NOISE AMPLIFIER CIRCUIT

D.1 Introduction

This appendix describes the process steps for the three-stage low noise amplifier circuit designed at K-Band using FGC lines. Two five hundred micron-thick, double-side polished high resistivity Si wafers are used for the circuit wafer and cavity wafer. All processing steps except etching are done in a clean room environment with deionized water (DI H_20) for rinsing. Unless otherwise indicated, all baking is done using a hotplate. In order to reduce line loss, and if no etching is to occur on a wafer, it is important to remove the masking dielectric before circuit processing.

D.2 Circuit Wafer Fabrication

WAFER PREPARATION

1. Measure the wafer thickness using Mituyoto gauge and the dielectric thickness with the SP.

2. Scribe wafer into appropriate sample sizes for processing.

3. Clean the sample with hydrogen peroxide: sulfuric acid (1:1.2) for 15 minutes. Rinse in DI water. Dry with nitrogen (N_2).

RESISTOR METAL WITH TANTALUM NITRIDE

1. Sputter tantalum nitride (TaN), titanium-tungsten (10%) (Ti/W) (3.5 minute deposition/1 minute deposition) on samples. This is equivalent to a sheet resistance R_S of approximately 33Ω/square.
2. Spin PR 1813 at 4krpm for 30 seconds. Softbake at 105 °C for 1 minute.
3. Align and expose resistor mask for 6 seconds at 20 mW/cm^2.
4. Develop wafer in MF351:DI (1:5) for 20-30 seconds only. Rinse for 2 minutes and dry with N_2.
5. Inspect lithography using light filtered microscope. Measure the width of the resistors using the micrometer in the microscope eyepiece.
6. Hard bake resist at 130 °C for 1 minute.
7. Etch TaN/TiW in RIE using SF_6 (10 sccm) and Ar_2 (5 sccm) at 10 mT with RF Power of 100mW for 6 minutes.
8. Descum in O_2 plasma asher with 150mW of RF power at 250mT for 3 minutes.
9. Strip PR and dismount samples in hot PRS2000 for 20-30 minutes. Rinse for 2 minutes and dry with N_2.
10. Clean samples in HCl:DI (1:10) for 2 minutes. Rinse for 2 minutes and dry with N_2.

CIRCUIT METAL (AU ELECTROPLATING)

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

3. Evaporate Ti/Au/Ti (500Å/1000Å/500Å) on wafer.

4. Spin PR1827 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

5. Align and expose circuit metal mask for 15 seconds at 20 mW/cm^2.

6. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

7. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute on hotplate.

8. Dektak to measure height of resist. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

9. Plate circuit metal 3 microns thick. Dektak to measure height of plated Au.

10. Remove resist in ACE/IPA. Dry with N_2.

11. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2. Etch Au seed layer in TFA Gold etchant for 30-45 seconds. Rinse for 2 minutes and dry with N_2.Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

12. Etch Ti/W in H_2O_2 for 5 minutes. Rinse for 2 minutes and dry with N_2.

NICKEL (NI) SOLDERABLE PADS (Optional)

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Spin HMDS, AZ5214 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose Ni pad mask for 4 seconds at 20 mW/cm^2.

4. Hardbake resist in oven for 1 minute at 130°C.

5. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.

6. Develop wafer in AZ 327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

7. Inspect lithography using light filtered microscope. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

8. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

9. Evaporate Ti/Ni/Au (250Å/1800Å/250Å) on wafer.

10. Lift-off metal in warmed ACE for approximately 2 hours.

POLYIMIDE SOLDER WELLS

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Spin adhesion promoter at 3.5 krpm and PI 2545 at 3.5 krpm for 30 seconds. Softbake at 140°C for 30 minutes in "dirty" oven.

3. Spin PR 1813 at 4 krpm for 30 seconds. Softbake at 105°C for 1 minute.

4. Align and expose Ni pad mask for 5 seconds at 20 mW/cm^2.

5. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2. The solution is developing the pattern and while etching the polyimide. After the first development and rinse, inspect the sample to see how much polyimide has been removed. Perform 15 second etches in developer until complete. The developer tends to overetch the polyimide if close attention is not given during this step.

6. Place sample in "dirty" oven at 150°C, increase temperature to 300°C. Hardbake polyimide at 300°C for 3 hours. Decrease temperature and take sample out when oven is at 150°C. Let sample cool for 20-30 minutes.

MIM CAPACITORS WITH ALUMINA

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.
2. Spin PR1827 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.
3. Align and expose capacitor post mask for 15 seconds at 20 mW/cm^2.
4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.
5. Inspect lithography using light filtered microscope. Hardbake at 130°C for 1 minute on hotplate.
6. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.
7. Evaporate 700Å Ti on wafer.
8. Spin AZ5214 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.
9. Align and expose capacitor span mask for 4 seconds at 20 mW/cm^2.
10. Hardbake resist for 1 minute at 130°C.
11. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.
12. Develop wafer in AZ 327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

13. Inspect lithography using light filtered microscope. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

14. Evaporate Al_2O_3/Ti/Au (1500Å/500Å/4000Å) on wafer.

15. Lift-off layers in warmed ACE overnight.

AIRBRIDGES

1. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

2. Spin HMDS and PR1827 at 3 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose airbridge post mask for 10 seconds at 20 mW/cm^2.

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Descum in O_2 plasma asher with 80mW of RF power at 250mT for 1 minute.

6. Evaporate Ti/Au/Ti (500Å/1000Å/500Å) seed layers on wafer.

7. Spin PR1827 at 3 krpm for 30 seconds. Softbake at 80°C for 20 minutes in oven.

8. Align and expose airbridge span mask for 22 seconds at 20 mW/cm^2.

9. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

10. Inspect lithography using light filtered microscope. Descum in O_2 plasma asher with 80W of RF power at 250mT for 1 minute.

11. Dektak to measure height of resist. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

12. Plate airbridges 2 to 3 microns thick. Dektak to measure height of plated Au.

13. Flood expose wafer for 3 minutes at 20 mW/cm^2. Develop resist in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

14. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2. Etch Au seed layer in TFA Gold etchant for 30-45 seconds. Rinse for 2 minutes and dry with N_2. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

15. Strip final resist layer and remove wafers from Si carrier by placing them in hot PRS2000 for 20-30 minutes. Rinse 3-5 minutes and dry with N_2.

D.3 Shielding Cavity Fabrication

ALIGNMENT MARKS

1. Spin HMDS, AZ5214 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

2. Align and expose alignment mark mask for 4 seconds at 20 mW/cm^2.

3. Hardbake resist for 1 minute at 130°C.

4. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.

5. Develop wafer in AZ 327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

6. Inspect lithography using light filtered microscope. Descum for 0.6 minutes at 80 W, of O_2 at 250 mT.

7. Evaporate Ti/Au (500Å/2000Å) on wafer.

8. Lift-off metal in warmed ACE for approximately 2 hours.

PROBE WINDOW DEFINITION (BACKSIDE)

1. Protect the backside of the wafer by spinning HMDS and PR 1827 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes.

2. Flip wafer over and spin HMDS and PR 1827 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose probe window (1) mask for 12 seconds at 20 mW/cm^2 using the infrared option on the mask aligner. The marks deposited earlier will be used for alignment.

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake resist in oven for 1 minute at 130°C.

6. Etch the dielectric (SiO_2) with buffered hydrofluoric acid (BHF) according to the thickness and etch rate of 1000Å/minute. Rinse for 2 minutes and dry with N_2.

PROBE WINDOW/CAVITY DEFINITION (FRONTSIDE)

1. Protect the backside of the wafer by spinning HMDS and PR 1827 at 3.0 krpm for 30 seconds. Hardbake at 130°C for 2 minutes.

2. Flip wafer over and spin HMDS and PR 1827 at 3.5 krpm for 30 seconds. Softbake at 105°C for 1 minute.

3. Align and expose probe window/cavity mask for 12 seconds at $20 mW/cm^2$. This mask protects the cavity, while exposing the probe windows so etching can occur from both sides of the wafer to reduce the probe window etch time by a factor of two

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake resist in oven for 1 minute at 130°C.

6. Etch the dielectric (SiO_2) with (BHF) at an etch rate of 1000Å/minute. Rinse for 2 minutes and dry with N_2.

7. Clean wafer with ACE, IPA. Dry with N_2. Dehydrate bake at 130°C for 2 minutes.

WAFER ETCHING (USING EDP)

1. Solution recipe for 1 X batch: 48mL of DI water, 48g of catechol, 0.9g of pyrazine, and 150mL of ethylenediamine. Heat the solution to 110°C and let stabilize for 30 minutes. The etch rate for this recipe and temperature is 72μm/hour.

2. Place the samples in BHF for 20 seconds to remove the native oxide layer and rinse for 3 minutes. Immediately place the samples in the solution and cover with aluminum foil.Place the samples in the solution and cover with aluminum foil. It should take no more than 45 minutes to etch the probe windows. Remove the samples from the solution and rinse in DI water for 5 minutes.

3. Place the samples in BHF at an etch rate of 1000Å/minute to expose the cavities and rinse for 5 minutes.

4. Immediately place samples back in the EDP solution and etch the desired cavity height based on the etch rate of 72μm/hour.

5. After etching, remove the samples from the solution and rinse in DI water for 5 minutes.

6. Inspect cavity depth with a microscope in a dirty (non-clean room environment) room. At this point the samples are contaminated and can not be taken back into the clean room until after a 6 hour cleansing process which removes EDP residue.

7. Place the samples in methanol for at least six hours. Rinse with ACE, IPA and then dry with N_2.

APPENDIX E

FABRICATION OF W-BAND OUTPUT DISTRIBUTION NETWORK

E.1 Introduction

The fabrication steps for the W-Band output distribution network with a conformal package are listed in this appendix. One hundred micron-thick high resistivity bare Si (HRS) wafers are used to fabricate the circuit and cavity layers. The wafers have been thinned from 500 to 100 μm with a mirror polish on both sides by Addison Engineering, Inc. [89]. All processing steps except etching are performed in a clean room environment with deionized water (DI H_20) for rinsing. Some common processing steps will be placed in this section so as not to repeat unnecessary steps.

WAFER PREPARATION

1. Measure the wafer thickness using the Mituyoto gauge and the dielectric thickness with the SP.
2. Scribe the wafer into appropriate sample sizes for processing (dependent on mask layout).
3. Clean the samples with hydrogen peroxide: sulfuric acid (1:1.2) for 15 minutes. Rinse for 3 minutes. Dry with nitrogen (N_2).

E.2 Circuit Wafer Fabrication

RESISTOR DEVELOPMENT

1. Sputter TaN/TiW (900Å≈ 2.5 minute deposition/100Å≈1 minute deposition) on samples. This is equivalent to a sheet resistance, R_S = 44 Ω/square.
2. Mount samples on Si carrier wafers for ease of handling. Spin photoresist (PR) AZ4620 at 2krpm for 30 seconds. Place sample on carrier and bake on hotplates of temperatures, 80°C and 130°C for 2 minutes each.
3. Spin PR 1813 at 4krpm for 30 seconds. Softbake at 105 °C for 1 minute.
4. Align and expose resistor mask for 6 seconds at 20 mW/cm^2.
5. Develop wafer in MF351:DI (1:5) for 20-30 seconds only. Rinse for 2 minutes and dry with N_2.
6. Inspect lithography using light filtered microscope. Measure the width of the resistors using the micrometer in the microscope eyepiece.
7. Hard bake resist at 130°C for 1 minute.
8. Etch TaN/TiW in RIE using SF_6 (10 sccm) and Ar_2 (5 sccm) at 10 mT with RF Power of 100 W for 5 minutes.
9. Remove resist with ACE, IPA. Dry with N_2.
10. Descum in O_2 plasma asher with 150 W of RF power at 250 mT for 3 minutes.
11. Strip PR and dismount samples in hot PRS2000 for 20-30 minutes. Rinse for 2 minutes and dry with N_2.
12. Clean samples in HCl:DI (1:10) for 2 minutes. Rinse for 2 minutes and dry with N_2.

CIRCUIT METAL DEPOSITION

1. Mount samples on glass slide carriers.

2. Spin HMDS and PR AZ5214 at 2.5 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose circuit metal mask for 5 seconds at 20 mW/cm^2.

4. Hardbake resist in oven for 1 minute at 130°C.

5. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.

6. Develop wafer in concentrated AZ327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

7. Inspect lithography using light filtered microscope. Measure the aspect ratio of the circuit metal. Descum in O_2 plasma asher with 80 mW of RF power at 250 mT for 1 minute.

8. Evaporate Cr/Au (500Å/9500Å) on wafer.

9. Lift-off circuit metal in warmed ACE for approximately 2 hours.

AIRBRIDGES

1. Mount samples on Si carrier wafers.

2. Spin HMDS and PR1827 at 3 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose airbridge post mask for 10 seconds at 20 mW/cm^2.

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Descum in O_2 plasma asher with 80 W of RF power at 250 mT for 1 minute.

6. Evaporate Ti/Au/Ti (500Å/1000Å/500Å) seed layers on wafer.

7. Spin PR1827 at 3 krpm for 30 seconds. Softbake at 80°C for 20 minutes in oven.

8. Align and expose airbridge span mask for 22 seconds at 20 mW/cm^2.

9. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

10. Inspect lithography using light filtered microscope. Descum in O_2 plasma asher with 80 mW of RF power at 250 mT for 1 minute.

11. Dektak to measure height of resist. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

12. Plate airbridges 2 to 3 microns thick. Dektak to measure height of plated Au.

13. Flood expose wafer for 3 minutes at 20 mW/cm^2. Develop resist in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

14. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2. Etch Au seed layer in TFA Gold etchant for 30-45 seconds (etch rate of 28Å/sec). Rinse for 2 minutes and dry with N_2. Etch Ti seed layer in HF:DI (1:10) for 3-5 seconds. Rinse for 2 minutes and dry with N_2.

15. Strip final resist layer and remove wafers from Si carrier by placing them in hot PRS2000 for 20-30 minutes. Rinse 3-5 minutes and dry with N_2.

E.2.1 Backside Metallization

1. Obtain carrier Si wafer and standoff pieces. Spin PR AZ4620 at 2 krpm for 30 seconds.

2. Place standoffs in strategic locations near the edge of the carrier wafer where the inverted circuit wafer will lie.

3. Place small amounts of resist on standoffs using swabs and mount inverted circuit wafer. Bake carrier on hotplates of temperatures, 80°C and 130°C for 2 minutes each.

4. Evaporate Cr/Au (500Å/4000Å) on backside of circuit wafer.

5. Place sample in hot PRS2000 for 20-30 minutes for dismounting. Rinse 3-5 minutes and dry with N_2.

E.3 Shielding Cavity Fabrication

ALIGNMENT MARKS (FRONTSIDE)

1. Mount samples on glass slide carriers.

2. Spin HMDS and PR AZ5214 at 2.5 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose alignment mark mask for 5 seconds at 20 mW/cm^2.

4. Hardbake resist in oven for 1 minute at 130°C.

5. Image reversal flood expose wafer for 90 seconds at 20 mW/cm^2.

6. Develop wafer in concentrated AZ327 for 30-50 seconds. Rinse for 2 minutes and dry with N_2.

7. Inspect lithography using light filtered microscope.

8. Evaporate Cr/Au (500Å/2000Å) on wafer.

9. Lift-off metal in warmed ACE for approximately 2 hours.

PROBE WINDOW DEFINITION (BACKSIDE)

1. Mount samples on glass slide carriers.

2. Spin HMDS and PR1827 at 3 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose probe window (1) mask for 12 seconds at 20 mW/cm^2 using the infrared option on the mask aligner. The marks deposited earlier will be used for alignment.

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake resist in oven for 1 minute at 130°C.

6. Etch the dielectric (SiO_2) with buffered hydrofluoric acid (BHF) according to the thickness and etch rate of 1000Å/minute. Rinse for 2 minutes and dry with N_2.

7. Place sample in hot PRS2000 for 20-30 minutes for dismounting and resist removal. Rinse 3-5 minutes and dry with N_2.

CAVITY DEFINITION (FRONTSIDE)

1. Mount samples on glass slide carriers.

2. Spin HMDS and PR1827 at 3 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose cavity mask for 12 seconds at 20 mW/cm^2. This mask exposes the cavity and probe windows from the frontside of the wafer.

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake resist in oven for 1 minute at 130°C.

6. Etch only half of the dielectric (SiO_2) thickness with buffered hydrofluoric acid (BHF) at an etch rate of 1000Å/minute. Rinse for 2 minutes and dry with N_2.

7. Place sample in hot PRS2000 for 20-30 minutes for dismounting and resist removal. Rinse 3-5 minutes and dry with N_2.

PROBE WINDOW DEFINITION (FRONTSIDE)

1. Mount samples on glass slide carriers. The alignment marks should be visible.

2. Spin HMDS and PR1827 at 3 krpm for 30 seconds. Softbake at 105°C for 1 minute on hotplate.

3. Align and expose probe window (2) mask for 12 seconds at 20mW/cm^2. This mask protects the cavity, while exposing the probe windows so etching can occur from both sides of the wafer to reduce the probe window etch time by a factor of two

4. Develop wafer in MF351:DI (1:5) for 60 seconds. Rinse for 2 minutes and dry with N_2.

5. Inspect lithography using light filtered microscope. Hardbake resist in oven for 1 minute at 130°C.

6. Etch the remaining dielectric (SiO_2) thickness in the probe windows with BHF. Rinse for 2 minutes and dry with N_2.

7. Place sample in hot PRS2000 for 20-30 minutes for dismounting and resist removal. Rinse 3-5 minutes and dry with N_2.

WAFER ETCHING (USING EDP)

1. Solution recipe for 1 X batch: 48mL of DI water, 48g of catechol, 0.9g of pyrazine, and 150mL of ethylenediamine. Heat the solution to 110°C and let stabilize for 30 minutes. The etch rate for this recipe and temperature is 72 μm/hour.

2. Place the samples in BHF for 20 seconds to remove any native oxide layer that may have formed. Rinse for 3 minutes and immediately place the samples in the solution and cover with aluminum foil. It should take no more than 45 minutes to etch the probe windows because the probe windows. Remove the samples from the solution and rinse in DI water for 5 minutes.

3. Place the samples in BHF to expose the cavities and rinse for 5 minutes.

4. Immediately place samples back in the EDP solution and etch the desired cavity height based on the etch rate of 72 μm/hour.

5. After etching, remove the samples from the solution and rinse in DI water for 5 minutes.

6. Inspect cavity depth with a microscope in a dirty (non-clean room environment) room. At this point the samples are contaminated and can not be taken back into the clean room until after a 6 hour cleansing process which removes EDP residue.

7. Place the samples in methanol for at least six hours. Rinse with ACE, IPA and then dry with N_2.

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