

**Design and Analysis of
RFIC Subharmonic Double Balanced Mixers
for Direct Conversion Applications**

by

Kiran Nimmagadda

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To my amma and nanna,
Usha Kumari and Subba Rao Nimmagadda

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CHAPTER 1

INTRODUCTION

Over the past decade there has been a major interest in the design and manufacture of silicon based integrated circuits for communications applications. These applications include wireless communication systems such as cellular telephones, cordless telephones, global positioning systems etc., and wireline communications such as analog and digital broadcast television tuners, cable telephony etc. One of the overriding concerns in the development of these radio frequency integrated circuits has been the drive towards lower cost, lower power and smaller size solutions with adequate performance. Consequently, there has been substantial research interest in migrating from the traditional super-heterodyne receiver architecture for communication applications to the direct conversion receiver architecture.

1.1 Direct Conversion Receivers

Traditionally, most wireless systems have used the superheterodyne receiver architecture (Fig. 1.1) where the incoming radio frequency (RF) signal is first downconverted to an intermediate frequency, filtered there and then downconverted to the

baseband where the information in the incoming signal is processed. This dual (or multiple) downconversion of the RF signal is very useful in improving the receiver sensitivity and the IF filtering helps in solving the image problem. The IF filters are very hard to integrate on a silicon IC in today's semiconductor technology and are a major impediment to integrating the entire receiver onto a single chip. One of the solutions is to use a direct downconversion receiver architecture (Fig. 1.2), where the incoming RF signal is downconverted directly to the baseband. This eliminates the need for the use of expensive off-chip filters, but has its own set of problems that need to be solved in order for the direct downconversion architecture to be useful in commercial applications.

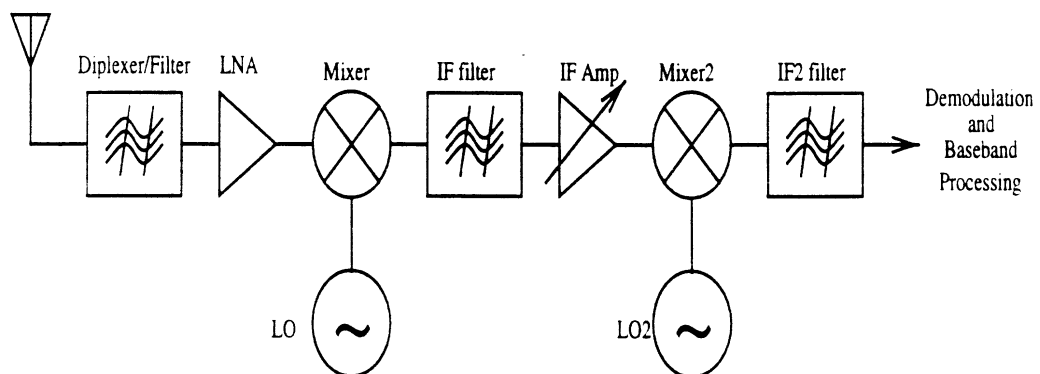


Figure 1.1: Super-heterodyne receiver architecture.

One of the main problems with the direct downconversion receiver architecture is the problem of local oscillator (LO) self mixing, resulting in a time-varying DC offset at the mixer output. As seen in Fig. 1.3, the in-band LO signal leaks and radiates into the RF front-end, and mixes back with the LO signal creating a dc offset at the mixer output. The LO signal which is reflected from the RF front-end varies with the antenna load, and therefore the DC offset is time varying. Since the IF amplifier

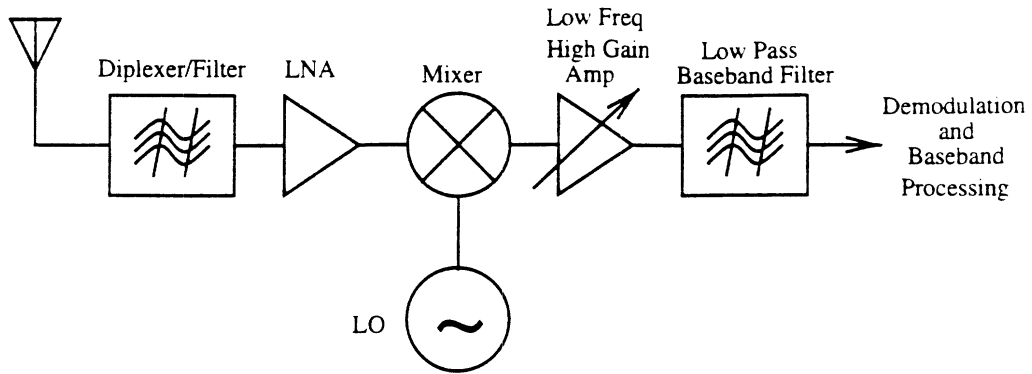


Figure 1.2: Direct conversion receiver architecture.

goes down to DC in direct-conversion receivers and has a lot of gain, the time varying DC-offset will easily saturate the IF amplifier and render the system useless.

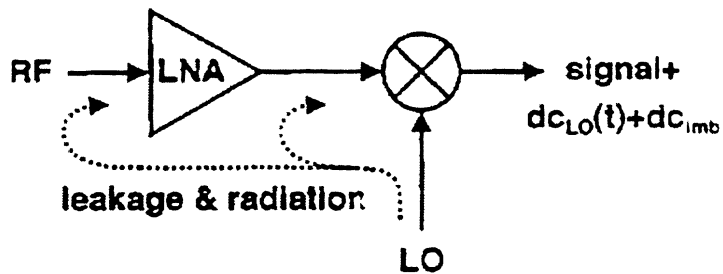


Figure 1.3: LO self mixing causes constant and time-varying dc offset.

On the other hand, if the LO signal is out-of-band and the mixing is performed with a harmonic of the LO signal (for example, $f_{IF} = f_{RF} - 2f_{LO}$ or $f_{IF} = f_{RF} - 3f_{LO}$), the result of the LO self-mixing will not be at DC and can be filtered at the IF output with a small capacitor. Subharmonic mixers accomplish this precisely. Subharmonic

mixers also allow the use of lower frequency LO signals and ease the phase noise requirement on the VCO's when compared to fundamental frequency mixing.

At the time of writing this thesis, there is quite some research being done in low-IF receivers which combine the benefits of the direct conversion architecture and the classical superheterodyne architecture [6],[7].

1.2 Thesis Overview

This thesis presents a novel subharmonic double balanced mixer (SDBM) topology that can be used in direct conversion receivers [8]. Chapter 2 presents previous research in subharmonic mixing and compares and contrasts passive mixers - which are the major form of most previous subharmonic mixer implementations, versus active mixers - which are relatively rare and a much recent form of subharmonic mixer implementations. Chapter 3 presents the crux of this thesis and includes a qualitative description of the SDBM topology, analytical expressions for DC performance, analysis for linearity and noise performance, and generalization of the second-harmonic mixer topology to n^{th} -harmonic mixer topology. The basic idea used in the SDBM is also shown to be useful for designing balanced doublers. Chapter 4 presents the design of a 1.9 GHz subharmonic mixer in SiGe bipolar technology, and presents the measurement results. The measured results of a balanced doubler are also shown. Chapter 5 presents a more linear version of the SDBM. Simulation results are presented for two different designs that improve the linearity of the mixer compared to the SDBM design presented in chapter 4. Chapter 6 includes concluding remarks and future work.

CHAPTER 2

SUBHARMONIC MIXERS

2.1 Recent research in subharmonic mixing

Subharmonic mixers in the microwave circuits field have been prevalent for a couple of decades now. It is possible to get subharmonic mixing even in the regular diode mixer by using the appropriate local oscillator (LO) filter and taking advantage of the nonlinear response of a well-pumped diode. However, in such mixers the mixing response at the fundamental frequency of the LO is greater than the mixing response at the second harmonic of the LO, and is a source of interfering signals and downconverted LO noise [9]. The fundamental mixing response is also an additional loss mechanism, since a large portion of the RF input power is converted to mixing frequencies near the LO and is radiated from the LO port. Hence, single diode mixers are rarely used in low-noise receivers.

A better way to accomplish subharmonic mixing is to use an anti-parallel diode pair (APDP) as shown in Fig. 2.1. By using the anti-parallel diode pair, one of the diodes conducts during the positive half-cycle of the LO, and the other diode conducts during the negative half-cycle of the LO signal. As a result, the conductance

waveform of the APDP will have a fundamental frequency of twice the frequency of the LO signal. By applying the RF signal to this APDP, mixing is achieved with twice the LO frequency. Several papers [10],[11] have used this technique recently for using a subharmonic mixers in receiver designs.

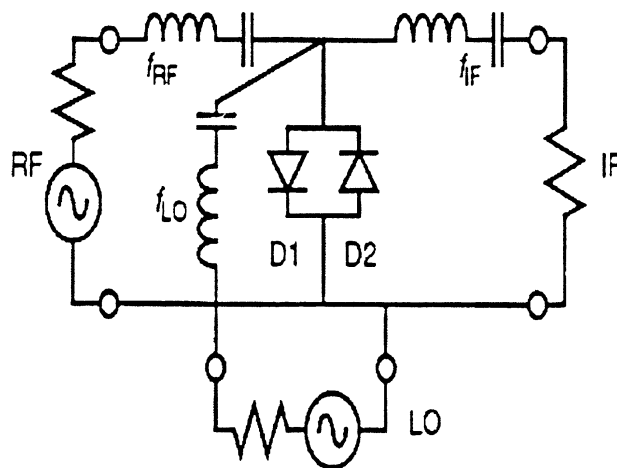


Figure 2.1: APDP structure for subharmonic mixing.

The APDP technique can be extended to diode ring mixers too. Diode ring mixers are balanced mixers since they eliminate the LO signal at the IF port without any special filters. Recent published results[12],[1],[13] use this technique to implement balanced subharmonic mixers for use in direct conversion receivers. Fig. 2.2 shows the implementation used by Matinpour et al. in [1].

All the mixers based on the APDP structure are passive mixers and just rely on the diodes to act as switches for the LO signal. Therefore, there is no amplification for the RF signal. Consequently, passive mixers (both fundamental and subharmonic) have a conversion loss from the RF port to the IF port, typically around 6 to 7 dB at 1-5 GHz. The most common active mixer is the Gilbert double balanced mixer which provides conversion gain in the mixing process. There has been some work recently

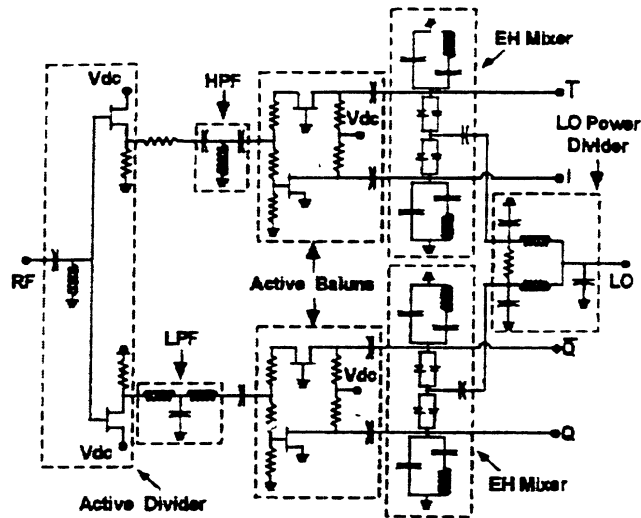


Figure 2.2: APDP structure used in recent implementations of subharmonic mixers (after [1]).

which modifies the basic Gilbert cell mixer to perform subharmonic mixing.

Yamaji et al. [2] used the emitter-coupled transistor pair (ECP) to perform harmonic mixing as shown in Fig. 2.3. The ECP has a limiting transfer characteristic with odd symmetry, and a large signal applied to the base input results in a rectangular wave at the collector output. When the RF signal is superposed with the large LO signal at the input, the output rectangular wave is pulse-width modulated by the RF signal and results in harmonic mixing. The work in [2] uses two ECP's in a balanced fashion to implement a balanced harmonic mixer to result in no LO leakage at the IF output (ideally).

Sheng et al. [3] employ a “two-level” LO switching core in place of the LO switching quad in the standard Gilbert cell mixer, as shown in Fig. 2.4. The two levels in the LO core are driven by differential LO signals which are in quadrature with respect to each other. These two levels of switching effectively double the LO frequency if the

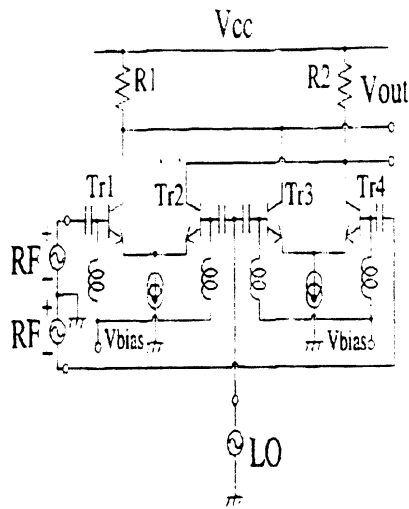


Figure 2.3: Balanced harmonic mixer using emitter coupled pairs (after [2]).

switching phases are offset by 90° .

The above idea of using the quadrature LO for subharmonic mixing is very similar to the subharmonic double balanced mixer (SDBM) presented in this thesis. The main difference is the use of a “one-level” LO switching core as shown in Fig. 2.5. By eliminating the second level in the switching core, this implementation of the mixer can be operated down to a power supply voltage of 1.5-2 V.

Lee et al. [4] extend the idea above to use a multiple phase lower frequency LO signal to accomplish harmonic mixing. They propose a multiphase reduced frequency conversion (MPRF) technique in which the effect of mixing with a single-phase high-frequency signal can be obtained by multiplying by a set of multi-phase reduced frequency signals. The 12-phase downconversion mixer used to obtain mixing with the third harmonic of the LO is shown in Fig. 2.6.

The above summary shows that subharmonic and n^{th} -harmonic mixers are an

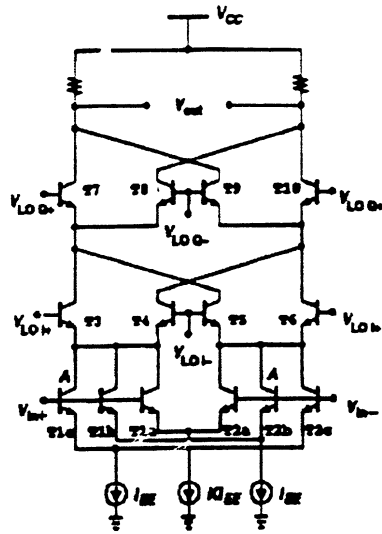


Figure 2.4: Subharmonic mixer with a two-level LO switching stage (after [3]).

active area of research for RFIC receivers, and this thesis presents a novel low-voltage implementation. It is believed that the results presented in this work are state-of-the-art and very competitive with other approaches.

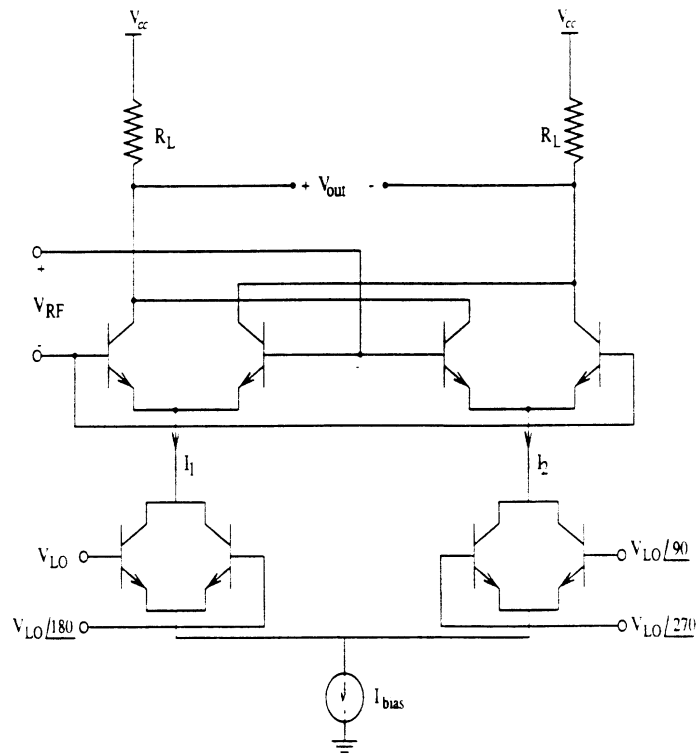


Figure 2.5: Simplified schematic of the novel Subharmonic Double-Balanced Mixer (SDBM).

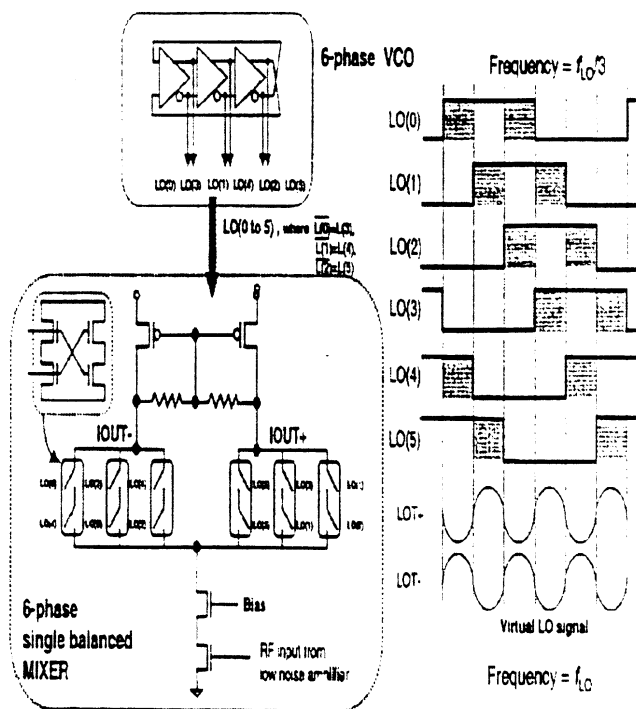


Figure 2.6: 12-phase downconversion mixer resulting in x3 subharmonic mixer (after [4]).

CHAPTER 3

SUBHARMONIC DOUBLE BALANCED MIXER: ANALYSIS

3.1 Introduction

In this chapter the novel subharmonic double balanced mixer (SDBM) is presented with qualitative and analytical descriptions.

3.2 Qualitative Description of the SDBM

A simplified schematic of the Gilbert cell mixer is shown in Fig. 3.1. A modification made in this circuit is the reversal of the traditional RF and LO ports, the reason for which will become apparent once the SDBM circuit is described. In this double balanced mixer topology, it is observed that the currents I_1 and I_2 switch at the rate of the LO frequency and are 180° out of phase. These currents are fed to the RF section, and the mixing between the RF and LO frequencies occurs in the current domain.

For a subharmonic mixer, the mixing needs to occur between the RF frequency

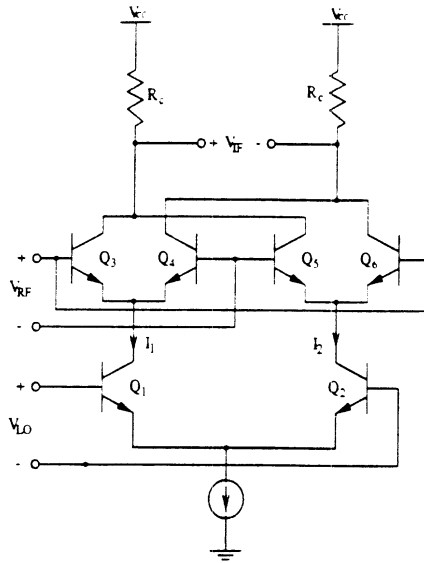


Figure 3.1: Simplified schematic of the Gilbert cell mixer.

and twice the LO frequency. So, if one can somehow generate I_1 and I_2 which switch at twice the LO frequency and which are 180° out of phase, subharmonic double balanced mixing is possible. The novel circuit topology shown in Fig. 3.2 does this precisely. It should be noted that there are two LO ports with each port driven by a differential (0° - 180°) voltage and the LO input at one port is 90° out of phase with the LO input at the other port.

The frequency doubling operation can be better understood by taking a closer look at the collector currents in the transistors in the LO section of the mixer. The collector currents in Q1, Q2, Q3 and Q4 are shown in Fig. 3.3. Notice the 0° , 180° , 90° , 270° phase of the four collector currents $i_c(Q1)$, $i_c(Q2)$, $i_c(Q3)$ and $i_c(Q4)$ respectively. It can be clearly seen that the current I_1 , which is the sum of the collector currents in Q1 and Q2, is switching at twice the LO frequency. In a similar fashion, it can be seen that the current I_2 , the sum of the collector currents in Q3 and Q4, is also switching at twice the LO frequency. The LO signal applied differentially to the bases of Q3 and Q4 is 90° out of phase with the the LO signal applied to Q1 and

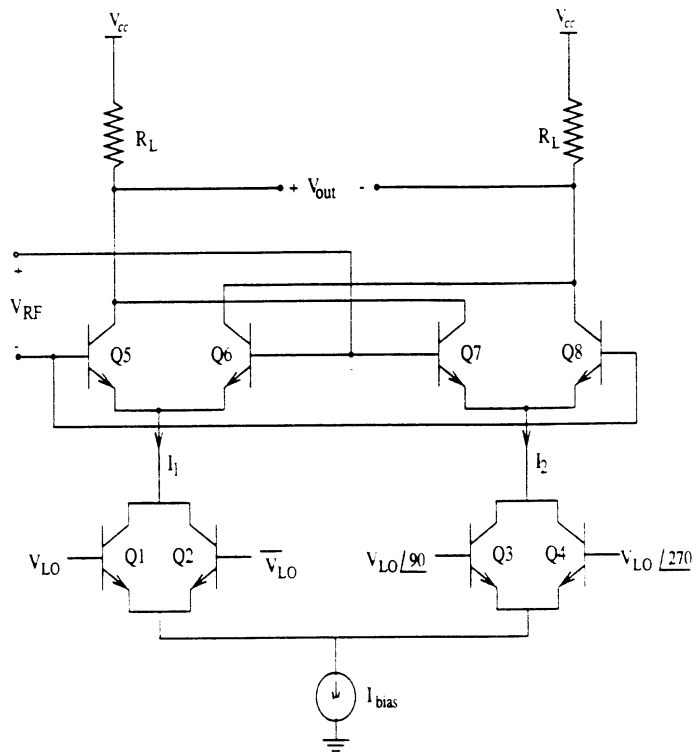


Figure 3.2: Simplified schematic of the novel Subharmonic Double-Balanced Mixer (SDBM).

Q2. As a result, the current I_2 is 180° out of phase with respect to current I_1 due to the frequency doubling effect. With I_1 and I_2 going into the RF section 180° out of phase, double balanced mixing occurs and with I_1 and I_2 switching at twice the LO frequency, subharmonic double balanced mixing is achieved.

3.3 DC Transfer Function of SDBM

In this section, general analytical expressions for the operation of the subharmonic double balanced mixer utilizing bipolar junction transistors are presented. The reader should refer to Fig. 3.4 for the circuit diagram and the various current definitions. For simplicity in the analysis, we assume that the bias current source I_{EE} has an infinite output resistance, that the base resistance of each transistor is negligible, and that the output resistance of each transistor is infinite.

The collector currents of the transistors Q1-Q2 can be related to the base-emitter voltages as follows:

$$I_{C1} = I_S e^{\left(\frac{V_{be1}}{V_T}\right)} \quad (3.1)$$

$$I_{C2} = I_S e^{\left(\frac{V_{be2}}{V_T}\right)} \quad (3.2)$$

where I_S is the saturation current of the transistors, and V_T is the thermal voltage.

Recognizing that $V_{be1} - V_{be2} = V_1$, we have:

$$\frac{I_{C1}}{I_{C2}} = e^{\left(\frac{V_1}{V_T}\right)} \quad (3.3)$$

Similarly,

$$\frac{I_{C3}}{I_{C4}} = e^{\left(\frac{V_2}{V_T}\right)} \quad (3.4)$$

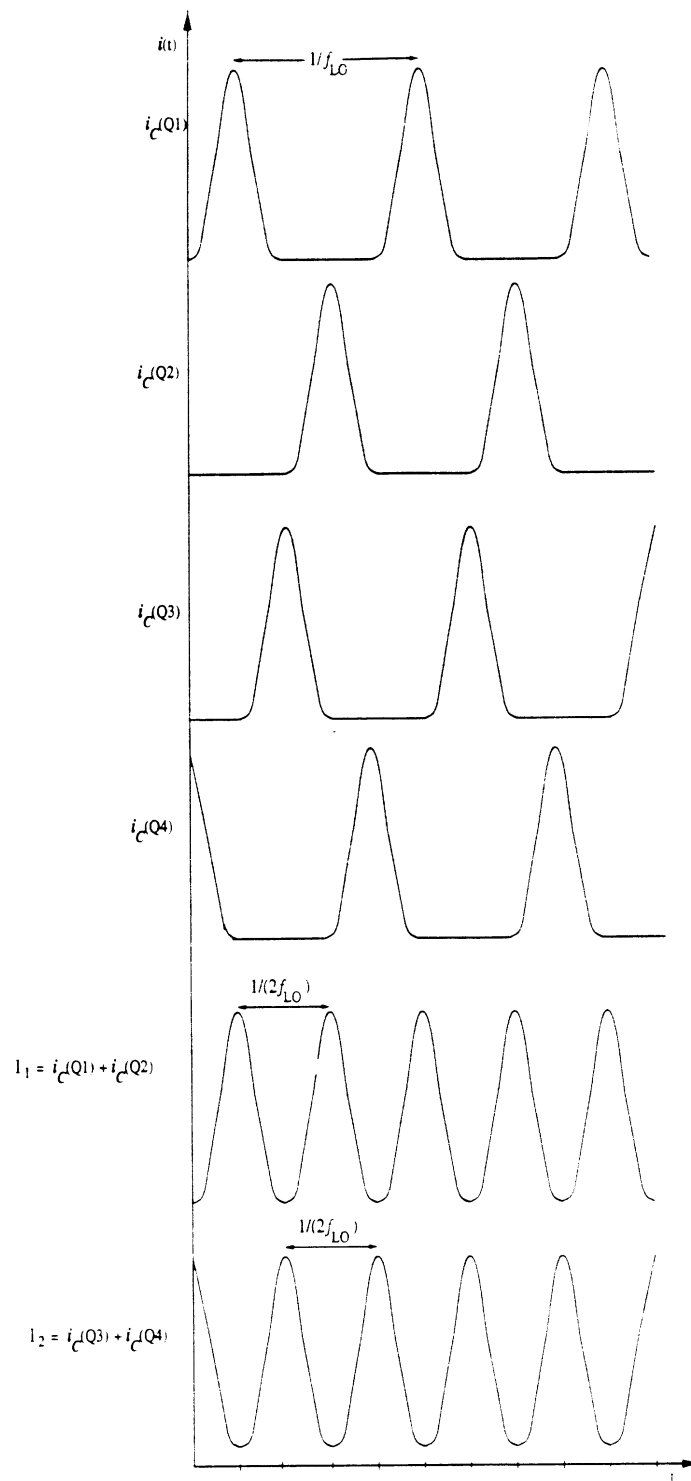


Figure 3.3: Collector currents in LO section illustrate the frequency doubling.

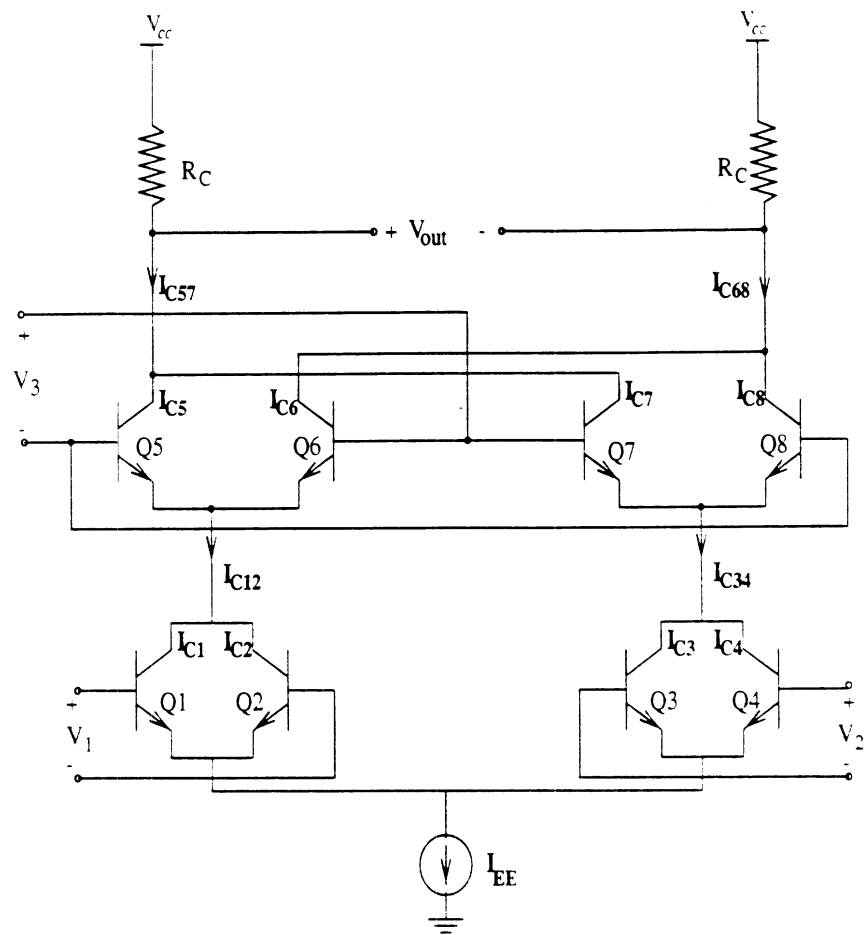


Figure 3.4: SDBM circuit with bipolar transistors.

Summing the collector currents of Q1-Q2 and Q3-Q4, we get:

$$I_{C12} = I_{C2} \left(1 + \frac{I_{C1}}{I_{C2}}\right) = I_{C2} \left(1 + e^{\left(\frac{V_1}{V_T}\right)}\right) \quad (3.5)$$

and,

$$I_{C34} = I_{C4} \left(1 + \frac{I_{C3}}{I_{C4}}\right) = I_{C4} \left(1 + e^{\left(\frac{-V_2}{V_T}\right)}\right) \quad (3.6)$$

Now, assuming that the voltage sources V_1 and V_2 have the same common-mode voltage, the base-emitter voltages of Q4 and Q2 can be related as:

$$V_{be4} - V_{be2} = \frac{V_1}{2} + \frac{V_2}{2} \quad (3.7)$$

which can be rewritten as:

$$\frac{I_{C4}}{I_{C2}} = e^{\left(\frac{V_1+V_2}{2V_T}\right)} \quad (3.8)$$

From equations 3.5, 3.6, 3.8:

$$\frac{I_{C12}}{I_{C34}} = \frac{1}{e^{\left(\frac{V_1+V_2}{2V_T}\right)}} \times \frac{1 + e^{\left(\frac{V_1}{V_T}\right)}}{1 + e^{\left(\frac{-V_2}{V_T}\right)}} = \lambda \quad (3.9)$$

We can express the currents entering the RF section (Q5-Q8) in terms of the bias current I_{EE} and λ as:

$$I_{C12} = \left(\frac{\lambda}{1 + \lambda}\right) \alpha_F I_{EE} \quad (3.10)$$

$$I_{C34} = \left(\frac{1}{1 + \lambda}\right) \alpha_F I_{EE} \quad (3.11)$$

Using the results of the DC transfer characteristic of emitter coupled pairs in [14], we can express the collector currents of Q5-Q8 as:

$$I_{C5} = \frac{\alpha_F \times I_{C12}}{1 + e^{\left(\frac{-V_2}{V_T}\right)}} \quad (3.12)$$

$$I_{C6} = \frac{\alpha_F \times I_{C12}}{1 + e^{\left(\frac{V_2}{V_T}\right)}} \quad (3.13)$$

$$I_{C7} = \frac{\alpha_F \times I_{C34}}{1 + e^{\left(\frac{V_2}{V_T}\right)}} \quad (3.14)$$

$$I_{C8} = \frac{\alpha_F \times I_{C34}}{1 + e^{\left(\frac{-V_2}{V_T}\right)}} \quad (3.15)$$

And, the output voltage can be derived as:

$$V_{out} = \Delta I \times R_C = (I_{C57} - I_{C68}) \times R_C \quad (3.16)$$

$$V_{out} = \alpha_F^2 I_{EE} \times \frac{1 - \lambda}{1 + \lambda} \times \frac{e^{\left(\frac{-V_2}{V_T}\right)} - e^{\left(\frac{V_2}{V_T}\right)}}{\left(1 + e^{\left(\frac{V_2}{V_T}\right)}\right) \times \left(1 + e^{\left(\frac{-V_2}{V_T}\right)}\right)} \quad (3.17)$$

where λ is as defined previously in terms of V_1 and V_2 .

3.4 Gain of the SDBM

To get an understanding of the available gain from the SDBM, we first calculate the low-frequency voltage gain of the mixer in Fig. 3.4 with the assumption that the pairs Q1-Q2 and Q3-Q4 experience complete, instantaneous switching at each zero-crossing point of V_{LO} .

If the LO waveforms have 50 percent duty cycle, the currents I_{C12} and I_{C34} from the LO section of the mixer will be square waves that are 180° out of phase: have an

average value of $\alpha_F I_{EE}/2$: an amplitude equal to $\alpha_F I_{EE}$: and a frequency of $2f_{LO}$.

The LO section currents can be expressed in time domain as:

$$I_{C12} = \alpha_F I_{EE} \left(\frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} (1 - (-1)^n) \cos(2n\omega_{LO}t) \right) \quad (3.18)$$

$$I_{C34} = \alpha_F I_{EE} \left(\frac{1}{2} - \frac{2}{\pi} \sum_{n=1}^{\infty} (1 - (-1)^n) \cos(2n\omega_{LO}t) \right) \quad (3.19)$$

Neglecting the higher LO harmonics,

$$I_{C12} = \alpha_F I_{EE} \left(\frac{1}{2} + \frac{4}{\pi} \cos(2\omega_{LO}t) \right) \quad (3.20)$$

$$I_{C34} = \alpha_F I_{EE} \left(\frac{1}{2} - \frac{4}{\pi} \cos(2\omega_{LO}t) \right) \quad (3.21)$$

Now, the RF section can be treated as consisting of two emitter coupled pairs formed by Q5-Q6 and Q7-Q8 as shown in Fig. 3.5. The small signal differential input voltage $v_{RF}(t)$ applied to the emitter coupled pair Q5-Q6 gets amplified to the output as $-g_m R_C \times v_{RF}(t)$, where $g_m = \frac{I_C}{V_T} = \frac{\alpha_F I_E}{V_T}$. The output voltage is the difference between the differential output voltages of the two pairs Q5-Q6 and Q7-Q8, and can be expressed as:

$$v_{out}(t) = \alpha_F \left(\frac{I_{C12} R_C}{V_T} - \frac{I_{C34} R_C}{V_T} \right) \times v_{RF}(t) \quad (3.22)$$

and, using equations 3.20 and 3.21, the output voltage in time domain can be approximated as:

$$v_{out}(t) = \frac{2\alpha_F^2 I_{EE} R_C}{V_T} \times \frac{4}{\pi} \cos(2\omega_{LO}t) \times v_{RF}(t) \quad (3.23)$$

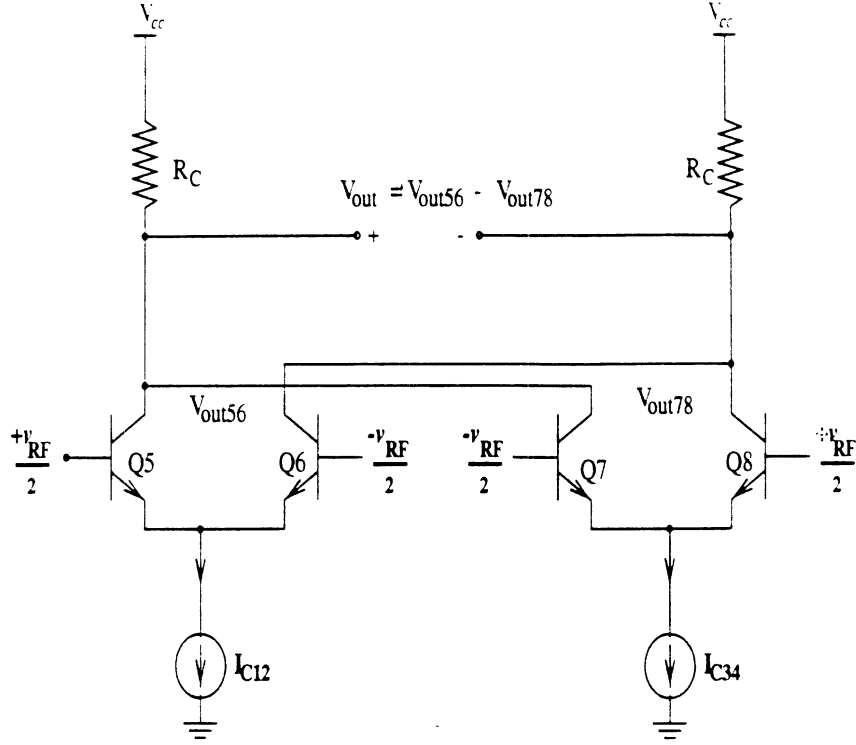


Figure 3.5: RF section of the SDBM.

Since multiplication of $v_{RF}(t)$ by $\cos 2\omega_{LO}t$ in the time domain is equivalent to shifting $V_{RF}(\omega)$ by $\pm 2\omega_{LO}$ and dividing the result by a factor of 2, the output voltage of the mixer in frequency domain is:

$$V_{IF}(\omega) = \frac{\alpha_F^2 I_{EE}}{V_T} \times \frac{4R_C}{\pi} \times V_{RF}(\omega - 2\omega_{LO}) \quad (3.24)$$

The voltage conversion gain is equal to the the output IF voltage, V_{IF} , divided by the input RF voltage:

$$A_V = \frac{4R_C}{\pi} \alpha_F^2 \frac{I_{EE}}{V_T} \quad (3.25)$$

For $R_C = 100 \Omega$, $I_{EE} = 8 \text{ mA}$, and $\alpha_F = 0.99$, the voltage gain of the mixer is about 30 dBV. At practical RF frequencies, the conversion gains of the circuit are lower than calculated above due to parasitic capacitances in the signal path. Also, the

LO section transistors do not act as ideal switches and this will cause a reduction in the gain too. More accurate values for the gain can be obtained by using full-model simulations in SpectreRF.

3.5 Distortion Performance of the SDBM

The distortion performance of downconversion mixers is usually specified by the input third-order intermodulation intercept point (IIP3) and is due to the third-order non-linearities in the mixer circuit. The principal source of distortion in active mixers is the RF input devices' non-linear conversion of signal voltage into current. Ideally, the LO switching section does not contribute to the non-linearity of the mixer. But, the sinusoidal nature of a practical LO drive and the non-linearities of the LO devices can also contribute to the overall distortion performance of the mixer.

The distortion analysis of the SDBM is complicated due to the reversal of the standard RF and LO sections as in the Gilbert cell mixer. The RF section can be linearized using emitter degeneration as shown in Chapter 4. But, there is a limit to the amount of degeneration that can be used and this is due to the fact that the mixing is happening in the RF section instead of the traditional LO section. Since mixing is a fundamentally non-linear process, linearizing the RF section negates the mixing process.

A better design of the SDBM is presented in Chapter 5, where the RF section can be linearized independent of the LO section and whose performance closely resembles that of traditional Gilbert type active mixers.

3.6 Noise Analysis of the SDBM

The biggest contributors for the noise figure of the SDBM are the thermal noise from the base resistance and the collector shot noise of the RF section devices. The LO section devices contribute noise also, but are difficult to analyze in the topology chosen for the SDBM where the traditional RF/LO sections are reversed. Please refer to Chapter 5 for the noise analysis of the more linear SDBM.

3.7 Balanced Doublers

The SDBM concept can also be used to build balanced frequency doublers. A simplified schematic of a balanced doubler is shown in Fig. 3.6. From the DC transfer character analysis of the SDBM done previously, the output voltage of the doubler can be expressed as:

$$V_{out} = \alpha_F I_{bias} \left(\frac{1 - \lambda}{1 + \lambda} \right) \quad (3.26)$$

where, λ is defined in equation 3.9, $V_1 = V_{in} \angle 0^\circ$ and $V_2 = V_{in} \angle 90^\circ$.

When the balanced doubler is driven by an input signal at frequency f_{in} , the best performance in terms of the isolation between $2f_{in}$ and f_{in} , $3f_{in}$, $4f_{in}$ etc. in the output voltage spectrum occurs when the transistors Q1-Q4 are driven hard. In the ideal case, when transistors Q1-Q4 are driven hard, the currents I_{C12} and I_{C34} will be square waves of amplitude I_{bias} and frequency $2f_{in}$. And, the maximum output voltage at $2f_{in}$ is $2I_{bias}R_C$.

Most other integrated circuit implementations of frequency doublers use some form of the translinear circuit principles described in [5] and are implemented in various technologies [15],[16],[17]. Most RFIC applications that use this multi-tanh

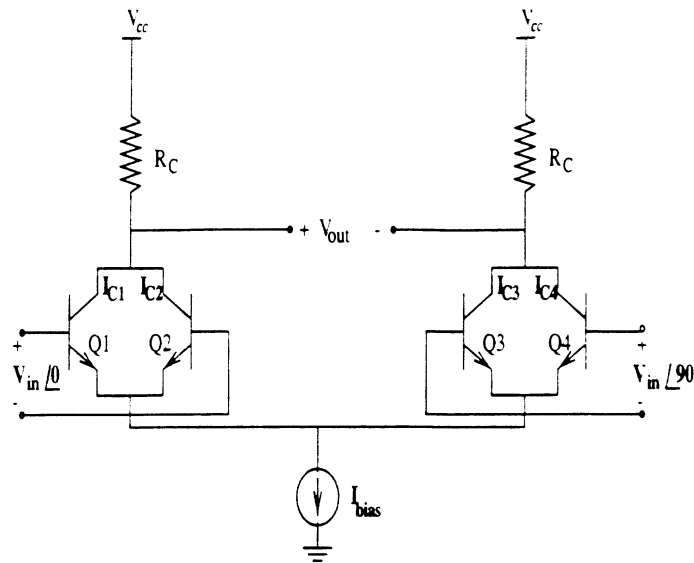


Figure 3.6: Simplified schematic of a balanced frequency doubler.

approach for frequency doublers need some form of LC-filtering in the load [17] to achieve adequate spectral purity of the second harmonic at the output. The balanced frequency doubler approach described here alleviates this problem.

CHAPTER 4

SUBHARMONIC DOUBLE BALANCED MIXER: DESIGN

4.1 Introduction

To understand and evaluate the advantages and drawbacks of the SDBM concept compared to other implementations that tackle the LO self-mixing problem, several simulation studies were done using the devices available in the Maxim GST3 SiGe bipolar process. The GST3 is a new high-speed IC process technology based on silicon germanium (SiGe), which features double-polysilicon bipolar transistors fabricated using a self-aligned double-polysilicon process that uses p-poly and n-poly to connect to the base and emitter. The transistors have a maximum f_T of 35 GHz. The process includes an NPN transistor, lateral PNP transistor, four layers of metals, two different poly-Si resistors, MOS capacitors, high-Q MIM capacitors and thick upper level metal layers for on-chip inductors.

The main implementation against which the SDBM was compared was the use of a multi-tanh frequency doubler followed by a Gilbert cell mixer presented by Meyer et al [17].

4.2 Comparison of SDBM versus Frequency Doubler + Gilbert Cell Mixer

A simplified schematic of the SDBM circuit designed in the Maxim GST3 process is shown in Fig. 4.1. The mixer is designed to operate at an RF frequency of 1.9 GHz and with an LO frequency of 900 MHz, resulting in an IF frequency of 100 MHz. The LO buffer stage which includes the RC-polyphase filter to generate the quadrature LO drive at 900 MHz is shown in Fig. 4.2.

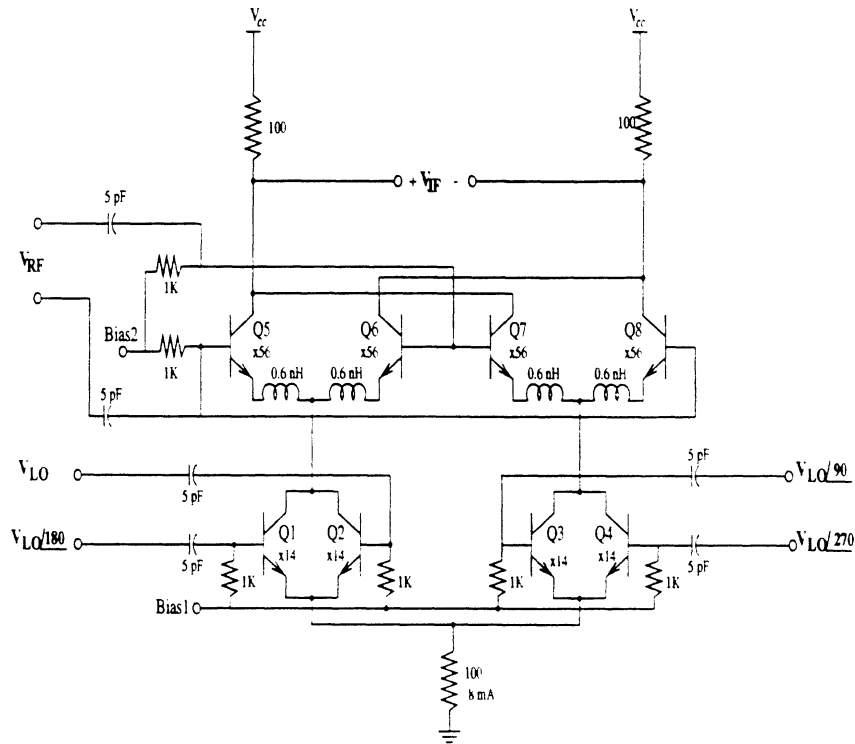


Figure 4.1: Subharmonic Double-Balanced Mixer (SDBM) schematic with an LO at 900 MHz and an RF at 1.9 GHz.

Based on the work in [17], a simplified schematic of the LO frequency doubler that was designed in the Maxim GST3 process is shown in Fig. 4.3. The frequency

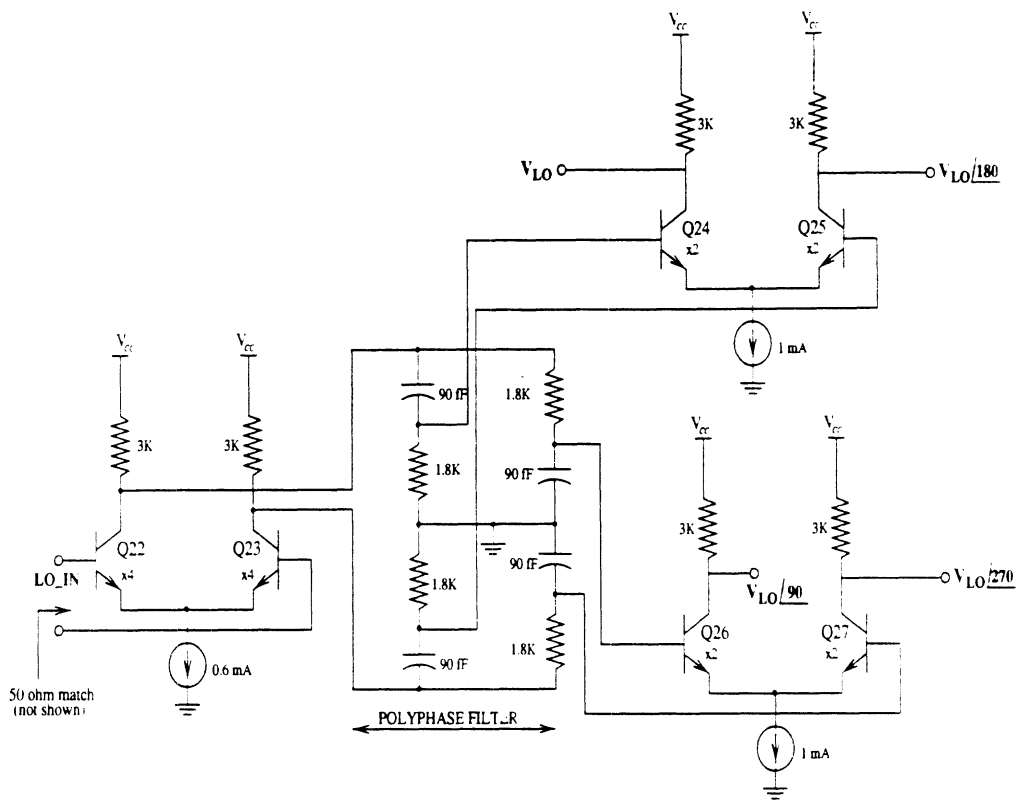


Figure 4.2: LO buffer and polyphase filter circuit at 90 MHz.

doubling is achieved by using a multi-tanh type circuit. Transistors Q1-Q4 perform the frequency doubling function and the inductive loads are used to peak the frequency response and attenuate the harmonics. Transistors Q5-Q6 form a simple differential pair and the inductive/resistive loads are chosen to supply a 600 mV_{ppk} signal to the LO port of the double-balanced Gilbert cell mixer. A simplified schematic of the Gilbert cell mixer is shown in Fig. 4.4, with transistors Q7-Q8 forming the RF section and Q9-Q12 forming the LO quad. Degeneration inductances of 1 nH are used in the RF section of the mixer to improve linearity. A biasing scheme similar to the one in [17] and in the SDBM design (which is described in detail in section 4.5.3) is used to provide a bias current of 8 mA in the mixer.

4.3 Comparison Simulation Results

The SDBM and the Gilbert Mixer with a frequency doubler were simulated using Cadence Spectre and SpectreRF with Maxim's GST3 process device models.

4.3.1 LO Feedthrough due to Coupling

For the LO to RF feedthrough simulations, several non-ideal effects were taken into account based on the models used at Maxim for the GST3 process:

1. A 33 pF bypass capacitor was assumed with a 0.8 nH series inductance on the Vcc pin, with an additional 5 nH inductance to an ideal Vcc source of 3 V.
2. To include capacitive coupling through the substrate, all parasitic capacitors were connected to the substrate node, which was then grounded through an inductor of 2 nH.
3. To include the parasitics due to the ESD protection setup, a 0.1 pF capacitor

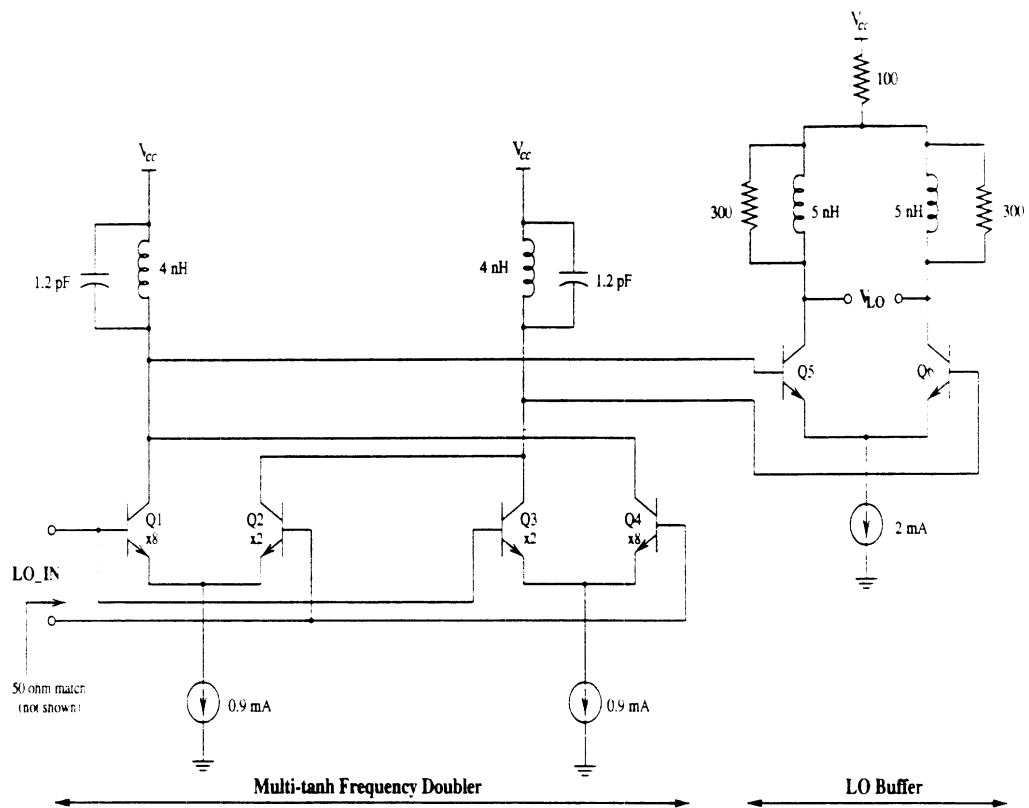


Figure 4.3: LO frequency doubler (900 MHz to 1.8 GHz) and buffer (1.8 GHz).

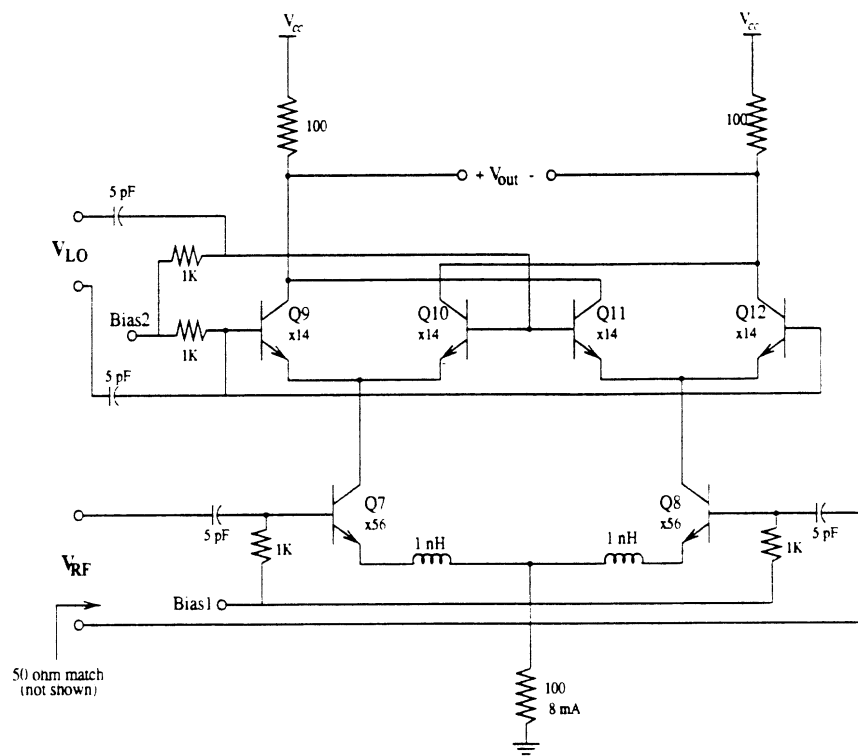


Figure 4.4: Gilbert cell mixer (standard design) used with the doubler circuit of Fig. 4.3.

to V_{cc} and a 0.1 pF capacitor to substrate was assumed for each port of the IC. An additional 0.1 pF was assumed for each bond-pad.

4. For package parasitics, a 2 nH inductance per lead was assumed. A mutual coupling coefficient of 0.3 was assumed for adjacent leads and 0.1 for non-adjacent leads. The IC was visualized to be bonded on a 10 pin package. The feedthrough was simulated for three different pin configurations (Fig. 4.5).

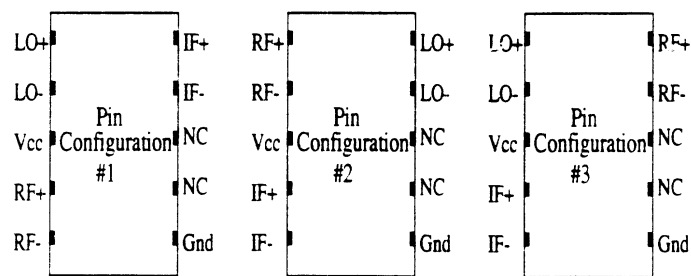


Figure 4.5: Pin configurations for feedthrough simulations (NC \equiv No connection).

With these additional impedances, the external matching networks at the RF and LO ports had to be slightly modified to get a 50 Ω differential input impedance. For the Glibert cell mixer design, the matching network consisted of a series inductance of 13 nH followed by a shunt capacitance of 150 fF across the bases of the input transistors. For the SDBM design, the matching network consisted of a shunt capacitance of 1 pF followed by a series inductance of 7.5 nH in series with the bases of the input devices. A time domain transient analysis was performed on both the mixers with an RF input of -30 dBm and LO inputs of -10, -16 and -20 dBm. The voltages at the RF port are presented in Table 4.1. The voltages at the IF port are presented in Table 4.2. The voltages at f_{LO} (900 MHz) and $2f_{LO}$ (1.8 GHz) were translated to dBm values assuming 50 Ω impedances at the RF port at the respective frequencies.

		Subharmonic Double Balanced Mixer			Doubler + Gilbert Cell Mixer		
Pins	Freq	P_{LO} -10dBm	P_{LO} -16dBm	P_{LO} -20dBm	P_{LO} -10dBm	P_{LO} -16dBm	P_{LO} -20dBm
Config1	f_{LO} 900MHz	38.4 μ V -78.3dBm	19 μ V -84.3dBm	11.9 μ V -88.5dBm	86.3 μ V -71.3dBm	44.3 μ V -77.1dBm	28.5 μ V -80.9dBm
	$2f_{LO}$ 1.8GHz	44 μ V -77.2dBm	34 μ V -79.5dBm	25.4 μ V -81.9 dBm	1.5mV -46.4dBm	1.2mV -48.7dBm	0.8mV -51.8dBm
Config2	f_{LO} 900MHz	0.74 μ V -112.6dBm	0.2 μ V -123.7dBm	11.9 μ V -88.5dBm	32.6 μ V -79.7dBm	17.7 μ V -85dBm	11.4 μ V -88.9dBm
	$2f_{LO}$ 1.8GHz	0.24mV -62.4dBm	0.3mV -60.3dBm	25.4 μ V -81.9dBm	1.5mV -46.5dBm	1.2 mV -48.7dBm	0.82mV -51.7dBm
Config3	f_{LO} 900MHz	56.5 μ V -75dBm	28.2 μ V -81dBm	18.2 μ V -84.8dBm	12.2 μ V -88.3dBm	6.6 μ V -93.6dBm	4.1 μ V -97.7dBm
	$2f_{LO}$ 1.8GHz	0.12mV -68.4dBm	0.14mV -67.2dBm	0.1mV -69.8dBm	44.2 μ V -77.1dBm	38.4 μ V -78.3dBm	27.5 μ V -81.2dBm

Table 4.1: Feedthrough simulations: Voltages at the RF port for different LO input power levels.

The IF voltage at the IF port was converted to power gain using $20\log(V_{IF}/V_{RF}) - 6$ dB. The -6 dB value is due to the 200 Ω load at the IF port.

The arrows in Tables 4.1 and 4.2 indicate the best conditions for the SDBM and the doubler + Gilbert cell mixer. It is seen that the $2f_{LO}$ feedthrough at the RF port is -77 to -82 dBm for both the mixers. However, a general look at Table 4.1 indicates that the SDBM has lower $2f_{LO}$ feedthrough levels on all pin configurations when compared to the doubler + Gilbert cell mixer. This is also true for Table 4.2 where the IF DC level of the SDBM is nearly independent of the pin configuration, while the doubler + Gilbert cell mixer is very dependent on the pin configuration. We therefore believe that the SDBM is a more robust circuit than the doubler + Gilbert cell mixer with respect to LO feedthrough.

		Subharmonic Double Balanced Mixer			Doublor + Gilbert Cell Mixer		
Pins	Freq	P_{LO} -10dBm	P_{LO} -16dBm	P_{LO} -20dBm	P_{LO} -10dBm	P_{LO} -16dBm	P_{LO} -20dBm
Config1	f_{IF} 100MHz	79.9mV 12dB	67.8 mV 10.6dB	51.3 mV 8.2dB	99 mV 13.9dB	98.8 mV 13.9dB	97.6 mV 13.8dB
	f_{RF} 1.9GHz	1.9mV -44.3dBm	1mV -49.8dBm	0.66mV -53.6dBm	1.6mV -46.1dBm	0.88mV -51.2dBm	0.53mV -55.5dBm
	f_{LO} 900MHz	1.2mV -48.4dBm	0.56mV -55dBm	0.34mV -59.5dBm	2.4mV -42.5dBm	1mV -49.9dBm	0.54mV -55.4dBm
	$2f_{LO}$ 1.8GHz	1mV -49.6dBm	1mV -49.7dBm	0.68mV -53.3dBm	2.4mV -42.3dBm	2.1mV -43.7dBm	1.3mV -47.8dBm
	DC	0.23mV	0.2mV	76 μ V	17.7mV	11.3mV	4.5 mV
Config2	f_{IF} 100MHz	78.8mV 11.9dB	67mV 10.5dB	51.3mV 8.2dB	98.9mV 13.9dB	98.7 mV 13.9dB	97.5 mV 13.8dB
	f_{RF} 1.9GHz	2.5mV -42dBm	1.7 mV -45.5dBm	0.66mV -53.6dBm	1.47mV -46.7dBm	0.84mV -51.5dBm	0.6 mV -54.5dBm
	f_{LO} 900MHz	31.5 μ V -80dBm	7.3 μ V -92.8dBm	0.33mV -59.5dBm	0.98mV -50.2dBm	0.4mV -57.9dBm	0.2mV -64.5dBm
	$2f_{LO}$ 1.8GHz	1.5mV -46.4dBm	1mV -49.8dBm	0.68mV -53.3dBm	7mV -33.2dBm	5.4mV -35.3dBm	3.7mV -38.8dBm
	DC	0.84mV	1.4mV	76 μ V	17.9mV	11.9mV	5mV
Config3	f_{IF} 100MHz	80.3mV 12.1dB	68mV 10.7dB	51.6 mV 8.3dB	99.2mV 13.9dB	99mV 13.9dB	97.8 mV 13.8dB
	f_{RF} 1.9GHz	2.2mV -43.1dBm	1.3mV -47.6dBm	1mV -50.3dBm	1.5mV -46.4dBm	0.84mV -51.5dBm	0.54mV -55.3dBm
	f_{LO} 900MHz	1.6mV -45.9dBm	0.76mV -52.4dBm	0.45mV -56.9dBm	1.8mV -45.1dBm	1mV -50.4dBm	0.62mV -54.2dBm
	$2f_{LO}$ 1.8GHz	1mV -49.2dBm	1.1mV -49.1dBm	0.8mV -52dBm	7mV -33.2dBm	5.4mV -35.3dBm	3.6mV -38.8dBm
	DC	0.28mV	0.62mV	0.44mV	0.11mV	0.26mV	0.22mV

Table 4.2: Feedthrough simulations: Voltages at the IF port for different LO input power levels and with $P_{RF} = -30$ dBm.

4.3.2 Noise Figure

The SDBM has a simulated noise figure of 7.6 dB and the doubler+Gilbert cell mixer has a simulated noise figure of 6.1 dB as per SpectreRF. The noise figure is virtually independent from the LO input power as shown in Fig. 4.6. If the buffers after the polyphase filter are designed as limiters in the SDBM design, the noise figure (and gain) of the SDBM will remain relatively constant with respect to the external LO drive.

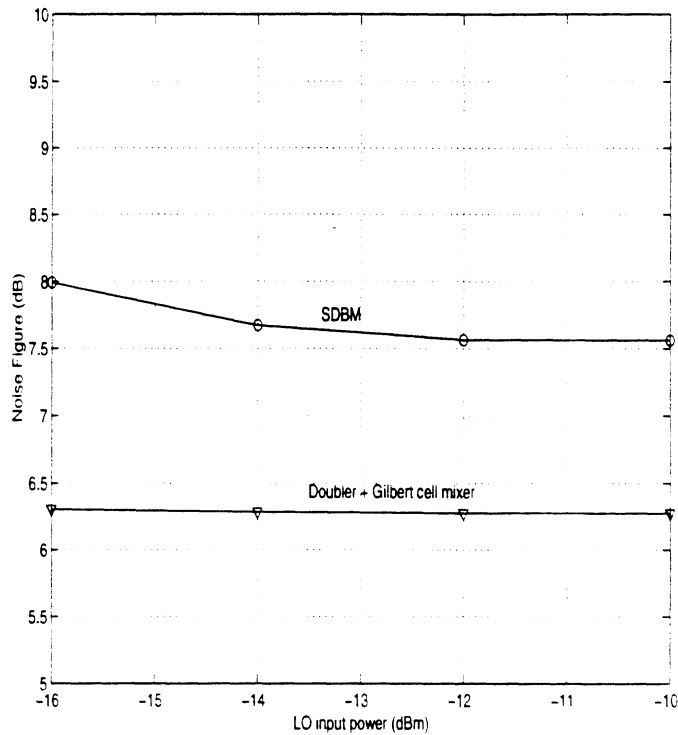


Figure 4.6: Noise Figure versus LO drive.

4.3.3 Two-Tone Test

A transient analysis with two tones applied to the RF port was performed on the SDBM and the Gilbert Mixer. Two tones with equal power were applied at 1.89 GHz

and 1.91 GHz at the RF port. The input at the LO port was -10 dBm at 900 MHz. The fundamental tones at 90 MHz and 110 MHz and the third order products at 70 MHz and 130 MHz were observed at the IF port. The harmonic signature for the SDBM is shown in Fig. 4.7(a) and for the Gilbert Cell Mixer is shown in Fig. 4.7(b). The third harmonic signature of the SDBM design shows a strange behavior and the reason is not fully known. It could be due to some harmonic component cancellation or addition due to various phases of the LO signals in the circuit.

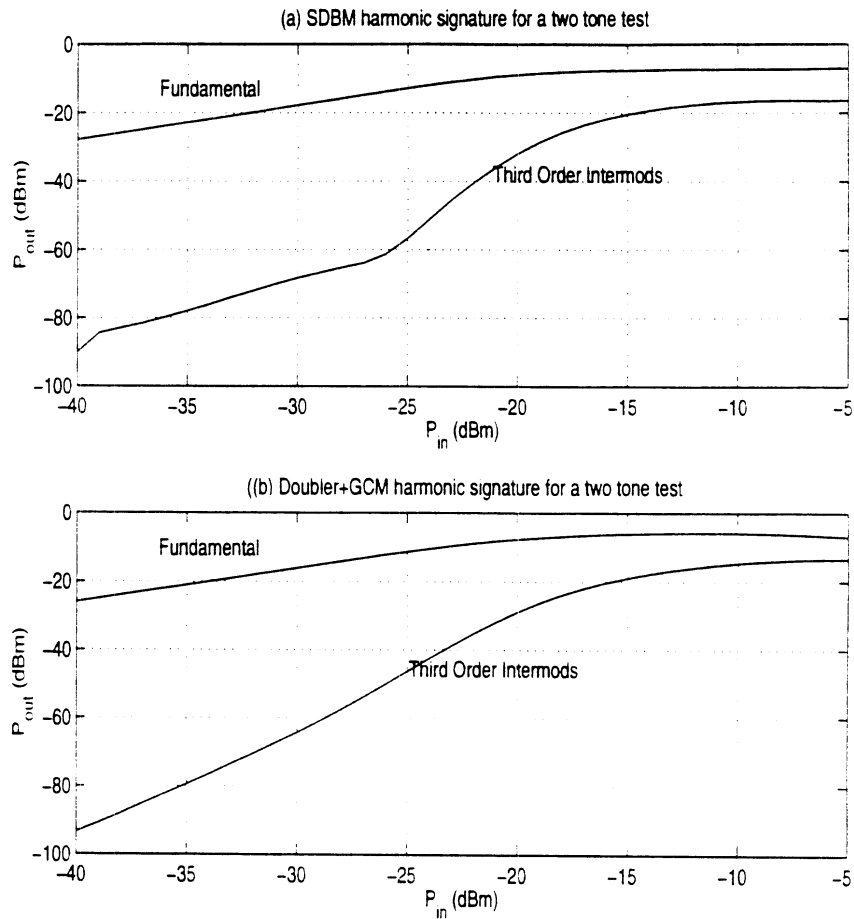


Figure 4.7: Harmonic signature in response to a two-tone test of (a) the SDBM (b) the doubler + Gilbert cell mixer.

The power gain of the SDBM is 12 dB and the input -1 dB compression point is -20 dBm. The power gain of the doubler + Gilbert cell mixer is 14 dB and the input -1 dB compression point is -20 dBm. The small extra gain (2 dB) in the Gilbert cell mixer can be traded off to improve the linearity by increasing the degeneration inductances.

4.3.4 Power Consumption and Chip Area

For both the mixer designs, a power supply voltage of 3 V was assumed. The SDBM design has a current consumption of 10.6 mA and the doubler + Gilbert cell mixer design has a current consumption of 10.8 mA. The power consumption in both the designs is therefore nearly identical.

The main difference in the area consumed by the two designs is in the amount of planar inductances used. In the SDBM design, four inductances of 0.6 nH each are used for degeneration in the RF section. The doubler + Gilbert cell mixer design uses two inductances of 1 nH each for the same purpose. In addition to this, the doubler uses two inductances of 4 nH each and the buffer following the doubler uses two inductances of 5 nH each. This represents an additional inductance of almost 18 nH in the doubler + Gilbert cell mixer design over the SDBM design.

Therefore it was estimated that the SDBM will occupy a substantially reduced area when compared to the doubler-mixer approach. The exact value (30%-70%) will depend on the layout of the inductors and the space they will occupy on the chip. A summary of the simulation results for both the SDBM and the doubler + Gilbert cell mixer are presented in Table 4.3.

	Subharmonic Double Balanced Mixer	Doubler + Gilbert Cell Mixer
Supply Voltage	3 V	3V
Current Consumption	10.6 mA	10.8 mA
Gain	12 dB	14 dB
Noise Figure	7.6 dB	6.1 dB
P_{-1dB} Compression Point	-20 dBm	-20 dBm
IIP3	Not Defined ¹	-6 dBm
Total Inductance	2.4 nH	20 nH

Table 4.3: Simulation results comparing SDBM with doubler + Gilbert cell mixer.

4.4 Test & Measurement Results of SDBM in Maxim Process

The SDBM circuit design described above was fabricated using Maxim's GST3 process and the fabricated die were mounted on a test board and tested at the University of Michigan. Several different die were tested and they were not functional. The DC current drawn from the power supply source varied wildly and the reason the chip failed is not fully known. It is thought that the GST3 run was not successful since it was a "test run" and the DC bias could not be maintained.

4.5 SDBM Circuit Design in Conexant 0.35 μ BiCMOS Process

A 2.5 GHz SDBM design which includes the mixer core, a polyphase filter for quadrature LO generation and LO buffers was designed using the Conexant 0.35 μ m

¹The slope of the third order intermods at RF power level less than -30 dBm is around 2.3 and changes abruptly at -25 dBm. Therefore, a clear definition of IIP3 for this circuit is not available. At RF levels below -30 dBm, the third order intermods in the SDBM are as low as in the doubler + Gilbert cell mixer.

BiCMOS process. The overall schematic of the design is shown in Fig. 4.8. The RF input is at 2.5 GHz and the LO input is at 1.2 GHz resulting in an IF output at 100 MHz. Conexant's BC35 process is a $0.35\mu\text{m}$, four layer metal commercial BiCMOS process with a maximum devices f_T of 25 GHz. The process incorporates $0.35\mu\text{m}$ minimum sized CMOS devices in an n-well, a 3 V and 5 V NPN transistor, a parasitic PNP transistor, two types of resistors (with resistivities of $100\ \Omega/\square$ and $500\ \Omega/\square$), a MIM RF capacitor, an RF varactor, and thick metal3 for inductors.

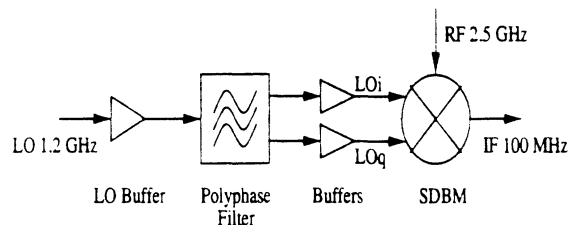


Figure 4.8: Schematic of the 2.5 GHz Subharmonic Double-Balanced Mixer (SDBM) circuit.

4.5.1 Mixer Core Design

A simplified schematic of the subharmonic double balanced mixer core is shown in Fig. 4.9. Transistors Q1-Q4 form the LO section and are biased at node Bias1 using a PTAT bias generator discussed in a subsequent section. Transistors Q5-Q8 form the RF section of the mixer. In order to keep the design simple, $100\ \Omega$ resistive loads are used at the collectors of Q5/Q6 and Q7/Q8. Also, for low-voltage operation with $V_{cc}=3\ \text{V}$, a $100\ \Omega$ resistor is used for biasing instead of an active current source. It should be noted that the output impedance of a transistor based current source is of the order of a few $100\ \Omega$ at 2.5 GHz and does not offer significant advantage over using an active current source. A tail current of 8 mA biases the mixer core. This

current was chosen to provide a good trade-off between the mixer gain, linearity and noise figure. Increasing the current beyond 8 mA poses dc voltage headroom problems due to increasing voltage drops across the bias and load resistors. The biggest noise contributor in the mixer core is the base resistance of devices Q5-Q8. The device sizes of Q5-Q8 are chosen to minimize the base resistance while keeping the current density in the devices at 70 percent of the peak- f_T current density. Having multiple base-emitter fingers in the device layout also helps in reducing the base resistance further.

Inductive degeneration in the RF section is used to improve the linearity of the mixer and to also improve the input matching. There is a limit to which the RF section can be degenerated, since beyond a 2 nH inductance, the mixer gain degrades severely with increasing degeneration inductance. Fig. 4.10 shows the simulated voltage gain of the mixer versus the degeneration inductance.

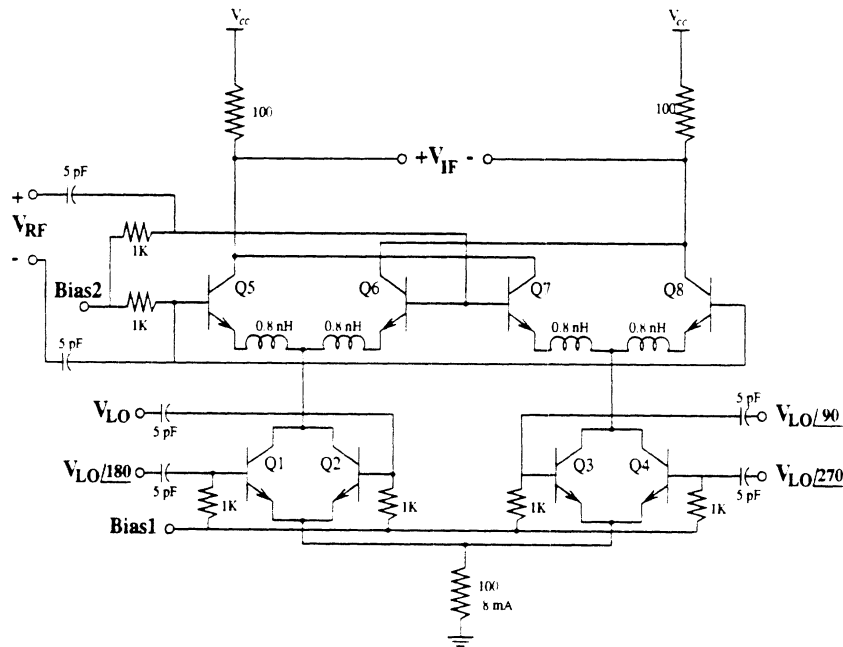


Figure 4.9: Subharmonic Double-Balanced Mixer (SDBM) schematic.

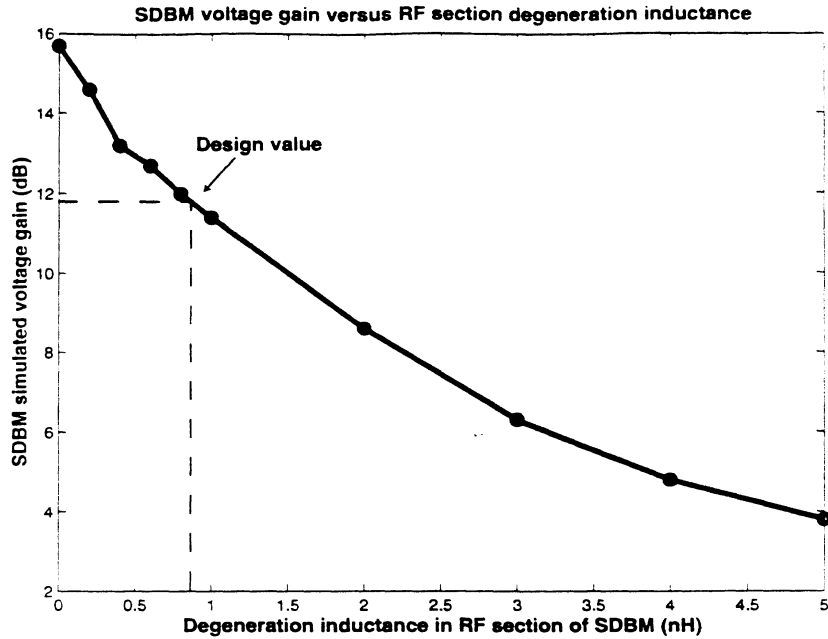


Figure 4.10: SDBM voltage gain versus degeneration inductance.

4.5.2 LO path design

A simplified schematic of the entire LO path which includes the first stage of the LO buffer, polyphase filter and the second stage of LO buffers is shown in Fig. 4.11. The first LO buffer amplifies the LO signal coming from off-chip and provides voltage gain to counteract the 7.8 dB voltage loss in the polyphase filter. The outputs of the polyphase filter are amplified by differential amplifier limiting stages before being fed to the two LO ports of the mixer. The LO drive at the mixer was chosen to optimize the dynamic range and is around 500 mV_{pk} . The polyphase filter outputs have phase and amplitude variation with LO input frequency. Nevertheless, the two differential LO quadrature signals maintain a 90° phase difference over a wide bandwidth. Fig. 4.12 shows the final simulated voltages at different points in the LO path. Fig. 4.13 shows the amplitude and phase variation of the I/Q paths in the frequency range of 0.8-1.6 GHz. It can be seen that the close to a 90° phase shift is

maintained over a wide bandwidth.

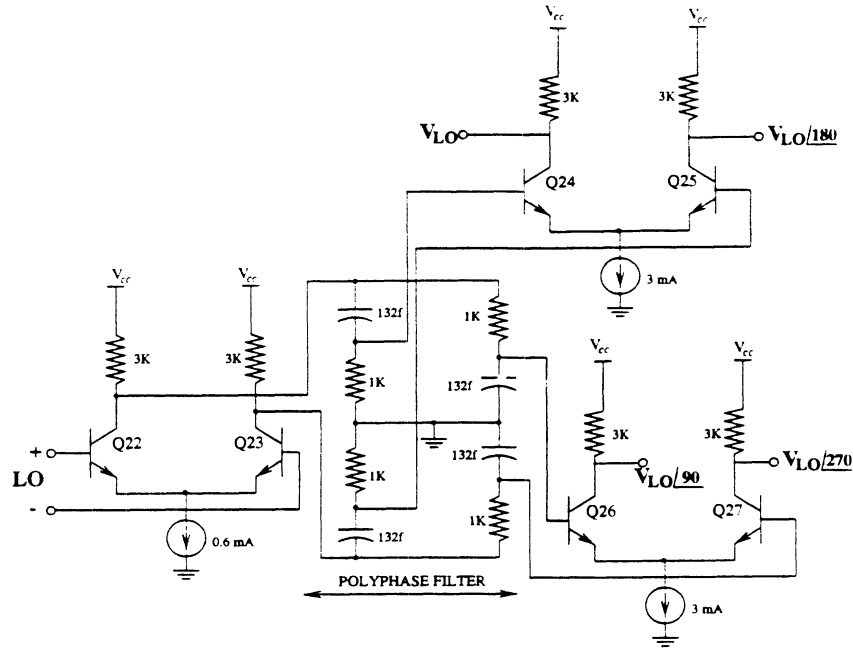


Figure 4.11: LO buffer and polyphase filter circuit.

4.5.3 Bias Circuit Design

The DC voltage at node Bias1 is designed to be a PTAT (proportional to absolute temperature) voltage so as to keep the input impedance of the RF port stable with respect to temperature variations [17]. The dc voltage at the node Bias1 is generated as shown in Fig. 4.14. The node Bias1 is shunted to ground using a 10 pF capacitor in order that the impedance at the node appears as a ground at frequency of operation of the mixer (>1 GHz). This ensures that the noise from the bias circuit does not contribute to the mixer noise.

Transistors Q9-Q14 form the basic PTAT bias cell where the emitter sizes of Q9 and Q10 have a ratio of 1:4 creating a V_{be} mismatch of $(kT/q) \times \ln(4)$ which appears across the 1 K Ω resistor producing the PTAT current. Q11 and Q12 form

LO Path Transient Analysis 1.2 GHz

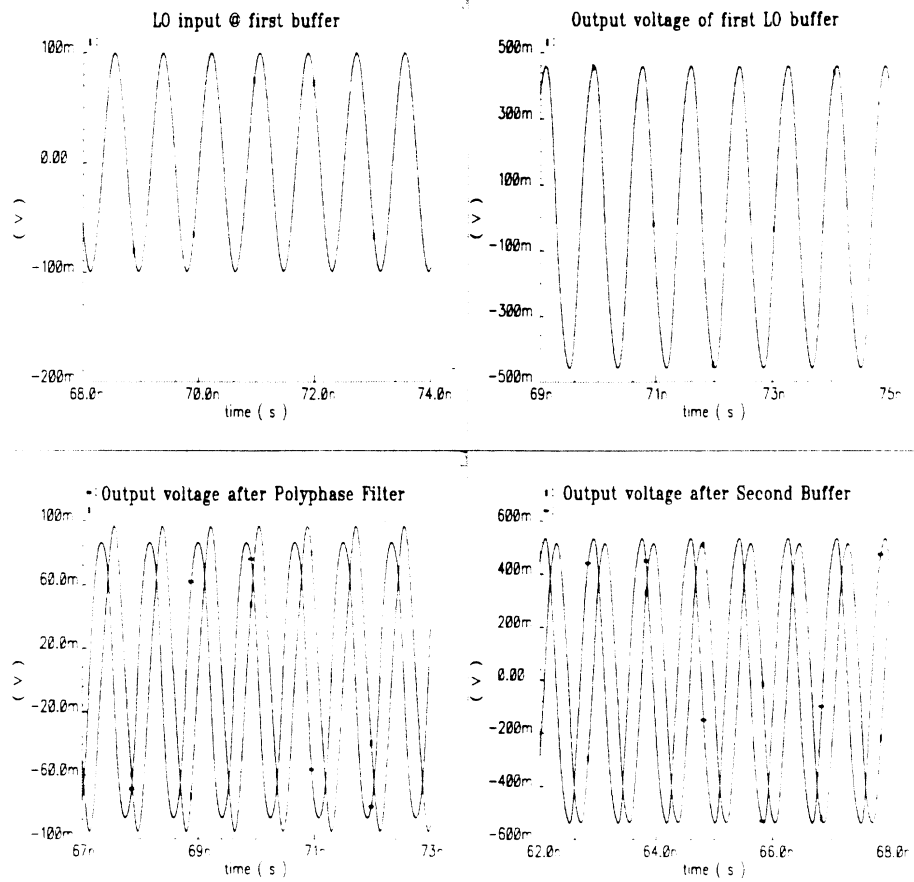


Figure 4.12: Simulated LO path voltages in time domain

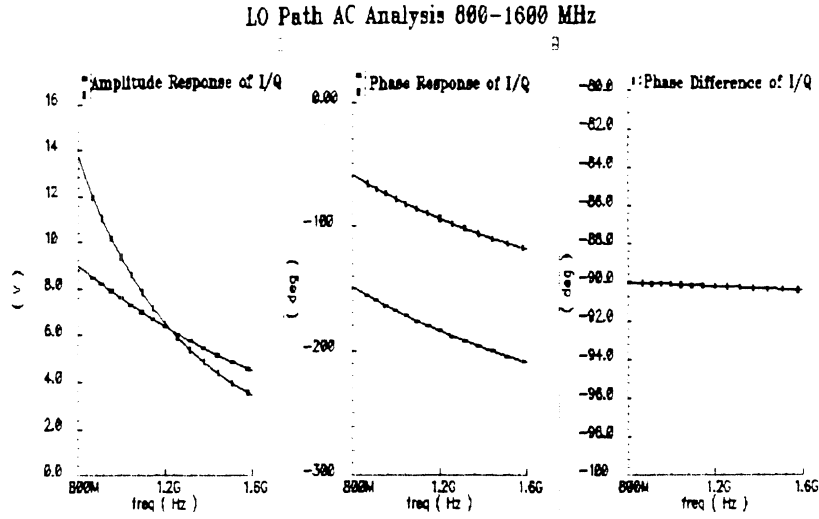


Figure 4.13: Simulated LO path output voltages in the frequency domain.

a cascode connection to improve the output impedance and the current matching in Q9 and Q10. The PTAT current is mirrored from Q13-Q14 to Q17 and Q20 with the appropriate multiplication factors provided by the emitter sizes of Q17 and Q20. Transistor Q15 is used to bias the pnp device Q16, which provides the base currents for the low β pnp devices Q13-14, Q17 and Q20. For bias purposes, the loading at the node Bias1 by the LO section transistors Q1-Q4 appears as an $\times 60$ transistor with a base resistance of $0.25 \text{ k}\Omega$ and an emitter resistance of 100Ω . To obtain the required 8 mA bias current in the mixer from the $400 \mu\text{A}$ PTAT current flowing through Q18 ($\times 3$ transistor), the base resistance of Q18 is chosen as $(8 \text{ mA}/400 \mu\text{A}) \times 2.25 \text{ K}\Omega = 45 \text{ K}\Omega$. The $2.25 \text{ K}\Omega$ resistor that is ratioed with the $45 \text{ K}\Omega$ resistor is made up of the $2 \text{ K}\Omega$ resistor attached to node Bias1, plus the $0.25 \text{ K}\Omega$ resistance formed by the four $1 \text{ K}\Omega$ resistors in parallel at the LO section transistors. In this current mirroring scheme, Q19 and Q21 form an npn-pnp current helper and allow operation down to

V_{cc} as low as 2.7 V [17].

The DC voltage at node Bias2 is generated by simple voltage division using two diodes and a resistor connected to V_{cc} . This is because the bias currents through Q5-Q8 are already fixed by the PTAT bias current in Q1-Q4 and the node Bias2 is biased by a simple source so that the transistors Q5-Q8 are always operating in the forward active region. The bias currents for the LO path are derived from a bandgap biasing circuit that utilizes the same PTAT cell described above.

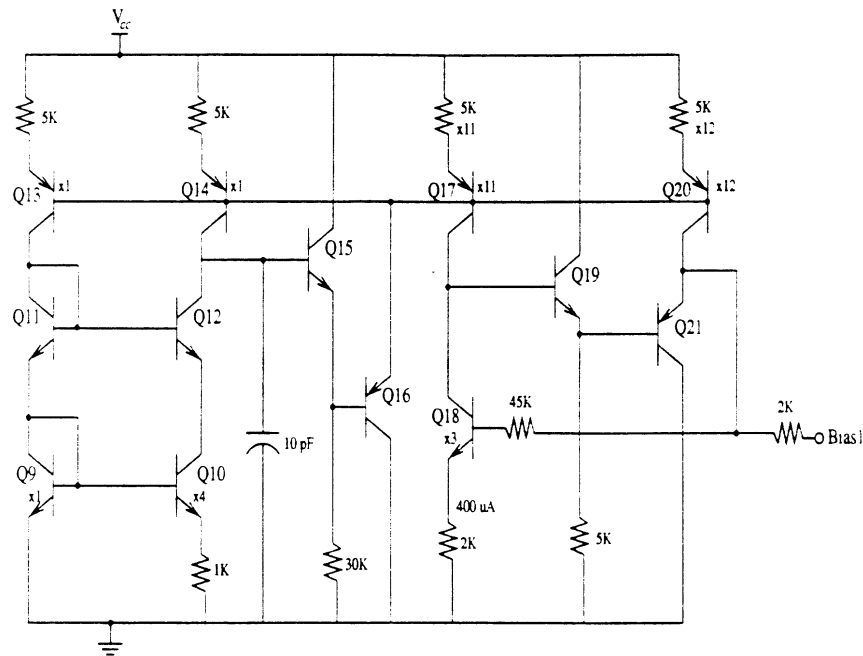


Figure 4.14: PTAT biasing circuit for node Bias1 in the SDBM.

4.6 Test & Measurement Results

The fabricated die (in the Conexant 0.35μ process) was mounted on a test board and the layout is shown in Fig. 4.15. The RF and LO differential ports on the die are probed using a differential probe which includes a balun to convert from differential mode to single ended coaxial mode.

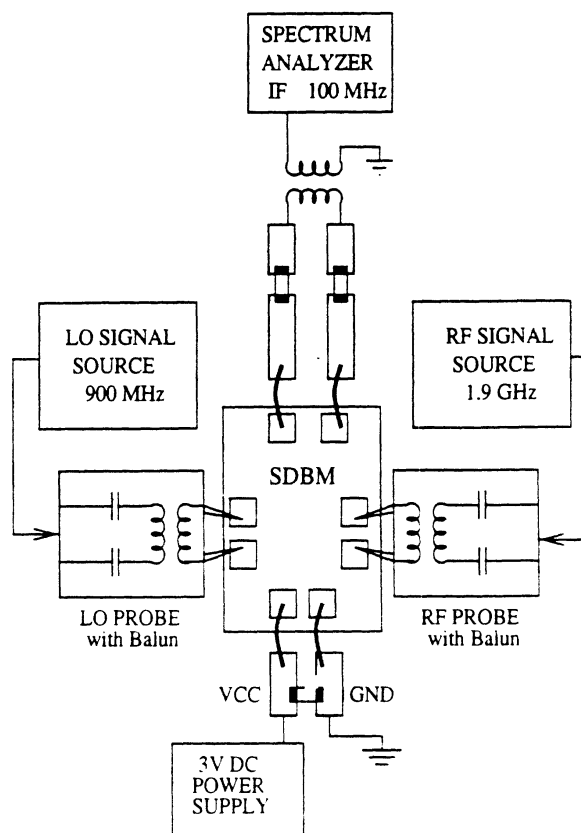


Figure 4.15: Layout of the test board for measurements.

The IF, VCC and GND pads on the die were wire-bonded to coplanar striplines on the test board. Fig. 4.16 shows a photomicrograph of the chip under test.

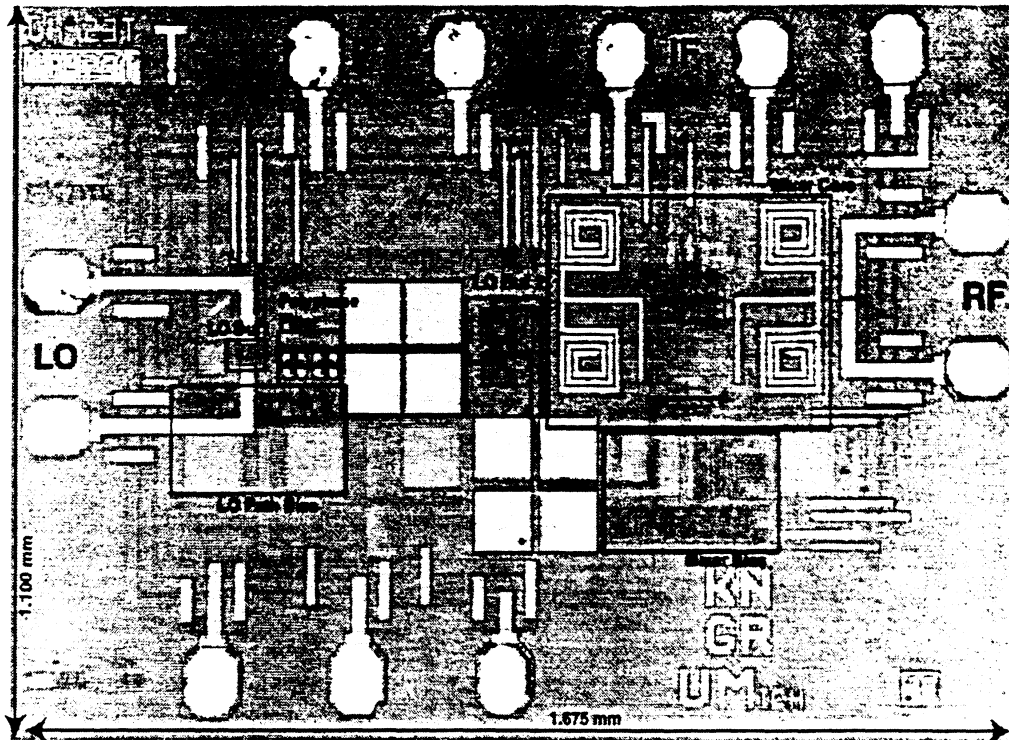


Figure 4.16: Photomicrograph of the SDBM chip.

The LO probe was matched to 100Ω with an S11 better than -10 dB over the frequency range of 800-1700 MHz, and the RF probe was matched over the frequency range of 1.3-2.3 GHz. Fig. 4.17 and Fig. 4.18 show the S11 of the RF and LO probes respectively. The RF probe has a loss of 0.7-0.9 dB across the frequency range of 1.2-2.4 GHz, and the LO probe has a loss of 0.4-0.5 dB across the frequency range of 0.8-1.4 GHz. DC block capacitors are also integrated into the probe [18].

Although the mixer was designed to work at 2.5 GHz, the measurements show that the mixer works well around at 1.9 GHz. All the measurement results below show the mixer operating at an RF frequency of 1.9 GHz, with an LO frequency of

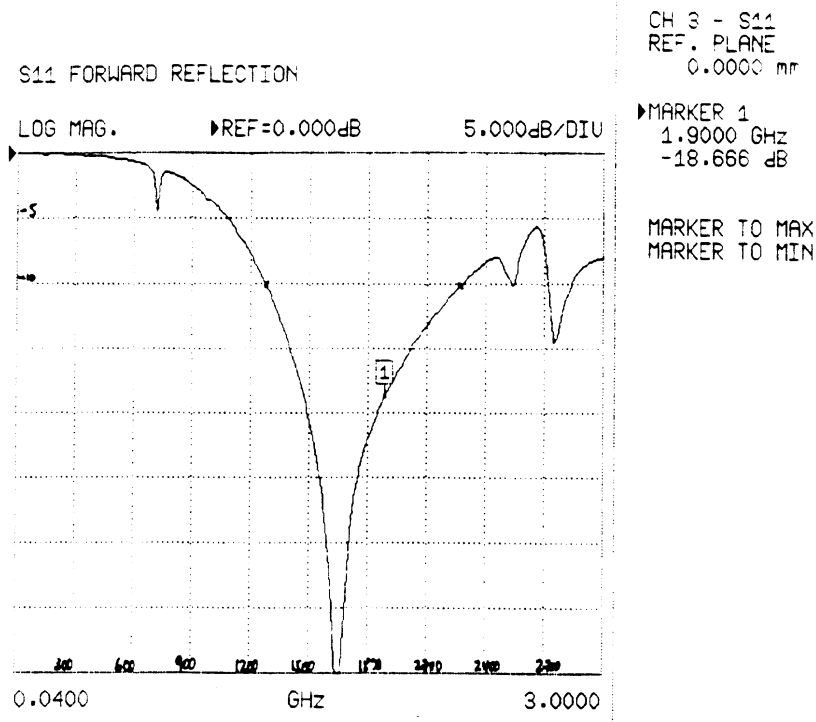


Figure 4.17: RF probe S11 with a 100 Ω differential load.

900 MHz resulting in an IF frequency of 100 MHz.

Fig. 4.19 shows the mixer power gain versus RF input frequency with the LO input frequency at 900 MHz and, an LO input power of 0 dBm into the mismatched LO port (LO port was not externally matched). The RF probe effects have been normalized out of the measurements.

A two tone test was performed to measure the input third order intermodulation point (IIP3) of the mixer. The two tones were at 1.89 GHz and 1.91 GHz resulting in fundamental tones at 90 MHz and 110 MHz, and third order intermods at 70 MHz and 130 MHz at the IF output. Fig. 4.20 shows the fundamental and intermod powers with respect to the two tone input powers. Extrapolation of the two curves results in an IIP3 of -3 dBm. Fig. 4.21 shows a plot of the mixer gain at 1.9 GHz as the LO input power at 900 MHz is varied from -20 dBm to 0 dBm. The mixer operates well

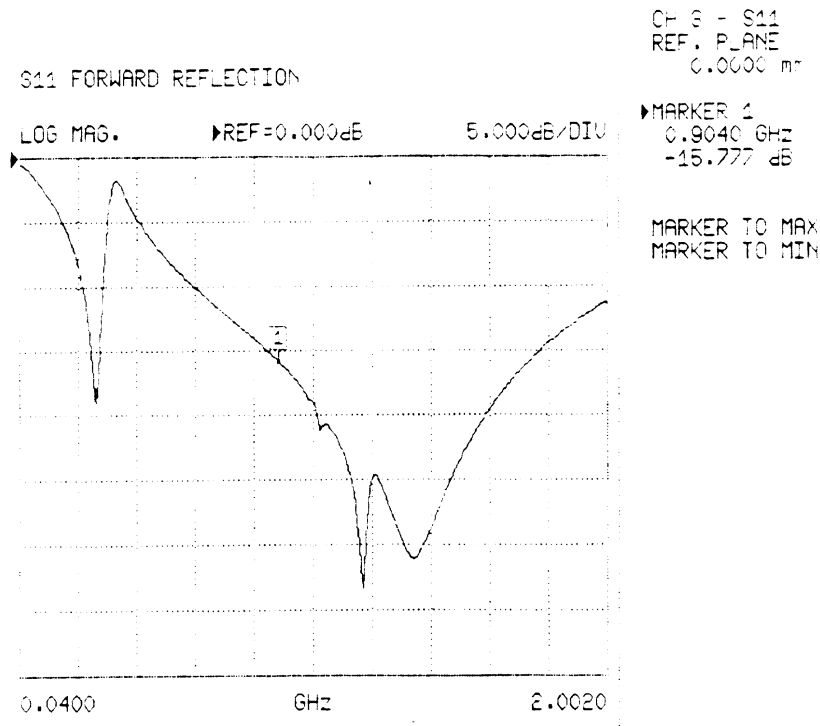


Figure 4.18: LO probe S11 with a 100 Ω differential load.

down to an input LO power (mismatched) of -12 dBm as shown by the gain versus LO power plot in Fig. 4.21.

The measured DC differential output level at the IF port with an LO input of 0 dBm and a mismatched RF port is about 10 μ V. It should be noted that it is hard to get accurate measurements at such low voltages. The measured single side band noise figure of the mixer was 10 dB at an RF input of 1.9 GHz and an LO input of 900 MHz. The measurement results are summarised in Table 4.4. The design kit from conexant also had only preliminary circuit models for the inductors. From the simulation results presented previously, it can be seen that the gain of the SDBM is fairly sensitive to the degeneration inductance and any change in the actual value of the inductance on the die will cause a shift in the measured gain.

The measurement results of the SDBM in comparison to other implementations

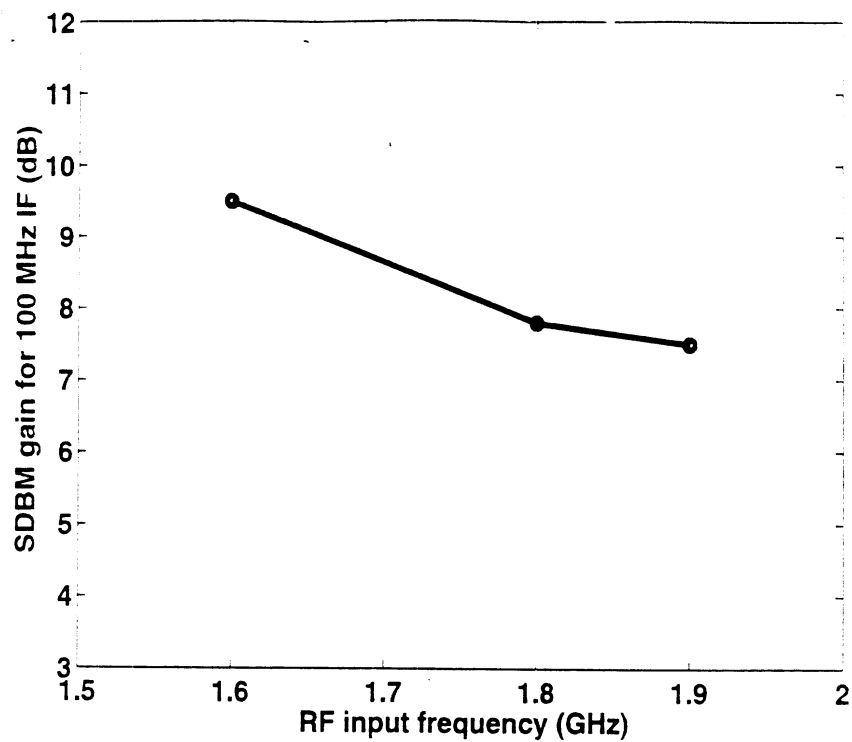


Figure 4.19: SDBM measured gain versus the RF input frequency.

Supply Voltage	3 V
Mixer Core Current	8 mA
LO Frequency	900 MHz
RF Frequency	1.9 GHz
Conversion Gain	7.5 dB
IIP3	-3 dBm
Input P_{-1dB}	-8 dBm
SSB Noise Figure	10 dB

Table 4.4: Summary of SDBM measurement results

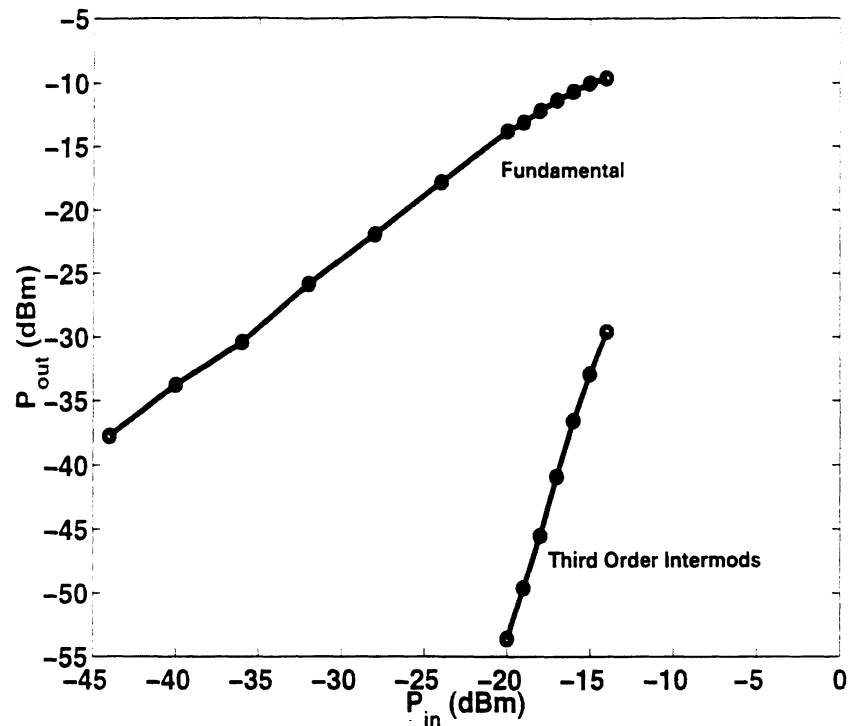


Figure 4.20: Measured SDBM harmonic signature at 1.9 GHz RF input.

of subharmonic mixers as discussed in Chapter 2 is shown in Table 4.5.

4.6.1 Deviation of Measured Results from Simulated Results

As was mentioned earlier, the measured results of the SDBM show a frequency shift in the operation of the mixer. The main reason could be in the absolute value shift of the polyphase filter resistors and capacitors due to process variation. The value of the capacitors used in the polyphase filters was very small and it is thought that the models do not adequately account for the fringing capacitance of these small values capacitors. Conexant was continually updating the process models, but we did not have latest design kit here at the University to reflect these changes in the process models. A secondary reason could be the frequency response of the RF probe which is designed to work well at 1.9 GHz and tends to be mismatched beyond 2.6 GHz.

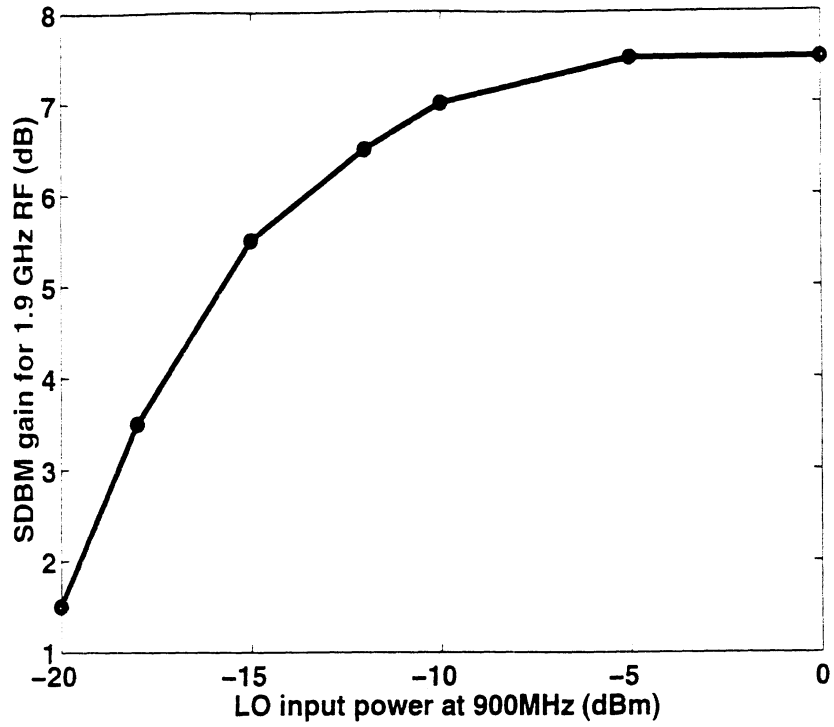


Figure 4.21: Measured SDBM gain at 1.9 GHz RF input versus the LO input power at 900 MHz.

	Yamaji et al [2] CICC 1997	Shimozawa et al [12] RFIC 1998	Matinpour et al [13] MTT Dec 2000	Sheng et al [3] JSSC Sep 2000	This work [19] RFIC 2001
Mixer Type	ECP	APDP	APDP	Two level Quadrature LO	Single level Quadrature LO
V_{cc}	2.7 V	-	2.7 V	3.3 V	3 V
I_{mixer}	5 mA	-	21 mA	2.8 mA	8 mA
f_{RF}	2 GHz	1.6 GHz	5 GHz	2 GHz	1.9 GHz
LO power	8 dBm	9 dBm	8 dBm	10 dBm	0 dBm
Gain	5.6 dB	-6 dB	-17 dB	17.2 dB	7.5 dB
SSB NF	17 dB	23 dB	15 dB	12.8 dB	10 dB
IIP3	-1 dBm	9 dBm	6 dBm	-5.1 dBm	-3 dBm

Table 4.5: Comparison of SDBM measurement results with other sub-harmonic mixer implementations

Both the linearity and noise figure performance of the mixer match the simulations closely. The measured gain of the mixer is lower than the simulated gain by about 6 dB. This could be explained by the variation of the load resistors from the simulated value. The load resistors were designed to be at $100\ \Omega$. The measured DC value at the IF port was 2.75 V, and assuming that the mixer has a tail bias current of 8 mA, the actual resistance of the load resistors is $(3.0-2.75)\ \text{V}/4\ \text{mA} = 62.5\ \Omega$. The total simulated current of the chip was 15.68 mA and the current drawn from the 3 V power supply during testing was 15.82 mA. So, the mixer current should be fairly close to the assumed 8 mA. This lower value of the load resistor leads to a mixer gain of 9.4 dB which is better agreement with the measured value of 7.5-9 dB.

4.7 Balanced Frequency Doubler Circuit Design

Using the idea of quadrature signal like in the LO path of the SDBM, a balanced frequency doubler circuit was be designed. Fig. 4.22 shows the schematic of the doubler circuit that was designed using the same Conexant $0.35\ \mu\text{m}$ BiCMOS process.

The input signal at 1.2 GHz is first applied to the polyphase filter to obtain the quadrature signals necessary for the function of the frequency doubler. The quadrature signals are then applied to the doubler core containing the transistors Q1-Q4. The bias current is set by the voltage at node Bias1 which forces the current in the tail resistor to be 1.2 mA. The output voltage at double the frequency is then buffered through a differential amplifier formed by Q5-Q6. Fig. 4.23 shows the simulated response of the designed circuit as the input signal voltage is swept at 1.2 GHz and the various harmonics of the output voltage are plotted.

It can be seen from the simulation that at large values of V_{in} , the doubler circuit

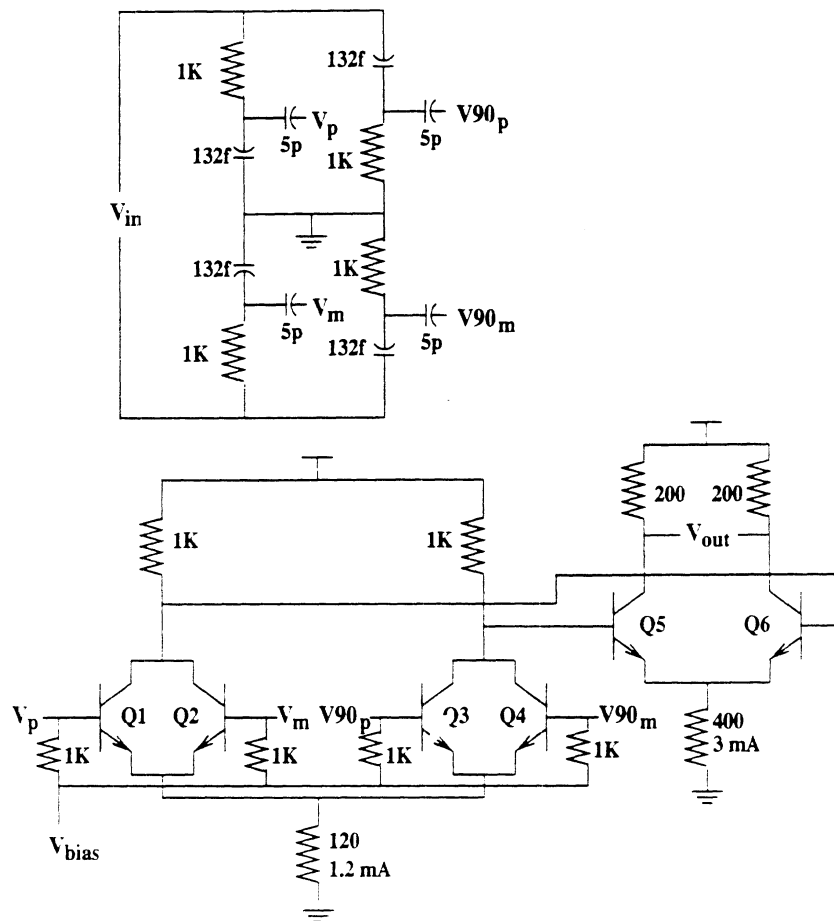


Figure 4.22: Balanced frequency doubler circuit schematic.

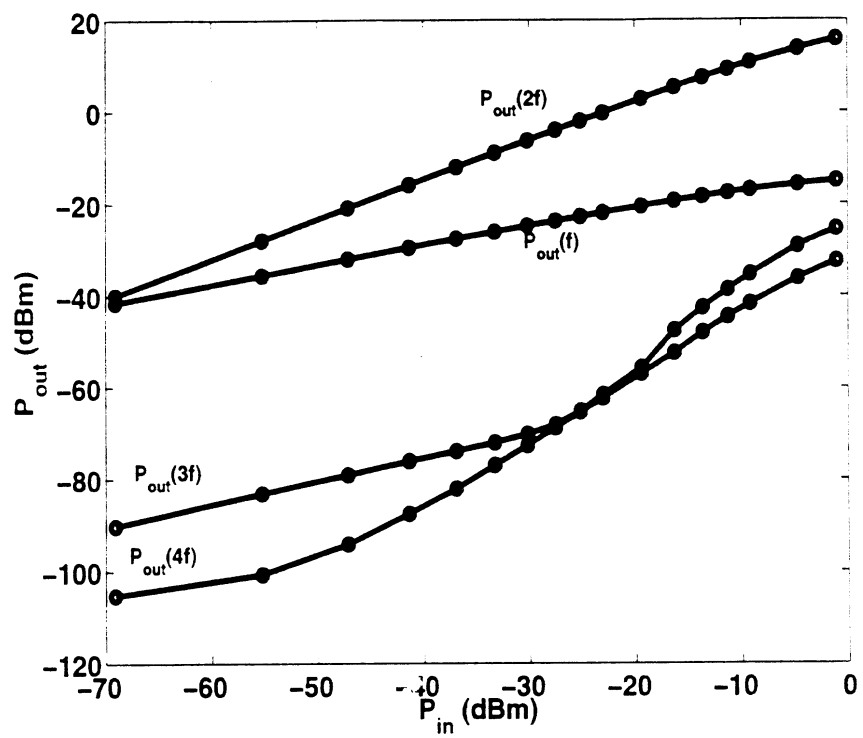


Figure 4.23: Simulated response of the balanced frequency doubler with input at 1.2 GHz

performs well with more than 30 dB of isolation between the $2f_{in}$ component and other frequency components at the output. At small values of V_{in} , the output shows a frequency component at f_{in} that is very close to the $2f_{in}$ component. This is due to a mistake in the design. Due to the quadrature nature of the input signal driving transistors Q1-Q4, the common emitter point of the four transistors gets modulated with the input signal. This in turn modulates the bias current and shows up at the output voltage. This problem can be reduced by using better current sources with higher output impedances.

4.8 Balanced Frequency Doubler Test & Measurement Results

Fig. 4.24 shows a photomicrograph of the balanced doubler fabricated in Conexant's $0.35\ \mu\text{m}$ BiCMOS process. The balanced frequency doubler die was mounted on a test board similar to the one used for the SDBM chip testing. The LO probe used for the testing of the SDBM was used as the input signal probe and the RF probe used for the testing of the SDBM was used as the output signal probe of the balanced frequency doubler circuit under test.

As was the case with the SDBM circuit, the measured response of the frequency doubler showed a shift in frequency. All the measurements discussed below are done with an input at a frequency of 900 MHz and the resulting output at 1.9 GHz. Fig. 4.25 shows the output power of the doubler at various harmonics as the input power is swept.

It should be noted that the simulation results presented earlier in Fig. 4.23 are at an input frequency of 1.2 GHz, while the measured results shown in Fig. 4.25 are at

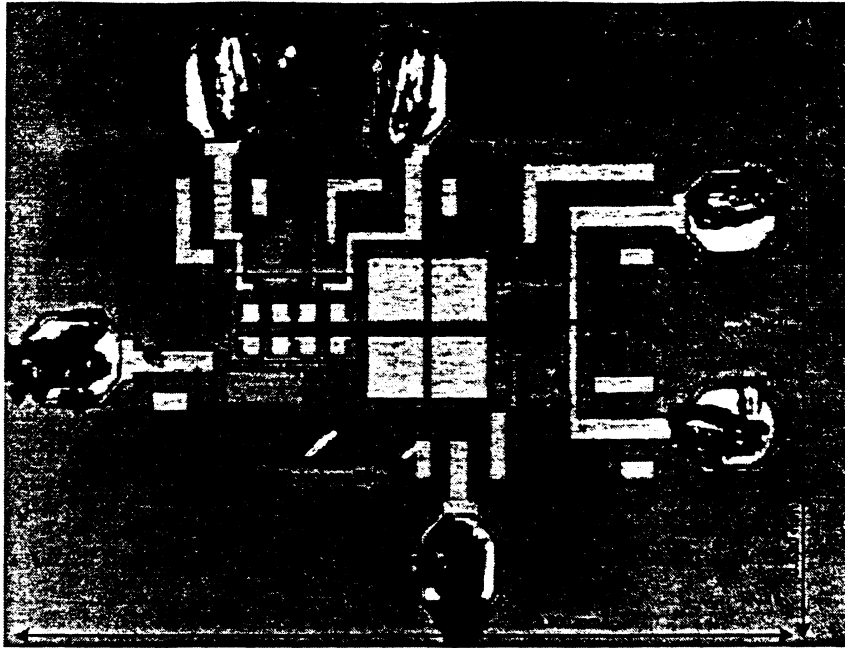


Figure 4.24: Photomicrograph of the balanced frequency doubler circuit

an input frequency of 900 MHz. The simulation results at 900 MHz are not presented here since the polyphase filter is designed to work at 1.2 GHz, and simulation results at 900 MHz will not give an accurate representation of the operation of the circuit. It should also be noted that the input and output ports while measuring the doubler were not matched and the plot above does not give an accurate value of the gain of the frequency doubler circuit. In a real RFIC application using the frequency doubler circuit, the impedance mismatch should not be a problem since the size of the core is small enough to consider the output as a voltage signal.

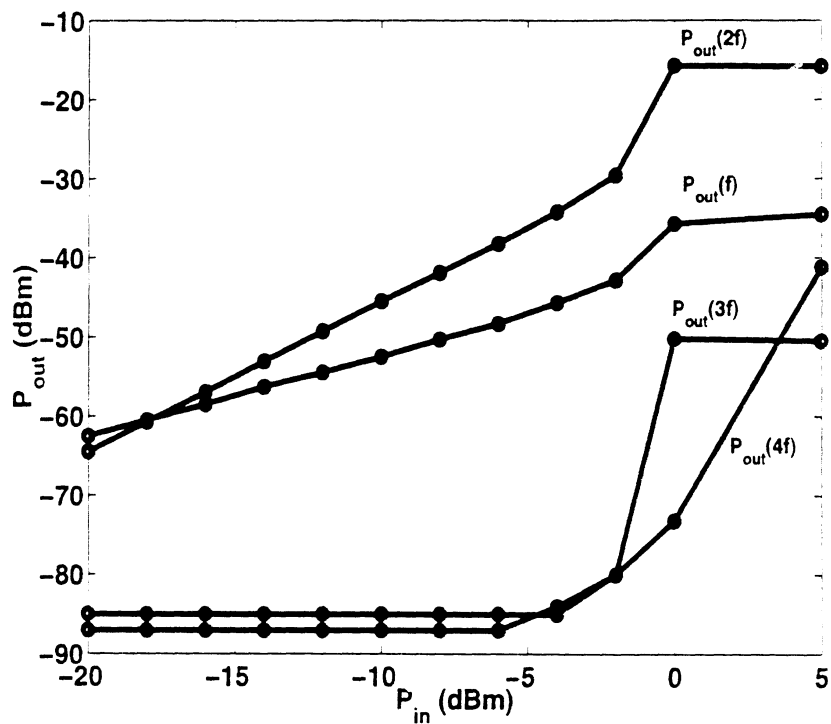


Figure 4.25: Measured response of the balanced frequency doubler with input at 900 MHz

CHAPTER 5

IMPROVING SDBM LINEARITY

5.1 Introduction

One of the big problems with the circuit topology of the SDBM described in the previous sections is that the RF section cannot be linearized independent to the mixing process which is inherently nonlinear. The circuit topology shown in Fig. 5.1 solves this problem. The DC transfer characteristic of this topology that is presented at the end of this chapter shows that the operation of this circuit topology is very similar to the operation of the SDBM circuit. The RF section is formed by transistors Q1-Q2 and can be varied quite a bit to improve the linearity of the mixer as will be shown in subsequent sections. The LO section is formed by transistors Q3-Q10 and replaces the quad transistors in the traditional Gilbert mixer with the equivalent doubling configuration. The LO section is driven by quadrature signals to achieve subharmonic mixing as explained in the previous chapters.

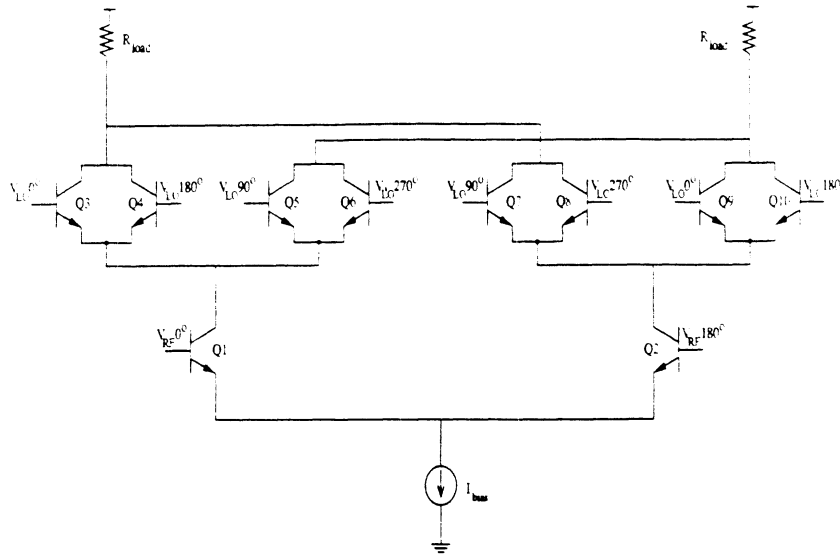


Figure 5.1: Circuit topology for a more linear subharmonic mixer

5.2 Linearizing the RF Section

The linearity of the RF section consisting of a differential pair transconductor in the linear SDBM presented above can be improved using several techniques. The most straight forward technique is to use emitter degeneration in the RF section. In this case, the mixer gain (and noise figure when resistively degenerated) is traded off for linearity. The high frequency nonlinearity analysis equations presented in [20] show that for a degenerated differential pair transconductance stage, the mixer IIP3 is improved with increase in the bias current. It also shows that transconductance stages with inductive degeneration have smaller input-referred third order intermodulation than those with resistive or capacitive degeneration.

Fong et al. [20] also show that a common-emitter transconductance stage can be biased at a lower current than a differential-pair transconductance stage with the same linearity and transconductance. But this will involve a trade-off of choosing a single balanced mixer over a double balanced mixer topology which will provide better

RF rejection at the IF port.

The multi-tanh technique presented by Gilbert in [5] can be used as another alternative to linearize the RF section transconductance stage. In the basic form of this method, two differential pairs are operated in parallel each with a base offset voltage which splits the individual g_m functions along the input voltage axis. The sum of these shifted g_m 's extends the input voltage range (Fig. 5.2) and provides an overall transconductance that is linear over this extended range.

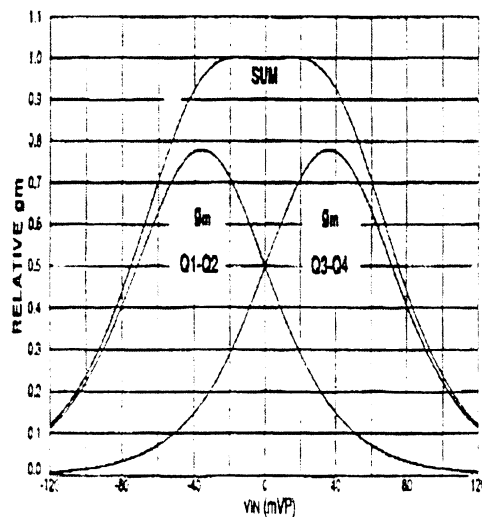


Figure 5.2: Extending input range using the multi-tanh technique: g_m for a multi-tanh doublet(after [5]).

Another alternative is to use transformers instead of a transconductance stage in the RF stage. As has been discussed previously, the input devices of the transconductance stage are the biggest sources of non-linearity in the mixer. If these devices are eliminated, the mixer linearity performance can be dramatically improved. Fig. 5.3 shows a typical implementation of this concept. It is important to use cascode devices in the RF section before the RF signal currents are fed in the LO section. The

cascode devices provide isolation between the LNA and the mixer and also provide isolation between the RF and LO ports of the mixer.

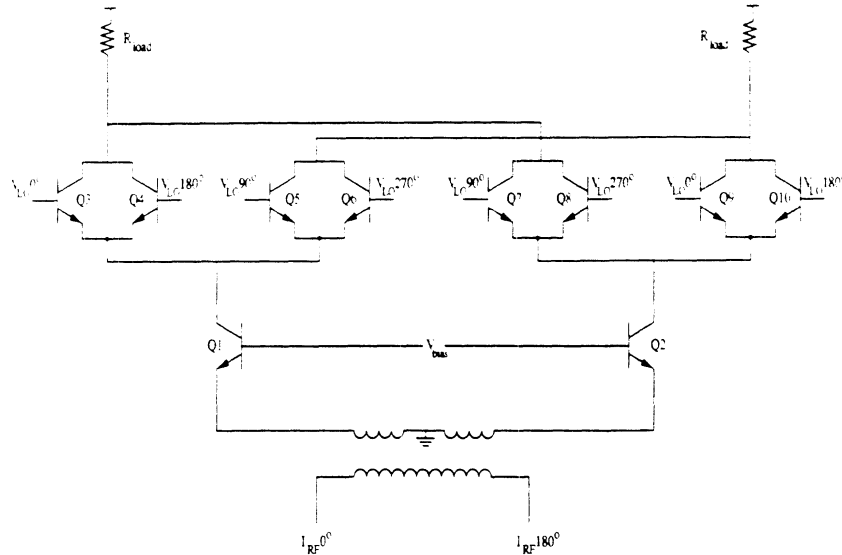


Figure 5.3: Linear SDBM circuit utilizing a transformer in RF section

5.3 Design of Linear Subharmonic Mixers

In this section, simulation results in Cadence SpectreRF will be presented for a linear subharmonic mixers utilizing the ideas discussed in the previous section.

5.3.1 Linear SDBM design

The first design is based on the SDBM design utilizing Conexant's $0.35 \mu\text{m}$ BiCMOS process as discussed in Chapter 4. The circuit schematic of the linear SDBM is shown in Fig. 5.4. Transistors Q1-Q2 form the RF section of the mixer. As in the previous SDBM design the 100Ω tail resistor is used to set the bias current of the mixer at 8 mA through a similar bias generator as discussed before. The bias current was not modified from the SDBM design to provide a good basis for comparison of

the linear SDBM with the SDBM design. The LO section transistors are now half the size of the transistors used in the previous SDBM design, while the RF section transistors are double the size. This keeps the current density in both the RF and LO section transistors at the same level as before ensuring the bias point corresponds to about 70 percent of the bias current corresponding to peak f_T of the bipolar devices. The RF section is linearized using the same degeneration inductors used as in the SDBM design and have an inductance of 0.8 nH each.

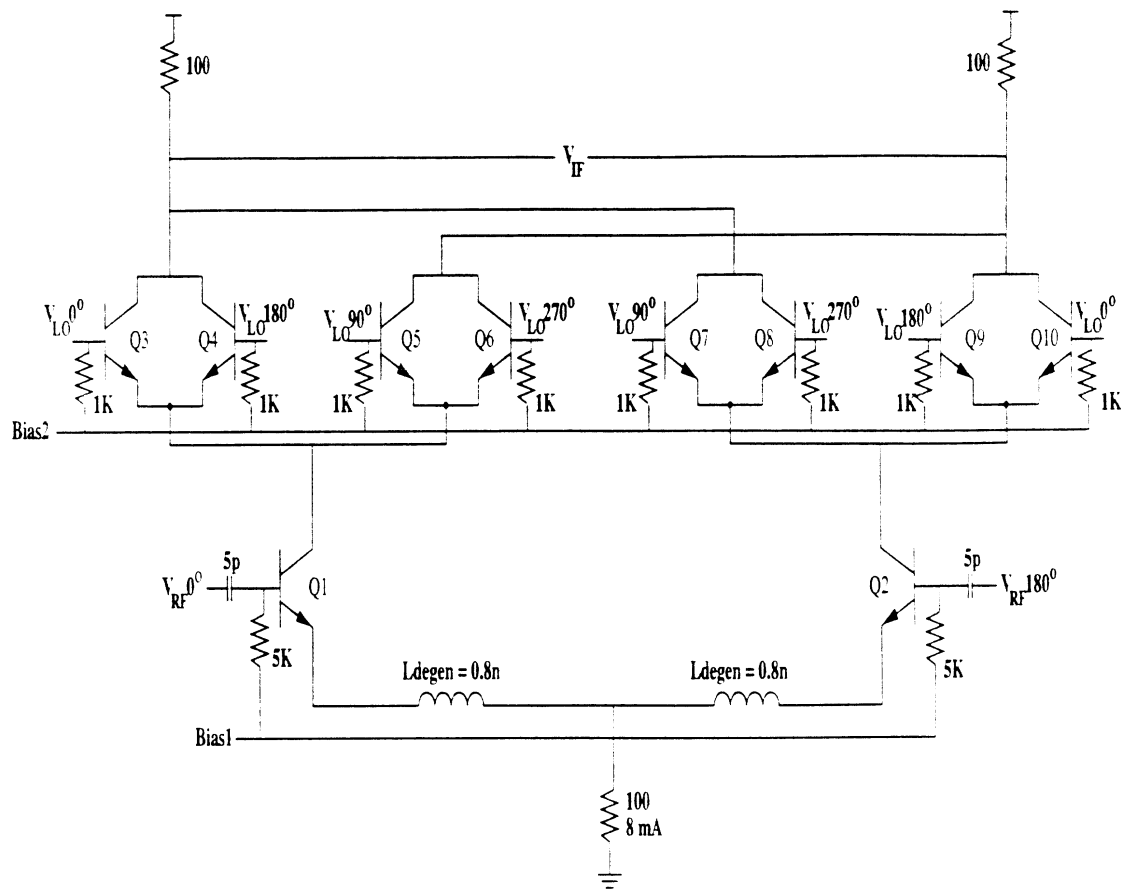


Figure 5.4: Circuit schematic of the linear SDBM.

A simplified schematic of the LO path used in the linear SDBM is shown in Fig. 5.5. This included the first LO buffer, the polyphase filter to generate the quadrature LO

signals and the second LO buffers which operate as limiters. A few changes were made in the design of the LO buffer from the things learnt from the SDBM test and measurement results and from more experience in designing mixers. The limiting buffers now have transistors Q28-Q31 which are cascode devices that improve the frequency response of the buffers. This allows the LO waveform appearing at the mixer to have a better characteristic for linearity performance. Also, the polyphase filter design is modified to have a better chance of achieving the targeted center frequency of 1.2 GHz. The capacitors in the filter were increased to minimize the effects of fringing capacitance. This comes at the expense of increasing the area taken up by the filter.

This design was simulated in Cadence SpectreRF with comparable results to the SDBM design. The various mixer performance metrics that were simulated using this design are summarised in Table 5.1.

Supply Voltage	3 V
Mixer Core Current	8 mA
LO Frequency	1.2 GHz
RF Frequency	2.5 GHz
Conversion Gain	13.6 dB
IIP3	-5 dBm
DSB Noise Figure	7.1 dB

Table 5.1: Summary of linear SDBM simulated results with $L_{degen} = 0.8$ nH

The design described above can be further optimized for linearity by trading off the gain and some noise figure. This can be easily accomplished by increasing the degeneration inductance used in the RF section of the linear SDBM. Fig. 5.6 shows the tradeoffs involved by plotting the mixer gain, noise figure and IIP3 versus the degeneration inductance used in the RF section of the mixer. As can be seen from

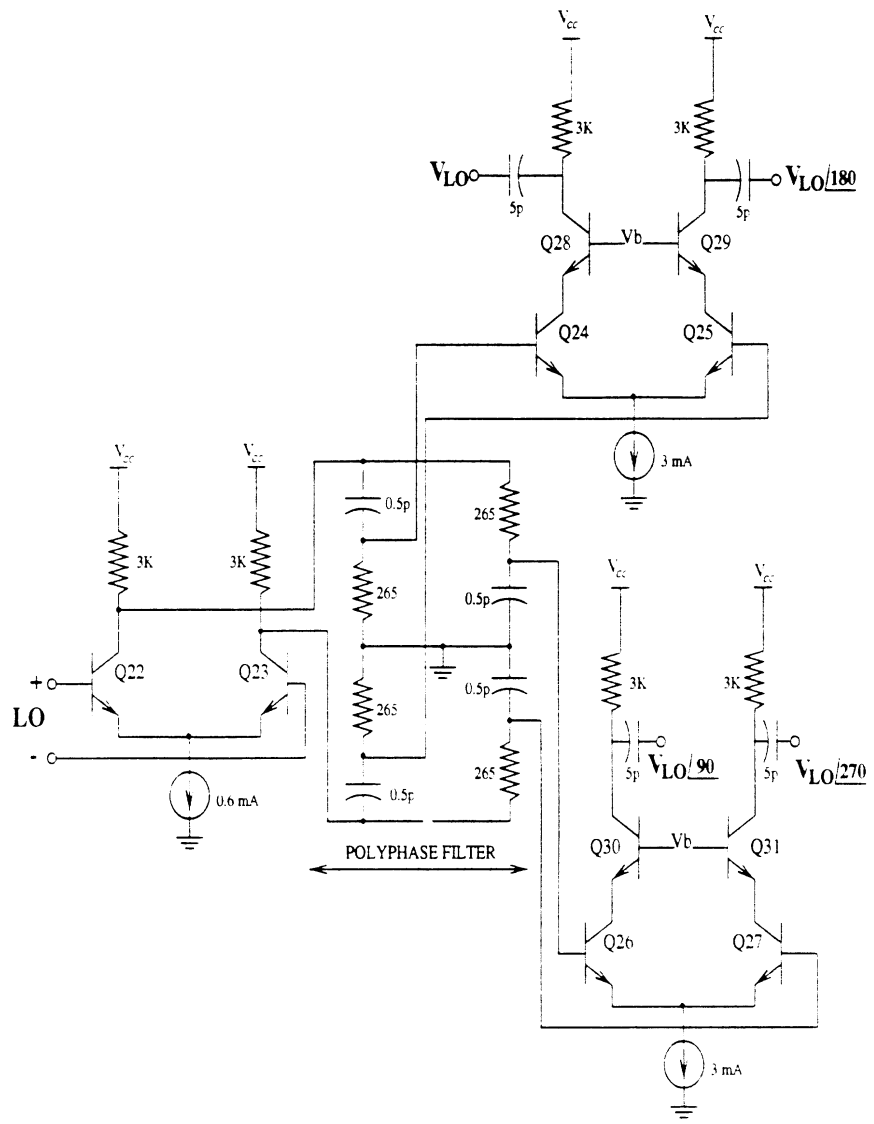


Figure 5.5: LO path for the linear SDBM design

the figure, as the degeneration inductance is increased from 0.8 nH to 2.5 nH, a improvement of 8 dB can be obtained in IIP3 with a corresponding degradation of 2 dB in noise figure of the linear SDBM.

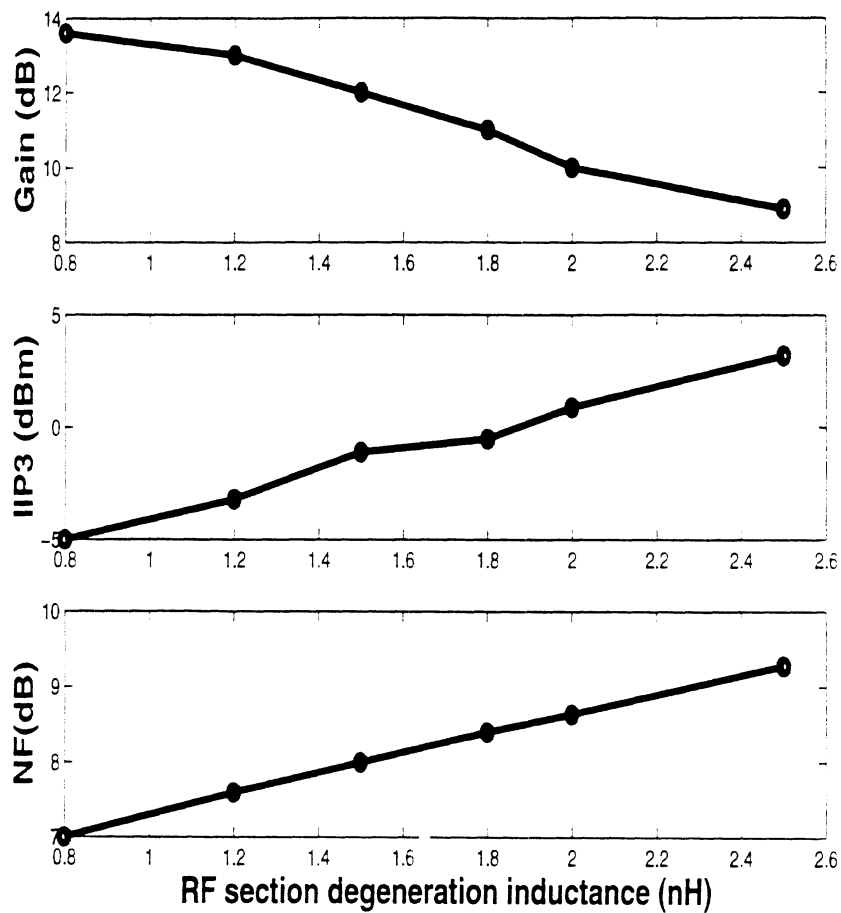


Figure 5.6: Simulated linear SDBM Gain, IIP3 and Noise Figure versus RF section degeneration inductance.

5.3.2 Transformer-based Linear SDBM Design

Modern RFIC process technologies provide the capability to use planar inductors and transformers to add another dimension of creativity and design flexibility. From

the observation that the biggest contribution to the non-linearity of the RF section is the transconductance devices, the linearity of an active mixer can be improved by eliminating these transconductance devices. The differential output current from the LNA can be directly fed into the mixer through the use of a balun/transformer. This improves the mixer IIP3 performance a lot. The disadvantage is that the mixer design will have to be coupled closely to the design of a very high gain LNA to compensate for the lower voltage gain and poorer noise performance of this type of mixer. A similar idea has been explored in [21], but the idea was not extended to the design of highly linear mixers.

A subharmonic mixer utilizing this idea was implemented using the balun available in the Conexant 0.35 μm BiCMOS process. For the sake of comparison with the linear SDBM design of the previous section, the bias current in transformer-based design was kept at the same 8 mA. Fig. 5.7 shows the circuit schematic of the mixer used to implement this design. The LO path of the design is essentially the same as that in the linear SDBM design and is shown in Fig. 5.5.

The cascode devices Q1-Q2 are used to convert the incoming RF signal into the current domain. The RF currents are then commutated using the LO switching transistors. The linearity of this mixer topology is limited by the non-linearity of the current gain in the cascode devices (which essentially depends on the non-linearity of the β of the RF section transistors) and the non-linearity contributed by the LO section transistors when they are driven hard as switches. Hence, the LO drive has to be limited so as not to degrade the linearity of the mixer. Since there is no voltage gain ahead of the LO switching section as in the linear SDBM, the LO section transistors dominate the noise performance. When the LO section transistors are turned on hard, they appear as cascode devices and their noise contribution is minimal. But, when

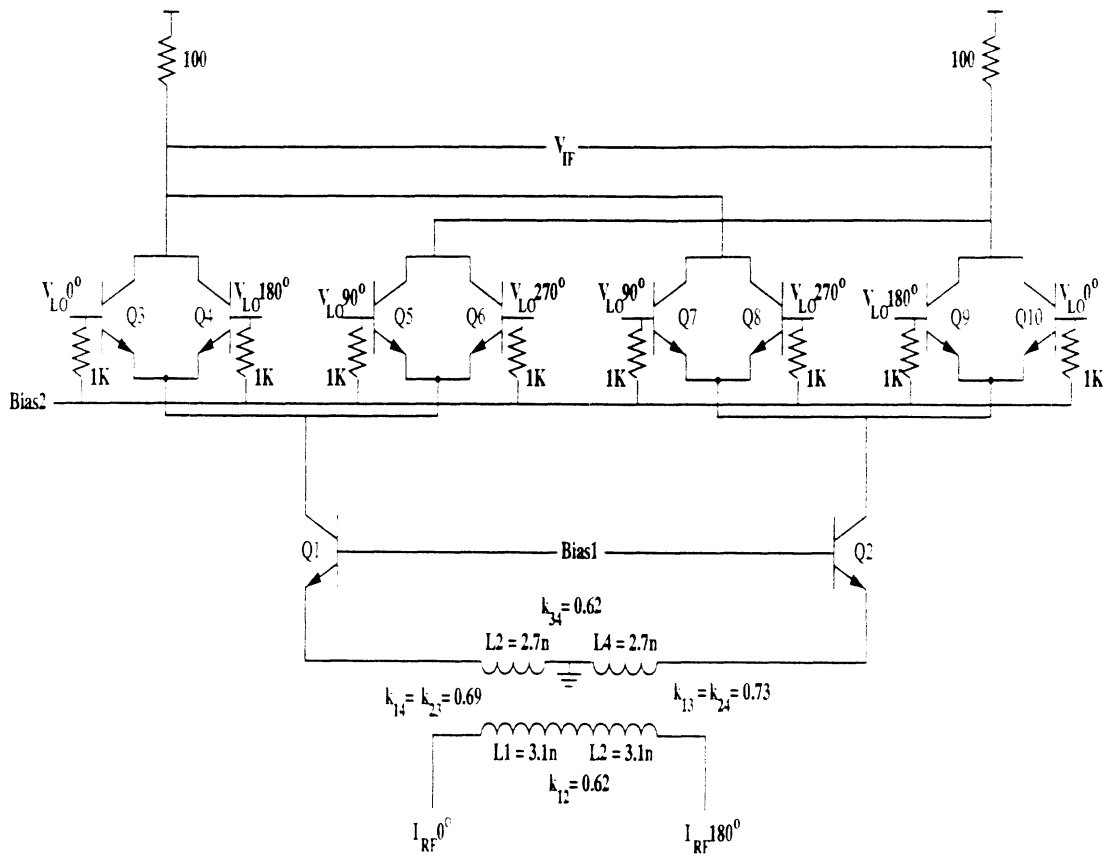


Figure 5.7: Circuit schematic of the linear SDBM with a transformer-based RF section.

the LO section transistors are in transition, the LO section appears as a combination of differential pairs and the transistor noise gets amplified to the output. Hence, the LO drive has to be as high as possible for the noise figure of the mixer to be minimized. Thus, the LO drive provides a classic trade-off between the linearity and noise performance of the mixer, and is chosen to be 450 mV_{pk} at the mixer. The dominant noise contributors in this topology are the collector current shot noise and the extrinsic base resistance thermal noise of the LO section transistors Q3-Q10.

Since this kind of mixer needs to be designed closely with the preceding LNA, all the simulated performance metrics of the mixer will be presented in voltage units rather than power units as is the custom. If the mixer were to be operated as a discrete component, the input and output of the mixer would have to be matched and using power units would be appropriate. But, this topology is by design meant to be used in an integrated receiver type application and in such a case there is no need to match the mixer to the traditional 50Ω .

Supply Voltage	3 V
Mixer Core Current	8 mA
LO Frequency	1.2 GHz
RF Frequency	2.5 GHz
Voltage Conversion Gain	4.5 dB
IIP3	$2.2 \text{ dBV} = 9.2 \text{ dBm} _{50 \Omega}$
Equiv Input Noise	$2.6 \text{ nV}/\sqrt{\text{Hz}}$

Table 5.2: Summary of transformer based linear SDBM simulated results.

The simulated performance metrics of the transformer based linear SDBM are shown in Table 5.2. Compared to the linear SDBM, the transformer based linear SDBM has about 14 dB to 6 dB (depending on the degeneration inductance in the linear SDBM design) better IIP3. Since this design was not matched at the RF

input, the noise performance cannot be specified by noise figure and the equivalent input noise is used as a performance metric. The transformer-based design has a higher equivalent input noise voltage of $2.6 \text{ nV}/\sqrt{\text{Hz}}$ as compared to the $1.9 \text{ nV}/\sqrt{\text{Hz}}$ of the linear SDBM. But, the output noise in both cases is comparable due to the lower gain in the transformer based design. Thus, in applications that demand high linearity, this mixer topology shows promise when it is preceded by a high gain low noise amplifier.

5.3.3 CMOS Subharmonic Mixers

The Gilbert cell mixer topology can be implemented using CMOS devices too, and the the quadratic nature of the devices as opposed to the exponential behaviour of bipolar devices lends this implementation for better linearity when compared to bipolar active mixers carrying the same current. One drawback with CMOS active mixers is that they tend to have significantly higher noise figure than their bipolar counterparts. The subharmonic mixer topology discussed so far in bipolar implementations can be adapted for CMOS processes also

5.4 Linear SDBM Analysis

5.4.1 DC Transfer Function

The Linear SDBM circuit topology has a DC transfer function that is very similar to the transfer function of the SDBM presented earlier. The reader should refer to Fig. 5.8 for the circuit diagram and the various current definitions. As in the case of the SDBM analysis, it is assumed that the bias current source I_{EE} has infinite output resistance, that the base resistance of each transistor is negligible, and that

the output resistance of each transistor is infinite.

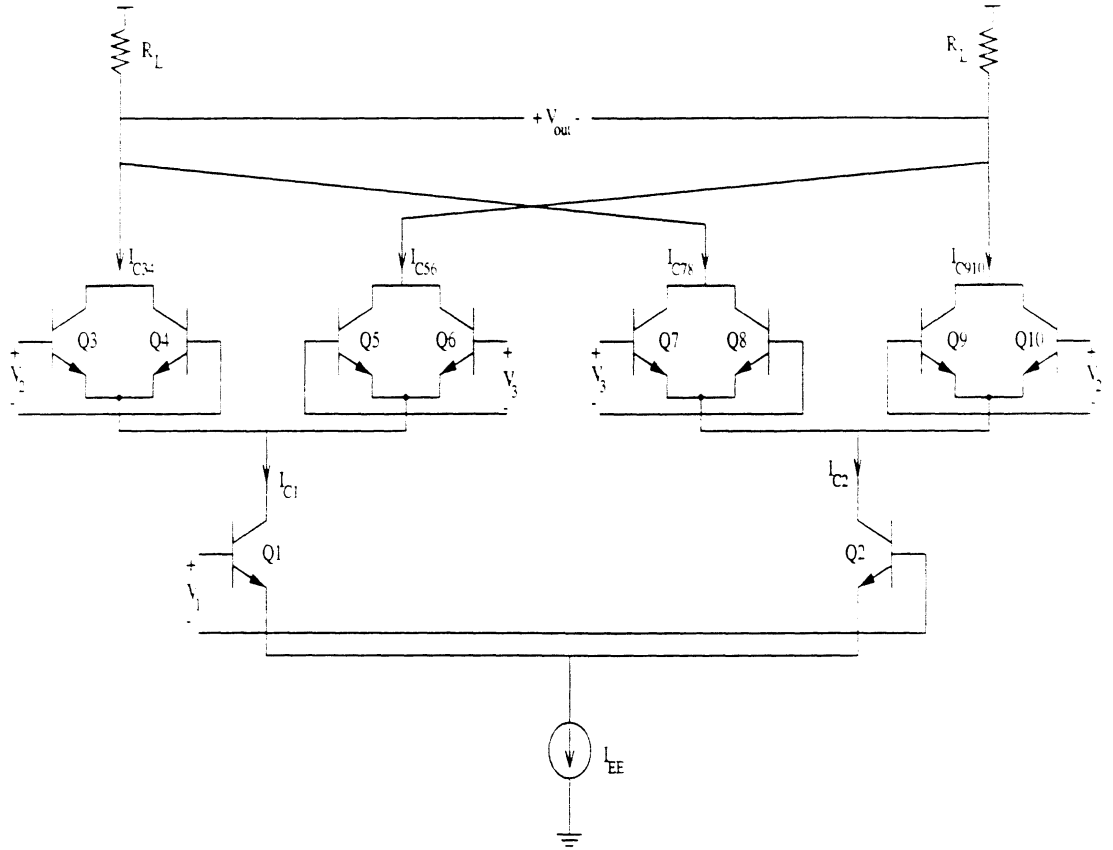


Figure 5.8: Circuit schematic of the linear SDBM for DC transfer characteristic analysis

Transistors Q1-Q2 form an emitter-coupled differential pair, and their collector currents are given by [14]:

$$I_{C1} = \frac{\alpha_F I_{EE}}{1 + e^{-\left(\frac{V_1}{V_T}\right)}} \quad (5.1)$$

$$I_{C2} = \frac{\alpha_F I_{EE}}{1 + e^{\left(\frac{V_1}{V_T}\right)}} \quad (5.2)$$

Now, realizing that transistors Q3-Q6 and I_{C1} form a similar circuit topology as transistors Q1-Q4 and I_{EE} in Fig. 3.4, and doing similar algebra as in equations 3.1 to 3.11, we get:

$$I_{C34} = \left(\frac{\gamma}{1+\gamma} \right) \alpha_F I_{C1} \quad (5.3)$$

$$I_{C56} = \left(\frac{1}{1+\gamma} \right) \alpha_F I_{C1} \quad (5.4)$$

where, γ is given by:

$$\gamma = \frac{1}{e^{\left(\frac{V_2+V_3}{2V_T}\right)}} \times \frac{1 + e^{\left(\frac{V_2}{V_T}\right)}}{1 + e^{\left(\frac{-V_3}{V_T}\right)}} \quad (5.5)$$

Similarly, for transistors Q7-Q10:

$$I_{C78} = \left(\frac{1}{1+\gamma} \right) \alpha_F I_{C2} \quad (5.6)$$

$$I_{C910} = \left(\frac{\gamma}{1+\gamma} \right) \alpha_F I_{C2} \quad (5.7)$$

The output voltage is given by:

$$V_{out} = (I_{C34} - I_{C78} - I_{C56} - I_{C910}) \times R_L \quad (5.8)$$

Substituting equations 5.3-5.4 and 5.6-5.7 in 5.8, and simplifying the algebra, we get:

$$V_{out} = \left(\frac{1-\gamma}{1+\gamma} \right) \alpha_F^2 I_{EE} R_L \tanh \left(\frac{V_1}{V_T} \right) \quad (5.9)$$

which is very similar to the output voltage derived for the SDBM circuit. For low frequency applications where linearity is not a concern, both the linear SDBM and SDBM topologies with ideal circuit elements have exactly the same output voltage.

5.4.2 Noise Performance of Linear SDBM

Both the RF and LO section transistors contribute to the noise figure of the linear SDBM presented in the previous section. The noise contribution of the RF section is analyzed quantitatively, while the LO section noise contribution is analyzed qualitatively.

For the noise contribution of the RF section, which is an emitter-degenerated differential pair, the output noise contribution is calculated due to each of the noise sources in the RF section devices. This output noise is divided by the transconductance to give the input referred noise power and compared to the noise power generated by the source resistance to obtain the noise figure of the RF section of the mixer [22].

Fig. 5.9 shows the small-signal noise model used to derive the noise contribution of the RF section. It can be seen that the circuit is symmetrical and the half-circuit concept can be used to derive the noise figure. In this model, Z_b is used to model the base extrinsic resistance and any series matching impedance. Z_π is the base-emitter impedance and it includes C_π , r_π , and C_b . R_S is the source resistance driving the mixer, and Z_{in} is the input impedance of the RF section. The C_μ of the transistors Q1-Q2 is neglected in this model. The output impedance of the bias current source can be absorbed into Z_E , when needed to be taken into account. The noise figure contributions can be divided into three different sources - collector shot noise ($\overline{i_c^2} = 2qI_Q$), base shot noise ($\overline{i_c^2} = 2qI_Q/\beta$), and thermal noise contribution from the

resistive components of Z_b and Z_E .

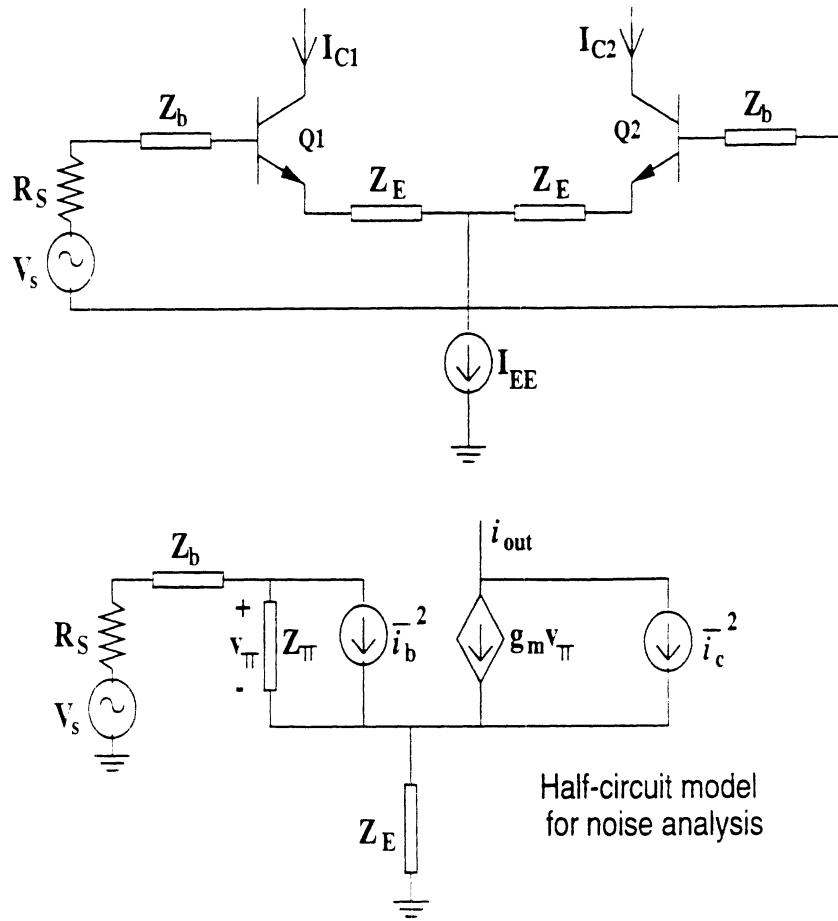


Figure 5.9: Linear SDBM RI section model for noise analysis

The output noise current power due the collector shot noise is $2qI_Q$. And, the transconductance i_o/v_s is $g_m v_\pi/v_s$ and can be derived as $g_m Z_\pi/(Z_\pi + Z_b + Z_E + R_S)$ and the equivalent input noise power due to the collector shot noise is given by:

$$\overline{v_{nc}^2} = \frac{2qI_Q \times (Z_\pi + Z_b + Z_E + R_S)^2}{(g_m Z_\pi)^2} \quad (5.10)$$

where $g_m = I_Q/V_T = I_{EE}/(2V_T)$ and, the noise factor contribution due to the collector shot noise can be obtained by dividing $\overline{v_{nc}^2}$ by the noise power due to the source resistance ($4kTR_S$), which when simplified gives:

$$F_{collector} = \frac{|R_S - Z_b + Z_E - Z_\pi|^2}{2g_m Z_\pi^2 R_S} \quad (5.11)$$

The output noise current power due to the base shot noise is given by $((Z_E - R_S - Z_b) \parallel Z_\pi)^2 \times 2qI_Q/\beta$. Using the same transconductance as in the case of the collector shot noise, the equivalent input noise power due to the base shot noise can be derived as:

$$\overline{v_{nb}}^2 = \frac{2qI_Q \times (Z_E + R_S + Z_b)^2}{3g_m^2} \quad (5.12)$$

Once again, the noise factor contribution due to the base shot noise can be obtained by dividing $\overline{v_{nb}}^2$ by the noise power due to the source resistance ($4kTR_S$), which when simplified gives:

$$F_{base\epsilon} = \frac{g_m |R_S + Z_b + Z_E|^2}{2\beta R_S} \quad (5.13)$$

Finally, the output noise current power due to the thermal noise in Z_b and Z_E is given by $(\frac{g_m Z_\pi}{Z_\pi - Z_b - R_S - Z_E})^2 \times 4kTRc(Z_b + Z_E)$ and the equivalent input noise due to the thermal noise sources is given by:

$$\overline{v_{nt}}^2 = 4kTRc(Z_b + Z_E) \quad (5.14)$$

And, the noise factor contribution due to the thermal noise in Z_b and Z_E is given by:

$$F_{thermal} = \frac{Rc(Z_b + Z_E)}{R_S} \quad (5.15)$$

Using equations 5.11, 5.13, 5.15, the overall noise factor (linear) of the RF section can be expressed as:

$$F = 1 + 2(F_{\text{collector}} + F_{\text{base}} + F_{\text{thermal}}) \quad (5.16)$$

and, noise figure $NF = 10\log(F)$ in dB.

From the equations above, it can be seen that the collector shot noise contribution to the noise figure can be reduced by increasing g_m , which can be done by increasing the bias current. The base shot noise contribution has an opposite dependence on g_m and is reduced by decreasing g_m . Hence, there is an optimum bias current where the total shot noise contribution is a minimum. R_S provides another degree of optimization to minimize the total shot noise contribution to noise figure, while the thermal noise contribution decreases as R_S increases. Unlike discrete mixers where R_S is typically fixed at 50Ω , in integrated circuit mixers R_S is the resistive part of the output impedance of the LNA preceding the mixer and can be used as a design variable to optimize the overall noise figure of the receiver. The thermal noise contribution can be reduced by making the device size as large as possible in order to reduce the extrinsic base resistance. Multiple finger base-emitter junctions can be used in layout to reduce this base resistance further. As the RF section device size increases, C_μ increases and this hurts the linearity of the transconductance stage, increases feedback from the collector to the base, reducing gain and making impedance matching difficult. Thermal noise contribution can also be kept to a minimum by using inductors for emitter degeneration instead of resistance. This comes at the expense of the much larger die areas of inductors.

The noise contribution from the LO stage switching transistors is much more difficult to analyze quantitatively and needs highly mathematical treatment [23]. The factors that the circuit designer has control over that can enable the minimization of this noise contribution are LO drive, LO waveform shape, and LO section transistor

sizing.

When the LO drive is high enough to turn one side of the LO section on and the other side off, the LO section devices appear as cascode devices and their noise contribution is minimized. Hence, large LO signal amplitudes are preferred to reduce the noise contribution of the LO section transistors. But, a large LO drive reduces the linearity of the switching stage. In bipolar transistor implementations of monolithic mixers, LO signal amplitudes between 300-500 mV are used to achieve low noise figure with acceptable linearity [24][25][19].

If the LO waveform is approximated as a square wave at a frequency of $2f_{LO}$, noise power at $2f_{LO} \pm f_{RF}$, $6f_{LO} \pm f_{RF}$, $10f_{LO} \pm f_{RF}$ etc. will be downconverted to the IF port and appear as output noise as shown in Fig. 5.10. Assuming that the transconductance and output noise power of the RF section are constant at all frequencies, the LO switching stage will increase the input referred noise contribution from the RF section by a factor of $(\frac{\pi}{2})^2 = 3.9$ dB [23]. But, if the switching operation is done by a sine wave, the input referred noise contribution from the RF section would be increased by a factor of 2 (3 dB) due to the mixing of noise down from both the RF frequency and the image frequency. In practical circuit applications, this factor will be somewhere between 3 and 3.9 dB. It should be noted here that while the ideal LO waveform for a Gilbert cell mixer is close to a square wave, the LO section of the linear SDBM design cannot be a square wave for subharmonic mixing to happen and needs to be closer to a sine wave. This is due to the rectification action of the doubling pairs of transistors that replace the LO quad in the traditional first harmonic mixer.

To reduce the thermal noise contribution from the base resistance, r_b of the LO section transistors, the device sizes must be reasonably large. Once again, there is a tradeoff with linearity as large device sizes lead to a large $C_{j\epsilon}$ and switching of $C_{j\epsilon}$

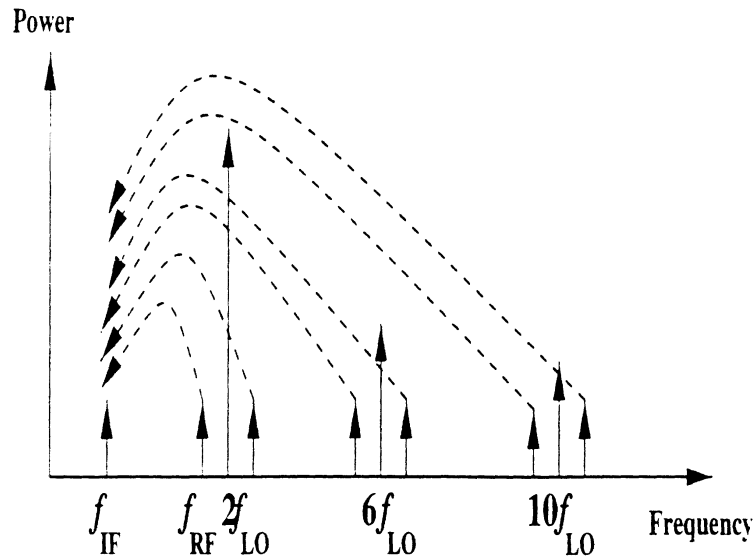


Figure 5.10: LO harmonics mix noise down to IF

with the large LO signal reduces the mixer linearity.

5.4.3 Linearity Performance of Linear SDBM

As in the case of the noise performance, both the RF section and the LO section of the linear SDBM contribute to the linearity of the mixer. Once again, the RF section can be analyzed quantitatively and the LO section contribution is dealt with qualitatively due to the large signal behavior.

Fong and Meyer [20][22] derive the analytical expression for the third order intermodulation products for the general case of a differential pair transconductance with emitter degeneration. Since the RF section of the linear SDBM is a differential pair with inductive degeneration, the volterra series equations derived in [20][22] are applicable to the RF section of the linear SDBM too. It was shown that the simplified analytical expression for the third order intermodulation products is given by:

$$|IM_3| \approx |A_1|^3(s) \frac{V_T}{2I_{EE}^3} \times (1 + sC_{je}Z_b(s) + sC_{je}Z_E(s)) \times |V_s|^2 \quad (5.17)$$

where, $A_1(s)$ is given by

$$A_1(s) = \frac{g_m}{2 \times (1 + sC_{je}Z_b(s) + Z_E(s) - s\tau_F g_m Z_b(s) + Z_E(s) + g_m Z_b(s)/\beta - Z_E(s)/\beta - g_m Z_E(s))} \quad (5.18)$$

where, $g_m = I_{EE}/2V_T$.

It can be seen from equations 5.17 and 5.18 that $|IM_3|$ depends on the magnitude of $1 + sC_{je}Z_b(s) + sC_{je}Z_E(s)$, and hence a differential pair stage with inductive degeneration is more linear than a stage with resistive degeneration, which in turn is better than capacitive degeneration. Also, the value of $|IM_3|$ is proportional to the cube of the ratio of the small signal transconductance of the RF section devices (through the numerator of $A_1(s)$) to the bias current (I_{EE}).

The LO section switching transistors also contribute to the IM_3 products at the IF output of the mixer. Up to an extent, increasing the LO drive improves the linearity performance of the LO section. This is because, a higher LO drive helps in keeping one side of the LO section turned on hard and the LO section devices behave as cascode devices which contribute little nonlinearity. But, as the LO signal amplitude increases, switching the base-emitter junction capacitance (C_{je}) of the LO section devices results in excessive current being pumped into the common emitter points of the switching stage through C_{je} [26][23]. Hence, at high LO drives, the linearity of the LO section decreases with increasing LO signal amplitude. For the same reason, the device size of the LO section transistors cannot be arbitrarily increased since this causes an increase in C_{je} and hence worsens the linearity of the LO section. In processes with high f_T , the LO section devices can be made to switch very rapidly and

the overall mixer non-linearity is dominated by the non-linearity of the RF section. But, in processes with low f_T devices, the LO switching stage can be a significant contributor to the non-linearity of the mixer.

5.4.4 Device Mismatch Effects

For the SDBM and linear SDBM designs presented in this thesis, the double-balanced nature of the mixers allow no RF and LO feedthrough to the IF port ideally. In reality, device mismatch effects will cause some feedthrough to the IF port. The effect of device mismatches between the LO section transistors in the linear SDBM design is equivalent to having an amplitude mismatch between the quadrature LO drive signals due to the different loading on the LO buffer outputs. Fig. 5.11 shows the simulated RF feedthrough (relative to the RF input signal level) at the IF port for amplitude mismatch between the I and Q paths of the LO signal driving the mixer. Fig. 5.12 shows the RF feedthrough for phase mismatch between the I and Q paths of the LO signals driving the mixer. The LO feedthrough to the IF port does not show any significant change due to the amplitude and phase mismatches of the I and Q paths of the LO signal driving the mixer. This is due to the large signal switching nature of the LO section of the mixer

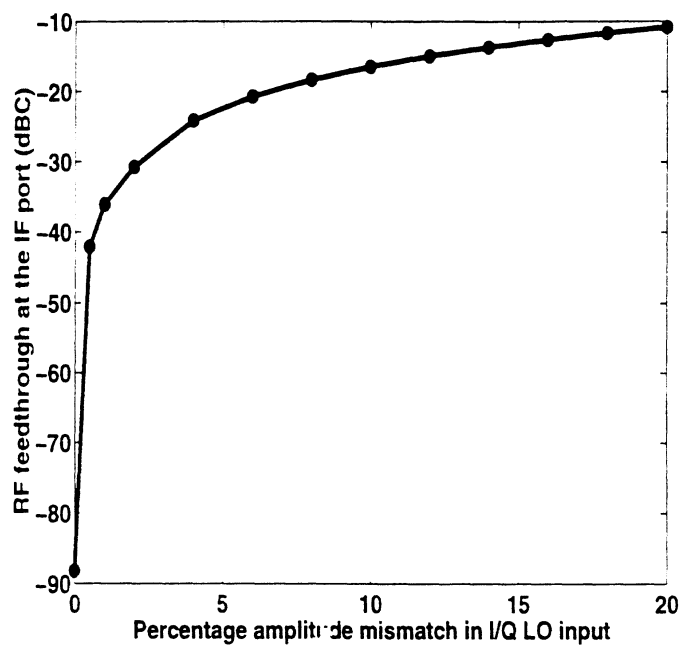


Figure 5.11: RF-to-IF feedthrough due to amplitude mismatch between the I/Q LO signals

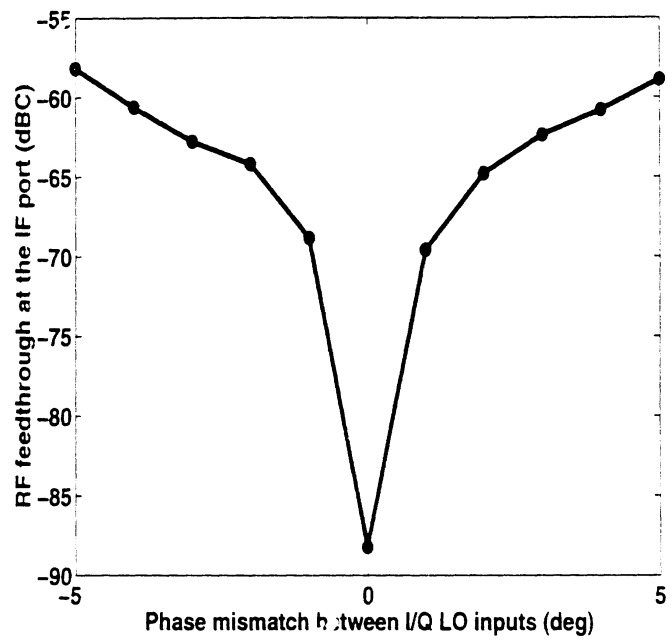


Figure 5.12: RF-to-IF feedthrough due to phase mismatch between the I/Q LO signals

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

This thesis has presented novel circuit topologies for implementation of subharmonic double balanced mixers in RFIC process technologies. The basic SDBM topology was designed and fabricated in SiGe HBT (Maxim GST3) and BiCMOS (Conexant bc35) commercial processes. While the chip designed in the Maxim process did not work functionally during testing of the fabricated die, the Conexant design was tested and measurement results are quite competitive to other subharmonic mixer design implementations. Qualitative and quantitative analyses for the various performance metrics (Gain, IIP3, Noise Figure) for the mixer design were also presented. Finally, simulation results were presented for linearizing the SDBM design.

6.1 n^{th} Harmonic Mixers

The concept of using a quadrature LO to obtain second harmonic mixing can be extended further to the design of higher order subharmonic mixers. The use of this concept for a third harmonic mixer is demonstrated in [4] as multiphase reduced-frequency conversion. The basic idea is that mixing with a single phase high frequency

periodic signal is equivalent to mixing with a set of reduced frequency multi-phase periodic signals. If these signals are sinusoidal, as is the case in most RF systems, this can be demonstrated by the following equations:

$$\cos(\omega_{RF}t) = 2^{\frac{N}{2}-1} \prod_{i=0}^{\frac{N}{2}-1} \sin\left(\frac{2\omega_{RF}}{N} \times t - \frac{2i\pi}{N} - \frac{\pi}{N}\right) \quad (6.1)$$

$$\sin(\omega_{RF}t) = 2^{\frac{N}{2}-1} \prod_{i=0}^{\frac{N}{2}-1} \sin\left(\frac{2\omega_{RF}}{N} \times t - \frac{2i\pi}{N}\right) \quad (6.2)$$

Using this concept, higher order harmonic mixers can be implemented. One of the problems to solve in order for these implementations to work is the design of precise phase shifters that can generate the multi-phase reduced frequency signals. One important application where these type of higher order harmonic mixers can be useful is in the design of fractional-N phase locked loops, where it is critical to choose the frequency plan carefully to avoid unwanted frequency spurs. High frequency implementations of these phase locked loops use mixers for dividing down in frequency and harmonic mixers can be used very effectively in these designs to limit unwanted frequency spurs.

6.2 CMOS Subharmonic Mixers

The Gilbert cell mixer topology can be implemented using CMOS devices too, and the the quadratic nature of the devices as opposed to the exponential behaviour of bipolar devices lends this implementation for better linearity when compared to bipolar active mixers carrying the same current. One drawback with CMOS active mixers is that they tend to have significantly higher noise figure than their bipolar counterparts.

The subharmonic mixer discussed so far in bipolar implementations can be adapted for CMOS processes also. Fig. 6.1 shows a CMOS version of the linear SDBM topology.

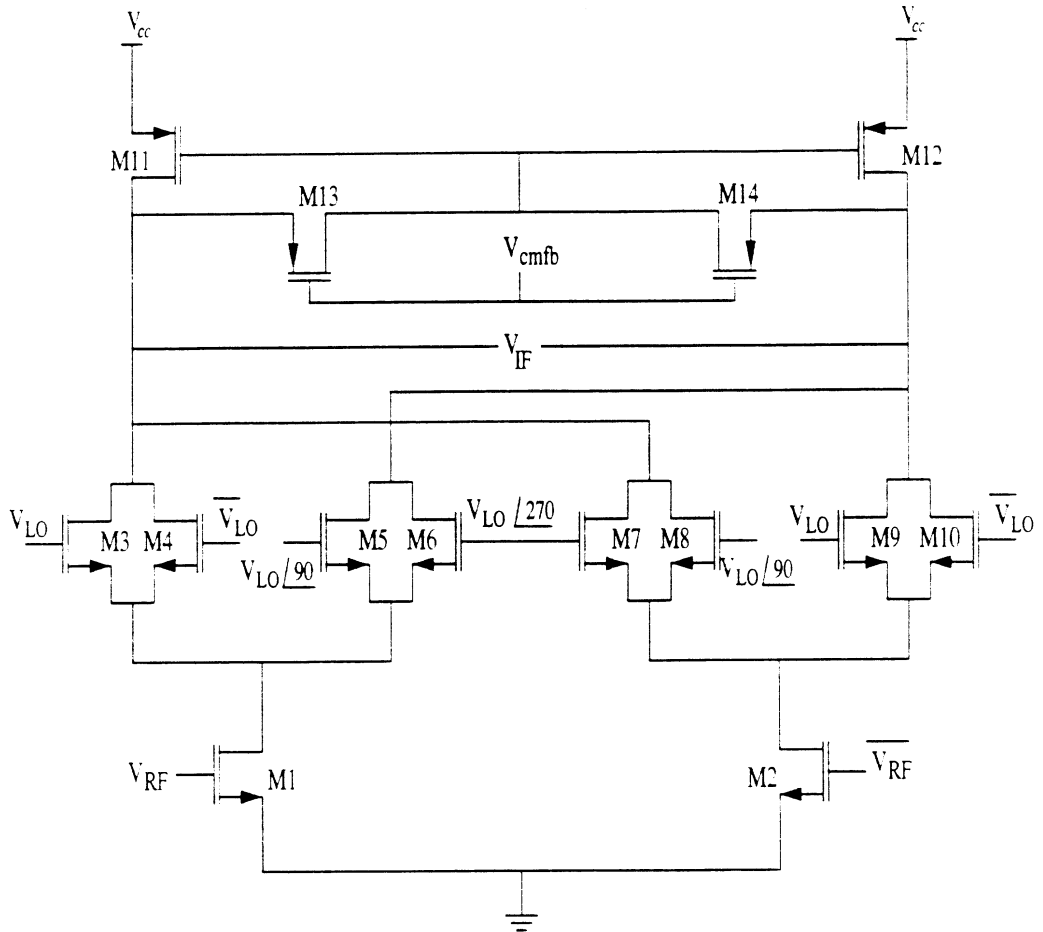


Figure 6.1: Circuit topology for a CMOS subharmonic mixer

Transistors M1-M2 form the RF section, which is a linear transconductance stage. This transconductance stage is more linear than a regular differential pair with a tail current source [27]. This can be seen from the following equations. The differential small signal output current for a differential pair with a tail current source of I_{bias} is:

$$i_{out} = 2\mu C_{ox} \frac{W}{L} v_{in} \sqrt{\left(\frac{2I_{bias}}{\mu C_{ox} \frac{W}{L}} - v_{in}^2\right)} \quad (6.3)$$

where, v_{in} is the small signal differential output voltage. For the case of a linear transconductor shown above which contains two identical common-source MOSFET's biased at the same V_{gs} and driven by a signal v_{in} whose amplitude is less than $2(V_{gs} - V_T)$, the differential output current is given by:

$$i_{out} = 2\mu C_{ox} \frac{W}{L} (V_{gs} - V_T) v_{in} \quad (6.4)$$

which has a linear relation to the differential input signal. Transistors M3-M10 form the LO switching section. MOS technology devices typically have much lower transconductance than their bipolar counterparts and the gain from the linear transconductance stage will not be very high. To get a decent amount of gain from the mixer, active loads need to be used for low-voltage implementations. M11-M12 form the active loads for the mixer, and M13-M14 are necessary to deal with the high voltage swing at the output of the mixer. M13-M14 are biased in the linear region and act as MOS resistors and the center-tap is used to force the common-mode voltage to an optimal point for the output swing through a common-mode feedback network.

6.3 Active Quadrature LO Generation

As was seen in this thesis, generating a quadrature LO signal is essential for the operation of active subharmonic mixers. The implementations shown in Chapters 4 and 5 utilize passive RC-networks in the form of polyphase filters to generate the requisite quadrature LO signals. This method has two disadvantages. One, the polyphase filter has considerable amount of voltage loss (6 dB ideally at resonance, more practically)

and the limited LO power available that is lost in the passive network needs to be boosted again using LO buffers which can consume quite a bit of power. Second, as the frequencies of operation of receivers go up, the R.C component sizes in the polyphase filter network go down and it will be increasingly difficult to obtain these components with acceptably accurate resistance and capacitance. Active quadrature LO generation solves both these problems.

José Cabanillas' excellent work [28] in quadrature VCO design here at the University of Michigan would be a good method of generating quadrature LO signals. The beauty of this approach is that for an integrated receiver with on-chip VCO to generate the LO signal, the quadrature signals are directly available and just need to be buffered (for isolation) before being delivered to the mixer. Care should be taken in layout to ensure that both the I-phase and Q-phase path of the LO have the same parasitic effects on the way to the mixer. There have been several other implementations of quadrature VCO's in literature [29],[30],[31],[32] that can also be used. Using a quadrature VCO along with a subharmonic mixer provides an attractive way of implementing a fully-integrated direct downconversion receiver.

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