033095-1-F

High Efficiency Micromachined Antennas: Micromachined Antennas for Microwave and Mm-Wave applications

FINAL REPORT
ONR Contract: N00014-95-1-0546

Linda P.B. Katehi

March 1997

33095-1-F = RL-2447

Final Report

on

High-Efficiency Micromachined Antennas

by

Linda P.B. Katehi

The University of Michigan

ONR Contract : N00014-95-1-0546

January 1997 – December 1997

Reporting period: January 1997-December 1997

Students and Research Associates:

Kavita Goverdhanam (student)

John Papapolymerou (student)

Jong-Gwan Yook (Research Associate)

Faculty: Linda P.B. Katehi and Gabriel Rebeiz

Other Contributing Students: Rashaunda Henderson and Gildas Gauthier

Other Contributing Research Staff: Kazem Sabet

Manuscripts Published or Submitted During the Reporting Period.

1. Linda P.B. Katehi et.al, Industrial Electronics Handbook, Chapter on "Si Micromachining in High-Frequency Applications," pp. 1547-1575, CRC Press, 1997.
2. I. Papapolymerou, R.F. Drayton and L.P.B. Katehi, "Micromachined Patch Antennas," Accepted for presentation in the *IEEE Trans. on Antennas and Propagation*, July 1996.
3. Kavita Goverdhanam, Rainee Simons and Linda P.B. Katehi, "Coplanar Stripline Propagation Characteristics and Bandpass Filters," *IEEE Microwave and Guided Wave Letters*, Vol. 7, No. 8, August 1997, pp. 214-216.
4. Kavita Goverdhanam, Rainee Simons and Linda P.B. Katehi, "Coplanar Stripline Components for High-Frequency Applications," to appear in *the IEEE Trans. on Microwave Theory and Techniques*, October 1997.
5. D.R. Drayton, R.M. Henderson and L.P.B. Katehi, "High-Frequency Circuit Components on Micromachined Variable Thickness Substrates," *IEE Electronics Letters*, Vol. 33, No. 4, February 13, 1997.

6. D.R. Drayton, R.M. Henderson and L.P.B. Katehi, "Monolithic Packaging Concepts for High Isolation in Circuits and Antennas," Submitted for publication to *the IEEE Trans. on Microwave Theory and Techniques*, 1997.
7. R.M. Henderson and L.P.B. Katehi, "Silicon-Based Micromachined Packages for Discrete Components," Proceedings of the 1997 International Symposium Microwave Theory and Techniques, June 1997, Denver Co, pp. 521-524 .
8. John Papapolymerou, Jack East and Linda P.B. Katehi, "GaAs vs. Quartz FGC Lines for MMIC Applications," Submitted to the Trans. on Microwave Theory and techniques.
9. Kazem Sabet, Linda Katehi and Kamal Sarabandi, "Wavelet-Based Modeling of Wire Antennas and Scatterers," Proceedings of ACES 1997, Monterey, March 1997.
10. Kavita Goverdhanam, Andreas Cangellaris and Linda P.B. Katehi, "Application of Multiresolution Based FDTD Multigrid," Proceedings of the 1997 International Symposium on Microwave Theory and Techniques, Denver, CO, June 1997.
11. Kavita Goverdhanam, Rainee Simons and Linda P.B. Katehi, "Micro-Coplanar Striplines – New Transmission Media for Microwave Applications," accepted for presentation in the 1998 International Symposium on Microwave Theory and Techniques.
12. Kavita Goverdhanam, Emmanouil Tentzeris and Linda P.B. Katehi, "Treatment of Boundaries in Multiresolution Based FDTD Multigrid," accepted for publication in the 1998 ACES Symposium Digest.
13. Rashaunda M. Henderson and Linda P.B. Katehi, "Silicon-Based On-Wafer and Discrete Packaging," Directions for the Next Generation of MMIC Devices and Systems, Plenum Press, New York, 1997, pp. 113-120.
14. John Papapolymerou, Rhonda F. Drayton and Linda P.B. Katehi, "Surface Wave Mode Reduction for Rectangular Microstrip Antennas on High-Index Materials," Directions for the Next Generation of MMIC Devices and Systems, Plenum Press, New York, 1997, pp. 153-160.

Honors and Awards

- 1997 Best Paper Award by the International Microelectronics and Packaging Society (IMAPS)
- First Prize in Symposium Paper Award Contest with Katherine Herrick for the paper ÒW-Band Micromachined Finite Ground Coplanar (FGC) Line Circuit Elements," IEEE MTT-S, Denver, CO, June 1997

Brief Description of Performed Research

This project concentrates on the development of high-efficiency Si micromachined antennas. Microstrip antennas are used in a broad range of applications from communication systems (radars, telemetry and navigation) to biomedical systems, primarily due to their simplicity, conformability and low manufacturing cost. With the recent development of microwave and millimeter-wave integrated circuits and the trend to incorporate all microwave devices on a single chip for low-cost and high density, there is a need to fabricate microstrip antennas in a monolithic fashion with the rest of the circuitry on semiconducting materials such as Silicon, GaAs or InP. These antennas despite their planar character and low cost suffer from high surface-wave excitation resulting in compromised efficiency, reduced bandwidth and degradation of the radiation pattern. Furthermore, in monolithic designs the feed lines share in most cases the same interface with the antennas and lead into parasitic radiation which deforms the antenna pattern and increases cross-talk. During the reporting period, our group has investigated the development of a variety of micromachined as listed below: (1) The antennas are Si micromachined for high-efficiency and are excited by a corporate feed network which is packaged on-wafer to achieve reduced parasitic radiation and reduced cross polarization levels. (2) Micromachined antennas fed by a vertically integrated network, which excites the radiation elements by electromagnetic coupling through planar slots printed on the ground plane of the antennas. (3) Micromachined antennas, which can be reconfigured by use of a very fast, very low loss, MEMS switch. (4) Modeling of antenna and circuit structures using time domain multiresolution analysis. The study performed in each of these areas is described in detail below.

PART I: Micromachined Antennas

- **Micromachined Antennas with a Packaged Feed**

These antennas have been micromachined on a Si substrate to incorporate an air cavity as shown in Figure 1. This air cavity alters the substrate of the and as a result reduces the excitation of parasitic substrate modes, improve efficiency while at the same time increases the bandwidth. The feeding network is packaged on wafer by its own micromachining packaging in order to eliminate parasitic radiation loss from the feeding line and reduce cross polarization.

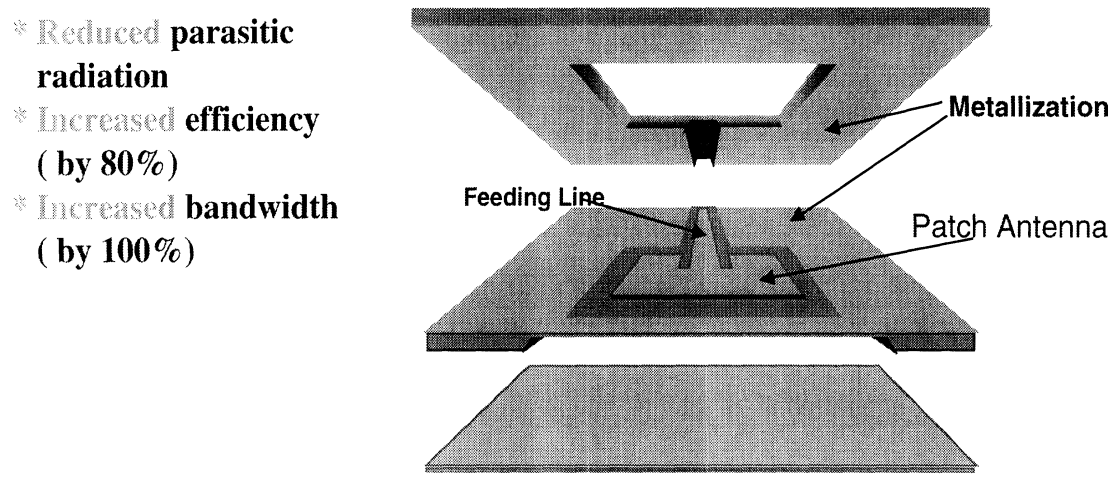


Figure 1: Micromachined Micropackaged Antenna

To develop the micromachined substrate, material is being removed laterally in an area under and around the patch in order to reduce locally the dielectric constant. The removal of the dielectric material underneath the antenna reduces the effective dielectric constant and has a noticeable increase in the bandwidth. Comparison between the bandwidth of a regular patch on Silicon and a micromachined patch has shown an increase of 72% (from 2.9% to 5% for a particular design). Extensive efficiency measurements showed excellent repeatability and demonstrated an increase of

approximately 30% (from 66% to 85%). This work has resulted in a number of presentations (see previous semi-annual report). During the reporting period, the studied summarized here has been presented extensively through a number of Symposium presentations and manuscripts which have either been published, accepted for publication or submitted [1], [4]-[7].

- **Micromachined Antennas Electromagnetically Coupled to the Feeding Network**

Antennas fed by a corporate feed are facing many implementation problems experienced as the operating frequency increases. During the past eight months we have investigated and successfully designed a variety of electromagnetically fed micromachined antennas. The variations we have investigated are involving two separate feeding mechanisms one from a microstrip and coplanar waveguide and two different coupling slot geometries, a single slot and a H slot for better matching and wider bandwidth. Figure 2 shows a schematic of micromachined patch fed by a packaged coplanar waveguide.

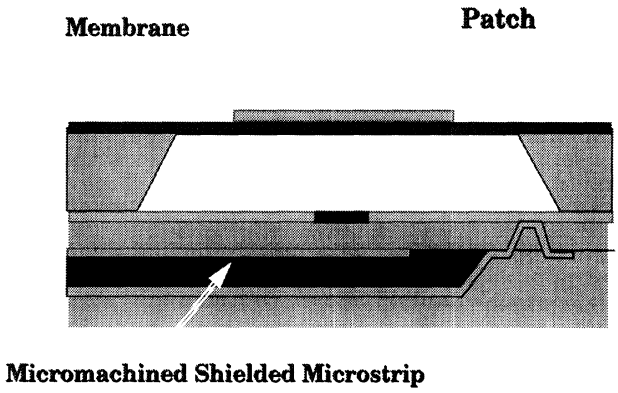


Figure 2: Micromachined Antenna Fed by a Coupling Slot.

Various antennas with operating frequencies at 17GHz, 24GHz and 94GHz have been designed and fabricated and preliminary results have demonstrated very good performance. All of the designs have been supported and validated by extensive modeling. Figure 3 shows theoretical results that predict antenna performance in W band

along with a picture of the real antenna as it has been fabricated and prepared for measurements. At the present time, we are in the process of performing measurements for input impedance, bandwidth and efficiency

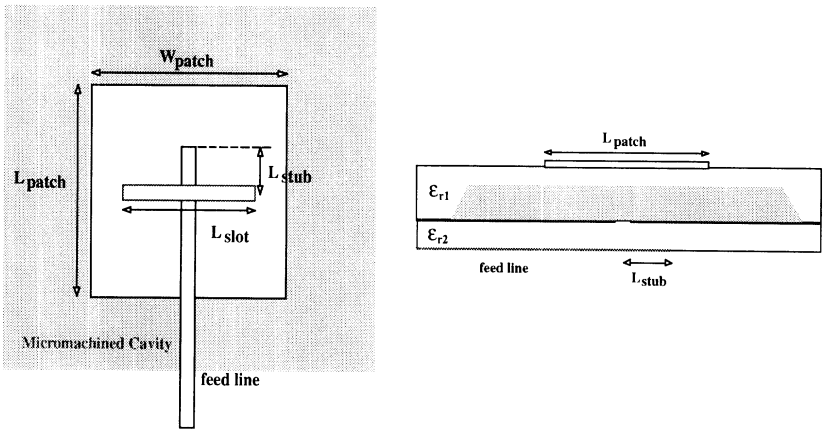


Figure 3: Schematic of a Micromachined Antenna

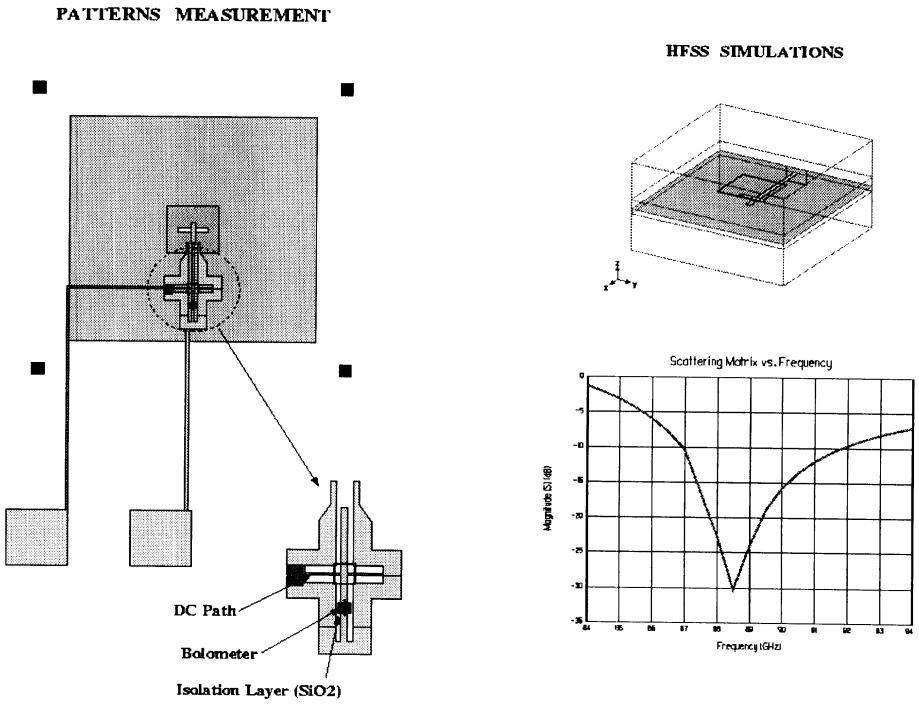


Figure 4: Theoretically Predicted Performance Using HP-HFSS

In addition to the microstrip and coplanar waveguide, coplanar strip lines (CPS) have been investigated for use in the antenna feeding network [2]-[3]. At the present time, we are in the process of designing micromachined antennas fed by a CPS line printed on a substrate made of 20μm polyamide layers on a high-resistivity Si substrate. The use of polyamides allows for the fabrication of CPS lines (see Figure 5) in a way that allows for flexibility in layout provides lines with desirable characteristics.

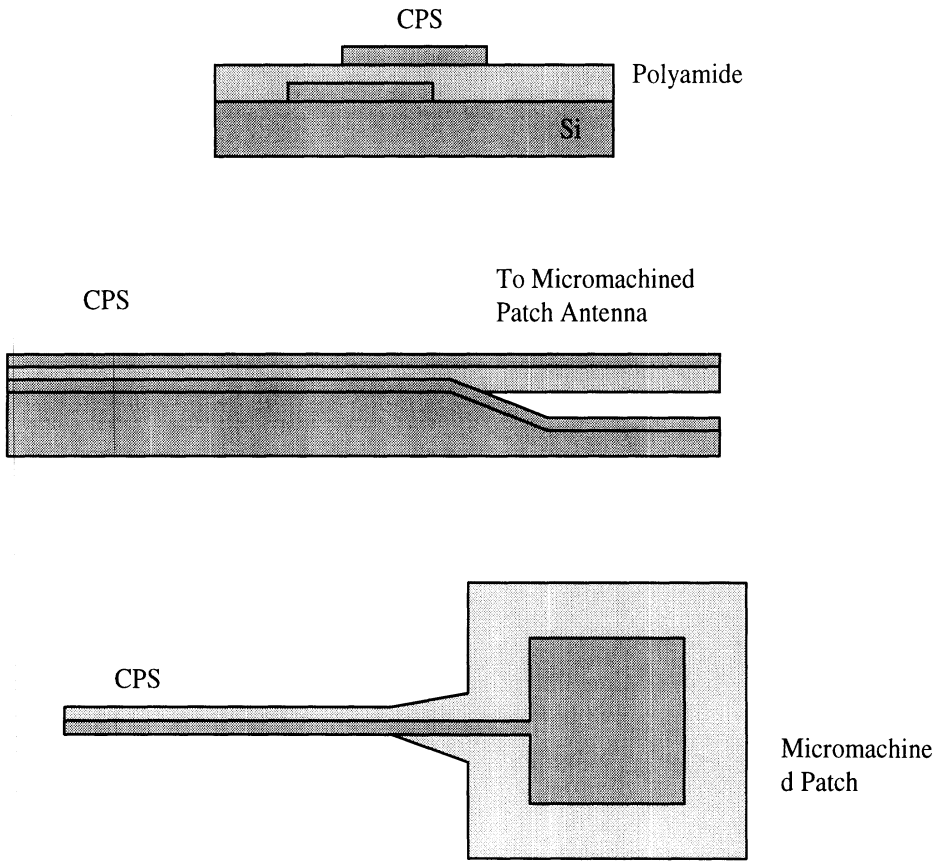
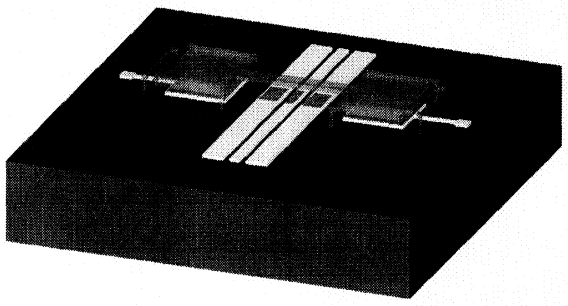


Figure 5: Micromachined Antenna Fed by a CPS Line

- **Micromachined antennas, which can be reconfigured by use of a very fast, very low loss, MEMS switch.**

Reconfiguring antenna characteristics including resonant frequency and polarization, is a desired capability in multifrequency or very broadband systems. In order to reconfigure an antenna, there is a need for very high-speed, small size, low insertion loss switches. PIN diodes have been used in the past in place of these switches, but have introduced many problems such as high loss and nonlinear loading to the antenna and have made the design of the new radiating structure very complicated. With the development of MEMS switches, the possibilities for the development of a high-performance reconfigurable antenna become unlimited. During this reported period, we have investigated the design and fabrication of a MEMS switch that has very high-speed, very low loss and high isolation.

- Switch Parameters
  $V_{pi} = 3$ V
  $K_z = 0.239$ N/m
  $t_s = 8.0$ ns
  $f_0 = 2$ kHz
  $Q = 27.87$



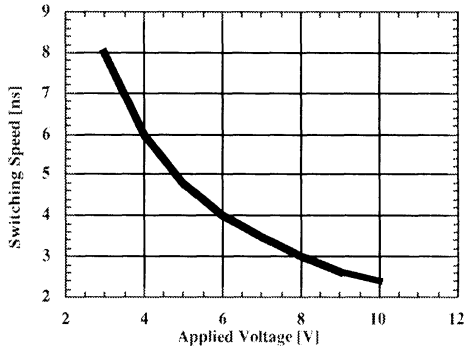


Figure 6: Schematic of the MEMS Switch with Theoretical Predictions

Figure 6 shows a schematic of the switch with the predicted speed as a function of the applied DC voltage. The use of MEMS switches allows for the development of antennas with time adaptive characteristics without compromising performance. The present state of the art has provided MEMS switches for high-frequency applications which can be switched on and off by use of unacceptably high dc voltages. The switch developed as part of this study is based on a unique approach that permits the use of much lower voltages, (less than 6 Volts) without compromising speed. Figure 7 shows a real picture of this switch as it has been fabricated recently. Presently, we are in the process of measuring the performance of these switches. The work from this effort will be extensively reported in the 1998 International Symposium of Microwave Theory and Techniques.

Micromechanical CPW Switch

SEM Pictures

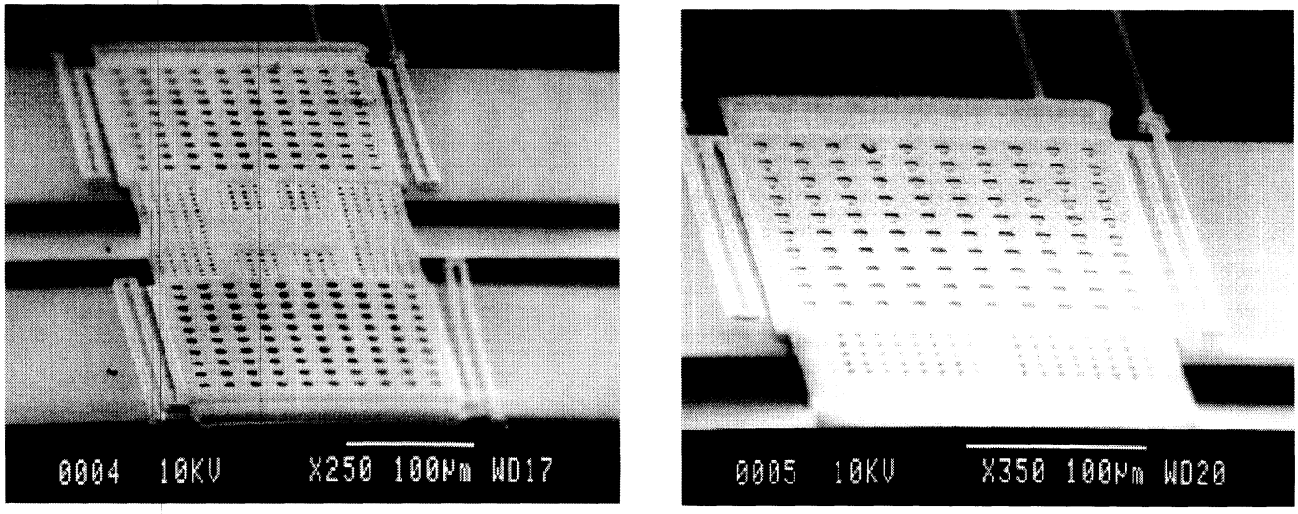


Figure 7: Picture of the Micromechanical Switch.

PART II: Multiresolution Analysis

- **Modeling of Antenna and Circuit Structures using Frequency Domain Multiresolution Analysis.**

Complex antenna and circuit problems require very intensive calculations due to the need to accurately simulate the underlying high-frequency effects and account for all the parasitic mechanisms. As part of this project, we have successfully applied a novel frequency domain scheme recently developed at the University of Michigan that allows for the very successful and computationally efficient solution of complex antenna problems. This technique has been applied to a variety of circuit and antenna problems and has demonstrated the capability to provide accurate solutions in a much more efficient ways than the conventional techniques. The whole idea in this approach is the use of wavelets in the expansion of the unknown functions. The use of wavelets allows for the computation of the values of the derivatives of the unknown field quantities in addition to the average values of the field. This allows for the development of novel space-adaptive schemes with unique capabilities. At the same time, the use of wavelets in the method of moments [8], produces very sparse matrices with excellent condition numbers which allows for the solution of problems which were very difficult to solve with conventional techniques.

Research Summary: 1997

Kavita Goverdhanam

I Development of Multiresolution based FDTD Multigrid:

The objective of this work is to develop a Finite Difference Time Domain (FDTD) multigrid using Haar wavelet based Multiresolution Analysis. This results in the Time Domain Multiresolution (MRTD) technique. It has been shown that an MRTD scheme that uses Haar scaling functions alone, results in the conventional FDTD technique [1]. Further, as per the theory of Multiresolution Analysis, any function which is expanded in terms of scaling functions of a lower resolution level, m1, can be improved to a higher resolution level, m2, by using wavelets of the intermediate levels. The motivation for this work stems from the several advantages offered by using a combination of wavelet and scaling functions as bases, instead of higher resolution scaling functions alone. The use of wavelet expansions has major implications in memory savings because wavelet expansion coefficients are significant only in areas of rapid field variations. This allows for the capability to discard wavelet expansion coefficients where they are not significant thereby leading to significant economy in memory. Different resolutions of wavelets can be combined so as to locally improve the accuracy of the approximation of the unknown function. This, combined with the fact that wavelet coefficients are significant only at abrupt field variations and discontinuities allows MRTD to lend itself very naturally to a Multigrid capability.

To begin with, MRTD technique was successfully applied in solving a variety of simple 2D electromagnetic problems, such as, a cavity and shielded stripline [2]. Having demonstrated the efficacy of MRTD in solving electromagnetic problems, in 1997, significant emphasis was placed on extending the MRTD technique to incorporate more complex geometries which included inhomogeneous dielectrics and 3D structures.

3-D Haar-MRTD Scheme:

The 3D MRTD equations were derived by applying the method of moments to Maxwell's equations by using Haar scaling as well as wavelets as basis functions to expand the electromagnetic fields. By sampling Maxwell's differential equations with scaling and wavelet functions, a set of simultaneous discretized equations were obtained [3]. For the first resolution level of Haar wavelets, the scaling and wavelet schemes decouple and coupling can be achieved only through the excitation term and boundaries.

While the 2D MRTD scheme dealt with geometries shielded by Perfect Metallic Conductors (PECs), the 3D MRTD scheme that has been developed, incorporates Perfect Magnetic conductors (PMCs) as well as absorbers. The Perfectly Matched Layer (PML) is used as an absorber. Thus the 3D MRTD scheme has the capability to analyze open structures as well, thereby broadening the range of applicability of the scheme. To validate the generalized 3D MRTD technique, the electromagnetic fields in geometries such as parallel plate and rectangular waveguide have been successfully evaluated, thus verifying the accuracy and the efficiency of the technique.

The aforementioned 3D MRTD scheme also incorporates inhomogeneous dielectrics. As mentioned earlier, for the first level of wavelet resolution, the scaling and wavelet schemes are decoupled, except at the location of the source and boundaries. Thus, at the region of interface between two dielectrics, where the scaling and wavelet functions are coupled, appropriate boundary conditions were applied to accurately model the dielectric interface. The fields in an inhomogeneous dielectric filled parallel plate waveguide have been accurately solved using the MRTD technique. Thus a generalized 3D MRTD scheme which incorporates the source term, PECs, PMCs, dielectric boundaries and PML absorbers has been developed, its performance has been verified and its numerous advantages have been demonstratedi. This establishes MRTD technique as the most efficient and simple tool that can be used to achieve FDTD Multigrid.

II Micro-Coplanar Striplines:

In this research effort, a new transmission line for microwave applications, referred to here as the Micro-Coplanar Stripline (MCPS), was studied [4]. Motivation for this work stems from the requirement of low-cost devices in wireless communication systems. One approach in addressing

the low-cost requirement is to combine the available digital silicon processing technology with the high frequency silicon germanium device technology. The size and complexity issues that arise with this integration lead to the requirement of novel integration techniques which rely on multi-layer three dimensional transmission lines constructed using very dielectric layers such as glass or silicon dioxide. The aforementioned MCPS line is aimed at meeting this requirement. It is fabricated on a high resistivity silicon (HR Si) wafer and has a very thin spin-on-glass (SOG) as a spacer layer separating two strip conductors. A number of MCPS geometries were characterized using the FDTD technique in order to obtain the characteristic impedance and effective dielectric constant. From these studies, it was proved that by varying the parameters involved, a wide range of desired characteristic impedances could be obtained. Preliminary studies have thus indicated that MCPS provides extremely compact and low cost circuits with wide design flexibility. Further investigation of the MCPS is in progress.

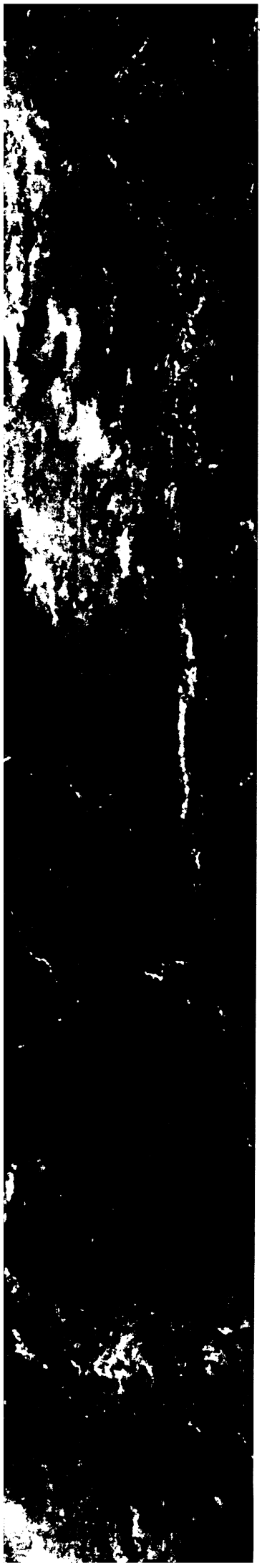
References

[1] K. Goverdhanam, E. Tentzeris, M. Krumpholz and L.P.B. Katehi, "An FDTD Multigrid based on Multiresolution Analysis", Proc. AP-S 1996, pp. 352-355.

[2] K. Goverdhanam, A. Cangellaris and L.P.B. Katehi, "An FDTD Multigrid Based on Multiresolution Analysis", Proceedings of the 1996 IEEE International Symposium on Antennas and Propagation, Baltimore, MA, pp. 352-355, July 1996.

[3] K. Goverdhanam, E. Tentzeris and L.P.B. Katehi, "Treatment of Boundaries in Multiresolution based FDTD Multigrid", Accepted for publication in the 1998 ACES Symposium digest.

[4] K. Goverdhanam, R.N.Simons and L.P.B. Katehi, "Micro-Coplanar Striplines - New Transmission Media for Microwave Applications", Accepted for publication in the 1998 MTT-S International Microwave Symposium Digest.



THE INDUSTRIAL ELECTRONICS HANDBOOK

Editor-in-Chief
J. DAVID IRWIN

CRC PRESS
IEEE PRESS

A CRC Handbook Published in Cooperation with IEEE Press

Library of Congress Cataloging-in-Publication Data

The industrial electronics handbook/edited by J. David Irwin.
p. cm.--(The electrical engineering handbook series)
Includes bibliographical references and index.
ISBN 0-8493-8343-9 (alk. paper)
1. Industrial electronics—Handbooks, manuals, etc. I. Irwin, J. David, 1939– . 11. Series.
TK7881.I52 1996
621.3-dc20

96-3070
CIP

International Standard Book Number 0-8493-8343-9
Library of Congress Card Number 96-3070
Printed in the United States of America 1 2 3 4 5 6 7 8 9 0
Printed on acid-free paper

120

Si Micromachining in High-Frequency Applications

Linda P. B. Katehi
University of Michigan

Gabriel M. Rebeiz
University of Michigan

Tom M. Weller
University of South Florida

Rhonda F. Drayton
University of Illinois-Chicago

Stephen V. Robertson
University of Michigan

Chen-Yu Chi
QualComm, Inc.

120.1 Introduction

Microwave and millimeter-wave planar-integrated circuits and antennas are the central nervous system in communication radars. In the past decade, the microwave field has been experiencing a technological revolution due to advances in solid-state devices, insulating and semiconducting materials, and circuit analysis techniques. Furthermore, the planarization of guiding structures to transmission lines in microstrip, stripline, or coplanar waveguide form provides great flexibility in design, reduced weight and volume, and compatibility with active devices and radiating elements.

There are, however, drawbacks to these planar geometries. These include frequency dependent mechanisms such as parasitic coupling and radiation, as well as increased ohmic loss, dielectric loss, and dispersion. These effects can seriously deteriorate electrical performance and can lead to costly, time-intensive design cycles (van Deventer et al., 1989; Dunleavy and Katehi, 1988). Suppression of some of these electromagnetic mechanisms, such as parasitic radiation and coupling, has led to improved performance, but requires very sophisticated solutions which add considerably to the weight and cost of the circuits (VandenBerg and Katehi, 1992; Harokopus and Katehi, 1989; Pengelly and Schumacher, 1988). Elimination of other deleterious effects, such as dispersion and ohmic loss, will require fundamentally new approaches to planarization and circuit integration.

In almost all design cycles, system components are typically developed and tested in an open environment. Once performance is tested and design is confirmed, the circuits are mounted into a metal housing which, in most cases introduces multiple parasitic resonances that interfere with the electrical performance of the circuit. In addition, this packaging approach often results in expensive packages that are mostly responsible for the resulting weight and volume of the units. Miniaturized high-frequency circuits with an integrated housing offer lightweight and controllable parasitics, making them appropriate for cellular and mobile communications where system requirements impose strict limits on electrical performance.

Recent advances in semiconductor processing techniques offer a historic opportunity to distinguish the monolithic from the planar character, and provide integration in all of the directions of the three-dimensional space (Weller et al., 1993a,b; Dib et al., 1991). The capability to incorporate one more dimension, and a few more parameters, in the circuit design, can lead to revolutionary shapes and integration schemes. These circuit topologies can reduce ohmic loss and eliminate parasitic radiation or parasitic cavity resonances without affecting the monolithic character of the design circuits. Operating frequencies are thereby extended and performance is optimized.

0-8493-8343-9/97/$0.00+$.50

Silicon miromachining can provide a variety of solutions to the previously mentioned problems resulting in transmission line and array approaches which are characterized by:

- Superior performance.
- Low-weight and volume.
- Easy fabrication.
- Great potential for low cost.

The characteristics shown above may be prioritized according to pre-existing needs, resulting in a number of approaches which use micromachining for millimeter- and sub-millimeter-wave circuit design.

120.2 Applications

The evolution of micromachined circuits and antennas for operation in microwave and millimeter-wave frequencies is still in its infancy. However, presented here is a description of recent accomplishments in this area, with emphasis on the effort performed at the University of Michigan. There are two techniques which have shown promise for use, and which extensively use micromachining to realize novel circuits. The first utilizes dielectric membranes to support transmission line and antenna configurations (Weller et al., 1993a,b; Dib et al., 1991) and emphasizes optimization of circuit performance. The second technique introduces new concepts in packaging such as adaptive or conformal packaging and, in addition to improvement in performance, it emphasizes size/volume/cost reduction (Drayton and Katehi 1982, 1993a,b). The merits of each approach, in relation to electrical performance, fabrication, and compatibility, will be presented, and the impact of the newborn technologies to the state of the art will be discussed.

Dielectric Membrane Supported Circuits and Antennas

Membrane supported radiating elements, such as the integrated-horn antenna, were first developed in 1987 by D.B. Rutledge and G.M. Rebeiz (Rebeiz et al., 1990) and have been further studied and developed at Michigan by G.M. Rebeiz and L.P.B. Katehi. SIS junctions on thin SiN membranes and have been successfully fabricated at MIT by E. Garcia et al. (1993). Furthermore, linearly tapered slot antennas and corner-reflector antennas printed on membranes have been developed by E. Kolberg et al. (Ekstrom et al., 1992) and have shown excellent performance. The fabrication of these radiating structures has led to the establishment of a membrane technology which is reliable, repeatable, and easy to employ. The successful use of membranes for antenna design led to the development of a membrane-supported transmission line, called microshield, which was presented for the first time in the 1991 MTT-S International Microwave Symposium (Dib et al., 1991). The microshield is only one of the possible membrane-supported geometries shown in Figure 120.1. All of these geometries are evolutions of conventional planar lines with one major difference; the substrate material underneath the lines has been removed and a membrane is utilized to support the conductors. Figure 120.1c shows a *membrane coaxial,* which resembles a rectangular coaxial, and is characterized by zero dielectric loss, zero dispersion, zero parasitic radiation while maintaining compatibility to planar monolithic geometries. This propagating structure is completely shielded and can provide passive circuit components with optimum performance. Figure 120.1a shows a *membrane coupled strip* line which very closely resembles the conventional coupled strip line and can provide very efficient antenna feeding networks. The third of the membrane geometries, Figure 120.1b, is the *microshield line* which resembles very closely the conventional coplanar waveguide. This line has zero dispersion, limited parasitic radiation and the capability to suppress the excitation of the unwanted slot mode due to the presence of the folded ground which operates as a continuous air bridge. The membrane line as a transmission medium has created the basis of a new technology, which can provide generic designs appropriate for circuit and antenna applications in the millimeter and submillimeter-wave region.

As shown in Figure 120.1, various configurations of membrane lines may require the use of two or three wafers, to provide a cavity shield on one or both sides. This cavity shield is necessary for some uniplanar geometries, where multiple ground planes or other conductors are in close proximity to the signal line. Figure 120.1a shows a membrane coplanar strip line, made of two high-resistivity <100> Si wafers, in which the electric field is confined to the surface area between the two strips. In this case shielding by the cavity is not required and, depending on the application, the line may operate in a variety of environments. All the membrane line configurations presented so far utilize at least two wafers, and the cavity structures under the signal lines may also be designed to control line characteristics. These membrane monolithic geometries are appropriate for a variety of applications including monolithic antenna and array feeding networks, diode mounting structures for receiver applications, networks for vertical integration, etc.

Membrane supported transmission lines are quasi-planar configurations in which a pure, non-dispersive TEM wave propagates through a two-conductor system embedded in a homogeneous environment. Homogeneity of the environment can be accomplished by using a 1.5-micron-thick dielectric membrane, or a few-micron-thick diaphragm, to support the signal lines, while ground is provided by a metallized micromachined cavity. This cavity is fabricated in Si wafers, using etchants such as KOH (potassium hydroxide) or EDP (ethylene diamine pyrocatechol), and is metallized using evaporation or plating. The signal lines are created by metal deposition on the membranes or diaphragms or can be grafted onto the supporting structure by lift-off techniques. Due to cavity shielding and the pure TEM character of the propagating mode, these lines possess a large single-mode frequency band (DC to > 1 THz), have very low losses and zero signal dispersion. Consequently, circuit components made of these line geometries can provide electrical performance which is superior to those of conventional planar circuits.

The success of membrane-supported circuits relies on the development of thin-film dielectric membranes or diaphragms

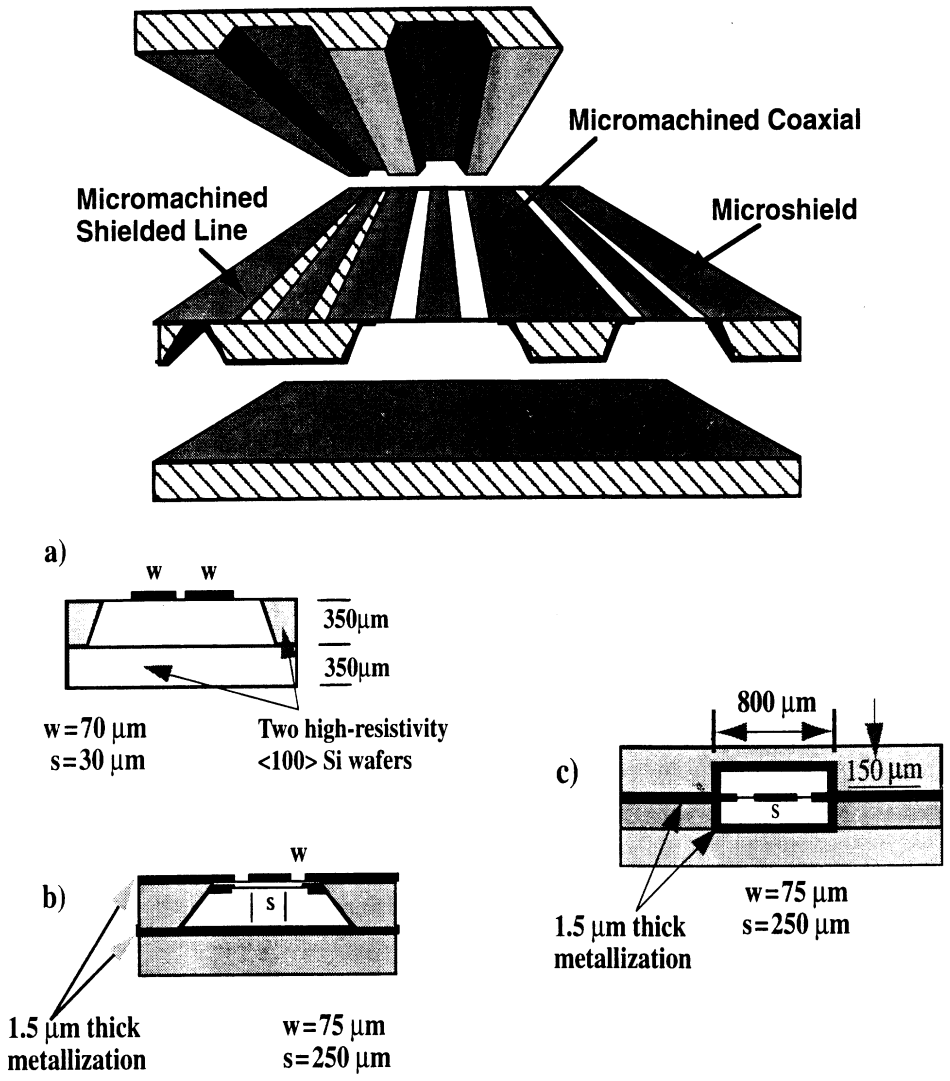


Figure 120.1 Micromachined transmission line geometries.

with good electrical and mechanical properties. These thin-film layers are grown on Si or GaAs wafers, and are used to support the planar conduct ng strip lines. In view of the previously mentioned performance objectives, the thin films must have low losses at microwave and millimeter-wave frequencies, as well as compatibility with semiconducting and conducting materials. Furthermore, mechanical considerations include reduced sensitivity to applied pressure and temperature variations, along with increased membrane or diaphragm sizes.

For the circuits presented in this chapter, the membranes are in a tri-layer $SiO_2/Si_3N_4/SiO_2$ configuration, with constituent thicknesses of 7000, 3000, and 4000 Å, respectively. The base layer (7000 Å) is grown using thermal oxidation, while the final two layers are formed using a low pressure chemical-vapor-deposition process (LPCVD). The materials used for the development of the dielectric membrane have very low losses from DC ($\rho > 10^{14}$ Ω-cm) well into the THz region. The small size makes the membranes transparent to propagating signals at frequencies as high as 1–3 THz, and provides a near-homogeneous air-filled environment to the propagating electromagnetic wave. Consequently, the wave exhibits very fast wave velocities, zero dispersion, and zero dielectric loss. To date, membrane dimensions as large as 9 mm × 9 mm have been fabricated for use in membrane lines with a yield greater than 95%.

Micromachined Lines for Miniature, Monolithic Packaging

In microwave and millimeter-wave circuit applications, the issue of RF packaging is becoming an important subject to address due to the lack of appropriate packaging configurations for high-frequency circuit design. Several years back, experts in the field of device and component development began to realize that packaging of such components was progressing at a much slower rate than the devices themselves. As a result, many problems observed in device and component performance at these frequencies are being attributed, after diagnostic testing, to the package in which they are housed. Typical problems associated with circuit packages, especially above X-band, include resonances due to the large physical geometry surrounding these circuits, cross-talk caused by parasitic radiation from neighboring circuits, and unwanted excitations that result in power leakage in the form of substrate modes. Many of these issues can be addressed by integrating the package with the circuit monolithically, which

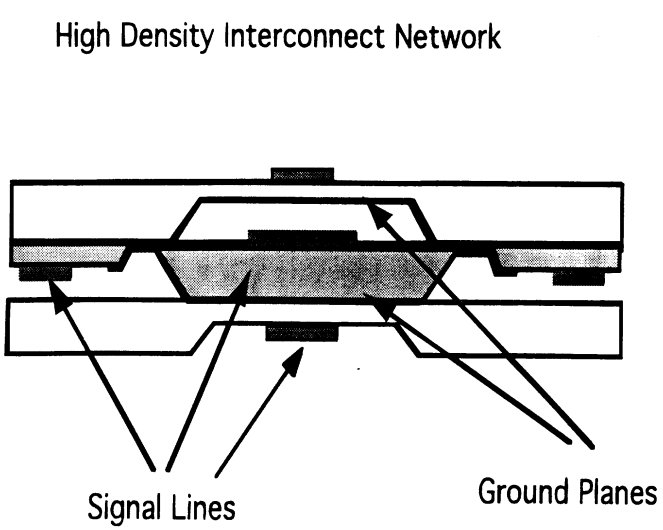


Figure 120.2 High-density micromachined interconnect network.

implies that the package is part of the circuitry and it is designed to meet performance specifications. Other desired attributes of an RF package include the capability to provide protection from hostile environments, appropriate means for heat removal, and mechanical support for components while introducing minimum performance degradation. With state of the art advances in semiconductor processing techniques, silicon micromachining can offer what conventional means have not been able to provide; packages which conform to the circuit geometry, require much less space, and provide superior mechanical, thermal, and electrical performance.

Although micromachining of silicon is a well established technology for sensor and biomedical applications, for the first time this technology is being applied to develop self-packaged circuit components for high-frequency applications. In the past few years, the use of Si micromachining in microwave and millimeter-wave circuit applications has been extensively explored at the University of Michigan, leading to many innovations. Among these have been the capability to develop self-packaged circuit components which have demonstrated superior electrical performance when compared to conventionally developed components. These micromachined circuit components may be of microstrip or coplanar waveguide (CPW) type and they are surrounded by an air-filled cavity in the upper region and a substrate-filled cavity in the lower region. Both cavities are integrated monolithically with the circuits to provide completely shielded geometries which are appropriate for a broad range of applications including high density interconnect networks such as the one shown in Figure 120.2. The use of micromachining has led to the development of a variety of planar circuits with optimum performance (Weller et al., 1993a,b; Drayton and Katehi, 1993, 1992a,b) and has demonstrated the capability to develop novel geometries and integration techniques.

This effort has led to the first demonstration of a high-frequency monolithic conformal package that follows the path of various line geometries, and is sized in such a way that its package resonance exists well above the desired range of operating frequencies. One very important characteristic of this packaging approach is that it provides monolithic self-packaged geometries which can be integrated within more complex planar circuit arrangements. Furthermore, this package can be integrated with any uniplanar technology and can incorporate any type of transmission medium such as microstrip, coplanar waveguide, coaxial line or stripline.

The concept of conformal packaging can be applied to a very broad range of applications. One such application is the development of planar diode mounting structures for detector and mixer applications. To demonstrate the flexibility offered by micromachining, the mounting structure for a K-band detector as shown in Figure 120.3 has been developed with both longitudinal shielding as well as cross cavity shielding. The cross-cavity junction implemented in the shielding allows for the incorporation of commercial diodes or other input paths to the existing circuit. The passive circuit in the mount consists of an input matching network, a diode mounting region, and a lowpass filter output. At the diode placement location, a cross-cavity is formed in both the upper and lower cavity regions and is designed to operate under cut-off as discussed earlier. For the embodiment presented here, the lower cavity dimensions form a substrate-filled waveguide which has the dominant effect on the package resonance.

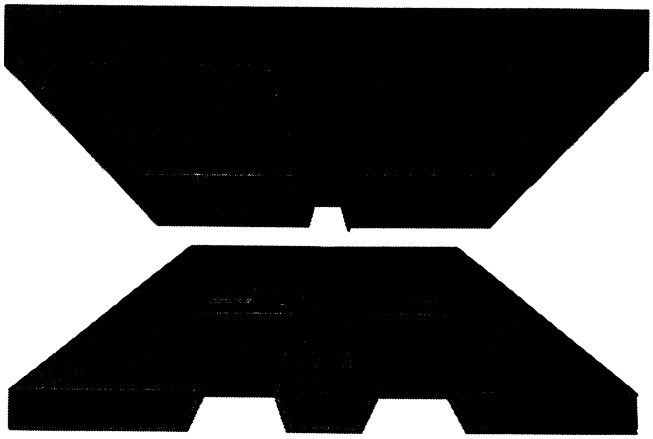


Figure 120.3 Conformal packaging.

The dimensions of the shield are chosen so that the package resonates at 54 GHz.

120.3 Fabrication Methodology

A detailed description of the processing steps involved in the fabrication of silicon micromachined circuits is presented in this section. The procedures are grouped into five primary categories, which are the growth of the tri-layer dielectric membrane, deposition of the circuit metallization, wet chemical etching (micromachining) of the silicon, backside metallization, and final circuit assembly. The membrane is mainly of importance in the realization of membrane-supported configurations, but is also useful as a temporary masking layer in general micromachining applications. Typically, a single oxide layer is more convenient when only the masking function is required. The silicon wafers must be at least single-side polished on the surface which will be patterned with circuit metallization, and double-side polished wafers are desirable when fine features are to be micromachined on the back side. If the etch patterns consist of relatively large openings and do not require great resolution, the additional expense of double-side polishing can be safely avoided. It is imperative, however, that silicon with a resistivity of at least 1500–2000 Ω-cm be used wherever silicon is exposed to the RF energy. This is done to avoid excessive dielectric loss, and necessitates the use of wafers which are grown using the float zone (FZ) process (Kramer, 1983). For completely metallized ground planes or RF shielding cavities, less expensive, low-resistivity (approximately 10 Ω-cm) wafers are utilized. These are typically grown using the Czochralski (CZ) method (Leadise, 1970).

There are undoubtedly countless numbers of possible variations and extensions of the techniques included here. The intent of this writing is merely to describe a reasonably broad set of procedures which have been found to be reliable for fabrication of the micromachined circuits. For more extensive reviews of silicon processing and micromachining, the reader is referred to Wolf and Tauber, (1986).

Dielectric Membrane Growth

The cornerstone of silicon micromachined, membrane-based transmission line architectures is the three-layer dielectric material on which the conducting lines are supported (see Figure 120.4.) This membrane comprises a thermally grown oxide which is subsequently layered with a silicon nitride and another oxide, both of which are deposited using low pressure chemical vapor deposition (LPCVD). By properly balancing the thickness of each layer, a composite in slight tension is obtained which remains rigid when the silicon substrate is removed, and is robust enough to withstand subsequent processing such as photoresist application and metallization. Furthermore, membranes with dimensions up to 8 × 8 mm^2 have been fabricated successfully with yields exceeding 95% (Weller et al., 1994a).

The critical issue in achieving flat, large area membranes is determining the correct thicknesses of the constituent layers. It is known that the thermal coefficients of expansion for amorphous SiO_2 and Si_3N_4 are greater and less than that of silicon; The value for silicon is 2.6 × 10^{-6}/°C, and the values for high-temperature CVD oxide and nitride are 5 × 10^{-7}/°C and 4–7 × 10^{-6}/°C, respectively (Maissel and Glang, 1970). Therefore, by adjusting the thickness of each layer, a net tensile stress can be left in the membrane when the wafer is cooled to room temperature from the 800–900°C temperatures in the LPCVD furnaces. High-yield membranes are obtained on 10cm diameter, 500–550 micron-thick wafers using values of 7500Å/500Å/4500Å for the thermal oxide, intermediate nitride, and top oxide layer thicknesses, respectively. A direct, experimental technique for determining the appropriate layer thicknesses is outlined in Ling (1993). The specific layer thicknesses given here have been slightly modified with respect to those given in Ling (1993).

Detailed procedures for membrane fabrication are outlined in the following:

- Pre-Furnace Wafer Clean: Prior to the thermal oxide growth, the wafers must be stripped and cleaned of all foreign materials to ensure a high-quality film and to prevent contamination of the furnace. The necessary steps are outlined in Table 120.1.
- Thermal SiO_2 Deposition: The thermal oxide is grown using a dry-wet-dry sequence at a temperature of 1100°C and a pressure of 1 ATM, with the temperature held at 800°C while transferring the wafers in and out of the furnace. The first and last dry oxide layers are dense films which are grown to thicknesses of 5–10 Å using an oxygen flow rate of 3 L/min. The intermediate wet layer is grown using flow rates of 1.7 L/min for O_2 and 2.5 L/min for H_2, yielding a faster growth rate but more porous film in comparison to the dry layers. The time required to grow a 7000 Å-thick oxide is approximately 3–4 hours.
- LPCVD Si_3N_4 and SiO_2 Deposition: Following the thermal oxide growth, the wafers are moved to an LPCVD furnace for deposition of the intermediate nitride and the final oxide. The furnace temperature is approximately 900°C, and the growth rates are around 50 Å/min and 70 Å/min for the nitride and oxide, respectively. Specific parameters for this process are given in Table 120.2.

Metallization Pattern Definition

This section outlines the procedure for depositing the thin-film metallization which constitutes the circuit pattern onto the front side of the wafer (see Figure 120.5). The steps described here are primarily based on the image reversal photoresist technique. In this process, dark features on the circuit mask correspond to areas which will be metallized, and this generally simplifies the alignment procedure since most of the mask is transparent (a clear-field mask). Also, in comparison to alternative methods such as the chlorobenzene process, the image reversal method has been found to yield more ideal metal profiles. Results with the chlorobenzene process demonstrated a phenomena known

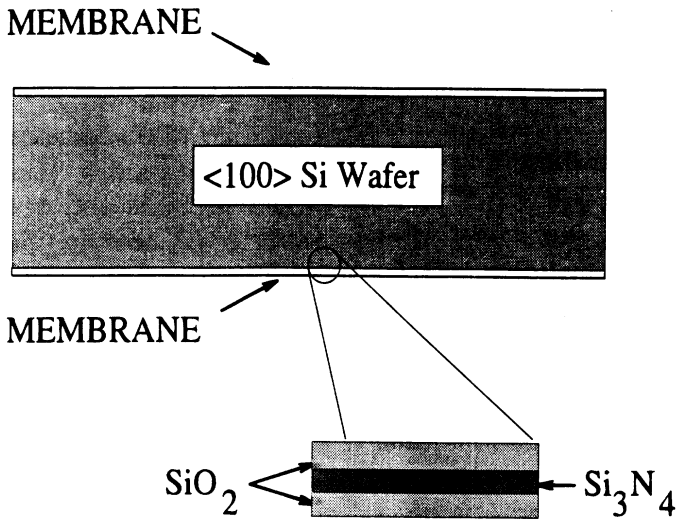


Figure 120.4 The tri-layer dielectric membrane grown on both sides of a silicon wafer.

Table 120.1 Prefurnace Clean Procedure

Solution	Ratio	T°C	Time (Min)
H_2O_2:NH_3OH:H_2O	1:1:15	90	10–20
H_2O quench		24	2
HF:H_2O	1:10 (Note 1)	24	1
H_2O quench		24	2
H_2O_2:HCL:H_2O	4:4:25	90	10–20
H_2O		24	5
H_2O rinse w/N_2 bubbling		24	Note 2
Spin in the rinser/dryer		24	5

Note 1: When cleaning wafers with critical oxide layers, a 1:100 solution can be used instead.
Note 2: The last rinse is continued until the bath resistivity exceeds 13–14 MΩ-cm.

Table 120.2 LPCVD Deposition Parameters. DCS Stands for Dichlorosilane

Dielectric Layer	T°C	Ingredients	Flow Rates (sccm)
Si_3N_4	800	NH_3	160
		DCS	40
SiO_2	900	N2 dilute	290
		N_2O	120
		DCS	60

as "lift-off flags," referring to metal profiles which have sharp, up-turned spikes at the edges of the pattern.

Before starting the procedure, appropriately sized silicon pieces must be prepared. This involves dicing, or simply scribing, a whole wafer into smaller pieces, making sure that the edges follow straight lines along the <110> crystal directions (either parallel or perpendicular to the major flat). If this is not done it will be impossible to correctly align the etch patterns with the crystal structure. This type of misalignment results in poor cavity definition and undercutting of the etch masking layers.

The circuit metallization sequence is as follows:

- Wafer Preparation: For best results, the wafer should be thoroughly cleaned using a 1:1 "piranha" etch (a 1:1 ratio of H_2SO_4:H_2O_2). The duration of the clean should be about 10 minutes, which is the approximate lifetime of the reaction.
- Image Reversal:
  a. Clean the wafer with acetone and IPA. Dehydrate-bake for 3 minutes on a hot-plate at 130°C. Keep desired membrane surface face up.
  b. Spin-apply HMDS (hexamethyldisilazane) adhesion promoter and AZ 5214-E photoresist at 2.5 KRPM. This yields a photoresist thickness of approximately 2.1 μm.

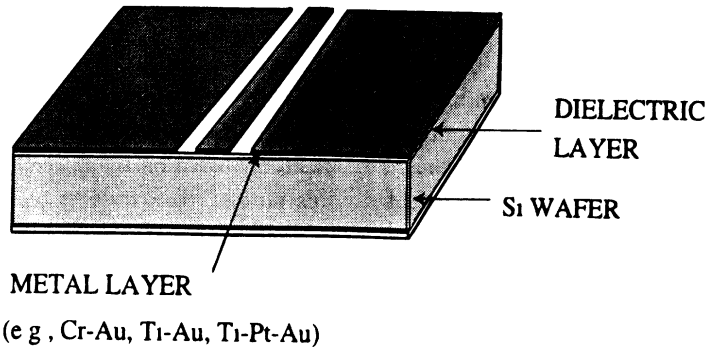


Figure 120.5 Circuit pattern deposited onto the front side of a wafer using thin-film application techniques.

c. Soft-bake 1 minute at 105°C on a hot-plate.
d. Align and expose for 8 seconds at 20 mW/cm^2 ultraviolet light intensity (λ = 405 nm). To achieve success in the subsequent micromachining steps, the mask must be aligned to a straight edge of the wafer, such that the patterns to be etched into the front or back side can be correctly positioned along the <110> crystal directions. This step is made easier if the mask incorporates long, straight alignment marks around the edge of the circuit area. These can be used to align the wafer via Θ-positioning, and if necessary, the pattern can then be translated back to the center of the wafer using x and y positioning only.
e. Post-bake 1 minute at 130°C on a hot-plate. This step causes the exposed photoresist to "cross-link," and leads to the formation of a thin crust on the upper surface.
f. Flood-expose for 120 seconds at 20 mW/cm^2 UV power density. This long exposure activates the photoresist which was not exposed previously.
g. Develop in AZ327MIF developer for 45–55 seconds. This removes the photoresist which was not exposed during the first alignment, and will also remove some of the photoresist beneath the edges of the cross-linked pattern. It is this undercutting that allows the subsequent lift-off process to succeed.
h. Check pattern definition of the evaporated metal using a microscope.

- Metal Deposition:

a. Descum the wafer using a 36 second, 80 W O_2 plasma etch.
b. Deposit metallization using evaporation techniques. Metal systems such as chrome-gold, titanium-gold, or titanium-platinum-gold are resistant to wet etching using the EDP solution. Alternatively, if thicker layers are necessary to minimize attenuation, copper or silver may be used instead of gold to reduce fabrication costs. Most anisotropic silicon etchants attack aluminum at a substantial rate, and therefore Al should not be used in applications requiring long etch times.
c. Soak in acetone for approximately 6 hours to dissolve the photoresist masking layer and complete the pattern lift-off.

The process described has been verified for line dimensions down to 10 μm, and evaporated metallization thicknesses up to 1.2 μm.

Due to the slow spin-rate for the photoresist deposition, beading will occur around the edges of the silicon piece, leaving up to 5 mm around the circumference which is non-usable. For 1–2 μm features, the beading should be removed using a technique such as that described in Gearhart (1994). Also, for metallization thicknesses up to 0.6 μm, the AZ 5214-E can be spun on at 4.5 KRPM. This provides about 1.4 μm photoresist thickness and is better for feature sizes down to 3–5 μm. Using this method, the first expose and flood expose times should be reduced to 4 seconds and 90 seconds, respectively.

It is important to point out that free-standing membranes of the type described in Dielectric Membrane Growth can withstand the circuit metallization procedure. Therefore, the silicon micromachining can precede the metal deposition if necessary. In this case, photoresist application requires that the wafer should first be attached to a support wafer, separated by small silicon standoffs (see Figure 120.6). The support/standoff/membrane wafer system can be temporarily assembled using a heavy photoresist "glue" such as 1400–37, and baked on a hot plate at 130°C for 1 minute. This assembly will easily survive the photoresist spin and alignment steps, and can be separated during the photoresist development stage to simplify drying. Alternatively, the circuit wafer can be separated during the second hot plate bake by handling it instead of the support wafer. Some type of standoff arrangement is also necessary during the metal evaporation, to prevent membrane failure, since evacuation of the chamber creates a high pressure differential across the membrane.

For applications requiring thicker metallization layers, the evaporation technique can be supplemented with gold electroplating. One method of implementing the plating process begins with the evaporation of Ti-Au-Ti or Cr-Au-Ti seed layers over the entire front (or back) wafer surface, using thicknesses of 500Å/1000Å/500Å, respectively. The photoresist is then applied and patterned using the image reversal technique. Alternatively, a 1400–37 positive photoresist process can be used to provide a thicker photoresist layer. This process requires a dark field mask, and is outlined in steps 1a–1h in the section on Silicon Micromachining. The next step is to remove the exposed Ti in the pattern openings using a 10:1 H_2O:HF etch for 3–10 seconds. The metallization can then be built up using electro-plating, and the Ti layer which remains outside the pattern will help to prevent lateral spreading of the plated Au. Finally, the photoresist is removed with an acetone soak or hot PRS-1000 photoresist stripper. Unwanted seed layer metals are removed using gold and chrome etchants, and 10:1 H_2O:HF for Ti.

Silicon Micromachining

The technologies related to silicon micromachining began to emerge in the 1960s (Lepselter, 1966), and continued to evolve into what is currently a wide array of techniques aimed at manipulating silicon for mechanical purposes. The development of complex micro-electro-mechanical systems (MEMS), sensors,

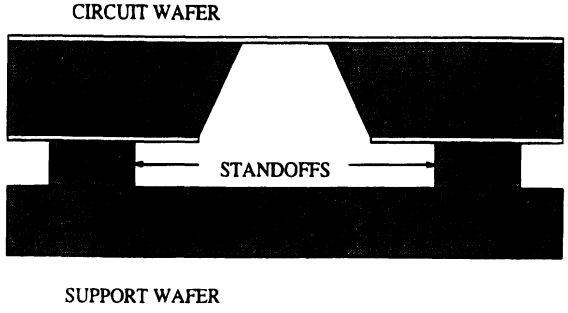


Figure 120.6 Circuit-wafer/standoff/support-wafer assembly used for the photoresist process on free-standing membrane pieces.

and actuators has driven many of the significant advancements in this area, and a large volume of related work has been published in journals on solid state electronics and processing. The microwave community, in which the use of micromachining is relatively new, now has the advantage of drawing upon these established resources to solve problems and develop new concepts for microwave circuits.

The procedure which will be presented here is a very basic approach to bulk silicon micromachining using an anisotropic etchant. It relies on the use of a wet etchant such as KOH (potassium hydroxide) or EDP (Finne and Klein, 1967) (ethylenediamine pyrocatechol) to remove silicon preferentially along certain crystal directions, thereby allowing the formation of well-defined cavity regions. In the work considered here, wafers with a <100> orientation are typically used, and the etch rates are about 50:50:1 for the <100>, <110>, and <111> directions, respectively, using EDP at 100°C (see Figure 120.7). Similar ratios are achievable using KOH, however this is generally not the etchant of choice for dielectric membrane-related work since it etches silicon dioxide much faster than does EDP. The SiO_2 etch rate in EDP is approximately 5 Å/minute, and in KOH the rate can be increased by an order of magnitude. Other masking films for EDP include Si_3N_4,Au, Cr, Ti, Ag, Cu, and Ta (Peterson, 1982).

To describe the complete micromachining procedure, a typical process flow for single-side etching from the back of a wafer is outlined in the following. It is assumed that single-layer oxides or oxide/nitride/oxide layers are in place and will serve as the masking films for the etchant.

- Wafer Preparation:
  a. Clean wafer with acetone and IPA. Dehydrate bake for 3 minutes on a hot-plate at 130°C. Keep desired membrane surface face up.
  b. Spin HMDS adhesion promoter and 1400–37 photoresist at 3.5 KRPM onto the front (desired) membrane surface. This provides a photoresist thickness of approximately 3.5 μm.
  c. Hard-bake 30 minutes at 110C° in an oven. Alternatively, a 1 minute bake at 130°C on a hot plate can be used. This photoresist serves to protect the front side of the wafer during the proceeding masking layer removal steps.
  d. Spin HMDS adhesion promoter and 1400–37 photoresist at 3.5 KRPM onto the back side of the wafer.

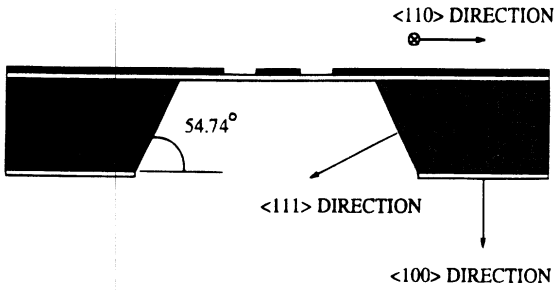


Figure 120.7 Etch profile for a ⟨100⟩ oriented silicon wafer using an anisotropic etchant.

  e. Soft-bake 30 minutes at 90°C in an oven.
  f. Align and expose the patterns to be etched into the silicon using a mask aligner and a dark-field photo mask, at an ultraviolet light power density of 20 mW/cm^2 for 15 seconds. The dark-field mask has openings in the emulsion or chrome which correspond to the areas where photoresist is to be removed, since 1400–37 is a positive resist. The etch pattern must either be aligned to the <110> direction using the wafer edges, or to a pre-aligned front-side metallization layer using infra-red alignment techniques.
  g. Develop in MF319 developer using a 5:1 MF319:H_2O solution for 60 seconds.
  h. Hard bake 30 minutes at 110°C in an oven.
- Masking Layer Removal
  a. Silicon dioxide masking layers can be removed using buffered hydroflouric acid (BHF). The etch rate is approximately 1000 Å/minute at room temperature.
  b. Silicon nitride masking layers are removed with a CF_4 plasma etch. In this process, the etching chamber is pumped down to 75 mTorr and CF_4 and O_2 are then flowed in at about 20 sccm and 0.5 sccm, respectively; the CF_4 flow rate is adjusted until the chamber pressure reaches 250 mTorr. After allowing the system pressure to stabilize, a 100 W RF plasma is ignited which will etch the nitride at a rate of approximately 700 Å/minute. The photoresist masking layer described in the previous steps can safely withstand 11–12 minutes of the plasma etch, but etch durations should be closely monitored if thinner photoresist products (e.g., AZ5214) are employed. When removing the middle nitride layer of the tri-layer composite membrane described in Dielectric Membrane Growth, the integrity of the photoresist mask is critical for the final SiO_2 etch using BHF. The photoresist etch rate in the plasma can be as high as 1500 Å/minute.
- Silicon Etching with EDP
  a. Prepare the EDP solution by combining the following ingredients in a large glass beaker, in the order listed: 96 mL of de-ionized H_2O, 96 gm of catechol, 1.8 gm of pyrazine, and 300 mL of ethylenediamine. (Different quantities of the solution can be mixed by proportionally adjusting the amount of each substance.) Cover the beaker tightly with heavy duty aluminum foil, place on a hot plate, and heat the solution to 110–112°C. It is convenient to use a thermometer probe with feedback to maintain a constant temperature. All mixing, heating, and etching must be done inside a well-ventilated fume hood.
  b. While the EDP is warming up, the final masking layer removal steps should be completed to expose the bare silicon. For example, this might pertain to the BHF etch of the lower thermal oxide layer of the membrane described in Dielectric Membrane Growth. Any native

oxide growth will impede the etching process, and should thus be removed using a quick (30sec) BHF dip. Photoresist can also be stripped off using acetone and IPA, since it will eventually come off in the EDP.

c. Place the wafers in a Teflon holder and place the holder in the heated EDP solution. Be certain to keep the beaker covered. The etch rate is approximately 1.2–1.4 μm/minute, and thus it takes 6.5–7 hours to etch completely through a 500 μm-thick wafer. These results pertain to fairly wide cavities (1–1.2 mm) and include the effects of "notching" (Findler et al., 1982), which refers to the increased etch rate along the cavity edges with respect to the rate in the center of the lower cavity surface. Narrower cavities, particularly those which come down to a point, tend to etch at somewhat higher rates.

d. When the etching is complete, the samples should be rinsed in warm de-ionized water, acetone, and IPA for approximately 15 minutes apiece. The samples should then soak in warm methanol for 6–10 hours to completely remove any EDP residue.

In certain applications it is convenient to use a thin Cr-Au layer to mask the EDP. The metallization can be deposited using the image reversal and lift-off procedure outlined in Metallization Pattern Definition. Also, in situations where different parts of a sample need to be etched to different depths, a multi-step etching procedure can be employed (Drayton et al., 1995; Chi and Rebeiz, 1994). In the first stage the masking layers are removed only from the areas which require the most etching, and the sample is placed in the EDP for a pre-determined amount of time. The sample is then removed from the EDP, cleaned with the water/acetone/IPA/methanol sequence (using a shorter duration for the methanol soak), and the masking layer is then removed from the other desired etch regions. The sample is then placed back in the EDP solution to complete the etch.

Backside Metallization

With many of the micromachined circuit geometries, it is necessary to deposit metallization on the backside of the circuit wafer following the silicon etching procedure. In some cases this may simply entail metallizing the entire back surface, which is easily accomplished using evaporation or electro-plating. The process is somewhat more complicated for the membrane-supported microshield line, since the metal must be selectively deposited inside the lower shielding cavity. It is necessary to cover the cavity sidewalls and some portion of the backside of the membrane, to provide an RF short between the upper ground planes and the cavity. To prevent a similar shorting of the transmission line itself, however, the region beneath the slots in the coplanar conducting lines must be shielded from the metallization. This selectivity is achieved with the use of the "shadow" mask illustrated in Figure 120.8. The mask is a silicon wafer that is processed along with the circuit wafer, and has openings etched into it through which the evaporated metal is allowed to pass. The shadow mask is correctly positioned on the backside of the circuit

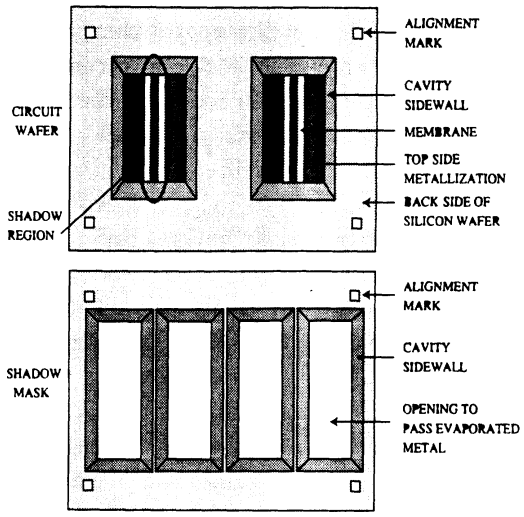


Figure 120.8 The etched shadow mask used for backside Metallization of the wafer.

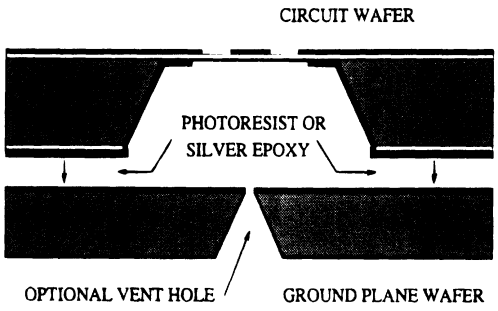


Figure 120.9 Final circuit assembly.

wafer using small alignment cavities that have been etched into each wafer, and temporarily attached using the photoresist adhesion technique described in the next section. The achievable resolution limit of this method is approximately 50 μm. Following the metal evaporation, the shadow mask is removed by soaking the wafers in acetone.

Circuit Assembly

The final phase of the fabrication sequence generally involves the assembly of two to three stacked wafer pieces, such as the ground plane, circuit, and shielding cavity (Figure 120.9). Accurate positioning of each level mandates the incorporation of alignment mechanisms such as patterns in the metallization, and micromachined cavities in the silicon which are etched completely and/or partially through the wafer. These alignment marks should be considered in the first phase of the circuit design.

Two convenient adhesives for bonding the wafers together are photoresist and silver epoxy. The photoresist technique is very useful for temporary assembly, and is common laboratory practice for the purpose of making electrical performance measurements. Using this approach, small drops of a photoresist such as 1400–37 are applied to a wafer, and then two pieces are aligned under a microscope or mask-aligner. The assembled wafers are then baked on a hot-plate at 130°C for approximately 60 seconds to cure the photoresist. The wafers can easily be separated by

soaking them in acetone. The silver epoxy technique follows the same basic steps and will also provide electrical contact if necessary. After applying the epoxy, the wafers are aligned and then baked in an oven at 100–120°C for approximately 2 hours, forming an essential y permanent bond between the wafers. The elevated cure temperature results in a high-conductivity contact.

In some cases it is desirable to provide a path for the release of gases when completely enclosing a cavity. For example, when the lower shielding cavity of a membrane-supported geometry is sealed, the membrane may be slightly deformed during the cure of the adhesive. Gases can be allowed to escape either by leaving some part of the contacting wafer surfaces free from photoresist or silver epoxy, or by putting scribe lines in the ground plane which lead out from the inside of the cavity. Alternatively, small air-holes may be etched into the ground plane wafer.

120.4 Membrane-Supported Distributed Circuits

The performance advantages of membrane supported transmission lines can be clearly demonstrated by observing the characteristics of various distributed circuits which are common to planar microwave circuitry and MMICs. The broadband TEM propagation afforded by membrane supported transmission lines permits a significant increase in performance levels for typical planar circuits such as filters, stubs, and power dividers. With conventional substrate supported designs, frequency dependent mechanisms such as radiation loss and dispersion may limit the operating bandwidth of distributed circuits, and may also serve to preclude their use for higher frequency applications. In the following sections, a summary of membrane supported distributed circuits which have been fabricated at the University of Michigan will be presented. In all cases, measurements were made on a vector network analyzer (HP8510) and a Thru-Reflect-Line (TRL) calibration technique was employed to deembed the measurements o the reference planes of the circuits.

Low Pass Filters

Perhaps the simplest example of a low pass filter is the stepped-impedance type of filter which uses short transmission line sections to approx mate the effects of a series-L/shunt-C configuration (see Figure 120.10). In this type of filter, series inductances are approximated by short sections of high-impedance transmission line, while low-impedance sections mimic the behavior of shunt capacitors. These transmission line sections may be cascaded to generate the required number of filter poles, and their lengths can be designed to produce either equal ripple (Chebyshev) or maximally flat (Butterworth) filter responses. The benefits of using membrane supported line for low pass filter applications are two-fold: first, the absence of the dielectric substrate ensures low passband insertion loss as a result of reduced dielectric and radiation losses; second, broadband TEM operation preserves the high frequency rejection of the filters, since performance degradation by higher order modes is avoided.

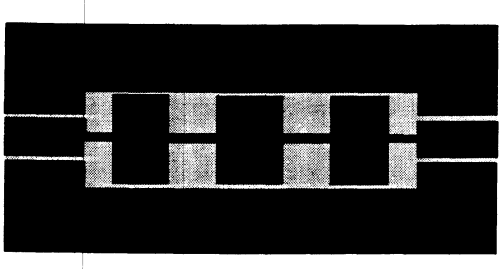


Figure 120.10 Layout of a typical stepped-impedance low pass filter in a CPW type of geometry.

With these benefits in mind, low pass filters have been studied using the microshield line geometry. First, a 5-section, 0.5 dB equal ripple, filter has been designed and measured from 10–40 GHz (Weller et al., 1993c). As shown by the results presented in Figure 120.11, the filter has a cutoff frequency of 26 GHz and a rejection of −25 dB at 40 GHz. The passband insertion loss remains less than 1 dB up to 23 GHz. The measured response agrees very well with theory up to 40 GHz, and the theoretical data for higher frequencies have been plotted to show the filter performance up to 80 GHz.

A microshield line low pass filter for W-band applications has also been designed (Robertson et al., 1994). This filter uses the same stepped-impedance geometry as discussed above, and is based on a 7-section, 0.5 dB equal ripple prototype. Once again, measured results are presented with theory (see Figure 120.12) and excellent agreement is achieved. The W-band filter has a cutoff frequency of 90 GHz, with pass-band insertion loss as low as 0.5 dB and out of band rejection better than 20 dB at 110 GHz. Measured data is presented from 75–110 GHz, which corresponds to the limitations of the test equipment, and theoretical data is shown for the frequency range of 40–140 GHz.

During W-band measurements, data were taken that allowed the extraction of the effective relative dielectric constant ($\epsilon_{r,eff}$) of the microshield line from 75–100 GHz (Marks and Williams, 1993). The graph of $\epsilon_{r,eff}$ in Figure 120.13 illustrates the very

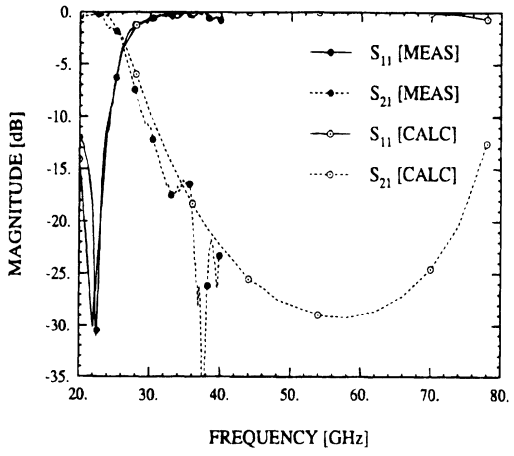


Figure 120.11 Measured S-parameters for a 5-section microshield low-pass filter. Theoretical data is from a method of moments full wave analysis (Pengelly and Schumacher, 1988).

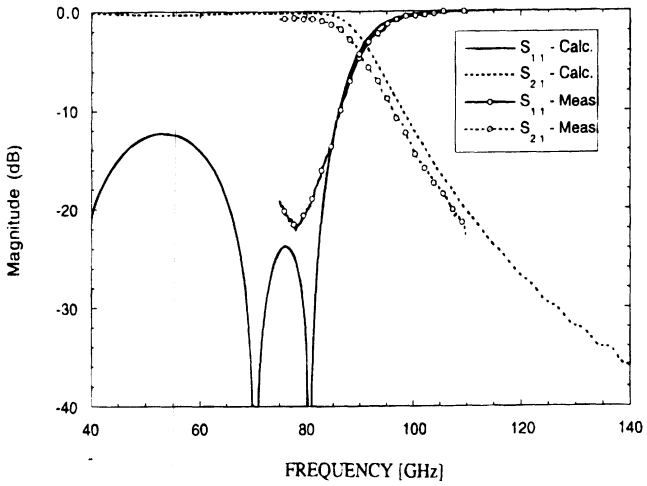


Figure 120.12 Measured and predicted response of a 90 GHz microshield low pass filter. Theoretical data is from a finite-difference time-domain full-wave analysis technique (vanDeventer et al., 1989).

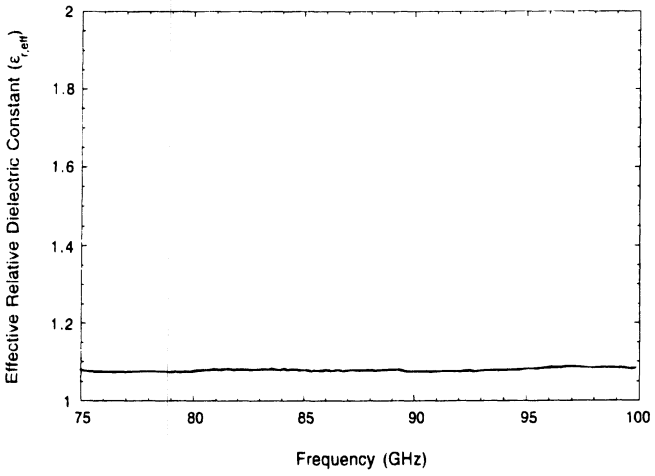


Figure 120.13 Measured effective relative dielectric constant ($\epsilon_{r,eff}$) of a microshield line from 75–100 GHz (Robertson et al., 1994).

minor influence of the membrane on the propagation characteristics of the microshield line. The presence of the dielectrics results in a value of 1.08 for $\epsilon_{r,eff}$, instead of the unity value that would be expected if the signal were propagating entirely in air. Also, very low dispersion is indicated, since the measured $\epsilon_{r,eff}$ remains very nearly constant vs. frequency.

Microshield Series Tuning Stubs

The microshield geometry is also well suited for implementing series type resonant stubs commonly seen in CPW circuits. These types of stubs form the basis for the design of resonant circuits such as filters and matching networks. Generally, stubs which are incorporated into planar transmission lines perform better when they are printed in the center conductor of the line instead of in the ground plane regions on either side of the line. This performance benefit results mainly from reduced parasitic loss caused by radiation from the stub.

Both open-end and short-end series stubs have been fabricated and measured at the University of Michigan (Weller et al., 1995b). The configuration for a typical open-end series stub is shown in Figure 120.14a This stub has a bandpass response when the length is equal to $\lambda_g/4$, and is useful in applications such as DC blocking and LO isolation. The measured response of an open-end series stub is given in Figure 120.14(a) along with theoretical response. The plot also shows the predicted radiation loss, which is below −25 dB throughout the first resonance of the stub. The short-end series stub is very similar to the open-end configuration, as shown in Figure 120.14b. This stub exhibits a band stop characteristic at it's first resonance, as demonstrated by the measured performance.

Wilkinson Power Divider

A Wilkinson power divider was the first microstrip circuit to be adapted to membrane technology (Weller et al., 1994b). Wilkinson power dividers make use of a lumped element resistor which is placed between the two output signal lines and serves to provide an input match at all three ports of the network. In the case of a membrane supported circuit, it is convenient to choose a central impedance of 106 Ω, so 73 Ω matching transformers are included at each port to match the divider to the 50 Ω terminations. The layout of a 33 GHz divider, including the matching sections, is shown in Figure 120.15a; the thin-film resistor is fabricated by evaporation of titanium to a thickness of 400 Å. For measurement purposes, the power divider was mounted on an aluminum fixture to provide the lower ground plane of the circuit and to facilitate connection to other MMIC chips via wire-bonding. The fixture also included an upper shielding surface for the power divider, since it was determined that membrane microstrip has a tendency to radiate due to the lack of high dielectric material to concentrate the electric fields within the transmission line. The *S*-parameter measurements plotted in Figure 120.15 show that the power divider performs well, with better than 15 dB isolation between the two output ports. Analysis of the measured results indicates that the insertion loss for a single divider is approximately 0.2 dB, compared to results of 0.4–0.5 dB for conventional microstrip based circuits (Hamadullah, 1988).

Lange Coupler

Lange (1969) first reported a 3-dB interdigitated microstrip hybrid in 1969. Due to the advantages of broad-band, low-loss and tight-coupling available in his design, the use of the Lange-coupler (Figure 120.16) as a directional coupling scheme has gained popularity among microwave engineers since then. Also due to the perfect symmetry in the design, a Lange-coupler can provide a 90-degree phase difference between the direct port and coupled port over a very wide frequency range (Figure 120.17). Therefore, Lange-couplers have been widely used in balanced amplifiers, single-balanced mixers, image rejection mixers, and phase shifters designed to achieve both phase and amplitude balance. Usually Lange-couplers are designed on a high dielectric constant material such as Duroid or GaAs. At millimeter wave range, the losses from these dielectric materials start to increase and can disturb the performance of the Lange-couplers. However,

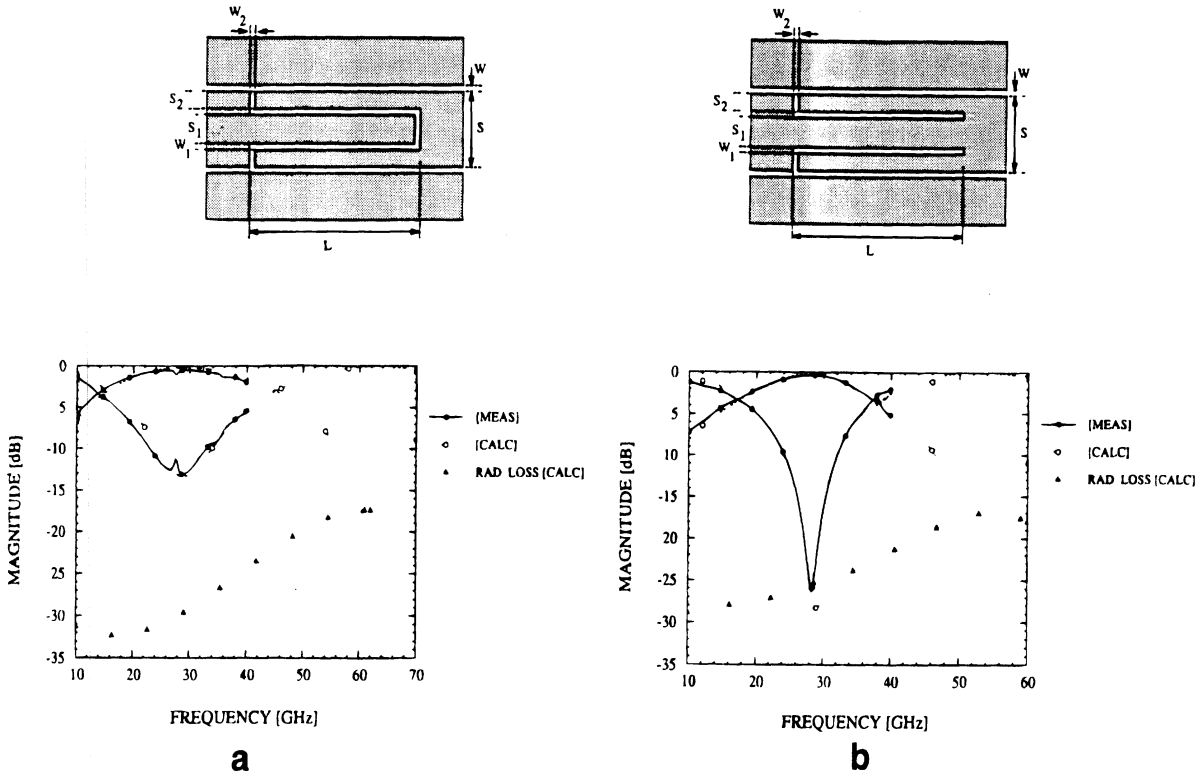


Figure 120.14 Measured S-parameters for open- and short-end series stubs in microshield line: (a) open-end series stub. (b) short-end series stub.

with micromachining technology, Lange-couplers can be built on a thin dielectric membrane to reduce the dielectric loss and improve the performance of the coupler for millimeter wave applications. Based on this concept, a membrane micromachined Lange-coupler has been built on a 350 μm silicon wafer, as shown in Figure 120.18. Grounded coplanar waveguides (GCPW) are used as the input/output feeding structures in the design. Also, six fingers are used to increase the coupling between fingers. The Lange-coupler has been tested from 5 to 20 GHz and the measured results are shown in Figure 120.19a. The coupling bandwidth ranges from 7 GHz to 19 GHz with an isolation better than −18 dB and return loss better than −13 dB. The phase difference between the coupled-port and the direct-port is shown in Figure 120.19b.

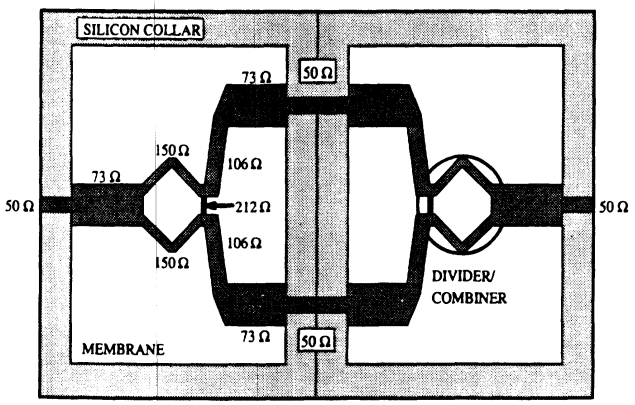
Resonators on Membrane

In this section, the performance of stripline and microstrip resonators on thin dielectric membranes will be discussed. The microstrip and stripline resonators are fabricated on a 350 μm-thick high-resistivity silicon wafer using the techniques discussed in Fabrication Methodology. The length of the meander resonator shown in Figure 120.18 is $\lambda_0/2$ at 13.5 GHz and its width is 500 μm. The metallization is gold electroplated to a thickness of 3 μm. The stripline resonator impedance is calculated to be 80.8 Ω and the microstrip resonator impedance is 104 Ω. The resonators are coupled by 150 μm gaps in the 50 Ω feeding transmission line. The measured S_{21} of each resonator is shown in Figure 120.19. The resonant frequencies for the stripline resonator are 13.555 GHz, 27.365 GHz and 39.636 GHz (Figure 120.19a), and are not exactly integer multiples of each other because the gap-coupling capacitance changes with frequency (Chang et al., 1993). Also, the peak S_{21} increases with frequency from −25.8 dB at 13.55 GHz to −10.4 dB at 39.36 GHz also due to the increase in the gap-coupling capacitance. The resonant frequencies for the microstrip resonator are 13.815 GHz and 27.163 GHz. No resonant frequency is seen at 39 GHz due to radiation loss. Table 120.3 shows the measured loaded-Q (Q_L) and the extracted unloaded-Q (Q_u) of these resonators in stripline and microstrip modes.

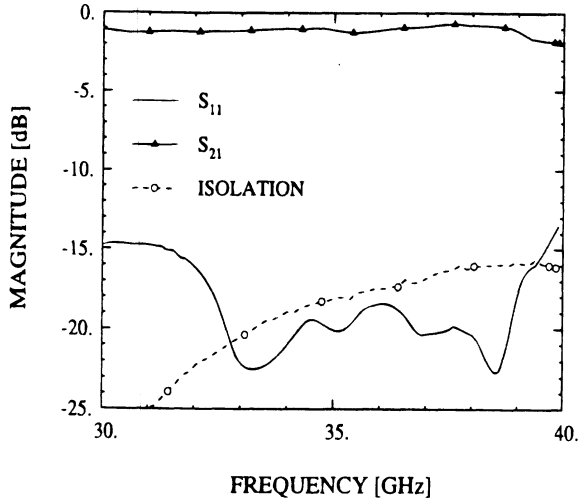
As is evident in Table 120.3, the stripline Q_s increases as $\sqrt{f}$ with frequency. This is an indication of conductor-loss limited performance and the absence of dielectric and radiation loss mechanisms. On the other hand, the microstrip line resonator suffers from radiation loss and its unloaded-Q decreases with frequency. The 13 GHz Q_u is 235 for the microstrip resonator and is about 15% less than that of the stripline resonator due to a small component of radiation loss. At 27 GHz, the radiation loss component is comparable to the conductor-loss component resulting in Q_u = 205 which is around half the value of the stripline resonator at this frequency. At 39 GHz, the radiation loss is very high and no Q-measurements could be done. It is possible to reduce the radiation loss by decreasing the height of the substrate or by increasing the width of the microstrip line.

Interdigitated Bandpass Filters

Micromachining has also been exploited to realize compact interdigitated filters for K-Band and Ka-Band (Chi and Rebeiz,



a



b

Figure 120.15 (a) Schematic of a membrane microstrip Wilkinson power divider, and (b) Measured *S*-parameters of back-to-back Wilkinson power dividers fabricated on membrane. Isolation was measured between the two output ports of a single divider.

1994). The interdigitated filter geometry, shown in Figure 110.20(a), uses quarter wavelength resonators similar to the structure discussed above. The resonators are implemented in a stripline configuration and coupled together in a broadside manner. They are suspended on a membrane between two shielding surfaces, but in this case, the shielding enclosure is provided not by a separately machined metal fixture, but by micromachined cavities which are integrated into the filter design. This integrated machined cavity structure, as illustrated by the two-dimensional cross-section in Figure 120.20(b), allows the filter to be fabricated with very small dimensions, allowing its use for high-frequency applications. In addition, the filter design itself is very compact, and can be used to realize filters for a wide range of bandwidths. Another advantage of the interdigitated filter geometry is that the second passband occurs at three times the bandpass frequency.

Synthesis of this filter is not easily accomplished using simple theoretical models, due to the effects of mutual coupling between multiple resonators, including non-adjacent resonators. As an alternative to complex and time consuming full-wave analysis techniques, microwave modeling is used to iteratively design the filter. The microwave model takes the form of a large scale replica of the micromachined filter which operates at 850 MHz. Since a pure TEM mode is excited within the structure, the measurements of the scale model provide a direct correlation to the performance of a miniature filter. And since the scale model can be easily handled and modified, its design can be modified and remeasured with great speed. This allows the design to be optimized before fabrication of the miniaturized interdigitated filter is initiated.

Measurements on the actual micromachined filter are performed through the use of grounded-CPW (GCPW) feed lines which enter the filter cavity through tunnels etched in the top wafer of the cavity assembly. Measured results from 2 to 40 GHz are shown in Figure 120.21, and are compared to scaled measurements of the microwave model performance. The micromachined filter exhibits a return loss better than −15 dB within the passband and a 1.7 dB port-to-port insertion loss at 20.3 GHz. The filter response is predicted very well by the scaled response of the microwave model.

Coupled Line Bandpass Filters

The coupled line bandpass filter is a familiar structure which has found use in many applications that employ microstrip transmission line. It also utilizes the half-wavelength resonator structure discussed earlier, but this type of filter cannot be used at higher frequencies since radiation losses and dispersion associated with the dielectric substrate become so large that filter performance is severely compromised. With membrane supported transmission line technology, however, coupled line bandpass filters which exhibit very high performance have been realized (Robertson et al., 1995). The geometry used for these filters is slightly different from previously discussed microstrip and stripline designs, however, in that it uses micromachining to precisely define the ground plane spacing for the microstrip line. Instead of relying on default wafer thickness to determine shield spacings, this structure employs micromachining to control vertical dimensions which are specified by the electrical performance requirements of the circuits. An example of this type of micromachining is illustrated in Figure 120.22, in which a three wafer assembly comprises a shielded membrane microstrip circuit structure. The middle circuit wafer contains the membrane supported conducting lines of the structure, while the lower ground plane wafer provides the micromachined cavity which acts as a ground to the conducting lines. The third wafer, on top of the assembly, remains completely planar, and is used simply for shielding and enclosure of the circuits. Fabrication of the ground plane wafers uses the 2-sided etching technique discussed in Silicon Micromachining to include windows which allow for on-wafer measurements of the circuits.

On-wafer probing is further facilitated by the use of GCPW probe pads which are required for the ground-signal-ground configuration of the probes. Since the filters are microstrip in

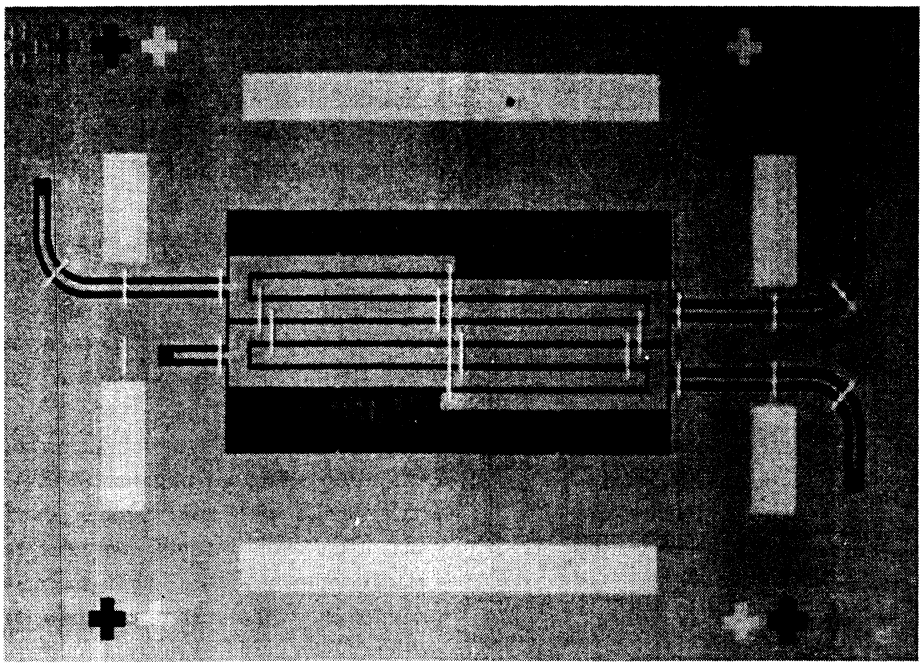


Figure 120.16 Photograph of a Lange coupler fabricated on a thin dielectric membrane. The membrane area appears lighter than the siiicon areas. Note the use of air-bridge technology integrated onto the membrane.

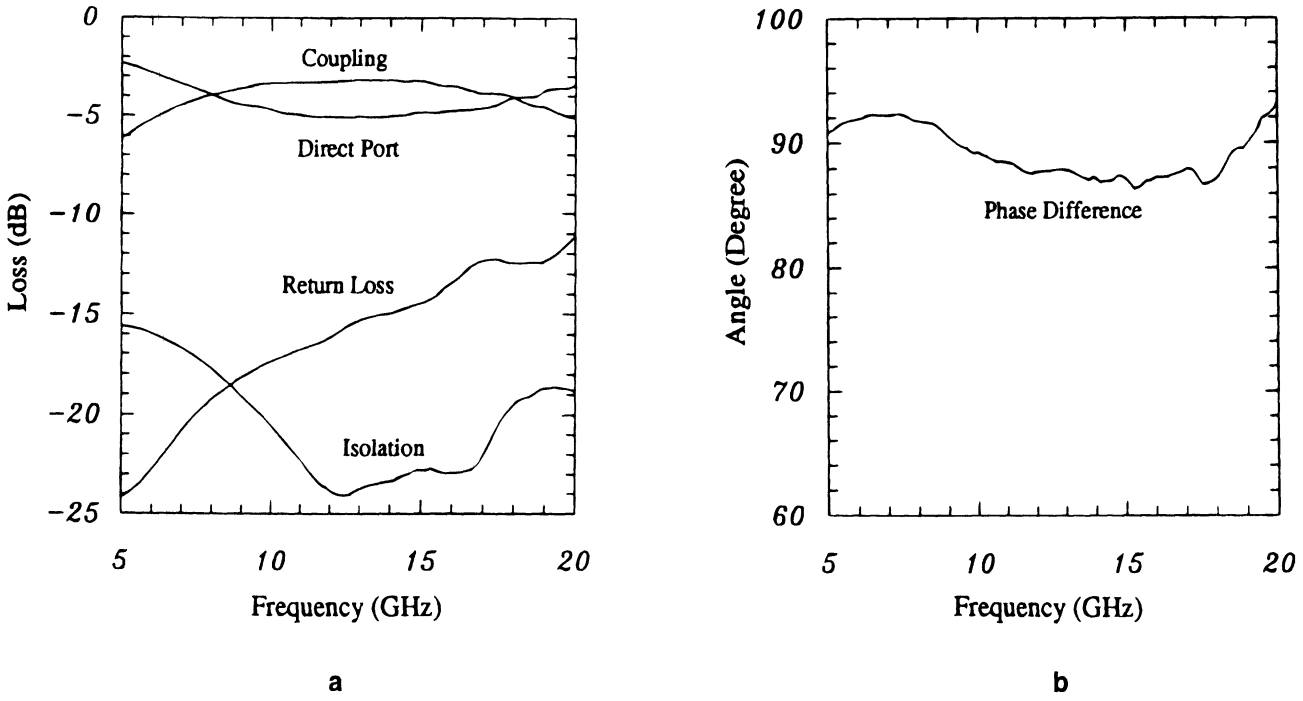


Figure 120.17 Measured performance of a membrane supported Lange coupler. (a) Direct and coupled port transmission, input return loss, and isolation. (b) Phase difference between the two output ports.

nature, a transition which utilizes a Klopfenstein impedance taper is used. This transition serves dual purposes of matching the 50Ω probe impedance to the 90Ω microstrip impedance and rotating the electric fields from their horizontally opposed configuration at the probe tips to a vertical orientation consistent with the dominant mode of microstrip propagation.

Development of bandpass filters for W-band applications is not readily accomplished with conventional quasi-static synthesis techniques available for low frequency filter design. Full-wave analysis techniques must therefore be employed for accurate circuit simulation. These techniques are generally computationally intensive and time consuming, however, so a low frequency modeling approach like that discussed in Interdigitated Bandpass Filters is adopted. Experimental iteration of the circuit design can be easily accomplished with this method, and accurate results may be obtained. Several coupled line bandpass filters have been

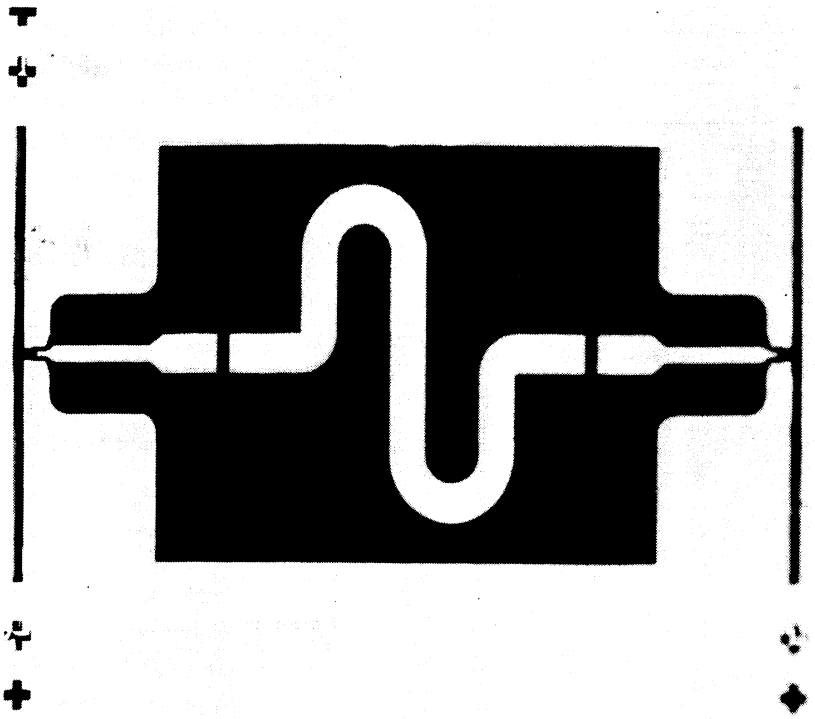


Figure 120.18 Photograph of a resonator structure fabricated on a thin dielectric membrane to study the difference between microstrip and stripline quality factors (Q's).

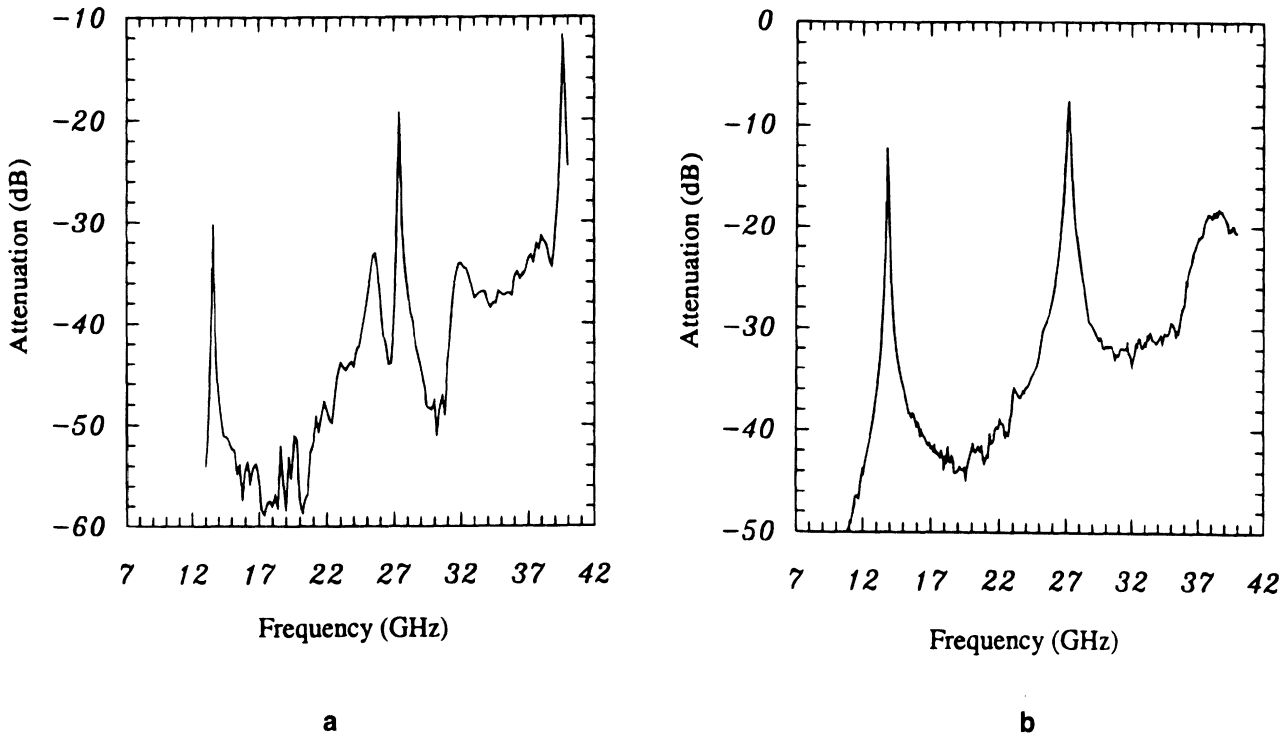


Figure 120.19 Measured insertion loss of (a) stripline and (b) microstrip resonators fabricated on membranes.

developed using a combination of full-wave analysis and modeling techniques. They are all based on equal ripple Chebyshev prototypes, and an example of one of these filters is pictured in Figure 120.23. This photograph shows a narrow-band 5-section filter, including the transitions and probe pads used for on-wafer characterization. The shielding wafer has been removed to view the top surface of the circuit, and the membrane area of the circuit appears dark compared to the lighter gray silicon support rim. Figure 120.24 shows a graph of the measured S-parameters of this filter from 75–110 GHz. The filter performance is characterized by low passband insertion loss, very sharp roll-off, and good out-of-band rejection. This level of performance cannot

Table 120.3 Measured Values of Loaded-Q and Extracted Values of Unloaded-Q for Stripline and Microstrip Resonators.

	Stripline			Microstrip	
	f_{01} (GHz) 13.555	f_{02} (GHz) 27.365	f_{03} (GHz) 39.636	f_{01} (GHz) 13.185	f_{02} (GHz) 27.163
Q_L	258	331	304	155	110
Q_u	272	386	465	234	207
$Q_{u,f}/Q_{u,f_{01}}$	1	1.42	1.71	1	0.88
$\sqrt{f/f_{01}}$	1	1.42	1.71	1	1.40
Skin Depth (μm)	0.676	0.478	0.395	0.676	0.478
α_T (NP/cm)	0.0052	0.0073	0.0111	0.0060	0.0137
R_s (Ω/cm)	0.84	1.18	1.80	1.25	2.85

be duplicated easily with conventional substrate supported structures, and can only be surpassed by expensive rectangular waveguide designs. While the waveguide filters predictably show better performance than the planar filter, the advantages of the planar filter in terms of cost, fabrication, and integrability are significant.

120.5 Conformal Micromachined Packaging

Planar transmission lines such as microstrip, stripline, and coplanar waveguide (CPW) have become conventional structures to use in the design of microwave and millimeter wave circuits due

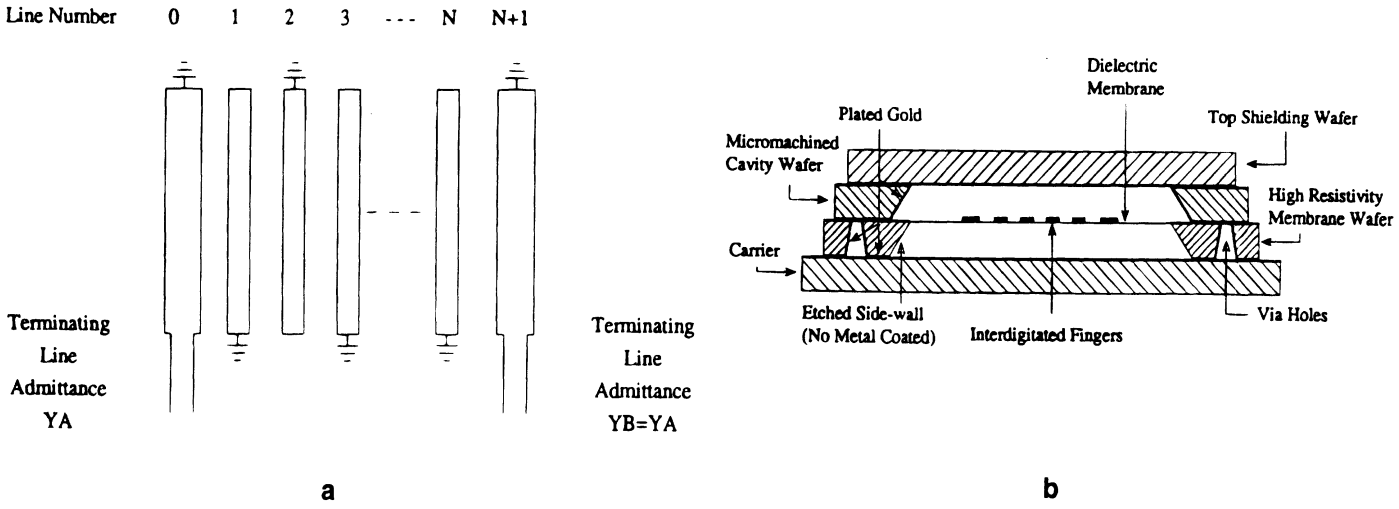


Figure 120.20 Interdigitated filter (a) circuit layout, and (b) two-dimensional geometry used to realize membrane suspended resonators.

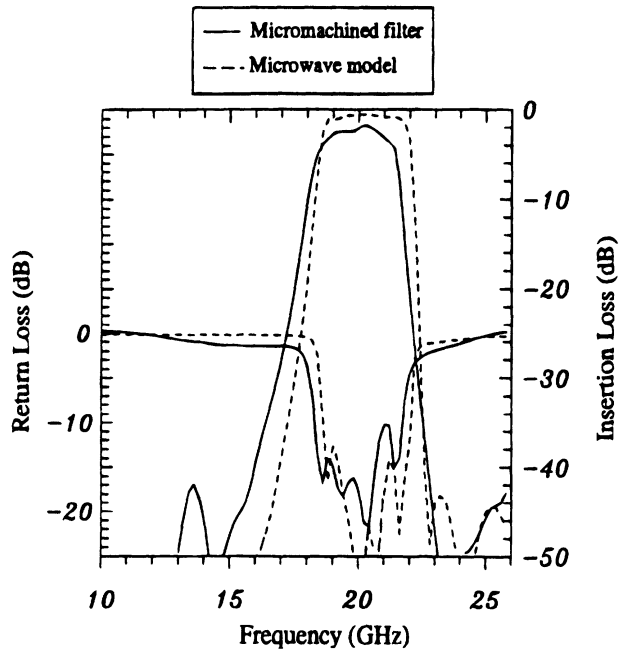


Figure 120.21 Measured response of the interdigitated membrane filter, shown with the scaled measurements of the microwave model.

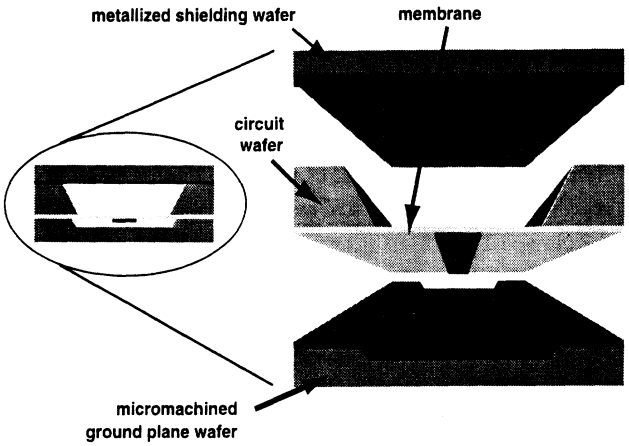


Figure 120.22 Schematic cross-section of a shielded membrane microstrip transmission line. The ground plane wafer and the circuit wafer are micromachined separately and then assembled with the metallized shielding wafer.

to the flexibility provided in fabricating passive components with predefined electrical functions as well as the enhanced ease in mounting active devices. Although microstrip and stripline have been utilized the most in passive circuits, limitations in mounting active devices have made the use of coplanar waveguide more popular since its physical geometry provides inherit advantages. A commonly observed problem in many of these lines, however, is degradation in circuit performance that results when coupling mechanisms associated with parasitics are excited along with radiation effects that arise in dense circuit environments. In order to address the above concerns, the development of a transmission line geometry that offers electrical performance comparable to conventional ones, maintains ease in device mounting, and reduces undesirable coupling effects, is required. This can be obtained with independent shielding of specific circuit components that can be achieved using micromachining techniques.

Since most high frequency circuit applications address development, modeling, fabrication and experimental characterization of systems prior to packaging, the effect of the housing on the electrical performance is very difficult to predict. As a result, the electrical response of many packaged circuits suffers significant performance degradation, mainly attributed to the introduction of unwanted parasitics along with the excitation of multiple shielding resonances resulting from the interaction between the circuit board and metallic housing. To address the issue of proximity coupling and cavity resonances, monolithically integrated cavities can be developed which provide effective shielding to individual components while maintaining an overall geometry that is small enough to avoid the multiple resonance excitation in the range of operating frequencies. From a cost perspective, since conventional housing elements can be rather expensive and impractical to optimize for each generic circuit board, a solution toward cost minimization is easily achieved by using micromachining techniques. Consequently, for system level designs where weight and volume reduction as well as controllable parasitics are critical issues, overall system costs are directly reduced using these techniques.

Since micromachining techniques are well-established in sensor applications, a wealth of information has been discovered on various processing techniques. This has been especially useful in the extension of micromachining techniques from the MEMS arena to high frequency circuit design where emphasis is being placed on the development of self-packaged miniature circuit components used for high frequency systems. In the area of packaging such components, a completely shielded (or self-packaged) micromachined circuit has been developed that is excited by a traditional planar transmission line based on coplanar waveguide. This planar structure is surrounded by an air-filled cavity in the upper region and a substrate-filled one beneath the line as shown in Figure 120.25. To address the specific design issues of shielding and isolation, a variety of micromachining processes have been explored and studied to identify the approach that provides circuits with the best electrical performance at these frequencies. Demonstration of the concept of micromachined circuits for RF applications is given through simple circuit components such as a tuning stub and lowpass filter. These simple components have been developed and their performance has been measured and compared to conventional transmission lines (Drayton and Katehi, 1993c), in this case coplanar waveguide.

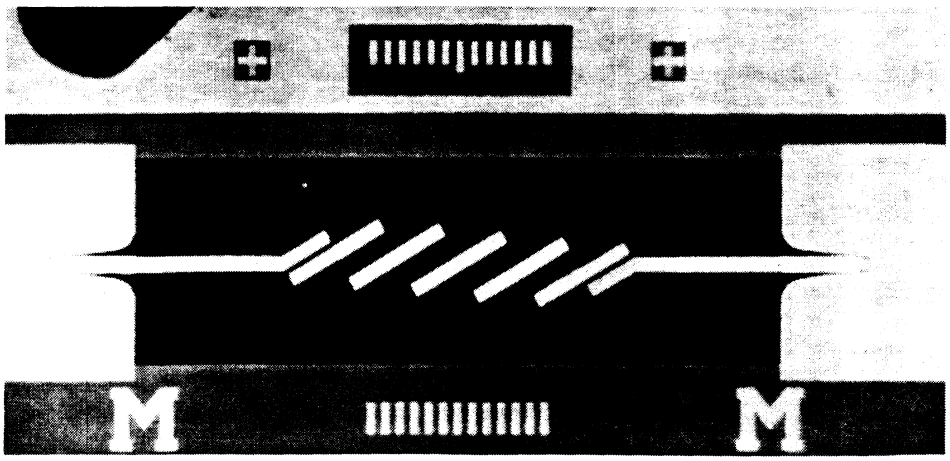


Figure 120.23 Photograph of a 94 GHz coupled line band pass filter. The photo shows the metallized side of the membrane with the micromachined ground plane wafer removed. The darker areas of the picture indicate the thin dielectric membrane.

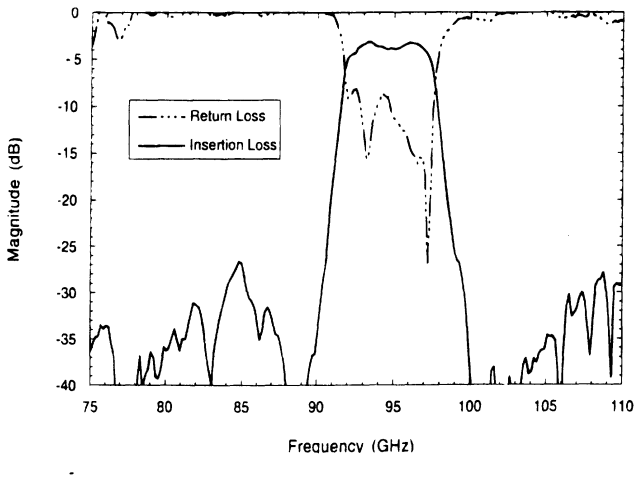


Figure 120.24 Measured response of a 5-section coupled line bandpass filter. The passband insertion loss is 3.4 dB, and the filter has a bandwidth of 6.1% centered at 94.7 GHz.

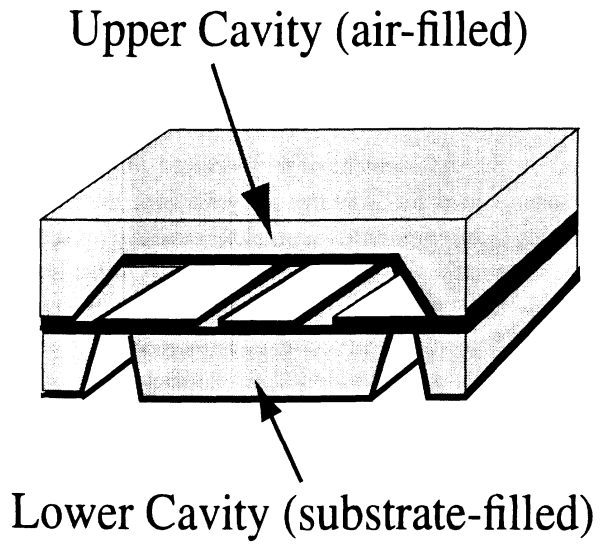


Figure 120.25 Three-dimensional cross section of micromachined lines where the shield and line are integrated monolithically.

The development of micromachined miniature circuit components for high frequency applications has been separated into two parts. The first part concentrates on *circuit development* where the response of a given circuit is determined and the specific circuit parameters are designed to achieve that response. The second part concentrates on *circuit characterization* which includes fabrication, described in Section 120.3, and measurement of the electrical performance of the self-packaged circuits with comparisons to theoretical predictions.

Design Approach for Micromachined Circuits

High frequency self-packaged micromachined circuits are developed in two parts: (a) circuit development and (b) circuit characterization. In part (a), theoretical predictions are made based on very accurate full-wave techniques (Kunz and Luebbers, 1993; Dib and Katehi, 1992; Mei and Fang, 1992; Betz and Mittra, 1992; El-Shandwily and Dib, 1990; Sheen et al., 1990; Zhang and Mei, 1988; Mur, 1981). Since these are complex and computer time intensive, they are inappropriate to use primarily as design tools. Therefore, initial circuit design is best achieved using simpler quasi-static model such as Puff (Wedge et al., 1991). With an entry level circuit design, the specific circuit geometry is determined and then analyzed using full-wave analysis techniques to verify performance. Improvements on the circuit performance are obtained though an iterative method which fine tunes the circuit dimensions to meet the given design requirements. Figure 120.26 shows a brief illustration of the procedures needed for realistic circuit development. In the circuit characterization part once the optimum design has been determined, fabrication is implemented using the procedures presented in Fabrication Methodology, and circuits are then tested to evaluate the overall circuit performance.

The micromachined circuits presented have a shielding environment that has been monolithically integrated into a two-wafer system and is made of cavities in both upper and lower regions. As shown in Figure 120.25, the upper region consists of a metallized air-filled cavity while the lower region has a substrate-filled cavity of high resistivity silicon, $\epsilon_r = 11.7$, which is also metallized on the lower side. To measure the response of these circuits, grounded coplanar waveguide (GCPW) feeding lines are used followed by upper and lower cavities that are grounded through direct contact with the ground planes of the coplanar lines. Shielding is achieved by developing a substrate-filled cavity beneath the line on the lower wafer while an air-filled cavity is formed over the line in the upper wafer. Descriptions of the individual wafer layers used to construct the completely shielded micromachined circuit are discussed in the next paragraph.

The *lower wafer* shown in Figure 120.27 consists of a high resistivity, single-side polished silicon wafer having a dielectric mask of silicon dioxide and a thickness of 350 μm. To develop

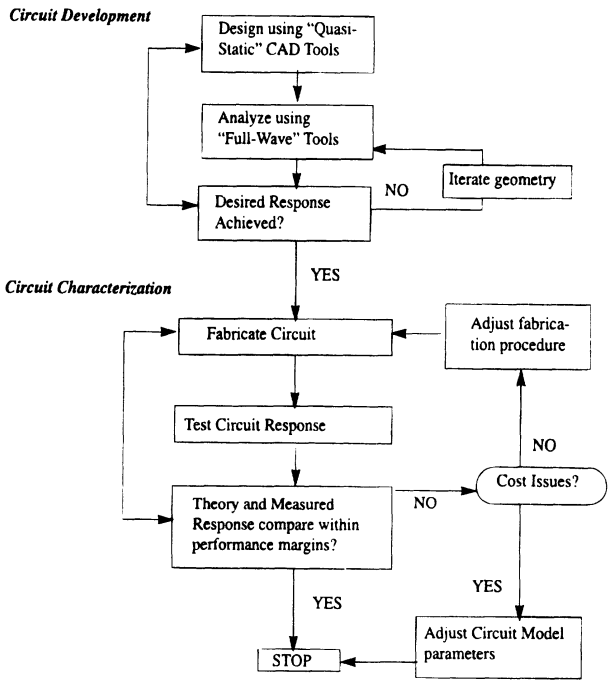


Figure 120.26 Design procedure for micromachined circuits.

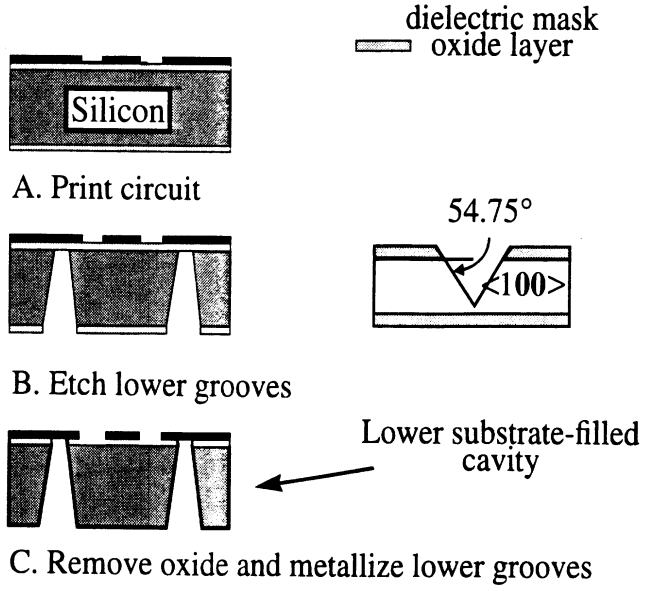


Figure 120.27 Lower Wafer Development. A. Transmission lines are printed on the top surface. B. Lower cavity is formed by etching v-grooves. C. Lower cavity grooves are metallized below the line forming direct contact to the upper ground planes.

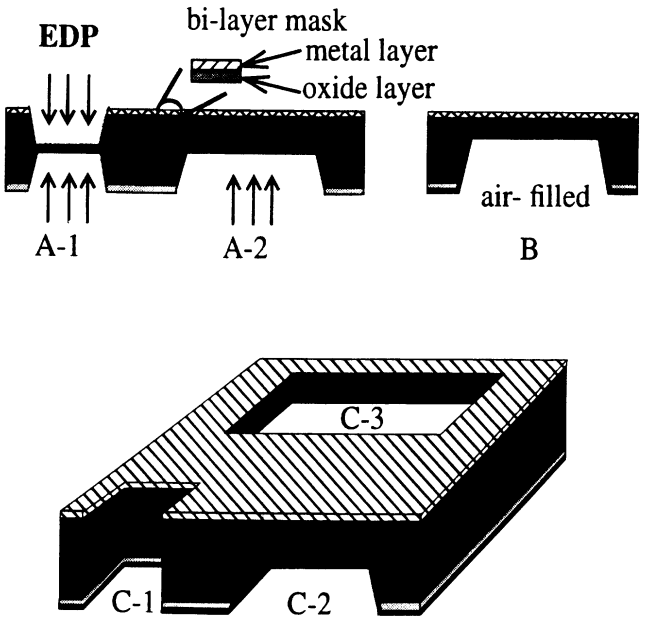


Figure 120.28 Upper Wafer Development. A. Probe windows and alignment marks (A-1) are etched from both sides while the upper cavity (A-2) is etched from one side only. B. The upper cavity is then metallized. C. Finally, the upper wafer sectional view after processing with the alignment marks (C-1), upper cavity (C-2) and the probe window (C-3).

the circuits, the planar lines are printed and electroplated to a desired thickness of 3 μm. With the circuits and alignment marks printed on the upper side, lower cavities are formed below the circuit surface by anisotropically etching the silicon away below the coplanar waveguide grounds to form a substrate filled cavity. Lastly, this cavity is metallized and electro-plated to achieve the desired thickness underneath the coplanar waveguide ground planes.

The *upper wafer*, shown in Figure 120.28, is formed utilizing a double-sided process to define the cavity areas and probe windows required to shield the circuit and allow probing access to the individual components, respectively. In this case, a 500 μm-thick, low resistivity silicon wafer with 7,500 Å of thermally grown oxide on both sides can be used. To allow the sequential etching, this requires at least two masking layers, one must be metal in order to facilitate infrared alignment. This double sided sequential etching process results in mechanically strong wafers when multiple cavities are employed, (Figure 120.30) as a result of the structural beam developed in the probe windows. This is especially useful to increase handling ease during mounting of the upper wafer.

Finally, integration of the upper shield to the lower shielded planar circuits is completed after alignment and attachment of the two wafers via the microscope using regular adhesion methods (see Figure 120.30). In applications where only upper half shielding is required, fabrication is easily achieved by excluding the lower cavity formation.

Experimental Validation and Discussion

To characterize the circuits up to 40 GHz, state of the art measurement systems utilize on-wafer probing techniques to measure planar circuit geometries. Using an HP 8510B Network Analyzer, an Alessi probe station and Cascade Microtech ground-signal-ground probes with a probe pitch of 150 μm accurate characterization is obtained using TRL calibration (Maury et al., 1987; Strid and Gleason, 1989; Ensen and Haer, 1978). As a result, all transitions between the ANA and the newly defined shielded circuit reference plane are taken into account and removed from the circuit response. Simple discontinuities have been implemented to show the realization of conventional circuits in a micromachined configuration. Two elements of interest are the *series open-end stub* and *stepped impedance low-pass filter* which are basic elements to many high frequency circuits such as filters, switches, RF blocks, etc.

The *series open-end tuning stub* has physical dimensions shown in Figure 120.31. Comparison between measurements and full wave analysis results is shown in Figure 120.32. As observed from this figure, the theoretical and experimental results exhibit a shift in the resonant frequency of about 6.9% since the micromachined circuit resonance occurs at 29 GHz compared to the 27 GHz response of the modeled circuit. Although the overall circuit performance is similar, the discrepancy in the resonant frequency can be attributed to the variations between the modeled circuit and the actual one fabricated and measured. The resonant frequency is affected by the fact that the measured line length behaves electrically shorter since there is rounding of the corners and edges of the stub fingers caused during fabrication, which is not accounted for in the model. In addition, metal thickness has been neglected although it has been found to contribute considerably to frequency shifts (Heinrich, 1990). Lastly, the difference in the magnitude between measurement and theory may be attributed to the fact that the theoretical model assumes a lossless system while in reality the circuit has both conductor and dielectric loss.

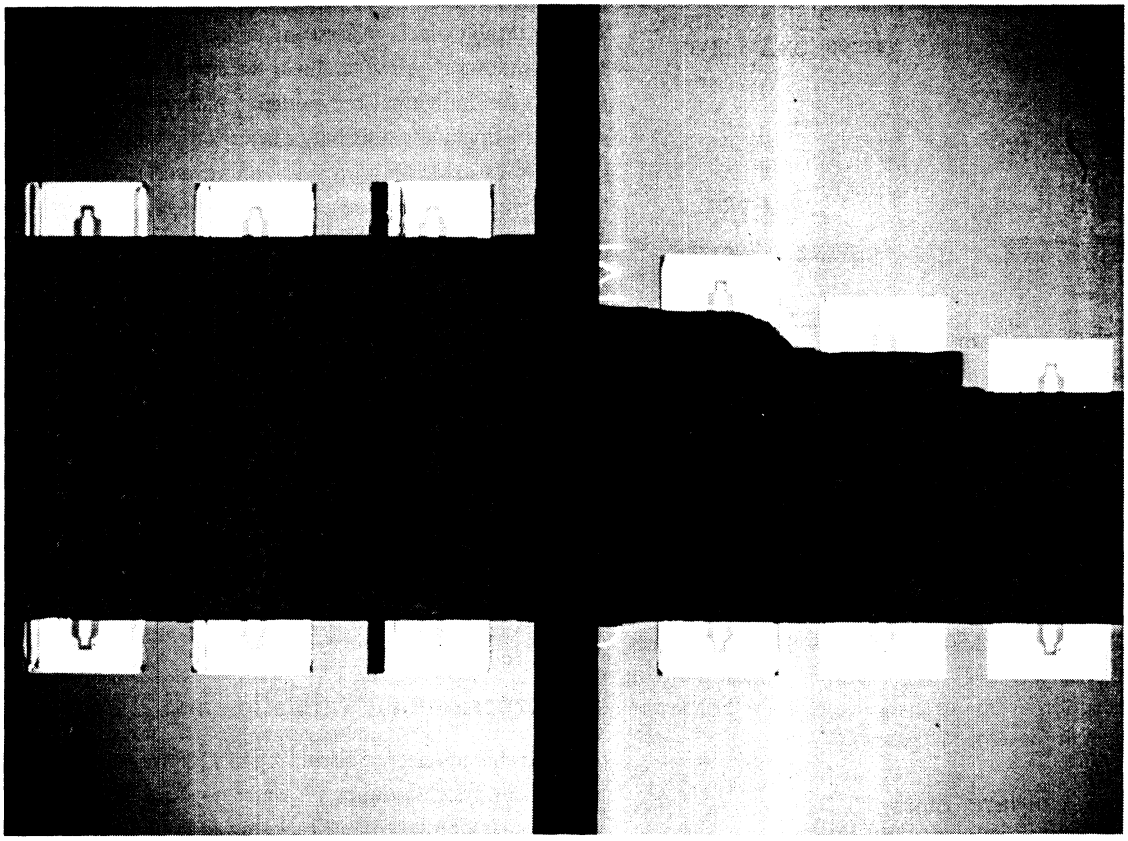


Figure 120.29 Photograph of circuit from top view where the probe windows are shown in relation to the transmission line wafer.

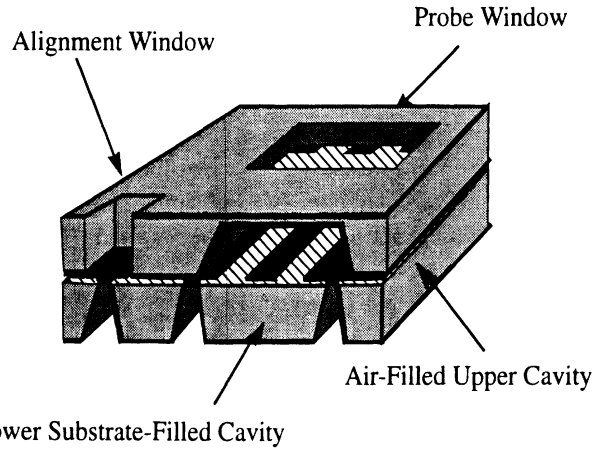


Figure 120.30 Completely shielded micropackaged circuit with lower and upper wafer alignment.

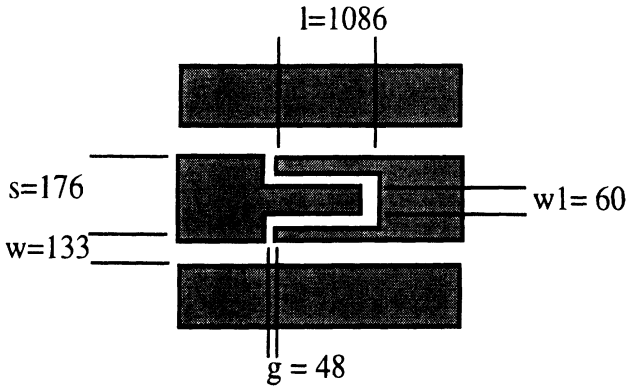


Figure 120.31 Series open-end tuning stub circuit dimensions in microns.

A *five-section stepped-impedance lowpass filter,* designed as shown in Figure 120.33, has high and low impedances of 100Ω and 20Ω respectively and is surrounded by the cavity structure described above. In Figure 120.34, measurements are shown and compared to theoretical results derived from quasi-static models where conductor and dielectric losses are included. Regarding conductor losses, care was taken to incorporate the specific metallization thickness and the appropriate surface resistivity corresponding to the various sections of microstrip line widths (van Dei enter, 1992). To realize 100 and 20 ohm impedance steps, 20 μm and 380 μm wide conductor lines are used with slot widths of 210 μm and 30μm. The total loss in the system, plotted in Figure 120.35, shows good agreement between theory and measured results thus confirming the effectiveness of the micromachined integrated shield and the elimination of loss associated with radiation effects.

To illustrate the effectiveness of the integrated shield, a lowpass filter with a series inductance is shown in Figure 120.36 where a comparison is made between the conventional coplanar waveguide circuit and the micromachined one. The performance of the grounded CPW circuit is affected by the excitation of substrate modes which add constructively and destructively to provide the ripple shown in the high-frequency end of the band. In this case, the effects are observed outside of the lowpass filter band while

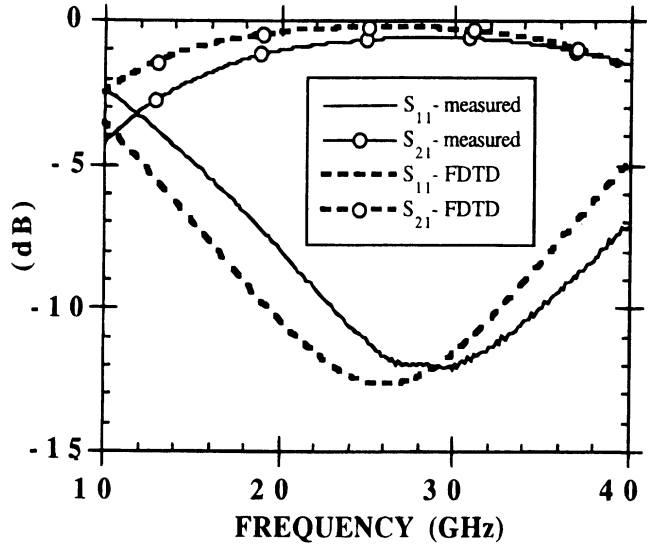


Figure 120.32 Measured vs. FDTD results for the micromachined shielded series open end stub.

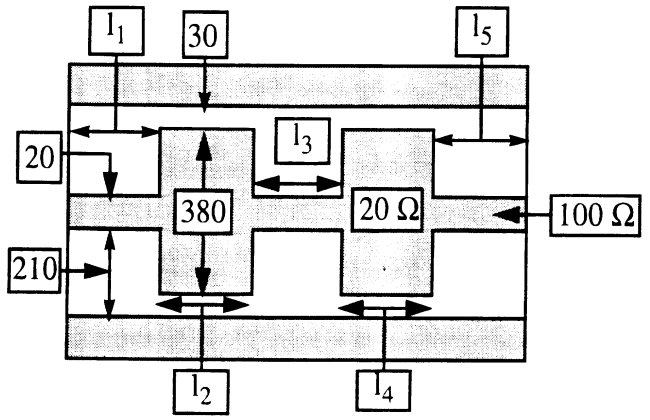


Figure 120.33 Dimensions of a 5-section stepped impedance lowpass filter having low impedance sections of 20 ohms and high impedance sections of 100 ohms.

in other filters, such as bandpass ones, the ripple could occur within the band. By choosing appropriate cavity dimensions in both regions of the micromachined shielded configuration, the effects of substrate modes are eliminated and the electrical response of the circuit in terms of the input reflection and the transmission coefficients are not affected by parasitic radiation but reveal the true characteristics of the circuit component itself.

Simple circuit geometries described above used in conventional planar line designs have been implemented in micromachined form; namely, a series tuning stub and a stepped impedance lowpass filter. The results show that micromachining offers great design flexibility to high frequency applications, while preserving electrical performance. The development of micromachined circuits for miniaturization includes highlights of the design fabrication required followed by measured results compared to quasi-static and full-wave theoretical ones. The resulting data presented prove that monolithic integration of the shield using micromachining techniques allows for the development of circuit components that offer comparable performance to conventional circuits.

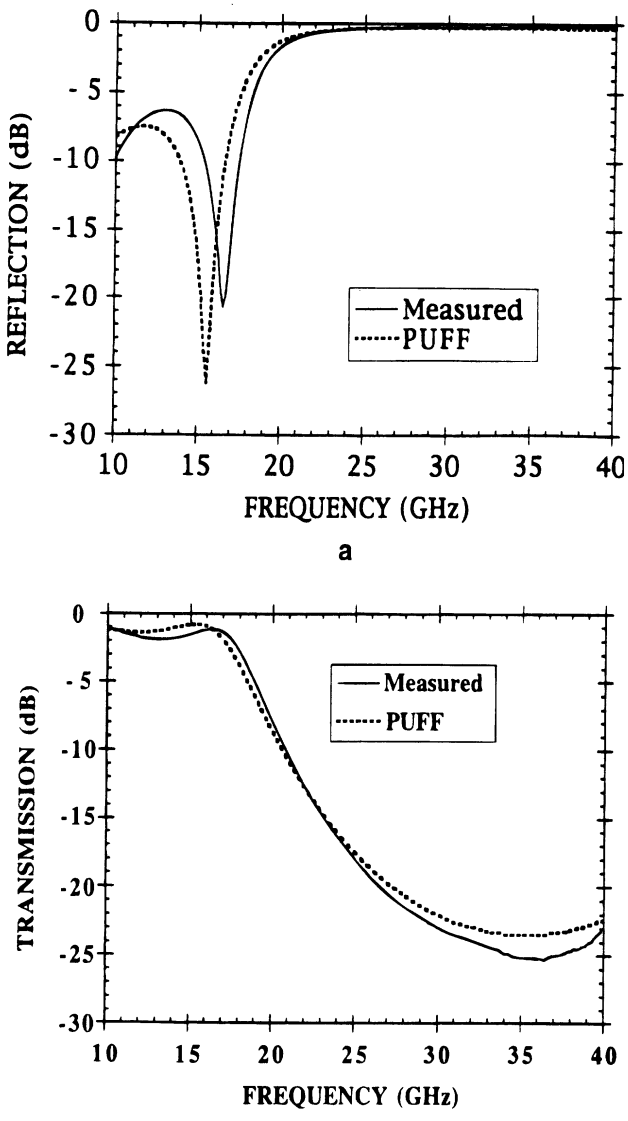


Figure 120.34 Comparison of reflection (a) and transmission (b) coefficient between the PUFF model and measured results for a 5-section stepped impedance lowpass filter.

120.6 Micromachined Lumped Elements

Planar lumped inductors and capacitors are used in most microwave active and passive integrated circuits as matching elements, bias-chokes and filter components. For frequencies below 12 GHz, these lumped elements are smaller than their transmission line equivalent circuits, and exhibit low-loss and wide bandwidth (Pucel, 1981; Alley, 1970). Recently, planar inductors have been used at 26–40 GHz and their equivalent model has been calculated using a full-wave electromagnetic solution (Abdo-Tuko et al., 1993). Still, the planar inductors show a large parasitic capacitance between the top metal and the ground plane which results in a resonant frequency between 16 and 30 GHz. The planar interdigitated capacitors also suffer from a large parasitic capacitance to ground which affects their performance as true lumped element series capacitors (Esfandiari et al., 1983).

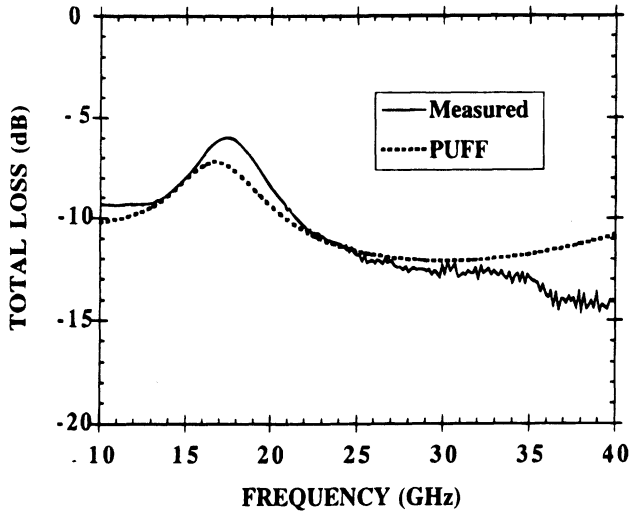


Figure 120.35 Loss comparison between the PUFF model and measured response for a 5-section stepped impedance lowpass filter.

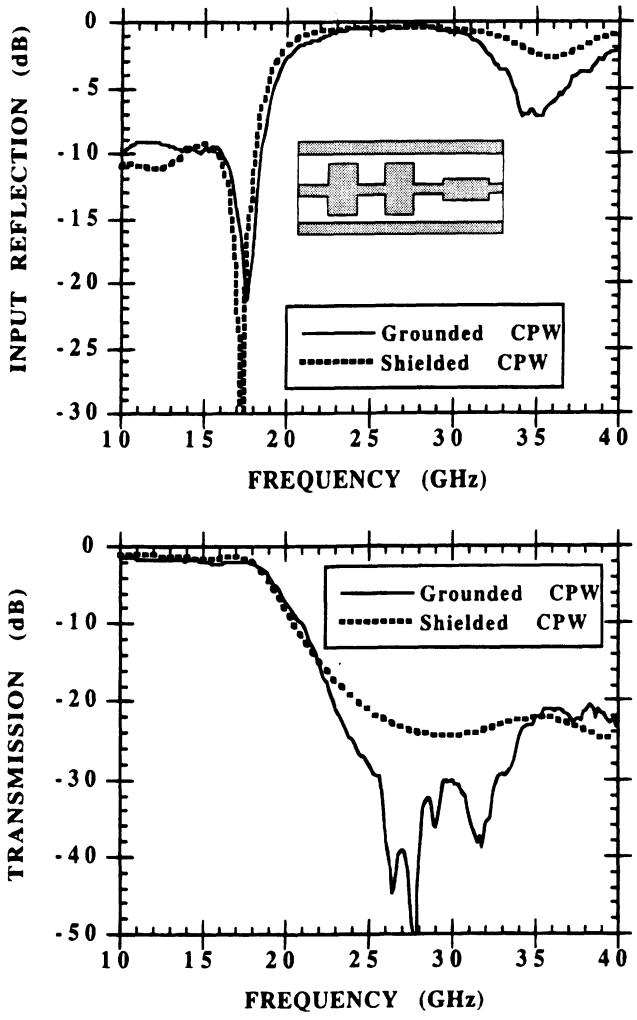


Figure 120.36 Comparison between a conventional CPW and micromachined shielded circuit having a lowpass filter (described above) connected through a half-wave length 50 ohm line to a series inductive line. The 50 ohm line has center conductor (s) and slot widths (w) of 180 and 130 microns, respectively and the inductive section has s and w dimensions of 20 and 210 microns, respectively, with a length of 65 microns.

The problems associated with the parasitic capacitance in planar microstrip inductors and capacitors can be solved by integrating them on a small dielectric membrane. The thin dielectric membrane is defined underneath the lumped element and does not affect the propagation properties of the microstrip line. The membrane is mechanically stable and is compatible with MMIC fabrication techniques as discussed in Fabrication Methodology. The planar inductors and capacitors are suspended in free-space and the quasi-static parasitic capacitance to ground is reduced by a factor of ϵ_r (ϵ_r = 11.7 for high resistivity silicon). Also, for the planar inductor, the quasi-static parasitic capacitance between the lines is reduced by a factor of $(1 + \epsilon_r)/2$ since half the electric fields are in air and half the fields are in the dielectric (Gupta et al., 1981). This reduction in the parasitic capacitance increases the resonant frequency of the inductor without changing the inductance value and the associated series resistance. The application areas of the micro-machined planar inductors and capacitors are in compact phase-shifters, filters, wide band matching networks, and bias circuits for amplifiers, doublers and mixers at millimeter-wave frequencies.

Microwave Measurements: Inductors

Two planar microstrip inductors were fabricated on a 355 μm-thick high-resistivity silicon substrate. Identical inductors using the same masks were also fabricated on a 1.2 μm-thick dielectric membrane using the micro-machining technique outlined previously. The membrane edge is aligned with the physical edge of the inductor as shown in Figure 120.37. The microstrip line is 1 μm-thick electroplated gold and the air-bridge dimensions are 250 μm × 40 μm and it is supported by 2 μm high posts made of electroplated gold. A photo of two completed inductors and their equivalent model are shown in Figure 120.38 and Figure 120.39. The microstrip inductor dimensions are outlined in Table 120.4 and are designed to yield an inductance value of 1.09 nH and 1.69 nH by using the following equation from (Gupta et al., 1981):

$$L_S(nH) = 0.01\, AN^2\pi[\ln(8A/C) + (1/24)(C/A)^2\ln(8A/C + 3.583) - 1/2] \quad (120.1)$$

where $A = (DO + DI)/4$, $C = (DO - DI)/2$ (see Figure 110.37), A and C are given in "mils" (1 mil = 25.4 μm) and N is the number of turns.

The TRL calibration routine is used to measure the loss of the 50 Ω microstrip line on a high resistivity silicon substrate (2000 Ω-cm) which is attached to the lumped inductor. The microstrip line is 1 μm long on each side of the inductor and exhibits a loss of 0.2 dB/mm from 3 GHz to 20 GHz. This implies that the loss of the microstrip line is dominated by dielectric loss in the substrate. The microstrip line loss is modeled as a matched attenuator (R_1, R_2, R_3). The reference plane for the inductor measurements is defined at the outer limit of the inductor geometries or simultaneously at the edge of the membrane (Figure 120.37).

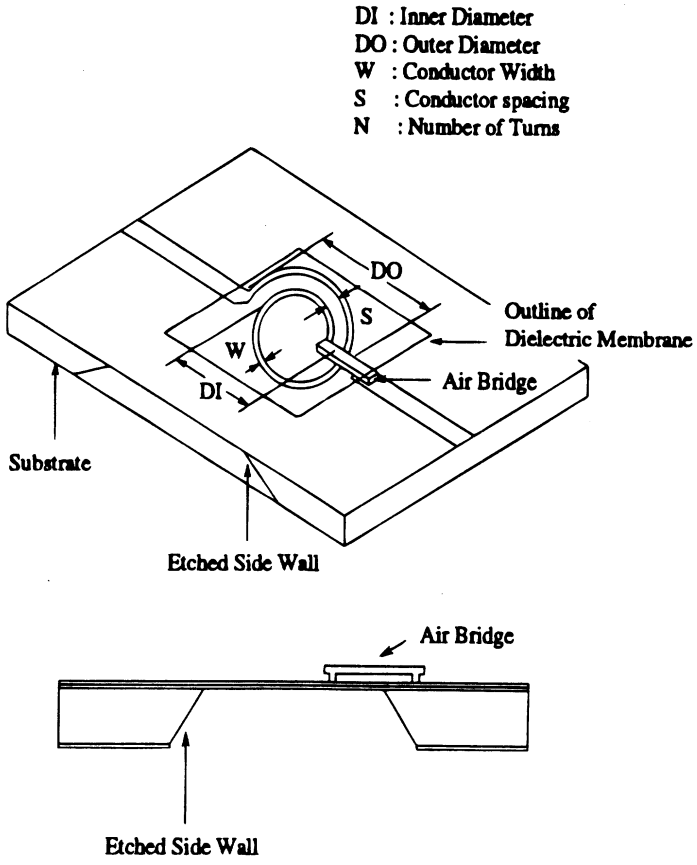


Figure 120.37 Layout of the planar inductor and the membrane outline. The membrane is defined only underneath the lumped element inductor (or capacitor).

First, inductors L_{1S} and L_{2S}, which were built on a high resistivity silicon substrate, are measured from 3 GHz to 20 GHz. Then, the EE$_{so}$f-Touchstone optimization routine is used to fit the equivalent circuit model to the measured *S*-parameters of these two silicon inductors. The measured and modeled S-parameters of these two inductors are plotted on a Smith chart in Figure 120.40. The equivalent values of L_s, R_s, C_p, C_s for inductors L_{1S} and L_{2S} are summarized in Table 120.5. It is seen that the equivalent inductance agrees quite well with Equation 120.1 and the resonant frequencies are 22 GHz and 17 GHz for a 1.2 nH and a 1.7 nH planar microstrip inductor, respectively.

To predict the behavior of the membrane inductors, the same equivalent circuits used in the silicon inductors are borrowed here. However, a slight modification of the equivalent circuits is required before they can be applied to the membrane inductors. In the equivalent circuit, C_p represents the parasitic capacitance between the spiral inductor and the bottom ground plane. From the quasi-static point of view, the capacitance value of C_p depends on the dielectric constant of the substrate. After the silicon substrate has been etched away, the dielectric material between the spiral inductor and ground plane becomes air only, which means the value of C_p should be reduced by a factor of ϵ_r (ϵ_r = 11.7). In the above equivalent circuit, C_s accounts for the mutual coupling between the inner turns of the spiral inductor. Furthermore, since half of electric field is in the air and the other half is confined in the substrate, the value of C_s need to be reduced by a factor of approximately $(1 + \epsilon_r)/2$ in the membrane inductor cases. The inductance L_s and the resistance R_s are not changed since the membrane and silicon inductors have identical geometries and they are independent of the substrate. The new equivalent circuits for membrane inductors appear and their values are shown in Table 120.5. Good agreement has been achieved between the measured S-parameters for membrane inductors L_{1M}, L_{2M} and the new equivalent circuits derived from L_{1S} and L_{2S} following the procedure discussed above. Both the measured and modeled S-parameters for the membrane inductors are plotted on a Smith chart in Figure 120.41.

The measured and modeled 3 GHz to 20 GHz reactance (X) of the inductors on a thick silicon substrate (L_{1S}, L_{2S}) and the inductors on a thin dielectric membrane (L_{1M}, L_{2M}) is shown in Figure 120.42. It is seen that the measured reactance (X) of the membrane inductors (L_{1M}, L_{2M}) agrees well with the simple equivalent model (3 GHz to 20 GHz). The resonant frequency of the membrane inductors is pushed to around 70 GHz and 50 GHz for a 1.2 *nH* and a 1.7 *nH* inductor, respectively. The parasitic capacitances are very low for the micro-machined inductors (C_p, C_s = 2–4 fF) and the membrane inductors can be used as "true" inductors up to 40–60 GHz. The model takes into account only the quasi-static capacitance of the lumped inductor and neglects the transmission-line effects of the pyramidal cavity underneath the lumped inductor and the radiation loss from the air. At mm-wave frequencies, the membrane inductors may result in lower resonant frequencies as predicted above due to non quasi-static effects (high-order modes).

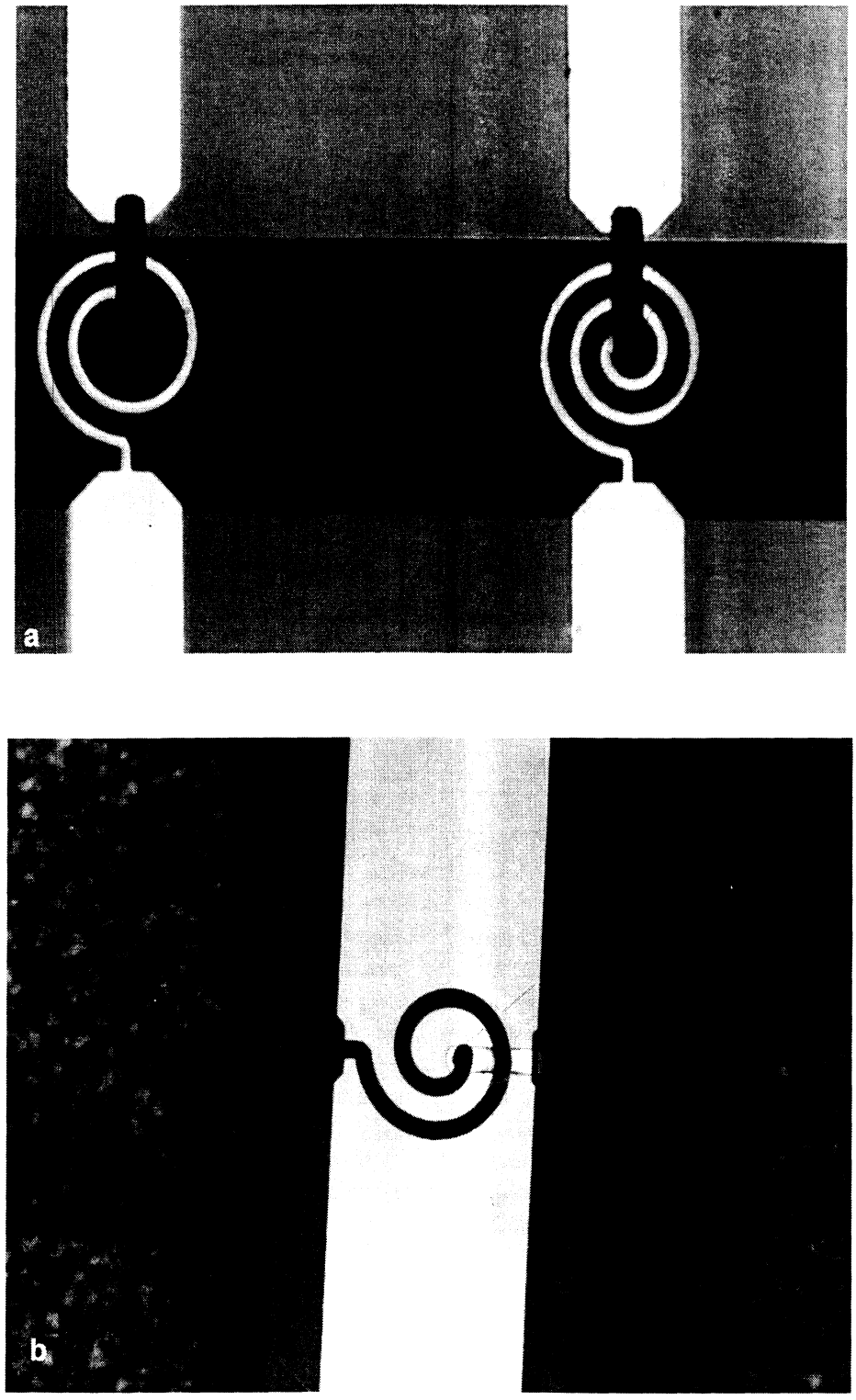


Figure 120.38 (a) A photo of the micromachined inductors L1M(*top left*) and L2M(*top right*) on a small dielectric membrane. (b) A picture of L1M. This picture was taken from the backside of the wafer.

The micromachined inductors behave exactly the same way as the standard planar microstrip inductors at microwave frequencies. Therefore, it is expected that the micro-machined inductor will exhibit a similar Q at microwave frequencies. A small LC series filter composed of a membrane inductor of value 0.9 nH (with a series resistance, R_s = 1.2 or 1.3 Ω) and a chip capacitor of value 1.2 pF was fabricated. The chip capacitor is a surface mount MIS type capacitor (Metelics MBIC-1002) and has a very high Q up to 12 GHz, and its effect on the measured Q is neglected at 4.3 GHz. The measured S_{11} of the series LC combination demonstrates a quality factor of Q = 20 at 4.3 GHz for the membrane inductor and is close to the expected value from the equation $Q = \omega_0 L/R_s$ (Figure 120.43). The measurements include the effect of the bond wires used to connect the silicon substrate to the coaxial connectors ($L_{bw} \sim 0.1$ nH). The associated Q of membrane inductors is expected to increase as

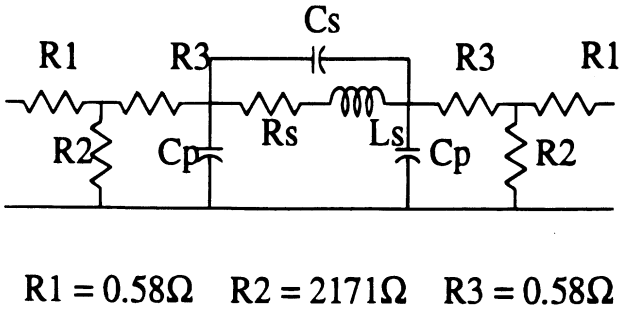


Figure 120.39 The equivalent circuit model of the spiral inductors. A 0.2 dB attenuator is placed at each end to model the loss in the 50 Ω microstrip line on the high resistivity silicon dielectric substrate.

Table 120.4 Physical Dimensions and the Corresponding Calculated Inductance Values for the Spiral Inductors. All Units are in μm (see Figure 120.37).

Components	*DI*	*DO*	*W*	*S*	*N*	$L_s(nH)$
L_{1S},L_{1M}	254	406.4	25.4	50.8	1.5	1.09
L_{2S},L_{1M}	101.6	406.4	25.4	50.8	2.5	1.69

Table 120.5 Modeled Values of R_s, L_s, C_s, C_p for Spiral Inductors and Membrane Substrate (see Figure 120.41).

Components	$R_s(\Omega)$	$L_s(nH)$	$C_s(fF)$	$C_p(fF)$
L_{1S}	3	1.2	10	33
L_{1M}	3	1.2	2	2.5
L_{2S}	5	1.7	6	45
L_{2M}	5	1.7	1.2	4

$\sqrt{f}$ with frequency (because the series resistance increases as $\sqrt{f}$(Gupta et al., 1981), (Daly et al., 1967) to yield a Q of 50–60 at 30–40 GHz.

Microwave Measurements: Capacitors

A similar fabrication technique was applied to planar interdigitated capacitors. In this case, the planar capacitors do not suffer from a low resonant frequency but from a relatively large shunt parasitic capacitance to ground (C_p). During modeling the parasitic capacitance to ground is generally included with the interdigitated series capacitance (C_s). However, it is advantageous to eliminate this parasitic capacitance to result in better millimeter-wave filters, phase shifters and matching networks. The micromachined membrane approach reduces the parasitic capacitance by a factor of ϵ_r. However, in this case, it also reduces the interdigitated series capacitance by a factor of $(1 + \epsilon_r)/2$.

Eight finger and four finger interdigitated capacitors were fabricated on a high resistivity silicon substrate and on a membrane. A photo of these two membrane capacitors is shown in Figure 120.44. The capacitor finger is 355 μm long and is 25 μm wide. The gap between the fingers is also 25 μm wide. The measured S_{11} from 7 to 20 GHz for the capacitors are shown in Figure 120.45. It is seen that the membrane interdigitated capacitor (of value around 110 *fF* for the eight finger capacitor and 55 fF for the four finger capacitor) follows the 1-R line on the Smith chart as expected from a capacitor in series with a 50 Ω load. The interdigitated capacitor on the silicon dielectric shows a large shunt capacitance effect due to the parasitic capacitance to ground. The measured S_{11} of the capacitors on the silicon substrate agree very well with published results

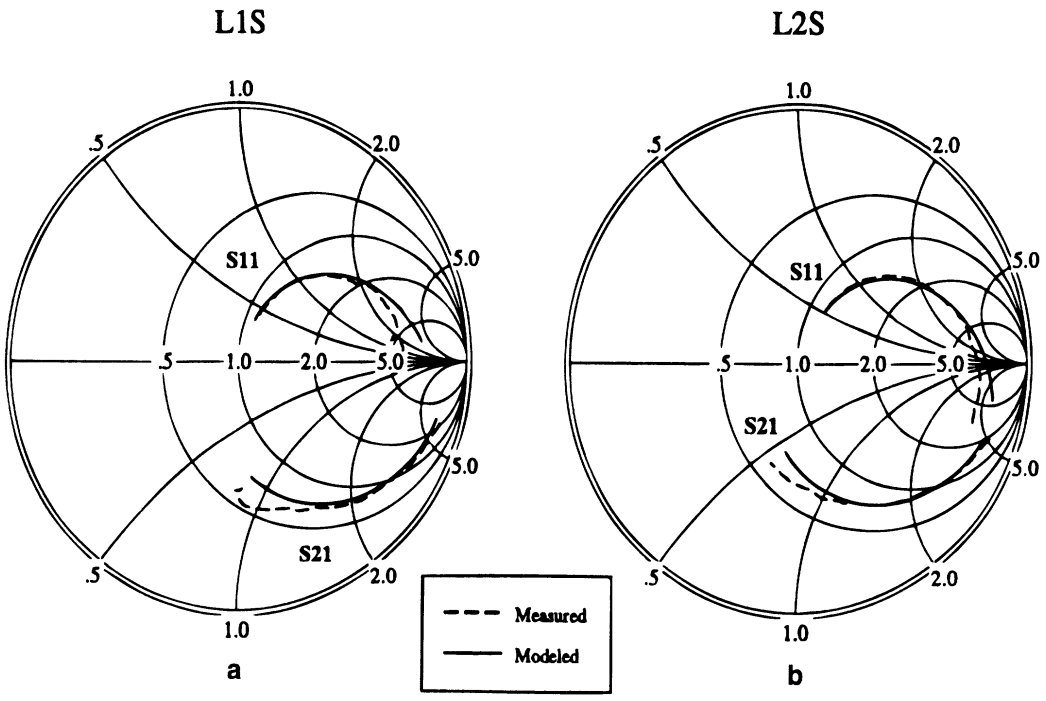


Figure 120.40 Measured and modeled S-parameters of silicon inductors (a) L_{1S} and (b) L_{2S}. Frequency sweep from 3 GHz to 20 GHz.

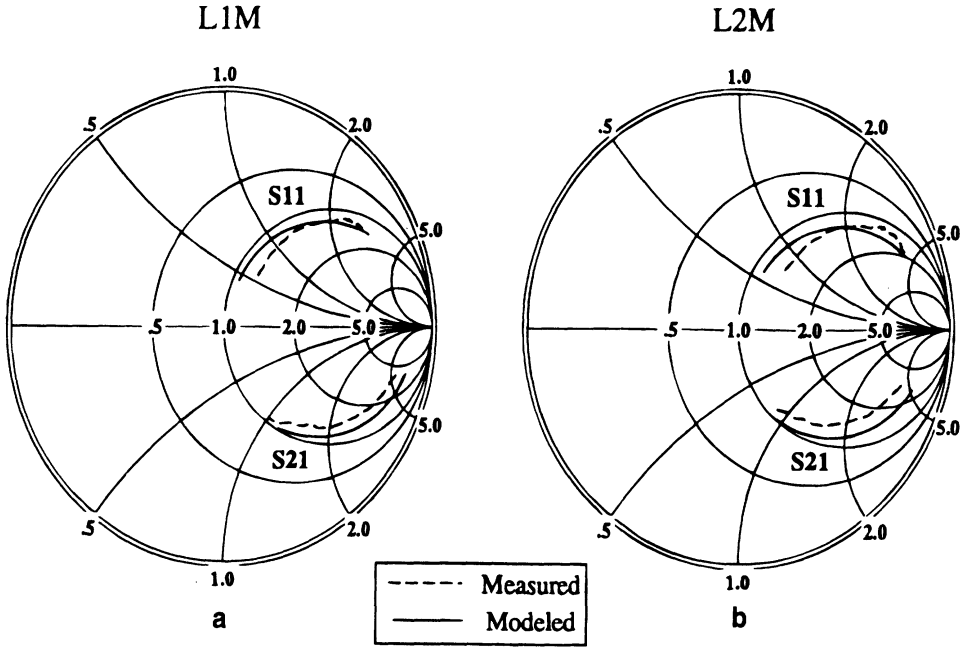


Figure 120.41 Measured and modeled S-parameters of membrane inductors (a) L_{1M} and (b) L_{2M}. Frequency sweeps from 3-GHz to 20 GHz.

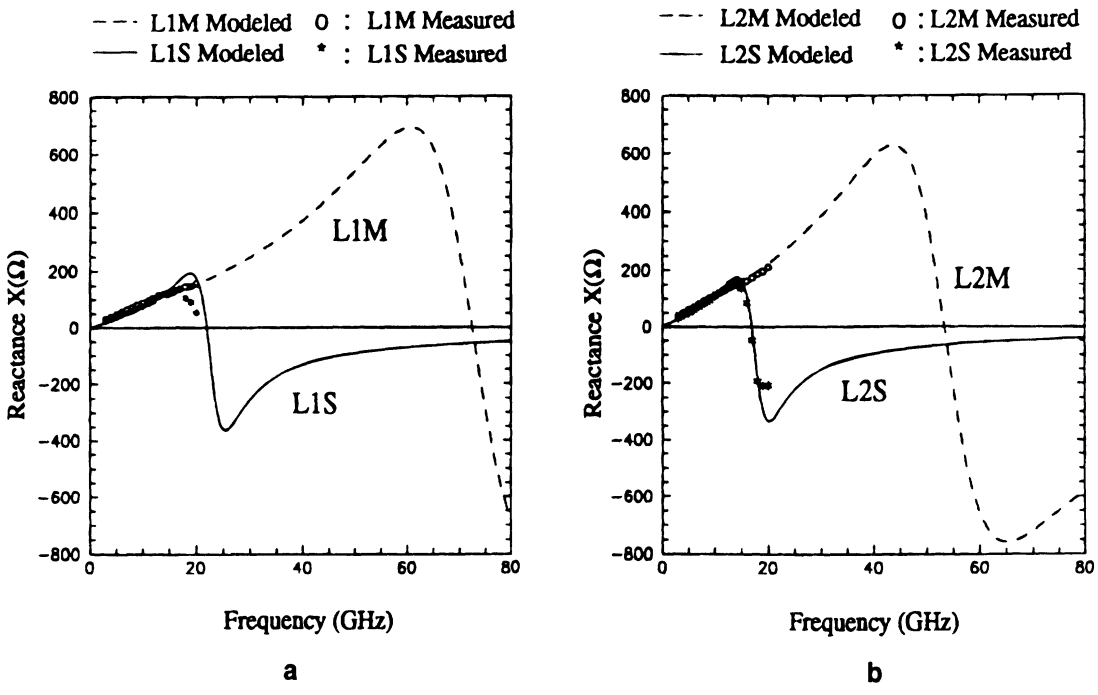


Figure 120.42 Measured and modeled reactance (X) of inductors (a) L_1 and (b) L_2. Frequency sweeps from 3 GHz to 20 GHz.

of similar capacitors on GaAs substrates (Esfandiari, 1983). Compared with dielectric supported capacitors, it is seen that the micro-machined membrane capacitors demonstrate much better performance at microwave frequencies. The quality factor of the membrane capacitors was not measured at microwave frequencies but is expected to be larger than the corresponding capacitors on the silicon substrate due to the absence of the dielectric losses.

120.7 Conclusions

The previous sections have outlined the progress to date on implementing distributed microwave circuit elements such as filters and tuning stubs in membrane supported transmission line geometries. At low frequencies, these membrane supported elements exhibit improved performance over their substrate based counterparts due to the elimination of parasitics and losses

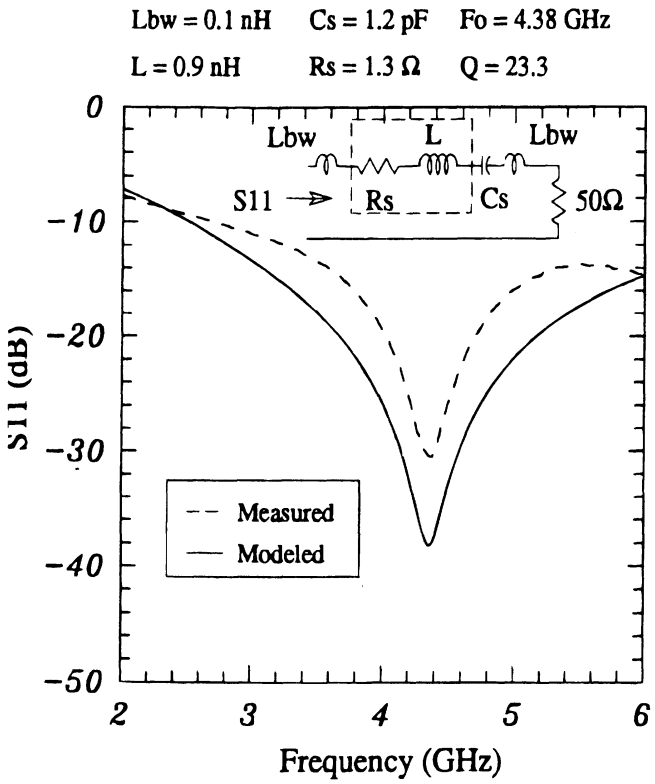


Figure 120.43 Measured and modeled S_{11} of a small LC filter. This filter shows that the 0.9~nH membrane inductor has a quality factor of 23.3 at 4.38 GHz.

associated with the dielectric material. At higher frequencies, problems associated with the substrates make conventional approaches unfeasible, and membrane supported components offer the only planar alternative to costly waveguide-based approaches. Membrane supported transmission lines and circuit components have been shown to perform very well in frequency bands all the way up to W-band (110 GHz). Circuits commonly used in CPW implementations are shown to have superior performance when realized with membrane supported transmission lines like microshield line. Low pass filters and resonant stubs have been measured up to 40 GHz with excellent results, and microshield line low pass filters have been tested as high as 110 GHz. Micromachining has also opened the doors to techniques for fabricating circuits that were previously restricted by cumbersome machining processes. Interdigitated filters were thought to be limited to very low frequencies where they could be manufactured using mechanical techniques, but membrane technology has allowed them to become high performance alternatives at 30 GHz. Planar millimeter-wave microstrip inductors and capacitors have been developed and fabricated on a high-resistivity silicon substrate using micromachining techniques. This micro-machining technique is compatible with via-hole technology in GaAs and InP MMIC processes. The micro-machined spiral inductors and interdigitated capacitors are suspended on a thin dielectric membrane to reduce the parasitic capacitance to ground. Since the parasitic capacitance to the ground can be reduced by a factor of ϵ_r, it renders a much higher resonance frequency in this

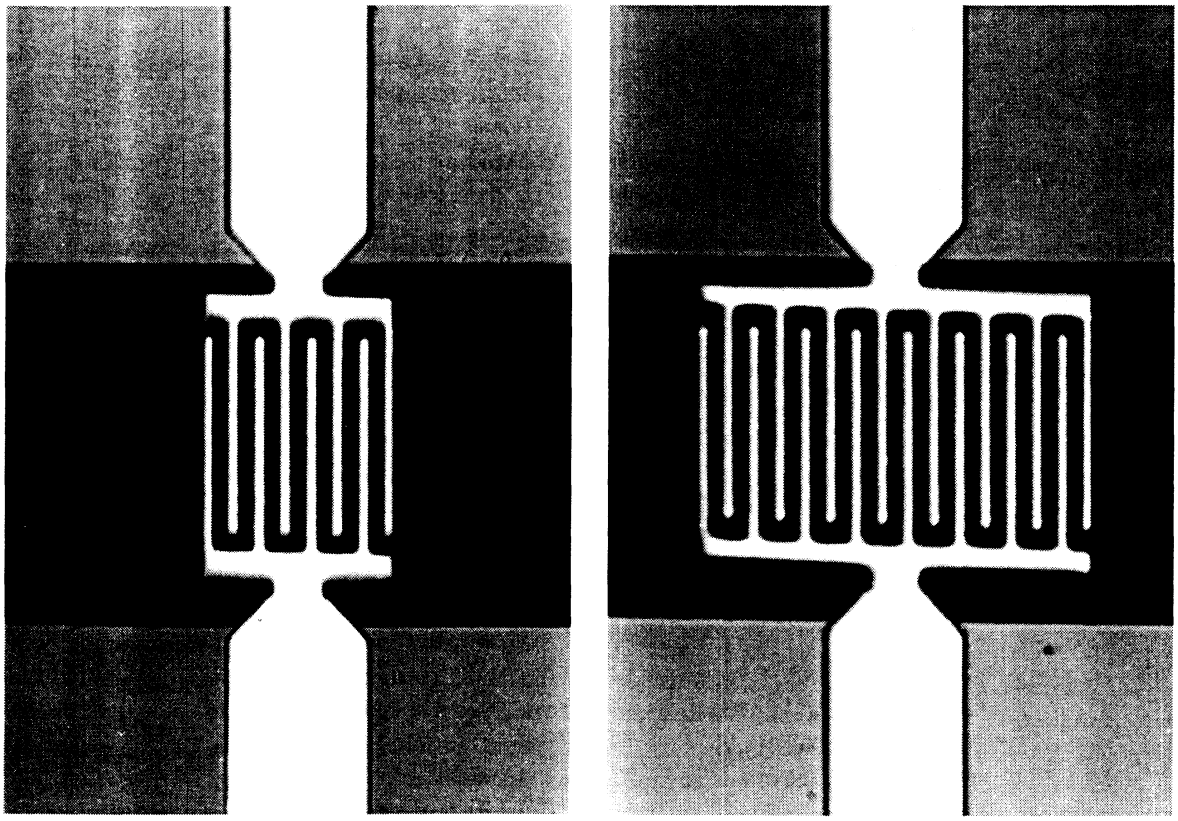


Figure 120.44 A photo of the interdigitated membrane capacitors.

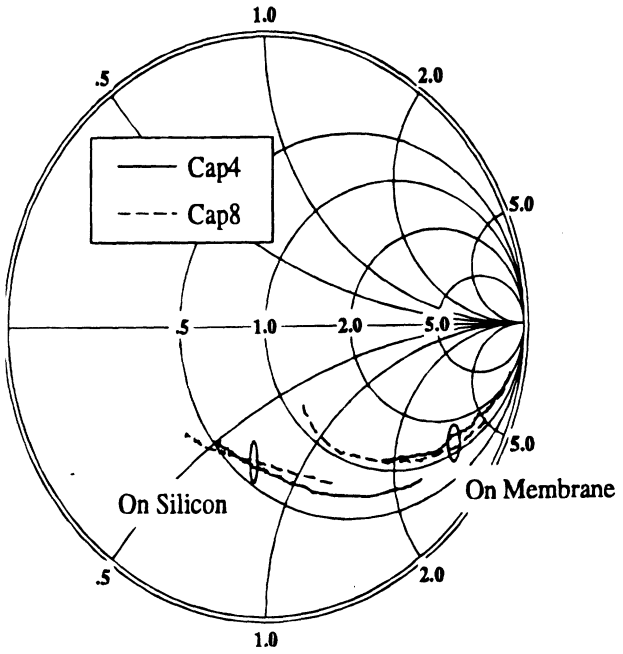


Figure 120.45 Measured S_{11} of eight-finger and four-finger interdigitated capacitors on both membrane and silicon substrate. Frequency starts at 7 GHz and stops at 20 GHz.

membrane structure compared to their Silicon/GaAs counterparts and makes this technology very attractive at millimeter-wave frequencies. This technique can also be applied to lumped elements in coplanar-waveguide transmission lines and micromachined filter design.

References

Abdo-Tuko, M., Naghed, M. and Wolff, I. 1993. Novel 18/36 GHz (M)MIC GaAs FET frequency doublers in CPW-techniques under the consideration of the effects of coplanar discontinuities, *IEEE Trans. Microwave Theory Tech.*, MTT-41(8):1307–1315.

Alley, G. D. 1970. Interdigital capacitors and their application to lumped-element microwave intergrated circuits, *IEEE Trans. Microwave Theory Tech.*, MTT-18:1028–1033.

Altschuler, H. M., and Oliner, A. A. 1960. Discontinuities in the center conductor of symmetric strip transmission line, *IRE Trans. Microwave Theory Tech.*, MTT-8:328–339, May 1960.

Betz V. and Mittra, R. 1992. Comparison and evaluation of boundary conditions for the absorption of guided waves in an FDTD simulation, *IEEE Microwave and Guided Wave Lett.*, 2(12):499–501.

Chang, J. Y., Abidi, A. A. and M. Gaitan, 1993. Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier, *IEEE Electron Device Letter*, 14(5):246–248.

Chi, C. Y. and Rebeiz, G. M. 1994a. Planar microwave and millimeter-wave lumped elements and coupled-line filters using micro-machining techniques, *IEEE Trans. Microwave Theory Tech.*, December.

Chi, C. Y. and Rebeiz, G. M. 1994b. Novel low-loss interdigitated filters for microwave and millimeter-wave applications using micromachining techniques, *24th European Microwave Conference Digest*, 2:1357–1359.

Daly, D. A. et al. 1967. Lumped elements in microwave integrated circuits, *IEEE Trans. Microwave Theory Tech.*, MTT-15:713–721.

Dib, N. I. and Katehi, L. P. B. 1992. Impedance calculation for the microshield line, *IEEE Microwave and Guided Wave Letters*, 2(10):406–408.

Dib, N. I., Harokopus, W. P., Katehi, L. P. B., Ling C. C., and Rebeiz, G. M. 1991. A study of a novel planar transmission line, presented at the *1991 IEEE MTT-S Int. Symp.* June, Boston, MA.

Drayton, R. F. and Katehi, L. P. B. 1992. Microwave characterization of microshield lines, *Digest of the 40th ARFTG Conf.*, December, Orlando, FL.

Drayton, R. F. and Katehi, L. P. B. 1993a. Experimental study of micromachined circuits, *Digest of the 1993 Int. Symp. Space Terahertz Technology*, March, Los Angeles, CA.

Drayton, R. F. and Katehi, L. P. B. 1993b. Micromachined circuits for mm-wave applications, *Digest of the 1993 European Microwave Conf.*, September, Madrid, Spain.

Drayton, R. F., Weller, T. M. and Katehi, L. P. 1995. Development of Miniaturized Circuits for High-Frequency Applications using Micromachining Techniques, *Int. J. Microcircuits and Electronic Packaging*, 3rd Quarter.

Dunleavy, L. P. and Katehi, L. P. B. 1988. Shielding effects in microstrip discontinuities, *IEEE Trans. Microwave Theory and Techniques*, MTT-36(12):1767–1774.

Ekstrom, H. A., Gearhart, S. S., Acharya, P. R., Rebeiz, G. M., Kolberg E. L., and Jacobson, S. 1992. 348 GHz endfire slotline antennas on thin dielectric membranes, *IEEE Microwave and Guided Wave Lett.*, 2(9):357–358.

El-Shandwily M. and Dib, N. 1990. Spectral domain analysis of finlines with composite ferrite-dielectric substrate, *Int. J. Electronics*, 68(4):571–583.

Engen, G. and Hoer, C. 1979. Thru-reflect-line: an improved technique for calibrating the six-port automatic network analyzer, *IEEE Trans. Microwave Theory Techn.*, 27(12):987–993.

Esfandiari, R. et al. 1983. Design of interdigitated capacitors and their application to gallium arsenide monolithic filters, *IEEE Trans. Microwave Theory Tech.*, MTT-31(1):57–64.

Findler, G., Muchrow, J., Koch, M., and Munzel, H. 1992. Temporal evolution of silicon surface roughness during anisotropic etching processes, *Micro Electro Mechanical Systems 1992*, February, 62–66.

Finne, R. M. and Klein, D. L. 1967. A water-amine-complexing agent system for etching silicon, *J. Electrochem. Soc.*, 965–970.

Garcia, E., Jacobson, B. R., and Hu, Q. 1993. Fabrication of high-quality superconductor-insulator-superconductor junctions on thin SiN membranes, *Applied Physics Lett.*, 63(7): August.

Gearhart, S. S. 1994. *Integrated Milimeter-Wave and Submillimeter-Wave Antennas and Schottky-Diode Receivers*, Ph.D. Thesis, The University of Michigan.

Gupta, K. C., Garg R., and Chadha, R. 1981. *Computer-Aided Design of Microwave Circuits.*, Artech House, Norwood, MA.

Hamadallah, M. 1988. Microstrip Power Dividers at Mm-Wave Frequencies, *Microwave Journal,* July, pp.116–127.

Harokopus, E. P., and Katehi, L. P. B. 1989. Characterization of microstrip discontinuities on multi-layer dielectric substrates including radiation losses, *IEEE Trans. Microwave Theory and Techniques,* MTT-37(11):2058–2066.

Heinrich, W. 1990. Full-wave analysis of conductor losses on MMIC transmission lines, *IEEE Trans. Microwave Theory Tech.,* 38(10):1468–1472.

Kramer, H. G. 1983. Float-zoning of semiconductor silicon: A perspective, *Solid State Technol.,* 137, January.

Kunz K. and Luebbers, R. 1993. *The Finite Difference Time Domain Method for Electromagnetics,* CRC Press, Boca Raton, FL.

Lange, J. 1969. Interdigitated stripline quadrature hybrid, *IEEE Trans. Microwave Theory Tech.,* MTT-17:1150–1151, December 1969.

Laudise, R. A. 1970. *The Growth of Single Crystals,* Prentice-Hall, Englewood Cliffs, NJ.

Lepselter, M. P. 1966. Beam-lead technology, Bell System Technical Journal, February, 233–254.

Ling, C. C.-S. 1993. *An Integrated 94-GHz Monopulse Tracking Receiver,* Ph.D. Thesis, Radiation Laboratory, University of Michigan.

Maissel, L. I. and Glang, R. 1970. *Handbook of Thin Film Technology,* ch. 6, 29–30, McGraw Hill, New York, NY.

Marks, R. B., Williams, D. F. 1993. NIST De-embedding Software, Program DEEMBED, Revision 4.04.

Maury, M., March, S., and Simpson, G. 1987. LRL calibration of vector automatic network analyzers, *Microwave Journal,* May, 387–391.

Mei K. and Fang, J. 1992. Superabsorbtion-A method to improve absorbing boundary conditions, *IEEE Trans. Antennas and Propagation,* 40(9):1001–1010.

Mur, G. 1981. Absorbing boundary conditions for the finite-difference approximation of the time-domain electromagnetic-field equations, *IEEE Trans. Electromagnagetic Compatibility,* 22(11):377–382.

Pengelly, R. S. and Schumacher, P. 1988. High-performance 20 GHz package for GaAs MIMICs, *Microwave Systems News and Circuit Techniques,* January, 10–19.

Petersen, K. E. 1982. Silicon as a mechanical material, *Proc. IEEE,* 70(5).

Pucel, R. A. 1981. Design considerations for monolithic microwave circuits, *IEEE Trans. Microwave Theory Tech.,* MTT-29(6):513–534.

Rebeiz, G. M., Kasilingam, D. P., Stimson, P. A., Guo, Y., and Rutledge, D. B. 1990. Monolithic millemeter-wave two-dimensional horn imaging arrays, *IEEE Trans. Antennas and Propagation,* AP-28, 1473–1482.

Robertson, S. V., Katehi, L. P. B., and Rebeiz, G. M. 1994. W-Band Microshield Low-Pass Filters, in *1994 IEEE MTT-S Digest,* pp. 625–628.

Robertson, S. V., Katehi, L. P. B., and Rebeiz, G. M. 1995. Micromachined self-packaged W-band band-pass filters, *1995 IEEE MTT-S Digest,* pp. 1543–1546.

Rutledge, D. B., Neikirk D. P., and Kasilingam, D. P. Integrated circuit antennas, *Infrared and Millimeter-Waves,* K. J. Button, ed., 10:1–90, Academic Press, New York.

Rutledge, G. M. 19??. Millimeter-wave and submillimeter-wave antenna structures, *US Patent* 4888, 597.

Sheen, D., Ali, S., Abouzahra, M., and Kong, J. 1990. Finite-difference time-domain method to the analysis of planar microstrip circuits, *IEEE Trans. Microwave Theory Tech.,* 38, 849–857.

Strid, E. W., and Gleason, K. R. 1984. Calibration methods for microwave wafer testing, *1984 IEEE MTT-S Int. Microwave Symp. Digest,* 93–97.

van Deventer, T. E. 1992. *Characterization of Two-Dimensional High Frequency Microstrip and Dielectric Interconnects,* Ph.D dissertation, The University of Michigan. December.

van Deventer, T. E., Katehi, L. P. B., and Cangellaris, A. 1989. An integral equation method for the evaluation of conductor and dielectric losses in high-frequency interconnects, *IEEE Trans. Microwave Theory and Techniques,* MTT-37(11):1964–1972.

VandenBerg, N. L. and Katehi, L. P. B. 1982. Broadband vertical interconnects using slot-coupled shielded microstrip lines, *IEEE Trans. Microwave Theory and Techniques,* MTT-40(1):81–88.

Wedge, S., Compton, R., and Rutledge, D. 1991. *PUFF Computer Aided Design for Microwave Integrated Circuits,* Version 2.0.

Weller, T. M., Katehi, L. P. B., Rebeiz, G. M., Cheng, H. J., and Whitaker, J. F. 1993b. Fabrication and characterization of microshield circuits, *1993 Int. Symp. Space Terahertz Technology,* March, Los Angeles, CA.

Weller, T. M., Rebeiz, G. M., and Katehi, L. P. 1993a. Experimental results on microshield transmission line circuits, *1993 IEEE MTT-S Digest,* pp. 827–830.

Weller, T., Katehi, L., Herman, M., and Wamhof P. 1994. Membrane technology applied to microstrip: A 33 GHz wilkinson power divider, *1994 IEEE MTT-S Int. Microwave Symp. Digest,* 2:911–914.

Weller, T. M., Katehi, L. P. B., and Rebeiz, G. M. 1995a. High performance microshield line components, *IEEE Trans. Microwave Theory Tech.,* 43(3):534–543.

Wolf, S. and Tauber, R. N. 1986. *Silicon Processing for the VLSI Era, Volume 1: Process Technology,* Lattice Press, Sunset Beach, CA.

Zhang X. and Mei, K. 1988. Time-domain finite difference approach to the calculation of the frequency-dependent characteristics of microstrip discontinuities, *IEEE Trans. Microwave Theory Tech.,* 36(12):1775–1781.

To be published in IEEE Transactions on Antennas and Propagation

Micromachined Patch Antennas

Ioannis Papapolymerou[†], Student Member, *IEEE*
Rhonda Franklin Drayton*, Member, *IEEE*,
Linda P. B. Katehi[†], Fellow, *IEEE*

[†]The Radiation Laboratory
EECS Department
The University of Michigan
Ann Arbor, MI 48109-2122 USA

*University of Illinois at Chicago
EECS Department
Chicago, Illinois 60607
USA

ABSTRACT

This paper presents the use of selective lateral etching based on micromachining techniques to enhance the performance of rectangular microstrip patch antennas printed on high index wafers, such as Silicon, GaAs and InP. Micromachined patch antennas on Si substrates have shown superior performance over conventional designs where the bandwidth and the efficiency have increased by as much as 64% and 28%, respectively. In this work, the silicon material is removed laterally underneath the patch antenna to produce a cavity that consists of a mixture of air and substrate with equal or unequal thicknesses. Characterization of the micromachined patch antenna is presented herein and includes a discussion on the bandwidth improvements, radiation patterns and efficiency of the patch. In addition, antenna placement on the reduced index cavity with respect to the high index substrate is described to achieve efficiency improvements over conventional patch antennas.

I. INTRODUCTION

Microstrip antennas are used in a broad range of applications from communication systems (radars, telemetry and navigation) to biomedical systems, primarily due to their simplicity, conformability, low manufacturing cost [1] and enormous availability of design and analysis software. As system requirements for faster data transmission in lighter compact designs drive the technology area, higher frequency design solutions with large density layouts require integration of microwave devices, circuitry and radiating elements that offer light weight, small size, and optimum performance. Compact circuit designs are typically achieved in high index materials, which is in direct contrast to the low index substrates imposed by antenna performance requirements. The ideal solution requires the capability to integrate the planar antenna on electrically thick low index regions while the circuitry remains on the high index regions in the same substrate. In the past, this requirement was satisfied by selecting the substrate that offers optimum component performance; unfortunately this led to hybrid integration schemes and high development cost. As the frequency increases, however, this approach becomes increasingly difficult and costs are prohibitively high. Microstrip patch antennas printed on high index substrates are revisited in this work with the primary objective to develop design solutions that can be integrated into monolithic circuit layouts while enhancing antenna performance.

Microstrip antenna designs show significantly degraded performance due to the pronounced excitation of surface waves in high index materials. As a result, the antenna has lower efficiency, reduced bandwidth, degraded radiation patterns and undesired coupling between the various elements in array configurations. Optimum antenna performance depends on the choice of dielectric material as well as the choice of feeding network and is achieved when the radiated power occurs primarily as space waves with little or no components of "undesired" surface waves. Such microstrip designs are typically fabricated on electrically thick, low index materials and characterized by maximum antenna bandwidth and efficiency as reported by a vast number of theoretical and experimental researchers.

Only a few experimental approaches have been put forth to resolve the excitation of substrate modes in microstrip antennas. In 1984, a substrate-superstrate configuration [2] using a horizontal antenna element showed an increase in the radiation efficiency. Superstrate materials such as GaAs or Si, however, require a very thin substrate thickness that yields exceedingly small values of radiation resistance. In the past three years, researchers have begun to use physical substrate alterations as a means of perturbing the surface wave excitation. Circular patch designs in duroid [3] are based on the choice of an appropriate patch radius to suppress the excited surface waves. Given the patch radius for a desired operation frequency, the antenna is forced to resonate at the first higher order mode (TM_{120}) rather than the dominant (TM_{110}) one. Other approaches rely on suspending the rectangular patch over an air cavity through the use of a membrane or over closely spaced periodic holes in the substrate (either drilled or micromachined) [4, 5]. In both cases the radiation efficiency is increased and antenna patterns are improved considerably as a result of the elimination of surface wave propagation. Herein, an approach different from the ones described above is followed which does not require the use of holes or dielectric membranes [6-8]. In this study, material is removed underneath the antenna by using selective etching techniques and the excitation of surface waves is suppressed by creating a micromachined cavity as shown in Figure 1, that produces a low permittivity environment for the patch antenna.

The micromachined planar antenna design can be integrated on the same wafer with Si and GaAs ICs without affecting circuit requirements. In order to demonstrate the capability of a micromachined antenna to be integrated effectively with circuits, an example of a microstrip patch fed by a microstrip line is studied. More specifically, the antenna is printed on a cavity region that is comprised of two dielectric sections: (a) air and (b) silicon substrate. Using micromachining techniques, silicon is laterally removed from the cavity region producing a silicon area that has thickness less than or equal to 50% of the original substrate thickness and an air region that is created by the removal of material. Described herein is the characterization of a silicon micromachined patch antenna. In order to characterize the patch, a cavity model is used to estimate the reduced effective dielectric constant while bandwidth and radiation patterns are measured to eval-

uate the antenna's performance. Lastly, evaluation of the antenna's efficiency using available test equipment is achieved by fabricating and measuring a duroid-based scaled model.

II. Micromachined Patch Antenna

To integrate patch antennas into circuit designs on high index substrates without losing the advantages of low index materials, the regions in the substrate which will house the radiating elements must have low index of refraction. This is achieved by using micromachining to eliminate a portion of the substrate material (see Figure 1). The micromachined antenna configuration consists of a rectangular patch centered over the cavity, sized according to the effective index of the cavity region and fed by a microstrip line. To produce the mixed substrate region, silicon micromachining is used to laterally remove the material from underneath the specified cavity region resulting in two separate dielectric regions of air and silicon. In this work, the amount of silicon removed varies from 50-80% of the original substrate thickness underneath the patch and a cavity model is described in the next section to provide an estimate of the reduced index value. The walls of the hollowed cavity are in general slanted due to the anisotropic nature of the chemical etching. In Section B, the scattering parameter measurements illustrate the antenna's bandwidth while field patterns indicate the radiated power.

A. Calculation of Reduced Dielectric Constant

A cavity model is used to predict the effective dielectric constant of the mixed air-silicon region for varying thickness ratios underneath the patch antenna. A quasi-static model, based on series capacitors, is used to determine the patch capacitance in the mixed region (Figure 2a):

$$C = \frac{\varepsilon_{eff} A}{t}, \tag{1}$$

where $\varepsilon_{eff} = \varepsilon_{reff}\varepsilon_o$. For simplicity the walls of the cavity are asumed to be vertical and the effective dielectric constant (ε_{reff}) is estimated by the following expression:

$$\varepsilon_{reff} = \varepsilon_{cavity}\left(\frac{L + 2\Delta L\frac{\varepsilon_{fringe}}{\varepsilon_{cavity}}}{L + 2\Delta L}\right), \tag{2}$$

$$\text{where } \frac{\varepsilon_{fringe}}{\varepsilon_{cavity}} = \frac{\varepsilon_{air} + (\varepsilon_{sub} - \varepsilon_{air})x_{air}}{\varepsilon_{air} + (\varepsilon_{sub} - \varepsilon_{air})x_{fringe}} \quad \varepsilon_{cavity} = \frac{\varepsilon_{air}\varepsilon_{sub}}{\varepsilon_{air} + (\varepsilon_{sub} - \varepsilon_{air})x_{air}}. \tag{3}$$

In the above expressions, ε_{cavity} represents the relative dielectric constant of the mixed substrate region and ε_{fringe} represents the relative dielectric constant in the fringing fields region. Equation (2) includes the open-end effect extension length ΔL to the antenna which can be found from [9], where ε_{fringe} is the permittivity used for the calculation of ΔL. The thickness parameters, x_{air} and x_{fringe}, are ratios of the air to full substrate thickness in the mixed and fringing field regions, respectively. For the silicon micromachined case shown in Figure 2a.1 x_{fringe} is taken as zero, whereas for the case of Figure 2a.2 $x_{fringe}=x_{air}$.

A plot of the theoretical and measured effective dielectric constant versus the air gap thickness for silicon substrate (ε_r=11.7) can be found in Figure 2b, where an effective dielectric constant of approximately 2.2 is achieved for a mixed air-silicon ratio of 1:1 using the capacitor model (eq. (2) with ΔL=0) and 3:1 ratio for the capacitor model with ΔL extension length (eq. (2) with ΔL calculated from [9]). The dimensions for the micromachined patch that was used to produce the results of Figure 2b can be found in Table 1 (parameters a,b and c are actual values since the walls are assumed vertical). Included also in Figure 2b is a data point based on the finite difference time domain model of the micromachined patch geometry. The FDTD calculation was based on a 3-D full-wave scheme that yields the return loss of the micromachined antenna and the effective permittivity of an 1:1 air-silicon substrate for a range of frequencies. Once the resonant frequency is

determined from the return loss, the effective permittivity of interest is found. Only one case of air-silicon substrate ratio has been simulated with FDTD in order to validate the quasi-static results for the effective dielectric constrant of the antenna that was fabricated and tested. Regarding the measured ("micromachined") data point of Figure 2b, the resonant frequency of the fabricated antenna was measured and [10] was used to extract the dielectric constant of the substrate for a patch having the same dimensions as the measured one. In the following sections, more extensive experimental data will be presented that prove the superiority of this type of micromachined antenna. The conventional and micromachined antennas will be defined as a patch fabricated on a regular substrate or as a patch fabricated on a substrate that has locally reduced index region, respectively.

B. K-Band Micromachined Patch

Two antennas were fabricated on silicon, with resonant frequencies in the K-band and air/substrate thickness ratios of 1:1 (see Table 1 for dimensions). In the silicon micromachined patch (SMP) antenna, the conductor has been electroplated to a metal thickness of approximately 3.2 μm and the substrate is chemically etched (EDP process) in a single etch step underneath the antenna. Since the walls of the resulting cavity are not vertical due to the anisotropic etching, dimensions for a, b and c in Table 1 represent average values.The lower ground plane is achieved by attaching adhesive copper tape of 25.4 μm thickness and the size of the silicon substrate where the antennas were fabricated was approximately 2.8 cm x 3 cm. Return loss measurements are shown in Figure 3 and were obtained using an HP 8510 Network Analyzer where the bandwidth ($|S11| \leq$ -10 dB) increases from 2.9% for the "regular" antenna to 5% for the SMP. Since bandwidth is inversely proportional to the quality factor, Q, defined as the ratio of total energy stored in the antenna to the energy dissipated or radiated from the antenna, the increase in bandwidth provides the first indicator of an increase in total radiation from the antenna. Efficiency measurements, however, need to be made in order to observe the increase in power radiated into space waves as opposed to power radiated into surface waves.

Radiation patterns were also taken for the two antennas and the results are shown in Figure 4, where significant differences in the E-plane pattern are observed while the H-plane patterns remain similar as expected. For measurement purposes, the silicon substrates that hosted the antennas were mounted on a 5.6 cm x 5 cm metallic holder that served as the ground plane. The silicon antenna pattern exhibits many ripples, that are due to the diffraction of strong surface waves from the edges of the finite ground plane, in contrast to the micromachined antenna pattern that is much smoother. Conclusive evidence, needed to show the suppression of surface waves, is obtained by evaluating the antenna gain and measured efficiency. Since test equipment at this frequency was unavailable, a scaled model has been developed for designs printed on high index (10.8) duroid substrate that operate at Ku-band resonant frequencies.

III. Characterization of Micromachined Patch Antennas

The last step in characterizing the micromachined patch performance is the evaluation of the antenna's efficiency. In order to utilize existing test equipment, a scaled model of the antenna is fabricated on a mixed air-substrate cavity and is realized by machining a high index (10.8) duroid substrate. During this phase, a comparison is made between the micromachined patch and conventional designs operating at the same frequency. Similar measurements to those of the micromachined antennas are obtained to determine the bandwidth and radiation pattern of the scaled models in addition to the measured efficiency. In the remaining sections, the theory of radiation-efficiency measurements is described first. Next, the antenna performance is characterized based on bandwidth, radiation patterns, and efficiency. Lastly, design parameters are discussed regarding the size of the micromachined cavity to produce enhanced efficiency over conventional designs.

A. Theory of Radiation Efficiency

To obtain the antenna gain of the patch antenna, radiation efficiency based on a radiometric method is used which compares the noise power of a lossy antenna under test (AUT) to a known load [11-12]. Antenna efficiency is obtained by characterizing the system receiver and then the

composite system (system receiver plus antenna). By measuring output powers of the receiver when connected to a hot (P_L^H) or cold (P_L^C) 50 Ω load, the noise factor is given in [13] as

$$F_r = \frac{(T_{HL} - T_{CL})}{T_{HL}(1 - 1/Y_r)}, \tag{4}$$

where the measured power ratio, Y_r, is P^H_L/P^C_L and the temperatures are T_{HL} =295 K and T_{CL} =77 K for hot and cold load, respectively.

Individual AUTs are measured in the composite system to obtain hot and cold measurements where the black body absorber (Ecosorb), placed in front of the antenna element, has been held at room temperature (T_{HA}= 295 K) for the hot load and has been immersed in liquid nitrogen (T_{CA}= 77 K) for the cold load. Note that the 50 Ω calibration load is submersed into the liquid nitrogen. The resulting composite system noise factor is expressed as

$$F_C = \frac{(T_{HA} - T_{CA})}{T_{HA}(1 - 1/Y_C)}, \tag{5}$$

where the measured power ratio of the antenna, Y_c, is P^H_A/P^C_A. Since the measured output noise powers of the receiver and the composite system with the hot load is known, the antenna gain can be obtained from the following expressions

$$P_L^H = KT_{HL}BG_rF_r \tag{6}$$

$$P_A^H = KT_{HA}BG_rG_AF_C \tag{7}$$

where G_r and G_A are the receiver and antenna gain, respectively. After dividing the two hot load power equations, (EQ 7) by (EQ 6), and substituting in the noise factor parameters, F_r (EQ 4) and F_c (EQ 5), the antenna gain expression becomes

$$G_A = \frac{P^H_A - P^C_A}{P^H_L - P^C_L} \tag{8}$$

Equation (8) assumes equal temperatures for the 50 Ω load and AUT in either the cold (T_{HL}=T_{HA}=295 K) or hot (T_{CL}=T_{CA}=77 K) load measurement.

A modified gain expression is shown in Equation (9) that accounts for temperature differences observed in the application of the test methodology in the measurement of the cold 50 Ω load and AUT. Since the absorber is immersed into liquid nitrogen and then removed to cover the antenna, the cold temperature is slightly elevated and is taken as T_{CA}=88 K while the 50 Ω load, submersed continuously into the liquid nitrogen, maintains a constant temperature, T_{CL}, of 77K. Hence,

$$G_A = 1.038\frac{P^H_A - P^C_A}{P^H_L - P^C_L} \tag{9}$$

B. Ku-Band Micromachined Patch Antenna

Since the available measurement set-up imposes an operating frequency range between 12.5 and 13.5 GHz, several rectangular patch designs are fabricated on duroid substrates of high (10.8) and low (2.2) index constants with substrate thickness, t, of 635 and 500 microns, respectively. Scaled model micromachined antennas were also fabricated in which the cavity is created by machine milling. The final geometry is similar to those shown in Figure 1 without the sloping sidewalls, and the dimensions for the various antennas can be found in Table 2, where the parameters a and b are given by their actual values and not the average ones since the sidewalls are vertical. To describe the findings of the various patch configurations investigated, the notation used in the following sections refers to antennas on full thickness substrates as "regular" high (10.8) or low (2.2) index designs and those printed on a mixed air-duroid cavity as scaled models. Each patch is fed by a 50 Ω microstrip feedline, is fabricated on a $(75\ mm)^2$ substrate, and is mounted in the test fix-

ture shown in Figure 5. Since the micromachined scaled model antenna resides over the mixed dielectric material, approximately 3.65 mm of the feed line has an impedance based on the mixed air-duroid region compared to the feedline of regular antennas on full thickness material. The width of the feeding line (560 μm) for the scaled model patch is maintained over the mixed region and is the same with the width of the 50 Ω line on full substrate resulting in a characteristic impedance of approximately 96 Ω The return loss is measured (Figure 6) and the input impedance values referenced at the RF connector are shown in Table 3; notice the good agreement between the scaled model and regular low index antenna. In Figure 6 the bandwidth of the scaled model increases to 2.3%, a 100% increase over the -10 dB bandwidth of the regular patch printed on the high index material. This increase in bandwidth is also observed in the silicon micromachined antenna and is an indication of the expected increase in total power (space and surface waves) radiated from the patch.

To minimize the interaction between the connector and the antenna in the radiation pattern measurements, a small piece of absorber is placed over the RF connector to reduce the effects of secondary reflections on the antenna pattern. In Figure 7 the "regular" high index pattern has a large peak in the E-plane at approximately -50 degrees, indicating large power leakage to surface waves. This behavior is also observed in [4]. In contrast, the scaled model patch shown in Figure 8 has a much smoother E-plane pattern and is very similar to the E-plane pattern of the "regular" low index antenna. As expected, the H-plane patterns are similar in all cases. The difference between the E-plane patterns of Figures 4b and 7 (both antennas are "regular") can be attributed to the slightly different dielectric constant, the different experimental set-up used for the pattern measurements and the fact that the distance between the antenna and the edge of the finite ground plane is not the same in terms of guided wavelengths .

C. Efficiency Measurements

The system configuration [5] is illustrated in Figure 9 and has component specifications consisting of an RF bandpass filter with an insertion loss of 3 dB in the 12.5 to 13.5 GHz range and a

mixer intermediate frequency (IF) of 1.5 GHz. Since the calibration plane of the system is at the RF connector, the measured efficiency values include the feed line, connector and mismatch losses. In order to determine the de-embedded antenna efficiency, the losses must be determined and extracted. The losses associated with the feed line lengths (Table 3) are calculated using HP Momentum [5,14]; the RF connector loss is based on an empirical value; and the mismatch loss is determined from the measured return loss data.

In Figure 10, the measured efficiency data, which are averaged values, show 73 ± 3 % for the scaled model having an air-substrate thickness ratio of 3:1 and 56 ± 3 % for the "regular" antenna printed on the high index material. The patch printed on 2.2 duroid was found to have an efficiency of 76±3 %. In Table 4, a summary of the measured efficiency, specific losses, and de-embedded efficiency are documented. The scaled model case shows sensitivity to the distance c between the radiating edges of the antenna and the edges of the micromachined cavity. From the results summarized in Table 5, it can be observed that for an air-substrate thickness ratio of 1:1 and separation c=0, the efficiency of the scaled model is similar to that of a patch on high index substrate. However, when the distance is at least twice the substrate thickness, 2t, for the same air-substrate thickness ratio, the de-embedded efficiency increases by about 10%. This is further validated in the measured data shown in Table 4 for a distance of c=3.783mm (6 times the substrate height, 6t). The improvements observed are attributed to the presence of fringing fields that usually extend one to two times the thickness t beyond the radiating edges of the antenna into the substrate environment. The above results emphasize the importance of the air-substrate thickness ratio on bandwidth, and also the importance of the distance between the radiating edge of the antenna and the micromachined cavity in order to enhance the antenna's efficiency.

The de-embedded efficiencies of the individual antenna elements (see Table 4) are 85% for the micromachined scaled model and 66% and 82% for the antennas on 10.8 and 2.2 duroid substrate, respectively. As a result, the efficiency of the micromachined patch increases by 28% over the high index patch and the efficiency performance approaches the patch on low index duroid within

the bounds of measurement error. When the modified efficiency expression is used to account for differences in the cold measurement of the 50 Ω load and AUT, the measured and de-embedded efficiencies increase by 2-3% as seen in Table 4. In this case, no significant difference is observed between either approach since the accuracy of the measurement system is 3%.

IV. CONCLUSIONS

The approach presented herein uses silicon micromachining techniques to physically alter the air-silicon thickness ratio by laterally removing material in selective regions of a high index substrate. To meet design space constraints and antenna performance requirements (bandwidth and radiation efficiency), this approach offers an easy method to optimize antenna size and maximize antenna performance in selective regions of circuits designed on high index substrates. The overall dimensions of the radiating element are determined by the effective dielectric constant (or index) of the material and can range from its smallest size in a high index material such as silicon (ε_r=11.7) to its largest size in an air substrate (ε_r=1.0) region.[1]

Characterization of the micromachined patch antenna has been presented to illustrate the advantages of selectively reducing the dielectric constant in specific locations of a high index material in order to enhance patch antenna performance. Both antenna configurations show an increase in the impedance bandwidth and smoother E-plane radiation patterns compared to patch designs in high index materials. Antenna efficiency measurements were performed on the scaled model reflecting similar values to the low index patch antenna (ε_r=2.2). For micromachined antennas, it is also shown that placement of the antenna's radiating edges with respect to the high index region is critical to improving the power radiated as space waves and must be at least twice the substrate thickness. Finally, a comparison between the high index patch and the micromachined scaled model shows bandwidth improvements by 64% from values of 1.4% to 2.3% and efficiency improvements by 28% from values of 66% to 85%, respectively. Therefore, enhanced antenna

1. A dielectric membrane supports the antenna element over an air cavity formed by etching the silicon entirely away.

performance has been achieved using this micromachining approach where the bandwidth and efficiency improvements indicate that patch elements can be integrated in compact MMIC designs on high index environments.

ACKNOWLEDGEMENTS

This work was supported by the Office of Naval Research under contract No. N00014-92-J-1070 and the Army Research Office (MURI Program) under grant No. DAAL03-92-G0109. The authors would like to thank Dr. Gabriel Rebeiz, Mr. Tommy Ellis for assistance in fabricating the duroid based antennas, Mr. Gildas Gauthier for helping with efficiency measurements and Rogers Corporation, Chandler, AZ, for the generous donation of the duroid substrates. The assistance of Drs. Rainee Simons and Richard Lee at NASA Lewis is also greatly appreciated in obtaining antenna pattern measurements.

V. REFERENCES

[1] D.M. Pozar, "Microstrip Antennas," *IEEE Proceedings,* Vol. 80, January 1992, pp.79-91.

[2] N.G. Alexopoulos and D.R. Jackson, "Fundamental Superstrate (Cover) Effects on Printed Circuit Antennas," *IEEE Trans. on Antenna and Propagation*, Vol. AP-32, No. 8, August 1984, pp.807-816.

[3] D. R. Jackson, J. T. Williams, et. al, "Microstrip Patch Designs that Do Not Excite Surface Waves," *IEEE Trans. on Antennas and Propagation*, Vol. 41, No. 8, August 1993, pp. 1026-1037.

[4] M. J. Vaugh, K. Hur, and R. C. Compton, "Improvement of Microstrip Patch Antenna Radiation Patterns," *IEEE Trans. on Antennas and Propagation*, Vol. 42, No. 6, June 1994, pp. 882-885.

[5] G.P. Gauthier, A. Courtay and G.M. Rebeiz, "Microstrip Antennas on Synthesized Low Dielectric-Constant Substrates," *IEEE Trans. on Antennas and Propagation,* Vol. 45, No. 8, August 1997, pp.1310-1314.

[6] T. M. Weller, L. P. B. Katehi, and G. M. Rebeiz, "High Performance Microshield Line Components," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 3, March 1995, pp. 534-543.

[7] R. F. Drayton and L. P. B. Katehi, "Development of Self-Package High Frequency Circuits Using Micromachining Techniques," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 9, Sept. 1995, pp. 2073-2080.

[8] S. V. Robertson, L. P. B. Katehi, and G. M. Rebeiz, "Micromachined W-Band Filters," *IEEE Trans. on Microwave Theory and Techniques,* Vol. 44, No. 4, April 1996, pp. 598-606.

[9] E.O. Hammerstad and F.Bekkadal, "A Microstrip Handbook," ELAB Report, STF 44 A74169, N7034 University of Trondheim, Norway, 1975.

[10] D.M. Pozar, *PCAAD: Personal Computer Aided Antenna Design*, Version 2.1.

[11] J. Ashkenazy, E. Levine and D. Treves, "Radiometric Measurement of Antenna Efficiency," *Electron. Lett.,* Vol. 21, No. 3, January 1985.

[12] D.M. Pozar and B. Kaufman, "Comparison of Three Methods for the Measurement of Printed Antenna Efficiency," *IEEE Trans. on Antennas and Propagation,* Vol. 36, No.1, January 1988, pp. 136-139.

[13] D.M. Pozar, Microwave Engineering, Addison Wesley, September 1993.

[14] HP EEsof, Inc.: Westlake Village, CA.

VI. BIOGRAPHIES

Ioannis Papapolymerou received the B.S.E.E. degree from the National Technical University of Athens, Greece, in 1993 and the M.S.E.E degree from the University of Michigan, Ann Arbor, MI, in 1994. He is currently pursuing the Ph.D. degree in electrical engineering at the University of Michigan.

His research interests include the implementation of micromachining techniques in microwave and millimeter-wave circuits, the development of both passive and active planar circuits on Silicon and GaAs for high frequency applications, as well as numerical techniques for the characterization of those circuits.

Mr. Papapolymerou has received the Outstanding Graduate Student Instructional Assistant Award in 1997 by the American Society for Engineering Education (ASEE), University of Michigan Chapter.

Rhonda Franklin Drayton received the B.S.E.E. from Texas A&M University, College Station, Tx. in 1988 and the M.S.E.E. and Ph.D. degree from the University of Michigan, Ann Arbor, MI in 1990 and 1995 respectively. She is currently an Assistant Professor in the Electrical Engineering and Computer Science Department at the University of Illinois, Chicago.

Her current research interests include development of high frequency planar circuits, antennas and packages for microwave and millimeter-wave applications using micromachining techniques.

She received First Prize for the Best Student Paper at the 1994 IEEE MTT-S International Microwave Symposium and the 1997 Amoco Silver Circle Award for Teaching Excellence from the University of Illinois at Chicago.

Linda P.B. Katehi received the B.S.E.E. degree from the National Technical University of Athens, Greece, in 1977 and the M.S.E.E. and Ph.D. degrees from the University of California, Los Angeles, in 1981 and 1984 respectively.

In September 1984 she joined the faculty of the EECS Department of the University of Michigan, Ann Arbor. Since then, she has been interested in the development and characterization (theoretical and experimental) of microwave, millimeter-wave printed circuits, the computer-aided design of VLSI interconnects, the development and characterization of micromachined circuits for millimeter-wave and submillimeter-wave applications, and the development of low-loss lines for Terahertz-frequency applications. She has also been theoretically and experimentally studying various types of uniplanar radiating structures for hybrid-monolithic and monolithic oscillator and mixer designs.

Dr. Katehi is a member of the IEEE Antennas and Propagation Society, Microwave Theory and Techniques Society, Sigma Xi, Hybrid Microelectronics, URSI Commission D, and a member of IEEE Antennas and Propagation Society ADCOM from 1992 to 1995. She also serves as an Associate Editor for the IEEE Transactions on Microwave Theory and Techniques. She has been awarded the IEEE AP-S W. P. King Award in 1984, the IEEE AP-S S. A. Schelkunoff Award in 1985, the NSF Presidential Young Investigator Award, an URSI Young Scientist Fellowship in 1987, the Humboldt Research Award in 1994, the University of Michigan Faculty Recognition Award in 1994 and the IEEE Microwave Theory and Techniques Society Microwave Prize in 1996.

LIST OF FIGURE CAPTIONS

Figure 1: Geometry of the micromachined patch antenna with mixed air-substrate region that has been laterally etched away.

Figure 2: Geometries used to determine the capacitance model for the micromachined patch antenna for (a.1) radiating edges into the high index silicon substrate and (a.2) radiating edges over the mixed air-substrate cavity. b) Graph of effective dielectric constant versus air gap thickness (percent) for the silicon based micromachined patch using the cavity and FDTD model compared to the measured response of the micromachined antenna (a.1 geometry).

Figure 3: Return loss measurement of the regular and micromachined patch antenna printed on a full thickness substrate and substrate with mixed air-silicon thickness ratio (1:1), respectively.

Figure 4: (a) E and H-plane radiation patterns of the micromachined antenna on silicon and of the (b) regular antenna on silicon.

Figure 5: Test Fixture with micromachined antenna mounted.

Figure 6: Measured return loss for the scaled model patch antenna, ε_{reff}=2.3 (etched), and regular patch antennas, ε_r=2.2 and ε_r=10.8.

Figure 7: Radiation patterns of a regular high index patch antenna (ε_r=10.8 and t=635 μm) at 12.84 GHz resonant frequency.

Figure 8: E and H-plane radiation patterns for (a) patch antenna on low index duroid substrate (ε_r=2.2 and t=500 μm) at resonant frequency of 13.044 GHz and (b) scaled model on a duroid substrate (ε_r=10.8 and t=635 μm) at resonant frequency of 13.165 GHz.

Figure 9: System diagram of the efficiency measurement set-up.

Figure 10: Measured efficiency for the scaled model and regular patch antenna designs.

LIST OF TABLE CAPTIONS

Table 1: Design parameters for the antennas on silicon substrates.

Table 2: Dimensions of the fabricated scaled model and regular antennas.

Table 3: Input impedance characteristics of the regular and scaled model antennas.

Table 4: De-embedded efficiency for the scaled model and regular patch antennas at resonance.

Table 5: Efficiency results and dimensions for two scaled model antennas on duroid substrate with ε_r=10.8.

FIGURES

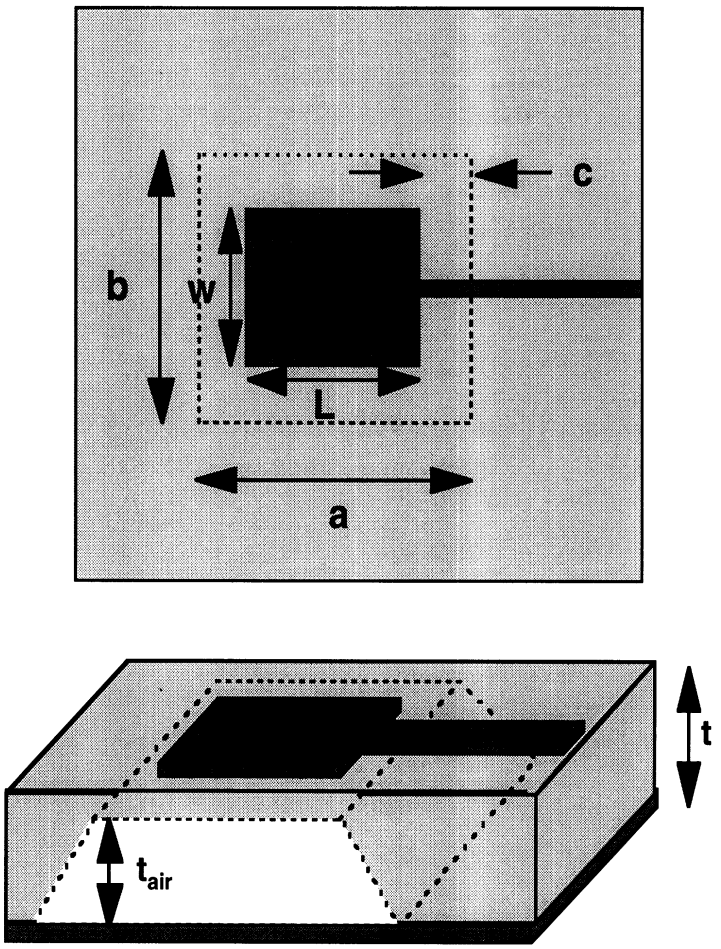
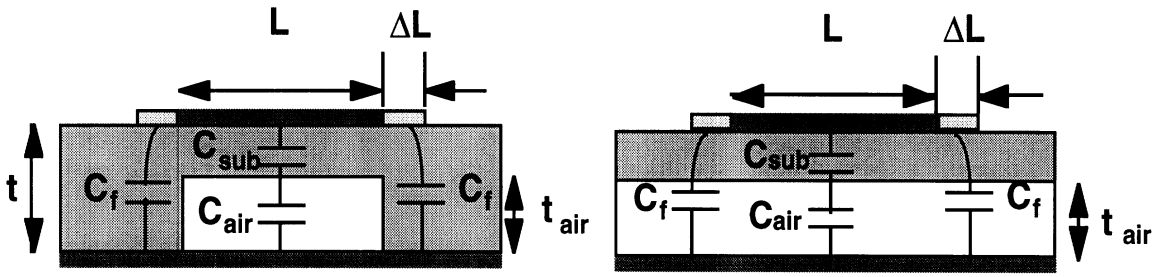


Figure 1: Geometry of the micromachined patch antenna with mixed air-substrate region that has been laterally etched away.



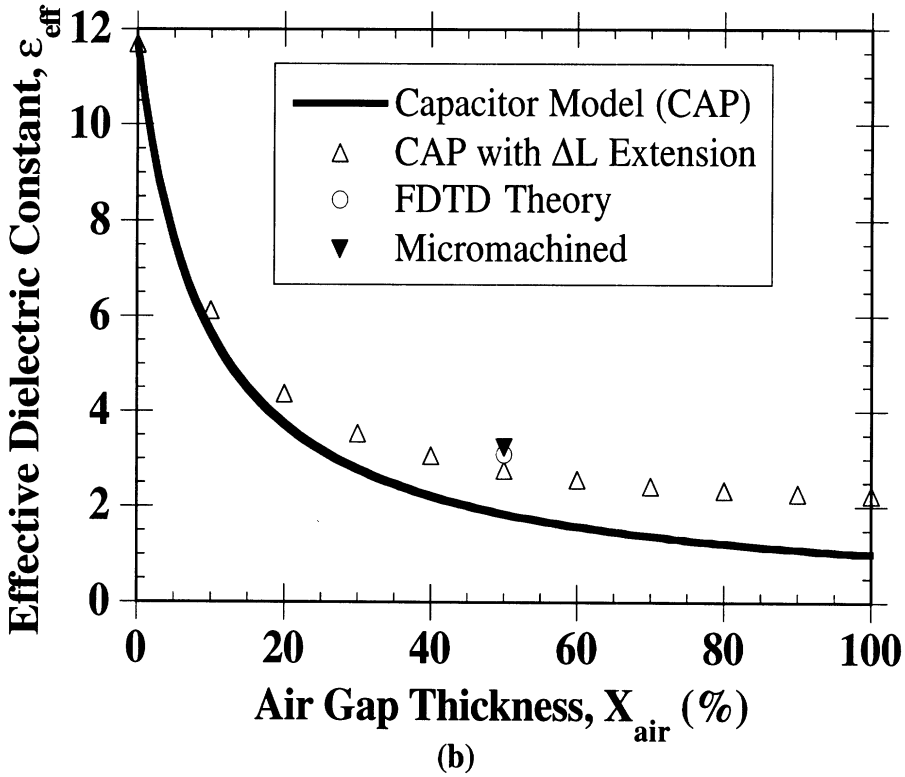


Figure 2: Geometries used to determine the capacitance model for the micromachined patch antenna for (a.1) radiating edges into the high index silicon substrate and (a.2) radiating edges over the mixed air-substrate cavity. b) Graph of effective dielectric constant versus air gap thickness (percent) for the silicon based micromachined patch using the cavity and FDTD model compared to the measured response of the micromachined antenna (a1 geometry).

Table 1: Design parameters for the antennas on silicon substrates.

Patch	t (mm)	t_{air} (mm)	L (mm)	w (mm)	a (mm)	b (mm)	c (mm)
Regular	0.355	0	2.019	4.08	0	0	0
Micromachined	0.355	0.165	3.616	3.445	3.616	8.108	0

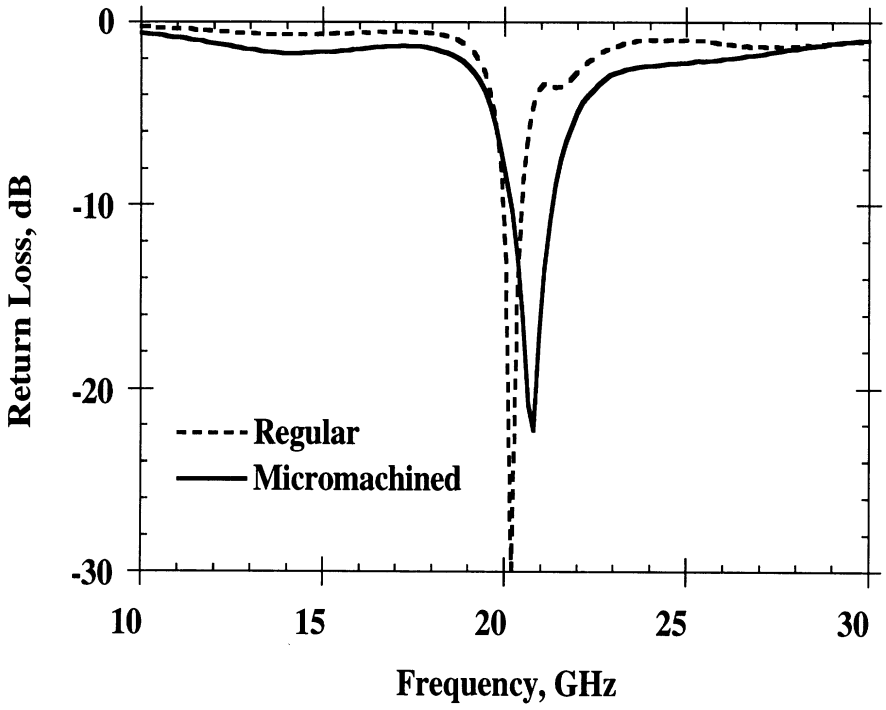
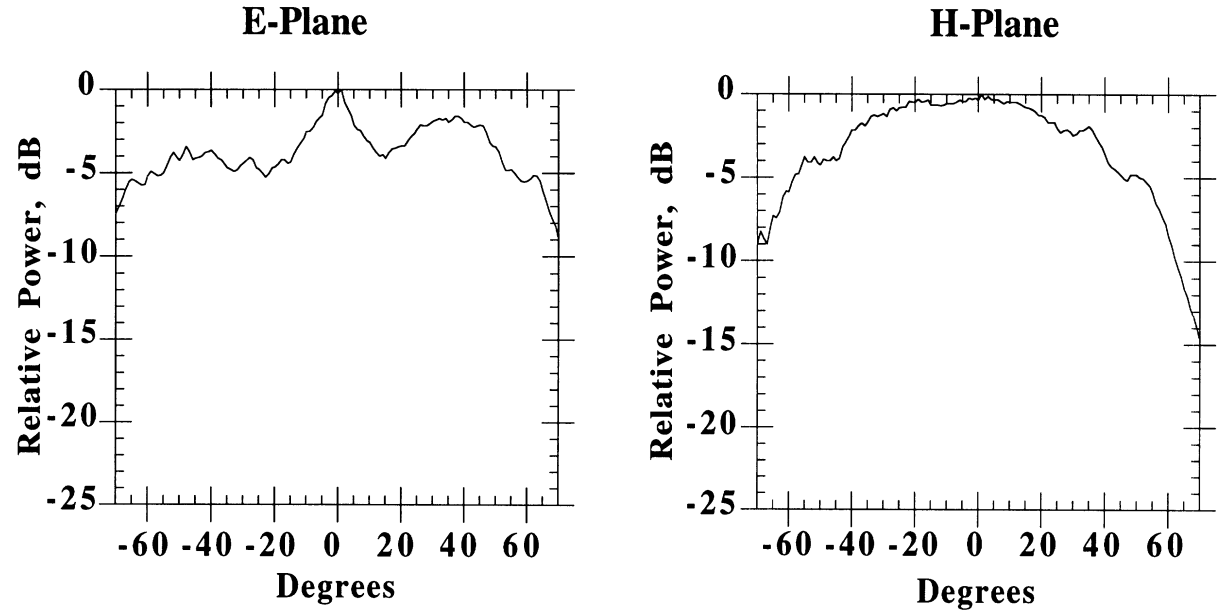
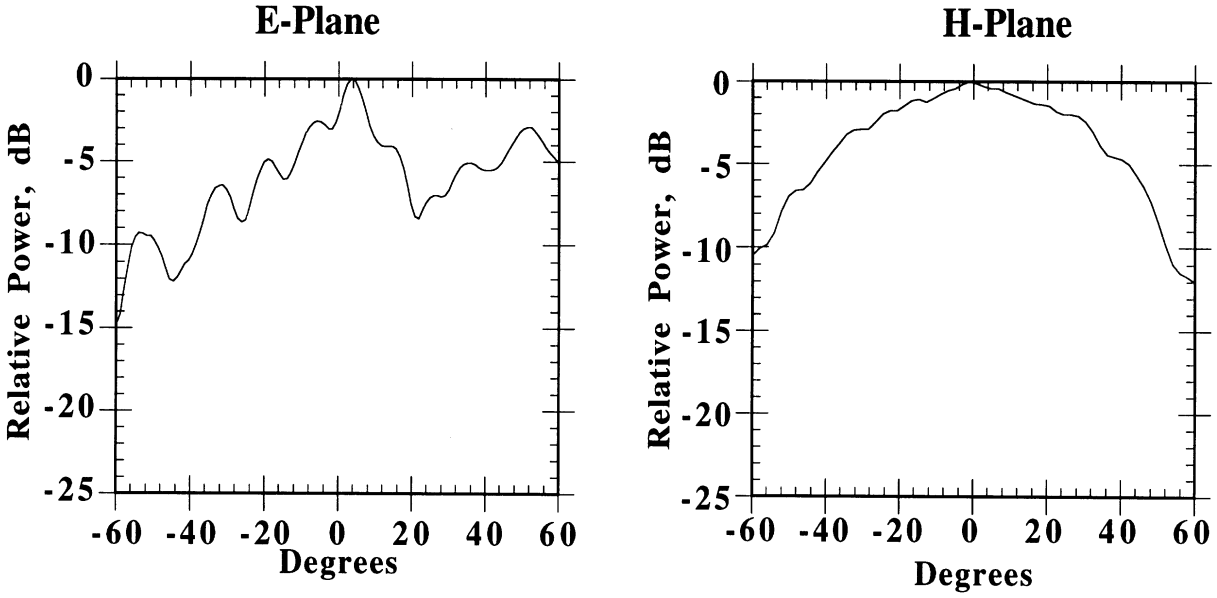


Figure 3: Return loss measurement of the regular and micromachined patch antenna printed on a full thickness substrate and substrate with mixed air-silicon thickness ratio (1:1), respectively.



(a) Micromachined Patch Antenna



(b) Regular Patch Antenna

Figure 4: (a) E and H -plane radiation patterns of the micromachined antenna on silicon and of the (b) regular antenna on silicon.

Table 2: Dimensions of the fabricated scaled model and regular antennas.

Patch	t (mm)	t_{air} (mm)	L (mm)	w (mm)	a (mm)	b (mm)	c (mm)
Regular (10.8)	0.635	0	3.750	4.420	0	0	0
Scaled Model (10.8)	0.635	0.476 (75%)	7.624	6.676	15.190	14.478	3.783
Regular (2.2)	0.500	0	7.570	7.340	0	0	0

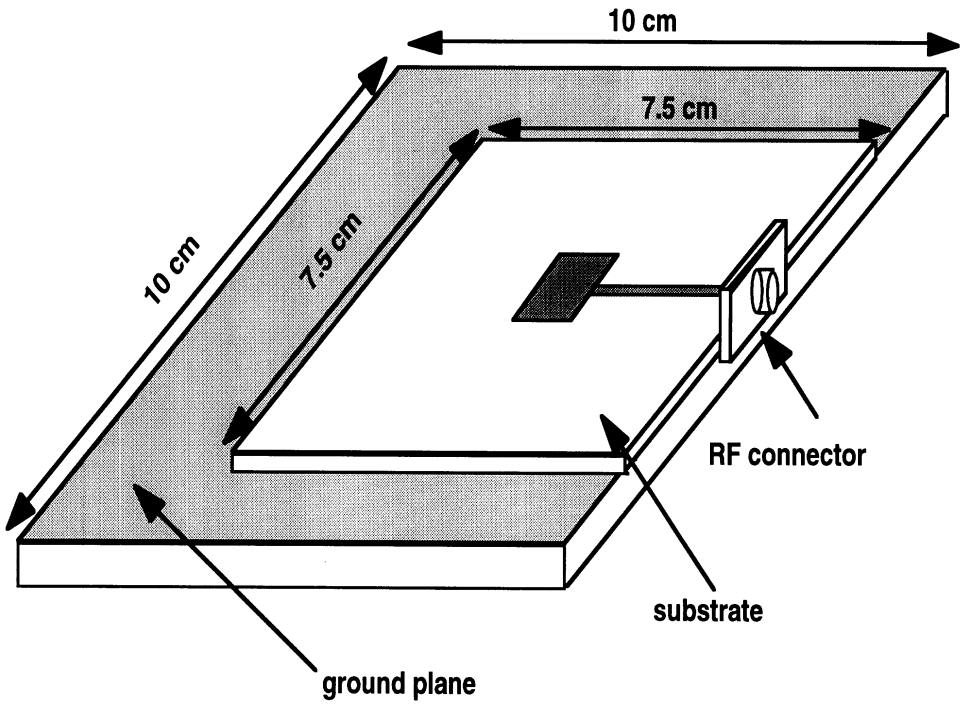


Figure 5: Test Fixture with micromachined antenna mounted.

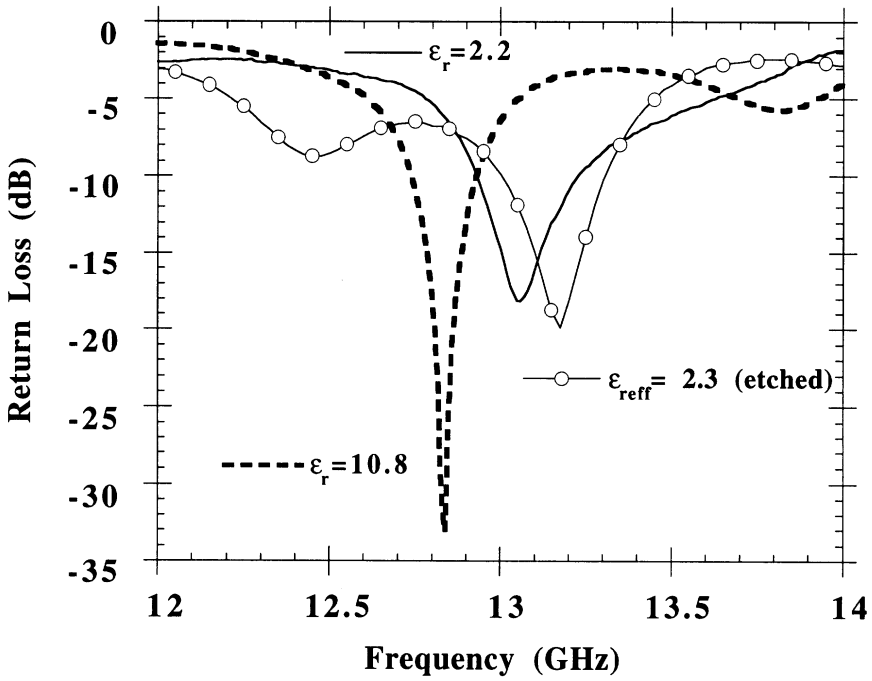


Figure 6: Measured return loss for the scaled model patch antenna, ε_{reff}=2.3 (etched), and regular patch antennas, ε_r=2.2 and ε_r=10.8.

Table 3: Input impedance characteristics of the regular and scaled model antennas

Patch	Input Impedance (Ω)	Resonant Frequency (GHz)	Feed Line Length (mm)
Regular (10.8)	49.2 - j0.37	12.84	27.6
Scaled model (10.8)	67.5 - j1.04	13.165	27
Regular (2.2)	67.5 - j0.14	13.044	34

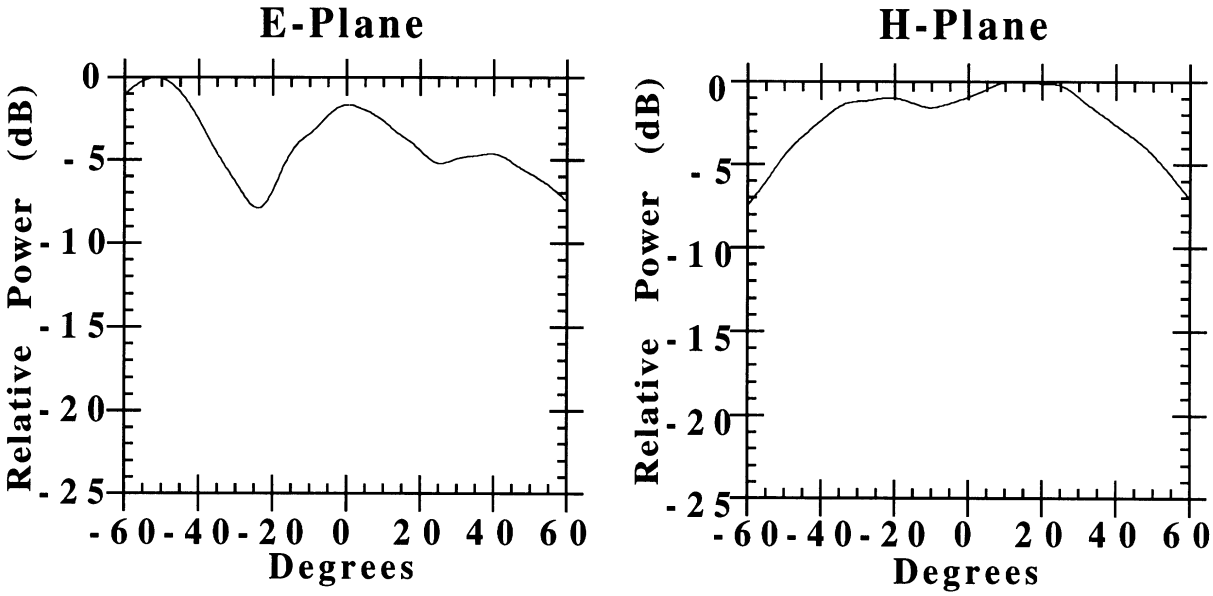
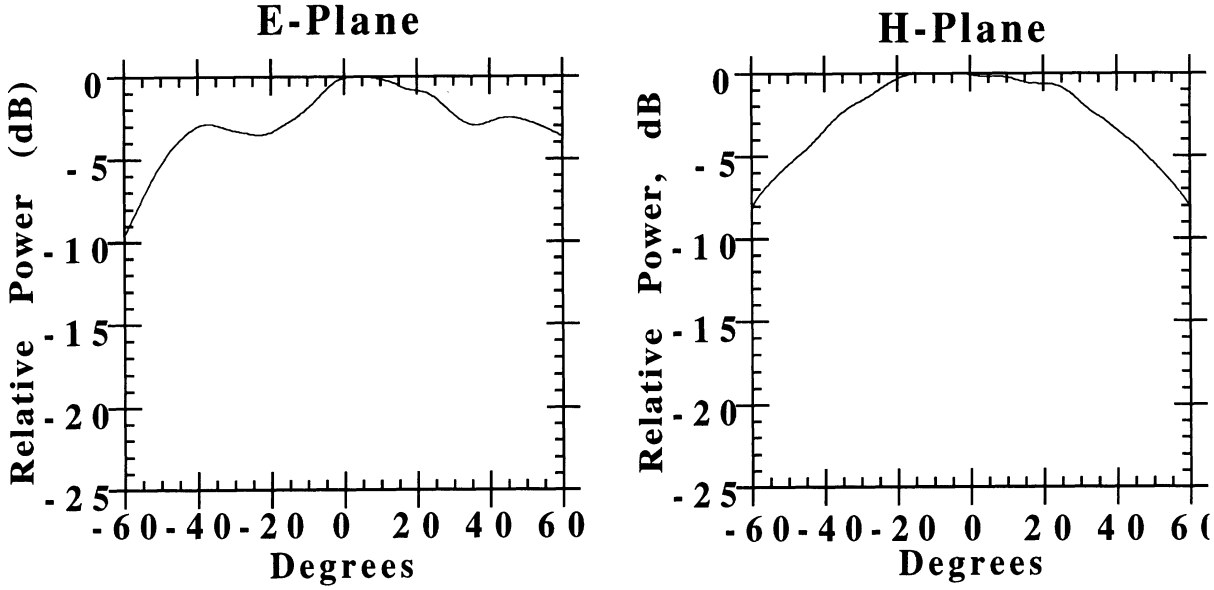
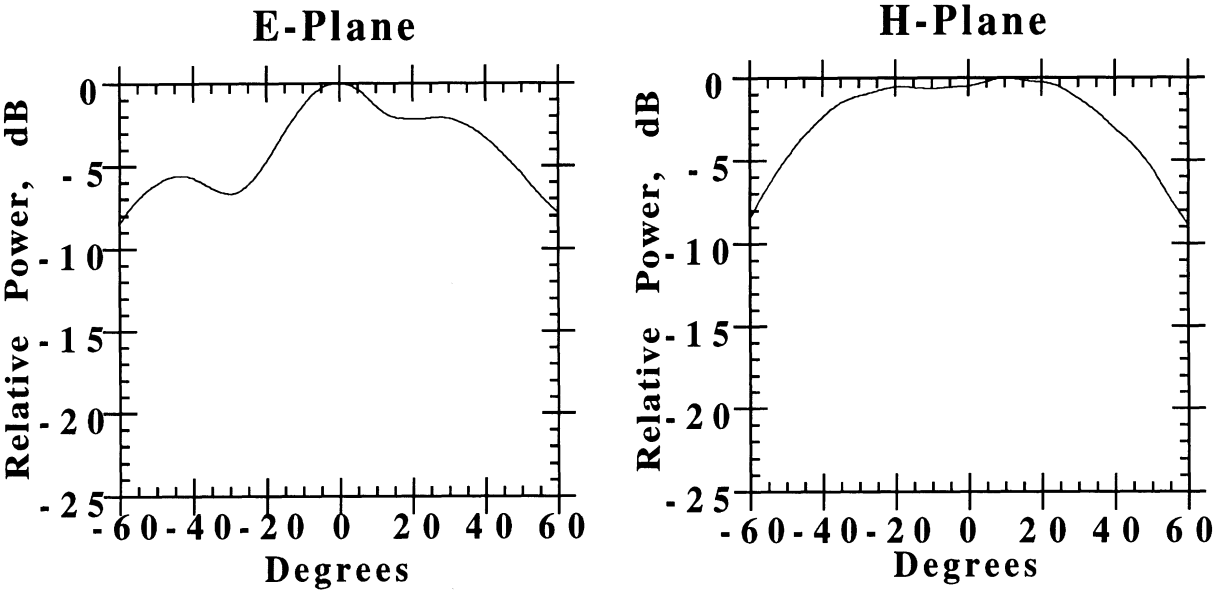


Figure 7: Radiation patterns of a regular high index patch antenna (ε_r=10.8 and t=635 μm) at 12.84 GHz resonant frequency.



(a) Regular Low Index Patch Antenna (ε_r=2.2)



(b) Scaled Model Patch Antenna (ε_{reff}=2.3)

Figure 8: E and H-plane radiation patterns for a (a) patch antenna on low index duroid substrate (ε_r=2.2 and t=500 μm) at resonant frequency of 13.044 GHz and (b) scaled model on a duroid substrate(ε_r=10.8 and t=635 μm) at resonant frequency of 13.165 GHz.

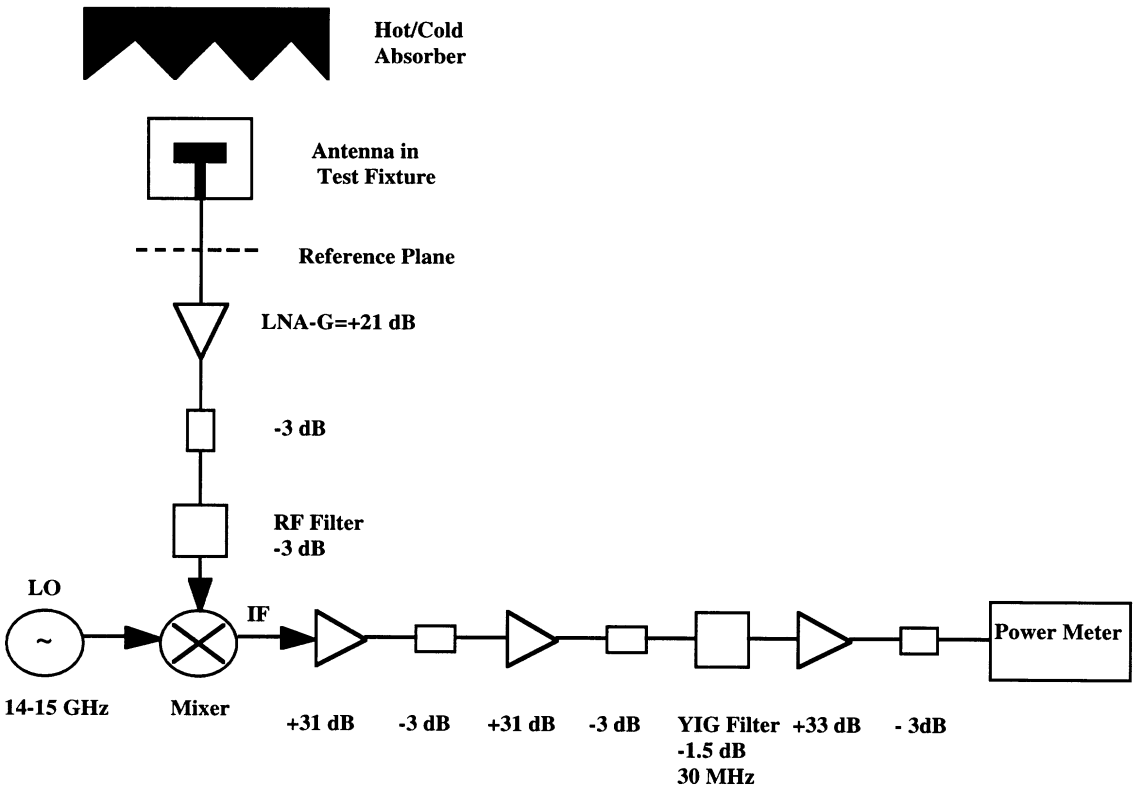


Figure 9: System diagram of the efficiency measurement set-up.

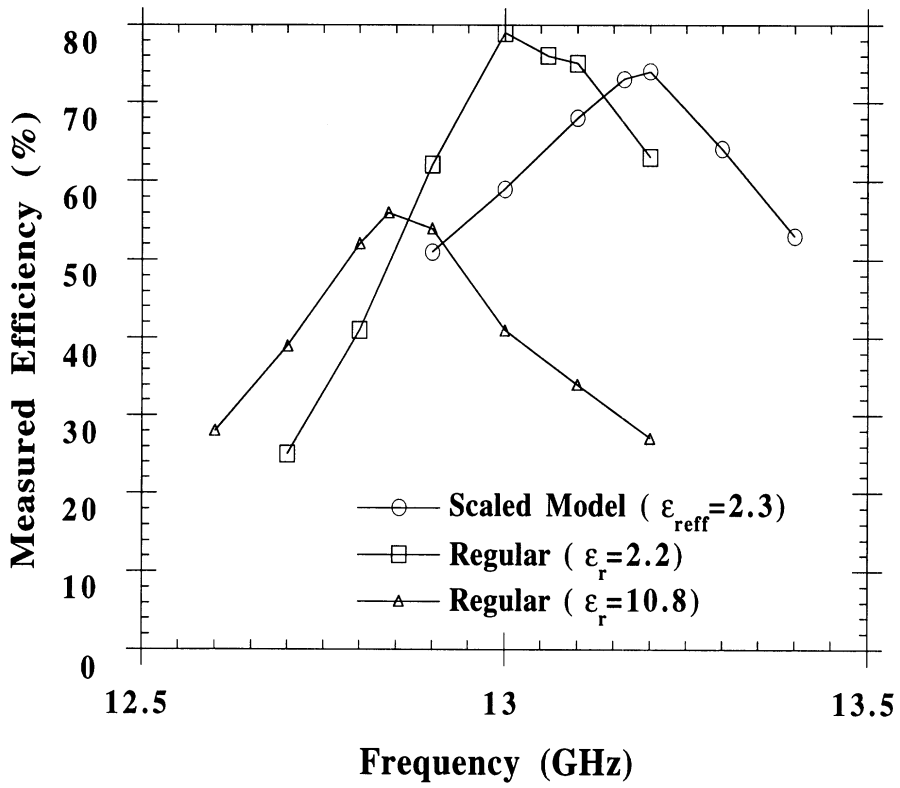


Figure 10: Measured efficiency for the scaled model and regular patch antenna designs.

Table 4: De-embedded efficiency for the scaled model and regular patch antennas at resonance.

Antenna	Regular ε_r=10.8	Scaled Model ε_r=10.8	Regular ε_r=2.2
Measured Efficiency			
Based on Equation (8)	56%	73%	76%
Based on Equation (9)	58%	76%	79%
Mismatch loss (dB)	0 (100%)	0.05 (99%)	0.08 (98%)
Connector loss (dB)	0.15 (97%)	0.15 (97%)	0.15 (97%)
Feed line loss (dB)	0.56 (88%)	0.48 (90%)	0.1 (98%)
Total loss (dB)	0.71 (85%)	0.68 (86%)	0.33 (93%)
De-embedded Efficiency			
Based on Equation (8)	66%	85%	82%
Based on Equation (9)	68%	88%	85%

Table 5: Efficiency results and dimensions for two scaled model antennas on duroid substrate with ε_r=10.8

Patch Antenna	Mixed air-substrate thickness ratio (1:1) c=0	Mixed air-substrate thickness ratio (1:1) c ≈2t
t (mm)	0.635	0.635
t_{air} (mm)	0.330	0.330
L (mm)	5.415	7.624
w (mm)	6.676	6.676
a (mm)	5.415	10
b (mm)	10.590	14
Measured efficiency	52%	65%
Total loss (dB)	0.69 (85%)	0.69 (85%)
De-embedded efficiency	61%	76%

Coplanar Stripline Propagation Characteristics and Bandpass Filter

Kavita Goverdhanam, *Student Member, IEEE*, Rainee N. Simons, *Senior Member, IEEE*, and Linda P. B. Katehi, *Fellow, IEEE*

Abstract— **In this paper, a coplanar stripline bandpass filter is developed. The propagation characteristics of the coplanar stripline used for the construction of the filter are presented in the form of phase constant and attenuation constant. The filter is characterized experimentally as well as theoretically by use of the finite-difference time-domain (FDTD) technique. The agreement between the measured and modeled filter characteristics is very good.**

I. Introduction

COPLANAR stripline (CPS) [1] as a transmission medium with the capability to provide uniplanar designs was introduced in the mid 1970's. It is well known that CPS lines make efficient use of the wafer area, have the capability to sustain back metallization without exciting parasitic modes within the range of the operating frequency and to simplify heat sinking and packaging in high-power applications (CPS power amplifiers). Extensive work on CPS lines in the recent past [2]–[4] has shown that CPS has the capability to provide excellent propagation characteristics and small discontinuity parasitics when appropriately designed. Recent studies of several CPS discontinuities have shown that CPS lines can find applicability to wireless communications through low-cost uniplanar microwave circuits such as filters, mixers, and antennas [2], [4]. Based on these results, CPS bandstop filters have been designed and characterized and these filters have demonstrated many advantages.

CPS filters have several unique features and advantages. Their uniplanar construction allows ease of fabrication. Also, these filters use series resonating elements which are fabricated within the 50-Ω strip conductors and, hence, are extremely compact when compared to microstrip filters. In addition, they do not require bond wires and air bridges to suppress higher order modes at discontinuities, resulting in simpler design when compared to conventional coplanar waveguide (CPW) filters.

This work presents a study of the dispersion characteristics of the CPS line along with its attenuation as a function of frequency. In addition, a CPS bandpass filter has been designed and fabricated, and its performance has been characterized both experimentally as well as numerically by FDTD simulation for performance verification.

Manuscript received February 17, 1997. This work was supported by the office of Naval Research.

K. Goverdhanam and L. P. B. Katehi are with the Radiation Laboratory, University of Michigan, Ann Arbor, MI 48109 USA.

R. N. Simons is with the NASA Lewis Research Center NYMA Group, Cleveland, OH 44135 USA.

Publisher Item Identifier S 1051-8207(97)05424-X.

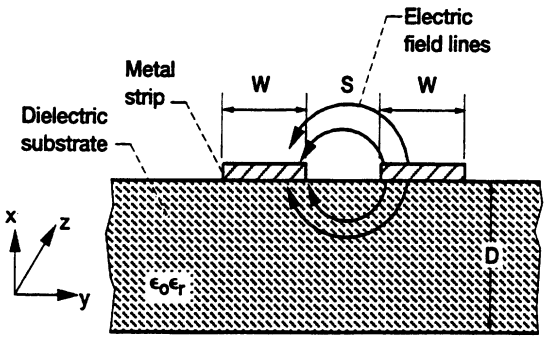


Fig. 1. Cross section of CPS.

II. Theoretical and Experimental Characterization

The coplanar stripline is supported by a dielectric substrate of relative permittivity ϵ_r and thickness D, as shown in Fig. 1. In a CPS [1], the electric lines extend from the edges of the strip conductors of width W across the slot of width S and remain strongly bound to the aperture between the two adjacent strips. As a result, the lines exhibit characteristics which are rather insensitive to the substrate thickness and presence of metallization on the other side of the substrate. Below, theoretical and experimental results for wave propagation characteristics in CPS lines and a CPS BP filter are presented and discussed extensively.

A. Measurement/De-Embedding Technique

All the measurements have been performed with the 8510 network analyzer using a set of CPS TRL on-wafer standards. The calibration standards consist of a CPS Thru, a CPS short circuit, and a CPS delay line and is performed using National Institute of Standards and Technology (NIST), a de-embedding software program [5]. This program solves a 12-term error model from the thru-line two-port measurements, the delay line two-port measurements, and the two one-port reflection measurements. The program then establishes electrical reference planes to which all de-embedded S-parameters are referred. In addition, it provides, the attenuation constant α. In order to suppress spurious modes, the CPS substrate is stacked on top with a 0.031-in-thick ($\epsilon_r = 2.2$) RT/Duroid 5880 and a 0.25-in-thick microwave absorber.

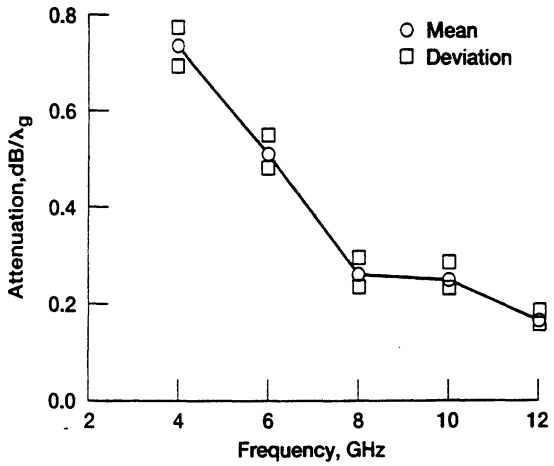


Fig. 2. CPS measured attenuation.

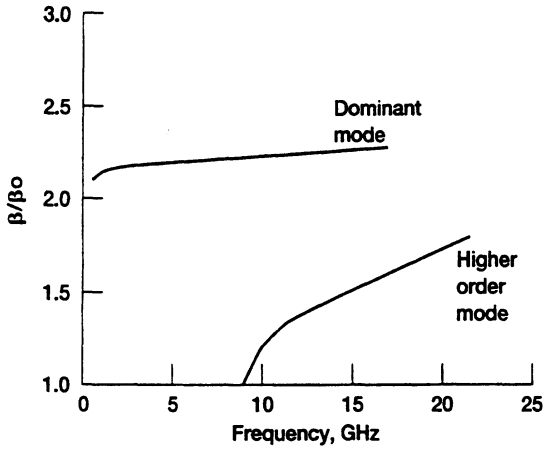


Fig. 3. CPS computed dispersion and higher order mode.

B. Theoretical Modeling

As mentioned above, the modeling was performed using the FDTD method, which is based on expressing Maxwell's curl equations in discretized space and time domains. In order to characterize a planar discontinuity, propagation of a specific time-dependent function is simulated using FDTD technique. In characterizing the filter mentioned above, a Gaussian pulse is used. The space steps Δx, Δy, and Δz are carefully chosen such that integral numbers of them can approximate the dimensions of the structure. In order to minimize the truncation and grid dispersion errors, the maximum step size is chosen to be less than 1/20 of the smallest wavelength in the computational domain. The Courant stability criterion is used to select the time step to ensure numerical stability. The values for Δx, Δy, Δz, and the time step Δt used for modeling the bandpass filter here are 127.0, 101.6, and 203.2 μm and 0.23 ps, respectively. The front and back planes of the FDTD mesh are terminated using super-absorbing first-order Mur boundary condition [6]. All the other walls are terminated using the first-order Mur boundary condition [7]. The circuit dimensions indicated in the following sections are the actual dimensions after fabrication. However, while performing the FDTD analysis, the exact fabricated dimensions could not be incorporated due to limitations in the uniform discretization adopted in the modeling.

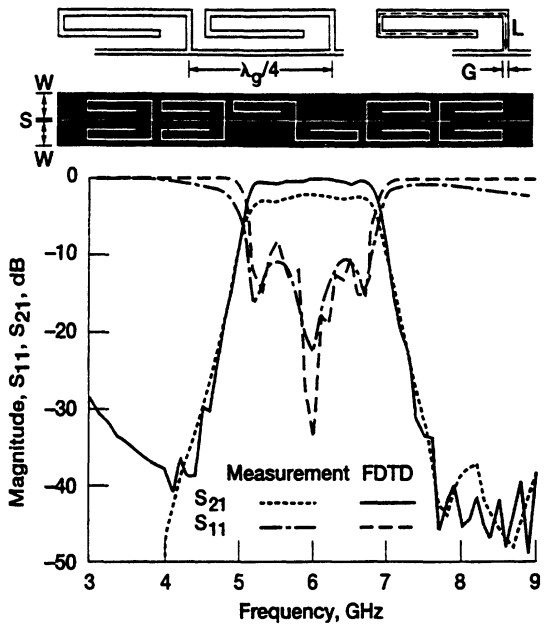


Fig. 4. CPS bandpass filter—geometry and measured/modeled characteristics.

III. Results and Discussion

In the following sections, measured results are shown for the attenuation constant of a CPS line as a function of frequency along with theoretically predicted dispersion and higher order mode characteristics. Also, the measured/FDTD-modeled characterization of a CPS bandpass filter is presented and compared.

A. Measured (De-Embedded) Attenuation

The attenuation α is de-embedded for CPS lines fabricated on RT/Duroid 6010 substrate of thickness $D = 0.03$ in and $\epsilon_r = 10.2$ with 1/2-oz. copper. Measurements are performed on CPS lines with a fixed strip width W (= 0.065 in) and slot width S varying from 0.0025 to 0.005 in in steps of 0.0005 in. This includes a 50-Ω CPS line with $W = 0.065$ in and $S = 0.004$ in. Fig. 2 shows the measured attenuation as a function of frequency for the above mentioned set of CPS lines. From the figure, we see that α varies from 0.735 dB/λ_g at 4 GHz to about 0.164 dB/λ_g at 12 GHz. The repeatability of the measurements are within 0.015 dB/λ_g at 4 GHz and 0.093 dB/λ_g at 12 GHz.

B. FDTD-Modeled Dispersion and Higher Order Modes

Fig. 3 shows a plot of the normalized propagation constant β/β_o as a function of frequency obtained using two-dimensional (2-D) FDTD technique for a CPS line with $D = 0.03$ in, $W = 0.065$ in, $S = 0.004$ in, and $\epsilon_r = 10.2$. It is noticed that the dispersion is almost linear up to 9.0 GHz with no higher modes. Onset of higher order modes begins at around 9.0-GHz frequency. This has been confirmed by measuring the S parameters. Measurements on a through line with $W = 0.025$ in, $S = 0.004$ in, $D = 0.01$ in, and $\epsilon_r = 10.5$ have shown that there is no onset of higher order modes up to 40 GHz. Smaller line dimensions and thinner substrates can

push the cutoff frequency to higher frequencies thus extending the operating range.

C. CPS Bandpass Filter

The schematic of a CPS bandpass (BP) filter is shown in Fig. 4. The filter consists of five sets of series stubs spaced $0.25\lambda_g$ apart where λ_g is the guide wavelength in the CPS at the center frequency f_o of the bandpass filter. The BP filter was fabricated on an RT/Duroid 6010 substrate of thickness 0.03 in and $\epsilon_r = 10.2$. The design guidelines for the circuit elements of the bandpass filter are summarized as follows: $L = 0.5\lambda_g$, $W = 0.070$ in, $S = 0.0035$ in, $G = 0.008$ in.

The measured and FDTD-modeled insertion loss (S_{21}) and return loss (S_{11}) of the BP filter are shown in Fig. 4. The filter exhibits excellent characteristics. Discrepancies between the measured and FDTD-modeled results for the filter is attributed to the zero-loss assumption incorporated in the FDTD models, in addition to coarse FDTD gridding. It has been observed that the bandpass characteristics repeat at center frequencies where the stub length becomes even multiples of quarter guide wavelength $0.25\lambda_g$ as expected. Also, at frequencies where the stub length becomes odd multiples of quarter guide wavelength $0.25\lambda_g$, low-pass characteristics are observed.

IV. Conclusion

The coplanar stripline as a transmission medium holds a great deal of potential in the emerging wireless communications industry and in the design of low-cost uniplanar microwave circuits such as filters, mixers, and antennas. In view of these advantages, a CPS Bandpass filter has been modeled and its performance has been characterized both experimentally and theoretically. In addition, CPS characteristics such as attenuation, dispersion, and higher order modes have been studied. It has been found that CPS has excellent propagation characteristics with linear dispersion. Onset of higher order modes is at the higher end of the frequency range of interest, thereby making CPS an ideal choice for the type of applications described herein.

References

[1] J. B. Knorr and K. D. Kuchler, "Analysis of coupled slots and coplanar strips on dielectric substrate," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, no. 7, pp. 541–548, July 1975.

[2] K. Goverdhanam, R. N. Simons, N. I. Dib, and L. P. B. Katehi, "Coplanar stripline components for high frequency applications," in *IEEE MTT Symp. Dig.*, 1996, vol. II, pp. 1193–1196.

[3] K. Goverdhanam, R. N. Simons, and L. P. B. Katehi, "Coplanar stripline components for high frequency applications," *IEEE Trans. Microwave Theory Tech.*, to be published.

[4] R. N. Simons, N. I. Dib, and L. P. B. Katehi, "Modeling of coplanar stripline discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 5, pp. 711–716, May 1996.

[5] NIST De-embedding Software, Program DEEMBED, Revision 4.04, 1994.

[6] K. Mei and J. Fang, "Superabsorbtion—A method to improve absorbing boundary conditions," *IEEE Trans. Antennas Propagat.*, vol. 40, pp. 1001–1010, Sept. 1992.

[7] G. Mur, "Absorbing boundary conditions for the finite-difference approximation of the time domain electromagnetic-field equations," *IEEE Trans. Electromagn. Compat.*, vol. EMC-23, pp. 377–382, Nov. 1981.

Coplanar Stripline Components for High-Frequency Applications

Kavita Goverdhanam, *Member, IEEE,* Rainee N. Simons, *Senior Member, IEEE,* and Linda P. B. Katehi, *Fellow, IEEE*

Abstract— **In this paper, coplanar stripline (CPS) discontinuities such as a narrow transverse slit, a symmetric step, a right-angle bend, and a T-junction are characterized and their performance is parameterized with respect to frequency and geometry. In addition, filter design using coplanar stripline discontinuities has been investigated. Lumped equivalent circuits are presented for some of the discontinuities. The element values are obtained from the measured discontinuity scattering parameters. The experimental results are compared with theoretical data obtained using the finite-difference time-domain (FDTD) technique for validation and show very good agreement.**

Index Terms—**Band-stop filters, coplanar stripline, discontinuities, FDTD technique, scattering parameters, TRL calibration, uniplanar circuits.**

I. Introduction

As with a coplanar waveguide (CPW), the coplanar stripline (CPS) [1] was introduced in the mid-1970's as a transmission medium with the capability to provide uniplanar designs. Due to its balanced configuration, it has found wide applicability in feed networks for printed antennas [2], [3]. As the application moves to higher frequencies and the size of the substrate becomes critical in triggering parasitic modes and uncontrolled radiation, lines which show less dependence on wafer thickness become better candidates. Among these lines, the CPW has attracted much more attention despite the limitations imposed by its large ground planes and the excitation of parallel-plate parasitic modes. The use of many vias to suppress these parasitic modes introduces many difficulties in the design and fabrication resulting in poor performance and high cost. In view of the above disadvantages, coplanar lines with finite-size grounds such as the CPS require more attention. The CPS has the capability to provide excellent propagation [4]. When appropriately designed, it has small discontinuity parasitics, makes efficient use of the wafer area, and can sustain back metallization without exciting parasitic modes within the range of the operating frequency. Lastly, heat sinking and packaging in high-power applications (CPS power amplifiers) is simplified.

Some CPS discontinuities such as an open circuit, short circuit, series gap, spur-slot, and spur-strip have been extensively studied and characterized in the past [5]. This paper presents an extensive characterization of some additional CPS discontinuities, such as a narrow transverse slit, symmetric step, right-angle bend, and a T-junction. The equivalent-circuit model-element values for these discontinuities are determined from the scattering parameters (S-parameters) which are de-embedded from the measured S-parameters using a thru-reflect-line (TRL) algorithm. The circuits are fabricated on a 762-μm-thick RT-Duroid 6010 substrate ($\epsilon_r = 10.2$) having 0.5-oz copper cladding. The experimental results are compared to data obtained using the finite-difference time-domain (FDTD) method for validation. The results of the CPS discontinuities studied above indicate potential applications in the emerging wireless communications industry in general, and in the design of low-cost uniplanar microwave circuits such as filters, mixers, and antennas in particular. This has been demonstrated by fabricating bandstop filters using CPS discontinuities. The performances of a few of these filters are presented. Here too, the measured filter response is compared with the results obtained by modeling the filter using the FDTD technique.

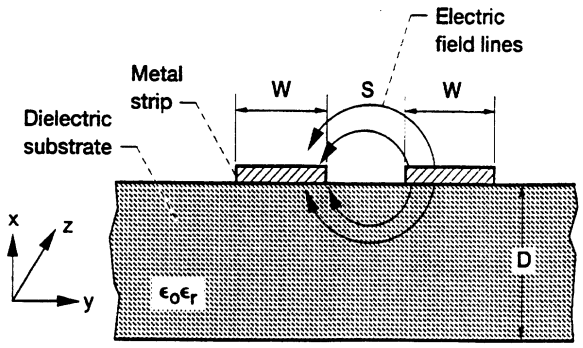


Fig. 1. Cross section of CPS.

II. Theoretical and Experimental Characterization

In a CPS [1], the electric-field lines from the strip conductors of width W extend across the slot of width S. The CPS is supported on a thin dielectric substrate of relative permittivity ϵ_r and thickness D, as shown in Fig. 1. This paper presents the study of several CPS discontinuities (see Figs. 2, 7, 9, 11, and 13) which find use in monolithic microwave integrated circuits (MMIC's). The study is performed both theoretically as well as experimentally and the two sets of results are compared for validation purposes.

A. Experimental Characterization

The measurements have been performed with an automatic network analyzer (HP8510C) using a TRL calibration technique. This technique utilizes on-wafer standards along with a pair of ground-signal RF probes [5]. The standards consist

Manuscript received December 5, 1996; revised June 20, 1997. This work was supported by the Office of Naval Research.

K. Goverdhanam and L. P. B. Katehi are with the Radiation Laboratory, University of Michigan, Ann Arbor, MI 48109-2122 USA.

R. N. Simons is with the NASA Lewis Research Center, NYMA Group, Cleveland, OH 44135 USA.

Publisher Item Identifier S 0018-9480(97)07107-X.

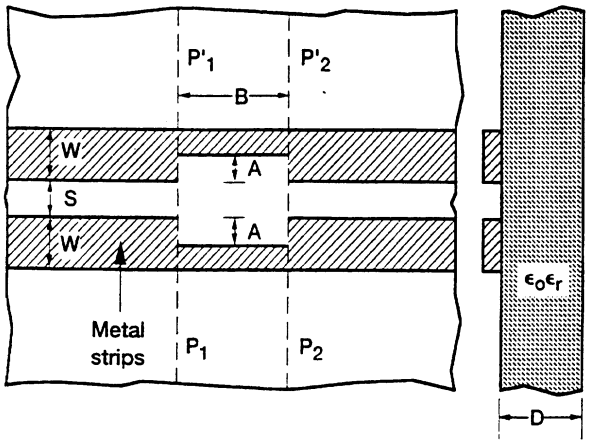


Fig. 2. Symmetric transverse slit and a step in the CPS strip conductors.

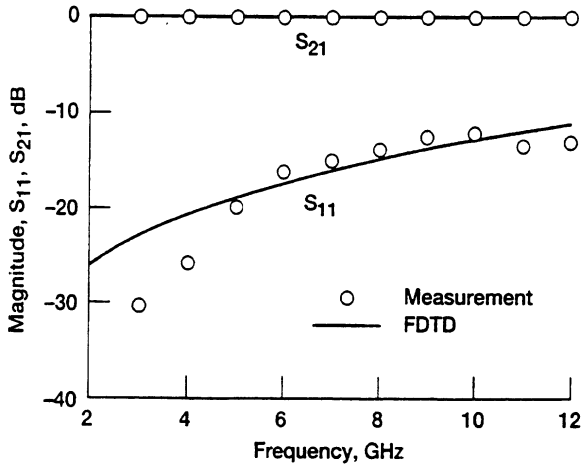


Fig. 3. Experimental and FDTD modeled magnitude of S_{11} and S_{21} for CPS slit. $A = 531.9$ μm, $B = 180.3$ μm.

of a CPS thru, a CPS short circuit, and a CPS delay line. The network analyzer is calibrated using National Institute of Standards and Technology (NIST) de-embedding software.[1] The reference impedance is set by the characteristic impedance Z_o of the delay line.

B. Theoretical Modeling

As mentioned above, the modeling was performed using the FDTD method, [6]–[9], which is based on expressing Maxwell's curl equations in discretized space and time domains. In order to characterize any planar discontinuity, propagation of a specific time-dependent function is simulated using the FDTD technique. In characterizing the discontinuities mentioned above, a Gaussian pulse was used. The space steps Δx, Δy, and Δz are carefully chosen such that integral numbers of them can approximate the dimensions of the structure. The Courant stability criterion is used to select the time step to ensure numerical stability. It is important to note at this point that the circuit dimensions indicated in the following figures are the actual dimensions after fabrication. However, while performing the FDTD analysis, the exact fabricated dimensions could not be incorporated due to limitations in the uniform discretization adopted in the modeling.

[1] NIST de-embedding software, program DEEMBED, Rev. 4.04, 1994.

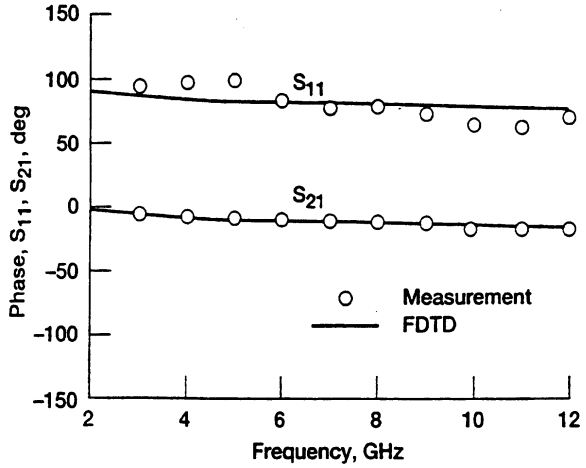


Fig. 4. Experimental and FDTD modeled phase of S_{11} and S_{21} for CPS slit. $A = 531.9$ μm, $B = 180.3$ μm.

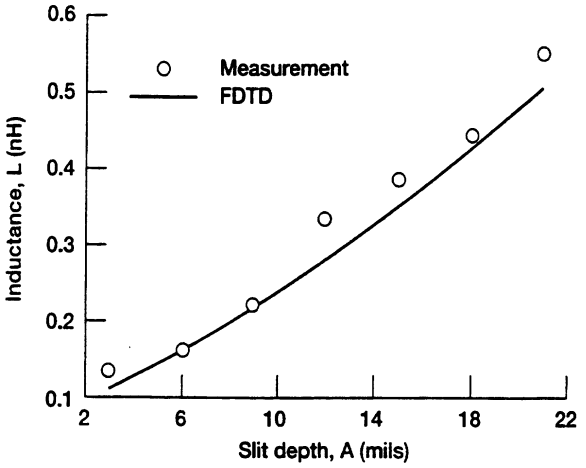


Fig. 5. Inductance determined from the de-embedded S-parameters and FDTD model as a function of slit depth at 9 GHz.

III. Results and Discussion

In the following section, results for a narrow transverse slit on a CPS line, a symmetric CPS step (Fig. 2), a CPS right-angle bend (Fig. 7), a CPS T-junction (Fig. 9), a CPS spur-slot bandstop filter (Fig. 11), and a CPS spur-strip bandstop filter (Fig. 13) are presented. For all the discontinuities considered here the slot width is 101.6 μm and the strip width is 762 μm, unless otherwise specified.

A. Narrow Transverse Slit and a Symmetric Step in the CPS Strip Conductor

A symmetric narrow slit of width B and depth A in the CPS strip conductor is shown in Fig. 2. The slit is modeled as a lumped inductor L located between the planes P_1–P_1' and P_2–P_2' in series with the line. The inductance is determined from the discontinuity S-parameters of the circuit, which are de-embedded from the measured S-parameters of the circuit. Figs. 3 and 4 show plots of the de-embedded and FDTD modeled scattering parameters as a function of frequency for a slit of depth $A = 531.9$ μm and width $B = 180.3$ μm. Fig. 5 shows the series inductance as a function of the slit depth A when the width B is held constant at 180.3 μm. As expected, the inductance increases with the slit depth.

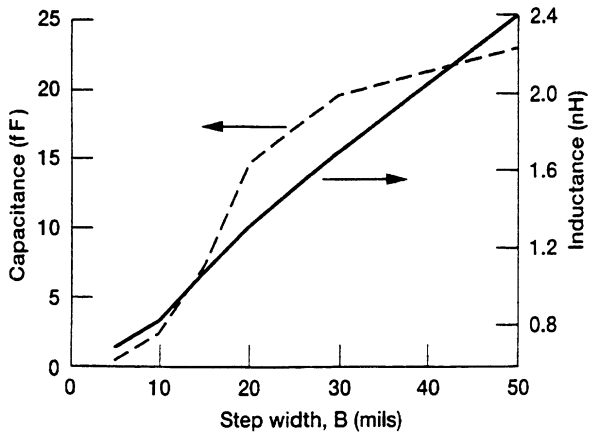


Fig. 6. Lumped fringing capacitance and series inductance determined from the de-embedded measured S-parameters as a function of step width at 6 GHz.

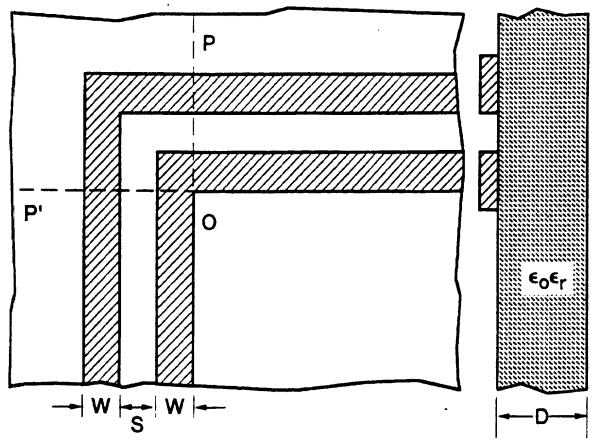


Fig. 7. CPS right-angle bend.

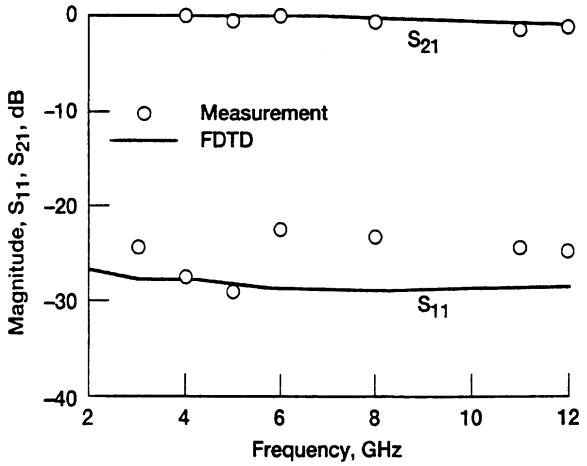


Fig. 8. Experimental and FDTD modeled magnitude of S_{11} and S_{21} as a function of frequency for CPS bend. $S = 101.6$ μm.

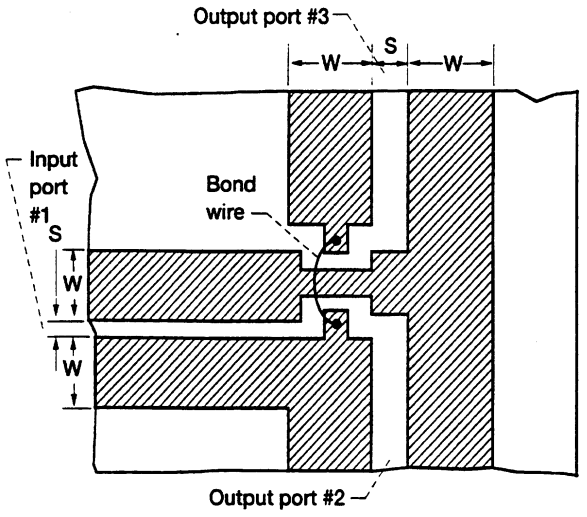


Fig. 9. CPS T-junction.

It would be noteworthy at this point that for small values of the slit width, the discontinuity can be modeled purely as an inductance to a very close degree of accuracy. The slight difference between the measured and FDTD results in Figs. 3–5 can be attributed to the difference in dimensions between the fabricated structure and FDTD model.

However, if the slit depth is kept constant and the slit width B is varied, the discontinuity can no longer be modeled purely as an inductive element. For larger slit widths, the discontinuity which is now a CPS step, needs to be modeled as a π-equivalent LC circuit where the capacitance, C, is the fringing capacitance and the inductance L is the series inductance. Fig. 6 plots the lumped fringing capacitance C and the series inductance L for a CPS step as a function of the step width at a frequency of 6 GHz for a fixed depth A of 533.4 μm. As expected, the capacitance is initially small, increases with step width, and eventually saturates. The measured scattering parameters for a typical slit step has been validated using the FDTD technique and are presented in Figs. 3 and 4. Hence, the FDTD modeling was not repeated for the remaining step widths. Consequently, Fig. 6 excludes the FDTD modeled equivalent lumped-circuit element values.

B. CPS Right-Angle Bend

A CPS right-angle bend is shown in Fig. 7. Several CPS bends have been fabricated with slot width ranging from 110 μm (4.33 mil) to 230 μm (9.06 mil) and the strip width fixed at 762 μm (30 mil). In all cases, it was seen that de-embedded measured S-parameters as well as the FDTD method show the reflection to be of the order of -20 dB or lower. Fig. 8 presents the results for a typical right-angle bend. Hence, it was concluded that compensation of the bend to improve VSWR is not required. This fact is used in the design of a CPS T-junction which follows next where the CPS line is bent at a few places without resulting in any noticeable parasitics due to the bend. Although Fig. 8 indicates low reflection losses for measured as well as modeled cases, it can be seen that the return loss in the case of FDTD modeling is lower. It is also seen that the measured magnitude of S_{21} is slightly lower than the S_{21} obtained by FDTD modeling. These differences can be attributed to the calibration accuracy of the measured results and to the fact that the FDTD scheme adopted here does not take losses into account.

C. CPS T-Junction

A CPS in-phase T-junction is shown in Fig. 9. The measured and FDTD modeled magnitude of S_{11}, S_{21}, and S_{31} as a function of frequency is shown in Fig. 10. As seen from the figure, power is almost equally divided between the output

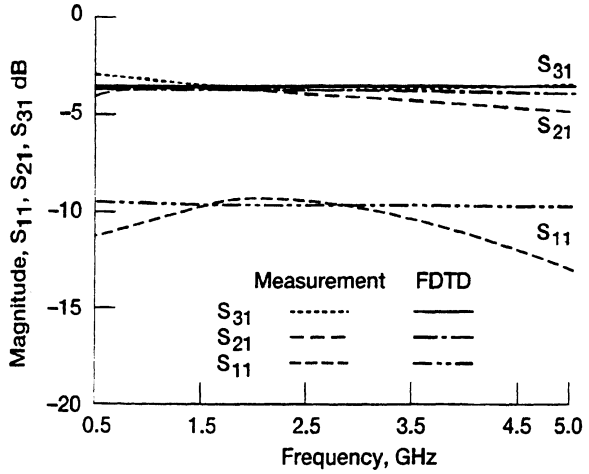


Fig. 10. Experimental and FDTD modeled magnitude of S_{11}, S_{21}, and S_{31} for a T-junction.

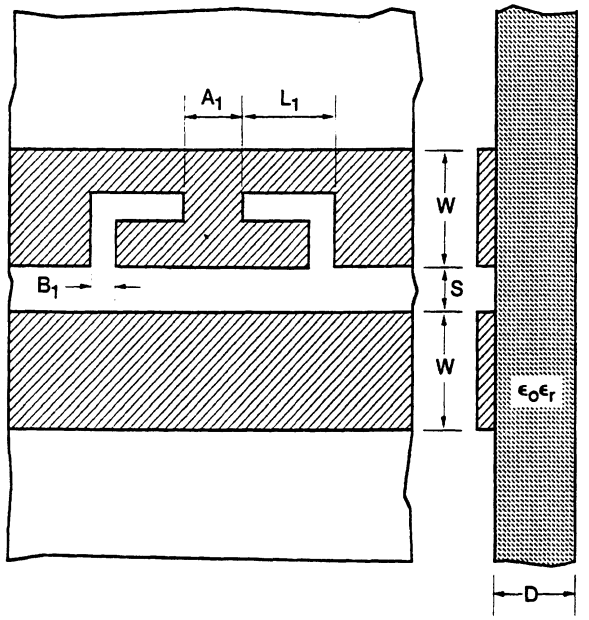


Fig. 11. CPS spur-slot bandstop filter.

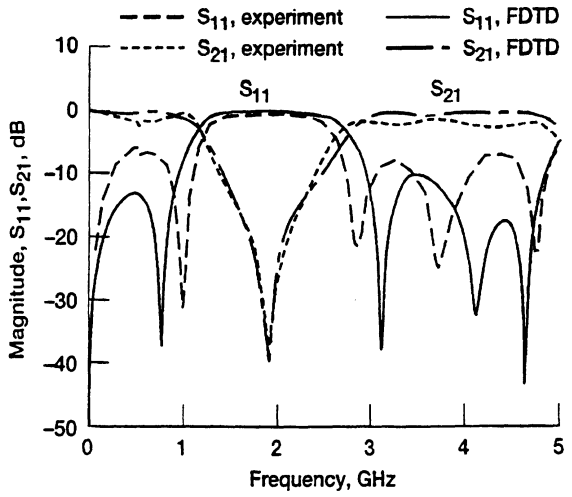


Fig. 12. Experimental and FDTD modeled magnitude of S_{11} and S_{21} for a spur-slot bandstop filter. $A_1 = 762\ \mu$m, $B_1 = 254\ \mu$m, and $L_1 = 16.256$ mm.

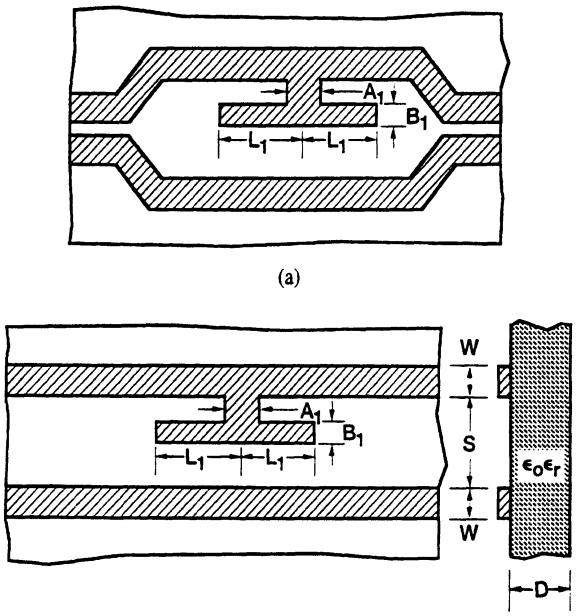


Fig. 13. (a) CPS spur-strip bandstop filter used in the measurement. (b) CPS spur-strip bandstop filter used in modeling.

ports 2 and 3. It was also observed that the phase of S_{31} and S_{21} was equal as expected. From Fig. 10 it is seen that there is a very good agreement between the measured and FDTD modeled power coupled to the two output ports.

D. CPS Bandstop Filters

The configuration of a CPS spur-slot bandstop filter is shown in Fig. 11. The spur-slot is convenient to use when W is large and S is small. It can be modeled as a short-circuit stub of length $L = \lambda_{g(\mathrm{cps})}/4$ in series with the main line. At resonance, the stub prevents the flow of RF power to the load. The measured and modeled S_{11} and S_{21} for the geometry is shown in Fig. 12. On the other hand, the spur-strip is convenient to use when W is small and S is large and can be modeled as two open circuit stubs each of length $L_1 = \lambda_{g(\mathrm{cps})}/4$ in parallel with the main line. Fig. 13(a) shows the configuration of a CPS spur-strip bandstop filter with a taper on either end. This was the configuration for which measurement was performed. Fig. 13(b) shows the configuration that was used to perform the FDTD modeling. Tapers were included in the measurement to accommodate a ground-signal RF probe of 254-μm (10-mil) pitch. However, while simulating the results using the FDTD method, the tapers were eliminated due to memory constraints. Fig. 14 shows the magnitude of measured and modeled S-parameters for the spur-strip filter. From Figs. 12 and 14, we see that there is a good agreement in the measured and modeled resonance frequency for both the filters. However, Fig. 14 shows a slight difference between the measured and modeled S_{21} for the spur-strip filter. This can be attributed to the tapers being excluded in the FDTD modeling. It is interesting to note that the spur-strip filter has a narrower bandwidth compared to the spur-slot filter indicating that the strip filter has a higher quality factor (Q) compared to the slot filter. As a point of interest, it is worthwhile mentioning that a spur-slot with four slots (with the two extra slots being a mirror image of the previous two) has the same resonance as the spur-slot structure in Fig. 11, but a broader bandwidth (lower Q).

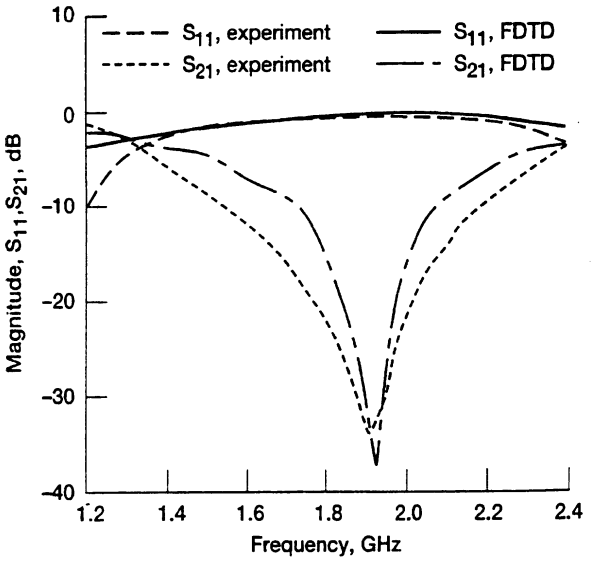


Fig. 14. Experimental and FDTD modeled magnitude of S_{11} and S_{21} for a spur-strip bandstop filter. $A_1 = 254$ μm, $B_1 = 254$ μm, $L_1 = 16.129$ mm, and $S = 762$ μm.

IV. Conclusion

The CPS as a transmission medium holds a great deal of potential because of several advantages, such as excellent propagation, small discontinuity parasitics, and efficient use of the wafer area. In view of these advantages, modeling of some CPS discontinuities which have several technical and commercial applications, was performed as a function of frequency and geometry. Good agreement was found between the experimental and theoretical results.

Acknowledgment

The authors would like to thank Dr. N. Dib for his suggestions and advise.

References

[1] J. B. Knorr and K. D. Kuchler, "Analysis of coupled slots and coplanar strips on dielectric substrate," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 541–548, July 1975.

[2] R. N. Simons, G. E. Ponchak, R. Q. Lee, and N. S. Fernandez, "Coplanar waveguide fed phased array antenna," in *IEEE Antennas Propagat. Int. Symp. Dig.*, vol. 4, Dallas, TX, May 1990, pp. 1778–1781.

[3] R. N. Simons, N. I. Dib, R. Q. Lee, and L. P. B. Katehi, "Integrated uniplanar transition for linearly tapered slot antenna," *IEEE Trans. Antennas Propagat.*, vol. 43, pp. 998–1002, Sept. 1995.

[4] M. Y. Frankel, J. F. Whitaker, and G. A. Mourou, "Optoelectronic transient characterization of ultrafast devices," *IEEE J. Quantum Electron.*, vol. 28, pp. 2313–2324, Oct. 1992.

[5] R. N. Simons, N. I. Dib, and L. P. B. Katehi, "Modeling of coplanar stripline discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 711–716, May 1996.

[6] X. Zhang and K. K. Mei, "Time-domain finite difference approach to the calculation of the frequency-dependent characteristics of microstrip discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1775–1787, Dec. 1988.

[7] K. K. Mei and J. Fang, "Superabsorption—A method to improve absorbing boundary conditions," *IEEE Trans. Antennas Propagat.*, vol. 40, pp. 1001–1010, Sept. 1992.

[8] T. Shibata and H. Kimura, "Computer-aided engineering for microwave and millimeter-wave circuits using the FDTD technique of field simulations," *Int. J. Microwave Millimeter-Wave Comput.-Aided Eng.*, vol. 3, no. 3, pp. 238–250, May 1993.

[9] N. I. Dib, R. N. Simons, and L. P. B. Katehi, "New uniplanar transitions for circuit and antenna applications," *IEEE Trans. Microwave Theory Tech.*, vol. 43, pp. 2868–2873, Dec. 1995.

Kavita Goverdhanam (S'95–M'97) received the B.E. degree in electronics and communication engineering from Osmania University, India, in 1991, the M.S. degree in electrical engineering from Villanova University, Villanova, PA, in 1993, and is currently working toward the Ph.D. degree at the University of Michigan at Ann Arbor, where she is researching time-domain characterization of microwave circuits including time-domain multiresolution analysis and development of novel microwave devices for high-frequency applications.

From 1991 to 1993, she was a Graduate Research Assistant at the Center for Advanced Communications, Villanova University. Since 1993, she has been with the Radiation Laboratory, University of Michigan at Ann Arbor, as a Graduate Student Researcher.

Ms. Goverdhanam was the recipient of the 1985 National Talent Search Scholarship sponsored by the National Council for Education Research and Training (NCERT), India, and was awarded the Outstanding Graduate Student Instructional Assistant Award in 1997 by the American Society for Engineering Education (ASEE), University of Michigan Chapter.

Rainee N. Simons (S'76–M'89–SM'89) received the B.S. degree in electronics and communications engineering from Mysore University, India, in 1972, the M.Tech. degree in electronics and communications engineering from the Indian Institute of Technology, Kharagpur, India, in 1974, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology (IIT), New Delhi, India, in 1983.

In 1979, he joined IIT as a Senior Scientific Officer, where he worked on finline components for millimeter-wave applications and also on the X-band toroidal latching ferrite phase shifters for phased arrays. Since 1985, he has been with the Space Electronics/Communications Division, NASA Lewis Research Center, Cleveland, OH, as a National Research Council Research Associate, and a Senior Engineer with both Sverdrup Technology, Inc., and Nyma, Inc. He is co-author of "Tapered Slot Antennas," a chapter in *Advances in Microstrip and Printed Antennas* (New York: Wiley, 1997).

Dr. Simons has received the Distinguished Alumni Award from his alma mater and several NASA Certificate of Recognition and Group Achievement awards.

Linda P. B. Katehi (S'81–M'84–SM'89–F'95) received the B.S.E.E. degree from the National Technical University of Athens, Athens, Greece, in 1977, and the M.S.E.E. and Ph.D. degrees from the University of California at Los Angeles, in 1981 and 1984, respectively.

In 1984, she joined the faculty of the EECS Department, University of Michigan at Ann Arbor. Since then, she has been interested in the development and characterization (theoretical and experimental) of microwave, millimeter printed circuits, the computer-aided design of VLSI interconnects, the development and characterization of micromachined circuits for millimeter-wave and submillimeter-wave applications, and the development of low-loss lines for Terahertz-frequency applications. She has also been theoretically and experimentally studying various types of uniplanar radiating structures for hybrid-monolithic and monolithic oscillator and mixer designs.

Dr. Katehi is a member of the IEEE Antennas and Propagation Society, Microwave Theory and Techniques Society, Sigma XI, Hybrid Microelectronics, URSI Commission D, and a member of IEEE Antennas and Propagation Society ADCOM from 1992 to 1995. She also serves as an Associate Editor for the IEEE Transactions on Microwave Theory and Techniques. She has been awarded the IEEE Antennas and Propagation Society W. P. King (Best Paper Award for a Young Engineer) in 1984, the IEEE Antennas and Propagation Society S. A. Schelkunoff Award (Best Paper Award) in 1985, the NSF Presidential Young Investigator Award, an URSI Young Scientist Fellowship in 1987, the Humboldt Research Award, the University of Michigan Faculty Recognition Award in 1994, and the IEEE Microwave Theory and Techniques Society Microwave Prize in 1996.

High Frequency Circuit Components on Micromachined Variable Thickness Substrates

Rhonda F. Drayton[1], Rashaunda M. Henderson[2], and Linda P. B. Katehi[2]

Department of Electrical Engineering and Computer Science

[1] The University of Illinois at Chicago, 851 S. Morgan (M/C 154), Chicago, Illinois, 60607

[2]The Radiation Laboratory, The University of Michigan, 1301 Beal Avenue, Ann Arbor, MI 48105

Index — micromachining, planar circuits, packaging

Abstract — This work presents the use of Si micromachining techniques to enhance high frequency planar circuit design flexibility by offering a method for varying the substrate thickness in selective locations on the wafer.

1.0 INTRODUCTION

Micromachining is being used for a number of high frequency applications to meet design requirements for compact circuits, high performance interconnect lines, monolithic packaging as well as novel array configurations feeding networks [1]. During the development of such technologies for use in low frequency applications, materials parameters such as size and thickness have been standardized in order to meet demands for high volume low cost circuits. A beneficial result is the use of established infrastructures and less expensive materials that can be integrated into circuit designs for high frequency applications. For example, in many complex MMIC designs requiring planar circuits and antennas, a critical design parameter for both components is the substrate thickness which depends on the transmission line topology selected. In particular, as active and passive elements are integrated into a single chip along with radiating elements, the selection of an optimal substrate thickness that offers overall high performance for each component function becomes impossible. Therefore, novel fabrication approaches that address this issue are necessary in order to satisfy design requirements for complex high performance circuits.

Presented herein is a micromachining methodology that extends flexibility to the design of circuits or radiating elements by allowing for local reduction of the substrate thickness in order to achieve excellent component performance. This concept is illustrated through the use of a simple transmission line that is implemented in a full thickness wafer environment with thickness reduction along the feedline.

2.0 CIRCUIT DESIGN /FABRICATION APPROACH

Interconnects printed on high index materials suffer from parasitic loss and higher order moding as the operating frequency increases which limits the ability to attain high electrical performance. To improve transmission line propagating conditions (quasi-TEM propagation), a wafer thickness of less than 250 microns is typically required. In applications that include radiating elements, this condition is important, yet contradictory, since optimum efficiency and high gain is achieved in substrate thicknesses on the order of $\lambda_{eff}/10$. As a result of this conflicting design requirement, fabrication processes that extend the circuit designer's capability to provide optimum electrical interaction between the feedline interconnects and other components offers major benefits. One solution to the design problem posed here is to selectively reduce the thickness of the wafer in specific interconnect locations that may be used to feed a radiating element. As an example, a micromachined packaged antenna is shown in [2] with a reduced thickness feedline interconnect to a microstrip patch antenna. In this letter, approach and implementation of micromachined microstrip lines printed on selectively reduced thickness regions is discussed.

The micromachined reduced thickness line offers two features, a reduced thickness region and a lower package under the microstrip line. The reduced substrate is formed by partially removing silicon from underneath the feedline while the lower package (see Figure 1) is formed when the material is completely removed in adjacent regions [3]. In this work, high resistivity silicon (3000 ohm-cm) with dielectric layers of $SiO_2/Si_3N_4/SiO_2$ is used and a bulk micromachining process based on anisotropic etching techniques [4] such as ethylene diamine pyrocatechol (EDP) is employed. First, the desired circuit is printed on the upper surface using standard lithography techniques. Next, three adjacent regions are defined on the bottom of the wafer to form the lower package and reduced thickness region (Figure 2-a). In the outer channels, which form the package, all dielectrics are removed (Figure 2-b) while a single protective oxide layer remains in the center conducting line region (CC). The outer channels are time-etched until 80% of the wafer thickness (Figure 2-c) has been reduced prior to removing the final oxide masking layer from underneath the center region (Figure 2-d). The center is then etched down 170 microns to reduce the conducting region substrate thickness while the outer channels are simultaneously etched entirely away (Figure 2-e). After removing the dielectric layers on the bottom of the wafer, a 1.5 micron metal layer of Ti/Al/Ti/Au is evaporated in order to provide metal continuity on the lower surface.

3.0 Measured Results

Measured data is obtained from an HP 8510C Network Analyzer and Alessi probe station with Picoprobes. A coplanar waveguide to microstrip transition is used with conductor and slot widths of 180 and 210 microns. The outer ground planes on the top side of the wafer are 380 microns away from the microstrip line to ensure microstrip mode of propagation. Figure 3 shows the calculated values of the effective dielectric constant for a thru line in the open and packaged configuration based on modeled [5] and measured data. In the case of the line printed on the thick substrate, there is close agreement between the measured and the decrease in dielectric constant can be attributed to the presence of conductor and dielectric losses not accounted for in the model. When the line becomes packaged, the slope of effective dielectric constant reduces indicating less frequency dependence and the effective dielectric constant is reduced.

4.0 Conclusion

A micromachined variable thickness through line interconnect has been developed. In this approach, micromachining has been used to custom design the substrate thicknesses in order to improve the performance of heterogeneous circuit components on the same wafer.

5.0 Acknowledgements

This work was supported by the Army Research Office and the Office of Naval Research.

References

[1] I. Papapolymerou, R. F. Drayton, and L. P. B. Katehi, "Micromachined Patch Antennas," submitted to *IEEE Transactions on Antennas and Propagation*, July 1996.

[2] Rhonda Franklin Drayton, Rashaunda M. Henderson, and Linda P. B. Katehi, "MTT-96 Conference paper", presented at the 1996 International Microwave Conference in San Francisco, CA, June 1996.

[3] Rhonda Franklin Drayton and Linda P. B. Katehi, "Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 9, pp. 2073-2080, September 1995.

[4] K. E. Bean, "Anisotropic Etching of Silicon," *IEEE Transactions on Electron Devices*, Vol. ED-25, No. 10, pp 1185-1193, October 1978.

[5] HP Microwave Design System.

LIST OF FIGURES

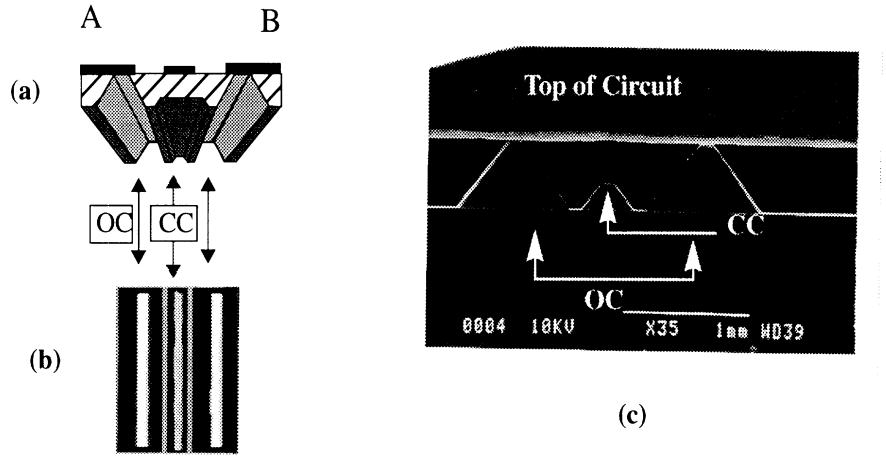


Figure 1 (a) Micromachined Variable Thickness Feedline cross-section (A-B), (b) Photograph of bottom view illustrates with outer channels (OC) and center conductor channel (CC), and (c) SEM photograph of circuit cross-section.

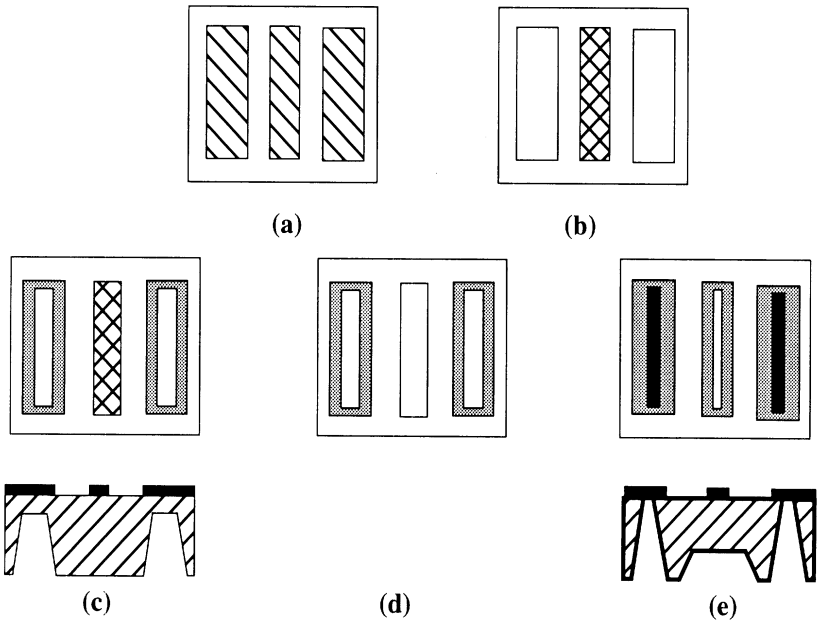


Figure 2 Fabrication Process (see description in text) for lower wafer development.

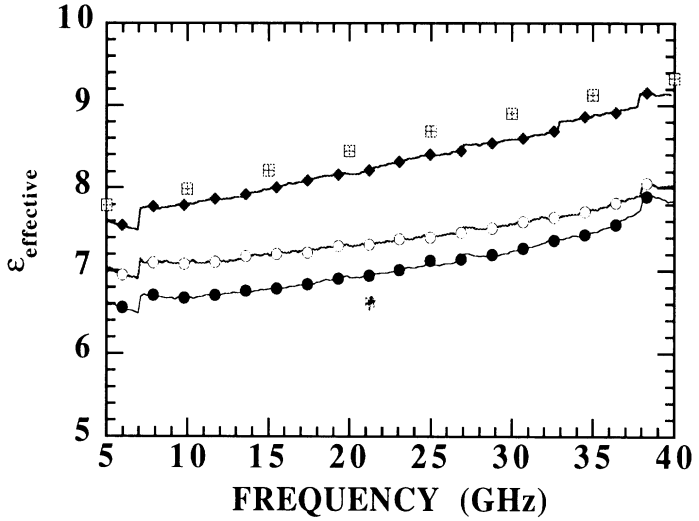


Figure 3 Microstrip effective dielectric constant for modeled data of open line on thick substrate (squares); measured data for open line on thick substrate (diamonds), micromachined lower shield (open circles), and micromachined completely shielded line (filled circles).

Monolithic Packaging Concepts for High Isolation in Circuits and Antennas

[1]Rhonda F. Drayton, [2]Rashaunda M. Henderson, and [2]Linda P. B. Katehi

[1]The Department of Electrical Engineering and Computer Science
The University of Illinois at Chicago Illinois 60607, USA
Ph: (312) 996-6495 Fax: (312) 413-0024
E-mail: drayton@eecs.uic.edu

[2]The Radiation Laboratory
The Department of Electrical Engineering and Computer Science
The University of Michigan, Ann Arbor, MI 48109, USA
Ph: (313) 647-1796 Fax: (313) 647-2106
E-mail: katehi@eecs.umich.edu

Abstract — **High frequency planar circuits experience large electromagnetic coupling in dense circuit environments. As a result, individual components exhibit performance degradation that ultimately limits the overall response of circuits. This study addresses cross-talk in planar microstrip lines by evaluating micromachined packages as a means to reduce this mechanism. Microstrip lines with straight and meandering paths can exhibit cross-talk coupling as high as -20 dB (i.e. when placed in a side-by-side arrangement). From our study, inclusion of a monolithic package reduces this effect by as much as -30 dB and consequently offers the requisite electrical and environmental protection as well as shielding of individual elements from parasitic radiation. This paper presents the development of the micromachined package for microstrip geometries, offers a discussion on cross-talk between straight and bending geometries in open and packaged configurations, and provides an evaluation of noise characteristics of the package. A packaged antenna element is also included as a demonstration of the potential use of micromachined packaging in array applications.**

I. Introduction

In high frequency applications, planar circuits and antennas are an integral part of high performance communication system design due to low cost, light weight, and small size. While low-power performance has been the major thrust issue for promoting technology growth in this area, another significant

attribute is the unlimited capability for miniaturization, which is extremely important in view of the demands to reduce entire systems onto a single chip that offer high levels of functionality. Higher frequencies of operation inherently reduce circuit size. This fact, coupled with the planar nature of these circuits, also increases the design flexibility in high density packaging of passive and active elements in semiconductor environments, such as silicon or GaAs. Cross-talk, however, is one critical performance issue that is common to most high density circuit layouts and occurs when circuits are located in close proximity to each other. Furthermore, electromagnetic (e-m) signal propagation is sensitive to this type of coupling (i.e. substrate mode or parasitic) and results in degraded electrical performance of the circuit.

In the past, several approaches have been taken to understand and minimize cross-talk interactions between planar circuits. For example, numerical models have been developed to predict the appropriate placement of planar circuit geometries that produce the least interactions [1]. In this case, coupling reduction as the highest priority is achieved, but optimization of size, placement, and space utilization are not considered. In another, packaging methods were developed to reduce coupling by separating different circuit functions into modular components similar to multi-chip module (MCM) approaches. By decomposing large systems into smaller units [2], interactions between different circuit functions are reduced. While this is an effective approach for large scale integrated (LSI) circuits, this approach does not address e-m field interactions within a given circuit layout that can be difficult to control and are known to cause degradation in the overall circuit performance.

Addressed in this study is cross-talk between two types of microstrip lines: straight and meandering that represent fundamental building blocks to high density interconnects and phased array applications. Therefore, the objectives of this work are: (1) to develop low-cost package solutions for microstrip lines; (2) to study the cross-talk behavior associated with open and packaged geometries; (3) to assess the noise associated with monolithic packages; and (4) to demonstrate the integration of a package with planar elements common to array applications.

II. Design Considerations

Microstrip, a popular transmission line type in high frequency circuits and antennas, offers many advantages for compact circuit miniaturization. In addition to the small size, low profile, and ease in conform-

ability, there are an abundant supply of circuit design models and simulation tools readily available for a designer's use. In this study, the crosstalk between straight and meandering microstrip lines is addressed by evaluating the e-m coupling found in different layouts and comparing them to the coupling found in an open and packaged configuration. The packaged configurations in this case are developed using Si micromachining technology [3] to produce monolithic conformal packages that follow the shape of individual planar elements being protected.

The following discussion on cross-talk is based on two circuit design configuration variables: (1) cross-section topology and (2) design layout. The cross-section topologies of interest are (a) open or (b) packaged (see Figure 1) geometries for the conventional and micromachined packaged microstrip lines, respectively. In each case, design parameters for 50 ohm lines are obtained, where open structures are based on commercially available CAD tools [4] and packaged ones on in-house CAD tools [5]. Each topology is then evaluated based on a combination of two adjacent microstrip lines, a straight thru line and a single section meander. The single section meander consists of a back-to-back right angle bend and will be referred to as a U-shaped line in the remainder of the paper. The two arrangements, shown in Figure 2, result in *Design Layout A*, which consists of a thru line and a U-shaped line and *Design Layout B*, which consists of two U-shaped lines.

To address the use of these structures in antenna arrays, consideration is also given to design criteria for high performance planar antennas and miniaturization of drive electronic circuitry. In high index materials, optimum performance is achieved when substrates modes are minimized or suppressed. In microstrip patch antennas, this occurs when the substrate is electrically thick, whereas in planar circuits, this occurs when the substrate is electrically thin. Hence, it is difficult to satisfy both criteria in high index semiconductor materials. With the use of Si micromachining, however, both thick and thin substrate regions can be defined such that the antenna can be printed on the thick material while the distribution lines and circuitry are printed on the thin material regions.

The fabrication approaches described herein will address both the packaging issues related to the microstrip line and the thickness reduction issues required to selectively etch regions in planar circuit layouts. Next, cross-talk and noise measurements will be discussed for close proximity circuit interactions

and micromachined packaging. Finally, the assessment of cross-talk coupling found in the various micromachined layout configurations will be presented.

III. Fabrication

A. Overview

The microstrip lines discussed are packaged using the micromachining approach developed in earlier work [6] for coplanar waveguide structures. To provide package grounding and equalization between the upper and lower cavity in microstrip based geometries, ground planes are positioned sufficiently far (380 microns) from the conductor in order to maintain a microstrip mode of propagation (see Figure 3 for dimensions). The general process is similar to one described in [6], where wet anisotropic etchants are used to develop the desired geometry. The protective dielectric layer in this case is a silicon oxide layer (7800 Å) on the upper cavity wafer and a membrane[1] dielectric layer (1.5 micron) on the lower circuit wafer. The wafer resistivity is 4 Ω-cm in the upper wafer and greater than 2000 Ω-cm in the lower wafer. Microstrip metallization thickness is 3 microns of electroplated gold and the package metallization is 1.5 microns of evaporated metal (Ti/Al/Ti/Au @ 500/15K/500/3K Å). Once the package is assembled, it is attached to a support wafer (with similar metallization) using silver epoxy in order to place it on the vacuum holes of the probe station wafer chuck. As an alternative, electrobonding techniques could also be used to secure the two wafers.

B. Substrate Thickness Reduction And Conformal Packaging Approach

Two fabrication methods were developed that allow for (a) selective reduction of the wafer thickness and (b) realization of convex corners around bends in the upper and lower cavity conformal packages. Wafer thickness reduction requires the use of a two step etch process to accommodate the deep etch requirement of the vias and package channels as well as the shallow etch requirement for the reduced thickness regions. First the vias and channels are etched several hours to remove approximately 400

1. A membrane is defined as silicon dioxide/silicon nitride/silicon dioxide layer (3500/4500/7500 Å).

microns of material while the reduced thickness regions remain protected. Then, these protected regions are opened and etched an additional 2 hours to remove 170 microns of material while the via and lower package channels are etched entirely through. In Figure 3, a scanning electron microscope (SEM) picture is shown of an inverted lower cavity package with a cross-section view of a via and a lower package cavity. Extensive details of the process are described in [7].

Conformal packages can be used to optimize space utilization in the development of high density circuits. Several challenges must be addressed, however, when implementing a conformal package around lines that exhibit curves and bends. In Figure 4, a top and bottom view of the circuit and cavity geometries for the U-shaped lines are illustrated. In this arrangement, the corners of the package are potential candidates for severe rounding during the wet etch process as a result of undercutting. Since wet anisotropic etchants selectively attack the various crystal planes at different rates, it is difficult to achieve a good etch stop in the absence of orthogonal planes without the use of adequate compensation.

Researchers, Bean and Abu-Zeid, discuss the use of anisotropic etching and corner etching issues in [8] and [9], respectively. A corner can be classified as concave[1] or convex[2] as seen in Figure 5. Wu found that convex surfaces are bounded by the fastest etching planes while concave corners are bounded by the slowest etching planes [10]. As a result, concave corners are easily formed without undercutting and convex corners typically exhibit undercutting that can only be reduced with the incorporation of appropriately sized compensation geometries located at the respective corners.

The compensation geometries used herein are squares and are implemented by centering each appropriately sized squares onto a convex corner (Figure 6). Through an iterative process, the best compensation square dimensions were found to be approximately 1.4 times the desired etched depth to produce the corners seen in the upper cavity package of Figure 5. Since a two-step etch is used to form the package, via, and reduced thickness regions, the U-shaped geometries require two sets of convex corner compensation squares to produce desirable corner shape (See Figure 7). Each is designed to accommodate the final depth requirements for the deep (550 micron) and shallow (170 micron) regions in the conformal package[3]. This

1. Convex (inside) corners are formed when two (110) crystal planes intersect to produce an interface that points inward.
2. Concave (outside) corners are formed when two (110) crystal planes intersect to produce an interface that points outward.
3. Maximum etch time in the two-step procedure should not exceed the time required to etch the deepest region. In this work, 12 hours is the maximum allowable etch time.

requirement is necessary in order to reduce the severity of undercutting observed in Figure 8 underneath the conducting line.

IV. Performance

A. Testing Method and Noise Definition

To accurately characterize the packaged planar design, s on-wafer measurement techniques are used that require coplanar waveguide based GGB PicoProbes (150 micron pitch), an Alessi High Frequency Probe Station, and an HP 8510C Network Analyzer. The test probes are de-embedded from the measurement data using a Short-Open-Load-Thru (SOLT) calibration even though LRM or TRL calibration methods could have been chosen. To excite the microstrip line, a coplanar-to-microstrip transition is implemented and is shown in Figure 2. The performance of the open and packaged circuits is determined by measuring scattering parameters which are used to describe the electrical characteristics of each line. Coupling mechanisms associated with different circuit layouts are evaluated and then compared to the minimum reference noise value of the packaged system. Since several circuits were fabricated in this study, some data will reflect an average value and will be indicated by "avg." in the plots.

Two types of noise are defined in this work: (1) non-contact and (2) contact. The non-contact noise is defined as the response when the probes are elevated above the circuit surface by 15 mm with a separation distance of 8.382 mm. This amount is identical to the separation found in the two U-shaped circuits in Design Layout B. The contact noise, which reflects an average value of different measurements, is defined as the excitation of a circuit at one port and the detection of transmitted signals in the package structure at different locations atop the circuit package (see Figure 9). In this measurement random propagating signals are detected on the upperside of the package by placing the probe near the opening of the cavity ports in order to determine the maximum noise contribution from the packaged configuration. Figure 10 shows a comparison between the contact and non-contact noise measurements and indicates a strong similarity between the measurements even though the contact noise tends to be slightly higher between 20 and 30 GHz by 10dB.

B. Electrical Characterization And Isolation

Section B.1 presents a discussion on the electrical response of the circuits in Design Layout A and B which correspond to open microstrip and micromachined packaged configurations, respectively. Measured data for the insertion loss are shown, total loss calculations are determined for each circuit type, and comparisons are made to identify the amount of radiation generated in each layout type. Section B.2 focuses on the measured cross-talk in the two layouts, where emphasis is placed on the interactions observed in the open and packaged configurations with comparisons made between the circuit layouts and noise of the system.

B.1 Circuit Characterization

The performance of the straight delay line (13.392 mm) and the U-shaped bend (13.392 mm) in an open environment are compared in Figure 11. In the lower frequency range, the insertion loss is similar for both lines. As the frequency of operation increases above 15 GHz, however the U-shaped lines radiate at the corner generating substrate modes. The increasing insertion loss causes the signal to begin to exhibit an oscillating effect above 30 GHz. From the calculated total loss ($1-|S11|^2-|S12|^2$), the U-shaped line can be as high as 65%, which is more than double the loss associated with the straight delay line.

A similar comparison is made between the open and packaged bend design. As frequency increases, the open bend performance degrades rapidly due to parasitic radiation as seen in Figure 12 for the insertion loss and total loss of the open and packaged bend. By comparison, the packaged bend has a much flatter response in the total and insertion loss data. Even though these values are slightly higher than those observed in the straight delay line, the overall performance is much better compared to the open U-shaped circuit. The higher loss in this case is associated with the additional ohmic loss introduced by the top metallization of the package. Radiation from the bend, on the other hand, has been eliminated in the packaged U-shaped design and shows similar total loss calculations to a straight line of similar length (see Figure 13).

B.2 Cross-Coupling and Circuit Isolation

In Figure 14, the open microstrip structure has coupling as high as -20 dB in the mid-range for Design Layout A and even higher coupling near -10 dB at frequencies above 25 GHz in Design Layout B. These results indicate coupling levels have a strong dependence on layout configuration. Similar coupling measurements have been performed on the packaged versior of Design Layout B. In Figure 15, the inclusion of a lower package cavity into the design decreases the cross-coupling substantially by approximately 20 dB. With a complete package that includes upper and lower cavities, an additional 10 dB reduction is observed. These results demonstrate that advanced monolithic packaging can reduce coupling below -45dB, which is in close agreement to the non-contact noise measurement observed earlier when the probes were suspended in air. In Figure 16 the contact noise and the packaged design show similar coupling up to 33 GHz. Above this value, the increased coupling in the contact noise measurement is associated with leakage that occurs at the input and output ports of the packaged line.

C. Single Antenna Element

In Figure 17, a patch antenna is demonstrated in a packaged feedline configuration. In a top view illustration of the antenna element, Figure 17b, a portion of the microstrip feedline is printed on a reduced thickness substrate region. Two ground pads are also printed on the circuit surface for bonding and package ground plane equalization. The package includes a window for the antenna element that has dimensions of 8.731 mm by 6.935 mm, which has a spacing of five times the substrate height (5h) between the window and antenna edge. This value ensures minimum interactions between the antenna radiation pattern and the package.

The performance of the open and packaged design is shown in Figure 18. The packaged antenna shows noticeable increase in bandwidth, approximately 110% for SWR <1.8, compared to the open design. This suggests that the packaged antenna efficiency is increased and that the propagation in the feedline is less sensitive to the resonant frequency of the antenna due to improved TEM propagation characteristics (β, Z_o) of the line on the reduced thickness region. This demonstration, therefore, indicates the potential for extending advanced packaging concepts to planar antenna array applications.

V. Summary

This paper demonstrates the substantial benefits of using advanced monolithic packaging concepts in planar circuit and antenna design. Specifically, we have demonstrated that electromagnetic coupling and parasitic radiation in high speed circuit interconnects and antenna feed networks can be eliminated by selectively packaging sections of planar circuits. The package development is based on Si micromachining and can be implemented with standard IC processing techniques required to develop complex circuits. Advanced packages also offer significant performance improvements to circuits that exhibit high radiation. Furthermore, these packages reduce circuit interactions between high density interconnects and offer coupling levels that are comparable to the overall noise found in the packaged system. As a result, these findings show that monolithic packages are very feasible for developing high isolation in distribution lines and feeding networks commonly used in high-speed interconnect and antenna array applications.

VI. Acknowledgements

This work was supported by the Army Research Office and the Office of Naval Research.

VII. References

[1] W. P. Harokopus, Jr. and Pisti B. Katehi, "Characterization of Microstrip Discontinuities on Multi-layer Dielectric Substrates Including Radiation Loss," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 37, No. 12, December 1989.

[2] D. E. Hackaman et. al, "WAFFLELINE- A Packaging Technique for Monolithic Integrated Circuits," *IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest*, pp. 59-62, 1984.

[3] K. E. Petersen, "Silicon as a Mechanical Material," *Proceedings of the IEEE*, Vol. 70, No. 5, pp. 420-457, May 1982.

[4] Hewlett Packard, EESOF Libra Software.

[5] N. Dib and L. Katehi, "Modeling of Shielded CPW Discontinuities Using the Space Domain Integral Equation Method (SDIE)," *Journal of Electromagn. Wave Appl.*, Vol.5, No. 4/5, 1991, pp. 503-523.

[6] Rhonda Franklin Drayton and Linda P. B. Katehi, "Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 9, pp. 2073-2080, September 1995.

[7] R. F. Drayton, R. M. Henderson, and L. P. B. Katehi, "High Frequency Circuit Components on Micromachined Variable Thickness Substrates," *IEE Electronics Letters*, Vol. 33, No. 4, pp. 303-304, 1997.

[8] K. E. Bean, "Anisotropic Etching of Silicon," *IEEE Transactions on Electron Devices*, Vol. ED-25, No. 10, pp 1185-1193, October 1978.

[9] Abu-Zeid-Corner and M. M. Abu-Zeid, "Corner Undercutting in Anisotropically Etched Isolation Contours," *J. Electrochem. Society*, Vol. 131, No. 9, pp.2138-2142, September 1984.

[10] Xian-Ping Wu and W. H. Ko, "Compensating Corner Undercutting in Anisotropic Etching of (100) Silicon", *Sensors and Actuators*, Vol. 18, pp. 207-215, 1989.

BIOGRAPHIES

Rhonda Franklin Drayton received the B.S.E.E. in 1988 from Texas A&M University, College Station, Tx. and both M.S.E.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI in 1990 and 1995 respectively. She is currently an Assistant Professor in the EECS Department at the University of Illinois at Chicago.

Her current research interests include development, fabrication and characterization of high frequency circuits and antennas for microwave and millimeter wave applications based on micromachining techniques as well as packaging of electronic/optoelectronic circuits.

She received First Prize for the Best Student Paper at the 1994 IEEE MTT-S International Microwave Symposium and the 1997 Amoco Silver Circle Award for Teaching Excellence from University of Illinois at Chicago.

Rashaunda M. Henderson received the B.S.E.E. degree from Tuskegee University, Tuskegee, AL in 1992 and the M.S.E.E. degree from The University of Michigan, Ann Arbor, MI in 1994. She is currently pursuing a Ph.D. in electrical engineering at The University of Michigan. Her research interests involve the experimental characterization and development of packages for high frequency circuits using silicon micromachining techniques. She has affiliations in IEEE, NSBE, and Eta Kappa Nu.

Linda P.B. Katehi received the B.S.E.E. degree from the National Technical University of Athens, Greece, in 1977 and the M.S.E.E. and Ph.D. degrees from the University of California, Los Angeles, in 1981 and 1984 respectively. In September 1984 she joined the faculty of the EECS Department of the University of Michigan, Ann Arbor. Since then, she has been involved in the development, modeling, fabrication and experimental characterization of millimeter and near-millimeter wave monolithic circuits and antennas.

She has been awarded with the IEEE AP-S W. P. King Award in 1984, the IEEE AP-S S. A. Schelkunoff Award in 1985, the NSF Presidential Young Investigator Award and an URSI Young Scientist Fellowship in 1987 and the Humboldt Research Award in 1994. She is an Associate Editor of the IEEE Antennas and Propagation Society, and Radio Science. She is a Fellow of IEEE, member of the IEEE AP-S, MTT-S, Sigma XI, URSI Commission D and an elected member of the IEEE Antennas and Propagation Society Administrative Committee.

FIGURES

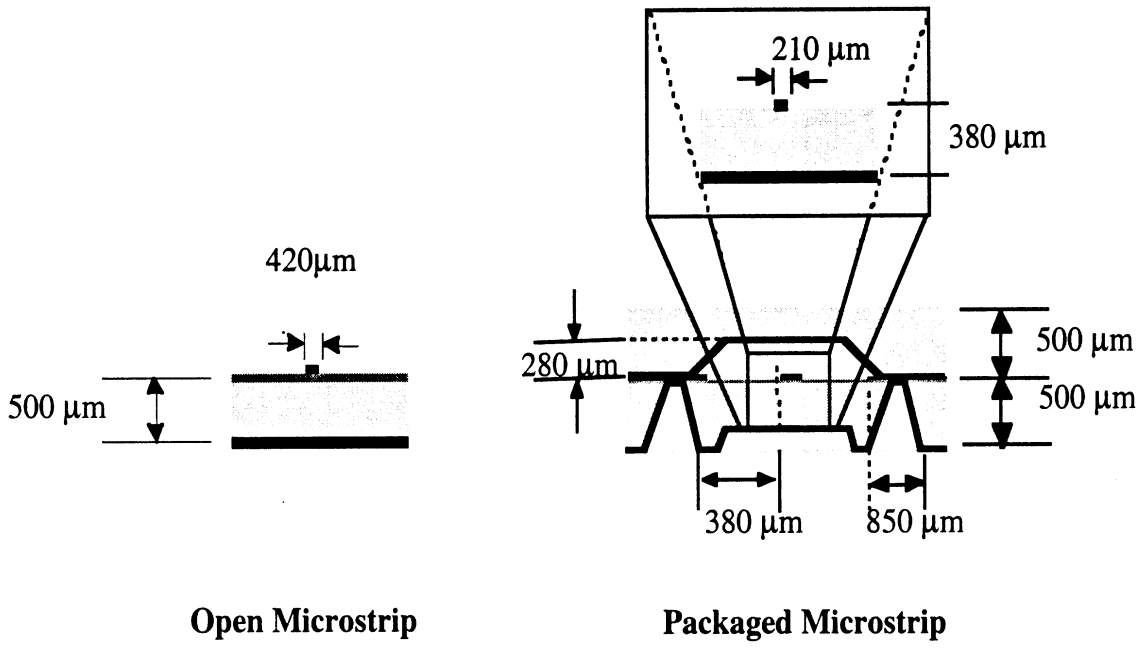


Figure 1. Circuit Topology: (a) Open Microstrip on full thickness wafer and (b) Packaged microstrip on reduced thickness wafer. The circuits are supported on a membrane dielectric consisting of an oxide/nitride/oxide tri-layer of 4500/3500/7500Å thickness, respectively.

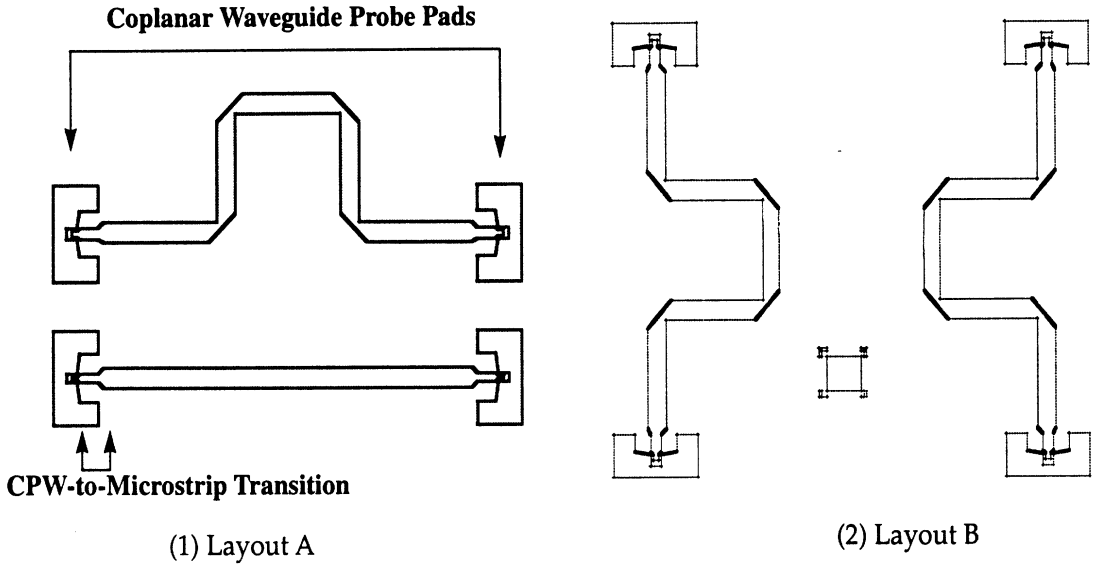
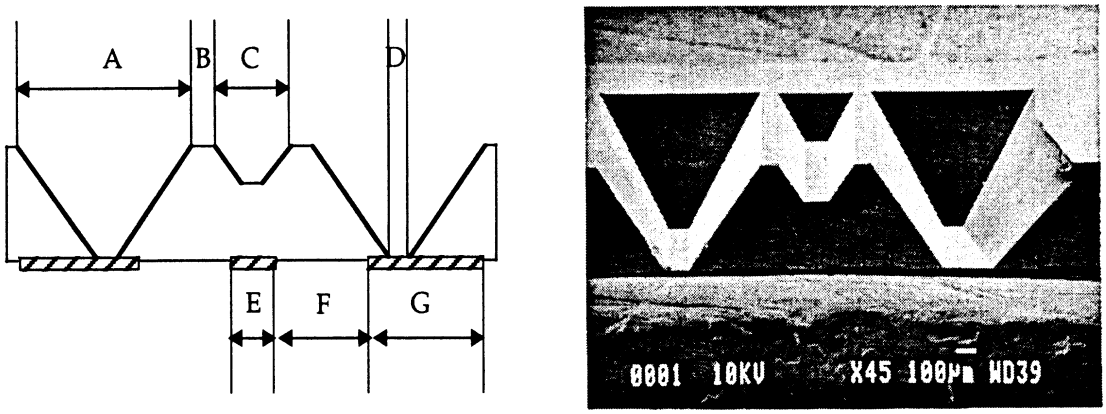
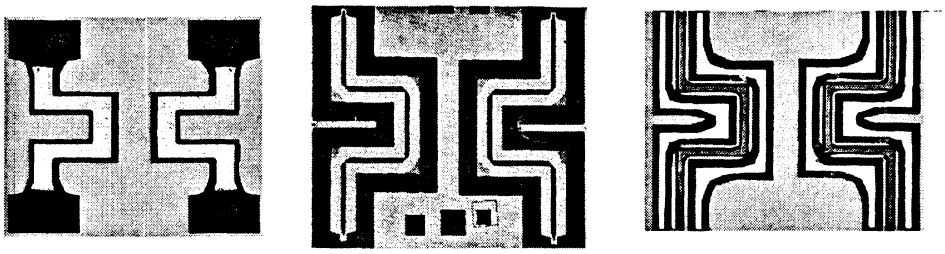


Figure 2. Layout Configurations: (1) Design Layout A: Thru Line and U-shaped (Back-to-Back Right Angle Bend) line and (2) Design Layout B: Two U-shaped lines.



(a) (b)

Figure 3. (a) Front view drawing of a microstrip printed on an inverted lower package with dimensions of A=850, B=100, C=400, D=150, E=210, F=380, G=750 and conductors that are indicated as hashed lines. All dimensions are in microns. (b) SEM photo of the inverted lower package developed during the two-step etch procedure.



(a) Upper Cavity Package (b) Circuit Layout (c) Lower Cavity Package

Figure 4. Micromachined Packaged U-Shaped Bend Circuits. (a) *Upper Cavity Package* with probe windows (shown in black) for testing. (b) *Circuit Layout* of a microstrip line. Conductors appear as the dark color. (c) *Lower Cavity Package* shows reduced thickness region in the center of the U-shaped line and lower package channels in the outer white regions.

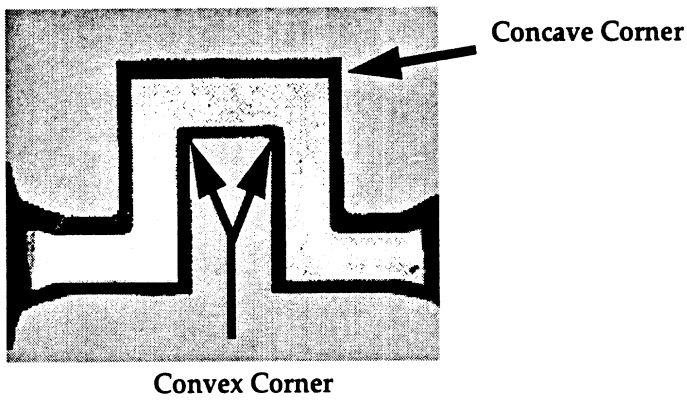


Figure 5. Photograph illustrating of convex and concave corners in the upper cavity of the package.

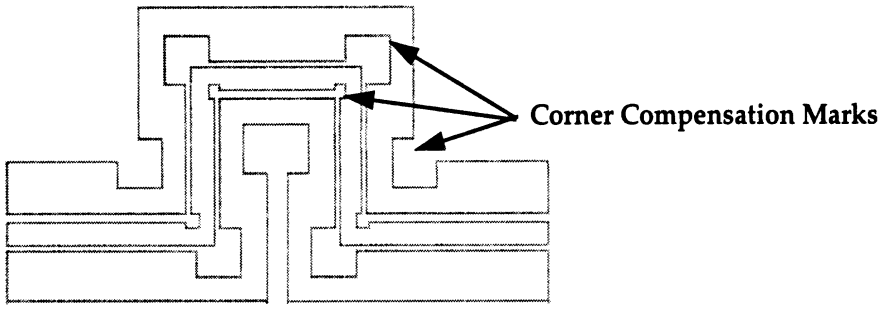


Figure 6. CAD drawing of the mask layout including the corner compensation required for the formation of the conformal package. The large square are located in the outer channels to form the package and the small squares are located in the inner channels of the reduced thickness regions.

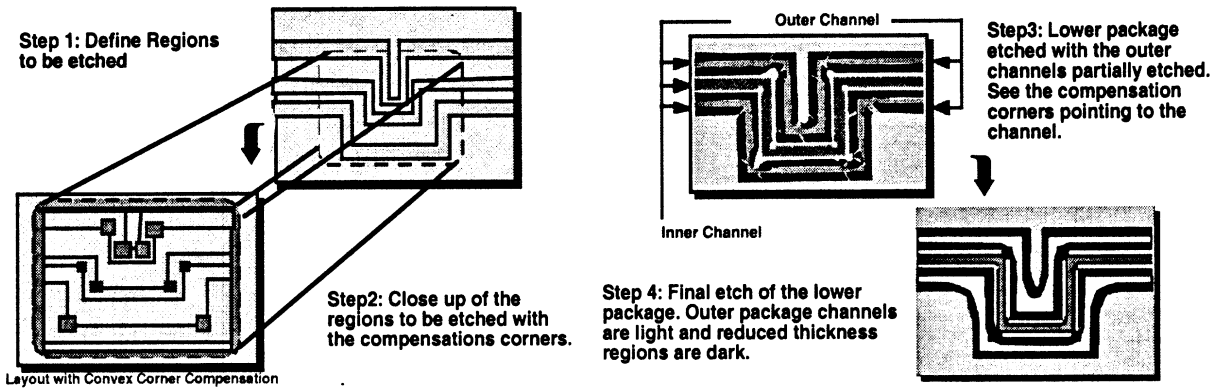


Figure 7. Process steps for the development of the Lower Package.

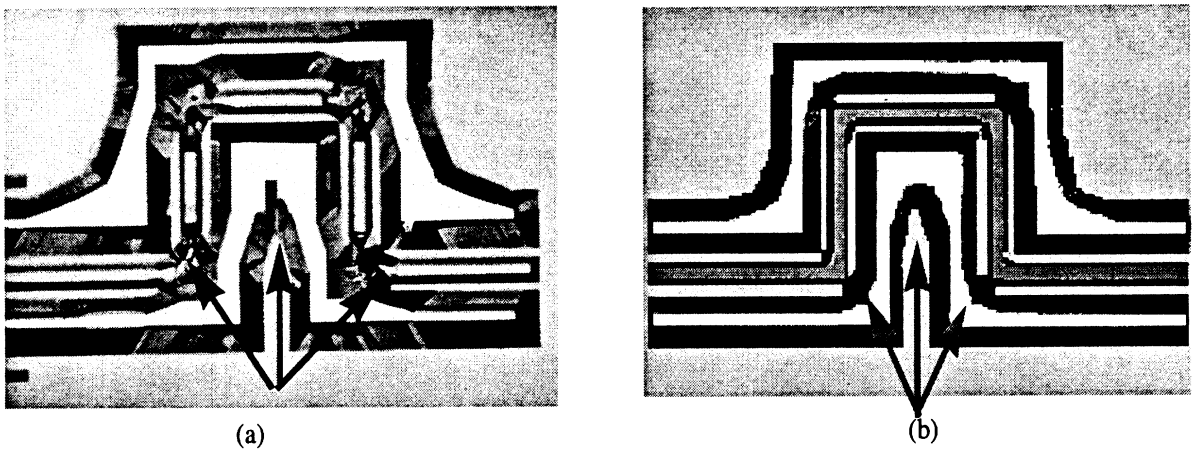


Figure 8. (a) Poor and (b) good compensation from the etch process.

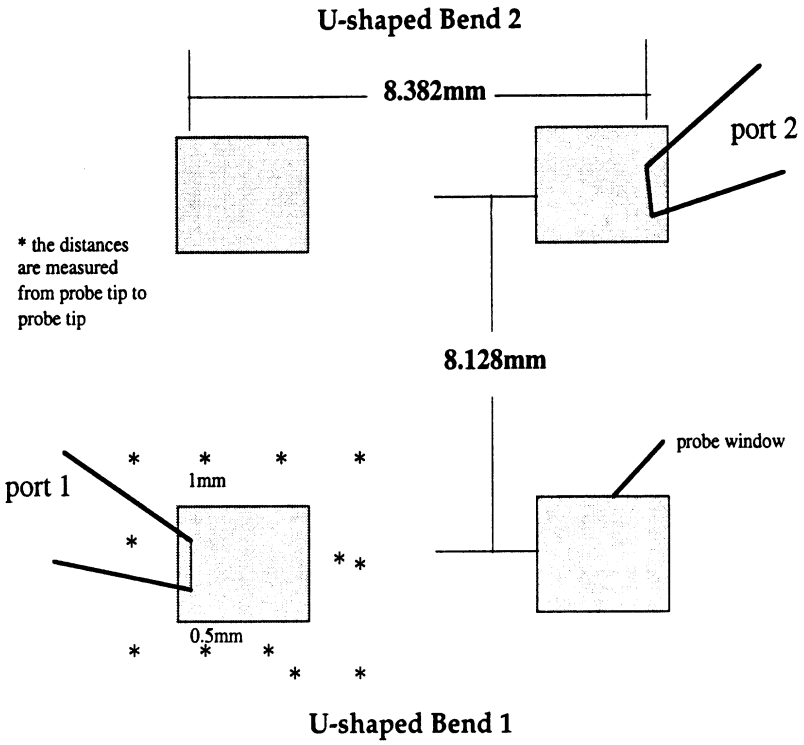


Figure 9. Grey blocks represent the probe window layouts in Design Layout B for the two U-shaped bends. Probing points in the contact noise measurement are indicated by stars at Port 1 for an input signal onto the conducting line at Port 2.

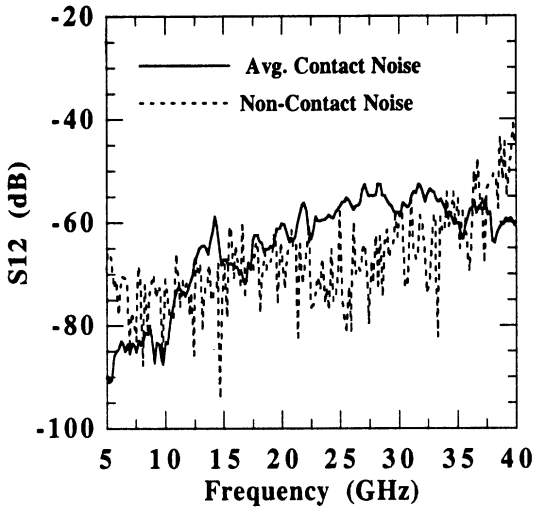


Figure 10. Noise data from Contact and Non-contact measurement.

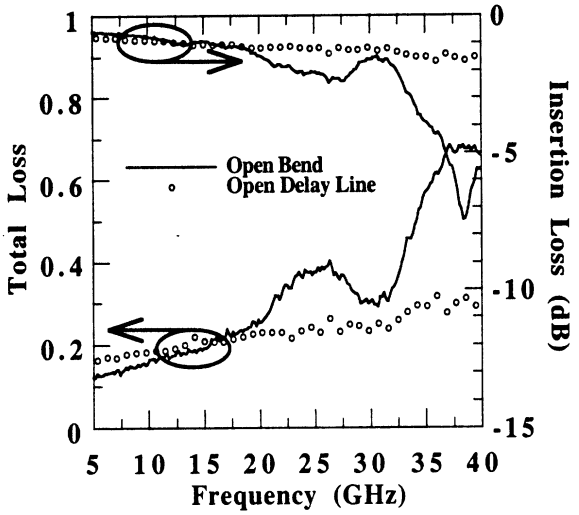


Figure 11. Electrical response of open microstrip circuits in for a delay line and U-shaped bend.

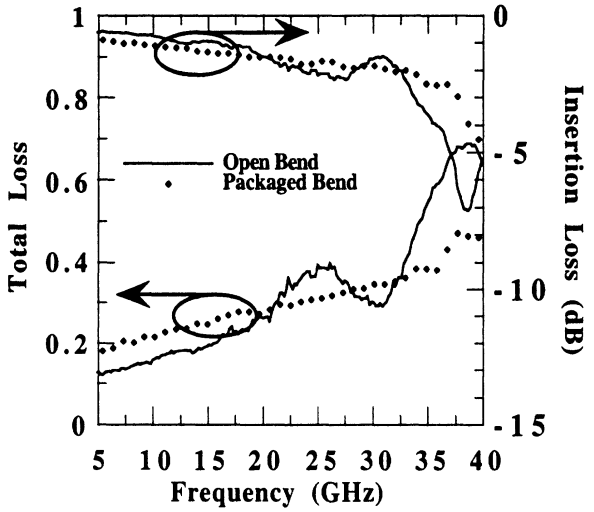


Figure 12. Electrical response of an open and packaged U-shaped microstrip circuit.

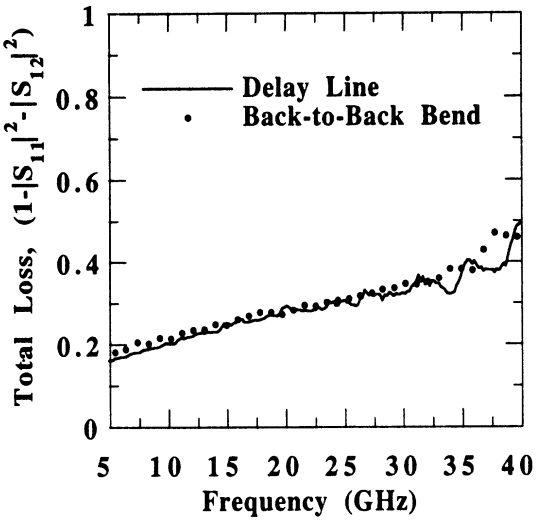


Figure 13. Electrical response of a packaged U-shaped bend and microstrip delay line circuit of similar length.

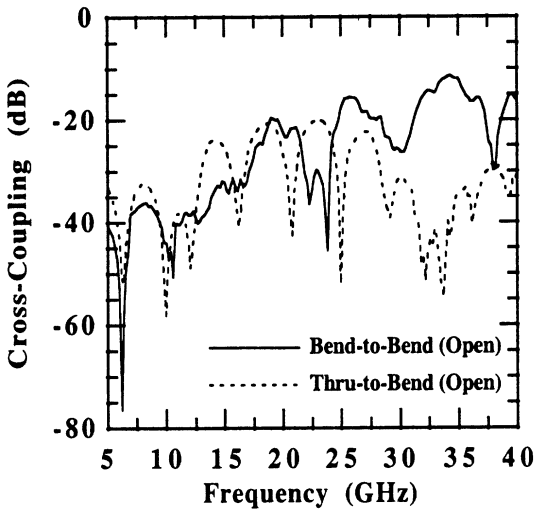


Figure 14. Comparison of cross-coupling effects in open microstrip structures for Design Layout A between the thru and U-shaped bend and Design Layout B between the two U-shaped bends.

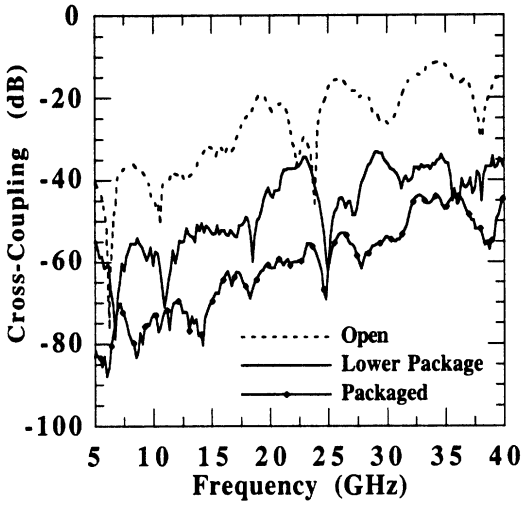


Figure 15. Cross-Coupling effects in Design Layout B for two U-shaped bends in open, lower half packaged, and full packaged designs.

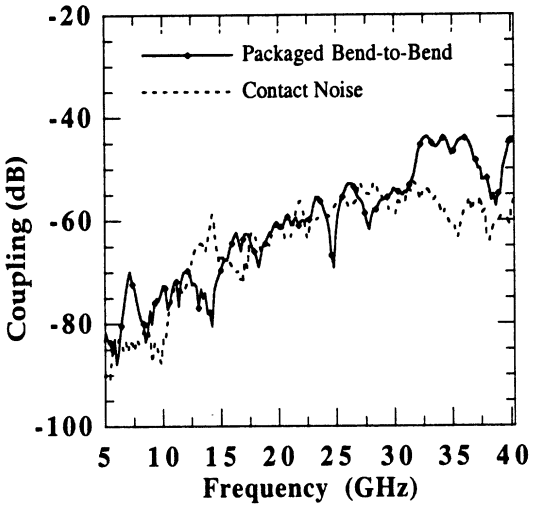


Figure 16. Comparison of coupling between two packaged U-shaped bends and the contact noise measurement of the packaged system.

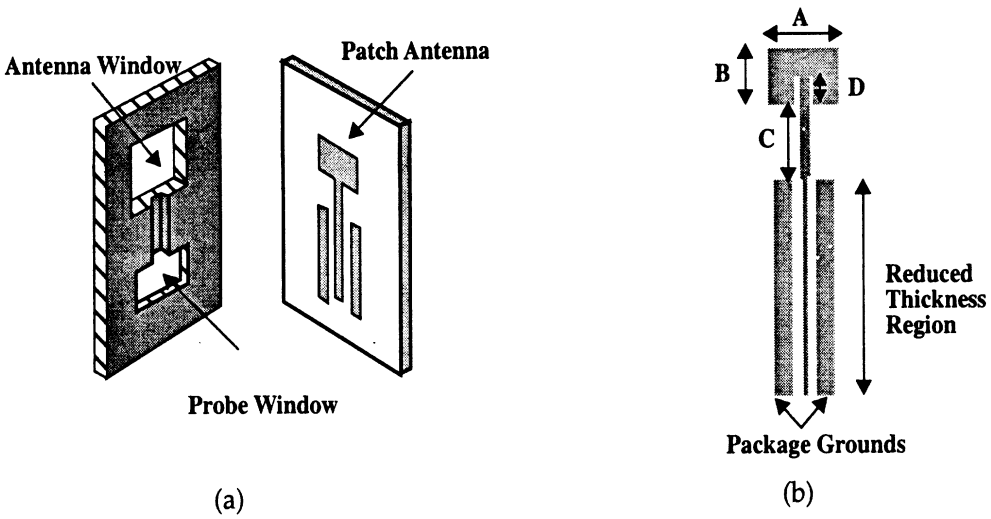


Figure 17. (a) Cross-Section of Packaged Antenna Configuration and (b) Top View of a microstrip patch antenna element of dimensions: A=2900, B=2200, C=2550, and D=1050. All dimensions are in microns.

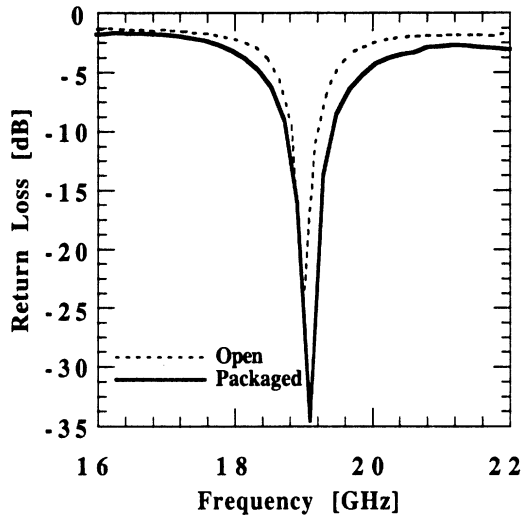


Figure 18. Packaged antenna with a straight thru line configuration on a reduced thickness region.

SILICON-BASED MICROMACHINED PACKAGES FOR DISCRETE COMPONENTS

Rashaunda M. Henderson and Linda P. B. Katehi

The Radiation Laboratory
The University of Michigan, Ann Arbor, MI 48109-2122
USA

ABSTRACT

A novel approach has been taken to develop low cost, high frequency (Ka-band), electronic packages. An existing thick film package for a phase shifter chip has been redesigned using silicon as the base material. This paper reports on the fabrication techniques and the measurement improvement found by coupling silicon micromachining techniques with standard IC processing.

1.0 INTRODUCTION

For several years, electronic packaging for microwave components and systems has taken the back seat to high frequency circuit design and development. While state of the art high frequency components and devices have been realized, the package has been found to cause system degradation with increased frequency. The electronic package provides physical and thermal protection as well as interconnection to subassemblies. In recent years, packaging has received increasing attention and efforts are underway to produce low cost, high quality, high frequency structures.

As a result, MCMs, hybrid and monolithic packages have been developed using cofired ceramic, printed wiring board and thick and thin film technologies. In addition to package design there has been a serious effort in developing commercial modeling tools that can predict the performance of packages in the circuit environment [1]. At this time, high quality packages are being made which tend to be quite expensive and excessive in volume and weight, characteristics that prevent them from wide use [2].

In view of the above, the capability to create a low cost, low weight and volume package which operates at high frequency, demonstrates high bandwidth characteristics, and offers physical protection while not degrading performance, would provide major advances in packaging. At The University of Michigan we have been able to successfully incorporate IC processing techniques with silicon micromachining to fabricate silicon-based packages for discrete and monolithically integrated components. Given the knowledge base developed in silicon micromachining, the goal is to take advantage of the electrical and mechanical properties of single crystal silicon so as to create low cost, high precision, miniature microwave and millimeter wave packaged components.

2.0 BACKGROUND/DESIGN/FABRICATION

Recent work, [3], has led to the development of self-packaged components that have excellent isolation from neighboring elements in addition to individual component protection. Self-packaged silicon components are an alternative to conventional structures, appropriate for low cost, low volume, miniaturized high density subsystems.

Silicon is the best substrate to use when it comes to high frequency packaging components. The mechanical properties as presented by Petersen [4] are excellent and comparable to certain metals. Using micromachining and IC processing techniques, via hole diameter and linewidth dimensions are the smallest possible, which is very much desired for the reduction of high frequency parasitics. The thermal conductivity of Ga As, In P, and Ge (80,65,68), (W/(m*K)) creates problems with heat dissipation. As compared to 92% alumina (18), Si (135) is an excellent heat sink, which makes it a very good packaging material [5]. By combining the electrical and mechanical advantages of silicon, low cost batch fabricated packaged components can be incorporated on-wafer to increase circuit density while remaining low in volume.

A package fabricated by Hughes Aircraft for NASA Lewis served as the model for this design. The high temperature cofired ceramic (HTCC) process is used to develop an alumina (92% pure, ε_r=9.5) hermetic package for a phase shifter chip (Figure 1). This package was reproduced using high resistivity silicon (ε_r=11.7). Figure 2

0-7803-3814-6/97/$5.00 © IEEE

shows the package layout (5 layers) and the through line used for characterization. A metal base is used for support, while an upper metallization layer and top lid are used to seal the package. A silicon substrate layer is used for RF input/output and DC bias lines. A hole is etched through the wafer for chip placement and a set of six micromachined vias are placed along the left and right of the IC for electromagnetic shielding. These vias are used in the seal frame layer as well. A center hole in the seal frame is etched for IC placement and two outer holes are used for wafer probing. The package dimensions are 7.112 x 7.112 x 1.27 mm. The alumina and silicon package differ in bias line width (smaller for silicon) and three ultrasonic wire bonds are used to connect the silicon package and IC as opposed to four in the alumina package. The vias and input/output microstrip feedline in the alumina package are displaced from the center for application reasons whereas the square vias and feedline are symmetric in the silicon design.

Conventional thin film processing technology is utilized to fabricate the package. A 50 ohm through line is used to characterize the effect of the package which incorporates sections of microstrip, stripline and shielded microstrip. Silver epoxy is used to attach the lid and provide the connection between the upper and lower metallization surfaces (electromagnetic shielding). Given the measurement setup, a 50 ohm grounded coplanar waveguide (GCPW) to microstrip transition is used (Figure 3). Via holes are etched to provide connection between the upper and lower metal surfaces. The via holes required in this package are developed by anisotropic etching using ethylene diamine pyrocatechol (EDP). Three microns of electroplated Au are used as the metallization for the package and IC (through line) (Figure 4).

3.0 RESULTS

The silicon package described earlier is characterized experimentally using an HP8510C Network Analyzer, and an Alessi probe station with 150 μm pitch GGB Picoprobes. A Thru-Reflect-Line (TRL) calibration was performed to deembed effects up to the open microstrip feedline.

Figures 5 and 6 show the insertion loss and return loss, respectively, for the alumina and silicon-based package. Over the whole frequency range, the insertion loss of the silicon package is better than that of the alumina package by 0.5 dB. The return loss for the silicon package is mostly attributed to the ohmic loss of the through line for which measured values are shown in Figure 7. The observed irregularity in the alumina package suggests parasitic effects not related to impedance mismatch. The estimated cost for the Si package (batch processing) is less than $1 and reflects a substantial reduction compared to conventional cofired ceramic packages.

4.0 CONCLUSION

We have shown that it is possible to develop silicon-based packages for discrete components using thin film processing and micromachining techniques. This effort is less expensive and outperforms its HTCC counterpart. This packaging approach can be extended to provide advanced packaging techniques where discrete as well as integrated components can be hosted by the same silicon wafer.

5.0 ACKNOWLEDGEMENTS

This work has been supported by contracts from the Army Research Office and the Office of Naval Research.

REFERENCES

[1] J.G. Yook, L.P.B. Katehi, et. al., "Experimental and Theoretical Study of Parasitic Leakage/Resonance in a K/Ka-Band MMIC Package," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 44, No. 12, December 1996.

[2] M.I. Herman, K.A. Lee, et. al., "Novel Techniques for Millimeter-Wave Packages," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 7, July 1995.

[3] R.F. Drayton, L.P.B. Katehi, "Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 9, September 1995.

[4] K.E. Petersen, "Silicon as a Mechanical Material," *Proceedings of the IEEE*, Vol. 70, No. 5, May 1982.

[5] J.E. Licari, *Multichip Module Design, Fabrication and Testing*, Mc-Graw Hill, Inc., New York, 1995.

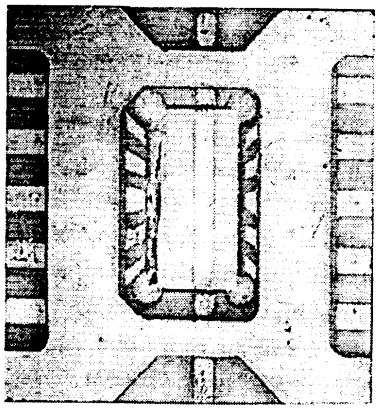


Figure 1 HTCC hermetic package designed by NASA Lewis.

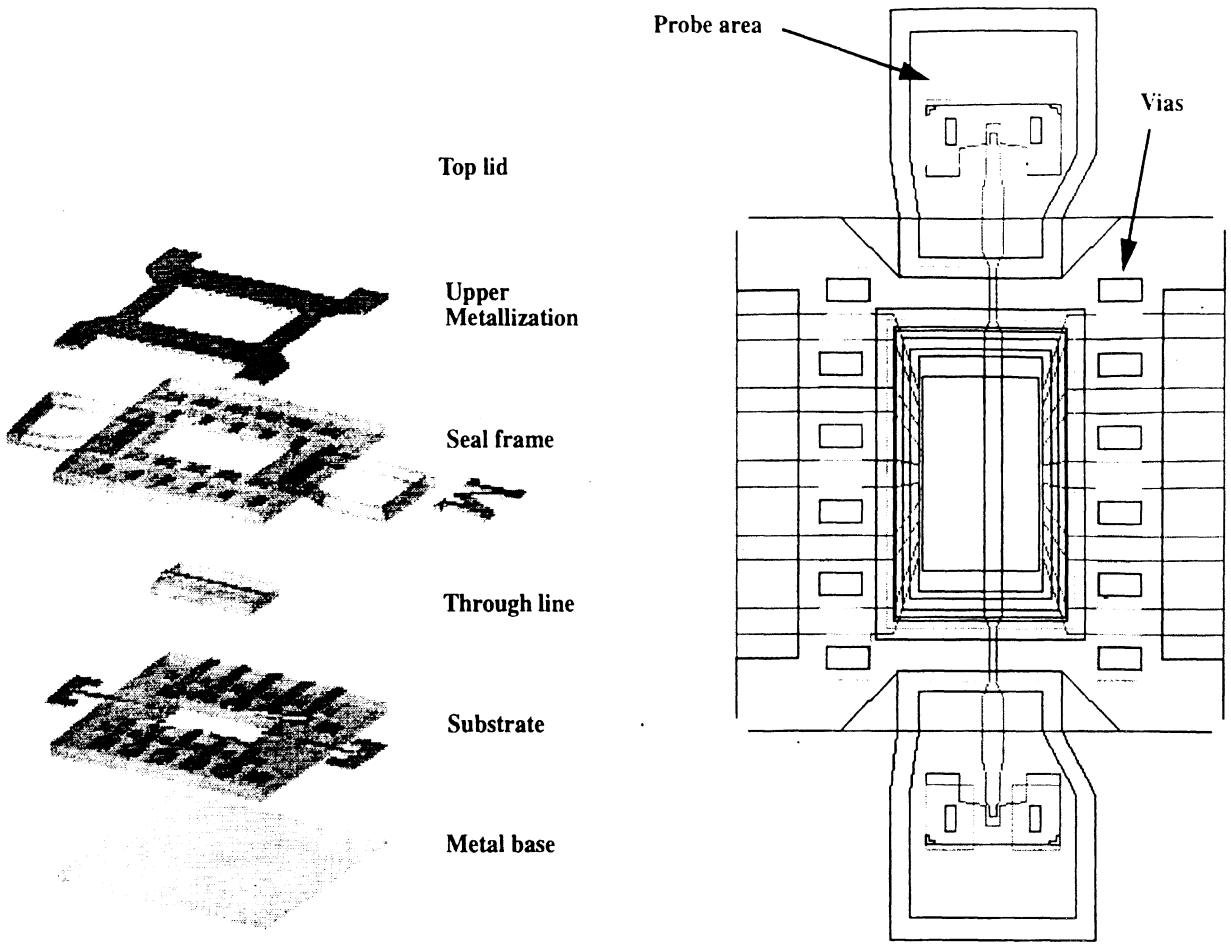


Figure 2 3-D view of package layers and actual CAD drawing with all layers superimposed.

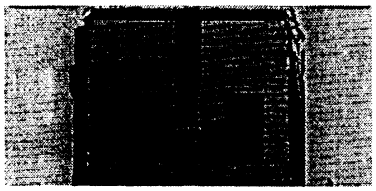


Figure 3 Photograph of probe window with GCPW to microstrip transition for on-wafer probing.

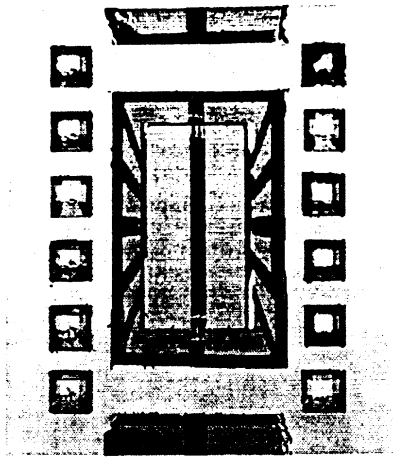


Figure 4 Micromachined silicon-based package.

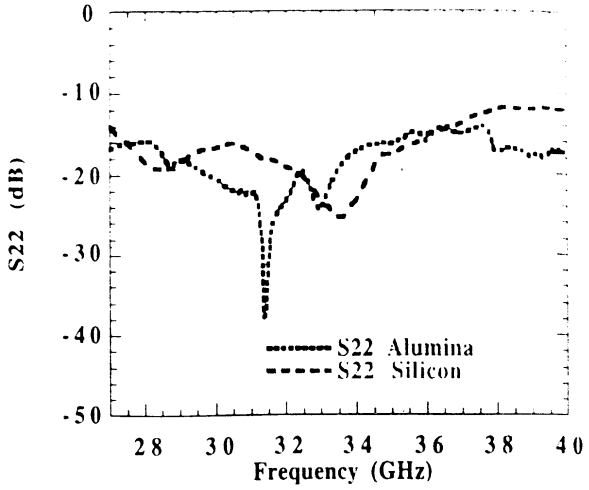


Figure 6 Return Loss

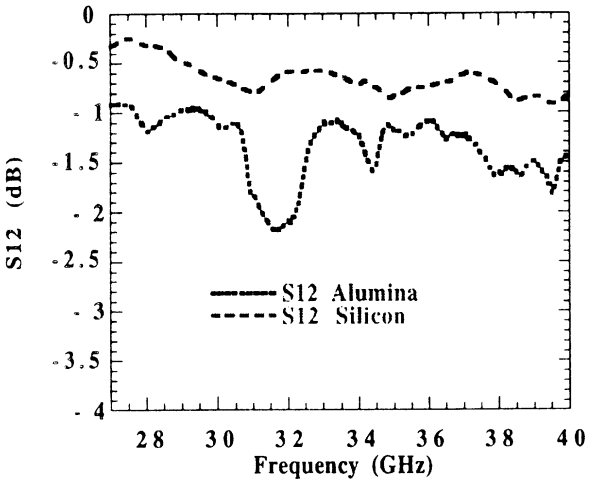


Figure 5 Insertion Loss

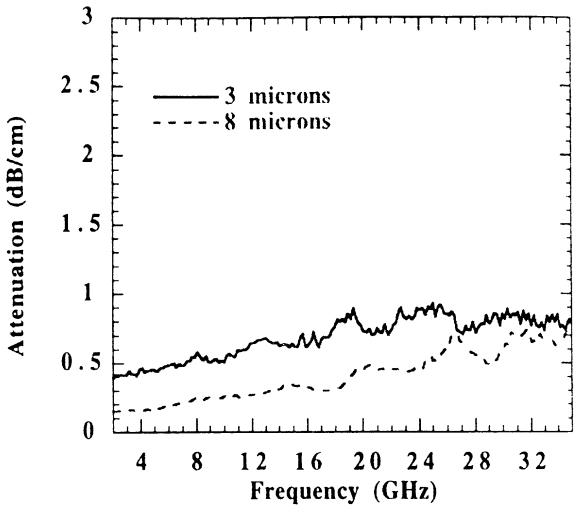


Figure 7 Attenuation of 9 mm through line in package.

Submitted for publication in IEEE Transactions on Microwave Theory and Techniques

GaAs vs. Quartz FGC Lines for MMIC Applications

John Papapolymerou, Jack East and Linda P.B. Katehi

Department of Electrical Engineering and Computer Science
The University of Michigan
1301 Beal Ave.
Ann Arbor, MI 48109-2122
FAX: (313) 647-2106

Abstract

The performance of FGC lines on GaAs and quartz for high frequency MMIC applications is experimentally investigated in this paper. The FGC lines on GaAs are covered with a thin layer of polyimide for passivation purposes. Permittivity and attenuation characteristics for these lines up to 118 GHz are presented and compared with the corresponding characteristics of FGC lines on a quartz substrate, commonly used for millimeter wave applications. The impact of different characteristic impedance values in attenuation properties for both GaAs and quartz is also addressed. Results indicate that the loss on the lines does not depend on the substrate material but rather on line geometry. All the lines tested show low loss and low dispersion characteristics.

1 Introduction

The Finite Ground Coplanar (FGC) transmission line is a modified Coplanar Waveguide (CPW) structure with improved performance at millimeter wave frequencies [1]. It consists of three strips, one for the signal and two for the ground, similar to the the CPW line, but with ground strips that are narrow. A back-side conductor is optional for the FGC line since the characteristics are independent of back side metallization. The main advantage of the FGC lines is that they do not support parallel-plate waveguide modes and as a result do not require via-holes for ground equalization. These vias introduce parasitics and increase fabrication complexity. The permittivity and attenuation characteristics of FGC lines on GaAs and Si have been extensively investigated by Brauchler [2]. Experimental results show that a nearly TEM mode propagates over a wide frequency range (2-118 GHz) and that loss is mainly ohmic. The use of full thickness substrates and the elimination of via holes for mode suppression will reduce the cost and complexity of MMIC design and fabrication at millimeter wave frequencies. The purpose of this short paper is to discuss the effect of polyimide passivation on these lines and to compare lines with different dimensions on both GaAs and quartz substrates. The results confirm the excellent performance of the FGC lines on GaAs.

High performance line structures are an important part of MMIC design and fabrication at millimeter wave frequencies [3]. Conventional microstrip lines have increasing dielectric loss with frequency. One solution to this problem is to use a low loss material such as quartz as a substrate. However, this requires bonding active circuits onto the quartz, which increases fabrication complexity especially at higher frequencies, while at the same time the requirement for thinned substrates for microstrip or via holes for CPW is still important to satisfy. FGC lines are conductor loss dominated, so the use of semiconductor substrates will have a small effect on the line loss properties. Furthemore, passivation is also an important part of MMIC fabrication. Polyimide is a well characterized dielectric material that has been extensively used in the past as a passivation layer and as a substrate for the fabrication of microstrip lines [4]-[5]. In this paper we investigate the effect of a thin polyimide coating on top of the GaAs FGC lines and compare their performance with low loss quartz based lines. The cross section of the fabricated FGC lines can be seen in Fig.1. Four configurations have been fabricated and tested: a) FGC lines on GaAs with Z_o=40, 50 and 60 Ω, b) FGC lines on GaAs with a 2 μm thick polyimide overlay and $Z_o = 50\ \Omega$, c) FGC lines on

GaAs with a 3 μm thick polyimide overlay and $Z_o = 50\ \Omega$ and d) FGC lines on quartz with Z_o=70, 90 and 100 Ω.

2 Fabrication

FGC lines have been fabricated on a 525 μm thick semi-insulating GaAs wafer and a 165 μm thick quartz wafer. The FGC line signal-strip (w), slot (s) and ground-strip (w_g) widths are 50, 45, 160 μm, respectively and correspond to a 50 Ω line for GaAs substrate and to 90 Ω for quartz substrate. The lines have been created by using standard lift-off process with a total metal thickness of 1 μm. After the lines are formed, polyimide Pyralin PI2545 is spun at 4 Krpm and 2.5 Krpm on top of the lines for two GaAs wafers, in order to get a thickness of 2 μm and 3 μm respectively. The pre-cure temperature for the polyimide film is 140^o C and the hard-cure 200^o C while the baking time is set to 30 minutes and 3 hours respectively. At the beginning and the end of the FGC lines the polyimide is chemically etched in order to allow the probe tips of the measurement system to be in electrical contact with the lines. The relative dielectric constant of the polyimide film is 3.5. The test FGC lines consisted of a thru line with a length of 1.0 mm, a short with a length of 0.5 mm and 3 delay lines with 1.388 mm, 4.106 mm and 10 mm lengths respectively.

3 Results and Discussion

All of the mesurements for the FGC line characteristics have been performed with an HP8510 network analyzer and a probe station using a variety of RF probes. De-embeding is achieved by performing a Thru-Reflect-Line (TRL) calibration with the help of Multical [6], a measurement program available from NIST. This program also provides the effective dielectric permitivity and attenuation characteristics of the lines under test, from the delay line measurements.

The effective dielectric constant of the various line configurations is shown in Fig. 2. As can be seen, the nearly constant behavior of ϵ_{eff} over the entire frequency range indicates the propagation of a nearly pure TEM mode. In addition, we observe that the thin film of polyimide is responsible for a slight increase in ϵ_{eff} for both the 2μm polyimide (1.4%) and the 3μm polyimide (2.8%) when compared to that of bare FGC lines. This increase is more pronounced at higher frequencies. However, ϵ_{eff} is comparable with that of bare lines over the entire frequency range , indicating

that the addition of polyimide does not significantly change the propagation characteristics of the lines.

Fig. 3 shows the attenuation per physical length for the four different cases. The straight line between 60 and 70 GHz represents a gap in the data. As can be seen, the polyimide increases the attenuattion constant with the effect being more pronounced in W-band (12%) and for the thicker polyimide (23% in W-band). The quartz has the smallest attenuation for all the lines. This lower loss when measured in dB/cm is due to the lower effective dielectric constant and higher characteristic impedance of the FGC line on quartz (90 Ω compared to 50 Ω for GaAs). Since in most microwave circuits lengths are expressed in terms of wavelengths, the attenuation per guided wavelength for the four different lines has been evaluated and is shown in Fig. 4. The results are comparable for all four cases with GaAs (bare or with polyimide) being slightly better than quartz. This indicates that the loss of FGC lines is ohmic in nature and independent of the substrate material. As a result, FGC lines are very good candidates for high frequency application circuits. Furthemore, we can conclude that the thin layer of polyimide that covers the FGC lines on GaAs for passivation purposes does not increase the total loss of the lines.

Since the characteristic impedances for the lines investigated were different for GaAs and quartz, additional lines with varying dimensions and impedances have been fabricated. The impedance range for the two substrates corresponds to a convenient range for line fabrication. The line dimensions and the corresponding Z_o can be seen in Table 1. From the measured attenuation per physical length, the attenuation per guided wavelength has been evaluated and can be seen in Fig.5 for GaAs and Fig.6 for quartz. From Fig. 5 we observe that the 50 and 60 Ω lines have practically the same attenuation while for the 40 Ω line there is an increase of about 100% at 60 GHz which is the center of the entire frequency range. Similarly, from Fig. 6 we observe that the attenuation for the 90 and 100 Ω lines is almost the same and that the 70 Ω line exhibits a 60% increase from the other two lines at 60 GHz. We should note here that the small ripple observed in the 90 and 100 Ω lines is due to ripple in the mismatched measurement system.

In order to better understand the behavior of the FGC lines versus impedance, the measured attenuation per physical length data have been curve fitted to a $a+b\sqrt{f}$ function and the extracted functions have been used in order to evaluate the attenuation per guided wavelength for three different frequency points in the center of each measured band. The final results can be seen in

Table 1: Geometrical characteristics for fabricated lines

substrate	w (μm)	s (μm)	Z_o (Ω)
GaAs	50	15.45	40
GaAs	50	64.5	60
Quartz	50	18.61	70
Quartz	50	64.5	100

Figs. 7-9 for both quartz and GaAs. From these figures we observe that the attenuation decreases as the impedance increases in a non-linear way. In terms of loss in dB/λ_g a 50 or 60 Ω line on GaAs is equivalent to a 90 Ω line on quartz. However, we should note that the 50 Ω and 60 Ω GaAs lines have the same geometrical dimensions with the 90 Ω and 100 Ω lines on quartz respectively, indicating a strong dependence of the total line loss on the geometrical characteristics rather than the substrate material and thickness. This feature makes FGC lines ideal for high frequency MMIC's.

Having found that in terms of loss GaAs and quartz are equivalent for the same FGC geometry, the choice of material for a substrate depends on other design criteria. If low cost is a major issue then quartz can be chosen with the active devices being flip-chip bonded to it. On the other hand if the active devices must be monolithically integrated with the rest of the circuitry, then GaAs is more appropriate with a thin overlay of polyimide for passivation. GaAs is also more suitable for applications above 120 GHz where the flip-chip bonding process increases fabrication complexity considerably.

4 Conclusions

FGC lines on GaAs with a thin overlay of polyimide have been fabricated and tested. Experimental results show a negligible increase in the effective dielectric constant and a small increase in the attenuation per physical length, when compared with bare FGC lines on GaAs. The attenuation per physical length of FGC lines on GaAs with or without polyimide is higher than that of FGC lines on quartz. The attenuation per guided wavelength, however, is almost the same for all types of

lines investigated in this paper, indicating that the total loss of FGC lines with the same geometry is independent of the substrate material. This allows for the use of a thin layer of polyimide over FGC lines on GaAs without increasing the total loss in actual circuits while providing passivation at the same time. In addition, the attenuation of the lines decreases in a non linear fashion versus characteristic impedance. Finally, FGC lines with a polyimide overlay can be used in millimeter wave receivers and transmitters fabricated on GaAs, where the active devices are monolithically integrated with the other circuitry and do not need to be flip-chip bonded as in the case of quartz.

5 Acknowledgement

The authors would like to acknowledge the help of Dr. Imran Mehdi of the Jet Propulsion Laboratory for providing the quartz material used in these experiments. This work has been partially supported by the Office of Naval Research and partially by NASA/JPL.

References

[1] F. Brauchler, S. Robertson, J. East and L.P.B Katehi, "W-Band Finite Ground Coplanar (FGC) Line Circuit Elements," *IEEE MTT-S International Symposium Digest,* June 1996.

[2] F. Brauchler, "Finite Ground Coplanar Passive and Active Circuits," *Ph.D. Dissertation,* The University of Michigan, Ann Arbor, 1996.

[3] F. Brauchler, J. Papapolymerou, J. East and L.P.B. Katehi,"W-Band Monolithic Multipliers,"*IEEE MTT-S International Symposium Digest,* June 1997.

[4] G. Ponchak, A. Downey and L.P.B. Katehi, "High Frequency Interconnects on Silicon Substrates," *Radio Frequency Integrated Circuit (RFIC) Symposium,* June 1997.

[5] H. Ogawa, T. Hasegawa, S. Banba and H. Nakamoto,"MMIC Transmission Lines for Multi-Layered MMIC's," *IEEE MTT-S International Symposium Digest,* June 1991.

[6] R.B. Marks and D.F. Williams,"Program MultiCal," *rev. 1.00, NIST,* August 1995.

Figure Captions

Fig.1 FGC lines on GaAs with a polyimide overlay.

Fig.2 Effective dielectric constant vs. frequency for the various FGC lines.

Fig.3 Attenuation per physical length vs. frequency for the various FGC lines.

Fig.4 Attenuation per guided wavelength vs. frequency for the various FGC lines.

Fig.5 Attenuation per guided wavelength for lines on GaAs with different Z_o.

Fig.6 Attenuation per guided wavelength for lines on quartz with different Z_o.

Fig.7 Attenuation per guided wavelength vs. characteristic impedance for lines on GaAs and quartz at f=19.1 GHz.

Fig.8 Attenuation per guided wavelength vs. characteristic impedance for lines on GaAs and quartz at f=50 GHz.

Fig.9 Attenuation per guided wavelength vs. characteristic impedance for lines on GaAs and quartz at f=94 GHz.

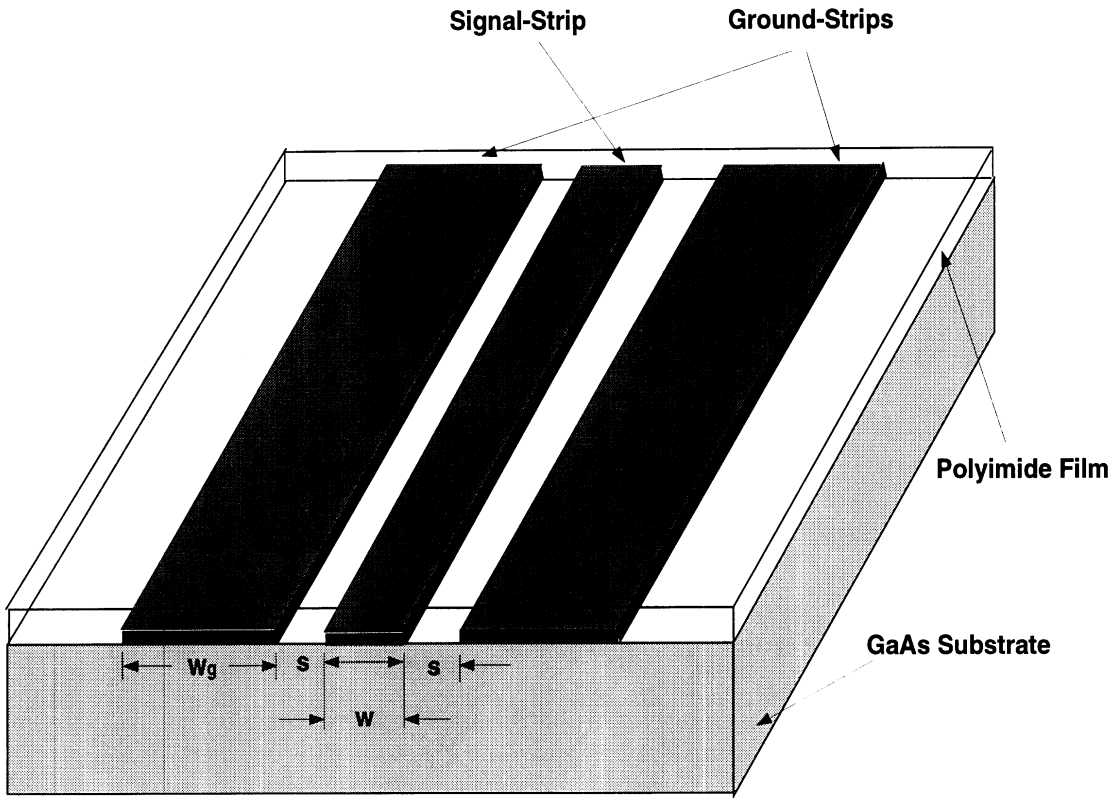


Figure 1: FGC lines on GaAs with a polyimide overlay.

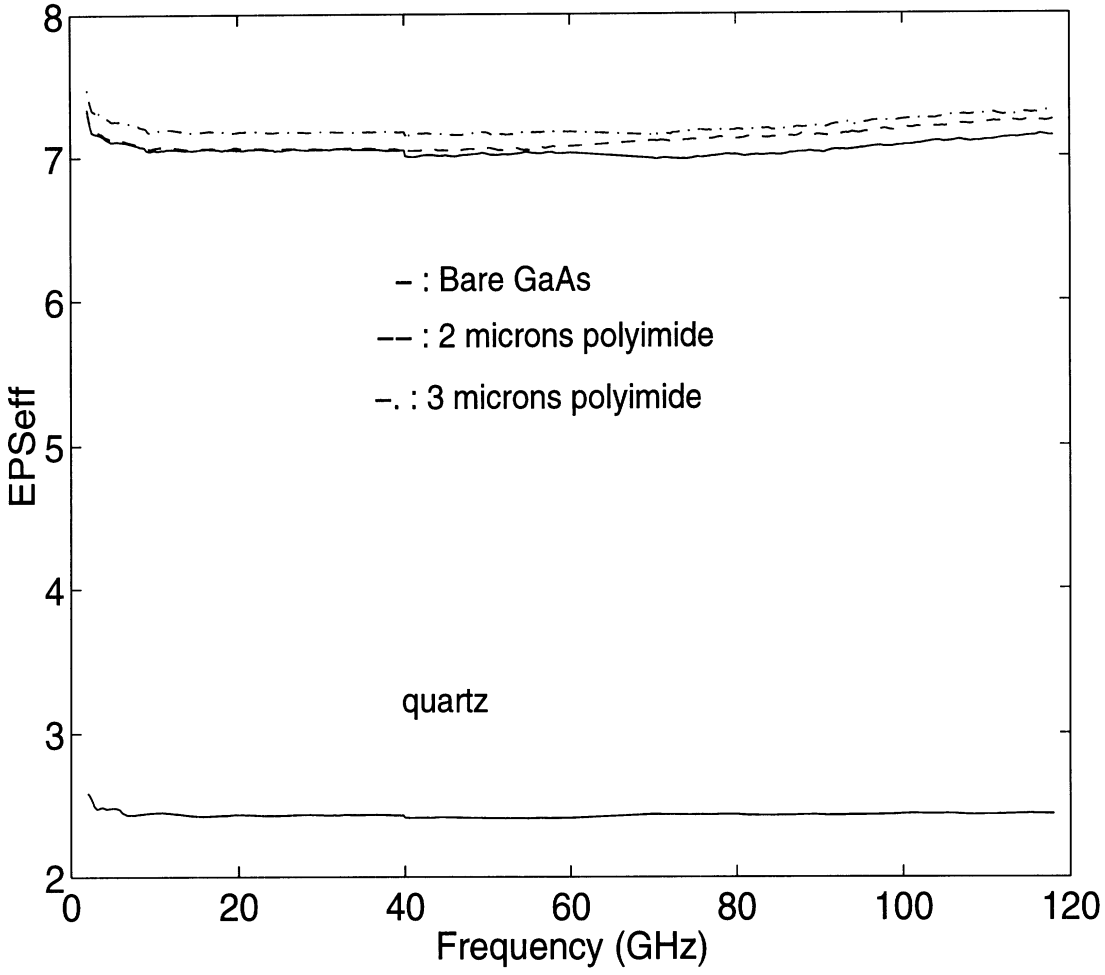


Figure 2: Effective dielectric constant vs. frequency for the various FGC lines

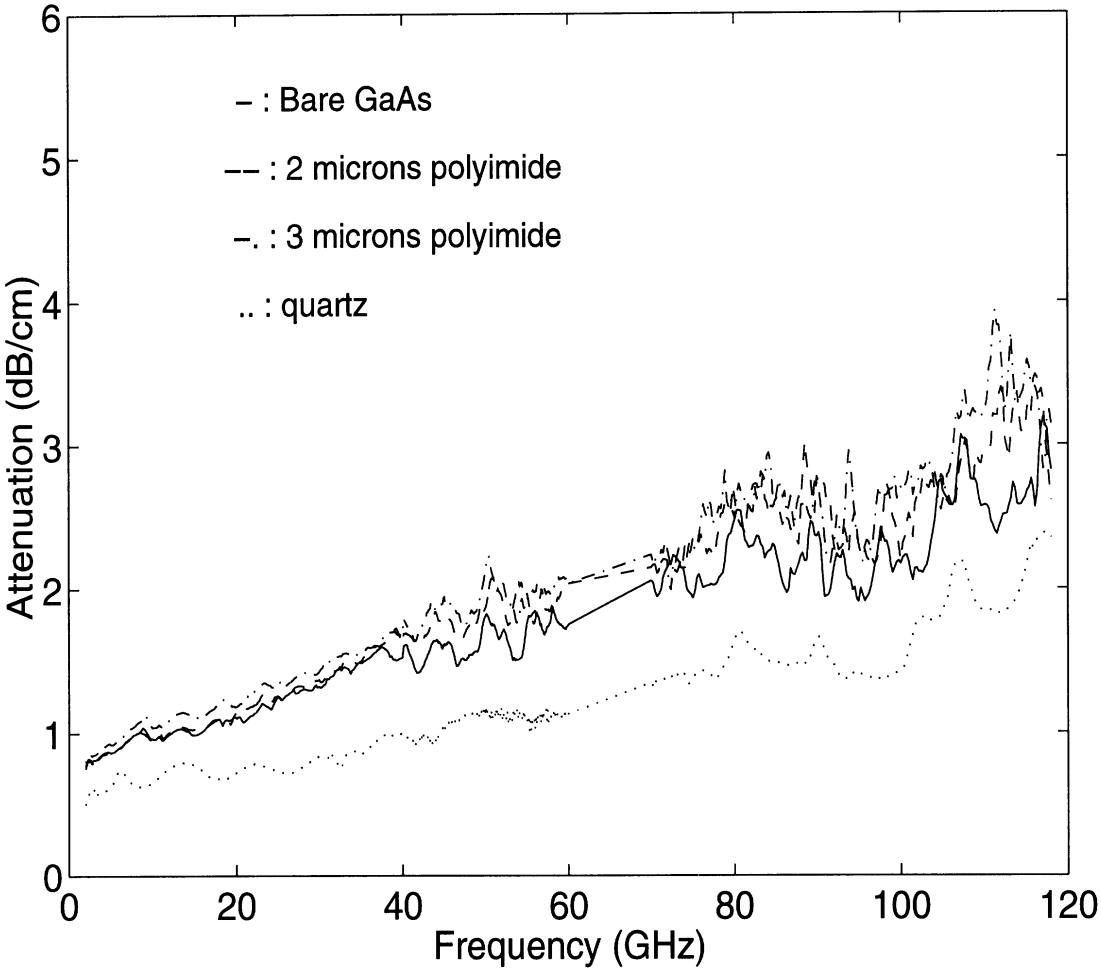


Figure 3: Attenuation per physical length vs. frequency for the various FGC lines

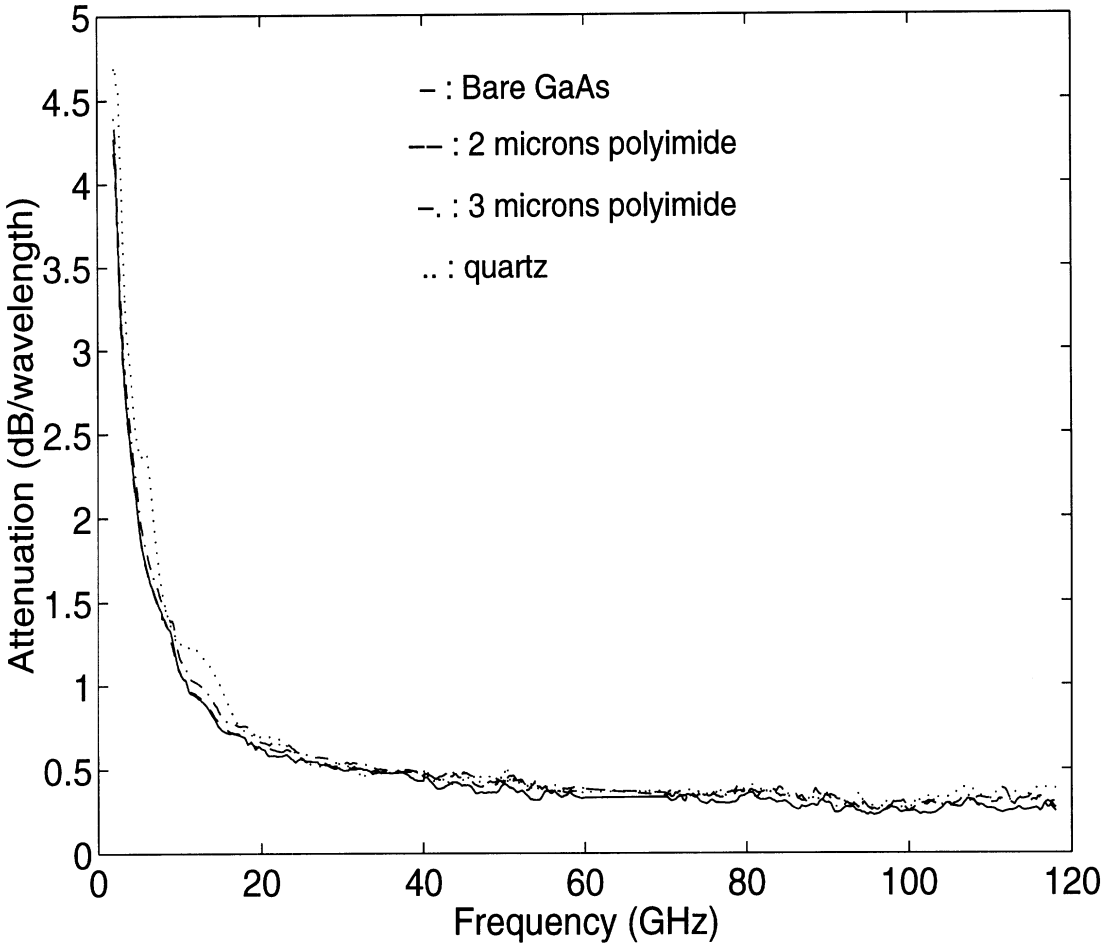


Figure 4: Attenuation per guided wavelength vs. frequency for the various FGC lines

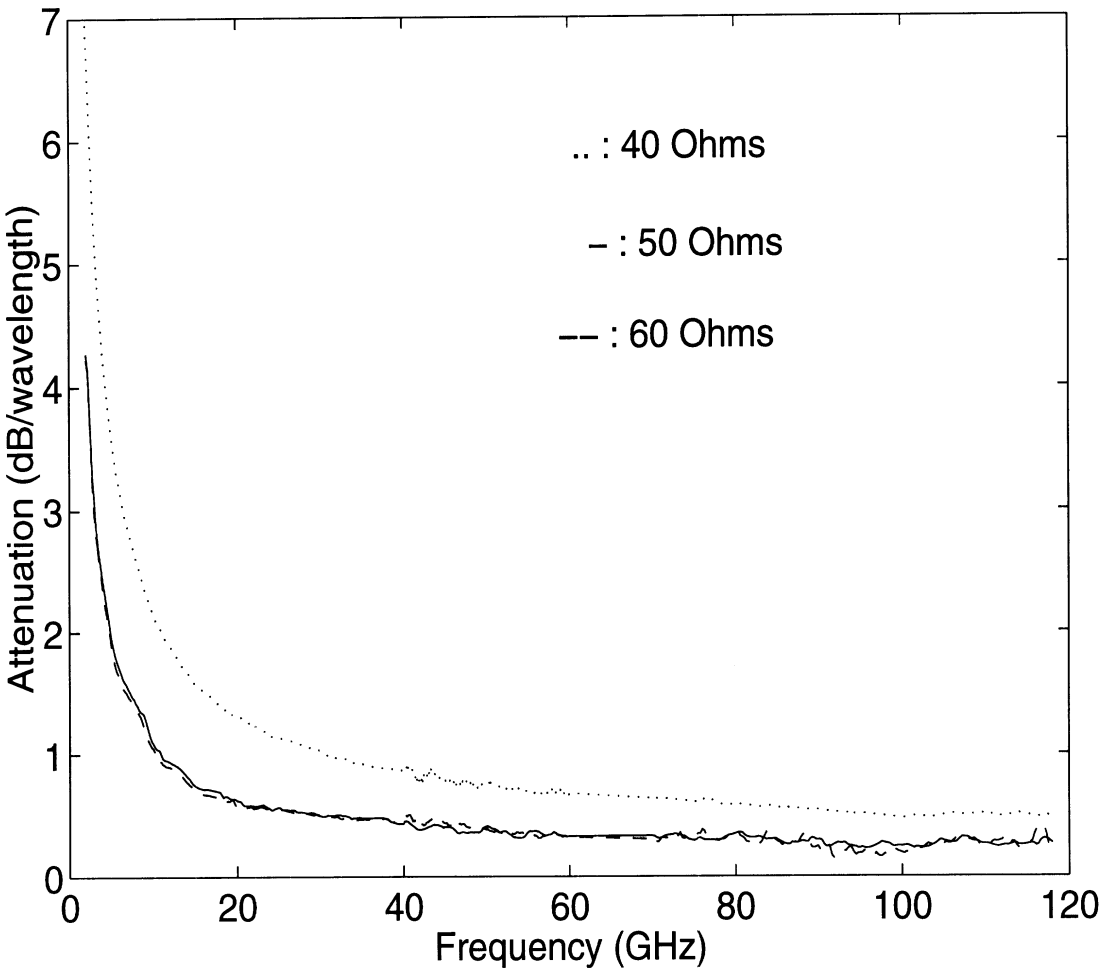


Figure 5: Attenuation per guided wavelength for lines on GaAs with different Z_o

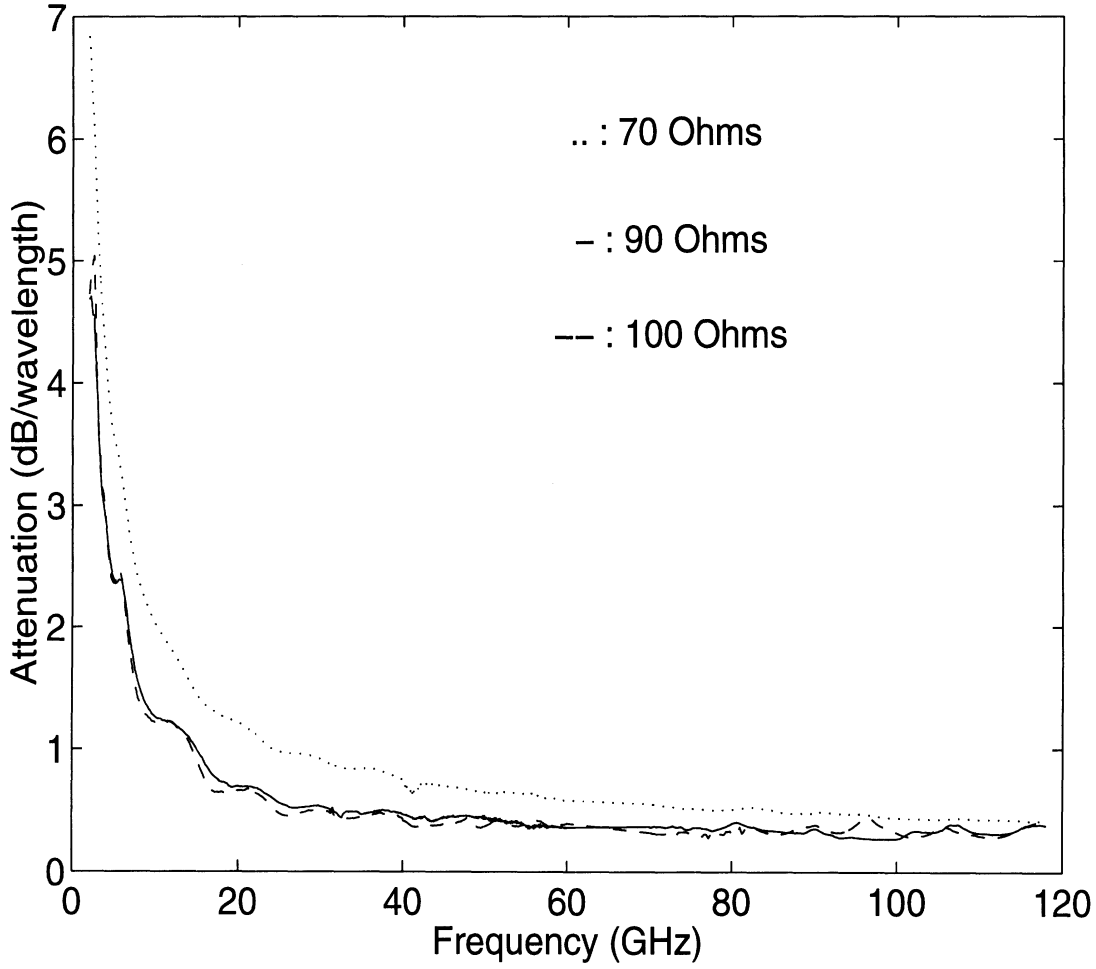


Figure 6: Attenuation per guided wavelength for lines on quartz with different Z_o

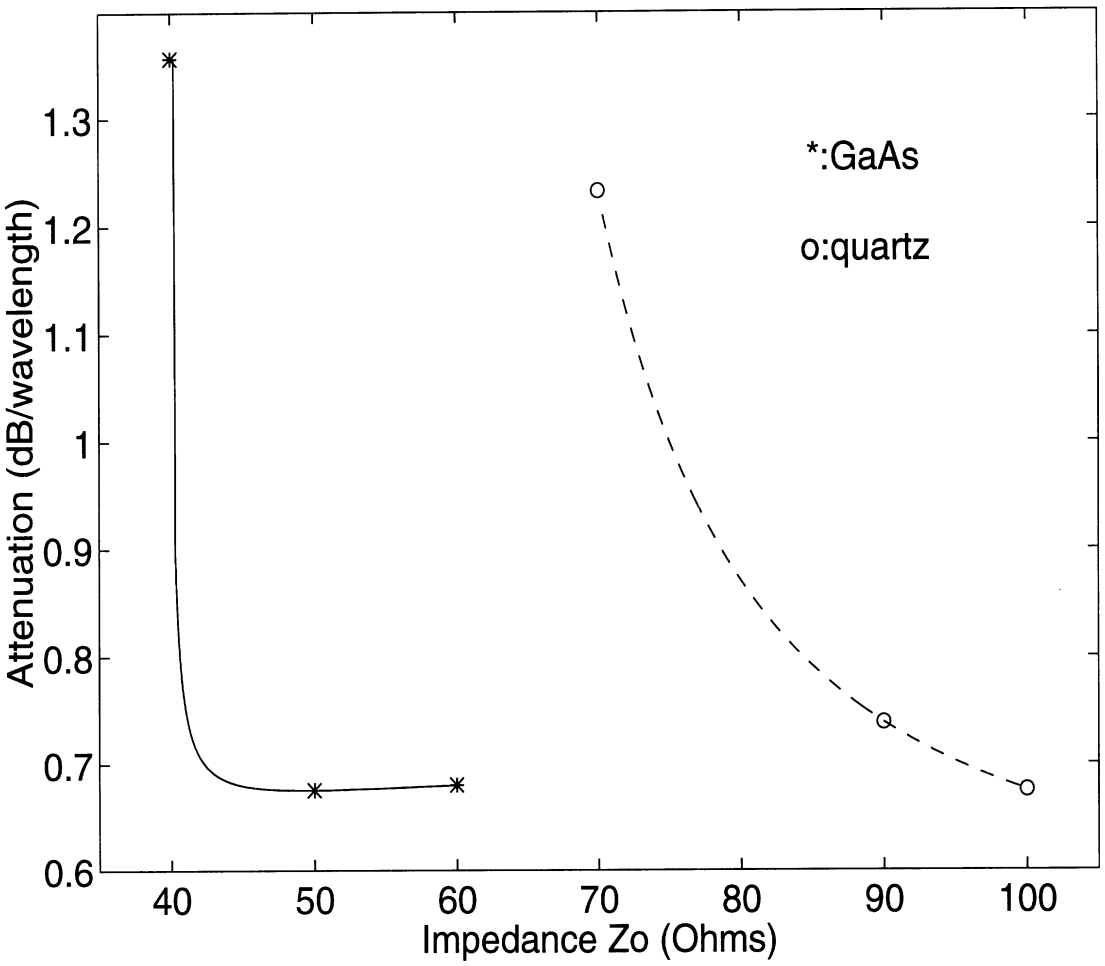


Figure 7: Attenuation per guided wavelength vs. characteristic impedance for lines on GaAs and quartz at f=19.1 GHz

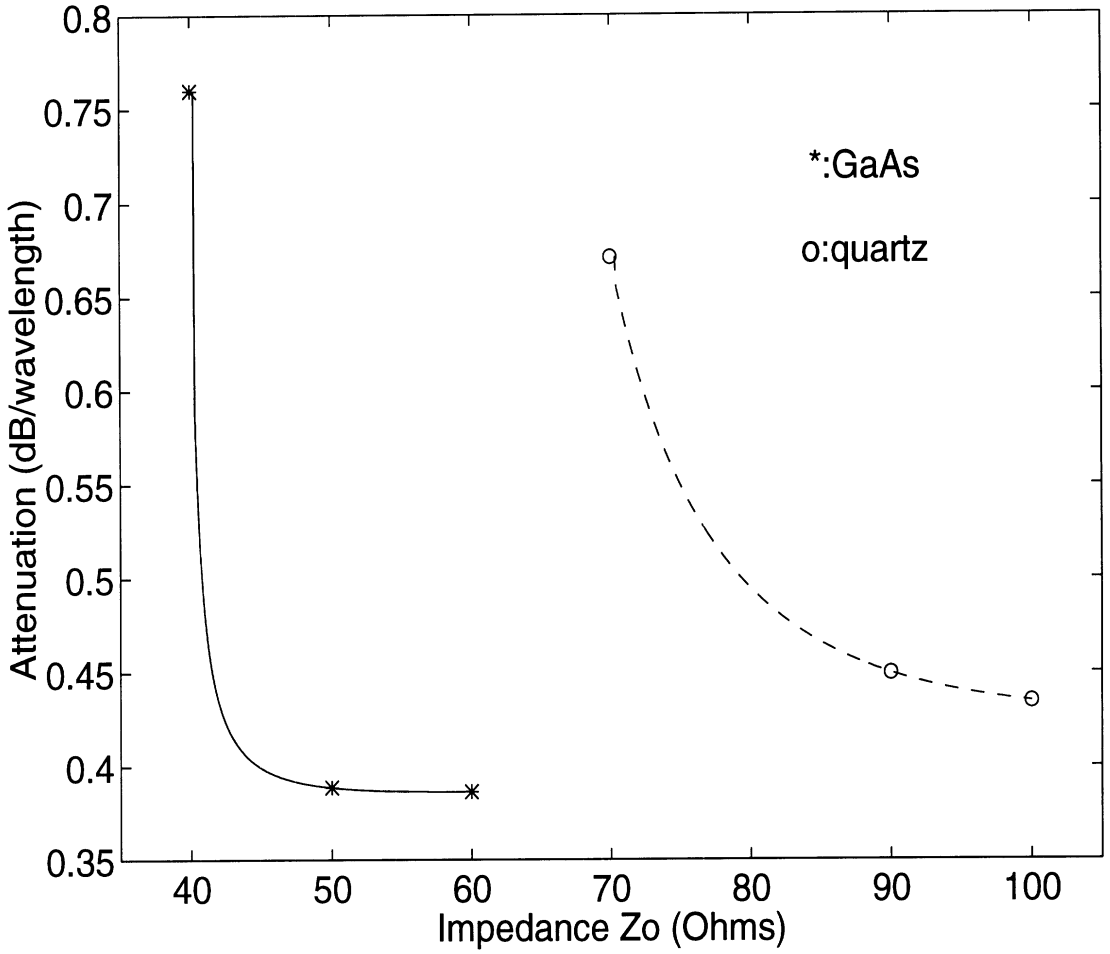


Figure 8: Attenuation per guided wavelength vs. characteristic impedance for lines on GaAs and quartz at f=50 GHz

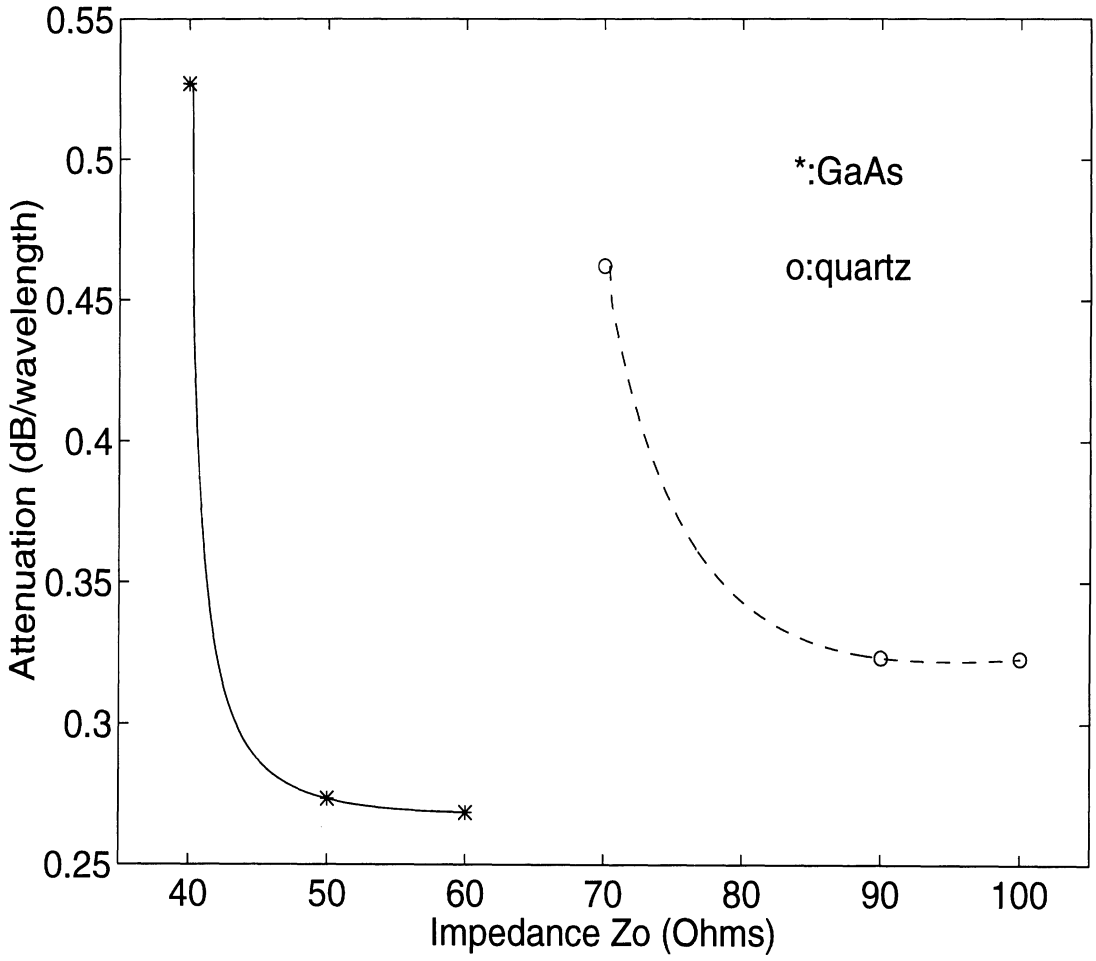


Figure 9: Attenuation per guided wavelength vs. characteristic impedance for lines on GaAs and quartz at f=94 GHz

WAVELET-BASED MODELING OF WIRE ANTENNAS AND SCATTERERS

Kazem F. Sabet†, Linda P.B. Katehi‡, and Kamal Sarabandi‡

† EMAG Technologies, Inc., 2901 Hubbard Rd., Suite E-116, Ann Arbor, MI 48105
‡ Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122

I. INTRODUCTION

During the past two decades, the method of moments (MoM) has widely been used to analyze wire antennas and scatterers in open boundary environments. This has led to the emergence of popular computer codes such as NEC and its derivatives, that are able to treat complex wire structures with a high degree of accuracy. These codes are of great practical interest not only due to the importance of wire antennas as popular radiating elements, but because many sophisticated structures can be modeled using wiregrid equivalents amenable to the thin-wire approximation.

Although theoretically, the conventional MoM-based codes offer infinite capability in view of complexity of the wire structure, they have a limited scope in practice due to the fullness of the moment matrices. As the number of unknowns increases, so does the size of the linear system to be solved. The treatment of very large linear systems often poses three major computational problems: 1) memory usage for the storage of the system, 2) computation time for inversion of the system, and 3) stability of the numerical solution. The storage dilemma has traditionally become the bottleneck of conventional integral-based numerical techniques. Computational speed is another major issue which quickly turns into a limiting factor when solving full linear systems. This is especially critical if the full-wave simulation is part of the antenna design process. In the meantime, large densely populated moment matrices suffer from poor condition numbers. This fact leads to some adverse consequences which directly affect the computational cost. For instance, to achieve numerical stability, it is often necessary to maintain a very high degree of precision in the numerical evaluation of the moment integrals. Poor condition numbers also deteriorate the convergence of iterative linear system solvers.

In the past couple of years, the newly developed theory of multiresolution analysis has opened new horizons for the application of the method of moments by making it possible to generate highly sparse linear systems [1]-[5]. It has been demonstrated the due to the cancellation property of wavelet basis functions, a wavelet-dominated moment matrix can be thresholded to render it highly sparse. The error introduced to the system solution due to the thresholding process can be kept minimum depending on the thresholding scheme and the threshold level. Retaining a high level of accuracy in spite of discarding a sizable number of negligible matrix elements is a clear indication of the improvement in the system condition number. This phenomenon originates from the mathematical properties of the multiresolution analysis leading to matrix regularization. An interesting and unique feature of multiresolution expansions is the fast wavelet transform (FWT), which establishes a recursive relationship among the basis functions at different resolution levels. When implemented, this algorithm can improve the computational efficiency by speeding up the matrix fill process in many cases. The wavelet concepts have been applied successfully to the modeling of printed microwave circuits and antennas, dielectric structures and scattering from two-dimensional geometries, to name a few [2]-[5].

In this paper, we investigate the modeling of wire antennas and scatteres using intervallic multiresoultion expansions. It will be shown how the fast wavelet transform (FWT) can easily transform a high resolution grid into a multiresolution wavelet-dominated grid. The radiation and scattering properties of various wire antenna arrays will be examined, and the major improvements in the computational speed, memory usage and numerical convergence of the solution will be discussed.

II. FORMULATION

The formulation of the wire structure in this paper is based on the generalized Pocklington integral equation. In order to avoid the source singularity of the free space Green's function, the thin wire approximation is utilized. In other words, filament currents are assumed at the center of the conducting wires for MoM expansion, and the testing procedure is carried out on the surface of the wire. Denoting by $G(\mathbf{r}|\mathbf{r}')$ the free space Green's function:

$$G(\mathbf{r}|\mathbf{r}') = \frac{e^{-jk_0|\mathbf{r}-\mathbf{r}'|}}{4\pi|\mathbf{r}-\mathbf{r}'|}, \tag{1}$$

one can then write:

$$\hat{\mathbf{s}}.\mathbf{E}^i(\mathbf{r}) = jk_0Z_0 \int_C \left[\hat{\mathbf{s}}.\hat{\mathbf{s}}'I(s') + \frac{1}{k_0^2}\frac{\partial I(s')}{\partial s'}\frac{\partial}{\partial s}\right] G(\mathbf{r}|\mathbf{r}')ds', \tag{2}$$

where k_0 and Z_0 are the free space propagation constant and characteristic impedance, respectively, the space curve C traces the wire geometry, and $\hat{\mathbf{s}}$ is the unit tangent vector along this curve. In the method of moments, the unknown wire current I(s) is discretized using a suitable set of basis functions. Pulse, triangular, cubic spline and piecewise sinusoidal functions are some of the popular choices for the expansion basis. The discretized integral equation is then tested using a suitable testing scheme to produce a system of linear algebraic equations. Point matching and Galerkin's technique are the most widely used testing schemes in MoM implementations. Once the linear system is solved and the unknown expansion coefficients are determined, the current distribution on the wires and near-field and far-field characteristics of the antenna such as input impedance, radiation pattern, beamwidth, etc., can easily be calculated.

In a wavelet-based MoM implementation of the wire structure, the unknown wire current is expanded in a multiresolution basis, containing scaling functions at the lowest resolution level plus wavelets at this and higher resolution levels up the desired degree of accuracy. We utilize an intervallic multiresolution analysis (MRA) which is naturally defined over a bounded interval. Specifically, the B-spline intervallic MRA is used in this paper. Intervallic expansions contain inner basis functions identical to the regular multiresolution expansions plus special edge basis functions which satisfy the desired boundary conditions of the problem. Thus, a typical intervallic multiresolution expansion looks like the following form:

$$\begin{aligned} f(x) \approx & \sum_{n=1}^{N_\phi^{(i)}(m_0)} c_n^{(i)}\phi(2^{m_0}x-n) + \sum_{l=1}^{N_\phi^{(e)}} c_l^{(e)}\phi_l^{(e)}(2^{m_0}x) \\ & + \sum_{m=m_0}^{M-1}\left[\sum_{n=1}^{N_\psi^{(i)}(m)} d_{m,n}^{(i)}\psi(2^m x-n) + \sum_{l=1}^{N_\psi^{(e)}} d_l^{(e)}\psi_l^{(e)}(2^m x)\right], \end{aligned} \tag{3}$$

where M is the highest resolution level required in the problem, $\phi(x)$ and $\psi(x)$ are the inner scaling function and wavelet, respectively, and $\phi_l^{(e)}(x)$ and $\psi_l^{(e)}(x)$ are the edge scaling functions and wavelets, respectively. Note that the number of shifted inner scaling functions and shifted inner wavelets depend on the resolution levels, while the number of edge scaling functions and edge wavelets are independent of the resolution levels and depend only on the order of the intervallic MRA. According to the definition of the MRA, the expansion of equation (3) is equivalent to the following high-resolution expansion made up of only scaling functions:

$$f(x) \approx \sum_{n=1}^{N_s^{(i)}(M)} c_n^{(i)} \phi(2^M x - n) + \sum_{l=1}^{N_s^{(e)}} c_l^{(e)} \phi_l^{(e)}(2^M x). \tag{4}$$

The equivalence between the two expansions (3) and (4) is a very important feature of the MRA, which indeed forms the basis of the fast wavelet transform (FWT). Using this algorithm, it suffices to compute the expansion coefficients of only scaling functions at the highest resolution level. The expansion coefficients of all other basis functions at lower resolutions can be computed recursively from these high resolution scaling coefficients. The aforementioned equivalence can be exploited in a very useful way. Suppose that the wire structure has already been discretized using a high resolution grid, and the impedance matrix has been computed at this resolution level. A MoM expansion composed of only high resolution scaling functions leads to a full moment matrix as discussed before. However, using the FWT, one can transform the high resolution scaling-only grid into a wavelet-dominated multiresolution grid at lower resolution levels. It is now the cancellation effect of the wavelet basis functions which will render the impedance matrix highly sparse. It should be noted that such transformation does not involve the tedious numerical integration task, which is carried out once during the computation of the original high resolution scaling-only matrix.

III. RESULTS AND CONCLUSION

The formulation developed in the previous section has been applied to a variety of wire antennas and scatterers including dipole arrays, loops, helical and other curvilinear antennas, etc. In all cases, the geometry of the antenna or scatterer is parameterized appropriately, and integral equation (2) is implemented. The structure is first discretized using a high resolution scaling grid. At this stage, one can employ the symmetries of the geometry, if any, to speed up the matrix fill process. Then using the fast wavelet transform, a wavelet-dominated multiresolution grid is generated, and its associated impedance matrix is computed from the original matrix through simple digital filters. The resulting sparse matrices are thresholded by discarding all the elements whose magnitudes fall below a certain threshold level with respect to the largest matrix element. Two or three resolution levels are typically used for the multiresolution grid, and normally threshold levels as high as 0.1% yield very satisfactory results. This is mostly due to the fact that the singularity of the kernel of the integral equations is avoided through the use of the thin wire approximation. Another important feature of this formulation is that in large structures which involve a large number of basis functions spread all over the geometry, it is possible to identify all negligible interactions which will be subject to thresholding. This pre-sorting is based on the premise that the Green's function is a function of only the distance between the source and observation points and not their absolute positions. A major acceleration of the matrix fill process can thus be achieved by skipping the numerical evaluation of the trivial interactions. After the impedance matrix has been rendered sparse due to thresholding, a sparse-based preconditioned biconjugate gradient (BiCG) solver is employed to solve the linear system. Due to the improvement of the system condition number, the BiCG solver usually converges very fast.

As an example, here we consider a two-element and a three-element array of full-wavelength dipoles of identical feeds with half wavelength separations. Figs. 1 and 2 show the current distribution on the center dipole of these arrays. The effect of the thresholding process and the threshold level on the current distribution have been explored in these figure. It is seen that at a threshold level of 0.1%, the current distribution is almost indistinguishable from the original distribution with no thresholding applied at all. While, the resulting wavelet-dominated matrices exhibit sparsity levels of 83% and 94.3% for the two- and three-element arrays, respectively. In particular, when the far-field characteristics are of primary interest, the threshold level can be raised to a much higher value without affecting the radiation pattern drastically. More numerical results including different types of wire antennas will be presented at the conference.

REFERENCES

[1] B.Z. Steinberg and Y. Leviatan, "On the use of wavelet expansions in the method of moments," *IEEE Trans. Antennas Propagat.*, vol. AP-41, pp. 610-619, May 1993.

[2] K.F. Sabet, "Wavelet-based modeling of microwave circuits and antennas," in *MTT-S Workshop Digest: Applications of Wavelets to Electromagnetics*, Organizers: L.P.B. Katehi and H. Ling, June 1996.

[3] K.F. Sabet and L.P.B. Katehi, "Analysis of integrated millimeter-wave and submillimeter-wave waveguides using orthonormal wavelet expansions," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-42, pp. 2412-2422, Dec. 1994.

[4] K.F. Sabet, J-C. Cheng and L.P.B. Katehi, "Efficient wavelet-based modeling of printed circuit antennas and arrays," submitted for publication.

[5] K.F. Sabet, K. Sarabandi and D. Zahn, "A Study of scattering from curvilinear surfaces based on wavelet concepts," in *URSI Radio Science Meeting*, July 1996.

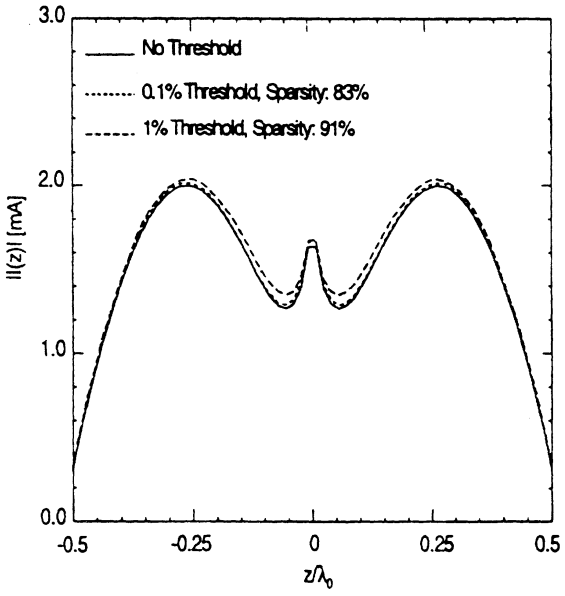


Fig. 1. Current distribution on a two-element dipole array (l=λ, s= λ/2).

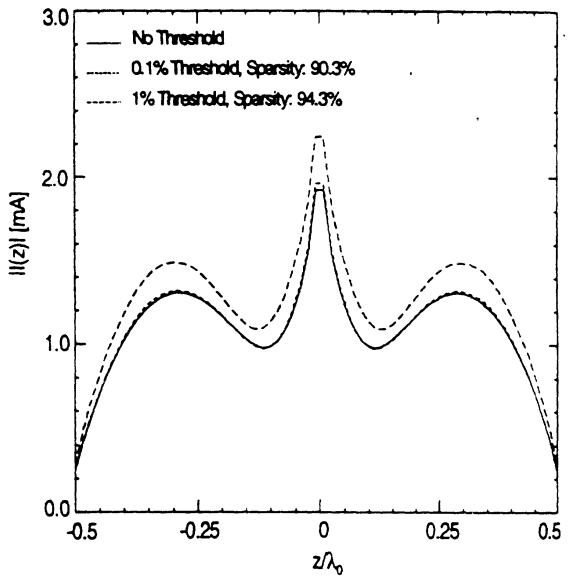


Fig. 2. Current distribution on the center dipole of a three-element dipole array (l=λ, s= λ/2).

APPLICATIONS OF MULTIRESOLUTION BASED FDTD MULTIGRID

Kavita Goverdhanam, Linda P.B. Katehi
Radiation Laboratory, Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI 48109–2122

Andreas Cangellaris
Department of Electrical Engineering
University of Arizona, Tucson, AZ

Abstract- A Multigrid 2-D Finite Difference Time Domain (FDTD) technique based on Multiresolution analysis with Haar wavelets is used to analyze structures such as an empty waveguide and a shielded stripline. The results obtained are compared with those computed using a finer resolution regular FDTD mesh. This comparative study illustrates the benefits of using wavelets in FDTD analysis.

I Introduction

Multiresolution Time Domain (MRTD) Technique is a new approach to solving time domain problems. This technique uses Multiresolution Analysis (MRA) to Discretize Maxwell's equations in time domain and demonstrates excellent capability in solving Electromagnetics problems [1], [2]. Depending on the choice of basis functions, several different schemes result, each one carrying the signature of the basis functions used in MRA. It is also important to note that the design of an MRTD scheme can be accomplished using one's own application-specific basis functions. MRTD technique using Haar scaling functions results in the FDTD technique [3].

Recently, an FDTD multigrid using the Haar wavelet basis has been developed and it has been demonstrated that such a scheme exhibits highly linear dispersion characteristics [3]. Motivation for this work stems from the theory of MRA which says that a function which is expanded in terms of scaling functions of a lower resolution level, m1, can be improved to a higher resolution level, m2, by using wavelets of the intermediate levels. In other words, expanding a function using scaling function of resolution level m1 and wavelets up to resolution level m2 gives the same accuracy as expanding the function using just the scaling functions of resolution m2. However, the use of wavelet expansions has major implications in memory savings due to the fact that the wavelet expansion coefficients are significant only in areas of rapid field variations. This allows for the capability to discard wavelet expansion coefficients where they are not significant thereby leading to significant economy in memory. Different resolutions of wavelets can be combined so as to locally improve the accuracy of the approximation of the unknown function. This, combined with the fact that wavelet coefficients are significant only at abrupt field variations and discontinuities allows MRTD to lend itself very naturally to a Multigrid capability.

In this paper, a 2D MRTD scheme based on Haar basis functions (first order resolution) is developed and applied to solve for the Electromagnetic fields in a

waveguide and a shielded stripline. The results obtained are compared with those computed using conventional FDTD technique. It will be shown that the wavelet coefficients are significant only at locations with abrupt field variations. This facilitates in obtaining accurate solutions by combining the wavelet and scaling coefficients only in regions where the wavelet coefficients are significant (discontinuities).

II The 2D-MRTD scheme

Consider the following 2-D scalar equation obtained from Maxwell's H-curl equation:

$$\epsilon \frac{\partial E_x}{\partial t} = \frac{\partial H_z}{\partial y} + \beta H_y \qquad (1)$$

This equation can be rewritten in a differential operator form as shown below:

$$L_1(f_1(x,y,t)) + L_2(f_2(x,y,t)) = g \qquad (2)$$

where L_1 and L_2 are the operators and f_1(x,y,t) and f_2(x,y,t) represent the electric/magnetic fields. We now expand the fields using a Haar based MRA with scaling functions ϕ and wavelet functions ψ [3]. The field expansion can be represented as follows:

$$f(x,y,t) = [A][\phi(x)\phi(y)] + [B][\phi(x)\psi(y)] + [C][\psi(x)\phi(y)] + [D][\psi(x)\psi(y)] \qquad (3)$$

where $[\phi(x)\phi(y)]$, $[\phi(x)\psi(y)]$, $[\psi(x)\phi(y)]$ and $[\psi(x)\psi(y)]$ represent matrices whose elements are the corresponding basis functions in the computation domain of interest and [A], [B], [C], [D] represent the matrices of the unknown coefficients which give information about the fields and their derivatives.

Application of Galerkin's technique leads to four schemes which can be represented as follows:

$$< [\phi\phi], L_1(f_1) + L_2(f_2) >=< [\phi\phi], g >: \phi\phi Scheme$$
$$< [\phi\psi], L_1(f_1) + L_2(f_2) >=< [\phi\psi], g >: \phi\psi Scheme$$
$$< [\psi\phi], L_1(f_1) + L_2(f_2) >=< [\psi\phi], g >: \psi\phi Scheme$$
$$< [\psi\psi], L_1(f_1) + L_2(f_2) >=< [\psi\psi], g >: \psi\psi Scheme$$

From this system, we obtain a set of simultaneous discretized equations. For the first resolution level of Haar wavelets, the above four schemes decouple and coupling can be achieved only through the excitation term and the boundaries.

The shielded structures analyzed here are terminated at Perfect Electric Conductors (PEC) and the boundary conditions are obtained by applying the natural boundary condition for the electric field on a PEC as shown below:

$$E_t^{\phi\phi}\phi(x)\phi(y) + E_t^{\phi\psi}\phi(x)\psi(y) + E_t^{\psi\phi}\psi(x)\phi(y) + E_t^{\psi\psi}\psi(x)\psi(y) = 0....AtPEC. \qquad (4)$$

where $E_t^{\phi\phi}$, $E_t^{\phi\psi}$, $E_t^{\psi\phi}$ and $E_t^{\psi\psi}$ are the scaling and wavelet coefficients of the tangential electric field at the boundary nodes.

The above equations are discretized by the use of Galerkin's method which results in a set of matrix equations of order N = M+1 where M is the order of the considered wavelet resolutions. These equations are solved simultaneously with the discretized Maxwell's equations to numerically apply the correct boundary conditions.

III Applications of 2D FDTD Multigrid and Results

The 2-D MRTD scheme derived above has been applied to analyze the Electromagnetic fields in a waveguide and a shielded stripline.

(a) Waveguide: An empty waveguide with cross-section of 12.7 x 25.4 mm is chosen. A coarse 5 x 8 mesh is used to discretize this mesh and 2D MRTD technique was applied to analyze the fields in this geometry. Fig. 1 shows the amplitudes of the wavelet and scaling coefficients of the electric field obtained by using MRTD technique. From this figure it can be seen that only the $\phi\phi$ and $\phi\psi$ coefficients make a significant contribution to the field and that the contribution of $\psi\phi$ and $\psi\psi$ is negligible. From the computed

coefficients, the total field is reconstructed using an appropriate combination of the scaling and significant wavelet coefficients. For the waveguide chosen here, elimination of the wavelet coefficients that have no significant contribution leads to 480 unknowns. The reconstructed field obtained by this mesh has the same accuracy as that of a 10 x 16 FDTD mesh with 960 unknowns which is in agreement with the theory of MRA. Fig. 2 shows the results of this comparison and demonstrates that the use of multigrid scheme provides a 50% economy in memory.

(b) Shielded Stripline : Next, a stripline of width 1.27mm is considered. It is enclosed in a cavity of area 12.7 x 12.7 mm so that the side walls are sufficiently far away to not affect the propagation. The strip is placed 12.7mm from the ground. A 40 x 40 mesh is used to analyze the fields in this geometry with the 2D MRTD technique. Fig. 3 shows the derived scaling and wavelet coefficients of the fields just below the strip. From the figure, it can be seen that among the wavelet coefficients, only $\psi\phi$ makes a significant contribution close to the vicinity of the strip where the field variation is rather abrupt. Fig. 4 shows the comparision of the total reconstructed field in the 40 x 40 MRTD mesh with that of a 40 x 40 and 80 x 80 FDTD mesh. From the figure it is clear that the field computed by 40 x 40 MRTD mesh using only the significant wavelet coefficients follows the results of the finer 80x80 mesh very closely, demonstrating once again the significant economy in memory as illustrated in Table 1. Fig. 5 shows the Normal Electric field plot of the strip and the variable mesh resulting from MRTD.

IV Conclusion

A Haar wavelet based 2D MRTD scheme was developed and applied to analyse the fields in a waveguide and a shielded stripline. The wavelet coefficients obtained are significant only in regions of rapid field variations. Thus the FDTD multigrid capability using MRTD technique has demonstrated significant economy in memory.

Table 1: Comparison of the memory requirements in FDTD and MRTD techniques

Technique	Unknown Coeff.
40x40 FDTD	9600
40x40 MRTD	11328
80x80 FDTD	38400

V Acknowledgments

The authors are greatful to NSF and ARO for their support.

References

[1] M.Krumpholz, L.P.B.Katehi, "New Prospects for Time Domain Analysis", IEEE Microwave and Guided Wave Letters, pp. 382-384, November 1995.

[2] M.Krumpholz, L.P.B.Katehi, "MRTD: New Time Domain Schemes Based on Multiresolution Analysis", IEEE Transactions on Microwave Theory and Techniques, pp. 385-391, April 1996.

[3] K.Goverdhanam, E.Tentzeris, M.Krumpholz and L.P.B. Katehi, "An FDTD Multigrid based on Multiresolution Analysis", Proc. AP-S 1996, pp. 352-355.

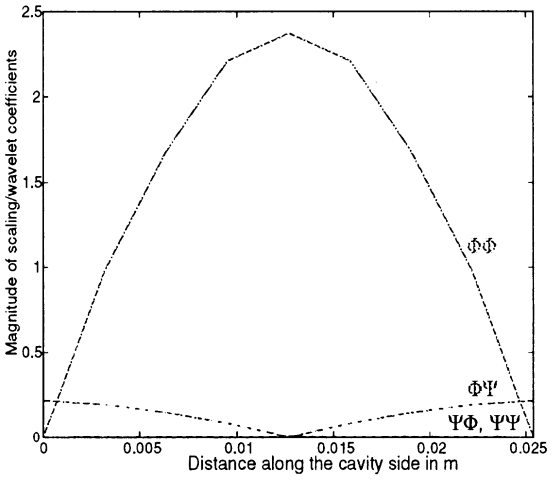


Figure 1: Amplitudes of Scaling and Wavelet Coefficients in a Waveguide.

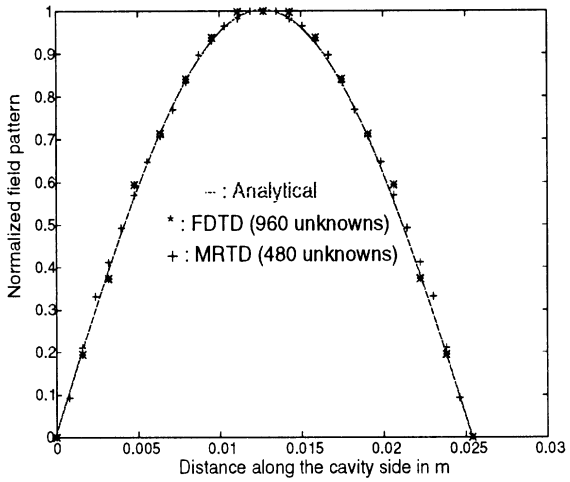


Figure 2: Comparison of MRTD, FDTD and Analytical Fields in a Waveguide.

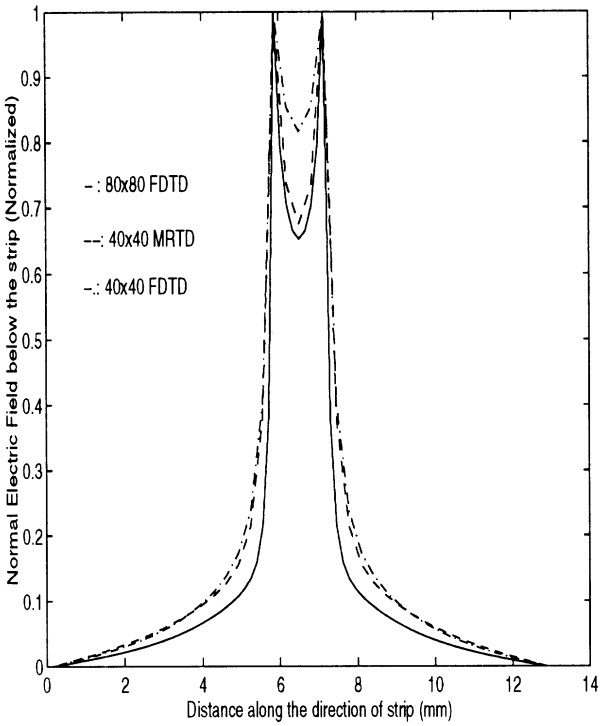


Figure 4: Comparison of Normal Electric Field under a stripline using MRTD and FDTD techniques.

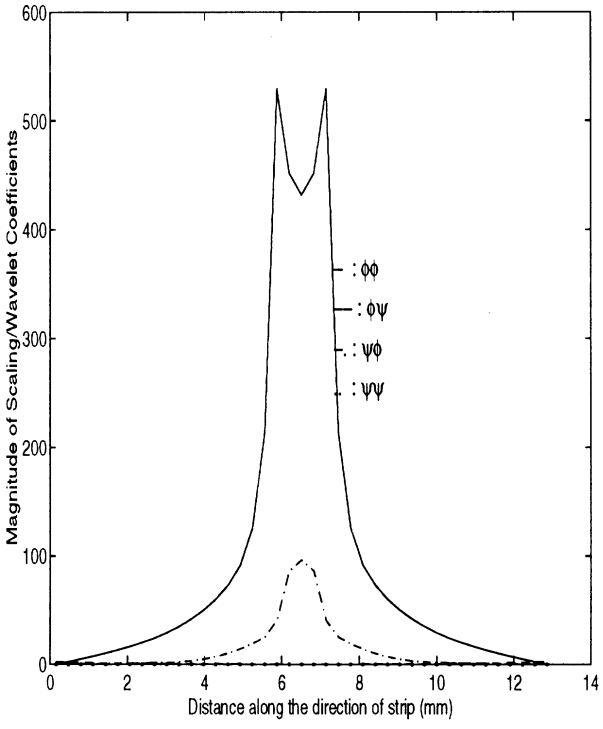


Figure 3: Amplitudes of Scaling and Wavelet Coefficients of a Shielded Stripline.

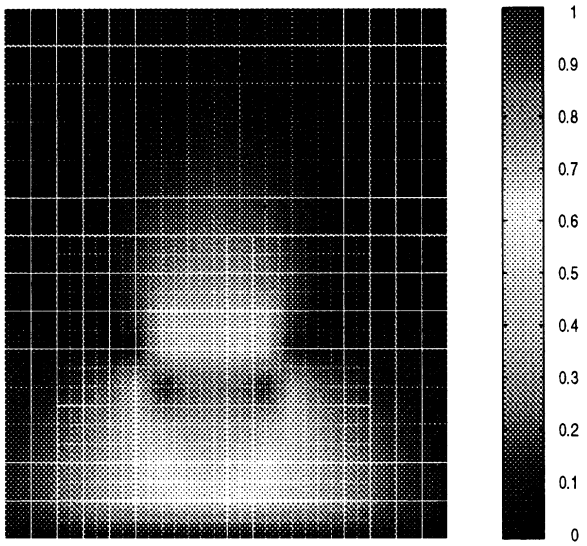


Figure 5: FDTD Multigrid and Field Plot of the Stripline.

Micro-Coplanar Striplines - New Transmission Media for Microwave Applications

Kavita Goverdhanam[1], Rainee N. Simons[2], Linda P.B. Katehi[1]
[1]Radiation Laboratory, EECS Department, University of Michigan,
Ann Arbor, MI 48109-2122, USA
[2]NASA Lewis Research Center NYMA Group, Cleveland, OH 44135

Abstract

In this paper a new transmission line for microwave applications, referred to here as the Micro-Coplanar Stripline (MCPS), is introduced. The propagation characteristics, such as, characteristic impedance (Z_o) and effective dielectric constant (ϵ_{eff}) for a range of MCPS geometries have been modeled using the Finite Difference Time Domain (FDTD) Technique and presented here. Also, preliminary experimental results on the performance of an MCPS-Microstrip transition and an MCPS-fed patch antenna are presented. The results indicate several potential applications of the MCPS line in microwave integrated circuit technology.

I Introduction

In recent years, wireless communications for audio, video and data transmission have witnessed tremendous growth. The essential requirements for these wireless systems are low cost for affordability and small size for portability. One approach in addressing low-cost requirements is to combine the available digital silicon processing technology with the high frequency silicon germanium device technology. The size and complexity issues that arise with this integration can be addressed by investigating novel integration techniques which rely on multilayer three dimensional transmission lines constructed using very thin glass or silicon dioxide layers. With appropriate interconnect technology available, customized innovative integrated packages can be realized by micromachining the silicon wafer [1]. These techniques, when realized, have the potential to meet the ever increasing demand to lower the cost and size of circuit components.

This paper presents a new transmission line, the Micro-Coplanar Stripline (MCPS). Fig. 1 shows the geometry of MCPS. The MCPS is fabricated on a high resistivity silicon (HR Si) wafer and has a very thin spin-on-glass (SOG) as a spacer layer separating two strip conductors. MCPS has several advantages some of which are discussed here: 1) The dimensions of the strip conductors as well as the spacer layer are of the order of a few microns for a 50 Ω transmission line. Thus the transmission line is very compact, resulting in small amount of parasitics when combined with active devices. 2) The strip conductors are on two levels, thus making vertical as well as horizontal integration possible. This can be useful in applications such as mixers using broad-side couplers with tight coupling and wide bandwidth. 3) The spacer layer is very thin, hence making it possible to realize large capacitances in a small area. This feature is very desirable in the design of compact lowpass and bandpass filters. 4) The two strip conductors form a balanced line, making the MCPS an ideal line for feeding integrated antennas, such as, patches, bowties and dipoles.

A number of variants of this basic structure, a few of which are shown in Fig. 2, can be used to achieve several advantages. Fig. 2a shows an insulating layer of Silicon dioxide (SiO_2) which can be used to effectively isolate the RF MCPS from the conductive properties of the low resistivity silicon (LR Si) wafer (few Ohms-cm) below. The advantage gained is that CMOS based circuits for signal processing on LR Si can coexist with the RF circuits thereby simplifying integration. Fig. 2b shows a possible configuration using HR Si wafer (> 3000 ohm-cm). The advantage here is that the HR Si wafer will lower the attan-

uation and also improve isolation between adjacent circuits. The additional dielectric layer can be used to improve field confinement or for building RF circuits. Fig. 2c shows a geometry where the upper dielectric layer is replaced by an LR Si wafer with an etched groove which can serve as a metal cover or a ground plane for circuits located above. The last configuration, shown in Fig. 2d, is an MCPS which is shielded and suspended inside an enclosure formed by two LR Si wafers with etched grooves. This line is expected to have very low attenuation since the ϵ_{eff} is approximately equal to that of air. Such a transmission line is ideal for constructing feed systems for high gain, high efficiency planar array antennas.

In the following sections, first, a brief description of the fabrication process for the MCPS is presented. Next, the propagation parameters of the MCPS, such as, Z_o and ϵ_{eff} for a range of MCPS geometries is presented. These have been modeled by using the well known FDTD technique [2], [3], [4]. Finally, to demonstrate the applications of this line, preliminary experimental results on an MCPS-Microstrip broadband transition and a feed network for a patch antenna have been presented. The experimental work was performed using a Duroid based MCPS line for the purpose of validating the applicability of the novel transmission line. Fabrication and measurement of SOG-on-Silicon based MCPS lines is currently in progress.

II Fabrication of MCPS:

To begin the fabrication process, the lower strip conductor is fabricated on the substrate (ϵ_{r2}) by a lift-off process [5]. Next, the dielectric spacer layer (ϵ_{r1}) is built-up to the required thickness by multiple spin-coats. Lastly, the upper strip conductor is fabricated using the lift-off process once again. An HR Si (> 3000 ohms-cm) silicon wafer is used as the base substrate and the gold metalization of about 1.0 μm thickness is used as the conductor. Accuglass 512 SOG is used as the dielectric spacer layer. The dielectric constant and thickness of the Accuglass used here are 3.1 and 2.5 μm respectively. If a higher dielectric constant or thicker layer is required, it is preferable to use other spin coating materials, such as, polyamides.

III Characteristics of MCPS.

A number of MCPS geometries have been characterized using the FDTD technique in order to obtain the characteristic impedance and effective dielectric constant. For these lines, a 400 μm thick Silicon substrate ($\epsilon_{r2} = 11.7$) is chosen. The thickness of glass ($\epsilon_{r1} = 3.1$) is 2.5 μm. Tables 1 and 2 below summarize the Z_o and ϵ_{eff} for SOG-on-Silicon MCPS with line widths (W) 135 μm and 94.5 μm respectively for overlap (S) ranging from positive (+27μm) to negative (-27μm). Here, '+' indicates an overlap between the lines and '-' indicates a separation. From the tables, it can be seen that as the overlap distance between the MCP strips increases, the characteristic impedance decreases. This is because with increasing overlap, the coupling (capacitance) between the lines increases, thereby reducing Z_o. Also it is seen that lowering the stripwidth increases Z_o. From these, it is obvious that by varying the parameters involved, a wide range of desired characteristic impedances can be obtained.

While the above line dimensions are useful for feeding patch antennas and transitions, for integrating CMOS with RF circuits, lines with much smaller dimensions are required. It has been found that a line with W = 10 μm and S = 4 μm yields characteristic impedance close to 50 Ω. Fabrication of this line on HR Si with a 2.5 μm SOG spacer layer is in progress. Although Fig. 1 does not show the probe pads, this line will be characterized using standard on-wafer RF probing equipment.

Table 1: Z_o and ϵ_{eff} of SOG-on-Silicon MCPS: D_1 = 2.5μm, D_2 = 400μm, W = 135μm

Overlap S (μm)	Z_o (Ω)	ϵ_{eff}
+27.0	10.7	3.49
+13.5	14.0	3.67
0.0	22.4	4.02
-13.5	51.2	5.61
-27.0	59.0	5.89

IV Applications of MCPS:

In order to demonstrate the efficacy of this line, a broadband MCPS-Microstrip transition and an MCPS fed Patch antenna have been experimentally

Table 2: Z_o and ϵ_{eff} of SOG-on-Silicon MCPS: D_1 = 2.5μm, D_2 = 400μm, W = 94.5μm

Overlap S (μm)	Z_o (Ω)	ϵ_{eff}
+27.0	11.1	3.40
+13.5	14.6	3.59
0.0	23.9	3.94
-13.5	58.4	5.50
-27.0	66.6	5.79

characterized. In doing so, MCPS circuits fabricated on 254 μm and 127 μm thick Duroid have been used.

a) **MCPS-Microstrip broadband transition:** The schematic of an MCPS-to-Microstrip back-to-back transition is shown in Fig. 3. In the figure, section A - B corresponds to the microstrip line while section C - D corresponds to the MCPS. The transition consists of a short length of a 50 Ω microstrip line of width 254 μm whose ground plane is abruptly truncated. At this plane, the tapered MCPS strip conductors form a junction with the microstrip line. At the junction, the tapered section of the MCPS conductors form a symmetric parallel plate line. The conductors of the parallel plate are flared out in opposite directions, forming the regular MCPS with W = 889 μm while facilitating impedance and mode matching. The relevant parameters of this geometry are as follows:
D_1 = 254 μm; ϵ_{r1} = 10.5; ϵ_{r2} = 1; W = 889 μm; W_1 = 254 μm. Fig. 4 shows the measured S_{11} and S_{21} of this transition. From the figure it can be seen that the insertion loss of the transition is close to 0.7 dB at the center frequency of 7 GHz and has a maximum value of 1.0 dB at 14 GHz. This includes the losses due to the two coaxial launchers of the Wilton test fixture which are of the order of 0.25 dB each. Thus it can be seen that deembedding will further reduce the insertion loss to 0.2 dB at 7 GHz, with the maximum loss being 0.5 dB at 14 GHz. These results indicate that the transition has excellent characteristics over a broad range of operation.

b) **MCPS Feed for a Patch Antenna:** The schematic of an MCPS fed patch antenna which is designed to operate at 19 GHz is shown in Fig. 5. In this circuit, power is coupled to the patch radiator through an MCPS-to-Microstrip transition. An interesting feature of this feeding network is that it can provide an optimum substrate for a given frequency band of operation by proper choice of the spacer layer thickness D_1 and dielectric constant ϵ_{r1}. The parameters of this circuit are given below:
D_1 = 127 μm ; ϵ_{r1} = 10.8; D_2 = 762 μm; ϵ_{r2} = 10.2; a = 3429 μm; b = 2286 μm. The measured return loss S_{11} of the antenna using an RF wafer probe (10 mil pitch) is shown in Fig. 6. As seen from the figure, the patch antenna resonates at 18.1 GHz while it is designed to resonate at 19.0 GHz. This shift is due to the parasitics added by the MCPS section which have not been deembedded. It can be seen from the figure that the antenna is well matched to the feed. This demonstrates the feasibility of using MCPS as feed lines in the design of antenna arrays for wireless applications.

V Conclusion

A new transmission line, the MCPS, which has the potential to provide extremely compact and low cost circuits with wide design flexibility has been introduced. The propagation characteristics for a wide range of circuit parameters have been presented. Also, the applications of this line has been demonstrated by characterizing an MCPS-Microstrip transition and an MCP-fed Patch antenna.

VI Acknowledgments

The authors are greatful to ONR (N00014-95-1-0546) for its support.

References

[1] R. F. Drayton and L. P. B. Katehi, "Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques", IEEE Trans. Microwave Theory Tech., Vol. 43, No. 9, pp. 2073 - 2080, Sept. 1995.

[2] X. Zhang and K. K. Mei, "Time-Domain Finite Difference Approach to the Calculation of the Frequency-Dependent Characteristics of Microstrip Discontinuities", IEEE Trans. Microwave Theory Tech., Vol. 36, pp. 1775 - 1787, Dec 1988.

[3] K. Goverdhanam, R. N. Simons and L. P. B. Katehi, "Coplanar Stripline Propagation Characteristics and Bandpass Filter", IEEE Microwave and Guided Wave Letters, Vol. 7, No. 8, pp. 214-216, August 1997.

[4] K. Goverdhanam, R. N. Simons and L. P. B. Katehi, "Coplanar Stripline Components for High-Frequency Applications", IEEE Trans. on Microwave Theory and Techniques, Vol. 45, No. 10, pp. 1725-1729, October 1997.

[5] R. Williams, "Modern GaAs Processing Methods", 2nd ed., Ch. 6, pp. 116, Artech House Inc., MA: Dedham, 1990.

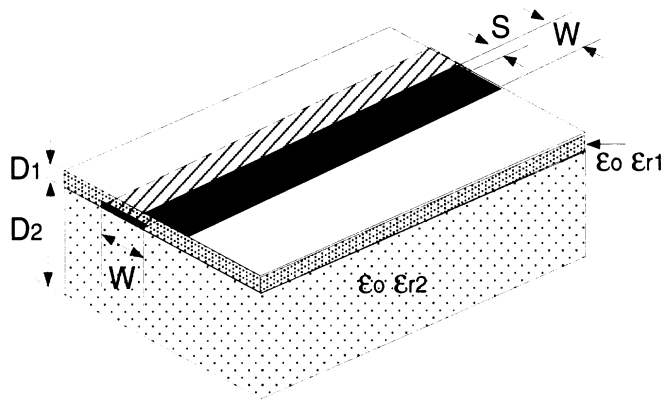


Figure 1: Geometry of MCPS line

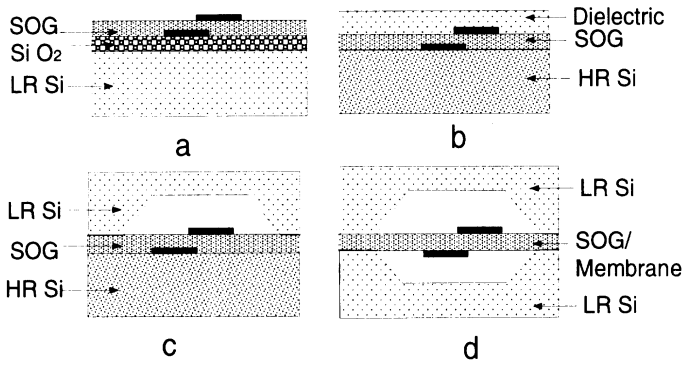


Figure 2: MCPS Variants.

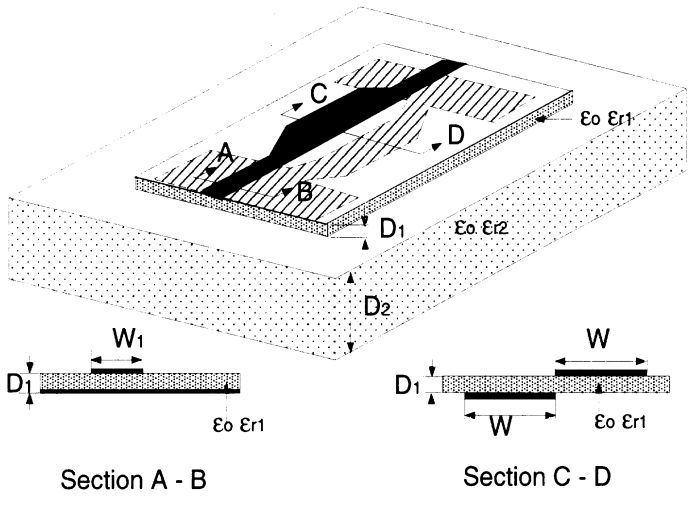


Figure 3: MCPS-Microstrip Transition.

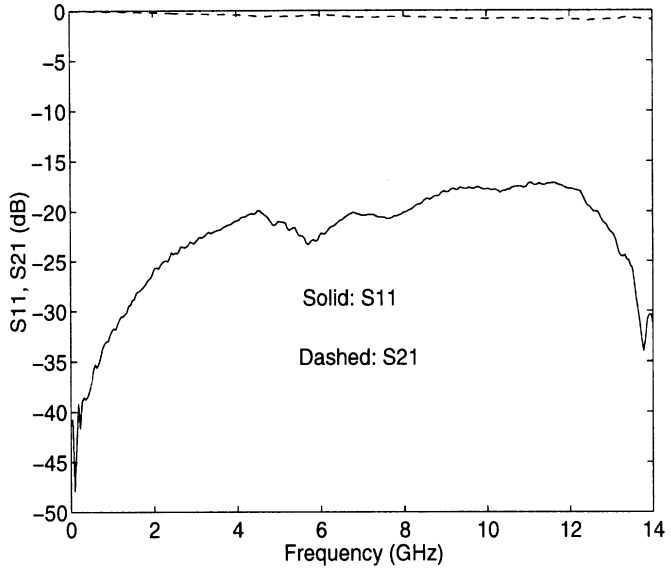


Figure 4: S_{11} and S_{21} of MCPS-Microstrip Transition.

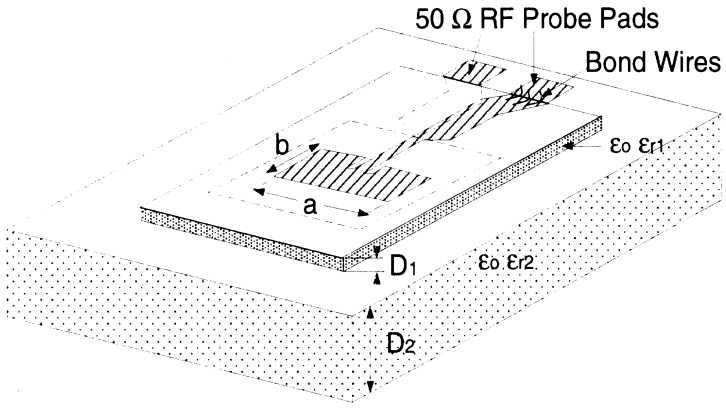


Figure 5: Patch Antenna with MCPS Feed.

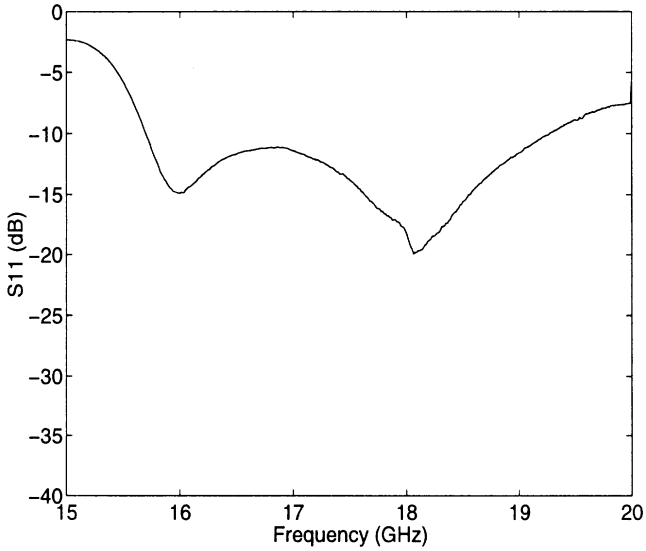


Figure 6: Return loss on MCPS-fed Patch Antenna.

TREATMENT OF BOUNDARIES IN MULTIRESOLUTION BASED FDTD MULTIGRID

Kavita Goverdhanam, Emmanouil Tentzeris, Linda P.B. Katehi
Radiation Laboratory, EECS Department, University of Michigan,
Ann Arbor, MI 48109-2122, USA

I Introduction

In the last few years, Multiresolution analysis has been successfully applied to finite difference time domain (FDTD) technique in solving a variety of electromagnetic problems [1], [2], [4], [5]. Multiresolution Time Domain (MRTD) approach uses Multiresolution Analysis (MRA) to discretize Maxwell's equations in time domain. The Electric and Magnetic field components are expanded in terms of scaling as well as wavelet bases. The new discretized equations can be derived by applying the Method of Moments in space and time domain. MRTD technique has demonstrated excellent capability in solving Electromagnetics problems [1], [2], [4], [5]. This technique lends itself very naturally to multigrid schemes due to the combined use of scaling and wavelet functions in selective regions of the computational domain.

The advantage of using a combination of wavelets and lower resolution scaling bases instead of higher resolution scaling functions alone is that wavelet coefficients are significant only in the areas of strong field variation and coefficients below a certain threshold level can be dropped without adversely affecting the conditioning of the formulated mathematical problem. This leads to significant economy in memory and computation time while enhancing field resolution in selective regions where both scaling and wavelet coefficients are used.

The use of different basis functions leads to a variety of MRTD schemes, each one carrying the signature of the basis used. Recently, MRTD based on Haar and Battle-Lemarie functions have been successfully applied to microwave propagation and transmission problems [4], [5]. In all these schemes, the method of formulation of the appropriate boundary condition at discontinuities is not very obvious. This paper focuses on the methodology of applying specific boundary conditions at dielectric and metal interfaces. Also, included is a discussion of MRTD as applied at the source region.

II 3-D Haar-MRTD Scheme

For simplicity we begin with of the 3D MRTD scheme with wavelets along the z direction. Consider the following equation obtained from Maxwell's H-curl equation:

$$\epsilon \frac{\partial E_x}{\partial t} = \frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} \tag{1}$$

This equation is rewritten in a differential operator form as shown below:

$$L_1(f_1(x,y,z,t)) + L_2(f_2(x,y,z,t)) = g \tag{2}$$

where L_1 and L_2 are the operators and f_1(x,y,z,t) and f_2(x,y,z,t) represent the electric/magnetic fields. We now expand the fields using the Haar based MRA with scaling functions ϕ in all three directions

and wavelet functions ψ [3] in the z direction alone. The field expansion can be represented as follows:

$$f(x,y,z,t) = [A][\phi(t)\phi(x)\phi(y)\phi(z)] + [B][\phi(t)\phi(x)\phi(y)\psi(z)] \quad (3)$$

where $[\phi(t)\phi(x)\phi(y)\phi(z)]$ and $[\phi(t)\phi(x)\phi(y)\psi(z)]$ represent matrices whose elements are the corresponding basis functions in the computation domain of interest and, [A] and [B] represent the matrices of the unknown coefficients which give information about the fields and their derivatives.

Application of Galerkin's technique leads to the following schemes:

$$< [\phi\phi\phi], L_1(f_1) + L_2(f_2) >=< [\phi\phi\phi], g >: \phi\phi\phi Scheme$$
$$< [\phi\phi\psi], L_1(f_1) + L_2(f_2) >=< [\phi\phi\psi], g >: \phi\phi\psi Scheme$$

Thus, by sampling Maxwell's differential equations with scaling and wavelet functions, we obtain a set of simultaneous discretized equations. For the first resolution level of Haar wavelets, the above schemes decouple and coupling can be achieved only through the excitation term and boundaries. In the following sections, the conditions to be applied at these locations will be discussed.

For the Haar based MRTD scheme, the parallel plate waveguide shown in Fig. 1 is used to illustrate the treatment of the aforementioned interfaces. The plates are assumed to be infinite in width for simplicity and are separated by a distance of 24mm. A single mode (TEM) operation is chosen throughout this study. For simplicity, the examples in the following sections specifically focus on MRTD scheme with only the first level of wavelet resolution. However, this techniques could easily be extended to a general scheme with multiple levels of wavelets.

In characterizing the circuits below, the Perfectly Matched Layer (PML) is used as an absorber. PML can be applied by assuming that the conductivity is given in terms of scaling and wavelet functions instead of pulse functions with respect to space [6]. The spatial distribution of the conductivity for the absorbing layers is modeled by assuming that the amplitudes of the scaling functions have a parabolic distribution. The MRTD mesh is terminated by a PEC at the end of each PML layer.

III Application of Source term in the Haar-MRTD scheme:

The considered parallel plate waveguide is excited such that it operates in the Dominant TEM mode. A signal with uniform spatial distribution along the waveguide cross section and Gaussian time distribution is chosen as the excitation. The amplitude of the scaling coefficients at the excitation plane is derived by sampling the excitation with pulse (Haar scaling) functions. The total electric field at the interface of the source and its adjacent cell must be continuous. Assuming that the field variation between these two cells is of the first order, it can be proved that the value of the first order wavelet coefficient is half that of the first derivative of the field. Thus, for a specific cell k with scaling and wavelet field amplitudes $E_k^{\phi\phi\phi}$ and $E_k^{\phi\phi\psi}$ respectively, the total field value at the position (k - 0.5)Δz equals $E^{+}_{tot,k-0.5} = E_k^{\phi\phi\phi} + 2E_k^{\phi\phi\psi}$ and location (k + 0.5)Δz equals $E^{-}_{tot,k+0.5} = E_k^{\phi\phi\phi} - 2E_k^{\phi\phi\psi}$. The amplitude of the wavelet coefficients at the excitation plane can be given by applying the continuity condition at the interface between the source and its adjacent cell: $E^{-}_{tot,k+0.5} = E^{+}_{tot,k+0.5}$. This leads to the following condition on the wavelet coefficients at the source location:

$$E_k^{\phi\phi\psi} = -0.5[E_{k+1}^{\phi\phi\phi} + 2E_{k+1}^{\phi\phi\psi} - E_k^{\phi\phi\phi}] \quad (4)$$

Figs 2. shows the scaling, wavelet and total electric fields, in a parallel plate waveguide which is shorted at one end with a PEC, without the use of the continuity condition, at an arbitrary time step after the incident pulse is reflected. It can be observed from the figure that the total field is not smooth; each cell interface introduces a spurious discontinuity. This implies that the coupled wavelet coefficients are not correct. Fig.3 on the other hand shows the scaling and wavelet coefficients along with the total field for the same geometry after applying the continuity equation (4). The smoothness of the total field here indicates that the wavelet coefficients have the right magnitude and phase when the source condition is applied. Without the continuity condition, the boundary conditions are satisfied only for the average field values (scaling coefficients), whereas, continuity condition ensures that the appropriate boundary conditions are satisfied on the total field which depends on the average field as well as the derivatives of the field (wavelet coefficients).

IV Treatment of PECs in the Haar-MRTD Scheme:

At the interface of a PEC, the total tangential Electric field is equal to 0. Since the location of the origin of the wavelet function coincides with the PEC, the requirement that the scaling functions have a zero value for this specific cell is a sufficient condition for the satisfaction of the boundary condition. Since the wavelet coefficients indicate the local derivatives of the field, they can have a nonzero value and can be calculated by applying continuity condition on the tangential electric field as shown in equation (4) above. For a PEC located at cell k = 0, applying equation (4) and noting that the scaling coefficient $E_0^{\phi\phi\phi}$ is zero at the PEC, we obtain the following equation for the wavelet coefficients.

$$E_0^{\phi\phi\psi} = -0.5[E_1^{\phi\phi\phi} + 2E_1^{\phi\phi\psi}] \tag{5}$$

Fig. 4 shows the reflected scaling, wavelet and total fields at an arbitrary instant of time in the aforementioned shorted parallel plate waveguide, before using equation (5) for the wavelet coefficient at the location of the PEC. Fig. 5 shows the same fields in the case where Equation (5) is used. The smoothness of the total electric field obtained here in contrast to the non-smooth field seen in Fig. 3 validates the necessity of applying the continuity condition at the PEC location.

V Treatment of Dielectric Interfaces in the Haar-MRTD Scheme:

At the interface of two dielectrics, the scaling and wavelet coefficients couple, even for the first order of wavelet resolution. Consider a dielectric interface at location k (assume the dielectric interface to be perpendicular to the direction of propagation) for the parallel plate waveguide considered above. Let the dielectric constant of the material to the left of the interface be ϵ_{r1} and that of the material to the right be ϵ_{r2}. By expanding the electric flux density (D) and electric field (E) in terms of the scaling and wavelet functions and applying the method of moments to the constitutive relationships, it can be shown that for the first resolution level of wavelets at the interface location k, their coefficients are related by the following coupled equations:

$$D_k^{\phi\phi\phi} = 0.5\epsilon_0[(\epsilon_{r1} + \epsilon_{r2})E_k^{\phi\phi\phi} + (\epsilon_{r1} - \epsilon_{r2})E_k^{\phi\phi\psi}] \tag{6}$$

$$D_k^{\phi\phi\psi} = 0.5\epsilon_0[(\epsilon_{r1} + \epsilon_{r2})E_k^{\phi\phi\psi} + (\epsilon_{r1} - \epsilon_{r2})E_k^{\phi\phi\phi}] \tag{7}$$

In addition to the coupled equations above, the continuity of the total tangential electric field at nodes adjacent to the interface needs to be ensured. Following the same procedure that leads to

equation (4), we obtain the following equations one cell to the left and right of the interface k.

$$E_{k-1}^{\phi\phi\psi} = +0.5[E_{k-2}^{\phi\phi\phi} - 2E_{k-2}^{\phi\phi\psi} - E_{k-1}^{\phi\phi\phi}] \quad (8)$$

$$E_{k+1}^{\phi\phi\psi} = -0.5[E_{k+2}^{\phi\phi\phi} + 2E_{k+2}^{\phi\phi\psi} - E_{k+1}^{\phi\phi\phi}] \quad (9)$$

Figs. 6 and 7 show plots of the scaling, wavelet and total flux density with and without the use of the above continuity equations respectively for the waveguide described above whose first half is filled with air and second half with a material of $\epsilon_r = 10$. As mentioned earlier, the plane of discontinuity in this case is perpendicular to the direction of propagation. The smoothness of the total field in Fig. 6 in comparison to its roughness in Fig. 5 validates the continuity conditions in equations 8 and 9.

VI Comparison with MRTD Schemes based on Entire-Domain Basis:

When entire-domain functions are used as scaling and wavelet basis for the development of Multiresolution schemes [2] [5], hard boundaries (e.g.PEC's) and excitation can be modeled in a similar way. E- and H- field components are expanded in terms of scaling and wavelet functions and the discretized equations are derived by using the method of moments. To obtain a desired excitation waveform at a certain position , a finite number of field coefficients surrounding the source point have to be updated. The stencil size varies from 8-12 for phase error less than 1^o per wavelength. The desired spatial distribution of the excitation is sampled with scaling and wavelet functions in space-domain to derive the appropriate coefficients for the neighboring points. Usually, the source is applied in the vicinity of one or more metallic planes. Unlike the FDTD where the consistency with the image theory is implicit in the application of the boundary conditions, for MRTD schemes based on entire-domain functions, this theory must be applied explicitly in the locations of Perfect Electric (PEC) or Magnetic Conductors (PMC). The total value of a field component at a specific cell is affected by a finite number of neighboring cells due to the entire-domain nature of the basis functions. Inserting the field expansions, the PEC boundary conditions of zeroing out the tangential-to-PEC E-field and the vertical-to-PEC H-field can be discretized by applying the method of moments. Due to the orthonormal nature of the expansion basis, it can be proved that the contribution of each neighbor at the location of the PEC has to be zero,a condition that can be satisfied with the explicit application of the Image theory. For example, even symmetry is applied for the normal-to-PEC electric field components and odd symmetry for the parallel-to-PEC. The Image Theory can be implemented automatically for an arbitrary number of hard boundaries.

Dielectric discontinuities are modeled by discretizing the constitutive relationships using the scaling and wavelet functions and solving a linear matrix equation [7]. Again, the stencil of the considered neighboring coefficients depends on the desired dispersion characteristics and usually range from 8-14 for dielectrics with ϵ smaller than 20. The conventional PML numerical absorber [8] can be extended assuming a spatial electric and magnetic conductivity distribution in terms of scaling and wavelet functions [6]. Generally, for MRTD Schemes based on entire-domain basis functions, the effect of discontinuities is not numerically localized, but is seen on a number of neighboring coefficients. Nevertheless, the procedure to apply the Boundary Conditions is the same for all MRTD schemes, though the details of implementation may be different.

VII Conclusion

The treatment of excitation condition, PEC boundaries and dielectric interfaces for the Haar as well as Entire Domain based MRTD schemes has been presented. These conditions have been validated by applying them to obtain the fields in a Parallel Plate waveguide. It has been shown that using the appropriate boundary conditions derived here is essential for obtaining smooth reconstructed fields.

VIII Acknowledgments

The authors are greatful to ONR (N00014-95-1-0546) and ARO (DAAH04-95-1-0321) for their support.

References

[1] M .Krumpholz, L. P. B. Katehi, "New Prospects for Time Domain Analysis", IEEE Microwave and Guided Wave Letters, pp. 382-384, November 1995.

[2] M. Krumpholz, L. P. B. Katehi, "MRTD: New Time Domain Schemes Based on Multiresolution Analysis", IEEE Transactions on Microwave Theory and Techniques, pp. 385-391, April 1996.

[3] K. Goverdhanam, E. Tentzeris, M. Krumpholz and L.P.B. Katehi, "An FDTD Multigrid based on Multiresolution Analysis", Proc. AP-S 1996, pp. 352-355.

[4] K. Goverdhanam, A. Cangellaris and L. P. B. Katehi, "Applications of Multiresolution Based FDTD Multigrid", Proc. MTT-S 1997, pp. 333-336.

[5] E.Tentzeris, M.Krumpholz and L.P.B. Katehi, "Application of MRTD to Printed Transmission Lines", Proc. MTT-S 1996, pp. 573-576.

[6] E.Tentzeris, R.Robertson, M.Krumpholz and L.P.B. Katehi, "Application of the PML Absorber to the MRTD Technique", Proc. AP-S 1996, pp. 634-637.

[7] R. Robertson, E. Tentzeris, M. Krumpholz, L.P.B. Katehi, "MRTD Analysis to Dielectric Cavity Structures", Proc. MTT-S 1996, pp. 1861-1864.

[8] J.-P. Berenger, "A Perfectly Matched Layer for the Absorption of Electromagnetic Waves", J. Computational Physics, vol. 114, pp. 185-200, 1994.

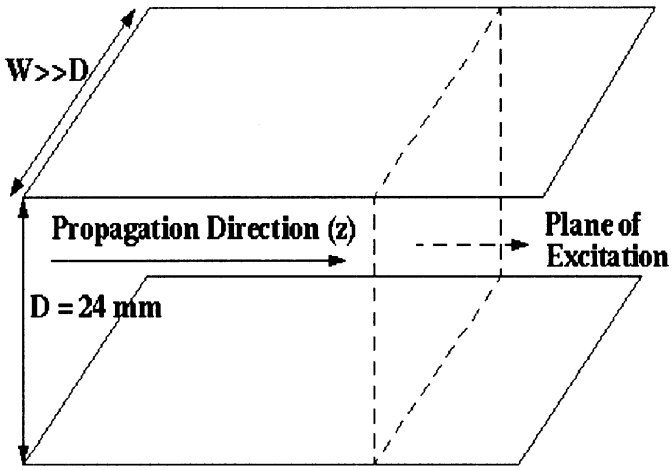


Figure 1: Parallel Plate Waveguide

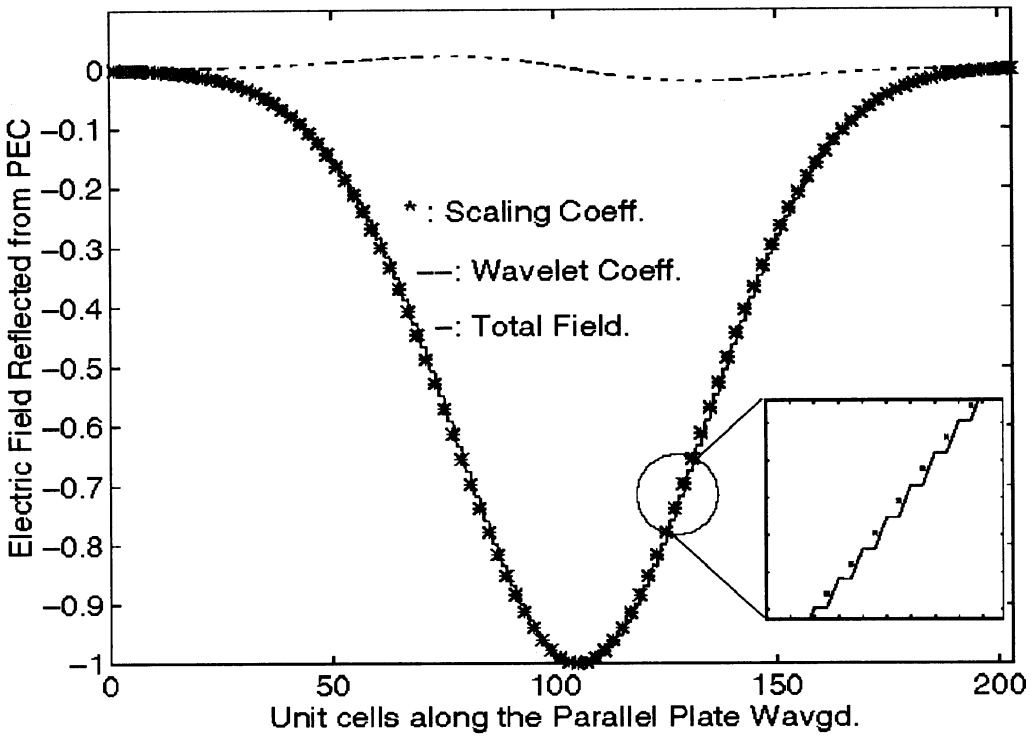


Figure 2: E field WITHOUT wavelet excitation condition in a Plate Waveguide.

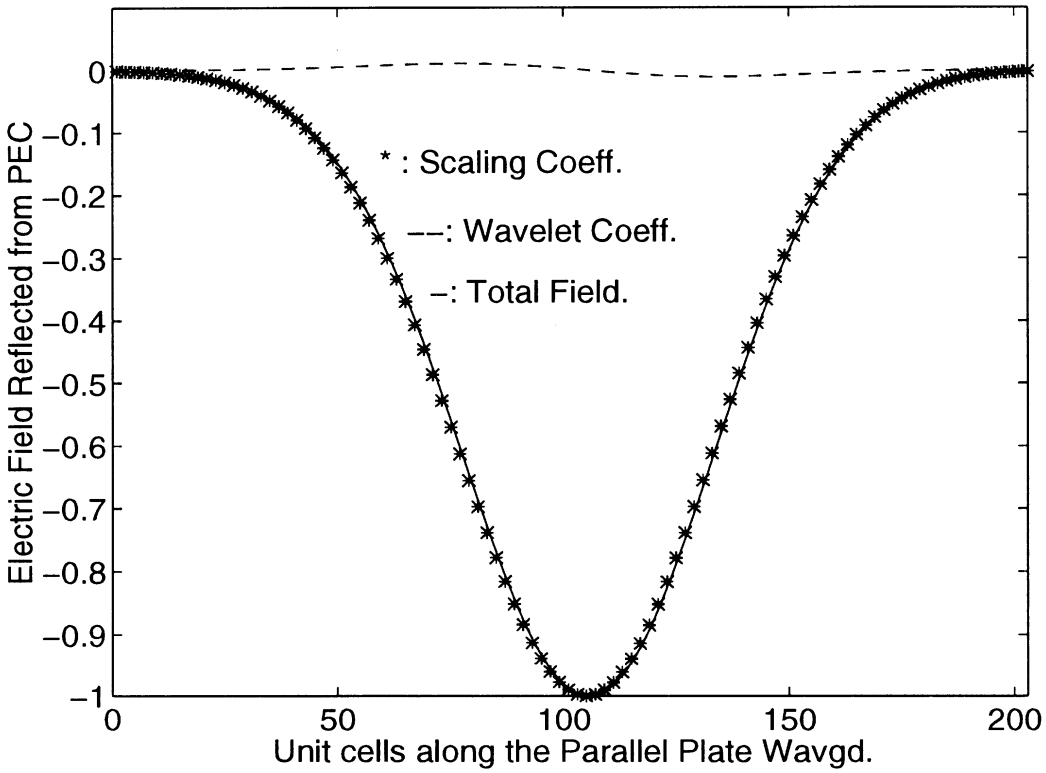


Figure 3: E field WITH wavelet excitation condition in a Plate Waveguide.

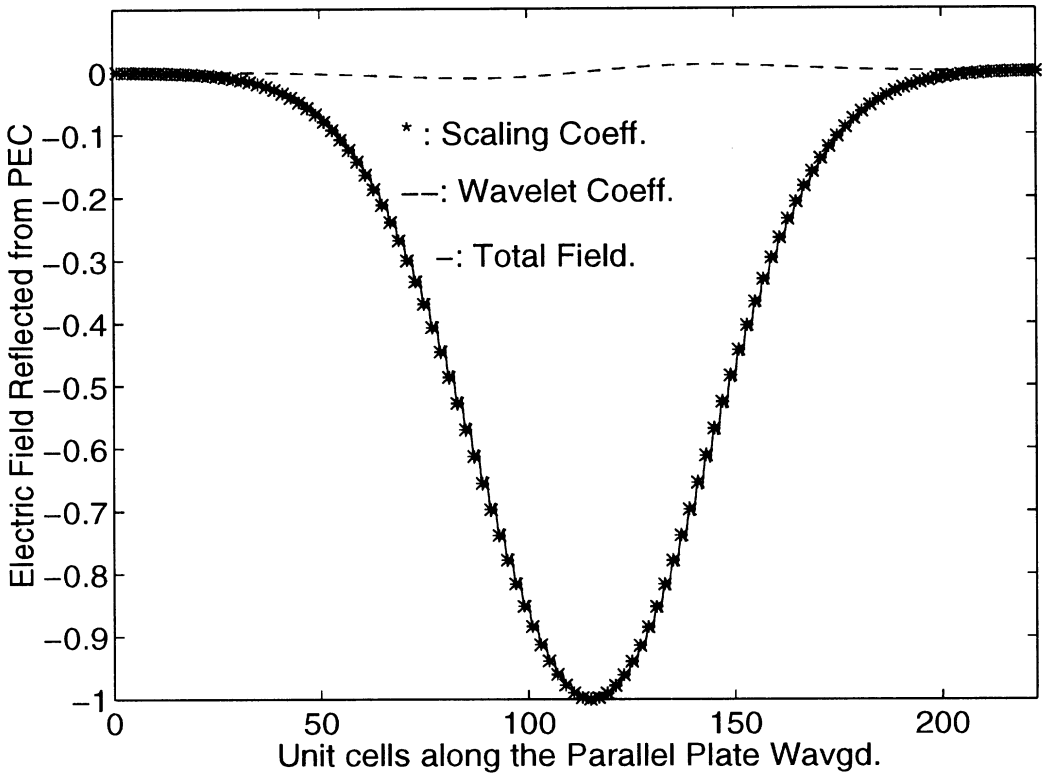


Figure 4: E field WITHOUT continuity condition at PEC in a Parallel Plate Waveguide shorted at one end.

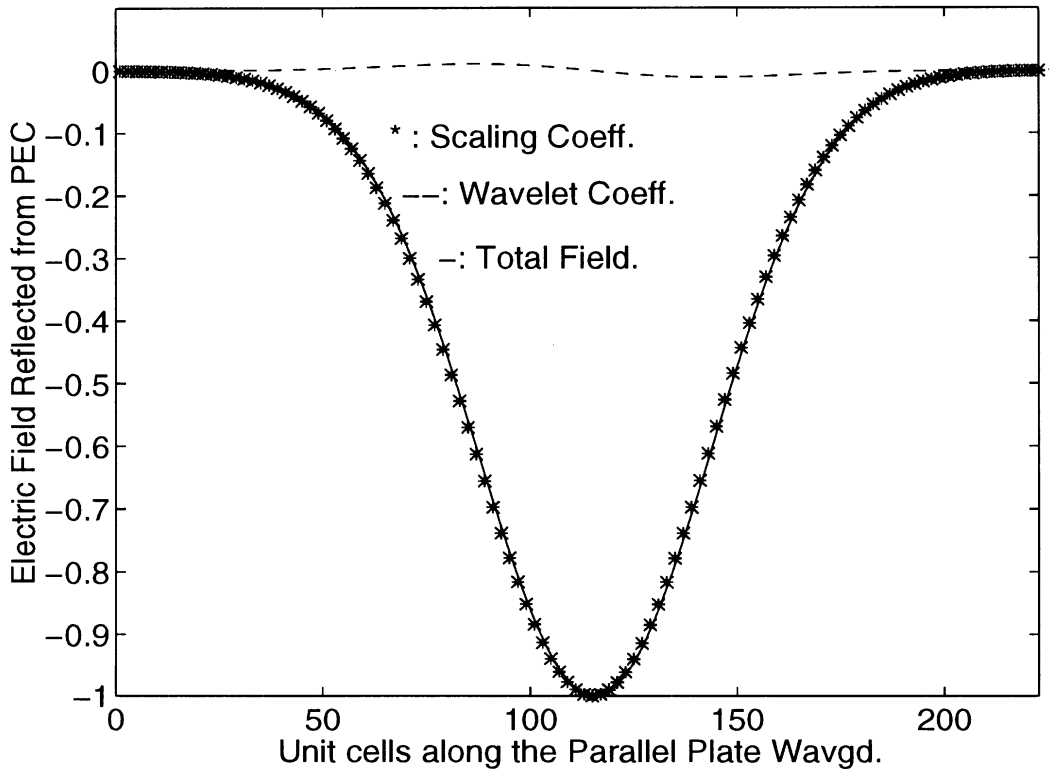


Figure 5: E field WITH continuity condition at PEC in a Parallel Plate Waveguide shorted at one end.

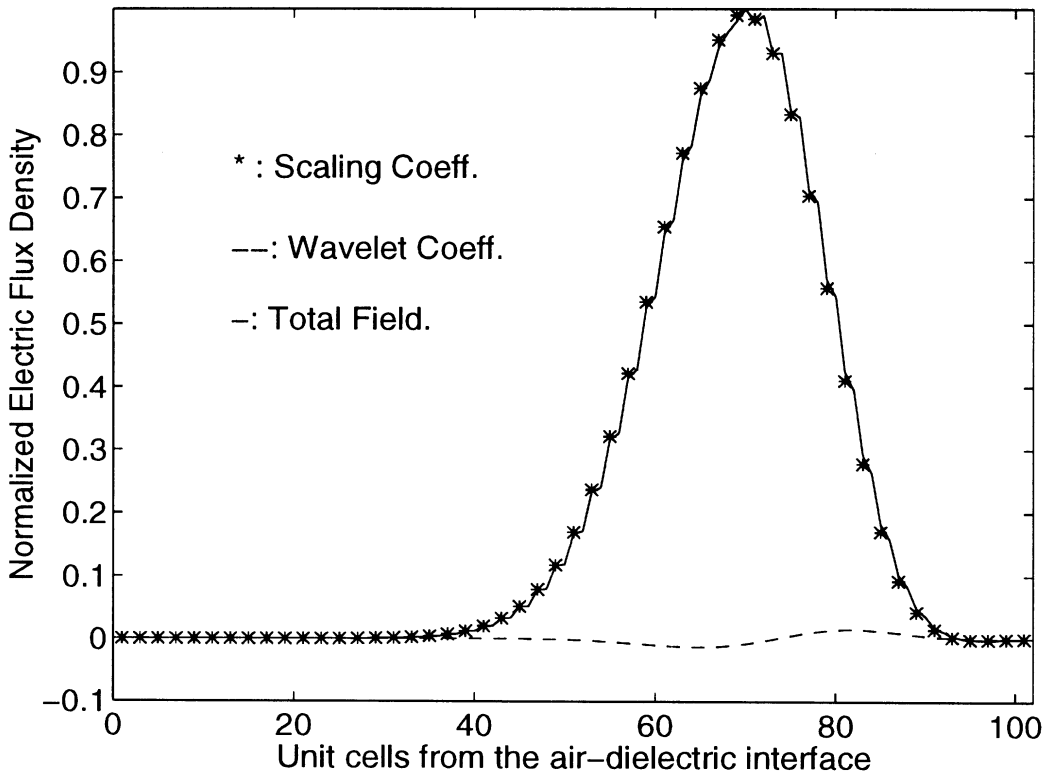


Figure 6: Flux density (D) WITHOUT wavelet continuity conditions in a Parallel Plate Waveguide half filled with dielectric of $\epsilon_r = 10$.

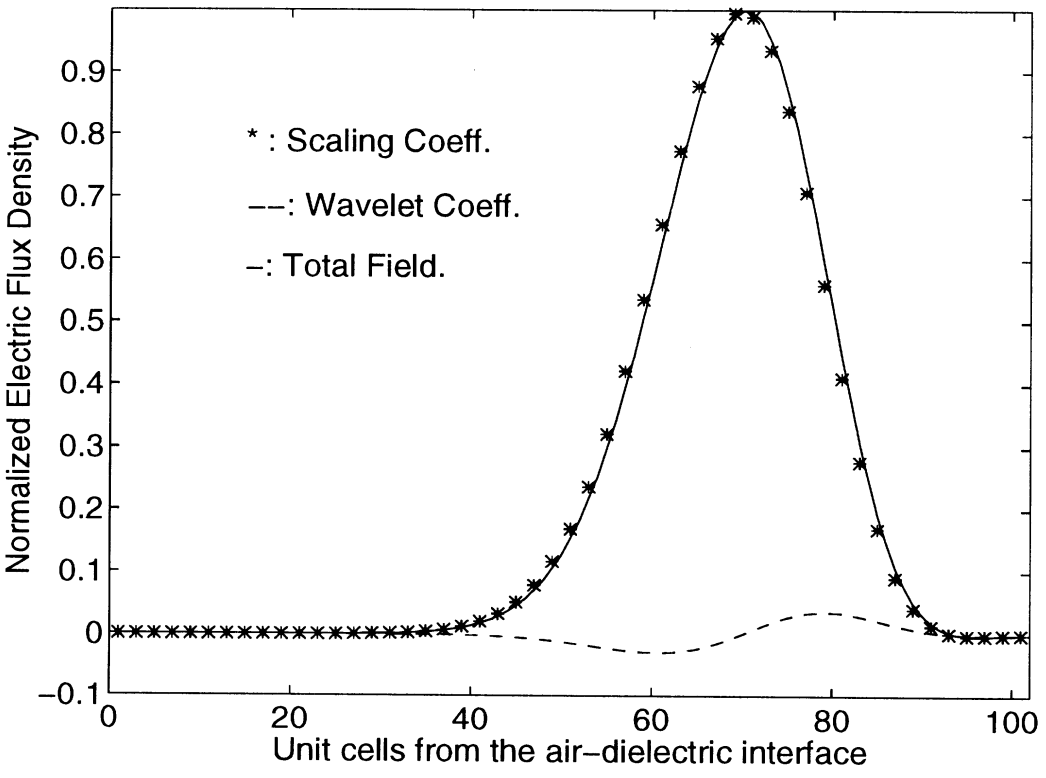


Figure 7: Flux density (D) WITH wavelet continuity conditions in a Parallel Plate Waveguide half filled with dielectric of $\epsilon_r = 10$.

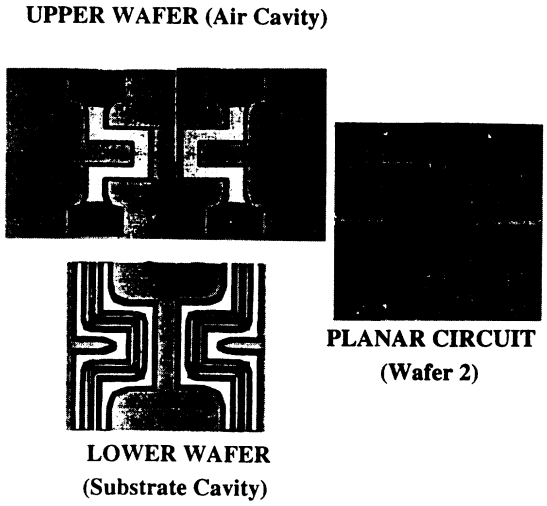


Figure 2. Back-to-back right angle bends.

Figure 3 shows the cross coupling between the two bends. By shielding the two lines the surface waves which couple them have been successfully eliminated and the cross coupling is reduced.

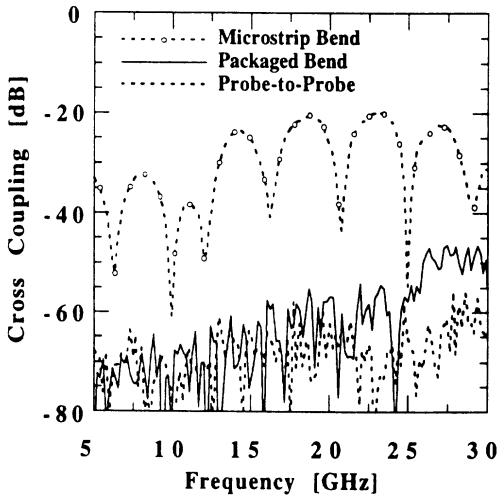


Figure 3. Measured cross coupling between open and packaged bends.

By providing upper and/or lower shielding cavities, it has been shown that these self-packaged structures enhance power transmission in feedlines for microstrip patch antennas. Figure 4 shows the return loss of a packaged and open microstrip fed patch antenna. One can see the improvement in bandwidth which is attributed to the packaged feedline maintaining the input impedance over the frequency range as compared to the open structure.

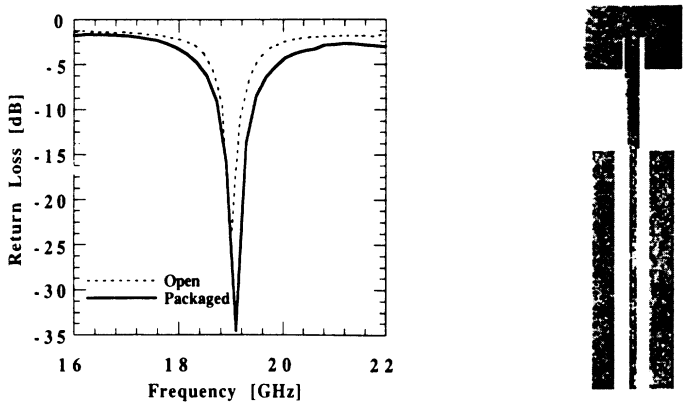


Figure 4. Return Loss for open and packaged microstrip fed patch antennas.

NUMERICAL MODELING OF MMIC PACKAGES

In the design process of electronic devices there exists a circuit design and analysis phase. It would be ideal if an engineer were able to use commercially available software which not only simulated the performance of his circuit but also considered the effects of the components which will be used to complete the packaging. A simulator of this kind would greatly reduce the cost associated with preliminary design and prototype iterations. Currently available software is not capable of giving the engineer information necessary in high frequency design.

An effort is underway where the FEM is being used to model a high frequency MMIC package for a phase shifter[3]. Using this code, the effects of package features (via holes, bonding wires, CD bias lines, symmetry and location of IC) are taken into account and able to provide much needed information with respect to these issues. The K/Ka-band hermetic package being modeled in Figure 5 has been fabricated by Hughes Aircraft Company for NASA Lewis Research Center.

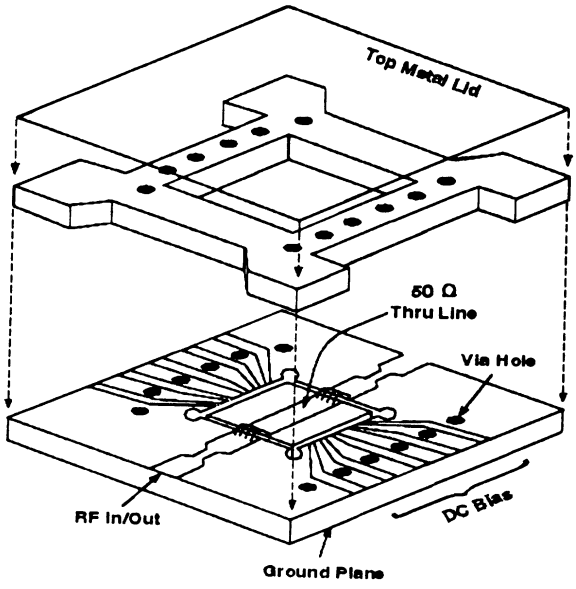


Figure 5. K/Ka-band hermetic package.

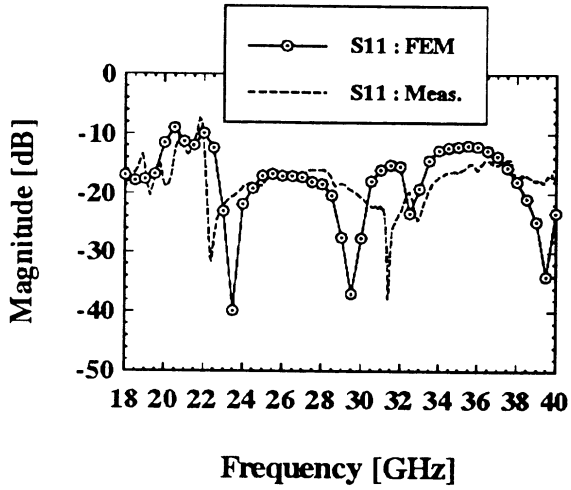


Figure 6. Return Loss for hermetic package.

Using HTCC processing techniques the (7.112 x 7.112 x 1.27) mm package is fabricated from alumina (95% pure, $\varepsilon_r = 9.5$). The experimental data compares well with the numerical results as seen in Figures 6 and 7 where a through line was used to characterize the package. This code also predicts how the package peripherals affected the response of the package[3].

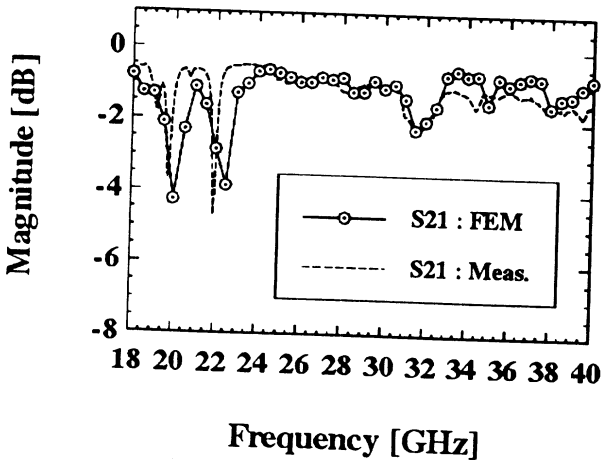


Figure 7. Insertion Loss for hermetic package.

SILICON BASED MMIC PACKAGE

Current research efforts are being conducted in the area of developing single chip carriers such as the one being modeled using the FEM code. We propose to use thin film technology to develop silicon based packages. There are many advantages to using an established silicon technology to develop high frequency high density electronic packages compared to other materials and assembly techniques. The smallest linewidth and via diameter realization is achievable and high frequency requirements can be easily met when employing this technique[4]. When compared to laminate and ceramic processing technologies thin film packaging offers increased circuit density and the capability to accommodate multilayer tile arrangements which are important in space applications where low volume, high performance, high frequency packaged structures are required[4]. Research shows that space communications can benefit from this packaging scheme to achieve reduced volume and weight[5]. Figure 8 shows the top views of the HTCC alumina and the thin film silicon phase shifter packages.

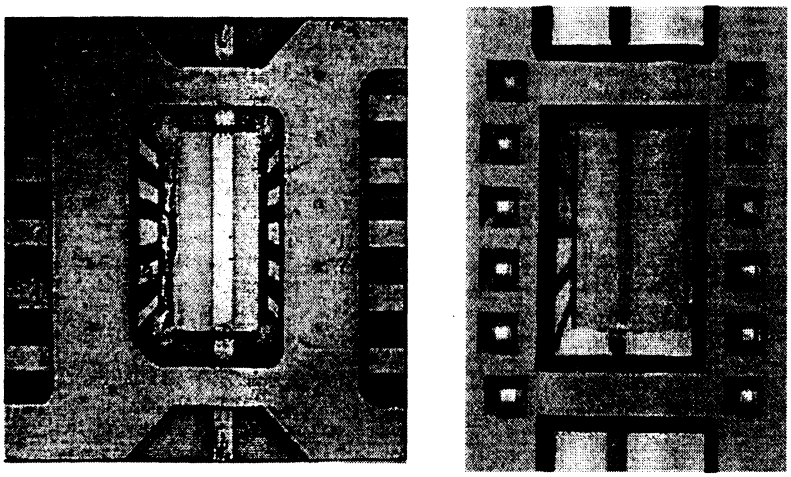


Figure 8. Photograph of HTCC and Thin film hermetic packages.

The processing techniques used to fabricate this silicon structure were standard IC steps such as metallization by evaporation and plating, photolithography and wet chemical etching to generate the 3-D structure. Four wafers comprise the package itself. They consist of metallized silicon as a holder for the package, two processed wafers which realize the transmission lines (open microstrip, stripline, and shielded microstrip) and one final wafer for the top cover to offer hermetic shielding. Figure 9 shows a plan view of the layers used in developing the package in addition to the through line being used for electrical characterization.

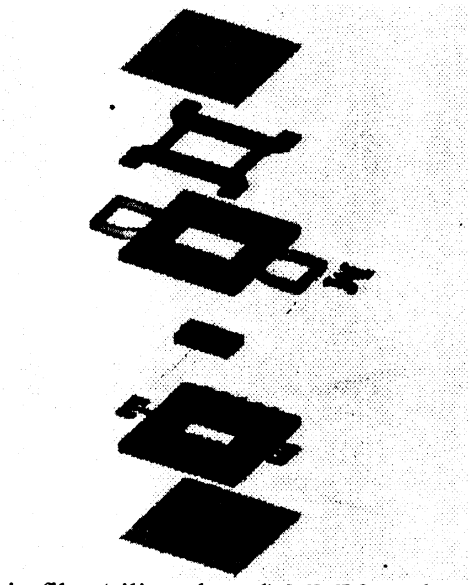


Figure 9. Thin film (silicon based) MMIC package layout.

FUTURE WORK/CONCLUSIONS

Research is underway at The University of Michigan in an effort to create the building blocks required for the development and design of high frequency circuits and packages which offer excellent electrical performance while achieving the cost and weight requirements proposed by industry. The theoretical characterization aids in reducing research dollars by providing the design engineer an alternative to expensive iterations on prototype designs. Figure 10 shows an example of the proposed future on-wafer packaging structures which has a hundred-fold reduction in cost.

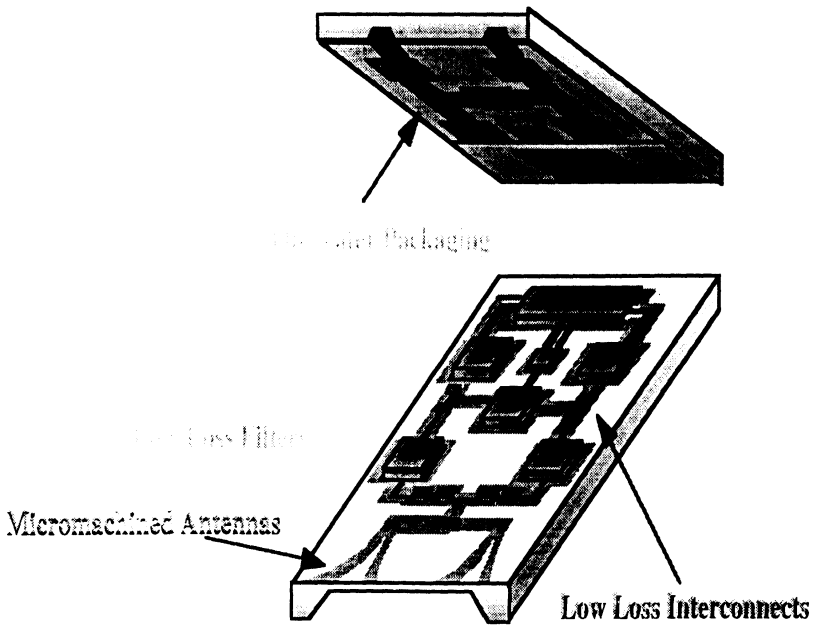


Figure 10. Future on-wafer packaging.

ACKNOWLEDGMENTS

This work has been supported by contracts from the Army Research Office and the Office of Naval Research.

REFERENCES

1. K. E.Petersen, "Silicon as a Mechanical Material," *Proceedings of the IEEE*, Vol. 70, No. 5 May 1982.
2. R. F. Drayton, et al., "Advanced Monolithic Packaging Concepts for High Performance Circuits and Antennas," in *1996 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1615-1618.
3. J. G. Yook, L. P. B. Katehi, et. al., "Experimental and Theoretical Study of Parasitic Leakage/Resonance in a K/Ka-Band MMIC Package" Submitted to *IEEE 1996 MTT-S Special Issue.*
4. J. E. Sergent and C. A. Harper, *Hybrid Microelectronics Handbook*, 2d ed.,Mc-Graw-Hill, Inc., New York, 1995.
5. M. I. Herman, K. A. Lee, et. al., "Novel Techniques for Millimeter-Wave Packages," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 43, No. 7 July 1995.

SURFACE WAVE MODE REDUCTION FOR RECTANGULAR MICROSTRIP ANTENNAS ON HIGH-INDEX MATERIALS

John Papapolymerou,[1] Rhonda F. Drayton,[2] and Linda P.B. Katehi[1]

[1]The Radiation Laboratory
EECS Department
The University of Michigan
Ann Arbor, MI 48109
[2]The University of Illinois at Chicago
EECS Department
Chicago, IL 60607

INTRODUCTION

Microstrip and slot antennas are used in a broad range of applications from communication systems (radars, telemetry and navigation) to biomedical systems, primarily due to their planar characteristics and low manufacturing cost[1]. With the recent development of microwave and millimeter-wave integrated circuits and the trend to incorporate all microwave devices on a single chip for low-cost and high density, there is a need to fabricate patch antennas on high-index materials such as Silicon, GaAs or InP. Because of their high index, these materials exhibit a pronounced surface wave excitation, thus leading to lower antenna efficiency, reduced bandwidth, degradation of the radiation pattern and undesired coupling between the various elements in an array design. Only a few approaches have been put forth to resolve the excitation of substrate modes in microstrip antennas, including using a substrate-superstrate configuration[2], adjusting the radius of a circular patch to a critical value[3], suspending the patch over an air cavity through the use of a membrane[4] or over closely spaced periodic holes in the substrate[5].

We have developed two different techniques in order to address the previously mentioned problems, based on the implementation of micromachining technology. In the first technique, material is removed laterally in a region under and around the patch antenna in an effort to locally reduce the dielectric constant. Experimental results have shown a significant increase in antenna efficiency, when compared with a regular rectangular patch. In the second technique, the resonant length of the patch is adjusted in order to minimize the dominant TM_0 surface mode. Because the dimensions required to suppress the surface wave are larger than the dimensions for the desired frequency of operation, dielectric material is removed in an area only under the patch. Simulation results (FDTD), have shown a significant

Directions for the Next Generation of MMIC Devices and Systems
Edited by N. K. Das and H. L. Bertoni, Plenum Press, New York, 1997

decrease in the excited surface waves between the micromachined antenna and the regular one.

REDUCTION OF THE EFFECTIVE DIELECTRIC CONSTANT (TECHNIQUE I)

Calculation of Reduced Dielectric Constant

In this approach, material is removed underneath the antenna by using selective etching techniques and the excitation of surface waves is suppressed by creating a micromachined cavity as shown in Figure 1.

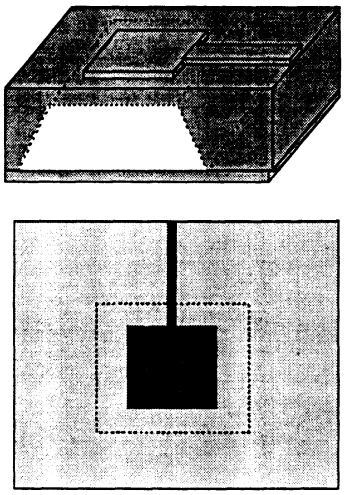


Figure 1. Geometry of the micromachined antenna with mixed air-substrate region that has been laterally etched away.

In order to predict the effective dielectric constant of the mixed air-dielectric (in our case Silicon or Duroid with ε_r=10.8) region for varying thickness ratios underneath the patch antenna, a quasi-static model based on series capacitors is used. A plot of the theoretical and measured effective dielectric constant versus the air gap thickness can be found in Figure 2, where an effective dielectric constant of approximately 2.2 is achieved for a mixed air-silicon ratio of 3:1 from the capacitor model that includes the open-end effect extension length ΔL.

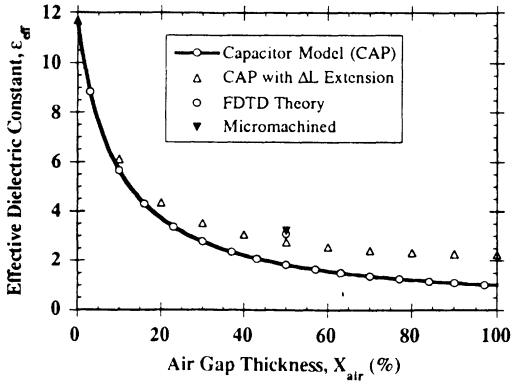


Figure 2 . Effective dielectric constant versus air-gap thickness (percent) for the silicon micromachined patch based on the capacitor model.

Return Loss, Pattern and Efficiency Measurements of Model Antennas

A micromachined patch antenna with an air-dielectric ratio of 3:1 was fabricated on a 635 μm thick Duroid substrate with ε_r=10.8, for checking the validity of our theoretical approach. The selection of this substrate is due to the fact that its dielectric constant is the closest possible to the one of Silicon (11.7). The dimensions of the antenna were 7.624x6.676 mm and those of the cavity 15.19x14.478 mm. The distance between the radiating edges of the patch and the edges of the machined cavity was 3.783 mm. Due to the specifications of the efficiency measurement system set-up the resonant frequency of the patch was between 12.5 and 13.5 GHz (f_{res}=13.165 GHz).

In order to compare the performance of the micromachined antenna with that of a regular antenna a conventional patch with dimensions of 3.75 x4.42 mm was fabricated on the same substrate (f_{res}=12.84 GHz). In addition, a regular antenna with dimensions of 7.57x7.34 mm was fabricated on a Duroid substrate with a thickness of 500 μm and ε_r=2.2. All three antennas were fed by a 50 Ω microstrip line for the best possible match and from the return loss that can be seen in Figure 3, we observe an increase in the -10 dB bandwidth of the machined antenna from 1.40% to 2.3% when compared with the bandwidth of the regular antenna on high index. In reality, the 2.3% bandwidth of the etched antenna is the same as the bandwidth of the low-index (2.2) regular antenna. Since bandwidth is inversely proportional to the quality factor, Q, defined as the ratio of total stored energy in the antenna to the energy dissipated or radiated from the antenna, the increase in bandwidth provides the first indicator of a potential increase in radiation efficiency.

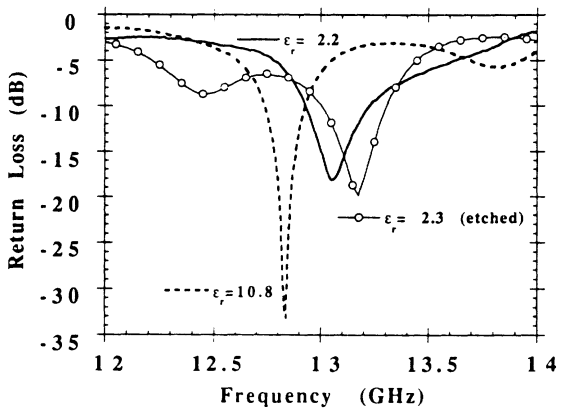


Figure 3. Return loss for the micromachined high-index patch, the regular high-index patch and the regular low-index one.

Radiation patterns were also taken for all three antennas and they can be seen in Figure 4, where we observe that the regular high index E-plane pattern has a large peak at about -50 degrees, indicating large power leakage in the form of surface waves. In contrast, the micromachined patch has a much smoother E-plane and is very similar to the one of the low index antenna. As expected, the H-plane patterns are similar in all cases.

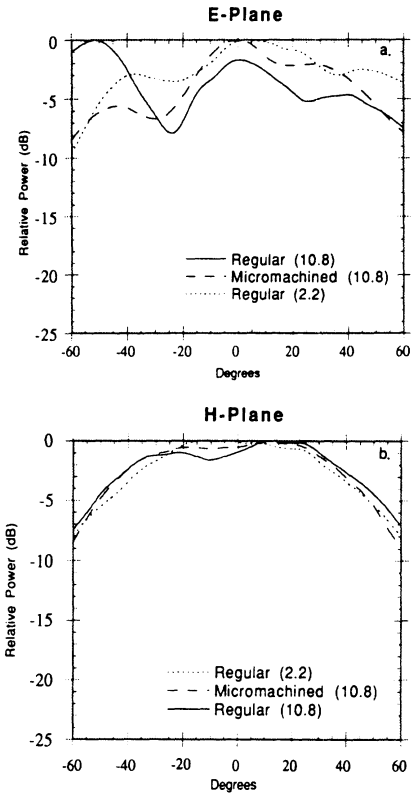


Figure 4. Radiation patterns for the regular high-index antenna, the micromachined antenna and the low-index antenna: a) E-plane and b) H-plane.

In order to obtain conclusive evidence about the increase in radiation efficiency of the micromachined antenna, efficiency measurements were performed for all three patches based on a radiometric method[6,7] and a hemispherical hot/cold load (black-body absorber Ecosorb). The three antennas were placed on a test fixture with an RF connector at the input of the feeding line. The efficiency measurement was referenced at the RF connector and ,thus, included besides the loss due to surface waves the feed-line loss (dielectric and conductor), the connector loss and the mismatch to the 50 Ω line loss. The results can be seen in Figure 5, where we observe that the efficiency of the micromachined patch at the resonant frequency is 73±3 % whereas the efficiency of the regular high-index patch is 56±3 %. The low-index regular antenna has an efficiency of 76±3 %.

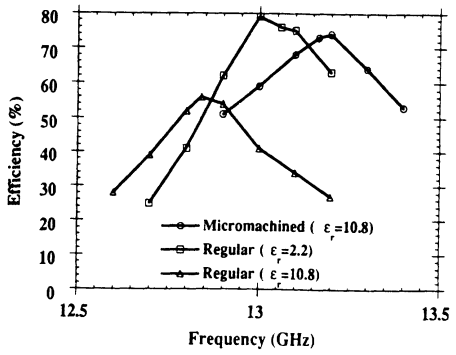


Figure 5. Measured efficiency for the micromachined and regular antennas.

From the above results, it is obvious that the micromachined antenna performs like a regular low-index antenna and gives a 30% increase in the measured efficiency when compared with the conventional high-index patch. We should also note here that since the measured efficiencies include losses irrelevant to the antenna (connector, feed-line and mismatch) a de-embedding process needs to be performed in order to get the efficiency of the antenna itself. This can be achieved by modelling the feed-line with a commercial software and calculating its losses, as well as by measuring the mismatch/return loss and using an empirical value for the RF connector loss. After de-embedding, the calculated efficiencies are 66% for the high-index regular patch, 85% for the micromachined high-index patch and 82% for the low-index regular patch. These results indicate that the micromachined antenna is successful in suppressing the losses due to surface waves.

ELIMINATION OF TMo SURFACE WAVE (TECHNIQUE II)

Thoretical Analysis

In this approach the resonant length of the rectangular patch is adjusted in order to minimize the dominant TM_0 surface mode. According to the equivalence principle and the cavity model, in terms of radiation a rectangular patch can be modeled as a rectangular loop of magnetic current. From the cavity model, the electric field of the dominant TM_{10} mode for the geometry shown in Figure 6 is given by:

$$E_z = A\cos\left(\pi\frac{y}{b}\right) \tag{1}$$

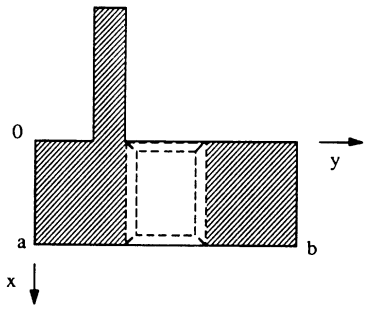


Figure 6. Micromachined antenna for the elimination of TMo mode.

where a,b are the width and the resonant length of the patch, respectively. The radiating edges are considered to be at y=0,b since only the dominant mode of the cavity is excited. The equivalent magnetic current at these two edges is:

$$\vec{M} = 2\vec{E}x\hat{n} = 2A\hat{x} \tag{2}$$

As it is known, a single Hertzian magnetic dipole, oriented in the x direction at a height z' above the ground will give rise to a TM_0 surface wave field given by:

$$\Psi = K(z, z')H_1^{(2)}(\beta_{TMo}\rho)\sin\phi \tag{3}$$

where β_{TMo} is the propagation constant of the TM_0 mode and K(z,z') is an amplitude factor that depends on the height of the source and the observation point. By integrating over the two radiating edges of the rectangular patch for the magnetic current distribution, the total surface wave field radiated by the magnetic currents takes the form:

$$\Psi = -4A\frac{B(z)}{\beta_{TMo}}H_1^{(2)}(\beta_{TMo}\rho)\tan\phi\cos\left(\beta_{TMo}\frac{b}{2}\sin\phi\right)\sin\left(\beta_{TMo}\frac{a}{2}\cos\phi\right) \tag{4}$$

where $B(z) = \int_0^h K(z, z')dz'$.

In order to derive the above expression the far field approximation for the phase of the radiated wave was used. The pattern of equation (4) is shown in Figure 7 (dashed line). By setting $b=\pi/\beta_{TMo}$ nulls are placed at the location of the peaks of the lobes at $\phi=\pi/2,3\pi/2$ so that four minor lobes replace the two major lobes (Figure 7, solid line). As a result, the surface wave pattern is reduced.

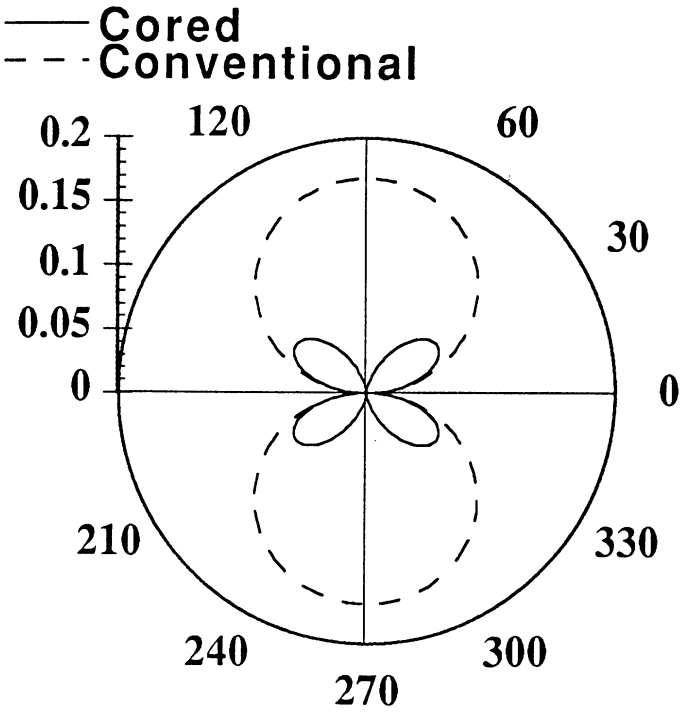


Figure 7. Surface wave field pattern for the regular antenna and the micromachined antenna.

Choosing b according to the above formula, results in a greater resonant length than the one chosen for the design frequency. In order to overcome this decrease in operating frequency, the material in a rectangular region under the patch is removed, thus creating a lower effective dielectric constant which will permit the desired increase in operating frequency. The length of this "cored" region is found from the transcedental equation, which is derived from the field expressions of the dominant mode cavity, after applying the boundary conditions at the various interfaces.

Results

In order to test the accuracy of the previous analysis a rectangular patch with a resonant frequency of 22.5 GHz was designed on a Duroid substrate with ε_r=10.8 and a thickness of 635 μm. Since for the given substrate , higher order surface modes exist above 40 GHz elimination only of the dominant TM_0 mode is sufficient. The micromachined patch was compared with a regular patch on the same substrate and with the same resonant frequency through FDTD simulations. The results can be seen in Figure 8, where measurement of the electric field inside the dielectric region shows a suppressed field for the micromachined antenna by at least 10 dB, when compared with that of the conventional patch.

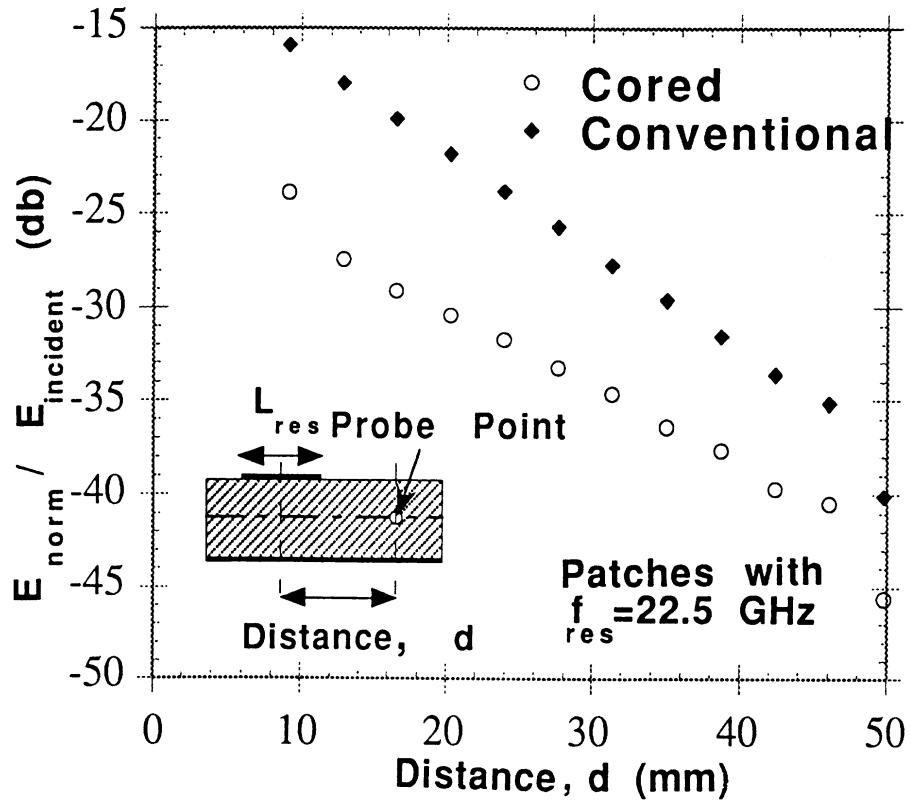


Figure 8. Normalized electric field inside the dielectric versus distance from the center of the antenna for the micromachined patch and the regular patch.

CONCLUSIONS

Two different approaches for the reduction of surface waves in rectangular microstrip antennas were presented in this paper. In the first technique, material was removed laterally underneath and around the patch and an increase of 64% and 30% was observed in the bandwidth and radiation efficiency, respectively. In the second technique, the resonant length of the rectangular patch was adjusted to a critical value in order to suppress the dominant TM_0 surface mode. Simulation results with FDTD showed a substantial decrease in the electric

field measured inside the dielectric. Since both approaches require the use of micromachining techniques and result in the enhancement of antenna performance, integration of these high-efficiency rectangular patches on MMIC's operating at high frequencies will be feasible, successful and easy.

ACKNOWLEDGMENTS

The authors would like to thank the Office of Naval research for the financial support of this project under contract No. N00014-92-J-1070.

REFERENCES

1. D.M. Pozar, "Microstrip antennas," *IEEE Proceedings*, Vol. 80 79:91 (1992).
2. N.G. Alexopoulos and D.R. Jackson, "Fundamental superstrate (cover) effects on printed circuit antennas," *IEEE Trans. on Antenna and Propagation*, Vol. AP-32, No. 8 807:816 (1984).
3. D. R. Jackson, J. T. Williams, et. al, "Microstrip patch designs that do not excite surface waves," *IEEE Trans. on Antennas and Propagation*, Vol. 41, No. 8 1026:1037 (1993).
4. M. J. Vaugh, K. Hur, and R. C. Compton, "Improvement of microstrip patch antenna radiation patterns," *IEEE Trans. on Antennas and Propagation*, Vol. 42, No. 6 882:885 (1994).
5. G.P. Gauthier, A. Courtay and G.M. Rebeiz, "Microstrip antennas on synthesized low dielectric-constant substrates," Submitted to *IEEE Trans. on Antennas and Propagation, (*1996).
6. J. Ashkenazy, E. Levine and D. Treves, "Radiometric measurement of antenna efficiency," *Electron. Lett.*, Vol. 21, No. 3 (1985).
7. D.M. Pozar and B. Kaufman, "Comparison of three methods for the measurement of printed antenna efficiency," *IEEE Trans. on Antennas and Propagation*, Vol. 36, No.1 136:139 (1988).