Annual Report

on

Micromachined High-Q RF Filters and Resonators for Communications Systems

By

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The University of Michigan

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Manuscripts Published or Submitted During the Reporting Period.

1. J. Papapolymerou, J.C. Cheng, J. East and L.P.B. Katehi, "A Micromachined High-Q X-Band Resonator", IEEE Microwave and Guided Wave Letters," Vol. 7. pp. 168-170, June 1997.
2. L. Harle, J. Papolymerou and L.P.B. Katehi, "The Effects of the Position of the Slot on the Performance of High-Q Micromachined Filter," submitted for presentation to the 1998 European Microwave Conference.
3. R.M Henderson and L.P.B. Katehi, "Silicon-Based Micromachined Packages for High-Frequency Applications," IEEE Transactions on Microwave Theory and Techniques, submitted January 1998.
4. Drayton, R.M. Henderson, and L.P.B. Katehi, "Monolithic Packaging Concepts for High Isolation in Circuits and Antennas, " IEEE Transactions on Microwave Theory and Techniques, in press.
5. Drayton, R.M. Henderson, and L.P.B. Katehi "High Frequency Circuit Components on Micromachined Variable Thickness Substrates, " IEE Electronics Letters, Vol. 33, No. 4, February 1997.

6. Weller, M. Imparto, M. Dunleavy, R.M. Henderson, S.V. Robertson and L.P.B. Katehi, "The Effects of Line Width and Slot Etching on Silicon-Based CPW at Mm-Wave Frequencies," presented at the 50th ARFTG Conference, Dec. 1997
7. Henderson and L.P.B. Katehi, ìSilicon-Based Micromachined Packages for Discrete Components,î Proceedings of the 1997 International Symposium Microwave Theory and Techniques, June 1997, Denver Co, pp. 521-524.
8. Weller, R.M. Henderson, S.V. Robertson and L.P.B. Katehi, " Optimization of Mm-Wave Distribution Networks Using Silicon-Based CPW," 1998 IEEE MTT-S International Microwave Symposium, to be presented in June 1998, Baltimore, Maryland.

Honors and Awards

- 1997 Best Paper Award by the International Microelectronics and Packaging Society (IMAPS)
- First Prize in Symposium Paper Award Contest with Katherine Herrick for the paper "W-Band Micromachined Finite Ground Coplanar (FGC) Line Circuit Elements," IEEE MTT-S, Denver, CO, June 1997

Brief Description of Performed Research

This project concentrates on the development of high-efficiency Si micromachined components. Specifically, it addresses the development of High-Q Filters using Si micromachined cavities. During the reporting period, our group has investigated the development of important issues related to the development of these filters: (1) Losses in Si wafers for a variety of resistivities (Part A) (2) Micromachined high-Q filters (Part B) (3) On-wafer packaging of circuit and filter components for high-efficiency and low loss (Part C). The study performed in each of these areas is described in detail below. Furthermore, at the end of each section copies of the submitted/accepted papers are included for further information

PART A: Losses in Si wafers for a variety of resistivities

Transmission Line Loss In Silicon

By Jim Becker

The successful extension of monolithic microwave integrated circuits (MMICs) in silicon to progressively higher frequencies requires an understanding of the fundamental limitations that this material presents. Of specific interest in MMICs is the loss which silicon introduces to signal propagation through a circuit at these frequencies. While a variety of measurement techniques have been explored to quantify this loss, including radar backscatter and waveguide-loading, we have found transmission line measurements to be the most reliable.

Characteristics of these planar transmission lines have been explored using an HP8510C network analyzer, a probe station, and a calibration/de-embedding routine developed at the National Institute of Standards and Technology. In short, one measures the S-parameters of given transmission line geometry for various line lengths and terminations; from these measurements, values of the effective dielectric constant and attenuation, for example, are computed.

The first transmission line studied was the finite ground coplanar waveguide (FGC). Such planar transmission lines were fabricated on silicon wafers of varying resistivity (from ~10 Ωcm to ~30000 Ωcm) using standard photolithographic processes. Measurements were carried out in the 2-40 GHz and 75-110 GHz ranges. As expected, the observed attenuation decreased with increasing substrate resistivity. It was found that the mean attenuation in the 75-110 GHz range (a range in which the differences in metal thickness between the various samples would be largely irrelevant due to the skin effect) decreased by approximately 0.7 dB/cm in using a wafer of resistivity equal to 30000 Ωcm versus one of 2000 Ωcm. It was found however, that silicon exhibiting a resistivity of 2000 Ωcm or greater allowed for acceptable loss performance.

Transmission lines using the coplanar strip (CPS) geometry were also investigated. It was found that implementation of a 50 Ω geometry using silicon (dielectric constant = 11.7 and 400 μm nominal thickness) required slot spacing on the order of 10 μm or less. Due to these tight dimensions, loss in CPS lines was found to be somewhat higher than in 50 Ω FGC lines. In addition, the quality of the calibration (in terms of the value of the return loss for instance) was not as high for CPS lines.

Alongside semiconductor materials such as silicon and gallium arsenide, certain ceramic-based materials, barium strontium titanate (BST) for example, are of considerable interest in the arena of microwave circuits. Presently we are exploring the possibility of transmission lines on BST wafers.

Jim Becker

Biography

Jim Becker received his bachelor's degree in materials science from the University Of Illinois, Urbana-Champaign in 1992. While an undergraduate, he spent a summer of research at Northwestern University exploring the possibility of nanostructure deposition using the tip of a scanning-tunneling microscope. Jim went on to receive a Master's degree in Electrical Engineering from Colorado State University in Fort Collins, Colorado. There he studied the epitaxial growth and photoelectronic properties of a series of novel materials, the semiconducting transition metal silicides, and demonstrated their potential use for infrared detection. Also while at Colorado State, Jim was the department of Electrical Engineering's nominee for the College of Engineering's annual teaching assistant award for the 95/96 academic year. Presently, he is pursuing a doctorate in the area of microwave circuits at the University Of Michigan in Ann Arbor, Michigan.

INTRODUCTION

Three measurement techniques were employed in an effort to determine the loss, a pertinent measure of which is the loss tangent, in silicon at 94 Ghz. The loss tangent of a material may be expressed as the ratio of the real and imaginary components of its complex permittivity. Thus, by determining a material's dielectric properties, we may estimate loss in the material.

Through the measurement of the backscattered signal from an object, for example, the complex permittivity of the target material may be determined. The first two techniques which were employed relied on the measurement of the backscattered signal from silicon; one was a free-space technique, and the other utilized a rectangular waveguide. The third, and final, technique involved fabricating transmission lines on silicon and measuring the properties of these transmission lines, most importantly, their attenuation.

RADAR TECHNIQUE

Using the backscattered signal from a metallized standard to calibrate a 94 Ghz radar system, the magnitude of the reflection coefficient of silicon was measured using a network analyzer. Measurements were performed on a "slab" of silicon wafers, consisting of between one and ten wafers (nominal thickness ~600 microns), terminated either by free space or by the metallized standard. Using standard expressions for the reflection coefficient in the above cases, an attempt was made to "best-fit" the measured data using the real and imaginary components of the permittivity as fitting parameters. A representative plot of the measured and predicted behavior is given in Figure 1.

The fitting procedure just described did not yield a unique value for the complex permittivity in that more than on value demonstrated reasonable agreement between the predicted behavior (using the standard reflection coefficient equations) and that observed experimentally. In an effort to determine the value of the real part of the permittivity, a waveguide method [1] was explored. (It was reasoned that with a definitive value of the real part of the permittivity in hand, the imaginary part of the permittivity could then be used as the sole fitting parameter in the analysis of the radar measurements.

RECTANGULAR WAVEGUIDE TECHNIQUE

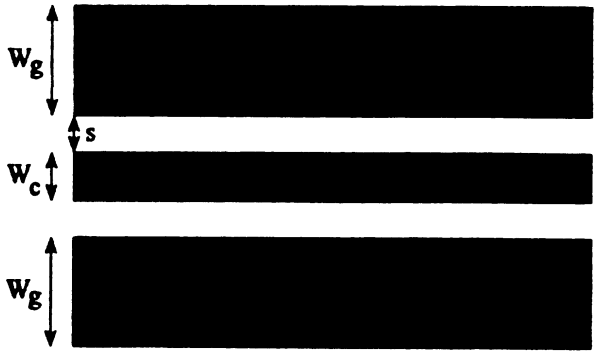
The waveguide technique required that pieces of silicon be cut so as to fit flush in a rectangular waveguide. Since a precise fit was required for reliable results, a WR-90 rectangular waveguide which operates in the 8-12 Ghz (X-band) frequency range was used. Such a waveguide has a cross-section which is 0.9 inches by 0.4 inches, whereas a waveguide operating at 94 Ghz, the WR-10, is but 0.1 inches by 0.05 inches in cross-section. It was felt that a measurement of the real part of the dielectric constant at X-band would be a good estimate of its value at W-band (~94 Ghz).

Shown in Figure 2 is a plot of the dielectric constant (i.e. the real part of the complex permittivity) of silicon using the rectangular waveguide technique. Clearly evident in the figure

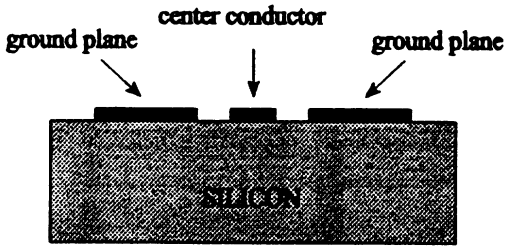
is a roughly 10% variation in the observed dielectric constant. Such a variation is significant and does not permit a definitive value to be used in analyzing the radar data. Due to the difficulty in extracting a precise value of the loss tangent of silicon using these techniques, a third method, one which would give an indication of the relative loss in samples of various resistivities, was investigated.

TRANSMISSION LINE MEASUREMENTS

Simple finite ground coplanar waveguide (FGC) transmission lines were fabricated directly on silicon (see figure below).



TOP VIEW



CROSS-SECTIONAL VIEW

An approximate 50 Ω geometry was realized using a center conductor width, W_c, of 50 microns, a strip spacing, s, of 45 microns, and ground plane widths, W_g, of 130 microns. The conductor consisted of an evaporated gold seed layer (titanium was used as the base of the seed layer to promote adhesion), which was subsequently plated for additional thickness. Measurement of the line parameters was accomplished using a calibration routine

Four wafers of different resistivities were used (see table I). The resistivity of each wafer was determined using a four-point probe technique; the measured resistivity was found to be within, or on the borderline of, the manufacturer's specified range in three of the four cases. I measured the resistivity of each sample several times and cannot explain the discrepancy in the case of sample 4. The last column in the table gives the final conductor thickness.

TABLE I: Sample Parameters

Sample Number	Specified Range (Ωcm)	Measured Resistivity (Ωcm)	Conductor Thickness (μm)
1	≥2000	2250	1.79
2	3535-6565	5686	2.10
3	10000-19000	9522	2.34
4	1000-2700	31000	2.60

Shown in Figure 3 is the attenuation exhibited by the FGC lines on each of the four samples in the 2-40 Ghz range. We see that the high resistivity substrate exhibits the lowest loss across the frequency range and that the loss generally increases with decreasing substrate resistivity (though the 5686 and 9522 Ωcm lines do cross in a number of places). It is important to note that it just so happens that the final conductor thickness increases monotonically with substrate resistivity (a simple coincidence of course). This suggests that the lower loss in the high resistivity substrates could also be due to reduced skin effect losses. At 40 Ghz however, each sample has a conductor thickness of at least 4.5 skin depths which makes comparisons based on substrate resistivity more meaningful. Nevertheless, measurement of the line characteristics were also made a W-band, the results of which are given in Figure 4.

The oscillatory nature of the attenuation curves made at these frequencies is in line with what others in our research group have found and thus are not particular to this set of measurements. At these frequencies, the conductor thickness in each case is many times the skin depth (>7 at 94 Ghz in all cases) and thus the overall trend toward lower loss with increasing substrate resistivity, as depicted in Figure 5, seems reasonable.

SUMMARY

While these series of investigations were unable to quantify the loss tangent of silicon, an overall trend of lower loss at higher substrate resistivities was observed. This behavior suggests that to achieve the lowest loss with silicon, one should opt for the highest substrate resistivity. Of course, there comes a point where obtaining samples of extremely high resistivity could prove to be probatively expensive. It should also be mentioned that members of our research group have been able to obtain low loss with similar substrates to that of item 1 using an oxide between the conductor and the silicon substrate. Thus a substrate of resistivity of greater than say, 2000 Ωcm may be sufficient in most cases.

Finally I would like to mention that an exhaustive literature search turned up only one paper regarding the loss in high-resistivity silicon. In this paper [2], using a resonator technique in a reduced-height waveguide, the authors found a loss tangent in 10000 Ωcm silicon of 1.3×10^{-3} (± 30%) in the 75-110 Ghz range.

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2. Joseph Buechler, Erich Kasper, Peter Russer and Karl M. Strom, Silicon High-Resistivity-Substrate Millimeter-Wave Technology. IEEE Transactions on Microwave Theory and Techniques, Vol 34, No 12 pp.1516-1521 (1986).

FIGURE 1

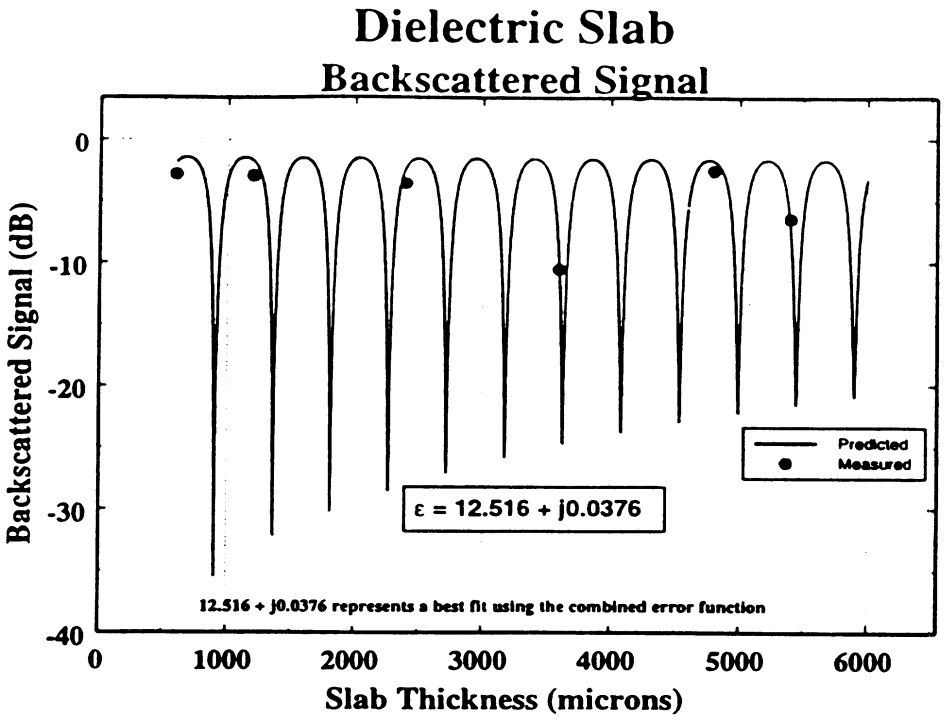


FIGURE 2

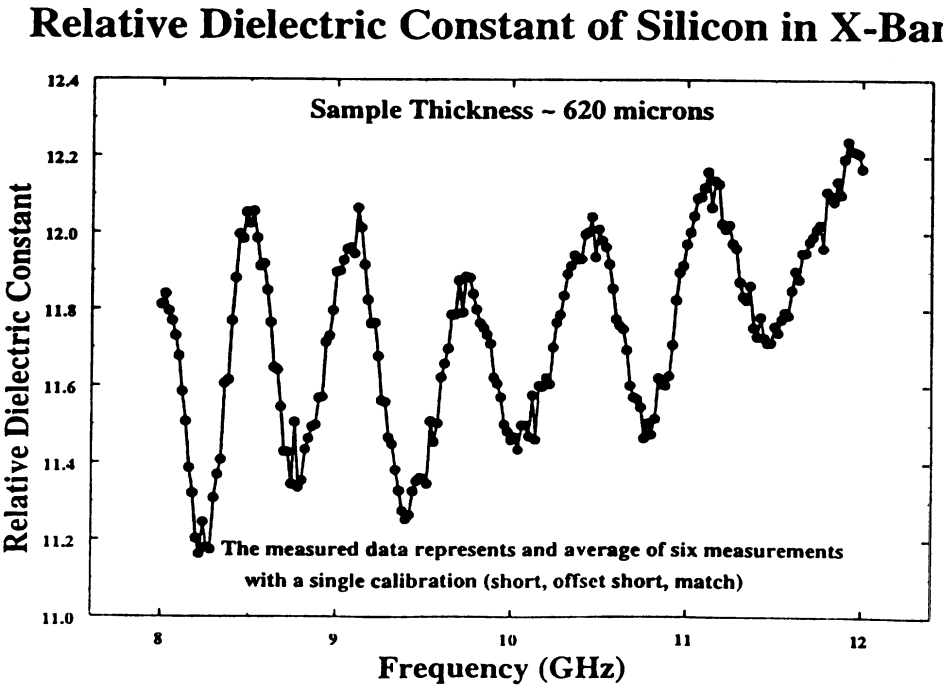


FIGURE 3

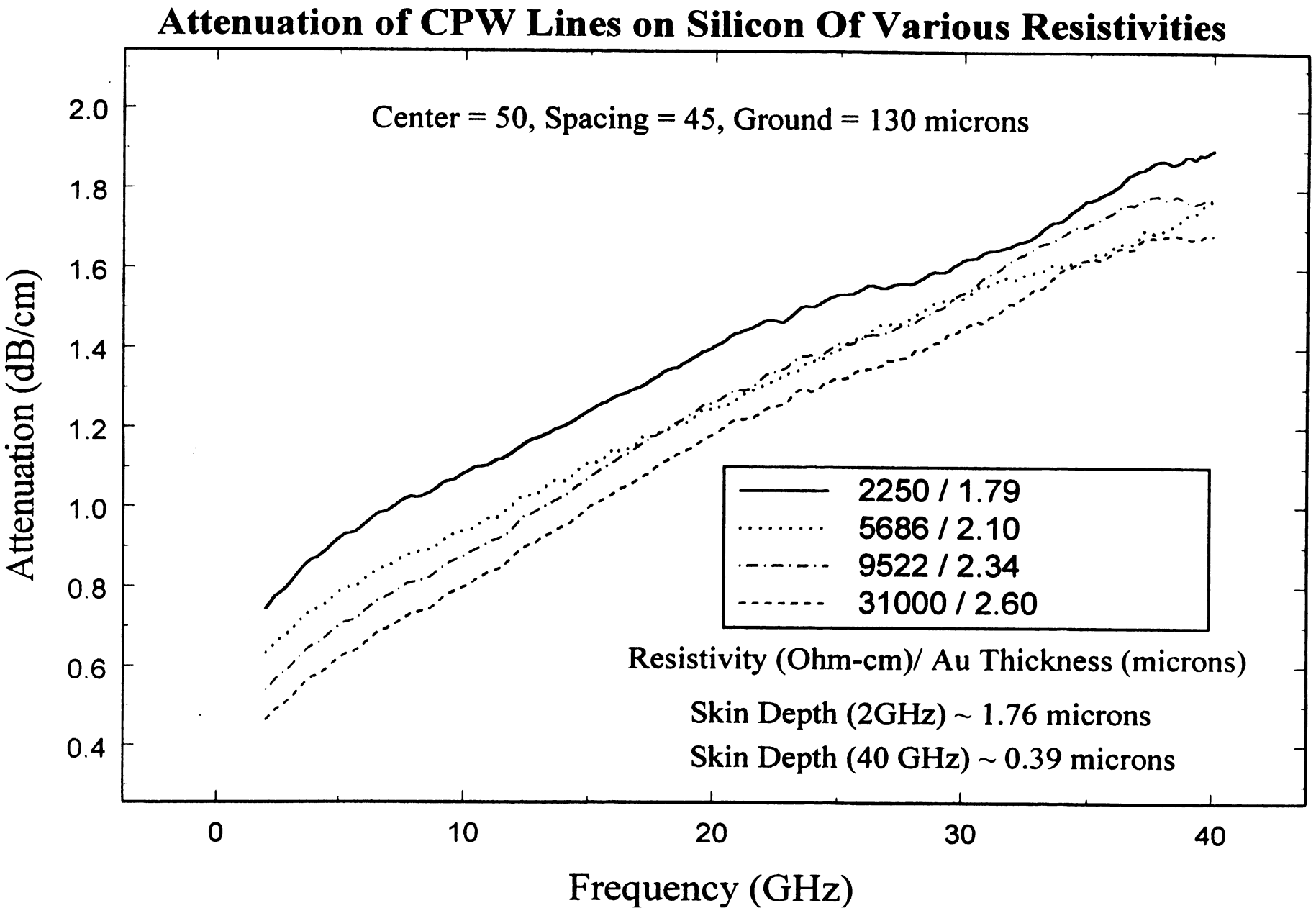

Attenuation of CPW Lines on Silicon Of Various Resistivities
Center = 50, Spacing = 45, Ground = 130 microns
Attenuation (dB/cm)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0
10
20
30
40
Frequency (GHz)
2250 / 1.79
5686 / 2.10
9522 / 2.34
31000 / 2.60
Resistivity (Ohm-cm)/ Au Thickness (microns)
Skin Depth (2GHz) ~ 1.76 microns
Skin Depth (40 GHz) ~ 0.39 microns

FIGURE 4

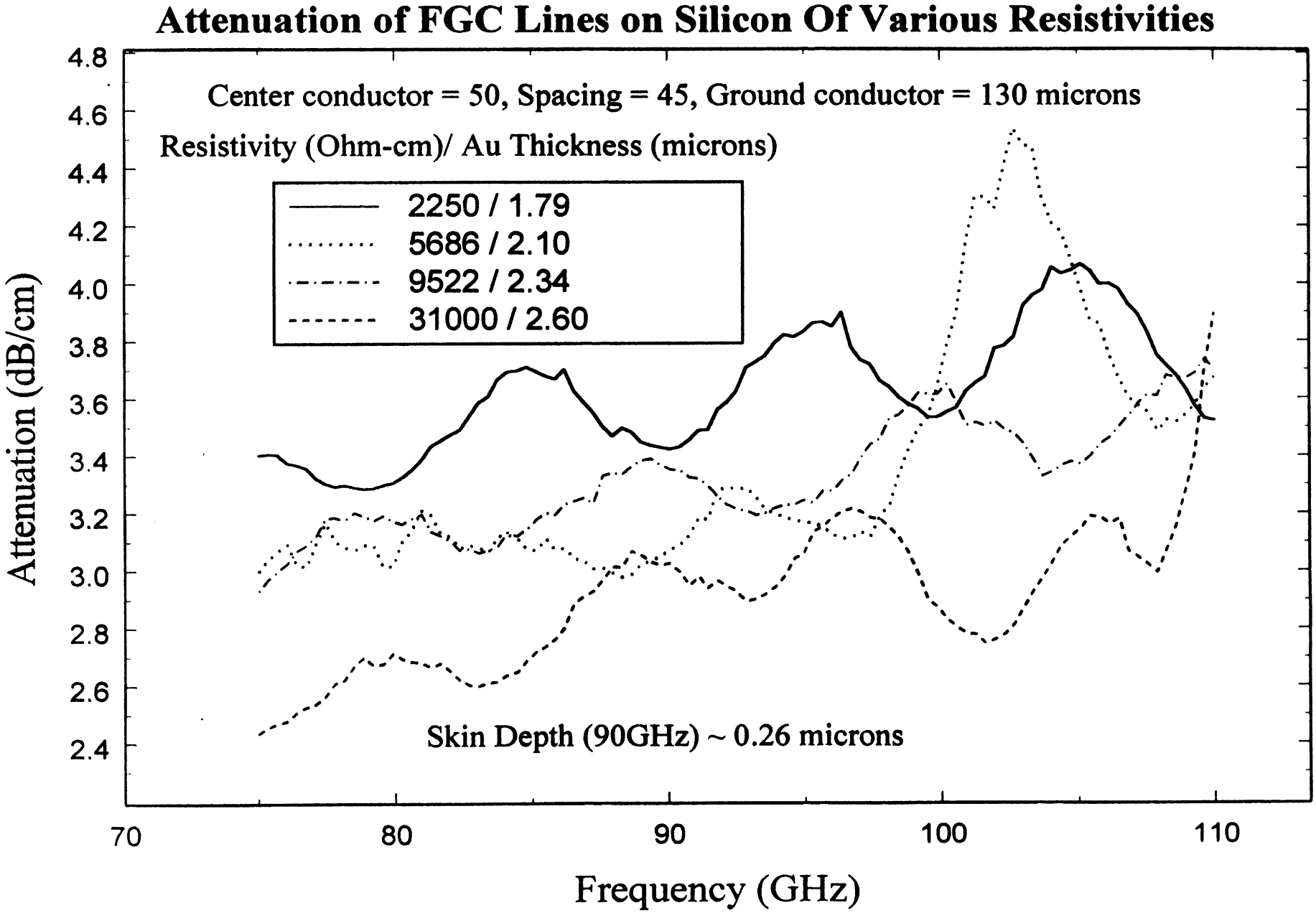
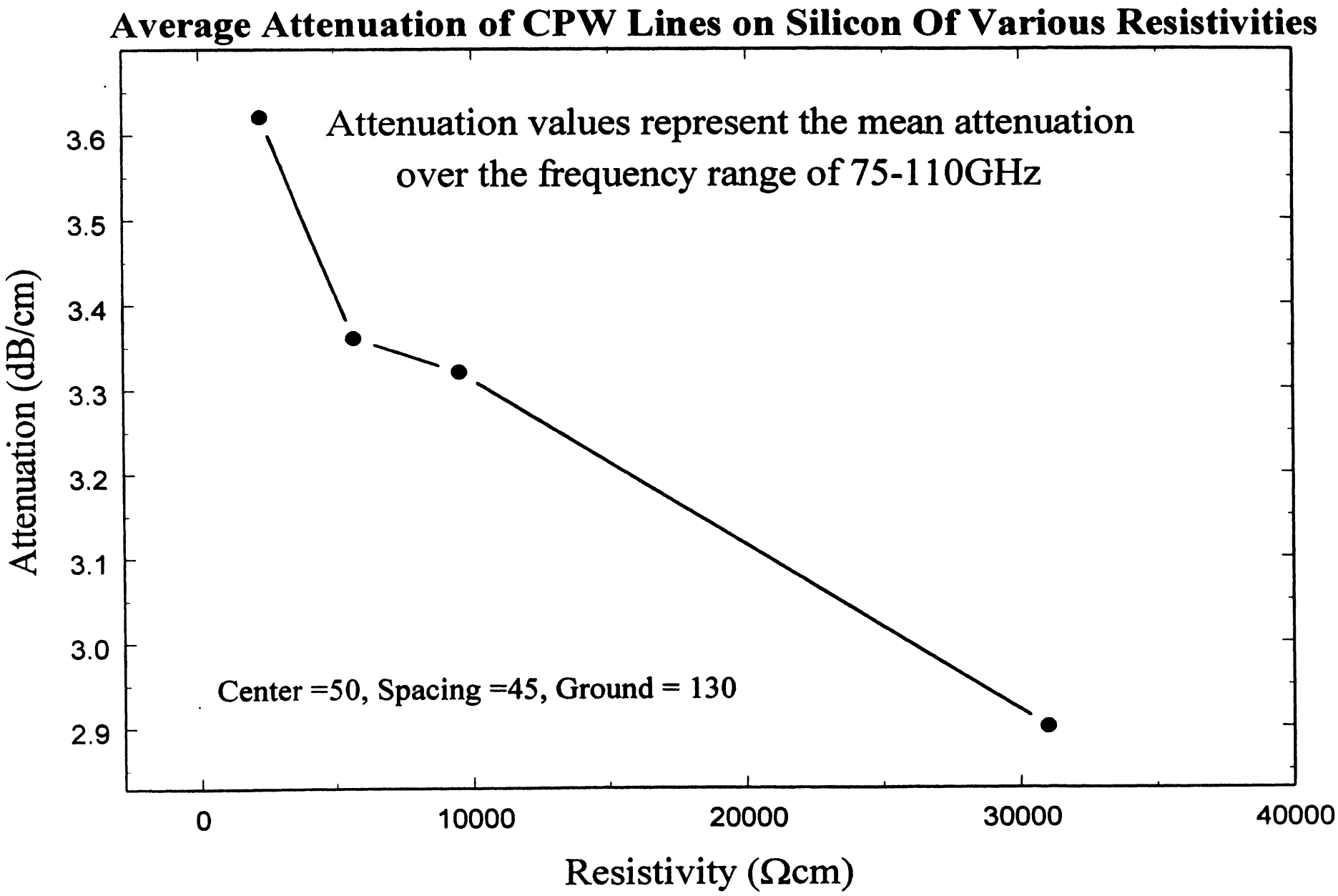

Attenuation of FGC Lines on Silicon Of Various Resistivities
Center conductor = 50, Spacing = 45, Ground conductor = 130 microns
Resistivity (Ohm-cm)/ Au Thickness (microns)
2250 / 1.79
5686 / 2.10
9522 / 2.34
31000 / 2.60
Skin Depth (90GHz) ~ 0.26 microns
Attenuation (dB/cm)
Frequency (GHz)
4.8
4.6
4.4
4.2
4.0
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
70
80
90
100
110

FIGURE 5


Average Attenuation of CPW Lines on Silicon Of Various Resistivities
Attenuation values represent the mean attenuation over the frequency range of 75-110GHz
Center =50, Spacing =45, Ground = 130
Attenuation (dB/cm)
3.6
3.5
3.4
3.3
3.2
3.1
3.0
2.9
0
10000
20000
30000
40000
Resistivity (Ωcm)

PART B: Micromachined high-Q filters

Lee Harle
GSRA, Radiation Lab
Prof. Linda P. B. Katehi
University of Michigan

Development of High-Q Microwave Resonant Cavity Filters
Summary of activity, 1/97 - 1/98

The filter project I have been working on was begun by John Papapolymerou as a resonant cavity project. The cavity circuit consists of two microstrip lines coupled through slots to one micromachined cavity, approximately 32 mm x 16 mm x 0.465 mm, producing a resonance around 10.3 Ghz, see Figure 1 [1]. The development of the cavity into a filter began in January 1997, when I began observing and learning fabrication techniques in the wafer processing clean room as John proceeded with his own research. I simultaneously began the development of an equivalent lumped element circuit of the cavity circuit using Libra microwave circuit simulation software. Configurations included ideal transformers to model the slots, RLC in various parallel and series combinations to model the behavior of the cavity, and an R between the transformers and the port to model stripline loss. It was understood that changing the slot position would result in a change in the input impedance. Hence, changing the transformer turns ratio would be proportional to slot position, and it was found that altering the turns ratio altered the bandwidth of the response. For series RLC, the higher the turns ratio, the narrower the bandwidth. For parallel RLC, the lower the turns ratio, the narrower the bandwidth. It is hoped that by developing a lumped element equivalent to a known cavity geometry, a correlation can be made between physical size and lumped element parameters, and hence any desired resonance and bandwidth response which can be modeled with an equivalent circuit can be transformed into a cavity circuit and produced in the lab.

In order to understand field behavior in relation to the cavity circuit in general, the slots and the stripline/slot/cavity transition, three dimensional modeling simulations were begun on a number of software platforms including HFSS, Momentum and Sonnet. Modeling was performed on the original single cavity configuration, as well as two cavities coupled together by various slot arrangements. Effort was largely concentrated on mapping the behavior of altered slot positions for single cavity configurations. It was discovered, as predicted by Libra simulations, that bandwidth varies with slot position. The original cavity resonator as designed and built by John with the slots approximately 1/2 wavelength apart produced approximately a 5% bandwidth around 10.3 GHz resonance. This design modeled in HFSS produced a 4.3% bandwidth at 10.35 GHz. Moving the slots farther apart by 1/4 wavelength produced a 6.8% bandwidth at 10.275 GHz. Moving the slots closer together by 1/4 wavelength produced a 1.3% bandwidth at 10.425 GHz. Two cavities with the slots in the "closer together" arrangement produced a bandwidth of about 1% around 10.4 GHz.

It was decided to fabricate several single cavity resonators, each with a different slot configuration, in order to fully understand the true influence of slot position before undertaking the task of multiple cavities coupled by slots. The cavity itself was also altered slightly. The original design involved a 500 (m wafer etched to form a 465 (m deep cavity whose interior was then completely metalized. Our process began with a 500 (m wafer which was etched completely

through, providing an open window in the wafer. The interior "walls" of the cavity were then metalized, another wafer that was to become the bottom of the cavity was metalized, the two wafers were bonded together with silver epoxy, and the entire cavity interior was again metalized to provided good step coverage and dc contact. At this time, one complete cavity circuit , with slot positions closer together than the original design, has been completed and measured. Filter behavior is observed, although it is lossy and does not exhibit the expected narrow bandwidth. Immediate attention will be given to solving this problem before proceeding to the next stage of assembling other altered slot position circuits and continuing with multiple cavity configuration fabrication.

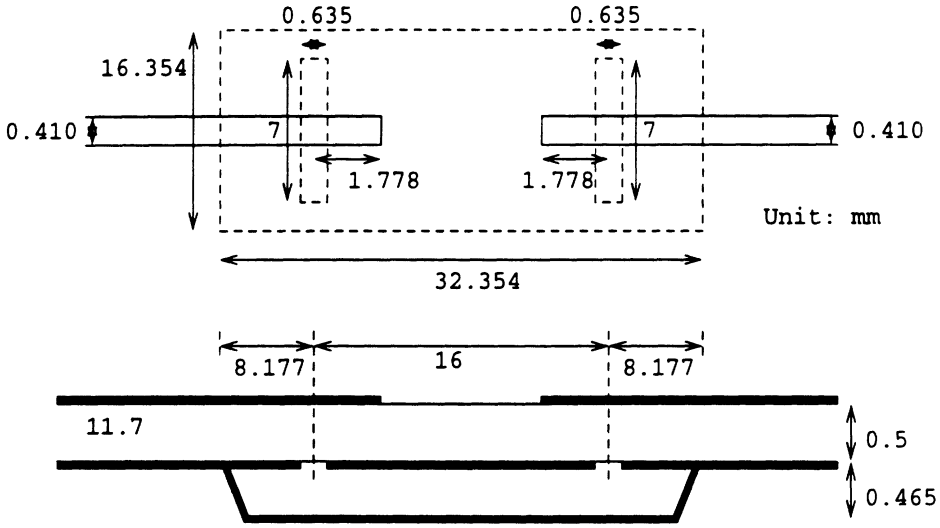


Figure 1

[1] J. Papapolymerou, J. C. Cheng, J. East, L. P. B. Katehi, "A Micromachined High-Q X-Band Resonator", IEEE Microwave and Guided Wave Letters, vol. 7, pp. 168 -170, June 1997.

Submitted to the 1998 European Microwave Conference

The effects of slot positioning on the bandwidth of a micromachined resonator

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Abstract

This paper presents the effect of slot positions on the bandwidth and the response of a micromachined high-Q X-Band resonator formed by a micromachined cavity. Theory and experiment indicate that a narrow-band, low-loss response can be achieved by changing the placement of the slots relative to the center of the cavity. As a result, narrow-band, low-loss, monolithic filters with small weight and planar characteristics can be designed.

I Introduction

Microwave high-Q resonators are traditionally made of metallic rectangular or cylindrical waveguides that are heavy in weight, costly to manufacture and difficult to integrate with monolithic circuits. Recently it has been shown [1] that a low-loss, high-Q resonator can be fabricated in a planar environment by using standard micromachining techniques [2]. The X-Band resonator shown in Fig. 1 consists of input and output microstrip lines that reside on top of a silicon wafer and couple energy into a micromachined cavity which is formed on a second wafer via slots. The energy that is inserted in the cavity can travel through it in the form of a propagating or evanescent wave. Measurements have shown an insertion loss of 0.36 dB and an unloaded quality factor Q_u of 506 that is in good agreement with the theoretical value of a rectangular metallic cavity of similar size [3]. This resonator can be used as a building element for the design and fabrication of narrow-band, low-loss filters and multiplexers made of multiple cavities of the same or different size. Energy between cavities is coupled via slots of different shapes and positions.

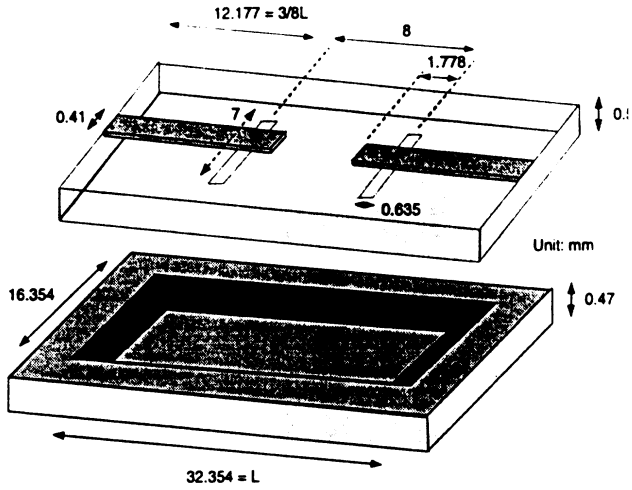

Figure 1: X-Band Resonator

Originally the slots are placed at 1/4 and 3/4 of the cavity length from the shorter edges of the cavity. Herein, we investigate both experimentally and theoretically the effects of reducing the distance between the two slots on the bandwidth and the insertion loss. In addition, theoretical results indicating the effect of

packaging on the performance of the resonator will be presented.

II Results and Discussion

The resonator shown in Fig.1 with the slots positioned at 3/8 and 5/8 of the cavity length from the shorter edges has been fabricated using two high resistivity 500 μm thick silicon wafers, with PECVD nitride grown on both sides of them. The microstrip lines are formed on the top surface of the first wafer by gold electroplating to a total thickness of 6 μm. CPW to microstrip transitions are included in order to measure the resonator with on-wafer probing. The ground planes of the CPW and microstrip lines are set at the same potential with the help of via holes. The cavity is fabricated on the second wafer by using chemical anisotropic etching (TMAH water based solution) up to a depth of 470 μm and is then metallized to a thickness of approximately 3 μm. The two wafers are finally bonded together using silver epoxy glue that is cured at 150^oC.

The fabricated resonator was measured using a TRL (Thru-Reflect-Line) calibration referenced at the slots and the results are compared with theoretical ones in Fig. 2. Theoretical results were obtained by using the HP High Frequency Structure Simulator [4]. As can be seen from Fig. 2 there is very good agreement between the simulated and measured response. The small discrepancy (1%) in the resonant frequency can be attributed to the inherent numerical error of the HFSS software and fabrication tolerances. The measured resonator exhibits a bandwidth of 2% (210 MHz) at a resonant frequency of 10.525 GHz. The insertion loss, after de-embedding the loss on the two open end stubs extending beyond the center of the slots, is measured to be -1.1 dB. Comparison of these results to the ones presented in [1] can be seen in Fig. 3 where we observe a 58% reduction in the bandwidth (from 500 to 210 MHz) and a 0.74 dB increase in insertion loss. These results indicate that by altering the positions of the coupling slots relative to the center of the cavity we can change (increase or decrease) the bandwidth of the resonator at the price of increased loss. This of course is expected since the

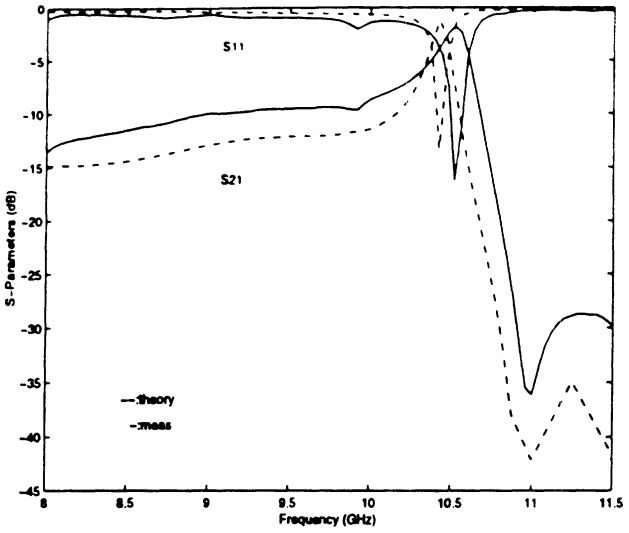

Figure 2: Measured and simulated results for the resonator of Fig.1.

Q_u of the resonator is determined by the cavity and is independent of the position of the slots. Preliminary simulations and measurements of the resonator with the slots positioned at 1/8 and 7/8 of the cavity length from the shorter edges show a bandwidth much greater than the original one of 500 MHz.

From Fig. 2 we can also observe a slight asymmetry in the response around the resonance. This is due to the fact that the two microstrip lines are close enough (0.4 λ_g) and power is coupled from one to the other directly via substrate modes. In order to eliminate this effect and make the response more symmetric around resonance we can use micromachined on-wafer packaging [5] to isolate the microstrip lines from one another both on top and inside the substrate. For this purpose an HFSS simulation was run where one PEC plane is placed on top of the structure and another is placed between the two lines shorting the top pec to the slot plane. Results can be seen in Fig. 4, where we observe that packaging reduces the suspected coupling occuring below 10.3 GHz by as much as 4 dB. In addition, we observe that there is a small coupling of about -16 dB below 10 GHz that can be attributed to evanescent modes excited around the slots inside the cavity. Presently study is under

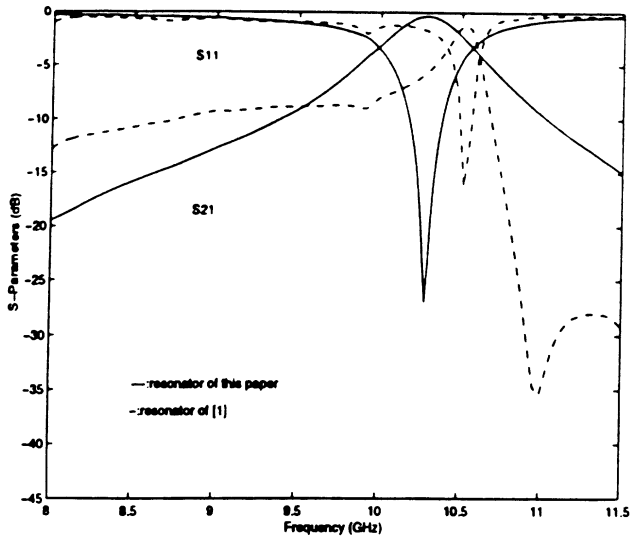

Figure 3: Measured results for the two resonators with different slot positions.

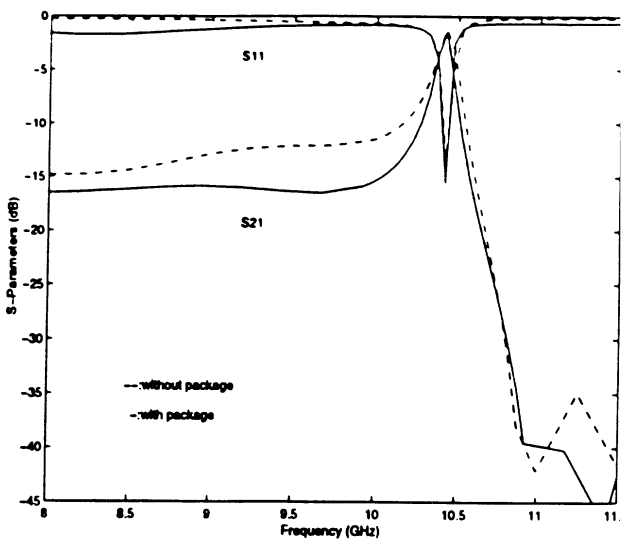

Figure 4: Simulated response of the packaged and non-packaged resonator.

way to further understand the effect of evanescent modes and improve out-of-band rejection. In a micromachined filter design with multiple cavities evanescent modes can be used instead of propagating ones to decrease the size of the cavities since these modes operate below cut-off.

III Conclusions

The effects of slot positions in a micromachined resonator have been presented. Although the Q_u is determined by the cavity itself, the bandwidth is determined by the relative position of the slots. Specifically when the slots are placed closer to the center of the cavity the bandwidth is reduced and the insertion loss is increased. The close proximity of the slots also produces direct coupling between the microstrip lines that can be eliminated with appropriate packaging of the structure and evanescent modes that affect the shape of the response around resonance.

IV Acknowledgement

This work was partly funded by the U.S. Army Research Office (MURI program) and partly by the U.S. Office of Naval Research.

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[2] R.F. Drayton, T.M. Weller and L.P.B. Katehi, "Development of miniaturized circuits for high-frequency applications using micromachining techniques," *International Journal Microcirc. Elec. Packaging*, vol. 3, 1995.

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PART C: On-wafer packaging of circuit and filter components for high-efficiency and low loss

Experimental Characterization of Silicon-Based Packages for High Frequency Applications

Future advances in electronic packaging research are very important because current package design limitations play such an integral role in the breakdown of millimeter-wave circuit performance. Novel processing techniques which can be used to realize low cost alternatives are needed for the communications industry, while other customers require high performance, high reliability solutions. Given the excellent mechanical and electrical properties of Si, micromachining and standard IC processing techniques are combined to realize monolithic and hybrid packages. This work focuses on developing packaging techniques for high frequency circuits using silicon (Si) as the base substrate material.

Currently a packaged three-stage low noise amplifier is being characterized where Si is the host substrate providing the bias and matching networks for InP HEMTs in a K-band design. Si-micromachining is combined with flip-chip device mounting techniques to show the usefulness of Si as a mechanical as well as electrical material for high frequency, low cost hybrid. The amplifier circuit is redesigned using shielded coplanar waveguide (CPW) and fabricated at Michigan while the transistors are provided for and mounted by Hughes Research Laboratories. Noise figure and S-parameter measurements are conducted at Michigan and are expected to show improvements over the original unshielded microstrip design.

During the fall of 1997, an extension of the work by K. Herrick on selective etching of slots in finite ground CPW was conducted. The characteristic impedance of transmission lines with total widths (S+2W+2Wg) of 300 to 400 microns was compared with non-etched lines of the same dimensions for 100 and 500 micron thick substrates up to W-band. It was confirmed that losses are reduced and impedance is increased by anisotropically etching the slots. This information will be used in the design of a vertically integrated Si-micromachined W-band power distribution/combining network.

In conjunction with Prof. T. Weller at USF, 45 and 90 GHz power dividers to be used in the W-band network were fabricated and measured.

During 1996, a Si-based package for discrete components was designed and fabricated using thin-film processing and Si-micromachining techniques. The Si chip carrier is based on a high temperature cofired ceramic (HTCC) hermetic package fabricated by Hughes Research Laboratories for NASA Lewis Research Center. Alumina is the base material used in the hermetic package that supports a phase shifter chip. The Si package was a redesign of the alumina one with changes made only in reference to fabrication differences. K-band package losses were reduced by as much as 0.5 dB with the Si design providing accurate line-width resolution and low loss interconnects between test circuit and package. Bulk micromachining of Si created the layers to assemble the package and provide an electromagnetic shield for circuit isolation.

In 1995, high density interconnects and conformal packaging issues were investigated with Prof. R. F. Drayton. Parasitic radiation and unwanted coupling due to substrate mode excitation was reduced by completely shielding Si interconnects. Drayton previously showed how to create the upper and lower shielding cavities for straight-line interconnects, however in high density circuits routing of transmission lines is such that right-angle bends are produced. Fabrication techniques were explored to realize cavities that can shield such lines by conforming to their shape. Cross-coupling between neighboring microstrip lines was reduced by as much as 40 dB up to Ka-band. By incorporating micromachining and IC processing techniques, Si substrates provided mechanical protection and electrical integrity for high performance circuits.

THE EFFECTS OF LINE WIDTH AND SLOT ETCHING ON SILICON-BASED CPW AT MM-WAVE FREQUENCIES *

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Abstract - An experimental study is in progress to investigate the performance of coplanar waveguide (CPW) transmission lines which are printed on high-resistivity silicon. In one sample group a nominal characteristic impedance of 50 Ω is maintained while the ground plane spacing and ground plane width are varied. In this group conventional CPW lines are included, as well as lines in which the slots have been etched to create a triangular-shaped recess between the center conductor and ground planes. The slot-etching technique is known to be an effective method to decrease attenuation, and is demonstrated here with measurements up to 67 GHz. In another group of samples identical lines with and without etching are characterized to determine the difference in attenuation and characteristic impedance. All lines used in this work are classified as finite ground CPW (FGC), as the ground plane width is comparable to the slot and center conductor dimensions.

1 Introduction

In recent years several important advances in mm-wave technology have been reported that involve the use silicon as the substrate material [1, 2]. A particular advantage of silicon that has driven considerable research is that it can be micromachined with high precision using a variety of dry and wet etch processes. This property has been utilized to develop such devices at 2.54 THz corner-cube antennas [3] and planar filters at 94 and 250 GHz [4, 5]. The machining capability also enables the realization of structures with integrated shielding and vertically-connected lines, paving the way for compact, multi-level mm-wave components.

If low loss, high performance silicon architectures are to be designed it is critical to have a thorough understanding of the attenuation characteristics of planar lines. In this study two groups of finite ground coplanar waveguide lines (FGC), in which the ground plane width is similar to the slot and center conductor width, were used. For the first group standard 50 Ω lines, with varying cross-section dimensions, were used as a benchmark to compare the characteristics of 50 Ω lines in which the silicon was selectively removed from the slots (Figures 1 and 2). Partial removal of the substrate has been known as an effective means of reducing loss [6] and the results presented

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herein demonstrate a mean reduction around 30–40%. In the second group of samples identical lines were tested with and without the etching process. This study included lines with varying aspect ratios and total line widths, and was conducted to understand how the etch process affects the line impedance and attenuation for a given geometry. The work presented herein follows from previous research described in [7].

2 Line Geometries

A listing of the coplanar waveguide lines studied in this work is presented in Figure 1. The standard, non-etched geometries were designed toward a characteristic impedance of 50 Ω using the program *LINPAR* [8]. This program takes into account finite ground plane widths, and was used to ensure that the characteristic impedance was maintained as variations were introduced in the parameter W_g. For the etched CPW lines, an approximate value of $\epsilon_{re} = 4$ was taken from previous related work [7] and used for the impedance calculations. A two-dimensional point-matching code was also utilized for the purpose of analyzing the inhomogeneous cross-section. It is worth noting that several fabrication-related parameters such as etch time, concentration and temperature affect the amount of undercutting that occurs beneath the conductors and thus the realized impedance. Better characterization of the processing was one of the goals of this work.

The lines were printed on a 525 micron-thick, (100)-oriented silicon wafer with a resistivity greater than 2000 Ω-cm. An 8500 Å-thick high temperature oxide was grown on each side of the wafer.

3 Circuit Fabrication

For Group A (see Figure 1), the circuit metal consisted of a 500/9500 Å Ti-Au layer that was deposited using an evaporation/lift-off process. For the CPW lines with etched slots, the required openings were formed in the oxide layer using buffered hydrofluoric acid (BHF), prior to metal deposition. After depositing the metal, the silicon machining was performed using a 20% tetramethylammonium hydroxide (TMAH) solution at 85° C. This is an anisotropic etchant that etches in the (100) direction at a rate of approximately 30 μm/hr.

For Group B, the lines were deposited by evaporating a 500/1500/500 Å Cr-Au-Cr seed layer and then electroplating to a thickness of 3 μm. The micromachining was performed using an F type ethylene diamine pyrocatechol (EDP) solution that etches at a rate of 80 μm/hr. For the non-etched lines the oxide layer was removed from the slot opening prior to measurement.

When the micromachined lines from Group A were first measured an excessive amount of loss was observed. As these characteristics are not found when other anisotropic etchants such as EDP are used, it is speculated that the TMAH etch chemistry results in a build-up of free-carriers at the silicon surface. It was discovered that a short (30 minute) post-KOH (potassium hydroxide) etch resolved the problem. The fact that TMAH can successfully be used with this procedure is important, since it has a low toxicity level compared to EDP and it etches SiO_2 at a slower rate than KOH.

4 Experimental Results

The measured results shown in the following sections were performed on-wafer using a vector network analyzer and 150 μm-pitch pico probes [9]. The instrument calibration was performed using the NIST mult-line thru-reflect-line (TRL) algorithm [10, 11].

The characteristic impedances of the lines from Group B were calculated by performing a short-open-load-thru (SOLT) calibration to the wafer probe tips and then measuring the return loss of the lines. The return loss, line length, effective dielectric constant and attenuation are then used with the Series IV/Libra transmission line model to curve fit the return loss data and extract the characteristic impedance.

4.1 Experimental Results

Group A

The measured attenuation for the etched 50 Ω CPW geometries is shown in Figure 3. The curves follow the expected behavior of decreasing attenuation with increasing line width, with the widest line (Set 6, S+2W = 378 μm) exhibiting a loss of 0.06 dB/mm at 30 GHz. For Set 1, which has a line width of 130 μm, the attenuation is approximately 0.2 dB/mm. A summary of the attenuation versus line width at 30 GHz is given in Figure 4. Similar data for the non-etched lines will be presented at the conference.

A comparison of the normalized phase constant, β/K_o, for each etched set is given in Figure 5. The results indicate that the phase velocity tends to decrease as the line width (S+2W) increases. This is partially the result of an increase in the relative amount of undercutting beneath the center conductor and ground plane with the narrower lines. The anisotropic etchant has a finite selectivity with respect to etch rates in different crystal planes, leading to an inevitable removal of some dielectric beneath the conductors (see Figure 2). The dispersive behavior of the wider lines is also evident, and may be caused by coupling to the CPW-like surface wave mode described in [12]. The critical frequencies for the TM and TE surface wave modes, at which the phase constants equal that of the CPW mode, are above 56 GHz for these geometries.

Group B

The measured attenuation for the geometries from Group B is given in Figures 6-9. The data in Figures 6 and 7 correspond to geometries in which the total line width (including the ground planes) is approximately 300 μm, for the non-etched and etched sets, respectively. There is a steadily increasing improvement with frequency for the etched geometries, resulting from an increase in the line impedance and the reduction in dielectric-related loss. The same trend is observed in comparing Figures 8 and 9, which correspond to lines that are approximately 400 μm wide. A summary of the data at 30 GHz (Figure 10) shows characteristic impedance and attenuation as a function of line aspect ratio, S/(S+W).

5 Summary

The results presented in this paper show that low loss CPW lines can be realized on high resistivity silicon substrates using simple slot etching techniques. Lines with ground-plane spacing

as small as 130 microns demonstrate an attenuation of 0.2 dB/mm at 40 GHz, which is 0.05 dB better than reported data for a comparable non-etched line on semi-insulating GaAs [13].

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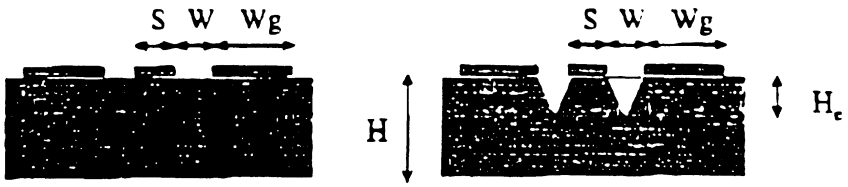

Non-Etched	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6	Set 7
W	25	36	36	54	72	72	108
S	41	58.5	58.5	87	117	117	175
Wg	82	117	185	278	234	370	351
Etched	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6	Set 7
W	27	39	39	58	78	78	116
S	77	111	111	167	222	222	339
Wg	370	185	234	278	234	370	351

GROUP A

	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6	Set 7	Set 8	Set 9
W	24	40	35	40	30	20	60	50	40
S	40	64	55	50	65	100	45	50	60
Wg	106	120	90	85	95	100	115	125	130
S+2(W+Wg)	300	384	305	300	315	340	395	400	400
Z_o Ω (non-etched)	55	55	53	55	54	38	64	42	54
Z_o Ω (etched)	85	70	75	82	68	54	90	88	80

GROUP B

Figure 1. Illustration of the non-etched and etched coplanar waveguide geometries. The etch depth, H_e, is approximately 0.7W. All dimensions given in the tables are in microns. The non-etched and etched lines in Group A are on separate substrates and were all designed toward a nominal 50 Ω impedance. The lines in Group B were measured before and after etching and cover a range of impedance values.

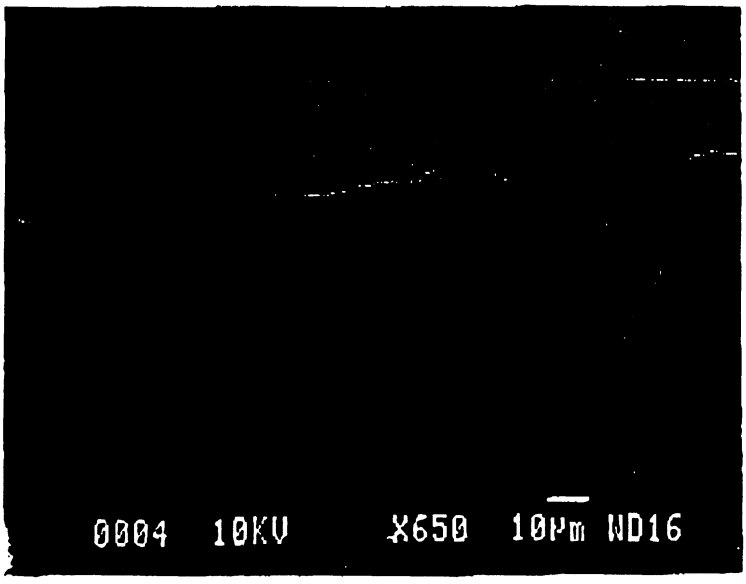

Figure 2. SEM microphotograph of an etched CPW line.

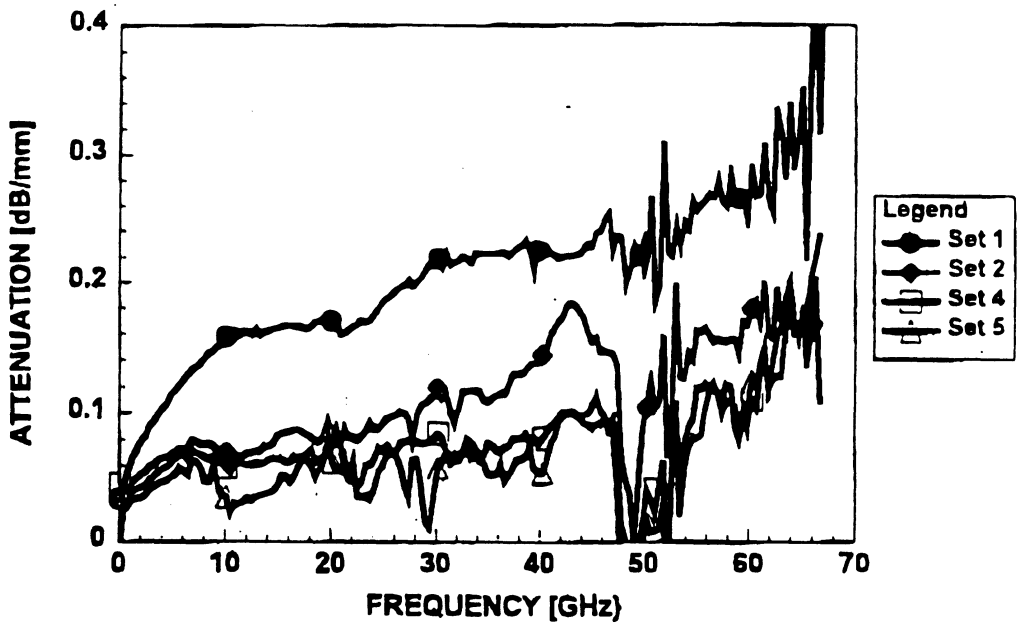

Figure 3. Measured attenuation for the etched Sets 1, 2, 4 and 5 from Group A.

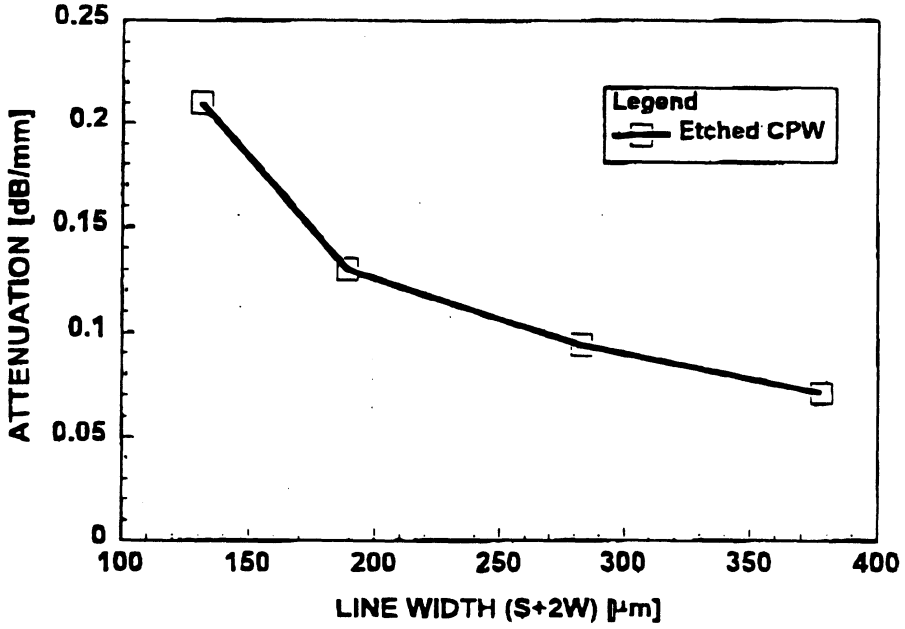

Figure 4. Measured attenuation at 30 GHz versus line width for the etched CPW lines from Group A.

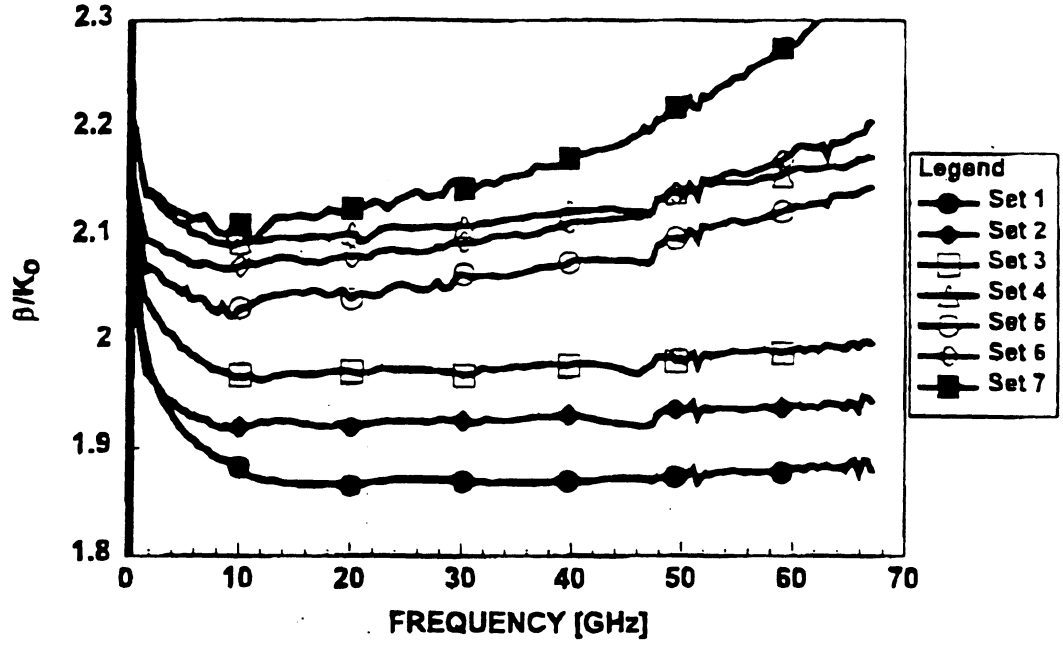

Figure 5. Normalized phase constant for the etched Sets 1-7 from Group A.

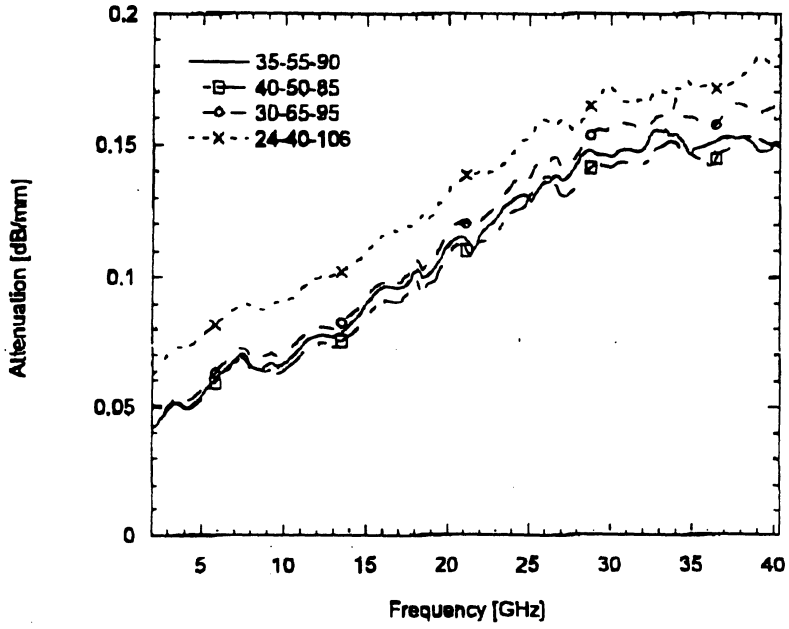

Figure 6. Measured attenuation for Sets 1 and 3-5 from Group B, without etching. The total line width is around 300 microns.

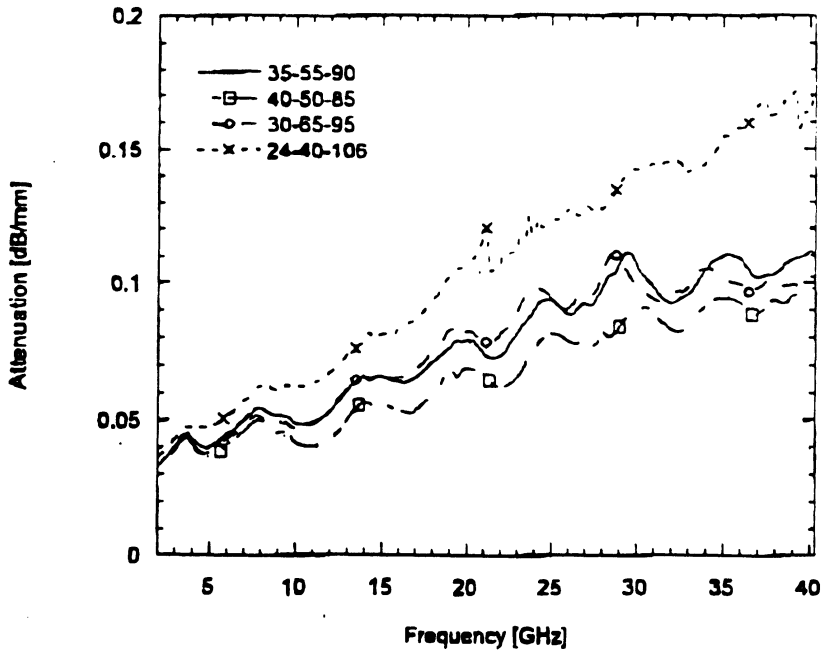

Figure 7. Measured attenuation for Sets 1 and 3-5 from Group B, with etching. The total line width is around 300 microns.

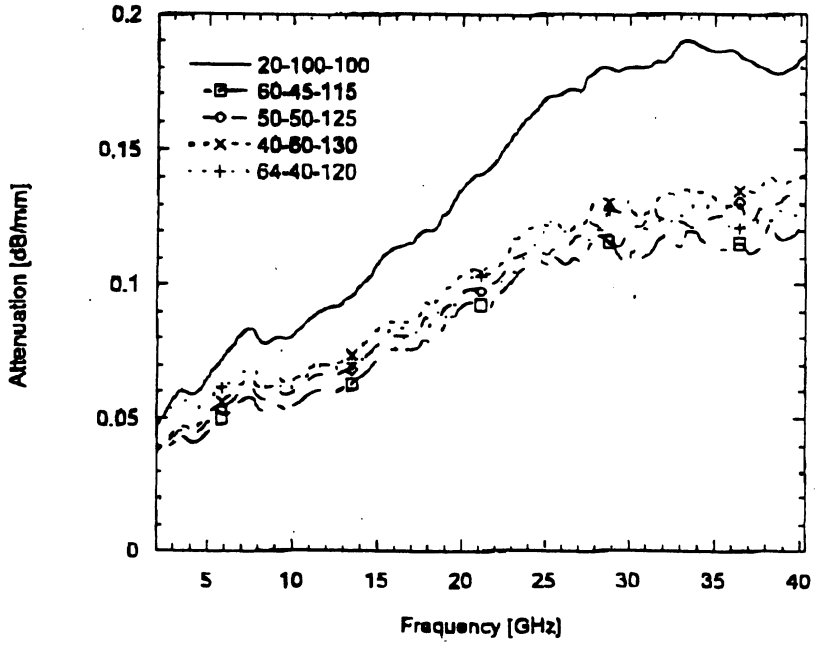

Figure 8. Measured attenuation for Sets 2 and 6-9 from Group B, without etching. The total line width is around 400 microns, except for Set 6 which is 340 microns wide.

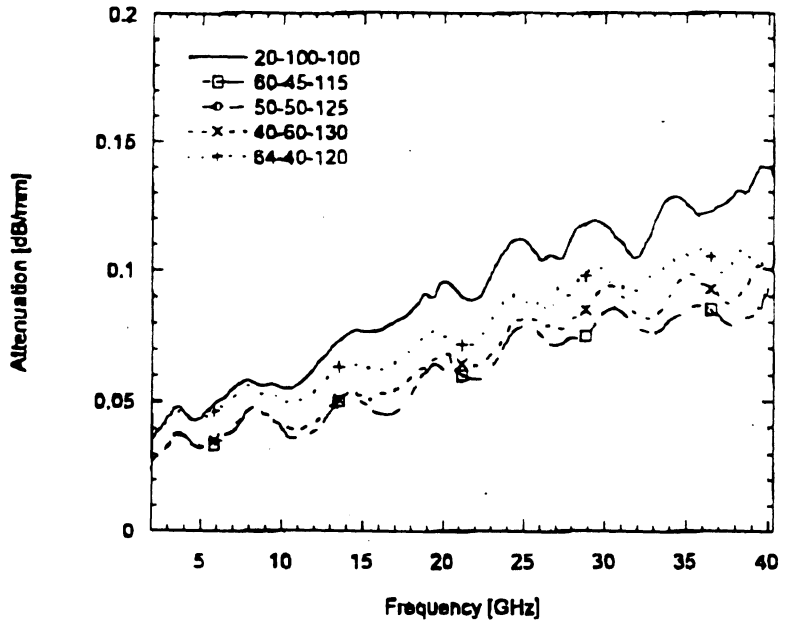

Figure 9. Measured attenuation for Sets 2 and 6-9 from Group B, with etching. The total line width is around 400 microns, except for Set 6 which is 340 microns wide.

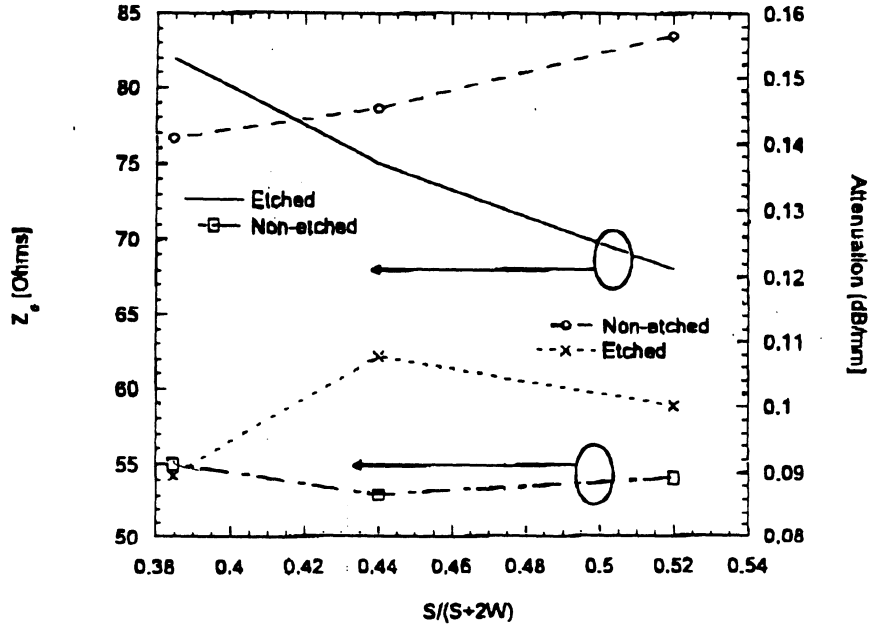

Figure 10. Measured impedance versus aspect ratio, S/(S+2W), for etched finite ground CPW lines from Group B, where S+2W is approximately 125 microns. The measured attenuation for etched and non-etched lines at 30 GHz is given on the right.

The Effects of Line Width and Slot Etching on Silicon-Based CPW at Mm-Wave Frequencies

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Outline

- **Introduction**
- **CPW Geometries**
- **Fabrication**
- **Experimental Results**
- **Conclusions**

Introduction

- Silicon use at mm-wave frequencies
  - Silicon mm-wave integrated circuits (SIMMWICs)
  - Micromachined transmission lines
  - Self-packaged circuits
  - Multi-level, stacked-wafer architectures
- Experimental characterization of attenuation is needed
- Slot-etching Si-based coplanar waveguide (CPW) :
  - Increase realizable characteristic impedance
  - Reduce line attenuation

Introduction

- This work focuses on experimental characterization of two groups of CPW lines
  - **GROUP A:**
    - Designed toward a nominal 50 Ω
    - 7 sets are standard CPW geometries
    - 7 sets have the silicon partially removed from the slots
  - **GROUP B:**
    - Identical cross-section dimensions
    - 9 sets are standard CPW geometries
    - 9 sets have the silicon partially removed from the slots

CPW Geometries

- Fabricated on 500 micron-thick, high resistivity silicon (greater than 2000 Ohm-cm)
- 0.85 μm-thick high-temperature SiO_2 layer on each side of the wafer
- Cavity depth on etched lines: $H_e = 0.7\ W$

CPW Geometries - Group A

Non-Etched

	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6	Set 7
W	25	36	36	54	72	72	108
S	41	58.5	58.5	87	117	117	175
Wg	82	117	185	278	234	370	351

Etched

	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6	Set 7
W	27	39	39	58	78	78	116
S	77	111	111	167	222	222	339
Wg	370	185	234	278	234	370	351

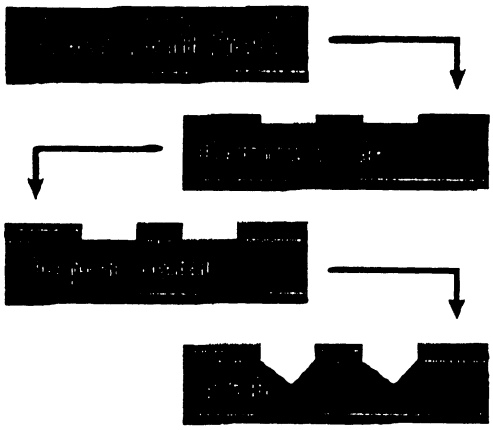
CPW Geometries - Group B

	Set 1	Set 2	Set 3	Set 4	Set 5	Set 6	Set 7	Set 8	Set 9
W	24	40	35	40	30	20	60	50	40
S	40	64	55	50	65	100	45	50	60
Wg	106	120	90	85	95	100	115	125	130
Wt	300	384	305	300	315	340	395	400	400
Zo NE	55	65	53	65	64	38	64	42	54
Zo E	85	70	75	82	68	54	90	88	80

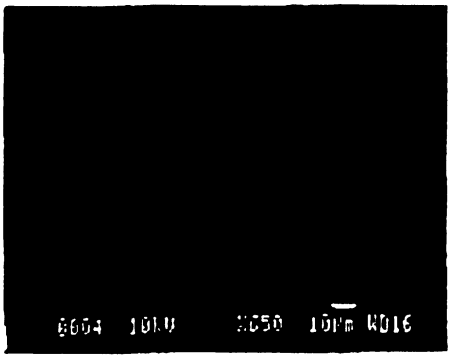
$Wt = S + 2(W + Wg)$ NE = non-etched E = etched

Fabrication

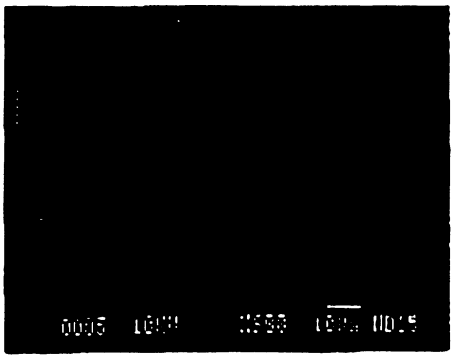
- Pattern wafer and remove oxide in slot regions using BHF
- Pattern wafer and deposit metallization (lift-off or plating)
- Etch silicon using anisotropic etchant (TMAH or EDP)



Fabrication

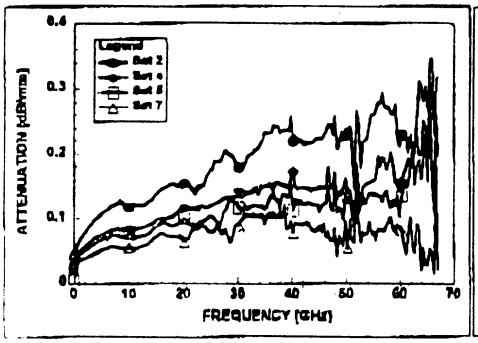


TYPICAL UNDERCUT

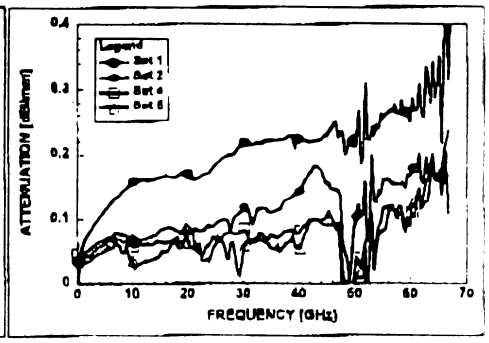


SEVERE UNDERCUT

Group A - Attenuation



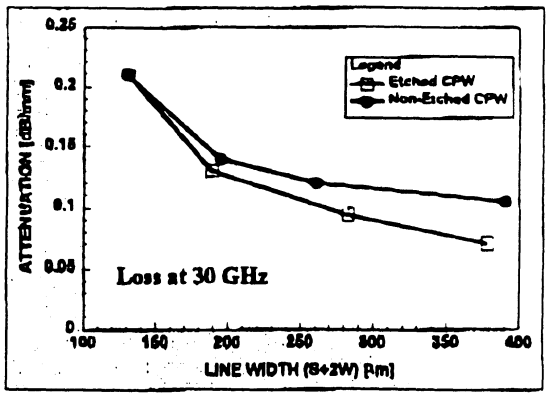
Non-etched CPW lines



Etched CPW lines

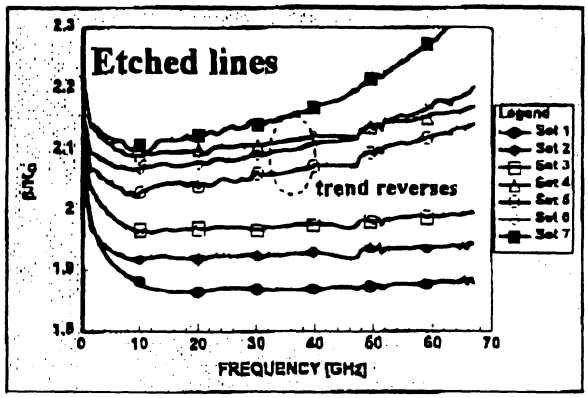
Group A - Attenuation

- Etching-induced reduction in attenuation increases with increasing line width
- For 400 μm-wide lines, loss decreases by 40%



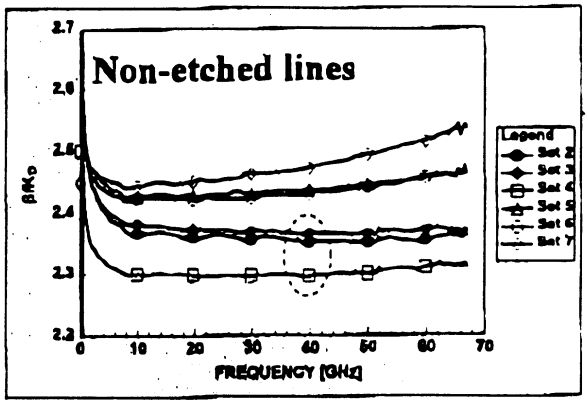
Group A - Phase Constant

- β <u>generally</u> decreases with decreasing line width
- Narrow lines have more severe undercut and more field confinement in the slots

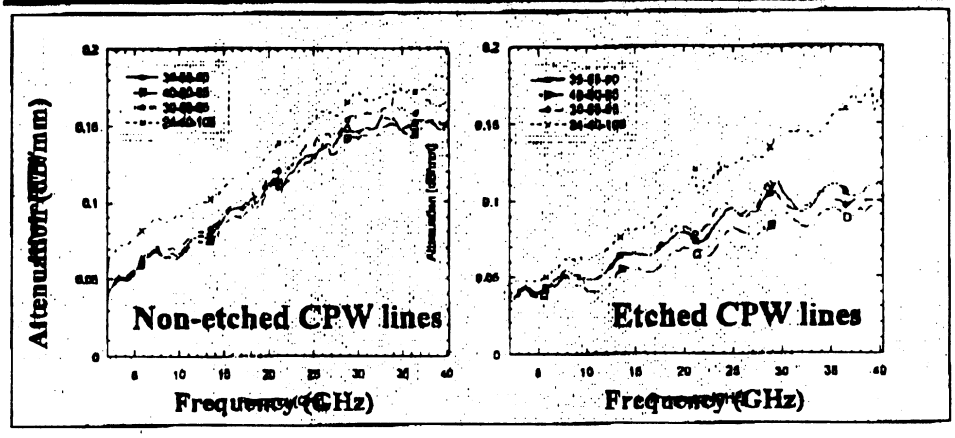


Group A - Phase Constant

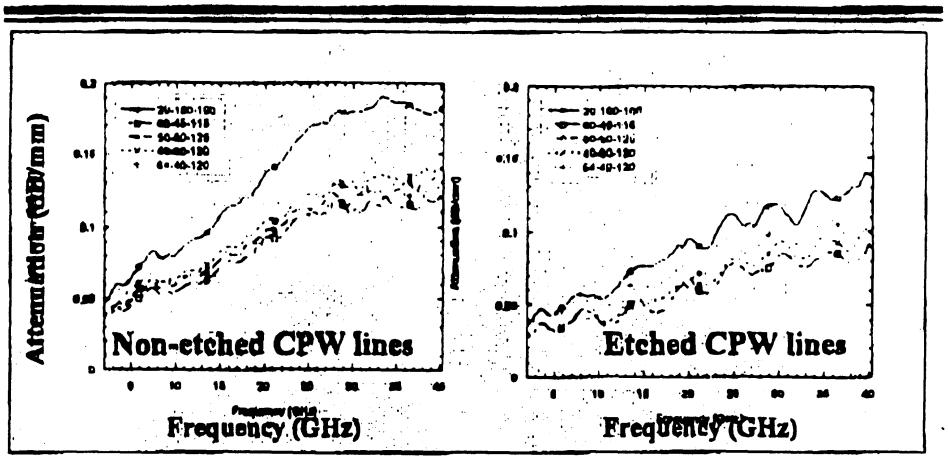
- β generally decreases with decreasing line width
- Wide lines show expected dispersion (partially due to finite substrate thickness)



Group B - 300 μm Wide Lines

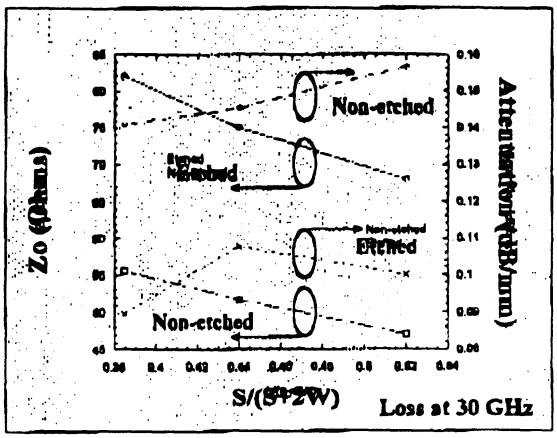


Group B - 400 μm Wide Lines



Group B - Attenuation and Z_o

- Attenuation decreases by approximately 40% with etching
- Impedance increases by approximately 50% with etching



Conclusions

- Extensive data on Si-based CPW attenuation has been presented
- For 50 Ω lines, partial removal of the silicon results in reduced loss: improvement increases with increasing line width
- Slot etching increases the impedance level which can be achieved, resulting in lower attenuation

Acknowledgements

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Optimization of Mm-Wave Distribution Networks Using Silicon-Based CPW

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Abstract **— This paper describes work relating to the optimization of silicon-based, coplanar waveguide (CPW) air-bridge and bend discontinuities. Experimental results verify that the return loss is improved by introducing a step-compensation in the CPW center conductor. The technique is demonstrated in the design of asymmetric coplanar-strip Wilkinson power dividers at 45 GHz.**

1 Introduction

Coplanar waveguide (CPW) is a uniplanar transmission line technology that provides excellent performance at mm-wave frequencies. However, circuit configurations such as power distribution networks are comprised of multiple bends, impedance steps and Tee-junctions which require some form of compensation to mitigate the associated parasitic effects. This work addresses the use of a step-taper in the CPW center conductor to improve the response of air-bridge and right-angle bend discontinuities. The step-compensation method is also demonstrated in the design of an asymmetric coplanar strip (ACPS) Wilkinson power divider that is fed by CPW lines.

The experimental results presented in this paper were obtained from on-wafer measurements using a Wiltron 360B vector network analyzer. Instrument calibration was performed using the NIST Multical software [1]. All circuits were fabricated on a high-resistivity (> 2000 Ω-cm) silicon wafer, and the gold traces were electro-plated to a thickness of 2.5 μm.

2 Air-Bridge and 90° Bend Compensation

An air-bridge in coplanar waveguide introduces an excess shunt capacitance due to the parallel-plate structure formed by the CPW center conductor and the air-bridge span. For the line geometries studied in [2], the value of this capacitance was determined to be around 1.5 times the value found from the simple, parallel-plate approximation. Based on the numerical and experimental modeling done in relation to this work, the scaling factor is dependent upon the aspect ratio of the CPW line beneath the span. Scaling factors between 1.5 and 3 have been observed for aspect ratios between 0.45 and 0.15, respectively.

The compensation for the excess air-bridge capacitance can be realized by reducing the width of the CPW line beneath the air-bridge. In [3] this technique was considered from the viewpoint of increasing the effective characteristic impedance of the line, in order to offset the decrease in Z_o affected by the air-bridge. A limitation of this perspective is that a localized narrowing of the center conductor may not provide enough compensation. An alternative approach taken here is to treat the air-bridge as a lumped capacitance, and then apply a transmission line model to derive the required length of high-Z_o line on either side of the air-bridge to achieve an impedance match in the desired frequency band. The resulting equation for the electrical line length on each side of the air-bridge (at the center frequency) is as follows:

$$\theta = \frac{Z_o^2 \, Z_h \, \omega C_{ab}}{2(Z_h^2 - Z_o^2)} \tag{1}$$

where Z_o is the nominal CPW impedance, Z_h is the impedance in the high Z section and C_{ab} is the air-bridge capacitance. A comparison of the measured return loss from a single air-bridge with and without the step compensation, is shown in Figure 1. While the low frequency response is worsened by the taper length, the performance in the band of interest around 45 GHz improves by approximately 12 dB.

One way in which air-bridges are frequently used is to suppress the excitation of the coupled slot-line mode in laterally asymmetric geometries such as a right-angle bend. Without proper compensation, the combined discontinuities of the bend and the air-bridges can lead to poor return loss performance. One approach for chamfering a 90° bend was recently reported in [4]. This is referred to here as the triangular taper, as illustrated in Figure 2. Using a similar transmission line model as described above, a second technique utilizing step compensation is derived (right-hand side of Figure 2). A comparison between these two methods is shown in Figure 3, along with the response of a non-compensated bend. These data come from measurements of a single bend, which has the second port terminated in a matched load. The targeted center frequency around 45 GHz was not obtained for the step-design, however an improvement of approximately 10 dB was achieved near 55 GHz.

3 Wilkinson Power Dividers

The underlying objective of this research is to develop high-performance distribution networks at W-band, and the geometry selected for power division and combination was the Wilkinson coupler. Previous authors have reported on 110 GHz Wilkinson designs using a coplanar waveguide approach [5, 6]. In this work, CPW and asymmetric coplanar strip (ACPS) [7] geometries are being pursued in parallel, since the characteristic impedances obtainable with silicon-ACPS provide greater versatility in the distribution network layout.

As a preliminary step toward the W-band network, several 45 GHz Wilkinson couplers were developed to examine the effects of the step compensation approach. A typical ACPS design, in a back-to-back configuration, is illustrated in Figure 4. The measured S-parameters for a single coupler with no compensation are shown in Figure 5. The insertion loss is approximately 3.4 dB, however the minima in S_{11}[1] and S_{22} are displaced by 20 GHz; this can be ascribed to excess capacitance at the input and output ports, as verified with circuit-level modeling. The results given in Figure 6 pertain to a single coupler which incorporates the step compensation at all air-bridges. The return loss at each port noticeably improves, with no degradation in the insertion loss.

4 Summary

This paper has described a step-compensation technique for improving the mm-wave performance of coplanar waveguide discontinuities such as air-bridges and bends. The approach was also demonstrated in the design of a silicon-based, 45 GHz ACPS Wilkinson power divider. Additional results for bend and Tee-junction geometries will be presented at the symposium, along with data on CPW and ACPS Wilkinson dividers at 45 and 90 GHz.

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[1] For the Wilkinson coupler results, port 1 is the input port in the divider configuration.

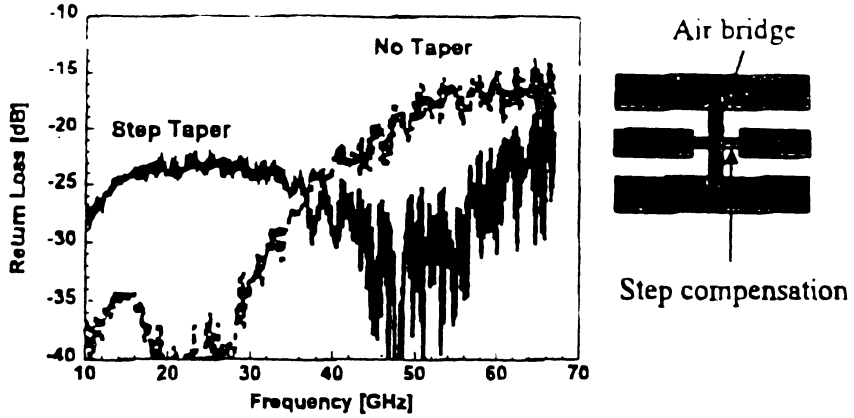

Figure 1. Measured return loss for a 30 μm-wide air-bridge (height=2.5 μm) across a coplanar waveguide transmission line (S=58 μm, W=36 μm), with and without step compensation. The center conductor width is reduced from 58 to 20 μm in the tapered section, and the step length is 150 μm.

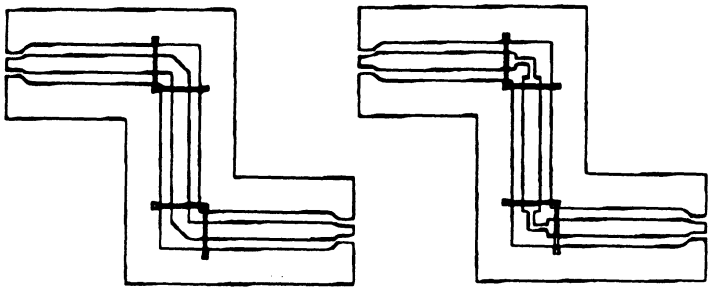

Figure 2. Illustration of coplanar waveguide (back-to-back) right-angle bends using a triangular taper after Gupta [4] (left) and a step-compensation taper (right).

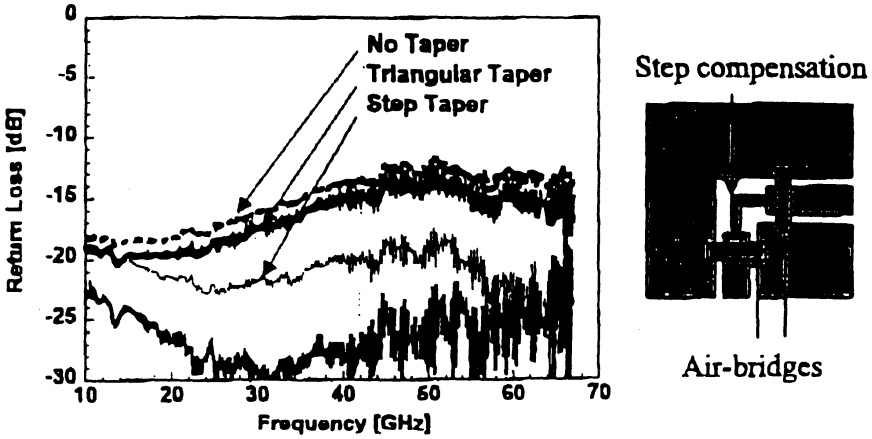

Figure 3. Measured return loss for coplanar waveguide right-angle bends, configured with a matched termination on the second port. Results are shown for a bend with no tapering, a bend using the triangular taper after Gupta [4], and the step taper. The air-bridge and CPW dimensions are the same as those given in Figure 1, and the tapered sections extend between the air-bridge locations. For reference, the measured return loss for the matched termination is also included (the unlabeled curve).

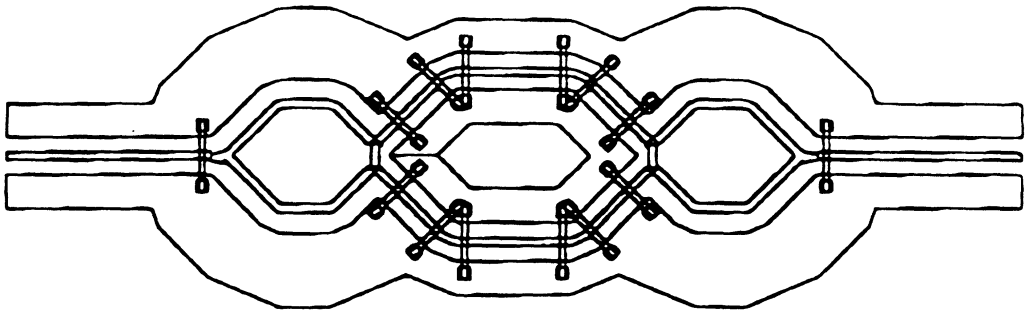

Figure 4. Illustration of a Wilkinson power divider using asymmetric coplanar strip (ACPS), with coplanar waveguide feedlines (shown in a back-to-back configuration).

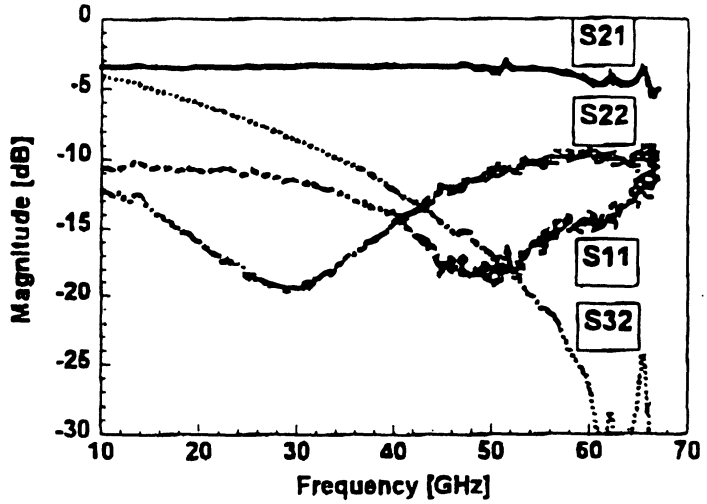

Figure 5. Measured S-parameters for a single ACPS Wilkinson power divider, using no air-bridg compensation (the third port is terminated in a matched load).

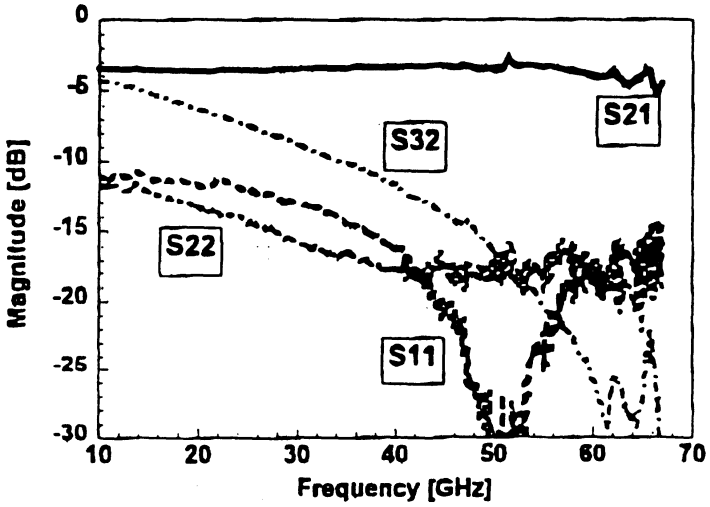

Figure 6. Measured S-parameters for a single ACPS Wilkinson power divider, using the step-compensation approach at each air-bridge (the third port is terminated in a matched load).

Silicon-Based Micromachined Packages for High Frequency Applications

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Abstract — **A novel approach is presented which is appropriate for low cost, high frequency electronic packages for discrete as well as integrated components. This approach is based on silicon (Si) micromachining and can effectively provide on-wafer and discrete packaging for high quality, high-precision miniature components. The fabrication techniques required in this approach are compatible with standard IC processing and for this reason provide very low fabrication cost. As an example, this paper presents the development of a Ka-Band package that can hermetically shield and electromagnetically isolate MMIC components such as a phase shifter. The performance of this package is compared to that of a ceramic one and demonstrates excellent electrical response in addition to high design versatility.**

I. Introduction

For many years electronic packaging for microwave and millimeter-wave components and systems was not considered as part of circuit design and development. Emphasis placed solely on electronic circuit design has led to the realization of inexpensive, light-weight, high performance circuits when operated in an open environment. A separate effort was later launched to produce an activity with emphasis on the design and fabrication of packages that could house electronic circuits and protect them from hostile environments and harsh operating conditions. Package development based on the consideration of thermal

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In the early eighties, Petersen extensively reported on the mechanical properties of Si and showed that the mechanical strength of this material was comparable to many metals [7]. Although Si is a brittle material, wafer chips on the order of 6 mm x 6 mm are quite rugged under normal handling conditions. Table 1 summarizes the basic material characteristics of Si and alumina. The excellent properties of Si and the numerous micromachining techniques available have allowed engineers to develop high performance miniature electromechanical devices [8], and membrane type transmission lines which can operate at frequencies as high as 1000 GHz [9]. GigaBit Logic developed a silicon-based package for GaAs circuits and compared the performance to a multi-layer ceramic one and found the silicon package characteristics to be better [10]. The thermal properties of Si are very good compared to those of ceramic materials and allow for excellent heat transfer between the semiconductor and package, thus, making Si an excellent candidate for high frequency MMICs.

In the following sections, the design, fabrication, and testing of a Si package that can provide on-wafer or discrete shielding to circuit components will be described. The performance of this package in terms of input match and loss will be evaluated and compared to a Ka-Band ceramic package designed to host a MMIC phase shifter.

II. Package Design

The Si-based chip carrier layout originated from a design fabricated by Hughes Aircraft Company for NASA Lewis Research Center [2] using high temperature cofired ceramic (HTCC) material with 92% alumina. In order to effectively compare performance, every possible effort was made to maintain the overall physical dimensions used in the ceramic package (Fig. 2) with the total size of the structure being 7.112 mm x 7.112 mm x 1.27 mm. Due to the difference in the electrical properties of alumina and Si, the geometry of the package was modified in order to keep the input and output reference impedance equal to 50 Ω and the operating bandwidth between 26 GHz to 40 GHz. Table 2 lists the redesign parameters for the Si chip carrier.

The Si-based package is comprised of four wafers: the carrier, the substrate, the seal frame, and the top cover. Each wafer carries one or two metallization layers as shown in Fig. 3. The carrier wafer has a metal

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variations have been developed and measured to determine the sensitivity of the electrical performance due to other layout asymmetries. In one of these designs, the I/O lines are symmetrically placed along the axis of the package to study the effects of feed-line symmetry while the vias have been left asymmetric as in the previous case. The final design has all I/O lines and shielding vias placed symmetrically from the center axis.

III. Fabrication and Assembly

A. Fabrication

A 500 μm, high resistivity, <100>, Si wafer with 7500Å of thermal SiO_2 was used to fabricate the package. The process flow consisted of wafer preparation, circuit metallization, and via formation and metallization. To provide the correct package thickness and the required stripline and microstrip substrate thicknesses for 50 Ω impedance realization, the wafer was thinned on one side from 500 to 350 μm using an HF nitric solution (isotropic etchant) with an etch rate of 11.5 μm/minute. Nitric acid is used to oxidize Si, while hydroflouric acid (HF) removes the oxide. Acetic acid helps polish the thinned surface while etching. Because the etch rate is reduced when the etchant becomes saturated, an additional measure was added to realize desired thickness repeatability. Before thinning, a narrow groove was diced 350 μm into the Si wafer from the unthinned side. When 150 μm of Si had been etched, the diced groove appeared and the sample was removed from the solution.

After thinning, the sample was cleaned with a sulfuric acid and hydrogen peroxide solution and the wafer and masking dielectric thicknesses were re-measured. The processing steps for the seal frame and substrate wafers required three masks each. Figure 6 shows the process steps for developing via holes in the substrate and seal frame wafers. In mask 1 narrow apertures were exposed by removing the dielectric using buffered hydroflouric acid (BHF). Mask 2 defined the metal overlay pads, the RF I/O lines, and the DC bias lines. The overlay pads (300 x 600 μm) covered the narrow apertures of the upper vias and helped in connecting the upper and lower ground planes for e-m shielding. Three microns of electroplated gold (Au) was used to metallize the lines and overlay pads. The backside of the wafer was masked with Cr/Au (500/2500Å) using a lift-off process and the wide aperture was etched in ethylyne diamine, pyrazine, cath-

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aligned the transmission line impedance mismatch and discontinuities will result in high reflections and degrade package performance. Metallized alignment crosses were fabricated on the substrate wafer and alignment windows were etched in the seal frame wafer. Visual alignment under a 5x microscope was used to bond the two wafers (Fig. 10). A more accurate method involving microsphere beads should be used where vias for the spheres are etched on the top of the substrate wafer and bottom of the seal frame wafer. One half of the bead rests in the substrate and the other half rests in the seal frame (Fig. 11) Enough beads can be placed within the layout to ensure accurate alignment [11]. Figure 12 shows a photograph of the assembled package without the top cover added.

IV. Evaluation and Results

The developed micromachined packages were evaluated for only electrical performance. Herein the results are discussed and compared to those of the ceramic package. Measurements were obtained with a microstrip through line representing the phase shifter integrated circuit just as in the case of the alumina package. On-wafer high frequency measurements were conducted using an HP 8510C network analyzer with an Alessi Probe Station and 150 μm pitch ground-signal-ground (GSG) GGB Picoprobes. The network analyzer was calibrated with Through-Reflect-Line (TRL) standards which shifted the reference plane to the same location where the alumina package was measured, thereby eliminating the effect of the GCPW-to- microstrip transition. Although not reported on in this paper, the dielectric properties of the package material can be extracted from the TRL measurements.

Figures 13 shows comparisons between the silicon and alumina packages. The data shown are for the original package design where the through line is centered and the two vias are shifted, with the top cover sealed on the package. The total loss of the silicon package was better than that of the alumina package by 0.04 dB to 0.3 dB. Table 3 lists the steps used in thick- and thin-film package processing. High temperature firing alters the surface of the conducting materials used in ceramic packages and increases the interconnect losses which has an impact on mm-wave circuit performance. Figure 14 shows the attenuation of a 9 mm line with three and eight microns of electroplated Au. This line length is typical of the length of a package and indicates conductor loss for Si-based packages can be further reduced by increasing circuit

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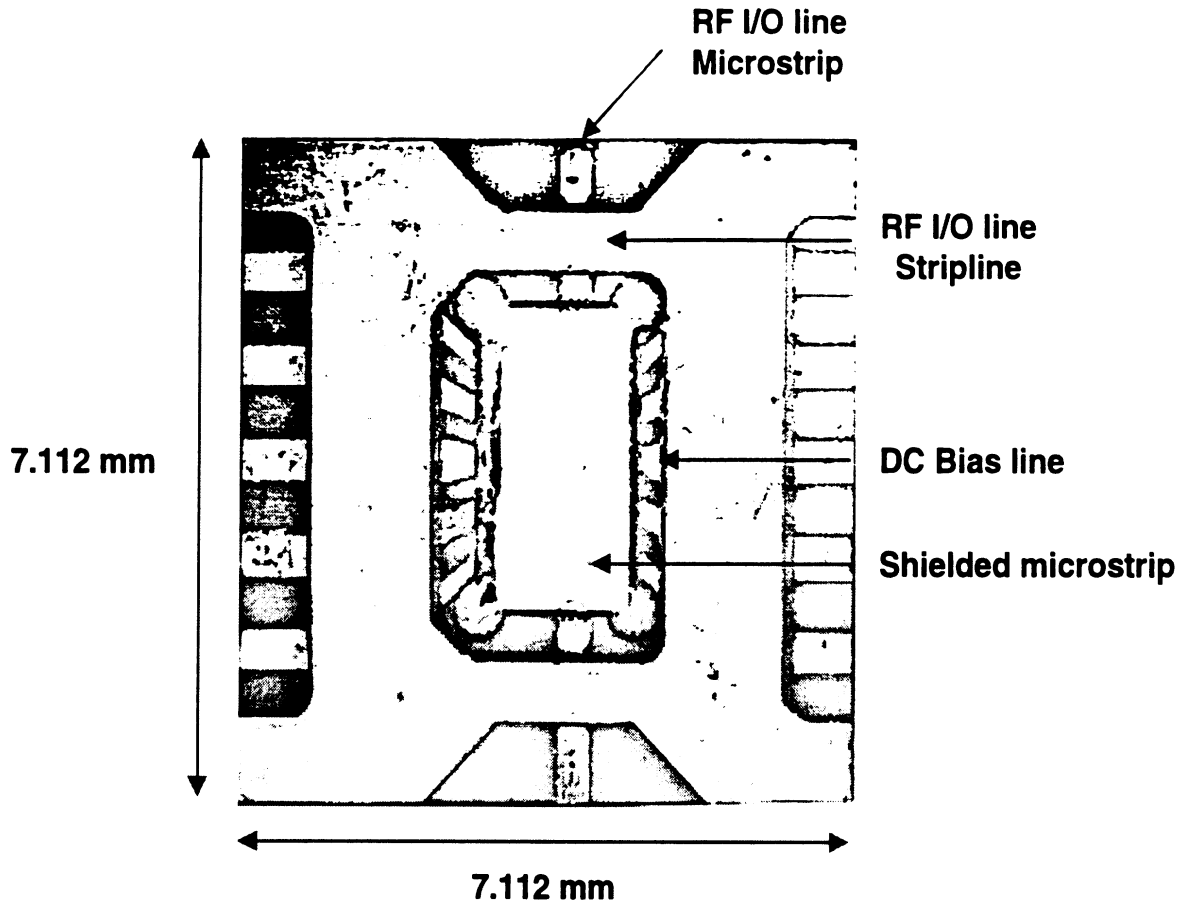

Figure 1. Actual photograph of K/Ka-Band ceramic package for a phase shifter chip.

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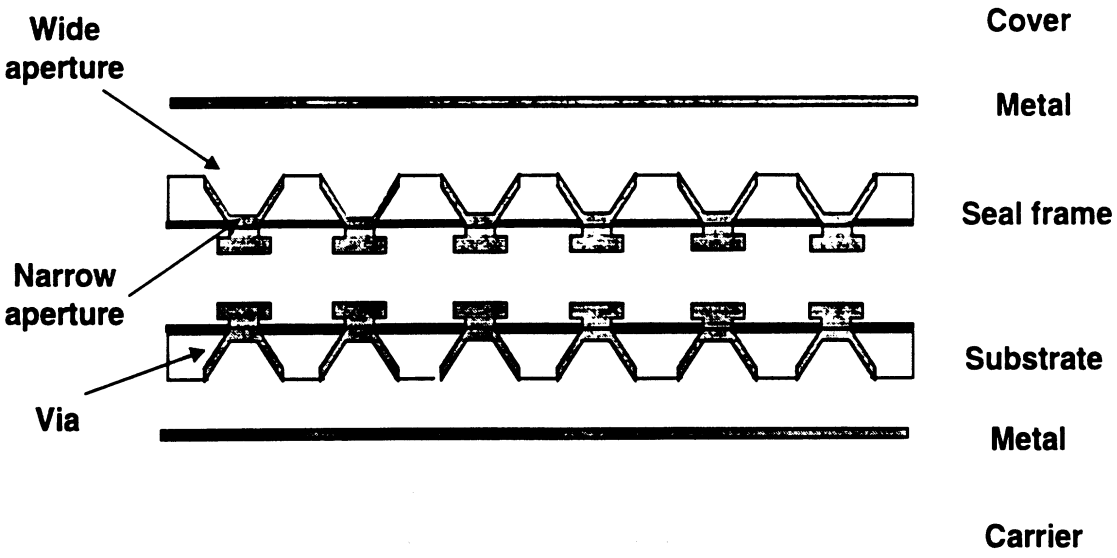

Figure 3. Cross-section of package.

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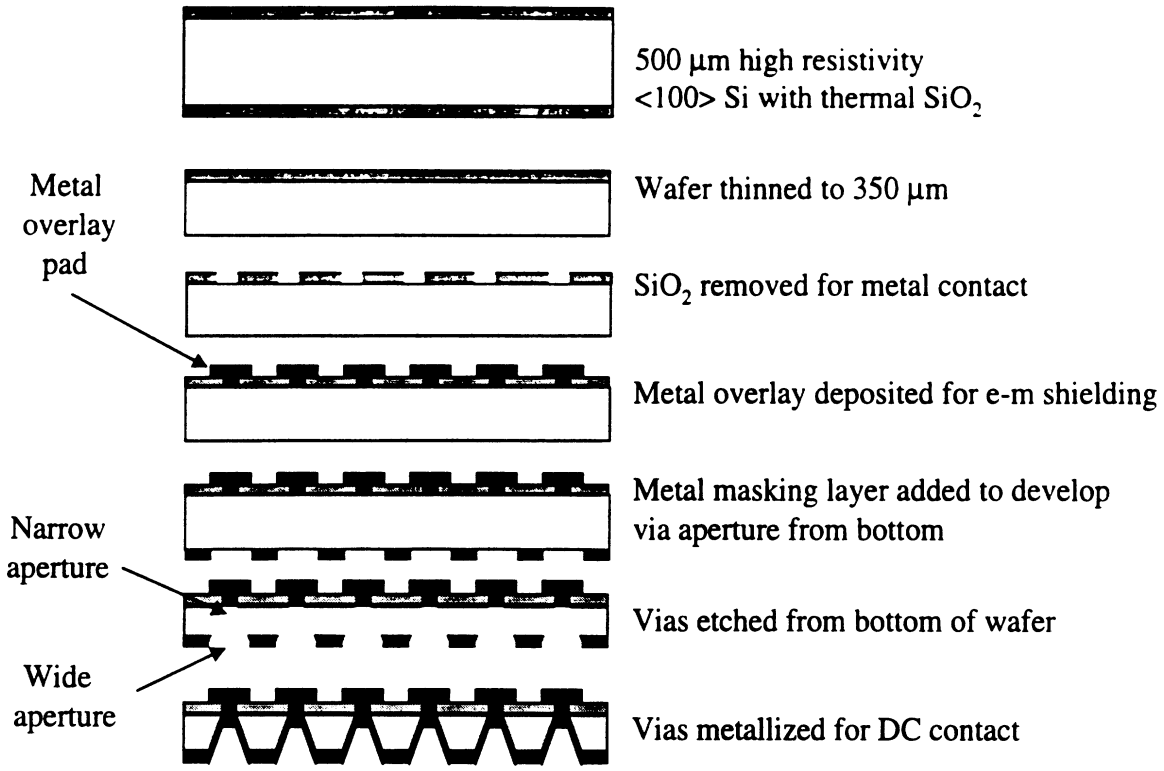

Figure 5. Via hole processing steps.

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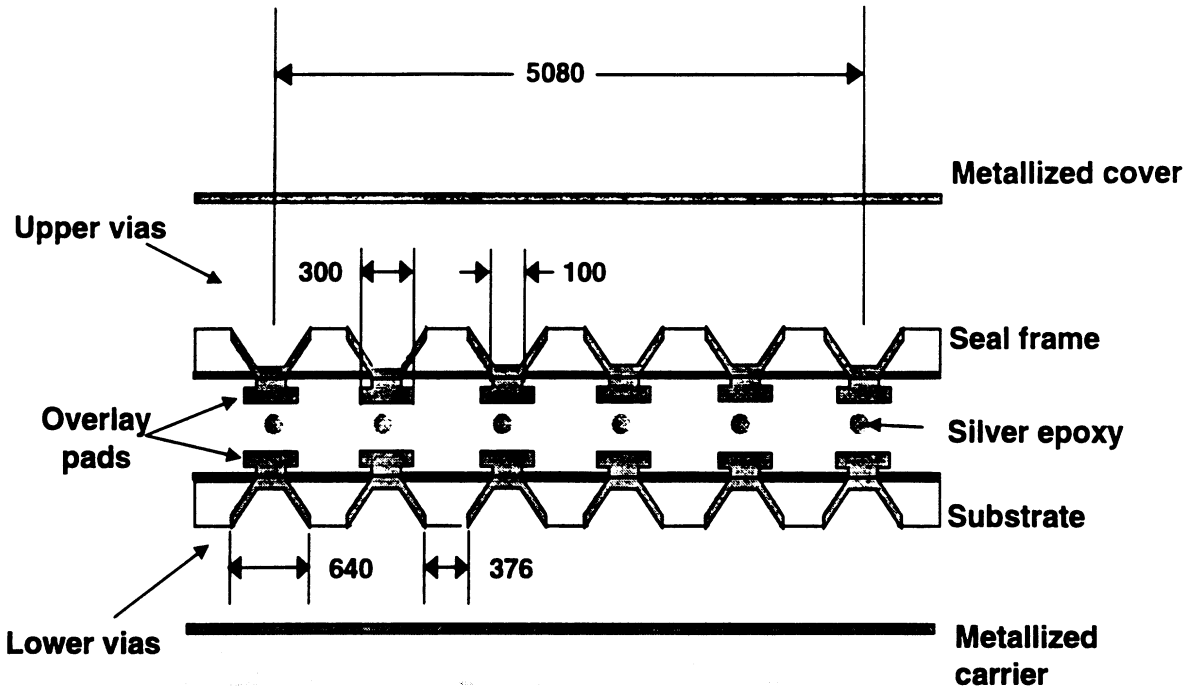

Figure 7. Via hole assembly. (Units are in microns.)

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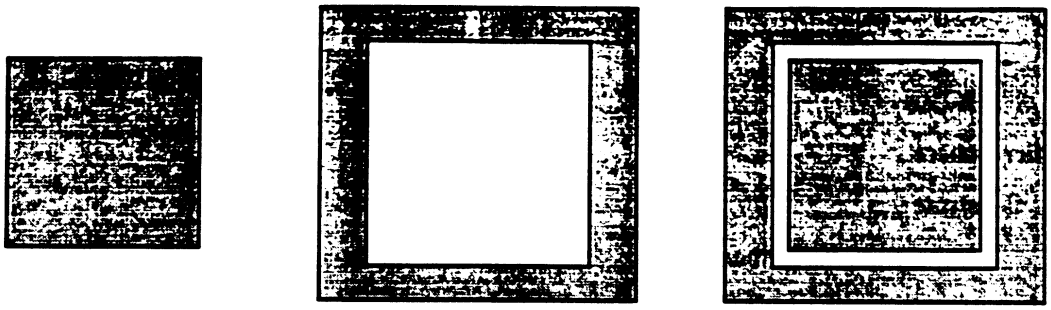

Figure 9. Techniques for wafer-to-wafer alignment. Substrate mark deposited during metallization. Seal frame mark etched. Both wafers are aligned and the markers look like the above after alignment.

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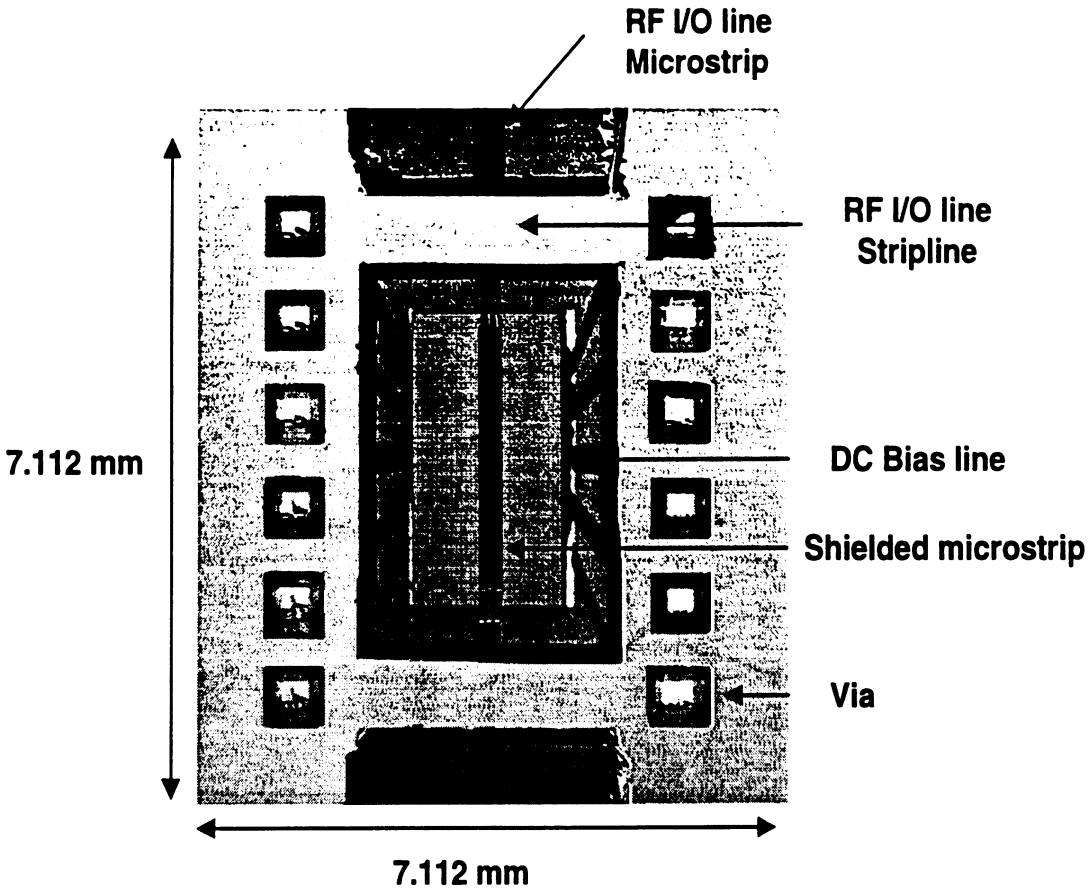

Figure 11. Photograph of actual Si-based package.

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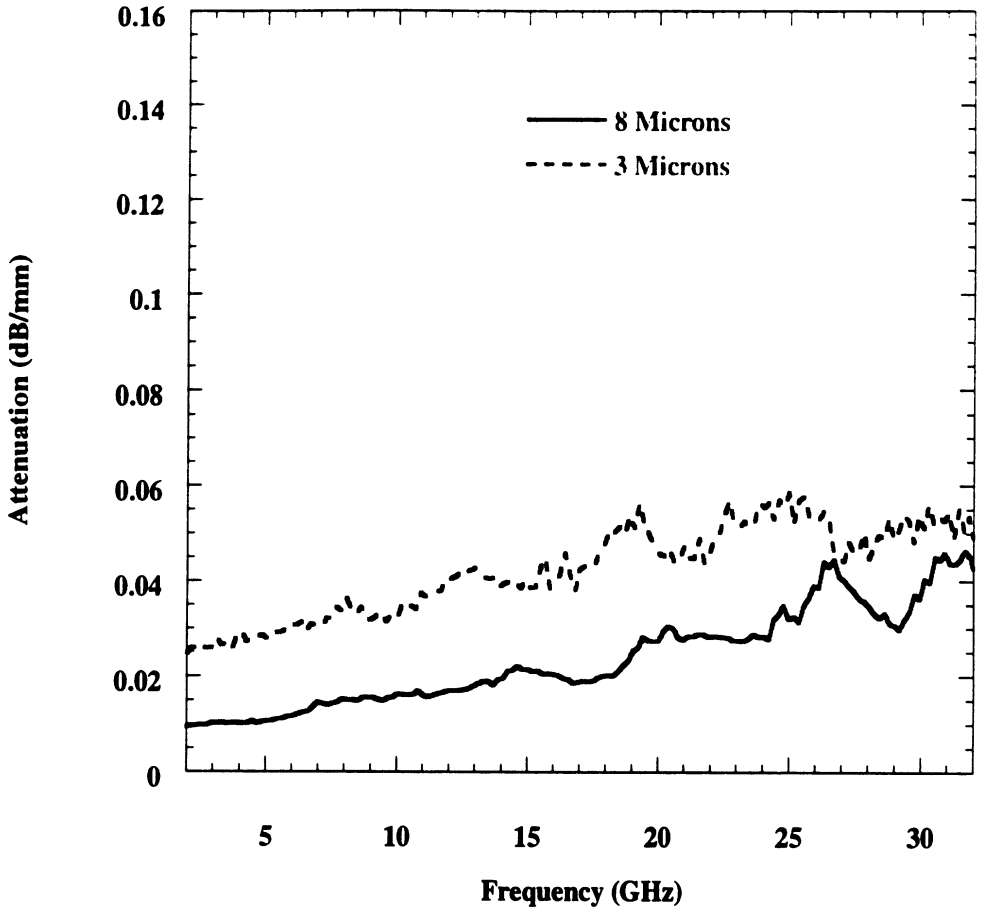

Attenuation of 9 mm line (typical package length) with three and eight microns electroplated gold.

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BIOGRAPHIES

Rashaunda M. Henderson received the B.S.E.E. degree from Tuskegee University, Tuskegee, AL in 1992 and the M.S.E. in electrical engineering from The University of Michigan, Ann Arbor, MI in 1994. She is completing the Ph.D. requirements in electrical engineering at The University of Michigan. Her research involves developing and characterizing Si-based packages fabricated with standard IC and micromachining techniques for high frequency applications. She has affiliations in IEEE, MTT-S, NSBE, Eta Kappa Nu and IMAPS.

Linda P. B. Katehi received the B.S.E.E. degree from the National Technical University of Athens, Greece, in 1977 and the M.S.E.E. and Ph.D. degrees from the University of California, Los Angeles, in 1981 and 1984 respectively. In September 1984 she joined the faculty of the EECS Department of the University of Michigan, Ann Arbor. Since then, she has been involved in the development, modeling, fabrication and experimental characterization of millimeter and near-millimeter wave monolithic circuits and antennas.

She has been awarded with the IEEE AP-S W. P. King Award in 1984, the IEEE AP-S S. A. Schelkunoff Award in 1985, the NSF Presidential Young Investigator Award and an URSI Young Scientist Fellowship in 1987 and the Humboldt Research Award in 1994. She is an Associate Editor of the IEEE Antennas and Propagation Society, and Radio Science. She is a Fellow of IEEE, member of the IEEE AP-S, MTT-S, Sigma XI, URSI Commission D and an elected member of the IEEE Antennas and Propagation Society Administrative Committee.

SILICON-BASED MICROMACHINED PACKAGES FOR DISCRETE COMPONENTS

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ABSTRACT

A novel approach has been taken to develop low cost, high frequency (Ka-band), electronic packages. An existing thick film package for a phase shifter chip has been redesigned using silicon as the base material. This paper reports on the fabrication techniques and the measurement improvement found by coupling silicon micromachining techniques with standard IC processing.

1.0 INTRODUCTION

For several years, electronic packaging for microwave components and systems has taken the back seat to high frequency circuit design and development. While state of the art high frequency components and devices have been realized, the package has been found to cause system degradation with increased frequency. The electronic package provides physical and thermal protection as well as interconnection to subassemblies. In recent years, packaging has received increasing attention and efforts are underway to produce low cost, high quality, high frequency structures.

As a result, MCMs, hybrid and monolithic packages have been developed using cofired ceramic, printed wiring board and thick and thin film technologies. In addition to package design there has been a serious effort in developing commercial modeling tools that can predict the performance of packages in the circuit environment [1]. At this time, high quality packages are being made which tend to be quite expensive and excessive in volume and weight, characteristics that prevent them from wide use [2].

In view of the above, the capability to create a low cost, low weight and volume package which operates at high frequency, demonstrates high bandwidth characteristics, and offers physical protection while not degrading performance, would provide major advances in packaging. At The University of Michigan we have been able to successfully incorporate IC processing techniques with silicon micromachining to fabricate silicon-based packages for discrete and monolithically integrated components. Given the knowledge base developed in silicon micromachining, the goal is to take advantage of the electrical and mechanical properties of single crystal silicon so as to create low cost, high precision, miniature microwave and millimeter wave packaged components.

2.0 BACKGROUND/DESIGN/FABRICATION

Recent work, [3], has led to the development of self-packaged components that have excellent isolation from neighboring elements in addition to individual component protection. Self-packaged silicon components are an alternative to conventional structures, appropriate for low cost, low volume, miniaturized high density subsystems.

Silicon is the best substrate to use when it comes to high frequency packaging components. The mechanical properties as presented by Petersen [4] are excellent and comparable to certain metals. Using micromachining and IC processing techniques, via hole diameter and linewidth dimensions are the smallest possible, which is very much desired for the reduction of high frequency parasitics. The thermal conductivity of Ga As, In P, and Ge (80,65,68), (W/(m*K)) creates problems with heat dissipation. As compared to 92% alumina (18), Si (135) is an excellent heat sink, which makes it a very good packaging material [5]. By combining the electrical and mechanical advantages of silicon, low cost batch fabricated packaged components can be incorporated on-wafer to increase circuit density while remaining low in volume.

A package fabricated by Hughes Aircraft for NASA Lewis served as the model for this design. The high temperature cofired ceramic (HTCC) process is used to develop an alumina (92% pure, ε_r=9.5) hermetic package for a phase shifter chip (Figure 1). This package was reproduced using high resistivity silicon (ε_r=11.7). Figure 2

shows the package layout (5 layers) and the through line used for characterization. A metal base is used for support, while an upper metallization layer and top lid are used to seal the package. A silicon substrate layer is used for RF input/output and DC bias lines. A hole is etched through the wafer for chip placement and a set of six micromachined vias are placed along the left and right of the IC for electromagnetic shielding. These vias are used in the seal frame layer as well. A center hole in the seal frame is etched for IC placement and two outer holes are used for wafer probing. The package dimensions are 7.112 x 7.112 x 1.27 mm. The alumina and silicon package differ in bias line width (smaller for silicon) and three ultrasonic wire bonds are used to connect the silicon package and IC as opposed to four in the alumina package. The vias and input/output microstrip feedline in the alumina package are displaced from the center for application reasons whereas the square vias and feedline are symmetric in the silicon design.

Conventional thin film processing technology is utilized to fabricate the package. A 50 ohm through line is used to characterize the effect of the package which incorporates sections of microstrip, stripline and shielded microstrip. Silver epoxy is used to attach the lid and provide the connection between the upper and lower metallization surfaces (electromagnetic shielding). Given the measurement setup, a 50 ohm grounded coplanar waveguide (GCPW) to microstrip transition is used (Figure 3). Via holes are etched to provide connection between the upper and lower metal surfaces. The via holes required in this package are developed by anisotropic etching using ethylene diamine pyrocatechol (EDP). Three microns of electroplated Au are used as the metallization for the package and IC (through line) (Figure 4).

3.0 Results

The silicon package described earlier is characterized experimentally using an HP8510C Network Analyzer, and an Alessi probe station with 150 μm pitch GGB Picoprobes. A Thru-Reflect-Line (TRL) calibration was performed to deembed effects up to the open microstrip feedline.

Figures 5 and 6 show the insertion loss and return loss, respectively, for the alumina and silicon-based package. Over the whole frequency range, the insertion loss of the silicon package is better than that of the alumina package by 0.5 dB. The return loss for the silicon package is mostly attributed to the ohmic loss of the through line for which measured values are shown in Figure 7. The observed irregularity in the alumina package suggests parasitic effects not related to impedance mismatch. The estimated cost for the Si package (batch processing) is less than $1 and reflects a substantial reduction compared to conventional cofired ceramic packages.

4.0 Conclusion

We have shown that it is possible to develop silicon based packages for discrete components using thin film processing and micromachining techniques. This effort is less expensive and outperforms its HTCC counterpart. This packaging approach can be extended to provide advanced packaging techniques where discrete as well as integrated components can be hosted by the same silicon wafer.

5.0 Acknowledgements

This work has been supported by contracts from the Army Research Office and the Office of Naval Research.

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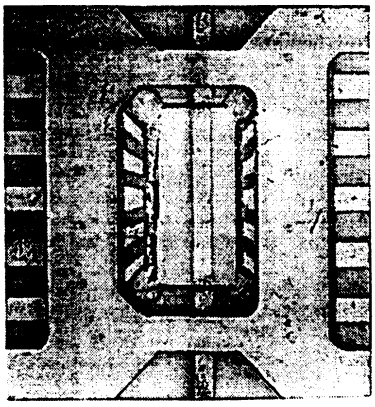

Figure 1 HTCC hermetic package designed by NASA Lewis.

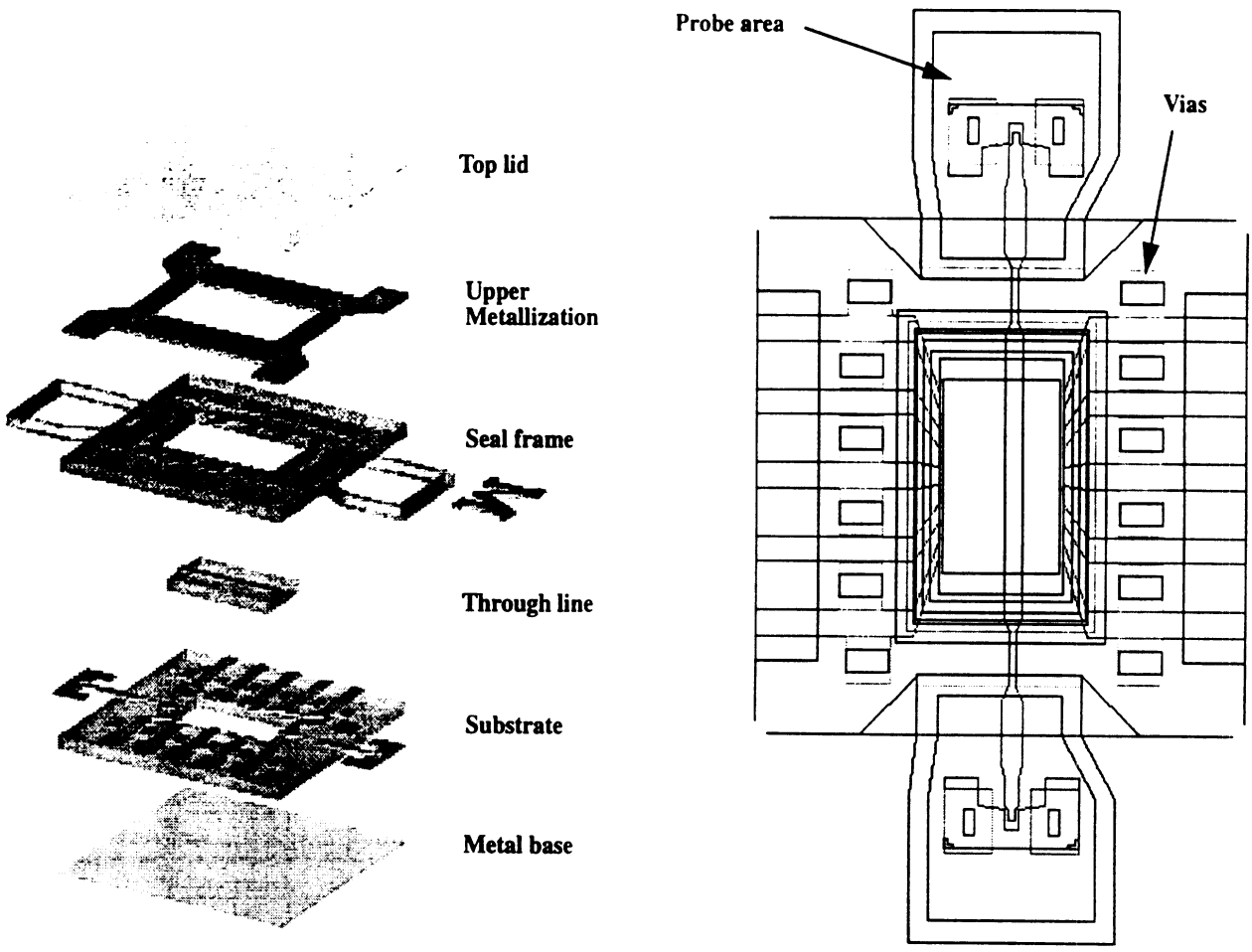

Figure 2 3-D view of package layers and actual CAD drawing with all layers superimposed.

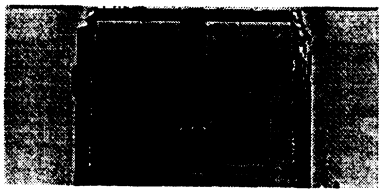

Figure 3 Photograph of probe window with GCPW to microstrip transition for on-wafer probing.

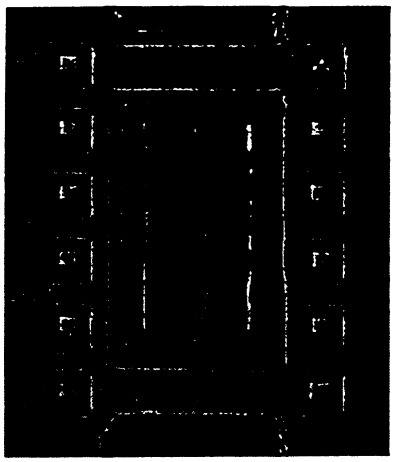

Figure 4 Micromachined silicon-based package.

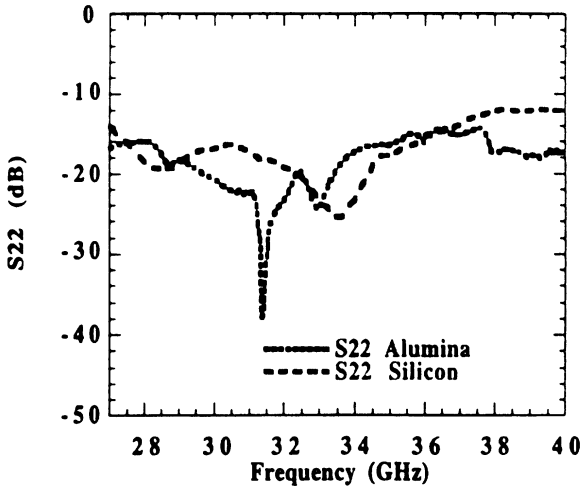

Figure 6 Return Loss

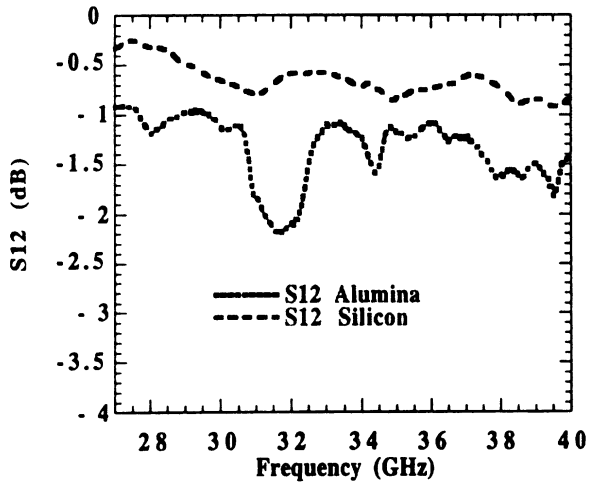

Figure 5 Insertion Loss

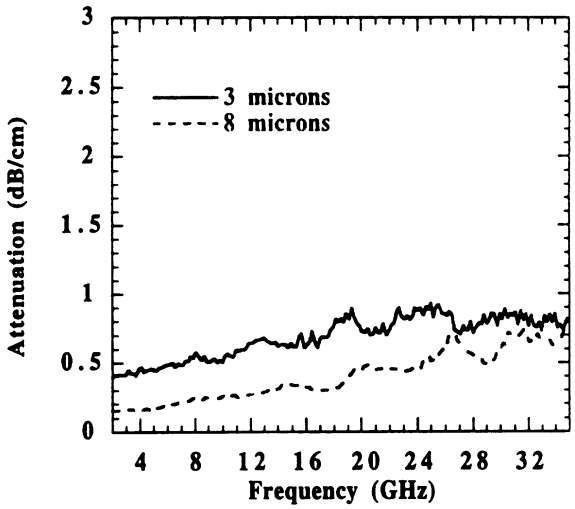

Figure 7 Attenuation of 9 mm through line in package.

High Frequency Circuit Components on Micromachined Variable Thickness Substrates

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Index — micromachining, planar circuits, planar antennas, packaging

Abstract — This work presents the use of Si micromachining techniques to enhance high frequency planar circuit design flexibility by offering a method for varying the substrate thickness in selective locations on the wafer.

1.0 INTRODUCTION

Micromachining is being used for a number of high frequency applications to meet design requirements for compact circuits, high performance interconnect lines, monolithic packaging as well as novel array configurations feeding networks [1]. During the development of such technologies for use in low frequency applications, materials parameters such as size and thickness have been standardized in order to meet demands for high volume low cost circuits. A beneficial result is the use of established infrastructures and less expensive materials that can be integrated into circuit designs for high frequency applications. For example, in many complex MMIC designs requiring planar circuits and antennas, a critical design parameter for both components is the substrate thickness which depends on the transmission line topology selected. In particular, as active and passive elements are integrated into a single chip along with radiating elements, the selection of an optimal substrate thickness that offers overall high performance for each component function becomes impossible. Therefore, novel fabrication approaches that address this issue are necessary in order to satisfy design requirements for complex high performance circuits.

Presented herein is a micromachining methodology that extends flexibility to the design of circuits or radiating elements by allowing for local reduction of the substrate thickness in order to achieve excellent component performance. This concept is illustrated through the use of a simple transmission line that is implemented in a full thickness wafer environment with thickness reduction along the feedline.

3.0 MEASURED RESULTS

Measured data is obtained from an HP 8510C Network Analyzer and Alessi probe station with Picoprobes A coplanar waveguide to microstrip transition is used with conductor and slot widths of 180 and 210 microns The outer ground planes on the top side of the wafer are 380 microns away from the microstrip line to ensure microstrip mode of propagation. Figure 3 shows the calculated values of the effective dielectric constant for a thru line in an open and packaged configurations based on measured data. The slope of effective dielectric constant is reduced as the package is incorporated. When an upper shield is added to the circuit to completely shield the line, the response shows a near flat value up to 22 GHz, indicating an effective dielectric constant that is less sensitive to frequency.

4.0 CONCLUSION

A micromachined variable thickness through line interconnect has been developed. In this approach, micromachining has been used to custom design the substrate thicknesses in order to improve the performance of heterogeneous circuit components on the same wafer.

5.0 ACKNOWLEDGEMENTS

This work was supported by the Army Research Office and the Office of Naval Research.

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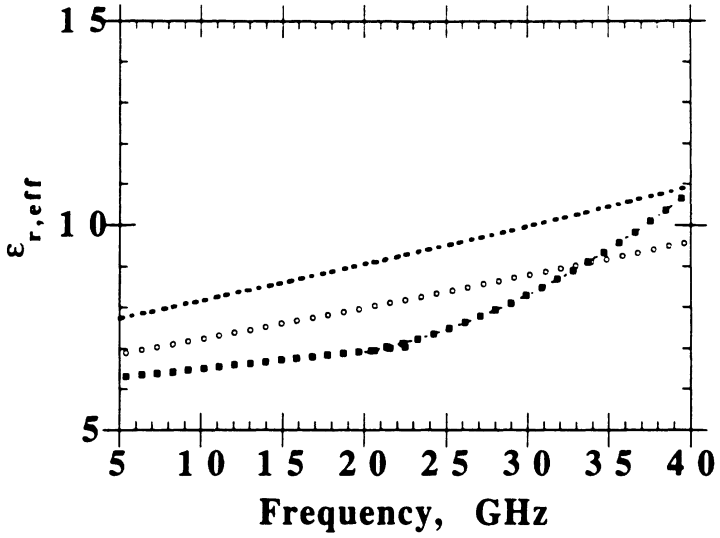

Figure 3 Plot of calculated effective dielectric constant, open (------), lower shield ( ), and completely shielded ( ).

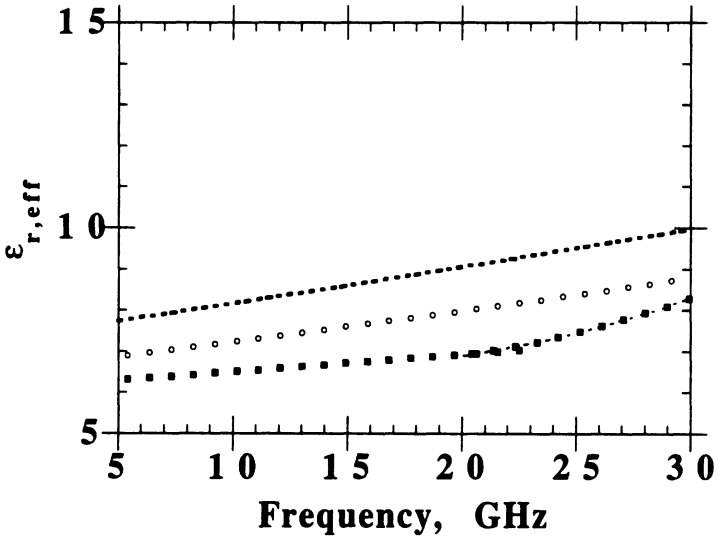

Figure 4 Plot of calculated effective dielectric constant, open (------), lower shield ( ), and completely shielded ( ).

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13. ABSTRACT (Maximum 200 words)

The project concentrates on the development of high-efficiency Si micromachined components. Specifically, it addresses the development of High-Q Filters using Si micromachined cavities. During the reporting period, our group has investigated the development of important issues related to the development of these filters: (1) Losses in Si wafers for a variety of resistivities (Part A); (2) Micromachined high-Q filters (Part B); (3) On-wafer packaging of circuit and filter components for high-efficiency and low loss (Part C). The study performed in each of these areas is described in detail. Furthermore, at the end of each section, copies of the submitted/accepted papers are included for further information.

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