

## AN INEXPENSIVE, HIGH PERFORMANCE PULSE-HEIGHT READOUT SYSTEM FOR PROPORTIONAL CHAMBERS \*

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We describe a simple system to read out pulse-height information from a large number of proportional chambers. Its main features are simplicity, low noise, and wide dynamic range. A complete system with 6000 channels was built for less than \$7 per wire, including fabrication and cabling. Typical readout time is  $< 6$  ms. The readout is designed to be triggered externally.

### 1. Introduction

In high energy physics experiments it is often desirable to read out pulse height information from a large number of proportional chamber wires. Typical examples of such applications would be hadron calorimeters, electromagnetic shower detectors, and neutrino detectors. The electronics must handle a large range of pulse heights; it must also be easy to set up and use. In large experiments with many wires to be read out, cost and reliability are major factors. We describe a readout system built for a neutrino experiment at Fermilab which digitizes pulse height information from 6000 wires. The data from groups of 200 wires are multiplexed sequentially into a 12-bit analog-to-digital converter (ADC), stored, and eventually read out to a computer through a CAMAC data bus. The total cost of building the system was less than \$7 per wire, including mechanical assembly, power supplies, and all cabling.

The dynamic range of the readout electronics is  $> 2000:1$  (saturation:noise). If the chamber high voltage is set to give a mean pulse height in ADC channel 40 for single minimum ionizing particles, over 100 particles per cell can be accommodated. Noise is less than 1 channel. The typical readout time is  $< 6$  ms.

It should be noted that in our experiment scintillation counters were used to provide an event trigger. The proportional wire chamber (PWC) electronics is *not* designed to provide information for triggering.

### 2. General description of detector

The proportional chambers we use are similar to those used in several other experiments [1,2]. Each cell consists of a hollow aluminum extrusion with a cross section approximately 24 mm square. The aluminum acts as the cathode. The anode is a 51  $\mu\text{m}$  diameter gold-plated tungsten wire running down the center of the tube. In our case the extrusions are either 3.6 m long (horizontal wires) or 1.5 m long (vertical wires). The chambers are organized into 30 double planes, each consisting of one plane with 64 horizontal wires and a plane with 136 vertical wires. Between each double plane is a calorimeter module containing lead plates totalling 75 mm in thickness, with liquid scintillator between the plates. Each of these modules is instrumented with 10 phototubes, the pulse heights from which are used to obtain the total energy deposited by an interacting neutrino in the module. The normal trigger requirement is a minimum energy deposition in the calorimeter modules with no signal from upstream veto counters. Calibration runs can also be made with a trigger which selects muons traversing the apparatus. When a trigger occurs, the pulses from the PWCs are stored on storage capacitors as described below, and after a short delay the readout sequence is initiated.

For safety reasons the PWCs were filled with a gas mixture of 20%  $\text{CO}_2$  in argon, though tests indicated better performance with pure ethane. All 6000 wires are run at the same high voltage, typically +2040 V. This gives a gas gain of approx.  $5 \times 10^3$ . A small PWC on which a radioactive source is mounted is used in a feedback loop to control the high voltage. The small PWC is in the same gas system as the rest of the chambers. The feedback system, which is similar to that

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in ref. 1, keeps the gas gain of the PWCs stable to better than 8% despite changes in atmospheric pressure, temperature and gas composition. The gas gain on each wire can be checked by looking at the pulse height with muons traversing the detector.

### 3. Overview of readout system

The readout system is shown schematically in fig. 1. The signal from the wire is capacitively coupled to the input of an operational amplifier integrator (LF357). Test pulses can also be injected into the amplifier input. The 1.8 pF capacitor in the integrator was chosen to get the highest possible voltage output for a given charge, consistent with a requirement of 5–10% uniformity in amplifier gain from channel to channel. The 300 k $\Omega$  resistor in parallel with the integrating capacitor allows charge to leak off with a time constant  $\approx$  550 ns. The analog switch between the output of the amplifier and the storage capacitor C is normally closed and the voltage across the capacitor is essentially equal to the output of the amplifier.

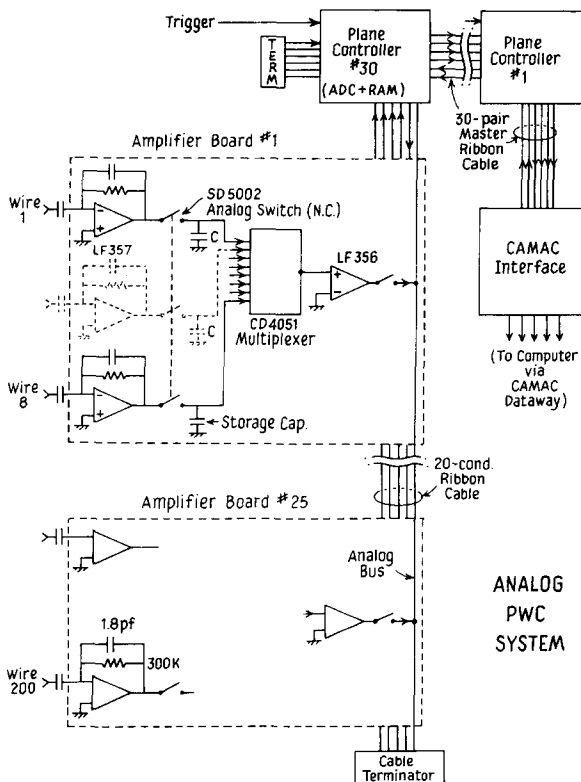


Fig. 1. Block diagram of the complete readout system. Each amplifier board contains electronics for 8 wires. The plane controllers control the readout, and if the pulse height is above the threshold they digitize and store the data.

Voltage pulses on the storage capacitor for test pulses of several amplitudes are shown in fig. 2. The pulses rise to a very broad maximum at about 700 ns. The position of the maximum is almost independent of the amplitude of the pulse (fig. 2). To store a pulse the analog switch is opened near the peak in  $V_C$ , i.e. about 700 ns after the passage of the particle. This gives the trigger electronics almost 700 ns to make a decision whether to hold an event and open the analog switch. No special storage element is needed or used in the amplifiers. The maximum in  $V_C$  is broad enough that timing jitter due to the varying distance between a particle's trajectory and the wire does not cause a very significant error.

In addition the timing of the peak was found to be quite consistent from one amplifier channel to another. (A few LF357's were found to vary significantly in this respect, and  $<$  3% of them were rejected.) The position and amplitude of the peak are, however, sensitive to the capacitance of the wire. In our case, since we had long wires and short wires, a small capacitance (22 pF) to ground was placed ahead of the input of the amplifier for the short wires so that the same amplifier cards could be used for both.

The SD5002 analog switches are a critical part of the readout. They can switch voltages up to approx. 15 V in times  $\sim$  10 ns; their on-resistance is  $\approx$  30  $\Omega$ , and their off-resistance is  $\sim$  10<sup>10</sup>  $\Omega$ . The circuit is easily capable of storing the information for times  $\geq$  1 s, but in our application the readout is completed within approx. 6 ms. Following the storage capacitor is a CD4051 8-channel analog multiplexer. A single multiplexer handles the 8 channels on one readout card. The output of the multiplexer goes through a buffer amplifier and is then gated onto a common analog data bus at the appropriate time in the readout sequence.

In our application it was convenient to group all 200 channels (25 boards on one double plane) into one

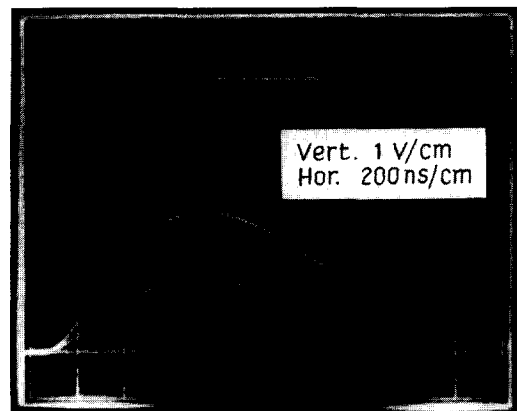


Fig. 2. Voltage on the storage capacitor for test levels of 0, 1.0, 2.0, and 4.0 V. For the 4.0 V level only the analog switch is opened to store the pulse.

subsystem which was handled by its own "plane controller". The plane controller initiates and clocks the readout sequence and takes the data off the analog bus. If the pulse height is above a settable minimum value the pulse is digitized by a 12-bit ADC and the output of the ADC and wire address are stored in RAM. The plane controller communicates with the amplifier boards by a single 20-conductor flat ribbon cable, which also supplies power to the boards.

The 30 double planes are serviced by 30 plane controllers which in turn are read out sequentially by a CAMAC controller under control of the PDP-11 data acquisition computer. The CAMAC controller communicates with the plane controllers through a single, 60-conductor, twisted-pair ribbon cable.

#### 4. The amplifier boards

Fig. 3 is a schematic of an amplifier board; two of the eight LF357 amplifiers are shown. Pins on these boards plug into mating sockets on a "high voltage" board which is permanently mounted on each 8-wire

proportional chamber extrusion. The high voltage boards contain resistors, hv decoupling capacitors, and protective diodes. A small resistance in series with the wire protects it against breakage if a discharge to the wire occurs. Fig. 4 shows a photograph of an amplifier board. Each board contains eight LF357N amplifiers, two SD5002 quad analog switches to switch the storage capacitors, and the CD4051 multiplexer. In addition there is a 74C10 gate, a 74C161 binary counter and a third SD5002 analog switch which serves various gating functions described below.

The wire amplifier is based on a National LF357 high-speed, FET-input operational amplifier. The amplifier output current is boosted with a 2N3904 emitter-follower to allow the use of a large (2200 pF) hold capacitor, which reduces the effect of capacitive feedthrough of the gate through the analog switch. The amplifier has 100% dc feedback, so that the emitter of the 2N3904 is normally very close to zero volts; the output of the amplifier is ac coupled to the hold capacitor to remove any residual dc offset.

In this circuit the amplifier is not an ideal operational amplifier because the LF357 is "slow" compared

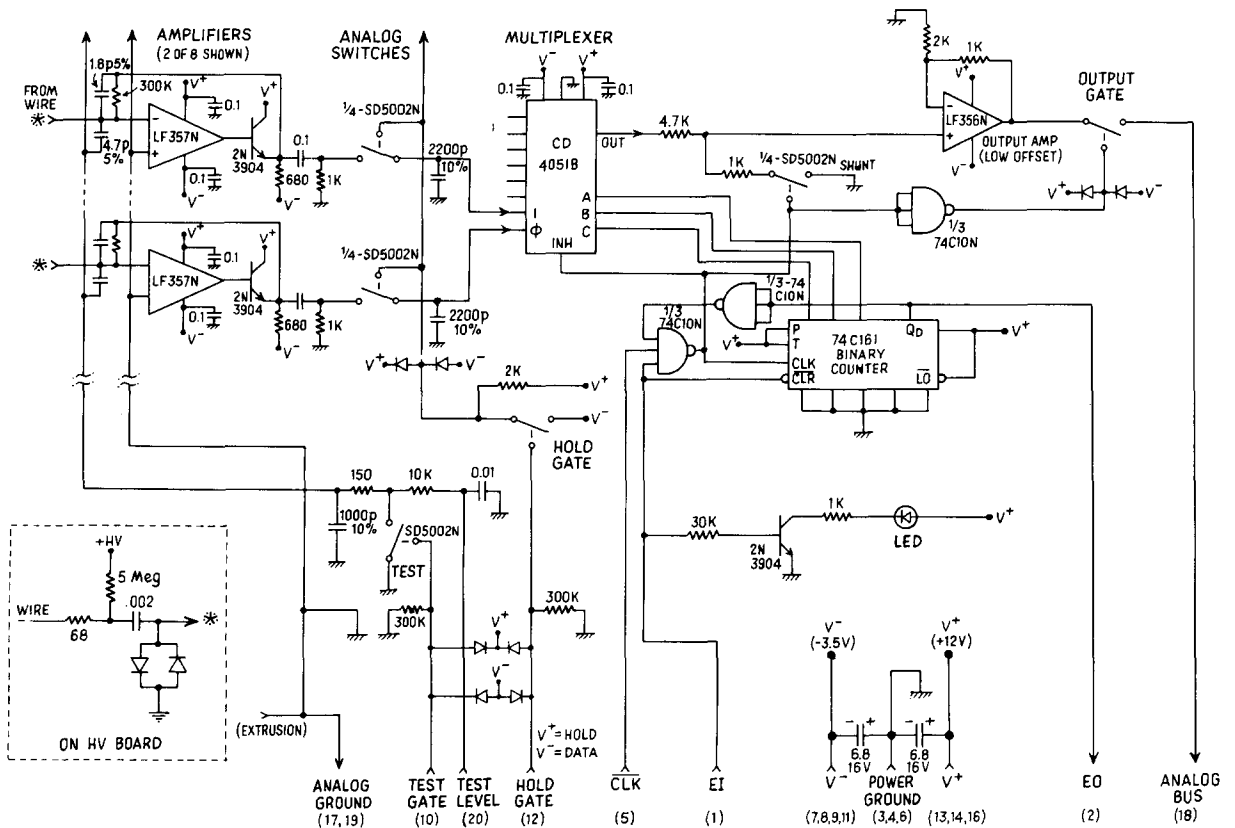


Fig. 3. Schematic of the complete amplifier board which services 8 wires. Only 2 of the 8 LF357 amplifiers are shown. The inset on the lower left shows the components mounted on the high-voltage board. Connections to the ribbon cable are at the bottom.

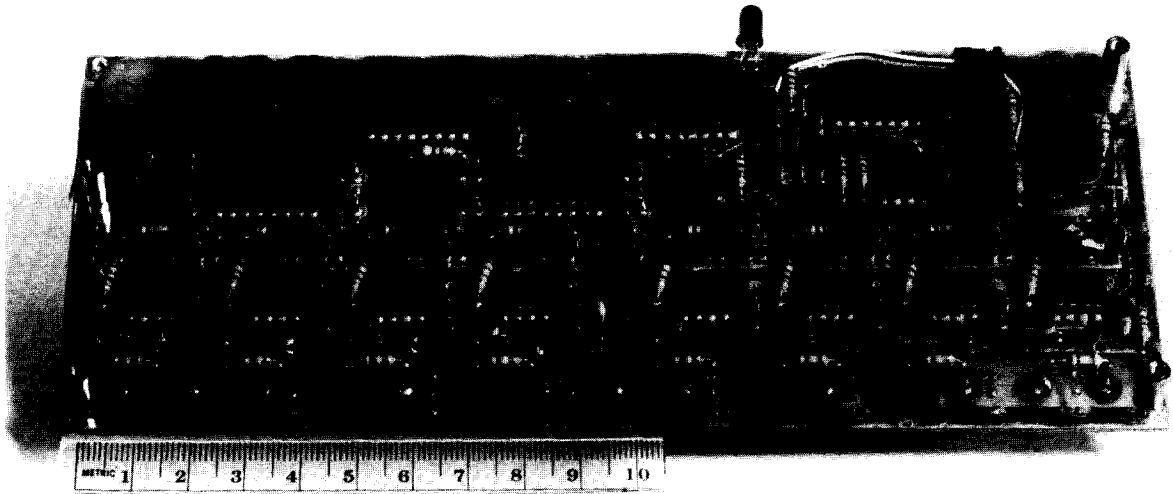


Fig. 4. Photograph of an amplifier board with complete electronics for 8 wires. The header for the 20-conductor ribbon cable is on the upper right. Connections to the chambers are through pins on the lower side of the board.

to the input signal. The input is thus not a true virtual ground. The amplifier input rises to approx. 0.3 V for a 6 V signal at the emitter output. The rise time and pulse height are noticeably affected by the wire capacitance. As noted earlier, some care was taken to make this capacitance the same for all wires.

The analog switch for each channel is one quarter of an SD5002 (Signetics or Semi Processes) D-MOS FET quad switch and is normally closed. To hold an event the switches are opened via the HOLD bus. The off-resistance of these switches is  $\sim 10^{10} \Omega$  so with a 2200 pF hold capacitor the circuit is capable of holding the signals for times  $\gtrsim 1$  s. The capacitive coupling of the gate signal into the hold capacitor causes an effective offset of approx.  $-40$  mV in  $V_C$ . Although this is approx. the same for all channels, it is the major source of the channel-to-channel variations in the pedestals.

Once stored the voltages on the hold capacitors can be read out onto the analog bus through the CD4051 8-channel multiplexer which is controlled by the 74C161 synchronous binary counter and the clock (CLK) signal. The readout is initiated upon receipt of an enable in (EI) signal on the ribbon cable. The binary counter then sequentially reads through the eight channels of the multiplexer synchronous with the CLK signal. The output of the multiplexer is put onto the analog bus through the LF356 buffer. After the 8 channels are strobed, the carry pulse from the binary counter forms an enable out (EO) pulse which is carried to the EI of the next board. (This is accomplished by twisting one pair of adjacent conductors in the flat ribbon cable between successive boards and cutting one.) The readout sequence thus steps through all 25 cards in one

double plane. The cable terminator routes the last EO back through the ribbon cable to the plane controller to signal that all channels have been read. An LED on each board shows when it is being read; this is useful if the readout ever hangs up, and as a visual indication that the readout is taking place.

On each board there is a third SD5002 quad analog switch which serves four functions: One channel is used to form the gate for the 8 analog switches upon receipt of a hold gate. One is used for the test pulses. It discharges a 4.7 pF capacitor into the input of each amplifier; the amount of charge is proportional to the test level, which also comes in on the ribbon cable. Another channel of the switch is used to gate the output of the LF356 buffer onto the analog bus. The fourth is used to discharge the stray capacitance at the input to the buffer amplifier between successive readout channels. This prevents a large pulse on one channel from being "remembered" when the next channel is strobed.

The clock cycle time is  $\approx 2 \mu\text{s}$  if the signal on the analog bus is below the selected threshold; this is determined by the time it takes for the analog bus to settle. For signals above the threshold the cycle time is approx.  $20 \mu\text{s}$  as set by the digitization time of the ADC.

After the computer completes the entire readout sequence, the analog switches are closed again. This automatically discharges the storage capacitors. The binary counters on all amplifier boards are reset by setting EI to the first board low; the EO is then carried to the EI of the next board and the reset ripples through all the boards. The system is then ready for another event.

5. The plane controllers

A block diagram [3] of the plane controller is shown in fig. 5. Each of the 30 plane controllers contains a 12-bit ADC, a hit threshold comparator so that only signals above a settable threshold are digitized, buffer memory, and control electronics. The plane controller communicates with each of the 25 amplifier boards it services through the 20-conductor ribbon cable and with the CAMAC interface through a single 30-twisted pair master ribbon cable (MRC). Supply voltages for the amplifier boards and the plane controller itself are brought into the plane controller through a separate Molex connector. Two BNC connectors are used to bring in the TEST GATE and HOLD signals which require more careful timing (see below).

The ADC is an Analog Devices AD574J 12-bit ADC, which is capable of a conversion in  $< 35 \mu s$ . The ADC and buffer amplifier for the hit threshold comparator are connected directly to the analog bus on the 20-conductor ribbon cable. Much care was devoted to proper grounding of the analog signals with the result that the pedestal widths were generally less than one ADC channel.

The buffer memory is 256 words of 20 bits each: 12

bits for the ADC data and 8 for the wire address. It is implemented from low-cost 2111 MOS RAMs. A pair of 74LS191 4-bit up/down counters contain the hit count which is initially zero. Upon receipt of a BNC-HOLD the plane controller initiates the readout of the amplifier boards by setting EI on the 20-conductor ribbon cable true. The readout then cycles through all the boards. Its completion is signalled when the LAST EO line comes up.

Whenever any plane controller is scanning it holds the MRC-BUSY line down. Once the MRC-BUSY line goes up the data stored in the plane controller RAMs can be read out by the CAMAC interface under control of the PDP-11 data acquisition computer. The order of readout is the order in which they are cabled. The plane address is read from a DIP switch in each plane controller. Four signals HOLD1-HOLD4 permit the system to be divided into four nearly independent sub-systems. In our case only two of these are used: one for PWC data and the other for a system of thermistors and gas pressure transducers which are read out between beam spills.

The readout of the data from a plane controller is initiated by setting the MRC-EI line true. The MRC-EI and MRC-EO lines constitute a cascading enable which

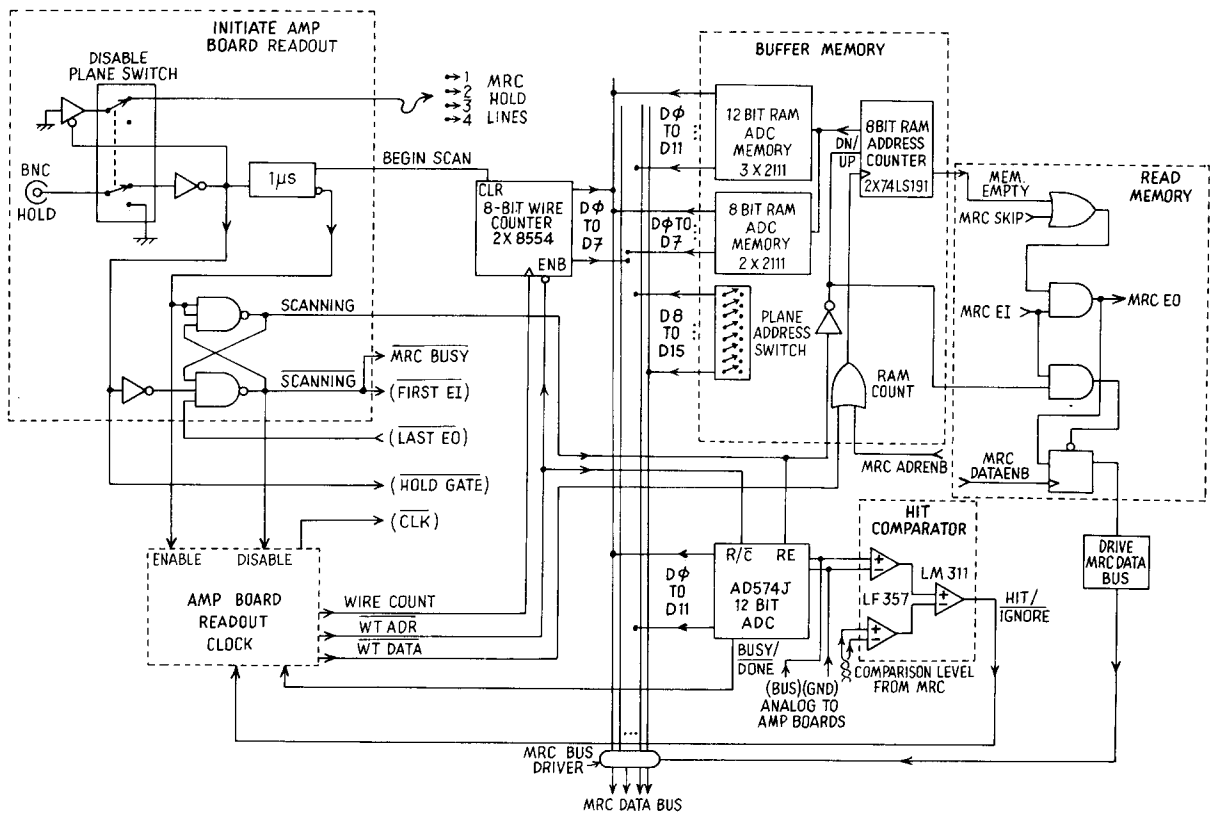


Fig. 5. Block diagram of the plane controller. Labels in parentheses refer to signals on the 20-conductor cable.

is carried from one plane controller to the next as in the readout of the amplifier cards. The last MRC-EO is looped back to the CAMAC interface to signal that readout is complete. During the readout the CAMAC interface alternately strobes the address enable ADRENB and data enable DATENB lines, and the appropriate information is put on the data bus as 16-bit words. During the address strobe the lower 8 bits are the wire address and the upper 8 are the plane address from the DIP switch. During the data strobe the lower 12 bits are the ADC data and the upper 4 bits are status (which should always be zero).

During normal data taking the MRC-COMPARE THRESHOLD was set to give a threshold for the readout about 25 mV above the average pedestal value. In other words only pulses which exceeded the average pedestal by more than 25 mV were read out. Typically one or two pedestals were more than 25 mV above the average and these channels would always be read. Pulses from minimum ionizing particles were recorded by setting MRC-COMPARE-THRESHOLD to  $-5.0$  V. The MRC-SKIP provides a means of flushing data in the currently selected plane controller which was useful in both testing and in recording pedestals.

## 6. CAMAC interface

The CAMAC interface [3] controls the overall system timing during the readout phase. It has two digital-to-analog converters to set the MRC-COMPARE-THRESHOLD and the MRC-TEST-LEVEL, and the data buffers to bring data to the CAMAC dataway.

The readout of the plane controllers is conducted by the CAMAC interface, in conjunction with the software running on the computer operating the CAMAC system. The software must loop until MRC-BUSY goes inactive; the "read status" CAMAC command with MRC-BUSY inactive then initiates the look-ahead readout of the system. While the computer is setting up to transfer the data, the CAMAC interface issues a MRC-DATAENB pulse to enable the first plane controller with any data; this is followed by a MRC-ADRENB pulse to read the wire address of the first hit in that plane. The first CAMAC data transfer will read this wire address, and initiate look-ahead to its ADC data by issuing a MRC-DATAENB. The next CAMAC data transfer will read this ADC data and initiate look-ahead to the next hit wire address by issuing a MRC-ADRENB. This sequence continues until the stored data are exhausted.

At the trailing edge of each MRC-DATAENB pulse, every plane controller decides whether it is to be enabled for the next MRC-ADRENB, depending on its MRC-EI status and hit wire count. When MRC-LAST-EO is sensed by the CAMAC interface, it will cease

returning the Q-response to a data transfer operation which signals the end of the readout.

The system is reset by sending a "clear" to the CAMAC interface. This resets the interface and generates a TTL pulse which is used to reset the flip-flops which generate the BNC-HOLD signals to the plane controllers.

The MRC-TEST-LEVEL, generated by a DAC in the CAMAC interface, is routed to all the amplifier boards through the plane controllers and ribbon cables. It allowed us to test all the amplifiers with signals from zero to well above saturation. The test pulse sequence is initiated by a BNC TEST GATE followed in approx. 700 ns by a HOLD.

## 7. Performance

The offset adjustments in the plane controller ADCs were adjusted to put the pedestals from a standard board at approx. 100 ADC counts. The distributions of pedestals for all channels then was found to have a width ( $\sigma$ ) of approx. 3.9 counts after a few peculiar channels were fixed. Noise in the system was such that the width of individual pedestals was  $\approx \pm 0.5$  counts. Under normal running conditions the wire high voltage was adjusted to put the peak in the pulse height distribution from muons at 35 counts above the pedestal. We were then able to set the threshold for the sparse scan at  $\sim 10$  counts above the average pedestal. Under these conditions the efficiency for muon pulses to be recorded in each plane of horizontal or vertical wires was found to be 93%. This is consistent with the efficiency expected in view of the 1.6 mm thick aluminum web of the PWC extrusions. Fig. 6 shows the output of two channels vs. test pulse amplitude. The output is quite linear until saturation occurs abruptly at about 3800 counts. This gives a useful dynamic range of one to one hundred equivalent particles passing through a single PWC cell. The distribution of gains of the individual amplifier channels was found to have a width  $\sigma = 5.0\%$ . This is consistent with the  $\pm 5\%$  tolerance of the 1.8 pF integrator capacitor and the 4.7 pF capacitor for the test pulse.

In general the overall performance of the system was limited by the PWCs themselves rather than the electronics. The gas gain is a sensitive function of wire diameter, wire positioning, gas composition, gas temperature and pressure [1]. The high voltage feedback system helped to stabilize the gain against slow drifts due to changes in gas purity, temperature or atmospheric pressure, but it could not help local variations due to wire diameter tolerances or temperature and pressure gradients. The gain of each wire could be determined with good accuracy by observing the position of the single particle peak in the pulse height distributions from the wire. Nevertheless it was desirable to keep the wire

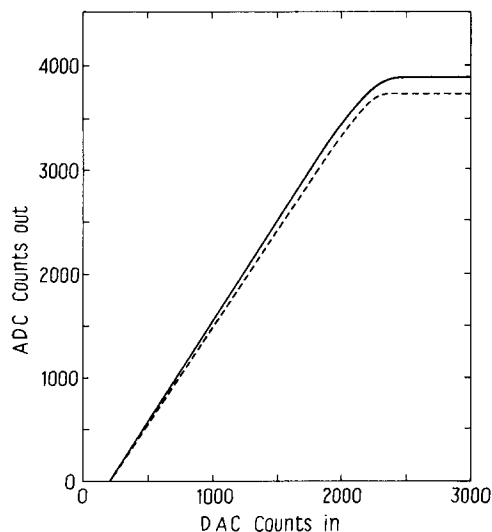


Fig. 6. ADC output vs. test level DAC for 2 channels. Under normal running conditions single particles give pulses about 40 ADC counts above pedestal.

gains as uniform as possible over the whole system so that software corrections to the pulse heights could be introduced at the latest possible stage in the analysis. Our success in achieving this is illustrated in fig. 7 which shows the distribution of the positions of the muon peaks for 1500 wires. The fwhm of the distribution is about 15%, which is quite satisfactory. No significant variation of pulse height with distance along the wire or distance of the track from the wire has been observed.

Unfortunately it is rather difficult with our apparatus to study the linearity of the pulse height vs. energy deposition in the PWCs. In our experiment this was not a major consideration because the primary energy information came from the phototubes on the lead-scintillator calorimeter modules between the PWC planes. To obtain the best possible linearity in the PWCs we used the maximum amplifier gain consistent with our other requirements of cost and dynamic range. We then operated the PWCs with the lowest practicable gas gain to minimize space charge effects. Tests of a prototype of our detector in a hadron beam showed that the total pulse height from the PWCs, summed over all planes, was a linear function of incident hadron energy. The success of these tests suggests that a calorimeter instrumented only with PWCs and a readout system like that described here should work well.

Other groups [1] with similar PWC systems have observed a significant variation of pulse height with the angle of the incident track relative to a normal to the wire. We looked for such an effect with incident muons. In our system we found  $\approx 5\%$  variation of pulse height with angle for tracks up to  $25^\circ$  to the normal (other

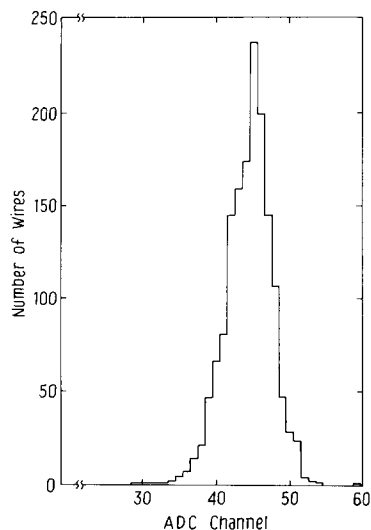


Fig. 7. Mean pulse heights for muons traversing the detector for approx. 1500 wires. No software corrections have been applied.

than the expected  $\cos \theta$  dependence), with either argon- $\text{CO}_2$  or pure ethane gas in the system. This presumably is because we used a lower gas gain which reduced space charge effects.

## 8. Reliability

After the initial checkout of the boards and some burn-in time, we observed very few failures. This is consistent with the very low parts count and low power dissipation of the system\*. In the initial checkout of the boards a significant number of bad SD5002 analog switches were found, but these switches proved reliable after the infant mortality stage. No careful statistics were kept on failures during operation, but after boards with more subtle problems (like pedestals out of tolerance or unusually slow gating) were weeded out, probably no more than 30 channels failed in several months of operation. No amplifier has ever been observed to oscillate.

On the whole our 6000 channel system proved to be impressively trouble-free and easy to operate.

## References

- [1] C. Bosio et al., Nucl. Instr. and Meth. 157 (1978) 35.
- [2] R.L. Anderson et al., Proc. IEEE Symp. on Nuclear science, San Francisco, 1977, IEEE Trans. Nucl. Sci. NS-25 (1978) 340.
- [3] Detailed schematics of the plane controller and CAMAC interface are available from the authors.

\* Each amplifier board (8 channels) draws only 80 mA from each of the +12 V and -3.5 V supplies so the total power dissipation is only approximately 150 mW per channel.