

BRIEF COMMUNICATION

A Microprocessor Device for the Real-Time Detection of Synchronized Alpha and Spindle Activity in the EEG

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MORROW, T. J. AND K. L. CASEY. *A microprocessor device for the real-time detection of synchronized alpha and spindle activity in the EEG.* BRAIN RES BULL 16(3) 439-442, 1986.—A microprocessor based device is described which permits the real-time detection of synchronized EEG activity within the frequency range of the alpha rhythm or sleep spindles. This device offers a reliable, inexpensive method for EEG analysis according to flexible, user selectable parameters. It can be used either on-line or off-line and provides information as to the occurrence and duration of alpha-spindle EEG activity.

EEG	Synchronized activity	Microprocessor	Frequency detection	Alpha rhythm
Sleep spindles				

IT is well known that during the transition from wakefulness to sleep, as well as during stage 2 sleep, the cortical EEG pattern becomes synchronized and increases in amplitude. The spectrum of frequencies present in the EEG during this time falls into two ranges, 8-12 c/sec (Alpha rhythm) which occurs during drowsiness and 11.5-15 c/sec (sleep spindles) which occur during sleep. Recent studies in our laboratory required the automated real time detection of synchronized EEG activity within the 6-17 c/sec range, as one measure of an animal's level of arousal or wakefulness during single unit recording in the thalamus. Although our laboratory minicomputer could have easily been programmed to detect the presence of these EEG frequencies, we chose to employ a dedicated, stand-alone device which could be used with limited or no additional computer resources. The output of this detector had to be compatible with a variety of other devices including a chart recorder and the lab computer system.

While several other analog and/or digital spindle detection systems have been described [1, 2, 3, 4, 5], most did not allow on-line detection of synchronized waveforms in real time [1,4] or required extensive computer processing of the analog signal [2,3]. Some designs employed phase-locked

loop technology, but we found these designs to be either unreliable or too slow to detect the low frequencies present in the EEG during alpha or sleep spindle synchronization [1, 2, 5].

THE EEG alpha-spindle synchronization detector described here uses a few analog integrated circuits and a 6502 microprocessor with control software in programmable read only memory (PROM), thus offering an inexpensive and reliable approach to the real time detection of alpha rhythm and sleep spindle activity. This system provides a binary output indicating the presence or absence of EEG synchronization (within the 6-17 c/sec range) according to flexible user defined criteria. It is very reliable in operation, relatively simple and inexpensive to construct, and requires no specialized instrumentation or computer interfacing.

SIGNAL PROCESSING

Analog Signal Conditioning

The analog section of the synchronization detector consists of three operational amplifiers and one voltage comparator circuit. The EEG signal, pre-amplified 1000 times and filtered (1 to 40 Hz) using standard neurophysiological

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BLOCK DIAGRAM OF THE ANALOG AND CPU CIRCUITRY

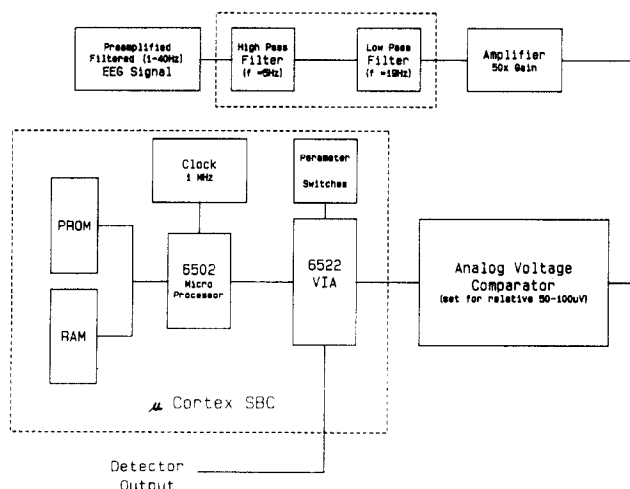


FIG. 1. Block diagram showing the basic interconnection of the analog pre-processor and the microprocessor circuits.

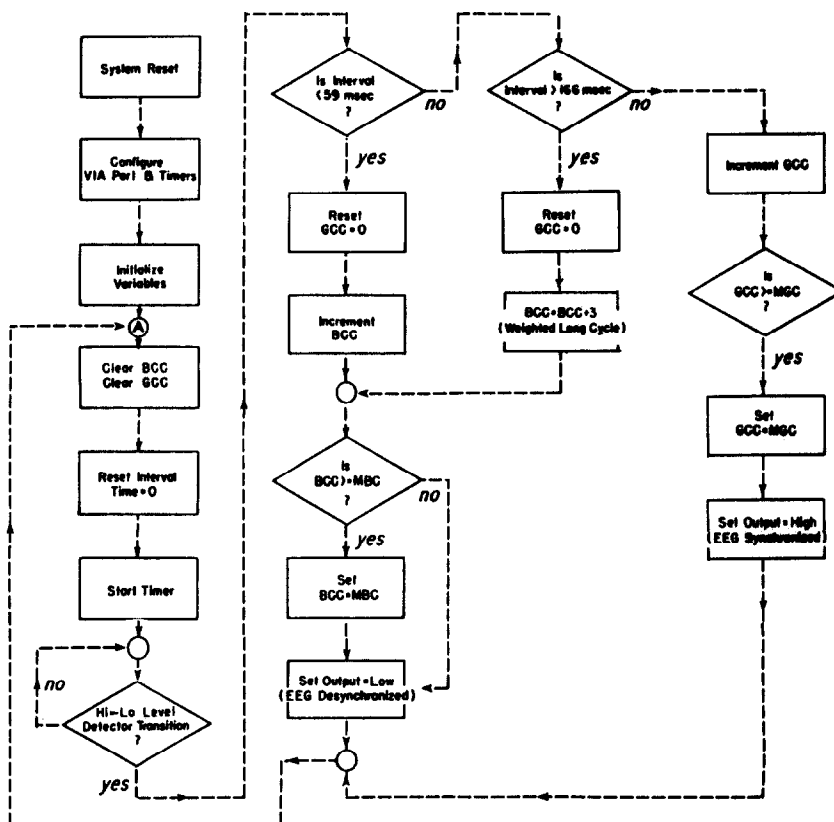


FIG. 2. Simplified microprocessor software flow diagram. BCC=Sequential Bad Cycle Counter, GCC=Sequential Good Cycle Counter, MBC=Maximum Bad Cycle Count, MGC=Maximum Good Cycle Count. Note the weighting of low versus high frequency out of band "bad cycles."

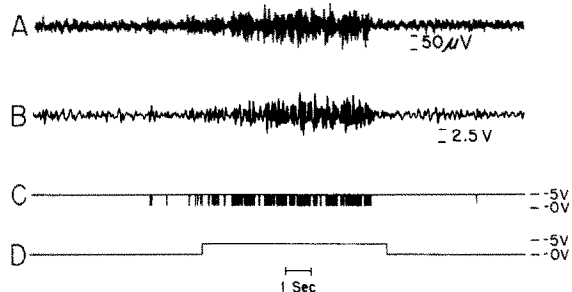


FIG. 3. Chart recordings illustrating the various inputs and outputs of the EEG synchronization detector. A: Cortical EEG input signal, pre-amplified (1000 \times) and pre-filtered (1–40 Hz). B: Output of the sync-detector signal conditioning filter. C: Output of the analog voltage comparator, with threshold set for 50 microvolts relative to the actual EEG amplitude. D: Output of the SBC indicating the occurrence and duration of synchronized EEG activity in the 6–17 c/sec range.

instrumentation and techniques, is fed to the input of the detector. Here, the signal is additionally filtered for activity in the 4–20 c/sec range using a narrow bandpass active filter. This filter was comprised of separate multiple-feedback high-pass and low-pass sections with a flat gain response and a 40 dB/decade rolloff. The conditioned signal is then amplified 50 times and processed through a voltage comparator with the threshold level set to between 25–100 μ V (relative to the actual amplitude of the EEG). For calibration, 25–100 millivolt, 6–17 c/sec sine wave from an external signal generator is applied to the input of the detector's filter stage, bypassing the 1000 \times preamplifier. The comparator's threshold control is then adjusted so that each time the incoming signal level exceeds this threshold value, the output of the comparator goes from high (+5 volts) to low (0 volts). Likewise, when the input no longer exceeds threshold, the comparator output returns to the high state. Controlled input hysteresis, built into the comparator circuitry, prevents the generation of multiple output transitions for each threshold crossing. Each cycle of the EEG waveform meeting this amplitude criterion is thereby converted into a digital signal for use by the microprocessor based frequency detection section.

FREQUENCY DETECTION

Microprocessor Hardware

Frequency processing by the alpha-spindle detector is accomplished by a small single board computer (SBC) consisting of a 6502 microprocessor (CPU) with a 1 megahertz system clock, a 6522 versatile interface adaptor (VIA), 1000 bytes of random access memory (RAM) and a socket for installation of up to 4000 bytes of programmable read only memory (PROM). A block diagram of the SBC and the analog signal conditioning circuitry is shown in Fig. 1. Frequency timing and all input and output between the analog circuitry and any display device (i.e., chart recorder) are provided by the system clock and the VIA, which has 16 bidirectional I/O lines, 4 control lines and two 16 bit counter-timers. The software for detection of synchronized EEG activity is programmed into PROM (see below), and plugged into a socket on the SBC. The complete microprocessor section on a 4 \times 5 inch printed circuit board, less the

software in PROM, is commercially available (uCortex/65 SBC, Cortex Research Corp, Northbrook, IL), thus eliminating the need for construction of any microprocessor circuitry.

Detection Software

The software used on the uCortex/65 SBC for the detection of EEG frequencies falling within a 6–17 c/sec range was developed in our laboratory on a Rockwell AIM-65 micro-computer system. A simplified flow diagram of the frequency-analysis algorithm is shown in Fig. 2.

The detection of synchronized EEG activity in the alpha or spindle range is determined by three critical parameters: waveform amplitude, waveform frequency, and duration of synchronization of the waveform (minimum number of sequential inband cycles). It is obvious from visual inspection of EEG records, that a given segment of alpha or spindle activity frequently includes transient periods where the waveforms are above or below the desired frequency bandwidth. Within certain limits, such brief out-band episodes can be ignored, and the entire segment containing them can be classified as in-sync. A system for the automatic detection of such synchronized EEG should take into account such waveform imperfections, and allow flexible analysis before determining that a segment of the input waveform is outside the desired synchronous frequency range or truly desynchronized. The system described here has attempted to include all of the above detection features.

The EEG signal amplitude requirement is determined by the analog pre-processor circuitry through adjustment of the level detector threshold. The frequency, duration and desynchronization criteria are tested completely with software (see Fig. 2). Using the T1 timer of the processor VIA setup as a free-running 1 msec clock, the EEG waveform frequency is tested by measuring the time interval between successive negative going transitions of the analog level detector output connected to the CA1 control line input of the VIA. If the interval between EEG waveform cycles is greater than 59 msec (frequency < 17 c/sec) or less than 166 msec (frequency > 6 c/sec) the sequential in-band waveform cycle counter (good cycle counter) is incremented and the out-band sequential cycle counter (bad cycle counter) is set to zero. When a preselected number of good cycles are counted, the output of the detector (VIA output) goes high (+5 volts) to indicate that the EEG is synchronized within the 6–17 c/sec (alpha or spindle) range.

When an EEG waveform cycle occurs outside the desired frequency range, the good cycle counter is reset to zero and the sequential bad cycle counter is incremented. If the interval between cycles is greater than the maximum of 166 (frequency < 6 c/sec), the bad cycle counter is incremented by three. If the input frequency is greater than 17 c/sec (interval < 59 msec) the bad counter is only incremented by one. Thus, the number of bad cycles is weighted depending on whether the frequency is above or below the desired detection band. When the bad cycle counter reaches a preset value, the output of the detector (VIA output, PB0) goes low (0 volts) to indicate that the EEG is either out-band or truly desynchronized, according to user-specified parameters. Actual selection of these good-bad cycle detection parameters is accomplished by several switches attached to VIA inputs. These switches can be set for from 1 to 16 minimum in-band and maximum out-band cycles.

The actual function of the EEG synchronization detector

described in this paper is illustrated in Fig. 3. Note that all of the above features are present: (1) amplitude sensing, seen as the presence or absence of output from the level detector, (2) frequency detection, (3) registration of the duration of synchronization, seen as the 0 to +5 volt transition of the detector output only after several good cycles occur; and (4) de-synchronization detection, seen as the shift of the detector output only after several bad cycles occur. Typical operating parameters used in our laboratory include a 50 μ V amplitude threshold, 3 cycles for minimum sequential good cycles and 8 cycles for maximum sequential bad cycles.

DISCUSSION

As a means of automatically detecting the presence of synchronized alpha or spindle activity in the EEG, the alpha-spindle detector described here compares very well with results obtained by visual scoring of EEG records. The EEG tracings of several subjects were both processed through the alpha-spindle detector and independently evaluated by four individuals for periods of synchronization in the 6–17 c/sec, alpha-spindle range. Differences in visual scorings were resolved by mutual consensus. Comparisons between the individual visual and automated detections showed 97.9% agreement on 48 of 49 alpha-spindle epochs. The detector also revealed the presence of synchronized activity for several additional in-sync episodes (approximately

12.2% more) than were reported with visual scoring. Further inspection of these records showed the presence of synchronized activity during all of these EEG segments.

The internal consistency and reliability of the alpha-spindle detector was tested by processing a 60 second segment of pre-recorded EEG activity through the device 20 times. The detector consistently and accurately identified all epochs of synchronized activity falling within the 6–17 c/sec range.

The EEG synchronization detector presented here offers advantages over previous designs. It permits user selection of all critical detection parameters including amplitude threshold and the minimum number of sequential in-band or out-band cycles required for in-sync or de-sync determination. The use of a simple software algorithm allows most parameters to be easily entered by setting a few switches. This device also operates reliably in real-time and indicates not only the occurrence of synchronized EEG activity but also the duration of such an episode. Finally, because the device is microprocessor based, the algorithm for sync-detection can easily be adapted to work over different frequency ranges or incorporate other detection criteria.

Circuit schematics and a software listing are available from the authors. A PROM containing the frequency detection software is available from J and T Associates, 2170 Steeplechase Dr., Ann Arbor, MI 48103.

REFERENCES

1. Broughton, R., T. Healey, J. Maru, D. Green and B. Pagurek. A phase locked loop device for automatic detection of sleep spindles and stage 2. *Electroencephalogr Clin Neurophysiol* **44**: 677–680, 1978.
2. Johns, M. W., E. B. Stear and J. Hanley. Tracking the dominant frequency of the EEG by phase-locked demodulation. *Electroencephalogr Clin Neurophysiol* **37**: 414–416, 1974.
3. Gaillard, J. M. and R. Blois. Spindle density in sleep of normal subjects. *Sleep* **4**: 67–77, 1981.
4. Matsubayashi, K., Y. Ishiyama, I. Homma and M. Ebe. Some characteristics of sleep spindles derived from automatic analysis. *Sleep* **4**: 392–399, 1981.
5. Pivik, R. T., F. W. Bylisma and R. J. Nevins. A new device for automatic sleep spindle analysis: The 'Spindicator.' *Electroencephalogr Clin Neurophysiol* **54**: 711–713, 1982.