

Process Integration for Active Polysilicon Resonant Microstructures

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Abstract

Microsensors based on active polysilicon resonant microstructures are attractive because of their wide dynamic range, high sensitivity and frequency shift output. In this paper, we discuss processing issues for integrating electrostatically-driven and -sensed polysilicon microstructures with on-chip nMOS devices. Surface-micromachining using sacrificial spacer layers is used to obtain released microstructures. A novel feature is the use of rapid thermal annealing (RTA) for strain relief of the ion-implanted, phosphorous-doped polysilicon. Resonance frequencies of cantilever beams indicate a lower-bound Young's modulus of about 90 GPa and an upper-bound compressive residual strain of only 0.002%, indicating that RTA is potentially useful for strain relief.

1. Introduction

Solid-state microsensors are currently being investigated for a wide variety of applications because of their potential for low cost and high performance. One promising approach uses resonant microstructures, where the resonance frequency of a mechanical element is made sensitive to a physical or chemical parameter of interest [1]. To measure the resonance frequency of a micro-mechanical structure, a means for producing and detecting its motion is needed. Vibration has been produced by several different methods, including thermal, piezoelectric and electrostatic drives. The resulting motion of the structure has been detected by using piezoresistors, piezoelectric thin films, capacitance variation (electrostatic detection), as well as other techniques. For conduct-

ing microstructures, including polysilicon, electrostatic drive and detection has several attractions [1]. The most important advantage of this technique is the simple mechanical structure that results. Because the microstructure itself is conducting, it can be used as one plate in the capacitor. Thus, electrostatic drive and detection does not require a complicated microstructure incorporating the additional thin films or diffusions that would be necessary for other drive and detection schemes mentioned above. This simplicity makes the mechanical properties of the microstructure much easier to control.

To vibrate polysilicon resonant microstructures, a sinusoidal electrostatic drive force is exerted on the microstructure by applying a signal consisting of an a.c. drive voltage v_d and d.c. polarization V_p to the drive electrode; the resulting microstructure motion is detected as current flowing through the device (Fig. 1). When the microstructure is driven at its first natural frequency f_1 , the device current and microstructure motion reach their maximum amplitude [1]. If the same pair of electrodes is used to drive the microstructure and sense its motion, the device is referred to as a one-port resonant microstructure [2]; if two electrodes are used to provide the driving force and motion detection, then it is a two-port resonant microstructure [1]. While the devices fabricated in this work are one-part microstructures, our results are directly applicable to other configurations.

Polysilicon resonant microstructures are fabricated using a set of processes referred to as surface micromachining [3]. A key feature of surface-micromachining processes is a sacrificial spacer layer, which is used to support the microstructure layer during deposition and patterning. The sacrificial layer is then etched away, leaving a free-standing microstructure (Fig. 2).

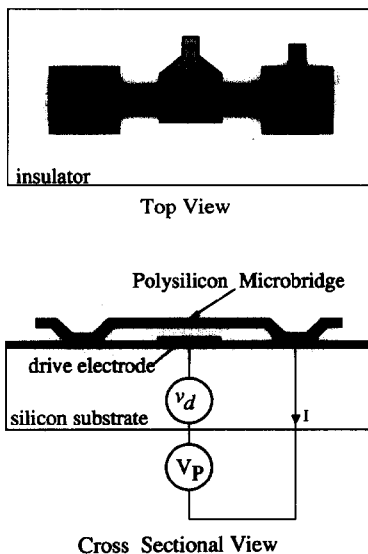


Fig. 1. Operation of resonant microstructures.

In order to integrate circuits with surface-micromachined structures, it is desirable to add the microstructures to previously fabricated circuits. A significant advantage of this approach is that the final steps in the process can be optimized for the mechanical properties of the microstructure. This partitioning generally results in a simpler overall process, because the impact of the complex circuit fabrication sequence on the micromechanical structures need not be considered. Under this scenario, it is desirable that the steps used to fabricate the microstructures have

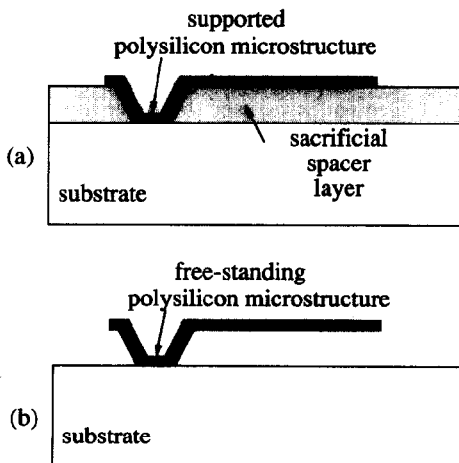


Fig. 2. Schematic representation of surface micromachining. (a) After patterning of the polysilicon microstructure; (b) after removal of the sacrificial spacer layer, leaving a free-standing polysilicon microstructure.

minimal impact on the electrical characteristics of the circuits. If this can be accomplished, the on-chip circuitry (except perhaps for the metallization) could be fabricated by an IC foundry.

A critical issue in the fabrication and operation of resonant microstructures is the mechanical properties of the beam material. If the material is under compression, then the resonance frequency f_1 will be decreased, with the potential for buckling in long beams. Tensile residual strain will raise f_1 and also reduce the amplitude of vibration. The control of residual strain in polysilicon by varying deposition temperature and annealing cycles has been studied extensively [4–6]. A furnace anneal in a nitrogen ambient is commonly used to relieve residual stress in phosphorus-doped polysilicon. This approach is not attractive for active microstructures with on-chip circuitry, since it will degrade the electrical characteristics.

In this paper, we address the fabrication of active polysilicon resonant microstructures, concentrating on the steps used to control the mechanical properties of the polysilicon and the interaction of these steps with on-chip circuitry. We describe a prototype fabrication sequence used to make electrostatically driven surface-micromachined polysilicon beams integrated with an nMOS depletion-mode transistor for capacitive detection of the beam vibration. We then present initial results of measurements used to estimate the plate modulus and residual strain of the polysilicon from the resonance frequencies of cantilevers and bridges.

2. Process Integration

The fabrication of polysilicon resonant microstructures with on-chip circuitry involves some important considerations that are not encountered in conventional silicon IC processing, some of which have been previously discussed by Howe [4]. In this Section, we discuss similar process integration issues, emphasizing the important interactions between the requirements of the micromechanical structures and on-chip circuits. Four areas, polysilicon strain relief, sacrificial spacer layer, active device protection and interconnect, deserve special consideration and are discussed in detail. This is followed by a description of the entire fabrication sequence.

2.1. Strain Relief of Polysilicon

An important process design consideration for active resonant microstructures is how to achieve low-strain polysilicon with good mechanical properties and still incorporate on-chip circuitry. Since the on-chip circuitry is subjected to all of the

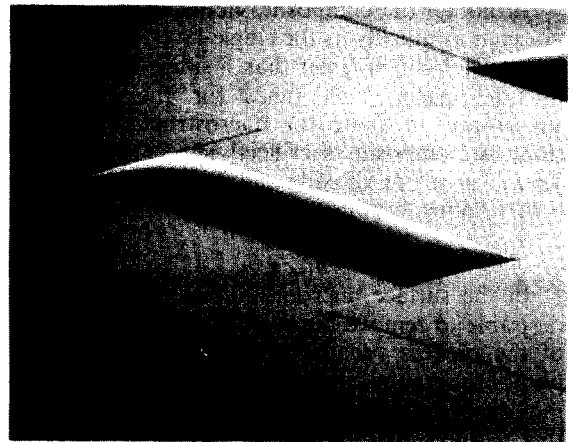
processing required by the polysilicon microstructures, including a thermal cycle that is generally required to relieve the high compressive stress of as-deposited polysilicon [4, 7], this strain-relief cycle and its effect on the on-chip circuitry must be carefully considered.

Many transistor and circuit parameters depend strongly on the location of dopants in the silicon substrate. For example, modern MOS processes have shallow source/drain diffusions to limit short-channel effects, and it is necessary to limit thermal processing following the diffusion implants to keep the junctions from being driven too deep. The transistor threshold voltages often depend on maintaining a threshold-control implant close to the substrate/gate oxide interface. Also, in a CMOS process latch-up immunity is influenced by careful control of the doping profile in the diffused well, as in a retrograde-well process.

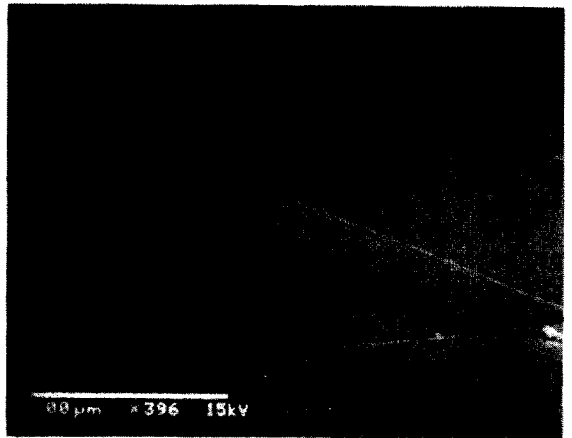
Conventional furnace steps have been investigated for strain relief of polysilicon [4, 8]. However, these steps use high temperatures and large thermal budgets, and would certainly have a detrimental effect on the on-chip circuitry. To minimize this problem, we have investigated rapid thermal annealing (RTA), with its associated low thermal budget, as a strain-relief technique for polysilicon microstructures. We have found RTA, for three minutes at 1150 °C, to be effective as furnace annealing for reducing the strain in as-deposited polysilicon. The low thermal budget for this process has a minimal effect on the on-chip circuitry but is very effective for reducing the high compressive strain in the polysilicon film, allowing free-standing microstructures to be incorporated with high-quality circuitry. Experimental data supporting these conclusions will be presented below.

2.2. Sacrificial Spacer Layer

Surface micromachining relies on very high selectivity between the sacrificial spacer layer and the polysilicon used for the microstructures. Etching of the sacrificial layer from under the microstructure must take place laterally, and distances of many microns are common. Thus very long etches are required to remove the sacrificial layer completely. Some form of silicon dioxide is commonly used as the sacrificial layer, because it is etched much more rapidly in hydrofluoric acid (HF) than is polysilicon (which remains essentially untouched). Phosphosilicate glass (PSG) is often used as the sacrificial layer, because it is etched more rapidly in HF than is undoped silicon dioxide. It can also be conveniently deposited using chemical vapor deposition (CVD), and is a common material in conventional IC processing.



(a)



(b)

Fig. 3. Scanning electron micrographs showing effect of sacrificial spacer layer on polysilicon film. (a) PSG spacer, resulting in badly distorted microstructure; (b) composite PSG/SiO₂ spacer, resulting in flat microstructure.

However, when a single-layer PSG sacrificial spacer is used, we observed that the polysilicon microstructure was severely distorted after the strain-relief cycle (Fig. 3(a)). Similar effects were observed during furnace annealing at 1100 °C of polysilicon/PSG/Si₃N₄ sandwiches [9]. This distortion may have occurred because the PSG spacer flows at 1100 °C and does not adhere well to the underlying Si₃N₄; this allows the microstructure to assume a relaxed configuration before the high compressive stress has been relieved. One way to avoid this problem is to use a composite sacrificial spacer of PSG on top of an undoped CVD silicon dioxide layer. In this configuration, the PSG still flows at the anneal temperatures but adheres well to the underlying silicon dioxide layer (which does not flow), thereby holding the polysilicon layer in place during the anneal procedure. This results in a flat, undistorted microstructure (Fig. 3(b)).

Although the composite sacrificial spacer does not etch as quickly as the single-layer PSG spacer, it does etch much faster than a single-layer silicon dioxide spacer; etch times for the composite spacer are adequate for microstructure fabrication. A composite sacrificial spacer comprising $1.6\ \mu\text{m}$ of silicon dioxide and $0.4\ \mu\text{m}$ of PSG with 6 wt.% phosphorous is used in this process.

2.2.1. Undercut protection

In the surface micromachining processes, it is desirable to remove the sacrificial layer at the end of the process because it is difficult to perform photolithography, depositions or further processing on free-standing microstructures. However, this requires that the active on-chip circuitry be exposed to the very aggressive HF etch that is used to remove the sacrificial layer. Clearly some means of protecting the active circuitry during the undercut etch is required. In our process we employ Si_3N_4 deposited by low-pressure chemical vapor deposition (LPCVD) to protect the active devices (as in the resonant-microbridge vapor sensor process [4]); Si_3N_4 is etched relatively slowly by HF.

A problem we found in using Si_3N_4 as an etch protection layer was a degradation or complete loss of the d.c. polarization voltage, V_p , between the drive electrode and the microstructure, when the silicon nitride layer covered the drive electrode [10]. Some possible explanations for this loss of voltage include surface leakage on the silicon nitride film or charge storage at the interface between the silicon nitride and the drive electrode silicon dioxide. Whatever the cause, this problem was solved by removing the silicon nitride over the drive electrode. Because it must be located under the microstructure, it is convenient to fabricate the drive electrode from the gate polysilicon layer, which is resistant to attack by HF. As a result, the removal of the Si_3N_4 layer does not affect the passivation against HF.

2.3. Interconnect

In our process, the polysilicon microstructure layer was also used as the circuit interconnect layer (rather than the aluminum metallization used in the resonant-microbridge vapor sensor [4]) since it had sufficient conductivity for this purpose. This interconnect approach was used in the multichannel microprobe [11] and has the advantage of not needing to be protected, as aluminum would, during the undercut etch.

If more complicated circuitry requiring low-resistance interconnect were added to the resonant microstructures, there are several different options available. If the circuitry, including interconnect, is fabricated by a foundry, then the interconnect

must be able to withstand the high temperature of the sacrificial spacer layer deposition and RTA strain-relief processes. A conventional plasma-CVD Si_3N_4 overglass layer can probably serve as the undercut protection layer. If bond pad openings are defined prior to microstructure formation, then the exposed material must also withstand the HF undercut etch. Tungsten meets all of these requirements, and is commonly used in the IC industry.

If, on the other hand, the interconnect layer can be deposited and defined after the microstructure polysilicon definition (but before the undercut etch), then it need not withstand the high-temperature steps. Tungsten can also be used under these circumstances. If it is necessary that the interconnect have minimal resistance, then gold is acceptable, since it is not attacked by HF.

2.4. Fabrication Sequence

The process integration issues discussed above provide the basis for a prototype fabrication sequence that builds heavily upon the resonant-microbridge vapor sensor process developed by Howe [4] and the multichannel microprobe process developed by Najafi and Wise [11]. The test vehicle was a test chip that includes several nMOS transistors to characterize the on-chip circuitry, and several active microcantilevers and active microbridges of different lengths to characterize the mechanical properties of the polysilicon.

The active resonant microstructures discussed here incorporate the one-transistor nMOS interface circuit shown in Fig. 4. The air-gap motional capacitance of the microstructure is buffered for off-chip detection by an integrated depletion-mode nMOS transistor, and the diode clamp is used to leak d.c. gate voltage of the transistor to ground.

The fabrication sequence begins by diffusing boron to form a p^+ ground plane that improves the isolation between the drive electrode and the

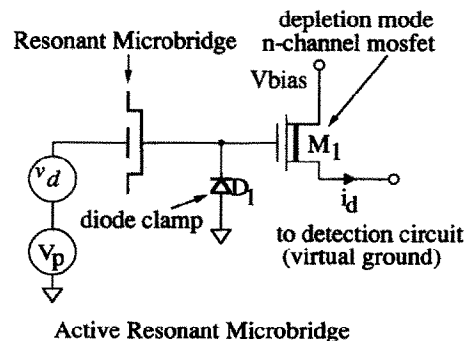


Fig. 4. On-chip interface circuit.

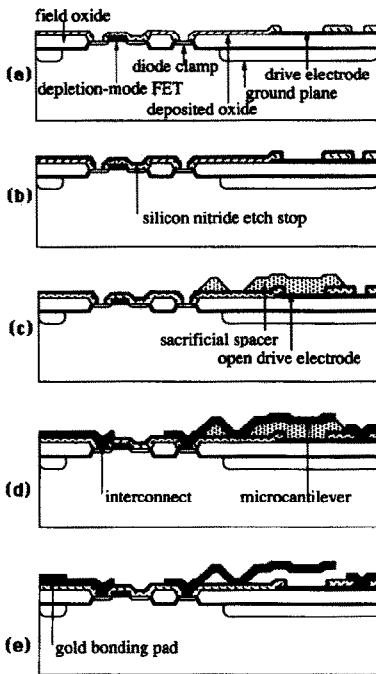


Fig. 5. Process sequence for active resonant microstructures: (a) after formation of ground plane and nMOS circuitry; (b) after patterning of the Si_3N_4 etch stop layer; (c) after patterning of the sacrificial spacer layer; (d) after patterning of the polysilicon microstructure layer; (e) after removal of the sacrificial layer.

resonant microstructure. With the p^+ ground plane defined, the on-chip transistor and diode clamp are fabricated by a conventional four-mask LOCOS nMOS process (Fig. 5(a)). As mentioned above, the gate polysilicon is also used as the drive electrode for the resonant microstructure; an n^+ diffusion was used for this purpose in the resonant-microbridge vapor sensor [4].

The next step is the deposition and patterning of the Si_3N_4 etch-stop layer used to protect the circuitry during the removal of the sacrificial layer (Fig. 5(b)). It is removed from the area over the drive electrode (as discussed above) and from the regions where the polysilicon interconnect layer makes contact to the silicon substrate at the diode in the on-chip circuit. With the active devices protected, the composite PSG/CVD SiO_2 sacrificial spacer layer itself is deposited and patterned (Fig. 5(c)).

After the sacrificial layer is defined, the polysilicon for the resonant microstructures is deposited to a thickness of $1\ \mu\text{m}$ by LPCVD at a temperature of $600\ ^\circ\text{C}$. Fine grain polysilicon was chosen for the microstructure because of its reported highly-reproducible characteristics and superior mechanical properties [8]. The polysilicon is then heavily doped with phosphorus using ion

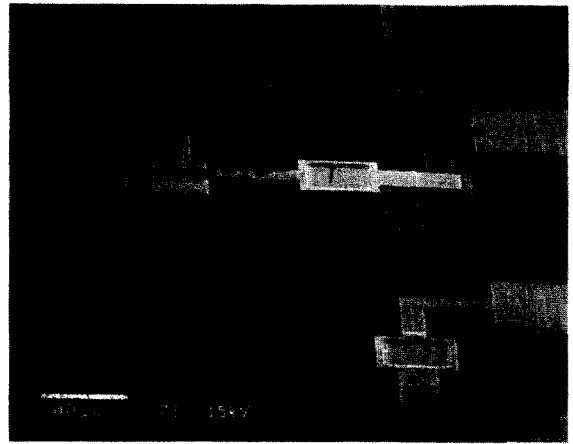


Fig. 6. Scanning electron micrograph of active microbridge.

implantation at an energy of $150\ \text{keV}$ and a dose of $5 \times 10^{15}\ \text{cm}^{-2}$. Next the RTA strain-relief procedure is performed. For our process, this is carried out in an AG Associates Heatpulse 610 RTA system. The wafer was rapidly heated (approximately two seconds) in a nitrogen ambient by quartz lamps to a temperature of $1150\ ^\circ\text{C}$, as measured by an optical pyrometer, and held at this temperature for three minutes. After the high-temperature soak the quartz lamps were shut off and the wafer rapidly cooled to temperatures below $600\ ^\circ\text{C}$ in approximately two seconds. After the RTA strain-relief procedure, the polysilicon microstructure is patterned (Fig. 5(d)).

Gold bonding pads are then added to the device. Gold was chosen for the bonding pads since it is compatible with the final HF undercut etch. Finally, the sacrificial layer is removed by

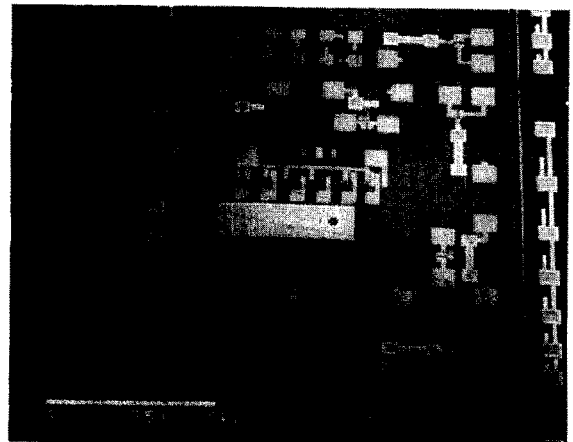


Fig. 7. Photomicrograph of test chip. Test transistors are in the middle, with active microstructures and interface circuits around the perimeter.

etching in concentrated HF and the devices are ready for packaging and testing (Fig. 5(e)). A scanning electron micrograph of an active microbridge fabricated by this process is shown in Fig. 6, and a photomicrograph of the entire test chip is shown in Fig. 7.

3. Experimental Results

In this Section we discuss some experimental results obtained from these test devices. The performance of the electrical devices (diodes and nMOS transistors) is discussed. Data on Young's modulus (E) and residual strain (ϵ) for polysilicon that has been strain relieved by RTA are then presented.

3.1. Electrical Devices

To measure the properties of the diode clamp in the on-chip interface circuit, the test chip includes a large-area diode. The measured characteristics of this device show that it is well behaved, with a clean breakdown ($BV = -39$ V). The minority carrier lifetime is $90 \mu\text{s}$, obtained from measurements of the small-signal junction resistance [10].

Figure 8 shows the drain characteristics (I_D versus V_{DS} with V_{GS} as a parameter) for transistors of widely varying dimensions. These transistors show normal behavior. Extracted transistor parameters are summarized in Table 1, and are close to design values. The conduction parameter k' for both transistors is slightly lower than expected for a surface-channel device with a 100 nm gate oxide, but this result is consistent with the buried-channel nature of the depletion transistor [10].

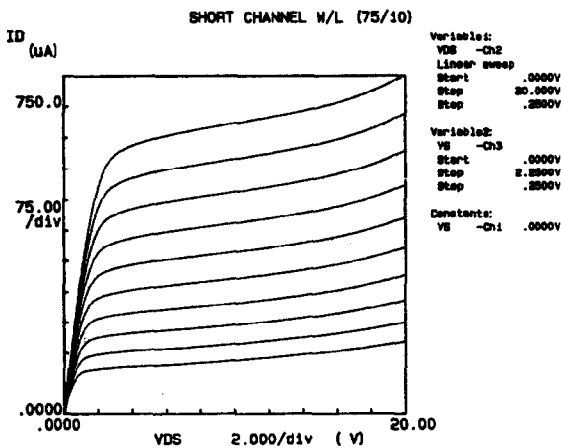


Fig. 8. Drain characteristics of test transistors.

3.2. Mechanical Properties of RTA Strain-relieved Polysilicon

The mechanical properties (plate modulus and residual strain) of polysilicon can be directly extracted from measurements of the resonance frequencies of microcantilevers and microbridges [12]. Our test chip included several microcantilevers and microbridges of different lengths for this purpose. The resonance frequencies of these devices were measured with a HP 4195A network analyzer and the measurement circuit shown in Fig. 9, or with a phase-locked-loop oscillator circuit that continuously vibrated the resonant microstructure at its natural frequency [10]. For these measurements the drive voltage was adjusted such that the amplitude of the microstructure motion was about ± 100 nm as measured by the device capacitance. Table 2 details the dimensions and typical measured resonance frequencies of the devices on the test chip.

The plate modulus $E/(1 - \nu^2)$, where ν is Poisson's ratio, can be found by measuring the resonance frequencies of microcantilevers of varying length. We actually measure the plate modulus rather than Young's modulus because the fabricated microcantilevers had dimensions more like plates than beams; in our devices $W/t \gg 1$, but $L/W \sim 1$ ($W \equiv$ width, $t \equiv$ thickness and $L \equiv$ length). Since microcantilevers are released structures with one free end, their resonance frequency is not affected by the average residual strain in the film. Assuming clamped boundary conditions at the fixed end, the first resonance

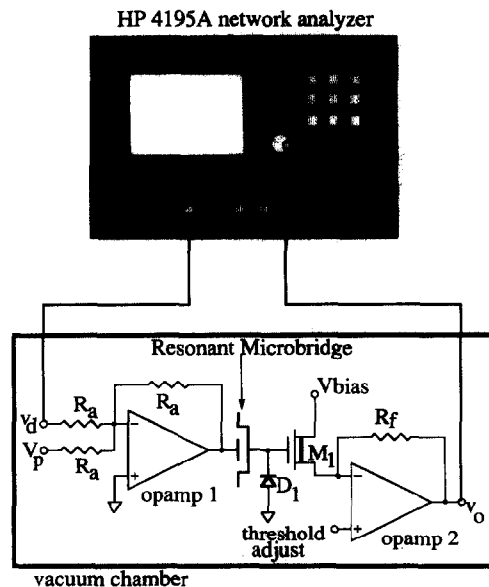


Fig. 9. Circuit for measurement of resonance frequency.

TABLE 1. Extracted transistor parameters

Parameter	Drawn transistor dimensions	
	$W = 75 \mu\text{m}, L = 10 \mu\text{m}$	$W = 10 \mu\text{m}, L = 75 \mu\text{m}$
V_T : threshold voltage	-1.64 V	-1.50 V
g_m : transconductance (in saturation, $V_{GS} = 0$ V)	140 μmho	1.5 μmho
k' : conduction parameter	11.8 $\mu\text{A/V}^2$	7.5 $\mu\text{A/V}^2$
λ : channel-length modulation parameter	0.018 V^{-1}	0.002 V^{-1}

frequency f_1 of the microcantilever is given by

$$f_1 = 0.615 \frac{t}{L^2} \left(\frac{E}{\rho(1-\nu^2)} \right)^{1/2} \quad (1)$$

where ρ is the mass density. Unfortunately, an exact value for Young's modulus could not be obtained from the test structures due to uncertain boundary conditions at the fixed end of the microcantilever. For an ideal clamped boundary condition at the fixed end, the resonance frequency of two microcantilevers of different lengths should scale as L^{-2} . This scaling is not observed in the test devices, indicating a deviation from the perfectly clamped boundary conditions [2]. The microcantilever flares at the anchor, as shown in Fig. 6, which is one source of deviation from clamped boundary conditions. As the length of the microcantilever becomes shorter, this overlap area causes a larger reduction of the resonance frequency of the microcantilever relative to that for ideal boundary conditions. In spite of these difficulties, a lower-bounds estimate of 90 GPa can be obtained for Young's modulus from the longest microcantilever on the test chip by using the equation for clamped boundary conditions and assuming $\nu = 0.25$ [5]. This value for Young's modulus is 50% less than that reported by Guckel *et al.* [5] for fine-grained undoped polysilicon, but within 10% of that reported by Murarka and Retajczyk [13] for coarse-grained heavily phosphorus-doped polysilicon.

TABLE 2. Microstructure dimensions and measured resonance frequencies

Device type	Length (μm)	Width (μm)	Thickness (μm)	Resonance frequency (Hz)
Cantilever	75	50	1.0	165 827
Cantilever	100	50	1.0	101 502
Bridge	175	50	1.0	210 487
Bridge	200	50	1.0	182 635

The residual strain ϵ in the polysilicon film can be found by measuring the resonance frequency of microbridge structures. Since microbridges are clamped-clamped structures, the residual strain in the microstructure film causes a shift in the resonance frequency of the microbridge in much the same way as increased tension causes a change in pitch of a guitar string. For the compressive strain that is typically found in polysilicon microstructures, the resonance frequency of microbridges is lower than the zero strain case and is given by

$$f_1 = 1.0279 \frac{t}{L^2} \left(1 - 0.147\epsilon \frac{L^2}{t^2} \right) \left(\frac{E}{\rho(1-\nu^2)} \right)^{1/2} \quad (2)$$

Again, the uncertain boundary conditions at the fixed ends of the microstructure make an accurate determination of residual strain in the polysilicon film problematic. Nevertheless, an upper-bounds estimate of 0.002% can be obtained by substituting the estimated plate modulus for polysilicon and using eqn. (2), which assumes clamped boundary conditions. This approach probably overestimates the residual strain, since the entire shift in resonance frequency of the microbridge is attributed to residual strain, when in actual fact a large part of this frequency shift is due to relaxed boundary conditions and a lower value of E . This value of residual strain is as low as any reported results [5, 6], indicating that RTA is a useful strain-relief technique.

4. Conclusions

Microsensors based on resonant sensing elements are a promising area of research. In this paper we have discussed integration for active polysilicon resonant microstructures, emphasizing the important considerations needed to fabricate free-standing polysilicon microstructures with previously-fabricated on-chip nMOS circuitry. In particular, RTA was employed to reduce the high intrinsic compressive strain of the as-deposited

polysilicon and our initial measurements suggest that this technique is a viable alternative to furnace annealing. RTA produces polysilicon films with very low strain (0.002%), at a reduced thermal budget, preserving the high quality of the nMOS circuitry. A composite PSG/CVD SiO₂ sacrificial layer was also developed to permit the fabrication of flat microstructures.

Although these results are very encouraging, further work is clearly needed. In particular, the RTA strain-relief technique was not studied systematically; no effort was made to optimize the anneal times, temperatures or polysilicon deposition parameters. However, our results were quite repeatable in that the extracted mechanical properties of the polysilicon films did not vary significantly through several process cycles. A careful study of RTA on various kinds of polysilicon (i.e., course fine grained, boron/phosphorus doped) is needed before the merits of this process can be fully evaluated. Also, additional circuitry, such as a complete on-chip sustaining amplifier, could be added to the resonant microstructures in cases where this would provide lower cost or improved performance. This additional circuitry could be implemented in a higher-performance circuit technology such as CMOS. Some of the results presented here may be useful for achieving these goals.

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