Process Alternatives and Scaling Limits for High-density Silicon Tactile Imagers

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Abstract

In this paper the process complexities and parasitic substrate coupling effects are compared for several different high-density capacitive tactile imagers. The dissolved-wafer process using diffused bulk-silicon row lines and metal-on-glass columns is found to offer the simplest process and fastest response, requiring only five non-critical masks and producing a settling time for the column charge of about 1 μs. Using this process, a 1024-element array with a force range of 1 gm and a spatial resolution of 500 μm produces a force resolution equivalent to seven bits. Scaled to a 4096-element array, this same process should produce a force resolution of nearly six bits for the same force range and a spatial resolution of 250 μm.

Introduction

Tactile imagers represent one of the most needed devices for precision robotic applications. Although many different approaches have been explored, silicon-based devices remain very attractive due to their potential for high density, high accuracy and low drift. Both piezoresistive and capacitive structures are possible for high-density arrays, each offering a different set of design and performance tradeoffs. For piezoresistive imagers, transducer offset and temperature problems become dominant as element sizes are reduced, whereas for capacitive devices the minimum detectable charge as set by circuit noise limits the resolution of the scaled device [1]. Both piezoresistive and capacitive arrays have been reported for high-density applications [2, 3], representing a contrast between deposited (undercut) and dissolved-wafer (bulk) approaches. Piezoresistive polysilicon arrays over sacrificial layers and capacitive structures based on silicon-to-silicon fusion bonding are some of the variations that might also be used [4, 5]. This paper compares five different capacitive structures and three fabrication processes for implementing high-density tactile imaging arrays and examines their performance. Parasitic coupling effects, which limit readout speed, are analyzed. For a 1024-pixel dissolved-wafer capacitive array, results are presented along with the expected scaling behavior of 4096-pixel arrays.

Overall Structure for High-density Capacitive Tactile Imagers

Figure 1 shows the overall structure for a capacitive tactile imager. An array of force-sensing elements is organized as an $X-Y$ matrix with peripheral circuits for driving voltage on the row lines and detecting the charge induced through the row–column crosspoint capacitors

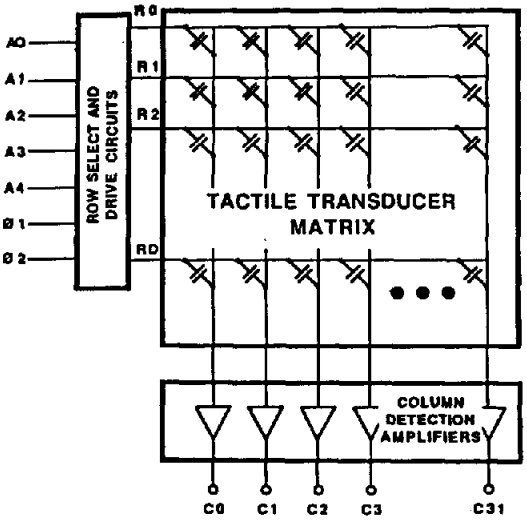

Fig. 1. Overall structure for a high-density capacitive tactile imager.

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onto the columns. The capacitance of these crosspoints is dependent on the local force on the elements. A switched-capacitor readout scheme is implemented to integrate the charge induced on the column as the selected row line is switched in voltage [6]. A force-independent dummy row line is switched using a voltage opposite to that of the selected row so that the net charge induced on the column is proportional to the difference between the selected crosspoint and the dummy capacitances, allowing the zero-pressure capacitance to be subtracted out. The output voltage of the switched capacitor circuit is independent of the parasitic column capacitance so long as the integrator gain is high. Since there are no active circuits within the array area, this configuration allows a higher element density and considerably simpler process than would be possible in active configurations.

Alternative Structures for the Sensing Element

Capacitive tactile imagers can be fabricated using a number of technologies, including the bulk-silicon dissolved-wafer process [3], the undercut process using deposited polysilicon films and the silicon-fusion and etch-back approach. Figure 2 shows cross-sectional views of the resulting structures. Although all these structures can be represented by the equivalent circuit shown in Fig. 3(a), the individual circuit parameters are quite different, resulting in different settling times and degrees of crosstalk between the columns. One of the principal parasitic effects limiting the readout speed of the array is the spurious charge induced in the columns due to the bounce in the substrate voltage as the row voltage is switched. This voltage bounce couples additional charge into the column line through the parasitic column-to-substrate capacitance, C_{CS}. To estimate these coupling effects, the circuit simulation program SPICE PLUS was implemented for 8 × 8-element

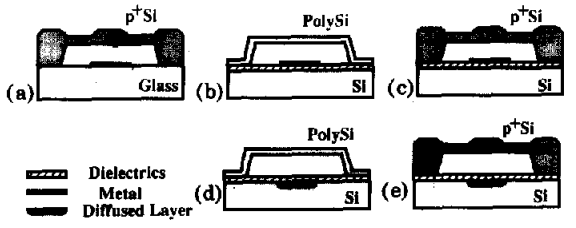

Fig. 2. Different structures for capacitor-based tactile imagers. (a) Dissolved wafer and electrostatic bonding, p^+ Si-to-metal on glass; (b) poly Si-to-metal on Si; (c) p^+ Si-to-metal on Si; (d) poly Si-to-diffused layer in Si; (e) p^+ Si-to-diffused layer in Si.

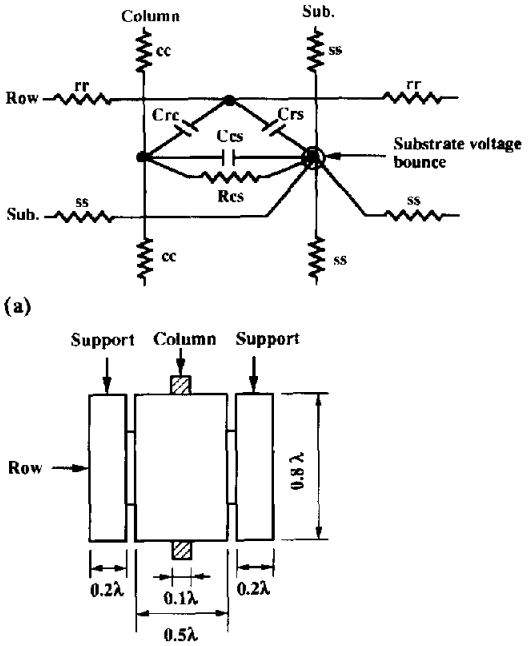

Fig. 3. (a) Equivalent circuit for a single element of a tactile imager. R_{cs} is included to aid d.c. convergence. Resistance: p^+, 2 Ω/□; diffused layer, 7 Ω/□; metal, 0.03 Ω/□; polysilicon, 70 Ω/□. Capacitance: diffused layer, 0.5×10^{-4} pF/μm^2 (area); 5×10^{-4} pF/μm (periphery). (b) Dimensions for a single tactile cell used with the parameters in Table 1. λ indicates spacing between elements. Separation gap, 2.3 μm above silicon surface; thickness, SiO_2 0.5 μm, metal 0.3 μm.

arrays for each of the structures shown in Fig. 2. The equivalent model parameters for each structure are listed in Table 1, where λ is the overall element (pixel) size as shown in Fig. 3(b). Figure 4 shows the transient substrate bounce voltages at a location farthest from the substrate ground for different structures when a 10 V voltage excursion is applied into the row line in 30 ns. For the structures with diffused silicon column lines (Figs. 2(d) and (e)), the substrate response is relatively slow due to the substrate resistance and the large parasitic row–substrate capacitance. The responses for the metal-on-dielectric column structures in (b) and (c) are more rapid. The substrate bounce voltage decreases more rapidly for the p^+ silicon row line and metal column in Fig. 2(c) than for the poly row line in (b) due to the lower resistance of the diffused bulk row line. Since the charge induced onto the column lines is the product of the substrate bounce voltage and the distributed column–substrate capacitance, and since this capacitance is large for all of these structures, the

TABLE 1. Parameters in the equivalent circuit, shown in Fig. 3(a), for the different capacitor-based tactile imagers of Fig. 2. Substrate resistance values are selected as low as possible to suppress the substrate coupling effects

	(a)	(b)	(c)	(d)	(e)
C_{rc} [pF]	$1.8 \times 10^{-6}\lambda^2$	$1.8 \times 10^{-6}\lambda^2$	$1.8 \times 10^{-6}\lambda^2$	$1.5 \times 10^{-6}\lambda^2$	$1.5 \times 10^{-6}\lambda^2$
C_{rs} pF]	0	$2.3 \times 10^{-5}\lambda^2$	$2.3 \times 10^{-5}\lambda^2$	$2.3 \times 10^{-5}\lambda^2$	$2.3 \times 10^{-5}\lambda^2$
C_{cs} [pF]	0	$2.8 \times 10^{-5}\lambda^2$	$2.8 \times 10^{-5}\lambda^2$	$2 \times 10^{-5}\lambda^2$ $+1.3 \times 10^{-3}\lambda$	$2 \times 10^{-5}\lambda^2$ $+1.3 \times 10^{-3}\lambda$
rr [Ω]	2	70	2	70	2
cc [Ω]	0.06	0.06	0.06	14	14
ss [Ω]	10^{12}	10	10	100	100
R_{cs} [Ω]	(10^{12})	(10^{12})	(10^{12})	(10^{12})	(10^{12})

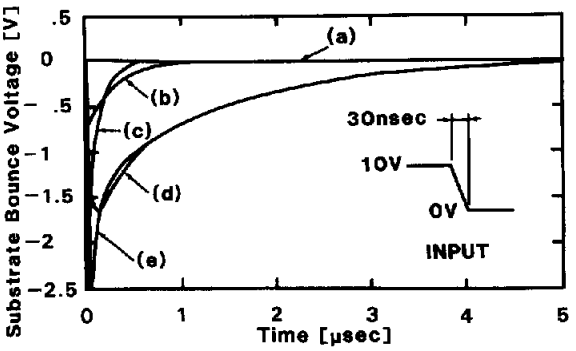

Fig. 4. Substrate voltage bounce for an 8 × 8-element array ($\lambda = 2$ mm) using the different structures shown in Fig. 3.

induced charge is still very significant at 1 μs. Even for the structure in Fig. 2(c), the substrate-induced noise charge resulting from substrate bounce is still approximately 1 pC for an eight-pixel column and $\lambda = 2$ mm. It is important that this charge does not overload the integration amplifiers or readout integrity will be lost. As the number of elements increases, a longer time is required for these coupling effects to subside due to the increase in the parasitic capacitance as compared to the transducer capacitance. For the structure in Fig. 2(a), the substrate voltage bounce is negligible due to the almost perfect isolation of the glass substrate, resulting in a very fast response.

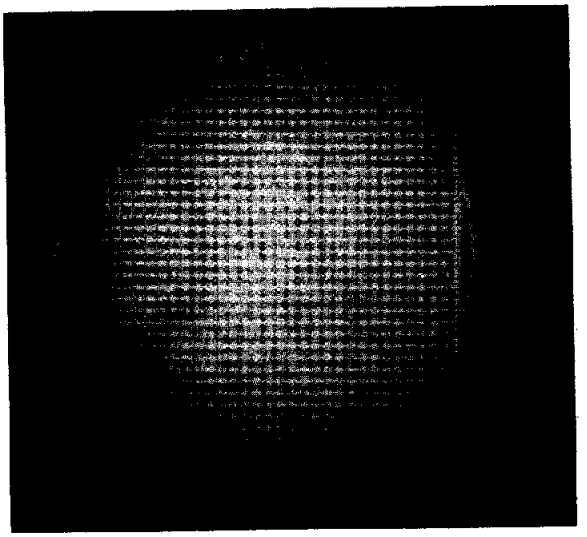

Fig. 5. A completed 32 × 32-element tactile imager shown on a U.S. Lincoln cent [3].

Table 2 compares these capacitive structures in terms of their process complexity and design flexibility. The dissolved-wafer process offers the simplest process, has very high yield and can provide the resolution and sensitivity required for a wide variety of applications. A 1024-element imager based on this process has been fabricated [3] and is shown in Fig. 5. The glass substrate measures 2.2 cm × 2.0 cm and is shown on a Lincoln penny.

TABLE 2. Comparison of dissolved wafer, undercut polysilicon and silicon–silicon bonding techniques for the fabrication of tactile imagers

Item	Dissolved wafer	Undercut polysilicon	Silicon–silicon fusion
Number of masks	3(2)/4(2)	4/5 for (*b*), 5/6 for (*d*)	3(2)/4(2) for (*c*), 3(3)/4(3) for (*e*)
Process complexity	Simple	Moderate/high	Moderate
Process sensitivity	Low	High	Moderate
Uniformity	Good	Good	Moderate/good
Yield	High	High/moderate	High/moderate
Sensing type	Capacitive	Capacitive/resistive	Capacitive/resistive
Sensitivity	High	High	High
Parasitics	Low	Moderate/high	Moderate/high
Circuit compatibility	No (Hybrid)	Yes	Yes
Upward scalability	Good	Moderate/low	Good

The imager utilizes a doubly-supported bridge structure that offers flexibility in setting the force sensitivity and the operating force range and lends itself easily to high-density arrays. The use of hybrid flip-chip circuits on the glass for multiplexed drive and readout appears to be an attractive alternative to monolithic circuits for this application due to the very large array size and the need for a simple array process.

Packaging Effects and Scaling Behavior

In use, the tactile imager of Fig. 2(a) is coated with a thin metallized pad. This pad electrically insulates the row lines from the external world and seals the areas under the transducing bridges from particulates. Parasitic coupling might also occur through this pad; however, simulations for pad thicknesses from 1 μm to 10 μm have shown the voltage bounce and induced column charge due to the presence of the pad to be negligible.

Since the crosspoint capacitance decreases rapidly with the dimensions, scaling the array to higher pixel densities to achieve higher spatial resolution results in decreased force resolution. The scaling limit for a given desired force range is thus determined by the minimum detectable charge, as set by the various readout noise sources (thermal noise, noise due to charge leakage, temperature drift, and reset noise charge [6]). For the 32 × 32-element array shown in Fig. 5, the minimum detectable charge is about 19 fC. Table 3 shows the scaling behavior of this capacitive tactile imager, based on the doubly-supported bridge structure [3]. A full-scale force range of 1 gm is assumed, at which point the zero force capacitance is designed to have doubled. Even for a 64 × 64-element array (4096 pixels), a force resolution of nearly 6 bits is achieved with a spatial resolution of 250 μm.

TABLE 3. Scaling behavior for a high-density tactile imager fabricated by the dissolved wafer technique

Element number	16 × 16	32 × 32	64 × 64
Cell spacing [mm]	1	0.5	0.25
Thin beam [μm^3]	600 × 268 × 4.8	300 × 134 × 3	150 × 67 × 1.9
Thick center plate [μm^3]	826 × 506 × 12	413 × 253 × 12	206 × 126 × 12
Plate separation [μm]	2	2	2
Zero force capacitance [fF]	1248	312	78
Force range [gF]	1	1	1
Terminal sensitivity [fF/gf]	1248	312	78
Min. detectable charge [fC]	33	19	15
Resolution [bit]	9	7	6

Conclusions

Several structures for implementing silicon capacitive high-density tactile imagers have been examined. The dissolved-wafer process using diffused bulk silicon row lines and metal-on-glass columns offers the fastest response, simplest process and greatest design flexibility. The element response to force is highly independent of the overlying pad, which acts only to transmit force to the transducing bridge structures and seal them from the external world. While the present 1024-element arrays have been implemented using off-chip discrete electronics, the use of hybrid circuitry on the glass should minimize interconnects and simplify imager fabrication for a wide variety of important high-precision applications.

Acknowledgements

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