A high-performance microflowmeter with built-in self test

Steve T Cho and Kensall D Wise

Center for Integrated Sensors and Circuits, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122 (USA)

(Received January 14, 1992, in revised form July 23, 1992, accepted July 27, 1992)

Abstract

This paper reports the development of a high-performance readout scheme based on a switched-capacitor circuit and intended for use with an ultrasensitive microflowmeter The microflow transducer improves significantly on the resolution of current flow devices and uses a differential capacitive pressure sensor to measure the flow The readout electronics feature a clocking speed of 100 kHz and can drive loads as high as 35 pF The high d c gain of the circuit topology (75 dB) is relatively insensitive to stray input capacitance and is ideally suited for a multichip sensor realization The uncompensated linearity of the overall readout circuit is 10 bits and the pressure/flow resolution is 12 bits Since ultrasensitive membranes respond to electrostatic forces, the output is characterized as a function of the duty cycle and pulse width of the readout clocking waveforms The membrane does not respond to these waveforms for high frequencies (> 50 kHz), but for lower frequencies the diaphragm deflects in response to the time-average voltage applied across the device A self-test mode can therefore be implemented simply by changing the duty cycle of this pulse By modifying the amplitude of the waveform, the device can be autocalibrated over a limited pressure range The transducer and circuitry have been integrated into a flow package, and the multichip device has been tested versus a calibrated gas flow

Introduction

Lack of resolution for very low flow rates is a major limitation for present flow devices For low-pressure semiconductor process applications, such as molecular beam epitaxy (MBE), low-pressure chemical vapor deposition (LPCVD), and reactive ion etching (RIE), there is a need to extend the sensitivity of flow measurements further into the sub-standard cubic centimeter per minute (SCCM) range We recently reported an ultrasensitive pressure-based microflowmeter [1, 2] which resolves 10^{-8} SCCM (nearly five orders of magnitude lower than commercial flowmeters), has a dynamic range extending over five orders of magnitude, and has a resolution exceeding 16 bits Although the transducer performance has been characterized, the issues related to the electronic readout of this ultrasensitive device have yet to be addressed This paper reports a custom CMOS readout circuit for this sensor as well as the overall performance for the flowmeter operating in an application environment The circuitry is challenging due to the high resolution of the transducer itself and the problems caused by the electrostatic forces generated during readout of its capacitive pressure sensor The circuitry has an accuracy of more than 10 bits and implements built-in self-testing It interfaces directly with a standardized digital bus interface for communication with the host process controller

Transducer and circuit operation

The transducer was fabricated using a previously reported single-sided dissolved wafer process [2], which uses silicon micromachining and diffused boron etch-stops to define the transducer structure Figure 1 shows a cross section of the microflowmeter and Fig 2 shows a three-dimensional view of the device Gas flows into the transducer through an inlet port at pressure $P1$ The gas then enters a flow channel and leaves the structure through an outlet port at pressure $P2$ If the channel is small enough to create a resistance to the flow, a pressure drop ($P1 - P2$) takes place across the channel The flow rate is the channel conductance multiplied by this pressure difference The pressure difference is measured by a capacitive pressure sensor, which is composed of a thin stress-compensated p^{++} boron-doped silicon membrane suspended above a metal plate [2] The

0924-4247/93/$6 00

© 1993 — Elsevier Sequoia All rights reserved

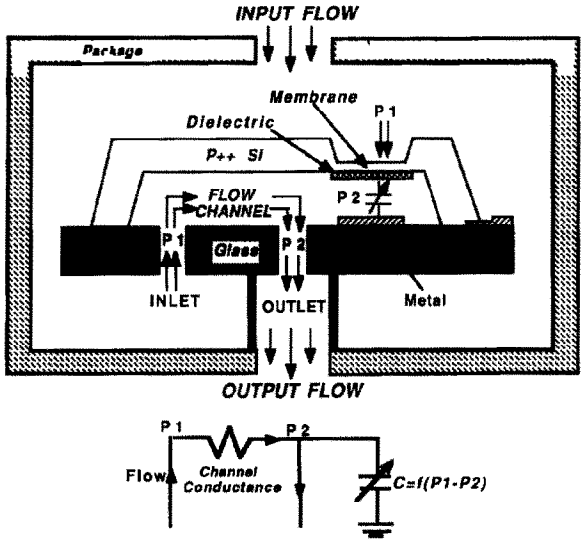


Fig 1 Cross section of the microflowmeter

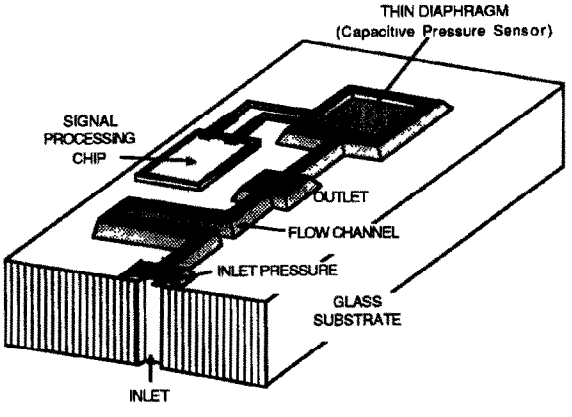


Fig 2 A three-dimensional view of an ultrasensitive microflowmeter The flowmeter is realized by extending the cavity of a capacitive pressure sensor to form an on-chip flow channel

pressure above the diaphragm and the pressure at the inlet ($P1$) are kept equal by the package used for the sensor, which also isolates the outlet port from the inlet By reading the capacitance, the pressure difference and subsequently the flow can be determined A fabricated transducer is shown in Fig 3

The pressure transducer can resolve pressures as low as 1 mTorr for 1 fF change in capacitance and has a pressure sensitivity of about 200 ppm/mTorr, the capacitance versus pressure response for small deflections is shown in Fig 4(a) The full-scale (FS) range of capacitive pressure sensors is typically defined to be the pressure required for a capacitance change equal to the zero-pressure

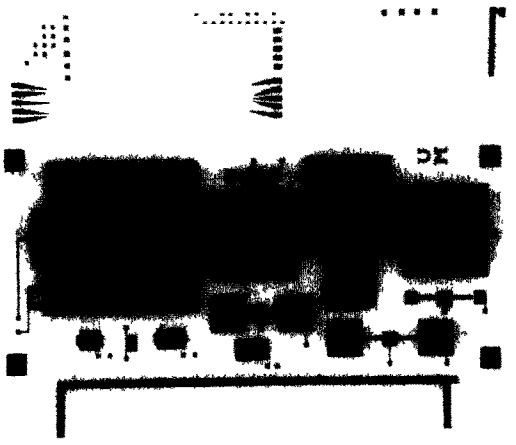
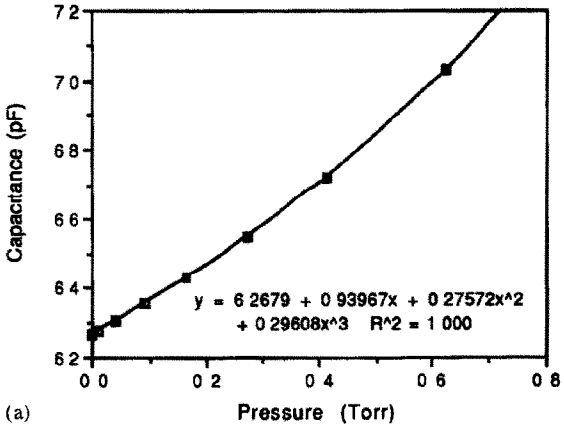
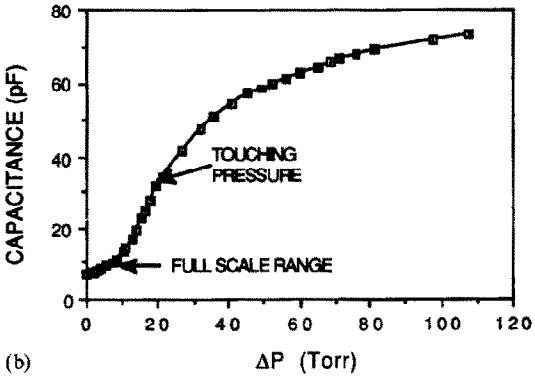


Fig 3 A fabricated ultrasensitive microflow sensor The chip measures 9 7 mm × 3 mm



(a)



(b)

Fig 4 Capacitance vs pressure response of an ultrasensitive capacitive pressure sensor (a) Small-deflection membrane response The linear pressure sensitivity is about 1 fF/mTorr (b) Full-range response The full-scale range has been extended by over an order of magnitude

capacitance ($\Delta C = C_0$), for this device it is about 4 Torr However, overpressure tests (creep, fatigue) conducted at approximately 20 times the full-scale range of these devices indicate that it should be possible to extend the range of operation by over an order of magnitude beyond full scale [3] During these tests, the change in zero-pressure offset was <0 2% FS and the change in pressure sensitivity was <0 030 fF/mTorr Furthermore, the change in hysteresis was <0 2% FS Since most of the hysteresis is observed at higher pressures and since the change in sensitivity is nearly two orders of magnitude below the minimum pressure sensitivity, these effects do not necessarily limit the resolution (the minimum increment that can be resolved with respect to the full dynamic range) of the device However, at high pressures in the linear range, the sensitivity change can limit the accuracy (the precision of the absolute measurement) to about 0 2% Therefore, the accuracy of the transducer is limited to 9–10 bits and the resolution is limited to 14–15 bits

A typical capacitance versus pressure response is shown in Fig 4(b) At approximately twice the full-scale pressure, the membrane touches the bottom metal plate, and for still higher pressures, it spreads out against this plate The glass acts as an overpressure stop to prevent the membrane from rupturing, and the membrane is coated with a dielectric to prevent the plates from shorting together During operation above this touching point, no tendency for the plates to adhere to one another when the pressure is reduced has been observed, however, it should be noted that the large overpressures were created by generating a vacuum in the cavity of the capacitive pressure sensor It is possible that under a more viscous ambient, plate adhesion could be an issue in device accuracy and/or reliability

Since the transducer is capacitive, the capacitance variation with pressure must be converted into a usable electrical signal in order to relay the signal off-chip The two most common readout circuits for capacitive transducers are relaxation oscillators [4–6] and switched-capacitor integrators [7, 8] Relaxation oscillators work on the principle that capacitors are energy-storage elements with charging time constants that are a function of their capacitive value Very high resolution (>10 bits), low pin count, and low power dissipation are major advantages to this technique However, relaxation

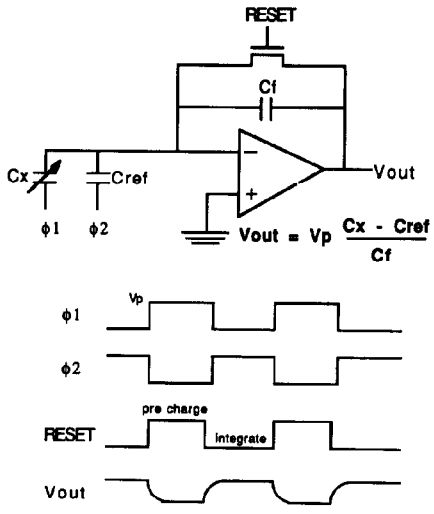


Fig 5 A switched-capacitor integrator for the measurement of capacitance

oscillators also have high temperature sensitivity and typically slow measurement time (>0 1 ms) Switched-capacitor circuits are based on converting a charge difference into a voltage using an integrator A switched-capacitor circuit, shown in Fig 5, was chosen for this application due to its low sensitivity to parasitics and temperature and its high speed During the pre-charge pulse, the transducer capacitor (C_x) is charged up and the output is set to ground As the RESET switch goes low (the integration cycle), the charge difference between a reference capacitor (C_{ref}) and the transducer (C_x) is converted to a voltage The output is given by

$$V_{out} = V_p \frac{(C_x - C_{ref})}{C_f} \tag{1}$$

where V_p is the amplitude of the input clock waveforms and C_f is the integration capacitor If the open-loop gain of the operational amplifier (op amp) is high, the circuit is insensitive to input parasitic capacitance (C_{ps}) and temperature effects and is well suited for a multichip hybrid implementation on glass

Readout performance

Measured performance

The switched-capacitor circuit comprises three elements the clocks, the reset switch, and the op amp Since the operating frequency range of the

circuit was not known initially, the clocks were generated off chip An important concern in switched-capacitor circuits is 'feedthrough error voltage' or 'reset noise voltage' [9] When the gate signal across the switch goes from high to low (i e , from pre-change to integration), the charge built up across the gate during the pre-charge can be injected into the negative input of the op amp and create offset errors Although there are elaborate techniques to cancel out this effect [9], a simple digital switch (an n- and p-channel transistor tied together in parallel) is sufficient to reduce this offset significantly Instead of building charge across the gate, the p-type transistor effectively acts as a dummy capacitor to provide an equal and opposite charge to cancel out the offset charge

The most important element in the readout scheme is the operational amplifier In general, most high-performance op amps are sufficient for this application A schematic of the op amp is shown in Fig 6 There are basically four parts to the op amp a bias string (transistors M8–M10), the input stage (transistors M1–M5), the output stage (M6, M7) and the compensation stage (M11, M12 and capacitor C_c) The bias string sets the gate of transistor M8 to a constant voltage, this effectively sets transistors M5, M11, and M7 as current sources The input stage is a CMOS differential amplifier which performs the differential to single-ended conversion The output stage is a source-follower configuration which defines the output voltage swing and the supplies charging currents for the load capacitance (C_L) The compensation stage provides internal phase compensation to minimize the oscillation on the output, the configuration for this stage uses a source-follower feedback to the input stage If the compensation capacitor (C_c) is directly connected to the integration capacitor (C_f), then an error charge can be injected into C_c in the same manner that clock feedthrough occurs with the reset switch The source-follower scheme isolates the compensation capacitor from the integrating capacitor in order to eliminate this feedthrough The op amp features a settling time of 2 6 μs for a 35 pF load and an open-loop gain of 75 dB, the output range is from −4 8 to 4 8 V for ±5 V supplies The circuitry was designed and fabricated using a standard single-metal double-poly p-well CMOS process with a minimum feature size of 3 μm The readout chip is shown in Fig 7 and the die dimensions are 0 68 mm × 0 9 mm

In evaluating the performance of the circuit, there are three areas to consider (i) the minimum resolution, (ii) the frequency range of the transducer for a read operation, and (iii) the implementation of the self-test/autocalibration mode In order to determine the resolution and accuracy of the readout circuit, the output voltage versus a known input capacitance must be characterized Ceramic capacitors accurate to 10 bits were used as input capacitors The amplitude of all waveforms was 5 V and the output voltage response was measured using a HP54110D Digitizing Oscilloscope with an accuracy of 1–20 mV, depending on the voltage scale An output waveform is shown in Fig 8, and the output voltage is shown as a function of the variable capacitance (C_x) in

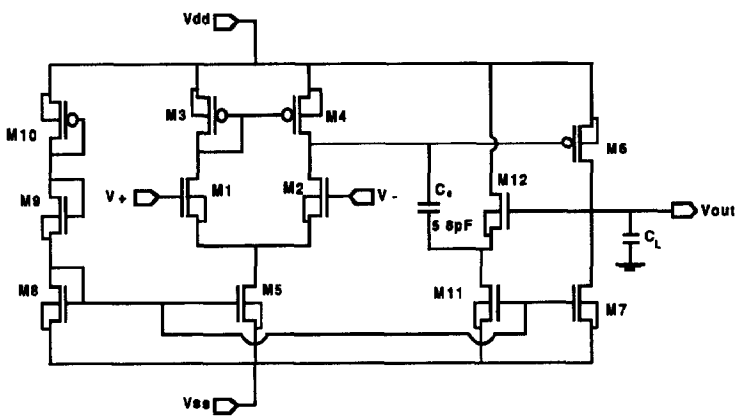


Fig 6 Topology for a high-performance CMOS operational amplifier This op amp features an open-loop gain of 75 dB, a settling time of 5 μs and an output voltage range of −4 8 to 4 8 V

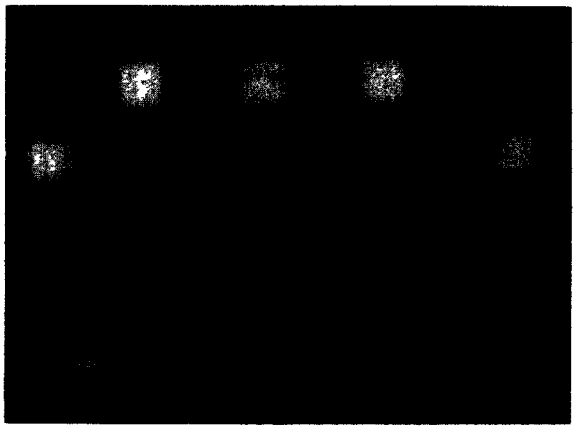


Fig 7 A fully integrated switched-capacitor readout circuit The chip dimensions are 0 68 mm × 0 9 mm

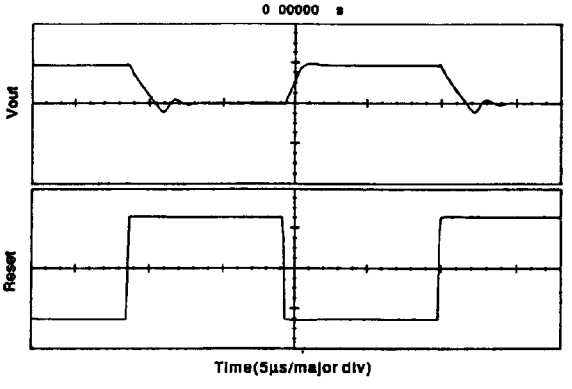


Fig 8 Output waveform for switched-capacitor operation The maximum clocking frequency is 100 kHz The reset waveform has a magnitude of 5 V and the magnitude of the output voltage is 1 9 V The x-axis has 5 µs per major division

Fig 9 The minimum integrating pulse width is limited by the settling time of the output waveform (3–5 µs), giving an equivalent maximum sampling (readout) rate of about 100 kHz Although 1 mV changes in the output are resolvable, the uncompensated linearity of the overall circuit is 10 bits (4 mV) However, since the input capacitors and the oscilloscope are also accurate only to about 10 bits, it is expected that the actual circuit performance is higher This measured performance is summarized in Table 1

A unique feature of the transducer structure is the membrane sensitivity to electrostatic force During the read operation, the voltages applied across the transducer capacitor can perturb the output response In order to evaluate these effects, the transducer was connected to the readout circuitry by aluminum wire bonds and was tested

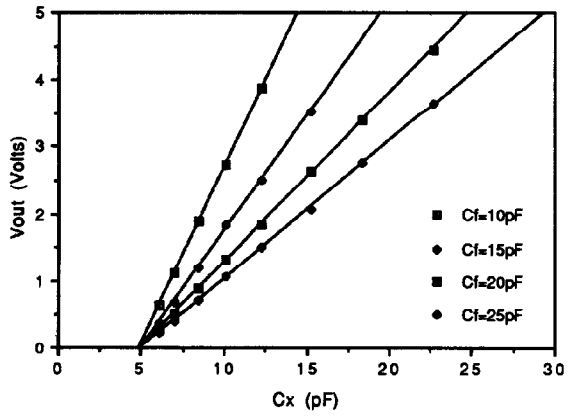


Fig 9 Output voltage vs varying capacitance The output is linear to within 10 bits and the linearity is independent of the value of the integration capacitor

TABLE 1 Performance of the switched-capacitor circuit

Open-loop gain	75 dB
0 1% settling time	2 6 µs
Output range	−4 8 to 4 8 V
Minimum detectable signal	1 mV (1 mTorr)
Linearity	> 10 bits
Power	1 56 mW
Supply voltage	±5 V

under zero-differential-pressure conditions Using a 50% duty cycle and an integration capacitor of 20 pF, the output was measured as a function of the input clock pulse width, the response is shown in Fig 10 For pulse widths greater than 10 µs, there is evidence of a slight membrane deflection (2 mV or an 8 fF change) due to the equivalent

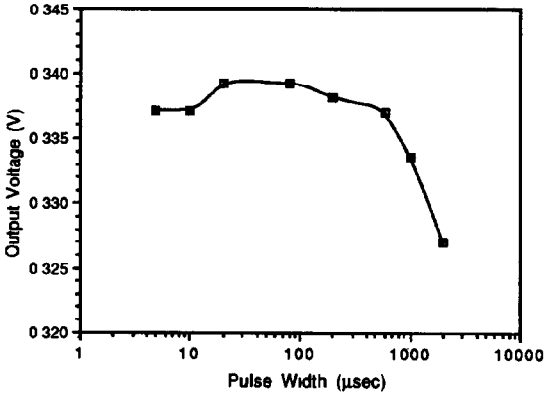


Fig 10 Output voltage vs integration pulse width The duty cycle of the measurement is 50% The voltage increases slightly (2 mV) with increasing pulse width, but the voltage decays with longer pulse widths due to leakage

force generated by the time-average voltage of the waveform In effect, this time-average voltage acts as a d c force across the plates However, an electrostatic force of 2 5 V should generate an equivalent pressure of 13 mTorr (or 13 fF) This corresponds to an error in the output voltage of 1 2 mV, which is within the error limits of the measurements (2 mV) If the pulse width is increased above 100 μs, the output voltage decreases This indicates that the junction leakage current of the reset switches is perturbing the output The measured voltage dropped 12 mV in approximately 2 ms, which gives a leakage current of 120 pA and a corresponding bulk lifetime of about 100 ns Therefore, to ensure a voltage drop of no more than 1 mV, the maximum integration time should be no more than 167 μs (corresponding to a minimum clock frequency of 3 kHz)

If the clock pulse width is <10 μs (still at 50% duty cycle), there is no evidence that any deflection due to electrostatic force takes place, even though the time-average applied transducer voltage is 2 5 V This is analogous to the RC circuit when the time constant is much larger than the pulse width of the applied voltage the change in the output is not significant In the same way that system functions are invisible to signals at certain frequencies, the membrane becomes transparent to the read waveform if the frequency is high enough The fundamental natural oscillation frequency of a square, homogeneous diaphragm is given by [11]

$$f_0 = \frac{Kh}{8\pi a^2}\left[\frac{gE}{12(1-\nu^2)\rho}\right]^{1/2} \tag{2}$$

where K is the mode factor from the Rayleigh–Ritz energy method, g is the acceleration due to gravity, and ρ is the density of the material Setting $K = 35\ 99$ [11] and inserting the other constants, the calculated resonance frequency is approximately 11 kHz, which is an order of magnitude less than the typical clocking speed

Since calibrated pressure signals can be generated electrostatically, this signal can be used to self-test the pressure sensitivity of the device The basic idea behind self-testing is that by measuring the response of the membrane to a constant calibrated pressure, the device sensitivity and drift can be monitored over time The pressure generated by the electrostatic voltage (ΔP) is given by

$$\Delta P = C^2 V_a^2 / 2\varepsilon A^2 \tag{3}$$

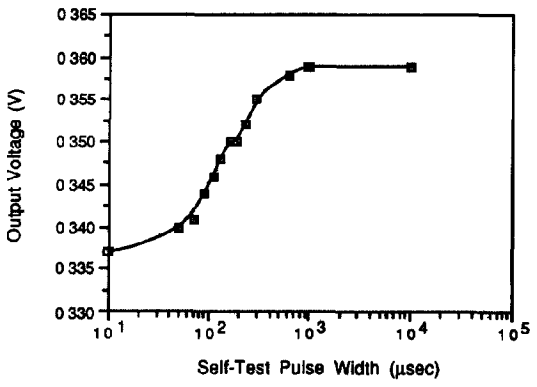


Fig 11 Output voltage vs self-test pulse width The output voltage saturates for a self-test pulse width of 0 7 ms

where C is the capacitance in response to the self-test pulse, V_a is the applied voltage, and A is the area of the capacitor plate, ΔP is the change in pressure with respect to zero pressure Since the capacitance is measured externally and if the 5 V self-test signal does not cause the membrane to pull in or collapse, ΔP can be precisely determined, independent of the operating pressure Since both ΔC ($=C - C_0$) and ΔP are known, the pressure sensitivity about the self-test pressure can be measured

If the pre-charge pulse width is much greater than the integration pulse, than a direct voltage is set up across the diaphragm, which can be used as a self-test signal The integration pulse was set to 10 μs and the pre-charge pulse width was varied The output response versus pulse width is shown in Fig 11 At approximately 0 7 ms, the output voltage saturates, indicating that this is the maximum deflection for the membrane The total voltage change is 22 mV, which gives an equivalent pressure of 87 mTorr, this output waveform is shown in Fig 12 A direct voltage of 5 V generates a theoretical pressure of 85 mTorr, thus, there is good agreement between the response of the self-test signal and the equivalent force that is generated If the amplitude (V_a) of the waveform is varied, then the capacitance versus a range of pressures can be measured In effect, the circuitry can perform an electrostatic self-calibration

Performance limitations

Full-scale range

In order to understand which mechanisms ultimately determine the full-scale range, accuracy,

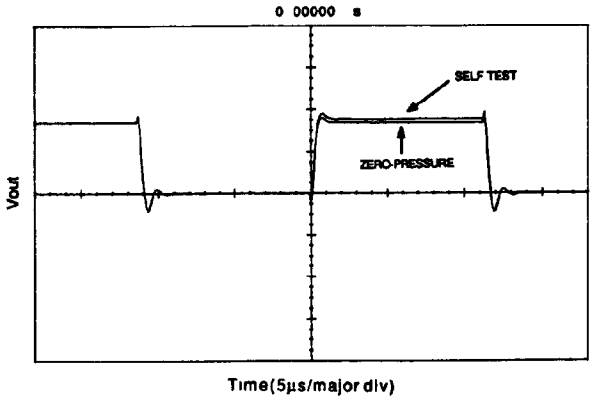


Fig 12 Output waveform for a self-test operation The self-test signal is 22 mV greater than the zero-pressure output voltage

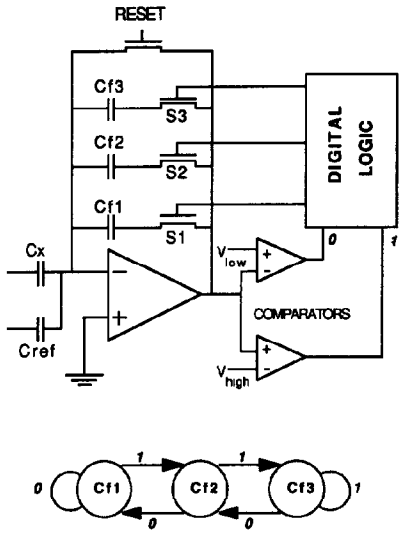


Fig 13 A circuit for increasing the dynamic range over five orders of magnitude for a switched-capacitor operation

resolution, and temperature sensitivity of the sensor, the performance limitations of both the transducer and readout circuit have been characterized The full-scale range of the sensor is limited by the circuitry The extended range of the capacitive transducer itself covers over five orders of magnitude (16 bits), with a maximum capacitance change of approximately 100 pF Assuming that the circuit output voltage resolution is approximately 1 mV, the output range of the readout electronics is about 12 bits (greater than three orders of magnitude), which is more than an order of magnitude less than that of the transducer Although the integration capacitor can be increased to accommodate larger capacitances, the resolution of very small capacitance changes would then be lost However, using multiple integration capacitors that are autoranging, the range of the circuitry can be extended to approach that of the transducer, a schematic of this circuit is shown in Fig 13 The circuit operation is fairly straightforward Three different integration capacitors ($C_{f1} = 5\,0$ pF, $C_{f2} = 50\,0$ pF, $C_{f3} = 150$ pF) can be implemented by the circuit, depending on the state chosen by the digital logic This digital logic is basically a finite state machine (FSM), which switches states according to the input from two comparators This FSM can be designed with simple digital gates or with flip flops When the state logic selects an integration capacitor, the switch in series with the capacitor (S1, S2, or S3) goes high while the other two switches stay low The transition diagram for the state machine is also shown in Fig 13 When the voltage level is too large for a particular integrating capacitor ($>4\,5$ V), logic 1 goes high and the state machine switches to the next highest valued capacitor If the voltage level falls too low ($<0\,5$ V), logic 0 goes high, and the state machine switches to the next lowest integrating capacitor For $C_{f1} = 5\,0$ pF, 1 fF or 1 mTorr is resolvable, for $C_{f3} = 150$ pF, 100 pF can be measured Therefore, this circuit can measure capacitance changes over five orders of magnitude

Accuracy and resolution

Since the accuracy of the circuitry is approximately 10–12 bits, the accuracy of the overall sensor is limited by that of the transducer (9–10 bits) [12] In terms of resolution, the transducer can resolve 1 part in 100 000 (>16 bits), while the circuitry can resolve about 12 bits The limits on the resolution are defined by (i) the minimum detectable signal charge, (ii) interconnect noise, and (iii) the parasitic capacitance The minimum detectable signal charge is essentially determined by the noise in the circuitry The principal noise mechanisms that affect the circuit performance are Johnson (or thermal) noise in the switches, reset charge injection at the input (or feedthrough error voltage), and leakage charge The total noise charge due to these mechanisms is approximately $2\,5 \times 10^{-15}$ C here [7, 13] The noise signal in volts is given by the error charge divided by the integration capacitance, therefore, the minimum detectable voltage is approximately 100 μV and

the expected resolution of the circuit is 15 bits Circuit techniques such as correlated double sampling can remove the noise components associated with the reset switch This approach theoretically reduces the noise associated with the reset charge and low-frequency Johnson noise by at least an order of magnitude With these mecahnisms eliminated, the principal remaining noise mechanism is leakage charge, and the expected circuit resolution should be increased to at least 16 bits

Another noise mechanism that can have a large effect on the circuit performance is the thermal noise in the interconnect The interconnect for one plate of the on-chip reference capacitors is a long polysilicon line This interconnect lead has a resistance of about 1 kΩ, which introduces noise into the measurement of the capacitance On an *LCR* meter, the thermal noise translates into a capacitive variation of 20 fF, which could account for the 4 mV non-linearity seen in the circuit output response This problem could be resolved by using micromachined capacitors (the interconnect resistance is only 30 Ω) or by using metal as the interconnect material

In evaluating the noise sources, the present resolution of the readout electronics is limited by the thermal noise in the on-chip reference capacitor interconnect and by the parasitic input capacitance The theoretical error introduced by the parasitic capacitance is given by [7]

$$\varepsilon(\%) = \left(\frac{1}{A_0} + \frac{C_x - C_{ref}}{A_0 C_f} + \frac{C_{ps}}{A_0 C_f}\right)100\% \qquad (4)$$

where A_0 is the d c gain and C_{ps} is the parasitic capacitance For a d c gain of 75 dB, an error of 0 03% (12 bits) is introduced into the measurement In order to achieve a resolution of 16 bits, a gain of 96 dB is required High-gain architectures (cascode or BiCMOS amplifiers) can offer open-loop gains at this level Although it is theoretically possible to obtain 14–16 bits of resolution and accuracy with the readout electronics, this is very difficult to achieve In order to realize 16 bits of accuracy, the voltage generators must have noise levels and accuracies on the order of 16 bits as well Most power supplies are stable to 10 mV, however, a 10 mV error on a 5 V supply would translate to an accuracy of only nine bits Thus, from a practical point of view, it is not the circuitry that is the limiting factor, but the instrumentation used with the circuit, at least at present

Temperature sensitivity

In evaluating the temperature sensitivity of the multichip sensor, the operation of the op amp, transducer, and reset switches must be taken into consideration A major advantage of the switched-capacitor readout technique is that the main circuit element is an op amp Op amps typically have low temperature sensitivity, and SPICE simulation results for the present op amp design operating at 100 °C show a decrease in the open-loop gain of only −0 8 dB, no change in output voltage range or settling time, and an offset shift of only 50 μV (compared with results at 23 °C) Due to the temperature dependence of the internal membrane stress, the pressure sensitivity of the transducer decreases by 30% over this range [3], but the overall sensor resolution is decreased by 1–2 bits For the readout electronics, the main circuit elements affected by temperature variations are the switches Leakage currents are very sensitive to temperature since the intrinsic carrier concentration is a strong function of temperature The junction leakage current can potentially double every 10 °C [13] For an integration period of 5 μs (corresponding to a clocking frequency of 100 kHz), the corresponding voltage drop would be 4 mV at 100 °C This ΔV would limit the resolution and accuracy of the circuit to 10 bits However, it should be noted that with more advanced CMOS processes, the leakage current can be reduced by as much as an order of magnitude below the present values

Flow characterization

In order to characterize the flow response of the multichip microflowmeter, a calibrated gas flow was applied to the sensor Since the flow range of the device is orders of magnitude below conventional calibrated flow ranges, an external flow channel was placed in parallel with the on-chip microchannel This external bypass tube was 2 mm in diameter and 23 5 cm long The response of the induced pressure drop generated by nitrogen gas flow is shown in Fig 14 The output is linear, which is in agreement with theory, and the slope of the line is equal to the channel conductance The measured channel conductance is $4\,72 \times 10^5$ cm^3/min The simplest theoretical solution for conductance through a long straight tube can be calculated from Poiseuille flow [14]

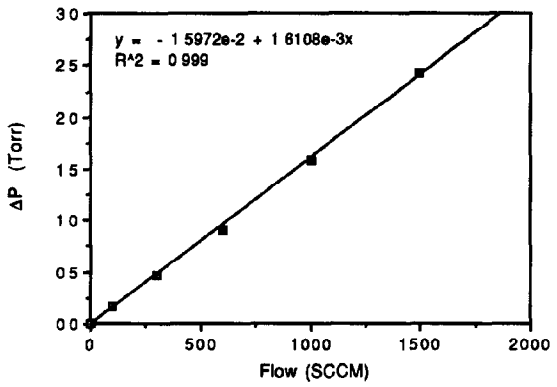


Fig 14 The pressure response of a hybrid ultrasensitive microflowmeter to an applied calibrated N_2 gas flow The channel conductance is $4\,72 \times 10^5$ cm^3/min

$$G_p = \frac{\pi d^4}{128\eta l}\frac{(P1 + P2)}{2} \quad (5)$$

where G_p is the channel conductance, d is the diameter of the pipe, η is the gas viscosity, l is the length of the tube and $(P1 + P2)/2$ is the average pressure across the inlet and outlet of the tube The calculated conductance is $5\,93 \times 10^5$ cm^3/min, therefore, the agreement between the theoretical and measured values is about 20% The main source of error in this calculation is probably due to the measurement of the diameter (this term is to the fourth power), the diameter was measured with an accuracy of 0 1 mm

Conclusions

At high-performance readout scheme for an ultrasensitive microflowmeter with a capacitive output has been presented The main circuit element is an op amp which features a d c gain of 75 dB and a 2 6 μs (100 kHz) settling time for a 35 pF load The high gain of the op amp cancels out the stray input capacitance The uncompensated linearity of the overall circuit is at least 10 bits and the minimum resolution is 1 mV for a 5 V full-scale output The output as a function of duty cycle and pulse width for a 50% duty cycle input clock was characterized The membrane does not respond to high frequencies (> 50 kHz), but does deflect in response to the time-average voltage applied to the device A unique feature of this circuit is that a self-test mode can be implemented simply by changing the duty cycle of the input clock pulse, if the amplitude of this waveform is varied, an electrostatic autocalibration can also be performed

The theoretical performance limits of the transducer integrated with the readout electronics were also discussed The full-scale range of the sensor is limited by the circuitry to 12 bits, although circuit techniques can be used to increase the range to 16 bits The maximum theoretical resolution and accuracy of the circuit are approximately 14–16 bits, however, the precision of the off-chip instrumentation ultimately determines the performance The accuracy and resolution of the device at 100 °C are limited to 10 bits due to leakage currents in the reset switches The transducer and circuitry were integrated into a flow package and the multichip device was tested with a calibrated flow The microflowmeter is currently being installed on an Applied Materials 8300 RIE where it is being applied to the development of automated micromachining processes for application in sensors and VLSI

Acknowledgements

The authors would like to thank Dr Khalil Najafi for his significant contributions to the various parts of this program and Dr Jin Ji and Mr Howard Goldberg for their assistance in the design and fabrication of the circuitry The financial support provided by the Semiconductor Research Corporation for this work is also gratefully acknowledged

References

1 S T Cho, K Najafi, C L Lowman and K D Wise, An ultrasensitive silicon pressure-based microflow sensor, *IEEE Trans Electron Devices, ED-39* (1992) 825–835
2 S T Cho, K Najafi and K D Wise, Internal stress compensation and scaling of ultrasensitive silicon pressure sensors, *IEEE Trans Electron Devices, ED-39* (1992) 836–842
3 S T Cho, K Najafi and K D Wise, Secondary sensitivities and stability of ultrasensitive silicon pressure sensors, *Tech Digest, Solid-State Sensor Workshop, Hilton Head, Island, SC, USA, June 1990*, pp 184–187
4 C S Sander, J W Knutti and J Meindl, A monolithic capacitive pressure sensor with pulsed-period output, *IEEE Trans Electron Devices, ED-27* (1980) 927–930
5 F Krummenacher, A high resolution capacitance to frequency converter, *IEEE J Solid-State Circuits, SSC-20* (1985) 666–670
6 M Smith, L Bowman and J Meindl, Analysis, design, and performance of a capacitive pressure sensor IC, *IEEE Trans Biomed Eng , BME-33* (1986) 163–174

7 Y E Park and K D Wise, A switched-capacitor readout circuit for capacitive pressure sensors, *Proc Custom IC Conf, Rochester, NY, USA, 1983*, pp 380–384
8 G J Yeh, I Dendo and W H Ko, Switched-capacitor interface circuit for capacitive transducers, *Proc 4th Int Conf Solid-State Sensors and Actuators (Transducers '85), Philadelphia, PA, USA, June 7–11, 1985*, pp 60–63
9 P E Allen and D R Holberg, *CMOS Analog Circuit Design*, Holt, Rinehart and Winston, New York, 1987
10 K Martin, New clock feedthrough cancellation technique for analog MOS switched-capacitor circuits, *Electron Lett*, *18* (1982) 39–40
11 D Y Young, Vibration of rectangular plates by the Ritz method *ASME Trans*, *72* (1950) 448–453
12 S T Cho, K Najafi, C L Lowman and K D Wise, An ultrasensitive silicon pressure-based microflow sensor, *IEEE Trans Electron Devices, ED-39* (1992) 825–835
13 R Gregorian and G C Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, New York, 1986
14 J F O'Hanlon, *A User's Guide to Vacuum Equipment and Technology*, Wiley, New York, 1980

Biographies

Steve T Cho received the BSEE degree from the Massachusetts Institute of Technology, Cambridge, MA, in 1985, the MSEE degree from the Ohio State University, Columbus, OH, in 1987, and the PhD degree in electrical engineering from the University of Michigan, Ann Arbor, in 1991 He was a research fellow in the Department of Electrical Engineering and Computer Science at the University of Michigan from 1991 to 1992 In 1992, he joined the Charles Stark Draper Laboratories, Cambridge, MA, where he is working on the development of micromachined integrated sensors

Kensall D Wise received the BSEE degree from Purdue University, West Lafayette, IN, in 1963, and the MSEE and PhD degrees in electrical engineering from Stanford University, Stanford, CA, in 1964 and 1969, respectively From 1969 to 1972 he was a research associate at Stanford, and from 1972 to 1974 he was on the technical staff at Bell Telephone Laboratories, Naperville, IL In 1974 he joined the Department of Electrical Engineering and Computer Science at the University of Michigan, where he is now professor and director of the Center for Integrated Sensors and Circuits