Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature

R.F. Wolffenbuttel
Laboratory for Electronic Instrumentation, Department of Electrical Engineering, Delft University of Technology, Mekelweg 4, 2628 CD Delft (Netherlands)

K.D. Wise
Center for Integrated Sensors and Circuits, Solid-state Electronics Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109-2122 (USA)

Abstract

Micromechanical smart sensor and actuator systems of high complexity become commercially viable when realized as a multi-wafer device in which the mechanical functions are distributed over different wafers and one of the wafers is dedicated to contain the readout circuits. The individually-processed wafers can be assembled using wafer-to-wafer bonding and can be combined to one single functional electro-mechanical unit using through-wafer interconnect, provided that the processes involved comply with the constraints imposed by the proper operation of the active electrical and micromechanical subsystems. This implies low-temperature wafer-to-wafer bonding and through-wafer interconnect. Au/Si eutectic bonding has been investigated as it can conveniently be combined with bulk-micromachined through-wafer interconnect. The temperature control in eutectic bonding has been shown to be critical.

1. Introduction

Several practical micromachining techniques in silicon have emerged from recent research. However, the complexity of the micromechanical systems that would potentially benefit from these developments often exceeds the performance limits of these technologies when applied to a single wafer. Silicon wafer-to-wafer bonding offers the designer of such a system an extra degree of flexibility to trade-off single-wafer concentrated complexity for multi-wafer solutions. Wafer-to-wafer bonding has been used in applications such as power devices [1], SOI [2–7] and has been particularly successful in integrated silicon sensors [8–11].

The main advantage of wafer-to-wafer bonding in the latter application is that it enables the separate fabrication of the sensor wafer and the wafer in which the active readout electronics is integrated, until the very last processing step. The sensor wafer can, therefore, be designed for maximum performance of the sensing element, without jeopardizing the performance of integrated active devices; the compatibility is not impaired. Moreover, the separation also allows for the use of different specialized foundries for processing of the sensor wafer and the readout wafer. Assembly can take place afterwards using relatively simple equipment, so that the batch fabrication advantage of the silicon technology is maintained. This approach, however, makes low-temperature wafer-to-wafer bonding and through-wafer interconnect mandatory.

Two techniques are widely employed for single-wafer micromachining; surface micromachining and bulk micromachining. Surface micromachining is based on the deposition of a sacrificial layer on a silicon substrate, the patterning of this layer and the subsequent deposition of a structural layer. Microstructures remain in the patterned structural layer after the selective removal of the sacrificial layer. In conventional surface micromachining with PSG as the sacrificial material, the lateral dimensions of fabricated microstructures are two orders of magnitude larger than the vertical machining capability. The lateral dimensions are determined by the die size, whereas the non-planarity is limited by the maximum width of the sacrificial layer (about 2–5 μm). Surface micromachining is, therefore, sometimes loosely referred to as a $2\frac{1}{2}$ dimensional sculpturing technique. Bulk micromachining allows the almost unrestricted sculpturing of a silicon wafer over all three dimensions. Anisotropic etching (usually along the (111) planes) or plasma etching enables the fabrication of wafer-thick cavities or trenches. High-boron-doped layers or pn junctions are conventionally em-

Elsevier Science S.A.
SSDI 0924-4247(93)00653-L

ployed to realize an automatic etch stop in order to obtain thin membranes, beams and cantilevers.

As bulk micromachining is a low-temperature processing step, it is compatible with the fabrication of integrated silicon smart sensors, in which the readout electronics are integrated on the chip. However, the integrity of the chip is seriously impaired by the (almost) through-wafer etching of the chip, which results in a reduced yield. This wafer integrity is fully preserved in surface micromachining and the low-temperature (LP)CVD techniques, that are used for the deposition of sacrificial and structural layers, ensure compatibility with integrated readout electronics. The main disadvantages of the surface micromachining are the limited design flexibility in the vertical direction and the high-temperature stress anneal in the structural layer.

Wafer-to-wafer bonding has the potential to overcome many of these problems. Individual wafers can be subjected to relatively simple bulk and/or surface micromachining steps and can subsequently be combined to realize a complex micromechanical function. The electronic circuits can, in principle, be integrated in any of the wafers, which further improves the design flexibility. As dicing and packaging take place after bonding, the micromechanical devices can be designed to be less prone to breaking during fabrication that would otherwise result from the reduced integrity of the individual bulk-micromachined wafer(s).

Wafer-to-wafer bonding

Silicon wafer-to-wafer bonding techniques can basically be classified into two categories: fusion bonding and intermediate bonding. Fusion bonding is based solely on the direct adhesion of two wafers that are brought into close contact at room temperature and subsequently heated up to about 1100 °C. Intermediate bonding is based on the addition of a material in between two wafers before pressing these together. This intermediate can be a polymer glue, a low-temperature melting glass or a metal at eutectic temperature. The intermediate bonding usually requires a much lower value of the processing temperature as compared to fusion bonding.

Silicon fusion bonding is based solely on the direct bonding of two wafers that are brought into close contact [1–4, 11, 12]. No adhesion materials are added. The two wafers that are to be bonded have to be flat (polished), clean and should be made hydrophilic (should contain a high density of OH groups attached to the surface) by boiling in nitric acid or immersion in an H_2O_2 NH_4OH bath. The wafers are brought into close contact at room temperature by either mechanical [4] or electrostatic [5] means. The bonding is generally assumed to take place according to a sequence of bonding-bridge replacements. Weak OH bridges are formed at mechanical contact at room temperature. The only voids that are observed in an IR transmission image are due to trapped particles (extrinsic voids) and the fracture strength remains below 1 MPa. Initial bonding takes place very rapidly and starts at the edge where the two wafers make first contact and propagates over the wafer surface within a few seconds. Some authors introduce the term 'bonding wave' to describe the course of the bonding.

Subsequently, the temperature is increased. Beyond 200 °C the fracture strength increases and intrinsic void formation becomes visible. These voids are additional to the extrinsic voids. At this stage the hydrogen bond between OH groups is assumed to be replaced by the oxygen bridge, whereby water is formed. The pressure of the trapped vapour is assumed to be responsible for the intrinsic void formation. A further increase in temperature results in dissociation of the water. The fracture strength increases and saturates at about 5 MPa, whereas the intrinsic void density decreases. These observations are in agreement with the model, as additional oxygen atoms become available to provide additional bonds and the hydrogen diffuses through the silicon lattice. As the vapour dissociates, the voids dissolve. An alternative theory is based on the lack of bonding time dependence of the fracture strength at a certain temperature [6, 13]. The authors suggest this to be due to the elastic deformation of the contacting wafers. The elasticity of the wafer increases with temperature which would allow for extra bonds to form. This theory is supported by an experiment that shows an increased fracture strength of thinned (and, therefore, more elastic) wafers. The intrinsic void formation is attributed to hydrocarbon contaminants at the wafer surface prior to the bonding and the annihilation of their effect at temperatures beyond 800 °C [14].

Beyond 1000 °C a maximum fracture strength of about 18 MPa is obtained with a void density that is acceptable in most applications. Increasing the temperature beyond 800 °C is assumed to result in the diffusion of oxygen into the crystal lattice and the replacement of oxide-bridge bonds by silicon-to-silicon bonds in one of the theories [4, 11, 12]. An alternative theory assumes the viscous flow of oxide to be responsible for the increased fracture strength [3, 15]. This viscous flow would also lead to the filling of microcavities at the bonding interface that are due to the surface roughness of the original wafers. The extrinsic void density is not reduced by this thermal treatment, so clean-room precautions have to be taken during bonding.

Notwithstanding the versatility and ease of operation, the silicon fusion bonding also shows two drawbacks.

The first major problem concerns the electrical interconnect between parts of the device located at different wafers. A three-wafer capacitive accelerometer as shown in Fig. 1 requires contacting to all wafer levels, whereas the mass wafer is the most suitable for the integration of the electronic circuits. The through-wafer interconnect could be realized using a tapered multi-wafer stack and by placing wire bonds in between. The lateral dimensions of the individual dies on the cap wafer should be smaller than those on the mass wafer and the latter should be smaller than the die size of the baseplate. The obvious disadvantage of this approach is the increased complexity of processing that is required to avoid loss of full wafer batch processing capability (e.g. etching of V-grooves at the dicing lane in the cap wafer and the mass wafer) and the increased costs of bonding and packaging.

Secondly, the deposition of the on-wafer interconnect and the subsequent patterning have to take place before the wafer-to-wafer bonding. Therefore, the interconnect should be able to withstand the bonding temperature. The conventional material used for interconnect is aluminum, which has a eutectic temperature at 577 °C. This implies that the aluminum becomes liquid at this temperature, which is due to the fact that it is contained in the binary Al–Si composition, and consequently the pattern information is lost. The problem can in principle be solved when resorting to silicides. A number of micromechanical techniques are feasible to resolve the through-wafer interconnection problem. However, the key issue that limits the practical applicability of those solutions is usually set by the processing temperature and its influence on junction diffusion and the on-wafer interconnect.

Conventional dopants in silicon (B, P and As) only demonstrate an appreciable diffusion at temperatures beyond 800 °C. Moreover, a rapid thermal anneal for 3 min at 1100 °C has been reported to be sufficient for reliable wafer-to-wafer fusion bonding [13]. This process step does not add significantly to the thermal budget. The rapid thermal anneal is part of a two-step approach and is in principle very interesting, as it allows an effective separation between the wafer-to-wafer alignment and pre-bond (at about 350 °C) and the high-temperature rapid anneal for creating a reliable bond. This technique is compatible with smart sensors with respect to the negligible junction diffusion, however the procedure is not compatible with aluminum on-wafer interconnect. The compatibility of the wafer-to-wafer bonding with integrated active devices in a standard process with the purpose of forming smart sensors is, therefore, mainly limited by the on-wafer interconnection problem.

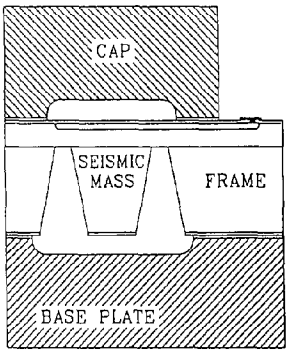


Fig. 1. Accelerometer with differential sense and servo drive capacitance.

Low-temperature wafer-to-wafer bonding

Intermediate bonding is the bonding of two silicon wafers using an intermediate layer; a polymer glue, a soft glass or gold beyond the eutectic temperature of the Au–Si binary system. The glue bonding is basically simple; a thin and reasonably uniform layer can be attached to the surface using spinning techniques. Pressing the wafers together and subsequent curing results in a bond. However, the glue bond is usually of poor reproducibility due to the limited control of the process. Corrosion due to outgassed products, thermal instability and penetration of moisture limits the reliability [16]. Moreover, the glue adhesion reveals only a limited compatibility with silicon processing. Nevertheless, this technique has been successfully applied for the fabrication of SOI devices [17].

Glass with a low softening temperature can be deposited on a silicon wafer to serve as an intermediate bonding material [16]. The temperature lowering is basically due to the addition of another substance. The resulting composition shows a phase diagram with a eutectic temperature that is significantly lower than that of pure glass.

One paper reports on the performance of #7570 glass [18]. This is basically a lead borate glass with a softening point at 440 °C. The bonding takes place using both mechanical and electrostatic contact force. A fracture strength in excess of 1.5 MPa is reported for bonding at room temperature, a mechanical stress of 100 kPa and an applied voltage in excess of 50 V. Although the authors do not provide much detailed information about the nature of the bonding process and the bonding mechanism at room temperature, bonding is assumed to take place due to local heating at the interface that results from the electrical current flowing through.

Another report describes the silicon wafer-to-wafer bonding using boron-doped glass as the intermediate material [19]. The glass is deposited on one of the

silicon wafers and subsequently this wafer is bonded to a second wafer at 450 °C. Bonding has been achieved, however this technique is very sensitive to phosphorus contaminants in the glass. Phosphorus leads to a drastic increase in the bonding temperature.

The performance of a bond based on sputtered #7740 borosilicate glass has been reported [20, 21]. A 1–5 μm thick layer is deposited on both wafers to be bonded. The wafers are subsequently electrostatically bonded at 400 °C with 50–200 V applied. The bonding takes about 10 min. A typical fracture strength of 2.5 MPa was obtained. The bonding mechanism is generally believed to be based on the drift of mobile sodium ions in the glass layers through the bonding interface, although the same effect has been observed for sodium-free glass [22]. The glass, although an electrical isolator at room temperature, is slightly conductive at the bonding temperature. The material is depleted near the interface due to the electrostatic repelling of ions. The voltage drop is, therefore, localized near the interface and a sufficient electrostatic contact force is available.

Recently, wafer-to-wafer bonding has been reported using sodium silicate as an intermediate layer [23]. A diluted solution of sodium silicate in water is spun onto one of the wafers to be bonded and after bringing the wafers into contact at room temperature and a subsequent anneal at 200 °C for 2 h, a bond with a surface energy of 3 J/m^2 was obtained. This value is comparable with the bonding strength for conventional silicon-to-silicon bonding at an anneal temperature in excess of 1000 °C, mentioned in the previous section. The obvious disadvantage of this technique is the introduction of sodium at the interface. However, the effect of the mobile oxide charge on the performance and reliability of integrated active devices is likely to be very limited, due to the fact that the bonding is performed as a post-processing step at low temperature.

Wafer-to-wafer bonding has also been demonstrated using metallic intermediate layers. Ti [24], PtSi [25] and $TiSi_2$ [26] have been reported to give reliable bonding after an anneal at 700 °C. In the case of titanium, a 5000 Å layer is E-beam evaporated on both wafers to be bonded. Subsequently, the wafers are brought into contact at room temperature and annealed at 700 °C in an oxidizing ambient for 20 min. The operating mechanism is believed to be similar to the silicon-to-silicon direct bonding, viz. via the formation of Ti–O–Ti bridges. Platinum silicides can be formed by E-beam evaporation of Pt while keeping the substrate at 350 °C. After etching of the Pt layer on top of the formed PtSi, the two wafers to be bonded are brought into contact at room temperature and annealed in a nitrogen ambient for 2 h at 700 °C. The special property of the silicide-based bond is the good electrical contact between the two bonded wafers.

Finally, there is the gold–silicon hard solder that has already been frequently used in VLSI for silicon die bonding to a substrate [16]. The silicon–gold binary system reveals the most dramatic reduction of the melting temperature. As shown in Fig. 2, the melting temperature is reduced from 1063 °C at pure gold to 363 °C, whereby 19 at.% silicon is dissolved in the eutectic silicon–gold compound. Eutectic die bonding is often used in industry. An Au/Si compound with 19 at.% Si is used as a substrate and heated up to a temperature slightly above the eutectic temperature (dashed line in Fig. 2). This Au/Si substrate acts as a solder and consumes silicon from the die after it is brought into direct contact. Silicon is dissolved until the saturation composition is reached (X_s in the Figure). Upon cooling a reliable bond was obtained. An extension of this technique is the micron bump bonding, in which multi-electrode contacts can be made between a die and the Si/Au substrate. Although this technique has so far only been used in die bonding, it can in principle also be employed for silicon wafer-to-wafer bonding with gold as an intermediate layer.

Eutectic gold bonding has already been implemented in 1979 by Ko *et al.* [27] for the fabrication of pressure transducers. This type of bond seems to introduce problems in the long-term stability of the sensor. The thermal mismatch introduces stress during cool down that relaxes with time. These problems will be demonstrated to be basically due to an insufficient temperature control during bonding.

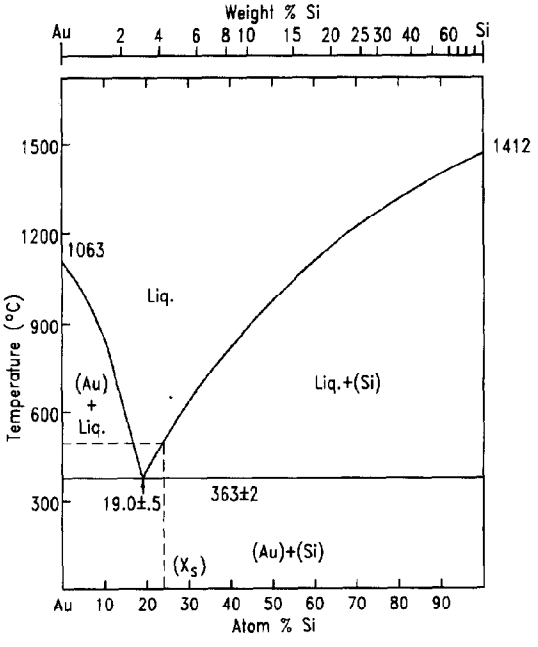


Fig. 2. Silicon–gold phase diagram.

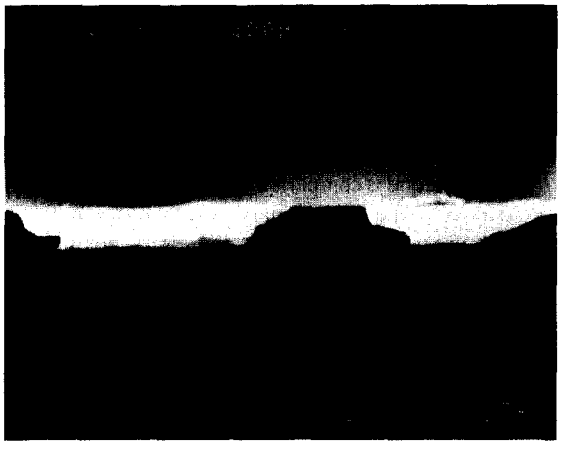
Si/Au wafer-to-wafer bonding

Eutectic gold die bonding is basically the *de facto* industry standard on die bonding and the application in silicon wafer-to-wafer bonding seems like an obvious extension. Problems associated with gold eutectic bonding are the long-term drift in sealed-cavity devices and the possible trap formation halfway to the bandgap. Contamination of silicon with gold would result in a severe reduction of the minority carrier lifetime in integrated active devices. However, many micromachining processes are already designed in such a way that the actual micromachining steps are performed as low-temperature post-processing steps outside the cleanroom. The intermediate eutectic gold bonding would be a natural extension of this approach. Under normal conditions silicon dissolves in the flowing gold and not vice versa, so there is, in principle, no gold doping of the wafer.

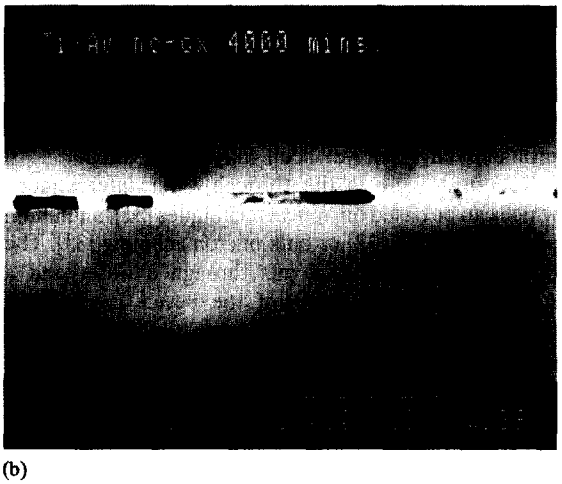
Standard 3″ p-type (100) Si wafers were thermally oxidized and 300 Å Ti and 1200 Å Au were subsequently E-beam evaporated. The Ti is deposited to avoid poor adhesion due to the low-surface energy SiO_2 layer. Finally, the wafers are brought into contact and placed on a hot plate with a 100 g distributed weight for between 5 and 4000 min at temperatures between 350 and 400 °C. Heating of the wafer beyond the eutectic temperature results in a change in surface texture due to the formation of fine silicon microstructures on top of the gold surface as shown in Fig. 3. This effect is already known from die bonding [16] and indicates that a 100% bonded area cannot be achieved. Although the shape and density of the final microstructures is almost time and temperature independent, the effect occurs after 60 s at 400 °C, 100 s at 390 °C, 5 min at 370 °C and 10 min at 365 °C. This observation strongly suggests that the mixing of Si into Au due to solid-state diffusion does not take place uniformly until the eutectic composition is reached (19 at.% Si), but rather clusters of silicon are formed. Obviously, reliable bonding cannot be achieved after microstructure formation, as only point-to-point contact is made where ridges overlap.

Bonding strength was evaluated using both the razor blade insertion test (razor should not penetrate) and by SEM observation of the cleaved bonded wafers [6, 24]. Figure 4(a) and (b) shows the detailed and wide view, respectively, and indicates a bonded area less than 50% for bonding at 400 °C almost irrespective of bonding time. Experiments indicate that a reliable bond with in excess of 90% bonded area is obtainable for bonding at 365 °C and 10 min, as shown in Fig. 5. Bonding time and temperature are very critical, however the texture of a monitor wafer can be used as a simple

Fig. 3. Structure of the Au/Si eutectic material after heating up to 390 °C.



(a)



(b)

Fig. 4. Detailed (a) and global (b) view of the eutectic bond after bonding at 400 °C for 4000 min.

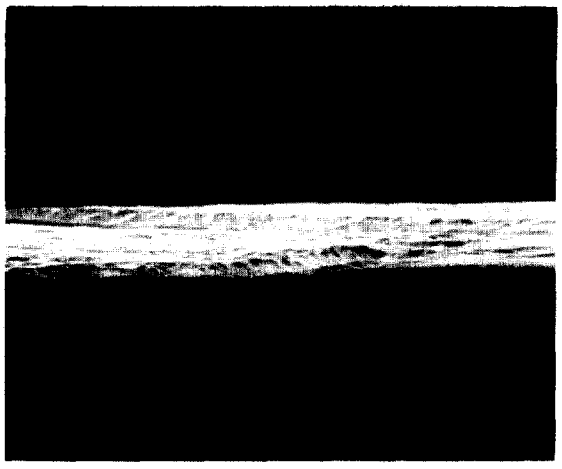


Fig. 5. The eutectic bond after bonding at 365 °C for 10 min.

indicator. Experiments have demonstrated the suitability of the eutectic low-temperature wafer-to-wafer bonding for multi-wafer smart sensors, the compatibility with techniques for through-wafer interconnect and the functional integrity of the bonded device. The sealing performance needs to be demonstrated using an endurance test on an integrated pressure sensor.

This technique is compatible with on-wafer aluminum interconnect. The Si/Al binary system has a eutectic temperature at 577 °C and is, therefore, not flowing at Si/Au eutectic bonding. The aluminum on-wafer interconnect can be deposited and patterned before the wafer-to-wafer bonding. In reality the problems are more complicated. First, the bonding temperature of 400 °C has the same effect on the patterned aluminum on one of the silicon wafers as sintering and care should be taken to avoid spiking. On the other hand it should be possible to combine the bonding and sintering. Secondly, the silicon dissolves to some extent into the aluminum [28]. Finally, stress is formed or relieved in the interconnect at this temperature by elastic or plastic deformation [29] and the reliability of the device could be severely impaired by the resulting voids [30]. These problems have not yet been fully investigated.

The next issue is the through-wafer interconnect, which can be based on optical techniques [31], aluminum electromigration [32] or bulk micromachining [33]. The bulk micromachining of pits through a wafer and a subsequent metal coating of the bevels is presently being investigated, as is its compatibility with gold intermediate bonding [34].

Conclusions

A low-temperature process has been designed for the fabrication of wafer-to-wafer bonded devices based on eutectic silicon–gold intermediate bonding. Smart micromechanical sensors and actuators can be fabricated with electronic and/or micromechanical functions distributed over various wafers, due to the low-temperature processing and the implementation of through-wafer interconnect. The area consumption required for bonding (sealing) and etching of through holes makes the technique less-suitable for high-density wafer-scale integration, but it is of great promise in smart sensors, where up to 10 leads is usually sufficient.

Acknowledgement

This work is supported in part by STW Project No. DEL 11.2609.

References

1 H. Ohashi, K. Furukawa, M. Atsuta, N. Nakagawa and K. Imamura, Study of Si-wafer directly bonded interface effect on power device characteristics, *Proc. IEDM '87*, pp. 678–681.
2 J.B. Lasky, S.R. Stiffler, F.R. White and J.R. Abernathy, SOI by bonding and etch-back, *Proc. IEDM '85*, pp. 684–688.
3 W.P. Maszara, Silicon-on-insulator by wafer bonding: A review, *J. Electrochem. Soc., 138* (1991) 341–347.
4 M. Shimbo, K. Furukuwa, F. Fukuda and K. Tanazawa, Silicon-to-silicon direct bonding method, *J. Appl. Phys., 60* (1986) 2897–2989.
5 T.R. Anthony, Dielectric isolation of silicon by anodic bonding, *J. Appl. Phys., 58* (1985) 1240–1247.
6 W.P. Maszara, G. Goetz, A. Caviglia and J.B. McKitterick, Bonding of silicon wafers for silicon-on-insulator, *J. Appl. Phys., 64* (1988) 4943–4950.
7 L.J. Spangler and K.D. Wise, A bulk silicon SOI process for active integrated sensors, *Sensors and Actuators, A24* (1990) 117–122.
8 R.W. Bowen, M.S. Ismail and S.M. Farrens, Aligned wafer bonding: a key to 3-dimensional microstructures, *J. Electron. Mater., 20* (1991) 383–387.
9 K.P. Petersen, P. Barth, J. Poydock, J. Brown, J. Mallon and J. Bryzek, Silicon fusion bonding for pressure sensors, *Proc. 1988 Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, USA, June 6–9, 1988*, pp. 144–147.
10 P. Barth, F. Pourahmadi, R. Mayer, J. Poydock and K.P. Petersen, A monolithic accelerometer with integral air damping and overrange protection, *Proc. 1988 Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, USA, June 6–9, 1988*, pp. 35–39.
11 P.W. Barth, Fusion bonding for fabrication of sensors, actuators and microstructures, *Sensors and Actuators, A21–A23* (1990) 919–926.
12 C. Harendt, H-G. Graf, B. Hoefflinger and E. Penteker, Silicon fusion bonding and its characterization, *J. Micromech. Microeng., 2* (1992) 113–116.
13 Q.-Y. Tong, X.-L. Xu and H. Shen, Diffusion and oxide viscous flow mechanism in silicon direct bonding process and silicon wafer rapid thermal bonding, *Electron. Lett., 26* (1990) 697–699.

14 K. Mitani, V. Lehmann and U. Gosele, Bubble formation during silicon wafer bonding: Causes and remedies, *Proc. 1990 Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, USA.*

15 R. Stengl, T. Tan and U. Gosele, A model for the silicon wafer bonding process, *Jpn. J. Appl. Phys., 28* (1988) 1735–1741.

16 R.K. Shukla and N.P. Mencinger, A critical review of VLSI die-attachment in high-reliability applications, *Solid State Technol.,* (July) (1985) 67–74.

17 T. Hamaguchi, N. Endo, M. Kimura and M. Nakamae, Novel LSI/SOI wafer fabrication using device layer transfer technique, *Proc. IEDM '86,* pp. 688–691.

18 M. Esashi, N. Nakano, S. Shoji and H. Hebiguchi, Low-temperature silicon-to-silicon anodic bonding with intermediate low melting point glass, *Sensors and Actuators, A21–A23* (1990) 931–934.

19 L.A. Field and R.S. Muller, Fusing silicon wafers with low melting temperature glass, *Sensors and Actuators, A21–A23* (1990) 935–938.

20 A.D. Brooks, R.P. Donovan and C.A. Hardesty, Low-temperature electrostatic silicon-to-silicon seals using sputtered borosilicate glass, *J. Electrochem. Soc., 119* (1972) 545–546.

21 A. Hanneborg, Silicon-to-thin film anodic bonding, *J. Micromech. Microeng.,* (1992) 117–121.

22 R.C. Frye, J.E. Griffith and Y.H. Wong, A field-assisted bonding process for silicon dielectric isolation, *J. Electrochem. Soc., 133* (1986) 1673–1677.

23 H.J. Quenzer and W. Beneke, Low-temperature silicon wafer bonding, *Sensors and Actuators A, 32* (1992) 340–344.

24 D. Noyak, A. Reisman and I. Turlik, Metal-to-metal bonding using an oxidizing ambient atmosphere, *J. Electochem. Soc., 135* (1988) 1023–1025.

25 M.S. Ismail and R.W. Bower, Platinum silicide fusion bonding, *Electron. Lett., 27* (1991) 1153–1155.

26 M.S. Ismail, R.W. Bower and B.E. Roberds, Polysilicon and titanium silicide + polycide fusion bonding for 3-D microdevices applications, *Proc. 1992 Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, USA,* pp. 86–89.

27 W.H. Ko, J. Hynecek and S.F. Boettcher, Development of a miniature pressure transducer for biomedical applications, *IEEE Trans. Electron Devices, ED-26* (1979) 1896–1905.

28 G.J. van Gurp, Diffusion-limited silicon precipitation in evaporated Al/Si films, *J. Appl. Phys., 44* (1973) 2040–2050.

29 D.S. Gardner and P.A. Flinn, Mechanical stress as a function of temperature in aluminum films, *IEEE Trans. Electron Devices, ED-35* (1988) 2160–2169.

30 K.Hinode, I. Asano and Y. Homma, Void formation mechanism in VLSI aluminum metalization, *IEEE Trans. Electron Devices, ED-36* (1989) 1050–1055.

31 L.A. Hornak and S.K. Tewksbury, On the feasibility of through-wafer optical interconnects for hybrid wafer-scale integrated architectures, *IEEE Trans. Electron Devices, ED-34* (1987) 1557–1563.

32 H.E. Cline and T.R. Anthony, Migration of fine molten wires in thin silicon wafers, *J. Appl. Phys., 49* (1978) 2412–2419.

33 J.C.-M. Huang and K.D. Wise, A monolithic pressure-pH sensor for esophageal studies, *Proc. IEDM '82, San Francisco, CA, USA, Dec. 13–15, 1982,* pp. 316–319.

34 R.F. Wolffenbuttel and K.D. Wise, Bulk-micromachined through-wafer interconnect for silicon wafer-to-wafer bonding, *Proc. Transducer '93, Yokohama, Japan, June 7–10, 1993,* pp. 194–197.