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BRIEF COMMUNICATION

A Pulse Height Discriminator and Post-Stimulus Histogram System using Integrated Circuits[1]

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SPEARS, R., G. SMITH AND K. L. CASEY. *A pulse height discriminator and post-stimulus histogram system using integrated circuits.* PHYSIOL. BEHAV. 5 (11) 1327–1329, 1970.—Integrated circuits can be used to construct a compact, relatively inexpensive device which performs the functions of spike amplitude discrimination and digital post-stimulus histogram generation. The logic diagram, detailed schematic, and mode of operation of such a system is presented and discussed.

Apparatus Pulse height discriminator Post-stimulus histogram system

THE ANALYSIS and acquisition of single unit data is greatly facilitated by the use of an on-line amplitude discrimination system which permits the selection of spikes from multiple-unit recordings. A number of such devices have been described [2, 3]. The post-stimulus histogram (PSH) is another widely used technique for quantifying the response properties of units in the central nervous system. Usually, amplitude discrimination and PSH generation requires the use of separate instruments which must be adjusted and synchronized for proper operation. The use of separate devices may also add unnecessarily to space requirements and to the expense of these operations, for the histogram read-out often requires an oscilloscope or other expensive display system. This report describes a compact, relatively inexpensive instrument which performs the amplitude discrimination, generates the PSH over a predetermined number of trials, and displays it in digital format. A number of outputs are available so that upper and lower discrimination levels, pulse output from the discriminator, and histogram bin width can be monitored.

A logic diagram of the complete system is shown in Fig. 1; Fig. 2 shows a detailed schematic with component values and parts identification. The system is designed to work with input pulses having rise times between 5 ms and 200 μs. The integrated circuit components use only positive potentials or pulses so that any negative potential at the input will not be seen at the output.

Input to the pulse height discriminator (PHD) section of the system (signal 1/p, Fig. 1) is taken from the single-ended output of a low-level AC coupled amplifier (e.g. Tektronix 122). This signal is applied to one input of each of two comparators (Fairchild I.C. U5B771031X); the other comparator inputs are each connected to the center taps of potentiometers used for establishing the upper and lower discrimination levels. Action potentials with peaks falling between these levels will generate an output pulse from the lower, but not upper, level comparator. The pulse width is equal to the width of the action potential as it crosses the lower level. This pulse is inverted, differentiated and re-inverted to provide an inverted positive pulse which represents the trailing edge of the input spike. This is applied to one of the inputs to the terminal AND gate D of the PHD. The positive pulse output of inverter A is differentiated and applied to one input of NOR gate B; the undifferentiated pulse is inverted through gate C to remove the pre-set to the flip-flop, thus allowing it to be simultaneously toggled by the inverted positive pulse from gate B. Thus, the leading edge of the input spike as it crosses the lower level causes the 1 output of the flip-flop to become 0. This output is reset to 1 again by the termination of the inverted pulse from gate C. The resulting pulse from the flip-flop is differentiated and inverted to provide another inverted positive pulse at the terminal PHD AND gate. Since both AND gate inputs represent the trailing edge of the input spike as it crosses the lower discriminator level, they are synchronous and produce a pulse output which can be monitored on an oscilloscope (point 3, Fig. 1) and applied to the counters of the post-stimulus histogram (PSH) section.

If the input spike crosses the upper discriminator level, two inverted positive pulses will be generated at the output of gate B, each representing the leading edge of the spike as it

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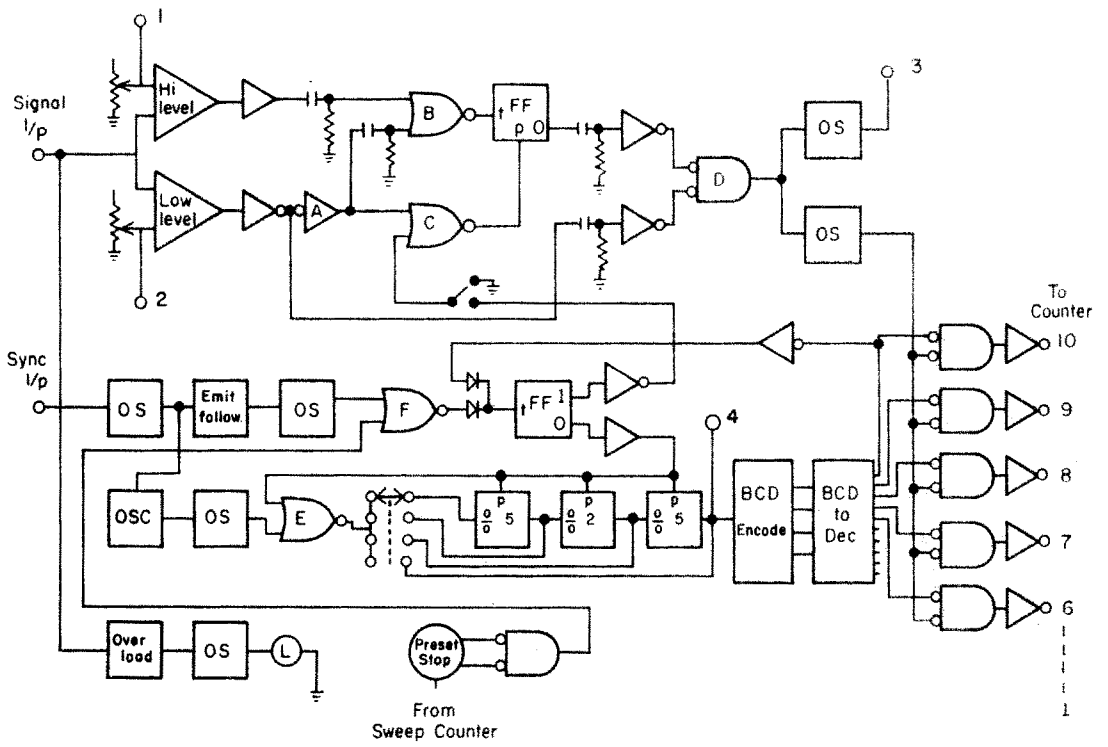

FIG. 1. Logic (RTL) diagram of combined PHD and PSH unit. The amplitude discrimination system is shown in the upper part of the diagram; below this is the PSH generation system.

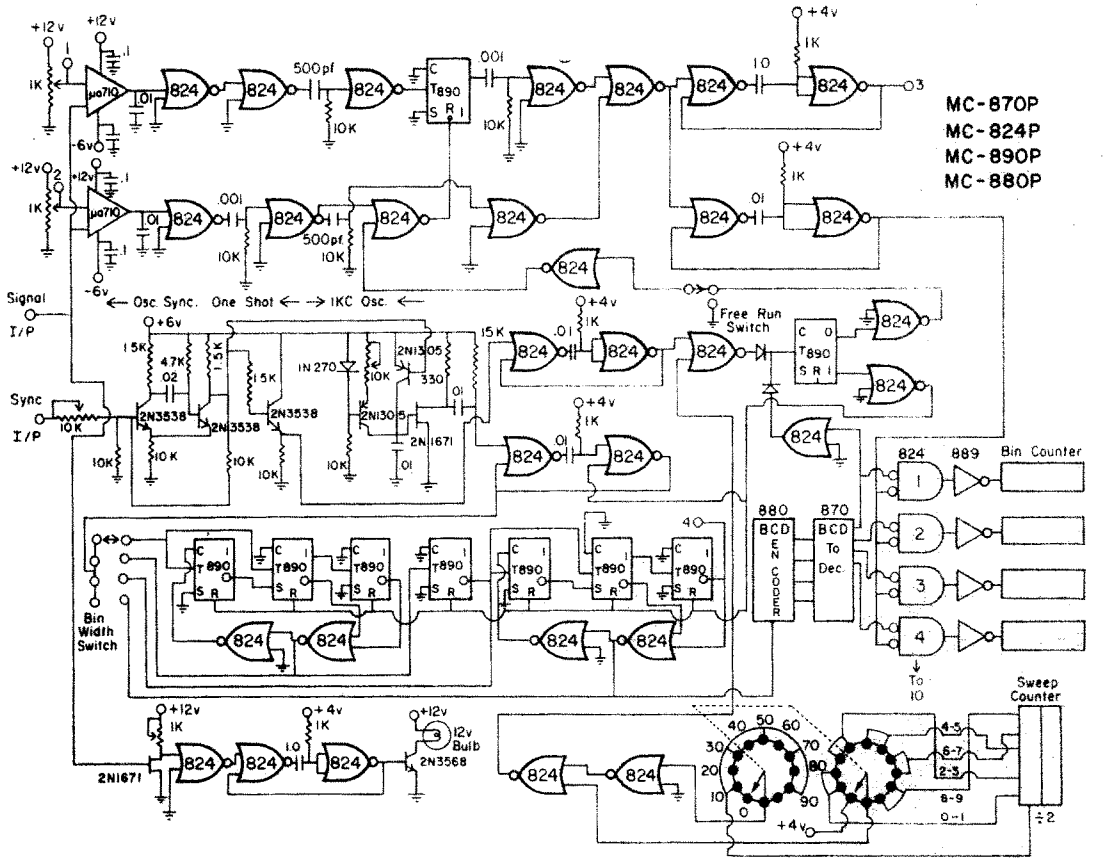

FIG. 2. Detailed schematic of the system shown in Fig. 1. Parts numbers of integrated circuit elements refers to Motorola RTL.

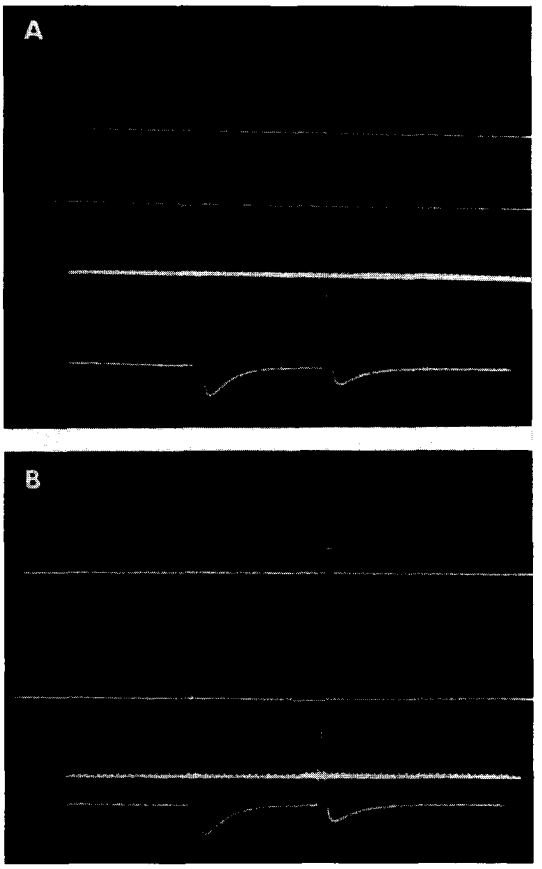

FIG. 3. Operation of the PHD system shown, using simulated action potentials of approximately 1 msec duration (lower traces in A and B). A: output pulse (top trace) triggered only by larger spike. B: output pulse (top trace) triggered only by smaller spike. Middle two traces represent upper and lower trigger levels.

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crosses both upper and lower levels. This will reset the flip-flop output before the termination of the inverted pulse from gate C. The resulting inverted positive pulse at the terminal AND gate D is not synchronous with the trailing edge pulse from the lower level detector, so no PHD output is generated.

The PSH portion of the system is triggered by a pulse synchronized with a stimulator. This pulse is used to synchronize an oscillator and is applied to one terminal of NOR gate E. A pre-set counter is triggered by the output of this gate until the desired number of stimuli have been delivered. At this point, the input to the other NOR gate terminal F goes positive, causing a flip-flop to change state and preventing further output from NOR gate E. Simultaneously, PHD output is prevented by the state change applied to gate C in the PHD section. Until the desired number of stimuli have been applied, however, the oscillator can be used to trigger any combination of frequency dividers to provide the desired histogram bin width. The frequency divider outputs are encoded (Motorola I.C. MC780P or MC88P) and then decoded to decimal form (Motorola I.C. MC77OP or MC870P) so as to sequentially distribute pulses to one input of a series of AND gates, one for each counter. The other input to each AND gate is the PHD output pulse. PHD output pulses are registered in each counter until the AND gate is closed. When the final AND gate is closed (end bin of the histogram), the state change is applied through an inverter to the flip-flop, which again disables the PHD and blocks the oscillator input to the frequency dividers until the next stimulus is applied. Input spikes which occur between post-stimulus analysis periods are therefore not counted in any bin.

The number of stimuli applied and the number of action potentials which occurred in each time bin are read directly from the counters. Bin width is read directly from the dial setting for the frequency divider and may be checked during sampling by displaying the output from the oscillator or frequency divider on an oscilloscope (point 4, Fig. 1). Figure 3 shows a display of the operation of the PHD section using simulated action potentials of different amplitude. A manually operated switch is available at one input to gate C to disable the automatic cut-off system and thus permit examination of the PHD output and PSH counters while setting the discrimination levels.

Regulated power supplies of +9V and −9V, +4V, and +3.8 V are required for the comparators, the oscillator, and the integrated circuits, respectively. The indicator lights require +6 V power supply, unregulated.

This system has been in operation for nearly 2 years. It is a simple, relatively inexpensive and reliable method for performing some of the initial steps in data reduction and analysis now commonly used by neurophysiologists. Computer time and memory can be reserved for more elaborate analyses which can be performed using the standard pulse output of the PHD. The system can be assembled by anyone with a knowledge of logic circuitry and some familiarity with integrated circuits. The estimated cost of the logic components is $200; inexpensive counters [1] are used in the systems now in operation and have proven satisfactory.

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