A 1-Mc Transistor DC Amplifier

By: E. M. Aupperle

Approved by: H. W. Farris

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1. The study reported was not exhaustive.
2. The results presented concern one phase of a continuing study.
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ABSTRACT

The design and evaluation of a stable, inexpensive, transistor dc amplifier capable of significant voltage gain from dc to several megacycles is presented. This device was built to serve in a wide-band, phase-lock loop application; however, it can replace a conventional operational amplifier in many circuits when space, weight, and bandwidth are important considerations. The amplifier features a differential input and an emitter follower, the latter to provide a low output impedance.
1. INTRODUCTION

The voltage gain of a typical dc amplifier is designed to decrease rapidly as a function of increasing frequency. Indeed, the unity gain frequency is seldom more than a few hundred kilocycles. This paper presents the design and analysis of a stable, wide-band, transistor dc amplifier. The amplifier incorporates a differential input stage and is terminated in an emitter-follower stage to provide a low output impedance. The open loop voltage gain of this simple four-transistor circuit is approximately 1000 at low frequencies. With an appropriate feedback resistor the circuit will provide a voltage gain of 50 with the 3db point at 1.1 Mc. Figure 1 is a picture of the completed amplifier.

Fig. 1. The completed dc amplifier package.
2. CIRCUIT DESCRIPTION

The basic open loop circuit is shown in Fig. 2. This circuit requires both a positive and a negative voltage supply, which conveniently permits a dc output centered about zero. The entire voltage gain results from the first two stages, while the third stage supplies a current gain and provides the low output impedance. The voltage gain of the differential input stage for low-frequency, small-amplitude signals is derived in the Appendix. The result for an appropriate choice of resistor values is:

\[ V_3 = -\frac{R_2\beta_1\beta_2(V_2-V_1)}{R_{s1}\beta_2 + R_{s2}\beta_1} \]  

(1)

where:

- \( V_3 \) is the instantaneous voltage across \( R_2 \)
- \( \beta_1 \) and \( \beta_2 \) are the respective values of beta for \( T_1 \) and \( T_2 \)
$R_{s1}$ and $R_{s2}$ are the respective values of the source impedance.

For the symmetrical case where $\beta_1 = \beta_2 = \beta$ and $R_{s1} = R_{s2} = R_s$, the gain becomes:

$$V_3 = -\frac{R_2\beta(v_2-v_1)}{2R_s} \quad (2)$$

It follows that a substantial voltage gain is possible with this unit, and, furthermore, the sole transistor parameter which affects the gain is $\beta$.

The voltage gain of the second stage is discussed in detail in many books on transistor circuit applications. The appropriate expression is:

$$\frac{V_0}{V_3} \approx -\frac{\alpha_3 R_4}{R_5 + \frac{r_e}{R_3} (1-\alpha_3)} \quad (3)$$

when:

$$R_4 \ll r_c \quad \text{and} \quad R_5 \ll R_6$$

If the constraint, $\frac{r_e}{1-\alpha_3} \ll R_5 \ll R_6$, applies to $R_5$, then the gain of the second stage is independent of all transistor parameters except $\alpha_3$, and Eq. 3 becomes:

$$\frac{V_0}{V_3} \approx -\frac{\alpha_3 R_4}{R_5} \quad (4)$$
When Eqs. 2 and 4 are combined, the open-loop voltage gain is given by:

$$V_0 = A_1A_2(V_2 - V_1)$$  \hspace{1cm} (5)

where:

$$A_1 = -\frac{\beta R_2}{2R_s} \text{ and } A_2 = -\frac{\alpha_3 R_4}{R_5}$$

It is to be observed that a phase reversal occurs for $V_1$ but not for $V_2$.

Amplifiers of this type are usually operated with some form of feedback. Consider the arrangement in Fig. 3. The gain for this circuit is also derived in the Appendix with the final simple results:

$$\frac{V_0}{V_2} = (1 + \frac{R_{fb}}{R_{s1}})$$  \hspace{1cm} (6)

when the forward gain, $\frac{V_0}{V_1}$, is negative and $\frac{|V_0|}{|V_1|} \gg \frac{R_{fb} + R_{s1}}{R_2}$.

3. EXPERIMENTAL EVALUATION

The actual experimental circuit is given in Fig. 4. The frequency response of this unit was obtained using a source with an internal impedance of 528 ohms.
Fig. 4. Complete circuit diagram.

The measured low frequency voltage gain was 53.5 with a 3db bandwidth of 1.1 Mc. The experimental frequency response curve is presented in Fig. 5. At 10 kc the input impedance was found to be 100 k ohms shunted with 35 pf, while the output impedance was 20 ohms. The output response to 1 kc, 10 kc, 100 kc, and 1 Mc square-wave input signals is shown in Fig. 6. The dc drift at room temperature (~25°C) re-
Fig. 6. Square wave response.

Fig. 7. Dc drift vs. operating temperature.
ferred to the input was approximately 1 mv/24 hr. A low frequency
noise voltage with a 50 µv rms level again referred to the input was
also observed. This fluctuation noise was reduced by an order of
magnitude when a high pass filter with a cut-off frequency of 15 cycles
was placed in the output circuit of the amplifier. Figure 7 indicates
the dc drift as a function of operating temperature.

4. APPLICATIONS

The total cost of materials for this amplifier, exclusive of
a mounting structure, is less than twenty dollars. All the components
are commercially available through electronic equipment suppliers.
Since the amplifier has many desirable electronic properties and also
is physically small, light weight, and inexpensive, it has many appli-
cations. Briefly, these include wideband transistor control systems,
a cheap and compact computer component, and satellite instrumentation
circuits. With an appropriate input or output filter this amplifier
could also be used as a wideband audio amplifier.

This unit was initially designed for use in a wideband
phase-lock circuit. The high dc gain of typical commercial circuits
was not required, however it was essential to have a one-megacycle
bandwidth. In this sense this amplifier is not equivalent to the
high dc gain operational amplifiers found in analog computer applica-
tions. By the addition of another stage of voltage gain it would be
possible to increase the dc open-loop gain to approximately 30,000.
Some loss of bandwidth would be expected, and the problem of stability
would increase.
APPENDIX

A very useful and practical input stage for a dc amplifier is the differential amplifier. A typical transistor circuit is shown in Fig. A.1. The output voltage may be taken across either $R_1$ or $R_2$, however, there is a 180-degree phase difference in these two voltages.

![Differential Amplifier Circuit](image)

Fig. A.1. Differential amplifier stage.

In the circuit of Fig. A.1 it is possible to set $R_1$ equal to zero without directly affecting $V_3$. However, when this is done the circuit no longer retains its insensitivity to variations in collector conductance of $T_1$. In general it is desirable to select matched transistors and set $R_1 = R_2$.

Consider now the low frequency, small-signal analysis of Fig. A.1. An equivalent circuit is depicted in Fig. A.2. Here the assumption is that $R_1 \ll r_{c1}$ and $R_2 \ll r_{c2}$, hence the parallel combinations are essentially equivalent to $R_1$ and $R_2$, respectively.

![Low Frequency Equivalent Circuit](image)

Fig. A.2. Low frequency, small-signal equivalent circuit of Figure A.1.
To simplify the following analysis we will define:

\[ R_{s_1}^* = R_{s_1} + r_{b_1} \]
\[ R_{s_2}^* = R_{s_2} + r_{b_2} \]

The following equations may then immediately be written:

\[ V_1 = R_{s_1}^* i_{b_1} + r_{e_1} i_{e_1} + R_3 (i_{e_1} + i_{e_2}) \]
\[ V_2 = R_{s_2}^* i_{b_2} + r_{e_2} i_{e_2} + R_3 (i_{e_1} + i_{e_2}) \]
\[ i_{e_1} = i_{b_1} (l + \beta_1) \]
\[ i_{e_2} = i_{b_2} (l + \beta_2) \]

These lead to the linear system:

\[
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix}
= \begin{bmatrix}
R_{s_1}^* + (l + \beta_1) r_{e_1} + R_3 (l + \beta_1) & R_3 (l + \beta_2) \\
R_3 (l + \beta_1) & [R_{s_2}^* + (1 + \beta_2) r_{e_2} + R_3 (1 + \beta_2)]
\end{bmatrix}
\begin{bmatrix}
i_{b_1} \\
i_{b_2}
\end{bmatrix}
\]

For the conditions

\[ R_3 \gg R_{s_1} \gg (\beta_i + 1) r_{e_i}, \beta_i \gg 1 \quad i = 1, 2 \]

it can be shown that

\[ i_{b_1} \approx \frac{R_3 (l + \beta_2) (V_1 - V_2)}{\Delta} \]
\[ i_{b_2} \approx \frac{R_3 (l + \beta_1) (V_2 - V_1)}{\Delta} \]

where:

\[ \Delta \approx R_3 [R_{s_1}^* (1 + \beta_2) + R_{s_2}^* (1 + \beta_1)] \]
Hence:

\[ i_{b_2} = \frac{(1 + \beta_1)(V_2 - V_1)}{R_s^* (1 + \beta_2) + R_s^* (1 + \beta_2)} = \frac{\beta_2 (V_2 - V_1)}{R_s^* \beta_2 + R_s^* \beta_1} \]

and

\[ i_{b_1} = -\frac{(1 + \beta_2)}{(1 + \beta_1)} i_{b_2} = -\frac{\beta_2}{\beta_1} i_{b_2} \]

This last result indicates that the phase of the two currents and hence the voltages across \( R_1 \) and \( R_2 \) are 180 degrees apart. The voltage across \( R_2 \) is given by

\[ V_3 = -\beta_2 R_2 i_{b_2} = -\frac{R_2 \beta_1 \beta_2 (V_2 - V_1)}{R_s^* \beta_2 + R_s^* \beta_1} \quad (A.1) \]

For the case of complete symmetry the above reduces to

\[ V_3 \approx -\frac{R_2 \beta (V_2 - V_1)}{2R_s^*} \]

If now \( R_{s_1} \gg r_{b_1} \) (i = 1, 2), then it follows that

\[ V_3 = -\frac{R_2 \beta_1 \beta_2 (V_2 - V_1)}{R_s^* \beta_2 + R_s^* \beta_1} \quad (A.2) \]

This is independent of all transistor parameters other than the two betas. Note that the above equations presuppose that the transistors are operating about a properly chosen quiescent point. A significant point to observe is that for \( V_1 = V_2 \), the input impedance is infinite, subject to the above approximate expressions.
Now consider replacing the input source A.3(a) with A.3(b). With the aid of Thevenin's theorem, the equivalent circuit of A.3(b) is as shown in Fig. A.4.

![Fig. A.3. Two input configurations: (a) Direct arrangement. (b) Feedback arrangement.](image)

Substituting this into Eq. A.2, there obtains:

\[ V_3 = \frac{R_2 \beta_1 \beta_2 \left( V_2 - \frac{R_{s1} V_0}{R_{s1} + R_{fb}} \right)}{\left( \frac{R_{s1} R_{fb}}{R_{s1} + R_{fb}} \right) \beta_2 + R_s \beta_1} \]

If one now sets: \( V_0 = A_2 V_3 \),

then:

\[ \frac{V_0}{A_2} = \frac{R_2 \beta_1 \beta_2 \left( V_2 - \frac{R_{s1} V_0}{R_{s1} + R_{fb}} \right)}{\left( \frac{R_{s1} R_{fb}}{R_{s1} + R_{fb}} \right) \beta_2 + R_s \beta_1} \]
or:

\[ \frac{V_0}{V_2} = \left( 1 + \frac{R_{fb}}{R_{s_1}} \right) \frac{1}{1 - \frac{1}{A_2 R_{s_1}^2 \beta_1} \frac{R_{s_1} \beta_1}{R_{s_2} \beta_2} \left( R_{fb} + R_{s_1} \right)} \]  

(A.3)

If we assume \( \beta_1 = \beta_2 = \beta \) and \( R_{s_1} = R_{s_2} \), this becomes:

\[ \frac{V_0}{V_2} = \left( 1 + \frac{R_{fb}}{R_{s_1}} \right) \frac{1}{1 - \frac{1}{A_2 R_{s_1}^2 \beta} \left( R_{fb} + R_{s_1} \right)} \]

For \( A_2 \gg 0 \) this system has regenerative feedback. Indeed the system will be unstable for

\[ 0 < A_2 < \frac{R_{fb} + R_{s_1}}{\beta R_{s_2}} \]

For \( A_2 < 0 \) the system is degenerative. The usual case is for

\[ |A_2 B| \gg \frac{R_{fb} + R_{s_1}}{R_{s_1}} \]

and for \( A_2 \) to be negative. Hence,

\[ \frac{V_0}{V_2} \approx 1 + \frac{R_{fb}}{R_{s_1}} \]

and if \( R_{fb} \gg R_{s_1} \), this leads to

\[ \frac{V_0}{V_2} \approx \frac{R_{fb}}{R_{s_1}} \]

This equation indicates that for the above assumptions the dc amplifier
with degenerative feedback has an overall voltage gain which, within
the above approximations, is independent of the transistor character-
istics. The value of this last result, of course, depends on the
stability of the open-loop gain.

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