

COMPUTER CONTROLLED  
OPTIMIZATION OF  
POWER SYSTEM INTEGRITY

A STUDENT DESIGN PROJECT

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## PREFACE

Recent power system breakdowns indicate the need for greater power system stability and integrity. Such blackouts as the Northeast power failure in 1965 and the Missouri Basin blackout in 1965 demonstrated a weakness in the human control over relays. As the regional systems become interconnected and power pools grow larger, the effect of major disturbance spreads over larger areas. The exchange of power within a pool influences the stability of the regional systems. Through a computer control approach this project sought to eliminate human error and increase power system integrity.

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INTRODUCTIONA. Project Objectives

The goal of this design project is to develop a computerized control system for large power distribution networks. Most previous work in the area of computer control of power systems has been purposely ignored in an attempt to establish a new outlook on an old problem. Due to the fresh approach, more problems were encountered than had been anticipated, and thus some aspects of this report are somewhat general. For this reason and because of the extreme flexibility of the many components of the system, exact analysis is virtually impossible. The numbers presented are representative and are well within an order of magnitude of expected costs.

B. Problem Analysis

The economics of power generation require that large generating plants be distributed in a rather nonuniform fashion in a power distribution system. Because of this non-uniform distribution of generation, power must be transmitted in rather large blocks to areas without generation capability. This bulk distribution system is subject to failures and these failures occasionally cause massive outages of the entire distribution system. Aside from these large outages, the reliability of the distribution system as a whole is remarkably high (the Detroit Edison Company boasts a reliability index of 0.99995; the index of reliability is the number of customer hours service is available divided by the total number of customer hours), and the problem of increasing this figure significantly is extremely perplexing and controversial. The system to be specified in this report will be one



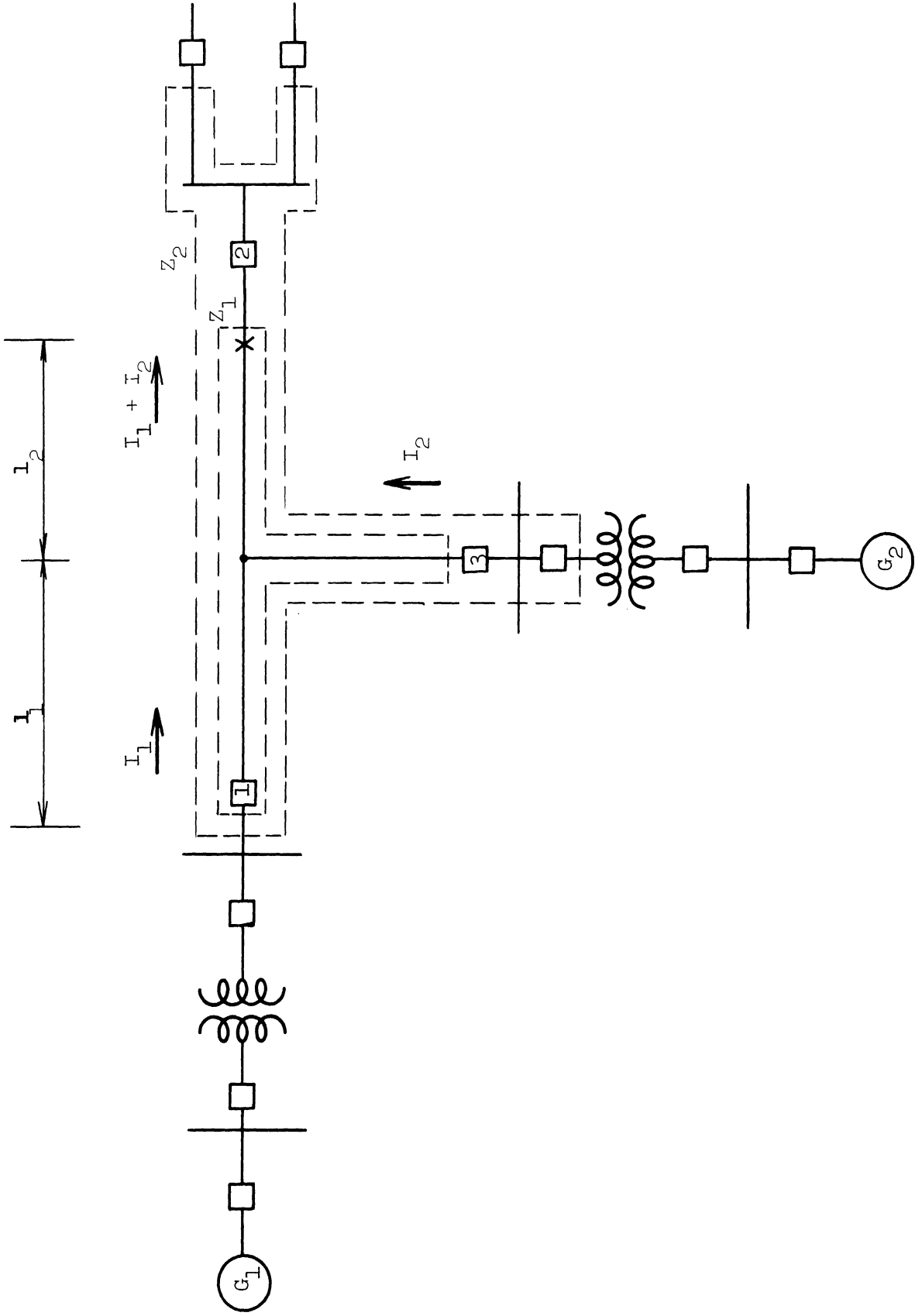
of computer control to increase reliability as far as massive outages are concerned, with little emphasis on routine servicing.

### Present Protection Scheme

Distribution systems can be divided into parts on the basis of voltage and power handling ability. Bulk distribution is carried out at 120 kv and above. Subtransmission at 20-40 kv is the next division in distribution. These two groups will be the focus of this analysis. The transmission lines are protected against damage from faults by distance or impedance relaying, which disconnects the line from service when a fault is detected on the line. These relays are set to activate if the impedance of the load as it appears at the relay drops to a value equal to the impedance of the shorted line. The distance from the relay to a short on the line will determine the impedance of the line and relays can be set to sense shorts on selected sections of lines. The relays have three active units which serve as immediate protection and backup protection for a given line section. As illustrated in Figure 1, the breaker at 1 will open immediately for a fault in zone 1 which is approximately 80% of the section length. Backup is provided by time delayed operation in zone 2 and further delay in zone 3 should any of the relays at positions 2, 3, 4, 5, or 6 fail to operate. This scheme is fast and reliable in the simple case presented. It is often supplemented with pilot relaying which is a communication tie between relays at the ends of a section.

If there is more than one terminal on a line the protection scheme is very much more complex. As in Figure 2, the impedance seen by the relay at 1 for a fault at x is now given as





Three Terminal Line Illustration

Figure 2

$$Z_F = Z_{(L_1 + L_2)} + \frac{I_2}{I_1} Z_{(L_2)} \dots\dots\dots (1)$$

where  $Z_{(L_1 + L_2)}$  is the impedance of line 1 + line 2, and  $Z_{L_2}$  is the impedance of line 2 so that the zone 1 setting of the relay at position 1 will have to be adjusted as the power delivered by the generation  $G_2$  changes. This proposed system deals mainly with this problem as it is one that is not easily solved without computerized coordination of the relay settings.

There is further protection at the generating plants and tie lines in the form of frequency relaying and overcurrent relaying. The setting of overcurrent relays can also be treated as an important part of updating the protection as the power demands change.

#### The Ideal Power System

The ideal power system should provide the maximum security for the minimum cost. To do this both corrective security and preventive security have to be investigated and used. Corrective security means that action to eliminate or minimize system breakdown is taken after a fault occurs. The major corrective measures to be taken are high speed switching to dampen out transients; rerouting power transmission; adding and/or dropping generation and/or load to match load and generation; and, if the system becomes unstable, optimally sectionizing the system. The basic philosophy here assumes the existence of an "omniscient" central computer which possesses a knowledge of all the factors governing the power system. This computer would then act in a predetermined manner. Such a set up would be able to distinguish among short circuits, through flows, and instability. Then either by high speed calculation or table

reference it would determine and take the best actions. But this omniscient computer must keep track of a number of variables, such as: power flow in lines of the system; power build-up curves consisting of spinning reserves, cold start up, and the stepping up of current generation; a list of load shedding; and line and equipment failure.

### Preventive Security

In addition the central computer will handle what is called preventive security. (i.e., the system is run in such a manner that it will remain stable in the event of a fault) In this case stability studies are used to determine safe operating limits for the system. These day to day operating limits would specify from what generators power should come, how much spinning reserve is needed, and how much power could be exported to or imported from another system. This stability could also be increased by resetting and checking the system's safety devices, in particular, the relays. Another possible method would be duplication of some or all the parts of the system. This redundancy would be undesirable for most parts of the system from an economic standpoint. In addition the computer should provide a fairly current status report for economic dispatch and the edification of the operator.

### System Limitations

Unfortunately today we are limited by the speed and capacity of the computers. In the case of corrective security, actions must be taken so quickly that the fastest computer we have now would only have time to receive the states of the system. There would be no time left

to do the computation. In addition under severe fault conditions, computation time would take about fifteen minutes. The communication speed required would necessitate the use of micro-waves. This is now too expensive to be feasible, although the cost of micro-wave communication is expected to come down. Finally the sensing devices would have to be faster--on the order of one-tenth cycle. There is hope that such a corrective philosophy can be enacted in the future. The advent of a solo-men type computer will bring a 1000-fold increase in computing speed. Even today we have a high speed current sensor (1/10 cycle) called the "Traser."

The preventive security can be used today, because it has no high speed requirements. If relays could be set and checked remotely, many of the human errors would be avoided. For example, in 1962 relays cut out the generation at Fort Randall Dam. This was a major cause in the loss of power to three million people. In January, 1965 false operation of differential relays resulted from an accident during maintenance. Again a widespread power loss occurred. Then there was the northeast power failure which was started by an incorrectly set over-current relay. Since relays have played such a crucial part in recent power failures, it was decided to examine this area.

#### System Expansion

Though present technology limits computer control to preventative security, advances will gradually make corrective security possible. High speed "Traser" sensors for current are being field tested with good results. These devices have 1/10 cycle response times which is adequate for transient detection and sampling. The cost of high speed communications is decreasing as microwave technology expands so that

with multiplexed scanning relatively simultaneous samples could be obtained throughout the system.

Computation speeds are still very slow considering the tremendous amounts of information to be processed. Only computers with parallel direct access memory and large arrays of processing elements will be able to handle the data input rates and computation speeds.

This system proposed can be adopted to corrective security with some effort. A high speed hybrid or solomon type computer can be added as a supervisor computer and all data lines and sensors can be converted to high speed. The organization, however, will remain unchanged.

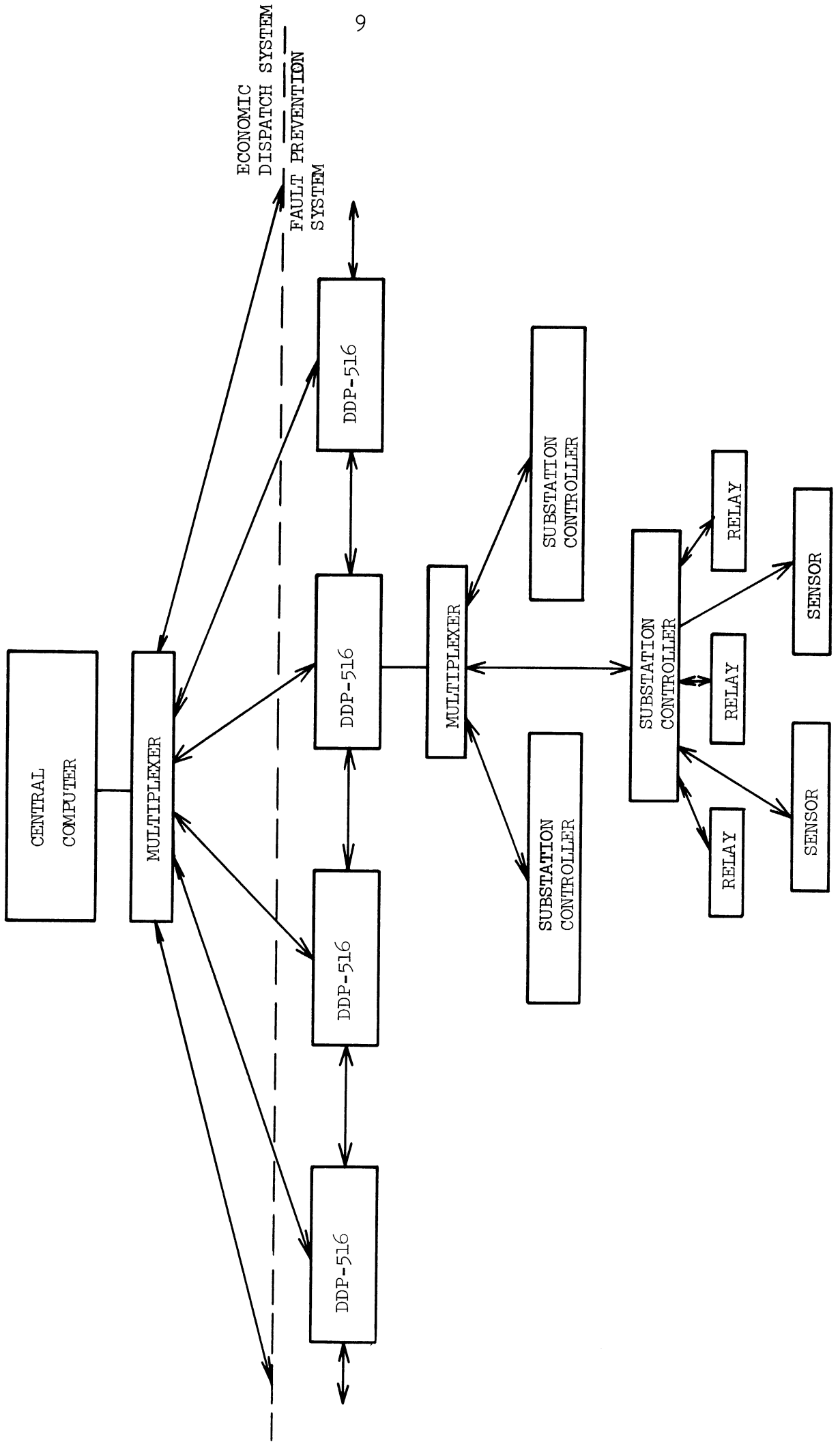
### C. System Specifications

The proposed system will provide the following functions.

1. Coordination of the settings of relays on multiterminal lines for maximum security against instability under all load conditions.
2. Coordination of the settings of overcurrent relays in the backup system.
3. On line spot checking of relay operation to anticipate malfunctions of relays.
4. Continual display of power system status for the dispatcher (display on request of dispatcher).
5. Planned line outages in advance to maintain security during maintenance periods.
6. Addition of economic dispatch.

To implement these functions the system as pictured in Figure 3 is proposed. Sensors will monitor power flow at each point of interest and each relay that needs adjustment will have a tap changing device under computer control. Each substation will have a control unit that

Figure 3





will multiplex sensor data and relay status (i.e., opened or closed) and setting for input to the computer covering the area. This control unit will also direct commands from the computer to the appropriate relay or generator control unit. The substation controllers will be supervised by small general purpose digital computers that will access each other in a manner appropriate to coordinate the relay settings across area boundaries. A control computer will be used for economic dispatch and over-current relay coordination with possible expansion to stability analysis as machine capabilities are increased.

#### D. Group Specifications and Responsibilities

##### 1. Relay Setting

Relay setting devices change the taps of the relay coil under computer control. These units accept a single word of data and will make the appropriate tap change. Relay lockout switches are provided so that appropriate tap changes will force operation for maintenance checks. The settings of the relays are available as input to the computer for checking.

##### 2. Substation Controllers

Substation control units are distributed one per substation on the two transmission systems discussed. These units receive commands from the small computers and perform the following functions:

- a. upon command provide the computer with sensor data from each line in a sequential manner.
- b. provide the computer with the setting of any relay specified by the computer.
- c. issue to any relay specified by the computer a setting spec-

ified by the computer.

- d. disconnect from service any relay specified.
- e. provide a word of data that contains the status of all relays in the substation.

### 3. Data Multiplexers

Analog data from the sensors in each substation is multiplexed to an analog to digital converter for input to the computer. The control for this unit is provided by the substation controller.

### 4. Computer Control

Algorithms for distance relay setting and over-current relay setting are developed along with scan controlling and command issue algorithms. Input-output and possible display techniques are developed.

### 5. Communications

Required communication links are specified and implemented.

## Chapter I

SUBSTATION CONTROLA. Introduction

In order to affect power system security using on-line digital computers, data must be available from all points in the system before computation can take place. Also, the computers must be capable of dispatching commands to relays in the system so as to provide coordination for maximum possible system security under various conditions and system configurations. Clearly the data gathering and command dispatching operations must be rapid to be effective, for often faults and line outages leave the system extremely vulnerable to catastrophic failure. At the same time, these processes must be economical in order to be feasible, for the number of points to be monitored and the number of relays to be coordinated in the typical power system is enormous, and it has been concluded that expensive methods could not be justified considering present system reliability.

Since the usual switchyard or substation has several input and output lines, it is obviously desirable to multiplex the data gathering and command dispatching signals within that substation over a single time-shared communications link. In this manner the data gathering and dispatching circuitry can be shared with obvious savings in both communications lines and substation equipment. With an average of three lines per substation in the Detroit Edison System for example, equipment and communications costs can be cut by a factor of three using multiplexing. This cost factor improves when high input-output density switchyards are considered.

Another advantage of multiplexing is the ability to expand the system without causing drastic communications system changes. If more input or

output lines are added to a switchyard, then the same terminal and communications equipment can be used with a negligible increase in hardware and no drastic data system modifications. Only a slight change in the utility program is required. In contrast, if each line monitor and relay has its own terminal and communications equipment, then the addition of several lines to a switchyard, or a power system modification, will cause drastic communications system changes. Other advantages of multiplexing include system uniformity and programming simplification. If the multiplexer is correctly designed, then much of the bookkeeping can be performed at the switchyard, thus simplifying the programming of the monitor computers as well as saving much computation time-which is obviously at a premium. The alternative solutions to the problem-either providing individual computers at each substation or else providing a separate communications channel for each line in the system-are both prohibitively expensive. For example, even using the least expensive commercially available computer, the DEC PDP-8/S, the cost of providing separate computers at each substation location is five to ten million dollars for the Detroit Edison System. And even if this organization were implemented, a high speed communications channel will still be required for each substation in the system.

Thus data and command dispatching to the various lines within a substation can be done most economically and effectively by multiplexers at these locations-multiplexers designed for slower, voice-channel telephone lines-each capable of providing all necessary data to the central computers, and each capable of dispatching all commands necessary to insure the integrity of the power system through relay coordination.

## B. Multiplexing Requirements

The substation multiplexers should be capable of performing the following duties:

1. Multiplexing of real power, reactive power, and power flow direction from each line terminating at a switchyard into a common communications channel at such a speed as to be both effective and economical.
2. Providing for on-line checking of all relays in the power system under actual circuit conditions.
3. Allowing on- or off-line changes in relay settings throughout the system from a central location.
4. Allowing read-in to the DDP-516 of the present setting of any relay setting in the system.
5. Providing fault or line outage locations on command for all lines in the system.
6. Interrupting the monitor computer in the event of a faulted line or an unexpected line outage.
7. Providing for self-checking of the multiplexer circuitry.

Clearly some of these functions are not needed at all substation locations, so that the multiplexer must have modular flexibility: in other words, the various logical functions must be designed so as to be capable of being added to the multiplexer with little or no wiring changes. This concept will eliminate costly "custom" designs at each substation, and possibly only one main-frame need be designed. Such a frame will accommodate not only varying substation complexities, but also various requirements within these substations. For example, at a three-terminal switchyard no economic dispatch calculations are involved. Therefore, at this type of substation, no reactive power data

need be taken, and in the ideal multiplexer this facility could be deleted with some savings in data transfer time and in equipment cost. Further, at this type of substation only three lines need be addressed, so that the full address register complement and associated decoders are not needed, etc.

The speed requirements of the multiplexers were defined by the use of reed-relay analog selector switches and by the requirement of using conventional voice channels in order to cut costs. The relays have a minimum open-close cycle time of 4.0 milliseconds. Since the data transfer is sixteen bits (as required for the DDP-516 computer), and since two power readings of eight bits each (corresponding to errors of less than 0.5% in conversion from analog to digital) can be packed into each sixteen bit word, then clearly there is no need to transmit at a rate of more than sixteen bits per ten milliseconds (allowing for A-to-D conversion time) or about 1600 bits/second. This data rate is clearly compatible with conventional Dataphone facilities. This relatively slow cycle time allows the use of inexpensive integrated circuit RTL, for the usual 200kHz maximum clock rate with this type of logic would not hamper operation in any way.

Another multiplexer requirement is compatibility with presently available equipment such as the Dataphone facility, thermal sensors for power measurement, the specified Honeywell DDP-516 computer, the geographic locations and the densities of substations, and distance (or impedance) type relays.

The multiplexer should place no unusual constraints upon the programmer, and should operate independently of the monitor computers; that is, it should require no timing pulses generated externally. It should be jam-proof; that is, the programmer at the central location should be in control of the multiplexing operation at all times. (It might be noted that

these particular conclusions and specifications resulted from experiments with PMX-1, an experimental multiplexer built for evaluating timing problems, described later in this paper and in detail in the Appendix.)

Probably the most important requirement of a suitable multiplexing system is reliability. Since the unit will control the relay settings within the power system, then clearly it must be extremely reliable to maintain system integrity. Data gathered through such multiplexers serves as operands for stability calculations, and thus functional errors cannot be tolerated. Relays could be improperly set, causing much more trouble than now exists. Possibly the most obvious source of error is component failure. The hardware used must clearly be extremely reliable--having wide temperature margins, high noise immunity, and a long mean-time-between-failure. Multiplexer units could conceivably be exposed to extreme environmental conditions--temperature ranges of -50 to +120 degrees F., humidity from 10-100%, salt spray, rain, wind, vibration, etc. Consequently the hardware must be carefully chosen, and good mechanical design must be carried through. The logic used must have extremely good noise immunity, for lightening, and other atmospheric disturbances, as well as switching transients, could play havoc with low-level circuitry.

Since errors are bound to occur due to noise and momentary component failure, error detecting circuitry must be provided. Parity checks on data transfers are needed, as are detection of improper data or opcode fields within an instruction. There should be hardware checking routines which can test the multiplexer's circuits at the command of the programmer. Perhaps such routines should be provided within the executive system of the monitor computers. The circuits should be designed so that the relays and the other equipment within the substation will revert to normal conditions in the event of a massive multiplexer system failure--an emergency source of power should be provided in such events. Finally, the unit should be

designed so that servicing would normally consist of changing logic cards.

### C. Realization of the Requirements

During the planning stages of the Power System many multiplexer organizations were proposed and considered. Most of these had one common feature: externally supplied timing pulses--slave operation. This was an attempt to simplify the circuitry within the multiplexers, and thus place most of the work of multiplexing upon the shoulders of the programmer. It was recognized that there was a need for a certain amount of uniformity within the multiplexers so that mass production techniques could aid in cutting costs. So with the concepts of slave operation and modular design firmly grounded, and with the basic requirements in mind, an experimental unit was built to evaluate the design and to uncover any unforeseen problems. This unit - the PMX-1 (Programmed Multiplexer - 1) was designed and built in the Systems Engineering Laboratory using the Digital Equipment Company's Logic Laboratories. A D.E.C. PDP-8 computer was used as the monitor computer, and a small test program was written. Details of the logic design of PMX-1 may be found in the Appendix. An abbreviated instruction list was adopted. This list, consisting of six instructions, is shown in Figure 1, Appendix I. The organization of PMX-1 is shown in Figure 2, Appendix I. All necessary registers were included in the design, so that accurate timing and cost evaluations could be made. One register, the OSR (mnemonic for Operand Storage Register) acted as a buffer register for both instructions and for power data. A line address register (LAR) held the address of the line being monitored or the address of the relay being set. A fault location register (FLR) held the locations of any lines within the system which were out of service due to planned outage or to faults, and the IRM signalled the PDP-8 via the interrupt request bus



whenever an unexpected change occurred in this register. The reed-relay analog switch and the analog-digital converter were constructed for realistic considerations of any timing problems. The various instructions were implemented using separate and logically complete packages for each, consistent with the concept of modular design. Thus an instruction (or group of instructions) could be added or deleted by simply unplugging the appropriate modules. The power readings (ordinarily from thermal sensors) were simulated using panel-mounted potentiometers, and relay operations were simulated using toggle switches and indicator lamps. A test program was written for the PDP-8 computer which would fully test the PMX-1 (Figure 17, Appendix I).

The results of these tests were extremely valuable in planning the final design, for many unexpected problems were encountered. During the course of the tests, the unit became hopelessly jammed several times -- jammed to such an extent that no program control could restore its operation. This problem points out a need for a drastic re-organization of the multiplexer: separate registers are needed for data and for instructions; and timing signals should be generated internally, contrary to the original design concept of external timing and slave operation. The idea of packing both real and reactive power for each line into one word was found to be feasible, but the need for better control circuitry for this function was demonstrated by the test results. The FLR and IRM worked well, calling for immediate action via the PDP-8 interrupt bus whenever a sudden fault occurred. The results of the reed-relay analog switch and A-to-D converter tests are shown in the appropriate section of this report; but in general, these devices did provide the high speed, high accuracy, and low offset voltage as required by the design.

Thus the construction of the PMX-1 provided extremely useful information for the design of PMX-2, the final multiplexer design. The jamming and timing problems which were uncovered inspired drastic system design changes, but the

basic idea remained the same. The construction of PMX-1 also provided some estimate of the cost of a final design, for an order of magnitude guess could then be made as to the quantities of gates, flip-flop, etc., required. A component count and cost for PMX-1 is shown in Figure 4, Appendix I.

Thus the final design of the multiplexing system should include the following additions and changes:

1. Separate data (DBR) and instruction (IBR) buffer registers to insure jam-proof operation.
2. Internally-generated timing and synchronizing signals so as to be completely independent of the monitor computers.
3. Additional operations as required for maintaining power system control and integrity.
4. Design consistent with integrated circuit technology and the Honeywell DDP-516.
5. Parity check with interrupt on data transfers.
6. Checks for invalid operation code and improper operand fields.
7. Power failure protection.
8. Self-checking routines and sequences.
9. Additional partitioning of the logic for ease of servicing and modular design.

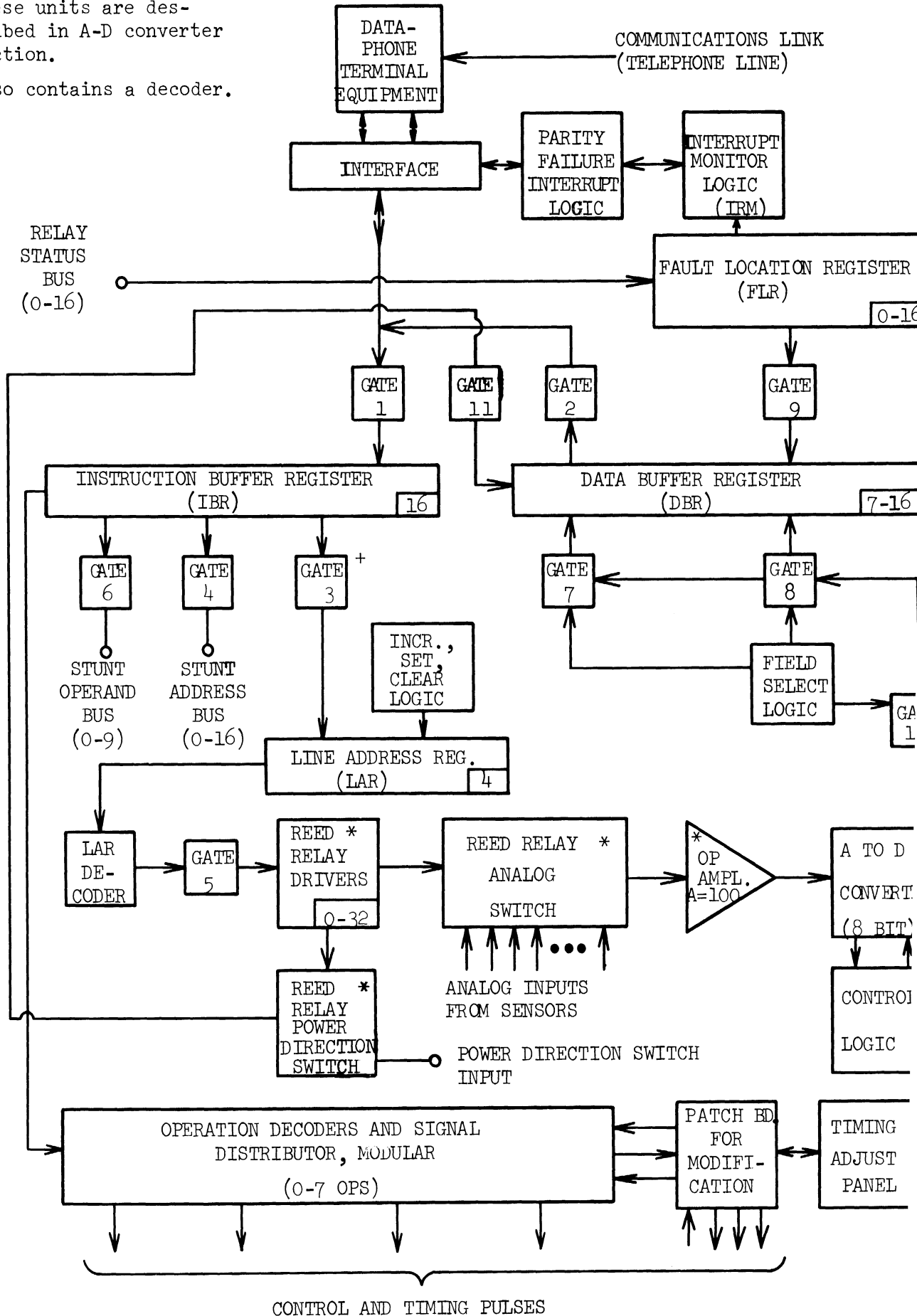
With these requirements in mind, the systems design of PMX-2 was evolved. The organization of the device is shown in Figure 1. The command list (Figure 2) was revised so as to include the operation (RRY,I,) which allows the present setting of any relay to be examined for checking purposes or for restoring the system after a central computer failure. The other

PMX-2 Organization

Figure 1.1

\* These units are described in A-D converter section.

+ Also contains a decoder.



PMX-2 COMMAND LIST

- OPCODE 0<sub>8</sub>: NO OPERATION (NOP)
- OPCODE 1<sub>8</sub>: SEQUENTIAL CONVERSION (SCV)
- Load digitalized real and reactive power into DBR at 8 msec. intervals, along with sign.
  - Transmit data after completion of loading.
  - Set last line flag (LLF) to 1 at the beginning of transmission of the last word.
  - Clear DRB and IBR after completion of transmission.
- OPCODE 2<sub>8</sub>: FAULT LOCATION EXAMINE (FLE)
- Load FLR into DBR
  - Set FLR flag (FLF) to 1
  - Clear DBR and IBR after completion of transmission of FLR contents.
- OPCODE 3<sub>8</sub>: SET RELAY (I) TO Y (SRY,I,Y)
- Set relay<sub>i</sub> to (y) of DBR.
  - Send finish word when relay has set.
  - Clear DBR and IBR when transmission is complete.
- OPCODE 4<sub>8</sub>: CHECK RELAY (I) ON LINE (CKR, I,)
- Disconnect trip coil of relay<sub>i</sub>.
  - Set relay<sub>i</sub> to dropout point.
  - Wait for relay operation signal from IRM.
  - Send (FLR) to DBR; set FLF to 1.
  - Restore relay<sub>i</sub> to normal operation.
  - Clear trip coil disconnect.
  - Clear DBR and IBR.
- OPCODE 5<sub>8</sub>: READ RELAY (I) (RRY,I,)
- Input relay setting to DBR
  - Clear DBR after completion of transmission

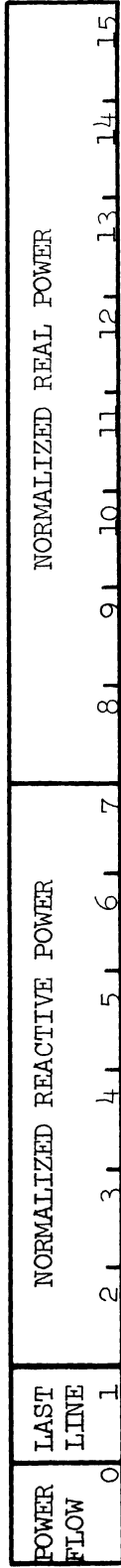
operations remained practically the same as in the PMX-1, except that the on-line relay checking instruction, (CKR, I, ), was made complete within itself. In the PMX-1, a long sequence of instructions was needed for on-line checking:

CLR	Clear all registers
CKR, I,	Disables trip circuit of relay <sub>i</sub>
SRY, I, Y	Sets relay <sub>i</sub> to such a value that it will drop out
FLE	Check for relay operation
SRY, I, Y'	Restore relay to normal setting
CLR	Clear registers and trip circuit
NOP	No operation, etc.

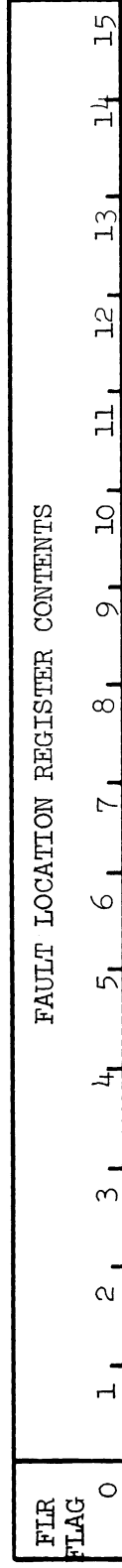
In the PMX-2, all these instructions are performed by calling for the (CKR,I,) instruction. The operation (SCV) reads real and reactive power data, as well as power direction, from each lines in the substation and sequentially transmits this data to the DDP-516 via a Dataphone link. The A-to-D converter controls the timing of this operation so that there is no possibility of premature data transfer prior to completion of the conversion process. The reed-relay switch sequentially selects the appropriate thermal sensor output (as determined by the line address register, LAR) within the substation and the A-to-D converter converts this voltage to a digital eight-bit word. These words are loaded into the appropriate half of the DBR at four millisecond intervals, so that a complete data word is assembled for transfer at eight millisecond intervals. A flag is set to one in the DBR (LLF) whenever the contents of the LAR equals a built-in constant (wired option). This allows any number of lines (up to sixteen) to be addressed by one LAR circuit, and thus only minor circuit changes are needed for modification. The (FLE) instruction inputs the fault

location register (FLR) to the DDP-516 via the DBR for examination. (SRY, I, Y) causes the address and operand fields of the DBR to be gated to the relays in the substation. All relays are connected to the same thirteen-wire bus within the substation for wiring simplicity. The operand field is first gated out, followed by the address field. A four-bit decoder, part of each relay, decodes the address portion of the instruction and thus enables the nine-bit operand field to be jam-transferred into the storage registers of the appropriate relay to be set. The address decoder thus acts as a device selector for the relay. The relays are then designed to make appropriate changes in taps and thus are set according to the Y-field of DBR. As shown in Figure 5, nine bits are provided for the Y-field of DBR. One of these bits specifies the special test setting of the relay, so that eight bits remain for setting the relay. The Y-field is further divided into two groups of four bits each, each group interpreted as a decimal (BCD) digit in excess-three code. Thus there are twenty possible relay settings; ten settings from 0-100%, and ten from 100-200% of the normal impedance of the line. Unused code groups in the Y-field signal an improper field error via the interrupt facility.

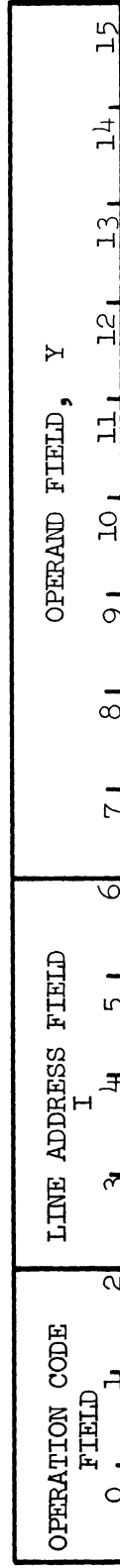
The operation (CKR, I,) disables the trip coil circuit of relay<sub>i</sub>, the address as again specified by the relay device selector. Thus even if the relay operates, the breaker will not. This enables the relay to be checked on-line for proper operation. The relay is set to a special tap by this instruction as specified by a one in bit seven of the operand field (see Figure 3) so that it will drop out, setting a one in the appropriate bit position of the FLR, and signalling the DDP-516 via the IRM that indeed the relay has operated. The FLR is transferred to the DBR for examination and the relay is restored to normal, as specified by all zeros in the Y-field of DBR. (RRY, I,) causes the present setting of relay<sub>i</sub>--the address



I. LINE DATA FORMAT



II. FAULT LOCATION FORMAT



III. INSTRUCTION FORMAT

PMX-2

IOT Formats

Figure 1.3

as specified by the Y-field of DBR--to be gated into the DBR for remote examination.

The FLR and IRM are designed so that any change in the FLR due to a relay operation will set a flip-flop in the IRM. Then, whenever the multiplexer has completed its present operation, a low-priority interrupt request bus of the DDP-516 is enabled to request a decision as to the effect of this line outage or fault.

For power failure protection, the multiplexer was designed to operate from a  $\pm 6$  volt source. Normally, power is provided by a regulated AC power supply which is connected in parallel with a storage battery large enough to accommodate the multiplexer for 4-6 hours of normal operation. The AC supply not only provides power for the multiplexer during normal operation, but also charges the storage battery. Thus in the event of a power failure the multiplexer will continue to operate normally until the condition is corrected. A low-priority interrupt is requested from the DDP-516 so that the computer will be aware of the condition which exists and can begin corrective procedures.

Each operation package is a plug-in unit, with all timing and enable pulses generated within the package. This enables packages to be deleted where they are not needed. All timing and enable pulses terminate on a patch board, so that changes and deletions can be implemented by grounding or interconnecting the appropriate points on the patch board. A timing panel is also provided so that the delays can be adjusted to suit the particular substation facility. For example, if reactive power data is not needed from a certain substation, then the appropriate hardware can be deleted from the DBR (bit position 2-7) and then the delay is changed from four to eight milliseconds. Of course, slight changes are also required on the patch board. Only one backpanel is required for all possible



multiplexer installations, regardless of the type or complexity of the substation. This will eliminate custom-designed units, and will cut costs by taking advantage of mass production techniques.

In order to estimate the cost of PMX-2, the cost of PMX-1 was used as a guide (Figure 4, Appendix I). Since the cost of integrated circuit logic (RTL) is about 1/3 the cost of D.E.C. logic modules (used in the PMX-1) then the cost of the gates, including packaging into appropriate modules should be about \$500. The cost of the backpanel, power supply, storage battery and control, mounting hardware and housing, the A-to-D converter, the analog switch, and wiring could add another \$500-1500 to the total cost. Therefore, a conservative cost estimate for the PMX-2 is \$2000 (selling cost). Mass production techniques should be able to cut this cost through quantity buying and automated hardware (wiring) production.

The mean-time-between-failure (MTBF) of the hardware depends upon the type of logic used, but for continuous operation, the multiplexers could have MTBF's of ten years or more. Since the reed relays have lifetimes of about  $10^9$  operations, failures in these components should never cause multiplexer failure, especially since the contact current is near zero. Since the substation will revert to normal operation in the event of a multiplexer failure, and since a DDP-516 interrupt points out faulty units, then these failure rates will not be detrimental to system integrity.

Thus the systems design described above (see Figure 1) should be an excellent realization of multiplexer requirements. All of the problems encountered in the PMX-1 are eliminated, and several refinements are added for flexible and reliable operation of the device. The cost is very small compared to having separate analog lines from each sensor, or to having a separate A-to-D converter and digital communications link for each line

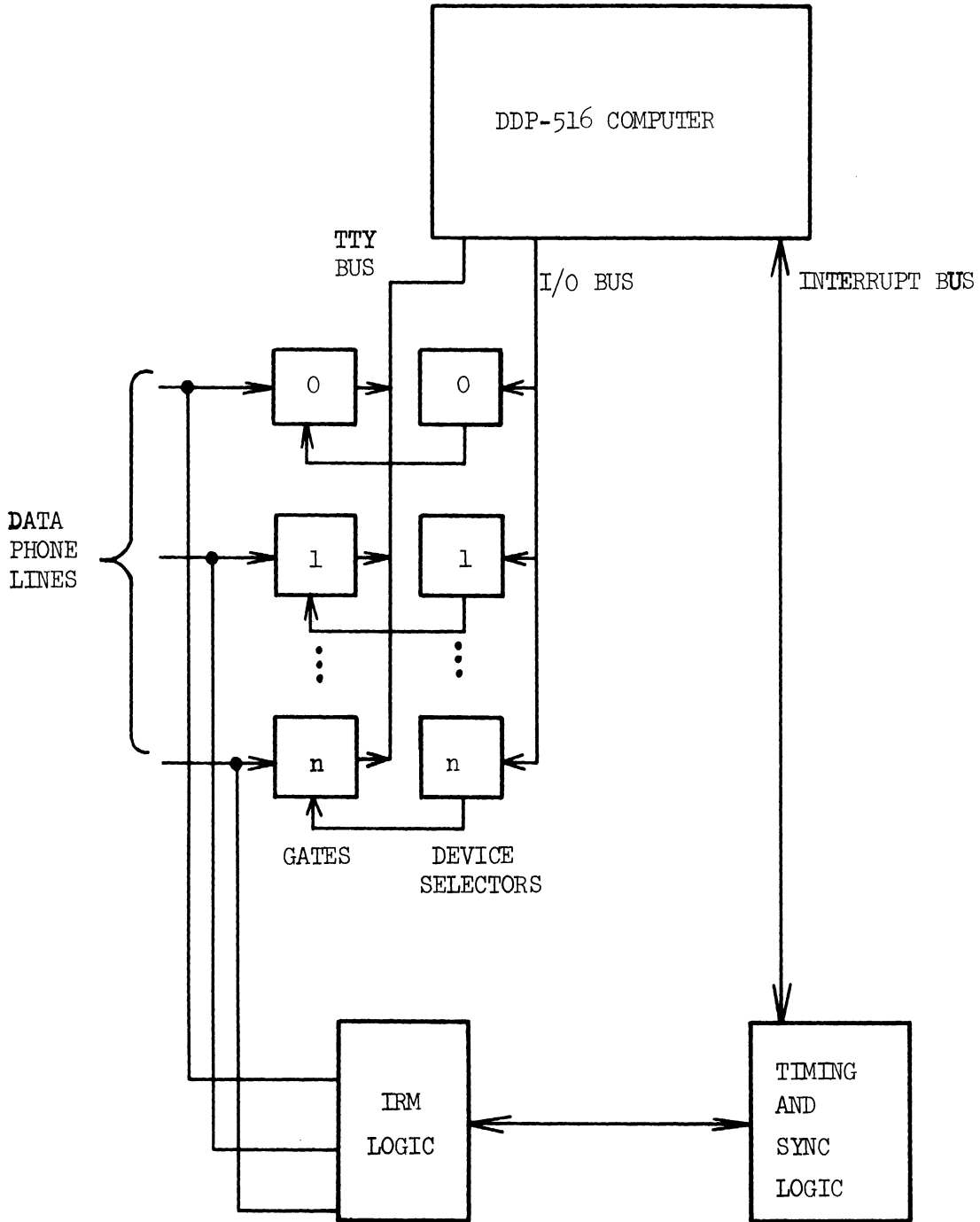
and relay in the system. The MTBF of the multiplexers should exceed ten years, and servicing would be easy due to built-in marginal testing facilities and modular construction. Maintenance, other than periodic marginal testing, should be non-existent, and many tests can be performed by the programmer. The PMX-2 should certainly fulfill the requirements of data and instruction multiplexing at the substation level.

So far, nothing has been said about multiplexing at the central computer location. This location is the termination point for 30-50 Dataphone lines, and all of these lines must be capable of communications with the DDP-516 on a one-at-a-time basis. Since the DDP-516 has teletype I/O facilities built-in, then it clearly has all of the necessary equipment for handling one such line with no required interfacing. Therefore, the function of the multiplexer is to connect the proper telephone line to the computer under program control. In addition, circuitry must be provided for synchronization and for monitoring interrupt requests. The proposed organization is shown in Figure 4. A device selector, which decodes appropriate bits of the DDP-516's memory buffer register, is provided for each terminating line. These selectors enable electronic switches (gates) which connect the appropriate telephone line to the DDP-516's teletype input bus. The DDP-516 already contains serial/parallel conversion equipment internally. In addition to these device selectors and gates, logic is required to generate synchronizing signals for the Dataphone lines and to monitor interrupt requests. The DDP-516 is connected to only one line at a time, but if a carrier is sensed by the IRM on any other than the line being presently monitored, then upon completion of the present cycle, the mainframe is interrupted, and a search is begun to find the line requesting the interrupt.

Most of the above hardware can be provided by the computer manufacturer as an off-the-shelf item, and only minor additions or modifications will be required for compatibility with the system.

DDP-516 Multiplexer

Figure 1.4



## Chapter II

SENSING, MULTIPLEXING, AND ANALOG TO DIGITAL CONVERSIONA. Introduction

At each substation real and reactive power must be determined, and sent in digital form to the local computer. This operation may be broken into three separate operations:

1. Sensing power (analog).
2. Data concentration (analog multiplexing).
3. Analog to digital conversion.

Four factors must be considered in the design of these subsystems: speed, accuracy, cost and reliability. Within these requirements and restraints, the final system was chosen.

B. Sub-System Description

The real and reactive power on each line is sensed by thermal converters, which give a proportional, low level voltage output. The analog voltage levels are then multiplexed to an analog to digital converter by reed relays through an operational amplifier. The proper relay is chosen by the substation control unit. The conversion takes place in an "up counter" type analog to digital converter when a pulse is received from the control unit and an output pulse occurs when the conversion has been completed. At this time the converter contents are jam transferred into the control unit.

### C. Sensors

The most important considerations in choosing power sensors were cost and accuracy. Time is only important when considering computer and conversion time since the system is not to provide responses to high speed system changes as would be required by faulty location and transient detection.

A reasonably priced low speed power sensor is currently used for economic dispatch that meets system requirements for accuracy (better than 1%). This device, supplied by the Sangamo Electric Company, is a thermal converter that produces a 30 millivolt nominal output at a cost of \$150 per phase, i.e., \$600 for total real and reactive power per line. The time response is 90% of full value in one second.

Other methods of power sensing were considered; e.g., wattmeter with optical sensor and high speed digital and analog sensing and associated multiplying units; however, accuracy, reliability, and development cost considerations indicated these to be less feasible approaches.

### D. Data Multiplexer

Rather than running individual analog lines from each sensor to the first level computer, it was decided to multiplex the analog signals and convert the information to a digital number at the substation. Besides reducing the expense of communication lines, this offers the added advantage of accuracy of digital data transfer, thus maintaining the accuracy required for economic dispatch. Due to the low level of the signal, either operational amplifiers would have to be used at the output of each sensor or a multiplexer with a

very small offset voltage would be necessary; offset voltage being the voltage drop across the multiplexer. For economic reasons the second approach was taken, requiring only one operational amplifier per substation. Solid state multiplexers are available, however, they are quite expensive and the offset voltage is too great for the desired accuracy. Offset is inherent in solid state switches, due to the voltage drop across the switching transistor. A typical offset voltage is 200 microvolts, which would mean an error of 1.3% at half load. The offset voltage is also a function of temperature, so that a correction factor could not easily be introduced. Since the speed provided by the solid state multiplexer is not necessary, a circuit was designed to employ reed relays; which have negligible offset voltage, operate times as low as 1 milliseconds and release times of less than 1 millisecond (the circuit design is provided in the appendix). At one operation every four minutes, a typical reed relay of many million operations would last indefinitely at 15 years per million operations.

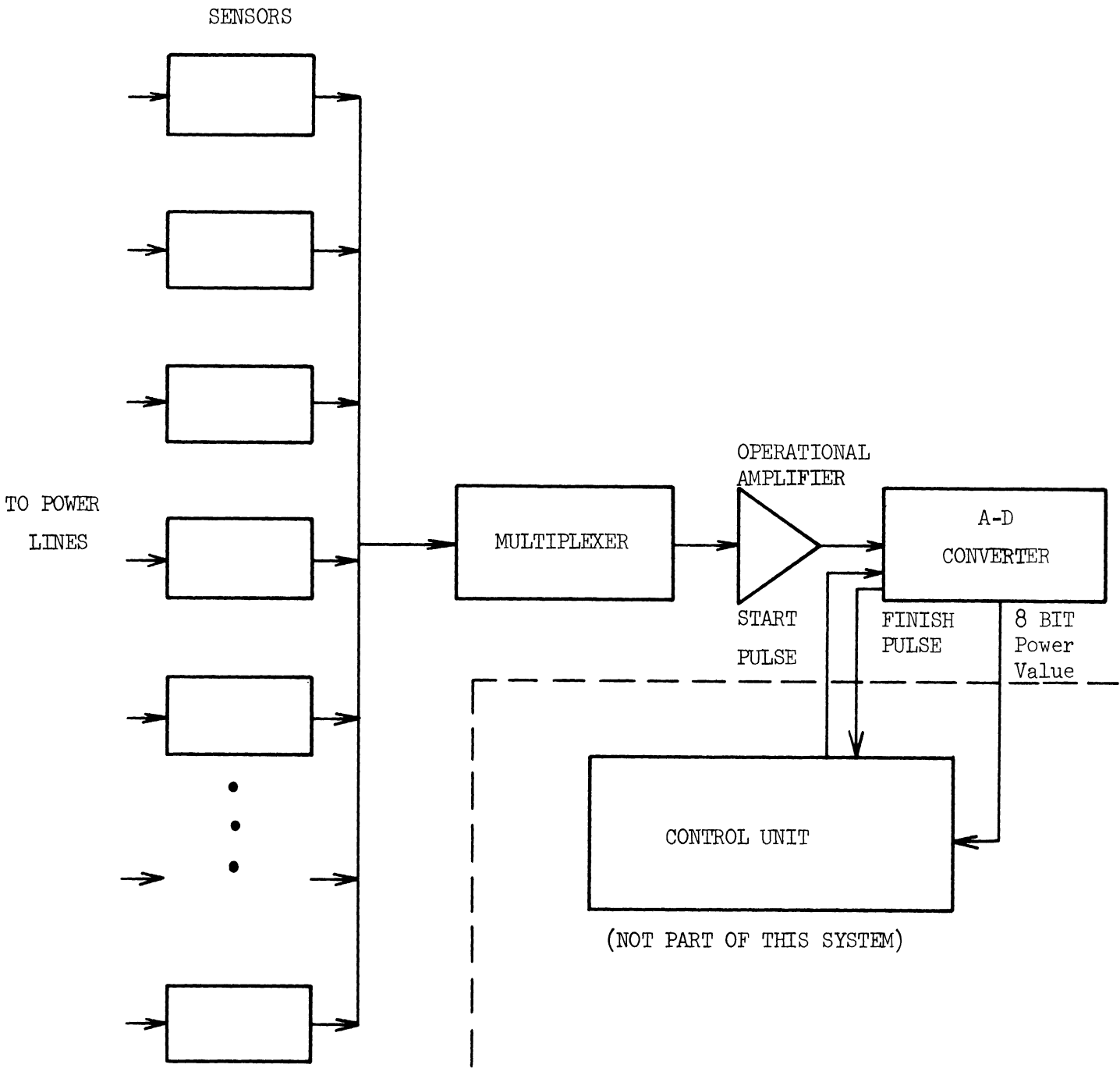
#### D. Analog to Digital Conversion

After the multiplexed signal is fed through an operational amplifier, it is to be converted into digital bits to be fed into the substation end of a digital multiplexer to be sent to the computer. The analog to digital conversion works as follows: the analog signal is fed into a voltage comparator where it is compared to an analog signal. This signal is proportional to the digital number stored in a flip-flop register. This register is initially set to zero and is incremented by pulses from a clock, gated by the comparator. The clock pulses are counted in the register until the number in the register

equals the analog signal value. The contents of the register are then transferred into the digital multiplex buffer register, the register is reset, and an output pulse is sent out. The unit then awaits a start pulse from the digital multiplexer. An additional circuit is required to end the conversion if the input signal is zero. (See block diagram) With an 8 bit register and a 2 MHz clock, it requires under 260 microseconds for the maximum conversion time. Allowing 2 milliseconds for relay closure and the damping of transients, .5 milliseconds for conversion time and 1 millisecond for relay opening, the operation would require less than 4 milliseconds per sensor.

Other methods of analog to digital conversion were considered but eliminated because of disadvantages in reliability and/or cost. For example, an up-down counter may be used instead of the chosen up counter. This can be used when sampling a changing signal, however, it loses its advantages vs. cost when multiplexing analog signals. Another possibility is to compare the analog signal with a saw-tooth analog voltage while counting clock pulses in a register until the two are equal. Besides the added expense of the saw-tooth generator, circuits would be required to maintain proper timing between the saw-tooth analog signal and the clock pulses. The up counter is simple, reliable, inexpensive, independent of clock frequency and well suited to analog multiplexing.

The total cost of the converter using Digital Equipment Corporation components is \$620; however, with the advent of inexpensive integrated circuits, a reduction to as little as \$200 is not unreasonable as an initial estimate.



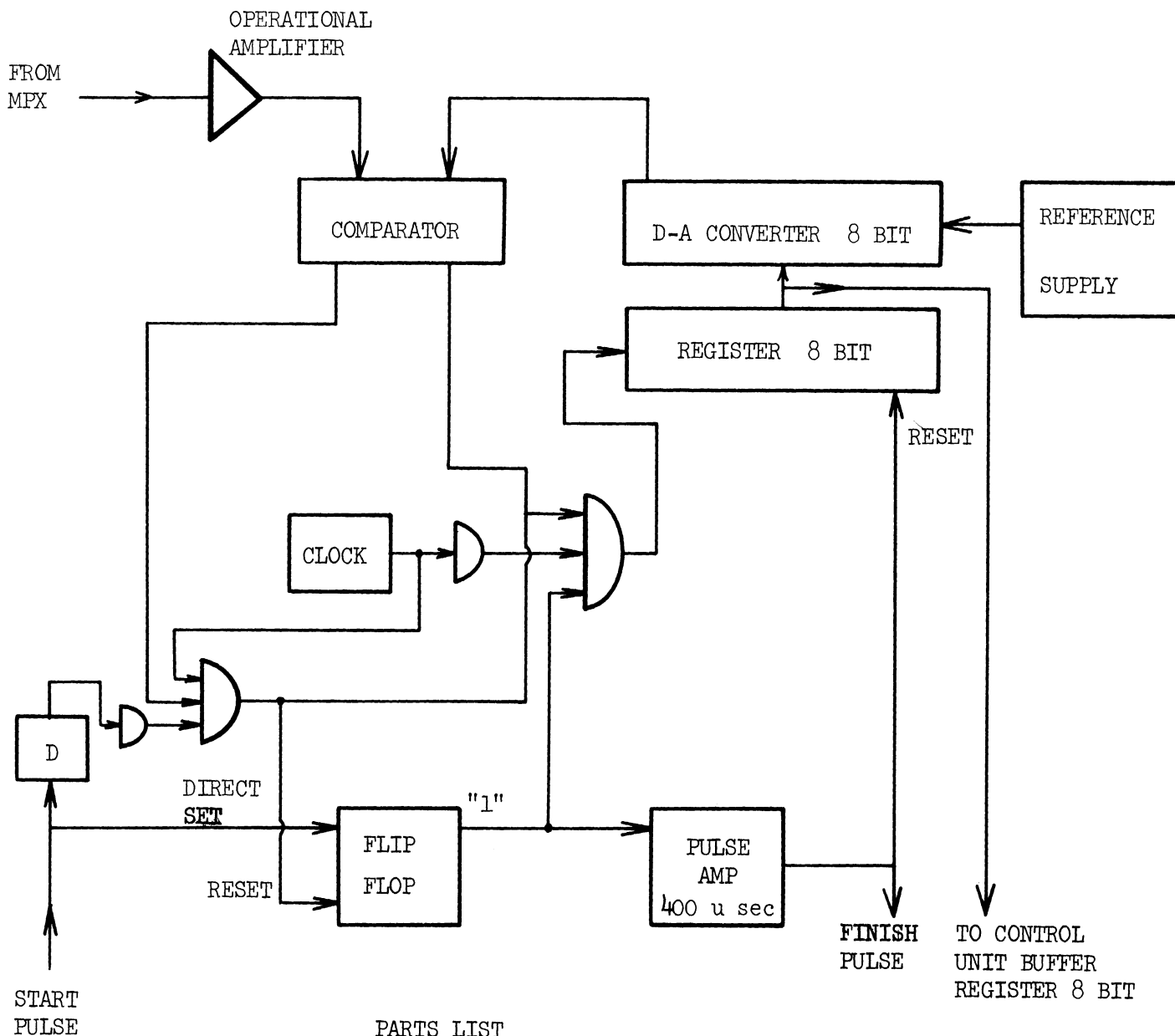
SYSTEM BLOCK DIAGRAM

Figure 2.1



Analog To Digital Converter Block Diagram

Figure 2.2

PARTS LIST

<u>QUANTITY</u>	<u>DESCRIPTION</u>
4	Gates
9	Flip-Flops
1	One Shot
1	Clock
1	Pulse Amplifier
1	Voltage Comparator
2	Digital To Analog Converters (3 bit)
1	Digital To Analog Converter (2 bit)
1	Reference Supply

The above circuit has been wired and tested using digital equipment logic.

Economic Summary:

The following is an economic breakdown of the subsystem:

1. Sensors                      \$600/line
2. Multiplexers                \$ 6/line
3. A-D Converter              \$200/substation

## Chapter III

COMPUTER RESPONSIBILITIES AND PROGRAMMINGA. Introduction

The setting of relays requires a vast amount of data about power flow, relay characteristics, and of course, grid layout. There now exist some computer programs which calculate proper settings given all this data. These programs are generally run off-line and the output (the correct settings) is used to set the relays by hand. Because of the time involved in physically going to each relay to set it, relays are usually only reset for seasonal change. A means of remotely setting relays could aid in maintaining system stability (especially where three terminal lines are involved.) This report deals mainly with the setting of distance relays since the majority of relays in use today are of this type (approximately 95%).

B. Choice of Computer

It was decided that several small computers would be more practical and economical than one very large computer because of the vast amount of storage required, and the distances involved in setting up communication for the entire system. Since the system can be easily divided into sections, several small computers could handle the job nicely.

The following were the criteria used in choosing a computer:

1. adaptability to this specific use
2. data transfer capabilities

3. reliability, and of course,
4. cost.

There are several computers which could be considered, among them Digital Equipment Corporation's PDP-8, Scientific Data System's Sigma 7, and Honeywell's DDP-516. The 16-bit word in the DDP-516, compared to the 12-bit word in the first two machines above, facilitates easy data handling and table setup (see Figures 3.2 and 1.3). The DDP-516 also has higher reliability due to its integrated circuit construction. The cost is slightly more than that of the others but the increased reliability and less programming required due to its easier data storage makes it more economical. The cost per computer is \$25,000.00. This price includes a 4096 16-bit word random access core and an ASR-35 teletype. The cost of the integer multiply hardware option and data transfer option is \$10,000 so that one computer unit cost would be \$35,000.

### C. Algorithm

The basic algorithm for the system operation is outlined in flow chart form (see Figure 3.1). The system is designed to remotely set and read distance relays, read power flow (both real and reactive) and direction, and be automatically notified (by computer interrupt) when a fault is detected. The program scans the power flow information and checks to see if there have been any changes since the last data input. Then it calculates the necessary relay setting to take care of all changes and again inputs system status data. Because of the computer's inherent speed, there should be no problem in re-

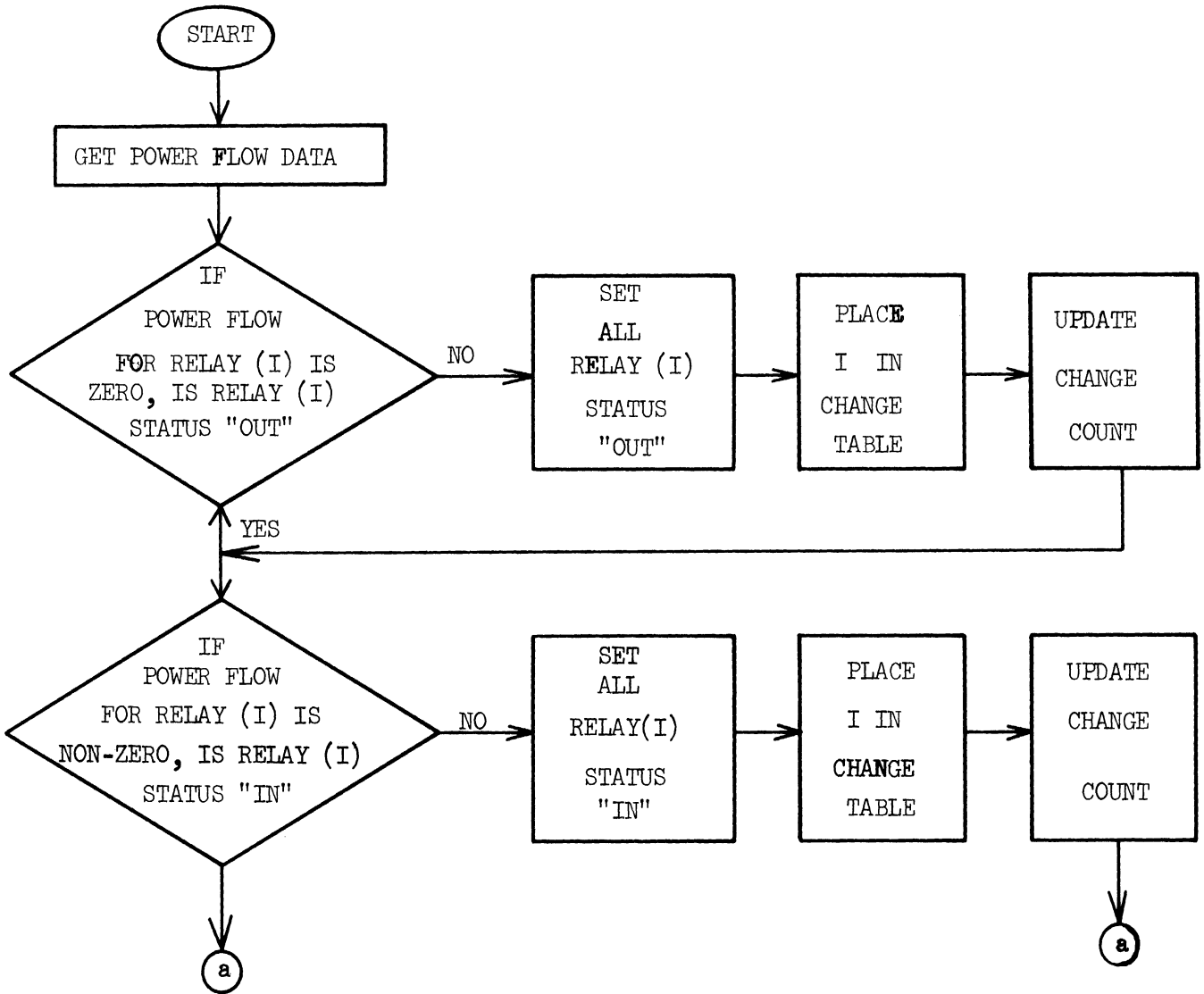


Figure 3.1a

General Flow Diagram (cont.)

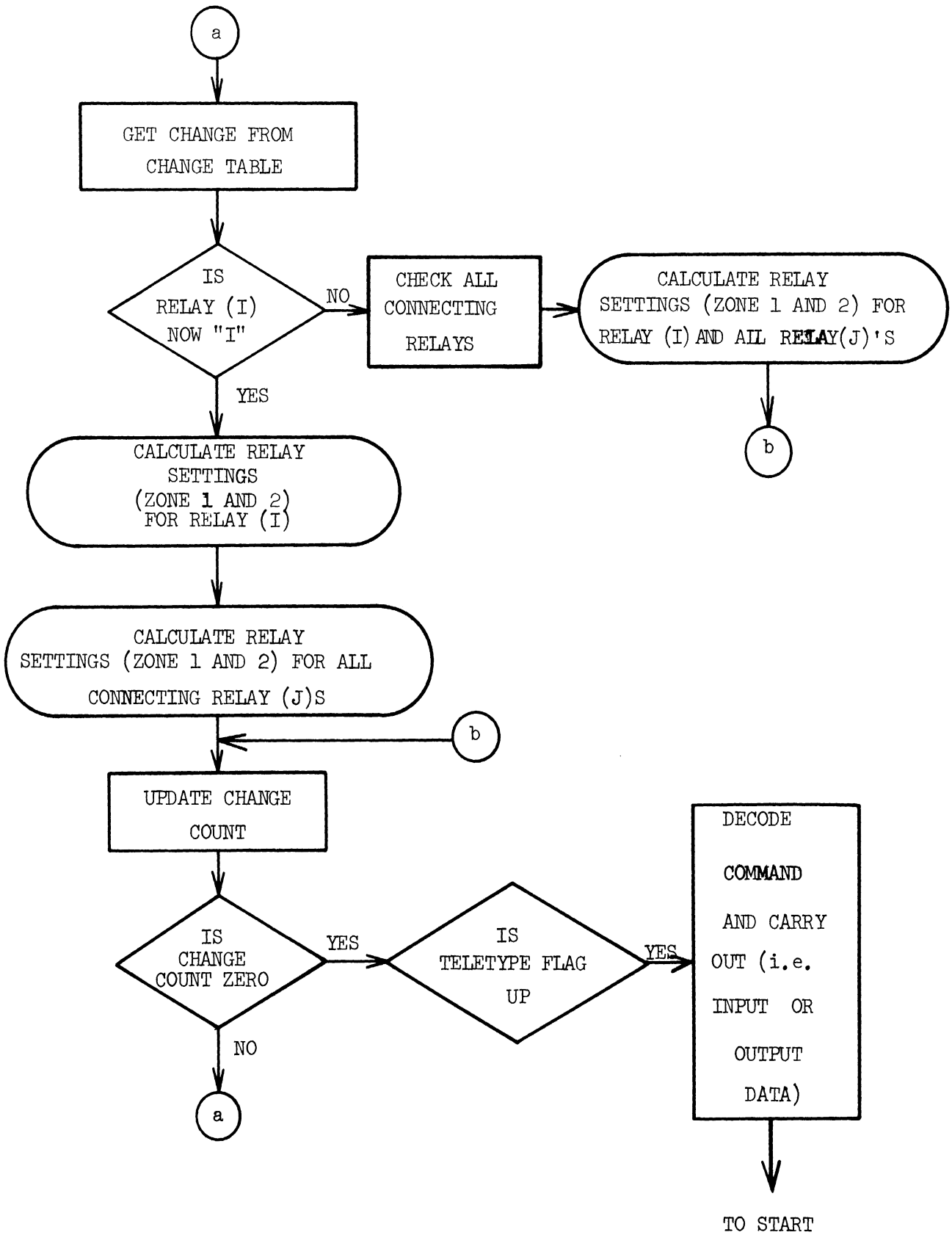


Figure 3.1b

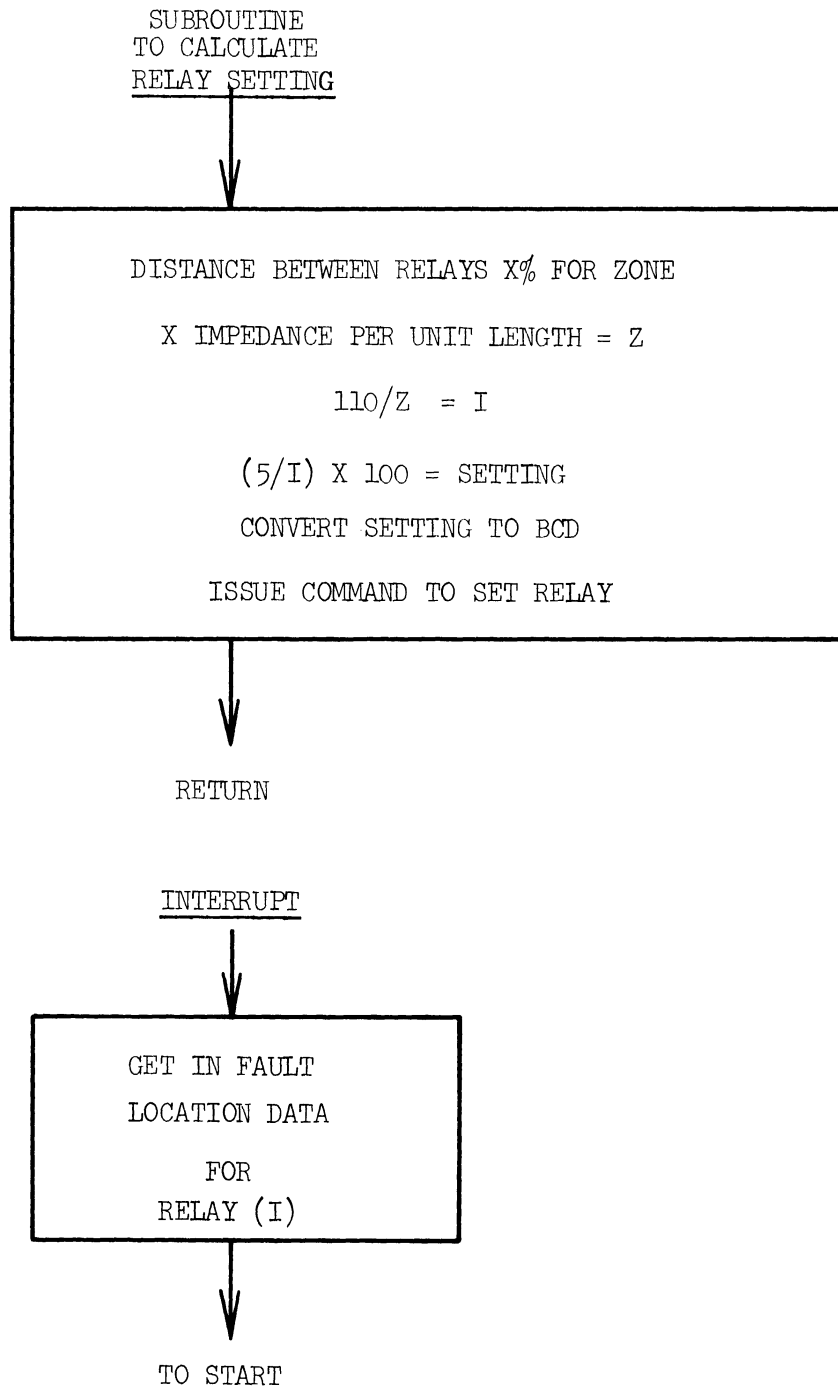
General Flow Diagram (cont.)

Figure 3.1c

setting relays in plenty of time to take care of most faults that might occur.

Each computer is multiplexed to about 50 substations or approximately 225 relays. These relays are within that computer's "realm." The tables in one specific computer deal only with the relays that that computer controls.

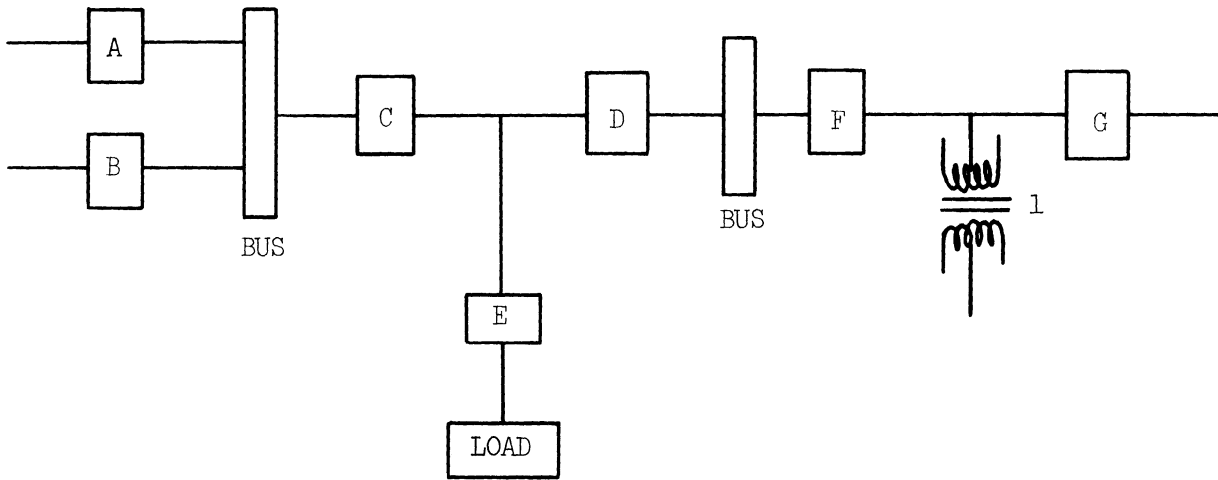
Operation of the program requires information about the system layout to be stored initially into tables. Specifically, the relay information tables (see Figure 3.2) must be set up. This requires that, for each relay in the system, all connecting relays, distances to them, and the substation with which they are associated, be specified, and the corresponding line impedance per unit length be input. For example, see Figure 3.3. This information need be entered only once and kept updated as lines are added. Of course, such information as the desired Zone 1 percentage and Zone 2 percentage must be entered. Software should allow these tables to be entered more easily. See Appendix V for examples of DDP-516 programming for the system.

It should be noted that in three terminal lines a Zone 2 setting may not always be possible. A Zone 2 setting should reach any relay that the Zone 1 setting does not reach but then the setting could greatly overreach in the other direction. The latter case really need not be considered, though, because in that situation a pilot wire is generally connected between the relays to force tripping.

Communication between computers must be implemented. A relay setting within computer A may depend upon power flow in a line that is not within computer A's realm, i.e., that is multiplexed to a







<u>RELAY</u>	<u>CONNECTING RELAY</u>	<u>DISTANCE</u>	<u>CONNECTION TYPE</u>	<u>IMPEDANCE</u>
C	A	0	3	--
C	B	0	3	--
C	E	14	0	.8
C	D	12	0	.8
D	C	12	0	.8
D	E	10	0	.8
D	F	0	3	--
E	C	14	0	.8
E	D	10	0	.8
F	D	0	3	--
F	G	6	0	1.0
F	1	8	2	1.0

Example Grid With Initial Input Required For It

Figure 3.3

to a neighboring computer. For this reason, "exterior information" (see Figure 3.2) must also be included within the realy information tables so computer A can properly access computer B to get the necessary information.

Communication by teletype allows reports to be printed out, tables to be queried, and changes or commands to be entered. Relays could be read right from the computer station at any time or power flow data could be gathered.

The power data is input whenever a command to "Begin Sequential Conversion" is given. The data is received through the accumulator in the format of Figure 1.3 and is stored into the power flow data table. Then all of the power flow data is checked for zero or non-zero and the bit for the corresponding relay status checked against this input. If any discrepancy is found, that relay status bit is changed and the relay designation put into the "change" tables marked for a later setting change. After all relay status bits are checked, the changing of settings is started. If the change was from "in" to "out" on a specific relay, there is no need to change that relay's setting but the connecting relay settings need to be changed. If the change was from "out" to "in" the relay settings for connecting relays and the specific relay will need to be changed. (Actually, in most cases, a relay changed from "out" to "in" does not require resetting of that relay because it was correctly set before it went "out.")

The equations for determining a relay setting are as follows:

$$D_{\text{total}} \times \% = D$$

$$D \times (Z/wD) = Z$$

$$110/Z = I$$

$$5/I \times 100 = \text{setting}$$

where  $D_{\text{total}}$  is total distance to nearest connecting relay, as defined in RELAY INFORMATION TABLE,  $(Z/wD)$  is the impedance per unit length for the line,  $\%$  is the Zone 1 or 2 percentage impedance desired. The distance relays which this system uses are normalized to 110 volts, 5 amperes and have settings ranging from 0 to 99. The command is output to the multiplexer to SET RELAY when the correct setting is calculated. All other connecting relays are similarly reset. The other changes within the change tables are handled. If there are any teletype commands, they are taken care of. Then the whole system is rescanned. When an interrupt occurs, scanning is immediately begun again in order to take care of the fault.

#### D. Options

If a very large central computer were in communication with all of the several DDP-516's, economic dispatch information or z-matrix and overcurrent relay settings could be calculated. Tsien ("An Automatic Digital Computer Program for Setting Transmission Line Directional Over-Current Relays", IEEE (83) 1964) describes an algorithm of forward and backward checking to set overcurrent relays. Hale and Ward ("Digital Computation of Driving Point and Transfer Impedances, AIEE Transactions (76) Pt. III, Aug. 1957) describe a method of z-matrix calculation. It would be impossible to do these types of computations with a DDP-516 complex because of the large computation time required. This would not allow sufficient scanning and checking time to maintain the scanning

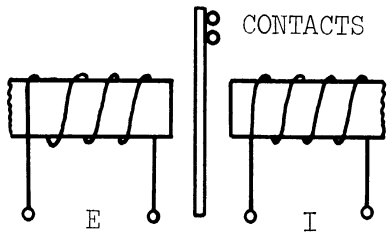
system proposed. A disc and cathode ray tube also would be very helpful on this system. A map of the grid stored on the disc and called out onto the CRT for modification would eliminate the necessity of entering all the connecting relays in the form as described above.

## Chapter IV

RELAY SETTING CONTROL INTERFACEA. Relay Description

The project objective is to provide coordinated relay settings for all relays in the system on the basis of generation and load conditions. The most basic necessity is to provide an interface device to implement the computer directives at the relay location. The relays of interest are of the directional distance type, and generally control three zones. The first zone relay provides instantaneous tripping for nearby faults. The impedance seen by this first zone relay varies with generation and load conditions. The second zone relay, if used on three terminal lines, also sees changes in load and generation conditions and therefore must be regulated. The third zone relay functions solely as backup protection and can be satisfactorily preset to some permanent value.

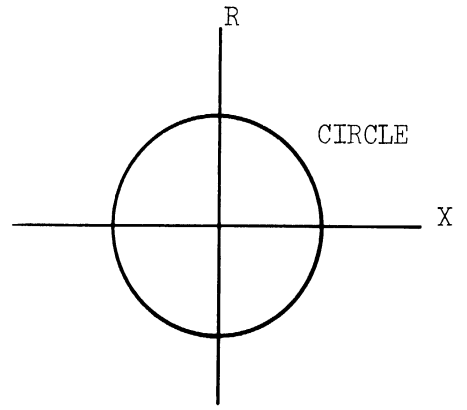
All distance relays operate by comparing the torque set up by a current coil winding with that set up by a potential coil winding. An example of this is the simple impedance relay element as shown in Figure 4.1. Thus, in effect, we have a measure of the transmission line impedance as seen by the relay. Under all conditions this impedance is not a true measure of distance along the line, and therefore the need for the mho and ohm units as shown in Figure 4.2. In these relays the torques are not proportional to current or voltage alone, but rather to the product of the current and voltage with a third quantity, which produces a polarizing flux. Any scheme to



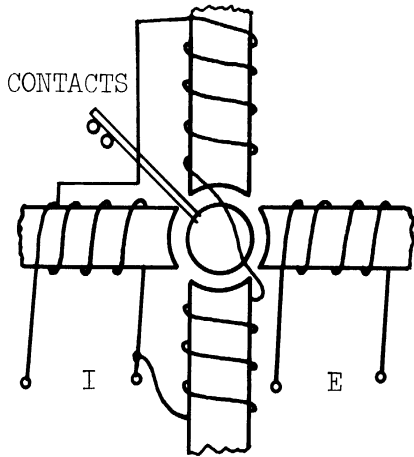
SCHMATIC

Impedance Unit

Figure 4.1.

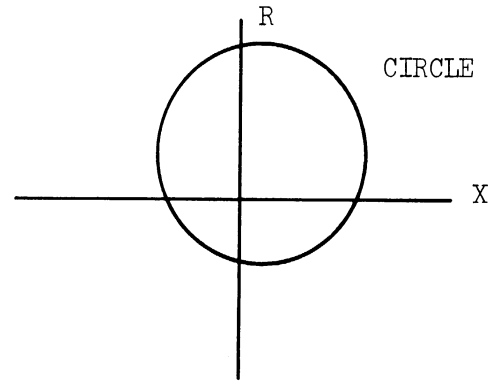


CHARACTERISTIC

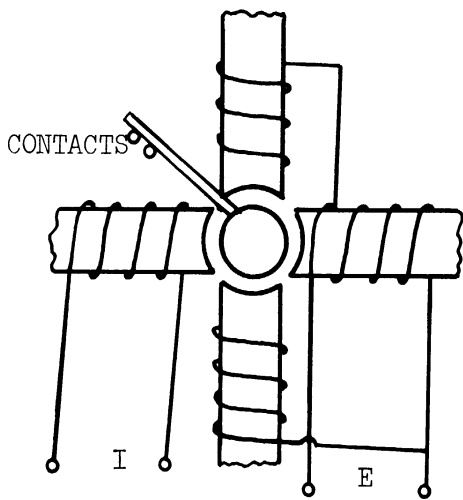


SCHMATIC

A. Ohm Unit

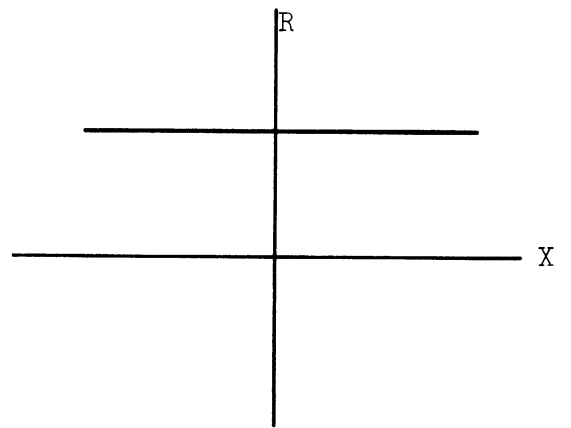


CHARACTERISTIC



SCHMATIC

B. Mho Unit



CHARACTERISTIC

Figure 4.2.

vary the value of current at which the relay will trip must involve varying the torque produced by this current. This requires varying the flux produced by a given current. This is done by changing the number of turns in the current coil by a tap block arrangement. The number of turns in the current coil is determined by two tap plugs, one for the ten scale and one for unit scale (see Figure 4.3). Thus, we can change the torque produced, in steps of 1%, in relation to the counterbalancing torque produced by the potential coil.

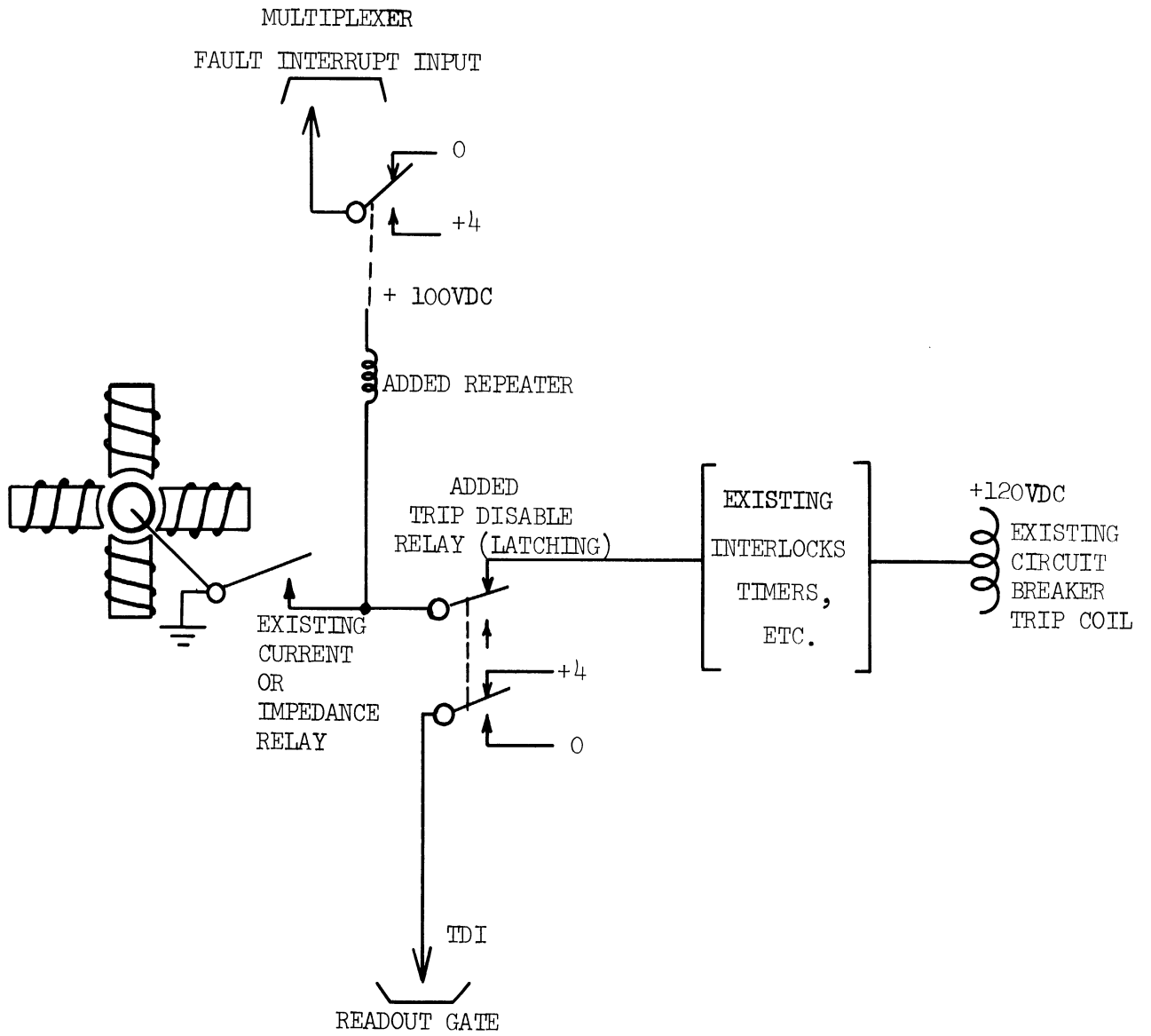
Our interface system will change the tap settings of the current coil by the use of switches to activate the desired taps. The settings for the directional distance relays have always been determined on a compromise basis to satisfy all line conditions. To our knowledge no attempt has ever been made to remotely control these settings in either an independent or coordinated manner.

#### B. Design Requirements

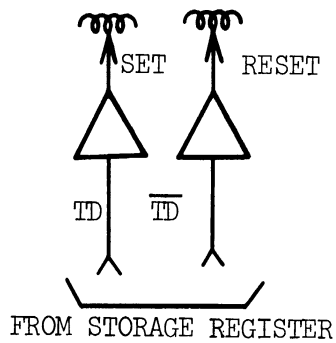
For optimum reliability and usefulness, the system must be able to satisfy the following design requirements:

1. Under no conditions can the switching operations open the secondary of the current transformer. Opening the circuit would allow extremely high voltage in the circuit and cause failure.
2. Should switching system power fail, the relay must maintain its last tap setting. The power for the switching system must come from source independent of the line it is controlling.
3. The computer must be able to interrogate the relay to obtain its tap setting.
4. The system logic must provide a means for the computer to





TRIP DISABLE DELAY



Relay Trip Circuit

Figure 4.3

test the relay function without tripping the line. This is referred to as on-line testing.

### C. Choice of Switch

A switch contact is required for each tap position in both the ten's and unit's scales. Electromechanical and solid state methods of performing the switching of these taps was investigated. All tap switching schemes require a logic package to receive and decode the computer command word and activate the proper switching functions. Since the basic structure of the logic required will change relatively little with different choices of switching device, the cost of logic circuitry is considered fixed and does not influence the selection of the switching device.

An arrangement of discrete electromechanical relays is described in Appendix III. Because of its cost and the physical space required this scheme was eventually rejected. Solid state tap switching using Silicon Controlled Rectifiers was extensively investigated. The SCR switching performed satisfactorily but was judged lacking in reliability and excessive in cost. This is detailed in Appendix IV.

The optimum switching device is regarded to be a rotary switch with bidirectional stepping drive. This arrangement requires a two section switch for each group of taps to be selected: a standard, make-before-break, heavy duty deck to handle the normal and fault current to the relay current coil from the current transformer; and a light duty BCD deck to provide the switch position in digital form to the position control circuitry and to the computer. Bidirectional drive enables setting changes without going through a complete revo-

lution of the switch. Make-before-break contacts are used to prevent an open circuit condition on the secondary of the current transformer. Since the switch is mechanically detented no power is required to hold its position and power failures will not cause loss of settings.

The switching device chosen is a combination of standard stock items and is readily available in any desired quantity and at a cost considerably less than discrete relays or SCR's. The power required for the logic can be supplied by the multiplexer and the supply for the stepping drive for all relays in the substation can be provided at low cost. This allows relay setting to be performed independent of the power on the line to be regulated.

#### D. Logic and Function Design

The control logic in each relay has several tasks: it must recognize its selection by the multiplexer; receive and store a command word; decode this command and perform the ordered functions; feedback tap switch positions and status to the multiplexer; and provide relay contact closure information to the fault interrupt inputs of the multiplexer. Analog and digital techniques are used to achieve these functions.

The relay trip circuit is modified to provide status information and on-line testing as shown in Figure 4.3. A REPEATER converts contact closure of the distance relay being controlled into appropriate binary levels to connect to the fault interrupt inputs of the multiplexer. This line is not gated and gives full time monitoring of the distance relay status. On-line testing is made possible by a TRIP DISABLE latching relay connected between the distance relay contacts

and the rest of the trip circuit, including timers, interlocks, and the circuit breaker trip coil. The status of this TRIP DISABLE relay is sent to the multiplexer along with the switch positions. Control of the TRIP DISABLE relay is accomplished using bit 7 of the command word. With the TRIP DISABLE relay actuated the taps may be changed to force operation of the distance relay without interrupting service.

The tap changing mechanism, shown in Figure 4.4, consists of two rotary switches with bidirectional stepping drive as discussed previously. One switch and positioning circuit is used for the 10% tap changes and a second is used for the 1% tap changes. The position command for each switch and the position feedback from the BCD deck of the switch are each in the form of four binary bits. These bits are converted to equivalent analog levels, subtracted, and a comparison of the results controls the stepping pulse inputs to the switch stepping motor. If the demanded position is less than the present position the switch is stepped-up at 1pps until the position agrees with that command. The down stepping process is exactly similar except for direction. The four bit position command inputs are obtained from the local storage register and the four bit position outputs are fed to read-out gating.

As shown in Figure 4.5, command read-in is accomplished by gating the multiplexer operand bits into RS flip flops which form a local storage register. This gating is enabled by two actions. The device selector gate in the particular relay must recognize its particular device code, and the IN/OUT direction line must be set for inward transfer of data. If the device code is not recognized or the IN/OUT line is set for outward transfer there is no read-in of data. If the device code is recognized and the IN/OUT line is set for outward trans-

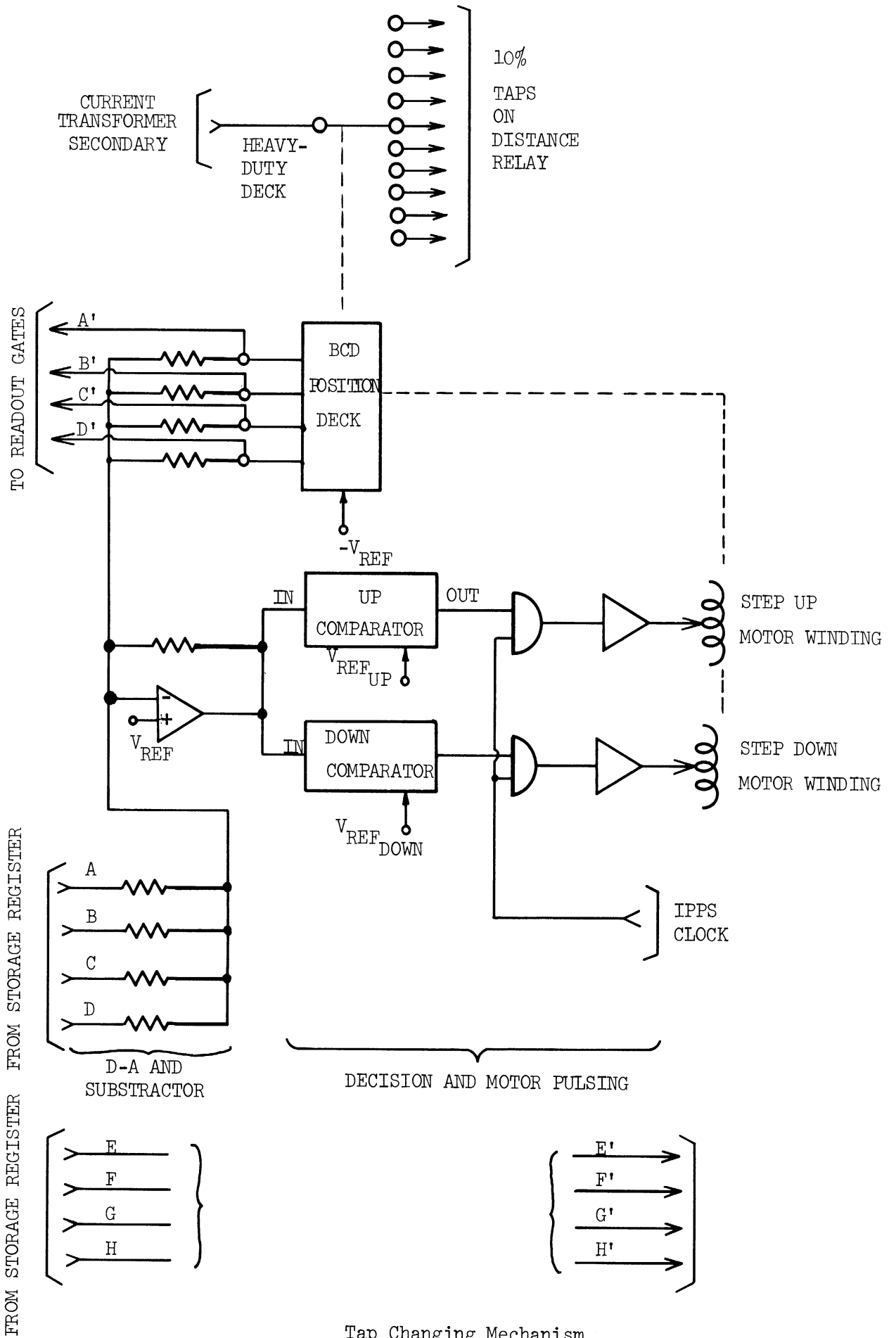
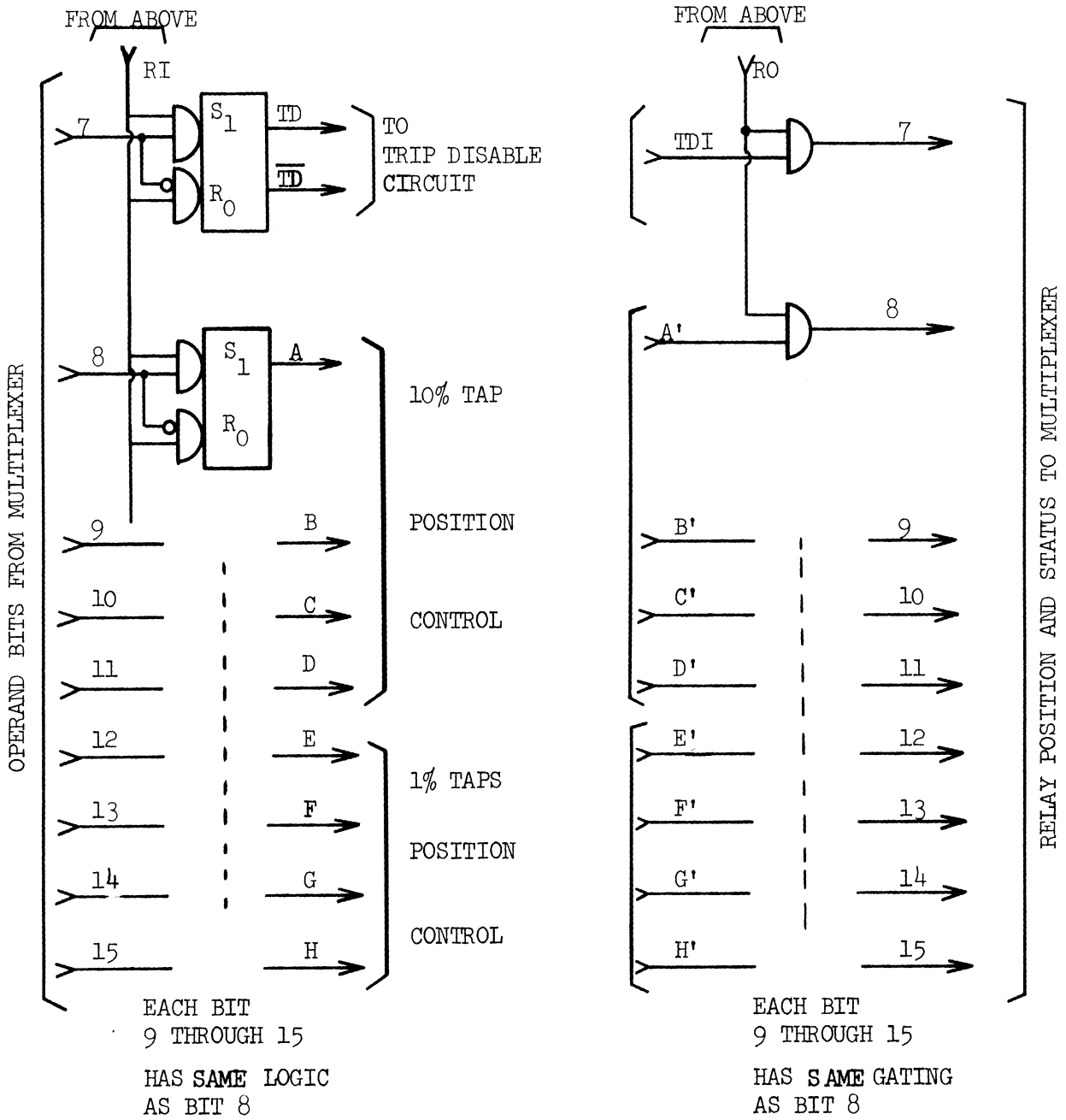
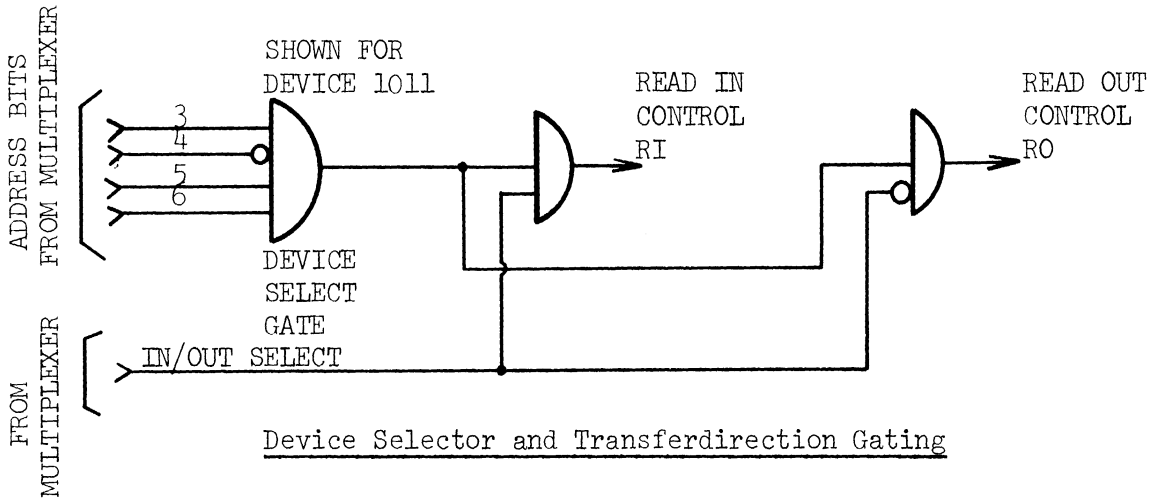


Figure 4.4



Device Selector Storage Register Readout Gating

Figure 4.5

fer of data then the position outputs from the switches and the status signal from the TRIP DISABLE relay are gated to the multiplexer in the same format as the commands arrive--bit seven is the trip disable/trip disable status, bits 8 through 11 are the 10% taps position command/position readout, and bits 12 through 15 are the 1% taps position command/position readout. Bits 3 through 6 from the multiplexer serve as the address bits to the device selector gates.

Power for the logic and amplifiers is derived from the multiplexer. The stepping switch motor power is supplied by a simple AC power supply with redundancy achieved by using the local substation DC supply. Since the stepping motor requires only pulses for operation, an RC combination is used to supply the motor coils. This enables large pulse currents to be drawn while keeping the average current drain low.

#### E. Costs

As previously mentioned the cost of the tap switching methods just described is the least of all investigated. The cost breakdown is as follows:

Logic Circuitry	\$25.00
Position Control	30.00
2 Rotary Switches and Motor	60.00
Packaging, etc.	35.00
	<hr/>
Total cost per distance relay to be controlled	\$150.00

It might be well to note that these are upper limits of cost estimates made.

## Chapter V

COMMUNICATIONSA. Introduction

In a computer oriented system, communication is very important. The communications must be inexpensive enough to allow the complete system to be economically feasible yet must be fast enough for the system to complete its required tasks.

There are three basic methods of communication:

1. Pair of wires can carry up to  $6 \times 10^6$  bits per second.
2. Coaxial channel can carry  $3 \times 10^8$  BPS one way. A coaxial cable with ten channels each way can carry  $6 \times 10^9$  BPS.
3. Wave guide can carry  $1 \times 10^{10}$  BPS in two directions.

Two forms of these are commercially available to us, phone lines (voice grade channels) and microwave links.

B. Speed Requirements

Preventive, not corrective, system fault protection will be used. Since the present system will involve relay checking and economic dispatch only, a communication rate of 5000 BPS will easily be sufficient.

The voice grade channels can carry digital information at the rate of 5,000 to 9,000 BPS.

A microwave link would be able to handle data at the rate of 15,000 BPS.



C. Component Costs

Digital data sent over voice grade phone lines costs \$1.00 per mile per month for the lines plus \$10.00 per month for terminal facilities if these are leased from Bell Telephone.

Microwave data transmission costs \$20.00 per mile per month plus \$15,000 for transmitting equipment and another \$15,000 for receiving equipment.

Transmitting equipment to send the data in analog form costs \$12.00 per month, receiving equipment costs \$26.00 per month and lines cost \$10.00 per month plus long distance charges.

Also, microwave transmission requires construction of small buildings for the transmitting and receiving equipment which costs a minimum of \$2,000 each.

Since digital lines must be used for relay checking, and since the analog equipment is more than the digital, it was decided to convert the analog information to digital and do all data transmission digitally.

Also, because of the huge costs of microwave equipment and because voice grade phone lines will be fast enough for economic dispatch and relay checking, voice grade phone lines will be rented from Bell Telephone.

Should the system for instantaneous fault protection be changed at some later date, the changeover to a new method of communication can be made with a minimum of expense because the equipment is only being rented rather than purchased.

Data will be transmitted at 2000 BPS, which is considered a

"synchronous rate" by Bell Telephone. Therefore, no interfacing is needed between the register and the data-phone.

If with later expansion later a faster rate is needed, a buffer can be rented from Bell for \$70 per month plus \$100 for installation. One of these would be needed at each substation or other location where checking is done.

#### D. System Cost Analysis

In order to get an idea what the cost of communications would be for an actual system, a cost analysis has been done for both Detroit Edison and for Consumers Power Company.

##### DETROIT EDISON

Computer Location	Inputs	Total Mileage of lines
Warren	55	550
Superior	44	810
Walton	49	490
Victor	53	780
Sandusky	42	840
		3470 miles

See Figure 5.1.

To link satellite computers with the main computer would require another 135 miles of lines.

Therefore, the total cost to Detroit Edison for communications, with five computers, would be:

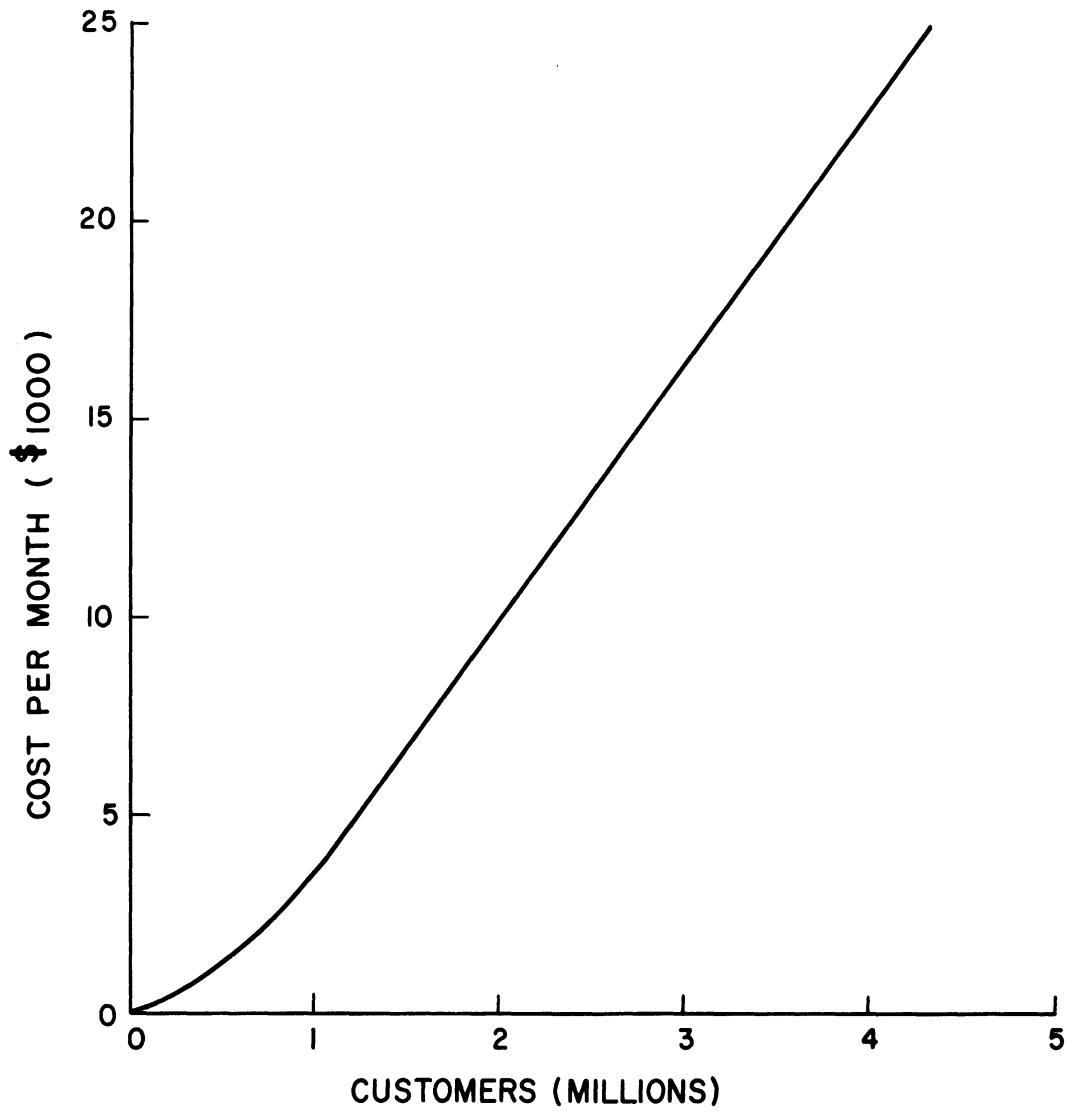


Figure 5.1

\$ 3600 per month	line costs
2500 per month	terminal equipment
<hr/>	
\$ 6100 per month	total

Along with this would be an initial investment of \$175,000 for computers.

CONSUMERS POWER

Computer Location	Inputs	Total Mileage of lines
Jackson	24	720
Grand Rapids	19	570
Saginaw	25	500
Gaylord	25	1250
		<hr/>
		2040 miles

See Figure 5.1.

To link satellite computers with the main computer would require another 320 miles of lines.

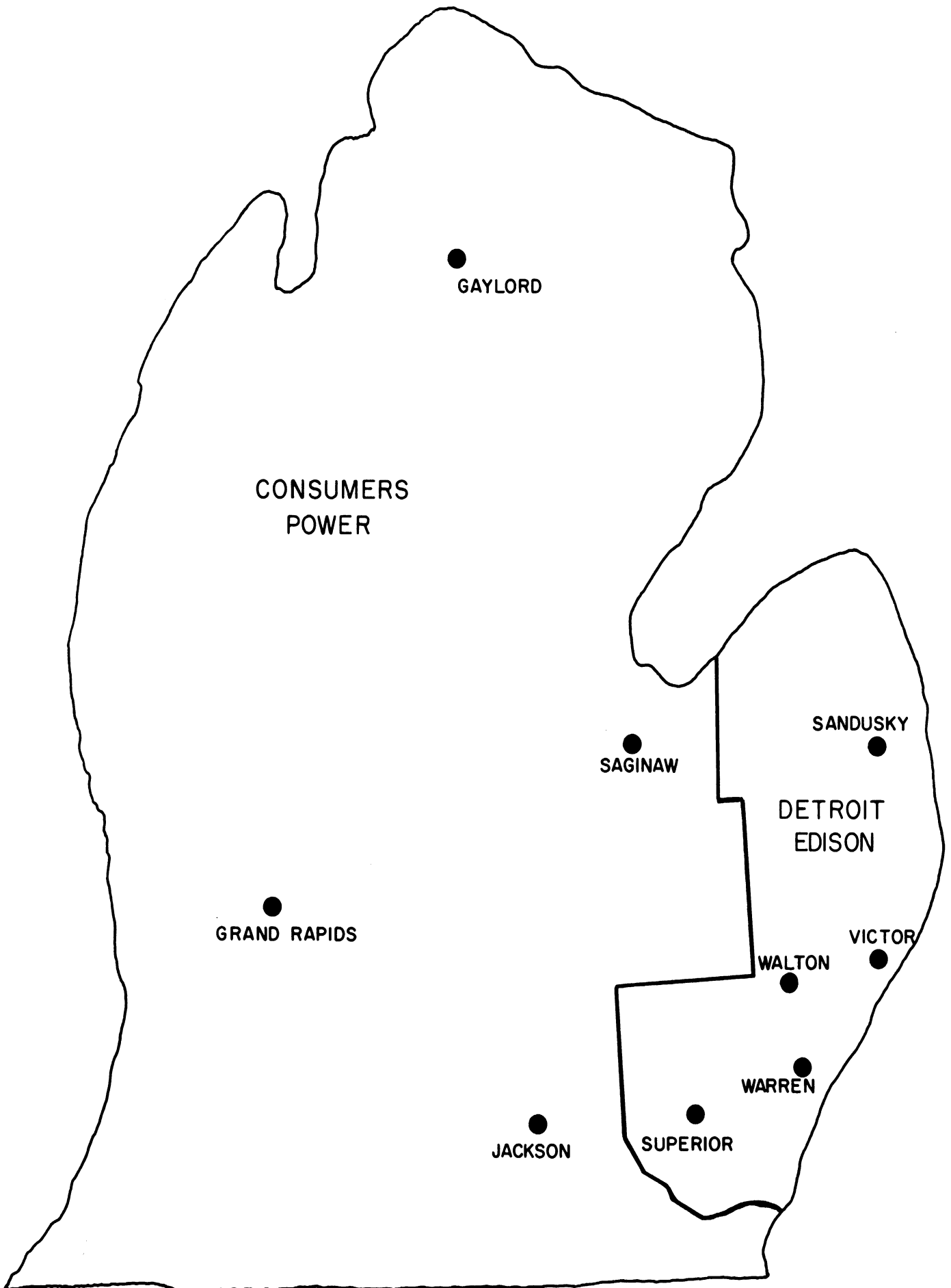
Therefore, the total cost to Consumers, with four computers, would be:

\$ 2400 per month	line cost
900 per month	terminal equipment
<hr/>	
\$ 3300 per month	total

In addition to this would be an initial investment of \$140,000 for computers.

See Figure 5.2 for an approximate graph showing the relation between the number of customers and the cost of communication to a company.

Figure 5.2



## APPENDIX I

PMX-1 ORGANIZATION AND LOGIC DESIGN

PMX-1 provided all necessary multiplexing functions for an accurate evaluation of the concept of time sharing the data and instruction dispatching operations within the substation. Six operations packages were constructed (Figure 1) so that a simple test program could be written, thus defining the programmer's role in the multiplexing process and providing some simple exercises in this aspect of the design. All required registers were included so as to effect an accurate cost analysis for future reference. The concepts of slave operation (external timing) and modular design were carried through the design religiously as consistent with the original design philosophy, and the results from this project were extremely valuable in planning the final design of a suitable multiplexing system.

The organization of PMX-1 is shown in Figure 2. A single buffer register, the OSR, is used for both data and instructions, and it contains twelve bit positions so as to be compatible with the PDP-8 computer used in the project. In order to save hardware while maintaining sufficient complexity for an accurate test, a two-line substation is simulated. Since each line terminating at a substation has both real and reactive power sensors (simulated by panel potentiometers) then only four monitor points need be addressed. Thus only two-bits of the line address register are included, along with a two-bit fault location register (FLR). A three-bit A-to-D converter and a four-point analog switch (read relay type) were constructed. In order to simplify gating, the real power, reactive power, and the FLR fields of the OSR are made disjoint, and each contains three bit positions (Figure 3), although one such position is not used in some cases. The above simplifications allow construction of the PMX-1 on D.E.C. standard Logic Laboratories (Figure 5). Indicators are provided for testing purposes (Figure 6).

PMX-1 COMMAND LIST

OPCODE  $0_8$ :     NO OPERATION                     (ACC =  $0000_8$ )                     NOP

OPCODE  $1_8$ :     SEQUENTIAL CONVERSION                 (ACC =  $0010_8$ )                     CON

          IOP $_{10}$  = OR instruction to OSR

          IOP $_{20}$  = Begin conversion (wait for data flag)

          IOP $_{1i}$  = Skip and Clear data flag if data flag = 1  
              = Do nothing if data flag = 0

          IOP $_{2i}$  = (OSR) to ACC if data flag was 1 and IOP $_{1i}$  occurred

          IOP $_{4i}$  = Clear OSR

OPCODE  $2_8$ :     FAULT LOCATION EXAMINE                 (ACC =  $0020_8$ )                     FLE

          IOP $_{10}$  = OR instruction to OSR

          IOP $_{20}$  = Initialize transfer

          IOP $_{40}$  = (FLR) to OSR and set ready flag to 1

          IOP $_{1i}$  = Skip if ready flag is 1  
              = Do nothing if ready flag is 0

          IOP $_{2i}$  = (OSR) to ACC if ready flag is 1

          IOP $_{4i}$  = Clear OSR and ready flag

OPCODE  $3_8$ :     SET RELAY (I) TO Y                     (ACC =  $0Y3I_8$ )                     SRY

          IOP $_{10}$  = OR instruction to OSR

          IOP $_{20}$  = (I) to LAR, etc. Wait 5 ms. for relay to set.  
              Then clear OSR.

          IOP $_{1i}$  = Skip if operation  $3_8$  is complete.

OPCODE  $4_8$ :     CLEAR REGISTERS                     (ACC =  $0040_8$ )                     CLR

          IOP $_{10}$  = OR instruction to OSR

          IOP $_{20}$  = Clear OSR, Interrupt flag, Relay disconnect.

PMX-1 COMMAND LIST

OPCODE 5<sub>8</sub>: CHECK RELAY (I) (ACC = 005I) CKR

IOP<sub>10</sub> = OR instruction to OSR

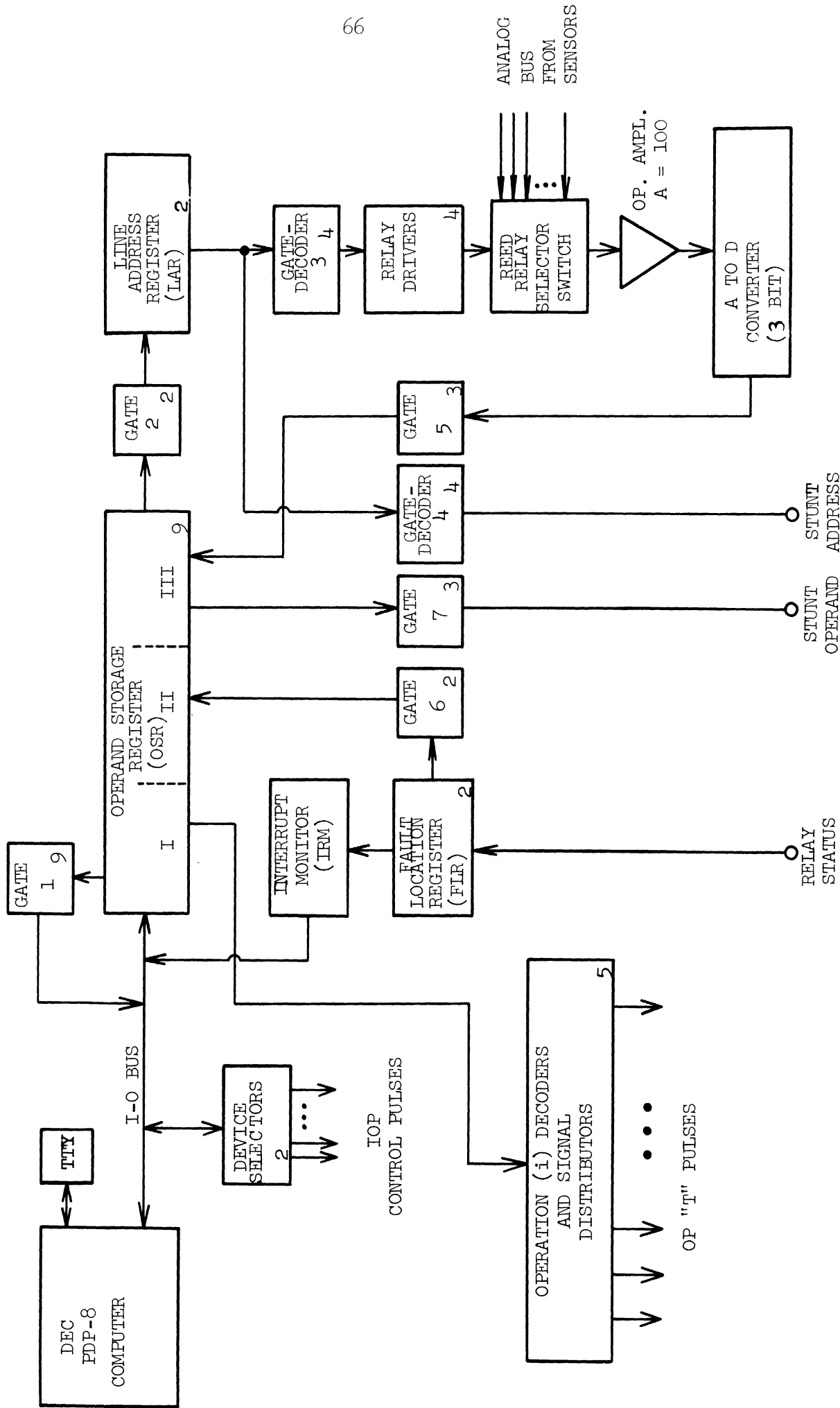
IOP<sub>20</sub> = Execute relay disconnect

IOP<sub>40</sub> = Clear OSR and continue disconnect until cleared



PMX-1 Organization

Figure A 1.2

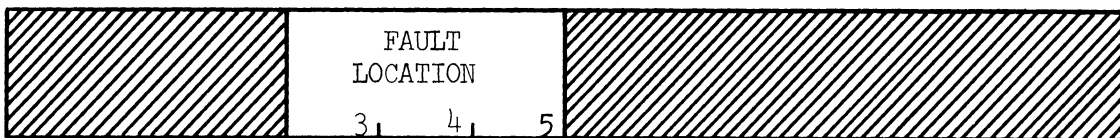


PMX-1 IOT Formats

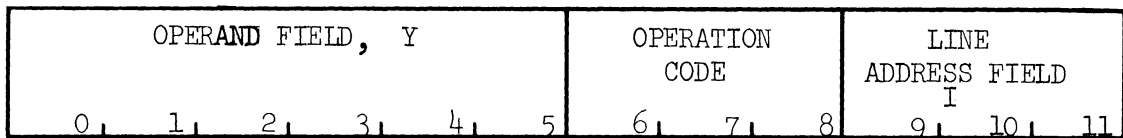
Figure A 1.3



I. LINE DATA FORMAT ( $b_0 - b_5$  not used)



II. FAULT LOCATION FORMAT ( $b_0 - b_2$ ;  $b_6 - b_{11}$  not used)



III. INSTRUCTION FORMAT

0 <sub>8</sub>	No Operation	(NOP,,)
1 <sub>8</sub>	Sequential Conversion	(SCV,,)
2 <sub>8</sub>	Set Relay (I) to Y	(SRY, I, Y)
3 <sub>8</sub>	Fault Location Examine	(FLE,,)
4 <sub>8</sub>	Clear Interrupt Flag, OSR, Disconnect Flag, LAR	(CLR,,)
5 <sub>8</sub>	Disconnect Relay (I)	(DIS, I,)

## POSITION

	1	2	3	4	5	6	7	8	9	10	
	R111	R202	R201 OSR	R201 OSR	R201 OSR	R201 OSR	R201 OSR	R201 OSR	R201 OSR	R201 OSR	ROW 1
	ROO1	R111 GATE 1	R107	R111 GATE 1	R202 FLR	R111 GATE 1	R201 LAR	R201 LAR	R107	R111	ROW 2
	R141 IRM	R111 IRM	R202 IRM	R602 IRM	ROO1	R111	R111	R111	R111	ROO1	ROW 3
	R201 OSR	R602	R107	R202	R111	R111	R111	R111	R202		ROW 4
	R111	R602	R302	R202	ROO2	R111	R111	ROO1	R302		ROW 5
	ROO1	R141								R602	ROW 6

PMX-1 Component Layout

Figure A 1.5

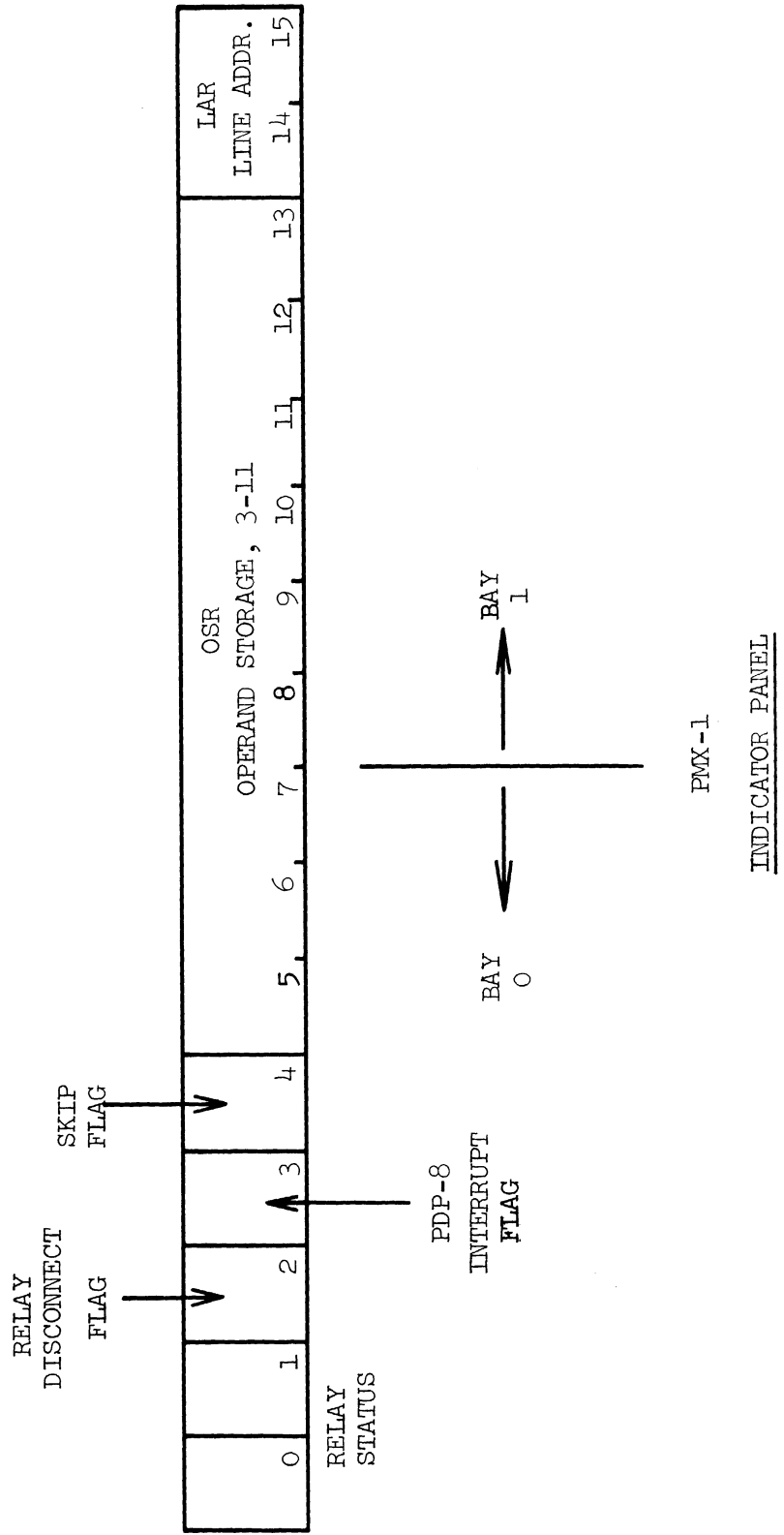


Figure A 1.6

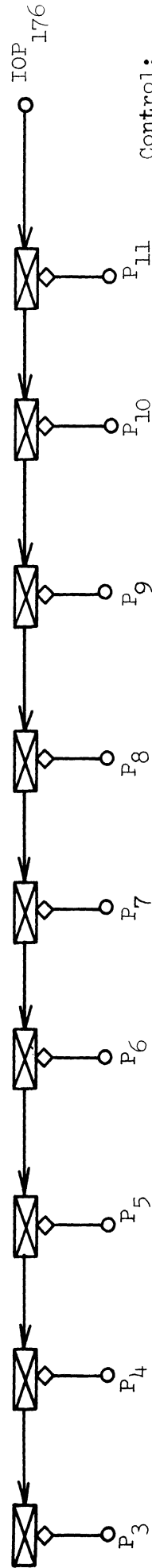
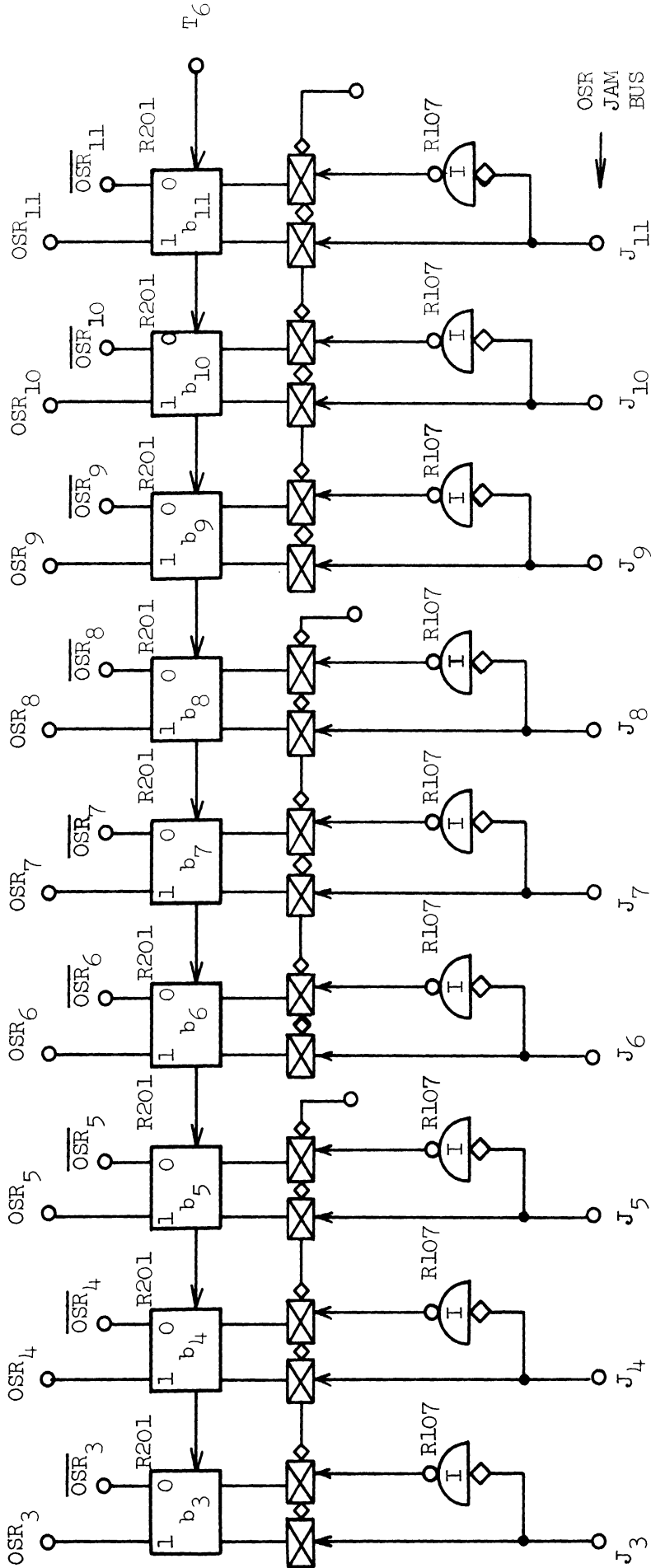
Referring to Figure 7, since only nine OSR bit positions are needed, bits 0-2 are deleted, effecting a further savings in hardware. The R-S flip-flop register has jam-transfer facilities for the various fields, while instructions from the PDP-8 are "ORED" into the cleared OSR through the lower set of DCD gates ( $P_3 - P_{11}$ ). Signals  $T_3$ ,  $T_2$ , and  $T_5$  enable jam-transfers into the FLR, reactive power, and real power fields, respectively. These T-signals are controlled by field select logic associated with each operation package. Gate 1 (Figure 8) gates the OSR contents into the PDP-8 accumulator when  $T_7$  is present, thus effecting signal transfers out of the multiplex r.

The FLR and IRM circuits are shown in Figure 9. The relay status bus is connected so that any relay operation will set the appropriate bit of the FLR to one.  $T_{14}$  enables transfer of the contents of the FLR to the OSR via Gate 6. The two pulse amplifiers in the IRM cause a one to be set in IFF if any change occurs in the FLR. Whenever the multiplexer finishes its present cycle, as indicated by  $OP_1$ ,  $OP_2$ , and  $OP_3$  all being zero, the interrupt request bus can then be grounded if IFF is set to one. Thus any change in the FLR causes an interrupt at the proper time.  $T_{39}$  clears the interrupt flag to zero when the PDP-8 acknowledges presence of an interrupt request.

The LAR circuitry is shown in Figure 10. The contents of the address field of OSR may be loaded into the LAR whenever  $T_9$ , occurs, via Gate 2. The LAR may be incremented by  $T_{50}$ , and cleared to zero by  $T_{16}$ . Gate 3 enables the relay driver whenever  $T_{10}$  occurs, and Gate 4 allows relays to be set by gating the address field specified by the LAR onto the set-relay bus.

Consistent with original design philosophy, the PDP-8 furnishes timing signals to the multiplexer. The IOP's (Input-Output Pulses) are used for timing, consisting of three 400 nanosecond pulses spaced approximately one microsecond apart, appearing during IOT (Input-Output Transfer) operations. Two sets of these pulses are used: one set to time inputs to the multiplexer ( $IOP_{176}$ ,  $IOP_{276}$ ,  $IOP_{476}$

Operand Storage Register OSR



Control:

- T<sub>2</sub> - Field I
- T<sub>3</sub> - Field II
- T<sub>5</sub> - Field III
- T<sub>6</sub> - CLR OSR
- IOP<sub>176</sub> - Load OSR

TO PDP-8  
OUTPUT  
BUS  
(P<sub>3</sub>-P<sub>11</sub>)

Figure A 1.7

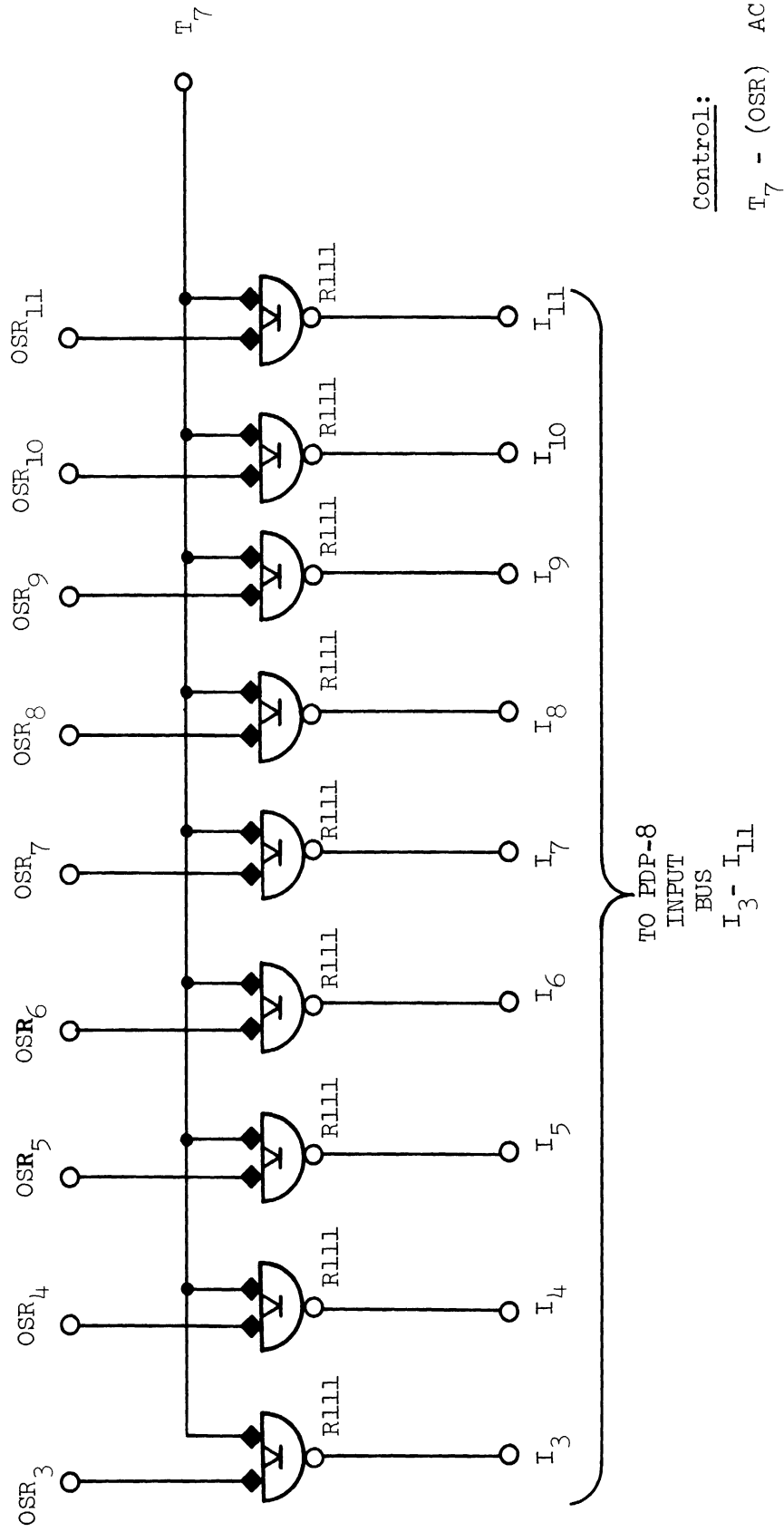
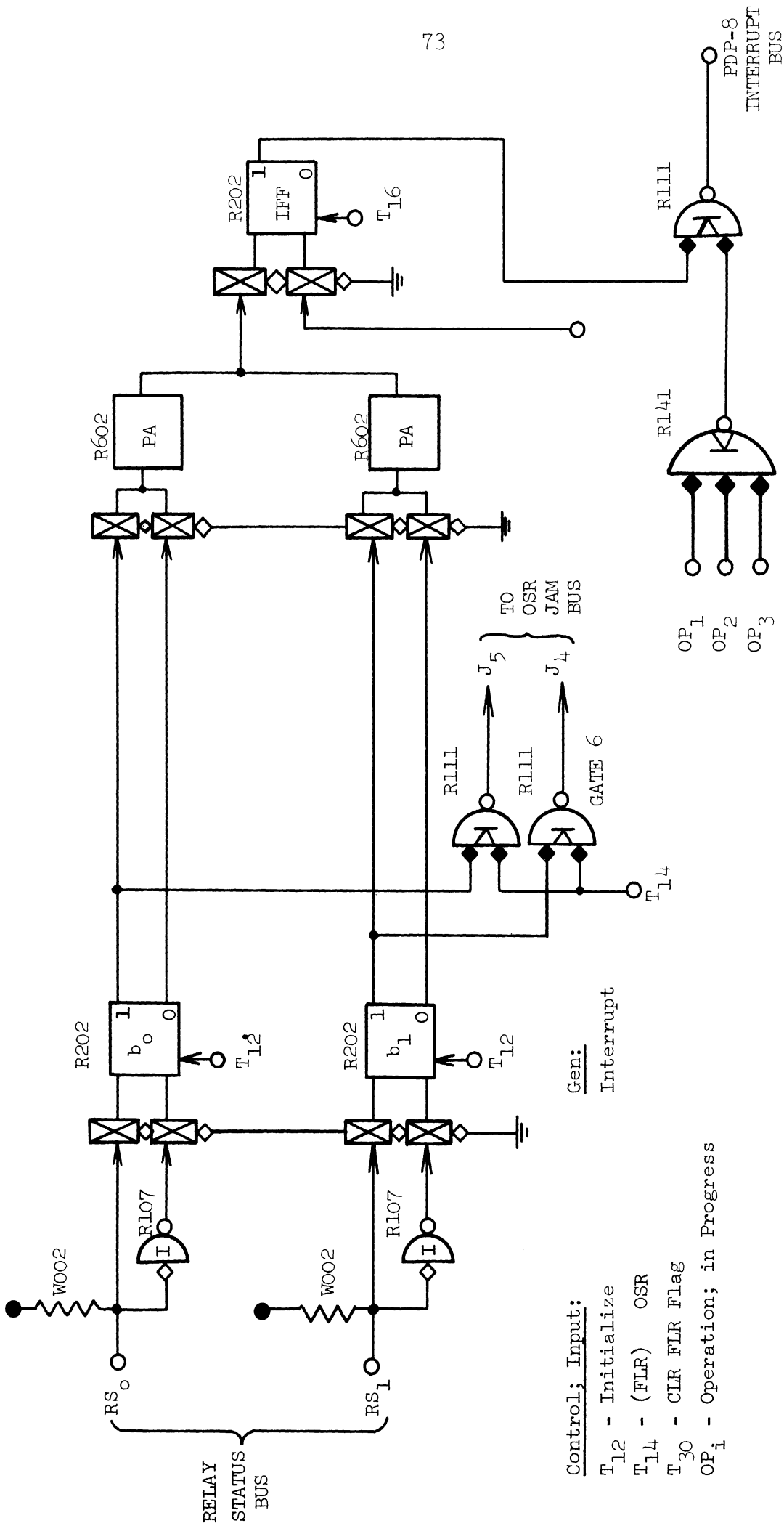


Figure A 1.8



Control; Input:  
 $T_{12}$  - Initialize  
 $T_{14}$  - (FLR) OSR  
 $T_{30}$  - CLR FLR Flag  
 $OP_i$  - Operation; in Progress

Fault Location Register and Interrupt Monitor

Figure A 1.9



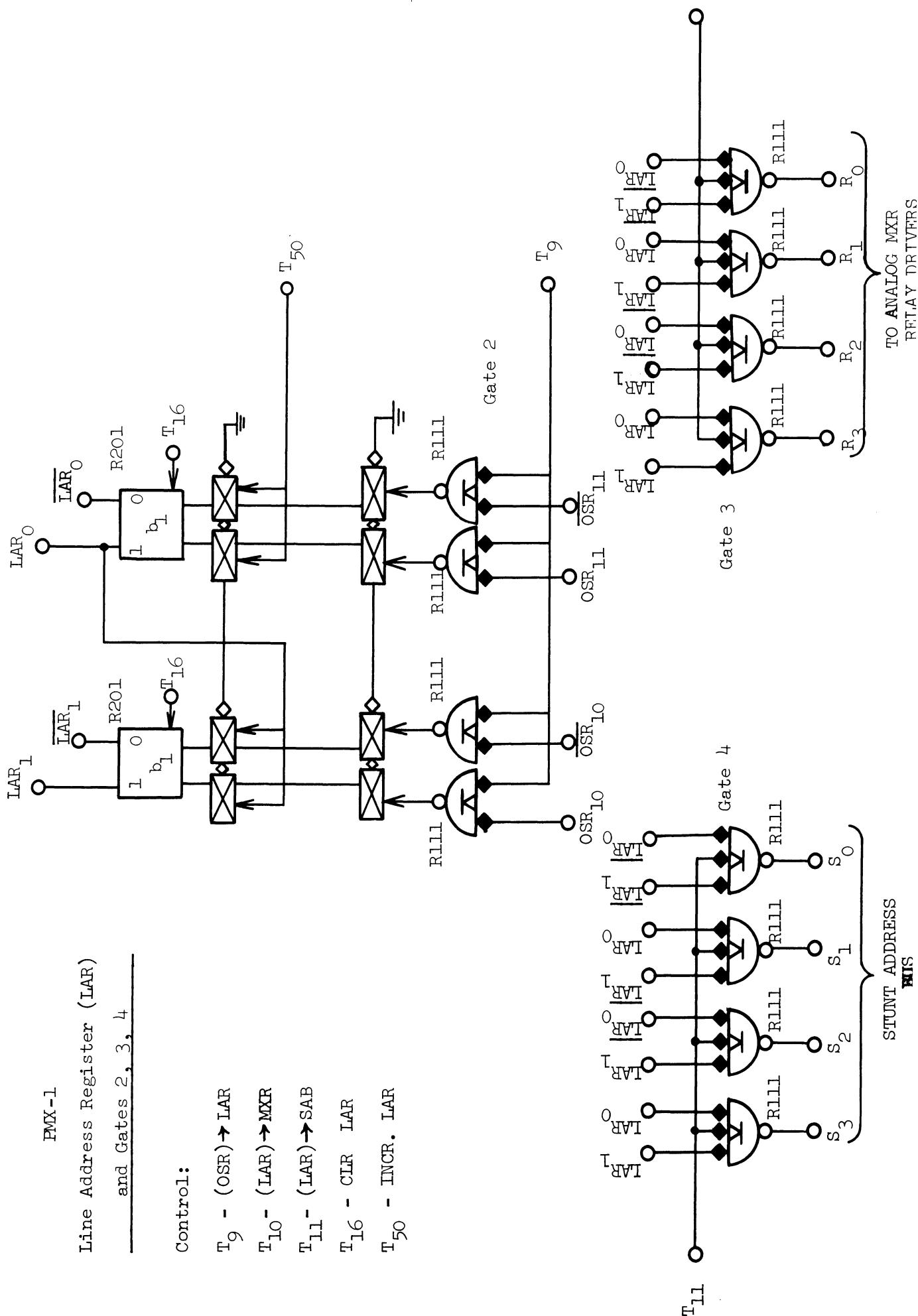
Figure A 1.10

FMX-1

Line Address Register (LAR)  
and Gates 2, 3, 4

Control:

- $T_9$  - (OSR)  $\rightarrow$  LAR
- $T_{10}$  - (LAR)  $\rightarrow$  MXR
- $T_{11}$  - (LAR)  $\rightarrow$  SAB
- $T_{16}$  - CLR LAR
- $T_{50}$  - INCR. LAR



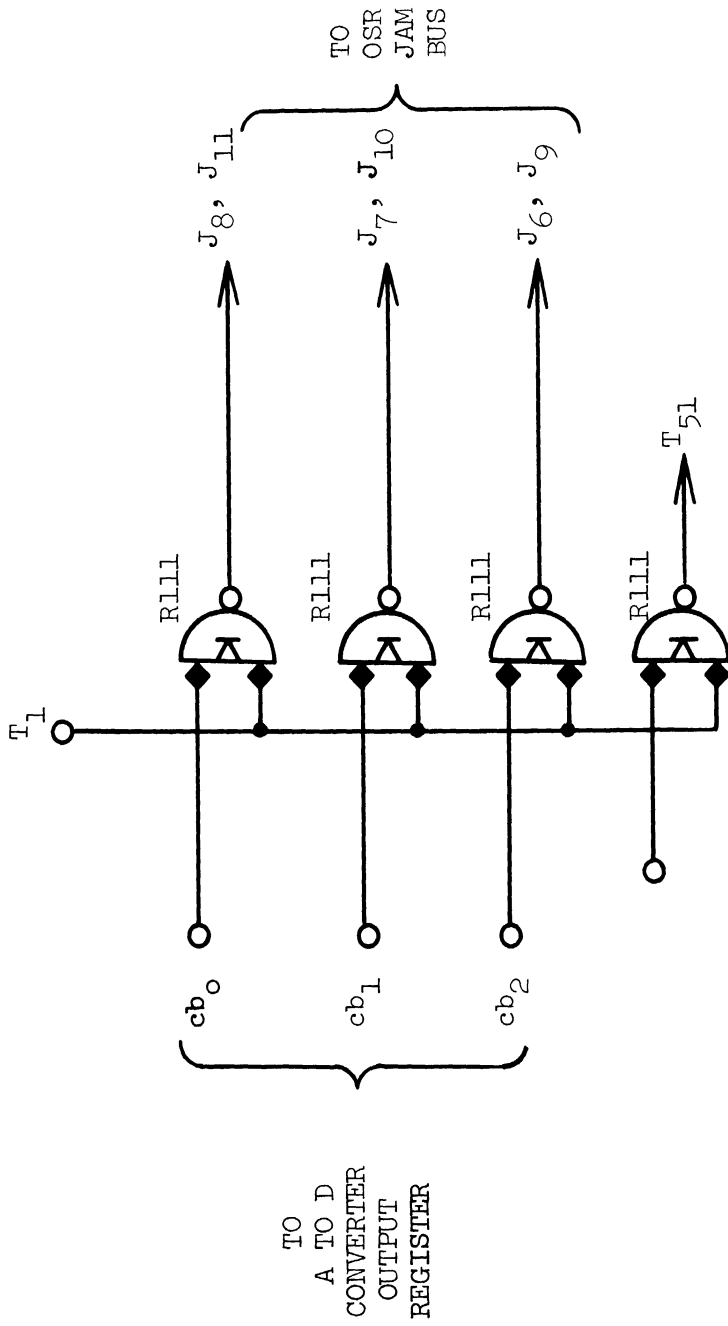
STUNT ADDRESS  
RIS

TO ANALOG MXR  
RELAY DRIVERS

and another set to time outputs from the multiplexer ( $IOP_{177}$ ,  $IOP_{277}$ , and  $IOP_{477}$ ). These pulses are derived by gating the PDP-8's IOP pulses through device selectors ( $76_8$  and  $77_8$ ) connected to the PDP-8/ I/O bus. In addition to timing input-output transfers, these pulses are used to time the operation packages of the PMX-1.

Now let us consider the operations packages of the PMX-1. The NOP instruction, corresponding to octal zero in bits 6, 7, and 8 of the OSR, does nothing, but places the multiplexer in standby mode. The SCV instruction (Figure 12) effects the power data transfer to the PDP-8.  $IOP_{176}$  loads the instruction into the OSR from the PDP-8 accumulator. When bits 6, 7, and 8 of the OSR are octal one coincident with  $IOP_{276}$ , the operation begins. FFA is set to one which enables the relay drivers through Gate 3 and  $T_{10}$ . The analog switch is now selecting line zero. At the end of a 3.5 millisecond delay through OS, which allows the relay contacts to settle,  $T_8$  occurs which begins the A-to-D conversion process on the line presently selected by the analog switch. When conversion is completed,  $T_{18}$  is generated by the converter, which increments the LAR (to line one), and the delay process is re-started through the lower DCD gate on  $PA_1$ . When the LAR has been incremented to line 3 and the converter finish pulse ( $T_{18}$ ) occurs,  $T_8$  is inhibited and FFA and FFB terminate the operation. At the end of assembly of each complete word, the DR flag (data ready) is set to one and the PDP-8 is notified of the ready condition via its skip bus. The OSR and the DR flag are cleared after a data transfer from the OSR to the PDP-8 accumulator by  $T_6$ . Gate 5 (Figure 11) transfers the A-to-D output register contents to the appropriate field of the OSR at the occurrence of  $T_1$ . TCFE determines the proper field by counting finish pulses,  $T_{18}$ . Odd pulses specify real power, while even pulses specify transfer to the reactive power field of OSR.

Operation FLE (Figure 13) inputs the FLR to the OSR for examination by the PDP-8. Whenever bits 6, 7, and 8 of the OSR are octal two during  $IOP_{276}$ , RFFF



PMX-1

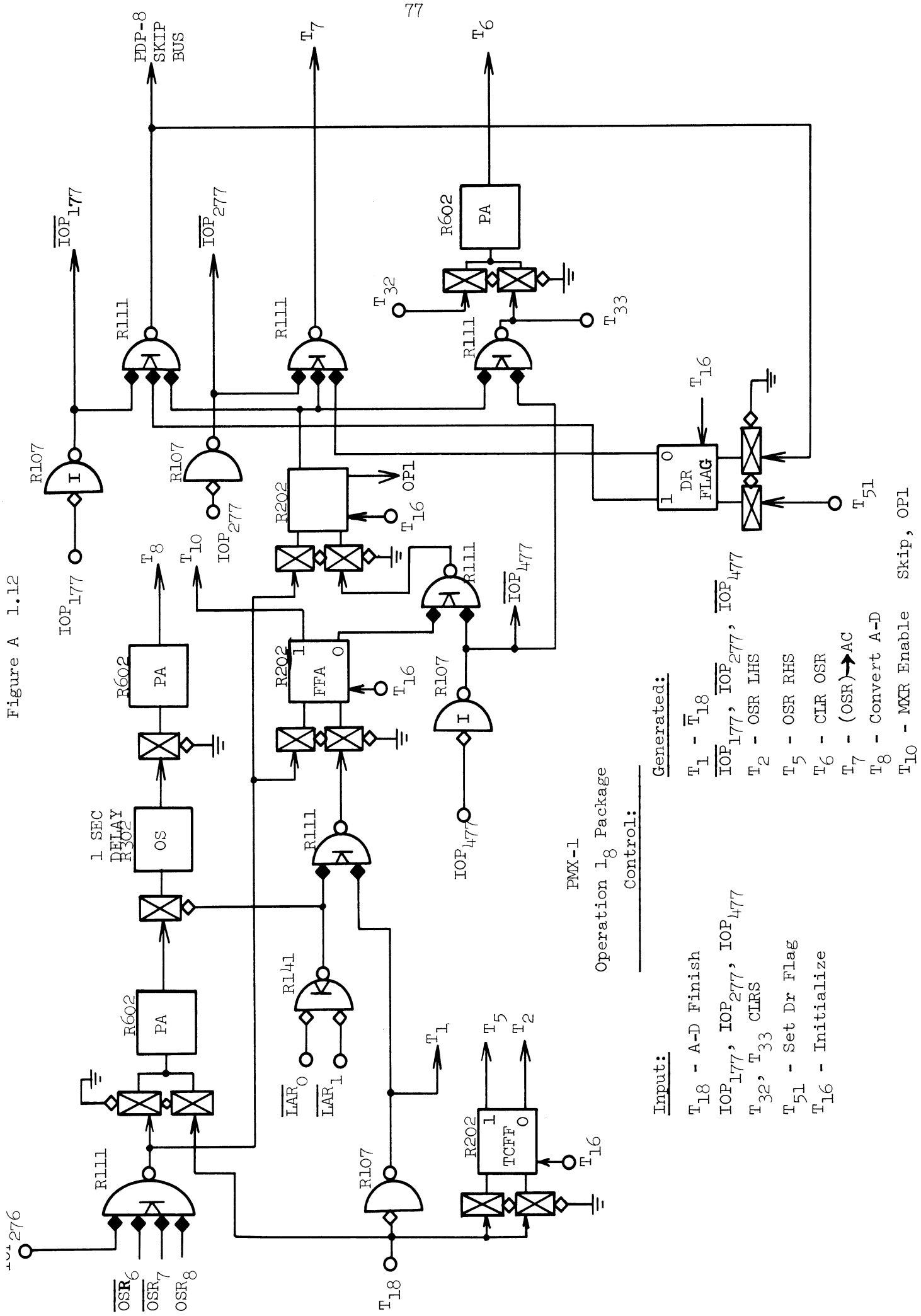
Gate 5

Control:  $T_5, T_1, T_{51}$

---

Figure A 1.11

Figure A 1.12

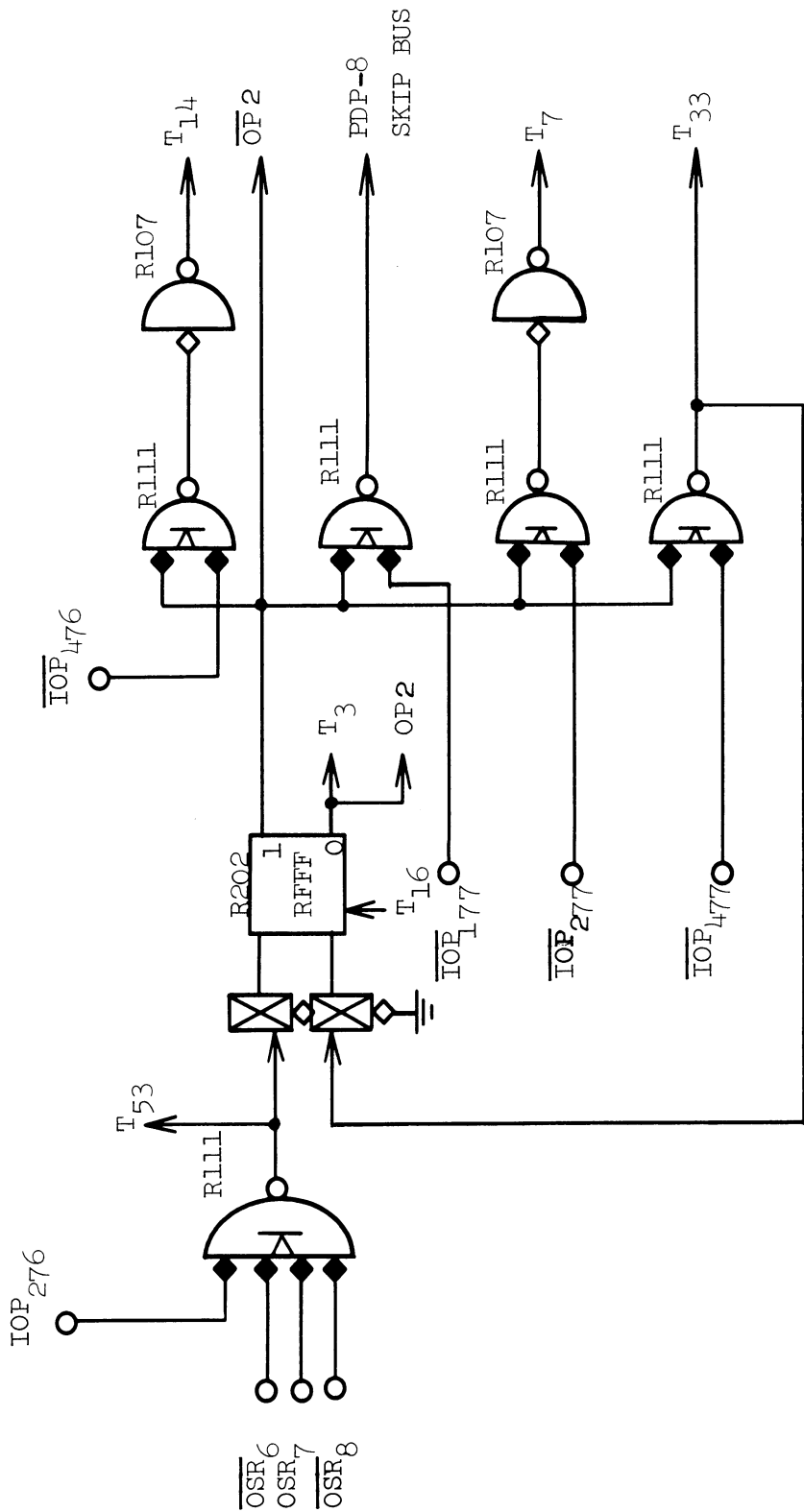


**Control:**  
 Operation 18 Package  
 PMX-1

**Input:**  
 T18 - A-D Finish  
 IOP177, IOP277, IOP477  
 T32, T33 CLR S  
 T51 - Set Dr Flag  
 T16 - Initialize

**Generated:**  
 T1 - T18  
 IOP177, IOP277, IOP477  
 T2 - OSR LHS  
 T5 - OSR RHS  
 T6 - CLR OSR  
 T7 - (OSR) → AC  
 T8 - Convert A-D  
 T10 - MXR Enable Skip, OP1

Figure A 1.13



PMX-1

Operation 28 Package

Control:

Input:

- IOP<sub>276</sub>, IOP<sub>476</sub>
- IOP<sub>177</sub>, IOP<sub>277</sub>, IOP<sub>477</sub>
- T<sub>16</sub>

Gen:

- T<sub>3</sub> - Init. Trans.
- T<sub>7</sub> - (OSR) AC
- T<sub>14</sub> - (FLR) OSR
- T<sub>33</sub> - CLR<sub>2</sub> OSR
- SKIP
- OP<sub>2</sub>

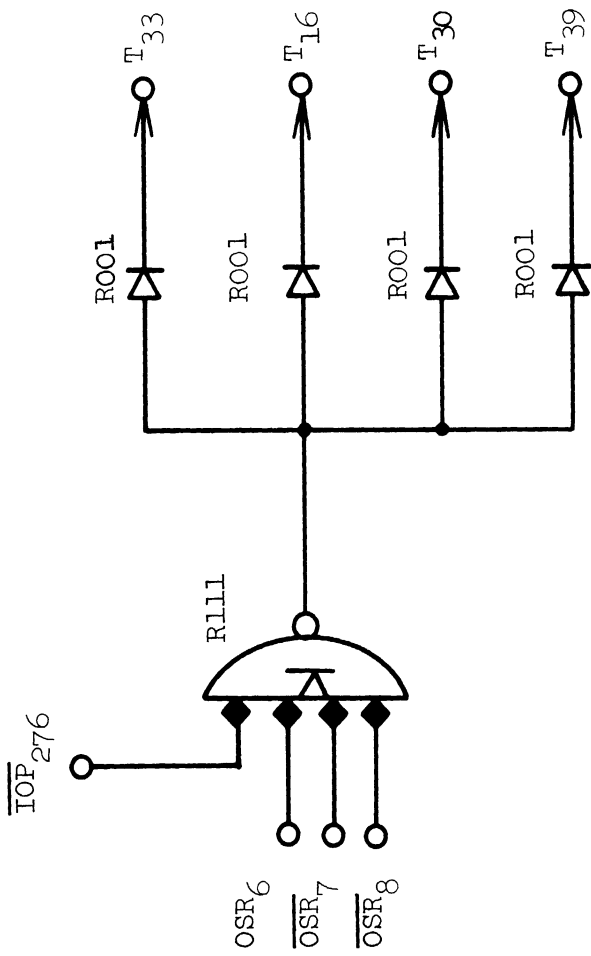
is set to one, and the FLR contents are gated via Gate 6 to the OSR. The PDP-8 is notified of the completion of the transfer via its skip bus.  $T_7$  gates the OSR contents to the PDP-8 accumulator at the proper time, and  $T_{33}$  clears the OSR after the PDP-8 finishes the examination.

Operation SRY, I, Y (Figure 14) sets the relay corresponding to the address field of the OSR to the contents of the Y field of the OSR. The operand (Y) field is gated to the set relay bus via Gate 6, and the address field via Gate 4. OS simulates the relay setting time, and the PDP-8 is notified of the completion of this operation via its skip bus.

Operation CLR (Figure 15) initializes the PMX-1 for operation and clears all registers and ready flags to zero. Operation CKR, I, (Figure 16) is used to check relays online.  $T_{55}$  sets the disconnect flag to one and thus disables the trip coil circuitry of the relay specified by the address field of the OSR. The disconnect is cleared by the CLR instruction through  $T_{39}$ .

Notice that all of the operation packages are modular, so that any may be deleted at will by interconnecting the appropriate T-signals. For example, suppose it were desirable to delete the FLR instruction from the PMX-1. In this case, the hardware for operation FLE (Figure 13) would be deleted in its entirety. In addition, the three inverters associated with  $T_3$  of OSR (Figure 7), the left-most three gates of Gate 1, and Gate 6 would be deleted.  $OP_2$  would be connected to -3 volts. Thus the unit is designed for plug-in modifications, which is one of the most important requirements for the multiplexer system.





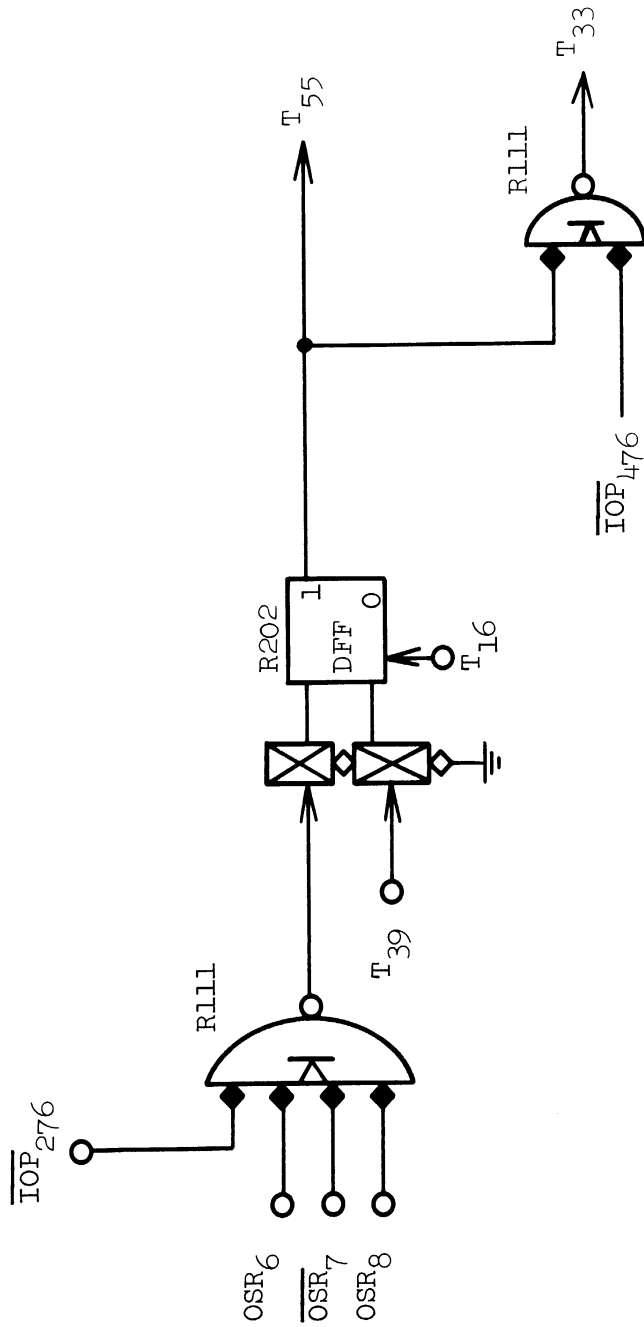
PMX-1

Operation <sub>48</sub> Package  
Control

Input:	$\overline{IOP}_{276}$	Gen:	T <sub>16</sub> - CLR LAR
			T <sub>32</sub> - CLR <sub>1</sub> OSR
			T <sub>33</sub> - CLR <sub>2</sub> OSR
			T <sub>39</sub> - CLR Disconnect

Figure A 1.15





PMX-1  
 Operation 58 Package  
 Control:

Input:	Gen:
$\overline{IOP}_{276}$	T <sub>55</sub> - Disconnect Relay
T <sub>16</sub> - CLR	T <sub>33</sub> - CLR, OSR
$\overline{IOP}_{476}$	

Figure A 1.16

PMX-1 COMPONENT COUNT AND COST\*

<u>D.E.C. PACKAGE:</u>	<u>QUANTITY:</u>	<u>TOTAL COST:</u>
R001	4	\$ 19.00
R002	1	5.70
R107	3	81.60
R111	17	238.00
R141	2	29.20
R201	11	242.00
R202	6	157.20
R302	1	47.20
R602	4	100.00
	<hr/>	<hr/>
	49	\$919.90

\*Total cost of logic modules only indicated. Add in cost of A-to-D converter, analog switches and relay drives, indicators and drivers, mounting hardware and power supply.

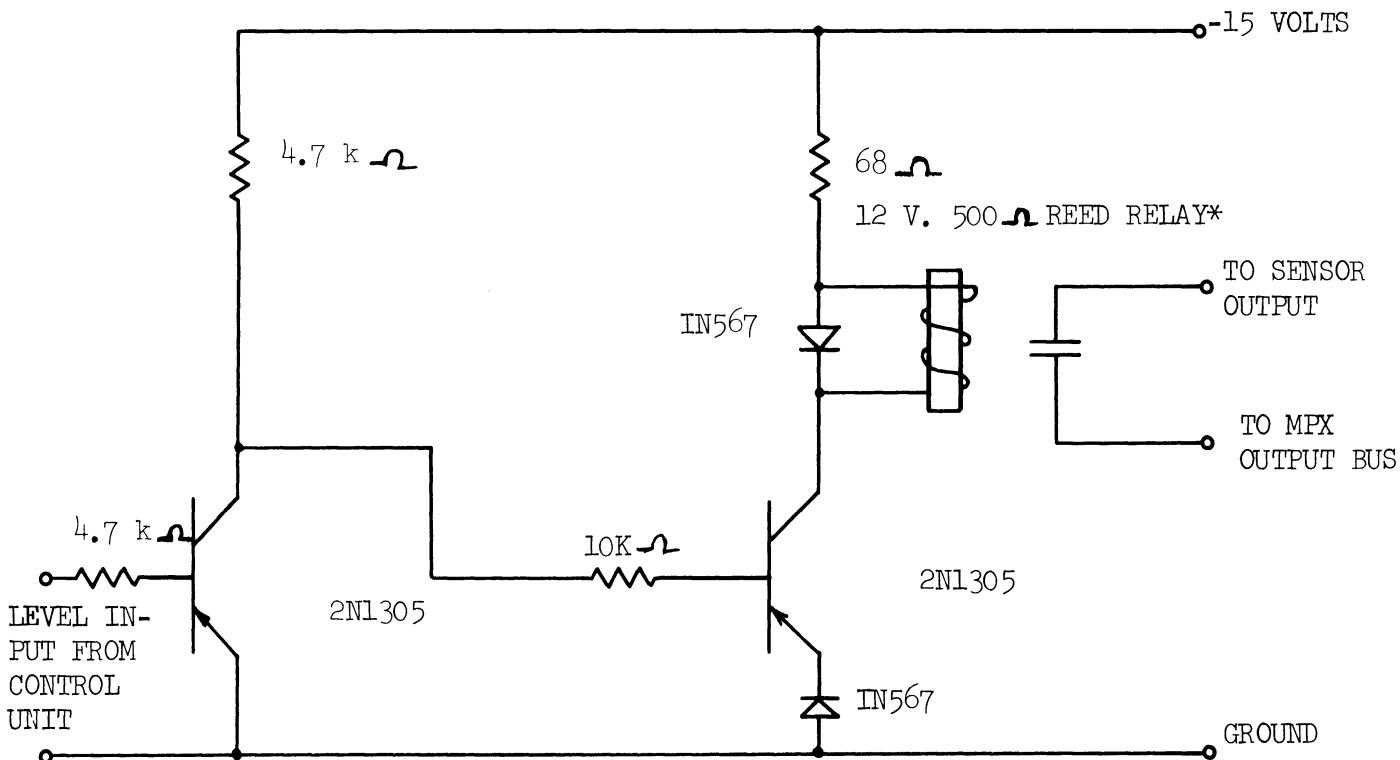
## APPENDIX II

DATA MULTIPLEXER

The reed relay data multiplexer was constructed as shown by the circuit and the following results were obtained. For an 8 millisecond square wave input, the reed relay required 1.8 milliseconds for closing and the settling of the contacts and .8 milliseconds to open. At 3 milliseconds total activation time, 1.0 millisecond was required for contact sealing time and .8 milliseconds open time. This reduction of close time is due to the reed relay not hitting higher resonant frequencies at the shorter time interval due to the periodic excitation. For the tested relay, a repetitive 2.4 millisecond activation time produced no noticeable contact bounce. At all time periods within the range of operation the contact bounce terminated before the required 2.0 milliseconds.

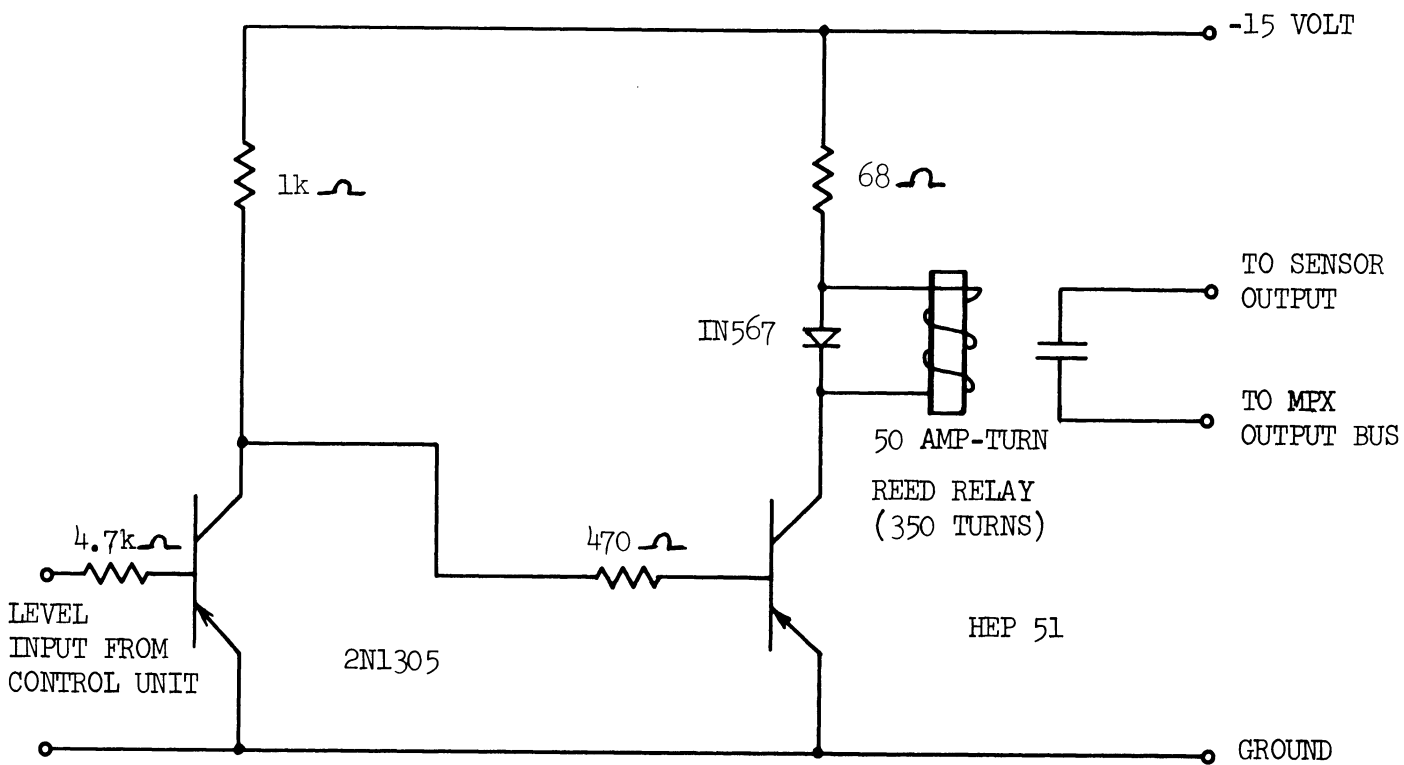
Analog Multiplexer

(Relay Driver)

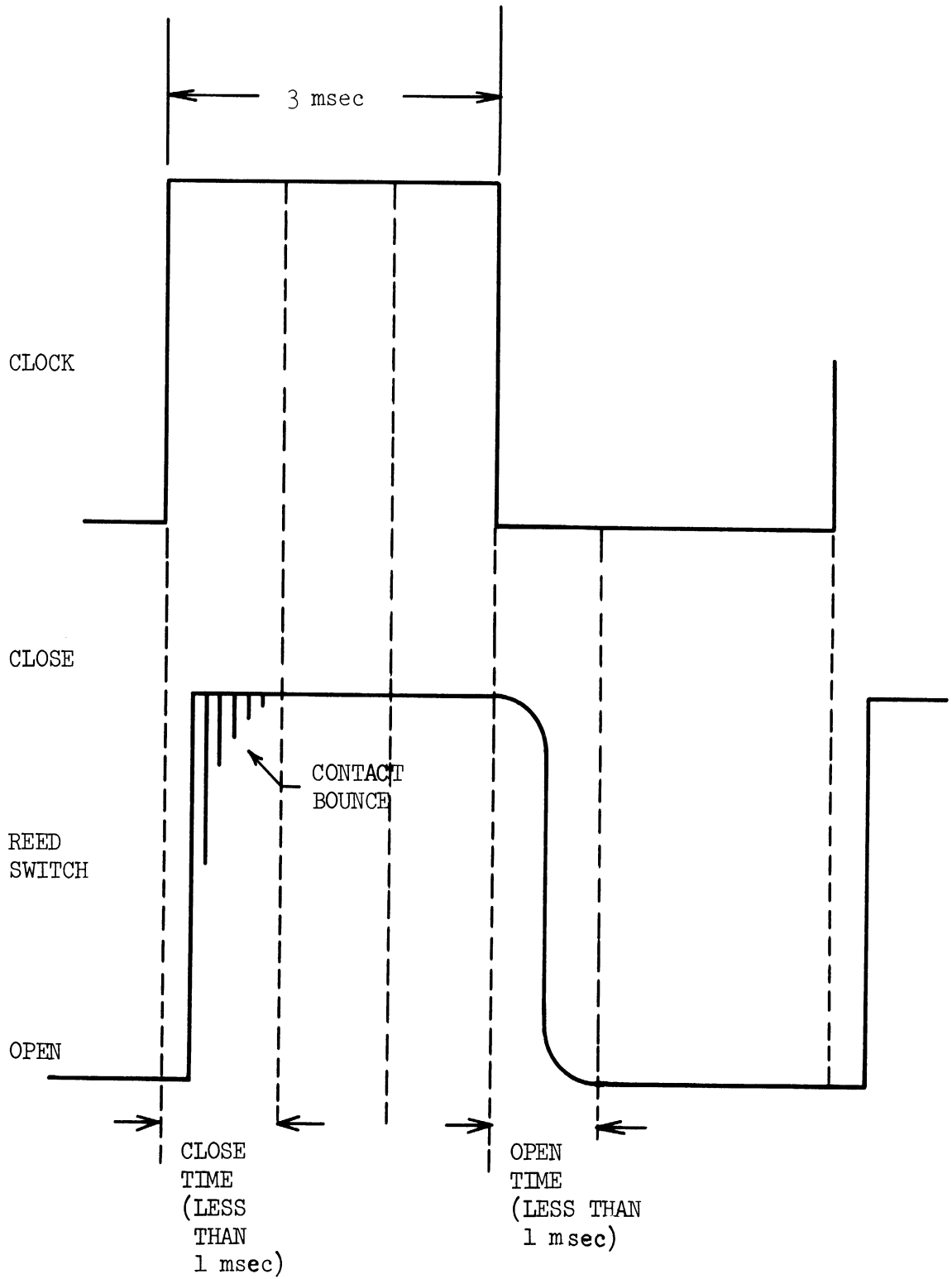


Designed Circuit

\*MAGNECRAFT W102 PCX-2



Tested Circuit



Reed Switch Contact Wave Form Under  
Experimental Conditions

Figure A 2.2

## Appendix III

DISCRETE RELAY SWITCHING

A feasible scheme of tap changing would use discrete relays to do the necessary switching (see Figure A 3.1). Suppose relay RK3 is actuated but it is now more desirable to have RK2 connected. The computer would send a four bit word to the logic which would decode it and then activate RK2. Once RK2 was activated the logic would then deactivate RK3. The necessity of holding RK3 until RK2 is activated is so that the secondary of the current transformer is never open circuited.

To avoid having current continuously applied to the relay which is presently **actuated**, a ratchet or latching relay should be used (e.g., Guardian Relay type 670C115A).

The cost and size requirements of this system prove undesirable. Nineteen relays at \$4.55 a relay cost \$86.45 for a unit. The approximate size of such a unit would be at least 190 cu. in., much larger than two servo units.

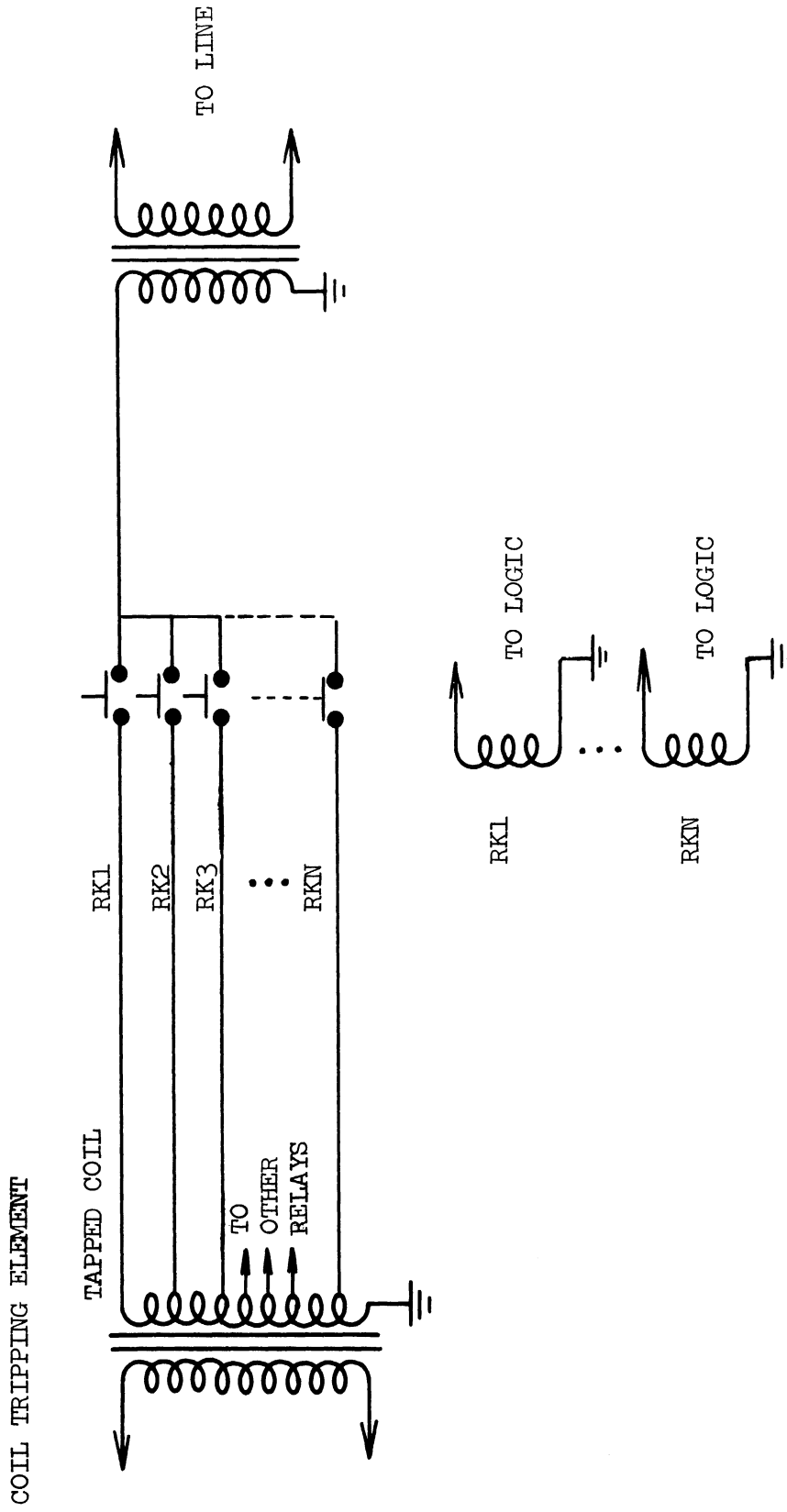


Figure A 3.1

## Appendix IV

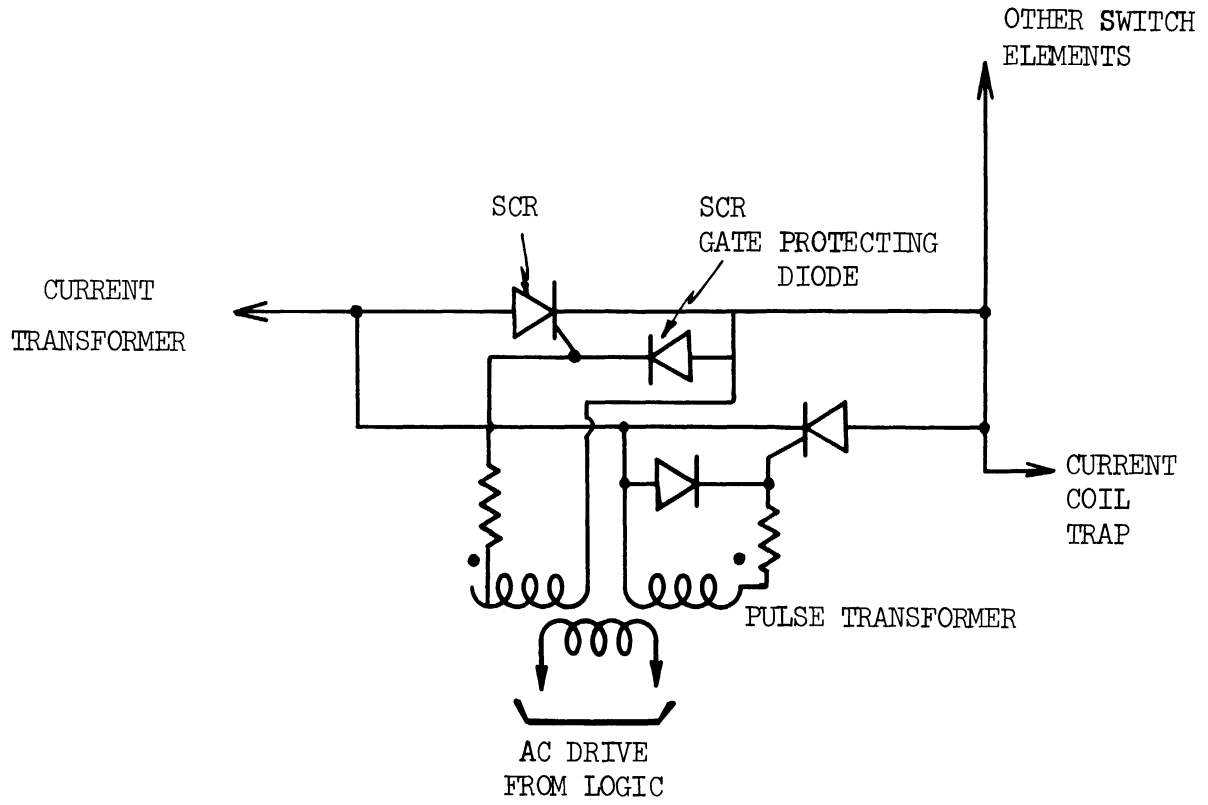
SOLID STATE TAP SWITCHING

A thorough investigation of a solid state means of performing the tap switching on the relay elements was conducted. The reason the research was performed is because of the reliability and maintenance-free operation of solid state circuits. If a reliable switching arrangement could be found, it would be more desirable than a mechanical device, even though perhaps more expensive, for these reasons.

The only solid state device able to perform the heavy current switching operations is a Silicon Controlled Rectifier (SCR). When a fault occurs on the power line the current can easily rise by a factor of twenty or more and no other device can tolerate this type of overload. The SCR is capable of very large short-time surge currents and yet can be regulated like a switch with low level signals obtainable from normal logic levels. Since the SCR is essentially a gated diode, two SCR's are needed in parallel facing in opposite directions to provide A.C. conduction. To gate the nine "ten's" scale and the ten "unit's" scale taps on the relay current coil, a total of thirty eight SCR's are required. Figure A 4.1 shows a representative current coil tap using this SCR switching method. To gate the SCR's a high frequency A.C. pulse is used since it is easier to switch an A.C. gating signal to the proper tap than a D.C. signal.

By using SCR's a problem develops concerning the first design criterion of never allowing an open circuit to appear on the current transformer secondary. The impedance vs. current characteristic is shown in Figure A 4.2 for a typical high current SCR. For alternating currents passing through

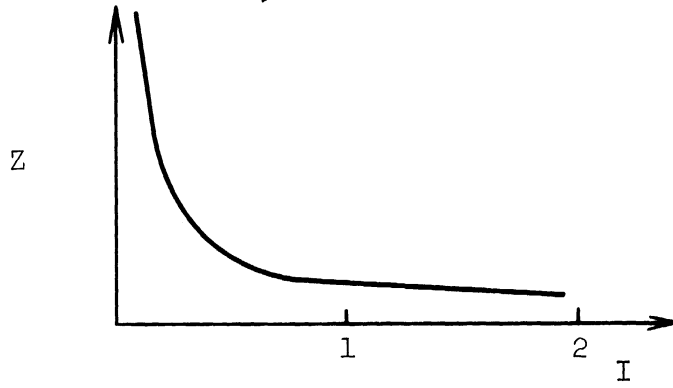




One of these is required for each individual tap to be switched.

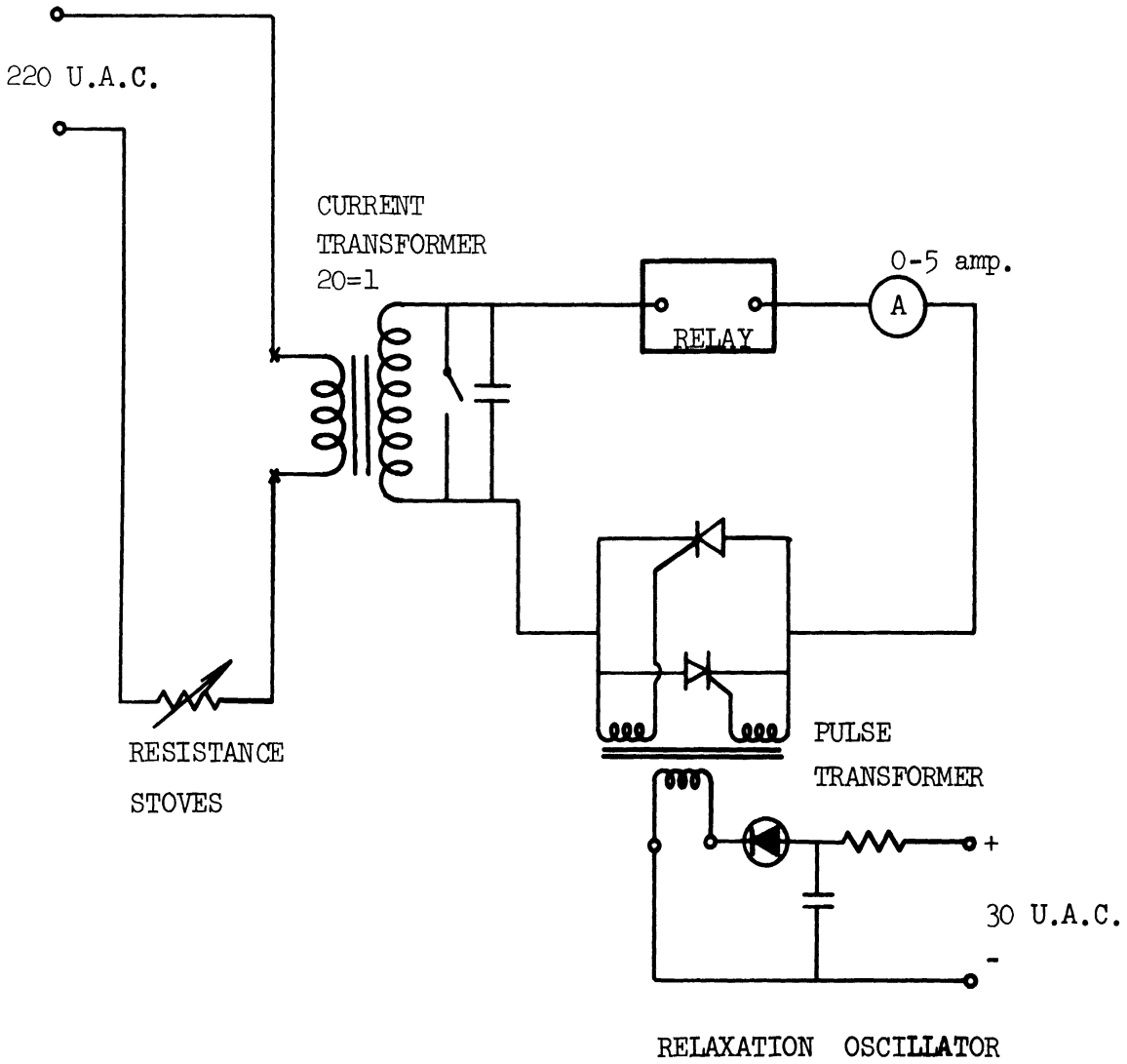
Tap Switching Element S.C.R.

Figure A 4.1



Impedance Vs. Current Characteristic

Figure A. 4.2



SCR Experimental Test Set-Up

Figure A.4.3

zero, the SCR will present a high impedance to the secondary of the current transformer which approximates an open circuit and causes extreme  $dv/dt$ . This is an intolerable condition in any SCR circuit since SCR's will fire themselves if a high  $dv/dt$  appears across the device. Thus all current coil taps will fire, not just the tap for the required setting.

To further investigate the  $dv/dt$  problem in an SCR circuit, a prototype model of one current coil tap was built up (Figure A 4.3) and laboratory tested. The current waveform across the SCR's when no current transformer is used (1:1 ratio) is as shown in Figure A 4.4. Note that near zero, no current can flow and a dead zone (open circuit) is formed. When the current transformer was used as shown in Figure A 4.5, the  $dv/dt$  of 800,000 v./sec. was sufficient to turn on the SCR's without a gating pulse. The pulsing frequency was 2Khz and no significant improvement was observed by increasing the pulsing rate. To circumvent this problem a capacitor was placed across the secondary of the current transformer (see Figure A 4.3). This solution is practicable because of the low current at the time of high voltage spikes. The capacitor can well take out the severity of the spike but cannot eliminate it all together. The equation governing capacitor operation is:

$$i = c \, dv/dt$$

The spike begins to occur where the current drops below .1 ampere. Therefore a 100 uuf capacitor would limit the  $dv/dt$  to 100 v./sec., an acceptable value, while presenting a 265 ohm impedance to normal 60 cycle current. The normal voltage across the current transformer is about 4 volts which means a current of only 7.5 ma. peak. In the lab test, the 100 uuf capacitor was seen to limit the spikes to 3.5 v. maximum value and a  $dv/dt$  of 1140 v./sec. When the secondary current was 4.5 amps., the waveform across the relay cur-

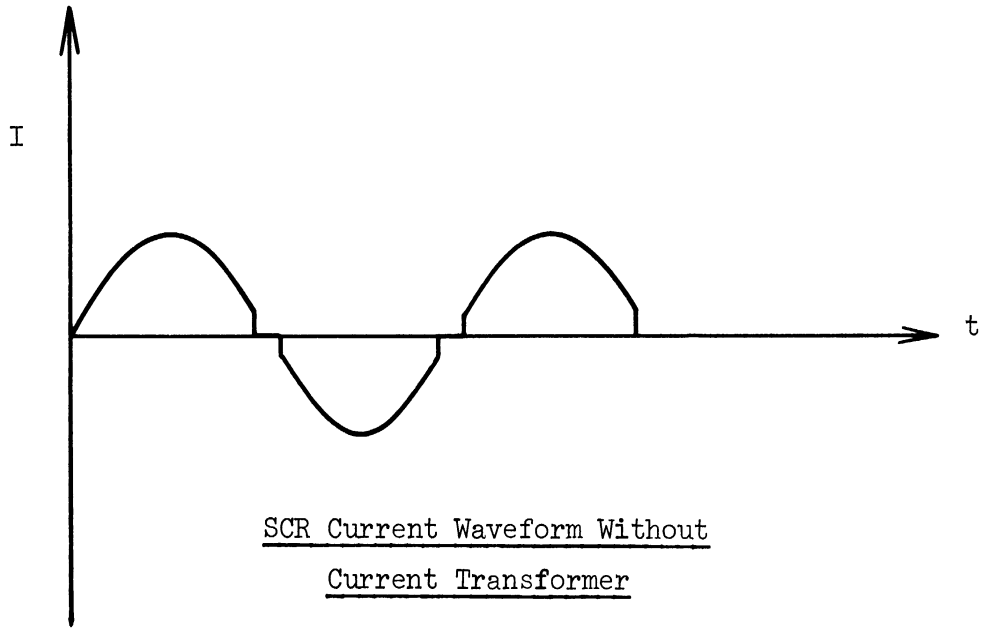
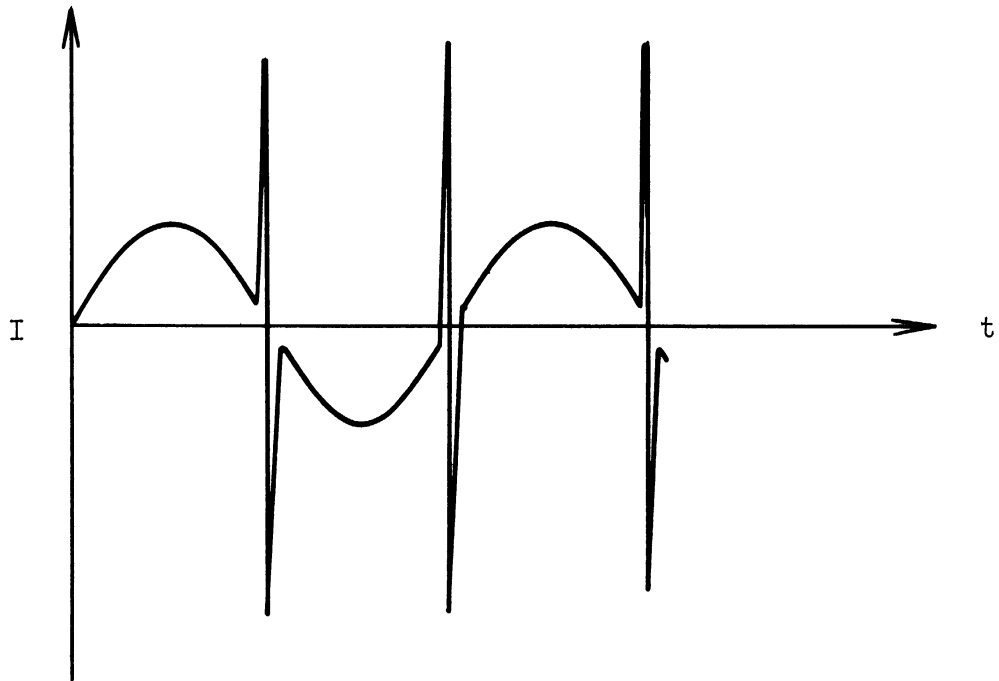


Figure A 4.4



SCR Current Waveform With Current Transformer

Figure A 4.5

rent coil was almost normal except for a 3.5 v. spike in the peak.

CONCLUSION:

The lab test showed that this is a feasible solution for low level operation. However, for current transformer of 1000:1 ratios, the spikes would be proportionally larger. Under line fault conditions, the case would again severely worsen because of the higher open circuit voltage. However, even if capacitors of the proper ratings could be found, reliability would still be lacking. A minor capacitor or SCR failure could cause the entire system to be damaged and could not continue to operate. The SCR is the least reliable of all solid state devices. To increase the reliability it would be necessary to place two additional SCR's at each ten's scale tap in parallel redundancy. Since the cost of the SCR's is near \$5.00 per unit, this would increase the already high price to a prohibitive amount. The cost for SCR's alone would be \$280.00. For these reasons, reliability and cost, solid state switching is considered not to be a feasible solution.

## Appendix V

EXAMPLES OF DDP-516 PROGRAMMING

The sequence to read in power flow data and store it in flow data table.

```

      SCV                BEGIN SEQUENTIAL CONVERSION
GET  SKS                '0005        IS DATA IN YET?
      JMP                *-1          NO, LOOP
      INA                '1005        GET DATA INTO REG. A
      LLS                1
      SPL                IS LAST-LINE FLAG SET?
      JMP                LAST         YES
      LRS                SHIFT BACK
      STA*               POINT        STORE INTO PROPER PLACE
                                      IN TABLE
      IRS                POINT        INCREMENT TO NEXT TABLE LOC.
      JMP                GET          GO TO GET NEXT INPUT
LAST LRS                .1
      STA*               POINT        STORE LAST DATA IN TABLE
      CRA
      ADD                POINTI       RE-INITIALIZE TO BEGINNING OF TABLE
      STA                POINT

```

The subroutine to calculate relay setting  
Given as parameters:

I - the relay number  
D - shortest distance to connecting relay  
PRCNT - Zone percentage  
ZU - impedance per unit length

```

CRA
ADD = '156/110 DECIMAL
IAB
DVI D

```

IAB  
CRA  
DVI PRCNT  
IAB  
CRA  
DVI U  
STA TEMP  
CRA  
ADD = '5  
MPY = '144/100 DECIMAL  
DVI TEMP  
STA Y  
CRA I  
ADD I  
ALS 9  
ADD Y  
IMA OP  
ANA = '160000/LEAVE OP CODE-OR IN RELAY INDEX AND SETTING  
ERA OP  
STA OP  
P SRY \*\* / SET RELAY I TO "Y"  
.  
.  
.

