THE UNIVERSITY OF MICHIGAN
COLLEGE OF ENGINEERING
Department of Electrical Engineering
Space Physics Research Laboratory

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DEVELOPMENT OF A DIGITIZED VOLTAGE GENERATOR FOR IONOSPHERIC PROBE MEASUREMENTS

Prepared on behalf of the project by:

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TABLE OF CONTENTS

ABSTRACT

The program of ionospheric research conducted by The University of Michigan's Department of Electrical Engineering makes extensive use of rocket-borne probes. Data are collected by means of an electrostatic sensor in the probe, and analyzed by means of a large, ground-based, general-purpose digital computer. To exploit the vast potential of the latter more fully, a development project was undertaken to modify, or redesign as necessary, present analog-type sensors. Means of generating an accurate series of discrete voltage levels, corresponding to a stairstep waveform, are investigated and an efficient method is described. The resulting compact, transistorized circuitry has been compensated for variations in supply voltages and ambient temperature to insure voltage level accuracies of better than 99% with less than 0.05% droop per step. In addition, means have been developed to provide two identical output waveforms with a high degree of electrical isolation.

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Concluded)

LIST OF FIGURES (Continued)

LIST OF SYMBOLS

a	amperes
C	capacitor
C_c, C_e	Q-Transporter stage collector and emitter capacitors, respectively
D	diode
E	supply voltage
$e_o(t)$	output voltage
e_n	Storage counter circuit output voltage
e_r	Storage counter feedback (error) voltage
f	frequency
h	transistor hybrid parameters; h_{fe}, h_{ob}, h_{ib}, h_{rb}
I,i	current
I_c, I_e	transistor collector and emitter currents, respectively
I_e, I_p	electron and positive ion probe currents, respectively
I_{CO}, I_{EO}	transistor leakage currents; collector to base and base to emitter, respectively
I_p	Unijunction transistor peak emitter current
I_T	total probe current
I_z	Zener diode reverse current
K	multiplier ($= 1 \times 10^3$)
K_o, K_1	fixed scale factors
k	Boltzmann's constant
M	multiplier ($= 1 \times 10^6$)
MV	multivibrator

m	multiplier (= 1 x 10^{-3})
N_p	positive ion density in the ionosphere
n	number of steps in stairstep voltage sweep
P_q, P_v	percentage change in charge and voltage, respectively
Q_n	Transistor no. n
Q, q	charge
q	unit of electric charge
q/k	unit electric charge/Boltzmann's constant = 1/11,600
R	resistor, resistance
R_{BB}	Unijunction Transistor Interbase resistance
R_{B_1}	Unijunction Transistor Base-One resistance
R_{B_2}	Unijunction Transistor Base-Two resistance
R_E	Emitter Follower Amplifier emitter resistor
R_g	effective series resistance of signal generator
R_i	input resistance
R_L	load resistance
R_{MV}	multivibrator high-level output resistance
R_o	output resistance
R_p	"plasma resistance"
R_{SAT}	transistor collector to emitter saturation resistance
r_b, r_c, r_e	transistor equivalent circuit resistances
S_n	switch no. n
s, sec.	seconds
T, t	time
T	temperature

T_e	electron temperature in the ionosphere
T_o	arbitrary reference time
$U(t)$	Unit Step Function
V,v	voltage, volts
V_{BB}	Unijunction Transistor Interbase voltage
V_{be}	transistor base-emitter voltage
V_c,V_e	transistor collector and emitter voltages, respectively
V_{CBO}	maximum rated transistor collector to base voltage
V_D	diode voltage
V_{in}	input voltage
V_n	negative supply voltage
V_o	output voltage
V_p	Unijunction Transistor peak emitter voltage
V_R	Zener diode reverse voltage
V_z	Zener diode reverse reference voltage
α	normal transistor current gain
$\bar{\alpha}$	current averaged transistor current gain
α_N	normal transistor current gain
α_I	inverted transistor current gain (collector and emitter terminals interchanged)
$\Delta V,\Delta q$	change in voltage and charge on output capacitor, C_c, resulting from single operation of Q-Transporter stage, respectively
δV	Probe electrode voltage
ϵ	small voltage change
η	Unijunction Transistor Intrinsic Standoff Ratio

μ	multiplier ($= 1 \times 10^{-6}$)
τ	RC or RL circuit time constant
ϕ_c, ϕ_e	Transistor collector and emitter junction voltages, respectively
Ω	ohms

I. INTRODUCTION

This report describes the development of a transistorized stepped voltage source to be used to implement electrostatic ionospheric probe experiments conducted by the Space Physics Research Laboratory of The University of Michigan, Department of Electrical Engineering.

A description of the experiment and the theoretical considerations pertaining thereto can be found in Scientific Report No. JS-1 of The University of Michigan's Office of Research Administration, dated August, 1961. Summarized briefly, the report describes how electron temperatures (T_e) and ion densities (N_p) in the ionosphere are deduced from measurements made by a rocket-launched instrumentation package, the sensor of which operates as a Langmuir probe. Part of the theoretical problem is establishing a region in which the electric fields are such that the desired quantities (N_p and T_e) can be most directly related to the voltage, $\delta V(t)$, applied across a set of electrodes and the resulting plasma current, $I(t)$. This includes the formidable problem of adequately describing the perturbation of the field due to the presence of the instrumentation hardware, and/or mitigating this effect by appropriate compensation techniques, often done with guard electrodes. When this is done, separate and synchronized voltage sources must be provided for the two electrode pairs. These sources must be isolated because circuitous current paths would otherwise result, since all external terminals of the probe are interconnected through the plasma. The arrangement of the electrodes and their voltage sources is shown in Fig. 1 for a "Dumbbell"-shaped probe. The current detector measures the current to the outer hemispherical collectors. Voltage

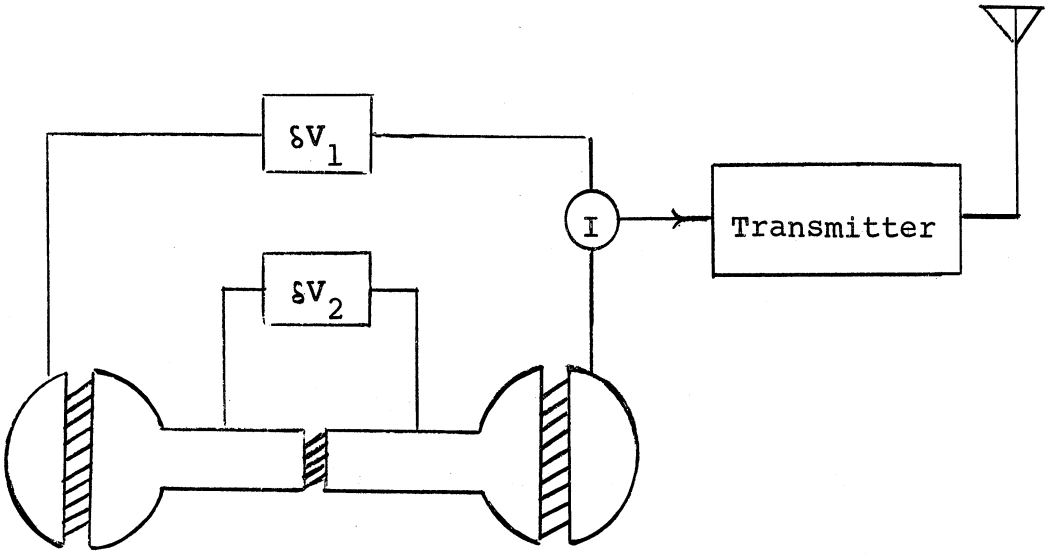


Fig. 1. Functional Block Diagram of "Dumbbell" Probe.

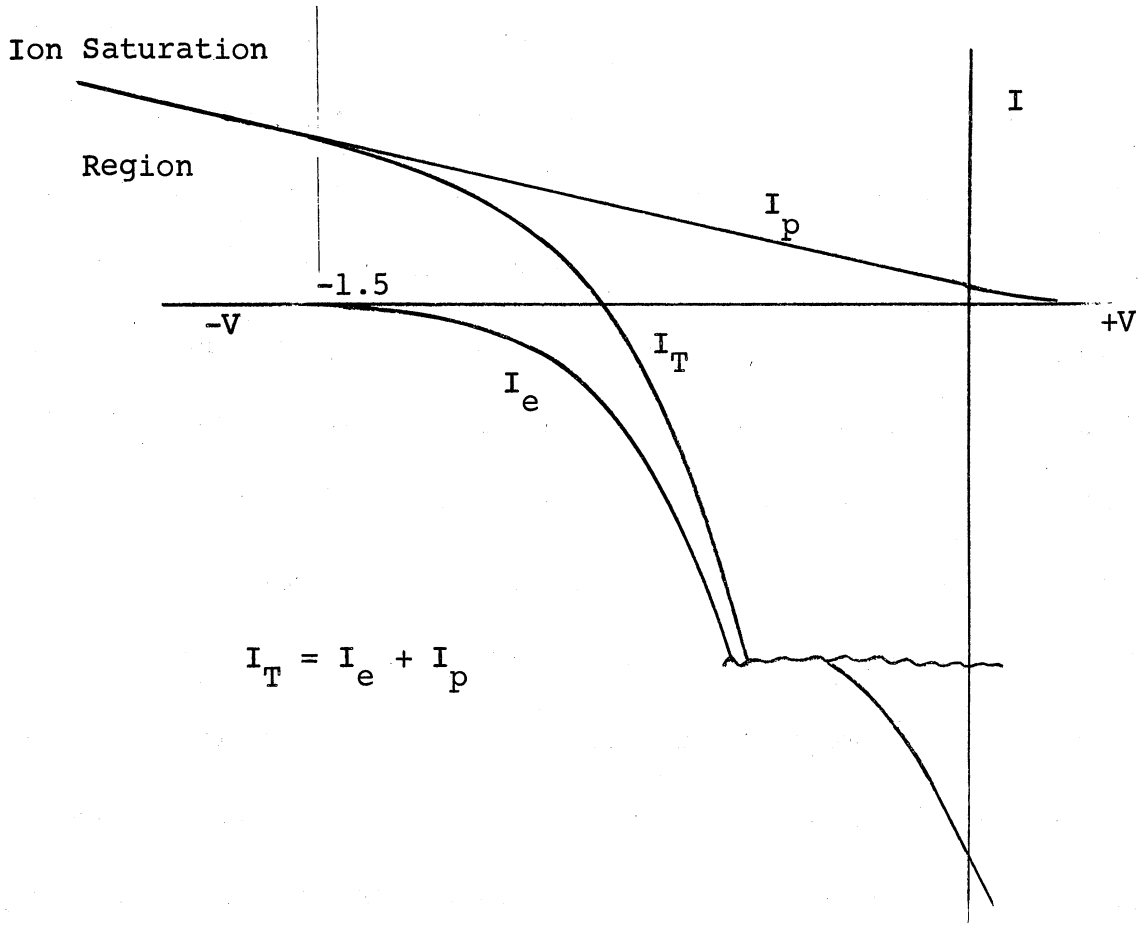


Fig. 2. Single Spherical Electrode Volt-Ampere Characteristic.

and current data are then telemetered to the ground for analysis.

Each voltage source, commonly referred to as a δV generator, establishes a potential across its pair of electrodes in the plasma. As an electrode is driven negative, with respect to the plasma, low-energy electrons are repelled and positive ions are attracted. The electron current falls to zero at a potential that is a function of the average energy (temperature) of these particles, as in Fig. 2. In the temperature range encountered (500-3000° K), this occurs between -0.3 and -1.5 vdc. Further excursions, to about -3 vdc, serve to define the positive ion saturation region of the V-I curve. The complete characteristic of the bipolar probe, shown in Fig. 3, is obtained by alternately reversing the polarities of the electrode pairs. Thus the dynamic range required of the δV's is -3 to +3 vdc.

In early experiments these requirements were fulfilled by two ganged, motor-driven potentiometers, each connected to a separate, regulated battery source, as shown in Fig. 4. This arrangement adequately fulfilled the requirements from the system point of view. The potentiometers provided linearity and duality; the motor shaft provided synchronization and adequate electrical isolation, and the batteries provided accurate reference voltages.

However, since the applied voltages vary linearly, the graphic record of the dynamic volt-ampere characteristic of the probe is a continuous curve. This feature necessitates tedious point-by-point graph reading to provide digitized data for computer solution of the pertinent variables, i.e., ionospheric electron temperatures and ion densities as a function of altitude.

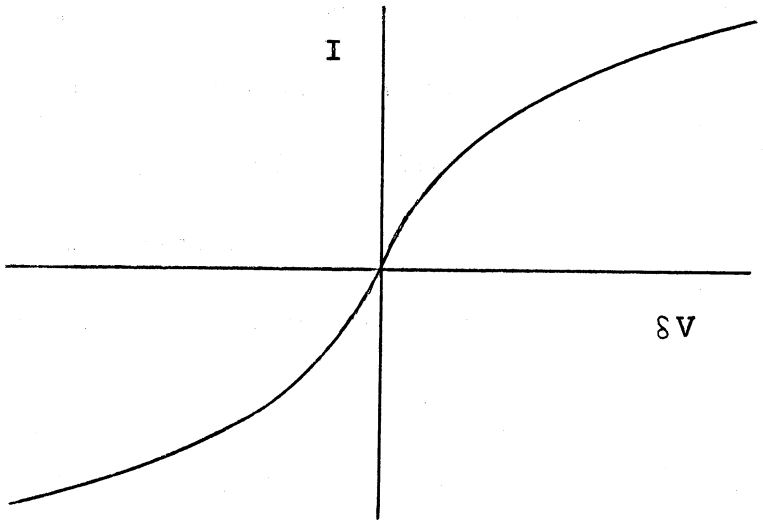


Fig. 3. Volt-Ampere Characteristic of Equal Area Bipolar Probe.

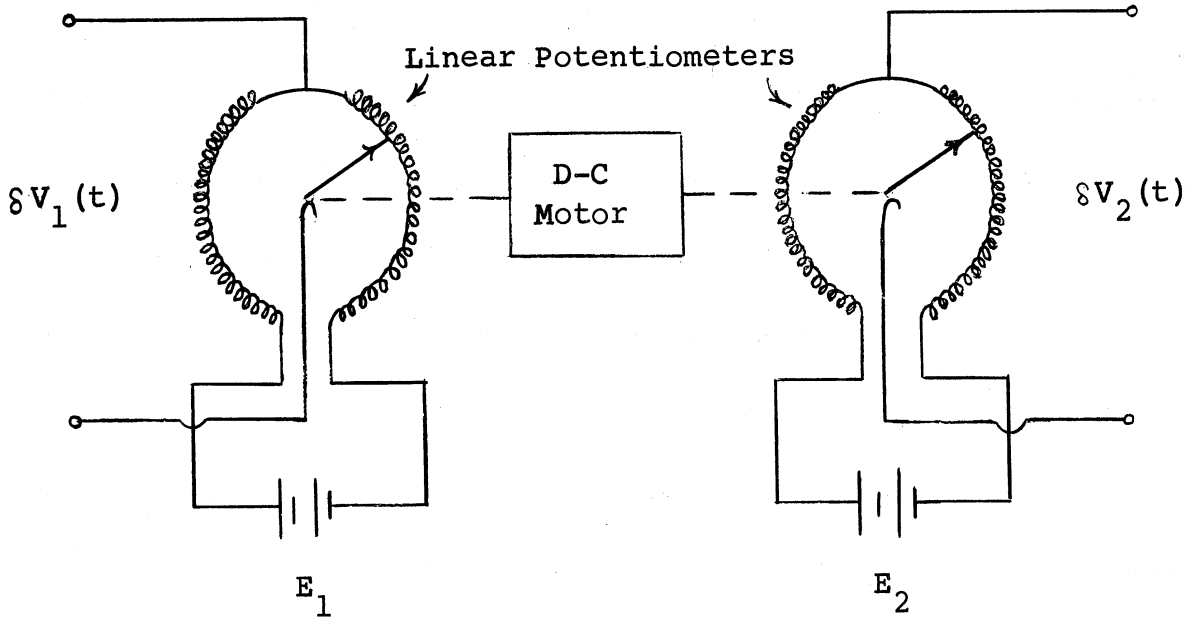


Fig. 4. Motor - Driven δV Generator.

Experience with these rocket probes has shown that five minutes of flight data require some 6 man-months of data reduction time, mainly as a result of the analog to digital conversion problem implicit in the graph-reading process mentioned above.

The improvements desired in equipment or techniques obviously must not compromise present accuracy for the sake of short-term economy. Yet, from the magnitude of the time intervals cited, it can be seen that the potential economic benefits to be reaped in this area are substantial. Hence it was thought expedient to reduce this excessive time lag by programming the δV generators to apply a series of discrete, digitized voltages across the probe electrodes, resulting in data in a form more conveniently read from the telemetered record. The ideal waveform can be described mathematically in terms of the Unit Step Function, U(t), i.e.:

$$V_o(t) = K_o + K_1 \left[U(t) + U(t - t_o) + \ldots U(t - nt_o) \right] \qquad (1)$$

where K_o can be an arbitrary d-c level, K_1 is an adjustable scale factor, t_o is the step length and n is the number of steps per cycle. Figure 5 describes this "stairstep" waveform graphically.

The following sections will discuss methods of generating this waveform, with provision for the two isolated outputs required by the experiment. Subsequently, the engineering details of the design of a circuit suitable for flight will be described.

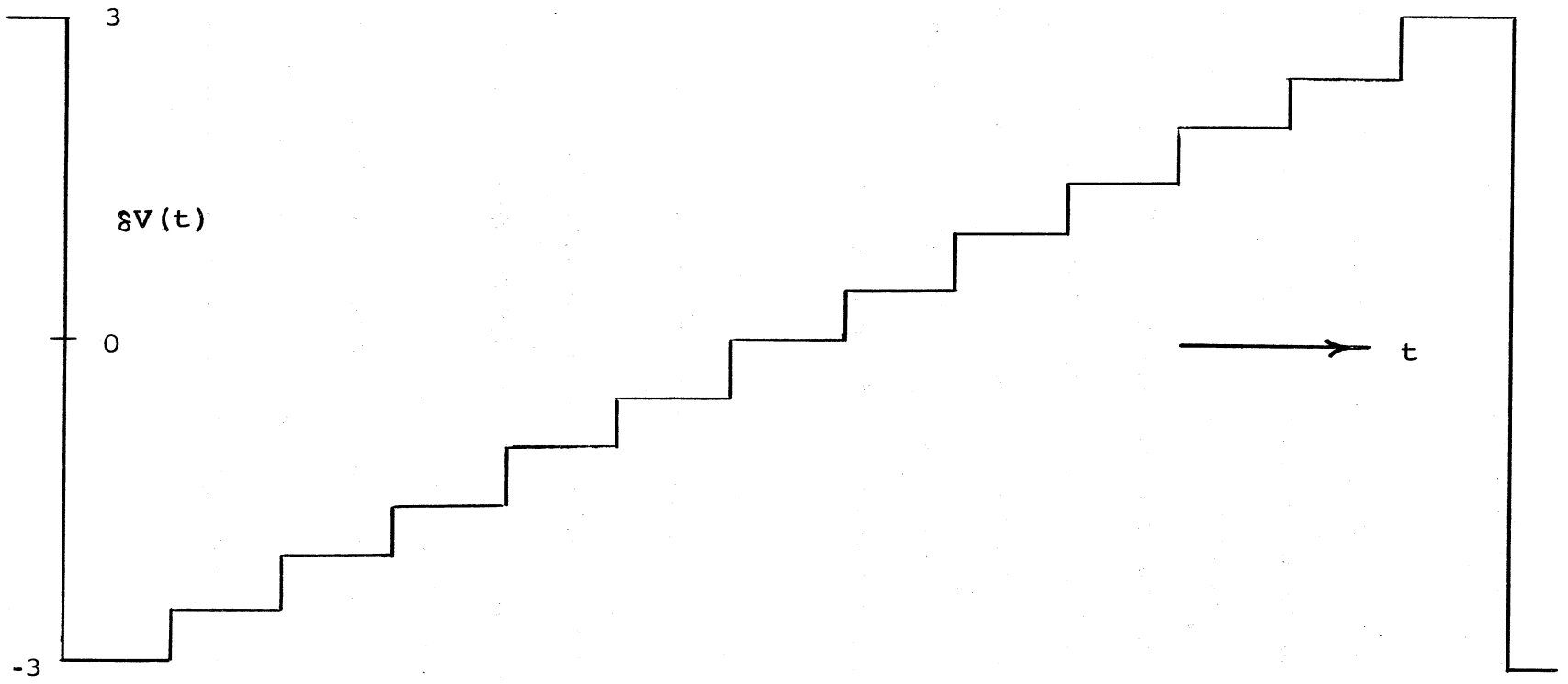


Fig. 5. Ideal "Stairstep" Waveform.

II. SYSTEM DESIGN

The System Design aspects of the problem consist in the optimum trade-off of performance specifications on the one hand, and the functional characteristics of realizable equipment, circuits, components and techniques, on the other. At this stage, initial solutions will be attempted in terms of symbolic "Black-Box" devices.

Initially, modifying the motor-driven δV generator to fulfill the new requirements was considered. Such modification would involve replacing that section of the system accounting for the linearity, i.e., the potentiometers, with a device exhibiting a discrete characteristic as a function of shaft position. This suggests a non-shorting, rotary switch. A preliminary design figure of 30 individual voltage levels per cycle [$n = 30$ in Eq. (1)], dictated switches whose cost and physical size were too great. This, as well as subsequent system modifications reducing the volume allotted to the δV generators to approximately two cubic inches, directed the course of the development toward an all-electronic solid-state system.

Electronically duplicating the desirable features of the electromechanical, motor-driven switch scheme imposes two general system-type problems:

(1) Generation of the stairstep-waveform subject to the stated volume limitations, and

(2) Provision for dual outputs synchronized and isolated to the degree afforded by the common motor shaft.

Although an effort will be made to treat each problem individually, their optimum solutions are not independent. As a result, it is advantageous to treat the

second problem first.

A. DUALITY

Means of satisfying the isolation and synchronization requirements for dual outputs can be divided into two categories. Either two distinct waveform generators are used as the design starting point, so that isolation is assured but synchronization must be provided, or a single waveform source is used, thereby eliminating the synchronization aspect, while complicating the isolation problem. Both approaches will be investigated below.

1. Dual Source—Identical, Isolated, and Synchronized Step Generators

If two separate electronic generators are used to obtain dual outputs, one may reasonably predict that each will be more involved in components, and hence less reliable than the electromechanical version of Fig. 4. The increased complexity suggests that some sort of voltage monitoring would be necessary for comparison of the two outputs. It is apparent from the nature of the experiment that an indication of a discrepancy between the two outputs will only confirm that the data are in error, since the relations between the measured variables, δV and I, are known in a useful way only under the precise guard-field condition that $\delta V_1(t) = \delta V_2(t)$. Therefore it is essential to use some sort of automatic feedback control to maintain the equality of step levels whenever separate generators are employed.

It is thus necessary to compare the voltages across the two isolated electrode

pairs, and to provide for feedback voltage control without introducing any mutual current paths. This is not feasible, even with high-input-impedance vacuum-tube circuits, because of the common (ground) connection between input and output in three element active devices. Therefore, without feedback voltage control and the assurance it provides, separate δV generators must be considered too unreliable for use in a dual system.

2. Single Source—Dual Output Systems

An alternative to the dual generator system is to generate a single voltage waveform and use it to drive a device that will in turn provide two identical, isolated reproductions. Two possibilities have occurred to the author: one involves the use of a dual-secondary transformer; the second makes use of switching techniques.

a. Dual-Secondary Transformer.—A transformer will provide dual, isolated outputs from a common source, but it is not a d-c operated device, and not directly applicable to the transfer of the 10-msec d-c pulses of Fig. 5. Therefore, modification of the input waveform is necessary to utilize the isolating features of the transformer as an output device. Specifically, it can be shown that the longest possible flat-topped wave that can be passed through a miniature pulse transformer with reasonable droop has a width of the order of 10 μsec. Therefore it would be necessary to chop each of the 30 required voltage levels into 1000 short pulses of 10-μsec duration. A block diagram of a method of implementing this idea is shown as Fig. 6.

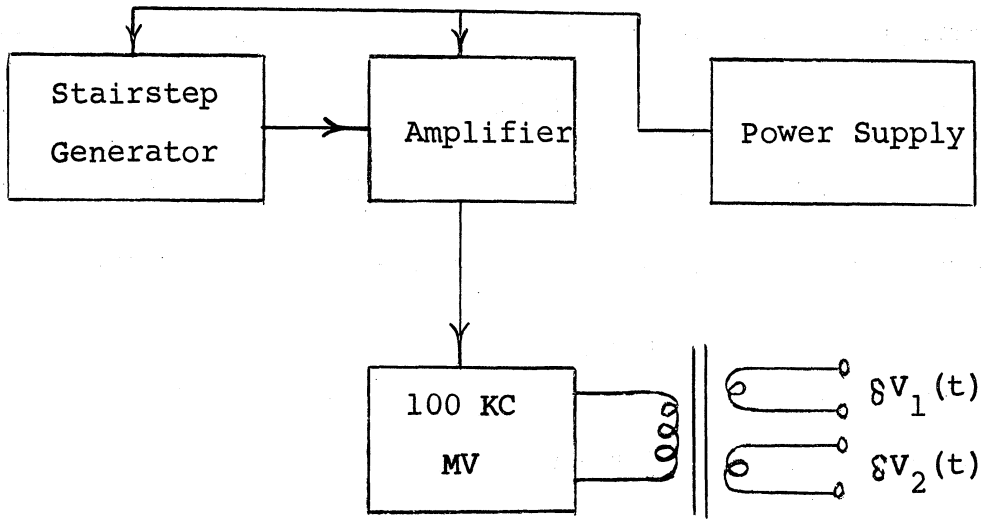


Fig. 6. Stairstep Generator with Transformer Coupled Dual Output.

The stairstep voltage generator output would be used as the collector supply for a 100/sec multivibrator oscillator. This arrangement would act as a combined Amplitude and Frequency Modulator. The AM would alter the magnitude of the output according to Eq. (1), while the FM arises from the fact that the charging voltage of the multivibrator RC circuits also varies, thus changing the pulse width. But if the center frequency were chosen so that the minimum frequency output does not result in unduly distorted pulses, this feature could be tolerated.

A more seriously undesirable feature is the shape of the composite envelope formed by the pulses. At best, it represents only an approximation to the desired flat-topped waveform. As the chopping rate is increased to reduce droop and to afford a closer approximation, rise times and switching transients become increasingly significant and detract from the useful data-collection time per cycle. Although an acceptable solution might be

reached using this approach, it is not to be expected without considerable compromise between the quality of the stairstep waveform and the volume of the output transformer.

b. Switching Techniques.—A general approach to the method of switching techniques is shown in block diagram form as Fig. 7.

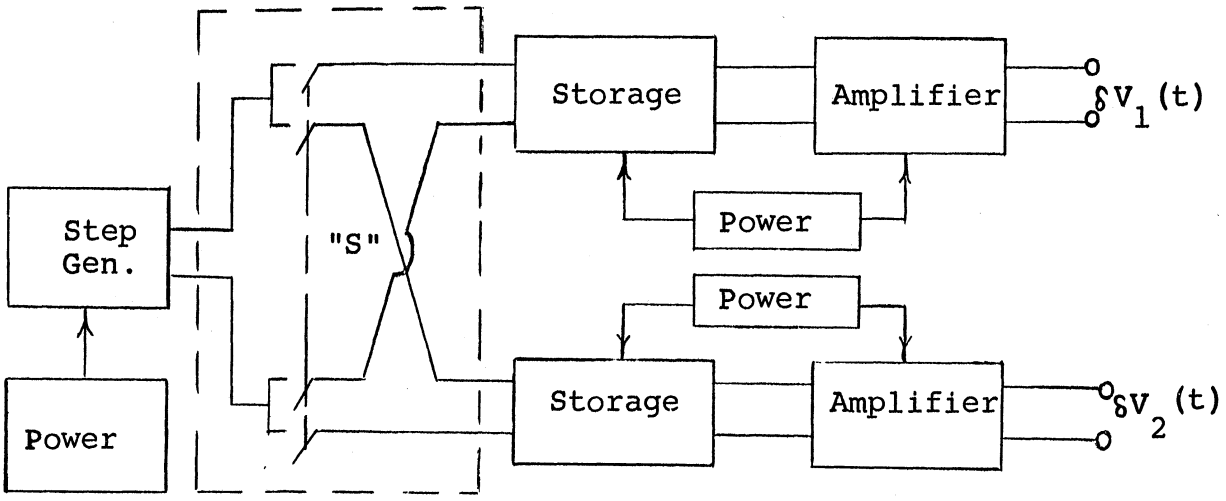


Fig. 7. Block Diagram of Stairstep Generator with Switched Dual Outputs.

Here a single source charges two storage devices (presumably capacitors) connected in parallel, thereby satisfying the synchronization requirement in addition to providing identical voltage amplitudes. Now d-c isolation can be achieved by activating the switches, which remove the source and separate the two output circuits. To achieve reasonable data-collection efficiency, the charging time must be kept small with respect

to the 10 msec step length.

It is clear, then, that this approach simply transfers the major system problems to the box labeled "S". Specifically, "S" must:

(1) have an asymmetrical switching cycle of 10:1 or better.

(2) be synchronized in some fashion with the source,

(3) have equal and low forward impedance in both paths, and

(4) have equal and high back impedance in both paths.

Before investigating possible means of fulfilling the above objectives, it is well to point out that the reason given above for rejecting feedback techniques, namely, that simultaneous isolation and feedback control were mutually exclusive, must now be modified in light of the time-shared case of Fig. 7. However, although realizable, neither voltage comparison nor automatic voltage control would now be necessary since both storage circuits would be in parallel while charging.

Returning to the selection of the switching unit "S" of Fig. 7, three devices deserve consideration:

(1) relays,

(2) transistors, and

(3) diodes.

Both relays and transistor switches require an external synchronization connection with the source, making unreliability likely. Furthermore, isolation of 100 megohms or better is desired. This figure is far in excess of the open-circuit impedance of present-day transistor switches. While relays are capable of exceeding this specification, they are not adapted to meeting the severe duty-

cycle requirements of approximately 0.5 msec "on" and 9.5 msec "off".

Diodes, on the other hand, would be ideal from two standpoints: they can be driven to forward resistances approaching 2 ohms and reverse resistances of the order of 1000 megohms. Being passive devices, moreover, synchronization and duty-cycle would be source-controlled without additional synchronization paths.

Requirements for the step generator of Fig. 7 follow directly from the above. In addition to being stable and reliable, it must:

(1) generate the waveform described by Fig. 5,

(2) be capable of delivering the output in the form of low-impedance discrete pulses that can forward-bias the diode switches and charge the capacitors rapidly, and

(3) be capable of maintaining the diodes in a high-resistance portion of their characteristic between pulses.

Having thus reached some conclusions about the duality problem, we can now turn to the other major problem - generation of the stairstep waveform itself.

B. STAIRSTEP VOLTAGE GENERATOR

Various means of generating a stairstep waveform are suggested by a broad interpretation of the composition of the waveform shown in Fig. 5. Three different interpretations are given below.

1. A Train of Unit Voltage Steps, Delayed, Added, and Stored

The stairstep waveform can be considered to be composed of a series of unit voltage steps sequentially added or accumulated by a storage device. This suggests the generation of a train of unit steps driving an adder circuit modified by a feedback loop as in Fig. 8. The suitability of such an arrangement would be largely determined by the properties of the delay device shown in the feedback loop..

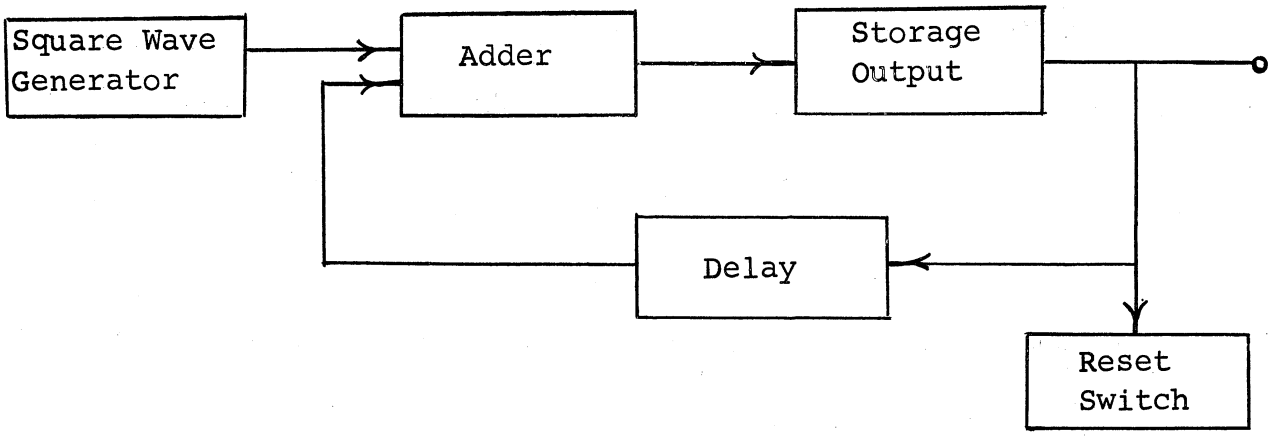


Fig. 8. Unit Step Implementation of Stairstep Generator.

The characteristics of delay devices are markedly dependent on the magnitude of the time delay required, which in this case is approximately 10 msec. This immediately rules out circulating delay devices of the lumped parameter or acoustic line varieties by virtue of their size. What is required, then, is an active delay device of the multivibrator class.

The weak point of this system, however, is the adder, which must be linear over a dynamic range of at least six volts.* Its inherent non-linearities could be compensated for by appropriate networks in the feedback

*A conservative figure, it will develop later.

loop. Yet, regardless of compensation, the adder would introduce unreliabilities, such as drift, previously avoided by the use of discrete devices such as the square-wave pulse generator and the active delay circuit. Fortunately, other waveform compositions are available for investigation.

2. Triggered Steps

The desired stairstep waveform can also be interpreted as composed of square waves added in series as shown in Fig. 9. Waves of this type could

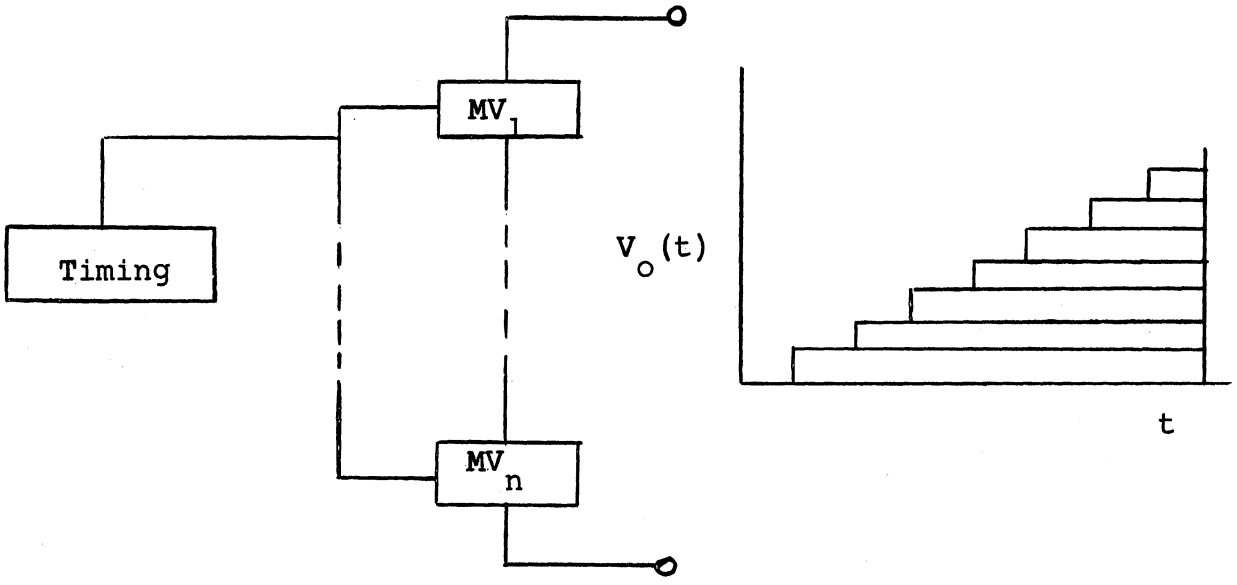


Fig. 9. Implementation of Stairstep Waveform Considered as Sum of Square Waves

be generated by bistable multivibrators, or other gating arrangements, all of which exhibit two salient characteristics:

(1) Accurate voltage increments could be assured since each level would be switched "ON" or "OFF" with no intermediate states possible.

(2) Separate square wave generators and switching arrangements would be required for each voltage level desired.

These characteristics suggest an electronic duplication of a mechanical switch in that each switch position and associated voltage tap correspond to a square-wave oscillator and associated gating or trigger circuit. Therefore, such an implementation has the same limitation as the mechanical switch: excessive size. In a general effort to avoid implementations that involve duplication of circuits and components performing identical operations sequentially, step generators containing storage or delay elements are necessary.

There are single circuits that combine the separate functions of addition and storage. One that uses capacitors for storage, a diode switching network for addition, and the timing circuits of a multivibrator for delay is the storage counter,[1] shown in Fig. 10. The exponential relationship between the sizes of the output steps can be eliminated by charging C_1 to a voltage proportional to the output voltage plus the input step. This can be accomplished by a variety of feedback techniques, one of which is shown as Fig. 11.

A derivation of the performance of these circuits is given in Appendix I. The conclusion that adequate step equality can be achieved by using feedback has great significance. For one thing, it means that the need for a linear d-c amplifier of wide dynamic range is eliminated, since this circuit embodies a method of pulse addition whereby the charge accumulated on one capacitor can be transferred to a second capacitor regardless of the latter's state of charge. This, in turn, means that the same components are utilized in generating an arbitrary number of equal steps - a feature not shared by other circuits and a virtual necessity if the volume limitations are to be met.

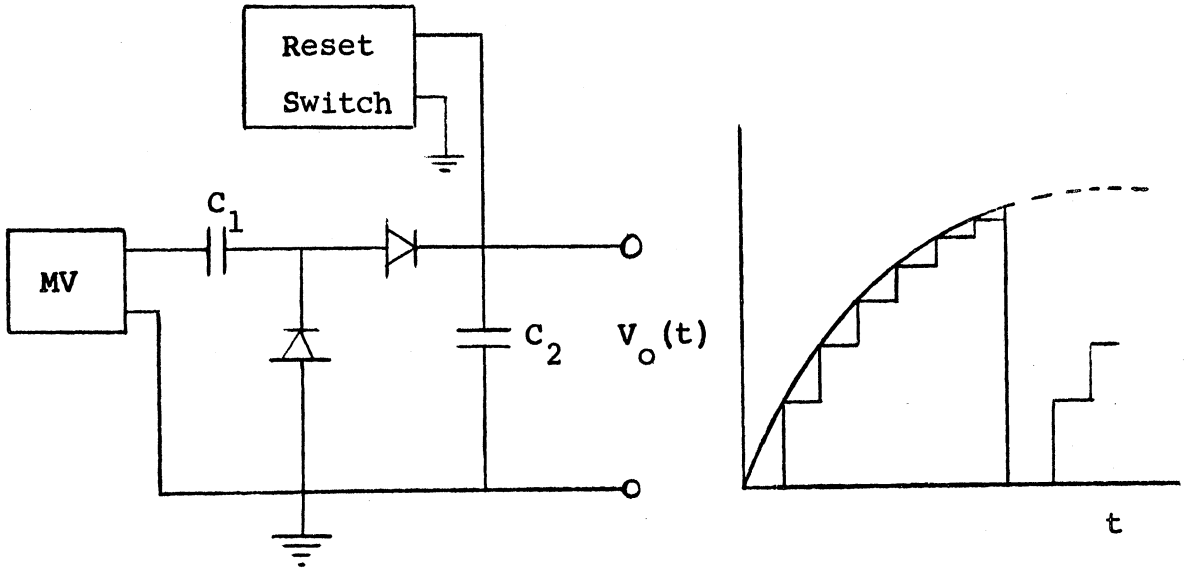


Fig. 10. Storage Counter Circuit with Output Waveform.

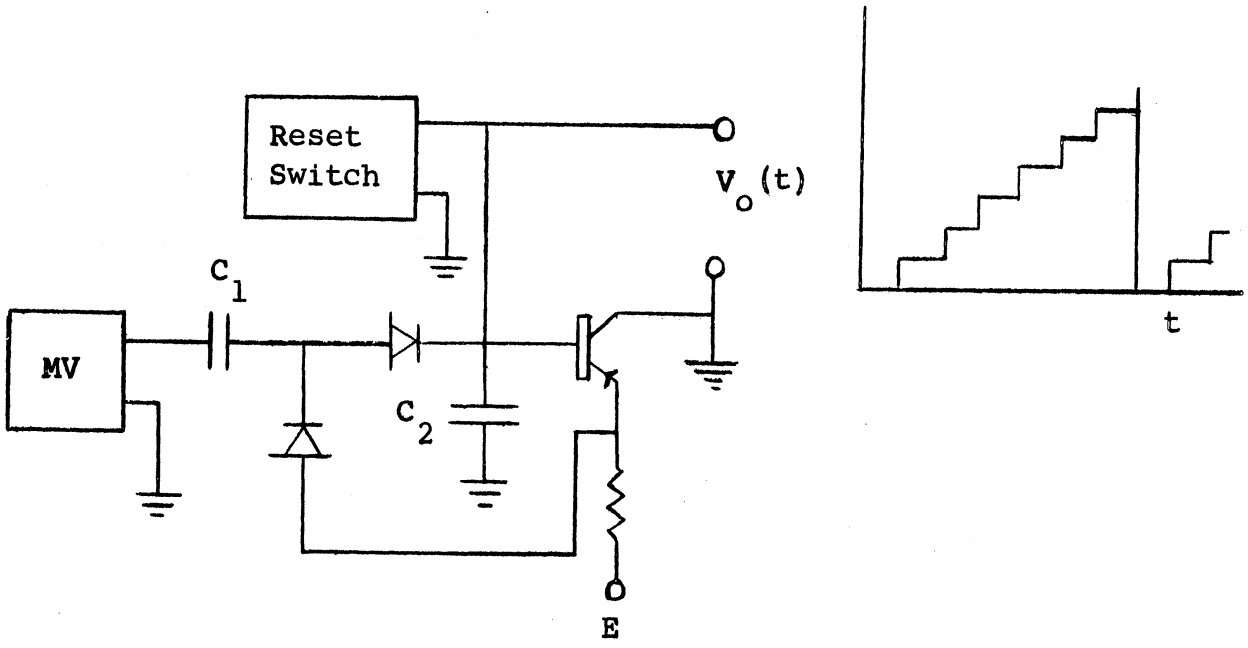


Fig. 11. Storage Counter Circuit Linearized by Feedback with Output Waveform.

However, the mechanism by which this charge transfer takes place, the familiar exponential process, never reaches steady state in any finite time. This is of negligible consequence in applications of pulse counting and frequency division for which the circuit was originally designed, but is a serious limitation in the present application, where an accurate voltage reference source is required. It will be shown below, however, that the same concept of charge transfer, combined with a faster transfer mechanism, will preserve the advantages coincident with the simplicity of this circuit.

3. Gated Linear Sweep

There is still another interpretation of the composition of the waveform represented by Fig. 4 that avoids duplication of circuits. This is to consider the waveform as the limiting case of a gated linear sweep as the charging time, t_c in Fig. 12, becomes arbitrarily small.

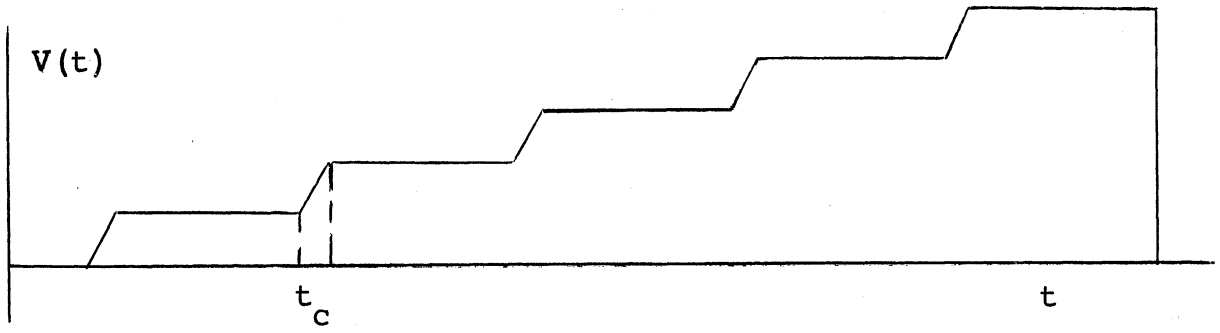


Fig. 12. Stairstep Waveform Considered as Limiting Case of a Gated Linear Sweep.

Linear sweeps are generated by very common and well-understood circuits. The simplest is the familiar RC integrator circuit shown in Fig. 13, where

$$e_o(t) = E(1 - e^{-t/RC})$$

$$= E\left\{\left[\frac{t}{RC}\right] - \frac{1}{2!}\left[\left(\frac{t}{RC}\right)^2\right] + \frac{1}{3!}\left[\left(\frac{t}{RC}\right)^3\right] - \ldots\right\} \quad (2)$$

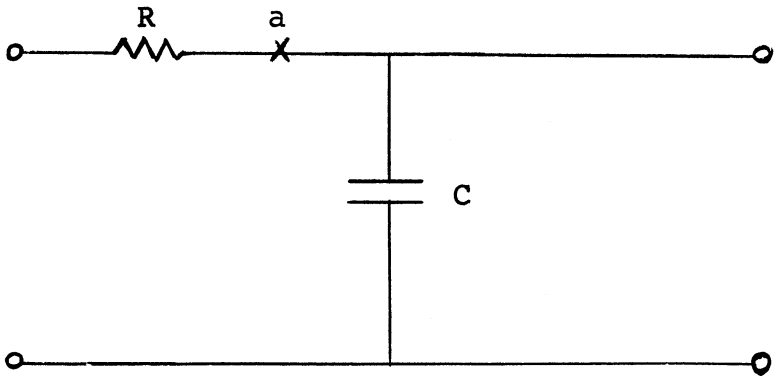


Fig. 13. RC Integrator Circuit.

Approximate linearity can be achieved by making RC very much larger than t, so that

$$e_o(t) \simeq E\left(\frac{t}{RC}\right) \qquad (3)$$

To achieve periods of constant output voltage, the charging current to capacitor C must be periodically interrupted by a switch placed at point "a". Either a tube or a transistor would be a suitable gate since both can be readily controlled by an external timing device. An additional requirement on the gate is that the current through it must be independent of the voltage across the capacitor to make the step increments proportional to time. Transistors, being current-operated devices, are ideally suited to this task. Reference to a typical set of transistor output characteristic curves as in Fig. 14 shows that, over a considerable portion of the operating range, the collector current, I_c, is virtually independent of collector voltage. This property of the transistor allows its use as a gate to achieve the waveform of Fig. 12, by the circuit configuration of Fig. 15.

Ideally, when switch S is in position 1, constant base current flows, resulting in constant collector current and linearly increasing output voltage.

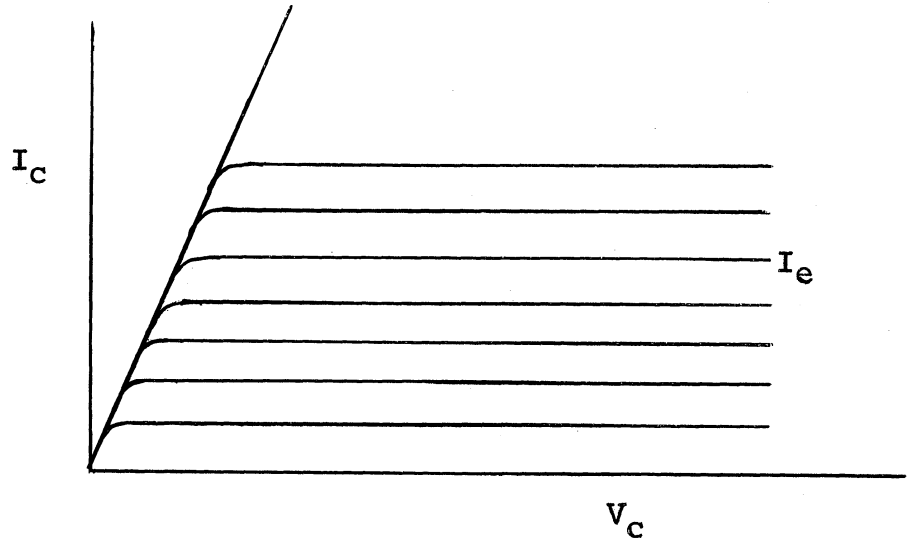


Fig. 14. Typical Junction Transistor Collector Characteristics.

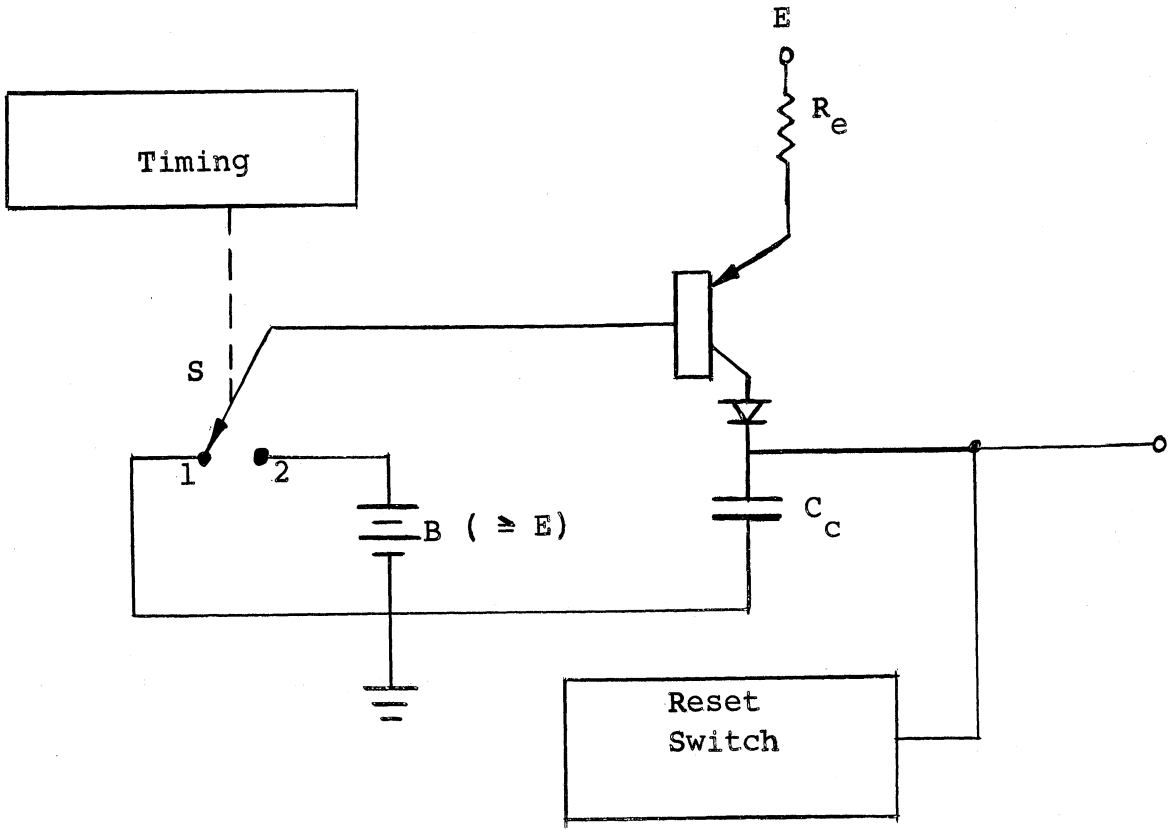


Fig. 15. Gated Linear Sweep Circuit.

In position 2, the transistor is cut off, since B is more positive that E, with the result that the emitter current is reduced to zero and the output voltage is constant. The timing device should be sufficiently asymmetrical to make the charging time negligible. Thus a gated linear sweep approach leads to a feasible step generator and, in addition, one that requires significantly fewer components than the other methods considered. It is clear, however, that if successive step amplitudes are to be identical, the charging times (the time S is in position 1) must be maintained constant.

4. Q-Transporter

It will be observed that the gated linear sweep circuit can be considered as a modulator, where the square-wave oscillator amplitude modulates the waveform generated by the sawtooth oscillator formed by R_e, C_c, and the voltage-operated reset switch. Not only must the step increments be equal, which has been the primary concern up to now, the level of each individual step must also remain constant from cycle to cycle.* This precise recurrence of d-c levels will occur only if the square wave and sawtooth oscillators are synchronized and locked in phase. It is, of course, possible to synchronize two oscillators so they become harmonically related. When their frequency ratio becomes large, however (e.g., 30:1, as it is here), pulse-counting synchronization systems require several stages of frequency dividers. This would make the control circuit almost as large as the controlled circuit, which seems extravagant.

*It is helpful to consider a stairstep waveform as a special case (zero velocity) of an "escalator" waveform in which the steps move progressivley up or down from cycle to cycle.

It is possible to eliminate the need for synchronization by making the length of time collector current flows independent (over a suitable range) of the period and duration of the timing pulses, so that, whenever a timing pulse is received, the gate is turned "ON" for a time that is less than, but not determined by, the duration of the timing pulse. This is accomplished by adding a capacitor, C_e, in the emitter circuit of the gating stage as in Fig. 16. Effectively, if R_e is large, C_e becomes the sole power source for

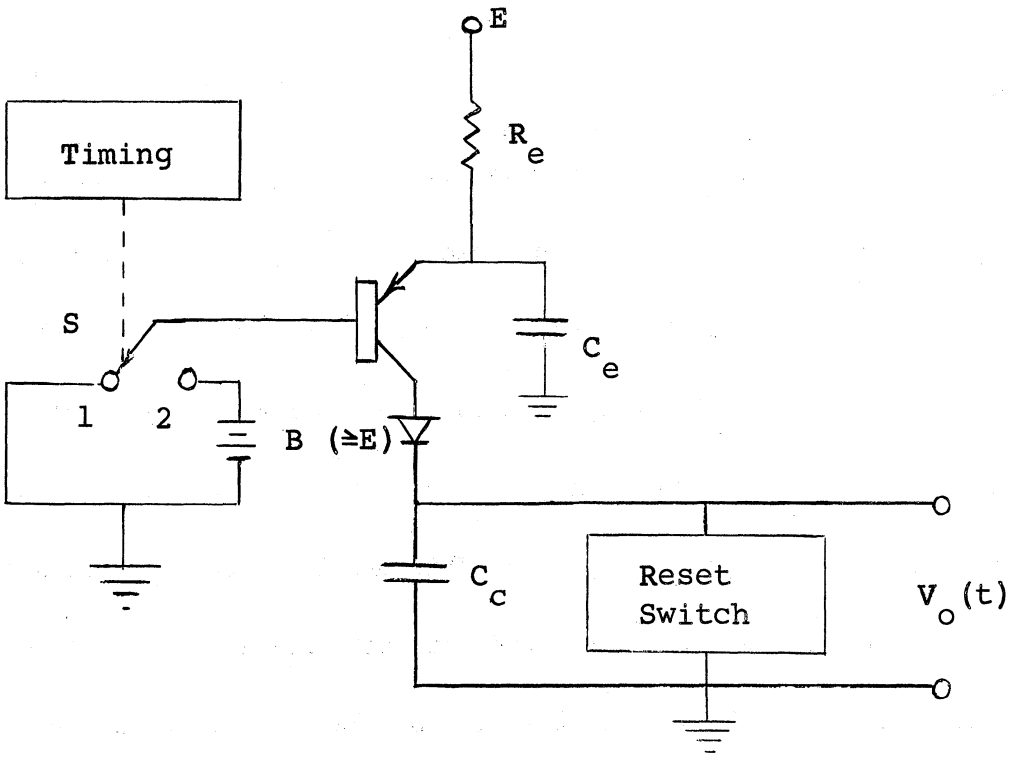


Fig. 16. Modified, Gated, Linear Sweep Circuit.

the transistor. Since the energy stored in C_e is finite and discrete, the gate will remain open (conducting) during a timing pulse only as long as the emitter voltage remains greater than the base-emitter threshold of the transistor. Transistor saturation resistances are typically so low (≃40 ohms) that RC circuits can be designed to decay during the duration of any reasonable

timing pulse. The discharge of the emitter capacitor, C_e, results in a pulse of collector current which deposits a discrete quantity of charge in the output capacitor, C_c, and produces a corresponding step in the output voltage. The depletion of the charge on C_e results in a quiescent cut-off condition that continues until the termination of the timing pulse. When switch S reverts to position 2, the resulting jump in base voltage unclamps the emitter voltage, which rises as C_e charges through R_e toward the supply voltage E. If steady state is achieved long before the next timing pulse, the amount of charge stored in C_e will be known and discrete. Thus the discrete increments made in the output voltage are independent of both the number of previous charging pulses and a wide range of variation in the frequency of the timing pulses.

This mode of operation of the transistor is based on the same physical principle that makes operation as a constant current source possible - yet the current is by no means constant, or even linear, by virtue of the character of the power source in the emitter circuit (C_e). For this reason it is convenient to think in terms of charge rather than current, i.e., when C_e discharges it gives up a charge, q_e, α of which is deposited on C_c in the collector circuit during each timing pulse. Hence, I will refer to this circuit as a "Q-Transporter."

By means of the mechanism described above and the switching technique of Part IIB, a satisfactory circuit for the generation of a stairstep waveform may now be designed. Subsequent sections will deal with the engineering design problems concerned with producing an efficient, reliable, voltage- and temperature-stable package.

III. CIRCUIT DESIGN

In this section the details of the Q-Transporter circuit will be examined and relations governing its use explained. A trigger circuit that provides a much sharper cutoff mechanism than base-emitter junction clamping shown in Fig. 16 is developed and an asymmetrical multivibrator timing source is given. Output circuits, such as the Unijunction voltage-operated reset switch, a low output impedance emitter follower amplifier and a zero reference circuit, are discussed in detail. Finally, power-supply requirements are treated and provision is made for compensation of random voltage and temperature changes.

A. Q-Transporter

As noted above, the fundamental property of junction transistors whereby collector current is independent of collector voltage for constant emitter current forms the basis by which equal voltage steps are generated. This property is depicted graphically by the static collector characteristic curves and described analytically by the equations of Ebers and Moll:[2]

$$I_e = \frac{\alpha_I I_{co}}{1-\alpha_N\alpha_I}\left[\exp\left(\frac{q\phi_c}{kT}-1\right)\right] - \frac{I_{eo}}{1-\alpha_N\alpha_I}\left[\exp\left(\frac{q\phi_e}{kT}-1\right)\right] \quad (4)$$

$$I_c = \frac{\alpha_N I_{eo}}{1-\alpha_N\alpha_I}\left[\exp\left(\frac{q\phi_e}{kT}-1\right)\right] - \frac{I_{co}}{1-\alpha_N\alpha_I}\left[\exp\left(\frac{q\phi_c}{kT}-1\right)\right] \quad (5)$$

where I_{co} and I_{eo} are the collector and emitter saturation currents, respectively; α_N and α_I are the normal inverted current gains, respectively; ϕ_c and ϕ_e are the collector and emitter junction voltages, respectively; T is the temperature in degrees Kelvin and $q/k = 1/11{,}600$.

These equations describe the operation of the transistor's pair of "internal diodes" in terms of the external currents. They are valid for large (d-c) input signals in all three operating regions: cutoff, active, and saturation. For current values at which the internal IR drops significantly alter the junction voltages, equivalent circuit analysis techniques, employing linear circuit elements, can be used in conjunction of the above relations.

Solving Eqs. (4) and (5) for I_c in terms of I_e yields:

$$I_c = I_{CO}\left[1 - \exp\left(\frac{q\phi_c}{kT}\right)\right] - \alpha_N I_e \qquad (6)$$

For the operation contemplated, the collector junction will always be reversed biased, so that ϕ_c will be negative. The exponential term will be less than .005 and hence negligible compared to 1, for ϕ_c less than -0.155 volts at T = 65°C, the highest operating temperature expected. Thus, if the transistor is operated in regions where the collector junction is reversed biased by more than 0.155 volts, the following simplication can be made:

$$I_c = I_{co} - \alpha I_e \qquad (7)$$

At this point a preliminary calculation is helpful to show the critical approximations and the criteria by which the optimum commercial transistor will be selected. Assume that in Fig. 16 the base-emitter junction is abruptly forward-biased so that collector current flows as given by Eq. (7). From the nature of the emitter source (C_e charged to voltage V_c), it is evident that I_e will be of the form $I_1 e^{-t/\tau e}$. (I_1 = maximum permissible emitter current).

Thus:

$$I_c = I_{co} - \alpha I_1 e^{-t/\tau e} \qquad (8)$$

and $$\delta V_o = \frac{Q_c(t)}{C_c} = \frac{1}{C_c}\int_o^T I_c\, dt$$

$$= \frac{1}{C_c}\int_o^T (I_{co} - \alpha I_1 e^{-t/\tau_e})\, dt$$

$$= \frac{I_{co}T}{C_c} - \frac{\alpha I_1}{C_c}(1 - e^{-T/\tau_e}) \qquad (9)$$

where αI_1 is negative for current flow out of the PNP transistor shown and where C_c will be determined by other considerations to be at least 1.0μfd. T, the duration of the charging period, and τ_e, the emitter-base circuit time constant, will subsequently be shown to be approximately 60 and 40 μsecs respectively. Typically, values of I_{co} and I_1 for the silicon PNP transistor 2N1036* are 0.005 μa and 20 ma, respectively. At 65°C, I_{co} will have increased to about 0.4 μa, which is still four orders of magnitude less than I_1 thus making the first term of Eq. (9) negligible during the charging phase when I_1 exists.

The question of leakage currents cannot be ignored. however, since I_1 is zero during most of the cycle. The effect of leakage currents during these periods will be treated in Section V on Error Analysis. But since under the most adverse temperature conditions I_{co} is negligible compared to I_1, the analyses can be extended by use of the linear equivalent circuit, which is commonly introduced for small signal a-c analysis. However, the assumption of small excursions about a stable operating point, commonly made in an a-c analysis, is by no means justified here. In fact, the operation contemplated will traverse

*Manufacturers' ratings and equivalent circuit parameters for all transistors used are given in Appendix II.

such an expanse of the operating region that substantial changes in the equivalent circuit parameters will result. The equivalent circuit of Fig. 17 is nonetheless extremely useful for establishing an important feature of the "Q-Transporter"; changes in the equivalent circuit parameters, resulting from bias current changes that appreciably alter the linearity of operation, will not affect the independence of collector current on collector voltage, provided that the junction-biasing conditions required by the Ebers and Moll equations are satisfied. The parameters of the equivalent circuit are shown to be functions of the bias currents and it is assumed that current-weighted average values exist for any operating path. For the PNP transistor shown, with both switches in position 2, $I_e = 0$, if B is greater than E. During this phase,

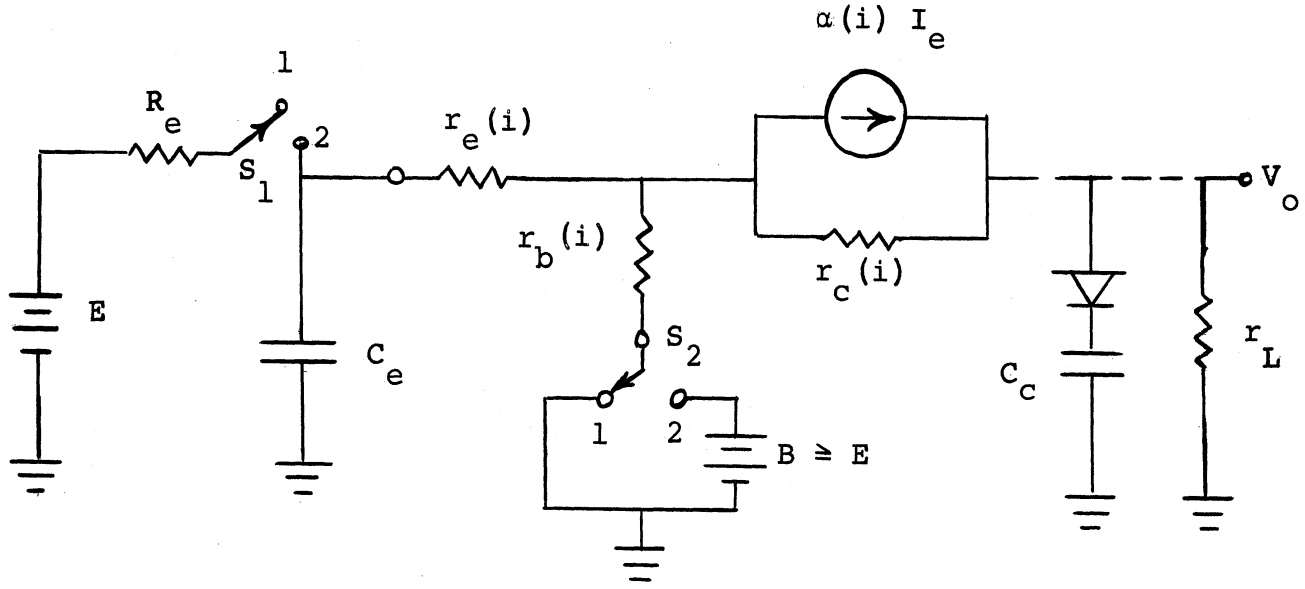


Fig. 17. Q-Transporter Equivalent Circuit.

C_e charges through R_e toward the supply voltage E. When both switches are changed to position 1, C_e discharges into the input impedance, $h_{ib}(i) = r_e(i) + (1 - \alpha)r_b(i)$, of the transistor causing $I_c = \alpha(i)I_e$ to flow in the collector circuit. When the current flow is terminated, either by equilibrium

between the voltages across C_e and C_c or by externally activating the switches, C_e will have lost a charge proportional to its change in voltage, whereas α of this charge appears across C_c and $(1 - \alpha)$ is dissipated in the input circuit resistance. Thus:

$$\Delta V_o = \frac{\Delta q_o}{C_c}$$

$$= \frac{\bar{\alpha} \Delta q_i}{C_c}$$

$$= \bar{\alpha} \Delta V_{C_e} \frac{C_e}{C_c} \tag{10}$$

where $$\bar{\alpha} = \frac{\int_{i=0}^{I} \alpha(i)\, i_e\, di}{\int_{i=0}^{I} i_e\, di} \tag{11}$$

is a current-weighted average which one would expect to be a constant somewhat less than α.

The significant result is with the form of Eq. (10). Anticipating future problems with variations in temperature, one could elect to sacrifice a possible voltage gain at this point in favor of making C_e identical to C_c. Thus, if placed in comparable thermal circumstances, the output would be:

$$V_o = \bar{\alpha} \Delta V_{C_e} \tag{12}$$

which is independent of the choice of temperature coefficients of both capacitors. Although this would permit the use of inexpensive capacitors for C_e and C_c as long as a matched pair could be obtained, it is an uneconomical solution from other standpoints. The value of C_c will be dictated by the maximum droop that can be tolerated when load current is drawn from it. The value of C_e, on

the other hand, cannot be selected independently of the circuitry by which its charge is replenished between pulses. It will be shown in the next section that the conflicting requirements of minimum step droop and minimum power consumption can best be resolved by matching the temperature coefficients of the two capacitors so that their ratio remains invarient, but need not necessarily be unity as first assumed.

B. TRIGGER CIRCUIT

In connection with implementing the base switch, labeled "S" in Fig. 15, it is assumed that a square-wave voltage source is available to provide the "Timing" pulses.

Consider first the circuit of Fig. 18, where an unilateral voltage divider

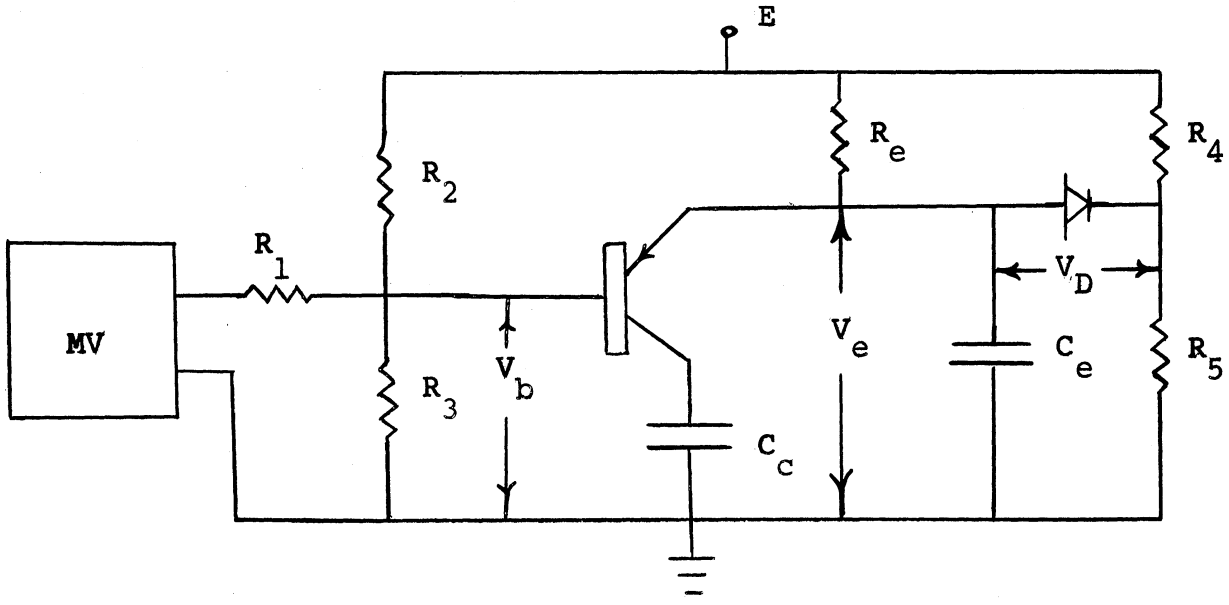


Fig. 18. Q-Transporter Trigger Circuit.

network has been added across C_e to permit charging to a steady-state voltage other than E. To find a relationship between the quiescent base voltage, V_b, and the voltage, V_e, to which the emitter is clamped by the divider, R_4 and R_5, when the base-emitter junction is reverse-biased and steady-state conditions exist, one can write for the emitter voltage:

$$V_e = V_{C_e} = \frac{R_5}{R_4 + R_5} E + V_D \qquad (12)$$

and for the base voltage:

$$V_b = \frac{R_3'}{R_2 + R_3'} E + V_D \qquad (13)$$

where:

$$R_3' = \frac{R_3 (R_1 + R_{MV})}{R_1 + R_3 + R_{MV}} \simeq R_3 \qquad (14)$$

since R_{MV}, the multivibrator open circuit resistance, is about 5 megohms, while the other resistances are of the order of several kilohms each. Thus the junction voltage is:

$$V_{be} = V_b - V_e$$

$$= \left(\frac{R_3}{R_2 + R_3} - \frac{R_5}{R_4 + R_5} \right) E + V_D \qquad (15)$$

It will be observed that Eq. (15) is linear and that the coefficient of E contains two terms of opposite sign. Thus the partial derivative of V_{be} with respect to E could be made to vanish by appropriate choice of the resistors. This would make the junction voltage independent of supply voltage variations. Proceeding formally,

$$\frac{\partial V_{be}}{\partial E} = 0 \qquad (16)$$

requires that:

$$\frac{R_3}{R_2 + R_3} = \frac{R_5}{R_4 + R_5} \qquad (17)$$

Since both voltage dividers are to have the same ratio, Eq. (17) suggests the possibility of (1) making the corresponding resistors equal, and (2) using the same components for both voltage dividers.

The latter can be achieved by the circuit shown in Fig. 19, which, in addition to consolidating the two voltage dividers, eliminates the separate emitter resistor, R_e. While the nature of the emitter voltage clamp has been

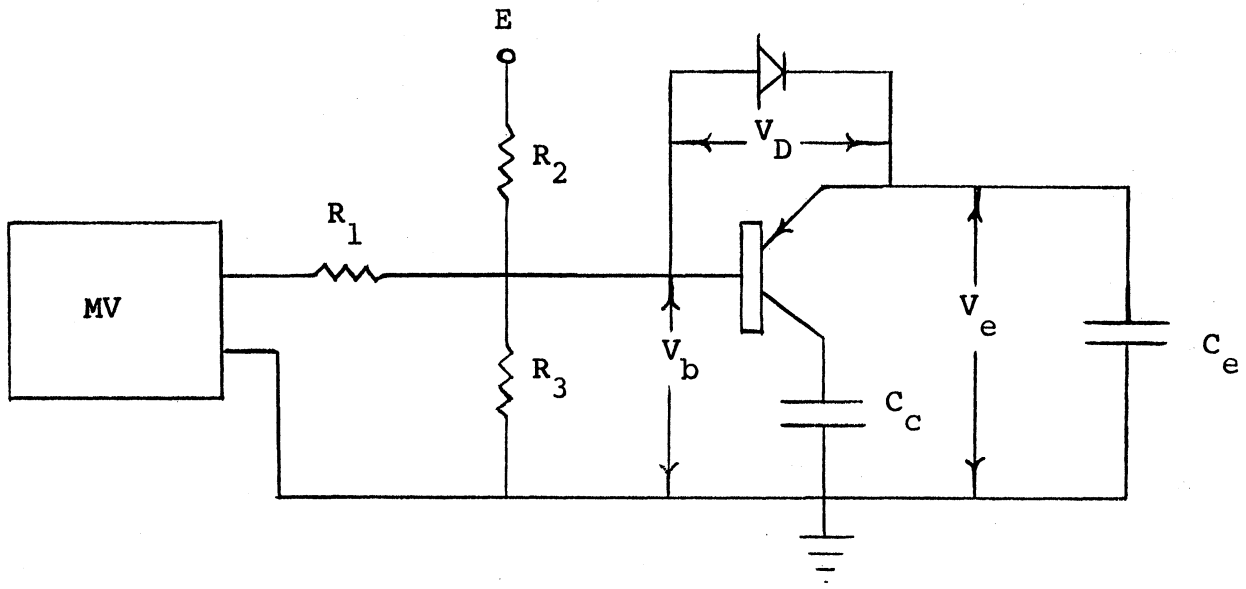


Fig. 19. Modified Q-Transporter Trigger Circuit.

changed from shunt to series to effect the consolidation, the repetitive property of the steady-state emitter voltage is preserved. Moreover, the diode paths connecting the base to the emitter, while bilateral, are mutually exclusive, so that discreteness of the transfered charge is assured.

The dynamic behavior of this circuit will now be investigated. Assuming that steady-state base and emitter voltages have been achieved, consider the instant the multivibrator switches "ON," changing its output impedance from R_{mv} to R_{SAT}, the collector to emitter saturation resistance (typically 40 ohms). If the switching is fast enough so that R_{SAT} can be considered a constant, the new base voltage will be:

$$V_b' = \frac{R_3''}{R_2 + R_3''} E \qquad (18)$$

where:
$$R_3'' = \frac{(R_1 + R_{SAT})\, R_3}{R_1 + R_{SAT} + R_3} \simeq \frac{R_1 R_3}{R_1 + R_3} \qquad (19)$$

If V_e exceeds V_b plus the threshold voltage of the forward-biased emitter-base junction (approximately 0.4 volts for silicon transistors), emitter current begins to flow:

$$I_e = I_o (1 - e^{-t/RC}) \qquad (20)$$

where:
$$R = h_{ib} + R_3 \qquad (21)$$

and:
$$I_o = (1-\alpha) \frac{V_e - V_D - V_b}{R + R_{SAT}} \qquad (22)$$

The time constant of the exponential term describes the rate of charge transfer between C_e and C_c. It can be seen that realistic values of resistance in Eqs. (19) and (21) indicate that R will not be less than 250 ohms. For C_e equal to 1.0 μfd, the minimum value of charge transfer time constant, τ_{min} will be approximately 250 μs. Thus it takes 1 msec (or 12% of the desired step duration) for the output voltage across C_c to reach 98% of its target value. Some improvement could be realized by reducing C_e, but this is not feasible for other reasons.* In any event, the basic problem of asymptotic charging and discharging of capacitors would still not be solved. The reader will recall that this is what led to the decision to reject the storage-counter circuit of Section II.

A charge-transfer circuit which reaches its target value in 1.0% of the step duration can be obtained by adding a capacitor in series with R_1, as in Fig. 20.

*Primarily the need to match the temperature coefficient of C_c.

After a trigger pulse this capacitor, C_1, would be charged (by the base current but mainly by the supply voltage through R_2 and R_{SAT}) so as to return the base voltage exponentially to the quiescent cutoff value, V_b. By proper selection of the time constant associated with the rise in base voltage, the exponential decay of the voltage across the emitter capacitor could be limited to the region of the first time constant, where the rate of charge transfer is

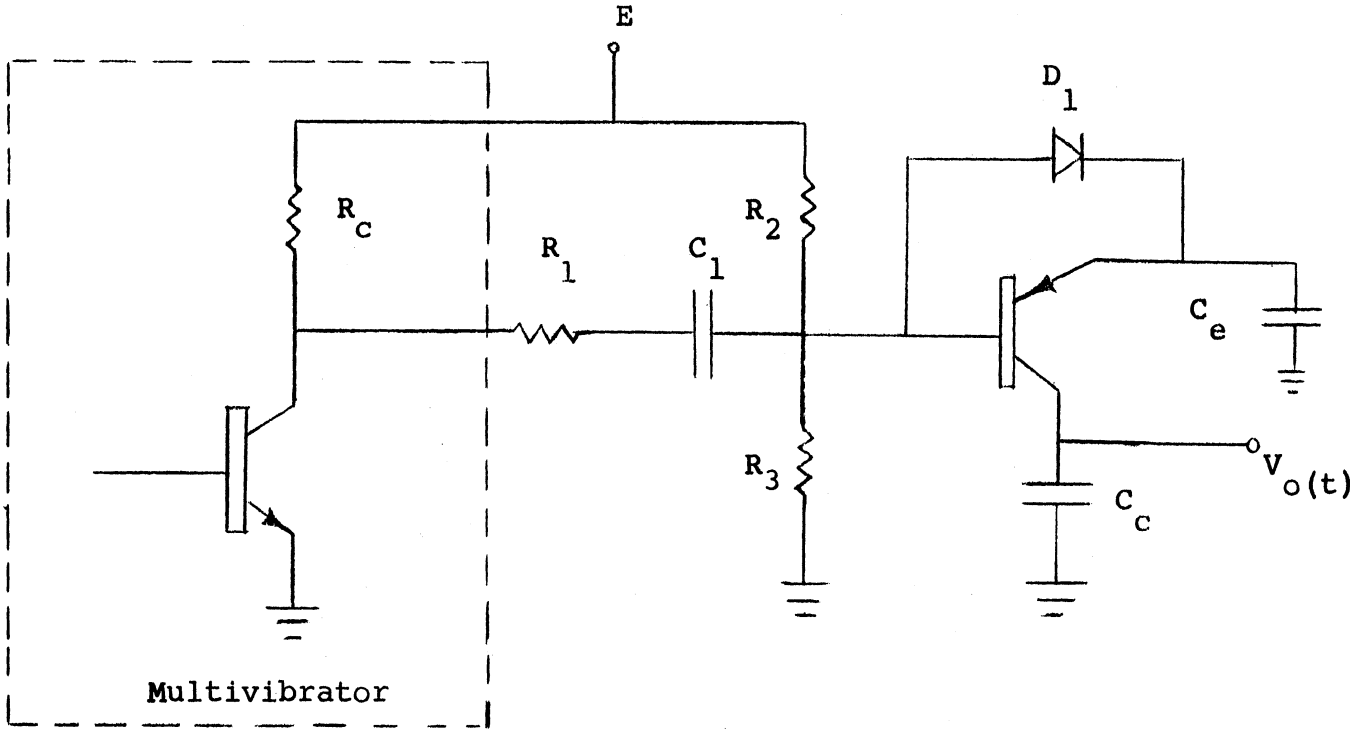


Fig. 20. Complete Q-Transporter Trigger Circuit.

maximum. Moreover, in addition to the high efficiency attained thereby, the sharp cutoff mechanism would exclude operation in the region of low junction voltages, where the temperature-dependence of the exponential term in Eq. (20) is significant.

However, to be effective in controlling the duration of charge transfer period, it is obvious that C_1 can exert critical influence over the step size, especially with variations in its nominal capacitance with temperature. Hence

it is advantageous to include in the circuit provision for a temperature compensation mechanism. In addition to the choice of temperature coefficient for C_1, additional flexibility can be achieved by the use of a temperature-sensitive resistor (thermistor or sensistor) for R_1. This resistance would also serve to limit the peak trigger current (through the multivibrator collector circuit) below the rated maximum of 20 ma. Note in Fig. 20 that between pulses C_1 will charge through R_c, R_1, and R_3 to:

$$V_{C_1} = E - V_b = \frac{R_2}{R_2 + R_3} E \qquad (23)$$

Thus, when the multivibrator switch saturates, the instantaneous maximum charging voltage will be:

$$V_b + V_{C_1} = E \qquad (24)$$

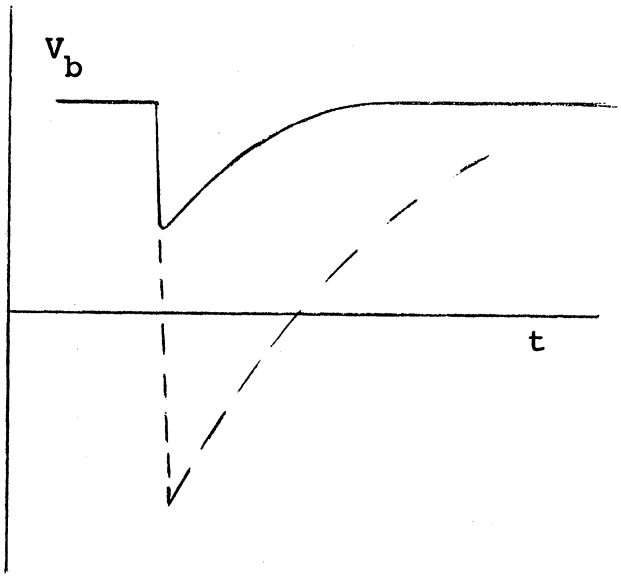
Hence the minimum value of R_1 required to limit I_c (max) to 20 ma is:

$$R_1 = \frac{E}{0.02} - R_{SAT} - \frac{R_2 R_3}{R_2 + R_3} \qquad (25)$$

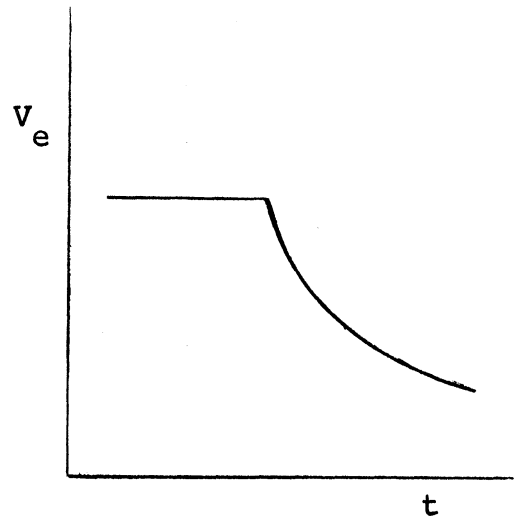
which is typically 1.5 kilohms.

Figure 21(a) shows the effect of a trigger pulse at time t_o on the base waveform. Since the voltage across C_1 cannot change instantaneously, the base voltage starts to drop toward minus V_{C_1} in a time determined principally by the transistor fall time. But even as the voltage falls, C_1 begins to charge through the rapidly diminishing multivibrator output impedance. The minimum base voltage attained is shown in Fig. 21(a) as about 4.5 volts below V_b, the steady-state value. This change takes place in, typically, 10 μsec. The base voltage then begins to rise according to the base time constant:

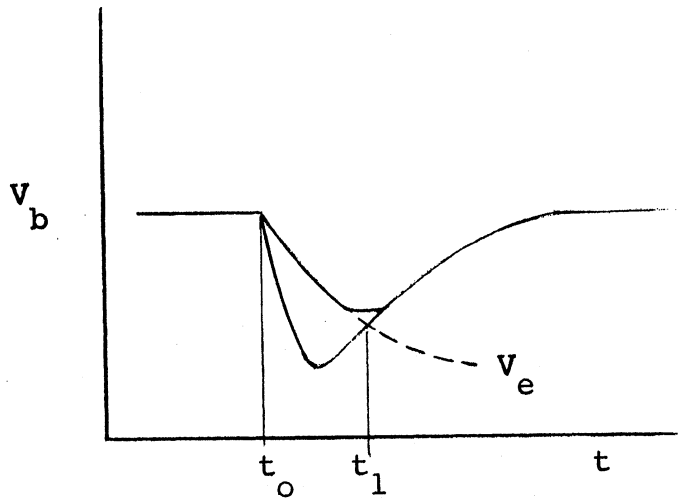
$$\tau_b = \left(R_1 + R_{SAT} + \frac{R_2 R_3}{R_2 + R_3}\right) C_1 \simeq 30 \text{ μsec.} \qquad (26)$$



(a) Base Voltage Response to Negative Trigger Pulse

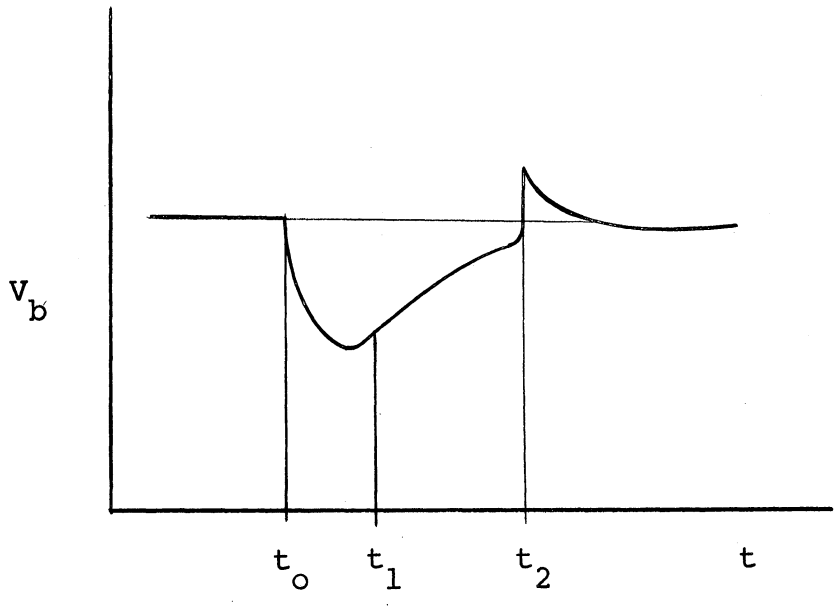


(b) Discharge of Emitter Capacitor Following Trigger Pulse

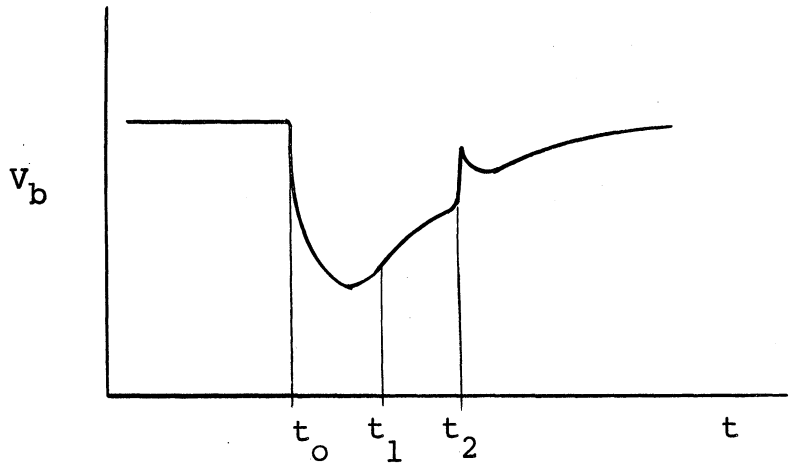


(c) Combined Response.

Fig. 21. Q-Transporter Base Waveforms.



(d) Overshoot Exceeding Quiescent Value.



(e) Overshoot Used to Accelerate Recovery, Without Exceeding Quiescent Value.

Fig. 21 (Concluded)

toward V_b. As soon as the base voltage has dropped more than 0.4 volts, the emitter-base junction of the Q-Transporter stage begins to conduct, and the emitter voltage, V_e, decays with time constant:

$$\tau_e = \frac{C_e C_c}{C_e + C_c} R_{CE} \simeq 50 \ \mu\text{sec}. \qquad (27)$$

as shown in Fig. 21(b). The emitter decay continues until the base and emitter voltages converge to within the 0.4 volt junction threshold, at which point, t_1, the Q-Transporter is abruptly reverse-biased and collector current ceases. Sketches of these two voltages are shown superimposed in Fig. 21(c) to exhibit the sharp cutoff mechanism. Once the transistor has been cut off, diode D_1 is forward-biased and C_e begins to charge, in parallel with C_1, toward V_b. At some point, t_2, along the exponential rise, the multivibrator reverts to its initial open circuit impedance of R_{MV}. If the switching were instantaneous, the base voltage would immediately overshoot to $(1 + \frac{2R_3}{R_2 + R_3})$ E, causing no change in the state of the Q-Transporter stage but altering the voltage to which C_e is charged, as shown in Fig. 21(d). The amplitude of the overshoot is a function of the magnitude of C_1 and hence is temperature-dependent. Furthermore, the variation with temperature is such as to augment rather than mitigate other thermal variations. It is evident that any direct measures taken to suppress this overshoot would also desensitize the circuit to the trigger pulse. However, if the "ON" time of the multivibrator is adjusted so that the overshoot occurs while the base voltage is low enough so that the increase is still less than V_b, the overshoot will actually accelerate the recharging of C_e. Figure 21(e) shows the base waveform with the multivibrator "ON" time so adjusted. The multivibrator frequency and asymmetry are determined once the step length and "ON" time are specified. The emitter circuit time constant, τ_e, must be much less than the "OFF" time to avoid dependence of step size on multivibrator frequency and to justify the assumption of steady-state conditions prior to the trigger pulse at t_o.

In addition to establishing the emitter-circuit charging time constant, R_2 and R_3 in series form a voltage divider that sets the quiescent base voltage, V_b, and the steady-state d-c level of C_e. Clearly this level must exceed the maximum voltage to be accumulated on C_c, the output capacitor. The maximum output voltage, in turn, is determined by the properties of the voltage-operated reset switch used to discharge C_c at the end of each sweep, as well as the magnitude of the supply voltage, E. The maximum voltage swing is determined in Part D of this section to be approximately 17 volts. Thus V_b must exceed this value. While it is advantageous to make both R_2 and R_3 small to reduce the recharging time of C_e, this increases the d-c power loss through the series combination to ground. Hence a trade-off is required between power loss on the one hand and charging time on the other. If the recharging of C_e could be completed in 7 ms after the trigger pulse, an 8-ms step length would allow a 12.5% margin of safety against decreases in multivibrator period. Since such changes are associated with increases in supply (battery) voltage, the margin appears ample. Thus, once the value of C_e is determined, R_2 and R_3 can be calculated.

The selection of C_e is related to the choice of C_c through the temperature-compensation aspect of Eq. (10), while C_c is determined in Section V from a consideration of step droop. The value of C_1 is based on considerations discussed on pages 33 and 34, where it was shown that it is the principal variable in τ_b. For a sharp cutoff characteristic, the base and emitter time constant, τ_e and τ_b, should be comparable. If there is an appreciable difference between them, the slope of the longer will approach zero, so that the shorter time constant will be the sole determinant of cutoff. The degree of freedom that does exist,

allows considerable flexibility in the choice of C_1 on the basis of physical dimensions, step size, and temperature coefficient. Of these, the temperature coefficient is by far the most important consideration, since it permits compensating for the appreciable variation in the voltage drops across D_1 and the emitter-base junction with temperature. The multivibrator collector-supply voltage can then be used as a fine adjustment of the step size.

For convenience, a summary of the dependence of the various parameters of this section is given below as Table I; Table II lists typical component values. Details of the step-generation process, depicted graphically in Fig. 21, are given explicitly in Table III and illustrated by means of the oscillograms of Fig. 22, where the sharp cutoff can be seen. The point at which the multivibrator reverts to the high impedance position (t_2) is visible as a change in the slope of the recharging portion of Fig. 22(c). The partially discharged emitter capacitor, C_{e_1} exhibits such a low impedance at this time that it suppresses the overshot that would otherwise occur. The duration of the charge-transfer period, the sharp cutoff mechanism, and confirmation of steady-state conditions prior to triggering at t_o, are all apparent in Fig. 22(d). Figure 23 displays the stairstep output voltage obtained from the Q-Transporter circuit.

TABLE I

SUMMARY OF Q-TRANSPORTER AND TRIGGER STAGE DESIGN CONSIDERATIONS

(1) Maximum rated multivibrator collector current determines the minimum value of R_1.

(2) Maximum acceptable step droop as well as physical size and temperature coefficient determine value and type of the capacitor used for C_c.

(3) Necessity of matching temperature coefficients suggests making C_e identical to C_c, while pressure to reduce recharging time requires use of a smaller value.

(4) The product of voltage-operated reset switch intrinsic standoff ratio and the supply voltage magnitude (ηE) determines the minimum quiescent base voltage $\left(\frac{R_3}{R_2 + R_3} E\right)$.

(5) Minimum power loss in R_2 and R_3 on the one hand and minimum recharging time for C_e on the other serve with no. 4 to define $R_2 + R_3$.

(6) Desired step size as well as system-temperature coefficient determine choice of C_1 (coarse) and R_1 (fine).

TABLE II

Q-TRANSPORTER AND TRIGGER CIRCUIT COMPONENT VALUES

R_1	R_2	R_3	R_c	C_1	C_e	C_c
1.2 K	1.8 K	6.8 K	10 k	.022 μfd	1.0 μfd	5.6 μfd

TABLE III

Q-TRANSPORTER STEP-GENERATION SEQUENCE
(To be used in conjunction with Figs. 21 and 22)

Time (μs)	Condition	R_{MV}	Base-Emitter Junction	R_{CE}	I_C	V_D	Note
0^-	quiescent	high	cutoff	high	0	nonconducting	
0-15	MV "ON"	falling	conducting	falling	rising	cutoff	
15	"	min	saturated	min	max	"	
15-60	"	"	"	"	"	"	
60	CUTOFF	"	cutoff	high	0	saturated	A
800	MV "OFF"	rising	"	"	0	conducting	B
6000	quiescent	high	"	"	0	cutoff	C
8000			CYCLE REPEATS				

Note A: Q-Transporter stage cuts off. C_1 and C_2 begin recharging in parallel.

Note B: Multivibrator changes state, causing overshoot in base voltage. Nonlinear resistance of diode increases, slowing charging of C_e.

Note C: Charging of C_e completed.

(a) Emitter Response
(2 ms/cm)

(b) Base Response
(2 ms/cm)

(c) Expanded View of Base Response
(1 ms/cm)

(d) Charge Transfer Portion of Base Response
(200 μs/cm)

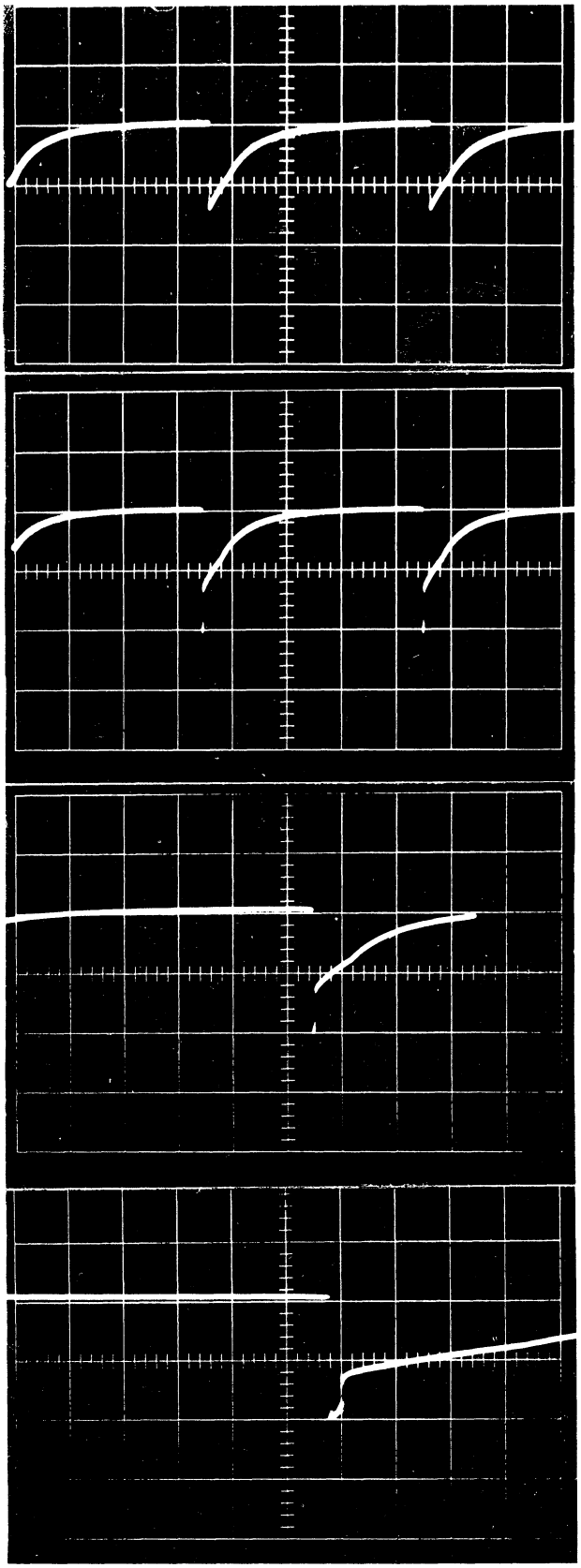
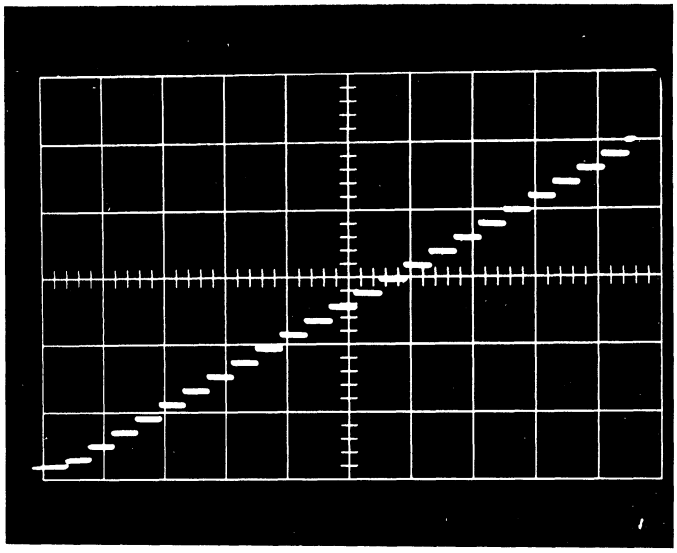
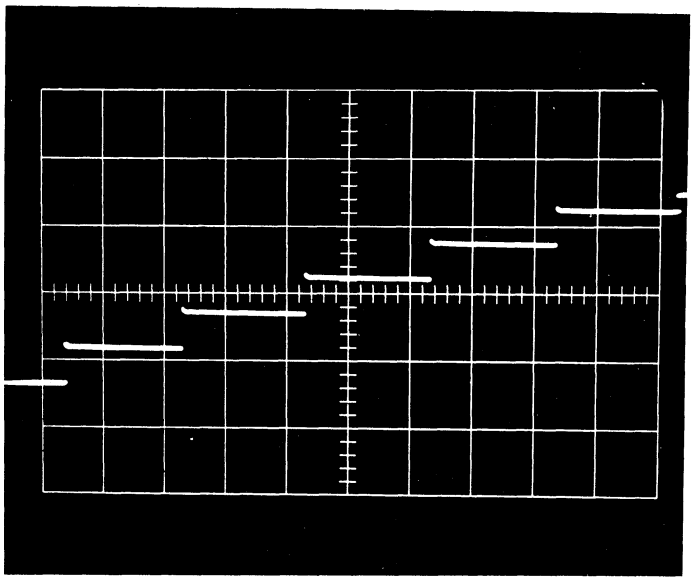


Fig. 22. Q-Transporter Response to Trigger Pulse.
(All vertical scales 2 volts per centimeter)



(a) Stairstep Output Waveform



(b) Expanded View of Output Waveform

Fig. 23. Q-Transporter Output Waveform.

C. MULTIVIBRATOR DRIVER CIRCUIT

The switching times required for efficient step generation with independence of supply voltage variations have been specified in Part B of this section with the aid of Fig. 21. The following is a discussion of the properties of an astable solid-state multivibrator to meet the requirements for the "Timer."

As previously mentioned, it is desirable to use the multivibrator frequency as a means of independent control over the step length and hence the repetition frequency of the stairstep output waveform. The most convenient means of exerting frequency control without affecting the degree of asymmetry is by varying the collector supply voltage. On that basis, a multivibrator of 9:1 asymmetry and base frequency of 70 cps at a nominal collector voltage of 13 vdc was designed using conventional methods.[3] Figures 24 and 25 show the circuit configuration and output waveform, respectively, of this multivibrator.

The temperature variation of the circuit, exclusive of capacitors, was then evaluated by placing the entire circuit, except for the capacitors, in an environmental oven. The resulting variation in the output frequency of the circuit is shown in Fig. 26. The variation is due principally to the temperature dependence of I_{CO} and V_{be} of both transistors. This variation was then matched by capacitors of opposite coefficients, while the resistors were adjusted for the desired base frequency and asymmetry. Table IV lists the component values used, and Fig. 27 shows the compensated temperature variation over a wide range of collector voltages.

TABLE IV

MULTIVIBRATOR COMPONENT VALUES

$R_{1,4}$	R_2	R_3	C_1	C_2	$Q_{1,2}$
10 K	100 K	82 K	.68 μfd	.022 μfd	2N338

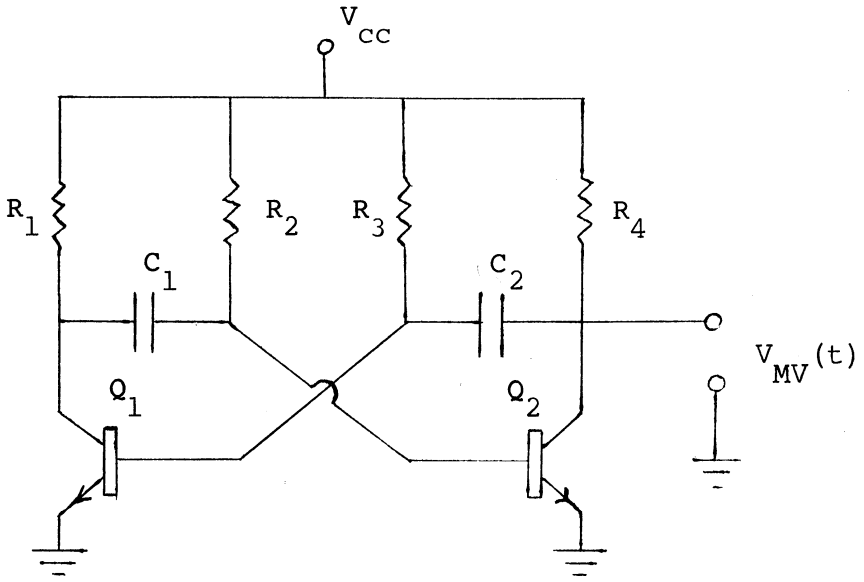


Figure 24: Multivibrator Circuit.

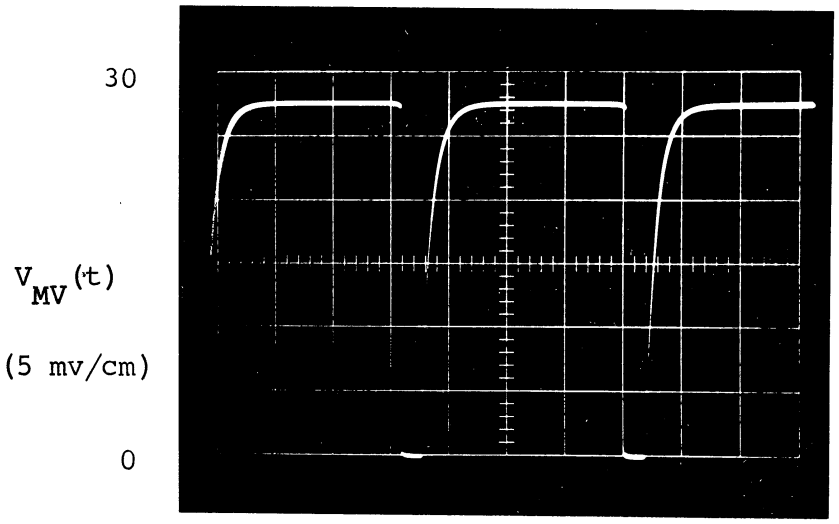


Fig. 25. Multivibrator Output Waveform

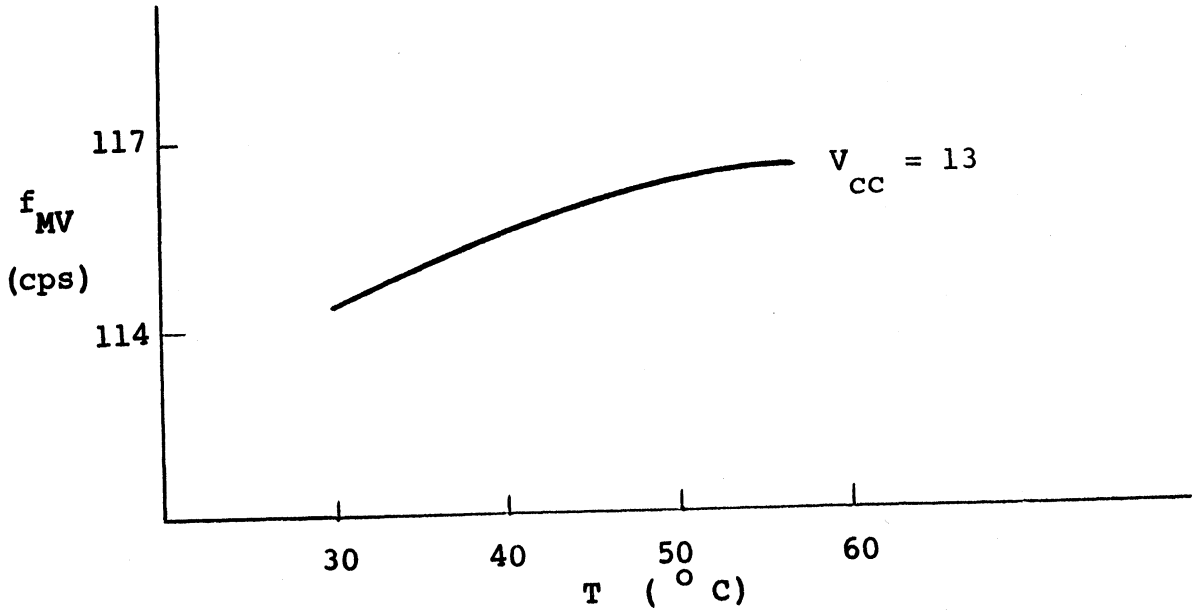


Fig. 26. Multivibrator Temperature Characteristic.

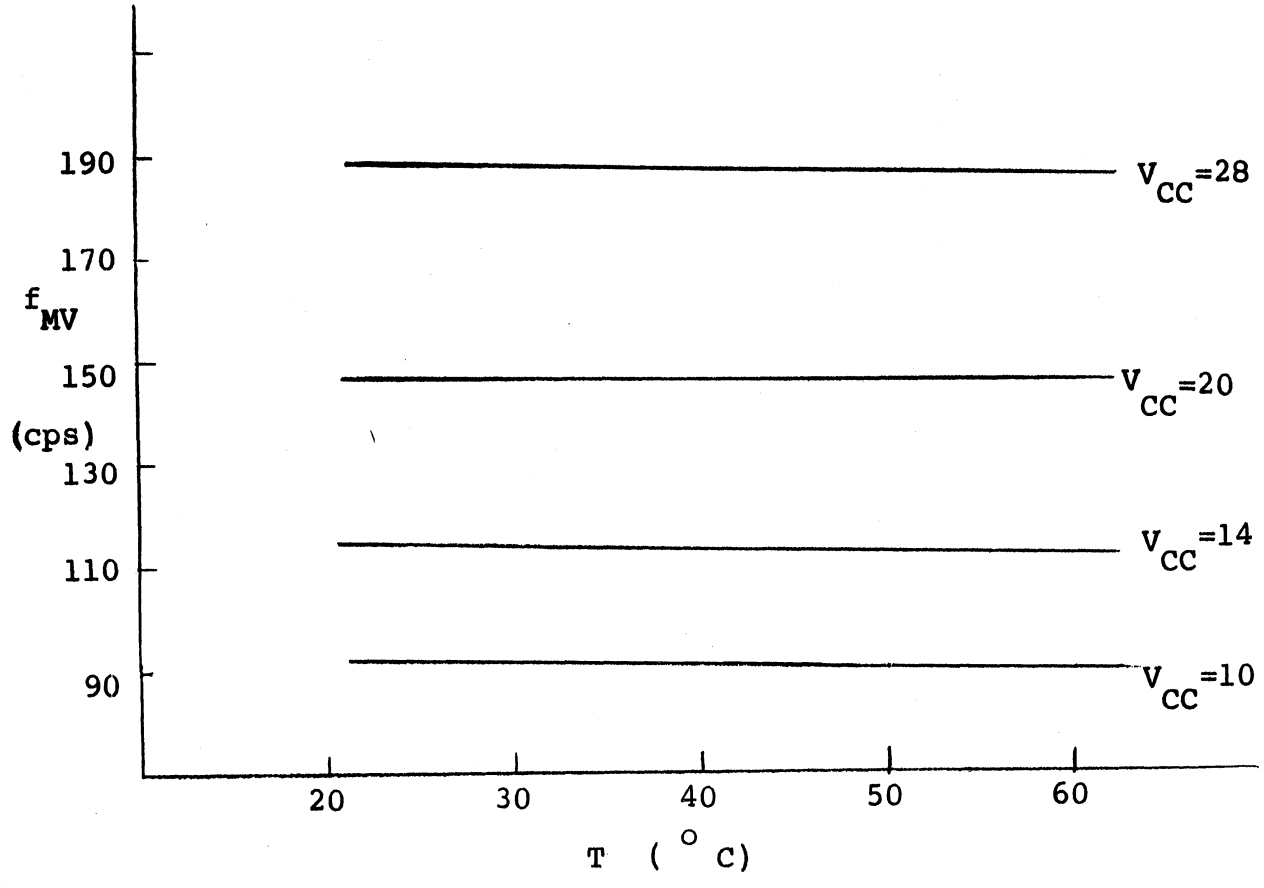


Fig. 27. Temperature Compensated Multivibrator Characteristic.

D. VOLTAGE-OPERATED RESET SWITCH

Throughout the preceding, it has been tacitly assumed that a means of rapidly removing the charge accumulated on the output capacitor, C_c, was available. Indeed, blocking oscillator and gas thyrathron circuits are quite commonly employed as voltage-operated switches. A solid-state equivalent of the thyratron is the Unijunction Transistor (formerly called the Double-Based Diode).[4,5] It is small and has a high discharge-current capability.

The applicable schematic and equivalent circuits for this device are shown in Figs. 28(a) and (b), respectively. The internal ohmic path (≃7K)

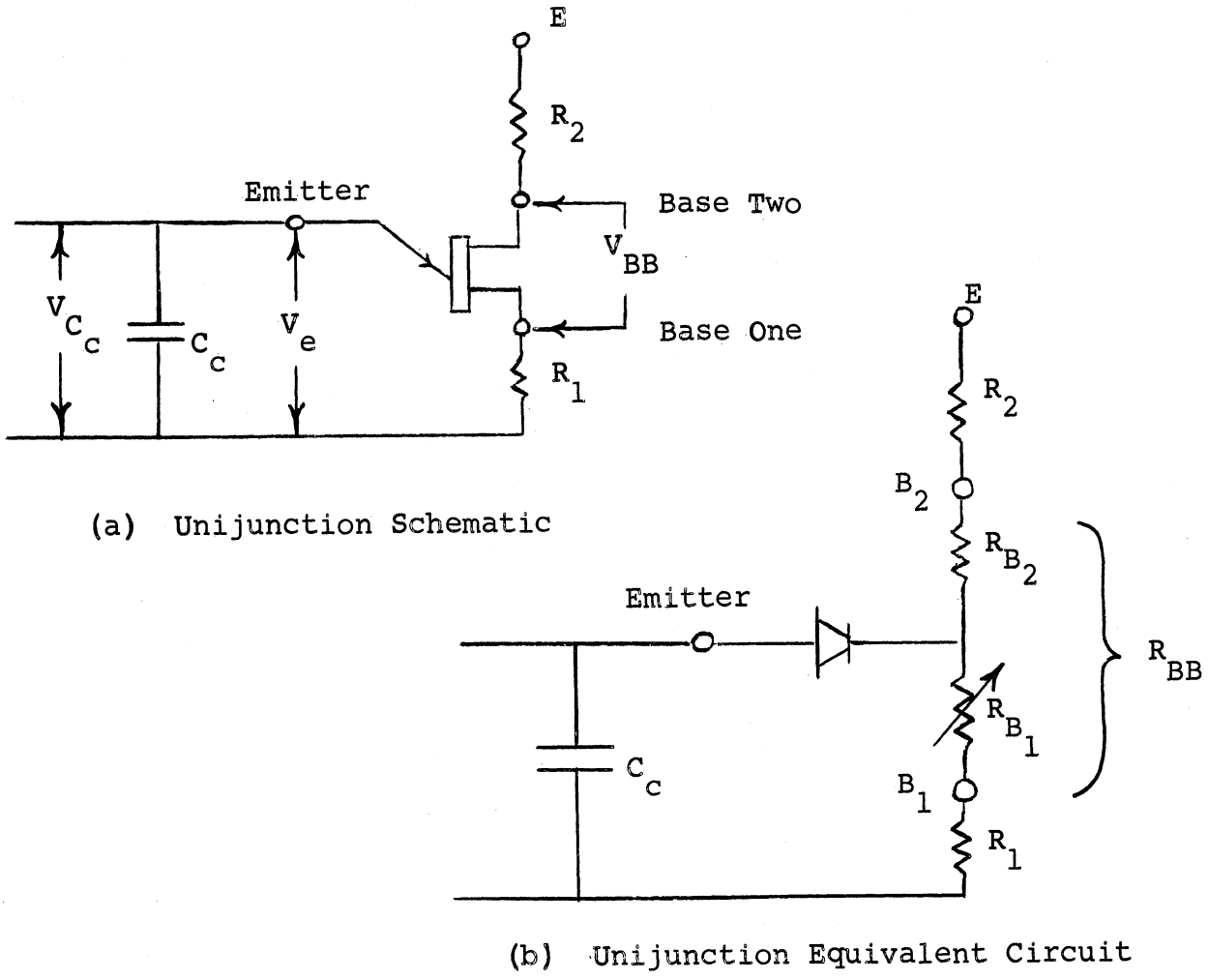


Fig. 28. Unijunction Transistor Schematic and Equivalent Circuits.

between the base-two and base-one terminals draws a steady-state direct current from the voltage source E, and establishes an open circuit voltage of

$$\eta V_{BB} = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} V_{BB} = \frac{R_{B_1}}{R_{BB}} V_{BB} \qquad \text{for } R_1 = 0 \qquad (28)$$

across the emitter and base-one terminals (input) by ordinary voltage divider action. For inputs less than V_{BB}, the PN emitter junction is reverse-biased and exhibits the high impedance characteristic of such diodes. If the externally applied voltage, V_{C_c}, is raised, the point will be reached where the emitter junction becomes forward-biased and current begins to flow from the emitter to base-one. Further increases in applied voltage will not raise the emitter voltage, V_e; on the contrary, V_e actually decreases. The emitter current, I_e, however, increases because R_{B_1} exhibits a negative resistance characteristic above a peak forward-current value, I_p. The forward-biased input characteristic of this device is stable until a critical value of emitter current greater than I_p is reached. Avalanche multiplication of base-one carriers then occurs, decreasing R_{B_1} according to Fig. 29.

Currently available commercial units are rated to pass peak discharge currents of 2 amperes. Figure 30 depicts the discharge time as a function of emitter capacitance. For C_c greater than 1.0 μfd, the exponential discharge exhibits an equivalent emitter-to-base-one series resistance of about four ohms, and typically takes approximately 200 μsec. This is about 3% of a typical step length.

The most seriously undesirable feature of this device is the variation of its input impedance (emitter to base-one) in the vicinity of the firing

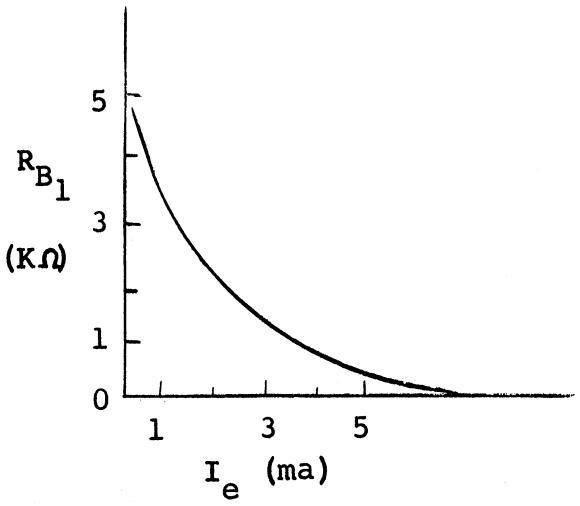


Fig. 29. Variation of Unijunction Base-One Resistance with Emitter Current.

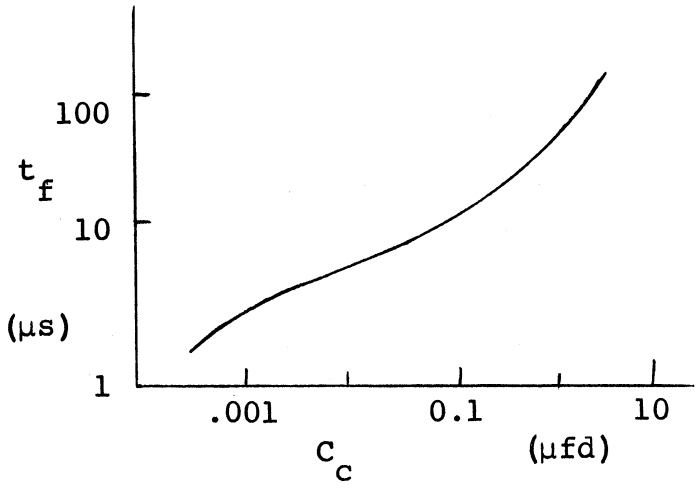


Fig. 30. Discharge Time versus Emitter Circuit Capacitance.

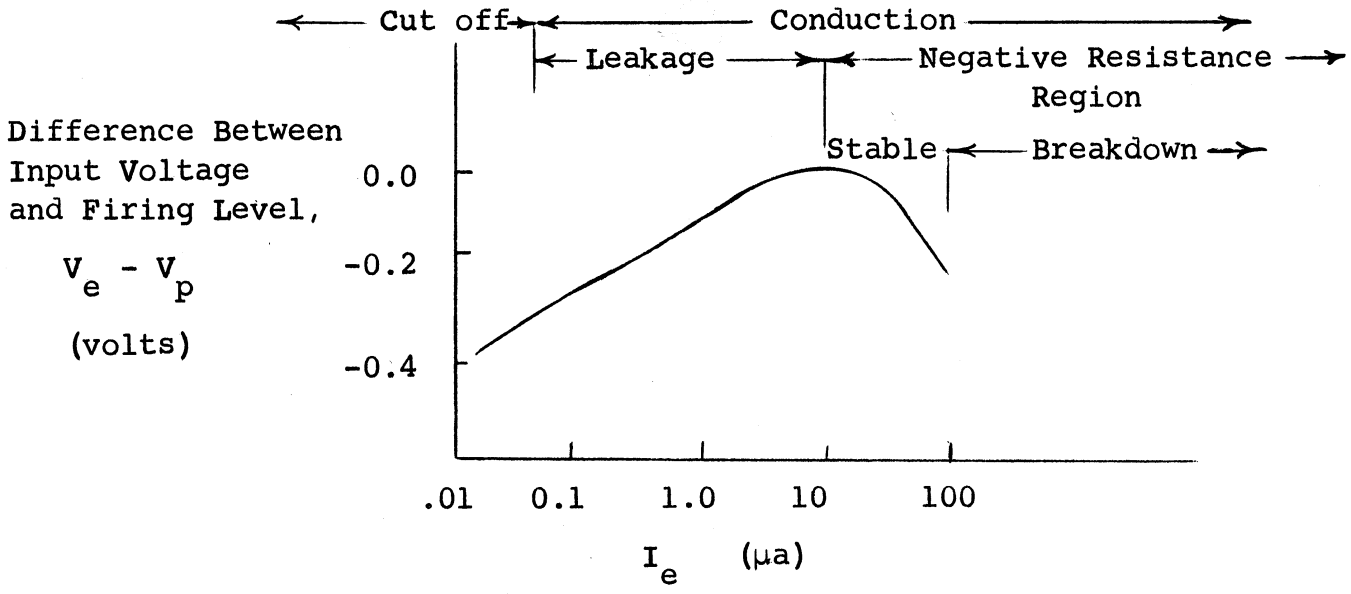


Fig. 31. Typical Unijunction Input Characteristic Near Peak Point.

point, V_p, as depicted in Fig. 31. The current multiplication mechanism by which the rapid discharge takes place is actually a current-operated phenomenon rather than the voltage-controlled mechanism suggested above. Of course this is really just another aspect of the same thing, but the current-biased description is more revealing in this instance—as it is for solid-state devices in general. Initiation of the current multiplication process requires an emitter current of from 2 to 100 μa, depending on the value of the interbase voltage, V_{BB}. Even for fixed values of interbase voltage, the emitter current required for avalanche breakdown exhibits considerable statistical deviation among specific Unijunctions. Thus the input terminals could draw up to 100 μa from the input capacitor C_c without initiating breakdown. For a 5.6-μfd input capacitor and an 8.0-ms step length, this results in a 1% droop on the last step before reset occurs. Previous steps would suffer proportionally less droop according to Fig. 31.

Two distinct methods of mitigating this effect are available. One is to increase the step size so that the knee of the input resistance curve, Fig. 31, is traversed in a single step. The second is to apply an external triggering signal either to raise V_e or to lower V_p by lowering V_{BB}, thereby inducing premature firing.

The first approach requires considerable modification of previous circuits. For a fixed number of steps an increase in step size increases the output swing and hence requires the addition of an output attenuator to realize the required levels. It will be shown subsequently that increasing the step size is desirable to facilitate establishing an unambiguous reference when the output voltage passes through zero. In the next section it will be shown that the principal

limitations in step size are the available supply voltages and the maximum reliable collector breakdown voltage ratings of the transistors. Therefore it is advantageous to consider the method of controlled breakdown by the application of a trigger pulse to one of the Unijunction terminals. Base-two is the terminal best suited to this role; any circuitry attached to the emitter would be additional loading on the output capacitor and would itself contribute to the droop, while application of a trigger signal to base-one would require the addition of a series impedance in that circuit which would increase the discharge time. It can be seen from the equation relating the firing voltage V_p to the interbase voltage V_{BB}:

$$V_p = V_d + \eta V_{BB} \tag{29}$$

(where V_d is the diode drop) that a reduction in V_{BB} by a factor ϵ would reduce V_p and cause the emitter to fire if V_e ($=V_c$) exceeded $V_d + \eta\ (V_{BB} - \epsilon)$. Due to the storage effects at the junction, the duration of the triggering pulse must exceed 0.6 μsec for pulse amplitudes of about two volts. This signal could be obtained from a separate timing source (multivibrator or sawtooth oscillator), but a more reliable solution is to derive the trigger from existing waveforms. Since ϵ is to be negative, it could be obtained from the collector waveform of the multivibrator that triggers the Q-Transporter stage as in Fig. 32. The latter introduces a 180° phase shift that causes a positive signal (the step) of about one-half volt to appear at the emitter terminal of the Unijunction. This, combined with a simultaneously applied two-volt negative trigger signal capacitively coupled to the base-two terminal, would quickly traverse the knee of the firing curve (Fig. 31).

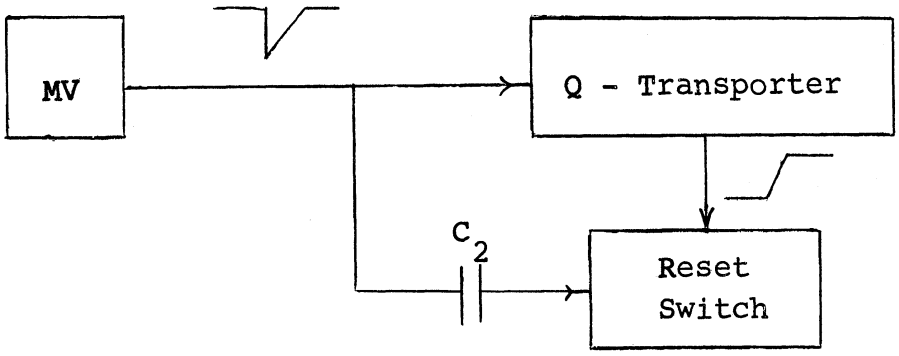


Fig. 32. Block Diagram of Unijunction Triggering Method.

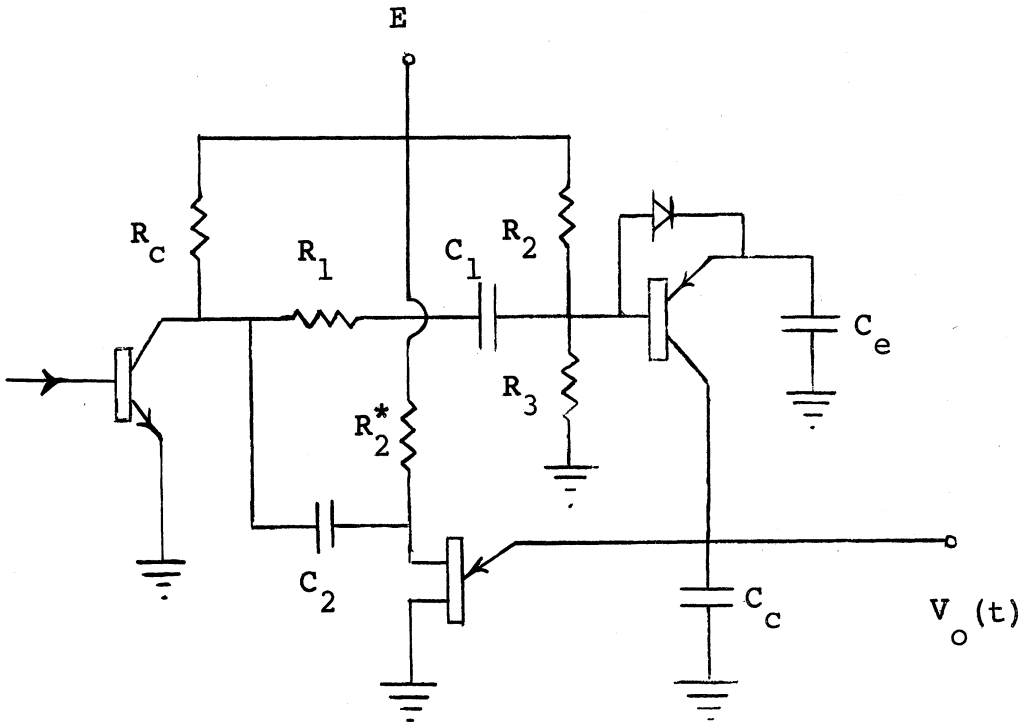


Fig. 33. Unijunction Triggering Circuit.

*R_2 of this Section is so designated to permit ready reference to the literature.[4,5]

Figure 33 shows the circuit implementation of these concepts. The base-two series resistance would exist regardless of triggering requirements for temperature-compensation purposes. Thus C_2 is the only additional component required. Its value can be calculated from knowledge of the minimum necessary pulse duration. When the output voltage of the multivibrator is maximum,

$$V_{C_2} = V_{BB} - V_{MV} = E\left(1 - \frac{R_2}{R_{BB}}\right) - V_{MV} \simeq E - V_{MV} \qquad (30)$$

Immediately after the multivibrator changes state,

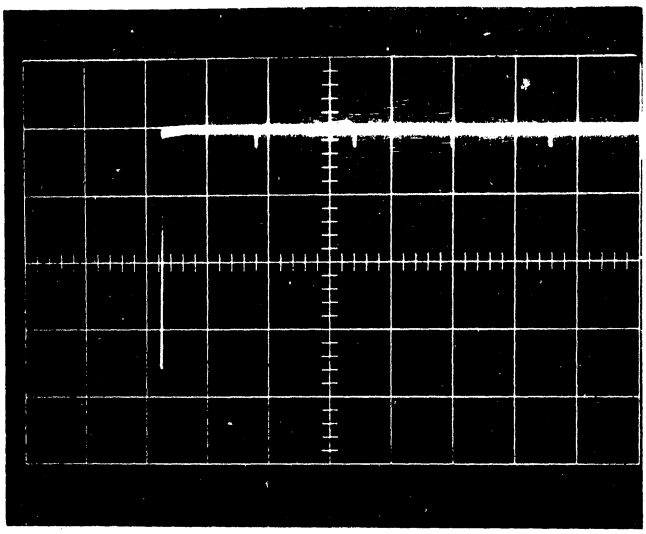
$$V_{BB} = V_{C_2} + (E - V_{C_2}) \exp\left[-\frac{t}{R_2 C_2}\right] \qquad (31)$$

For a pulse width of at least 1 μsec, $R_2C_2 \simeq 1 \times 10^{-6}$; and C_2 will be 0.003 μfd when R_2 is shown to be 330 ohms in Eq. (32). The finite value of multivibrator switching time, with the above value of C_2, prevents V_{BB} from being instantaneously shorted to ground and the Unijunction thus firing at every multivibrator pulse. V_{BB} actually drops only about two volts, or four step heights, which is sufficient virtually to eliminate the Unijunction's contribution to droop.

Figure 34 is a photograph of the actual interbase voltage, V_{BB}. The large 17-volt spike occurs during the discharge of C_c, at the end of a sweep. The smaller 1.5-volt spikes are the capacitor-coupled trigger pulses from the multivibrator. It can be seen that they occur exactly one step length apart. An expanded view of the discharge spike is shown in Fig. 35. The discharge time is seen to be slightly over 200 μsec. Even on this fast trace, the slope of the leading edge of the discharge spike appears infinite.

V_{BB}

(5 v/cm)

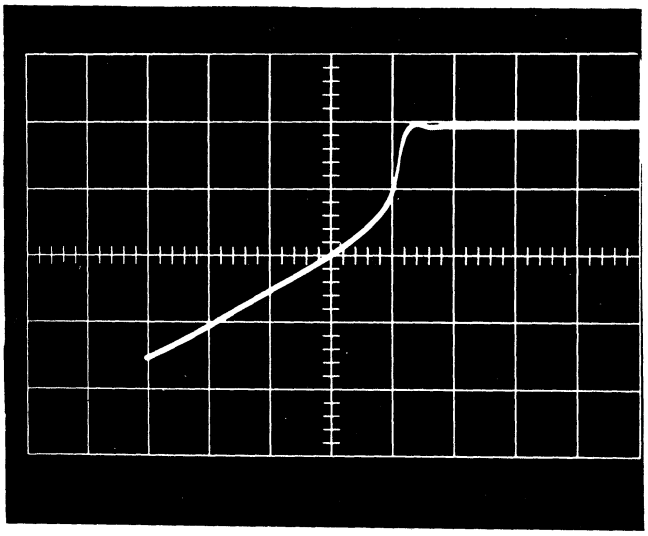


t (5 ms/cm)

Fig. 34. Oscillogram of Unijunction Interbase Voltage, V_{BB}.

V_{BB}

(5 v/cm)



t (50 μs/cm)

Fig. 35. Oscillogram of Unijunction Discharge Spike in Interbase Voltage.

The fact that these trigger pulses are applied to base-two of the Unijunction each time the multivibrator changes state, or n - 1 times as often as necessary, is an inconsequential feature of this arrangement. The additional power is only 2.5 μw and the additional discharge current through the multivibrator averages 3.3 μa while the finite switching time likewise limits the peak discharge current to much less than the maximum transistor rating of 20 ma. The switching time is so predominant in determining the magnitude of the trigger pulse that a temperature variation of ± 100% can be tolerated for the trigger capacitor.

Much more critical, however, is the temperature variation of the firing point [Eq. (38)] of the Unijunction. From the equivalent circuit of Fig. 28(b), it is evident that η will be independent of temperature since R_{B_1} and R_{B_2} are formed by a tap on the same homogeneous material (a bar of silicon) and hence have the same temperature dependence. The variation of the junction diode voltage, V_d, moreover, can be compensated for by modification of the inter-base voltage (V_{BB}) in Eq. (38) by the addition of resistance in either the base-one or base-two leads or both. The resistance is chosen so that the voltage divider ratio forming V_{BB} exhibits the precise fraction of the temperature dependence of R_{BB} necessary to compensate for the coefficient of V_d. The manufacturer's empirically derived formula:

$$R_2 \simeq \frac{0.70\ R_{BB}}{E} + \frac{1 - \eta}{\eta} R_1 \qquad (32)$$

determines R_2 to be 330 ohms for $R_1 = 0$ in Fig. 28(a). The firing point stability under these conditions approaches the manufacturer's claim of 0.001 %/°C.

E. OUTPUT AMPLIFIER

The reader will recall from Fig. 1 that the stairstep voltage output of the δV generator is to be applied across the series combination of the current detector and the hemispherical collectors to measure the "plasma resistance," R_p. Given the known voltage steps and measuring the current at each level, the Ohm's Law calculation for R_p will include the series resistances of both the δV generator and the current detector as well as R_p. In practice, R_p ranges from several megohms in the ion saturation region to several hundreds of kilohms at the lower applied voltages, whereas the series resistance of the current detector is about 10 kilohms.[6] Correction is made for the voltage drop across this resistance in reducing the flight data. It is desired that the δV series resistance be as low as possible so that, in the event of any variation during flight, the change in correction factor will be negligible. Thus an amplifier of nearly perfect linearity, wide dynamic range, and low output impedance is required. Moreover, the amplifier input resistance must be high enough so that the current drawn from the output capacitor, C_c, during the long data-collection intervals between pulses, causes only negligible step droop.

An amplifier configuration that satisfies the above requirements is the emitter-follower circuit. The equivalent circuit representation of Fig. 36 can be solved for the input and output resistances to yield the results given in Eqs. (33) and (34), respectively.

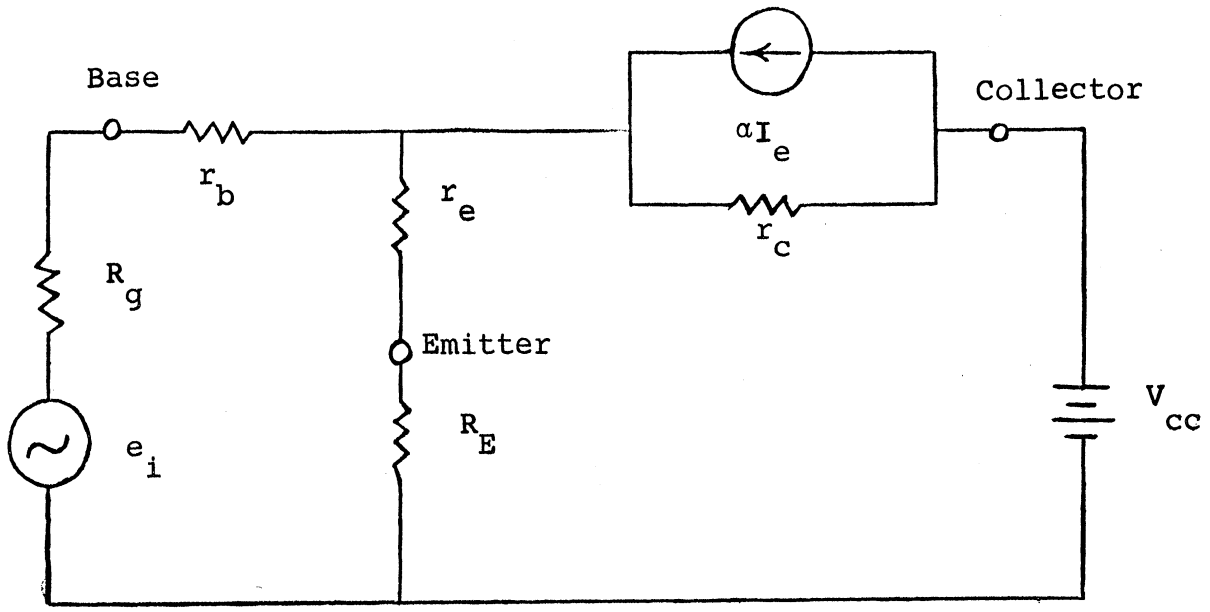


Fig. 36. Emitter Follower Equivalent Circuit.

$$R_i = r_b + r_c \frac{r_e + R_E}{(1-\alpha) r_c + r_e + R_E} \tag{33}$$

and

$$R_o = r_e + r_c (1-\alpha) \frac{R_g + r_b}{R_g + r_b + r_c} \tag{34}$$

It is clear initially that R_i can never exceed $r_b + r_c$ ($\simeq$ 10 megohms) regardless of the value of the emitter resistor while R_o can never be less than $r_e + (1-\alpha)r_b$ [$\simeq$ 63 ohms]. It is advantageous to approach these limiting values, since they represent the minimum loading on C_c and the minimum series resistance, respectively. Therefore, the transistor for the first stage of the amplifier must have high collector resistance as well as high gain and low leakage. A survey of commercially available transistors indicates that the 2N338 silicon grown junction (diffused base) best meets these requirements. For convenience, a summary of its significant parameters is given below as Table V. More complete descriptions of all transistors used are given in Appendix II.

TABLE V

PROPERTIES OF 2N338 TRANSISTOR

α	r_e	r_b	r_c	I_{CO}
0.99	33	3K	10 M	0.002 μa

The impedance transformation ration (Z_{in}/Z_o) attainable with a series of N emitter follower stages each of current gain A is about A^N. For A = 100, N = 3 gives a transformation ratio of 10^6. This figure indicates that the limiting impedances of 10 megohms and 63 ohms given by Eqs. (33) and (34) for the input and output, respectively, can be closely approached by three stages. Considering the three-stage amplifier of Fig. 37, it is of interest to calculate the three emitter resistors and to specify the over-all input and output impedances.

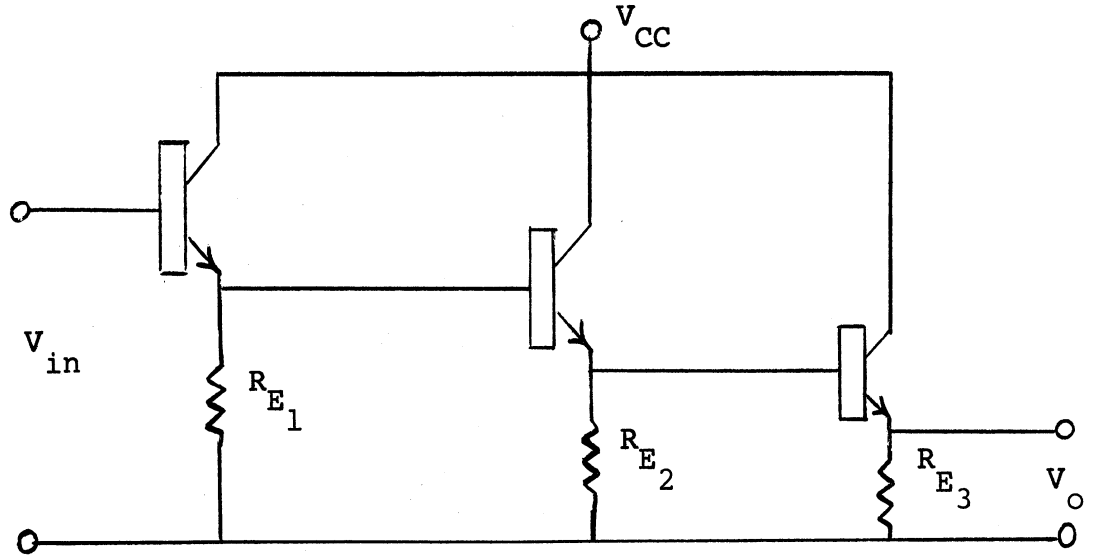


Fig. 37. Emitter Follower Amplifier Circuit.

Since the maximum emitter current for the 2N338 is 20 ma,

$$R_{E_3} = \frac{V_e}{I_e} = \frac{16}{20} K = 800 \text{ ohms, minimum} \quad (35)$$

Twenty milliamperes drawn from the 28-volt supply is over 1/2 watt of power - as

much as will be required to operate the rest of the device. Hence, R_{E_3} should be increased to at least 10 times the minimum value above, or to 8 K, to reduce the power consumption by a factor of ten. But if it is necessary to tap down on the final emitter resistor (R_{E_3}) to obtain a lower amplitude output swing, the voltage divider thus formed will introduce additional series resistance that could be as much as 1/2 R_{E_3}. Setting R_{E_3} equal to 5 K seems to be a reasonable compromise; the output resistance would then be between 63 and 2600 ohms, depending on tap position, while the maximum current drawn from the power supply is 3.2 ma. On this basis the input resistance to the final stage is:

$$R_{i_3} = (10) \frac{5}{50 + 5} M = 910K \qquad (36)$$

An emitter resistance of 100 K would limit the maximum emitter current of the second stage to 160 μa and reduce the effective load resistance of that stage to:

$$\frac{R_{E_2} \cdot R_{i_3}}{R_{E_2} + R_{i_3}} = \frac{100\ (910)}{1010} K = 90K \qquad (37)$$

The input resistance to the second stage would then be:

$$R_{i_2} = (10) \frac{90}{50 + 90} M = 6.43\ M \qquad (38)$$

An emitter resistance of 3.3 megohms would limit the maximum emitter current of the first stage to 6 μa, and reduce the effective load resistance of that stage to:

$$\frac{R_{E_1} \cdot R_{i_2}}{R_{E_1} + R_{i_2}} = \frac{3.3\ (6.4)}{9.7} M = 2.15\ M \qquad (39)$$

The input resistance to the complete three-stage amplifier would then be:

$$R_{i_1} = (10)\frac{2.15}{2.15 + .05} = 9.7 \text{ M} \qquad (40)$$

Therefore the limiting value of 10 megohms is closely attained. From Eq. (34) the minimum stage output impedance, which occurs when the driving source has zero internal impedance, is 63 ohms. This value is approached using a three-stage amplifier even if the source is assumed to have infinite internal impedance. Since three stages of impedance transformation very closely approach the limiting values set by the transistors, adequate circuit performance is assured in spite of relatively large variations in transistor parameters of random origin. Moreover, provision for an accurate zero reference is more readily achieved as a result of the flexibility due to the large range of impedance transformation realizable with this circuit.

The transfer function of the emitter follower circuit, however, involves the nonlinear threshold drop across the forward-biased base-emitter junction. Figure 38 shows this characteristic of current-operated devices. The region of nonlinearity can be avoided by application of a positive d-c bias of at least 2 volts magnitude. [If necessary, this bias could be removed after the emitter

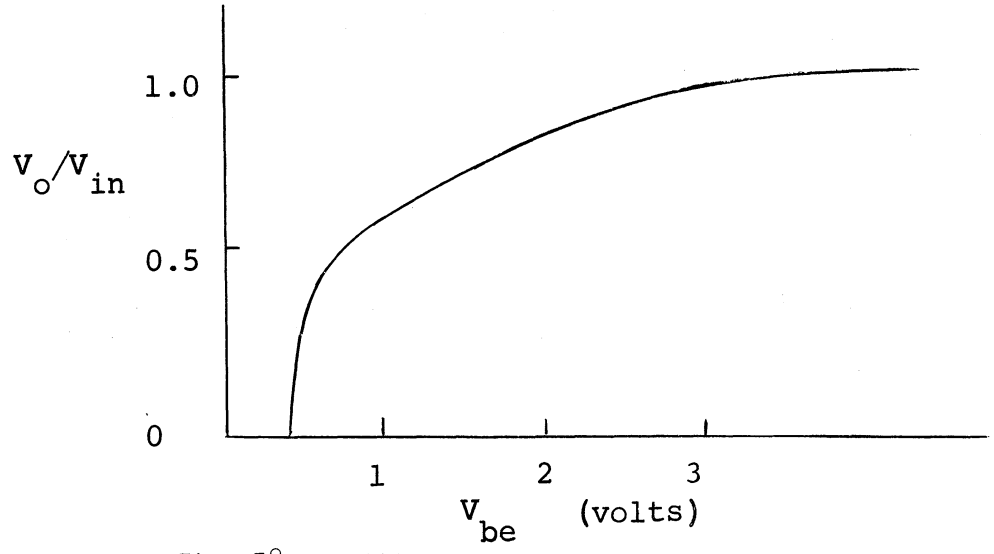


Fig. 38. Emitter Follower Stage Voltage Gain.

follower amplifiers by an appropriate d-c source placed in series with the output terminals.] In the present application, the biasing voltage already exists at the input terminals of the amplifier as a result of the residual (valley) voltage remaining on C_c after the firing of the Unijunction reset switch. This is typically 2.5 volts. Biasing of the output is necessary in either case, however, to provide an output sweep which centered on zero volts.

An additional requirement of the amplifiers is that the collector voltage exceed the maximum voltage swing to be expected to avoid clipping. The requirement that $V_{o_{max.}} = V_{cc} \leq V_{CBO}$ is easily satisfied and allows the collector voltage to be obtained from any convenient point in the circuit. This permanent reverse-biasing of the base-collector junction will result in the flow of leakage current into the capacitor, which tends to replenish the charge lost due to the flow of base current into the amplifier. The effect of this leakage current will be treated in Section V.

F. ZERO REFERENCE

To correct for the particles collected solely as a result of the velocity of the probe through the ionosphere, the current resulting when zero voltage is applied across the probe terminals must be measured. The special significance attached to the measurement at this particular voltage level makes adjustment of the stairstep waveform, so that one step falls precisely at zero, an unreliable solution, since a drift of even a few millivolts would be unacceptable. Recognizing this, present electronic δV's, having a sawtooth output waveform,[6] employ a zero reference circuit consisting of a parallel combination of two reversed diodes in series with one output lead, as in Fig. 39. Ideally, when

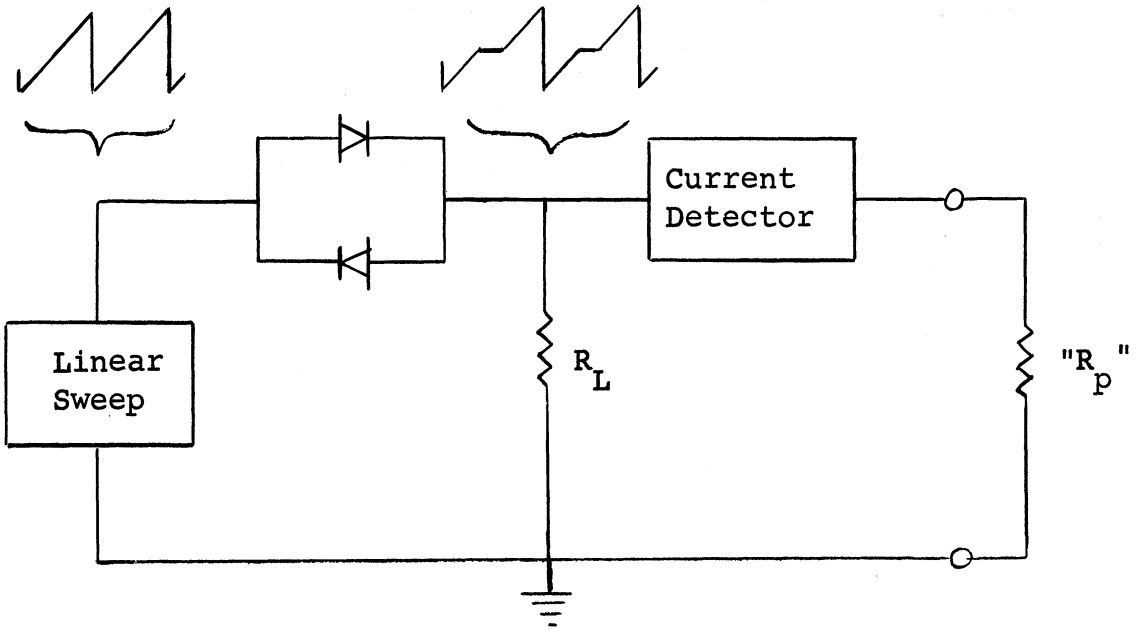


Fig. 39. Diode Zero Reference Circuit.

the driving voltage is less than or equal to the threshold voltages of the diodes, the generator portion of the current through the output resistor R_L is reduced to zero; yet the voltage swing is unaffected beyond the threshold region either side of zero volts. Of little consequence is the finite dynamic resistance of the conducting diodes, as shown in Fig. 40, since it merely

alters the slope of the driving sawtooth waveform.

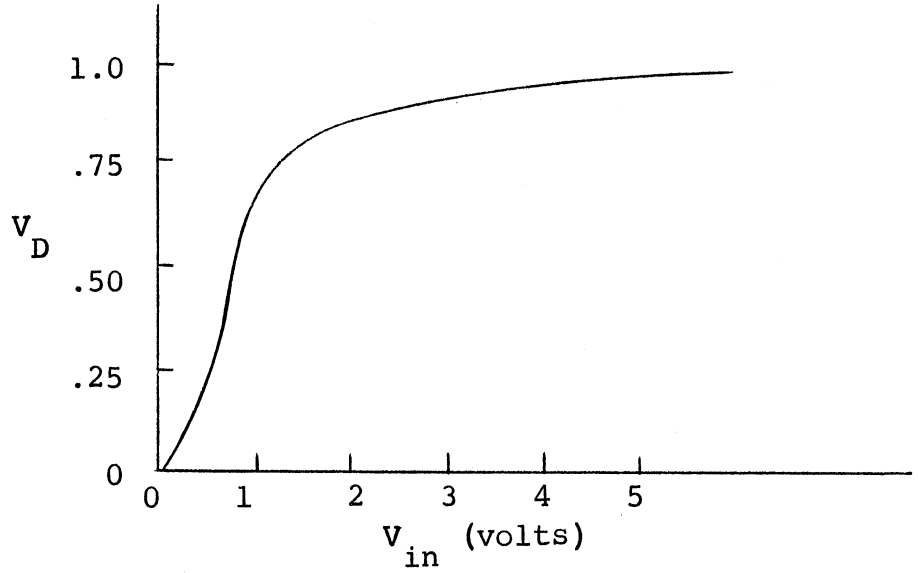


Fig. 40. Silicon Diode Forward Transfer Characteristics.

When the driving voltage is a stairstep waveform, however, the nonconstant voltage drop across each conducting diode superimposes its nonuniformity upon the steps. Consequently, to preserve the uniformity attained thus far, a switching device of more ideal characteristics is required. Switches may be considered to fall into two general categories, active and passive, according to the nature of their activation - diodes clearly belonging to the latter class: moreover, both types of switches can be utilized in two distinct modes, series or parallel (shorting) - the above diodes clearly representing the former use. Figure 41 shows the application of this concept to the circuit under discussion.

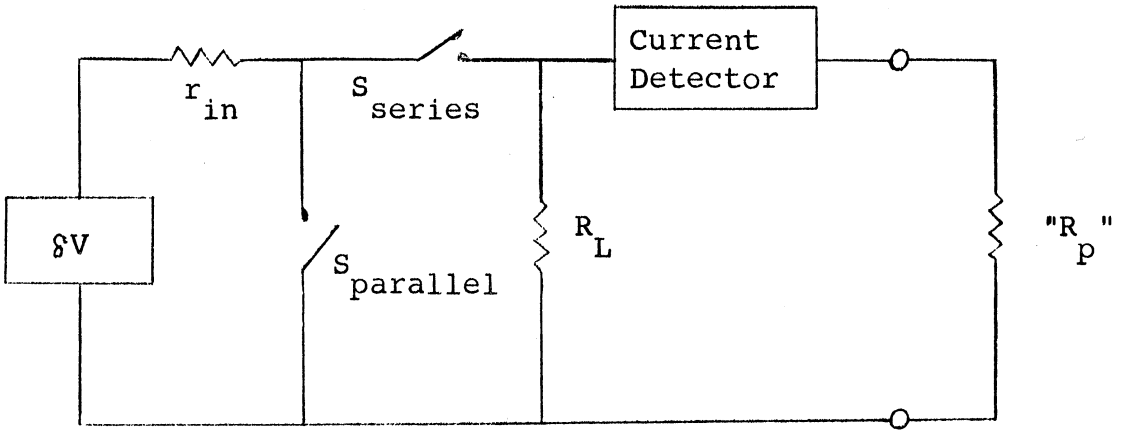


Fig. 41. Generalized Zero Reference Circuit.

A solid-state parallel switch, either active or passive, employed to short the generator terminals at a specified time for a specified duration, would be a device that could be driven from a high impedance state to a low, or saturated, state. As such it will always exhibit some finite resistance (40 ohms for a transistor) and a residual voltage (400 mv, typically) and hence would be even less satisfactory than simply adjusting one of the original steps to be coincident with zero. The diode arrangement above thus represents the only mode of operation (series) capable of meeting the requirements of an acceptable reference. To find a more satisfactory transfer characteristic than that exhibited by the passive diode switch, the above requirements suggest investigation of active series switches. Consequently,a transfer function similar to the emitter-follower characteristic of Fig. 38, which exhibits a region of constant base-emitter voltage drop, is mandatory to avoid a calibration curve. However, this transfer function is not directly usable since the region of uniform junction drop has only been approached at the maximum sweep excursion of 3.0 volts. The bias possibilities considered when this problem was discussed in the previous section (emitter-follower output amplifier) are not applicable here, since a zero reference requires deliberate use of the entire characteristic curve including the transition (knee) region. Therefore, the only alternative is to increase the step size (and hence the input swing, if the number of steps is to be held constant) sufficiently so that the knee of the transfer characteristic is but a small portion of the total excursion. Of course, it is then necessary to employ a final voltage divider to restore the stairstep amplitude to the desired output level.

The maximum increase in step size is limited by the maximum positive amp-

litude of the voltage swing and the number of steps required. The former is determined by the level of the positive voltage source and the intrinsic stand-off ration (η) of the Unijunction voltage-operated reset switch, which are fixed externally at 28 vdc and 0.67, respectively. The trigger techniques used to reduce the step droop caused by the Unijunction reduce the maximum positive limit of the output swing by some two volts to approximately 17 volts. For 30 output step levels each step would be approximately 0.57 volts and the first four steps on either side of zero would be foreshortened as a result of the non-uniform diode drop. Ideal performance near zero would require at least 2.5 volt steps, a 75-volt swing and 110 volts for the Unijunction base-two supply. This supply voltage is not consistent with current instrumentation plans, and, furthermore, voltage swings in excess of 35 volts are entering the region where the probability of a transistor failure due to collector breakdown is not remote.

Thus, the only compromise now apparent is to increase the step size as much as possible (to slightly over one-half volt) and to provide a calibration curve for the steps adjacent to zero. In practice its use would be contingent on the economics of the trade-off between the inconvenience involved and the utility of the information available at that level. The reader will perhaps recall from Figs. 2 and 3 that this is the area where the measured current consists of contributions from both electrons and positive ions, and that the information sought by this experiment occurs principally after one component or the other of the total measured current has nearly vanished. This occurs at the higher voltage levels and reduces somewhat the necessity of a calibration curve near zero δV.

Figure 42 shows an emitter follower type zero reference circuit used in conjunction with the output amplifier of Fig. 37. Only one additional transistor and one resistor are required. The stairstep input waveform, V_{in}, driving this circuit is shown in Fig. 43. The corresponding output waveform, V_o, as well as two expanded views that exhibit the area around zero volts, are shown in Fig. 44.

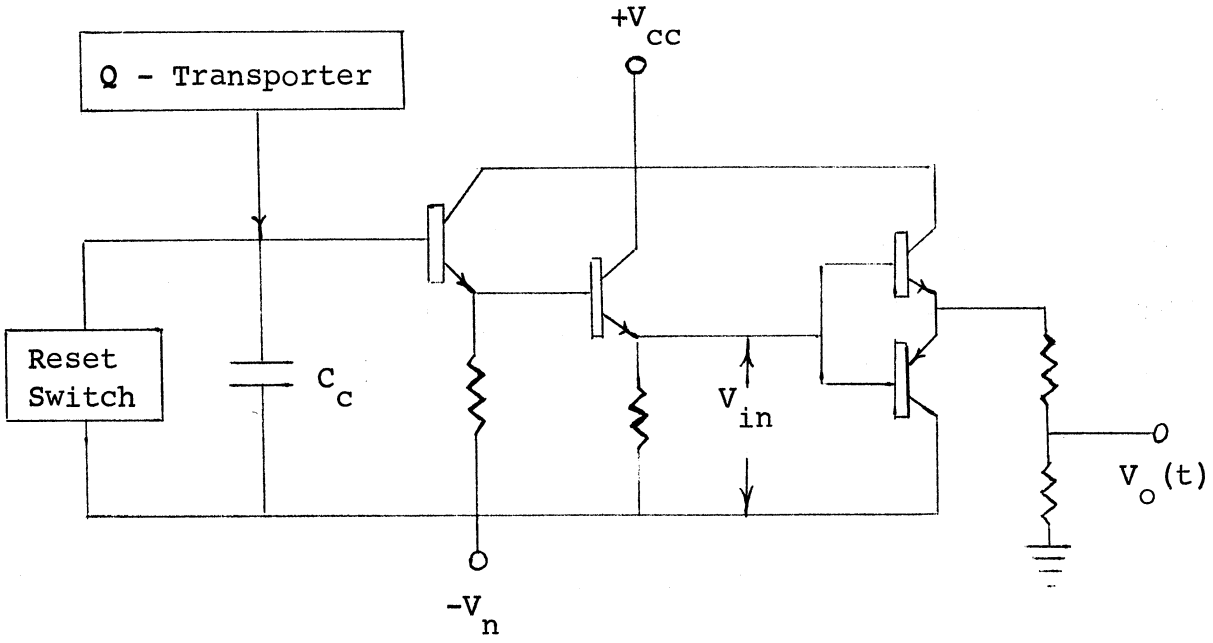


Fig. 42. Emitter Follower Zero Reference Circuit.

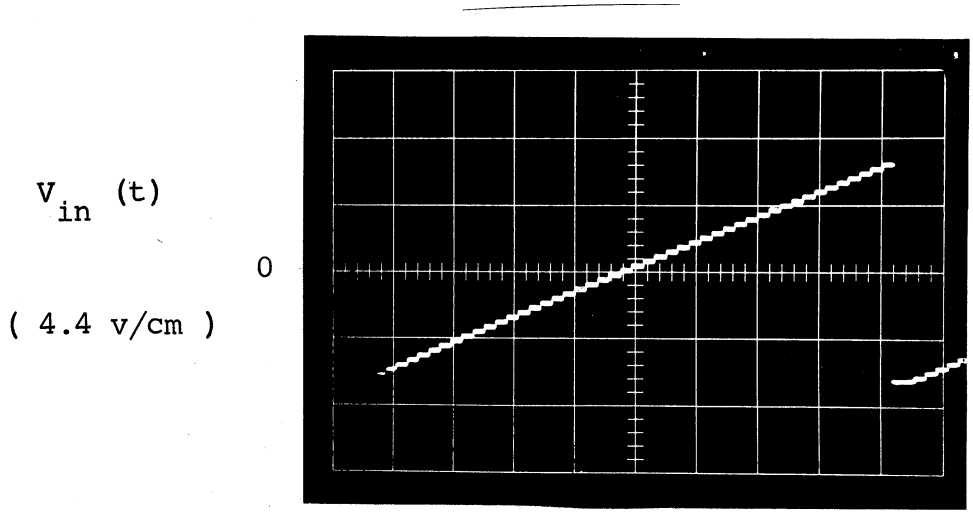
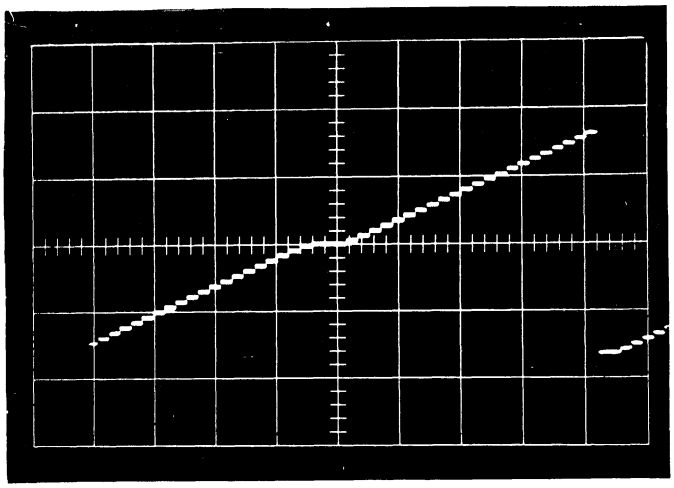


Fig. 43. Zero Reference Circuit Input Waveform.

(a)

V_o @ 2.0 v/cm

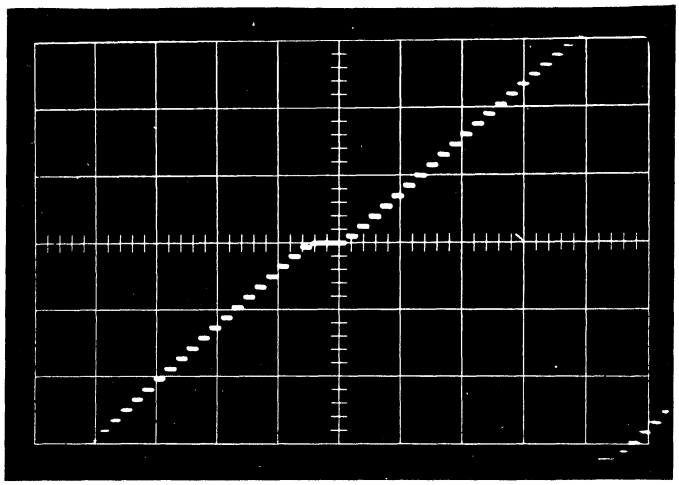
t @ 42.4 ms/cm



(b)

V_o @ 1.0 v/cm

t @ 42.4 ms/cm



(c)

V_o @ 0.5 v/cm

t @ 8.5 ms/cm

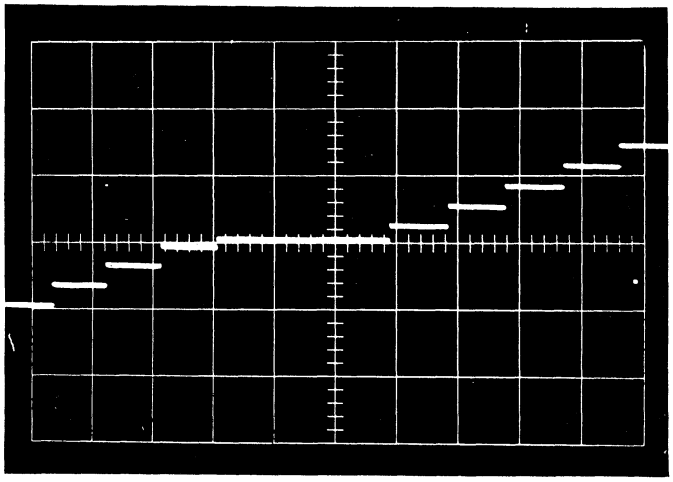


Fig. 44. Zero Reference Circuit Output Waveform.

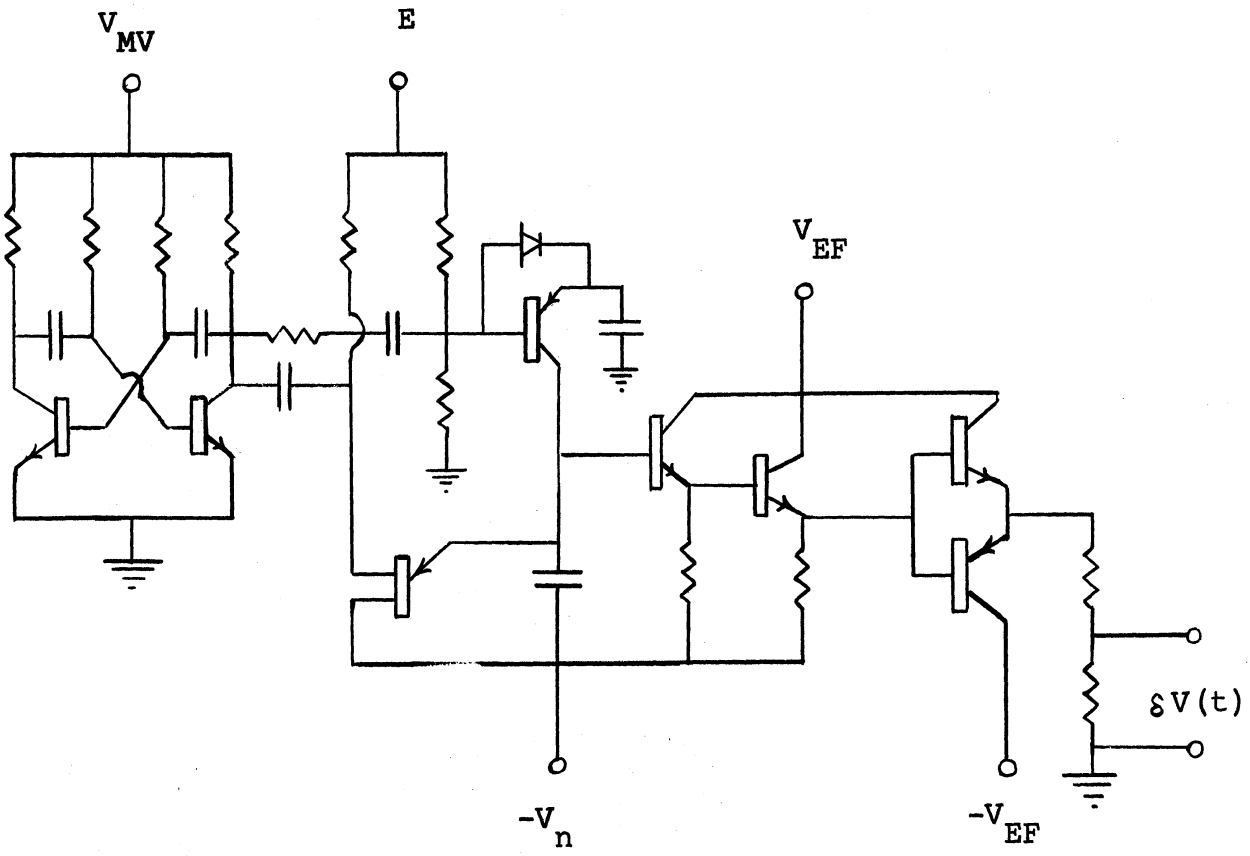


Fig. 45. δV Schematic Indicating Required Supply Voltages.

G. POWER SUPPLIES

Figure 45 is a schematic diagram indicating the required supply voltages for the circuitry developed. It is assumed that adequately regulated and temperature-compensated plus and minus 28-volt sources are available.

The maximum output swing has been shown to be approximately 17 volts. Therefore, the negative line voltage V_n must be half of this plus one half of the valley voltage bias level or about 10 volts to center the output swing on zero. To allow for minor variations in the valley point of the Unijunction and in the base-emitter drops of the emitter followers, it is convenient to determine the voltage that precisely centers the sweep about zero by supplying this negative voltage from a variable external power supply as discussed in the parts-selection procedure of Section VI. The permanent negative voltage level could be obtained from the negative 28-volt source by a simple voltage divider, but additional regulation is easily obtained by the use of a zener reference diode. Figure 46 shows the temperature coefficients of typical zener diodes. Since a single diode providing the required 10 volts would exhibit a negative temperature coefficient of 0.06 %/°C, it is necessary to use two diodes in series to develop 10 volts drop and a net temperature coefficient of zero. Figure 47 exhibits the typical reverse characteristic of these diodes. Since decreases in supply voltage magnitude are the most likely variation to occur, the diode operating point must be sufficiently past the knee of the curve to provide adequate regulation. The corresponding current is determined from the characteristic curve and this, with regulator input and output voltage levels, determines the value and power rating of the series dropping resistor.

An additional requirement of the negative supply is that it be capable of passing, in the reverse direction, positive pulses from the series combination of C_c and the Q-Transporter. These currents, which reach peaks of about 80 ma for a few microseconds, greatly exceed the regulation range of the zener. Moreover,

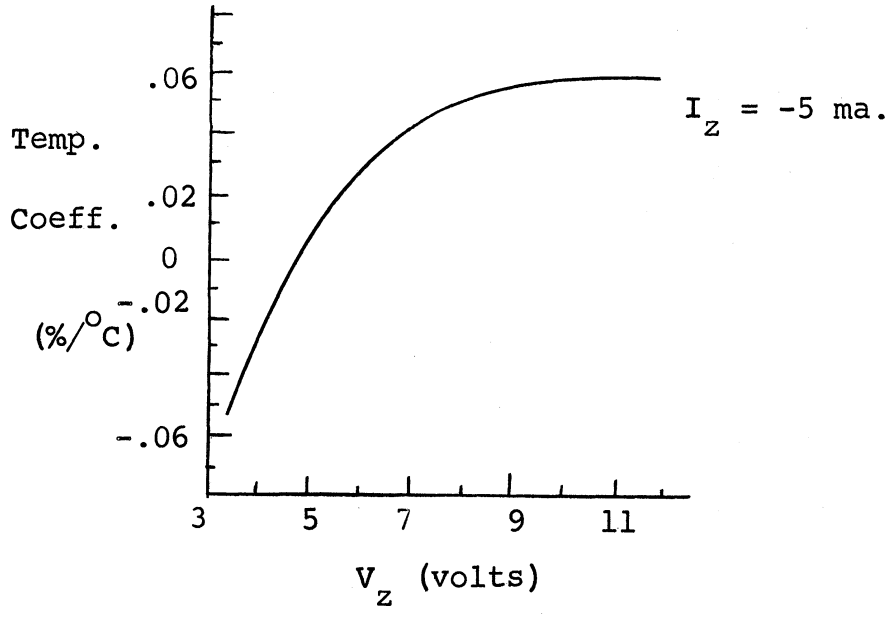


Fig. 46. Typical Temperature Coefficients of Zener Reference Diodes.

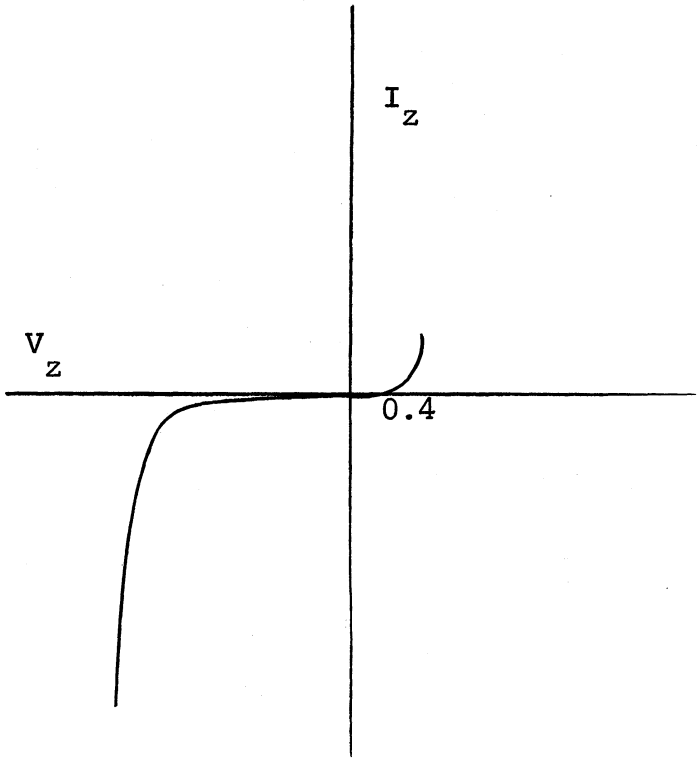


Fig. 47. Typical Zener Diode Reverse Characteristic.

if this current were made to pass through the dropping resistor and the power supply to the ground, the rise time of the steps would increase thirty-fold. Any switching device used at this point to reduce temporarily the charging resistance would in addition short out the negative supply, and hence involves the interrupting of large currents and a consequent power loss. Even more important than the power loss is the overshoot that occurs if the negative supply should be temporarily shorted to provide a low impedance path to ground. The output voltage would then change by V_n. The zener diode itself provides this switching function, since the change in current from -5 ma to + 75 ma causes the terminal voltage to change from -10 to + 0.7 volts. To suppress this overshoot, a shunt capacitance is added across the zener diode. If the capacitance is large enough, it can accommodate the change in charge of C_c without an appreciable shift in voltage level. Moreover, because of the low dynamic impedance of the zener in parallel with the capacitor, the time constant of this circuit can be made low compared with the step length, even for large values of capacitance.

The positive supply voltages present considerably less difficulty. The circuitry of the Q-Transporter and the Unijunction stages have already been designed to operate from the +28-volt supply. For ease of construction, the multivibrator supply voltage will be used to adjust the frequency of the trigger pulses for continuous control of the stairstep repetition rate. The magnitude of the trigger pulse can be maintained constant and independent of the multivibrator frequency by returning the collector resistor (R_6) of the output transistor, Q_2, directly to the +28-volt supply. Since, by reason of the high degree of asymmetry, Q_1 will be conducting 90% of the time, a voltage divider can be formed by inserting a dropping resistor in series with the collector resistance R_1.

If R_3 and R_4 are returned to this point as in Fig. 49, independent frequency control can be achieved by adjusting either R_1 or R_2. Inasmuch as the voltage at the divider will increase during the trigger pulse period when Q_1 is cut off, a further increase in the degree of asymmetry is attained. The frequency range of 80 to 200 cps as in Fig. 27 can be achieved in this way with a 70% reduction in power consumption over a zener-regulated source.

To achieve linearity in the emitter-follower stages, the impedance of the collector circuit must be low compared with that of the emitter. Moreover, the collector voltage, V_{cc}, must be less than the transistor breakdown voltage and greater than the maximum base voltage. For the 2N338, V_{CBO} is 45 volts maximum and the base voltage peak is about 9 volts. Thus the final amplifier stages, Q_7 and Q_8, of the zero reference circuit can be returned to +28 and -10 (V_n) volts, respectively. It is to be noted, however, that the emitters of Q_5 and Q_6, the first two amplifier stages are already biased by V_n to center the output on zero volts. This bias voltage is in series with the collector supply voltage, so that the sum of the magnitudes must be less than V_{CBO}. A greater measure of reliability can be achieved by keeping V_{cc} as far below rated breakdown as possible, but any voltage divider used for this purpose will also introduce series resistance into the collector circuit. As this resistance is reduced, of course, steady-state power consumption increases. Typically, 48 mw are dissipated to reduce the collector voltage 16 volts, while introducing 2000 ohms of collector resistance. Although this is a situation where voltage regulation is not required, a zener regulator diode may be used to advantage to reduce collector impedance. Figure 48 shows the variation of zener diode dynamic impedance for typical breakdown (zener) voltages and biasing currents. Thus a 12-volt zener

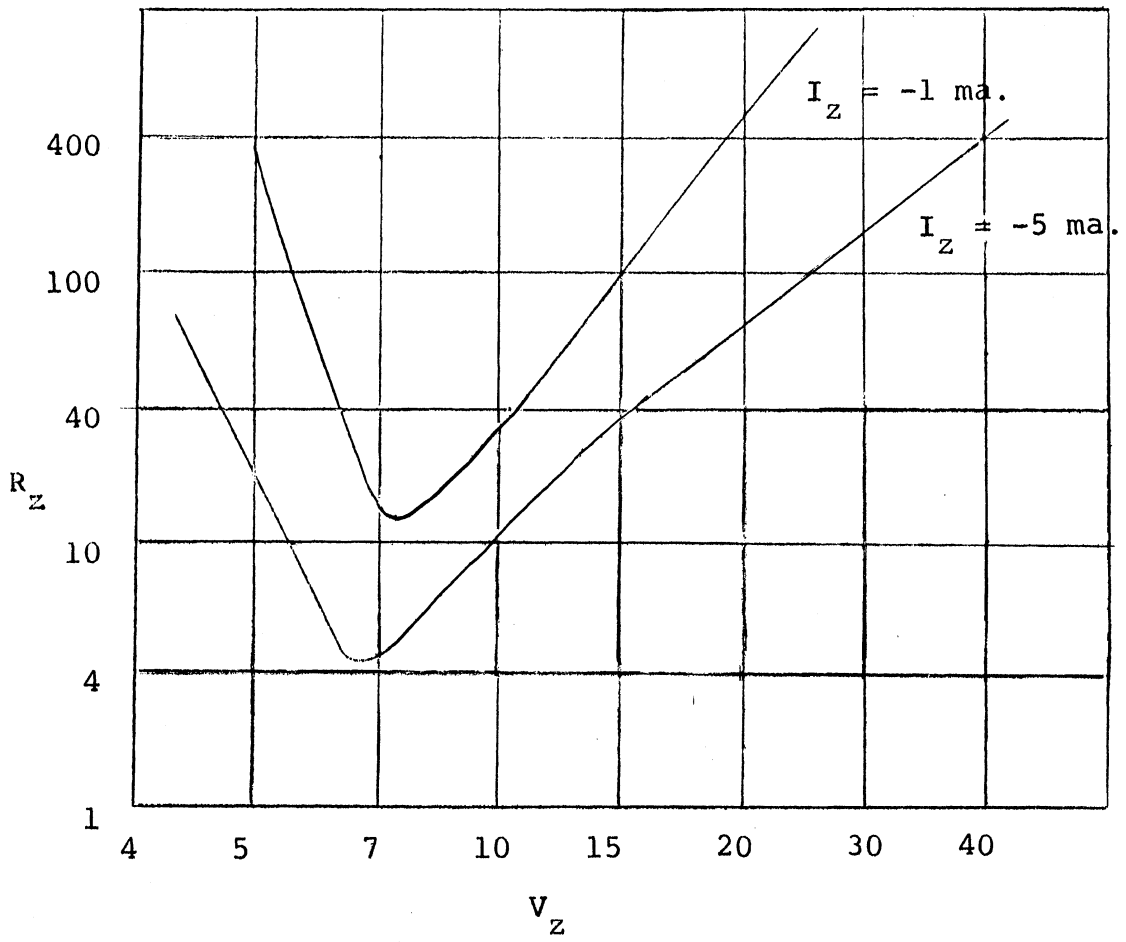


Fig. 48. Variation of Zener Diode Dynamic Impedance.

drawing 1 ma will reduce V_{ce} to 26 volts maximum, while introducing less than 100 ohms of collector resistance. The steady-state power dissipated has been reduced by 1/3 to 16 mw.

The complete circuit diagram of the stairstep waveform generator, including power-supply features, is shown in Fig. 49. Component values are listed in Table VI.

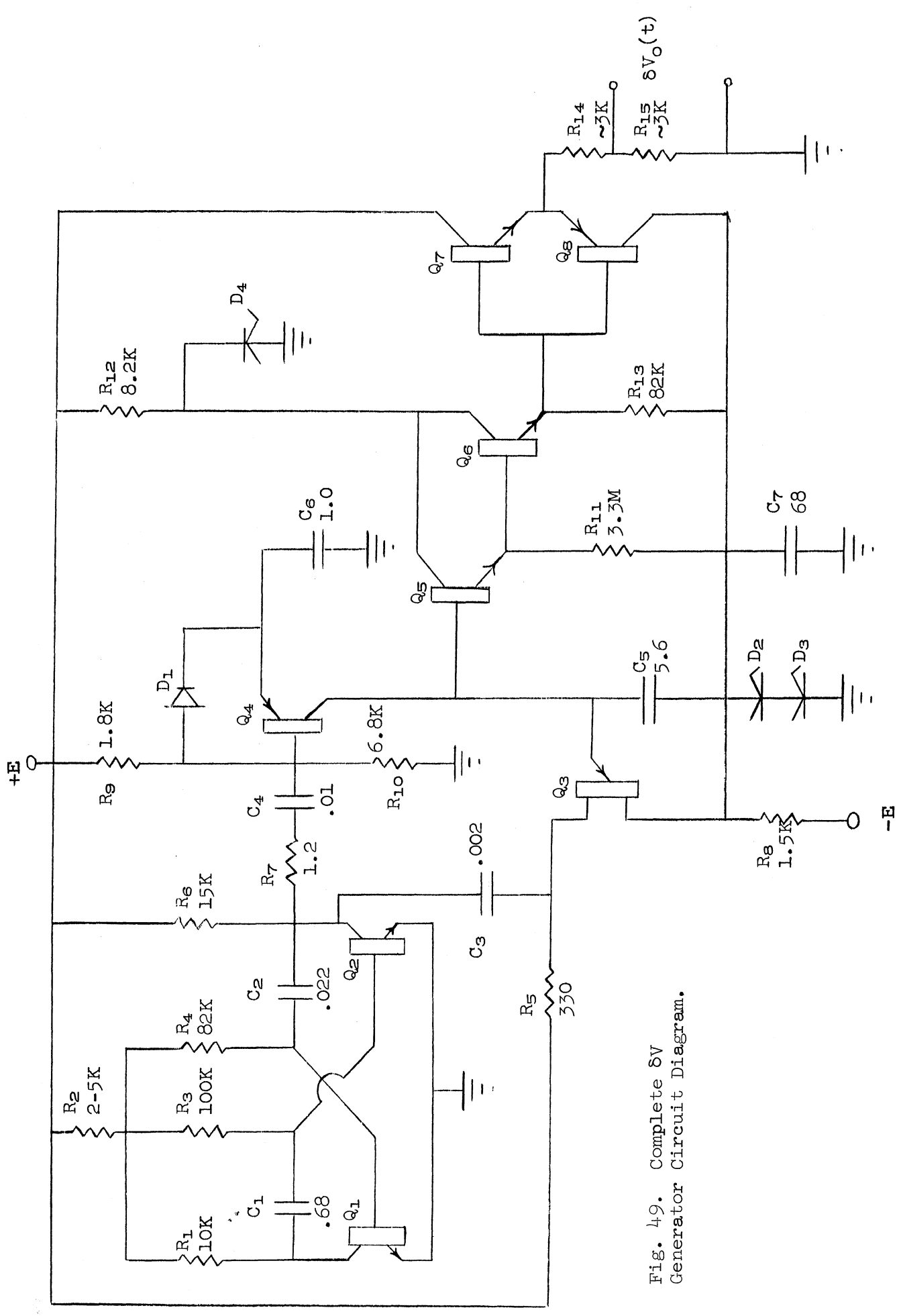


Fig. 49. Complete 8V Generator Circuit Diagram.

TABLE VI

STAIRSTEP GENERATOR COMPONENT VALUES*

	Q	C (μfd)	D
1	2N338**	.68	1N645
2	2N338**	.022	4.5 volt zener
3	2N492	.002	6.0 " "
4	2N1036	.01	12 " "
5	2N338	5.6	
6	2N338**	1.0	
7	2N338**	68.0	
8	2N1036***		

*See Section VI for component test procedures.

**May be replaced by the 2N793 for a reduction in volume (95%).

***May be replaced by the 2N329B or equivalent.

All resistors are 1/10 watt except R_8 and R_{11}, which are rated 1/4 watt.

All capacitors are rated for a minimum d-c working voltage of 35 volts except C_7, which may be rated at 15 volts.

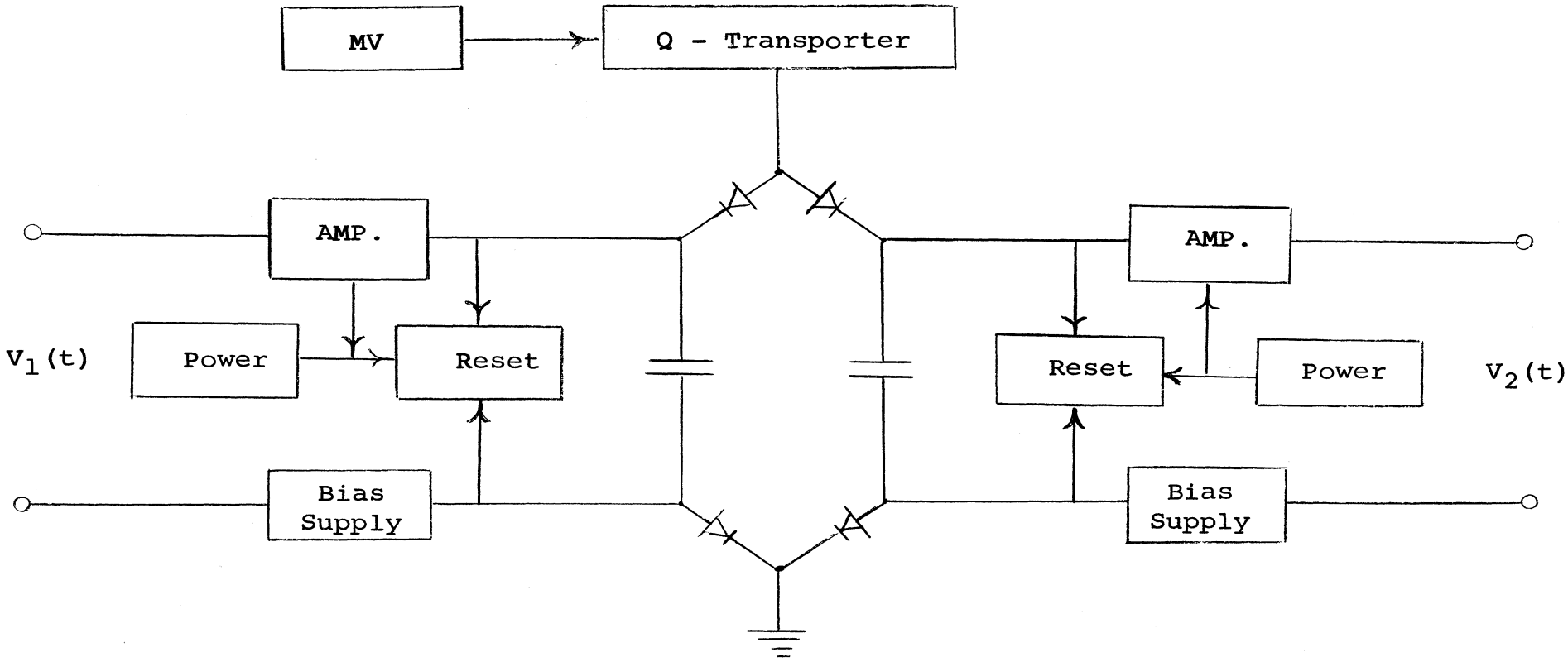


Fig. 50. Dual Output Circuit.

IV. DUAL OUTPUT CIRCUIT

The circuit design of a single-output stairstep waveform generator was discussed in Section III. This unit, without further modification, has application in Langmuir probes in which the guard and collector circuits do not require d-c isolation. The first flight test of the unit will be in such a system. In the present section, however, the switching techniques of Section II are applied to yield dual, isolated outputs from the step generator so that it may be used, as planned, in the isolated guard-collector probe configuration of Fig. 1.

A. DIODE SWITCHES

Figure 50 shows the essentials of a diode-switching system which provides the separation and isolation necessary for the dual outputs. A single Q-Transporter stage and its associated multivibrator and trigger circuit charge two identical output capacitors through the diode bridge circuit shown. The diodes permit connection of the capacitors only during the charging phase and isolate them between pulses. Identical output circuits, including a separate zero reference, Unijunction reset switch, as well as separate power supplies are necessary to maintain d-c isolation of the output circuits.

The power source and bias supply shown for each system need not be isolated from each other, but both are required; the former, to provide the power gain for the stairstep voltage developed across the output capacitor and to operate the Unijunction reset switch, the latter, to center the output sweep on zero volts. Each pair of power supplies could thus be a single tapped source. Inasmuch as each supply is isolated from the source that provides the charging pulses to

C_c, the biasing supply may be placed directly in series with the output, irrespective of ground connections, thereby simplifying the design requirements since the charging pulses need not flow through the bias supply.

Diodes of exceptionally high reverse impedance and low leakage are used for the bridge circuit. Figures 51 and 52 depict the reverse characteristics of the type FD300 diodes used. During the charging pulses, the impedance of the path shunting the capacitors is as little as twenty ohms, which insures that the charging currents to each capacitor are identical. Between pulses (during the data-collection interval) the path between the capacitors contains two back-biased diodes, each exhibiting a reverse impedance of at least 2×10^5 megohms. Thus isolation of the two outputs approaches the region where leakage resistance paths (on the printed circuit board primarily) are the limiting factors.

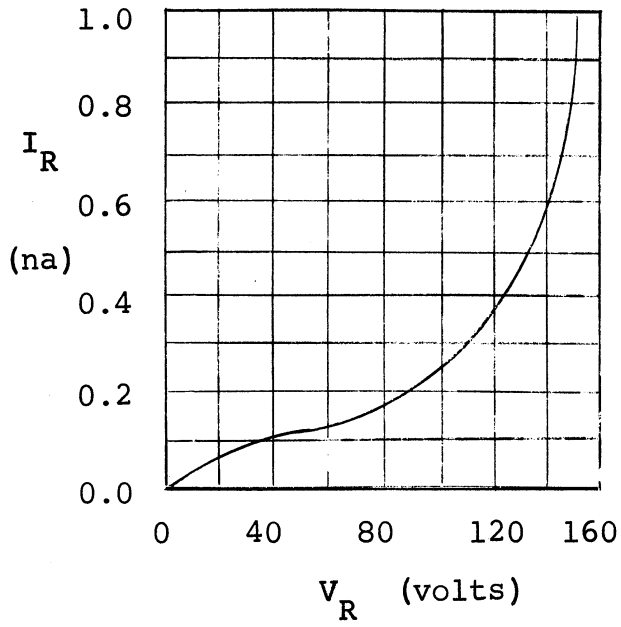


Fig. 51. Bridge Diode Reverse Characteristics (at 25°C).

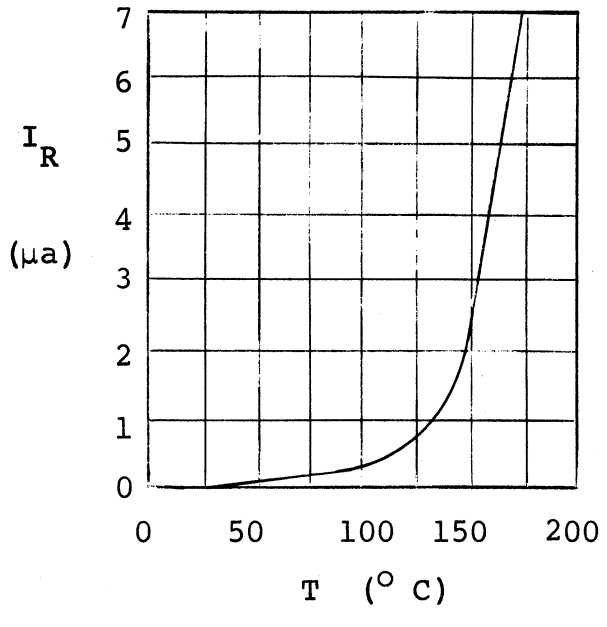


Fig. 52. Bridge Diode Reverse Characteristics Versus Temperature (at V_R = 125 volts).

B. SYNCHRONIZATION OF RESET LEVELS

Concern about the use of separate power supplies for the two isolated systems arises from the voltage dependence of the firing points of the Unijunction reset switches. It has already been shown that the performance of the emitter-follower amplifiers is independent of a wide range of variation in collector-supply voltage. To preclude the possibility of a power-supply variation or other change causing the Unijunctions to reset on different steps and thereby lose synchronization, techniques analogous to the external triggering method discussed in Section III D may be employed. The constraint of d-c isolation (even for transients, which may be of long duration compared with the step length because of the high value of "plasma resistance") prevents the use of an extension of the capacitive coupling method previously used to prevent step droop. An alternative means of synchronization is the coupled transformer scheme in Fig. 53. The transformer polarities will be arranged so that the

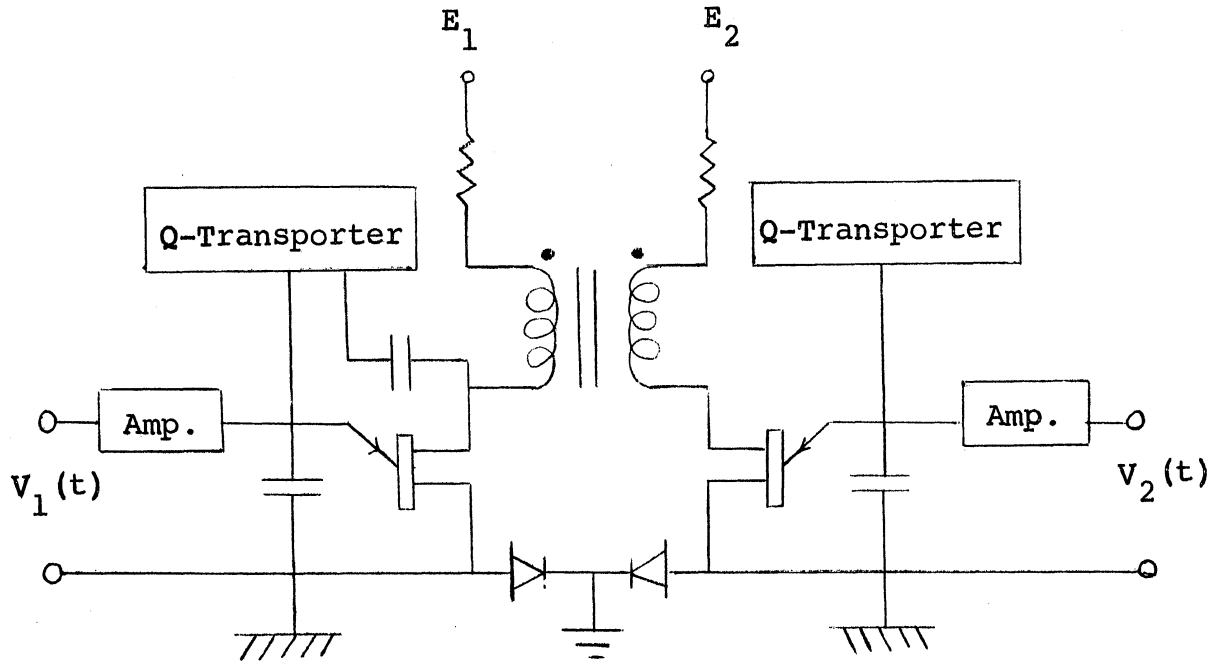


Fig. 53. Transformer Synchronization of Reset Levels.

firing of either Unijunction develops a pulse in the base-two circuit of the other that reduces its interbase voltage, thereby causing it to fire. The value of transformer inductance required can be calculated in a manner analogous to that used to determine the value of capacitive coupling needed; i.e., by specifying the minimum pulse duration, τ, required for reliable triggering. For $\tau = L/R \simeq 1 \times 10^{-6}$ seconds, where R is the sum of the Unijunction interbase resistance, R_{BB}, and the external base-two resistance, R_2, L = 7 millihenries. Miniature pulse transformers in this region are readily available.

The circuit of Fig. 54 is used to evaluate the degree of synchronization attainable by this means. The reset switch of a single δV generator is inductively coupled to a Unijunction sawtooth oscillator shown on the right of the transformer in Fig. 54. This test oscillator circuit simulates the firing of the second δV generator, while allowing more convenient measurement of the firing voltage, since the emitter voltage is continuous. Triggering of the δV

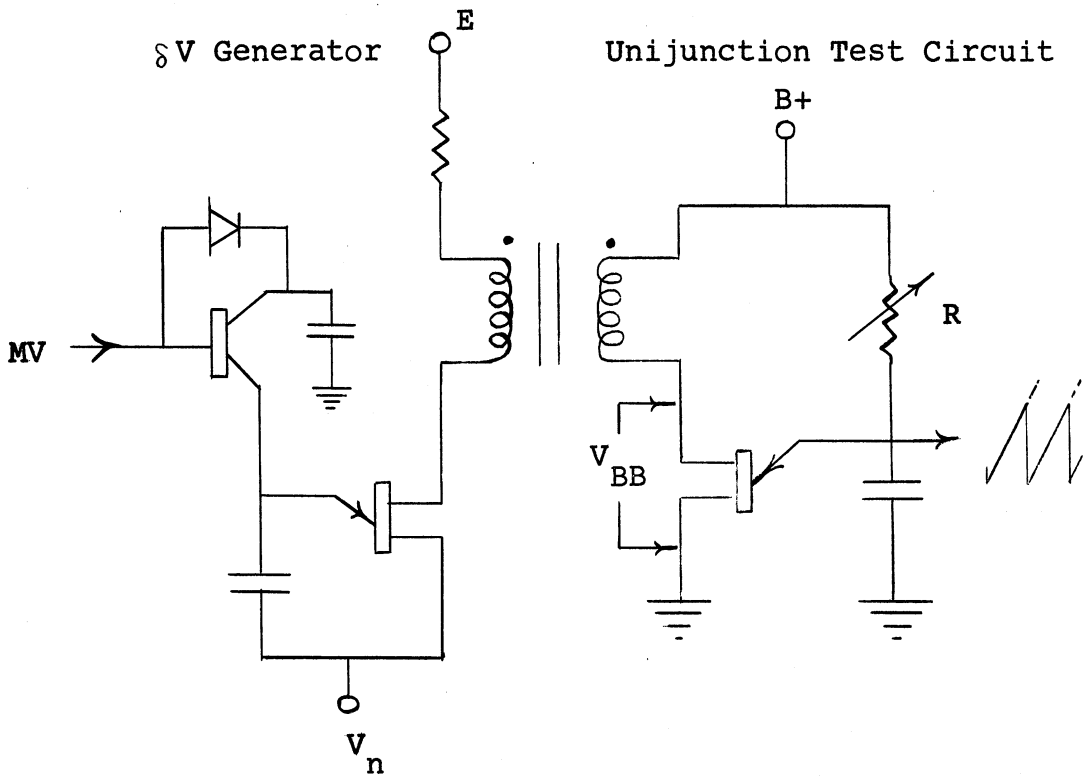


Fig. 54. Dual System Synchronization Test Circuit.

reset switch developed a negative 6-volt, 7-μsec spike in the interbase voltage of the test Unijunction. This resulted in a 1.6-volt drop in the emitter firing point, V_p, or synchronization over three step levels. This is equivalent to a ± 10% frequency zone of synchronization and should adequately compensate for any discrepancies likely to occur between the two output circuits during flight. Figure 55 shows the transformer coupled synchronizing pulse, developed by the firing of the 8V reset switch, as it appears across the interbase resistance of the second Unijunction. The overshoot that appears after the negative pulse would not occur until after the discharge was completed (~ 250 μs) if the second Unijunction had been permitted to fire. Firing was prevented (by reducing the interbase voltage to zero) to exhibit clearly the magnitude and duration of the coupled pulse.

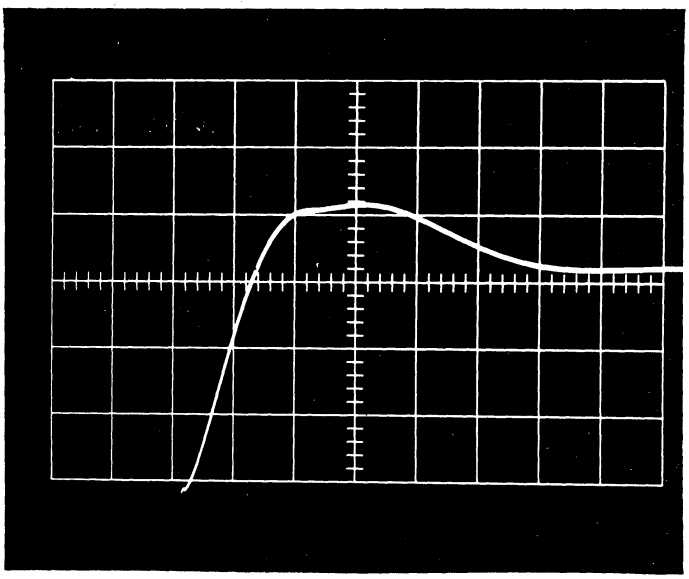


Fig. 55. Transformer-Coupled Synchronizing Pulse.

The sawtooth oscillator test circuit in Fig. 54 is additionally useful for experimentally selecting the optimum Unijunction transistors for flight purposes. The output voltage across the emitter capacitance is a sawtooth

sweep whose minimum is the Unijunction valley voltage V_v, and whose maximum is the peak point voltage V_p. The amplitude of the output swing is thus equal to $V_p - V_v$ (a quantity that is to be maximized to develop the largest possible step and thereby minimize the effect of the nonlinear region of the zero-reference amplifiers).

In addition, by means of careful adjustment of R, it is possible to achieve an equilibrium condition where the emitter voltage will neither increase nor decrease, since the direct current supplied through R that is flowing into the forward biased emitter junction is insufficient to initiate avalanche breakdown according to Fig. 31. By means of this steady-state condition, the value of the peak point currents of a sample of Unijunction transistors may be conveniently determined. The significance of this parameter is that it has been shown in Section III D to contribute directly to the droop of the top steps.

According to the manufacturer's specifications, the quantity $V_p - V_v$ may vary from 11.8 to 17.8 volts under the intended operating conditions, and the peak point emitter current has been found to vary from 2 to 30 μa in a sample of six units, which makes knowledge of these parameters mandatory for each Unijunction and the use of this simple circuit extremely advantageous.

V. ERROR ANALYSIS

A. STEP DROOP

When the charging of the output capacitor through the Q-Transporter stage was discussed, it was asserted that the leakage current, I_{CO}, was at least four orders of magnitude less than the charging current and hence negligible. This was a reasonable conclusion for the time interval concerned. Attention will now be directed to the interval between charging pulses where the same leakage currents will have a more prominent role.

Figure 56 depicts the currents that flow during the data-collection intervals between charging pulses. The transistor leakage currents tend to

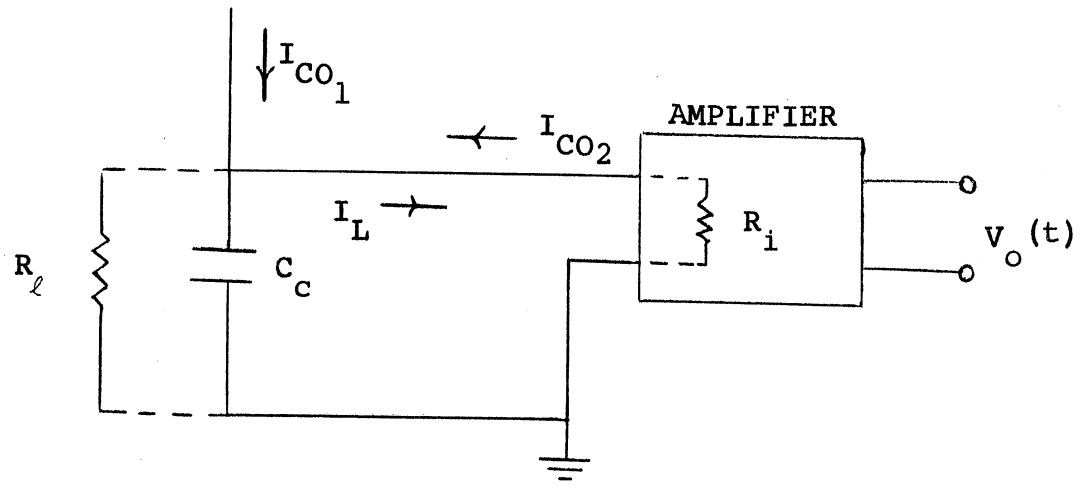


Fig. 56. Output Capacitor Currents.

replenish the charge lost by C_c as a result of the finite shunt (leakage) resistance of the capacitor as well as the flow of load current, I_L, into the input resistance of the output amplifier. It has been shown that the latter is subject to the fundamental physical restriction of the shunting effect of the collector equivalent resistance, r_c. The capacitor leakage resistance has been experimentally determined to be of the order of 10^9 ohms, which is negligible compared to collector resistances in the vicinity of 10^7 ohms.

Thus, immediately after a charging pulse, the charge on the output capacitor is given by:

$$q_c(t) = C_c V_c(t) \tag{41}$$

and the load current by:

$$I_L = \frac{V_c}{R_i} e^{-t/\tau} \tag{42}$$

where $\tau = R_i C_c \simeq 25$ sec and $0 \leq t \leq 8$ ms. Thus I_L is virtually constant and equal to V_c/R_i, for t equal to the step length, T, of 8 ms.

The change in charge on C_c due to the flow of collector leakage current and load current during the interval between charging pulses will thus be:

$$\Delta q_c = (2I_{CO} - I_L)\, T \tag{43}$$

for a percentage change in charge of:

$$P_q = \frac{\Delta q_c}{q_c} = \frac{2I_{CO} - I_L}{C_c V_c} T \times 100$$

$$= \left(\frac{2I_{CO}}{V_c} - \frac{1}{R_i} \right) \frac{T}{C_c} \times 100 \tag{44}$$

The variation of the capacitance of C_c with temperature affects the output voltage to an extent beyond that described by Eq. (44). Thus the percentage change in output voltage, P_v, is P_q/K_t, where K_t is the temperature coefficient of C_c expressed as a percentage of the 25° capacitance value. Values of P_v at the end of each step length (droop) have been calculated for changes in temperature over the design range of step voltage (V_c). The other parameters in Eq. (44) are assumed constant with the step length, T, equal to 8 msec, C_c equal to 5.6 μfd, and the emitter-follower input resistance, a conservative 5 megohms. The calculations and results are shown in Table VII below.

TABLE VII

P_v, PERCENTAGE DROOP OF OUTPUT STEPS WITH TEMPERATURE

T (°C)	I_{CO} (μa)	V_c (vdc)	P_q (%)	ΔC_c (%)	P_v (%)
-5	0.0002	0.5	-.0286	-2.3	-.0293
"	"	17.0	"	"	"
25	0.005	0.5	-.0258	0	-.0258
"	"	17.0	-.0286	"	-.0286
55	0.135	0.5	-.0486	2.3	+.0476
"	"	17.0	-.027	"	-.0264
65	0.40	0.5	+.20	3.15	+.1937
"	"	5.0	-.006	"	-.0055
"	"	10.0	-.017	"	-.0166
"	"	17.0	-.022	"	-.0214

These values, based on Eq. (44), demonstrate the following facts:

(1) That were it not for the temperature dependence of the leakage term in Eq. (44), the percentage droop would be exactly the same for all the steps regardless of voltage level.

(2) That while the departure from zero slope is uniformly small, the deviations are cumulative, resulting in maximum error at the higher voltage levels.

(3) That high leakage currents impart positive slopes to the initial steps, since significantly more charge is added than is extracted during periods of low output voltage.

(4) That the load-current term can be reduced by increasing the input resistance of the amplifier.

(5) That the over-all percentage droop is inversely proportional to the magnitude of C_c.

Since the variation of I_{CO} is so great over the design temperature range, it is not feasible to attempt to match the load current with the leakage currents that flow into C_c to reduce the cumulative error. This would be the equivalent of an attempt to match a linear variation with an exponential and is possible only over small intervals. Therefore step droop and cumulative error are best reduced by the approach previously employed, i.e., using low leakage transistors, large output capacitance, and high amplifier input resistance. The results attained (Table VII) are deemed adequate for the experiment.

B. ENVIRONMENTAL EFFECTS

The following is a description of the performance of the δV stairstep

generator circuit under adverse voltage and temperature conditions. Attention is directed toward the degree to which the number of steps, the step size, and the d-c level of the steps remain constant.

1. Voltage Stability

Variations in supply voltage can affect the output waveform in three ways: (1) the number of steps may change, (2) the step size may change, and (3) the d-c level of the waveform may change. The first variation, the number of steps, is affected principally by changes in the firing level, V_p, of the Unijunction reset switch, if the step size and d-c level are constant. V_p, in turn, is directly proportional to the regulated supply voltage, E. The voltage divider action of the Unijunction between the base-two and emitter terminals, provides an additional regulation factor of η. For a step size of 510 mv (a 17-volt swing with 30 steps, it is possible to center the firing point between two steps so that as much as a $\pm$200-mv variation can occur without changing the output swing by one step. Therefore regulation of the positive 28-volt supply to within 300 mv or about 1% is adequate to insure against variation in step number.

The second variation, step size, is affected principally by changes in the collector voltage of Q_2 and/or in the steady-state Q-Transporter base voltage, V_b. Since these circuits have been designed to be self-compensating in Section III B, variations several times the above tolerance of $\pm$300 mv may be experienced without adverse effects.

The third variation, changes in the d-c level of the stairstep waveform, are the result of changes in the negative supply voltage, V_n, used to center the waveform on zero volts. This biasing voltage is obtained from the negative

28-volt supply by a series-dropping resistor and a zener diode. The supply voltage is itself regulated to within ±300 mv, while careful selection of the operating current for the zener diode (set by the value of series dropping resistance) can result in regulation of V_n to within a few millivolts.

2. Temperature Stability

Variations in ambient temperature affect principally the nominal value of capacitors and the magnitude of the voltage drops across semiconductor junctions. The capacitance variation has previously been accounted for in Sections III B and V A. The variation of junction voltage drops can be compensated by careful selection of the temperature coefficient of the trigger circuit capacitor, C_4. By this means compensation of step size with temperature to less than 3% over the range of from 0° to 50°C has been attained. Finer compensation requires the use of measuring equipment approximating, or better still, exceeding, the resolution of the recording equipment used in the actual flight. The degree of compensation attainable is principally a function of the patience exercised in the selection of the coefficients of C_4 and R_7 of Fig. 49.

3. In-Flight Calibration

Previous instrumentation packages employed an internal calibration circuit to check system performance during flight. For approximately one second out of every thirty, the output of the linear δV is removed from the probe electrodes and applied to a known resistance standard. The δV output is assumed constant and accurately known, allowing calibration of recorded galvanometer deflections in terms of the calculated current through the known resistance. In this manner,

changes occurring in modulation, transmission, demodulation, and recording equipment may be detected and considered.

The first flight test of the digitized δV generator, described herein, will be as part of such a system. Internal switching and timing circuits will apportion data-collection and calibration times between the two δV generators, providing both linear and discrete data, and permitting evaluation of the stability of the discrete step levels in terms of the stability of the output of the proven linear δV generator. It is expected that such a test will be made late this year, in an experiment requiring only a single-output δV.

VI. PRACTICAL CONSTRUCTIONAL DETAILS

To facilitate the construction of the circuit described in the preceding sections, control of the output parameters (the number, amplitude, and duration of the steps, and the repetition frequency) has been concentrated in a few key components. As a result, the other components are not subject to stringent tolerances, and may be assembled into the circuit without extensive testing. Experience will dictate if quality control testing of the Go, No-Go variety is justified to determine whether these components are within manufacturer's specifications. The exceptions are capacitors C_5 and C_6 of Fig. 49 (previously referred to as C_c and C_e), whose temperature coefficients are of vital importance. A method for determining the temperature coefficients of large capacitors such as these, has been developed and is detailed in Appendix III.

It will be noted, especially from Section III, that a single transistor type is often used in more than one circuit application. The 2N338, for example, is used as a switching device in the multivibrator circuit and as an impedance transformer in the emitter follower stages, while the 2N1036 is used as a Q-Transporter as well as an impedance transformer. Different qualities are required for these roles, and transistors of the same lot are subject to wide variations in parameters, which makes selection desirable and profitable.

A. TRANSISTOR SELECTION

Transistors may be evaluated by measuring the hybrid (h) equivalent circuit parameters, the collector leakage current, I_{CO}, and the collector breakdown voltage V_{CBO}. These parameters are conveniently measured on such instruments as

the Owens Laboratories Semiconductor Test Set, Model 310. Transistors exceeding rated leakage or failing to meet the specified collector breakdown requirements are not used. Acceptable 2N338's are then ranked in descending order of input impedance (h_{ob}^{-1}) and used in the following sequence: Q_5, Q_6, Q_7, Q_1, and Q_2. Q_5 is the preferred position because of the high amplifier impedance required at the input to avoid step droop. Q_1 and Q_2 can be further differentiated by selecting the unit with minimum saturation resistance (R_{CE}) for the Q_2 position.

Collector leakage currents to 10^{-14} amp may be evaluated by means of the Keithley Electrometer used as shown in Fig. 57. This measurement is especially useful for determining the optimum 2N1036 for the Q-Transporter stage (Q_4).

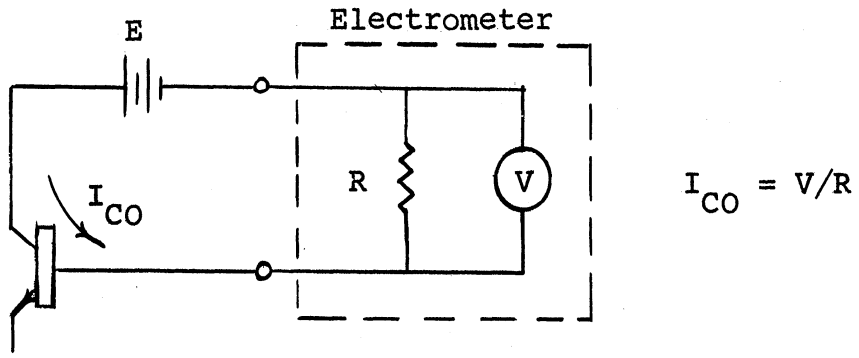


Fig. 57. Transistor Leakage Current Measurement Circuit.

Unijunction Transistors (2N492) have been evaluated in Sections III D and IV B. In summary, the test circuit of Fig. 54 is used to select the Unijunction possessing minimum peak emitter current (I_p) and maximum emitter voltage swing ($V_p - V_v$).

B. CIRCUIT ADJUSTMENT

The range of voltage variation across the output capacitor, C_c, is controlled

by the parameters of the Unijunction reset switch connected across it. This voltage swing has been set by zero-reference considerations, Section III F, at the maximum feasible variation of 17 volts. Under this restriction, the step size and the number of steps cannot be chosen independently, since the product must remain constant at 17 volts. Yet the design is such that the 17-volt swing can be divided into anywhere from 10 to over 100 equal levels, while the step size (as well as the total voltage output swing) can then be adjusted by a voltage divider to the desired levels.

Separate circuit adjustments are provided to control:

(1) the step size across C_c,

(2) the step length (and sweep repetition frequency), and

(3) the symmetry of the voltage swing about the reference at zero.

The step size is controlled principally by the value of C_4. Although R_8, R_9, and the quantity C_6/C_5 (C_e/C_c) also exert varying degrees of control, they are subject to other considerations that restrict their range of values. Variation of C_4 from 0.01 to 0.1 μfd results in a range of step sizes from 0.313 to 1.07 volts, based on a 17-volt swing. This is adequate control for most intended applications.

After the value of C_4 has been selected to provide the desired step size, its temperature coefficient is determined empirically to compensate for variation in step size with temperature. Considerable flexibility in the choice of temperature coefficient can be achieved by making C_4 two parallel capacitors or making R_7 a temperature-sensitive resistor, or both, as needed.

The step length, which for a fixed number of steps determines the stairstep repetition frequency, is controlled by adjusting the frequency of the multivibrator

driver. The range of repetition frequencies is limited at the high end (short step lengths) by the degree of asymmetry obtainable from the multivibrator; and at the low end (long step duration) by the maximum permissible step droop. The latter could be reduced, of course, by the use of a larger capacitor for C_c, since at the lower sweep frequencies more time could be alloted to the reset operation (discharging of C_c through the Unijunction) while maintaining the same ratio of sweep time to reset time. As described in Section III G, R_2 provides multivibrator frequency control without altering the magnitude of the trigger voltage or appreciably changing the degree of asymmetry. A frequency variation of from 40 to 178 cps results from a change in R_2 of from 0.0 to 68 kilohms. The asymmetry changes by less than 12% over this range. If required, the frequency range could be extended in either direction, while still maintaining control with R_2, by appropriate adjustment of R_3 and R_4.

In addition to the voltage reference at zero, a negative reference may be easily added to the waveform as a calibration check. A zener diode placed from the emitter of Q_6 to ground will clamp the output at the zener voltage whenever the driving voltage is more negative. To prevent clamping of the positive portion of the swing at the 0.4 volt forward breakdown of the zener, a junction diode is inserted in series, as shown in Fig. 58.

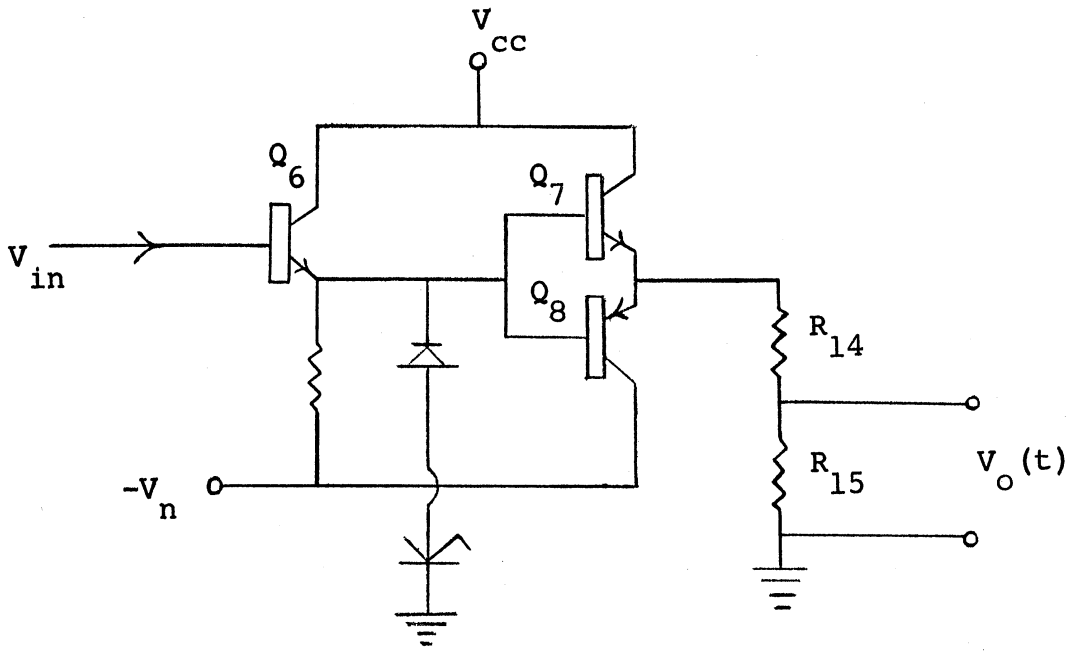


Fig. 58. Negative Voltage Reference Circuit.

Once the above adjustments for step size, number, and length have been made, the precise biasing voltage, V_n, that centers the sweep on zero volts can be determined. This is most readily done by inserting a variable d-c voltage source in place of diodes D_3 and D_4. The diodes are then selected such that their sum exhibits the required drop with nominally zero temperature coefficient, by means of Fig. 46 and experimental verification. Finally, the values of R_{14} and R_{15}, the output voltage divider, are selected so that the output voltage swing has the correct amplitude (nominally -3.0 to +3.0 volts) and so that the total series resistance is approximately 5 kilohms.

The components are placed on the printed circuit board in slightly elevated positions to prevent lead stress with board flexure. Transistors are elevated about 1/8 inch to provide space to accommodate a heat sink

during the soldering operation. The components are then encased in insulating foam* to dampen mechanical shock and vibration and to offer thermal resistance to the flow of heat from external sources. Figures 59 and 60 are photographs displaying the wiring connections and component arrangement on the printed circuit board, respectively.

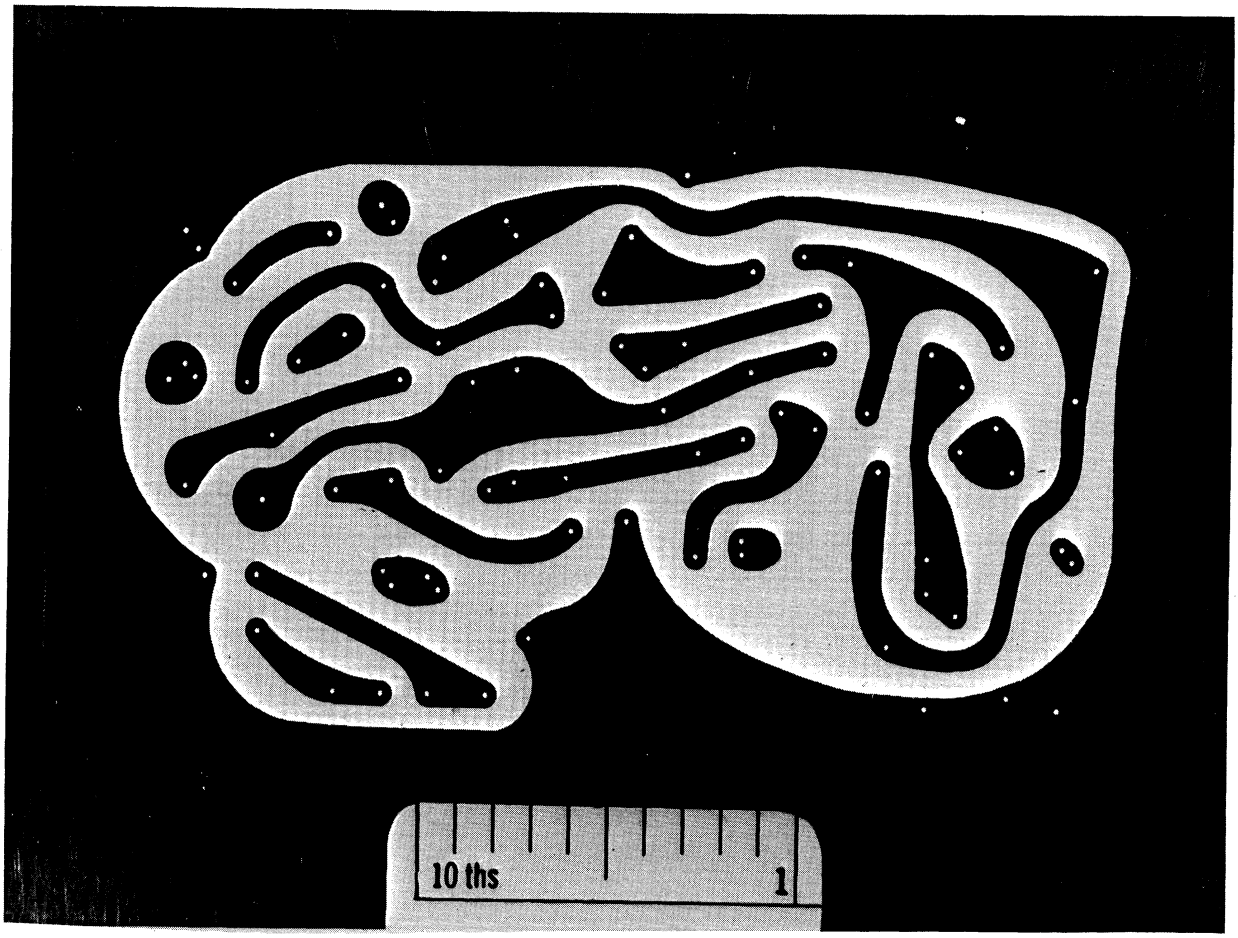


Fig. 59. Wiring Connections on Printed Circuit Board.

*Resin no. 1111, RAD Electronic Plastics, Inc., Brooklyn, N.Y.

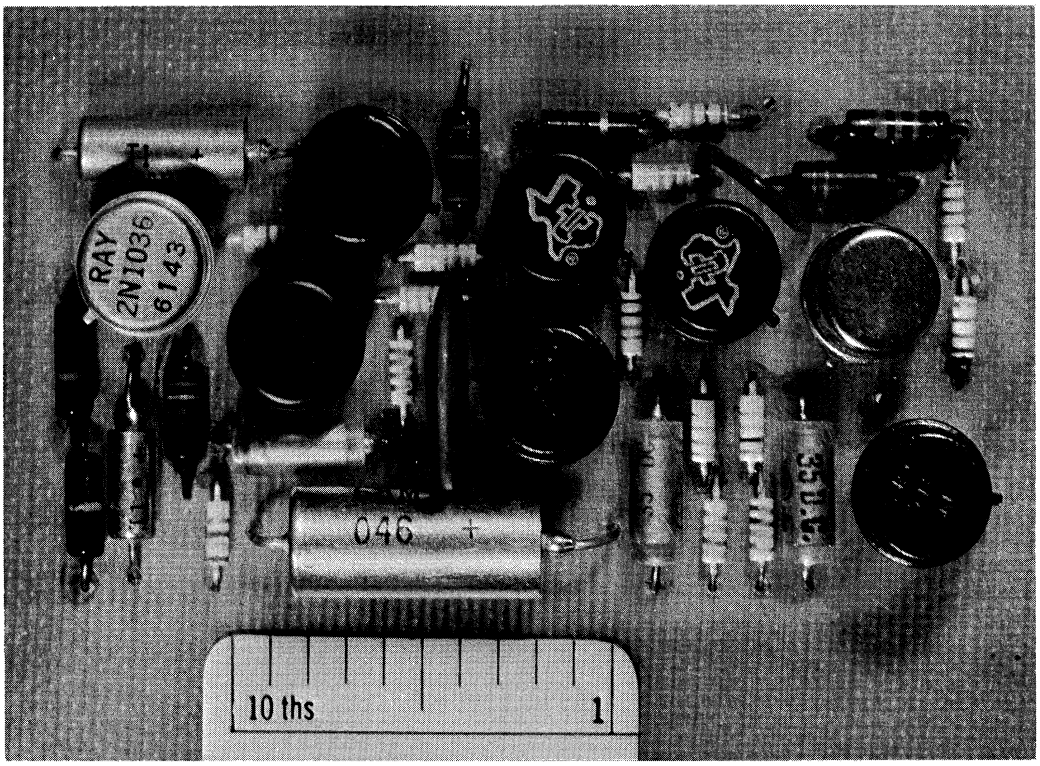


Fig. 60. Component Arrangement on Printed Circuit Board.

APPENDIX I

STORAGE COUNTER STAIRSTEP WAVEFORM GENERATOR[1]

The square-wave voltage source of Fig. 10 can be conveniently represented by the battery and switch arrangement of Fig. I-1, where r_b represents the multivibrator high-level output impedance.

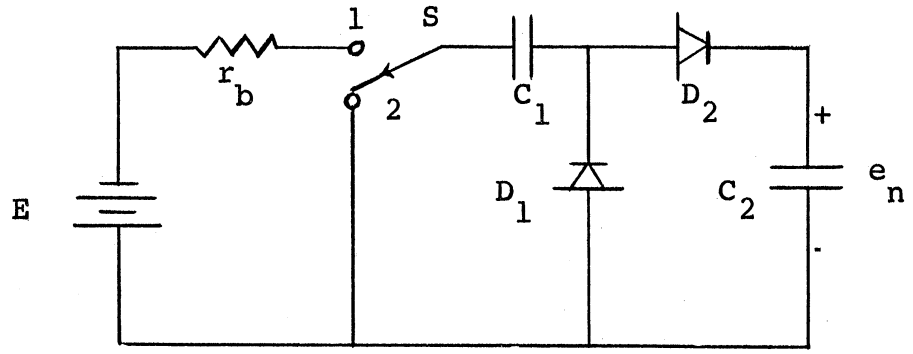


Fig. I-1. Diode Counter Circuit.

When switch S is in position 1, C_1 charges through the forward resistance of diode D_1 and the internal resistance of the battery source with time constant $\tau_1 = C_1 (r_b + r_{D_1})$. If this is short compared with the length of time S is in position 1, the steady-state condition of $F_{C_1} = E$ will be attained. When S is switched to position 2, charge flows from C_1 to C_2 through D_2 with time constant $\tau_2 = \frac{C_1 C_2}{C_1 + C_2} r_{D_2}$ until $V_{C_1} = V_{C_2}$, if the time the switch is in position 2 is much greater than τ_2.

Assuming steady-state conditions are achieved (an absolutely necessary condition for voltage reference applications of this circuit), the relationships between successive pulses to C_2 can be determined from the principle of

of conservations of charge:

$$\sum q\ (t_1) \quad = \quad \sum q\ (t_2) \tag{I-1}$$

Thus:

$$V_1\ (t_1)\ C_1 + V_2\ (t_1)\ C_2 = V_1\ (t_2)\ C_1 + V_2\ (t_2)\ C_2 \tag{I-2}$$

But at time t_2, when S is in position 2: $V_1\ (t_2) = V_2\ (t_2) = V_o\ (t)$, so that:

$$V_1\ (t_1)\ C_1 + V_2\ (t_1)\ C_2 = (C_1 + C_2)\ V_o\ (t_2) \tag{I-3}$$

After n pulses, the output voltage on C_2 will be e_n, so that from Eq. (3):

$$E\ C_1 + e_n\ C_2 = (C_1 + C_2)\ e_n + 1 \tag{I-4}$$

Thus the step increment Δe_n can be written:

$$\Delta e_n = e_n + 1 - e_n = (E - e_n)\ \frac{C_1}{C_1 + C_2} \tag{I-5}$$

Since Δe_n is a function of n, the step increments will not be uniform. This feature must be eliminated before the circuit could be considered for voltage reference purposes.

The circuit of Fig. I-2 is an attempt to accomplish this by means of the feedback path that alters the charging voltage to C_1 according to the level of C_2.

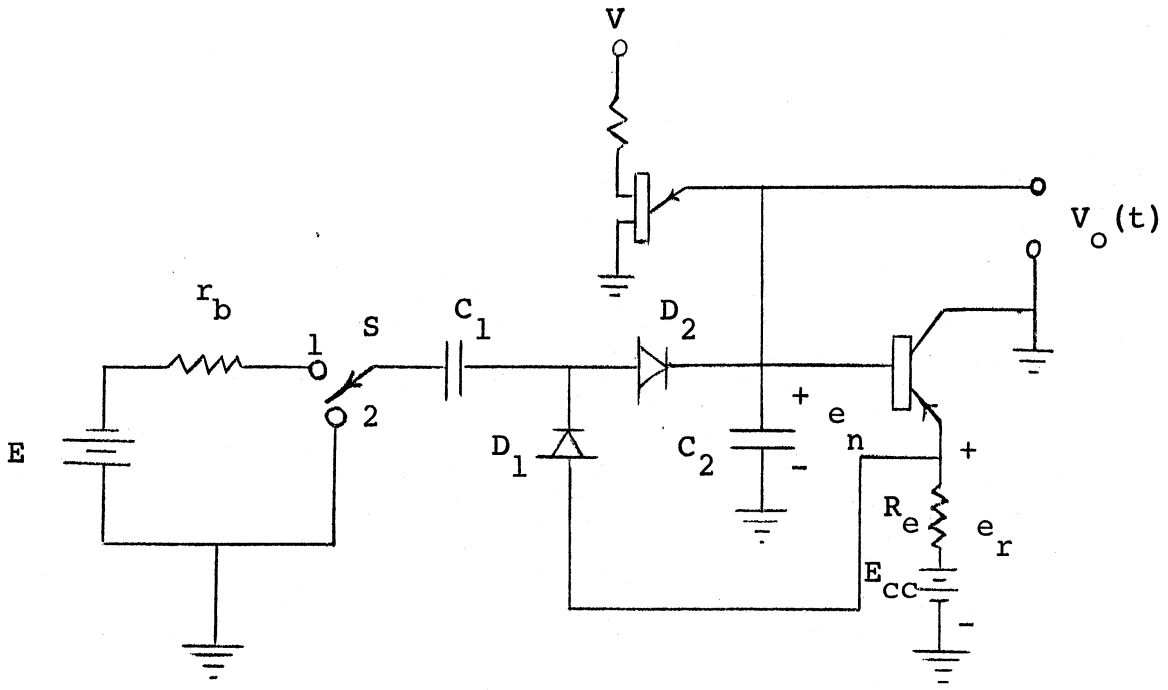


Fig. I-2. Linearized Storage Counter Circuit.

The transfer function of the emitter follower feedback amplifier insures that the error voltage e_r is of the same sign and nominally the same magnitude as the output voltage e_n.

Proceeding as before, application of Eq. (3) yields:

$$(E + e_r)\, C_1 + e_n C_2 = (C_1 + C_2)\, e_{n+1} \tag{I-6}$$

and

$$e_{n+1} = (E + e_r)\, \frac{C_1}{C_1 + C_2} + e_n \frac{C_1}{C_1 + C_2} \tag{I-7}$$

so that

$$\Delta e_n = e_{n+1} - e_n$$

$$= (E + e_r - e_n)\, \frac{C_1}{C_1 + C_2} \tag{I-8}$$

For unity gain in the emitter follower stage, e_r equals e_n, making the step increments independent of n for perfect uniformity.

However, it is apparent from Fig. I-2, that the emitter resistance, R_e, across which the error signal e_r is developed, is in series with the path by which C_1 recharges and hence τ_1 is increased. Moreover, since the loading on C_2 is to be kept to a minimum (certainly no less than 5 megohms) to prevent droop, R_e must be large. The simultaneous requirements of high input impedance with unity voltage gain can be met by a multi-stage emitter-follower amplifier as discussed in Section III D.*

In spite of the low output impedance attained thereby, the fact that the charging current to C_1 flows through the emitter resistance causes a transient spike to appear in the emitter voltage. When switch S begins the recharging phase of the cycle, the emitter load impedance is abruptly changed. The magnitude of the resulting transient could be suppressed, of course, by the addition of a capacitor from the emitter to ground, but this would increase the recovery time as well. As a consequence, it is not possible to obtain the output signal from the same resistance used to develop the error signal. Separate multi-stage emitter-follower amplifiers are thus required, and the loading on C_2 is automatically doubled.

If this concession is made, the time constants of the charge transfer processes, and the degree to which steady-state conditions are achieved in each phase of the cycle can be calculated. Since E_{cc} must exceed the expected

*High input impedance could be achieved, of course, by use of a vacuum-tube stage operating as a cathode follower, even with relatively low values of load resistance.

output swing of 17 volts, it is convenient to make it the low impedance supply voltage of 28 volts. Assuming unity gain feedback, Eq. (8) becomes:

$$e_n = 28 \frac{C_1}{C_1 + C_2} \qquad \text{(I-9)}$$

C_2 has been determined from leakage considerations and Unijunction peak discharge current limitations to be 5.6 μfd. For half-volt steps, Eq. (9) shows C_1 to be approximately 0.1 μfd. τ_2 is thus about 10 μs, while τ_1 is approximately 1.5 ms. These values were calculated assuming a minimum value of diode forward resistance. This is valid for the instant after switching when the driving voltage is a maximum. But as the driving voltage decays, the nonlinear characteristic of the diodes describes how the series resistance increases, so that the charge transfer is never really completed in four or five times the value of the above time constants. The equilibrium process implicit in the short value of τ_2 could be utilized to replenish the charge lost as a result of the excessive loading on C_2, were it not for the asymmetry demanded by τ_1. Since 7.5 ms of the 8.0-ms step length is the minimum time required for the recharging of C_1, C_2 would be disconnected from the charging source for over 90% of the cycle. Some improvement could be realized by reducing the series resistances contributing to τ_1, but this results in increased steady-state power drain on the voltage supply. Increasing the step length would improve the charge-transfer situation, but the excessive droop would contribute increased output error. Thus the charge transfer mechanism of this circuit is either too slow or too power consuming to be suitable for use as a miniaturized reference source.

APPENDIX II

TRANSISTOR PARAMETERS

Q	Type*	V_{CBO}	I_{CO} (μa)		h_{FE}			r_e	r_b	r_c (MΩ)		
			typ	max	min	typ	max			min	typ	max
2N1036	PNP	50	.005	1.0	34	60	88			-	.89	1.02
2N338	NPN	45	.002	1.0	45	80	150	33	2K	1	10	-
2N793	NPN	45	.002	2.0	78	-	330	49	740	.83	2	-

* All silicon transistors.

2N492 Unijunction

V_{BB} = 60 volts max.

I_E = 2 amp peak

I_{EO} = .03 μa typ.
12 μa max.

I_p = 4 μa typ.
12 μa max.

η = .56 min
.62 typ.
.68 max.

R_{BB} = 6.2 K min
7.5 K typ.
9.1 K max.

V_v = 1.2 volts min.
2.2 volts typ.
3.9 volts max.

APPENDIX III

EXPERIMENTAL DETERMINATION OF THE TEMPERATURE COEFFICIENTS OF LARGE ELECTROLYTIC CAPACITORS

Matching of the temperature coefficients of C_c and C_e (C_5 and C_6 in Fig. 49) is an experimental procedure calling for accurate measurements. The capacitors in question have large nominal capacitance values, low working voltages, and small temperature coefficients (capacitance variation is typically $\pm$ 2% over the range of interest), which all compound the measurement problem. As a result, the shortcomings of the available methods of capacitance measurement are briefly described and a simple, accurate alternative is proposed. While the capacitance range from 0.5 to 10 μfd is of principal interest, the technique is applicable and often more accurate in other ranges where the more common techniques can also be employed.

The so-called common techniques include direct capacitance-meter measurements and indirect resonance and bridge measurements. The direct-reading capacity meter, a Heathkit CM-1, has a maximum capacity limitation of 0.1 μfd. The sensitivity at this range is such that deviations of 1% can be detected, although not measured accurately, thus precluding the possibility of using series combinations of capacitors to extend the range. Resonance techniques suffer from an analogous accuracy limitation in that frequency changes of the order of 1% can only be detected - not measured accurately.

The bridge technique available employs a General Radio Type 740 Capacitance Test Bridge. Although somewhat more accurate than the previous techniques and useful to 100 μfd, it has the incredible property of applying 90 volts a-c

across the unknown capacitor. If the unknown is an electrolytic, as most capacitors of manageable size in this range are, then a d-c bias voltage of at least 45 volts must be applied in series with the a-c signal voltage. Hence, peak voltages across the capacitor will always exceed 130 volts. This precludes measurement of capacitors with lower breakdown ratings, which includes those of manageable size.

To provide a more satisfactory method, it was felt that means should be investigated of measuring the time in which the unknown capacitor charged through a known impedance to a voltage less than its rated breakdown. The necessary switching involved could be adequately handled by circuits of the multivibrator class. The conventional two-stage astable (free running) multivibrator, however, uses two timing capacitors so that the inherent accuracy is limited to the degree which the asymmetry can be measured (presumably) on an oscilloscope. The multivibrator configuration employing a single active stage (Unijunction transistor), on the other hand, derives its timing sequence from the charging and discharging of a single capacitor. This circuit is shown as Fig. III-1 where Q_1 is the Unijunction Transistor and C is the capacitor to be measured. The operation of the Unijunction is adequately described elsewhere.[4,5] Q_2 has been added simply for the convenience of having a large output voltage swing. The base-emitter terminals could very well have been replaced with a diode and the square-wave output taken from the base-two terminal of Q_1.

When voltages are applied, base current flows through R_3, saturating Q_2. C then charges through R_2 toward voltage E_2 as given by:

$$V_c = V_{ab} = E_2 (1 - e^{-t/R_2C}) \qquad \text{(III-1)}$$

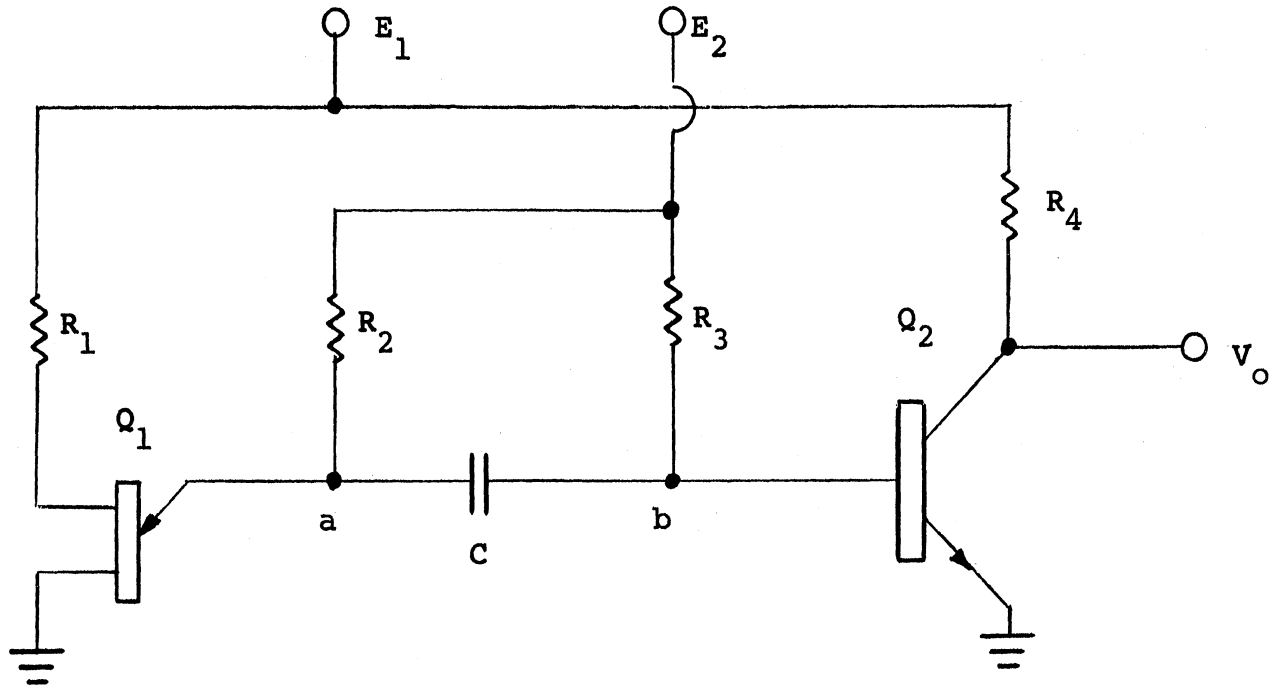


Fig. III-1. Capacitor Test Circuit.

If the exponential is replaced by its Taylor series expansion, then Eq. (1) becomes:

$$V_c = E_2 \left[\frac{t}{R_2C} - \frac{1}{2!}\left(\frac{t}{R_2C}\right)^2 + \cdots \right] \qquad \text{(III-2)}$$

If R_2C is made much larger than t, then Eq. (2) can be approximated as:

$$V_c = E_2 \frac{t}{R_2C} \qquad \text{(III-3)}$$

The charging sequence is terminated when V_c reaches the firing voltage of the Unijunction (called the peak voltage and designated V_p). Thus, Eq. (3) can be solved for the charging time t_c:

$$t_c = \frac{V_p}{E_2} R_2C \qquad \text{(III-4)}$$

Similarly on the discharge cycle, the current path is through R_3 and V_c can be written:

$$V_c = V_{ba} = + (E_2 + V_p) \frac{t}{R_3 C} \qquad \text{(III-5)}$$

This discharge sequence is terminated when V_c given by Eq. (5) reaches the cutoff voltage of the Unijunction (called the valley voltage and designated V_v). Thus Eq. (5) yields the discharge time:

$$t_D = \frac{V_v}{E_2 + V_p} R_3 C \qquad \text{(III-6)}$$

Equations (1) through (4) can be modified for the residual voltage, V_p, remaining on C after the discharge cycle. Thus Eq. (4) becomes:

$$t_c = \frac{V_p}{E_2 - V_v} R_2 C \qquad \text{(III-7)}$$

The frequency of the output square-wave thus becomes:

$$f = \frac{1}{t_c} + \frac{1}{t_D}$$

$$= \frac{1}{C} \left(\frac{\frac{1}{V_p R_2}}{E_2 - V_v} + \frac{\frac{1}{V_v R_3}}{E_2 + V_p} \right)$$

$$= \frac{K}{C} \qquad \text{(III-8)}$$

Therefore, the output frequency is inversely proportional to the capacitance C,

within the accuracy of the approximation made in Eq. (3). The degree of approximation can be seen from Eqs. (6) and (7) to be:

$$\frac{t_D}{R_3C} = \frac{V_v}{E_2 + V_p} \qquad \text{(III-6)}$$

and

$$\frac{t_c}{R_2C} = \frac{V_p}{E_2 - V_v} \qquad \text{(III-7)}$$

Thus V_v, V_p, and E_2 are to be selected so as to minimize the terms of Eqs. (6) and (7). Since V_v and V_p are fractions of E_1, this is equivalent to a selection of E_1 and E_2. Obviously E_1 is to be made as small as practical and conversely for E_2. For $V_p = 4.5 (E_1 = 7.5)$ and $E_2 = 300$, t_c was measured at 12.5 ms so that:

$$\frac{t}{R_2C} = \frac{12.5 \text{ ms}}{(1.8)\ (5.6)} = 1.22 \times 10^{-3}$$

for an error of 0.12% by neglecting all terms of Eq. (2) after the first.

Table III-1 lists the component values used in an experimental determination of the temperature coefficients of several Texas Instruments', SCM series, tantalum electrolytic capacitors. The capacitors were placed in an environmental oven and connected to the measuring circuit by a one-foot length of shielded cable. Figure III-2 shows the experimental results, which verify both the above theory as well as the manufacturer's data for the capacitors. The results are relative to the room temperature (25°C) capacitance value. Absolute measurements are possible, but of course require calibration of the circuit with a known standard.

A Hewlett-Packard Electronic Counter, Model 523B, was used for the frequency

measurements. This instrument displays frequencies less than 100 cps to three significant digits with an accuracy of $\pm$ 1 count. Period measurements can also be made to improve accuracy. The manufacturer claims that the possible error using automatically averaged period measurements does not exceed 0.006% at these frequencies.

TABLE III-1

CAPACITOR TEST-CIRCUIT COMPONENT VALUES

	R (Ω)	Q	V (vdc)
1	330	2N492	7.5
2	1.8 M	2N338	300
3	1.8 M		
4	10 K		

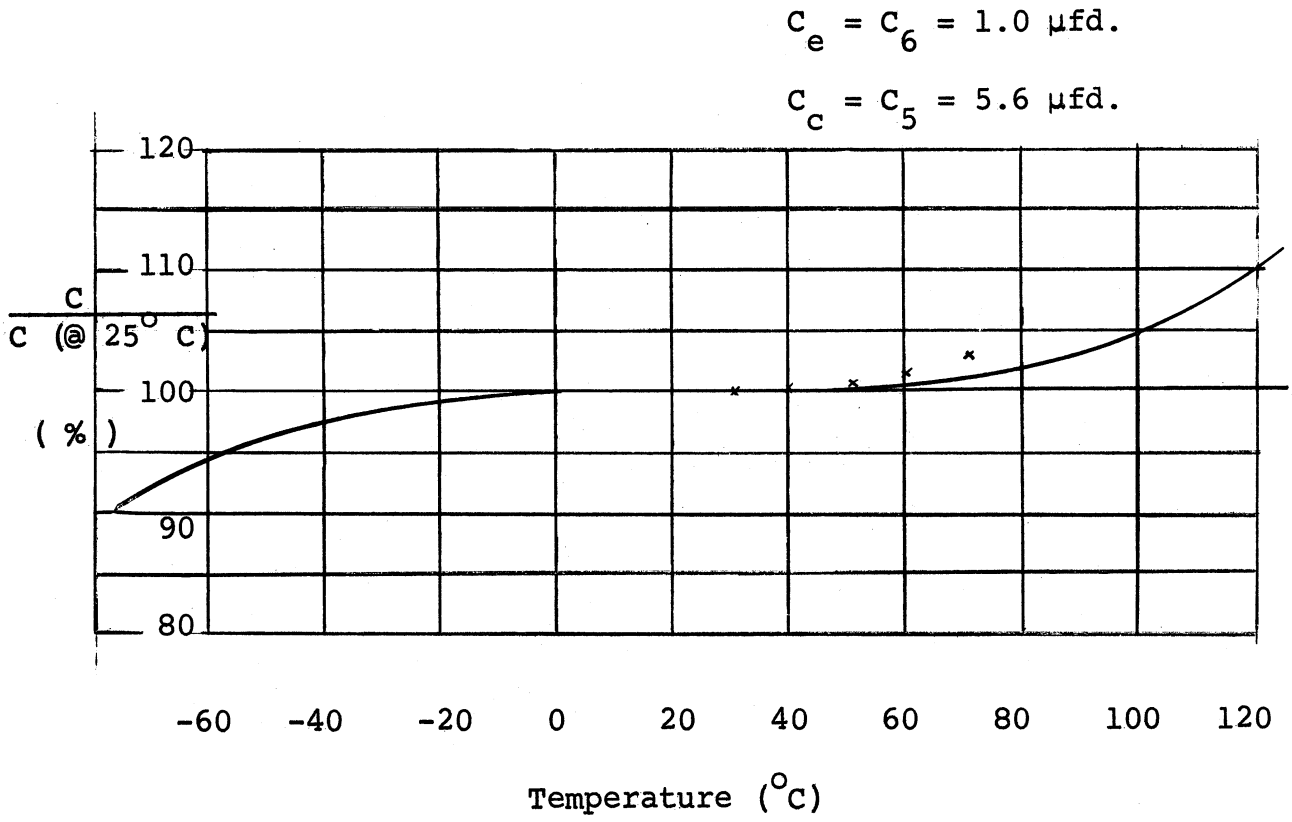


Fig. III-2. Temperature Characteristic of Texas Instruments' SCM Series Tantalum Electrolytic Capacitors.

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