ERRATA

Page

vi Figure 3.5(b) caption: "π/T" should read "τ/T."

74 Figure 3.20, bottom curve: "K=10DB" should read "K=-10DB."

83 Figure 3.27, drawings on right side: "G( )=..." should read "G(ω)=...," two places.

84 line 12: "...automatic-phase control..." should read "...automatic phase-control...."

137 line 6: "If in" should read "If an."

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PRECISE FREQUENCY SYNTHESIS USING NONPRECISE TUNING COMPONENTS

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ABSTRACT

This dissertation treats the effective utilization of non-precise tuning components in unique techniques for precise frequency synthesis. Frequency synthesis is the generation of sinusoidal RF signals of precisely-controlled and accurately-known arbitrary frequencies.

Nonprecise components which are examined in detail under the several limiting conditions of operation are solid-state devices, such as variable capacitance diodes, ferroelectric capacitors, and controllable inductors.

The significance of combining a discrete-frequency reference and an electronically-tuned phase-lock oscillator in the generation of precise frequencies is that it is possible to construct a unit whose output frequency can have certain discrete values.

This unit, called a discrete-frequency generator, has an output frequency which is precisely one of the harmonics of the discrete-frequency reference. By using several discrete-frequency generators, each with different incremental steps, combining, and taking the mixed output, it is possible to cover a wide over-all range in small incremental steps.

The design and construction of a discrete-frequency synthesizer which tunes over a 1-Mc range in 10-kc steps (two significant figures) is carried out to demonstrate the practicability of the proposed technique. The discrete-frequency reference is provided by a five-stage shift-register generator. The shift-register generator is synchronized by a crystal clock which has a long-term frequency stability of one part in 10^5. The spurious output of the synthesizer is at least 55 db below the desired output.

The significant consequences of this investigation result from the extreme flexibility afforded by completely electronic tuning methods. The incorporation of the nonprecise components through the use of phase-lock circuitry has made it possible to develop a technique of frequency synthesis which permits the rapid selection of precise frequencies, is adaptable to remote control, may be readily programmed, and theoretically is unlimited in frequency range of operation.

CHAPTER I

INTRODUCTION

1.1 Statement of the Problem

Frequency synthesis is the generation of sinusoidal RF signals of precisely-controlled and accurately-known arbitrary frequencies. This study treats the effective utilization of nonprecise tuning components in unique techniques for precise frequency synthesis.

Nonprecise components which are examined in detail under the several limiting conditions of operation are solid-state devices such as variable capacitance diodes, ferroelectric capacitors, and controllable inductors.

The significant consequences of this investigation result from the extreme flexibility afforded by completely electronic tuning methods. The incorporation of the nonprecise components through the use of phase-lock circuitry has made it possible to develop a technique of frequency synthesis which permits the rapid selection of precise frequencies, is adaptable to both remote control and electronic programming using analog or digital methods, and theoretically is unlimited in frequency range of operation.

This paper is divided into five chapters. The statement of the problem and a discussion of current techniques for providing precisely-controlled frequencies are presented in Chapter I.

A study of various electronic tuning methods using solid-state devices is carried out in Chapter II. This study formulates basic decisions regarding the limitations of tuning elements and voltage-controlled oscillator circuit parameters.

The system concept of a generalized discrete frequency synthesizer is presented in Chapter III. The significant contribution of combining a discrete frequency reference and an electronically-tuned phase-lock oscillator in the generation of precise frequencies is that it is possible to construct a unit whose output frequency can have certain discrete values. This unit, called a discrete-frequency generator, has an output frequency which is precisely one of the harmonics of the discrete-frequency reference. By using several discrete-frequency generators, each with different incremental steps, combining and taking the mixed output, it is possible to cover a wide over-all range in small incremental steps. The question of how to minimize for a given power spectrum the peak-to-peak amplitude of a signal is presented. A term peak factor is defined and a relationship which can be effectively used as a figure of merit in the design of an appropriate frequency spectrum is developed. In addition, a study and evaluation of various methods for the efficient production of high-order harmonics with balanced energy in the frequency band of interest is carried out.

Of the various methods presented for generating a discrete-frequency reference, the shift register generator method is particularly interesting. The digitally-generated linear maximal sequence fulfills the condition of minimum peak factor while providing a reasonably uniform amplitude spectrum over a given band of interest. From a practical point of view, the shift register generator is simple to implement. Logic modules can be taken off the shelf and put together to form a discrete frequency reference. In addition, by using clock dividers and coincidence gates in conjunction with the shift register generator, it is possible to obtain any number of discrete frequency references

each with different incremental steps.

Also in Chapter III an analysis of the problem of combining two signal frequencies to obtain a single signal frequency in the form of their sum or difference while using phase-lock oscillators of a practical design is carried out.

Many authors have attempted to describe the various performance characteristics of the phase-lock oscillator loop but no one of these has treated the aspect in a manner sufficiently complete for the present purposes. Therefore, the basic operating principles of a phase-lock loop are presented and analyses are made in instances where the literature is not complete. For example, an analysis is carried out to determine frequency sensitivity, loading effects, and other characteristics of voltage variable capacitors when used as the tuning element in an oscillator tank circuit. Based on this analysis a figure of merit is developed which is defined as the product of the frequency sensitivity S and the Q of the oscillator tank circuit. In addition, equations for the convergence time of a phase-lock oscillator loop are developed.

In Chapter IV the design, construction, and testing of a two-digit synthesizer are carried out to demonstrate the practicability of the system.

Chapter V is devoted to a summary and conclusions. Suggestions for further research are presented and specific applications in which the proposed technique for precise frequency synthesis would be particularly useful are given.

1.2 Survey of Other Methods of Precision Frequency Synthesis

The development of frequency control circuits will be traced briefly and the technical forces causing their evolution will be discussed.

1.2.1 Tunable LC Oscillator. The simple tunable LC oscillator was a practical way of generating channel frequencies when crowding of the spectrum was not a problem and frequency inaccuracies could be tolerated.

1.2.2 Crystal Oscillator. Crowding of the spectrum necessitated closer channel spacing and increased frequency accuracy. The increased frequency accuracy was provided by the crystal oscillator.

1.2.3 Multiple Crystal Frequency Synthesizer. As it became apparent in multi-channel equipment design that a choice of one of hundreds of channels was required, the multiple crystal synthesizer was developed (Ref. 1). The principle is illustrated in Fig. 1.1. The

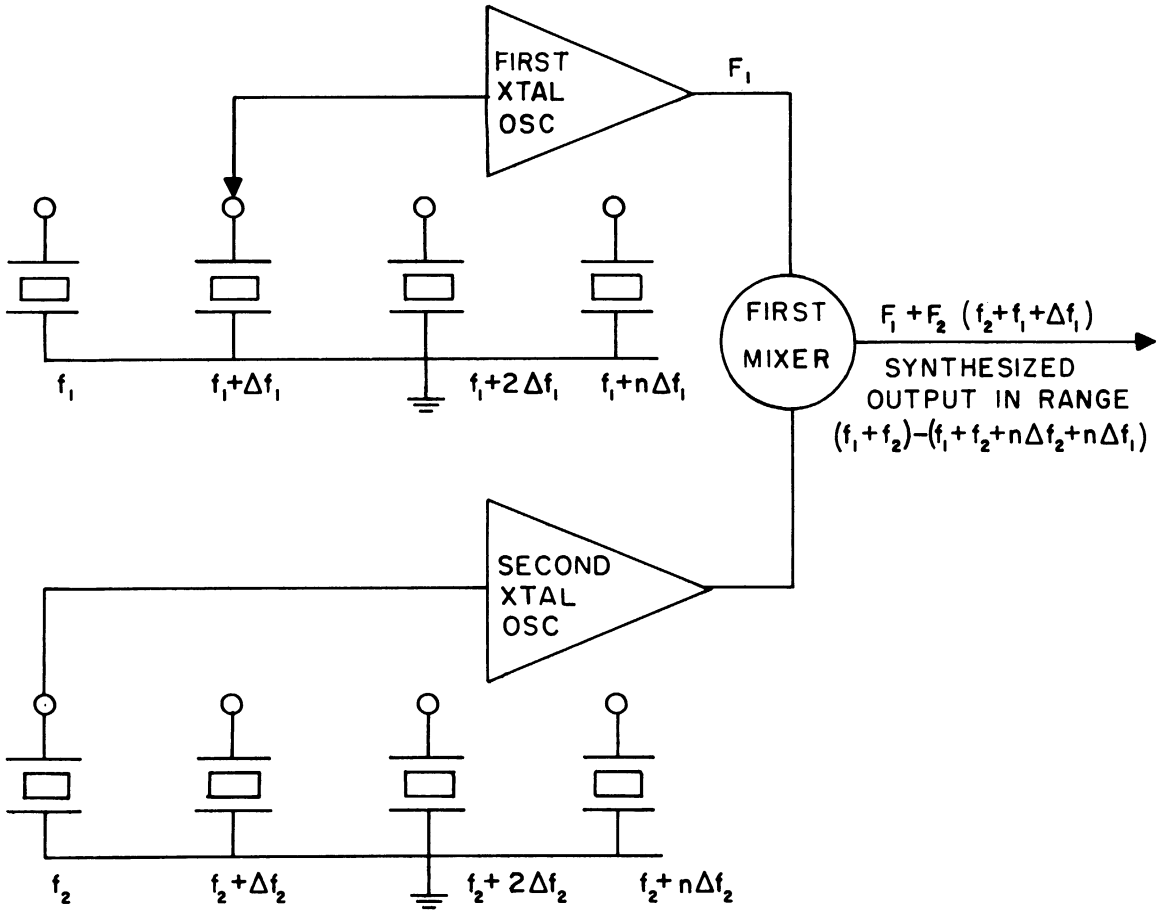


Fig. 1.1. Block diagram of a multiple crystal frequency synthesizer.

frequencies of several crystal oscillators were mixed to produce the desired output frequencies. Each oscillator was provided a means of selecting one of ten or more crystals so that a large number of channel frequencies could be synthesized.

1.2.4 Single Crystal Frequency Synthesizer. To accommodate additional channels the channel spacing was reduced. This, however, necessitated maintaining channel frequencies within a tolerance as small as $\pm\frac{1}{2}$ part per million. A system proposed by H. J. Finden (Ref. 2) retains the advantages of the multiple crystal synthesizer but eliminates the problem of maintaining a large number of crystals to the same accuracy. The accuracy and stability of the output signal are esentially equal to that of the reference oscillator. The principle is illustrated in Fig. 1.2.

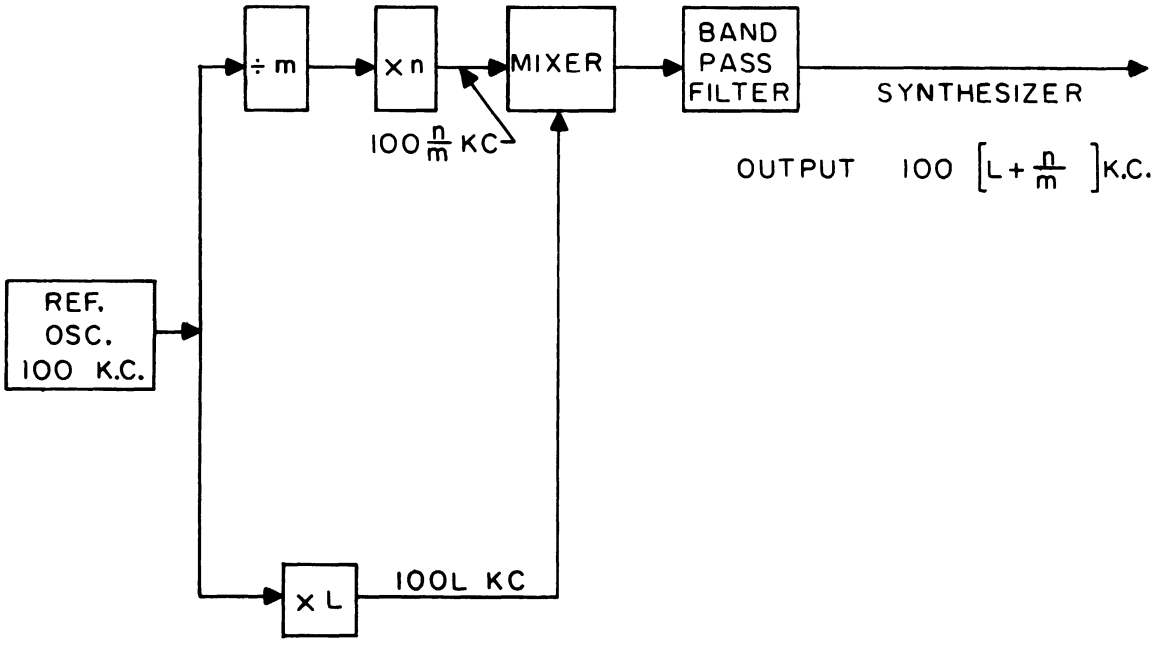


Fig. 1.2. Block diagram of a single crystal frequency synthesizer.

Basically, the single crystal frequency synthesizer is a circuit in which harmonics and subharmonics of a single standard reference oscillator are combined to form a multiplicity of output signals which are all harmonically related to a subharmonic of the standard reference oscillator.

1.3 Stabilized Master Oscillator Frequency Synthesizer

1.3.1 Servo System. A system proposed by E. W. Pappenfus (Ref. 3) and G. J. Camfield (Ref. 4) uses an indirect technique in which the output frequencies are obtained from a variable oscillator, which in turn is controlled by reference crystal oscillators. The principle is illustrated in Fig. 1.3. The control is both mechanical

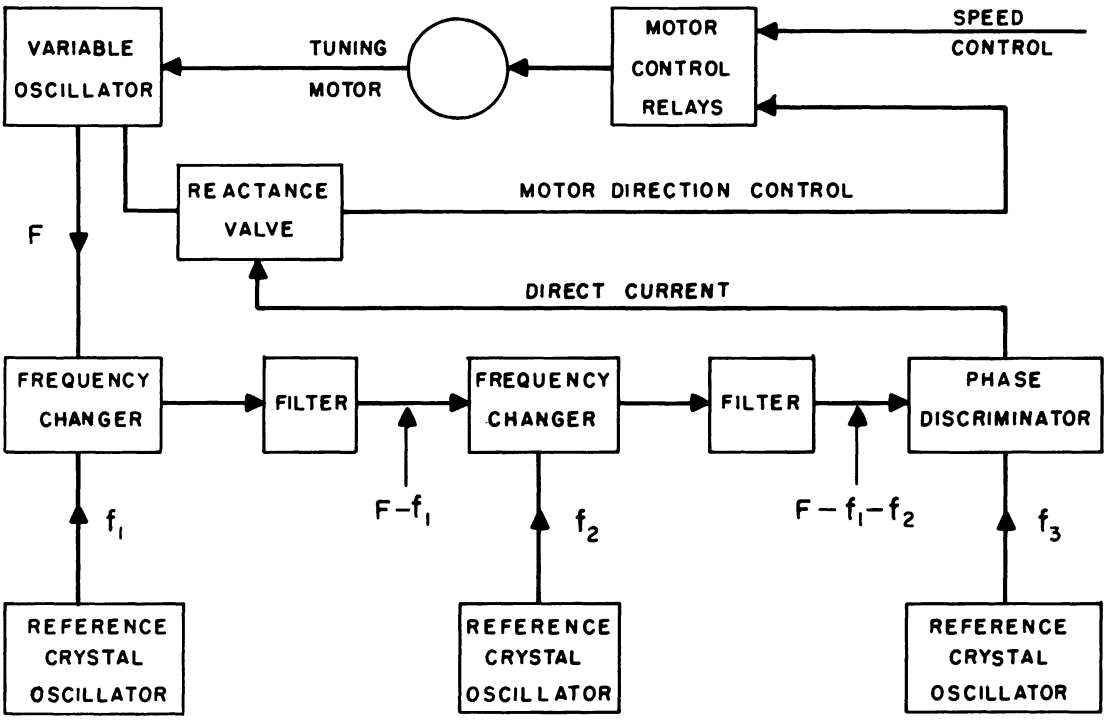


Fig. 1.3. Block diagram of a stabilized master oscillator frequency synthesizer.
(Servo System)

by means of a tuning motor and electronic by means of a reactance tube. The frequency F_1 of the variable oscillator is varied until the output from the second filter reaches the frequency f_3, at which time the phase discriminator operates and the tuning motor automatically stops. When the motor stops, $F = f_1 + f_2 + f_3$. F may be changed by altering any of the reference crystals. If the system used twenty crystals in two groups of ten each to control the first two reference oscillators (so that f_1 and f_2 could each have any one of ten values), then F could have any one of a hundred values. Admittedly, if ten harmonics of a single crystal-oscillator had been used for each group a hundred frequencies for only two crystals could be obtained. It was felt, however, that high-order harmonic selection involves the use of precision circuits which must be maintained accurately on tune and which may offer the possibility of being tuned to an incorrect harmonic. In addition, a unit comprising one crystal plus harmonic-selection circuits tends, if anything, to be larger and to require more power than a unit using a number of crystals. For the system to operate satisfactorily, the open loop set-on accuracy of the master oscillator must be within ±5 kc. This is accomplished by constructing a very stable mechanically-tuned oscillator with a reactance tube in the tank circuit for lock-on purposes when the oscillator is brought within the ±5 kc limitation. The stability of the system described above depends upon the stability of the frequencies used at the translating mixers.

1.3.2 Sampled Data System. A system proposed by N. G. Alexakis (Ref. 5) uses an entirely different principle, i.e., a preset frequency counter, to tune and stabilize a master oscillator. The

basic elements as shown in the block diagram of Fig. 1.4 are a voltage-

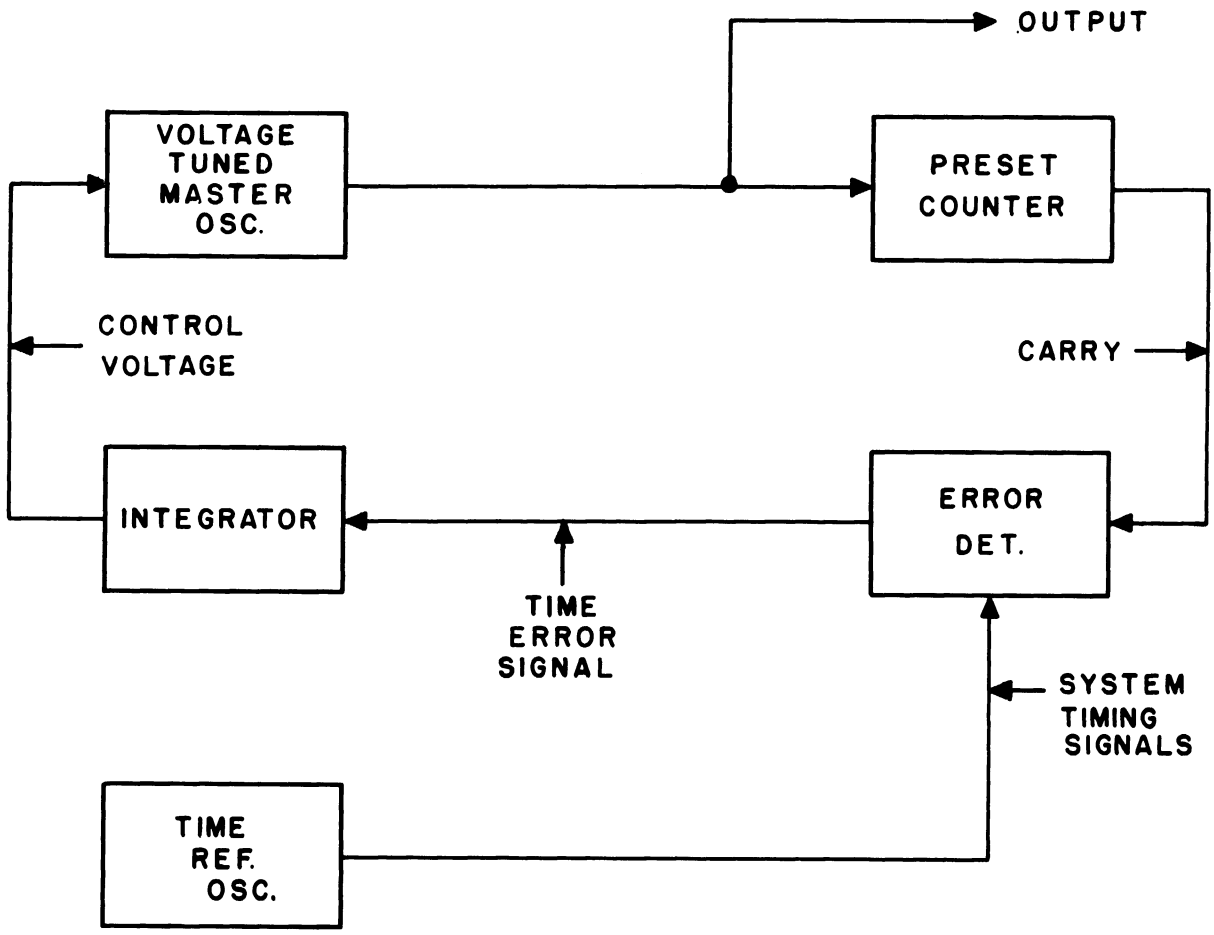


Fig. 1.4. Block diagram of a stabilized master oscillator frequency synthesizer.
(Sampled Data System)

controlled oscillator, preset counter, timing signal and error detector.

The fixed reference time interval is compared with the variable interval required by the counter. If the variable time is less than the one-second fixed interval, then the master oscillator frequency is too high. If the variable time is greater than the reference interval, the master oscillator frequency is too low. The error signal thus developed is a constant-amplitude pulse of varying duration and either

positive or negative polarity. The voltage-controlled master oscillator requires a proper dc voltage to reduce the error to zero. This voltage is derived from the time-varying error signal by an integrating circuit.

1.4 The Status of Current Work--Summary

As indicated in previous sections, several direct approaches to frequency synthesizers have been made. Using multiple decks of crystals and mixing the outputs of several crystal oscillators is one method.

A second method uses only one crystal oscillator of high precision which is fed to multiplier-divider chains and harmonic generators. The desired harmonic in each decade bank is selected by mechanically-tuned high Q filters, and the outputs of the various filters are suitably mixed to furnish the desired output frequency.

A further refinement in this area is the use of a variable frequency master oscillator to obtain the desired frequency. The master oscillator is in turn controlled by reference to crystal oscillators. The control in this case is both mechanical and electronic.

The final system described which uses a voltage-controlled oscillator and a preset counter to obtain the desired frequency output has much to recommend it since it is a straightforward and quite simple technique.

The significant consequences of the proposed technique result from the extreme flexibility afforded by completely electronic tuning methods. The incorporation of the nonprecise components through the use of phase-lock circuitry has made it possible to develop a technique of frequency synthesis which permits the rapid selection of

precise frequencies and is adaptable to both remote control and electronic programming, using analog or digital methods. Theoretically, this technique is unlimited in frequency range of operation.

CHAPTER II

HISTORICAL BACKGROUND ON THE STUDY OF ELECTRONIC TUNING METHODS USING SOLID-STATE DEVICES

2.1 Electronic Tuning

Electronic frequency control is flexible, versatile, and in many instances essential where fast frequency selection and low tuning power are required. During the past few years, two methods of electronic tuning using solid-state elements have evolved:

(1) Magnetic tuning which uses the principle that the inductance in a resonance circuit may be varied by means of a magnetic bias field, and

(2) Electric tuning which uses the principle that the capacitance of the resonant circuit may be varied by an electric bias field.

The ideal tuning element for frequency synthesis applications, whether it uses the principle of magnetic or electric tuning, should have the following characteristics:

(1) RF loss is negligibly small.

(2) Tuning capabilities should extend to at least 1000 megacycles with little change in Q.

(3) The temperature coefficient of frequency should be zero from minus 50 degrees centigrade to plus 100 degrees centigrade.

(4) Frequency ratios should be at least 10 to 1 with relatively small control power. In

addition, the operating frequency should extend to 1000 megacycles with this ratio.

(5) Frequency selection should be rapid, using step or continuous control.

(6) Tuning elements should be small, compact and capable of large scale manufacture with only a small fraction of rejects.

(7) Isolation of controlled and controlling signals should be possible.

Since this ideal does not exist and it is unlikely that it will be developed within the next few years, the present choice for a particular tuning method and tuning element must be a compromise to obtain a close approach to the ideal in those properties most important for a specific application.

2.2 Magnetic Tuning

During the past fifty years, attempts have been made to construct controllable inductors without moving parts and cover as much of the frequency spectrum as possible at a reasonable expense of control power. A controllable inductor is a device comprising a number of windings. Some of these windings carry alternating current; others, carrying direct or slowly varying current, are used to determine the magnetic state of the core and thus to control the alternating current in the winding first mentioned. The usefulness of these earlier results was limited to very low radio frequencies. Although the laminated core technique used at that time was considerably improved by the use of nickel-iron alloys and etching processes to reduce the lamination thickness, difficult production methods and low Q's prevented any

significant use of these tuning units. From 1930 to 1945 attempts were made to develop an RF tuning element using powdered iron materials. Those efforts did not produce units which could be called practical. A representative example was developed by W. J. Polydorff (Ref. 6) in 1944. The unit described produced a change of inductance of approximately 4 to 1 and had a Q of 50 in the frequency range of 200 to 400 kilocycles with a control power requirement of 25 watts. The weight of the unit was in excess of 25 pounds.

Since 1945, a new class of magnetic core materials called ferrites has been developed (Ref. 7). These materials, which have a wide variation of permeability with applied field, have enjoyed prominence in the magnetic tuning field because of their high resistivity and freedom from eddy-current losses at high frequency. Fig. 2.1 shows a schematic representation of a controllable inductor having one signal winding and two control windings. The signal winding is drawn in two sections, shown orthogonal to the control winding, to indicate that inductive coupling between the control and signal windings

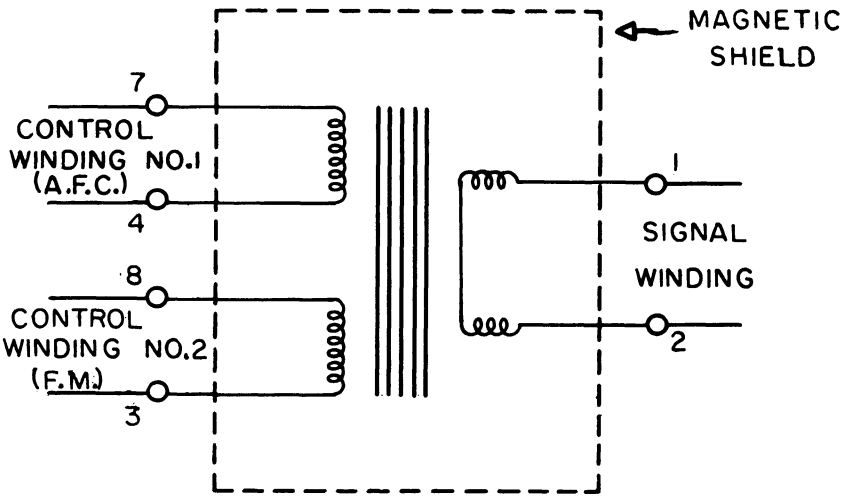


Fig. 2.1. Schematic diagram of a typical controllable inductor.

has been cancelled. A magnetic shield surrounds the ensemble to prevent stray fields from influencing its behavior.

Ferrites used as magnetic core materials consist of oxides of metals and are formed at high temperatures. All materials that exhibit ferromagnetism are paramagnetic when heated above the Curie temperature.[1] Permeability (μ) of a magnetic material is defined as the ratio of B/H where B is the flux density in lines per square centimeter (gauss) and H the magnetizing force in gilberts per centimeter (oersteds). The permeability of the magnetic material is low at low flux density, maximum at some moderate flux density, and quite small when the core is saturated. The permeability at low magnetizing force (the limit as B and H approach zero) is called the initial permeability (μ_o).

In addition to the previous terms there is another term called incremental permeability (μ_Δ) which is a function of ΔH and H_o. The magnetic quantities involved are shown in Fig. 2.2. The dotted

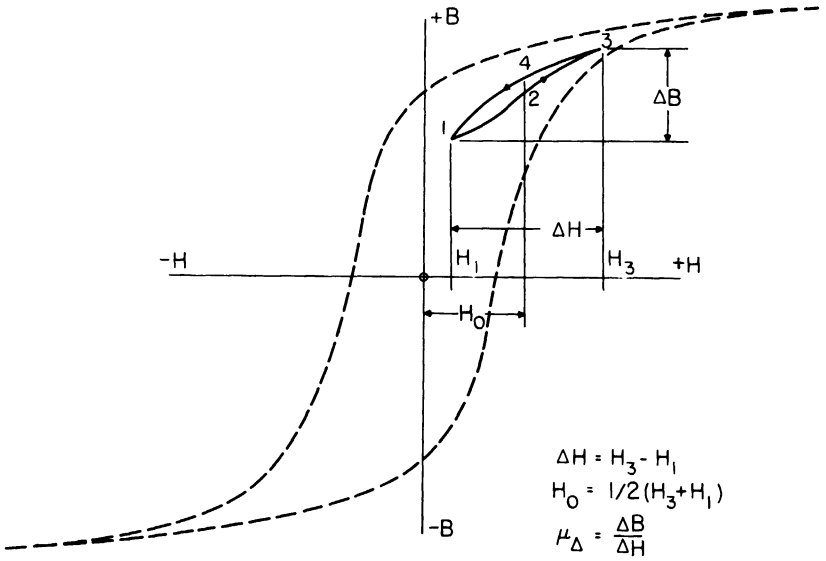


Fig. 2.2. Definitions of magnetic parameters.

[1]Curie temperature--point below which the material ceases to be paramagnetic.

curve represents a B/H or hysteresis loop for some magnetic material. The solid curve shows the change in magnetic flux density B under the influence of a small cyclical variation in magnetic field. Although B is a double-valued function of H, it is possible to define incremental permeability as $\mu_\Delta = \Delta B/\Delta H$ as the material is cycled around the path 1-2-3-4-1. H_o is the mean value or dc component of the magnetic field. Incremental permeability is also defined as the permeability offered to an ac magnetizing force superimposed on a dc magnetizing force. In describing a ferrite material we must know its history, H_o, ΔH and the frequency of operation. The initial permeability μ_o for very small or zero flux densities is an inherent property of the material under consideration. For various ferrite materials in which we are interested the μ_o lies between 2 and 1500. The incremental permeability (μ_Δ) of a ferrite material decreases monotonically with increasing H_o for a constant ΔH. The maximum theoretical change in permeability is μ_o/μ_c where μ_c is the permeability at saturation. Since μ_c approaches unity, the maximum change in inductance is proportional to μ_o. The maximum change in frequency we can expect due to the permeability change is

$$\sqrt{\frac{f_{max}}{f_{min}}} = \mu_o$$

From a practical point of view the hysteresis effect simply means that if the control current is raised from zero to a given value, one signal inductance is obtained. If the same control current value is approached from a high current setting, a different value of signal inductance will occur.

Magnetic tuning units are now being produced with very good stability. By a suitable choice of core material there is generally a value of control current for which the temperature coefficient over a broad temperature range is substantially zero, with coefficients of opposite sign on either side of this current setting. Signal winding coefficients of 0.5%/°C are encountered, although more typical values are 0.1% to 0.2%.

At frequencies up to 10 megacycles, inductance change ratios in the hundreds are feasible. Typical units designed for applications between 10 and 50 megacycles have ratios in the order of 30 to 100. In the 50 to 100 megacycles range, this drops to between 3 and 6; and above 100 megacycles to less than 2. The curve of Fig. 2.3 shows the

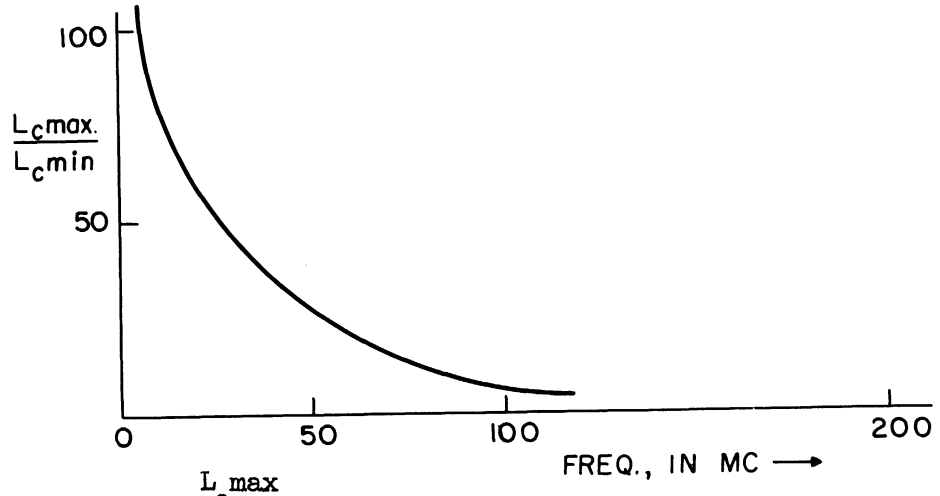


Fig. 2.3. $\frac{L_c max}{L_c min}$ of typical magnetic tuning unit vs. frequency.

ratio of maximum to minimum inductance plotted versus frequency.

Representative Q values are in the low hundreds for frequencies up to several megacycles. They range between 40 and 100 for frequencies up to 50 megacycles, dropping to between 10 and 50 at 100 megacycles and perhaps 5 to 10 at 200 megacycles. The curve of

Fig. 2.4 shows the typical values of Q plotted versus frequency.

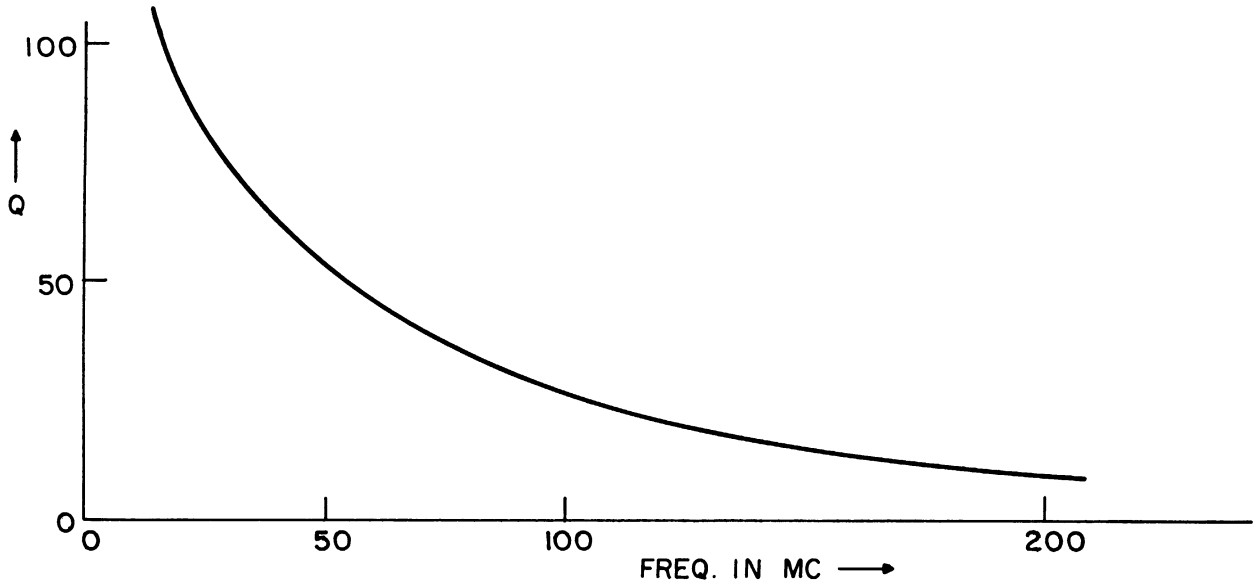
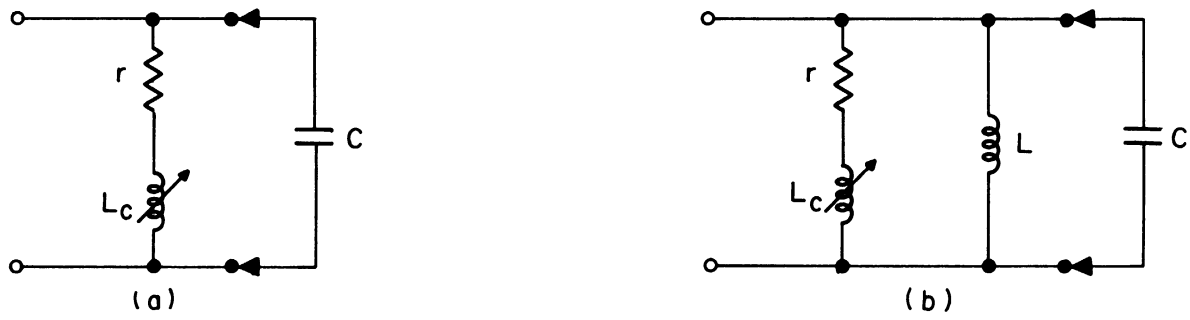


Fig. 2.4. Q of typical magnetic tuning units vs. frequency.

Figure 2.5a illustrates the basic circuit for application of



L_c = controllable inductance
r = loss associated with controllable inductance
L = loss free inductance
C = total capacitance in tank circuit

Fig. 2.5. Basic circuit for application of a controllable inductance L_c in a tuned circuit.

a controllable inductance in a typical tank circuit. It may frequently be true that the tuning ratio (TR) may be greater than necessary but the circuit Q may be unacceptable due to inherent losses in the controllable inductance. Fig. 2.5b depicts a method of increasing the tuned circuit Q by including a small loss-free coil in shunt with the controllable inductance.

$$Q_{coil} = \frac{\omega L_c}{r} \tag{2.1}$$

$$TR_{coil} = \frac{L_c max}{L_c min} \tag{2.2}$$

The Q of the controllable inductance with the loss-free coil in shunt is

$$Q_{circuit} = Q_{coil} \left[\frac{L_c + L}{L}\right] \tag{2.3}$$

while the tuning ratio becomes

$$TR_{circuit} = TR_{coil} \left[\frac{L_c min + L}{L_c max + L}\right]^{\frac{1}{2}} \tag{2.4}$$

If $L >> L_c$ then the frequency range will be determined by the available inductance range of the controllable inductance. However, if $L_c >> L$ then a definite gain in Q may be achieved only through a loss in effective inductance variation range.

The control power required to obtain the full inductance variation of low level units is approximately 1 watt. Some commercially available inductors, however, have been made to operate at a level of about 0.1 watt. The control power is interrelated with the required

$\frac{L_{c\,max}}{L_{c\,min}}$ ratio and frequency and will vary somewhat. The relationship between control current and signal inductance is nonlinear, the percentage change in inductance per unit control current being greatest for small control current values. Since this is undesirable, appropriate compensation circuitry has been developed.

Since step frequency control of the proposed synthesizer is envisioned, the problem of furnishing the electronic means for magnetic tuning may become quite difficult. The following typical example serves to illustrate the seriousness of the problem. In the frequency range 1 to 3 Mc, it is desired to step from 1 to 2 Mc in 1 microsecond. The circuit has the following properties:

Control inductance = 3 henries

Required control current shift = 10 ma

Control voltage $e = L \frac{di}{dt} = 3 \times .01 \times 10^6 = 30{,}000$ volts

Peak control power $p = 300$ watts

A voltage of 30,000 volts presents not only a serious problem in control circuit design, especially in transistor circuits, but also in voltage insulation in the design of the control winding itself.

The voltage across the control winding may be reduced at the expense of a larger control current. Since the magnetic field is proportional to the number of ampere turns (NI) and since the inductance of the control winding is proportional to N^2, then by reducing N by a factor 10 the control circuit has the following properties:

Control inductance = .03 henries

Required control current shift = 100 ma

Control voltage = $L \frac{di}{dt}$ = .03 x .1 x 10^6 = 3,000 volts

Peak control power = 300 watts

An improvement is achieved in the voltage across the control winding but at the expense of increased control current. In both cases the power calculation of 300 watts is an instantaneous or peak demand lasting only 1 microsecond.

In conclusion, the study and development of ferrite material has resulted in a controllable inductance having a volume less than one cubic inch, weighing slightly over one ounce, and being capable of tuning a frequency range of 7 to 1 at 1 Mc to 1.5 to 1 at over 200 Mc. Q's of the order of 100 - 10 are obtained over this frequency range and the average temperature coefficient of the elements is below .03%/°C.

2.3 Electric Tuning

Increasing interest in the use of voltage-variable capacitors for electronic frequency control has resulted in the development of two different classes of capacitors:

(a) The ferroelectric capacitor and

(b) The voltage variable diode capacitor.

A clarification of the distinction between the ferroelectric capacitor and the voltage variable diode capacitor appears desirable and will be carried out in the following brief discussion.

2.3.1 Ferroelectric Capacitors. In the past decade there has been a considerable development of a new group of nonlinear dielectric materials called "ferroelectrics." These materials, although the name stems from the Latin word for iron, do not contain appreciable amounts of iron. Rather, the name indicates the close resemblance the mechanism of electrical polarization to that of the magnetization

of ferromagnetic materials discussed under Section 1.1.

Ferroelectricity can be described as a spontaneous polarization. Polarization in dielectric materials may be due to:

(1) Alignment of permanent electric dipoles,

(2) Displacement of the + and - ions relative to one another (e.g., Na^+ and Cl^- in NaCl) or

(3) Displacement, relative to the positive nucleus of the negative charge of the electrons.

Ferroelectricity will occur if any one of these mechanisms, either singly or in combination occurs spontaneously, i.e., without the application of an external electric field. A number of materials exhibit ferroelectricity, but on the whole the phenomenon is rather rare. Ferroelectric materials are always piezoelectric but the converse is not always true, e.g., quartz. Barium titanate ($BaTiO_3$) is, from a practical point of view, the most important ferroelectric and, when mixed with a nonferroelectric buffer material, such as strontium titanate, becomes a suitable material for many practical applications.

In a conventional capacitor a graph of Q vs. V is essentially linear, i.e., a straight line with slope (C) proportional to the dielectric constant (ϵ).

The relationship of these quantities is expressed as

$$Q = CV \tag{2.5}$$

where Q is the charge stored, C is the capacitance and V is the applied voltage.

In a ferroelectric capacitor the plot of charge versus voltage is not a straight line; i.e., it is nonlinear. If a complete

cycle of positive and negative voltages is applied, the result is a hysteresis loop as shown in Fig. 2.6. Although the hysteresis loop

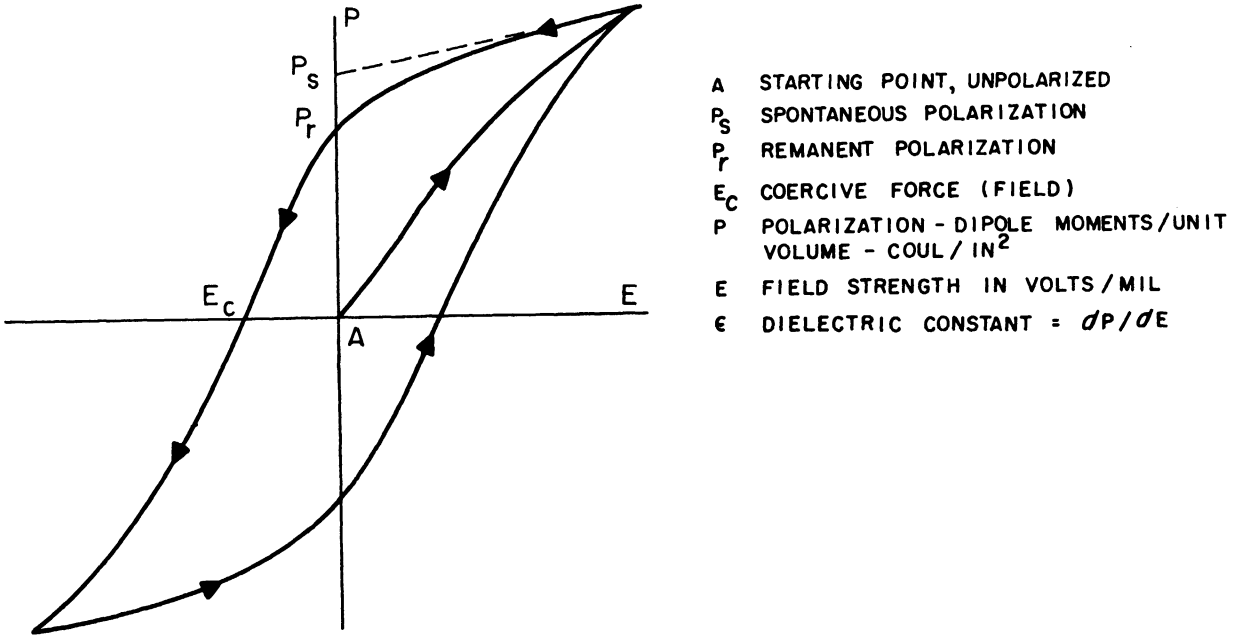


Fig. 2.6. Ferroelectric capacitor hysteresis loop.

is not included in the definition on nonlinearity, it is exhibited by all nonlinear dielectrics and thus may be considered an inherent property.

The hysteresis loop can be explained by considering the behavior of the barium titanate crystal (Ref. 8).

At room temperature this crystal has a tetragonal form which is similar to a distorted cube in which one axis, the "c" axis, is elongated by a spontaneously occurring electric dipole along that direction, while the other two axes, both "a" axes, since they are identical in every respect, are shortened. The dielectric constant along the "a" axes is at least several times greater than that along the "c" axis.

Along the "c" axis the polarization may have two directions, oppositely oriented, which may be called positive and negative. When the voltage along the "c" axis is varied in sign, the dipole flips from one stable position to the other. Since a finite field is necessary to reorient the dipole, there is little change in polarization until a critical field level is reached. A rapid change in crystal polarization occurs when this level is reached, and subsequent increases in field strength produce little further change in polarization. When the field is reversed, this process is repeated, with opposite polarity conditions prevailing.

In the ceramic of which practical capacitors are formed, the barium titanate forms into a multitude of tiny crystallites whose spontaneous dipoles are randomly oriented. Therefore, there is no favored "c" direction, and the statistical average of the elemental orientations cancels to zero. With no biasing electric field applied to the dielectric the observed dielectric constant lies between that characteristic of the "c" direction and that of the "a" directions. It is somewhat closer to the "a" value since "a" axes are more abundant.

Referring to Fig. 2.6 and beginning at point A, there is initially no net polarization before voltage is applied. When a dc bias is applied to the material, some of the dipoles originally oriented randomly will align themselves with the field, and a partial "c" axis is induced perpendicular to the electrode faces. As a consequence, the dielectric constant decreases. As the biasing voltage (applied field) is increased, more and more dipoles are reoriented, and the dielectric constant continues to decrease as the polarization in the new "c" direction increases. This proceeds until a further increase

in bias fails to yield a proportionate increase in polarization. This presumably occurs as a result of the supply of randomly oriented dipoles becoming exhausted.

In the polycrystalline ceramic many of the elemental dipoles are incapable of being oriented perpendicularly to the electrode faces due to their position in the ceramic matrix. At best they can be elastically strained in the direction of the field.

When the field is reduced, these strains relax and some polarization is lost. However, since a large number of dipoles are oriented into a stable condition, they remain so and the charge stored in this manner is not recovered. This makes up the remanent polarization, P_r. When the field is reversed, a certain field strength, E_c, is required to reduce the polarization to zero and further increase in field switches the dipoles to the reverse direction. When the field is again reversed, the plot of polarization versus field duplicates the upper path. It is seen, therefore, that the point A is not traversed again and that the process is not reversible.

The behavior of a given capacitor can be shown graphically since its capacitance is proportional to the dielectric constant, ϵ, which is the slope of the hysteresis loop.

The shape of the loop is affected by the peak field strength applied, temperature and frequency as well as the material of which the dielectric is composed. In general, the sides of the loop become more vertical and the saturation region flattens out with higher peak fields. The dipole switching occurs at a very fast rate. It has been known to follow pulses of the order of 1 microsecond and smaller. The zero bias dielectric constant does fall off somewhat above the region

of about 700 Mc/s, and it is to be expected that the hysteresis loop will change at the higher frequencies.

Another effect described by W. J. Merz (Ref. 9) which may be observed in certain ferroelectric ceramic materials is the double hysteresis loop phenomena. In this case the double hysteresis loop occurs over a rather large temperature range and is caused by a transition from a nonferroelectric state via a shift in the Curie temperature with applied field.

The double hysteresis loop phenomena may be demonstrated very graphically as shown in Fig. 2.7 by means of a butterfly plot (Ref. 10). For convenience, the incremental capacity, which is proportional to the $\epsilon\Delta$ of the sample is plotted against the applied field. From a practical point of view the hysteresis effect means that if the control voltage is raised from zero to a given value, one signal capacitance is obtained. If the same value of control voltage is arrived at from a high voltage setting, a different value of signal capacitance will occur.

Presently available ferroelectric capacitors have relatively poor temperature stability (Ref. 11). There is no value of control voltage that gives a zero temperature coefficient over a wide temperature range as was the case in ferrite tuning. The design of circuits using ferroelectric tuning which must operate over a wide range of ambient temperatures must therefore include temperature control of the capacitors. This is not a serious peoblem, however, because of the very small volume occupied by the capacitors. It is not difficult to build a capacitor tuning unit and a low-watt thermostatically-controlled heater in a miniature oven having a volume of .01 cubic inch.

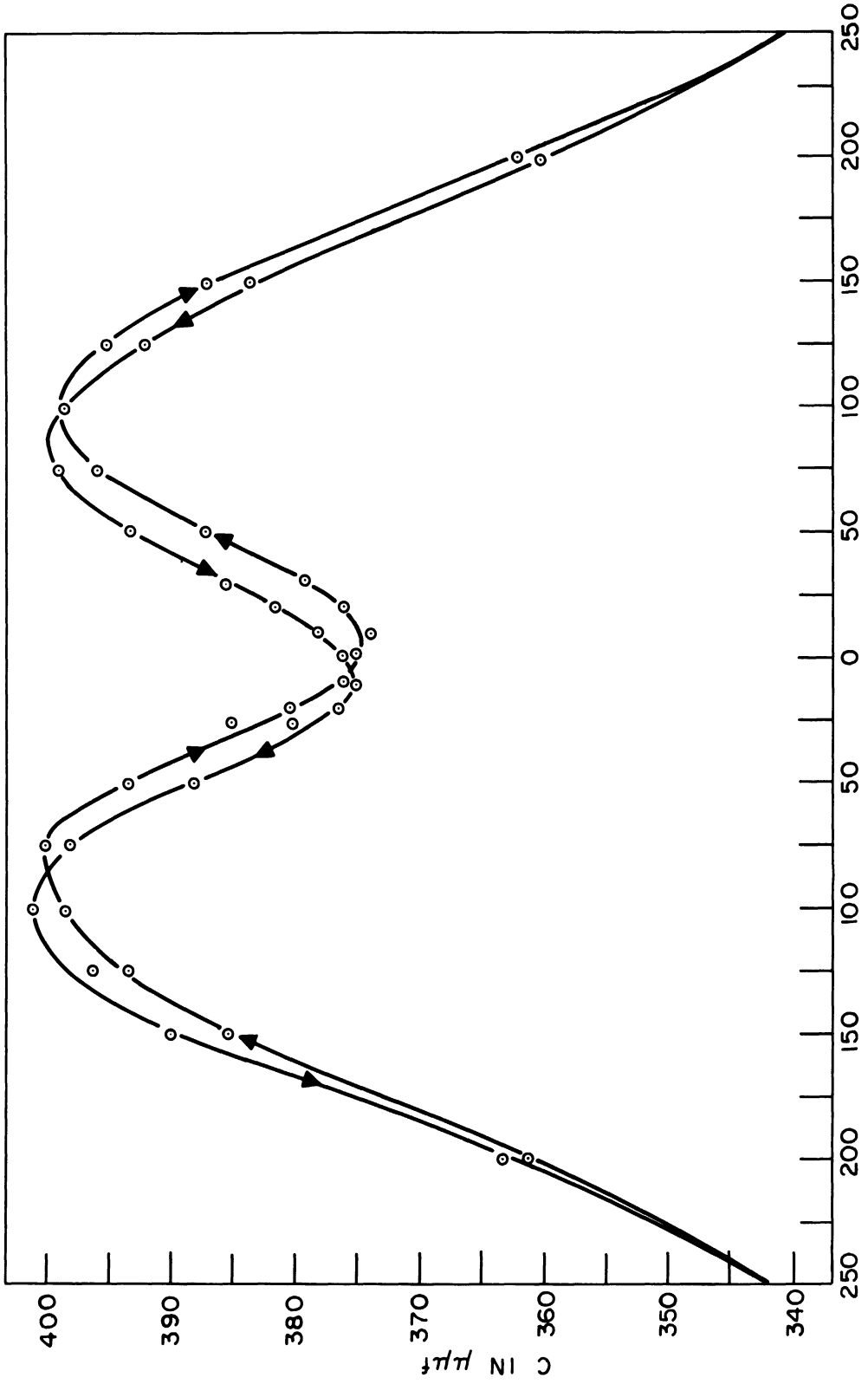


Fig. 2.7. The static capacity-field butterfly loop for a typical ferroelectric ceramic.

Figure 2.8 demonstrates the stability of a typical ferroelectric capacitor with and without the use of the thermostating techniques. The temperature of the environment was varied from +40°C down to -20°C. In both cases, the ratio of the value of capacity at various temperatures to that at 40°C was plotted as a function of temperature in degrees C.

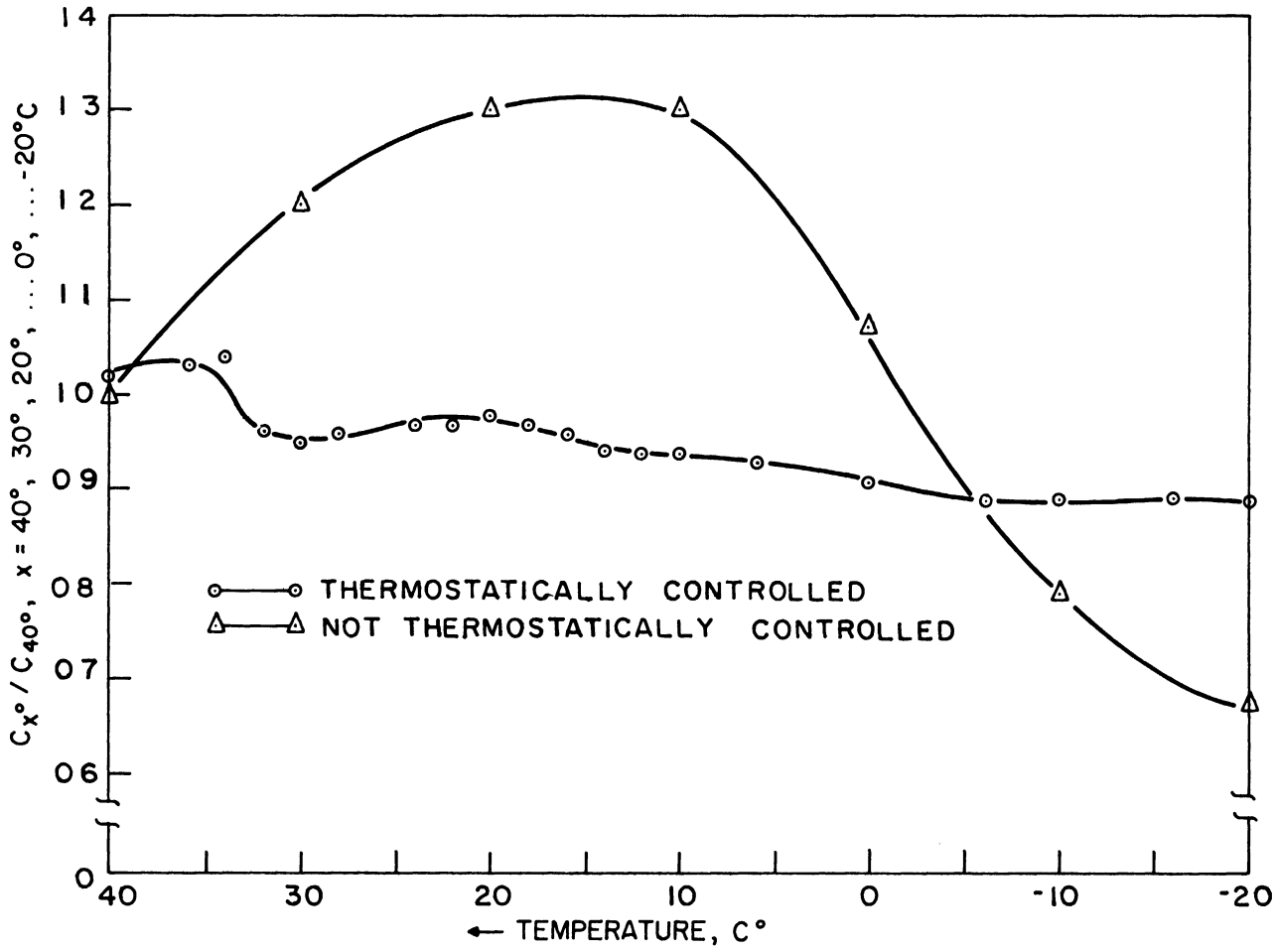


Fig. 2.8. Ratio of capacitance, C_{x^o}/C_{40^o}, vs. temperature in degrees centigrade.

At frequencies up to 100 Mc ferroelectrics are available with capacitance change ratios in the order of 10:1 at a field strength of about 100 volts/mil. The capacitance tuning ratio drops to perhaps 8:1 at 1000 Mc and to about 2:1 at 3000 Mc for the same field strength. The curve of Fig. 2.9 shows the ratio of maximum to minimum capacitance plotted versus frequency.

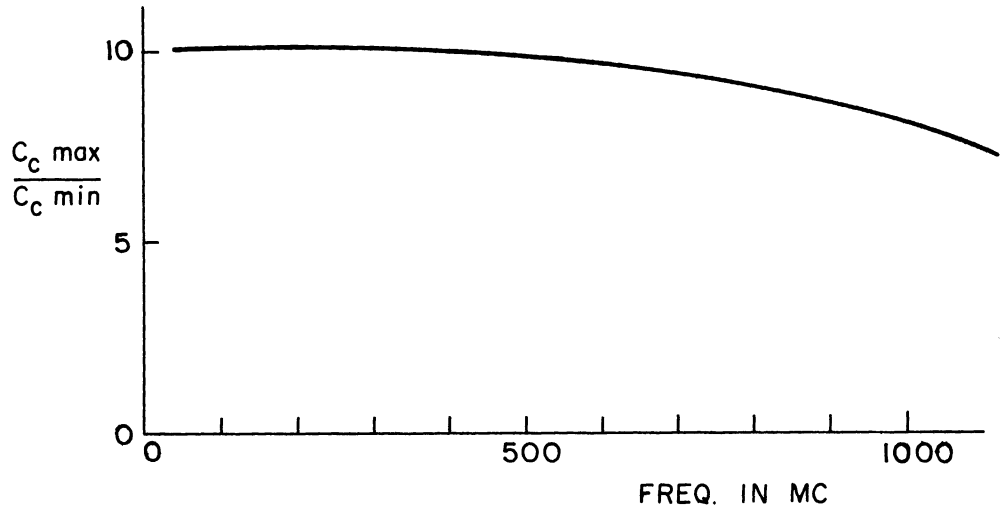


Fig. 2.9. $\frac{C_{c\,max}}{C_{c\,min}}$ of typical ferroelectric capacitor vs. frequency.

Representative Q values in the order of 100 are available for frequencies up to about 10 Mc. The Q values are in the order of 50 at 100 Mc, 10 at 1000 Mc, and about 3 to 6 at 3000 Mc. The curve of Fig. 2.10 shows typical values of Q plotted versus frequency. Since in a tuned tank circuit both Q and frequency increase with an increasing bias field, a reasonable Q is maintained over the tuning range.

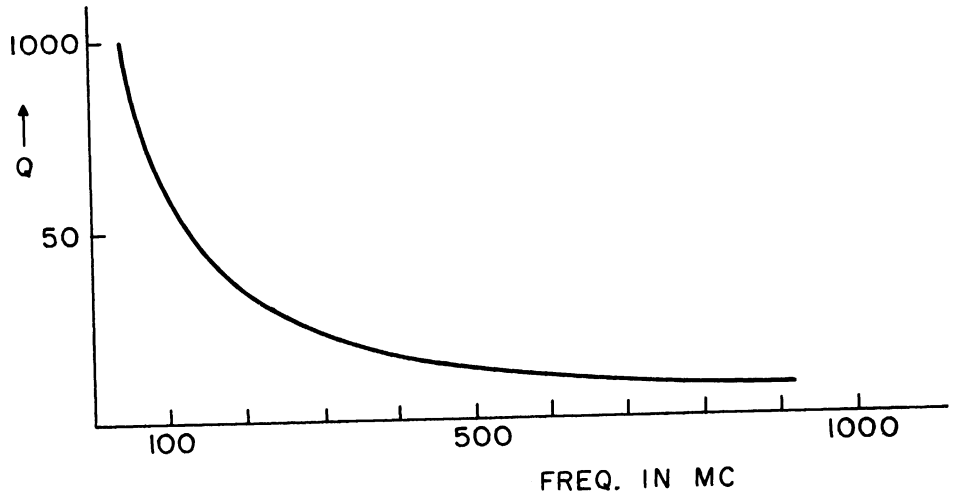
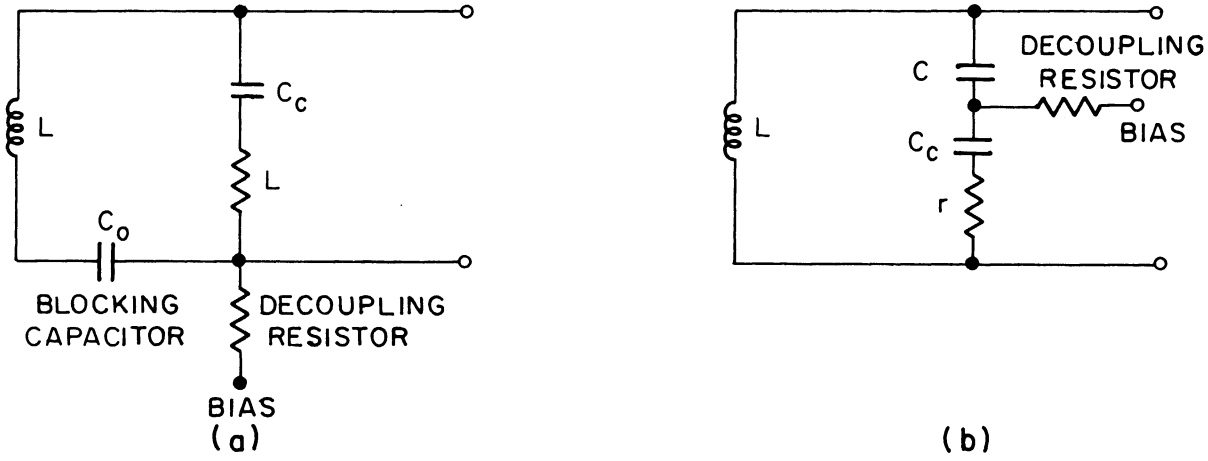


Fig. 2.10. Q of a typical ferroelectric capacitor versus frequency.

Figure 2.11a illustrates the basic circuit for application of a voltage variable capacitance in a tuned circuit. In many cases, the circuit Q may be satisfactorily high when this simple circuit is used, and if C_o is chosen much larger than the maximum capacitance of the ferroelectric, the frequency range will be determined by the available capacitance range of the ferroelectric. However, it may often be true that the losses in the ferroelectric material cause an unacceptable decrease in circuit Q. Fig. 2.11b depicts a method of increasing the tuned circuit Q by including a small loss-free capacitor (C) in series with the ferroelectric.



L = total inductance in tank circuit
r = loss associated with ferroelectric capacitance
C = loss-free capacitance
C_c = controllable capacitance (ferroelectric)

Fig. 2.11. Basic circuit for application of a ferroelectric capacitor in a tuned circuit.

$$Q_{cap} = \frac{1}{\omega r C_c} \tag{2.6}$$

$$TR_{cap} = \frac{C_c max}{C_c min} \tag{2.7}$$

The Q of the ferroelectric capacitor with the loss-free capacitor (C) in series is

$$Q_{circuit} = Q_{cap} \left[\frac{C_c + C}{C}\right] \tag{2.8}$$

while the tuning ratio becomes

$$TR_{circuit} = TR_{cap} \left[\frac{C_c min + C}{C_c max + C}\right]^{\frac{1}{2}} \tag{2.9}$$

If $C >> C_c$, the frequency range will be determined by the available capacitance range of the ferroelectric. However, if $C_c >> C$, then a definite gain in Q may be achieved but only through a loss in effective capacitance variation range.

The energy required to obtain the full capacitance variation is

$$E = \int_0^{V\,max} C(V) \cdot V \, dV \qquad (2.10)$$

This energy generally results in a power demand of a few milliwatts for most low frequency-swept devices.

The relationship between control voltage and signal capacitance is nonlinear, the percentage change in capacitance per unit control voltage being greatest for small control voltage values. Since in many cases this is undesirable, shaping of the control voltage must be done to compensate for the nonlinearity.

The problem of furnishing the electronic means for tuning a ferroelectric capacitor is not serious. An example of step frequency control is shown below: In the frequency range 1 to 3 Mc, it is desired to step from 1 to 2 Mc in 1 microsecond. The circuit has the following properties:

Control capacitance = 200 μμf

Required control voltage shift = 50 volts

Control current $i = C \frac{de}{dt} = 200 \times 10^{-12} \times 50 \times 10^{6} = 10$ ma

Peak control power P = .010 x 50 = .5 watt for 1 microsecond

A control current of 10 ma may be easily obtained from transistor circuits, so the design problem is reasonably simple.

In conclusion the study and development of ferroelectric material has resulted in a controllable capacitance having a volume less than .001 cubic inch, weighing a few grams, and being capable of tuning a frequency range of 10 to 1 at 100 Mc to 3 to 1 at over 3000 Mc. Q's of the order of 100 - 3 are obtained over this frequency range. Coefficient of capacitor drift with temperature depends upon bias voltage and for a nominal bias voltage is about 1%/°C.

2.3.2 Voltage Variable Diode Capacitor. The voltage sensitivity of semiconductor junction capacitance was understood prior to 1940. Not until recently, however, has this property been exploited for broad use in electronic circuitry (Ref. 12).

The reverse voltage on a semiconductor junction is supported by a region which is depleted of mobile carriers, as shown by Fig. 2.12. As the applied reverse voltage is changed, the depletion width (Wd) necessary to support the voltage changes. This depleted region acts as an insulator, resulting in a capacitance which varies in an inverse manner with applied voltage.

Voltage sensitivity of capacitance depends on the impurity distribution in the junction region. The more abrupt the junction, the greater the depletion width depends on applied voltage, resulting in a higher voltage sensitivity of capacitance.

For a parallel plate arrangement, the p-n junction has a capacitance equal to:

$$C = \frac{\epsilon A}{Wd} \qquad (2.11)$$

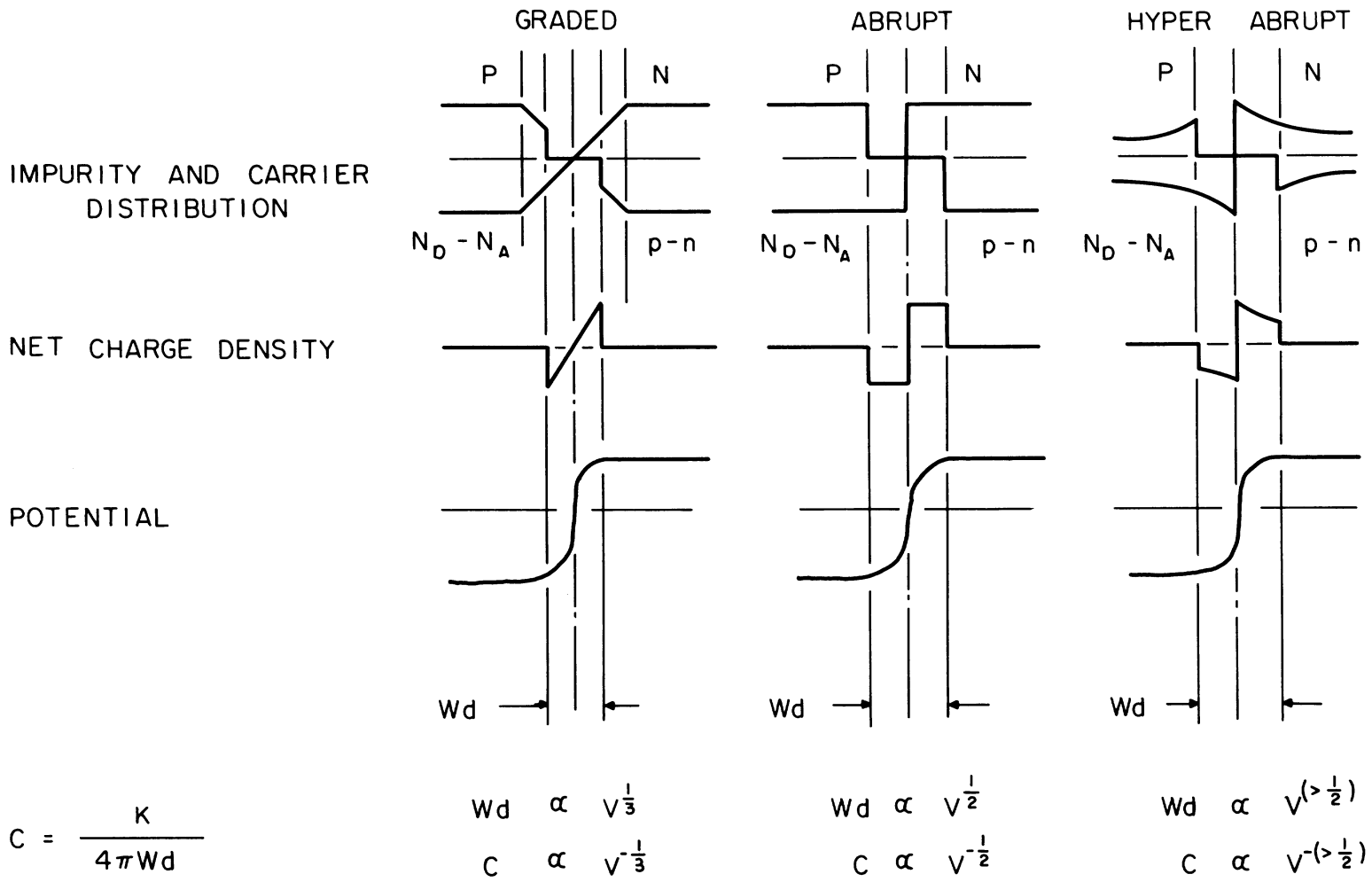


Fig. 2.12. Voltage sensitivity of capacitance.

ϵ = permittivity of the dielectric

A = junction area

Wd = width of the depletion region

For the case of an abrupt junction, the depletion width is given by:

$$Wd = 1 = K_1 \sqrt{V + V_o} \tag{2.12}$$

combining Eqs. (2.11) and (2.12) for an abrupt junction

$$C = \frac{\epsilon A}{K_1 \sqrt{V + V_o}} \tag{2.13}$$

where

K = a constant

V_1 = applied bias voltage

V_o = internal contact potential (0.3 to 0.9 volts)

When V_o is small with respect to V an abrupt junction exhibits a capacitance which varies with the inverse square root of voltage. Other capacitance voltage functions may be obtained across differently graded p-n junctions. If, for example, the semiconductor changes from p to n in a linear manner the capacitance varies as the inverse cube root of the applied voltage.

Voltage variable capacitance diodes have relatively good temperature stability (Ref. 13). The capacitance is fairly independent of temperature at the higher bias levels and becomes increasingly more sensitive with decreasing bias levels. This agrees quite closely with theory since the major uncompensated temperature effect is the internal contact voltage, V_o, term in Eq. (2.13). For silicon, V_o is approximately

.08 volts at 25°C and decreases to .04 volts at 150°C. The result is an approximately linear temperature sensitivity of about .15%/°C at 0.5 volts, .025%/°C at -4 volts, becoming negligible at higher voltages.

At frequencies up to 50 Mc voltage variable capacitance diodes are available with capacitance change ratios in the order of 5:1 with a voltage change of -2 volts to 100 volts. Using special fabrication techniques capacitance change ratios of 5:1 may be maintained up to several hundred megacycles.

Representative Q values in the order of 100 at 50 Mc can be obtained commercially. The value of Q drops to about 10 at 500 Mc and to about 5 at 1000 Mc. The curve of Fig. 2.13 shows typical values of Q plotted versus frequency. Since the Q of the capacitor equals $\frac{1}{\omega C_c r}$ and r remains practically constant over a wide frequency range, the product Qf remains practically constant, giving a curve which is a rectangular hyperbola.

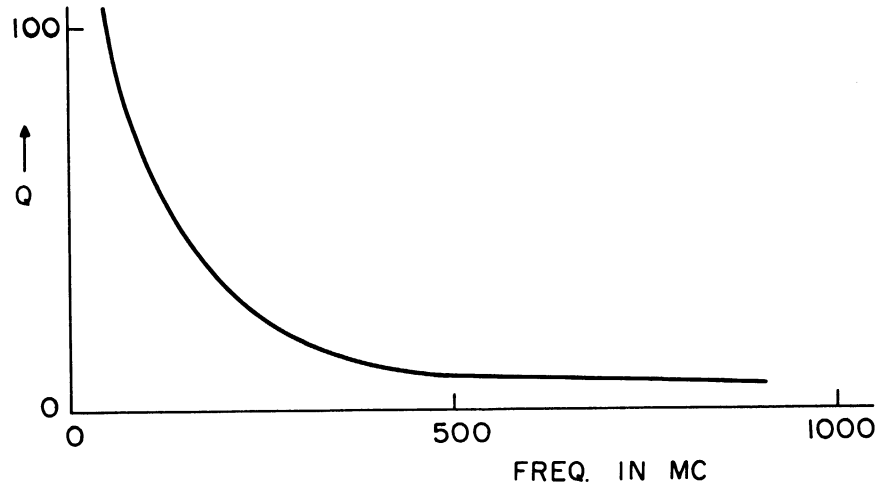


Fig. 2.13. Q of a typical voltage variable diode capacitor vs. frequency.

Figure 2.14 illustrates the basic circuit for application of a voltage variable capacitance diode in a tuned circuit. In many cases,

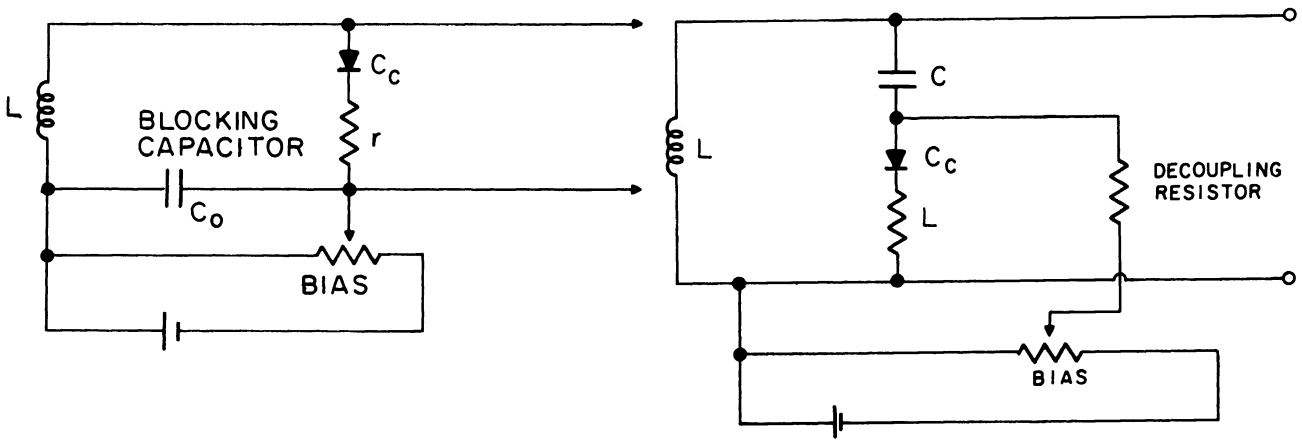


Fig. 2.14. Basic circuit for application of a voltage variable capacitance diode in a tuned circuit.

the circuit Q may be satisfactorily high when this simple circuit is used, and if C_o is chosen much larger than the maximum capacitance of the diode, then the frequency range will be determined by the available capacitance range of the diode. However, it may often be true that the diode's reverse losses cause an unacceptable decrease in circuit Q. The same method of increasing the tuned circuit Q as described on pages 29-30. for the ferroelectric capacitor may also be used for the diode. Although the gain in Q is offset by loss in effective variation capacitance range, it does reduce the amount of ac across the diode--a desirable feature, because if the ac were an appreciable fraction of the lowest bias voltage applied, there would be modulation of the capacitance of the diode by the signal.

Figure 2.15 presents a suggested arrangement of two diodes in such a way as to increase the circuit Q (if this is found to be

seriously reduced by losses in a single diode), while retaining a relatively large available capacitance sweep.

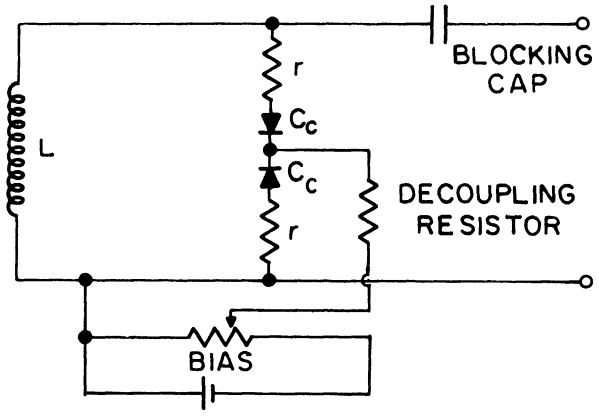


Fig. 2.15. Alternate method of increasing circuit Q.

The energy required to obtain the full capacitance variation generally results in a power demand of a few milliwatts for most low frequency-swept devices.

As in the case of the ferroelectric capacitor the relationship between control voltage and signal capacitance is nonlinear, the percentage change in capacitance per unit control voltage being greatest for small control voltage values. Since in many cases this is undesirable, shaping of the control voltage must be done to compensate for the nonlinearity.

The problem of furnishing the electronic means for tuning a voltage variable capacitance diode is not serious, and as in the case of the ferroelectric capacitance the control current may be easily obtained using transistor circuits.

In conclusion the study and development of voltage variable capacitance diodes has resulted in a controllable capacitance having a

volume less than .01 cubic inches, weighing a few grams and being capable of tuning a frequency range of 5 to 1 up to several hundred Mc. Q's of 100 at 50 Mc dropping to a value of 10 at 500 Mc are readily available. The coefficient of capacitor drift with temperature depends upon bias voltage, and for a nominal bias voltage of -4 volts is about .025%/°C.

2.4 Conclusion

From the foregoing discussion it is evident that the choice of a tuning element for frequency synthesis applications depends upon many factors such as frequency range of operation, tuning ratio, rapidity of frequency selection, temperature stability, control power, and environment in which the device is to be operated. No one tuning element possesses all the characteristics of the ideal tuning element discussed in Section 1.1. The controllable inductor, for example, has a high tuning ratio and Q, particularly in the lower frequency ranges with relatively small control power and good temperature stability. In addition, isolation of the controlled and controlling signals is possible. The controllable inductor presents some problems in control circuit design when step frequency operation is required and might create some difficulty if microminiaturization of the circuitry were a necessity.

The ferroelectric capacitor has a substantial tuning ratio and Q over a wide frequency range with almost negligible control power. The ferroelectric capacitor does not present any problems in control circuit design when step frequency operation is required and due to its very small size is well suited to microminiaturization. It has, however, rather poor temperature stability and in most cases would require a thermostatically controlled oven for proper operation. Since the controlling signal is nearly always at a lower frequency compared

to the controlled signal, isolation is easily accomplished using decoupling circuits.

The voltage variable capacitor diode has an adequate tuning ratio and Q for many applications over a wide tuning range and with negligible control power. It does not present any problems in control circuit design when step frequency operation is required and due to its small size is well suited to microminiaturization. It has good temperature stability and does not demonstrate any hysteresis effects. However, where high RF voltage may be developed across them, the junction must be back-biased far enough so that no part of the signal voltage swing causes the net voltage applied to the junction to go positive, or clipping will result. As in the case of the ferroelectric capacitor, isolation of the controlled and controlling signals is easily achieved by using a decoupling circuit.

The self-heating of ferroelectric and back-biased diode capacitors is considerably less than that of a controllable inductor for the same type of service. In addition, lead inductance limits controllable inductor operation at high frequencies whereas lead inductance does not necessarily dilute the tuning range of ferroelectrics and diodes.

In general it can be said that the present choice for a particular tuning element must be a compromise in order to obtain a close approach to the ideal in those properties most important for a specific application.

A comprehensive tabulated comparison of electronic tuning devices is carried out in Appendix A.

CHAPTER III

ANALYSIS OF THE GENERALIZED DISCRETE FREQUENCY SYNTHESIZER

3.1 System Concept

The analysis of the generalized discrete frequency synthesizer may be better understood by first considering the building blocks. The system is essentially comprised of two basic units:

(1) A crystal (or other high precision frequency standard) controlled discrete-frequency reference (DFR).

(2) A wideband phase-lock oscillator (PLO).

As shown in Fig. 3.1, the DFR consists of a crystal-controlled clock oscillator, multiplier or divider chains, a harmonic generator having an output rich in harmonics, and a band-pass filter.

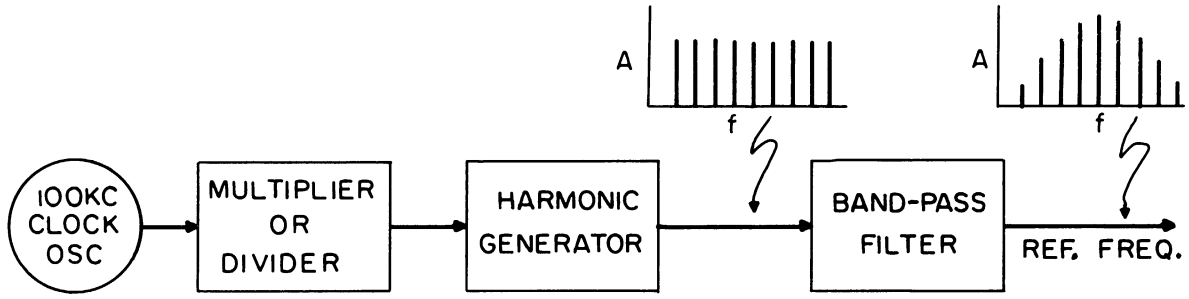


Fig. 3.1. Discrete frequency reference (DFR).

Ideally, the filter output consists of a limited set of harmonics of approximately equal amplitude. For example, the filter output could contain components every kilocycle in the band from 110 to 120 kc. Thus the output of the DFR is the equivalent of many crystal oscillators, all with a precise harmonic relationship.

The PLO shown in Fig. 3.2 has the function of reproducing

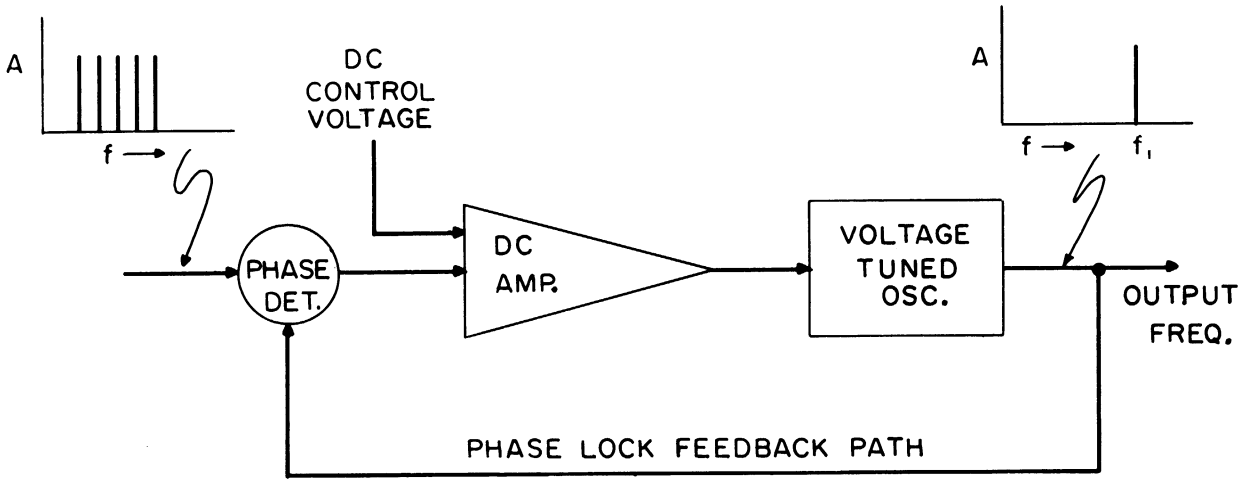


Fig. 3.2. Phase-lock oscillator (PLO).

cleanly one of a number of frequency components applied to its input. It thus acts as a tunable narrowband filter. The voltage-tuned oscillator has its output frequency and phase compared in the phase detector with the desired harmonic of the input waveform. If these are of the same frequency, the output of the phase detector will be a dc voltage dependent upon the phase difference of the oscillator and the reference. This dc voltage is amplified and fed to the control element in the oscillator. If the oscillator frequency tends to drift or change in any way, this attempted change is first sensed as a phase-difference change in the phase detector. This produces a change in phase detector output voltage which acts to hold the oscillator frequency constant. In short, if the oscillator tends to drift, its output phase relative to that of the reference will change but its average frequency (f_1) will remain fixed.

Note that in automatic frequency control systems the frequency

of the oscillator is compared to a reference frequency, e.g., the resonant frequency of a passive circuit, and the frequency difference--not phase difference--is used to generate a signal which tends to reduce the frequency difference. Such a system requires a small but finite error of the controlled variable (the output frequency) in order to operate. The phase-lock system, on the other hand, requires no steady-state error of the controlled variable but instead utilizes an error in the integral of the controlled variable, i.e., an error in phase difference.

When not in phase-lock the oscillator frequency may be brought within the capture range of the desired harmonic by means of the externally applied dc voltage.

By combining the discrete-frequency reference, Fig. 3.1, and the phase-lock oscillator, Fig. 3.2, it is possible to construct a unit whose output frequency can have certain discrete values. This unit, called a discrete-frequency generator (DFG), (Fig. 3.3) has an output

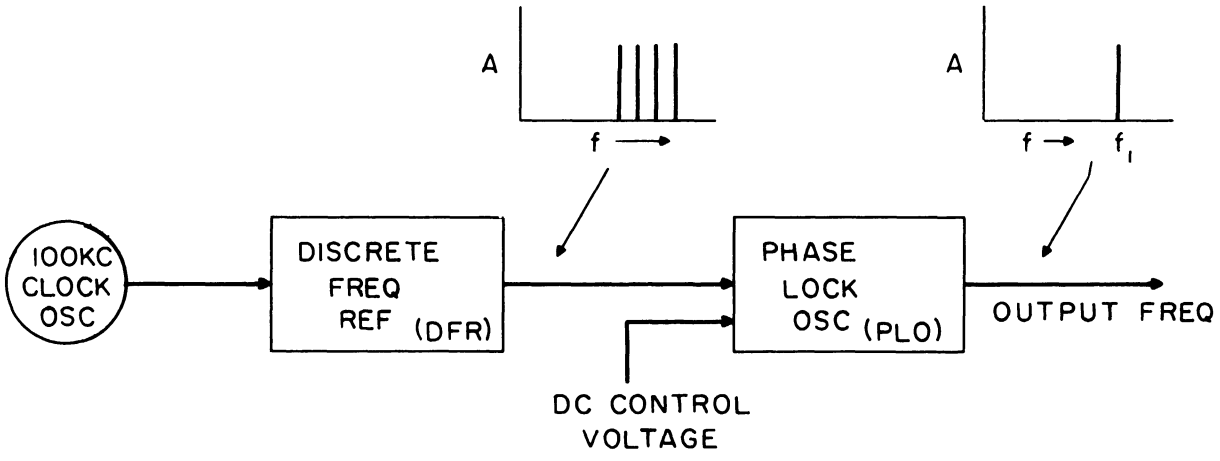


Fig. 3.3. Discrete-frequency generator (DFG).

frequency which is precisely one of the harmonics of the discrete-frequency reference. The number of different frequencies that can be selected is a function of the voltage-tuned oscillator set-on accuracy. If, for example, it is desired to tune the DFG over a 10 Mc range and, in addition, if it is assumed that the relatively unprecise tuning elements will not allow open-loop set-on accuracies greater than about $\pm$ 5 percent, then the DFG can only cover the 10 Mc range accurately in 1 Mc steps. This, in effect, means that the discrete-frequency reference can not have components spaced any closer than 1 Mc over the 10 Mc band.

Starting with this as a basic unit to produce one digit of the desired frequency, decade units are added to furnish the desired number of significant figures.

Operations and details of a proposed generalized discrete-frequency synthesizer may be understood with the aid of the example shown in Fig. 3.4.

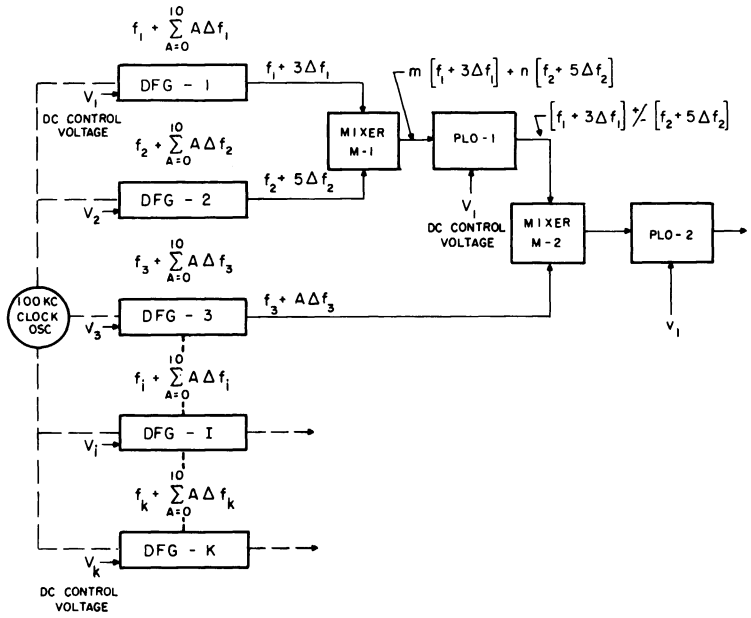


Fig. 3.4. Generalized discrete-frequency synthesizer.

A single clock oscillator and suitable multiplier-divider chains furnish the basic frequency Δf_i ($i = 1, 2, \ldots, k$, for DFG-i; $i = 1, 2, \ldots, k$, where Δf_i is the harmonic spacing of DFG-i). The range of DFG-i is f_i to $(f_i + 9\Delta f_i)$ in Δf_i steps, and if it is assumed that $\Delta f_1 > \Delta f_2 > \ldots > \Delta f_k$ then the total range of the k-digit synthesizer is $10\Delta f_1$ in Δf_k steps. For example, if $\Delta f_1 = 5$ Mc and $\Delta f_k = 100$ kc, the range of the synthesizer is 50 Mc in 100-kc steps. As indicated in Fig. 3.4, the range of DFG-1 is f_1 to $(f_1 + 9\Delta f_1)$ in Δf_1 steps, and of DFG-2 is f_2 to $(f_2 + 9\Delta f_2)$ in Δf_2 steps. Single output frequencies, e.g., $f_1 + A\Delta f_1$ from DFG-1 and $f_2 + B\Delta f_2$ from DFG-2, are fed to mixer (M-1). The output of the mixer contains components $m(f_1 + A\Delta f_1) \pm n(f_2 + B\Delta f_2)$, where m and n are positive or negative integers. The output of the mixer is fed to the phase-lock oscillator (PLO-1), whose operating range is confined to the frequency range $(f_1 + A\Delta f_1)$ +/- $(f_2 + B\Delta f_2)$, where +/- means either + or -. Higher-order harmonics in the mixer output which happen to fall within this band are of such low amplitude that they are ignored by PLO-1.

The voltage-tuned oscillators in DFG-1 and DFG-2 are brought to the approximate vicinity of the selected reference components by means of rough tuning dc voltages V_1 and V_2. The phase-lock loops then take over and bring the oscillators into precise frequency alignment with the selected components. The same rough tuning voltages V_1 which are applied to DFG-1 are also applied to PLO-1. This brings the frequency of the voltage-tuned oscillator of PLO-1 within the capture range of the desired $(f_1 + A\Delta f_1)$ +/- $(f_2 + B\Delta f_2)$ frequency, where its phase-lock loop takes over and brings the oscillator into precise frequency alignment. The capture range of PLO-1 must be at

least $9\Delta f_2$ wider than the capture range of DFG-1, so the same tuning voltage can effect capture at any frequency $(f_1 + A\Delta f_1) +/- (f_2 + B\Delta f_2)$.

Additional decades operate in a similar manner producing a final output frequency of $(f_1 + A\Delta f_1) +/- (f_2 + B\Delta f_2) +/- \ldots,$ $(f_k + j\Delta f_k)$ which has the desired range of 10 Δf_1 in Δf_k steps.

This example shows a generalized discrete-frequency synthesizer capable of producing frequencies to k digit accuracy with high precision, since the whole system is crystal-controlled by a single clock oscillator.

The synthesizer system may be further modified to give any desired frequency between the steps of the lowest order digit. This may be done by furnishing a vernier oscillator at the low frequency tuning range of Δf_k.

The operating range of the synthesizer may be placed in any desired position in the frequency spectrum up to approximately 300 Mc with presently available transistors and solid-state tuning elements.

As indicated in Chapter I, to achieve an efficient synthesis technique basic research in a number of problem areas is required. For example:

(1) A study and evaluation of the various methods for the efficient production of high-order harmonics with balanced energy distribution over the frequency band of interest is required.

(2) Basic research in phase-lock oscillator design with particular attention directed toward operation at higher frequencies and toward such dynamic characteristics as capture range, capture stability, rapid frequency convergence, and purity of the output signal is needed.

(3) An analysis of the problem of combining two signal frequencies to obtain a single signal frequency in the form of their sum or difference while using tunable narrowband filters, i.e., PLO's of a practical design with arbitrarily-limited frequency discrimination characteristics, is required.

These problem areas will be considered in detail in the following sections.

3.2 Discrete Frequency Reference

To initiate the study and evaluation of the various methods for the efficient production of high-order harmonics with balanced energy distribution over the frequency band of interest, a generalized statement of the problem is in order:

(1) What class of time functions will produce a given frequency spectrum?

(2) Of this class which functions will have the maximum amount of the total available spectrum energy in the band of interest and at the same time have a minimum peak-to-average voltage characteristic?

(3) What practical methods are available for generating these desirable functions?

3.2.1 Definition of Peak Factor. Any periodic function with period T which may be represented by a Fourier Series has the form

$$e(t) = \frac{E_o}{2} + \sum_{n=1}^{\infty} E_n \cos (n\omega_o t + \theta_n) \qquad (3.1)$$

where E_o, E_k, θ_k ($k = 1, 2, 3, \ldots$) are all real and $\omega_o = \frac{2\pi}{T}$.

The average power of e(t) across a 1-ohm resistor is defined as follows:

$$P_{avg} = \frac{1}{T} \int_0^T [e(t)]^2 \quad dt \tag{3.2}$$

Parseval's theorem states that whenever e(t) is bounded and integrable over the period then

$$\frac{1}{T} \int_0^T [e(t)]^2 \quad dt = \frac{1}{2} \left[\frac{E_o}{2}^2 + \sum_{n=1}^{\infty} E_n^2 \right] \tag{3.3}$$

Let

$$f(t) = A \cos (\omega t + \theta) \tag{3.4}$$

where f(t) is a single frequency function with peak value A. The average power of this single frequency function is

$$P_{avg} = \frac{1}{T} \left[A^2 \cdot \frac{T}{2} \right] = \frac{A^2}{2} \tag{3.5}$$

and is completely independent of both frequency and phase. If the average power of the single frequency function f(t) is equated to that of the arbitrary periodic function e(t), one finds that

$$\frac{A^2}{2} = \frac{1}{2} \left[\frac{E_o}{2}^2 + \sum_{n=1}^{\infty} E_n^2 \right] \tag{3.6}$$

or

$$A = \sqrt{\frac{E_o}{2}^2 + \sum_{n=1}^{\infty} E_n^2} \tag{3.7}$$

A term "peak factor" may now be defined as the ratio of the peak-to-peak value of any function e(t) to the peak-to-peak value of

a sine wave function f(t) of equivalent average power.

$$\text{Peak factor} = \text{pf} = \frac{\text{P-P value of } e(t)}{\text{P-P value of sine wave } f(t) \text{ of equivalent average power}} \tag{3.8}$$

From Eq. (3.8) it is clear that the pf of a sine wave function is unity. To determine the absolute upper and lower limits over which the peak factor may be expected to range, consider the pf of a function e(t) under the following conditions:

Let

$$e(t)_{max} = E_{max} \qquad e(t)_{min} = E_{min}$$

$$0 \leq t < T \qquad 0 \leq t < T$$

where:

$$E_{max} \geq 0, \qquad E_{min} \leq 0$$

The above requirements merely state that functions with large dc values are excluded. The peak factor of such a function may be written as

$$\text{pf} = \frac{E_{max} - E_{min}}{2\sqrt{\frac{2}{T}\int_0^T [e(t)]^2 \, dt}} \tag{3.9}$$

For fixed values of E_{max} and E_{min} the pf is determined solely by the value of the integral

$$\int_0^T [e(t)]^2 \quad dt.$$

The value of this integral is a maximum when $|E_{max}| = |E_{min}|$ and e(t) is always equal to E_{max} or E_{min}. The pf under these conditions reaches its minimum

$$pf_{min} = \frac{2\,E_{max}}{2\sqrt{\frac{2}{T}\int_0^T E_{max}^2\,dt}} = \frac{1}{\sqrt{2}} = .707 \qquad (3.10)$$

The upper bound of pf is quickly found from Eq. (3.9); indeed, as the value of the integral goes to zero the pf goes to infinity.

From the above analysis it may be concluded that the absolute range of the peak factor is from a minimum value of .707 to a maximum value of infinity. To demonstrate this fact somewhat more graphically consider the peak factor of the function e(t) shown in Fig. 3.5(a).

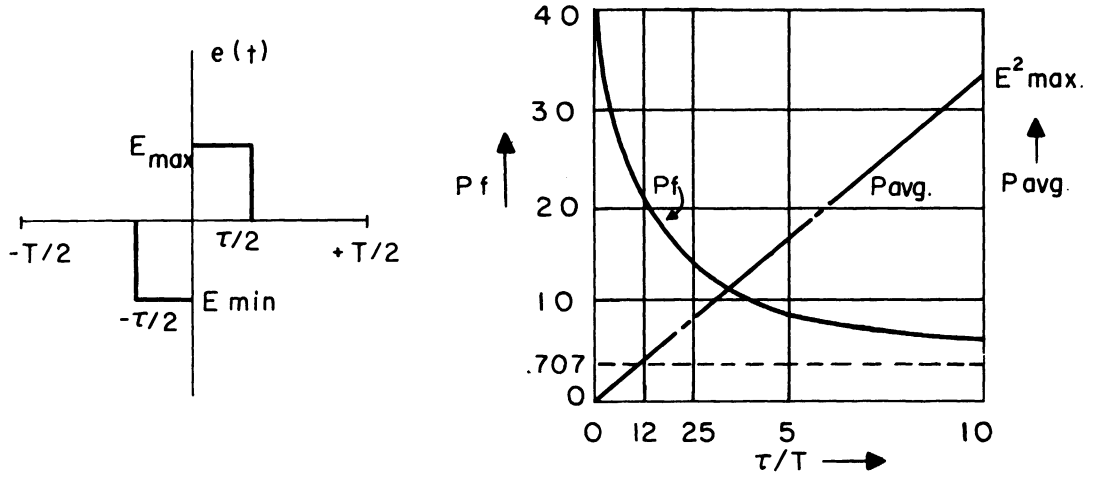


Fig. 3.5. (a) Rectangular function e(t)
(b) Peak factor (pf) and average power (P_{avg}) of e(t) versus the ratio τ/T.

Let

$$E_{max} - E_{min} = 2\,E_{max}$$

The average power of the function is

$$P_{avg}\,e(t) = \frac{1}{T}\int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} E_{max}^2\,dt = 2\,E_{max}^2\,\frac{\tau}{2T} \qquad (3.11)$$

The equivalent power of a sine wave as given in Eq. (3.5) is

$$P_{avg} = \frac{A^2}{2} \tag{3.12}$$

Equating these two functions gives

$$\frac{A^2}{2} = 2 E_{max}^2 \frac{\tau}{2T} \tag{3.13}$$

or

$$A = 2 E_{max} \sqrt{\frac{\tau}{2T}} \tag{3.14}$$

The peak factor becomes

$$pf = \frac{E_{max} - E_{min}}{2A} \tag{3.15}$$

$$pf = \frac{1}{2\sqrt{\frac{\tau}{2T}}} = \frac{1}{2} \sqrt{\frac{2T}{\tau}} \tag{3.16}$$

If E_{max} is held constant, then pf goes to infinity as τ goes to zero and pf goes to .707 as τ goes to T.

As the pf goes to infinity, the power in the spectrum goes to zero; and as the peak factor goes to its minimum value of .707, the power in the spectrum reaches a maximum.

The results of pf and P_{avg} plotted vs. the ratio of $\frac{\tau}{T}$ are shown in Fig. 3.5(b).

In the particular case discussed above, i.e., the rectangular wave, one might conclude that operation at the point of maximum power in the spectrum and minimum pf would be ideal, but it must be remembered that although the spectrum power is a maximum it is predominantly rich in low frequency content while the power in the desired band of interest

may be very low.

From the above analysis one can see that the peak factor is a necessary but not sufficient condition to be effectively used as a figure of merit in the design of an appropriate frequency spectrum. In general, a relationship is needed which takes into consideration both peak factor and the ratio of power in the band of interest to the total available spectrum power. Such a relationship can be defined as:

$$pf^* = pf \cdot \sqrt{\frac{P_T}{P_I}} \tag{3.17}$$

where pf is the peak factor as defined in Eq. (3.8), P_T is the average power of e(t) and P_I is that average power of e(t) contained in the band of interest. Clearly

$$\sqrt{\frac{P_T}{P_I}} \geq 1 \tag{3.18}$$

Using the relationship in Eq. (3.3) it can be shown that

$$pf^* = \frac{E_{max} - E_{min}}{2\sqrt{\frac{E_o^2}{2} + \sum_{n=1}^{\infty} E_n^2}} \cdot \frac{\sqrt{\frac{1}{2}\left[\frac{E_o^2}{2} + \sum_{n=1}^{\infty} E_n^2\right]}}{\sqrt{\frac{1}{2}\left[\sum_{n=j}^{k} E_n^2\right]}} \tag{3.19}$$

Where it is assumed that the dc term is not included in the term

$$\sqrt{\frac{1}{2}\left[\sum_{n=j}^{k} E_n^2\right]}$$

the equation reduces to

$$pf^* = \frac{E_{max} - E_{min}}{2 \sum_{n=j}^{k} E_n^2} \tag{3.20}$$

where j and k represent the desired harmonics to be included in the band of interest.

Admittedly, the sum $\sum_{n=j}^{k} \sqrt{E}_n^2$ is not always easy to calculate given e(t), but it can be done using straightforward techniques. On the other hand, given E_n rather than e(t) it is not routine to obtain the set of e(t), thus making the determination of $E_{max} - E_{min}$ very difficult.[1] The question of how to adjust the phases of a multicomponent signal, having a given power spectrum, to minimize its "peak factor" has been a long-standing problem in multi-carrier telegraphy, radar, and many other applications in which it is desired to minimize, for a given power, the peak-to-peak amplitude of a signal. This problem has not yet yielded to a closed form of solution. An approximate solution has been suggested (Ref. 14) which considers frequency modulated signals. It was found that for a certain class of FM signals a simple approximate relationship exists between the phase angles and the power spectrum. By adjusting the phase angles of a signal with a given power spectrum, one is able to obtain a waveform which resembles an FM signal and has a peak factor nearly as low.

The questions might be asked, what is the maximum peak factor of a function with N spectral components and what advantage may be obtained by adjusting the phases of the various components.

---

[1] This set E_n of amplitude components does not uniquely determine the time function e(t). A different time function exists for each set of phase angles θ_n.

Let

$$e(t) = \frac{E_o}{2} + \sum_{n=1}^{N} E_n \cos (n\omega_o t + \theta_n) \tag{3.21}$$

where N is so chosen that all

$$\sum_{n=N+1}^{\infty} E_n \cos (n\omega_o t + \theta_n) \text{ may be neglected.}$$

The average power as defined in Eq. (3.3) is

$$P_{avg} = \frac{1}{T} \int_o^T [e(t)]^2 \, dt \cong \frac{E_o^2}{4} + \frac{1}{2} \sum_{n=1}^{N} E_n^2 \tag{3.22}$$

Again, equating Eq. (3.22) to the average power of a sine wave, one finds that

$$A = \sqrt{\frac{E_o^2}{2} + \sum_{n=1}^{N} E_n^2} \tag{3.23}$$

The peak-to-peak excursion of e(t) is defined as $2\, e_{max}$. The peak factor then becomes

$$pf = \frac{2\, e_{max}}{2A} = \frac{e_{max}}{\sqrt{\frac{E_o^2}{2} + \sum_{n=1}^{N} E_n^2}} \tag{3.24}$$

For the particular case where $e(t) = E \sum_{n=1}^{N} \cos (n\omega_o t + \theta_n)$ (3.25)

the maximum peak factor becomes

$$pf = \frac{NE}{\sqrt{NE^2}} = \sqrt{N} \tag{3.26}$$

Equation (3.26) proves that the maximum peak factor is equal to the square root of the number of desired spectral components and occurs only when the $\cos (n\omega_o t + \theta_n)$ of Eq. (3.25) is equal to unity for

each component.

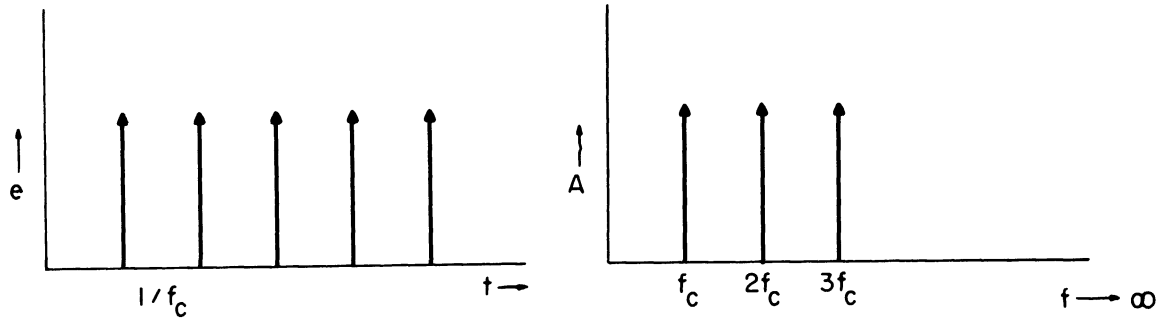
If one assumes that by proper adjustment of the phases of the function a minimum peak factor of 1 could be achieved, then the ratio of maximum to minimum peak factor is

$$\frac{pf_{max}}{pf_{min}} = \sqrt{N} \tag{3.27}$$

It follows that for a small number of spectral components there is little to be gained by adjusting the phases. However, as the number of spectral components increases, e.g., N = 10, there may be a considerable advantage in phase adjustment.

3.2.2 Methods of Generating a Discrete-Frequency Reference. Four methods of generating a discrete-frequency reference are analyzed. These methods are (a) the Repetitive-Impulse method, (b) the Shift-Register-Generator method, (c) the Parametric method, and (d) the Modulation method.

(a) The Repetitive Impulse Method. The ideal frequency spectrum would consist of spectral components of balanced amplitude with the desired harmonic spacing over the frequency range of interest. The ideal spectrum and its time function are shown in Fig. 3.6.

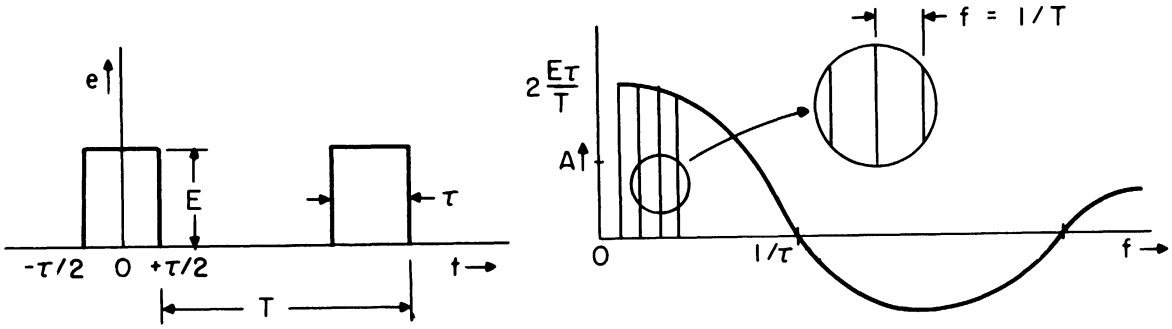


(a) Time function. (b) Frequency spectrum.

Fig. 3.6. Repetitive impulse (f_c = clock frequency).

Although the frequency spectrum shown in Fig. 3.6(b) is desirable, it is impossible to generate a repetitive impulse as shown in Fig. 3.6(a). Generation of pulses approaching the ideal, i.e., nanosecond pulses with repetition frequencies greater than 50 Mc, is possible using the recovery effect of certain types of pn junction diodes (Ref. 15).

Perhaps the most straightforward method for providing a uniform amplitude spectrum is to utilize a clock oscillator frequency equal to the required separation of the harmonics. The clock output is used as a trigger signal for a blocking oscillator or diode harmonic generator which has an output waveform very rich in harmonics. The desired harmonics are selected by means of a filter and amplified to obtain the energy required for proper operation of the phase-lock loop. A time function which is realizable and its associated frequency spectrum are shown in Fig. 3.7. The relationships among the parameters of the pulse



(a) Time Function (b) Frequency Spectrum

Fig. 3.7. Repetitive finite pulse.

of Fig. 3.7(a) and the frequency spectrum of Fig. 3.7(b) may be summarized as follows:

(a) The repetition frequency f determines the spacing of the lines representing the Fourier components but has no effect on the envelope curve drawn through the ends of the lines.

(b) The pulse shape determines the shape of the envelope curve; for a rectangular pulse the envelope always has the form of $\frac{\sin x}{x}$ where $x = \frac{1}{2}\ \omega\tau$.

(c) The pulse duration τ determines the spacing of the zeros of the envelope curve.

(d) Since the spacing of the zeros is $1/\tau$ and that of the lines is $f = \frac{1}{T}$, the number of spectral components within each loop of the envelope is $\frac{T}{\tau}$.

Although the time function shown in Fig. 3.7 is realizable and may be used to provide a reasonably uniform amplitude spectrum over a given band of interest, a more detailed examination of the repetitive finite pulse and its associated frequency spectrum must be carried out to determine how to optimize its use in a synthesizer. The question might be stated as follows: For the case of the repetitive finite pulse how does the peak factor and average power in the band of interest vary as a function of the pulse width τ and the number of spectral components N?

Referring to Fig. 3.7 assume the pulse height E and the period T of the time function remain constant. From the frequency spectrum select a given number of spectral components N, all of the same sign and in the desired range, by means of an ideal band-pass filter.[1]

Under the above conditions examine both peak factor and the average power contained in the band of interest as a function of the pulse width.

---

[1] An ideal band-pass filter as defined here will pass all frequencies within its pass band without amplitude distortion while rejecting all other frequencies. At the same time the phase shift across the pass band will remain constant or at most change linearly.

The Fourier Series for the time function e(t) out of the band-pass filter takes the form

$$e(t) = \sum_{n=j}^{k} E_n \cos n\omega t \tag{3.28}$$

where

$$\omega = 2\pi f$$

$$E_n = \frac{2\tau E}{T} \cdot \left[\frac{\sin \frac{n\pi\tau}{T}}{\frac{n\pi\tau}{T}} \right] \tag{3.29}$$

From Eq. (3.28) it can be seen that the peak value of the function e(t) occurs at t = 0, T, 2T, ..., etc.

At these points cos nωt = 1 for all n, and e(t) has the value

$$e(t) = \sum_{n=j}^{k} E_n, \quad t = 0, T, 2T, \ldots$$

The average power in the band of interest can be obtained with the use of Eq. (3.3) and is

$$P_{avg} = \frac{1}{2} \sum_{n=j}^{k} E_n^2 \tag{3.31}$$

Under these conditions

$$pf^* = Pf \tag{3.32}$$

where

$$pf = \frac{\sum_{n=j}^{k} E_n}{\sqrt{\sum_{n=j}^{k} E_n^2}} \tag{3.33}$$

To obtain useful results the following conditions were imposed and the problem programmed for the IBM-704 computer.

Let

$$T = 10^{-5} \text{ sec}$$

$$E = 1 \text{ volt}$$

$$\tau = \frac{10^{-6}}{Z}$$

where Z is the value in Mc of the first zero in the frequency spectrum and is varied in discrete steps in the range 1 to 40 Mc.

$$N = 11 \text{ components}$$

where the components are in the range from

$$n = 100 \text{ to } n = 110.$$

Peak factor and average power as functions of the position of the first zero (Z) are shown in Fig. 3.8. For the first zero locations below the band of interest both power and peak factor vary

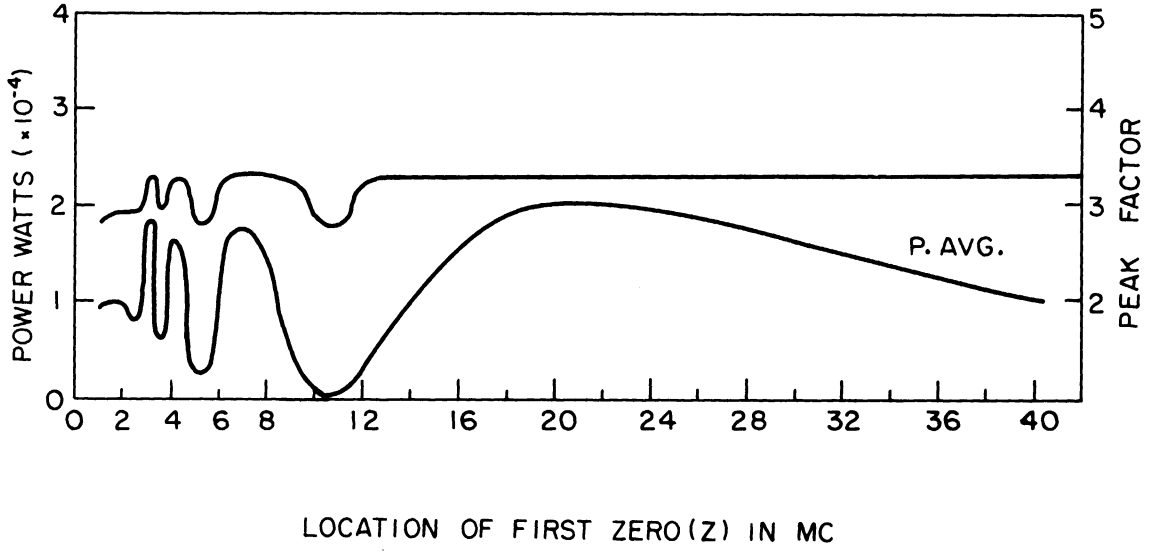


Fig. 3.8. Peak factor (pf) and average power (P_{avg}) in the band of interest vs. the location of the 1st zero (Z) in Mc for N = 11 spectral components.

wildly. For first zero locations above the band of interest the peak factor becomes a constant independent of the first zero location. The power in the band of interest on the other hand rises from a minimum at Z = 11 Mc to a maximum in the range Z = 20 to 22 Mc and falls off as Z increases.

Under the given conditions then, a pulse width τ should be chosen such that the first zero of the frequency spectrum will fall in the range 20 to 22 Mc.

The question might now be asked, what happens if the number of spectral components is increased? The results of increasing the number of spectral components while holding all other conditions the same are shown in Figs. 3.9 and 3.10.

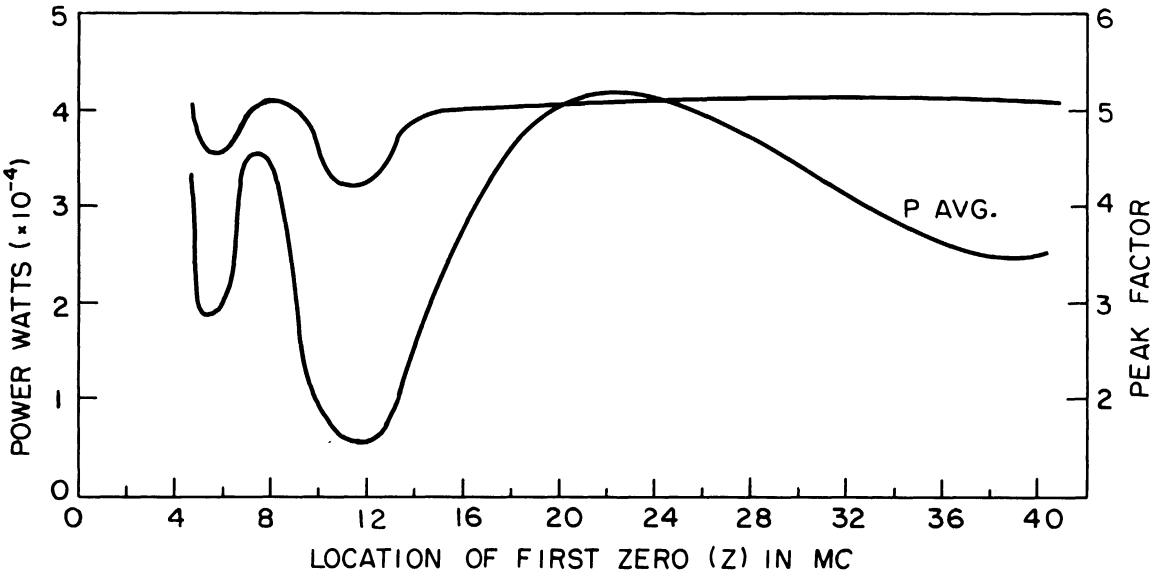


Fig. 3.9. Peak factor (pf) and average power (P_{avg}) in the band of interest vs. the location of the 1st zero (Z) in Mc for N = 26 spectral components.

In Fig. 3.9 N = 26 and the spectral components are selected in the range n = 100 to n = 125. The general behavior of the peak factor and average power as a function of the position of the first zero is very similar to the case where N = 11. The regions where the peak factor

becomes independent of first zero position and the power in the band reaches a maximum, however, have both moved out in frequency. The peak

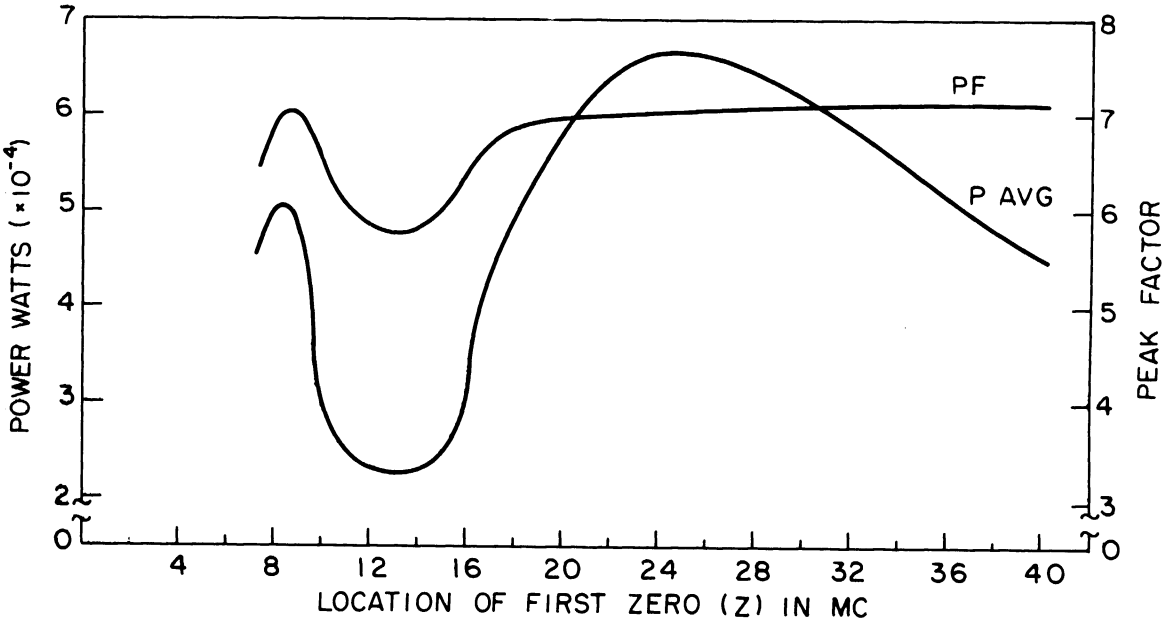


Fig. 3.10. Peak factor (pf) and average power (P_{avg}) in the band of interest vs. the location of the 1st zero (Z) in Mc for N = 51 spectral components.

factor becomes independent of first zero location beyond about 16 Mc while the maximum power in the band of interest occurs when the first zero is located in the range 22-24 Mc.

In Fig. 3.10 N = 51 and the spectral components are selected in the range n = 100 to n = 150. Again, the general behavior of the peak factor and average power as a function of the first zero is quite similar to the previous two cases with the exception that the peak factor becomes independent of the first zero location beyond about 20 Mc and the power in the band of interest reaches a maximum when the location of the first zero occurs in the range 24-26 Mc.

It is interesting to note that if the points of the first zero which give maximum power are plotted vs. N, the number of spectral

components, their locus will approximate a straight line of the form,

$$10\ Z = N + 199 \tag{3.34}$$

This equation is plotted in Fig. 3.11.

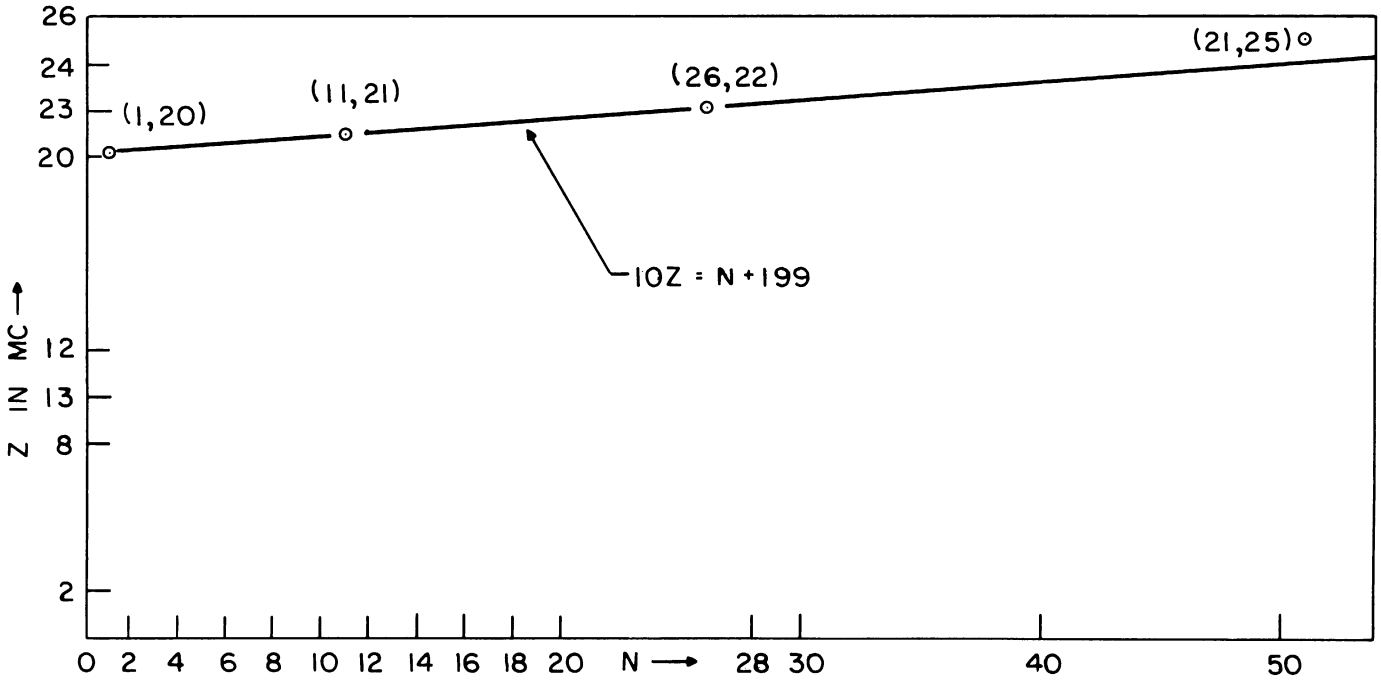


Fig. 3.11. Location of 1st zero (Z) in Mc vs. the number of spectral components (N) for maximum power in the band of interest.

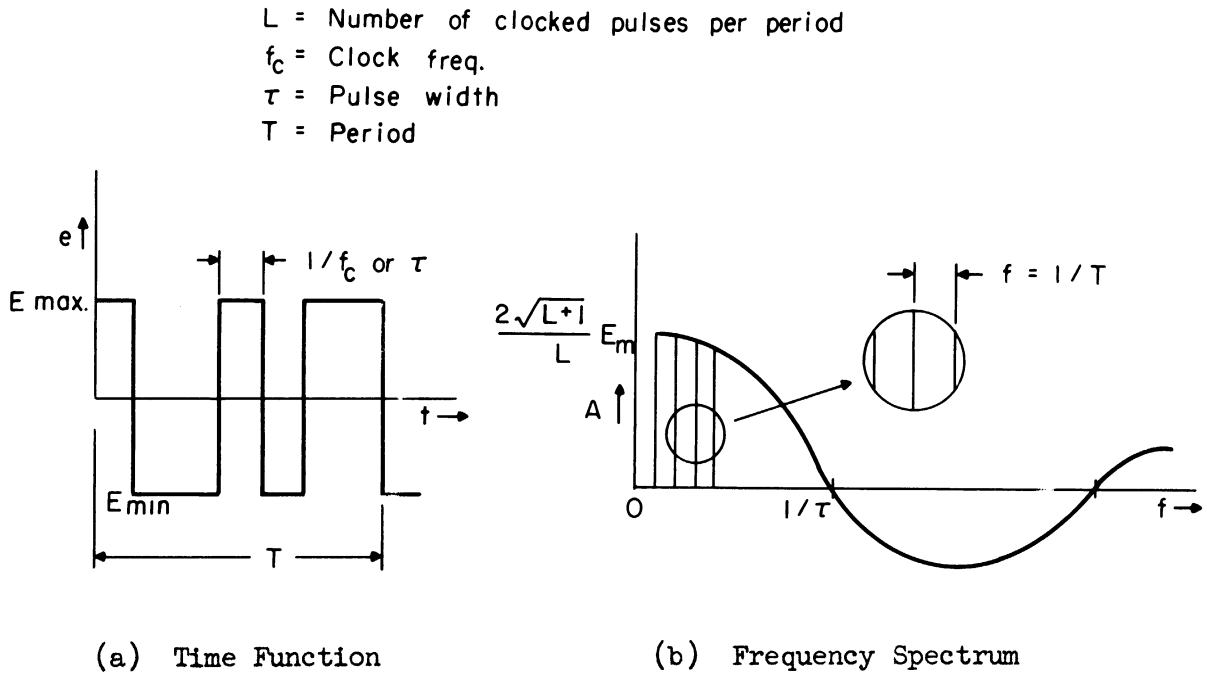
From the results of the analysis of the repetitive finite pulse, one can conclude that the expected peak factor is approximately equal to $\sqrt{N}$ as predicted in Eq. (3.26) and verified in the curves of Figs. 3.8, 3.9, and 3.10. Also the peak factor is independent of the location of the first zero of the frequency spectrum when the first zero is placed somewhat above the desired band of interest. In addition, the average power in the band of interest reaches a maximum when the location of the first zero occurs at some point above the band of interest. This point of maximum power can be found with the

aid of the curve of Fig. 3.11.

In general, to achieve optimum utilization of a repetitive finite pulse in generating a discrete-frequency reference, it is only necessary to derive the location of the first zero above the band of interest which will give the maximum amount of power.

(b) The Shift-Register Generator Method. As indicated in Eq. 3.9, the minimum attainable value of peak factor occurs when the function e(t) is always equal to E_{max} or E_{min} where $|E_{max}| = |E_{min}|$. The peak factor under these conditions is found to be .707. It is interesting to consider the possibility of generating time functions which fulfill the above conditions while providing a reasonably uniform amplitude spectrum over a given band of interest.

The digitally-generated linear maximal sequence (Ref. 16) shown in Fig. 3.12(a) will produce a line spectrum which has a $\frac{\sin x}{x}$ envelope and has the spacings as shown in Fig. 3.12(b). A digital



(a) Time Function (b) Frequency Spectrum

Fig. 3.12. Digitally-generated linear maximal sequence.

sequence refers to a succession of binary states which in this case are regarded as consisting of E_{max}'s and E_{min}'s where $|E_{max}| = |E_{min}|$.

From Eq. 3.2 the average power is found to be

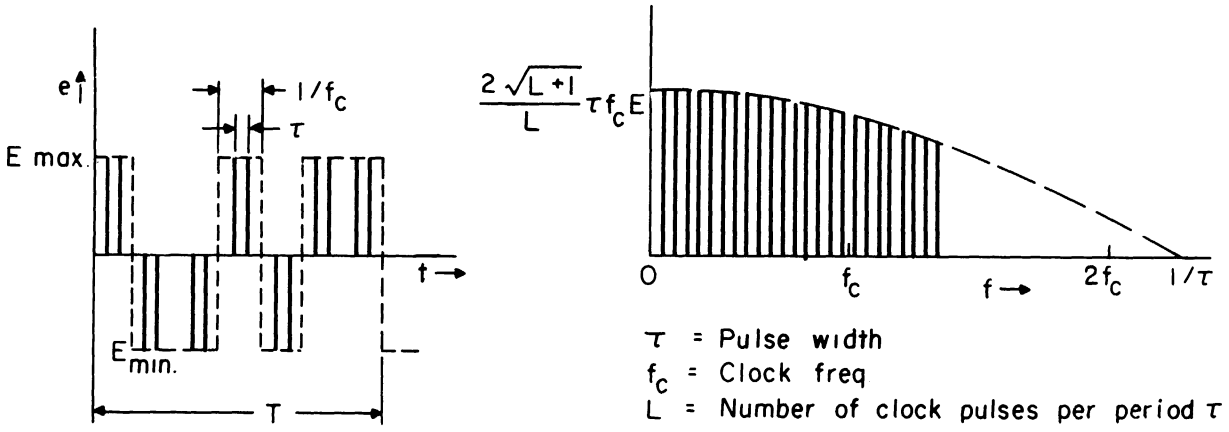
$$P_{avg} = \frac{1}{T} \int_0^T [e(t)]^2 \, dt = \frac{1}{T} E^2_{max} \, T = E^2_{max} \qquad (3.35)$$

The peak factor can be found from Eq. (3.10) to be

$$pf = \frac{2 E_{max}}{2\sqrt{\frac{2}{T} \int_0^T E^2_{max} \, dt}} = \frac{1}{2} = .707 \qquad (3.36)$$

From Eq. (3.36) it may be observed that the peak factor of the digitally-generated linear maximal sequence is a constant independent of the fundamental period T.

At this point it might prove interesting to investigate peak factor (pf) as a function of pulse width (τ) when the clock frequency (f_c) is held constant. The time function and frequency spectrum for this case are shown in Fig. 3.13. From the standpoint of increasing



(a) Time function (b) Frequency Spectrum

Fig. 3.13. Digitally-generated linear maximal sequence where $\tau < \frac{1}{f_c}$.

the amount of energy in the high-frequency components one must decrease the pulse width τ. The graph of Fig. 3.14 is a plot of peak factor vs.

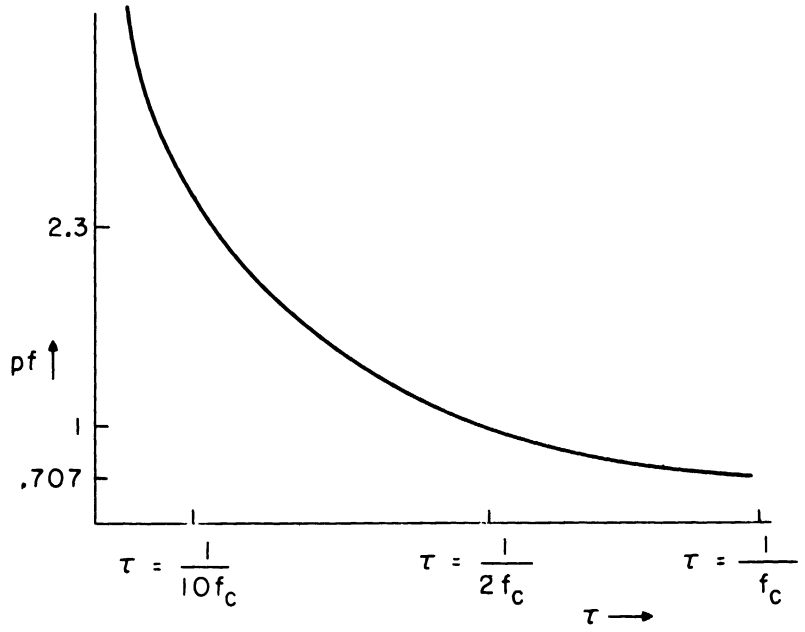


Fig. 3.14. Peak factor vs. pulse width (τ) for fixed clock frequency (f_c).

the pulse width. The peak factor ranges from a minimum value of .707 (point where $\tau = \frac{1}{f_c}$) to a maximum value of infinity (point where $\tau = 0$).

From the graph a reasonable range for f_c is

$$.25 \leq \tau f_c \leq 1 \tag{3.37}$$

In particular, for a peak factor of unity

$$\tau f_c = \frac{1}{2} \tag{3.38}$$

A basic shift register to which modulo-two adders have been added can be used to generate digital sequences (Ref. 16).[1] In

[1]Brief excerpts on the fundamental properties of shift-register-generator sequences have been taken from Ref. 16 and presented here.

the past the major use of a shift register was in the arithmetic unit of a digital computer. A shift register consists of a series of bistable elements with the capability of moving the contents in each element to the next element by means of a "shift" pulse. A shift register is thus a storage unit which moves its stored contents one position for each shift pulse.

To form a shift-register generator, modulo-two adders are added to form feedback loops. The addition table for modulo-two addition is shown in Fig. 3.15; circuits which operate according to this

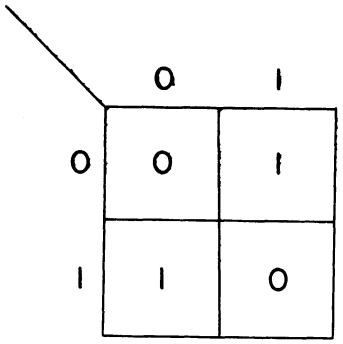


Fig. 3.15. Modulo-two addition table.

table are often referred to as "exclusive-or" circuits. There is no output when the inputs are alike, and there is an output whenever the inputs are different. Modulo-two addition can be viewed as ordinary addition written to the base two, where only the least significant digit is recorded.

A simple generator consisting of one adder along with the basic shift-register is shown in Fig. 3.16, where the numbers in the blocks refer to the bistable elements of the basic shift-register.

To see that this is truly a generator and not just a storage device, consider an initial storage of six ones. The next five inputs will all be zeros since the initial ones will continue to be shifted into both the fifth and sixth stages for five shifts. The total

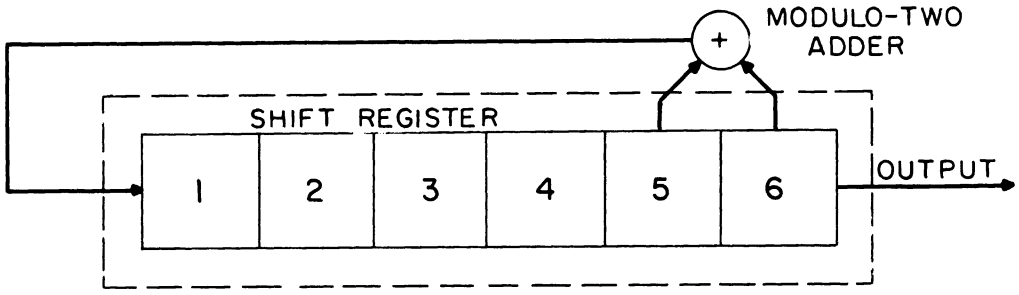


Fig. 3.16. A simple shift-register generator.

sequence has a period of sixty-three digits (compared to six for storage) and is repeated over and over.

When one connects a shift-register as a sequence generator, it is found that the output sequence is a function of the particular feedback connections made. Also, for some connections, the output sequence depends on the initial loading of the register. This has led to the grouping of the output sequences into two types: maximal sequences and nonmaximal sequences. This grouping is based on the "length" or "period" of the output sequence. For a given number of stages in a register, there exists a maximum to the number of digits which occur before the sequence begins to repeat itself. It is quite easy to establish this number. Consider a simple generator of n stages; if, as it is shifted, the register successively contains every combination of n zero-and-ones, the output sequence will be the largest possible. Since there are 2^n different n-digit binary numbers, this would seem to be the maximum period possible. However, the sequence generator cannot possess all zeros in its stages (if it did, the generator would remain in this state and produce

the all-zero sequence); for this reason the largest possible period for a linear n-stage shift register is 2^n-1. Thus if a given output sequence has a period equal to 2^n-1, then that sequence is called a maximal length sequence.

$$L = 2^n - 1 \tag{3.39}$$

where:

L = length of maximal length sequence

n = number of stages in the shift-register generator

Consider the six-stage generator shown in Fig. 3.16. With this connection, a sequence 63 long is obtained; since $2^6 - 1 = 63$, this is a maximal sequence.

If a given output sequence has a period shorter than L, that sequence is termed a nonmaximal length sequence.

The feedback connections of a generator determine whether the output sequence will be maximal or nonmaximal. Maximal sequences can be obtained from a generator with any number of stages (n). In this particular study interest will be in maximal sequences only, although nonmaximal ones could conceivably prove useful.

Returning to Eq. (3.38) where for unit pf, $\tau f_c = \frac{1}{2}$, and assuming that clock frequencies (f_c) in the order of 10^8 cycles are obtainable, then τ becomes

$$\tau = \frac{1}{2f_c} = .5 \times 10^{-8} = 5 \times 10^{-9} \tag{3.40}$$

$$\tau = 5 \text{ nsec}$$

Pulse widths of 5 nsec are well within the state-of-the-art.

Of the various methods presented for generating a discrete-frequency reference the shift-register-generator method is particularly interesting. The digitally-generated linear maximal sequence not only fulfills the condition of minimum peak factor while providing a reasonably uniform amplitude spectrum over a given band of interest, but is independent of the fundamental period T. From a practical point of view, the shift-register generator is simple to implement. Logic modules can be taken off the shelf and put together to form a discrete-frequency reference. At the present state-of-the-art, clock frequencies of 20 Mc are available which means that first zero locations of approximately 40 Mc in the $\frac{\sin x}{x}$ frequency spectrum are achievable with a unity peak factor.

By using clock dividers and coincidence gates in conjunction with the shift-register generator, it is possible to obtain any number of discrete-frequency references, each with different incremental step. In order to explain the method and the relevant properties of numbers considerations, the following example of dividing down by successive factors of 10 is developed.

The basic idea is that if one periodically samples a linear maximal sequence properly one obtains another linear maximal sequence with the same number of digits per period. The term "properly" means the sampling rate k and the number of digits $L = 2^n - 1$ have no common factors. In the example of dividing down by successive steps of 10 one must arrange that the period contains no factor of 5 or 2. Obviously, it contains no factor of 2 since L is an odd number. One must now choose the proper number of stage n so that 5 is not a factor

of L. This is not very restrictive since one may use any number of stages so long as they are not multiples of 4. The proof of this is given in Appendix B.

Under these conditions then it is possible to divide down the original sequence by a factor of 10 obtaining a second sequence with a spectral spacing $\frac{1}{10}$ as great. Dividing again by the same factor, a third sequence may be obtained with a spectral spacing $\frac{1}{100}$ of the original sequence. This simply means that if one were to start with a discrete-frequency reference of 10 components spaced 100 kc apart, additional sets of 10 spectral components could be derived spaced 10 kc, 1 kc, etc.

(c) The Parametric Method. A promising technique is discussed which is capable of presenting a uniform amplitude spectrum, one component at a time (as opposed to the entire reference spectrum), to the input of the phase-lock oscillator. In essence, this type of discrete-frequency reference can be thought of as a comb from which a single tooth can be selected at will. The principle component in this circuit is a parametric amplifier (Ref. 17). The equivalent circuit of a typical two-tank frequency converter is shown in Fig. 3.17. This model has tuned

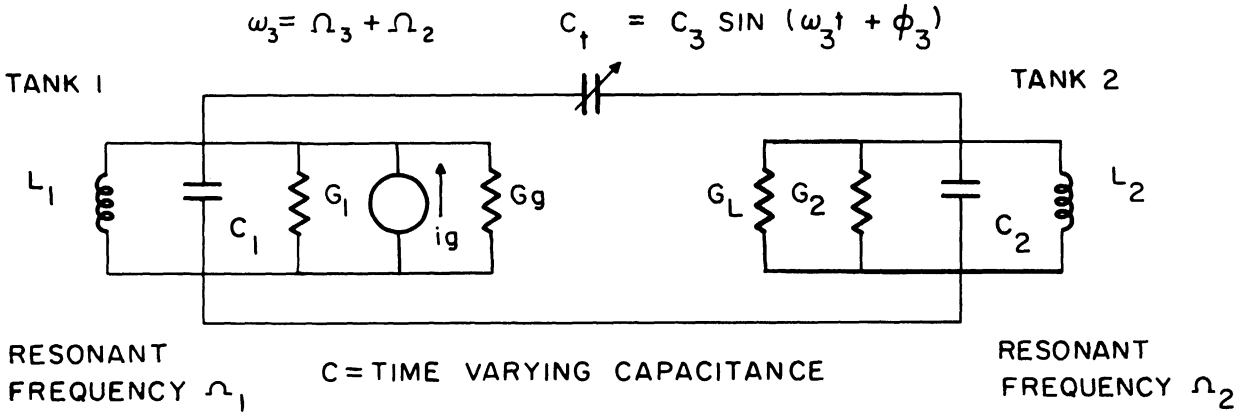


Fig. 3.17. An equivalent lumped circuit for the two-tank variable-parameter system.

circuits at both the signal frequency and at the "idler" or lower sideband frequency. (In the case of the lower-sideband up-converter, the idler frequency becomes the output frequency.)

The variable capacitance C_t serves to couple together the two high Q tank circuits of resonant frequencies Ω_1 and Ω_2, respectively. The variable capacitance is driven sinusoidally at a rate $\omega_3 = \Omega_1 + \Omega_2$. If a voltage exists across one of the tanks at its resonant frequency, a second voltage is developed across the second tank at its resonant frequency by the mixing action in the variable capacitance. The phase of the second voltage is automatically adjusted so that net energy flows into the tank circuits from the pumped capacitor.

Consider now the conditions for amplification. A signal generator, tuned to $\omega_1 \cong \Omega_1$ is coupled into tank 1 and an output load GL_2 is coupled into tank 2. The magnitude of the capacitor variation (C_t) is reduced to a value just below the point where oscillations occur. The signal generator is then responsible for the existence of $V(\omega_1)$ across tank 1. The mixing action in the variable capacitor will then result in producing $V(\omega_2)$ across tank 2. The converted signal, as is the case in mixer circuits where the local-oscillator frequency is higher than the input frequency, exhibits a modulation inversion since a signal $\omega_1 + \Delta\omega$ applied to the first tank gives rise to a signal $\omega_2 - \Delta\omega$ in the second tank.

In the practical operation of this system as a discrete frequency reference from which a single component may be selected at will, the input circuit would have to tune over a large frequency range, perhaps 10 to 1. The necessary adjustment of the amplifier in this case would be very difficult. Consequently, being limited by the present

state-of-the-art, operation with an untuned input is almost mandatory.

As described by Fisher (Ref. 18), the tuned circuit at the input may be eliminated to allow the design of a simple-to-adjust, tunable amplifier. The equivalent circuit of a single-resonance lower sideband up-converter is shown in Fig. 3.18. The parameters are the same as in Fig. 3.19.

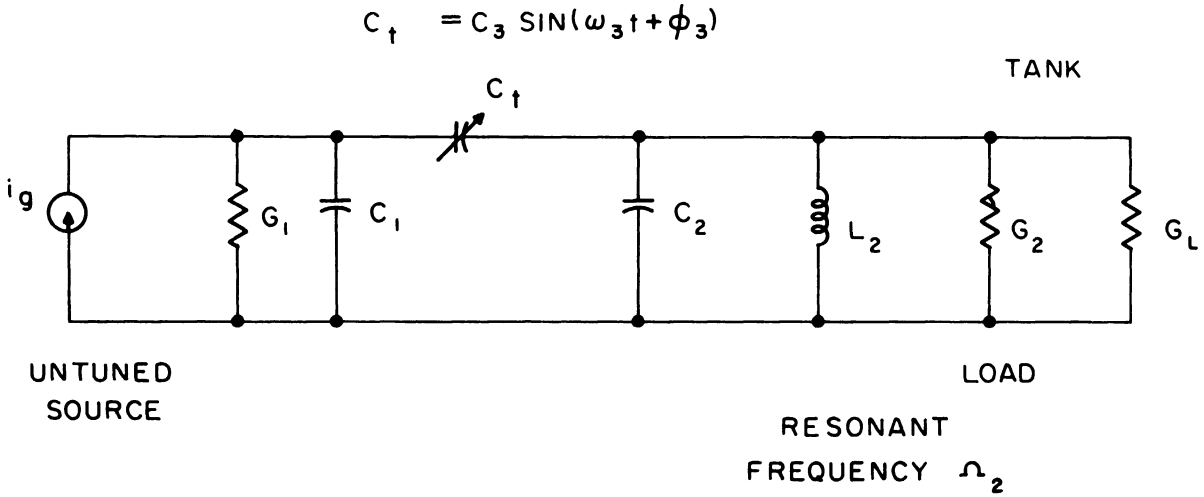


Fig. 3.18. Theoretical model of a single-resonance parametric amplifier.

Consider, as shown in Fig. 3.19, that the output of the

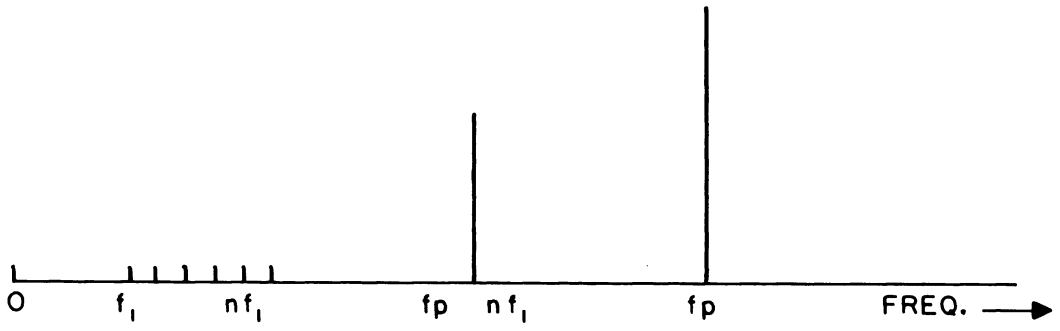


Fig. 3.19. Frequency spectrum of a single-resonance lower-sideband up-converter.

harmonic generator is a very low level frequency spectrum with components of nf_1 (where n is an integer). A lower sideband up-converter is used to convert a selected component of this spectrum to the frequency

$f_p - nf_1$. Even though the converter is untuned at the input, tuning at the difference frequency produces large regenerative gain at its low frequency image, and high rejection of unwanted mixing products or comb components is obtained.

The gain of the single-resonance lower-sideband up-converter is

$$G \approx G_o \frac{1}{1 + \frac{G_o}{B_T^2} (\omega_o - \omega_r)^2} \tag{3.41}$$

for $G_o >> 10$

where

ω_r = resonant frequency of the output tank after the pump (or local oscillator) frequency has been applied

ω_o = output frequency

G_o = midband gain of the output tank

B_T = bandwidth of the output tank before the pump is applied.

Let

$$1 + \frac{G_o}{B_T^2} (\omega_o - \omega_r)^2 = K \tag{3.42}$$

for $K > 10$

$$\frac{G_o}{B_T^2} (\omega_o - \omega_r)^2 >> 1 \tag{3.43}$$

Thus from Eq. (3.42)

$$K \cong \frac{G_o(\omega_o - \omega_r)^2}{B_T^2} \tag{3.44}$$

Define a term

$$B_K = 2(\omega_o - \omega_r) \tag{3.45}$$

where B_K is twice the spectral spacing of the discrete-frequency reference.

Substituting Eq. (3.45) into Eq. (3.44) and solving for the ratio of the $\frac{B_K}{B_T}$ one obtains

$$\frac{B_K}{B_T} \cong \sqrt{\frac{4K}{G_o}} \tag{3.46}$$

If the ratio of $\frac{B_K}{B_T} = 1$, then

$$K_{db} = G_{o_{db}} - 6 \text{ db} \tag{3.47}$$

Figure 3.20 is a plot of the ratio of the B_K/B_T versus the amplifier gain with K as the variable parameter. For a given ratio $\frac{B_K}{B_T}$, K shows the amount of spectral component suppression one would receive for a given value of gain.

To clarify this discussion somewhat, consider the example shown in Fig. 3.21. The solid curve is the pass-band of the output tank before the pump is applied. Assume the output frequency ω_o is at the resonant frequency ω_r and the adjacent two spectral components ω_a and ω_b are at the 3 db points (i.e., $\frac{B_K}{B_T} = 1$). Turn on the pump and adjust

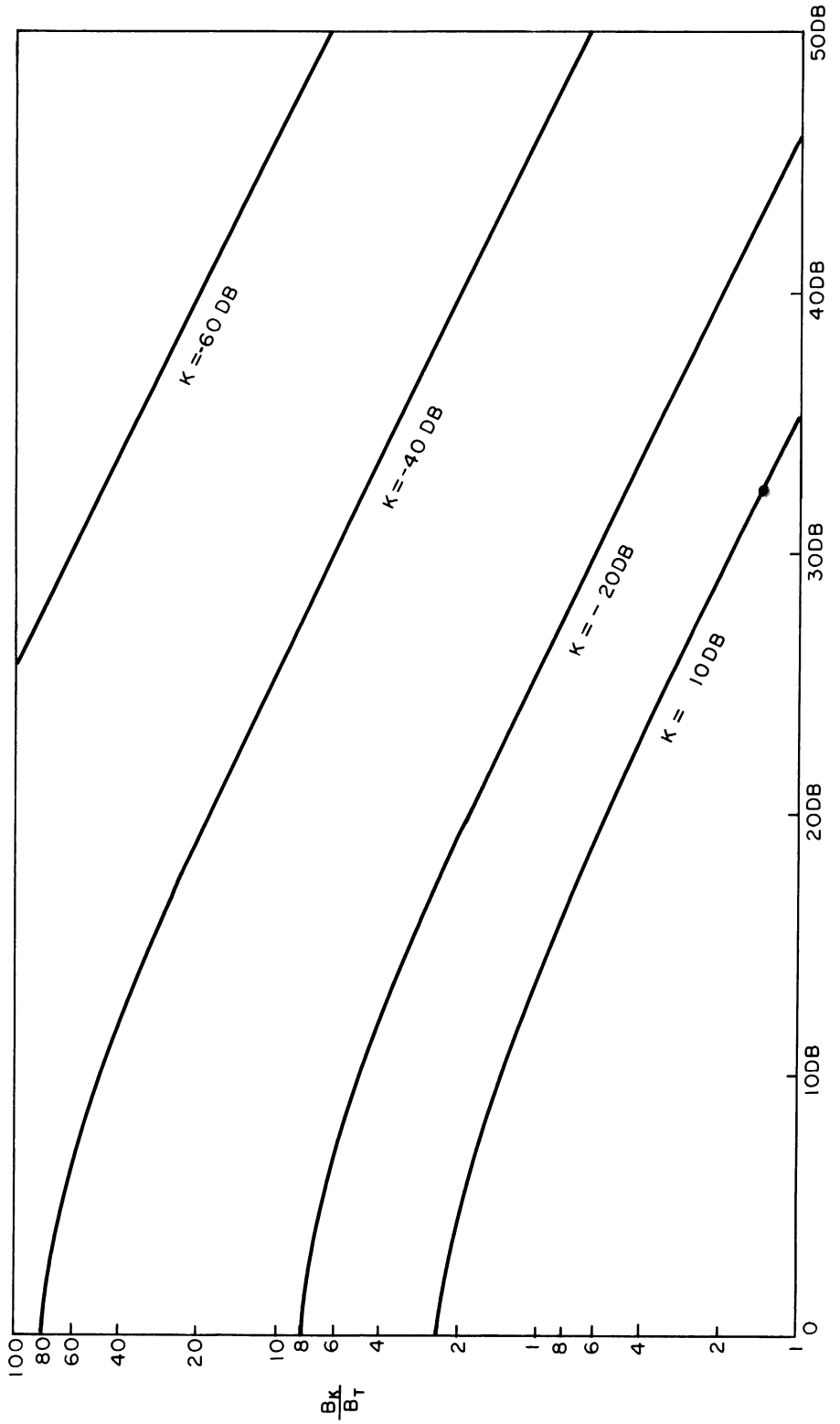


Fig. 3.20. Plot of $\frac{B_K}{B_T}$ vs. amplifier gain for a given K.

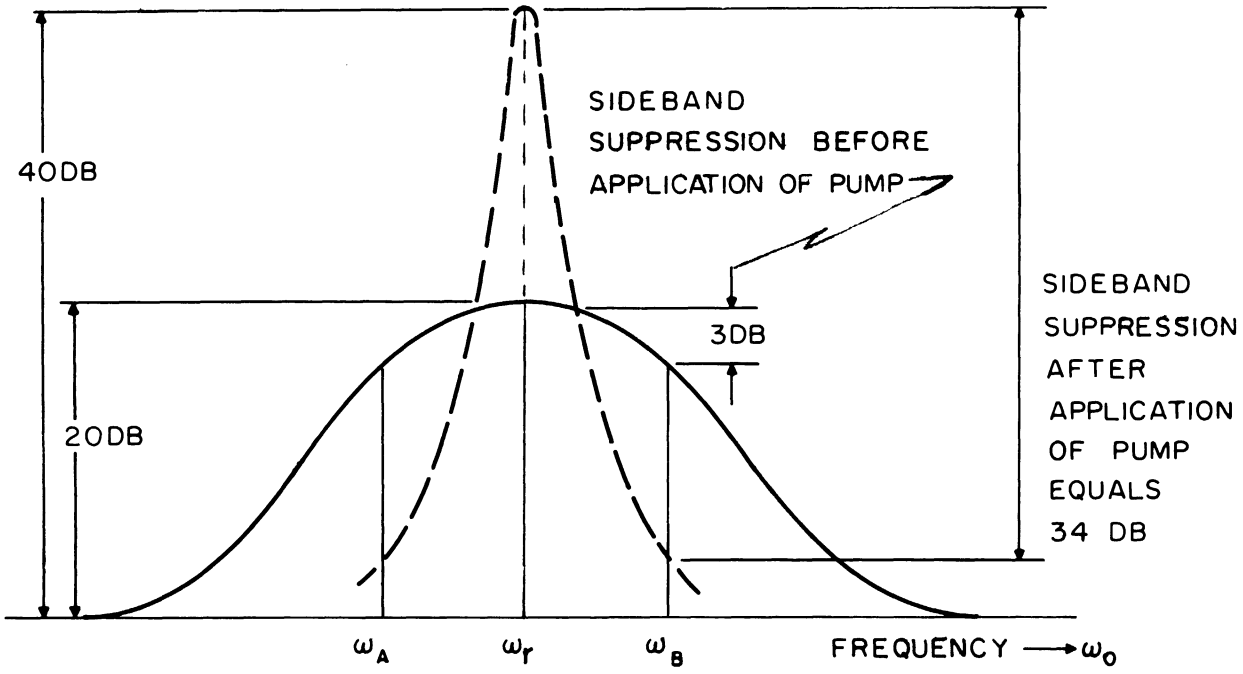


Fig. 3.21. Sideband suppression in output tank before (solid curve) and after (dotted curve) application of pump.

the power level until the gain of the amplifier is 40 db as indicated by the dotted curve. At this point it can be found from the chart of Fig. 3.20 that the gains of the two adjacent spectral components are suppressed by a factor of approximately 34 db.

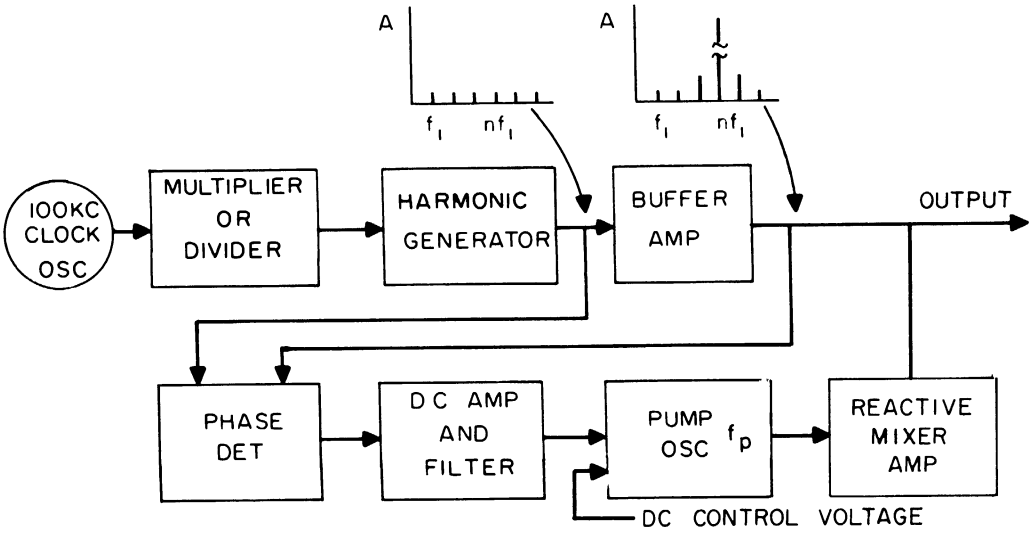
It is an inherent characteristic of a single resonance parametric amplifier that as pump power is increased the pass-band of the output tank not only narrows down but will actually shift in frequency; (this shift in frequency of the output tank reflects an inductive reactance into the input circuit which in effect peaks up the input signal at the desired frequency). In the final analysis then what was originally an untuned input (before pumping) becomes a wide range tuned input (with pumping). In the practical application of the device if it is desired

to tune from one value of n to another the pump is first disabled and a coarse tuning voltage applied to center the output pass-band over the desired value of n. The resonant frequency of the output tank will shift away from the desired value of n as the pump power is brought up to the level which will give the required suppression of adjacent spectral components. To correct for this shift a fine tuning voltage may be introduced by means of error-correcting circuits as shown in Fig. 3.22.

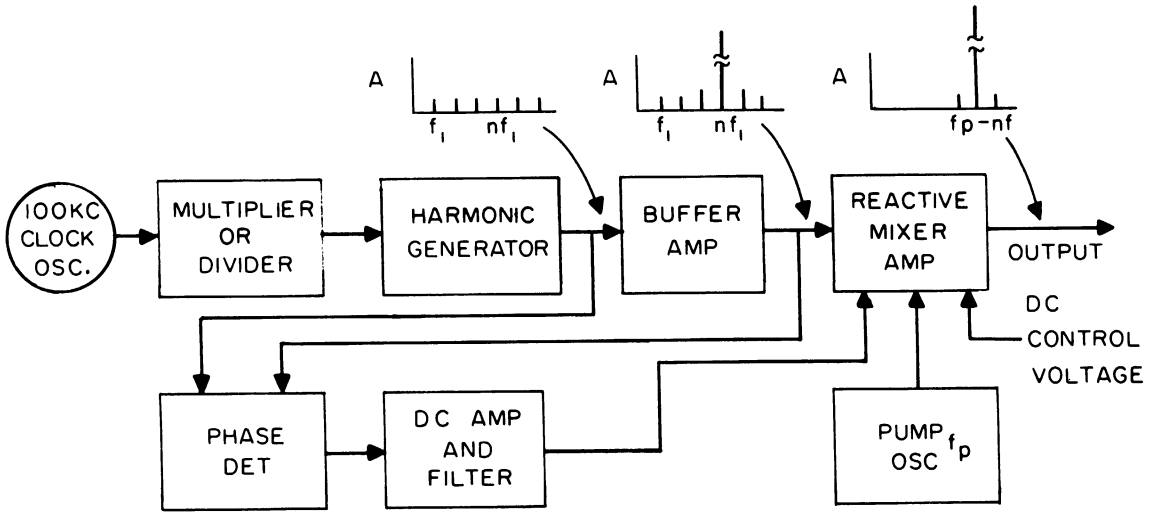
For either of the two above types the error-sensing circuit works in the same manner. The output of the comb generator (a low frequency, wideband spectrum) is applied to a buffer stage as well as the phase detector. Since the output of a buffer stage is the input to the low frequency tank at the reactive mixer, the signal at this point (also in or near lock) is essentially a sine wave with a frequency equal to one of the harmonics of the comb. The particular harmonic depends on the rough tuning voltage. The phase of this sine wave depends on the tuning of the idler tank in Type 1 and the pump in Type 2.

It is desirable to make the phase angle as small as possible in order to maximize the Q of the reactive mixer circuits. This is done by comparing the phase of the appropriate comb component and buffer amplifier output. This "error" signal is detected and amplified and then applied to either the pump or output tank respectively.

In conclusion, it should be noted that the technique of presenting a uniform amplitude spectrum, one component at a time, will simplify the design problems of the phase-lock loop. The adjacent spectral components of the discrete-frequency reference, if not attenuated, will appear as modulation at the output of the phase detector to modulate the VCO and produce undesirable FM components. The design of sharply



TYPE 1 FIXED TUNED OUTPUT TANK.
VARIABLE TUNED PUMP OSCILLATOR.



TYPE 2 VARIABLE TUNED OUTPUT TANK.
FIXED TUNED PUMP OSCILLATOR.

Fig. 3.22. Block diagram of error-correcting circuit for a single-resonance lower-sideband up-converter.

tuned rejection filters with little envelope phase delay (phase delay in the pass band results in a reduction of the capture and lock range of the system) is difficult to achieve, thus any prefiltering of the discrete-frequency reference will certainly lessen the design problems of the phase-lock loop.

(d) The Modulation Method. Both amplitude and frequency modulation techniques may be used to generate a given set of spectral components in the desired band of interest.

The amplitude modulation technique relies upon the fact that the spectrum of any periodic time function, e.g., the repetitive finite pulse, is symmetric about zero frequency. By multiplying the time function of a desired spectrum, centered about zero by some carrier frequency which is centered in the band of interest, the spectrum is effectively translated to the band of interest and the required number of spectral components which are evenly distributed on either side of the carrier frequency may be selected by means of a band-pass filter.

Consider the following amplitude-modulated wave

$$v = M_a(t) \quad Ve^{j\omega_o t} \tag{3.48}$$

where $M_a(t)$ the modulating function is the time function of the desired spectrum centered about zero and $Ve^{j\omega_o t}$ represents the carrier frequency centered in the band of interest. If the n^{th} frequency component of the modulating wave has the magnitude C_n, the modulating waveform can be represented as

$$M_a(t) = \sum_{n=-\infty}^{\infty} C_n e^{jn\omega_1 t} \tag{3.49}$$

where $t = \frac{2\pi}{\omega_1}$ the period of the modulating wave.

The Fourier Series expansion of the modulated wave is

$$v = V \sum_{n=-\infty}^{\infty} C_n e^{j\omega_o t} e^{jn\omega_1 t} \tag{3.50}$$

or

$$v = V \sum_{n=-\infty}^{\infty} C_n e^{j(\omega_o + n\omega_1)t} \tag{3.51}$$

Thus the spectrum of the amplitude-modulated wave is a symmetrical spectrum centered about ω_o as pictured in the sequences of Fig. 3.23 shown below.

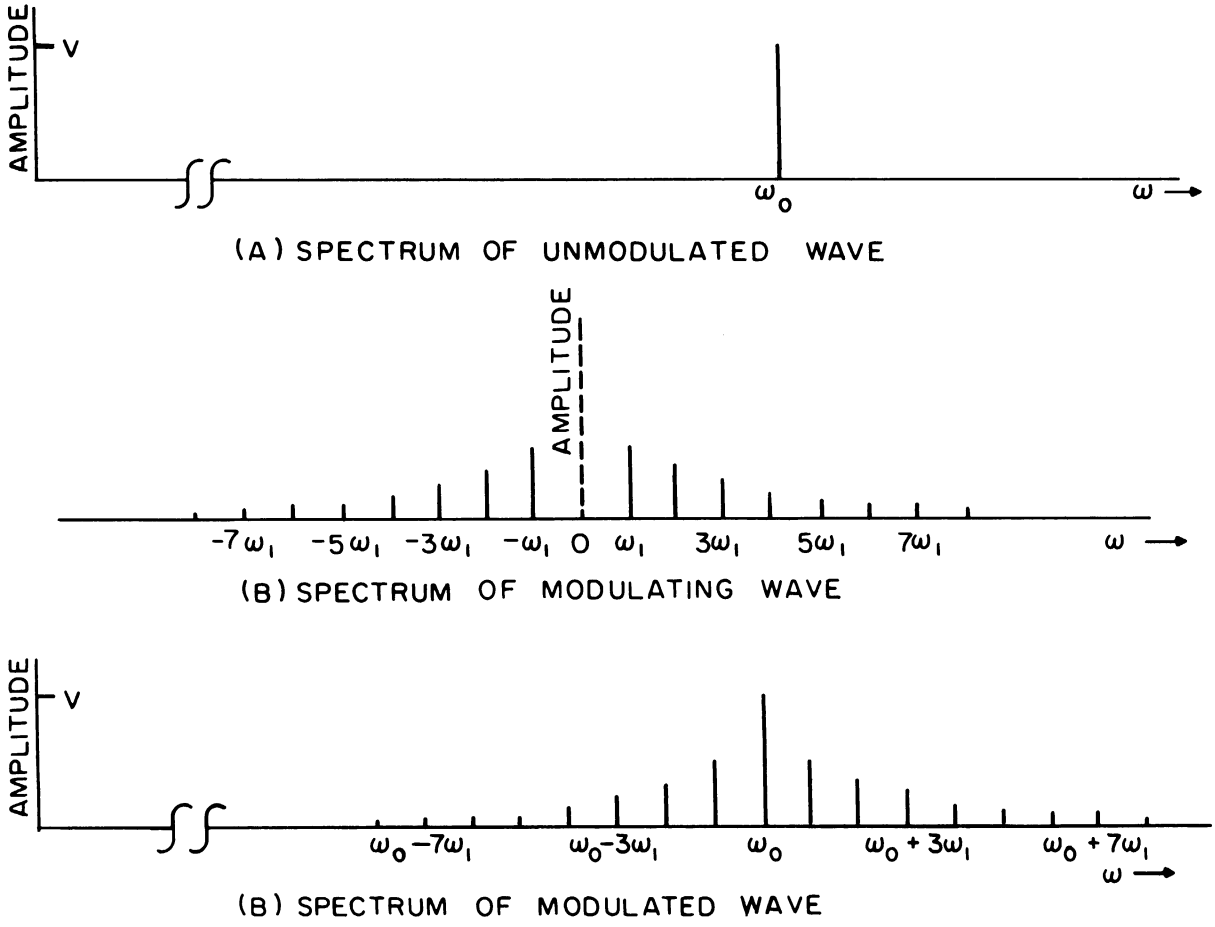


Fig. 3.23. Spectrum of an AM wave.

If the band of interest is small compared to the carrier frequency, it would seem advantageous to use a pulse wide enough to generate a spectrum where the first zero occurs at a point somewhat beyond the frequency equal to the half-bandwidth desired. If this pulse were then used to amplitude-modulate a carrier centered in the band of interest, a relatively large amount of the total energy would be concentrated in the band of interest and the time waveform would have a much lower peak factor than if the repetitive impulse method (method a) were used. A comparison of the repetitive impulse method (method a) and the amplitude modulation method (method d) are shown in Fig. 3.24 below.

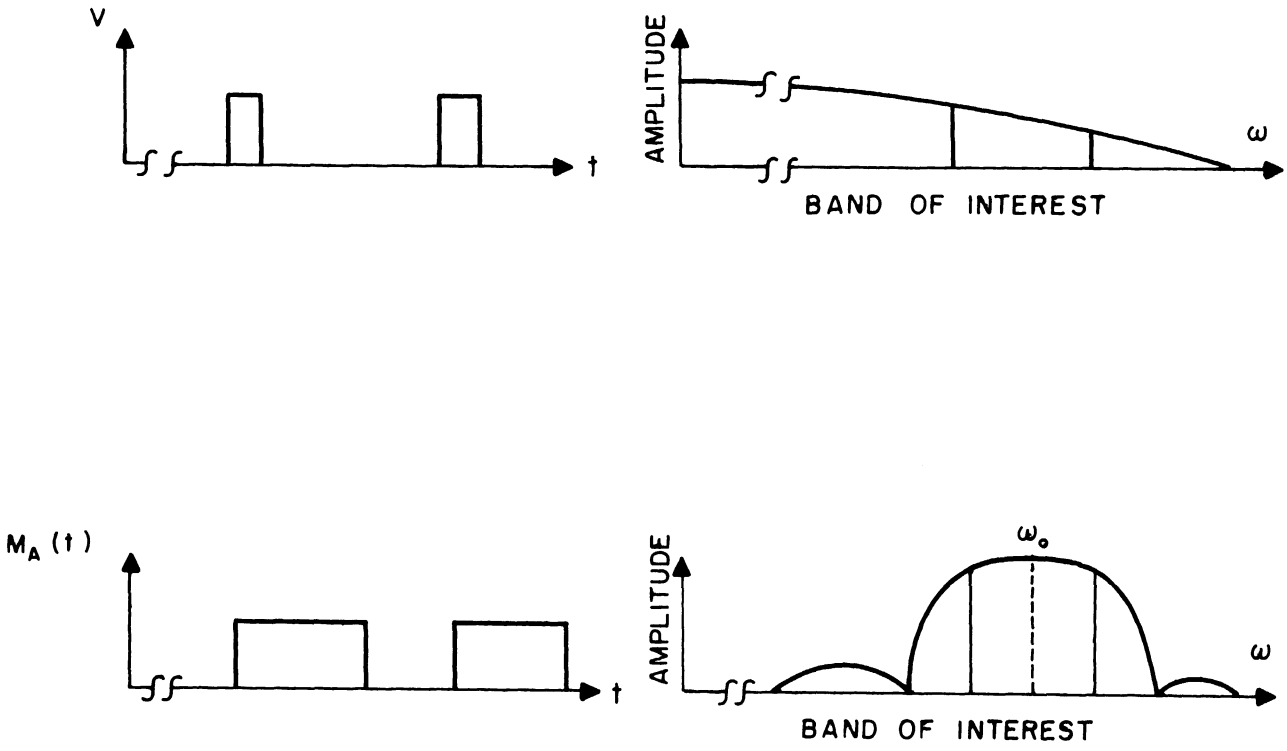


Fig. 3.24. Comparison of the repetitive finite pulse and the amplitude-modulation techniques.

The frequency modulation technique relies upon a rule which can be used intuitively as a general principle. The principle may be stated as follows: The spectral contributions of an FM wave are functions of the rate of change of frequency during the entire cycle; the longer the frequency of an FM wave remains in a certain range of frequencies, the greater will be the spectral contributions in that frequency range.

Based on the above principle, the only FM waveform that will generate a spectrum of uniform amplitude components is a linear function of time. Consider a modulating function of the type

$$M_f(t) = \omega_o + \Delta\omega - \frac{2\Delta\omega}{T} t \qquad (3.52)$$

A sketch of this function is shown in Fig. 3.25.

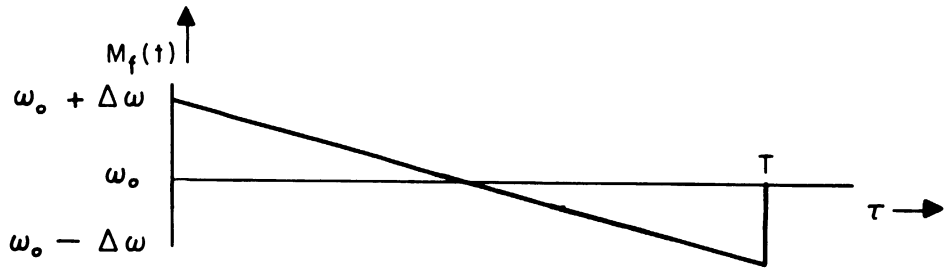


Fig. 3.25. Linear FM waveform.

The modulated waveform is given by

$$v = V \cos[(\omega_o + \Delta\omega)\, t - \frac{2\Delta\omega}{T}\, t^2] \qquad (3.53)$$

The amplitude of the spectral components is therefore

$$C_n = \frac{V}{T} \int_o^T e^{-j\frac{2n\pi}{T} t} \times \cos[(\omega_o + \Delta\omega)\, t - \frac{2\Delta\omega}{T}\, t^2]\, dt \qquad (3.54)$$

This integral is in general quite difficult to evaluate; however, by means of numerical methods and with the aid of the computer it can be evaluated.

The spectrum of the frequency modulated wave is sketched below in Fig. 3.26.

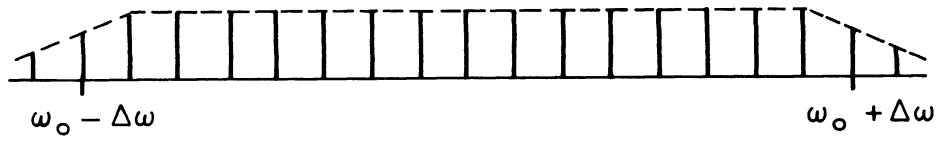


Fig. 3.26. Frequency spectrum of the linear FM waveforms.

The sawtooth wave would yield an even flatter spectrum if the corners of the time function were rounded off.

In conclusion, both AM and FM techniques would be quite simple to implement. The FM wave, although somewhat more difficult to analyze, does have a very low peak factor. In fact, the peak factor is unity, the same as that of a sine wave.

Although the major part of the section has dealt with the spectra of easily generated time functions such as rectangular pulses, triangular waveforms, etc., other time waveforms may yield very interesting spectra. One possible technique for finding useful time waveforms is to determine the inverse Fourier transform of the envelope of the desired spectrum. The resulting time waveform is aperiodic but it can be made periodic by cutting the waveform off at some time and repeating the wave. Where one should cut depends upon the waveform and upon the requirements of the desired spectrum. Two possible transforms and sketches of both frequency and time functions are shown.

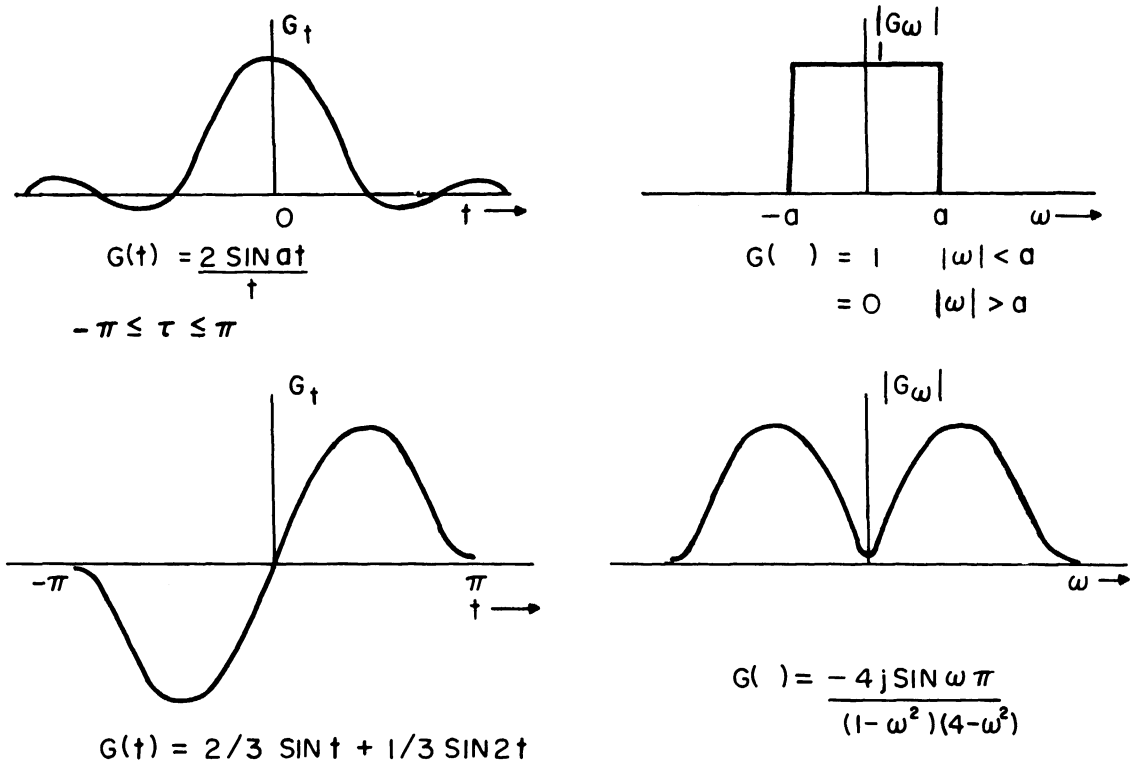


Fig. 3.27. Examples of useful spectra and their associated time waveforms.

It is interesting to note that in the sketch of Fig. 3.27(a) the time function is made periodic by cutting off the wave at the point where the 3rd zero occurs and repeating the waves. In Fig. 3.27(b) it is not necessary to cut off the wave since the time function is already periodic.

3.2.3 Summary. A study and evaluation of the various methods for the efficient production of high-order harmonics with balanced energy distribution in the frequency band of interest has been carried out.

The concept of peak factor has been analyzed and a relationship which can be effectively used as a figure of merit in the design of an appropriate frequency spectrum has been developed. The method used to generate the discrete-frequency reference will, in general,

depend upon the final design conditions imposed. For example, if the desired number of spectral components is not large and the band of interest is high in frequency, it is advantageous to use AM or FM modulation techniques. If the band of interest is high in frequency and a number of very closely spaced spectral components are required, the parametric method may prove very useful since it provides a high degree of adjacent spectral component suppression. The shift-register generator method provides a good general technique which reduces to practice very easily and can be used under a wide variety of conditions.

3.3 Phase-Lock Oscillator

A vital element of the discrete-frequency generator (DFG) is the phase-lock oscillator (PLO) or automatic-phase control (APC) system as it is sometimes called. There are varied and sometimes conflicting uses for a phase-lock oscillator, e.g., a PLO system can be used to reduce the jitter or frequency noise of a high power oscillator such as a klystron or with somewhat different design parameters, it can be used in a receiver to increase the power level and attenuate the noise of a weak FM signal. In the frequency synthesis field which involves the generation and selection of a single frequency signal, a poor signal-to-noise ratio may result--the noise in this case taking the form of adjacent frequency components of the reference generator and small deviation FM or phase jitter of the desired component. A PLO can be used as a high-Q filter to select a desired signal, attenuate unwanted components, and reduce phase jitter.

In addition, a PLO can be used to track input frequency changes, e.g., Doppler shift of satellites, for sweep synchronization of the color sub carrier in the color-television system and for FM discriminators.

In the case of the generalized discrete frequency synthesizer the PLO would ideally have a wide acquisition and lock range, a very rapid lock-in capability and small noise bandwidth. These features, as it will be shown, are not fully compatible.

Many articles have attempted to describe the various performance factors of the PLO loop but no one of these articles is sufficiently complete for our present purposes (Refs. 19 and 20).

In the following sections, an analysis will be made of those properties which determine acquisition and lock range. convergence times, output spectral purity and frequency range of operation.

Acquisition range is the largest unlocked frequency difference at which synchronization will occur. The lock range is the total drift in the unlocked oscillator which can be exactly compensated by the locked system. Convergence time is the total time it takes to go from one locked frequency to another. The output spectral purity depends upon the filter bandwidth of the system which in turn expresses the performance of the system as a low-pass filter with respect to FM noise components existing in the input to the system and as a high-pass filter with respect to FM noise components generated within the output oscillator. In addition, techniques for optimizing PLO loop performance to allow their use in a synthesizer satisfying a specific need and an evaluation of the limits of operation subject to the present state-of-the-art will be presented.

3.3.1 Theory of Operation. The elements of a typical phase-lock loop are shown in Fig. 3.28. Reference signal input to such a loop may be assumed to be $E_i \sin \theta_i(t)$.

The output of the voltage-controlled oscillator (VCO) is given

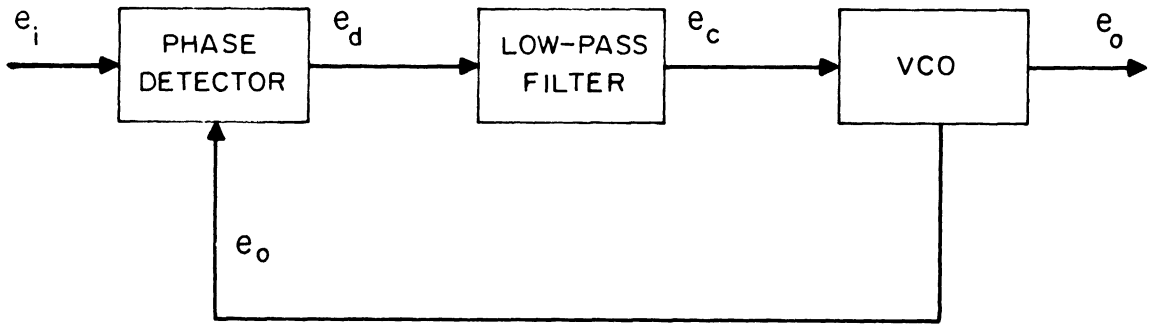


Fig. 3.28. Block diagram of phase-lock loop.

$$e_o(t) = E_o \sin \theta_o(t) \tag{3.55}$$

where

$$\theta_o(t) = \omega_c(t) + \theta(t) \tag{3.56}$$

Substituting Eq. (3.56) into Eq. (3.55) one obtains

$$e_o(t) = E_o \sin [\omega_c t + \theta(t)] \tag{3.57}$$

The voltage $e_o(t)$ has a frequency associated with it given by

$$\dot{\theta}_o(t) = \omega_o t = \omega_c + \dot{\theta}(t) \tag{3.58}$$

and this frequency is observed to consist of a constant determined by the rough-tuned or free-running frequency of the oscillator ω_c plus a time-varying term proportional to the actuating signal.

Briefly, the operating principles of such a loop are as follows: The phase detector can be mathematically represented as a multiplier and operates in this system to give

$$e_d = e_i(t) \times e_o(t) \tag{3.59}$$

$$= [E_i \sin \theta_i(t)] \times [E_o \sin \theta_o(t)] \tag{3.60}$$

$$= \frac{E_i E_o}{2} \left\{ \cos [\theta_i(t) - \theta_o(t)] - \cos [\theta_i(t) + \theta_o(t)] \right\} \tag{3.61}$$

Since the filter following the multiplier is low-pass, it will not pass the sum frequency term, thus the multiplier output e_d is proportional to the cosine of the difference phase.

$$e_d = K_1 E_i E_o \cos \theta(t) \tag{3.62}$$

where

$$\theta(t) = \theta_i(t) - \theta_o(t) \tag{3.63}$$

and K_1 is the sensitivity of the phase detector $(\frac{1}{\text{rad. volts}})$.

If it is assumed that the multiplier is a balanced phase detector composed of peak-detecting diodes, and if the VCO output voltage E_o is much greater than the reference signal voltage E_i, then a simplified form of the multiplier output voltage can be derived. As shown in the vector diagram of Fig. 3.29 one of the detector diodes is fed with the sum of E_o and $\frac{E_i}{2}$, the other is fed with the difference of these two vectors. The resulting rectified voltages E_{d_1} and E_{d_2} can be established by trignometric relations.

$$E_{d_1}^2 = \frac{E_i^2}{4} + E_o^2 - E_i E_o \cos \theta \tag{3.64}$$

$$E_{d_2}^2 = \frac{E_i^2}{4} + E_o^2 + E_i E_o \cos \theta \tag{3.65}$$

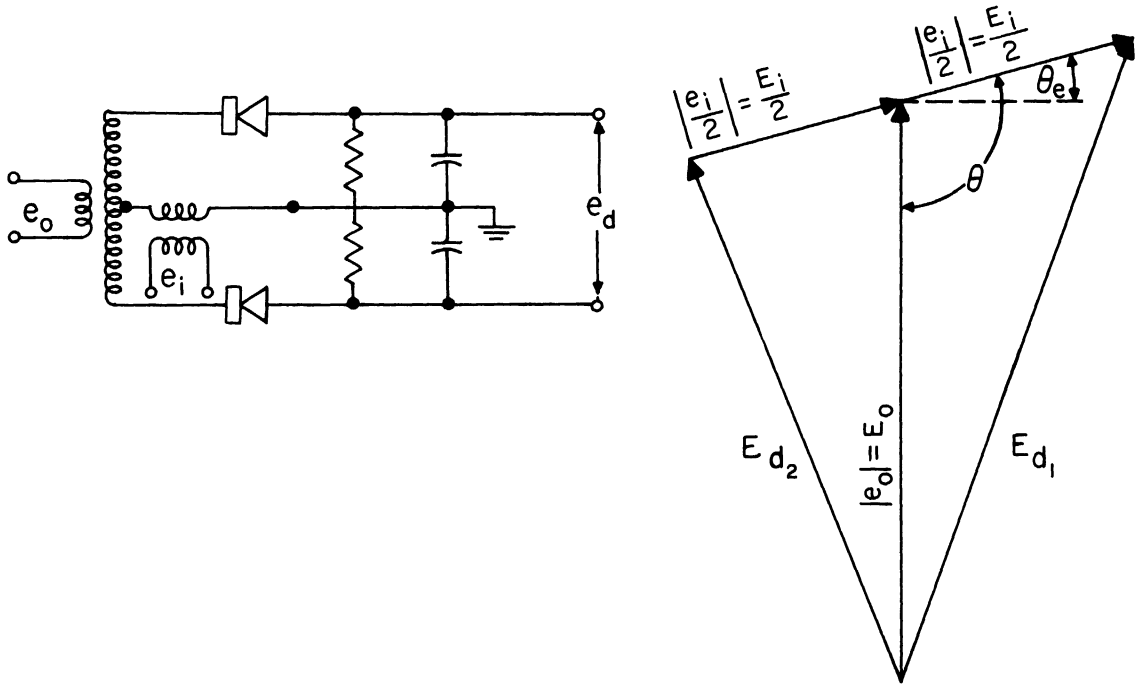


Fig. 3.29. Circuit and vector diagrams of phase-detector circuit.

The phase-detector voltage is equal to the difference of the rectified voltages, i.e.,

$$e_d = E_{d_1} - E_{d_2} \tag{3.66}$$

Subtracting Eq. (3.65) from Eq. (3.64) one obtains

$$e_d = E_{d_1} - E_{d_2} = \frac{-2\, E_i\, E_o \cos\theta}{E_{d_1} + E_{d_2}} \tag{3.67}$$

If

$$E_o \gg E_i$$

$$E_{d_1} + E_{d_2} = 2E_o \tag{3.68}$$

Substituting Eq. (3.68) into Eq. (3.67) one obtains

$$e_d = E_{d_1} - E_{d_2} = - E_i \cos \theta \tag{3.69}$$

Since $\theta = \theta_e + \pi/2$, Eq. (3.69) becomes

$$e_d = E_i \sin \theta_e \tag{3.70}$$

One can see that due to the balanced nature of the phase detector the dc voltage due to the VCO has been removed. In addition, for a large VCO output voltage the multiplier output voltage e_d is independent of the output level of the VCO.

Denoting the linear transfer function of the loop filter as $F(p)$, the VCO control voltage becomes, in the general case,

$$e_c = F(p)\, K_1\, E_i\, E_o \sin \theta_e(t) \tag{3.71}$$

Assuming the frequency of the output of the VCO consists of a constant equal to the free-running frequency of the oscillator ω_c, plus a time-varying term proportional to the actuating signal, and assuming furthermore that the VCO has a linear control characteristic $K_2(\frac{\text{rad/sec}}{\text{volt}})$, then the oscillator output frequency becomes

$$\omega_o(t) = \omega_c + K_2\, e_c \tag{3.72}$$

$$\omega_o(t) = \omega_c + F(p)\, K_1 K_2\, E_i\, E_o \sin \theta_e(t) \tag{3.73}$$

The output phase $\theta_o(t)$ becomes

$$\theta_o(t) = \int_o^t \omega_o(t)\, dt = \omega_c t + \int_o^t K_1\, K_2\, F(p)\, E_i\, E_o \sin \theta_e(t)\, dt \tag{3.74}$$

Substituting $\theta_e(t) = \theta_i(t) - \theta_o(t) - \pi/2$ into Eq. (3.74) one obtains

$$\theta_e(t) = \theta_i(t) - \omega_c t - \int_o^t K_1 K_2 F(p)\, E_i E_o \cos \theta_e(t)\, dt - \pi/2 \tag{3.75}$$

Differentiating both sides of the equation (3.75) yields

$$P\theta_e = P\,\theta_i - \omega_c - K_1 K_2 F(p)\, E_i\, E_o \sin \theta_e \tag{3.76}$$

rearranging gives

$$P\theta_e + K_1 K_2 F(p)\, E_i\, E_o \sin \theta_e = P\theta_i - \omega_c \tag{3.77}$$

The product $K_1 K_2\, E_i\, E_o$ may be defined as K, the gain constant, and has the dimensions of radians per second. K represents the maximum frequency shift at the output of the system per radian phase shift at the input.

The equation may now be written

$$P\,\theta_e + KF(p) \cos \theta_e = P\,\theta_i - \omega_c \tag{3.78}$$

This equation represents the general differential equation of the PLO loop. $P\,\theta_e$ is the instantaneous difference frequency between the reference signal and the VCO signal. $P\,\theta_i$ is the instantaneous frequency of the reference signal while ω_c is the free-running VCO frequency.

The simplest loop is one in which the loop filter has no energy storage elements (i.e., produces a constant transfer ratio F(p) = 1). If the difference frequency between the reference signal and the free-running VCO signal is defined as

$$\Delta\omega = P\,\theta_i - \omega_c = \omega_i - \omega_c \tag{3.79}$$

and is constant, the steady-state solution

$$\cos \theta_e = \frac{\Delta\omega}{K} \tag{3.80}$$

This means the system has a steady-state phase error which is proportional to the initial set-on error $\Delta\omega$ and inversely proportional to the gain constant K. Since the maximum value of $\cos \theta_e = \pm 1$, the system will acquire and stay in lock over a frequency range

$$|\Delta\omega|_{\text{lock range}} \leq K \tag{3.81}$$

Figure 3.30 is a plot of $P\,\theta_e$ vs. θ_e for a given constant set-on error of $\Delta\omega$ and describes the operation of the system. For lock-on to occur, the error frequency curve must intersect the abscissa--at the point where the VCO output frequency equals the reference frequency. There are two possible intersections, but only one of these is stable, the other corresponds to a condition of positive rather than negative feedback. If the frequency error $P\,\theta_e$ is positive, the phase error θ_e tends to increase; for negative frequency error, θ_e decreases. The stable intersection is called the locked operating point and indicates the

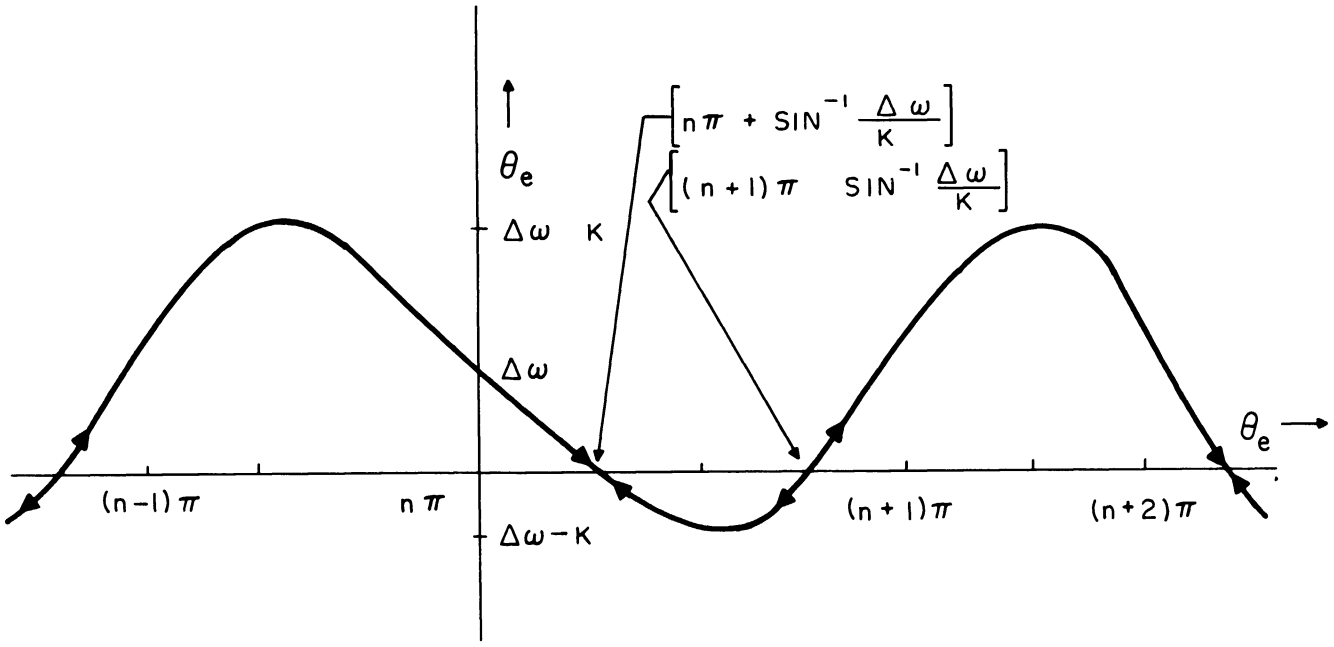


Fig. 3.30. First-order loop pull-in behavior (n even integer).

phase error θ_e required to maintain lock. If the frequency of the VCO drifts, it will remain locked but the operating point will move toward one end of the stable region. At $|\Delta\omega| > K$ the VCO will unlock and continuous frequency modulation of the oscillator will result.

Under the assumption that the phase error is small, Eq. (3.78) may be linearized by substituting

$$\theta_e \sim \sin \theta_e \text{ for } \frac{-\pi}{2} < \theta_e < \frac{\pi}{2} \tag{3.82}$$

Using the linearizing assumption and letting the transfer ratio F(p) = 1, Eq. (3.78) becomes

$$P(\theta_i - \theta_o) + K(\theta_i - \theta_o) = P\,\theta_i \tag{3.83}$$

$$P\,\theta_o + K\,\theta_o = K\,\theta_i \tag{3.84}$$

This leads to a transfer function

$$\frac{\theta_o}{\theta_i}(P) = \frac{K}{P + K} \tag{3.85}$$

Using LaPlace transforms, the transient response of the loop to a sudden step of input phase $|\theta i|$ becomes

$$\frac{\theta_o\,(P)}{\theta_i\,(P)} = \frac{K}{p(p + K)} \tag{3.86}$$

which in the time domain becomes

$$\frac{\theta_o}{|\theta_i|}(t) = 1\text{-}e^{-Kt} \tag{3.87}$$

A plot of the transient response of the system for F(p) = 1, i.e., a direct connection between the phase detector output and the oscillator control stage is shown in Fig. 3.31. It should be noted that

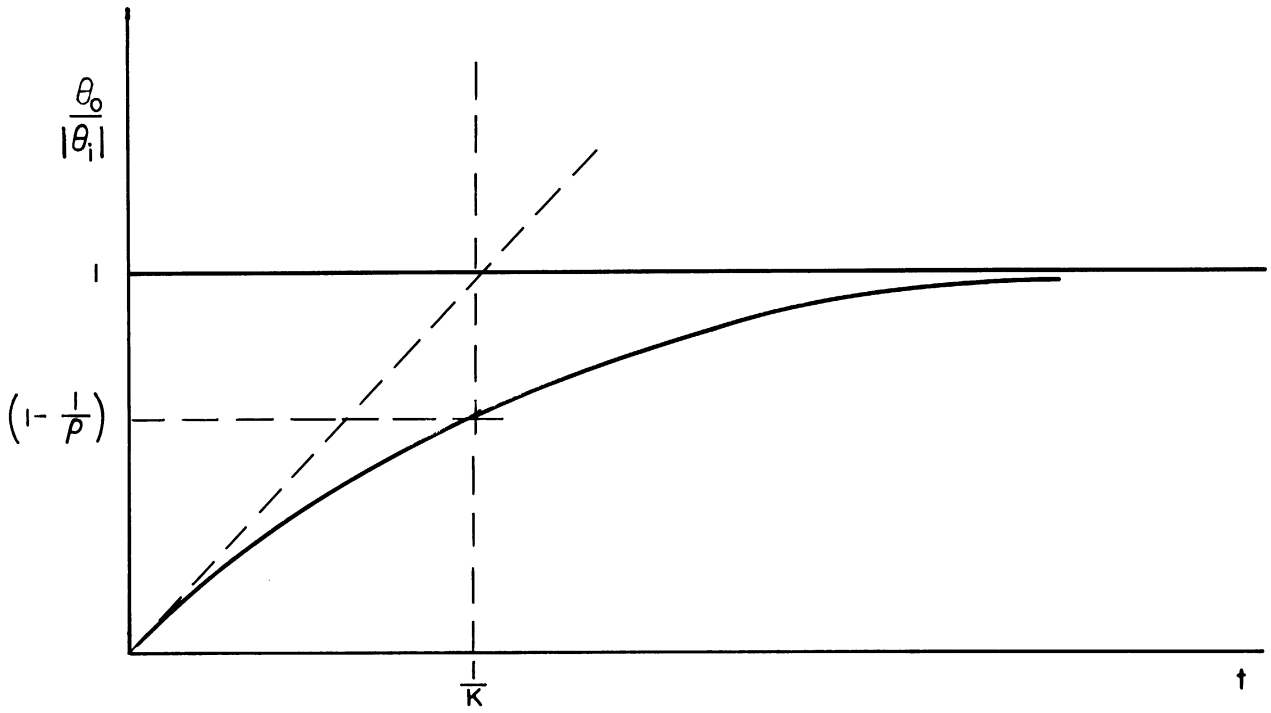


Fig. 3.31. Transient response plot of $\frac{\theta_o}{|\theta_i|}(t) = 1\text{-}e^{-Kt}$.

for large error angles the transient response will be slower than shown on Fig. 3.31 because of the error in the approximation $\theta_e = \sin \theta_e$.

The frequency response of the system is found by comparing the steady-state sinusoidal waveform of θ_o with that of θ_i for a sinusoidal θ_i input

$$\frac{\theta_o}{\theta_i}(j\omega) = \frac{1}{1 + j\frac{\omega}{K}} \tag{3.88}$$

The simple loop behaves like an RC filter and has a cut-off frequency[1] of

[1] Cut-off frequency ω_c is defined as that frequency where the loop gain is down by a factor of 3 db.

$$\omega_c = K \tag{3.89}$$

The complete frequency response locus of the system is shown in Fig. 3.32.

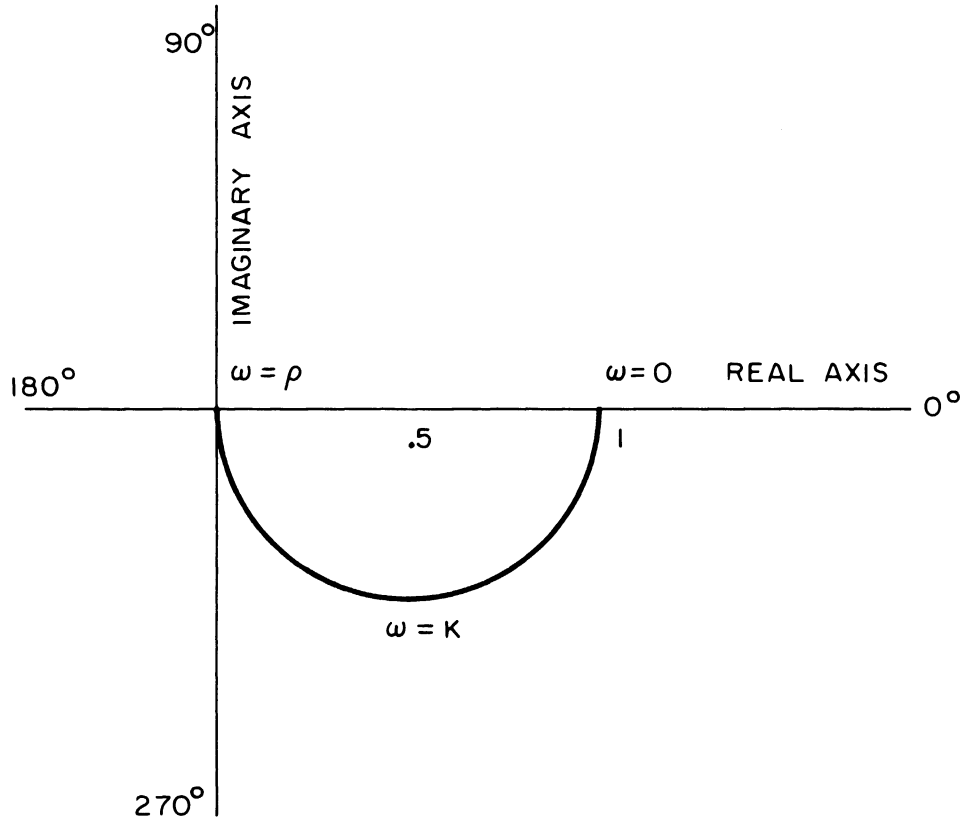


Fig. 3.32. Frequency response plot of $\frac{\theta_o}{\theta_i}(j\omega) = \frac{1}{1 + j\frac{\omega}{K}}$.

The mean-square phase fluctuation at the output of the locked oscillator loop will be equal to the input noise-to-signal ratio times the ratio of power gain for noise and signal. Since the signal has an infinitesimal bandwidth, and since the noise power may reasonably be expected to be spread uniformly over a wide band, the output noise-to-signal ratio or mean-square phase fluctuation as shown by George (Ref. 21)

will be equal to the ratio of input noise spectral density to signal power ratio times the noise bandwidth of the closed-locked oscillator loop.

The noise bandwidth of the system is the integral with respect to frequency of the magnitude of the gain transfer function of the loop. This gain transfer function is given in Eq. (3.88). The noise bandwidth is then found to be:

$$B = \int_0^\infty \left| \frac{\theta_o}{\theta_i} (j\omega) \right|^2 d\omega \tag{3.90}$$

Note that the integral is taken only from zero to infinity because of the low-pass output of the phase detector. Alternatively, we might say that only half the noise gets to the phase detector, that is, that half which is in phase with the reference signal.

Equation (3.88) can be substituted into Eq. (3.90) and the integration carried out to yield

$$B = \frac{\pi}{2} K \text{ rad/sec} \tag{3.91}$$

This means the system has a noise bandwidth (B) which is proportional to the gain constant K.

Pull-in time may be determined for the first-order loop by use of Eq. (3.78) in the following manner.

Let $F(P) = 1$ and $P\,\theta_i - \omega_c = \Delta\omega$

Equation (3.78) then becomes

$$P\,\theta_e + k \sin \theta_e = \Delta\omega \tag{3.92}$$

where θ_e is the instantaneous phase error between the reference signal

and the VCO signal.

Since

$$P\,\theta_e = \frac{d\theta_e}{dt}$$

Equation (3.92) can be rewritten as

$$\frac{dt}{d\theta_e} = \frac{1}{\Delta\omega - K \sin \theta_e} \tag{3.93}$$

whence the pull-in time is given by

$$t = \int_{\theta_{e\ initial}}^{\theta_{e\ final}} \frac{d\theta_e}{\Delta\omega - K \sin \theta_e} \tag{3.94}$$

Since $\theta_{e\ final} = \sin^{-1} \frac{\Delta\omega}{K}$, it is observed that the pull-in time (t) will be infinite. This is to be expected since the Lipschlitz[1] condition as described by Rauch (Ref. 22) is not violated at the singular point. Actually we are interested in the time required to obtain a zero difference frequency. A reasonable approximation to this time may be obtained by integrating Eq. (3.94) to a value of θ_e such that a one cycle difference frequency exists. This is given by

$$\Delta\omega - K \sin \theta_{e1} = 1 \tag{3.95}$$

or

$$\theta_{e1} = \sin^{-1} \left(\frac{\Delta\omega - 1}{K} \right) \tag{3.96}$$

Define a zero difference frequency time t_{ZDF} such that

---

[1] $|\Delta\omega - K \sin \theta_e' - \Delta\omega + K \sin \theta_e''| = K\,|\sin \theta_e' - \sin \theta_e''| \leq C|\theta_e' - \theta_e''|$
where $C \geq K$.

$$t_{ZDF} = \int_{\theta_{e\ initial}}^{\theta_{el}} \frac{d\theta_e}{\Delta\omega - K \sin\theta_e} \quad \text{where } K^2 > \Delta\omega^2 \tag{3.97}$$

$$= \frac{1}{\sqrt{K^2 - \Delta\omega^2}} \ln \frac{-K + \Delta\omega \sin\theta_e - \sqrt{K^2 - \Delta\omega^2}\cos\theta_e}{\Delta\omega - K\sin\theta_e} \Bigg|_{\theta_{e\ init.}}^{\theta_{el}} \tag{3.98}$$

$$= \frac{1}{\sqrt{K^2 - \Delta\omega^2}} \ln \left[\frac{\dfrac{-K + \Delta\omega \sin\theta_{el} - \sqrt{K^2 - \Delta\omega^2}\cos\theta_e}{\Delta\omega - K\sin\theta_e}}{\dfrac{-K + \Delta\omega \sin\theta_{e\ init.} - \sqrt{K^2 - \Delta\omega^2}\cos\theta_{e\ init.}}{\Delta\omega - K\sin\theta_{e\ init.}}} \right] \tag{3.99}$$

$$= \frac{1}{\sqrt{K^2 - \Delta\omega^2}} \ln \left[\frac{-K + \Delta\omega\left(\frac{\Delta\omega - 1}{K}\right) - \frac{\sqrt{K^2 - \Delta\omega^2}\sqrt{K^2 - (\Delta\omega - 1)^2}}{K}}{\dfrac{-K + \Delta\omega \sin\theta_{e\ init.} - \sqrt{K^2 - \Delta\omega^2}\cos\theta_{e\ init.}}{\Delta\omega - K\sin\theta_{e\ init.}}} \right] \tag{3.100}$$

now

$$\sqrt{K^2 - \Delta\omega^2}\sqrt{K^2 - (\Delta\omega - 1)^2} = \left(K^2 - \Delta\omega^2\right)\sqrt{1 + \frac{2\Delta\omega - 1}{K^2 - \Delta\omega^2}} \tag{3.101}$$

$$\cong \left(K^2 - \Delta\omega^2\right) + \tfrac{1}{2}(2\Delta\omega - 1) \tag{3.102}$$

In all instances except at the extreme limits of the capture range

$$(2\Delta\omega - 1) \ll K^2 - \Delta\omega^2 \tag{3.103}$$

Thus Eq. (3.100) reduces to

$$t_{ZDF} \cong \frac{1}{\sqrt{K^2 - \Delta\omega^2}} \ln \left[\frac{-\frac{2}{K}\left(K^2 - \Delta\omega^2\right)\left(\Delta\omega - K\sin\theta_{e\ init.}\right)}{-K + \Delta\omega\sin\theta_{e\ init.} - \sqrt{K^2 - \Delta\omega^2}\cos\theta_{e\ init.}} \right] \tag{3.104}$$

As a typical example let $\theta_{e\ init.} = -90^{o}$, thus $\sin \theta_{e\ init.} = -1$ and $\cos \theta_{e\ init.} = 0$.

Equation (3.104) becomes

$$t_{ZDF} \cong \frac{1}{\sqrt{K^2 - \Delta\omega^2}} \ln \left[-\frac{2}{K} \frac{(K^2 - \Delta\omega^2)\ (\Delta\omega + K)}{-(K + \Delta\omega)} \right] \tag{3.105}$$

$$t_{ZDF} \cong \frac{1}{\sqrt{K^2 - \Delta\omega^2}} \ln 2 \frac{(K^2 - \Delta\omega^2)}{K} \tag{3.106}$$

When $K \gg \Delta\omega$

$$t_{ZDF} \cong \frac{\ln 2\ K}{K} \tag{3.107}$$

For $K = 10^5$

$$t_{ZDF} \cong 10^{-5} \ln 2 \times 10^5 \cong 10^{-4} \text{ sec} \tag{3.108}$$

As indicated in Eq. (3.104) the pull-in time for a simple loop depends upon the initial phase error $\theta_{e\ init.}$, the gain constant K and the initial frequency offset $\Delta\omega$. Since the noise bandwidth of the loop is directly proportional to the gain constant, then an increase in bandwidth will decrease the pull-in time, other factors remaining constant.

The open-loop gain of the system is defined as $\frac{\theta_o}{\theta_e}$ and may be obtained as follows:

From Eq. (3.88)

$$\frac{\theta_o}{\theta_i}(j\omega) = \frac{1}{1 + j\frac{\omega}{K}}$$

while from Eq. (3.63)

$$\theta_i = \theta_e + \theta_o$$

By substituting Eq. (3.63) into Eq. (3.88) and solving for $\frac{\theta_o}{\theta_e}(j\omega)$, the open-loop gain becomes:

$$\frac{\theta_o}{\theta_e}(j\omega) = \frac{1}{j\frac{\omega}{K}} \tag{3.109}$$

Figure 3.33 shows a plot of the open-loop gain of the system.

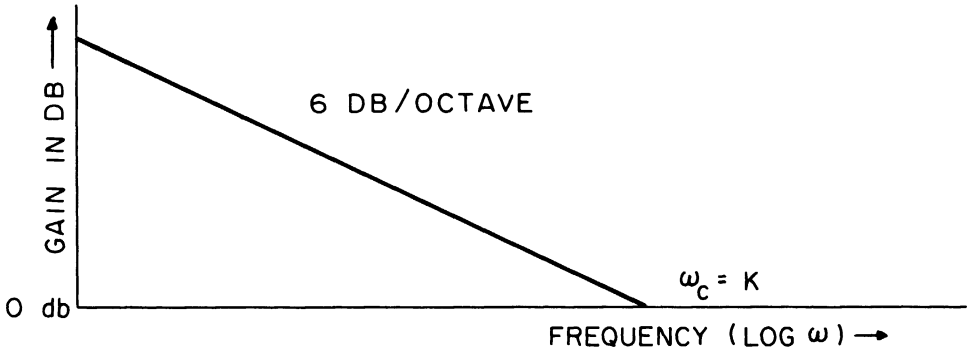


Fig. 3.33. Open-loop gain of system.

The loop gain decreases with frequency, intersecting the zero db (unity gain) line at a frequency $\omega_c = K$. This frequency was previously defined as the cutoff frequency (Eq. 3.89) of the closed-loop system. This simply means that the transfer characteristic of the system equals unity under locked conditions ($\omega_i = \omega_o$) for input variations with rates below ω_c and falls off for rates above ω_c. It should be noted that due to the single integration term[1] the loop gain decreases at a rate of 6 db per octave.

---

[1] Since the control of the oscillator adjusts its frequency while the error signal is detected in a phase detector (which detects the integral of frequency with respect to time), the servo loop contains one ideal integration.

Since the open-loop gain-frequency curve completely defines the characteristics of the system, it is easily seen that the lock range and acquisition range are equal to each other and proportional to the gain constant K. In addition the cutoff frequency ω_c is equal to the gain constant K.

The conclusions to be drawn regarding the first-order loop are:

(a) The loop will acquire lock within one cycle provided the frequency error is less than the cutoff frequency ω_c.

(b) The lock-in time is governed by the initial phase error $\theta_{e\ init.}$, the initial frequency offset $\Delta\omega$ and the gain constant K.

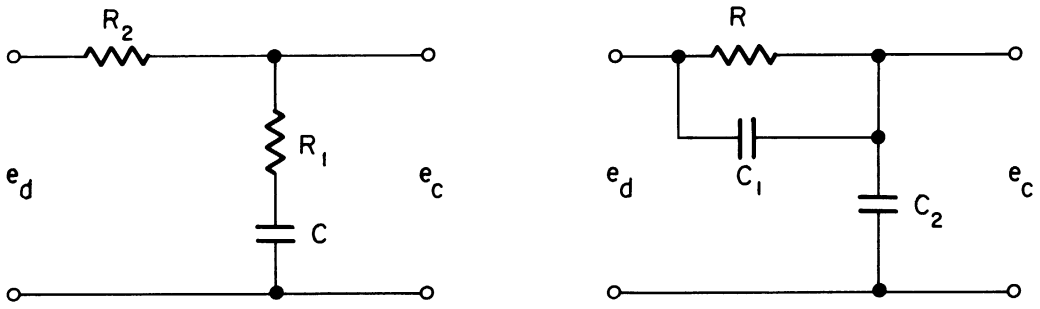
(c) The lock range, capture range, cutoff frequency, and noise bandwidth are all proportional to the gain constant K.

(d) The steady-state phase error of the system is proportional to the initial detuning and inversely proportional to the gain constant K.

It was shown in Eq. (3.80) that for small steady-state phase errors due to average frequency drift the gain constant has to be made as large as possible. If it is desired to reduce the effects of noise attendant with the input reference signal, the gain constant should be made as small as possible as shown in Eq. (3.91). A proper compromise of gain must then be found to insure adequate performance of the system for all requirements. In other words, the system capability should include independent control of bandwidth and gain constant at least over a limited range of operation.

Independent control of the bandwidth and gain constant can be achieved by the use of a more elaborate control network as shown in Fig.

3.34. Networks of this type are called proportional plus integral-control networks (Ref. 23).



$$\tau_1 = R_1C \qquad \tau_2 = (R_1 + R_2)C$$

$$\tau_1 = RC_1 \qquad \tau_2 = R(C_1 + C_2)$$

$$F(p) = \frac{e_c}{e_d}(p) = \frac{1 + \tau_1 p}{1 + \tau_2 p}$$

Fig. 3.34. Proportional plus integral control networks.

If one prescribes the transfer function of the control network to be

$$F(p) = \frac{1 + \tau_1 p}{1 + \tau_2 p} \tag{3.110}$$

then by substituting Eqs. (3.63), (3.82), and (3.110) into Eq. (3.78) one obtains

$$p^2\theta_o + \left(\frac{1}{\tau_2} + K\frac{\tau_1}{\tau_2}\right)p\theta_o + \frac{K}{\tau_2}\theta_o = K\frac{\tau_1}{\tau_2}p\theta_i + \frac{K}{\tau_2}\theta_i \tag{3.111}$$

where θ_o and θ_i are again relative phase angles. To simplify Eq. (3.111) it is convenient to introduce the following parameters

$$\omega_n^2 = \frac{K}{\tau_2} \tag{3.112}$$

and

$$2\xi\omega_n = \frac{1}{\tau_2} + K\frac{\tau_1}{\tau_2} \tag{3.113}$$

where ω_n is the resonant frequency of the system in the absence of any damping and ξ is the damping ratio. In terms of the new parameters the time constants of the control network are

$$\tau_1 = \frac{2\xi}{\omega_n} - \frac{1}{K} \tag{3.114}$$

and

$$\tau_2 = \frac{K}{\omega_n^2} \tag{3.115}$$

With these definitions Eq. (3.111) becomes

$$p^2\theta_o + 2\xi\omega_n p\theta_o + \omega_n^2\,\theta_o = (2\xi\omega_n - \frac{\omega_n^2}{K})\,p\theta_i + \omega_n^2\,\theta_i \tag{3.116}$$

Using LaPlace transforms the transient response of the loop to a sudden step of input phase $|\theta_i|$ becomes

$$\frac{\theta_o(p)}{\theta_i(p)} = \frac{(2\xi\omega_n - \frac{\omega_n^2}{K})\,p + \omega_n^2}{p\left(p^2 + 2\xi\omega_n p + \omega_n^2\right)} \tag{3.117}$$

which in the time domain becomes

$$\left|\frac{\theta_o}{\theta_i}\right|(t) = 1 - e^{-\xi\omega_n t}\left[\cos\sqrt{1-\xi^2}\;\omega_n t - \frac{\xi - \frac{\omega_n}{K}}{\sqrt{1-\xi^2}}\sin\sqrt{1-\xi^2}\;\omega_n t\right] \tag{3.118}$$

For $\xi < 1$ the system is underdamped, for $\xi = 1$ critically damped and for $\xi > 1$ overdamped. In order to avoid sluggishness of the system, a rule of thumb may be followed (Ref. 24) making $.4 < \xi < 1$. The

transient response (Eq. 3.118) can be plotted in dimensionless form if certain specifications are made for the ratio ω_n/K. Since the time constant τ_1 of the control network must be positive or at most equal to zero, the maximum value for ω_n/K can be found from Eq. (3.114), and is

$$\left.\frac{\omega_n}{K}\right|_{max} = 2\xi \tag{3.119}$$

In this case the control network is reduced to a single time constant network ($\tau_1 = 0$). On the other hand, if for a fixed value of ω_n the gain of the system is increased towards infinity, the minimum value for ω_n/K becomes

$$\left.\frac{\omega_n}{K}\right|_{min} = 0 \tag{3.120}$$

Plots of the transient response of the system for these two limits assuming a damping ratio of $\xi = 0.5$ are shown in Fig. 3.35.

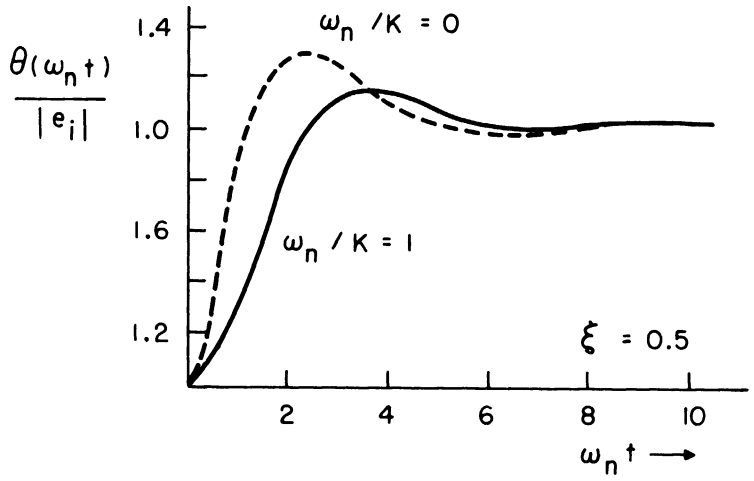


Fig. 3.35. Transient response of system.

The frequency response of the system may be found from Eq. (3.111) and is

$$\frac{\theta_o}{\theta_i}(j\omega) = \frac{1 + j2\xi \frac{\omega}{\omega_n}\left(1 - \frac{\omega_n}{2\xi K}\right)}{1 + j2\xi \frac{\omega}{\omega_n} - \left(\frac{\omega}{\omega_n}\right)^2} \tag{3.121}$$

Plots of the frequency response of the system for the two limit values and assuming a damping ratio of $\xi = 0.5$ are shown in Fig. 3.36. The curves show that the cut-off frequency of the system for $\xi = 0.5$ is approximately

$$\omega_c = \omega_n \text{ rad/sec} \tag{3.122}$$

The noise bandwidth of the system may be obtained by substituting Eq. (3.107) into Eq. (3.90). This substitution results in the following equation.

$$B = \omega_n \int_0^\infty \frac{1 + 4\xi^2\left(\frac{\omega}{\omega_n}\right)^2\left[1 - \frac{\omega_n}{2\xi K}\right]^2}{1 - (2 - 4\xi^2)\left(\frac{\omega}{\omega_n}\right)^2 + \left(\frac{\omega}{\omega_n}\right)^4} \cdot d\frac{\omega}{\omega_n} \tag{3.109}$$

The integration can be carried out by means of partial fractions and yields

$$B = \frac{4\xi^2 - 4\xi \frac{\omega_n}{K} + \left(\frac{\omega_n}{K}\right)^2 + 1}{2\xi} \frac{\pi}{2}\omega_n \tag{3.110}$$

For small values of ω_n/K it can be shown that Eq. (3.110) reaches a minimum when $\xi = 0.5$. Thus the noise bandwidths for the limit values of ω_n/K and $\xi = 0.5$ become

$$B\left|\frac{\omega_n}{K} \to 1\right. = \frac{\pi}{2}\omega_n = \frac{\pi}{2} K \frac{\text{rad}}{\text{sec}} \tag{3.111}$$

and

$$B\left|\frac{\omega_n}{K} \to 0\right. = \pi\omega_n \frac{\text{rad}}{\text{sec}} \tag{3.112}$$

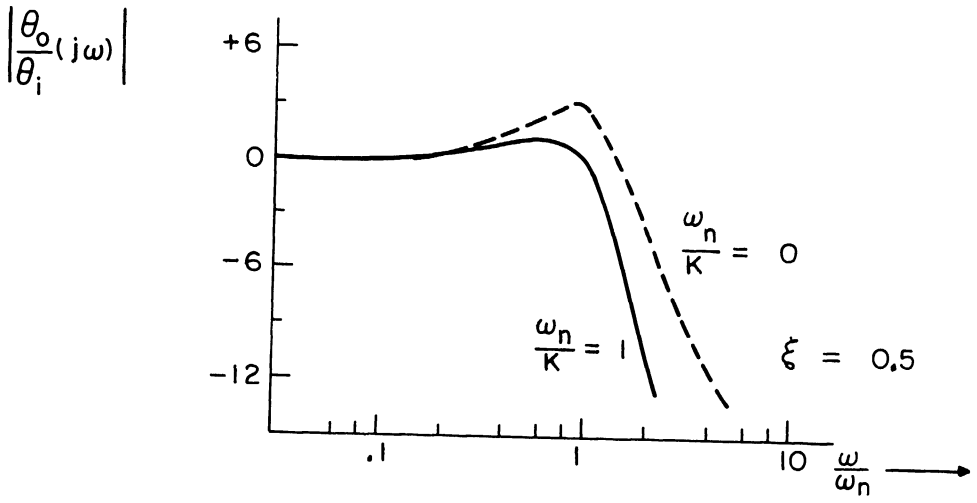


Fig. 3.36. Frequency response of system.

The response curves of Figs. 3.35 and 3.36, as well as the above derivations, show that the gain constant and the bandwidth of the system can be adjusted independently if a double time constant control network is employed.

In the study of the synchronized system it was permissible to assume small phase angles, thus linearizing the differential equation (Eq. 3.78). This simplification cannot be made for the evaluation of the pull-in performance of the system. The pull-in or capture range is defined as the range of difference frequencies, between the input signal and the free-running VCO signal, over which the system can reach synchronism.

Assuming that the difference frequency between the reference signal and the free-running VCO signal is constant as defined by Eq. (3.79), Eq. (3.78) may be written

$$p\theta_e + KF(p) \sin \theta_e = \Delta\omega \tag{3.127}$$

Mathematically then, the capture range is the maximum value of $\Delta\omega$ for which, irrespective of the initial condition of the system, the phase difference θ_e reaches a steady-state value.

As indicated in Eq. (3.81) with F(p) = 1, solution of the nonlinear equation is straightforward (integration may be carried out using separation of variables). In this special case which has been treated in detail by Labin (Ref. 25), the capture range is found to be equal to the lock range, i.e.,

$$|\Delta\omega|_{\text{capture range}} < K \tag{3.128}$$

In the case of the more elaborate control network where $F(p) = 1 + \tau_1 p/1 + \tau_2 p$, Eq. (3.127) becomes

$$p^2\theta_e + \frac{1}{\tau_2} + K \frac{\tau_1}{\tau_2} \cos \theta_e \, p\theta_e + \frac{K}{\tau_2} \sin \theta_e = \frac{\Delta\omega}{\tau_2} \tag{3.129}$$

This equation can be simplified by inserting the coefficients defined in Eqs. (3.112) and (3.113), and by dividing the resulting equation by ω_n^2. This leads to the dimensionless equation

$$\frac{1}{\omega_n^2} p^2\theta_e + \left[\frac{\omega_n}{K} + \left(2\xi - \frac{\omega_n}{K}\right) \cos \theta_e\right] \frac{1}{\omega_n} p\theta_e + \sin \theta_e = \frac{\Delta\omega}{K} \tag{3.130}$$

A further simplification is possible by defining a dimensionless frequency

$$y = \frac{1}{\omega_n} p\theta_e = \frac{1}{\omega_n} \frac{d\theta_e}{dt} \tag{3.131}$$

and one obtains a first-order differential equation from which the dimensionless time $\omega_n t$ has been eliminated. Substituting Eq. (3.131) into (3.130) one obtains

$$\frac{dy}{d\theta_e} = \frac{\frac{\Delta\omega}{K} - \sin\theta_e}{y} - \frac{\omega_n}{K} - \left(2\xi - \frac{\omega_n}{K}\right)\cos\theta_e \tag{3.132}$$

There is presently no analytical method to solve this equation. The equation completely defines the slope of the solution curve $y(\theta_e)$ at all points of $a\theta_e$ - y plane, except for the points of stable and unstable equilibrium, $y = 0$, $\Delta\omega/K = \sin\theta_e$. The limit of synchronization can thus be found graphically by starting the system with an infinitesimal velocity Δy at a point of unstable equilibrium, $y = 0$, $\theta_e = \pi - \sin^{-1}\Delta\omega/K$, and finding the value of $\Delta\omega/K$ for which the solution curve just reaches the next point of unstable equilibrium located at $y = 0$; $\theta_e = 3\pi - \sin^{-1}\Delta\omega/K$. The method is discussed by Stoker (Ref. 26) and has been used by Tellier and Preston (Ref. 27) to determine the capture range for a single time constant control network.

To establish the limit curve of synchronization for given values of ξ and ω_n/K, a number of solution curves must be plotted with $\Delta\omega/K$ as a parameter. These solution curves can best be obtained by means of an analog computer. The limit of capture range in terms of $\Delta\omega/K$ then can be interpolated to any desired degree of accuracy. The result obtained in this manner by Gruen (Ref. 28) is shown in the dimensionless graph of Fig. 3.37, where $\Delta\omega/K$ is plotted as a function of ω_n/K for a damping ratio $\xi = .5$. Since this curve represents the stability

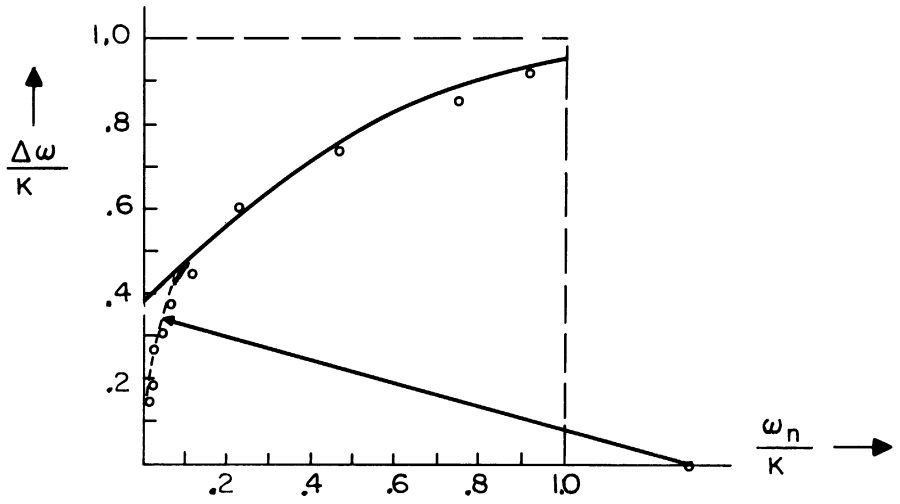


Fig. 3.37. Capture range of system.

limit of synchronization for the system, the time required to reach synchronization is infinite when starting from any point on the limit curve. The same applies to any point on the $\Delta\omega/K$ axis with exception of the point $\Delta\omega/K = 0$. Since this axis describes a system having either infinite gain or zero bandwidth, neither of which has any real practical significance, any discussion concerning this axis is meaningless. The practical capture range therefore lies inside the solid boundary. The individual points on the figure represent the measured pull-in curve of a particular system for which the damping ratio was maintained at $\xi = 0.5$. For small values of ω_n/K this pull-in curve can be approximated by its circle of curvature which, as indicated by the dotted line, is tangent to the $\Delta\omega/K$ axis and whose center lies on the ω_n/K axis. The capture range thus can be expressed analytically by the equation of the circle of curvature. If its radius is denoted by R, the circle is given

$$\left(\frac{\omega_n}{K} - R\right)^2 + \left(\frac{\Delta\omega}{K}\right)^2 = R^2 \qquad (3.133)$$

Thus, for $(\omega_n/K) \rightarrow 0$, the capture range is approximately

$$\left|\Delta\omega_{\text{capture}}\right|_{\left(\frac{\omega_n}{K}\right)\rightarrow 0} < \sqrt{2R\omega_n K - \omega_n^2} \approx \sqrt{2R\omega_n K} \qquad (3.134)$$

R can be interpreted as a constant of proportionality which depends on the particular design of the system, and which increases as the system gets closer to the theoretical limit of synchronization.

Equation (3.134) shows that the capture range for small values of ω_n/K is proportional to the square root of the product of the cut-off frequency ω_n and the gain constant K. Since the bandwidth of a second order APC system can be adjusted independently of the gain constant, the pull-in range of such a system can exceed the noise bandwidth by any desired amount.

The pull-in or capture time as shown by Richman (Ref. 29) depends upon the initial frequency offset, Δf cycles per sec, and the noise bandwidth, B cycles per sec, in the following manner:

$$t \cong 4\frac{\Delta f^2}{B^3} \qquad (3.135)$$

Equation (3.135) is valid except near the limit of the capture range where capture time approaches infinity.

3.3.2 Design Procedure. The theory discussed above is best illustrated by means of the following example. Suppose a phase lock loop is to be designed in which the total phase jitter must not exceed 5°. In addition the noise bandwidth is to be 1 kc/s and the voltage

tuned oscillator drift 2 kc/s.

The required gain constant is found from Eq. (3.80) yielding

$$K = \frac{\Delta\omega}{\sin\theta_e} = \frac{2\pi \cdot 2000}{.087} = 144{,}000 \text{ radians/sec} \qquad (3.136)$$

Since $|\Delta\omega_{\text{lock-in}}| \leq K$ the system will hold synchronism over a frequency range of 144,000 radians/sec. K is large compared to the required bandwidth; therefore the resonance frequency of the system is established from (3.112)

$$\omega_n = \frac{B}{\pi} = 2 \cdot 1000 = 2000 \text{ radians/sec} \qquad (3.137)$$

The time constants of the control network, assuming a damping ratio of 0.5, are determined from (3.114) and (3.115) respectively

$$\tau_1 = \frac{2\xi}{\omega_n} - \frac{1}{K} = \frac{1}{2000} - \frac{1}{144{,}000} \approx 5 \times 10^{-4} \text{ sec} \qquad (3.138)$$

$$\tau_2 = \frac{K}{\omega_n^2} = \frac{144{,}000}{2000^2} = \frac{.144}{4} = .036 \text{ sec} \qquad (3.139)$$

The capture range of the system is determined from (3.134)

$$\begin{aligned} |\Delta\omega_{\text{capture}}|_{\frac{\omega_n}{K} \to 0} &< \sqrt{2\xi\,\omega_n\,K} \\ &< \sqrt{2 \times 10^3 \cdot 144 \times 10^3} \\ &< 17 \times 10^3 \text{ rad/sec} \end{aligned} \qquad (3.140)$$

A proper choice of gain distribution and control network impedances still has to be made to fit a particular design. For example, if the peak amplitude of the reference voltage is .01 volt and the peak amplitude of the output voltage is 1 volt, then the sensitivity of the

oscillator control stage must be $K_2 = 14.4 \times 10^6$ radians/sec/volt. If the capacitor is assumed to be .01 μf for the control network of Fig. 3.34, the resistors R_1 and R_2 become respectively 50×10^3 ohms and 4×10^6 ohms to yield the desired time constants. For an initial frequency offset of $\Delta f = 1$ kc/sec, the capture time as given by (3.135) becomes

$$t \cong 4 \frac{\Delta f^2}{B^3} \cong \frac{4 \cdot 10^6}{10^9} \approx 4 \times 10^{-3} \text{ sec} \qquad (3.141)$$

In the design of the phase-lock oscillator a great deal of subjective experimentation is required. The procedure is to first design the best oscillator possible to produce the desired output frequency. To develop a suitable oscillator design, an analysis has been carried out to determine loading effects, frequency sensitivity, and other characteristics of voltage variable capacitors when used as the control element in the oscillator tank circuit. Based on this analysis the practical limits of both the tuning element and oscillator circuit parameters may be proposed.

Assume the simple circuit of Fig. 3.38 where L is the total circuit inductance, C_c is the circuit capacitance including stray but not the tuning element capacitance, C* is the capacitance of the tuning element, r_c represents the circuit losses while r* represents the loss associated with the tuning element. R is merely a decoupling resistor.

The frequency sensitivity of the circuit shown in Fig. 3.38 may be expressed as

$$S = \frac{\Delta f}{\Delta V} \frac{\text{kc}}{\text{volt}} \qquad (3.142)$$

$$= \frac{\Delta f}{\Delta C} \cdot \frac{\Delta C}{\Delta V} \qquad (3.143)$$

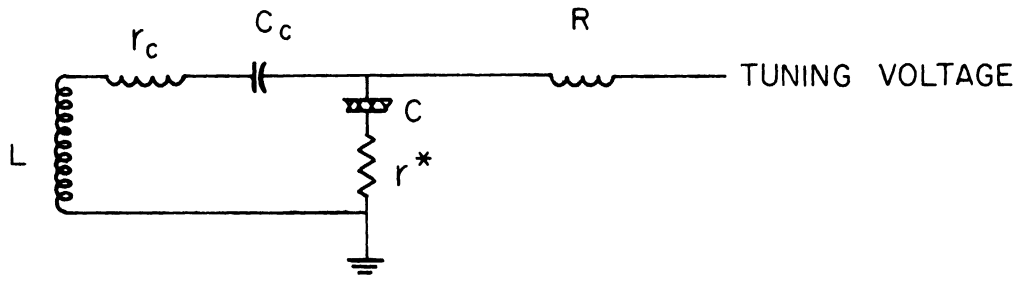


Fig. 3.38. Equivalent circuit of a typical oscillator tank circuit.

where

$$C = \frac{C^* C_c}{C^* + C_c} \tag{3.144}$$

Taking the differential of Eq. (3.144) with respect to voltage yields

$$\frac{\Delta c}{\Delta c^*} \cdot \frac{\Delta c^*}{\Delta V} = \frac{C_c}{\Delta c^*} \left[\frac{C^* + \Delta C^*}{C^* + \Delta^* + C_c} - \frac{C^*}{C^* + C_c} \right] \frac{\Delta C^*}{\Delta V} \tag{3.145}$$

For ΔC^* small this becomes

$$\frac{\Delta C}{\Delta V} = \frac{C_c^{\,2}}{(C_c + C^*)^2} \frac{\Delta C^*}{\Delta V} \tag{3.146}$$

A plot of the capacitance of the tuning element (in this case a ferroelectric capacitance) versus the control voltage is shown in Fig. 3.39. The solid line shows the actual dependence of capacitance on control voltage while the dotted curve indicates that a rectangular hyperbola provides a good approximation to the solid curve over a large portion of the tuning range.

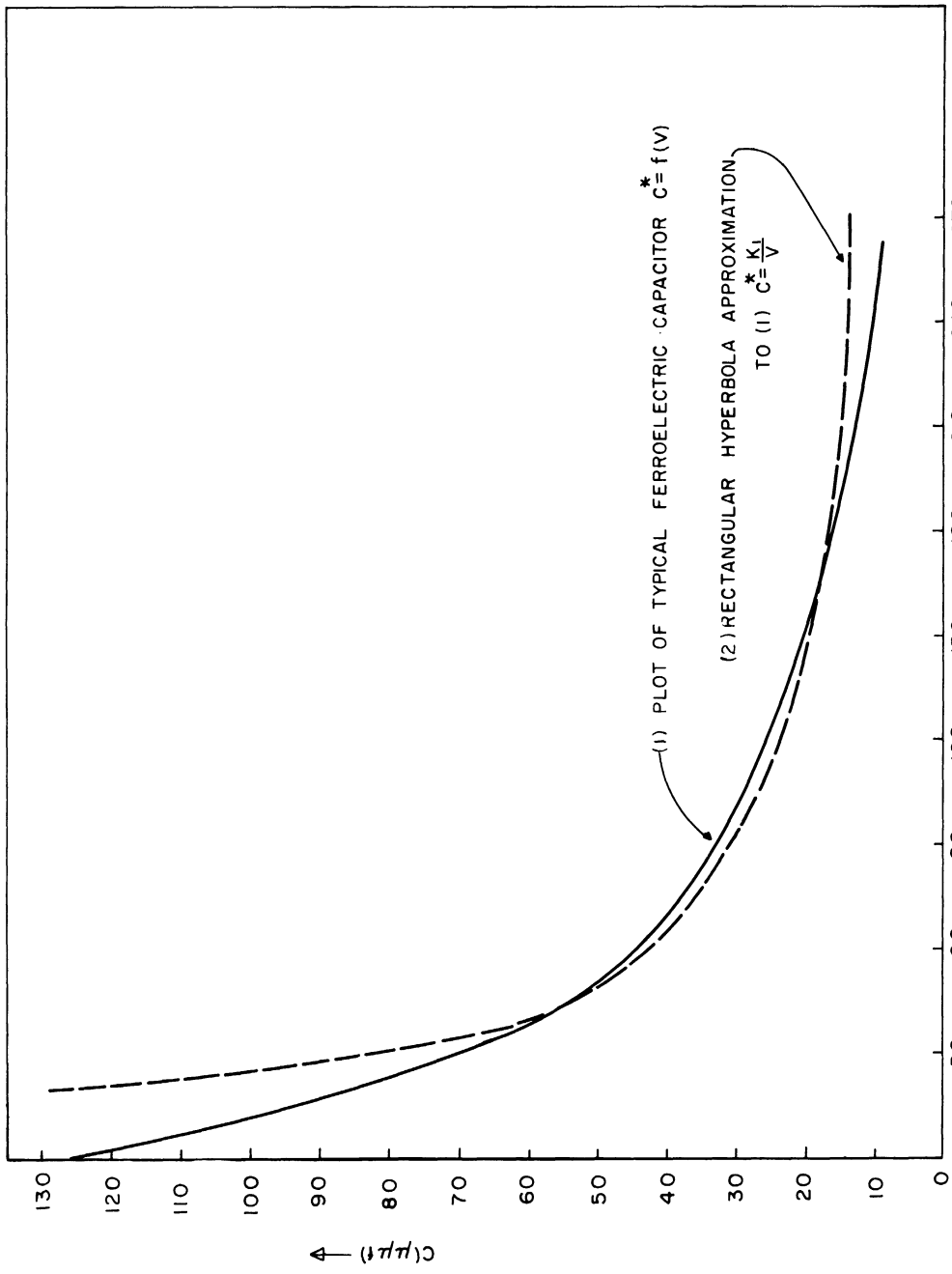


Fig. 3.39. Capacitance of ferroelectric capacitor vs. tuning voltage.

Thus

$$C^* \cong \frac{K_1}{V} \tag{3.147}$$

where:

K_1 is a constant for a given ferroelectric capacitance,

and

V is the control voltage.

If the tuning element is a back-biased diode then the dependence of C* on V may be given by

$$C^* = \frac{K_2}{\sqrt{V_o - V}} \tag{3.148}$$

where K_2 is a constant for a given diode, V_o is the contact potential, which varies slightly for different diodes, and V is the control voltage.

In the case of the ferroelectric capacitor

$$\frac{\Delta C^*}{\Delta V} \cong - \frac{K_1}{V^2} \tag{3.149}$$

and since from Eq. (3.147)

$$K_1 \cong C^*V \tag{3.150}$$

then

$$\frac{\Delta C^*}{\Delta V} \cong - \frac{C^*}{V} \tag{3.151}$$

Substituting Eq. (3.151) into (3.146) gives

$$\frac{\Delta C}{\Delta V} = \frac{-C_c^{\,2}}{(C_c + C^*)^2} \cdot \frac{C^*}{V} \tag{3.152}$$

The resonant frequency of the circuit of Fig. 3.38 is

$$f = \frac{1}{2\pi\sqrt{L}} \; C^{-\frac{1}{2}} \tag{3.153}$$

The ratio $\Delta f/\Delta c$ for small Δc is

$$\frac{\Delta f}{\Delta C} = -\tfrac{1}{2} C^{-1} \frac{1}{2\pi\sqrt{LC}} \tag{3.154}$$

Substituting Eq. (3.153) into (3.154) yields

$$\frac{\Delta f}{\Delta C} = -\frac{f}{2C} \tag{3.155}$$

To obtain an expression for the frequency sensitivity of the circuit, substitute Eqs. (3.155) and (3.152) into (3.143)

$$S = \frac{\Delta f}{\Delta C} \cdot \frac{\Delta C}{\Delta V} \tag{3.156}$$

$$= \frac{f}{2C} \cdot \frac{C_c^{\,2}}{(C_c + C^*)^2} \cdot \frac{C^*}{V} \tag{3.157}$$

$$= \frac{f}{2V} \cdot \frac{1}{1 + \frac{C^*}{C_c}} \tag{3.158}$$

From Eq. (3.158) it can be seen that the sensitivity varies directly as the oscillator frequency and inversely as the control voltage. For a fixed value of control voltage a small value of C* is desirable.

A second factor which has a decided effect on the loading of the tuned circuit is the loss factor (r*) associated with the tunable element.

The Q of the tunable element may be represented as

$$Q^* = \frac{1}{\omega C^* r^*} \tag{3.159}$$

The total Q of the circuit can be written as

$$Q_T = \frac{1}{\omega \left(\frac{C \; C_c}{C^* + C_c} \right) \left(r^* + r_c \right)} \tag{3.160}$$

The Q of the circuit, if the tunable element does not have any loss associated with it, may be represented as

$$Q_c = \frac{1}{\omega \; C \; r_c} \tag{3.161}$$

From Eq. (3.144)

$$C = \frac{C^* \; C_c}{C^* + C_c} \tag{3.162}$$

or

$$Q_c = \frac{1}{\omega \left(\frac{C^* \; C_c}{C^* + C_c} \right)} \tag{3.163}$$

The ratio of the circuit Q with loss in the tunable element (Q_T) to the Q without loss (Q_c) is

$$\frac{Q_T}{Q_c} = \frac{r_c}{r^* + r_c} \tag{3.164}$$

From Eq. (3.159)

$$r^* = \frac{1}{Q^*\omega C^*} \tag{3.165}$$

while from Eq. (3.163)

$$r_c = \frac{1}{\omega\, Q_c \left(\frac{C^*\, C_c}{C^* + C_c}\right)} \tag{3.166}$$

Substituting Eqs. (3.165) and (3.166) into (3.164) we have the following:

$$\frac{Q_T}{Q_c} = \frac{1}{1 + \frac{Q_c\, C_c}{Q^*\,(C^* + C_c)}} \tag{3.167}$$

For $C^* >> C_c$

$$\frac{Q_T}{Q_c} = \frac{1}{1 + \frac{Q_c\, C_c}{Q^*\, C^*}} \tag{3.168}$$

Since the product of Q*C* is reasonably constant over a given range the loading of the oscillator tank does not change radically with changes in control voltage.

To minimize loading use a large Q*C* product. For maximum sensitivity it was found that a small C* was desirable. It appears then that the conditions for minimum loading and maximum sensitivity counter one another and a compromise must be made.

It is possible to define a figure of merit which takes into consideration both the sensitivity and loading. This figure of merit may be defined as the product of the frequency sensitivity, S, and the Q_T of the oscillator tank circuit. Combining Eqs. (3.158) and (3.164) one has

$$SQ_T = \frac{Q_c f}{2V} \left[\frac{1}{\left(1 + \frac{r^*}{r_c}\right)\left(1 + \frac{C^*}{C_c}\right)} \right] \tag{3.169}$$

Equation (3.169) reduces to

$$SQ_T = \frac{fQ^*}{2V} \left[\frac{1}{1 + \frac{r_c}{r^*}} \right] \tag{3.170}$$

The interesting case, i.e., $r^* >> r_c$, occurs at the higher frequencies. Thus, Eq. (3.170) becomes

$$SQ_T = \frac{fQ^*}{2V} \tag{3.171}$$

To maximize Eq. (3.171) for a given frequency the ferroelectric capacitor should possess a high Q* at the control voltage. In addition the control voltage should be maintained at as low a level as possible.

To get at the case where $r_c >> r^*$ (low frequency case), reduce Eq. (3.169) to the form

$$SQ_T = \frac{Q_c f\, C_c\, r_c}{2V\, C^*} \left[\frac{1}{r_c + r^*} \right] \tag{3.172}$$

or for $r_c >> r^*$

$$SQ_T = \frac{1}{4\pi\, V\, C^*\, V_c} \tag{3.173}$$

It is seen then for the low frequency case where the circuit losses are fairly high, the tunable element loading effect becomes negligible, and the SQ_T product is determined mainly by the expression for the sensitivity S. Thus a small tunable element C* is desirable.

The conclusions regarding the performance of an APC system can be summed up as follows: Three parameters, which are (1) the gain constant k, (2) the damping ratio ξ, and (3) the resonance or cutoff frequency ω_n, completely describe the performance of the system. These parameters are specified by the requirements of the particular application and define the overall design of the system. It has been shown that among the systems with zero, single, and double time-constant control networks, only the latter fulfills the requirement for achieving good noise immunity, small steady-state phase error, and large capture range.

3.4 Analysis of Frequency Choices for the Frequency Synthesizer

In the development of the frequency synthesizer system the combining of two-signal frequencies to obtain a single frequency signal in the form of their sum or difference is one of the most basic operations. When the ratio between the two frequencies to be combined is low the method is quite straightforward, since the desired result can be arrived at by using a mixer and a filter. When the ratio between the two frequencies increases, the problem of separating the desired sideband from the undesired cross-modulation products becomes progressively difficult and eventually impractical.

Two signal sources ω_1 and ω_2 applied to a nonlinear element (mixer) produce a spectrum of modulation products of the general form $m\,\omega_2 \pm n\,\omega_1$, where m and n are integers and + or - indicates the upper or lower sideband spectra. An elemental frequency-combining circuit is shown in the block diagram of Fig. 3.40. Two signal frequencies, ω_1 and ω_2, are connected to a nonlinear element or mixer m_1, while the phase-

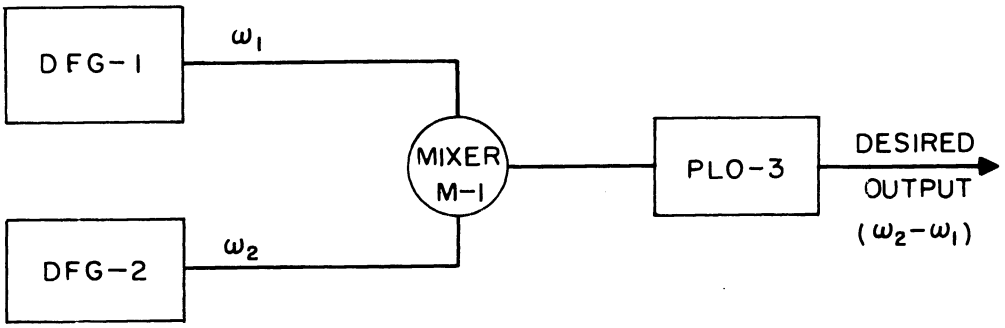


Fig. 3.40. Elementary frequency-combining network.

lock oscillator PLO-3 selects and locks to the desired sum or difference frequency and suppresses to a desirable degree the other modulation products, in particular the other sideband product and the carrier frequency (the higher of the two primary frequencies).

The frequency differences between a desired modulation product $(\omega_2 \pm \omega_1)$ and the nearest unwanted modulation products are equal to the lower of the two frequencies to be combined. Thus the higher the ratio between ω_2 and ω_1 frequencies, the more difficult are the frequency-discrimination requirements that must be met by the PLO-3 design.

An example of the technique which may be employed to determine the proper frequency choices in the present synthesizer design is presented below.

Assume the desired condition is to have the range of DFG-1 cover 10 kc in 1-kc steps, the range of DFG-2 cover 90 kc in 10-kc steps, and thus the mixer (M-1) output will cover 100 kc in 1 step. If the lock-in range of PLO-3 is limited to a range of 150 kc, then by a suitable choice of ω_1 and ω_2 the unwanted mixer components which fall in the

desired band ($\omega_2 \pm \omega_1$) are sufficiently low in amplitude that the oscillator will lock on only the desired component. The order of mixed harmonics such as $m\,\omega_2 + n\,\omega_1$ is defined as $|m| + |n|$, and the value of $|m| + |n|$ is selected to be some arbitrarily large number (e.g., 8 to 10). A systematic treatment was suggested by L. W. Orr and is as follows:

Let ω_1 range from a to a + 10 kc
and ω_2 range from b to b + 90 kc;
Let the guard band have a width G kc

The desired output $\omega_2 - \omega_1$ will range from b-a-10 to b-a+90. There are to be no low-order harmonics between b-a-10-G and b-a+90+G. Let the desired band fall between the Nth and (N+1)th harmonic of ω_1.

Based on the above assumptions the following equations can be set up.

$$N(a+10) = b-a-10-G \tag{3.174}$$

$$(N+1)a = b-a+90+G \tag{3.175}$$

which reduces to

$$a = 100 + 10N + 2G \tag{3.176}$$

$$b = (N+2)a-G-90 \tag{3.177}$$

Assume the guard band is 20 kc wide and let N = 1.

$$a = 100+10+40 = 150 \tag{3.178}$$

$$b = 450-20-90 = 340 \tag{3.179}$$

The desired output, $\omega_2 - \omega_1$, ranges from b-a-10 to b-a+90 or from 180 to 280 kc. The case for N = 1 is plotted in Fig. 3.41. Table I indicates the harmonics which fall in the desired band $\omega_2 - \omega_1$. It

should be noted that harmonics below order 8 do fall in the operating region.

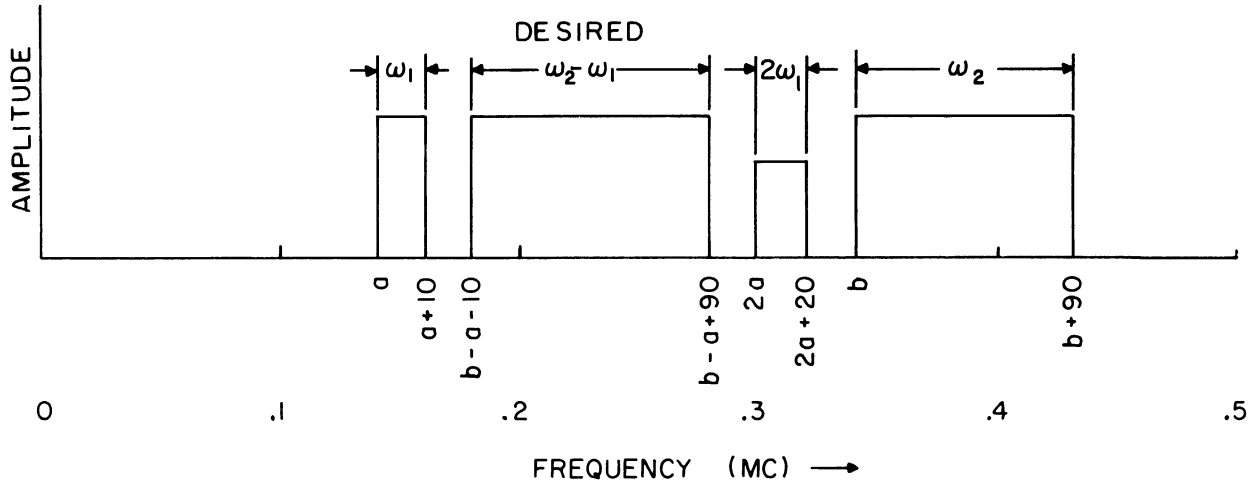


Fig. 3.41. Frequency spectrum for case N = 1, G = 20 kc.

Additional cases have been calculated and the tabulated results appear in Table II. The two numbers in the columns of harmonics are the values of m and n which result in a harmonic of $m\,\omega_2 - n\,\omega_1$ or $-m\,\omega_2 + n\,\omega_1$ falling in the useful output band.

It appears from these calculations that to obtain a harmonic-free desired band up through order 8, the desired band must be placed between the 5th and 6th harmonic of ω_1 (i.e., N = 5) regardless of the width of the guard band. The first undesired harmonics will then be $2\,\omega_2 - 8\,\omega_1$.

The design of PLO-3 is such that although many of these higher-order harmonics may fall in the operating range they will not fall within the set-on limits of the PLO-3 thus giving additional discrimination against unwanted harmonics in the system. The harmonics which do fall within the set-on limits will be ignored by PLO-3 since they will not contain sufficient energy to permit capture.

$N = 1$

$G = 20$ kc

$\omega_2 - \omega_1 = 180$ to 280 kc

Harmonic	Order (m+n)	Frequency Range
$2\omega_2 - 3\omega_1$	5	200-410 kc
$2\omega_2 - 4\omega_1$	6	40-260
$-2\omega_2 + 6\omega_1$	8	40-280
$-2\omega_2 + 7\omega_1$	9	190-440
$3\omega_2 - 5\omega_1$	8	220-540
$3\omega_2 - 6\omega_1$	9	60-390
$3\omega_2 - 7\omega_1$	10	0-240
$-3\omega_2 + 8\omega_1$	11	0-240
$-3\omega_2 + 9\omega_1$	12	70-420
$-3\omega_2 + 10\omega_1$	13	210-580

Table I. Order of harmonics falling in desired operating range 180-280 kc.

G = 20 kc				Harmonic (Amn cos $(m\omega_1 + n\omega_2)t$ of order (m + n)									
N	a kc	b kc	$(\omega_2 - \omega_1)$kc	5	6	7	8	9	10	11	12	13	14
1	150	340	180-280	2,3	2,4		2,6 3,5	2,7 3,6	3,7	3,8	3,9	3,10	
2	160	530	360-460		2,4	2,5			3,7	2,9 3,8	2,10 3,9	etc.	
3	170	740	560-660			2,5	2,6				3,9	3,10	2,12
4	180	970	780-880				2,6	2,7	-	-	-	etc.	
5	190	1220	1220-1120					2,7	2,8	-	-	etc.	
G = 50 kc													
1	210	490	270-370	2,3	2,4			2,6	2,7				
3	230	1010	770-870			2,5	2,6			-	-	-	etc.
5	250	1610	1350-1450					2,7	2,8	-	-	-	etc.

Table II. Order of harmonics (m + n) falling in desired operating range $(\omega_2 - \omega_1)$.

CHAPTER IV

SYNTHESIZER DESIGN CONSIDERATIONS

4.1 Design Philosophy

An experimental synthesizer which embodies the arrangement shown in Fig. 3.4 was designed, constructed, and tested for the purpose of demonstrating the practicability of the system. In the interest of facilitating construction and testing, some compromises were made. These were as follows:

(a) Transistor circuitry would be employed throughout but no attempt would be made to minimize the number of components and the package size. In a finalized version of a synthesizer some redesign, utilizing smaller cases and printed circuit techniques coupled with a reduction in the required number of components, would permit a much smaller package size.

(b) Commercial power supplies would be used for all control and operating voltages. Again, some redesign of the system incorporating less critical voltages and single battery operation could effect a considerable reduction in both the size of the overall system and the power requirements.

(c) The synthesizer would be designed to tune over a 1 Mc range in 10 kc steps (two significant figures). If additional significant figures are desired or a larger range is required for a specific application, additional modules may be added.

(d) Decade tuning would be used (10 steps per significant figure) although for certain applications where the synthesizer might be remotely programmed, a different number of steps per significant figure

might be more appropriate.

(e) The primary reference would be a standard crystal with a stability of approximately one part in 10^5. If more stability is desired, a primary reference of greater stability may be employed.

(f) Push-button tuning would be used, however the synthesizer would lend itself well to a number of different methods of programming.

As a result of these considerations, a two-digit synthesizer was constructed as shown in Fig. 4.1. The discrete-frequency reference

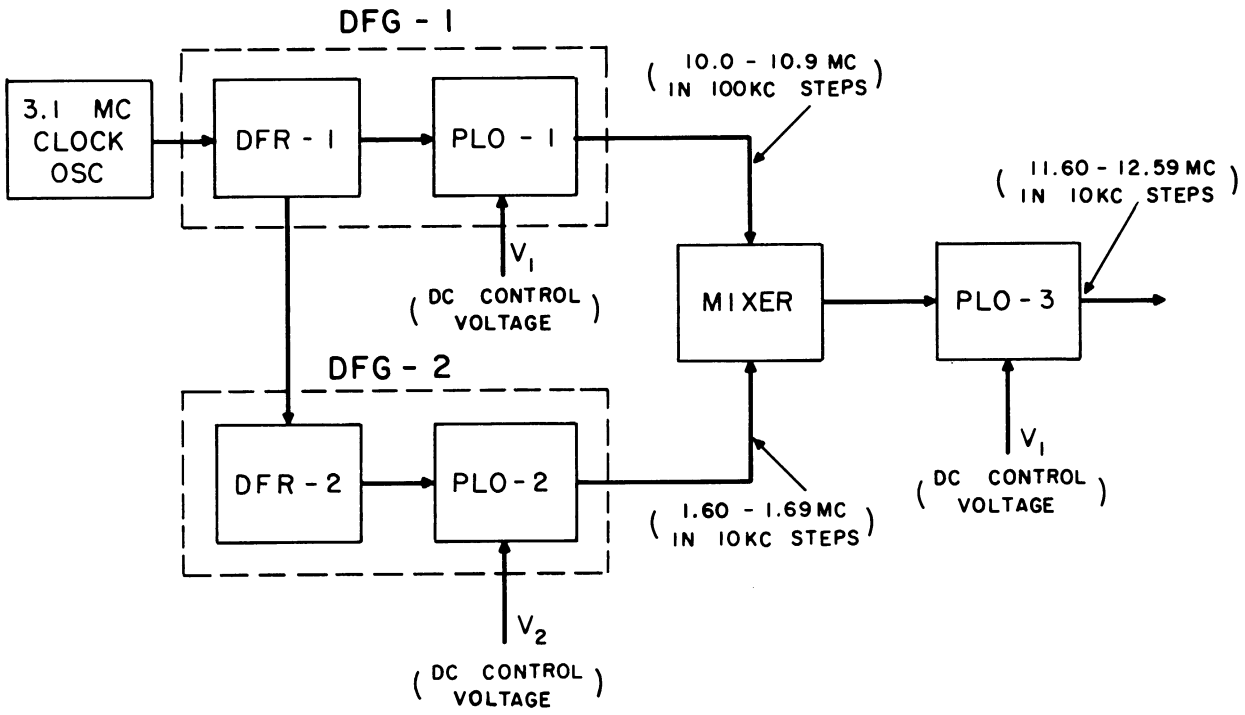


Fig. 4.1. Two-digit synthesizer.

is provided by a five-stage shift-register generator which is synchronized by a 3.1 Mc crystal clock. The output of DFG-1 is in the range 10.0-10.9 Mc in 100 kc steps. The output of DFG-2 is in the range 1.60-1.69 Mc in 10 kc steps. The outputs of DFG-1 and DFG-2 are combined in the mixer which in turn has an output in the range 11.60-12.59 Mc in 10 kc steps.

4.1.1 Discrete-Frequency Reference. The discrete-frequency reference is a digital waveform generator utilizing commercially available logic modules. As shown in Fig. 4.2, it consists of a master clock, a basic five-stage shift-register generator, a clock divider and coincidence circuits. Two sequences are generated; one with a period of 10 μsec

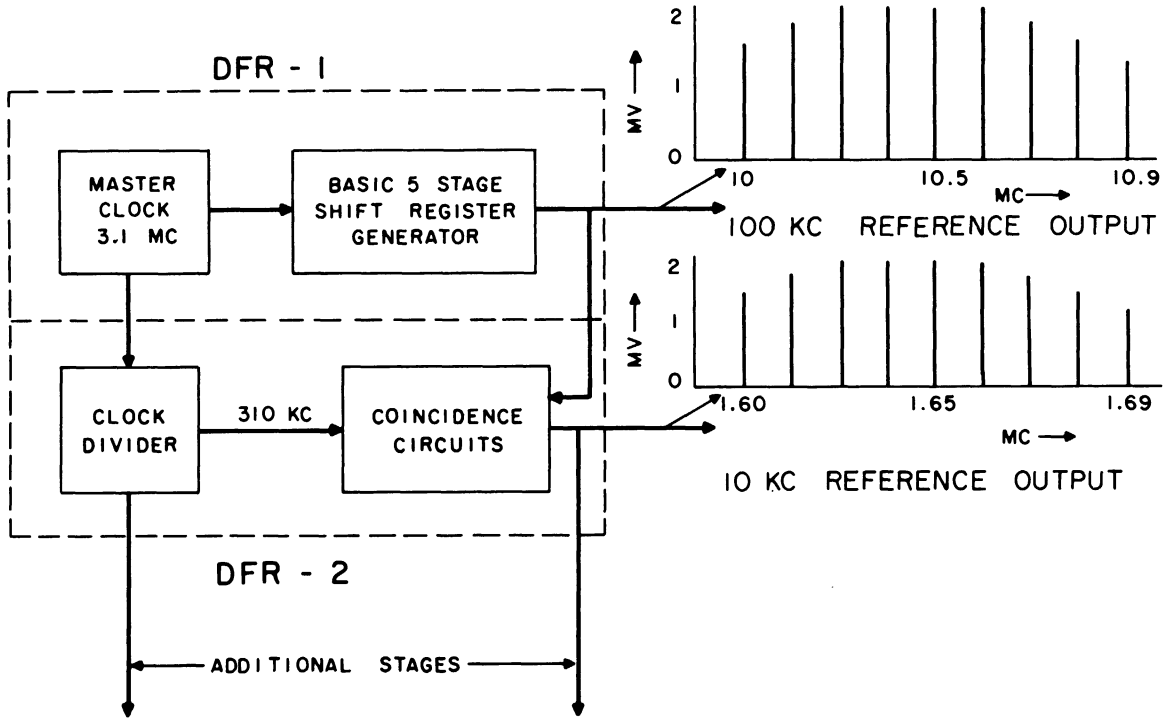


Fig. 4.2. Discrete-frequency reference.

and one with a period of 100 μsec. These sequences yield harmonics spaced at 100 kc in the tuning range of PLO-1 and harmonics spaced at 10 kc in the tuning range of PLO-2.

4.1.2 Phase-Lock Oscillator. The phase-lock oscillator in its elementary form consists of (1) a voltage-tuned oscillator, (2) a phase detector and (3) a control network, composed of a low-pass filter and dc

amplifier combination, as shown in the block diagram of Fig. 4.3. The

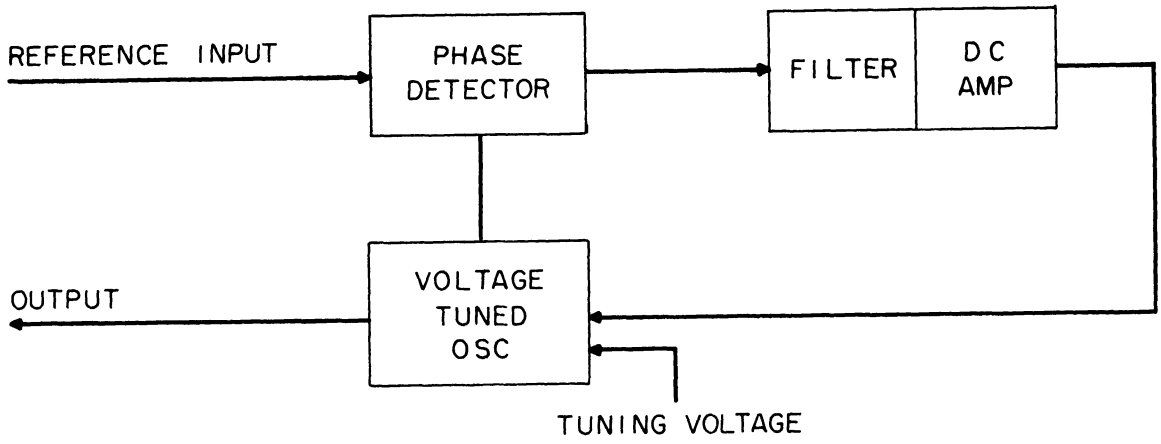


Fig. 4.3. Phase-lock Oscillator.

schematic diagram of PLO-1 is shown in Fig. 4.4 and will be described in some detail. Since the operation of PLO-2 and PLO-3 are very similar, they will receive only brief comment.

4.1.2.1 Voltage-Controlled Oscillator. The oscillator is a straightforward adaptation of the Hartley oscillator circuit to transistors. The oscillator tunes the range from 10 to 11 Mc upon application of 0 to +10 volts at the tune connection and has an open-loop set-on accuracy of better than 10 kc throughout its tuning range. This means that tuning to the vicinity of any one of 10 discrete frequencies in the range 10 to 11 Mc is easily accomplished. Oscillator output is taken from the unbypassed emitter, since this provides good isolation in addition to a low impedance source. The output amplifier is included only for experimental convenience. It feeds a 50-ohm coaxial cable at a level of a few hundred millivolts.

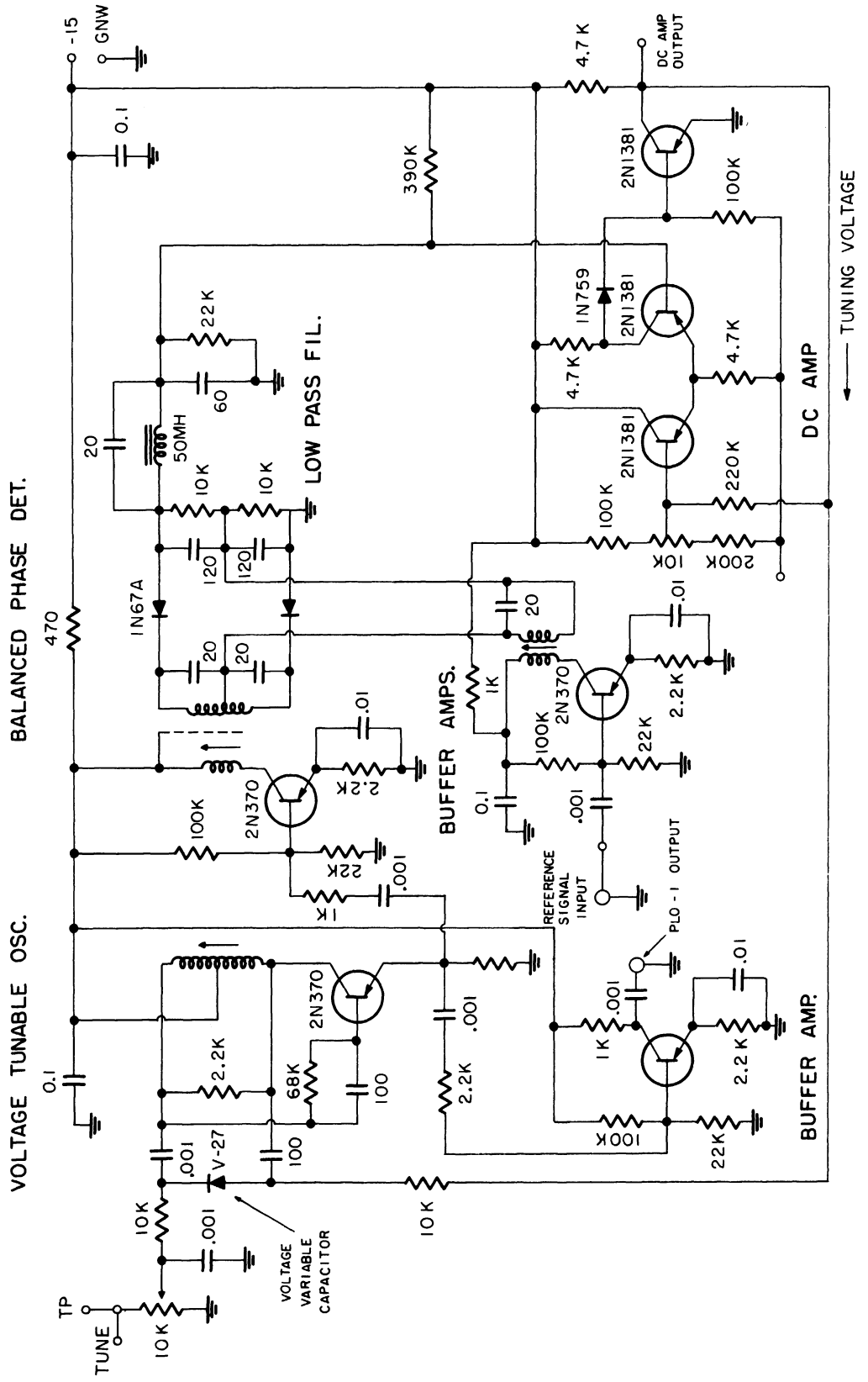


Fig. 4.4 Schematic diagram of PLO-1.

4.1.3 Phase Detector. The phase detector is a balanced type constructed for wideband operation and adequate isolation between inputs. The electrostatic shield between primary and secondary windings of the oscillator signal coil was found necessary to preserve good balance characteristics. The advantage of this type of detector is that variations in input signal levels do not seriously affect the detector output. For experimental purposes both the oscillator and reference inputs are provided with buffer amplifiers. The output of the phase detector is a function of the phase difference between the oscillator and reference inputs as shown in Fig. 4.5. The voltage across the balanced coil in

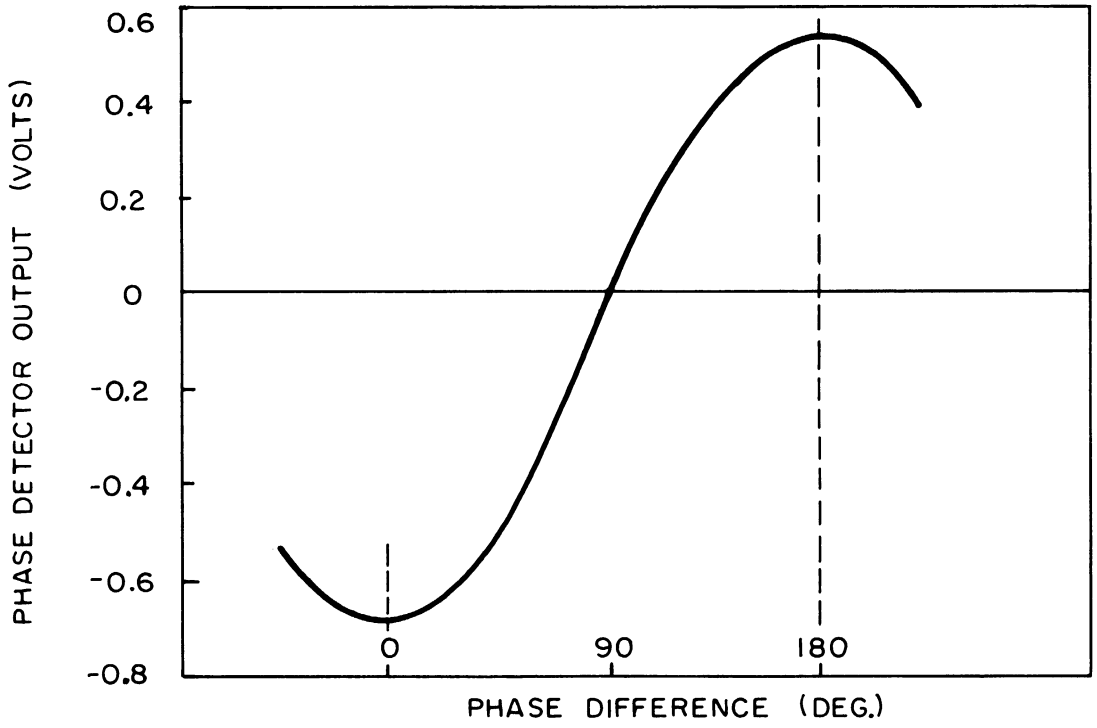


Fig. 4.5. Characteristic curve of the phase detector.

the phase detector due to the oscillator signal is plotted as a function of frequency in Fig. 4.6(a). At the same point the voltage resulting from the reference signal is presented in Fig. 4.6(b). In these measure-

ments the reference signal was maintained at 350 μv or about the level required for a 30 kc capture range. The coils are peaked on the high

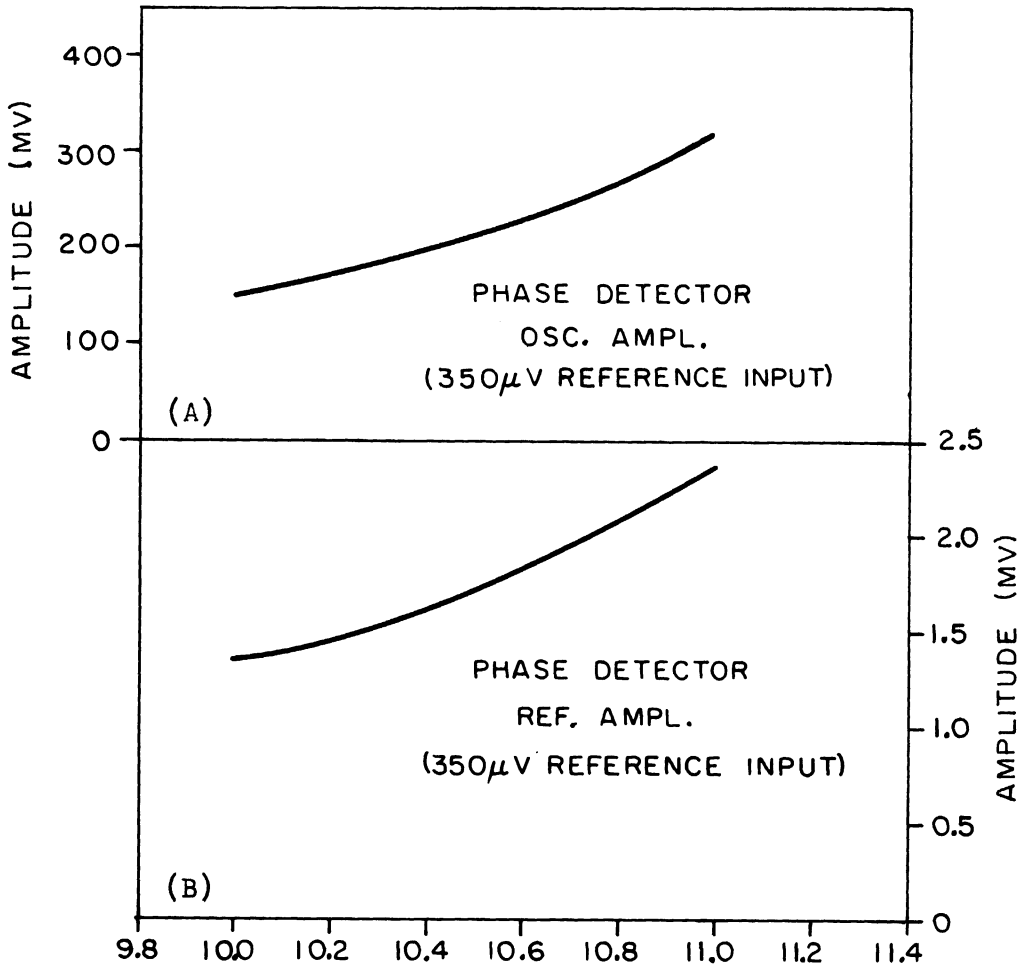


Fig. 4.6. Oscillator and reference amplitude at the phase detector coil as a function of frequency.

frequency side of the 10-11 Mc range for the reason that the oscillator sensitivity falls off at high tuning voltages. The frequency response of the phase detector is shown in Fig. 4.7.

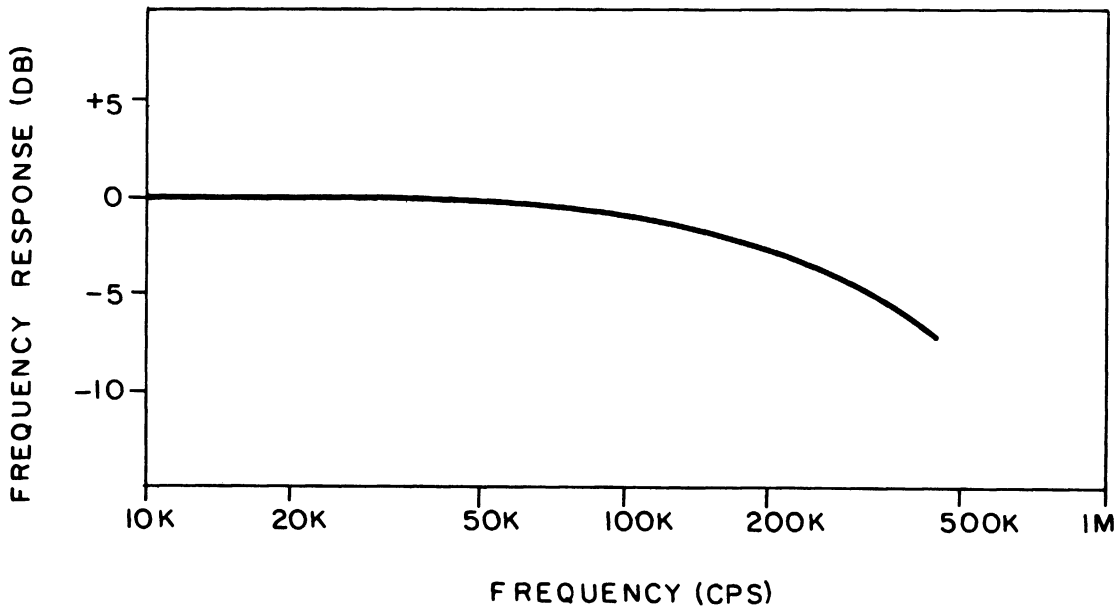


Fig. 4.7. Phase-detector frequency response.

4.1.4 Control Network. The use of the control network at the phase detector output enables one to make the overall gain constant (K) as large as desirable and at the same time restrict the loop bandwidth for good noise immunity (i.e., noise which arises from adjacent spectrum point modulation of the output). In the PLO, the control network takes the form of a dc amplifier followed by a low-pass filter. Goals for the control network include:

(1) Maintain a phase shift from dc to the maximum expected pull-in requirement (in this case 30 kc) as low as possible.

(2) Attenuate frequencies above the maximum expected pull-in range as rapidly as possible in order that unfiltered adjacent spectrum modulation be minimized.

(3) Provide adequate gain up to the maximum pull-in

requirement expected.

An unstable mode of operation exists in a feedback amplifier when the open-loop gain is equal to unity and the open-loop phase shift around the loop is 180 degrees. The design problem that exists in any closed-loop system, then, is to insure that open-loop gain is much less than one when the open-loop phase shift is 180 degrees. Due to the three control network requirements not being mutually compatible, some design compromises were necessary to insure an adequate stability margin.

The dc amplifier whose frequency response is shown in Fig. 4.8 provides a convenient means for experimenting with loop gain. It has a

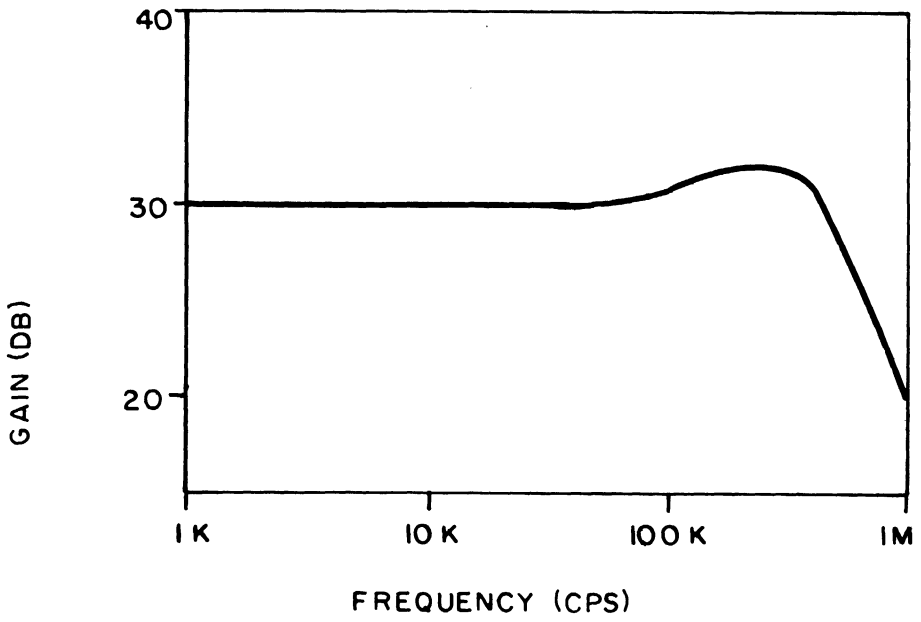


Fig. 4.8. Dc amplifier gain-frequency characteristic.

bandwidth in excess of 600 kc, a gain of up to 40 db, a high input impedance and low output impedance. The dc amplifier is more complex than would be necessary in a nonexperimental circuit and in fact its use may be unnecessary in a final model of the phase-lock loop.

The low-pass filter is an m-derived type which cuts off about 40 kc. To reduce adjacent spectrum point modulation of the output, an infinite attenuation point at 100 kc was included. In some cases it may be necessary to include infinite attenuation points at 200 kc, 300 kc and etc., as well as at 100 kc. The phase shift is such as to permit operation out to a capture range of 30 kc without loop oscillation. The amplitude characteristics of this filter are shown in Fig. 4.9.

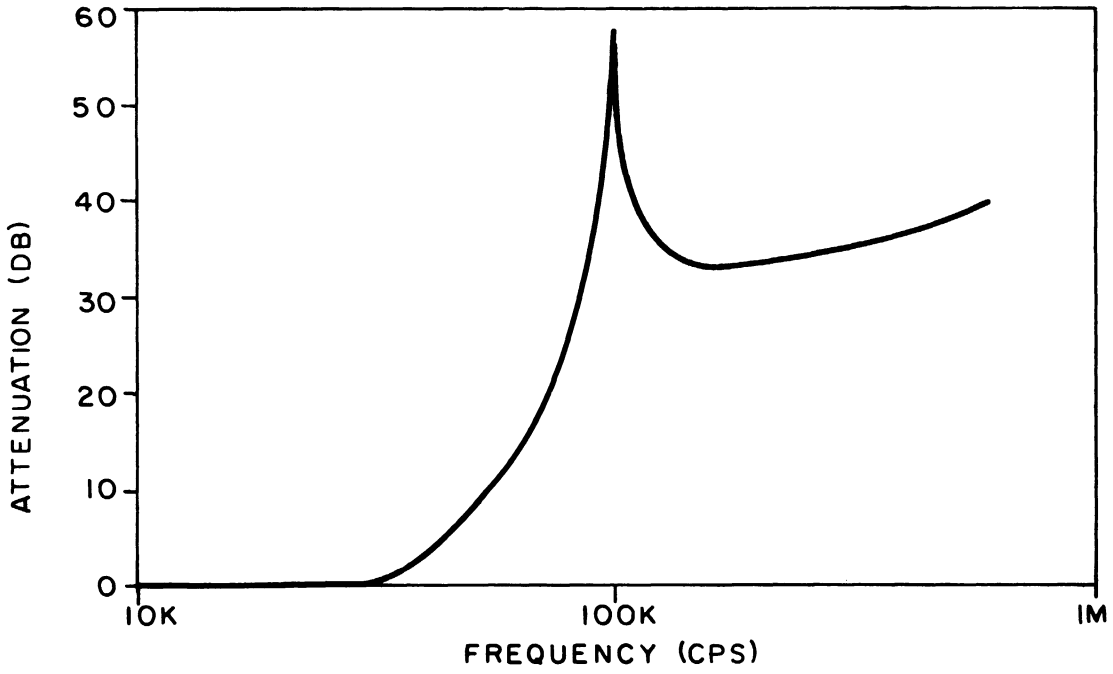


Fig. 4.9. Low-pass filter attenuation vs. frequency characteristics.

4.1.5 Measurements. Measurements were made on the basic units, i.e., the discrete-frequency reference and the phase-lock oscillators, to determine their individual operating characteristics. The basic units were then assembled and measurements were made to determine over-all system performance.

4.1.5.1 Discrete-Frequency Reference Measurements. The amplitude spectrum of DFR-1 is shown in Fig. 4.10. The spectrum of DFR-1 has the form of a sin x/x distribution with the 1st zero at the master clock frequency, in this case 3.1 Mc. As shown in the figure, DFR-1 has a relatively uniform distribution of spectral components, spaced 100 kc apart, in the desired operating range of 10 to 11 Mc. The output of DFR-2

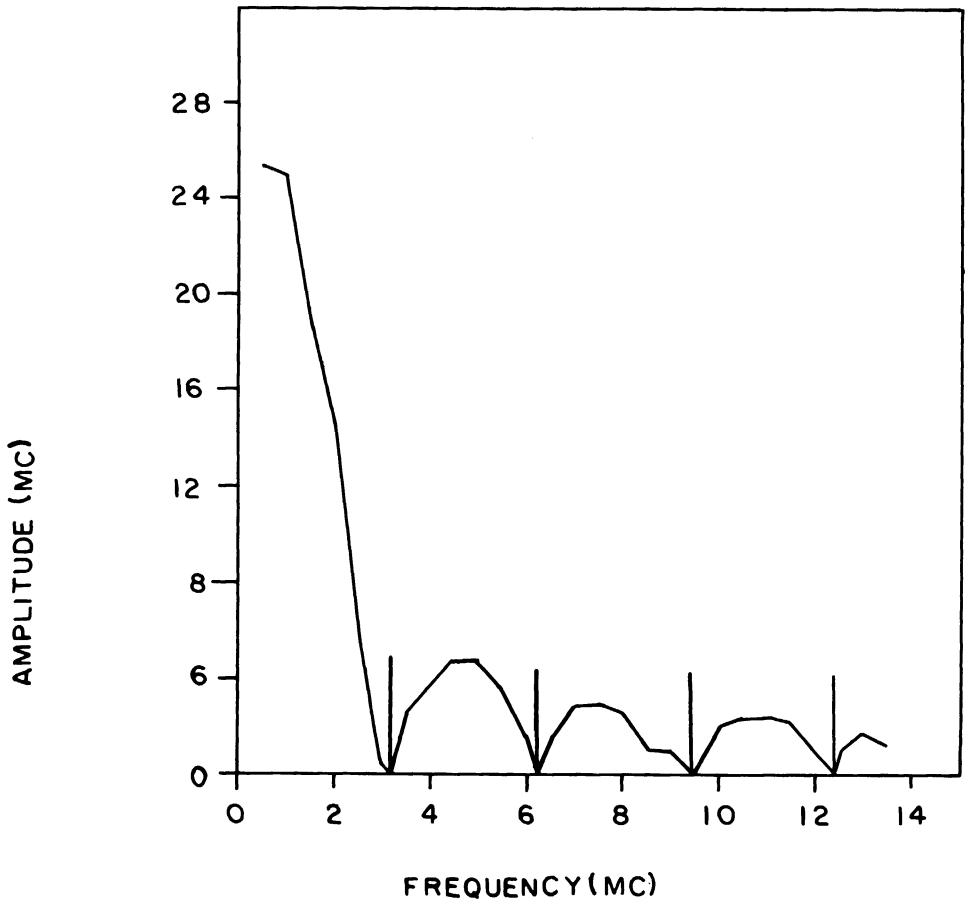


Fig. 4.10. Discrete-frequency reference amplitude vs. frequency.

also has a relatively uniform distribution of spectral components, spaced 10 kc apart, in the desired operating range of 1.60 to 1.69 Mc. Since the capture range of each PLO is a function of the energy in the reference signal and, since it is desirable to have the same capture range at each

reference point, it is important that a uniform distribution of spectral components be obtained throughout the desired operating range.

4.1.5.2 Phase-Lock Oscillator Measurements. The measurements of such dynamic characteristics as capture range, lock range, convergence time, stability, and spectral purity have been obtained and are described in the following text.

The capture and lock ranges, which were found to be approximately equal, vary as a function of the input reference amplitude as shown in the example of Fig. 4.11. It can be seen from the figure that for any

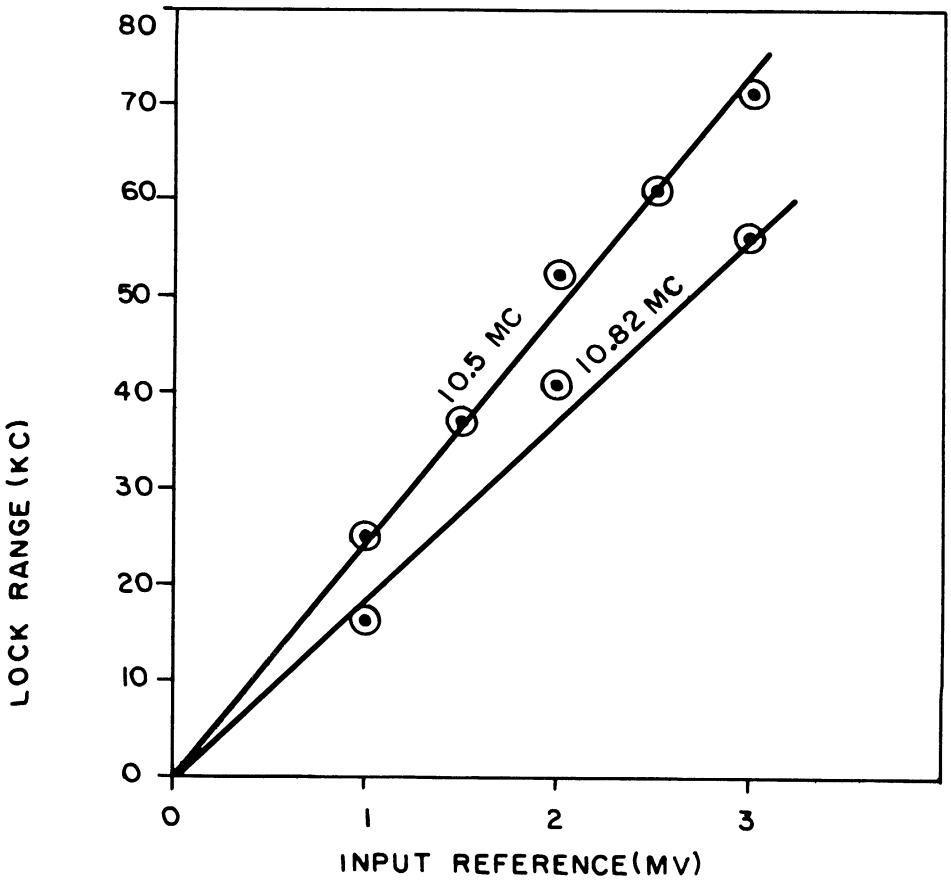


Fig. 4.11. Lock range vs. reference input of PLO-1.

given frequency the capture and lock ranges are linear functions of the

reference amplitude. For a given constant input reference amplitude of 2 mv, it was found that the capture and lock ranges of PLO-1 varied between the limits of 40 and 50 kc over the desired operating range. While in the case of PLO-2, the capture and lock range varied between the limits of 4 and 5 kc over the desired operating range. A plot of lock range versus frequency for PLO-1 is shown in Fig. 4.12. If in

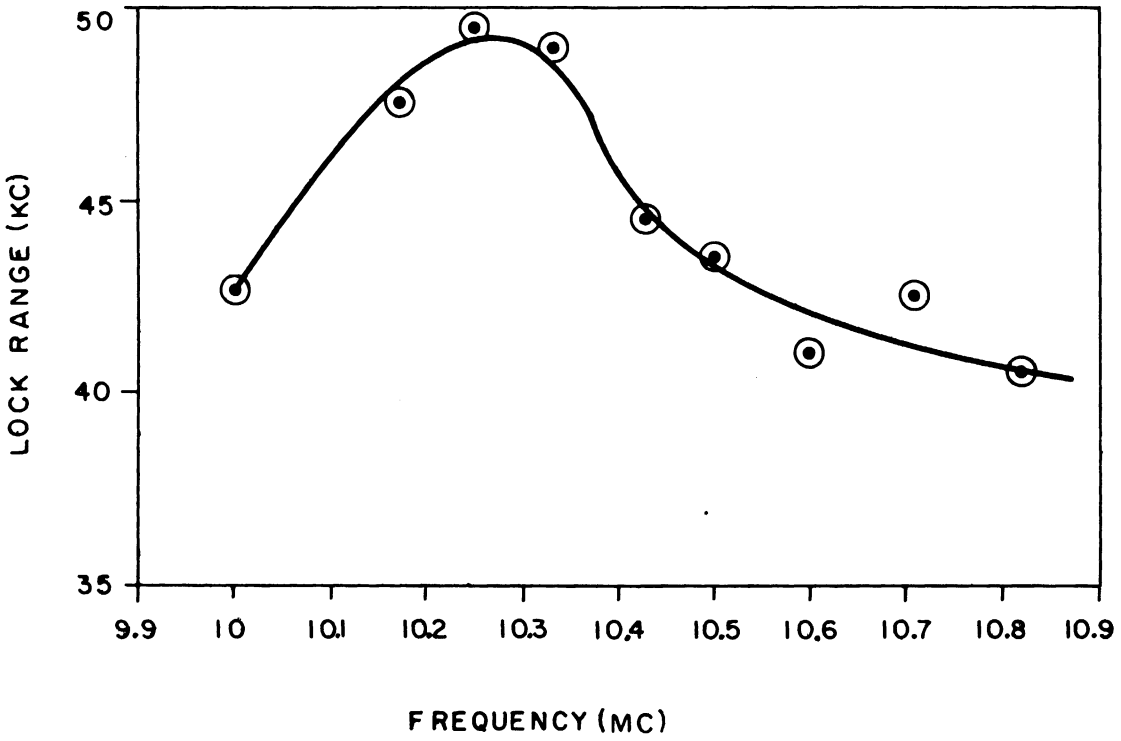


Fig. 4.12. Lock range vs. frequency of PLO-1 with a reference input of 2 mv.

average lock range of PLO-1 is assumed to be ~ 45 kc/sec over the operating range, then from the expression for gain constant $K \leq \Delta\omega/\sin\theta_e$, it is found that $K \leq \Delta\omega/1$ for $\theta_e = \pi/2 = 2\pi \cdot 45{,}000 = 284{,}000$.

PLO stability may be broken down into two cases, namely, locked and unlocked. Lock stability depends on the stability of the primary reference which in this case is approximately 1 part on 10^5.

Unlocked stability depends on many factors such as temperature variations, supply voltages variations, and component variations.

The seriousness of the temperature problem may be demonstrated by the curves of Fig. 4.13. Curve 1 shows the frequency drift versus temperature of PLO-1 with the dc amplifier in the circuit. Curve 2 shows

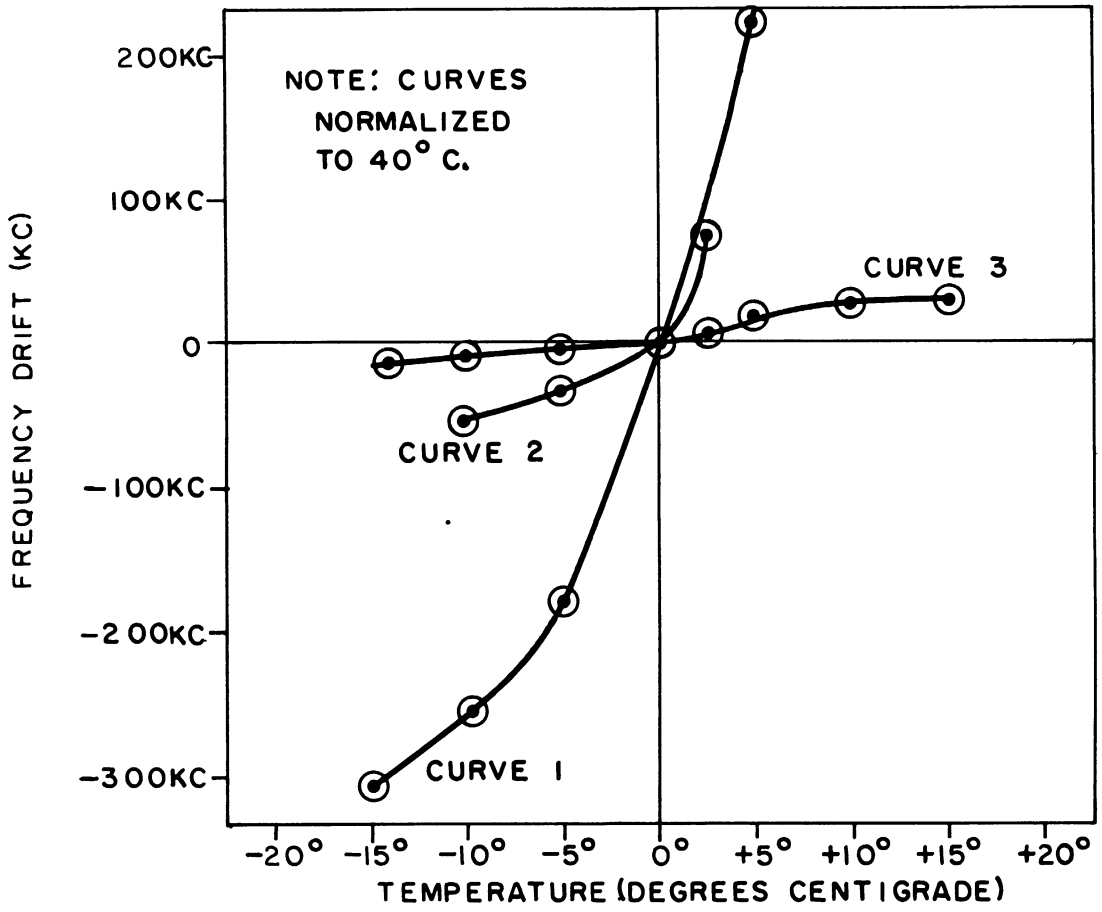


Fig. 4.13. Frequency stability vs. temperature for PLO-1.

the frequency drift versus temperature of PLO-1 with the dc amplifier out of the circuit. It can be determined from the curves that with the dc amplifier in the circuit, the drift at 30° C is approximately 10 kc/C°,

while without the dc amplifier the drift is approximately 3 kc/C°. From these results it is obvious that some type of temperature compensation or control must be incorporated, if the system is to perform properly. Curve 3 is a plot of a typical PLO without dc amplifier after some redesign work had been done on the loop. In the redesign of the loop the oscillator was changed from an adaptation of a Hartley to a Colpitts circuit with the tank circuit between base and ground rather than between base and emitter. In addition, a more rigid mechanical structure and better electrical shielding all contributed to bring the temperature drift down to approximately 1 kc/C°.

Figure 4.14 is a plot of the unlocked stability of PLO-1 as a function of power supply voltages. In the case of both the +10 volt supply and the -15 volt supply, a change of approximately 200 millivolts will cause a variation in frequency of about 40 kc. Although frequency instability due to supply voltage variations is a serious limitation in

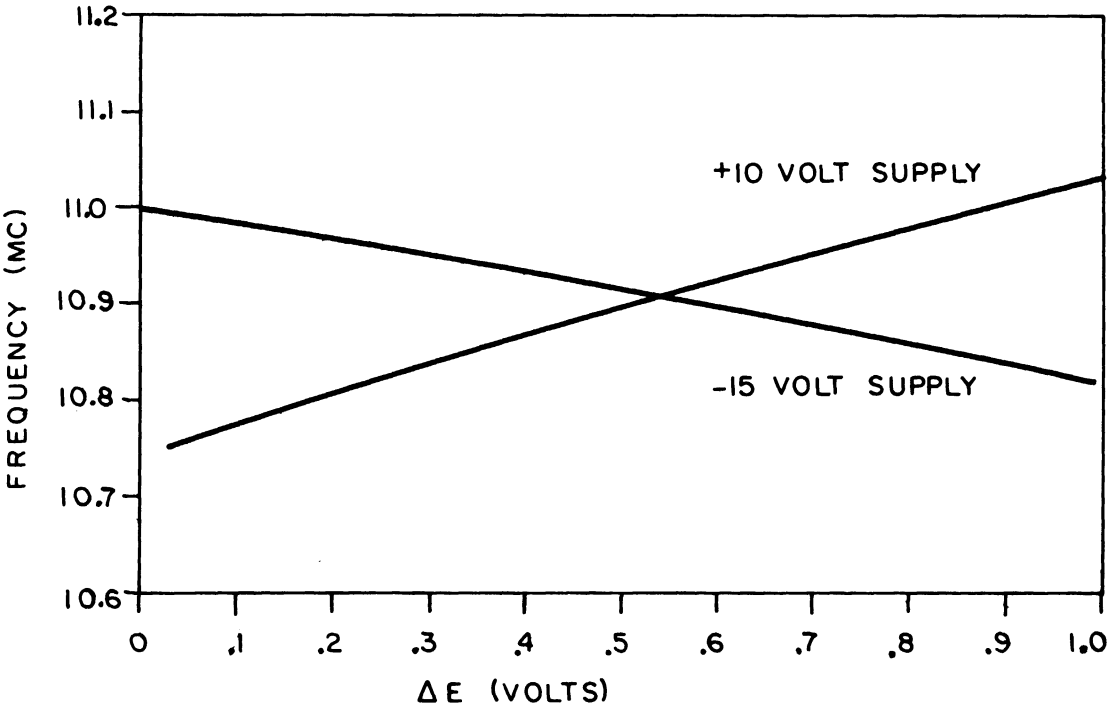


Fig. 4.14. Frequency in Mc vs. supply voltage changes (ΔE) in volts of PLO-1.

the laboratory model, the problem can be overcome to a large extent by including voltage regulation with Zener diodes as references in a final model.

Convergence time has been defined as the total time it takes to go from one locked frequency to another. The pull-in time of the loop itself was discussed in Chapter III, where a reasonable approximation to the time required to obtain a zero difference frequency was developed for the simple case (Eq. 3.104) and stated for the general case (Eq. 3.135).

In any practical application the tuning voltage must be applied to the tuning diode through some drive network. From the standpoint of tuning, the VCO appears as shown in the circuit arrangement of Fig. 4.15

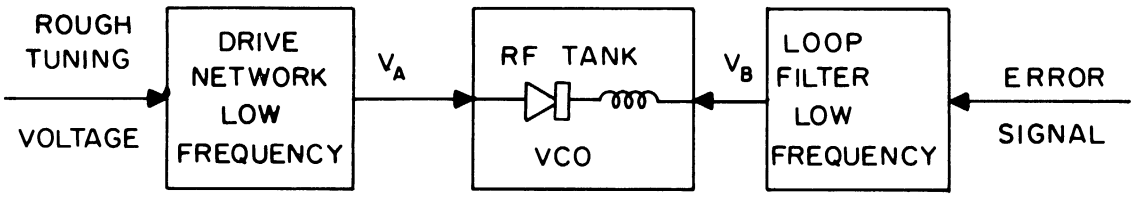


Fig. 4.15. Block diagram of VCO tuning circuit.

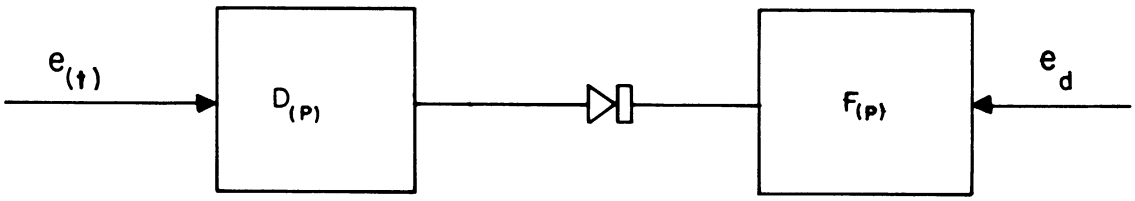


Fig. 4.16. Simplified diagram of VCO tuning circuit.

or more simply the low frequency circuit is given by Fig. 4.16, where e_d is the phase-detector output voltage, F(p) is the transfer function

of the loop filter, e_t is the tuning voltage and D(p) is the transfer function of the drive network. Assuming F(p) has been designed to meet certain basic loop requirements and is a known function, then the pull-in time for the loop itself may be estimated quite closely. For example, a 100 kc loop will take approximately 10 μsec, and a 1 kc loop 1 μsec to pull-in if the voltage applied to the diode places the frequency of the VCO well within the capture limits of the loop. Typical pull-in and escape times will be less than indicated by the example due to greater accuracy in set-on voltages and the use of large withdraw voltages.

At this point close attention to the design of a drive network D(p) must be given so that the over-all convergence time is not appreciably lengthened. For example, assume that D(p) is the transfer function of the circuit shown in Fig. 4.17.

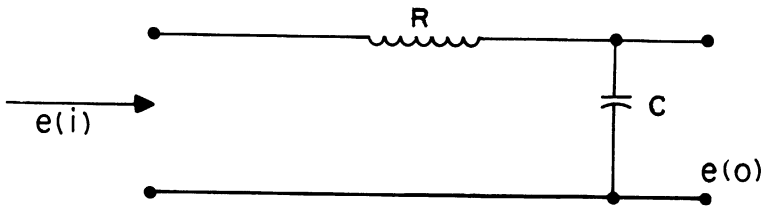


Fig. 4.17. Circuit of simplified drive network.

Hence $D(p) = \frac{1}{1 + PRC}$. The step response to this function is shown in Fig. 4.18.

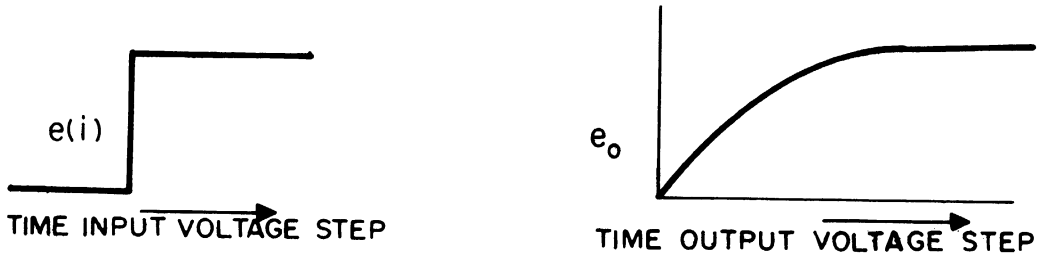


Fig. 4.18. Step response of simplified drive shown in Fig. 4.17.

For a 100 kc loop, unless the RC time constant is sufficiently small, a major part of the convergence time will be associated with the response of the drive circuit. In the case of a 100 kc loop one would pick RC $<<$ 10 μsec. Usually this condition leads to a resistor which is so small as to load the tuned circuit significantly. To obtain a more rapid response than is possible with this simple network, consider the drive circuit shown in Fig. 4.19.

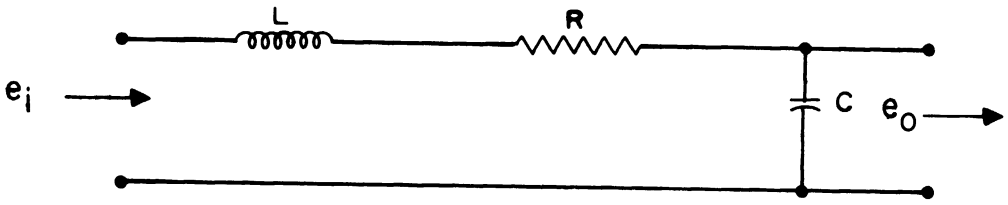


Fig. 4.19. Circuit diagram of a more complex drive network.

The transfer impedance for this network is given by:

$$\frac{e_o}{e_i} = Z(p) = \frac{1}{LC} \cdot \frac{1}{p^2 + \frac{R}{L}p + \frac{1}{LC}} \qquad 4.2$$

Let

$$\frac{1}{LC} = \omega_o^2 \qquad 4.3$$

and

$$\xi = \frac{R}{2}\sqrt{\frac{C}{L}} \qquad 4.4$$

Thus,

$$Z(p) = \frac{\omega_o^2}{p^2 + 2\xi\,\omega_o P + \omega_o^2} \qquad 4.5$$

The step response of this two-pole network is given in many texts, e.g., Truxel (Ref. 30) and will not be repeated here. Since it is desirable to minimize the convergence time, a fast-rise time in the drive network is required. A fast-rise time is provided by small ξ. However, a small ξ

also implies large overshoot. A compromise choice of $\xi = .7$ gives an overshoot of approximately 5 percent and provides rise time less than $3.2\pi/\omega_o$ sec. If one requires the minimum convergence time for a system which has a loop pull-in time of 10 μsec, the following condition should be imposed

$$\frac{3.2\pi}{\omega_o} < 10\ \mu\text{sec}$$

As an example, select

$$\frac{3.2\pi}{\omega_o} = 3\ \mu\text{sec}$$

thus

$$f_o = 1\ \text{Mc}$$

Hence,

$$\frac{1}{\omega_o^2} = LC = \frac{10^{-12}}{4\pi^2} .$$

Thus, for C = .0025 μf, L = 10 μh and $R = 1.4\sqrt{\frac{L}{C}} = 1.4\sqrt{\frac{10 \times 10^{-6}}{2.5 \times 10^{-9}}} \cong 90\ \Omega$.

If it is necessary to have an even more rapid response than can be provided with the two-pole network, more complex circuits with finite zeros and additional poles can be considered.

A sketch indicating the performance of the voltage V_b on the control side of the tuning diode for a prescribed voltage V_a on the drive side of the tuning diode is shown in Fig. 4.20. The input step voltage is arbitrarily shown as 1 percent below the required voltage for some desired frequency f_1 and 5 percent below the required voltage for a second desired frequency f_2. This simply means that for a given frequency the voltage across the diode must be a constant. Thus, there must be a dc correction voltage on the control side of the diode proportional to the error in set-on accuracy of the drive voltage. It should be noted that

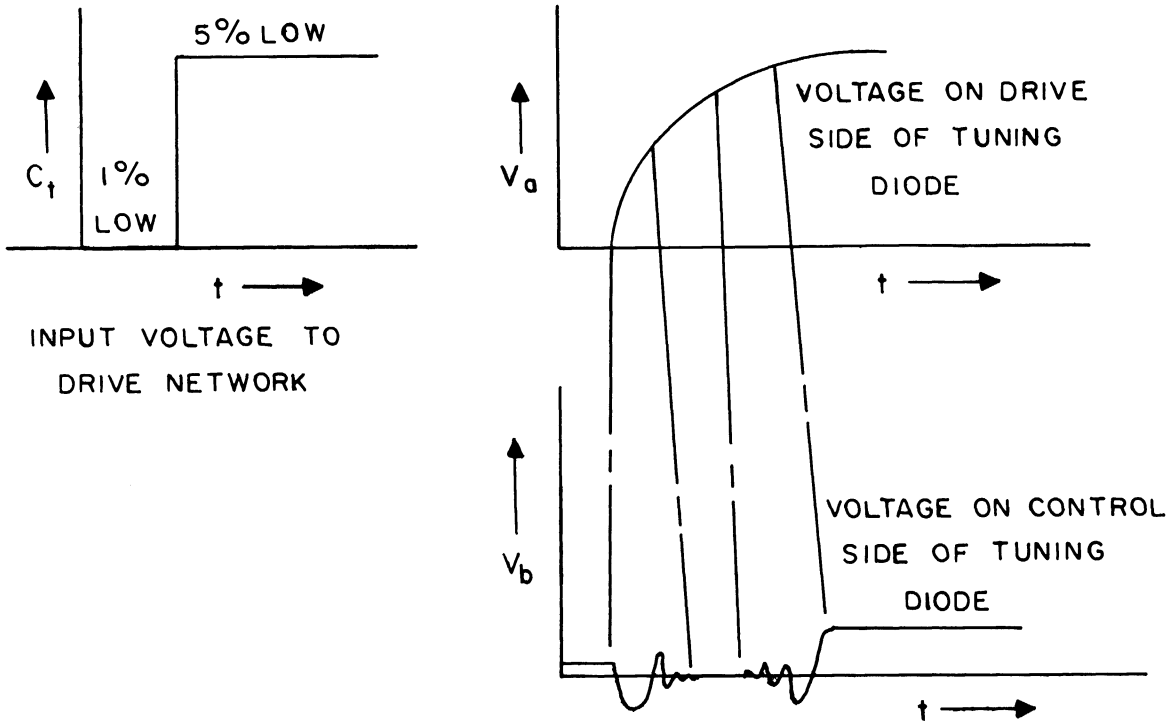


Fig. 4.20. Expected drive and control circuit operation under switching conditions.

as the voltage V_a on the drive side of the diode begins to rise the voltage V_b on the control side begins to drop in an effort to maintain the voltage across the diode constant. As V_a pulls further away, however, the lock range of the system is exceeded and a voltage proportional to the beat frequency between the VCO and the reference is obtained. As the frequency of the VCO is driven further from the reference frequency, the beat frequency increases and its amplitude decreases until the output of the phase detector drops to essentially zero. As the voltage V_a takes the VCO closer to the new reference frequency, a high frequency low amplitude beat is observed. This beat decreases in frequency and grows in amplitude until the capture range is reached and the system falls into synchronism. At this point a dc correction voltage is obtained which is

proportional to the error in set-on accuracy. If the above analysis is correct, then the output frequency of the VCO should change as a function of time as shown in Fig. 4.21.

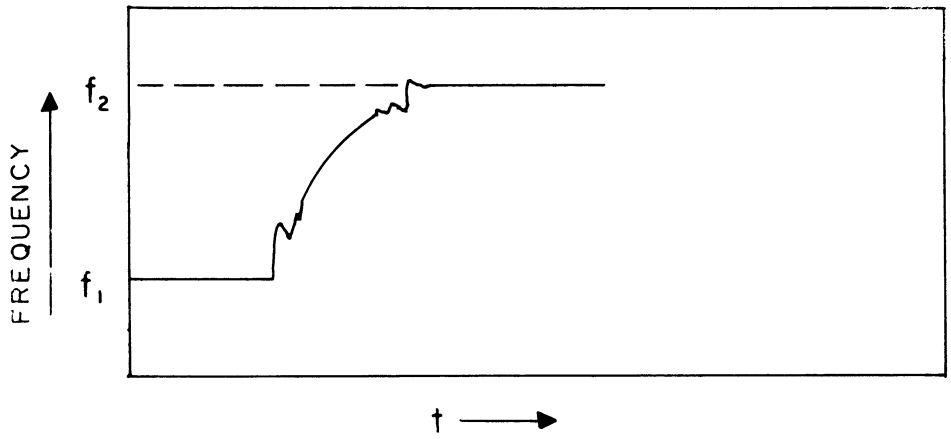
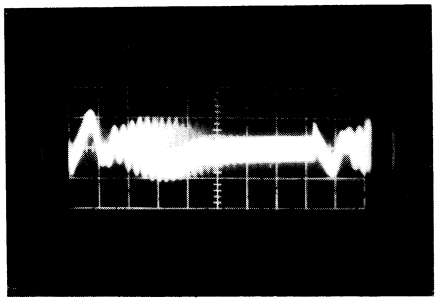


Fig. 4.21. Expected frequency variation under switching conditions.

An actual measurement of the convergence time of PLO-1 was made by applying a repetitive square wave in series with the rough-tuning voltage and of such a magnitude as to carry it from one locked state to another. The results of this measurement are shown in the photo of Fig. 4.22.



NOTE: Sweep rate is 20 μsec per cm.

Fig. 4.22. Actual drive and control circuit operation under switching conditions.

It should be noted that the photograph consists of many sweeps and, since

the capture time is a function of the starting phase or phase between the reference and VCO; when it, the VCO, is brought within the capture limits, the capture time will vary. The maximum convergence time for PLO-1 appears to be approximately 100 μsec. Since PLO-1 has a bandwidth of about 40 kc, the pull-in time of the loop itself should be about 25 μsec. The drive circuit of PLO-1 is a simple RC network with a time constant of approximately 50-60 μsec. Thus, the convergence time is made up of the sum of these two or approximately 100 μsec. No attempt was made to minimize the convergence time of PLO-1 by utilizing a fast-drive voltage. If rapid switching is a requirement, then a more complex network as discussed earlier in this section could be used as the drive network.

In summary it should be reemphasized that drive circuit considerations only become important when the bandwidths are large. For example, a bandwidth of 100 kc has a pull-in time of approximately 10 μsec, thus the time constant of the drive network should be kept as small as possible to maximize convergence times. In the case of a 1 kc bandwidth, the pull-in time is approximately 1 msec, thus reducing the time constant of the drive circuit to a value much below 100 μsec will not alter the total convergence time appreciably.

Spectral purity of the discrete-frequency generator is simply a measure of the purity of the output signal. In other words, how closely does the output signal approach a sine wave? The purity of the output signal will be examined under steady-state conditions since this is the mode of operation.

The first factor is intermodulation of adjacent harmonics in the detector of the phase-lock loop. This intermodulation produces

spurious sidebands at multiples of the reference generator repetition rate. These amplitudes may be obtained from a spectrum analyzer, calibrated receiver, or indirectly through an observation of the waveform at the tuning diode. The amplitudes of these spurious sidebands were measured with respect to the desired output signal using a calibrated receiver and are presented in Fig. 4.23.

A second factor is loop noise itself. Primarily due to the dc amplifier and discrete-frequency reference, the noise is confined to frequencies below approximately 1 kc/sec. Since spectrum analyzers are presently unavailable in this region, a simple narrowband discriminator was constructed having a bandwidth of approximately 1 kc at 10 Mc. The series of photographs shown in Fig. 4.24 indicate the relative noise in the system. Photograph A shows the output of the narrowband test discriminator without an input signal, while Photograph B shows the output of the test discriminator with a sine wave input from the HP 606 Signal Generator. Note the trace of 60 cycle line frequency leaking through. Photograph C is the output of the discriminator with PLO-1 in the system and the HP 606 Signal Generator used as a sine wave reference. Photograph D is the same setup as Photograph C with the exception that the discrete frequency reference has been substituted for the HP 606. The difference between Photographs B and C is a relative indication of the noise contributed by the loop itself. It is felt that the major part of this noise is contributed by the dc amplifier and transistor power supplies. Since Photograph D is not greatly different from Photograph C, it is assumed that the discrete-frequency reference contributes little additional noise to the over-all system.

A third factor causing deterioration of the DFG-1 output results

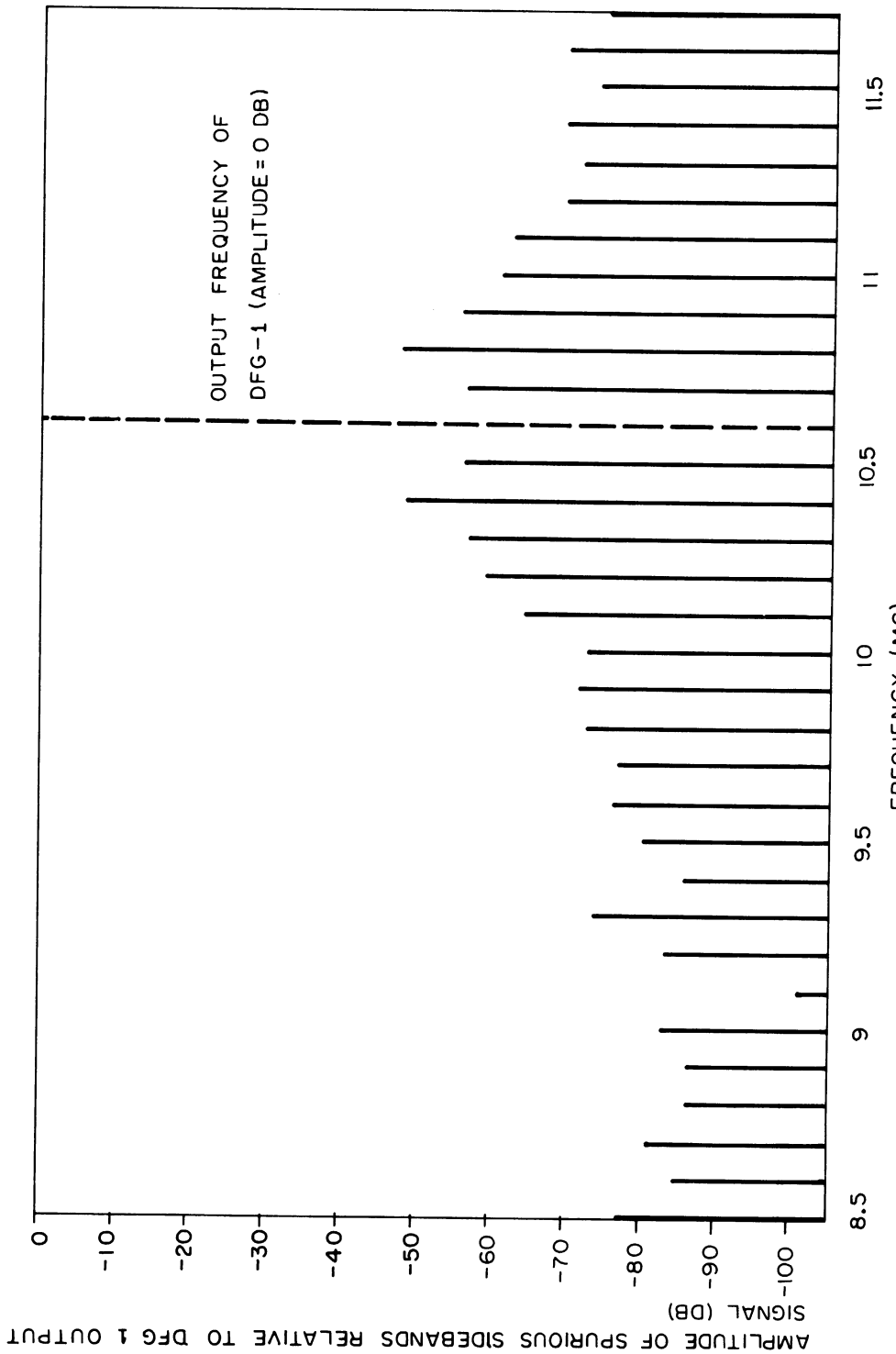
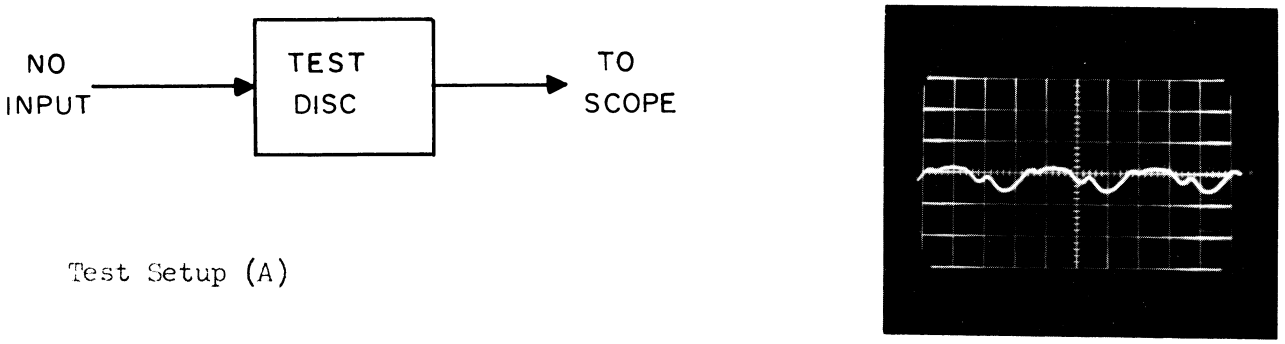
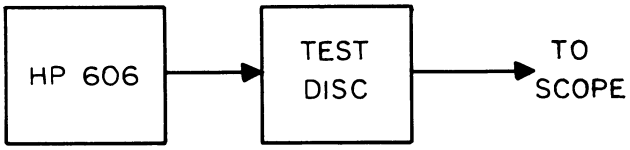


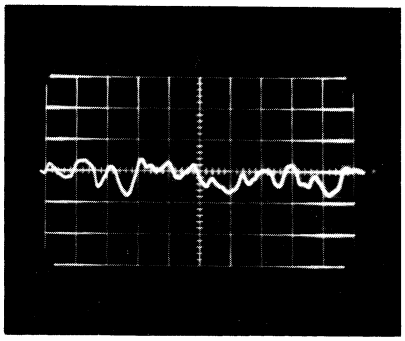
Fig. 4.23. Amplitude of spurious sidebands relative to DFG-1 output signal versus frequency.

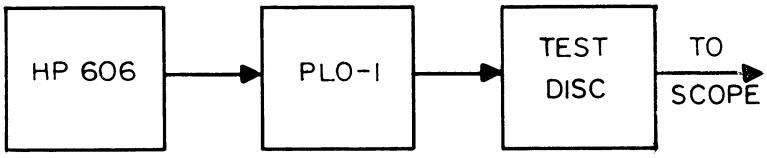


Test Setup (A)

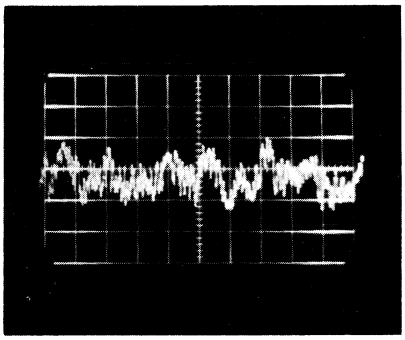


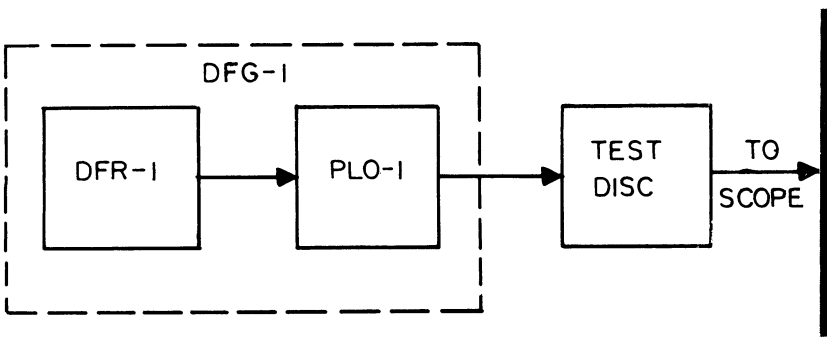
Test Setup (B)





Test Setup (C)





Test Setup (D)

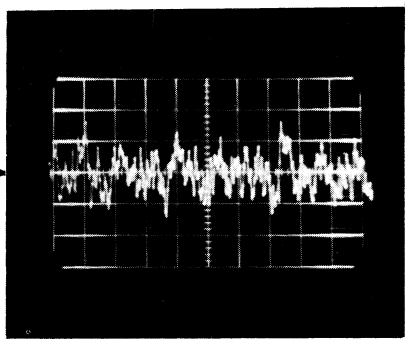


Fig. 4.24. A relative measure of the noise output of the system.

from clipping and distortion of the DFG signal itself. This distortion generates harmonics of the DFG frequency which, however, are easily removed through more careful design of the oscillator and buffer stages in the DFG unit. In addition, much of the distortion is removed when the synthesizer is connected to other equipment such as transmitters or receivers which have additional tuned stages. A plot of the actual 10 Mc output signal of DFG-1 is shown in Fig. 4.25.

Measurements made on the operating characteristics of PLO-2 and PLO-3 shown in Fig. 4.1 (page 126) indicate that their performance meets design requirements. In addition, the output of DFR-2 is somewhat cleaner and has a more uniform amplitude distribution than DFR-1.

Measurements made on the over-all system indicate that the two-digit synthesizer does perform as predicted. In a practical design, however, several considerations deserve attention. The unit should be mechanically rugged, and electrically well-shielded. The system should incorporate less critical operating voltages and single battery operation

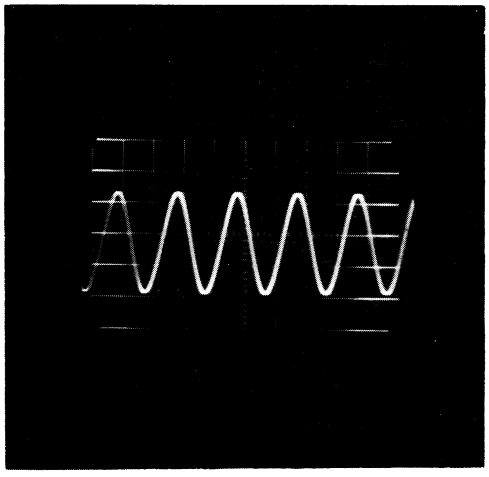


Fig. 4.25. 10 Mc output signal of DFG-1.

and lastly, a different number of steps per significant figure might be more appropriate, especially if remote programming is anticipated.

CHAPTER V

SUMMARY AND CONCLUSIONS

5.1 Introduction

In the preceding chapters it has been demonstrated that effective use can be made of nonprecise tuning components in unique techniques for precise frequency synthesis.

The nonprecise components which are examined in detail under the several limiting conditions of operation are solid-state devices such as controllable inductors, ferroelectric capacitors, and variable capacitance diodes.

5.2 Summary of Results

The significant consequences of this investigation result from the extreme flexibility afforded by completely electronic tuning methods. The incorporation of the nonprecise components through the use of phase-lock circuitry has made it possible to develop a technique of frequency synthesis which permits rapid selection of precise frequencies, is adaptable to both remote control and electronic programming, and theoretically, is unlimited in frequency range of operation.

A study of various electronic tuning methods using solid-state devices is carried out in Chapter II. This study formulates basic decisions regarding the limitations of tuning elements and voltage controlled oscillator parameters.

The system concept of a generalized discrete-frequency synthesizer is presented in Chapter III. The significant contribution of combining a discrete-frequency reference and an electronically-tuned phase-lock oscillator in the generation of precise frequencies is that it is possible

to construct a unit whose output frequency can have certain discrete values. This unit, called a discrete-frequency generator, has an output frequency which is precisely one of the harmonics of the discrete-frequency reference. By using several discrete frequency generators, each with different incremental steps, combining and taking the mixed output, it is possible to cover a wide over-all range in small incremental steps.

The question of how to minimize for a given power spectrum the peak-to-peak amplitude of a signal is presented. A term "peak factor" is defined and a relationship which can be effectively used as a figure of merit in the design of an appropriate frequency spectrum is developed. In addition, a study and evaluation of various methods for the efficient production of high-order harmonics with balanced energy in the frequency band of interest is carried out.

Of the various methods presented for generating a discrete-frequency reference, the shift register generator method is particularly interesting. The digitally-generated linear maximal sequence fulfills the condition of minimum peak factor while providing a reasonably uniform amplitude spectrum over a given band of interest. From a practical point of view the shift-register generator is simple to implement. Logic modules can be taken off the shelf and put together to form a discrete frequency reference. In addition, by using clock dividers and coincidence gates in conjunction with the shift-register generator, it is possible to obtain any number of discrete-frequency references each with different incremental steps.

The basic operating principles of a phase-lock loop are presented and analyses are made in instances where the literature is not complete. In particular, a figure of merit is developed which determines the effects

of frequency sensitivity and loading of the tuning element on the controlled oscillator. In addition, equations for the convergence time of a phase-lock loop are developed.

An analysis of the problem of combining two signal frequencies to obtain a single frequency in the form of their sum or difference while using phase-lock oscillators of a practical design is carried out.

In Chapter IV the design, construction, and testing of a two-digit synthesizer was carried out to demonstrate the practicability of the system. The synthesizer was designed to tune over a 1 Mc range in 10 kc steps (two significant figures). If additional significant figures are desired or a larger operating range is required for a specific application, additional modules may be added. The discrete-frequency reference is provided by a five-stage shift-register generator. The primary reference is a standard crystal which has a long-term frequency stability of one part in 10^5. Over-all system stability may be increased by increasing the stability of the primary reference.

The purity of the output signal was examined under steady-state conditions and it was found that the greatest contribution of noise was due to intermodulation of adjacent reference harmonics in the detector of the phase-lock loop. This intermodulation produces spurious sidebands at multiples of the reference generator repetition rate. In this particular synthesizer the spurious output is 50 db below the desired output. Additional sideband suppression may be obtained by improving the low-pass filter characteristics or using a prefiltering technique between the discrete-frequency reference and the phase-lock oscillator. Loop noise primarily due to the dc amplifier and discrete-frequency reference is confined to frequencies below approximately 1 kc/sec and was found to be

too low to degrade the output signal significantly.

The convergence time of the over-all system is less than 250 μsec in 10 kc steps. In 100 kc steps the convergence time is less than 100 μsec and could be reduced to ~ 20 μsec by reducing the time constant of the drive network.

5.3 Suggestions for Further Research

The results of this investigation suggest several problems which seem worthy of study:

(a) An investigation of basic techniques associated with generating a uniform amplitude frequency spectrum with the maximum amount of the total available spectrum energy in the band of interest and with a minimum peak-to-average energy ratio is recommended. An approximate approach to the problem is presented in Chapter III, Section 3.1.

(b) While it is permissible to assume small phase angles for the study of the synchronized system thereby linearizing the differential equation, this simplification cannot be made for the evaluation of the pull-in performance of the system. The solutions to nonlinear differential equations are necessary if one is to establish the limit of synchronization. With 1st- and 2nd-order nonlinear differential equations the limit of synchronization can be found graphically as indicated in Chapter III. However, the solutions to higher order nonlinear

differential equations (as would be the case if more complex control networks were used) become very unwieldy. It is suggested that a detailed investigation of high-order systems employing generalized nonlinear techniques would allow one to describe the pull-in behavior of an APC system more completely and to derive the optimum system parameters required for any particular application.

(c) To date, the analyses of phase-lock oscillators have been restricted to sinusoidal reference signals. In some cases the analyses have included the effects of white Gaussian noise along with the reference signal. Since the analyses of phase-lock oscillators with arbitrary periodic reference signals have not appeared in the literature, and since this problem is pertinent to synthesizer design, additional study should perhaps be undertaken.

(d) Since only one of the reference components of the discrete-frequency reference need be available to the VCO at one time, improved stability and efficiency result if the unwanted components are suppressed. A promising technique (as described in Chapter III, Section 3.2.2) for implementing spectral sorting arises through the properties of reactive mixers. With further research in this area, it might be possible to employ this technique

directly as a frequency synthesizer, thus eliminating the need of an additional output oscillator.

(e) The availability of a means of precise tuning and rapid frequency selection at remote locations suggests further work on, and exploitation of the discrete-frequency synthesizer. Since the synthesizer may be readily programmed using analog or digital techniques, it is applicable to frequency-hopping communication systems where precise tuning and rapid frequency selection are requirements. In addition, it may be used to advantage where several slave receivers at remote locations must be tuned to precisely the same frequency as required in remote-controlled direction finding nets. A further application is in airborne navigation systems requiring fast selection of predetermined channels, as required by high performance aircraft.

APPENDIX A

COMPARISON OF ELECTRONIC TUNING DEVICES

	Magnetic Tuning Units	Ferroelectric Capacitors	Variable Capacitance Diodes
Size	~ 1 cu. in.	.001 cu. in.	.003 cu. in.
Weight	1 oz.	< 10 gms.	< 10 gms
Temp. Sensitivity	.04%/C° @ 10 ma	1%/C° @ 20 v	.025%/C° @ 4 v
Hysteresis	Yes	Yes	No
Available Frequency Tuning Ratio at			
1 Mc	12:1	3:1	2:1
100 Mc	2:1	3:1	2:1
500 Mc	1.3:1		
1000 Mc		1.5:1	1.3:1
Maximum Useful Frequency	< 500 Mc	1 kMc	10 kMc
Q for f = 10 Mc	7200	~ 200	> 200
100 Mc	50	750	750
1000 Mc	10 @ 500 Mc	~ 5 @ 3 kMc	~ 10 @ 10 kMc
Open Loop Set-on Accuracy (% of range)	3 - 5%	5 - 10%	1 - 2%
Tuning Power Requirement	~ 1 watt	Negligible	Negligible
Control Cirrent or Voltage Range	0 - 50 ma	0 - 200 volts	0 - 60 volts
Restriction in Amplitude of RF	—	—	Peak RF voltage must not exceed back bias value
Remarks	Rugged construction Fairly expensive Matched pairs are expensive	Cheap to manufacture Matched pairs are cheap	Fairly cheap to manufacture Matched pairs are expensive

APPENDIX B

LIMITATIONS ON SRG USED FOR DECADE SPECTRAL DIVISION

The following is proof that the only limitations on the shift-register generator used for decade spectral division are that:

(1) It be a maximal sequence, and

(2) The number of stages is not a multiple of 4.

Lemma $5 \mid 2^n - 1 \iff 5 \mid 2^{n-4} - 1$

Proof

$\Longleftarrow$:

$$2^{n-1} = 2^4(2^{n-4}) - 1$$

$$= 16(2^{n-4}) - 16 + 15$$

$$= 16(2^{n-4} - 1) + 15$$

If $5 \mid 2^{n-4} - 1$ and since $5 \mid 15$, then 5 divides the right hand side. This means 5 divides the left hand side which is $2^n - 1$.

$\Longrightarrow$:

$$(2^n - 1) - 15 = 16(2^{n-4} - 1)$$

If $5 \mid 2^n - 1$ and since $5 \mid 15$, then 5 divides the left hand side. This means 5 divides the right hand side which is $5 \mid 2^{n-4} - 1$.

Note 5 and 16 have no common factors; therefore, the only way 5 can divide the right hand side is for $5 \mid 2^{n-4} - 1$.

Theorem $5 \mid 2^n - 1 \iff 4 \mid n$

Proof

$\Longleftarrow$: $4 \mid n$

Note that $5 \mid 2^4 - 1$.

By induction using that part of the lemma dealing with increasing index, i.e., $(5 \mid 2^{n-4} - 1 \implies 5 \mid 2^n - 1)$ implies $5 \mid 2^{4 \cdot m} - 1$.

$\Longrightarrow$: If one were to assume that $5 \mid 2^k - 1$ where k is not a multiple of 4, then applying the lemma with the finite number of steps in direction of decreasing index (i.e., $5 \mid 2^{n-1}$), implies $5 \mid 2^{n-4} - 1$.

We find that 5 divides one of the numbers $2^1 - 1$, $2^2 - 1$, or $2^3 - 1$, but since 5 divides none of these the assumption that $5 \mid 2^k - 1$ where k is not a multiple of 4 is absurd.

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32	Chief, Bureau of Ships, Code 691C, Department of the Navy, Washington 25, D. C.
33	Chief, Bureau of Ships, Code 684, Department of the Navy, Washington 25, D. C.
34	Chief, Bureau of Naval Weapons, Code RAAV-33, Department of the Navy, Washington 25, D. C.
35	Commander, Naval Ordnance Test Station, Inyokern, China Lake, California, ATTN: Test Director - Code 30
36	Director, Naval Research Laboratory, Countermeasures Branch, Code 5430, Washington 25, D. C.
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38	Director, Air University Library, Maxwell Air Force Base, Alabama, ATTN: CR-4987
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40	Office of the Chief of Ordnance, Department of the Army, Washington 25, D. C., ATTN: ORDTU
41	Chief, West Coast Office, U. S. Army Signal Research and Development Laboratory, Bldg. 6, 75 S. Grand Avenue, Pasadena 2, Cal.
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43-44	Chief, U. S. Army Security Agency, Arlington Hall Station, Arlington 12, Virginia, ATTN: IADEV
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46	President, U. S. Army Airborne and Electronics Board, Fort Bragg, North Carolina
47	U. S. Army Antiaircraft Artillery and Guided Missile School, Fort Bliss, Texas
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52	Operations Research Office, John Hopkins University, 6935 Arlington Road, Bethesda 14, Maryland, ATTN: U. S. Army Liaison Officer
53	The John Hopkins University, Radiation Laboratory, 1315 St. Paul Street, Baltimore 2, Maryland, ATTN: Librarian
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56	ITT Laboratories, 500 Washington Avenue, Nutley 10, New Jersey, ATTN: Mr. L. A. DeRosa, Div. R-15 Lab.
57	Director, USAF Project Rand, via Air Force Liaison Office, The Rand Corporation, 1700 Main Street, Santa Monica, California
58	Stanford Electronics Laboratories, Stanford University, Stanford, California, ATTN: Dr. R. C. Cumming
59	Willow Run Laboratories, The University of Michigan, P. O. Box 2008, Ann Arbor, Michigan, ATTN: Dr. Boyd
60	Stanford Research Institute, Menlo Park, California, ATTN: Dr. Cohn
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65	Commanding Officer, U. S. Army Signal Research and Development Laboratory, Fort Monmouth, New Jersey, ATTN: U. S. Marine Corps Liaison Office, Code AO-4C
66	President, U. S. Army Signal Board, Fort Monmouth, New Jersey
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76	Director, National Security Agency, Fort George G. Meade, Maryland, ATTN: TEC
77	Dr. B. F. Barton, Director, Cooley Electronics Laboratory, The University of Michigan, Ann Arbor, Michigan
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