JOURNAL OF ELECTRONIC TESTING: Theory and Applications, 5, 347–365 (1994)

Technology and Layout-Related Testing of Static Random-Access Memories

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Received December 1, 1993; Revised June 9, 1994.
Editor: V.D. Agrawal

Abstract. Static random-access memories (SRAMs) exhibit faults that are electrical in nature. Functional and electrical testing are performed to diagnose faulty operation. These tests are usually designed from simple fault models that describe the chip interface behavior without a thorough analysis of the chip layout and technology. However, there are certain *technology and layout-related* defects that are internal to the chip and are mostly time-dependent in nature. The resulting failures may or may not seriously degrade the input/output interface behavior. They may show up as electrical faults (such as a slow access fault) and/or functional faults (such as a pattern sensitive fault). However, these faults cannot be described properly with the functional fault models because these models do not take timing into account. Also, electrical fault models that describe merely the input/output interface behavior are inadequate to characterize every possible defect in the basic SRAM cell. Examples of faults produced by these defects are: (a) static data loss, (b) abnormally high currents drawn from the power supply, etc. Generating tests for such faults often requires a thorough understanding and analysis of the circuit technology and layout. In this article, we shall examine ways to characterize and test such faults. We shall divide such faults into two categories depending on the types of SRAMs they effect—silicon SRAMs and GaAs SRAMs.

Keywords: Array layout, cell technology, Gallium Arsenide (GaAs), high electron mobility transistor (HEMT) RAMs, I_{DD} testing, I_{DDQ} testing.

1. Introduction

During the last two decades, the increasing complexity and speed of SRAMs has necessitated rapid advancement of testing techniques. The complexity of testing and cost of test equipment have also gone up considerably. The major driving force for manufacture of SRAMs has been high quality, yield and throughput. In the early days of memory testing, only electrical and parametric measurements were performed at the interface. Increasing speed of memory devices necessitated rigorous speed tests such as access time tests to verify correct functionality. These tests came to be classified under AC parametric tests. With increased complexity, it became necessary to perform algorithmic functional testing as well as electrical testing. These two techniques were often employed together to analyze faults associated with electrical and functional behavior, which were often correlated. Both these techniques use very simple fault models, such as stuck-at, coupling, and delay fault models. The tests designed around these simple fault models were found to have a good fault coverage but not necessarily a good *defect* coverage. As time passed, a need was felt to devise new tests for defects and faults by examining the under-

lying layout and the cell *technology*. It has been found that a large number of defects that might translate into faults are technology-specific. A GaAs SRAM, for example, has a different set of canonical fault types than a silicon SRAM, because of some unique processing and device characteristics. The array layout is a function of the cell technology and defects therein must be analyzed for a proper understanding of testing requirements.

This article describes attempts till date to characterize and test faults caused by layout-related defects in SRAM cell arrays. There are three popular techniques used in such characterization and testing. Often, these techniques are used together. They include:

- **Simulating the effect of layout defects**: Defects such as broken pullup transistors, floating gates, etc. in the SRAM cell are analyzed quickly and modeled accurately. One common approach is the *inductive fault analysis* (IFA) technique which models shorts and opens as spots of missing metal or extra metal respectively. Another popular approach is to design an equivalent circuit of the SRAM cell in the presence of the defect. Computer simulation or equivalent circuit analysis is then performed to design the fault model or the *fault-defect vocabulary*.
- **Current measurements**: Physical measurement of the quiescent and dynamic currents drawn from the power supply (called I_{DDQ} and I_{DD} respectively) is also a very popular technique. Defective SRAM cells are typically associated with an abnormally large value of these currents.
- **Simulating the effect of varying circuit parameters**: This is done by designing a simplified equivalent circuit model to predict fault effects of varying circuit parameters and verifying these using analog circuit simulators such as SPICE. This technique is very useful in measuring limits of correct operation of SRAMs.

We shall now describe some past work in this area on testing silicon SRAMs and then give a detailed account of our own work in the area of fault modeling and testing of Gallium Arsenide (GaAs) SRAMs.

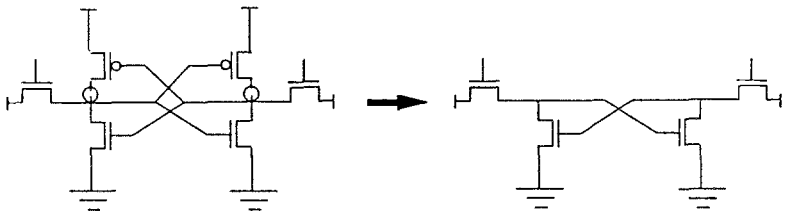
2. Faults in Silicon SRAMs and Their Testing

Silicon SRAMs exhibit a variety of faults that are technology and layout-dependent. A variety of approaches have been used to study and test these faults. Some of these approaches are based on modified functional test algorithms and others are based on a study of the actual electrical characteristics of faulty SRAM layouts. These faults and their tests are described below.

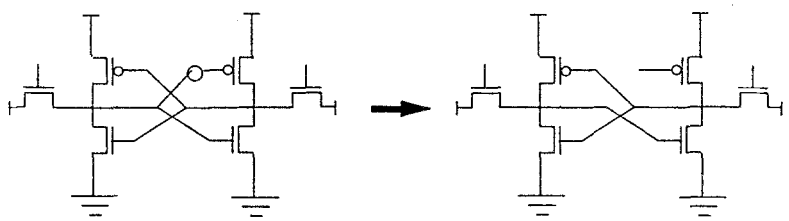
2.1. Testing for Static Data Loss

SRAM devices can lose data stored in them because of leakage currents that can change the state of the cell when the pull-up device is defective or broken such that it forms an open circuit. In SRAMs, the function of the pull-up device (which is often a depletion mode NMOS with gate shorted to source, and should, theoretically, act as a resistance) is to supply the leakage current to hold the cell in its state.

Testing for static data losses in SRAMs is a difficult task. The difficulty arises because static data losses typically start to occur after long periods of time (of the order of seconds or even more) and that would result in impractical delays in testing. Testing them under worst case conditions (called 'burn-in') to accelerate failure is also not very reliable because it is known precisely how chips age under burn-in conditions with regard to static data losses. Dekker [7, 8] described how to detect static data losses in SRAMs with 100 GΩ resistors as pull-up devices. Dekker noticed a broken pull-up resistor to cause a static data loss in about 100 ms. He then modeled this defect using the *inductive fault analysis* (IFA) technique in which shorts and opens are represented as spots of extra metal or missing metal. Computer simulation or manual analysis using equivalent circuits can then be used to design a suitable fault model. Dekker proposed the algorithm IFA-9 (Inductive Fault Analysis-9) also known as '9N Test' around such a fault model based on the chip



(a) Open source fault and its equivalent circuits



(b) Open gate fault and its equivalent circuit

Figure 1. Fault model used by the SDD technique; courtesy [14].

layout. This algorithm uses a march test with two delays of 100 ms each.

A technique known as *soft-defect detection* (SDD), accomplished at room temperature was described by Kuo et al. in [14]—this provides a complete data retention test of a CMOS SRAM array. The SDD technique has two components—an *open circuit* test that checks for connectivity of the *p*-type load transistor, and a *cell-array* test that carefully monitors the standby array current to detect abnormally high current leakage. The technique is described below.

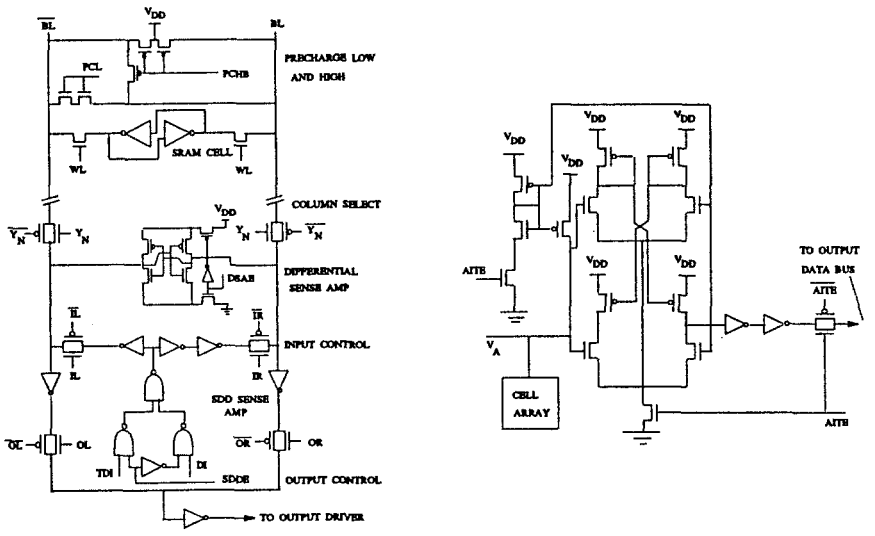
2.1.1. Fault Model Used by the SDD Technique. An SRAM cell consists of a pair of cross-coupled inverters. In the SDD technique, each of the two cross-coupled inverters is tested independently. This model is shown in Figure 1.

Testing two cross-coupled inverters independently has its own problem: the parasitic effect of one inverter can clamp the input 1 level from reaching the switching point of the other inverter. The clamping can be overcome by reducing the ratio of the conductance between the driver and the access transistors. This can be achieved at the device fabrication level by decreasing the size ratio between the driver and access transistors, or at the circuit level by reducing the gate voltage for the driver transistor with respect to the access transistor.

Simulation studies performed by the authors indicate that lowering the array supply voltage to 2.9 V would cause an acceptable switching time for both input 0 and input 1 for a fault-free SRAM cell. Accordingly, the targeted layout and circuit parameters used were: array supply voltage: 2.9 V, threshold for passing or failing the SDD open-circuit test: 150 ns. They used an effective channel length of 0.95 μm for all cell transistors, and a gate voltage of 5 V for the access transistors.

2.1.2. The SDD Test Strategy. The SDD test strategy consists of (a) an open circuit test, for testing the right as well as the left inverters; and (b) a cell-array current test, for fine-tuning the above test by performing a built in or external test of the array current with an all zero and an all one data background.

1. **SDD Open-Circuit Test:** In this test, each inverter is independently provided with a 0 (1) input and its output simultaneously examined for a 1 (0) level. This requires simultaneous read and write operations to the cell under test, which is done using a special circuit de-



(a) (b)

Figure 2. Circuit technique for (a) the SDD open-circuit test, and (b) cell-array current detection test; courtesy [14].

sign to be discussed shortly. An open circuit at the gate or the drain of the load might result in an abnormally long time for the output to respond to the input, if at all it responds. However, even if a cell passes this test, it does not necessarily follow that it is not defective; simulation studies done indicate that a defective cell with a floating-gate P-channel load transistor can actually pass this test when the effective conducting P-channel current is between 50 and 290 μA for the prescribed 150 ns switching time. Therefore, the next test is also used in conjunction with the open-circuit test.

2. **Cell-Array Current Test:** With a background of all 0s (all 1s) for the left (right) inverters, a floating gate transistor of a faulty SRAM cell that passed the open-circuit test might produce an abnormally large standby current, which may be greater than the normal array leakage current. The authors have designed an internal current detection circuit for the SDD cell-array current test.

2.1.3. Circuit Design. The circuit diagram for the SDD open-circuit test is shown in Figure 2. The circuit is described below.

This circuit can perform simultaneous read and write operations—this is necessary since the switching response of an inverter is verified by applying an input signal (write) and simultaneously detecting the output signal (read). This can be achieved if the right (left) output transmission gate and the left (right) input transmission gate are simultaneously activated. One of the two input transmission gates ($IL/\overline{IL}$ or $IR/\overline{IR}$) and the corresponding output gate ($OR/\overline{OR}$ or $OL/\overline{OL}$) are activated using a mux and inverters as shown in Figure 2.

During the open-circuit test, the bit-line pair has to be precharged high and low (depending on whether the input is coming from the left or the right), so that switching times under both conditions are verified. This necessitates the incorporation of a special precharge circuit as seen in Figure 2.

We already noted that the open circuit test considers each inverter of a cross-coupled pair independently. Since during this test, we are not performing a normal read operation (i.e. precharging to high both the lines of the bit-line pair initially and then sensing differential voltage at the outputs of the cross-coupled inverters), the sense amplifier has to be completely isolated from the bit-line pair. This was achieved by gating a control signal called $DSAE$ to the sense-amplifier.

The array supply voltage is clamped to the prescribed 2.9 V from the usual 5 V using a special circuit, as shown in Figure 2. For the second

part of the test strategy (the cell array current test), the authors have used a current-mirrored differential sense amplifier to compare the cell array current to a reference current. This current detection can be performed at high speed if the array power node V_A is precharged to the switching point of the differential sense amplifier, and then disconnected from the power supply V_{DD} during the array current detection.

2.1.4. Effectiveness of the SDD Scheme. The SDD circuitry can be fully built-in with only a 2% increase in the module area for a 16 Kb array, and this percentage decreases for a larger array size. The total SDD test time for the 16 Kb module is about 1.5 ms, with most of the time being spent for current testing. Also, in an experimental 16 K module, SDD was found to identify a greater percentage of defective cells than contentional test patterns such as marching 0s and 1s.

2.2. I_{DDQ} Testing Using the Inductive Fault Analysis Approach

This testing paradigm also uses a test metric dependent on the detection of *defects*, rather than *faults*. A defect is an actual physical condition of the hardwave that might manifest itself as a fault. A defect is physically injected into the layout in this scheme; for example, it may be modeled as a spot of extra metal or missing metal in the layout. This test monitors the quiescent power supply current (denoted by I_{DDQ} (for CMOS ICs), which should be very small under normal conditions) for each test vector, and detects any defect that causes abnormally high values of this current. For example, a short or an abnormal leakage causes a state dependent I_{DDQ} which is typically a few magnitudes larger than the steady-state quiescent value under normal conditions, the reason being that both the n- and the p-transistors will be turned on. The effectiveness of I_{DDQ} testing for SRAM chips especially for short circuit and open circuit defects has been demonstrated by Meershoek [18, 19], and electrical effects caused by stuck-open faults in CMOS ICs have been tested by Soden et al. [28] using this paradigm.

Soden et al. [28] have shown that I_{DDQ} measurements can detect stuck-open faults (SOF) in *some* designs, but not necessarily in all. Their experiments were performed on a static CMOS ROM SA3002 (2k × 8), which is functionally equivalent to the Intel 8355. They analyzed open metal defects in the drain interconnections of NMOS transistors located in the NOR gates of the address decoders of these ROMs. These open metal defects caused a high-impedance state at the output when certain test patterns were applied. Some defects which they dealt with were defective metal patterning (for example, missing metal in a long section on top of the polysilicon and intermediate oxide that ends abruptly at the edges of the polysilicon), this defect was believed to be the result of the failure of the photoresist to adhere in this region of the mask. The chip failed a ping-pong test in which the contents of each memory address were read before and after those of every other address—abnormally high I_{DDQ} values were associated with these failures.

It has been found that the measurement of I_{DDQ} is a very sensitive technique for the detection of stuck-open defects in CMOS ICs. Hence the time constant of the floating node is important for establishing the validity of the I_{DDQ} measurement technique for such defects; the time constant should be small compared to test vector clock periods, otherwise the elevated value of I_{DDQ} will be slow to be detected in the same vector that causes the high-impedance state.

The effectiveness of the I_{DDQ} fault model was investigated by Meershoek [19]. They used a special I_{DDQ} monitor that used an op-amp-controlled current mirror circuit to measure the current. The other tests that they performed were continuity checks, functional march tests, current tests for the standby read and write currents. The set of these four tests was found to produce a highly sensitive and effective test program.

2.2.1. More Recent Inductive Fault Analysis Testing in SRAMs Using High-Resolution Vocabulary of Defects and I_{DDQ} Testing. Naik et al. [22] performed failure analysis of high density CMOS SRAMs using realistic defect modelling

and I_{DDQ} testing. The authors have proposed the improvement of yield by the use of a methodology for rapid and accurate failure analysis, developed at Carnegie Mellon University [15, 16]. This methodology performs defect modeling with the help of a realistic *high-resolution fault-defect vocabulary.* Such a vocabulary consists of multi-dimensional failure representations obtained by simulating both functional and I_{DDQ} testing. The authors have summarized results obtained through the application of this methodology for a high density SRAM fabricated in a 1.2 μ CMOS process at the Philips IC Advanced Development and Manufacturing Center, Eindhoven, the Netherlands.

Introduction of redundant rows and columns (for example, for self-repair of embedded memories) has triggered interest in memory testing capable of indicating geometrical characteristics of defective parts of the memory. A widely used diagnostic approach is the use of bit-maps of faulty cells. A *bit-map* is an image of the memory core with marked defective cells. Use of a bit-map in failure analysis has many advantages and great potential for enhancements which may greatly improve the resolution of defect diagnosability. The traditional bit-map approach has a very serious limitation, namely, poor resolution of the mapping from defects (or signatures thereof) to bit-maps, as explained below.

A traditional approach to failure analysis of memories chooses a set of easy-to-predict defects and converts each into a pattern of failing bits in a bit-map, called a *signature*. A typical defect-signature relation may be provided by analyzing a spot of extra metal shorting the *bit* and $\overline{bit}$ lines of a single column. Thus, an entire column of cells will be marked as faulty. When such a pattern appears in a bit-map, it may be concluded that the probable cause is a spot of extra metal with diameter smaller than 2λ of metal lines plus 3λ spacing between these lines and larger than one spacing.

Now the spectrum of distinct signatures in the defect to bit-map vocabulary is usually small and incomplete, meaning that not every signature maps to a unique bit-map and actual bitmaps generated during testing may not be found in the defect-signature vocabulary. Hence, adhoc

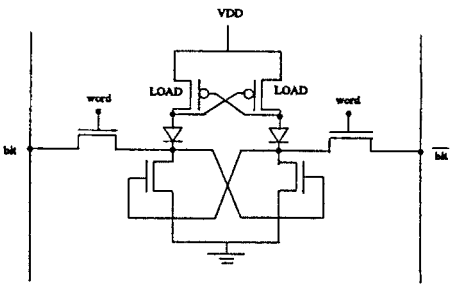


Figure 3. One cell of the Philips 64 K SRAM; courtesy [22].

methods for builting the defect-signature vocabulary cannot support potentially high resolution of defect diagnosis.

Naik et al. in their article [22] have built a high-resolution vocabulary by using an Inductive Fault Analysis (IFA) approach. The last step of an IFA approach, namely, evaluation of the result of testing of the defective memory, is the most expensive and the most important in improving diagnostic resolution. So instead of producing 'black-and-white' bit-maps consisting of the mere identification of faulty and fault-free cells, 'colored' bitmaps that contain information pertaining to full electrical characterization of affected cells is necessary for higher resolution.

The authors conducted their study on the Philips 64 K full CMOS SRAM chip, fabricated in a 1.2 μ twin-tub CMOS process with a p epitaxial layer on a $p+$ substrate using single polysilicon and double metal interconnect. This cell has a standard structure with 4 NMOS transistors, 2 pMOS transistors and 2 polysilicon diodes, as shown in Figure 3. The *bit* and $\overline{bit}$ are formed using second metal while the global rows, power and ground lines are horizontally running first layer metal. The word-line is made of polysilicon and runs horizontally. The cross-coupled connections within each cell are made with buried contacts to both $n+$ and $p+$ diffusions using n and p type polysilicon gate material respectively.

In the horizontal direction, the memory array has 16 blocks that are 32 bits (or 4 bytes) wide; in the vertical direction, there are 128 rows. Addressing of a byte involves (a) appropriate row selection (1 row out of 128), (b) appropriate block selection (1 block out of 16), followed by

(c) appropriate byte selection (1 byte out of 4). Each memory cell can be independently accessed. Each block has 32 vertical *bit-$\overline{bit}$* line pairs. Read and write operations are performed in the usual manner.

Generation of the defect-signature vocabulary was done using Monte Carlo simulation. The authors used the minimum repeatable section of the layout (an 8×2 cell portion of the core). The defect simulator, VLASIC was used to randomly place 150,000 spot defects on the layout and determine what circuit faults, if any, had occurred. There were two operations which the defect simulator performs: (a) extraction of defects that are too small to cause a change in the electrical diagram of the circuit; (b) grouping of defects causing exactly the same modification of the circuit (for example, all defects shorting the same two nodes in the circuit are grouped together).

The vocabulary was formed by considering one representative from each group formed in step (b). The authors first identified defects that had easily predictable signatures on the bit-map, and then they looked into those for which signatures had to be obtained by extensive circuit simulation. The authors found out that only about 3000 of the 150,000 defects were major ones that had to go through step (b) of the two-step operation above, and only about 300 of these had to be analyzed to form the vocabulary. The authors have stated that approximately 10% of these cases were evaluated by inspection and the rest were simulated using the Philips inhouse circuit simulator, described below.

For simulating electrical testing, they used a neighborhood of 5×5 cells surrounding the defective cell in order to mimic all the load effects. Instead of performing the extremely expensive task of applying all 2^{25} possible combinations to the neighborhood, they struck a compromise between cost of simulation and diagnostic information obtainable by applying test vectors such that only the defective cell and its eight immediate neighbors are tested with all possible combinations of 0s and 1s.

They generated 67 unique bit-map patterns in the end. Each such pattern was found to correspond to a certain set of possible defects that caused it. The smaller the cardinality of this set, the greater the resolution of the pattern. It was found that diagnostic resolution can be increased if the number of possible defects causing a certain pattern can be narrowed down using current (I_{DDQ}) measurement simulations.

2.3. Testing of SRAMs by Monitoring I_{DD}, the Dynamic Power Supply Current

While I_{DDQ} testing was fairly effective in detecting a general variety of CMOS defects not usually considered by functional testing, for example gate oxide short, punch-through and leakage, it was found to have some shortcomings [29]. It is mostly limited to fully complementary logic (one that ideally draws no current from the supply during quiescent steady state conditions, and draws current only during switching transients), and is typically slower than voltage-type testing. Moreover, I_{DDQ} testing alone is often not sufficient and it is usually regarded as a good way of augmenting functional testing (stuck-at) to achieve greater defect coverage. To make I_{DDQ} testing faster, the soft-defect-detection approach [14], described earlier, used the concept of built-in current monitors for fast current sensing.

The idea of I_{DDQ} testing has been recently extended to I_{DD} testing. In this technique, the *dynamic* power supply current is measured. As described a little later, there exists a relationship between the dynamic power supply current and a variety of SRAM defects causing pattern sensitive and stuck open faults. The technique described by Su and Makki [29] uses a novel technique for distributing power to the cell array, resulting in low area overhead and a high defect coverage of the above defects. Their built-in current monitors make the whole test scheme quite efficient.

2.3.1. Defect Models for I_{DD} Testing. Su and Makki [29] have studied the relationship between the dynamic power supply current I_{DD} and various RAM defects that induce pattern sensitive faults. Some defects they consider are cell open faults caused by opens in the wiring, gate, or along drain/source and cell short faults caused by breakdown in the insulating layer sep-

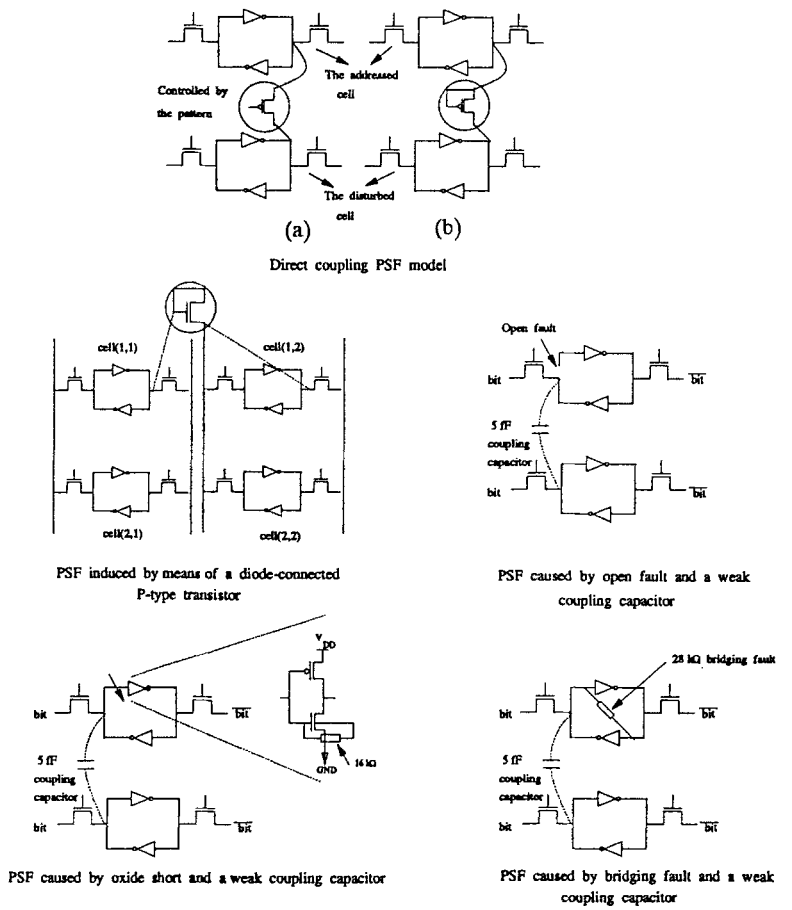


Figure 4. Defect models for I_{DD} testing; courtesy [29].

arating nodes belonging to different cells. Each class of defects resulted in a peculiar response of the dynamic power supply current I_{DD}. The various fault models for the defects under consideration are illustrated in Figure 4 [29].

The various pattern sensitive defects modeled by the authors are enumerated below:

1. **Diode-Connected Transistor Short:** An electrical coupling is induced between two SRAM cells using the model in Figure 4(a). This interaction is in one direction—logic changes in a cell c_1 affects the contents of another cell c_2, but not vice versa.
2. **Open Fault:** A PSF is induced as a result of an open drain fault in a cell (which prevents the pull-up transistor from reinforcing the bit-line voltage). This causes the cell to be easily disturbed by even a weak capacitive coupling to another cell. Such a cell is thereby very susceptible to pattern sensitivity. This fault model is shown in Figure 4(b).
3. **Gate Oxide Short:** A gate oxide short is modeled by a resistor shorting the gate to the substrate. This causes current to flow into the substrate as leakage current, as shown in Figure 4(c).
4. **Bridging Faults:** A resistive bridge between the inputs of two cross-coupled inverters in conjunction with a weak coupling capacitor between cells c_1 and c_2 having a value of about 20 fF, constitutes this fault model. Writing a 0 in cell c_2 causes cell c_1 to switch states.

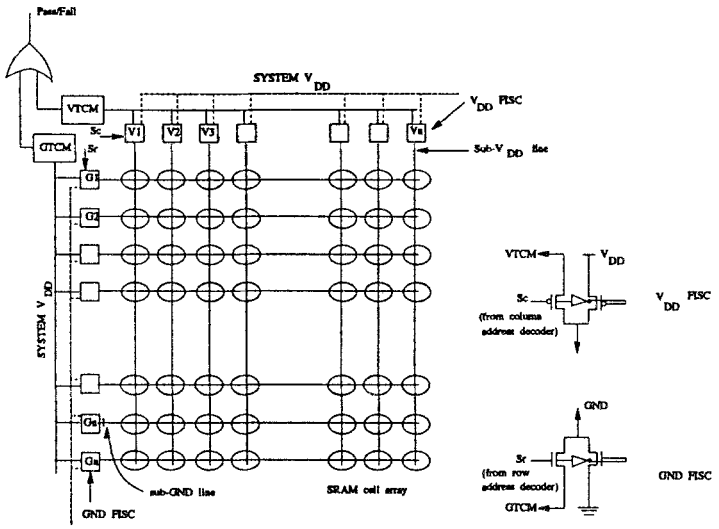


Figure 5. Circuit design for an I_{DD} testable SRAM; courtesy [29].

2.3.2. I_{DD} Response to the Above Defects. In a fully complemented CMOS circuit, a momentary current path, I_{DD}, between V_{DD} and ground is established only during the period of a state change. When a memory cell changes state, it is expected to produce a large I_{DD} pulse. Because of PSFs however, some other cell may also produce a large pulse. Thus a PSF can be detected under such conditions if the supply lines to each cell can be separately monitored.

The total I_{DD} response for each defect class has been studied by the authors. They concluded from their experiments that each state transition (whether intended or erroneous) results in a significant I_{DD} pulse of finite duration (about 2 ns). These pulses are detectable at the V_{DD} and ground rails. The cell whose state is being changed is expected to have a significant pulse; however, some other cell which is coupled to the first cell might also produce a significant pulse.

2.3.3. Circuit Techniques for I_{DD} Testing. The authors have designed an I_{DD}-testable SRAM structure by adding two current monitors—called VTCM (V_{DD} Transient Current Monitor), and GTCM (Ground Transient Current Monitor). In this scheme, the system V_{DD} and ground lines are distributed to all parts of the array through *F*ault *I*Solation *C*ontrol Circuitry (FISC). In this circuit, all cells on the same column share a common V_{DD} line, and all cells on the same row share a common ground line. The function of the FISC is to switch the supply lines to a given cell between the current monitors and the system power lines. The row and the column select lines are used to enable the FISCs. The circuit diagram is shown in Figure 5.

2.3.4. Circuit Performance and Overhead. Since an $\sqrt{n} \times \sqrt{n}$ SRAM array has a total of $2\sqrt{n}$ rows and columns, the number of FISCs required is $2\sqrt{n}$, using a total number of $8\sqrt{n}$ transistors, since each FISC requires 4 transistors. Since one VTCM and one GTCM are used, the cost of the FISCs becomes an overhead. The performance degradation noticed because of FISC with regard to rise and fall times is negligible. However, the individual cycle time for current monitoring may be about 25% longer than that for voltage monitoring. Other circuit overhead like additional input/output is seen to be negligible from the circuit design.

2.4. Faults in Gallium Arsenide (GaAs) SRAMs and Their Testing

Gallium Arsenide HEMT (high electron mobility transistor) devices, which are the fastest switching elements available today (with the exception of superconducting devices that oper-

ate at cryogenic temperatures), have now begun to make inroads into the world of commercial memory chip design. GaAs devices are preferred to superconducting devices because of their compatibility with ECL and other silicon logic families, and their ability to operate at room temperature. A 1 Kbit SRAM using GaAs HEMTs (high electron mobility transistors) may have a 500 ps access time, clearly outperforming both ECL and CMOS in terms of speed.

One major problem with GaAs memories is that the address access time over the whole address space varies as widely as 150 ps, i.e. 30% of the nominal access time. This problem has been attributed to process variations and design problems which are not normally encountered with silicon SRAMs. Parasitic resistances are a much more serious problem with GaAs devices because of higher currents and lower operating voltages. Leakage currents are much larger relative to the operating currents and voltage margins are low. Hence GaAs devices have a number of distinct failure modes, which lead to faults unlike those commonly seen in silicon. Mohan and Mazumder [21] have explored several of these failure modes and identified fault models and parametric test procedures for the faults.

Since the basic structure and processing sequence of GaAs devices are different from those of silicon MOSFETs, the failure mechanisms are also different. Systematic variations in process parameters, such as threshold voltage across a wafer and across a chip, are observed more prominently in GaAs than in MOS. Moreover, new failure modes such as inter-electrode resistive path formation [9, 10] have been observed in GaAs. As a result, fault modeling and testing of GaAs memory devices requires the identification and characterization of process, design and layout-related faults.

Failure modes of GaAs circuits lead to different types of faulty operation in SRAMs. Several kinds of pattern sensitive faults (PSFs) are studied by the authors. Some of these faults cannot be detected even by efficient test algorithms; knowledge of the cause of such PSFs is required in order to design efficient test procedures. Variations in process parameters are seen to result in delay faults. Another peculiar fact observed in GaAs SRAMs is that data retention faults have an entirely new mechanism, apart from the stuck-open mechanism observed in silicon [7, 14]. Parametric test procedures for these faults are described shortly.

The defects in GaAs wafers can be classified as primary and secondary defects. Primary defects are material-related ones affecting factors such as compositional purity, control of stoichiometry and crystalline perfection. These defects manifest themselves at the device level in the form of faults such as threshold voltage variation, mobility degradation and charge trapping. Deep donor levels associated with DX centers in the AlGaAs layer off the HEMT play a major role in electron capture and release [6], leading to various problems such as kinks in the V-I characteristics of the HEMT. Trap related problems result in threshold voltage and transconductance shifts with temperature changes [12]. Surface defects known as *oval defects* are a by-product of the material growth process [2]. These defects range in size from submicron levels to a few microns. The effect of an oval defect in the gate region of a HEMT is to prevent the transistor from turning off.

Threshold voltage variations over the wafer is a major problem in GaAs. With improved processing technology, this problem can be alleviated to some extent but never completely eliminated. Typical state-of-the-art parameters for threshold voltage variation over a wafer are as follows $V_{TE} = 0.278$ V; $\sigma(V_{TE}) = 11.3$ mV; $V_{TD} = -0.602$ V; $\sigma(V_{TD}) = 14.2$ mV, the subscripts denoting enhancement and depletion mode devices respectively.

Secondary defects, on the other hand, are the ones introduced during wafer processing in the form of surface and sub-surface damage. These defects are responsible for most of the observed faults in the circuit, such as SAF's, bridging faults, etc.

A major secondary defect associated with GaAs devices is ohmic contact degradation and interdiffusion of gate metal with GaAs. This results in increased *on* resistance of the transistor, and decreased saturation current and pinch-off voltage; it may also bring about gate-to-channel

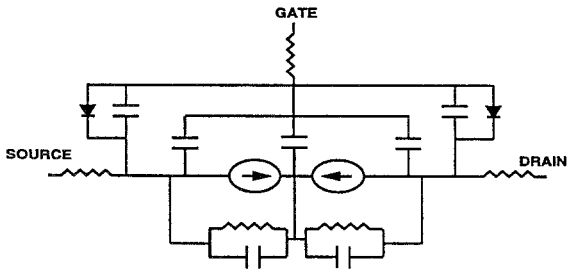


Figure 6. Equivalent circuit for HEMT.

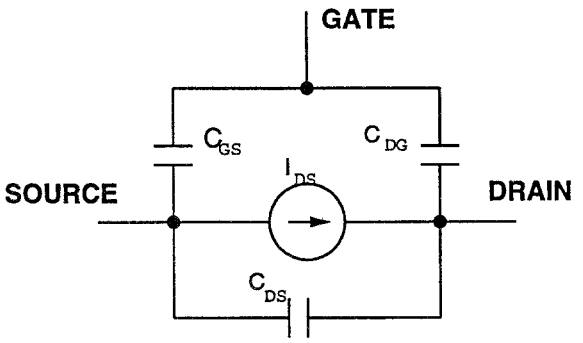


Figure 7. Simplified equivalent circuit for HEMT.

short. Further, the depletion-mode transistors may develop interelectrode metallic paths due to electromigration and processing defects. Fracturing may also some failure modes. For a discussion on these various failure modes, see [9, 10, 24, 25].

The basic memory cell consists of two cross-coupled inverters connected to complementary *bit* and $\overline{bit}$ lines via pass gates. This circuit is analyzed with the help of a simple equivalent circuit model, to identify the fault effects of variations in element parameters. This simplified analysis is then verified with the help of SPICE simulations using a more complex numerical model [31]. The HEMT model is shown in Figures 6 and 7 and is a simplified version of the model presented in [31] and used in the simulator [30]. Typically, the gate-source capcitance C_{GS} is the dominant capacitance term; C_{GS} is about five times C_{GD} and ten times C_{DS} [27]. The dependent current source equations and the read and write operations are explained in [21]. Static analysis of the memory cell during the read and write cycle provides information on the regions

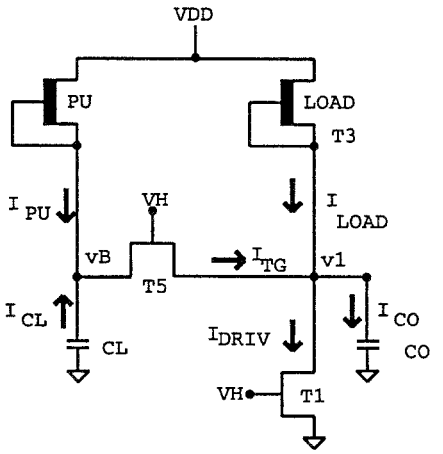


Figure 8. Devices involved in the read operation.

of correct, incorrect and slow operation (see Figures 12 and 13).

2.4.1. Design-Related Errors. Simulation Studies. To observe design-related errors, the memory circuits were simulated with different values of process and design parameters such as transistor widths and threshold voltages. These variations were found to either cause the circuit to operate very slowly or to become totally dysfunctional.

It was observed that as the thresholds for the depletion load and enhancement device are increased, the delay increases as predicted, finally resulting in erroneous operation. When the enhancement mode threshold voltage is reduced to nearly 0 V erroneous operation due to the inability of the enhancement mode transistors to turn off, was observed. The observed results were seen to be in agreement with the predicted ones.

Design-related errors were induced by varying the widths of the load resistor, transmission gate, the driver transistor and the bit-line pullup transistor. Since $\beta \propto W/L$, the β-ratio of two transistors is just the ratio of their widths if they have the same length. For studying design-related errors of GaAs SRAMs, therefore, the authors consider various ways of varying parameters of the circuit, such as

(a) varying the width of the transmission gate and load transistors (with the lengths kept constant), (b) varying the width of the pullup tran-

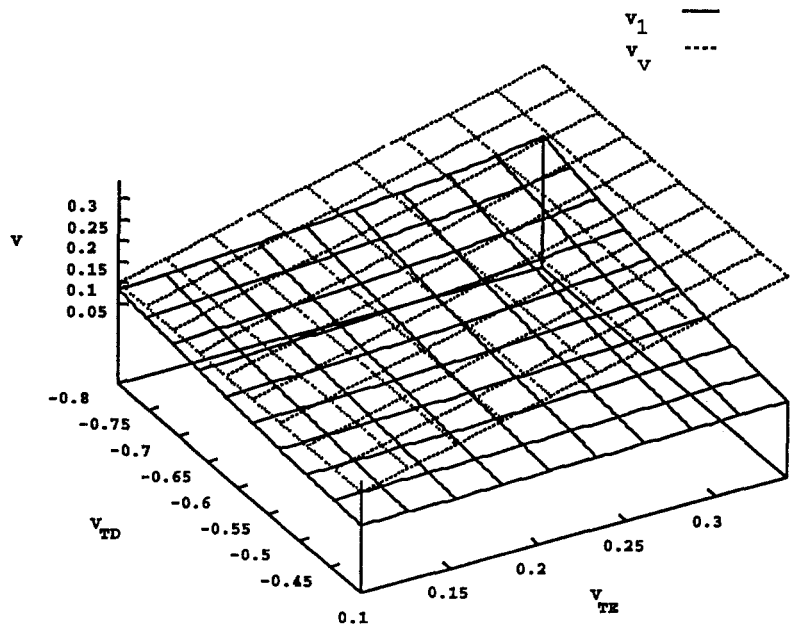


Figure 9. Variation of V_1 with threshold voltage.

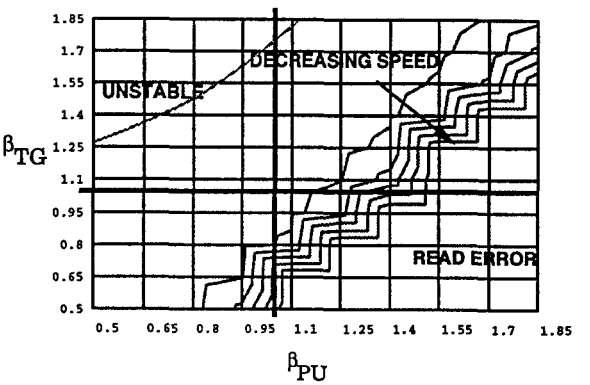


Figure 10. Read error as a function of pull-up (PU) and access transistor (TG) β's.

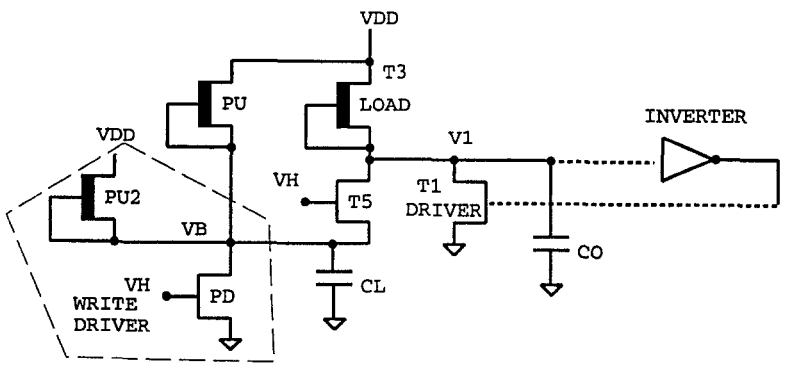


Figure 11. Simplified circit for analyzing the write operation.

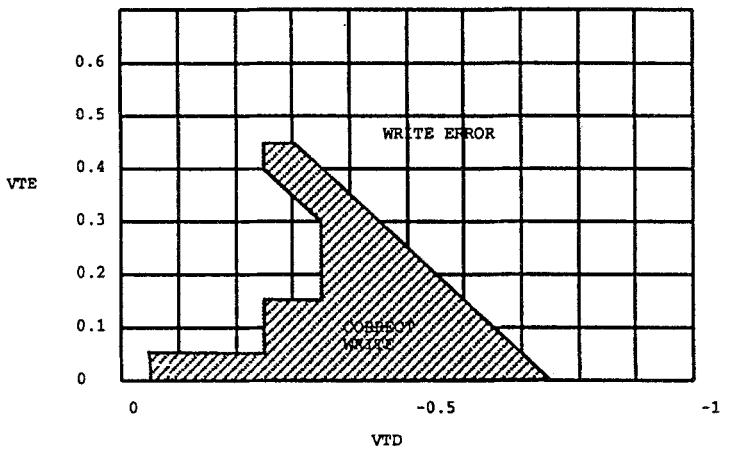


Figure 12. Write error as a function of threshold voltages.

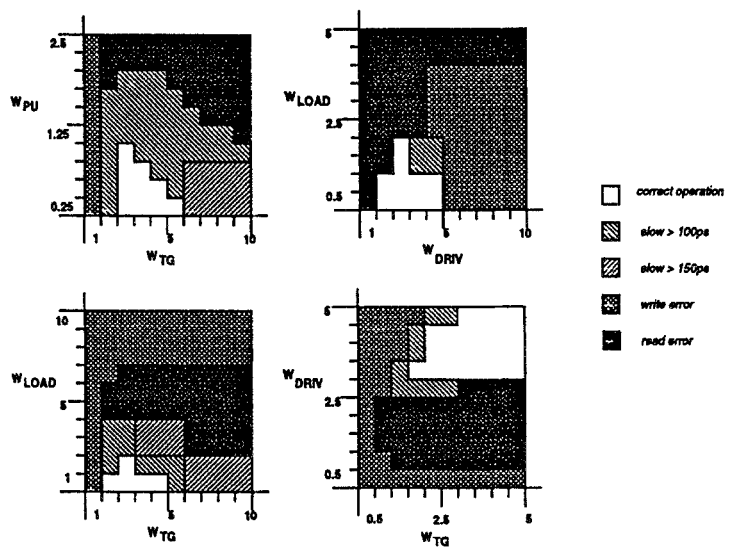


Figure 13. Effect of parameter variations: simulation results.

sistor and the transmission gate (again with the lengths constant), and (c) varying the width of the transmission gate and the driver, and measured the operating speed and functional integrity of the read and write operations.

When matched devices are used as in the differential input stage of the sense amplifier or in the memory cell itself, variation of device parameters can cause erroneous operation due to mismatching. However, the intra-chip or intra-die variation of parameters is very small and is not deterimental to proper circuit operation. Simulations have shown that a V_{TE} mismatch of 0.3 V is needed to cause wrong latching of the memory cell; the typical variation is of the order of a few millivolts. Similarly, the extent of the mismatch in transistor widths required to produce an error is equal to the nominal width of the transistor. These extreme conditions are more properly described as catastrophic failures rather than parameter variations, and will be described soon.

As the operating temperature of the device increases, the electron mobility decreases and parameters such as threshold voltage are seen to shift [5]. While the temperature dependence

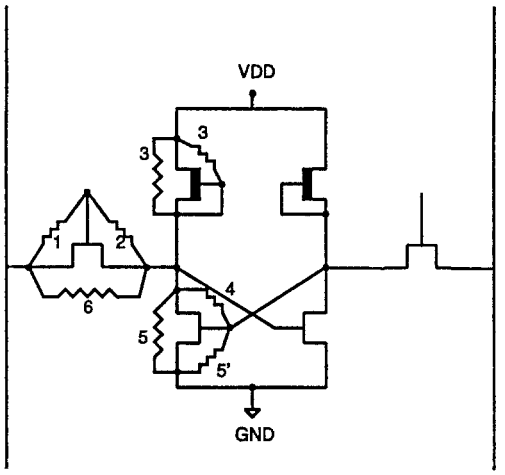


Figure 14. Canonical set of resistive paths.

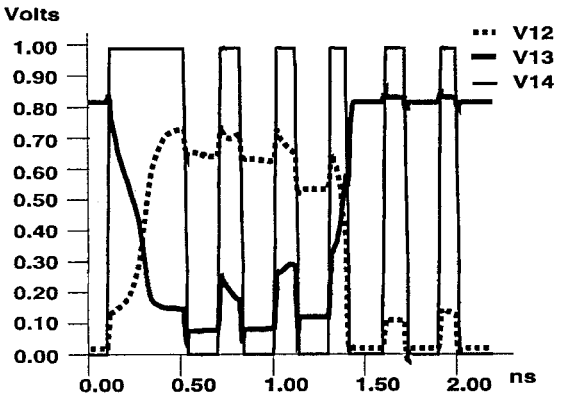


Figure 15. Simulation of cell with missing load: V12 and V13 are the cell storage nodes. The figure shows a write followed by 3 read operations the last one causing the cell to change state.

of MESFETs is well defined in MESFET circuit simulators, there are no widely accepted temperature-dependent HEMT models and the HEMT simulator [31] assumes that the operating temperature is 300 K. Hence temperature effects must be approximated by variations of other parameters such as threshold voltage, β, and so on.

2.4.2. Catastrophic Failure Modes. The process and material-related defects may produce either slow operation (delay faults) or, beyond a certain point, read and/or write errors. Sometimes these defects may lead to catastrophic circuit

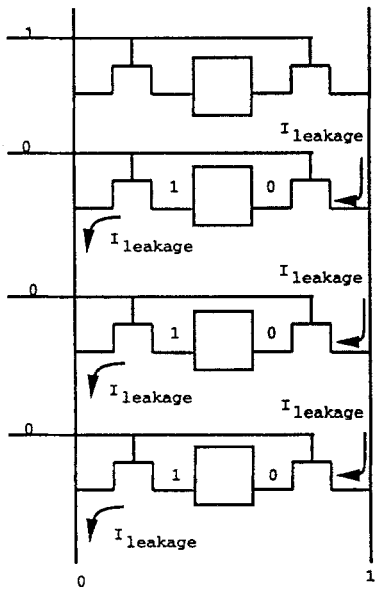


Figure 16. Parametric pattern sensitive fault due to leakage current.

modifications (faults), mostly manifested in the form of shorts and stuck-open faults. These are described in [21]. Figure 14 displays a canonical set of catastrophic resistive shorts. These may lead to the following circuit modifications:

- Resistive shorts between transistor electrodes/ increased leakage current
- Bridging of metal lines—shorts between two adjacent signals
- Stuck-open transistors

Each transistor in the circuit could thus be stuck-open, or have a resistive path between any two of its electrodes. Any two lines in the circuit that lie within some arbitrary distance from each other in the layout, could be bridged. All these aberrations considered either individually or in groups, lead to a large number of modified, 'faulty' circuits. The coupling capacitance between lines, being small when air-bridge technology is used, is neglected, and the primary coupling mechanism is due to resistive bridging.

These faulty circuits have been analyzed and simulated to obtain the equivalent functional faults. For resistive shorts the basic memory cell together with the *bit* and *word* line circuits

were simulated with a whole range of resistance values of simulate the 'short'.

2.4.3. Analysis of Resistive/Leakage Current Failure Modes. Inter-electrode resistive paths and excessive leakage currents form the most commonly observed defect in processing as well as in aging and reliability studies. Since the memory cell is symmetric with respect to the *bit* and $\overline{bit}$ lines, it is sufficient to consider resistive/leakage paths between electrodes of transistors of one half of the memory cell. Inter-electrode paths could occur between the source and the gate, or between the drain and the gate or between the source and the drain of a transistor. The following is a list of all possible paths that can occur in a single half-cell (see Figure 14). Not shown in the figure are the gate-substrate paths that connect the gate to the substrate and may be modeled as increased gate-leakage current.

- Type 1: *bit* line to *word* line
- Type 2: *word* line to cell storage node
- Type 3: cell storage node to power supply
- Type 4: cell storage node to ground
- Type 5: *bit* line to cell storage node

The operation of the memory cell in the presence of resistive path between two nodes may by analyzed using a simplified equivalent circuit similar to the circuit used to analyze normal circuit operation in the previous section.

The first table shows the results of a resistive path between the gate and source (*bit* line) nodes of the transmission gate connected to the *bit* line. The main effect of this error is to cause the *write*(0) operation to fail. The *read*(0) operation also fails because the *bit* line which is supposed to be at 0 is connected to the *word* line which goes high when enabled, causing the *bit* line voltage to increase. The second table shows the effect of the above fault on a different cell connected to the same *bit* line. The next one shows the effect of a short between the gate and source nodes of a transmission gate. This time the gate node (*word* line) is shorted to the cell directly. As a consequence, the cell follows the *word* line when the resistance is small. When the resistance is large there is

Gate-source short on transmission gate - *bit* line to *word* line

R (Ω)	Write	Read	Comments
100	Write 0 fails Write 1 delay < 100 ps	Weak 1	Write 0 fails Write/Read 1 slow
500	Write 1 delay > 100 ps Write 0 fails	Weak 1	
1000	Delay > 100 ps	Read 0 fails	
2000	Delay > 150 ps	Same as above	

Gate-source short on transmission gate: *word* line to cell

R (Ω)	Write	Read	Comments
100	Cell follows *word* line		Cell follows *word* line
500	Weak 1 - decays after 22 ps	Read 1 error	
1000	Weak 1 - decays after 60 ps	Read 1 error	
2000	Weak 1 - decays very slowly	OK OK	Data retention problem
5000	OK	OK	OK

Coupling between cells of the same *bit* line due to a *bit* line to *word* line short in one of the cells

R (Ω)	Write	Read	Comments
100	Write 1 fails	Read error	
500	Write 1 fails	Read error	
1000	OK	Read 1 error	Cell flips to 0 when read
2000	OK	Read 1 error	
5000	OK	OK	OK

Figure 17. Read and write errors caused by different failure modes.

a data retention problem. It may be noted that this problem occurs even though there is no missing pull-up which is the chief cause of data retention problems in silicon SRAMs, as we have seen before.

2.4.4. Stuck-Open Faults. A stuck-open fault on a transistor is characterized by the transistor being stuck in the cut-off region with an open circuit between the drain and the source nodes. Stuck-open faults are caused by catastrophic

failures and usually result in some major circuit malfunction. The stuck-open fault is equivalent to a missing transistor fault; it is also the limiting case of a device mismatch problem. Simulations of the memory cell with various stuck-open faults show that the behavior is equivalent to either a stuck-at fault or to a data retention problem.

2.4.5. Coupling and Pattern-Sensitive Faults. The authors have also considered the failure of multiple transistors simultaneously because of inter-electrode metallic paths. These defects cause coupling and pattern-sensitive faults that cannot be detected by the standard NPSF algorithms found in [1] and [23]. It is possible that more than one device is affected by such defects. Another problem is that of increased leakage currents in normally off devices; this problem is accentuated in HEMT memories by the fact that the ratio of the ON to the OFF currents in HEMTS is much lower than in silicon transistors. This leads to row/column pattern sensitive faults as described below.

1. **Increased Drain-Source Leakage Currents in Access Transistors:** The final result was seen by the authors to be a function of the relative strengths of the *bit*-line and *word*-line drivers and of the resistance of the path between the *bit* and *word* lines. The following behavior was observed:

   - if the *bit* line driver is stronger than the *word* line driver, cell C (where the defect occurred) could get written even when not selected;
   - if the *word*-line driver is stronger than the *bit*-line driver, all cells on the *bit*-line are stuck-at-zero;
   - if the strengths of the two drivers are comparable, the read operation is slowed down;
   - if more than one cells connected to the same *bit* line suffer a *bit*-line to *word*-line short, then depending on the resistance of each path from the *bit*-line to the *word*-lines, either all cells on the *bit*-line are stuck-at-zero, or the read operation is very slow; and
   - if this defect occurs in more than one cell connected to the same *word* line, all bits on the word-line are stuck-at-one.

   The dominant fault effect of this failure mode, considered in isolation, was the creation of multiple cell-stuck-at faults along the same *bit*-line, and the creation of delay faults for all cells on a single *bit*-line.
2. *Word* **Line to Cell-Storage-Node Short:** A single such defect could lead to data retention problems in a cell, and could also cause the cell to be stuck-at-one(0). However, it is the presence of multiple defects of this type that leads to interesting new pattern-sensitive faults.

The first case to be considered has multiple defects of type 2 in cells connected to the same *word*-line. It is assumed that the resistance of the path from a cell storage node to the *word*-line is high enough to avoid data retention and stuck-at problems for the cell. Now, if all the cells with defect 2 store a 1, there are multiple resistive paths from the *word*-line to the nodes storing a 1. The effective resistance of the path from the *word*-line to a node at logic level 1 is thereby decreased. These so-called storage nodes are actually driven by an inverter—so the effect of multiple defects of type 2 is to connect many drivers in parallel to the *word*-line. If the strength of these drivers is more than the strength of the *word*-line driver, the *word*-line is stuck-at-one. Another aspect of this problem is the fact that some cells might have a defect 2 which connects the *bit*-line to the cell storage node, while some others might have the defect in the other half of the cell, connecting the complementary storage node with the *word*-line. In that case, the *word* line fault is sensitized by a pattern of 1s and 0s such that each cell with a path between the storage node and the *word*-line stores a 1, while each cell with a path between the complementary storage node and the *word*-line stores a 0, so that the *word* line gets a maximum strength 1 drive.

2.4.6. Test Procedures for Coupling and Multiple Faults. Well-known test procedures exist for virtually every kind of functional faults in

memories. The objective of this section is to identify test procedures tha test only those faults that were described in earlier sections.

1. **Leakage Current Tests:** A sliding diagonal test is ideal to detect this type of fault. The fault is sensitized by a pattern of all 1s (0s) on the cells in the *bit*-line and testd by writing and reading 0 to one cell.
2. **Tests for Multiple *Word* Line to Storage Node Shorts:** If the cell defects were uniformly distributed between the two storage nodes, 2^n patterns would be necessary to guarantee that the fault is sensitized, where n is the number of cells on a single *word* line. An analysis of the causes of the gate-drain short reveals that this short is caused by a metallic path between the electrodes that develops as a result of stress, aging and the voltage difference between the two electrodes. Hence this defect can be made to manifest itself by continuously storing a pattern of all 1s and all 0s. This would lead to the devlopment of paths between the storage node and *word* line of every potentially defective cell. These failure mode can then be detected by simple stuck-at tests for each cell since the faults do not mask one another.
3. **Other Multiple Shorts and Their Tests:** There are three other types of shorts that can occur in a single memory cell. These are cell storage node to power supply, cell storage node to complementary cell storage node, and cell storage node to ground.

A resistive path between the cell storage node and power supply obviously causes the cell to be stuck-at-one, and a resistive path between the cell storage node and ground causes the cell to be stuck-at-zero. A resistive path between a complementary pair of storage nodes would tend to equalize their voltages and thereby prevent them from being at opposite polarities. This would cause a write operation on a cell to fail; i.e. the two node values cannot be modified by a write operation. Subsequent read operations would always give the same result regardless of what is written in the cell, assuming that the hysteresis of the sense amplifier can take care of fluctuations from its threshold voltage due to noise.

Multiple faults of the same type for storage nodes shorted to power supply or to ground do not mask one another or create new classes of pattern-sensitive faults. Hence such faults can be detected by a march test or a classical RAM test pattern such as the $30n$ pattern of Nair et al. [23].

Faults coupling different memory cells occur due to shorts between lines of adjacent cells. The effect of these faults is to cause coupling between a cell and one of its two neighbors on the same *word* line since the layout ensures that other cells are separated by power and ground lines. Hence a simple $8n$ test which reads and writes 1 and 0 on each cell in the presence of all combinations of 1 and 0 in the two adjacent cells is sufficient to cover all expected pattern-sensitive faults of this type.

3. Conclusion

The article describes the manner in which abnormal chip behavior caused by layout defects for a given SRAM cell technology can be used as a criterion for SRAM testing. Conventional functional and electrical testing have a limited defect coverage because they consider a simplified fault model based upon only the input/output interface behavior of an SRAM cell. New generations of tests try to achieve a higher defect coverage than the conventional ones by examining the cell layout and technology. These tests are performed in a variety of ways—by measuring the quiescent or steady-state power-supply current (I_{DDQ} or I_{DD}), by mapping cell layout defects into faults, or by simulating the cell array to study the fault effect of parameter variations. There are various advantages of performing such tests—they are less generic, more device-specific, and give a better idea of actual failure modes; besides, they achieve a high defect *and* fault coverage. Another important advantage of these techniques is that they can be used for *precise diagnosis* of defects—those that do cause faults and those that don't, thereby being more useful for cell repair and reconfig-

uration purposes. Conventional testing, on the other hand, employs simple and generic fault models and is thereby quite cheap. It however fails to achieve precise fault diagnosis and usually has a very limited defect coverage.

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