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Selection of Voltage Thresholds for Delay Measurement

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Abstract. Since all physical devices have a finite non-zero response time, the notion of delay between the input and output logic signals arises naturally once digital abstraction is done. This delay should be positive and non-zero, since a physical device takes a finite amount of time to respond to the input. Defining a strictly positive delay is not a problem in the abstract domain of logic signals, since input and output "events" are precisely defined. However, when the signal non-idealities are accounted for, the notion of events is blurred and it is not obvious how to define delay such that it reflects the causal relationship between the input and the output. By necessity, we define the start and end points of these events by determining the time instants when the signals cross some appropriate voltage thresholds. The selection of these voltage thresholds for logic gates as well as simple interconnect wires, is the subject of this paper. We begin by a discussion of what we mean by signal delay and how it arises in a logic gate. With this background, starting from ideal inputs to ideal inverters and concluding with physical inputs to physical inverters, we examine the problem of threshold selection for inverters through a logical sequence of model refinement, using a combination of analytical and experimental techniques. Based on the insight gained through this analysis, we examine the problem for multi-input (both static and dynamic) gates as well as point-to-point interconnect wires. We show that thresholds derived from the gate's DC voltage transfer characteristic removes the anomalies, such as negative delay and large sensitivity to input waveshape effects, that can arise with the widely used 50% and 10%–90% thresholds. Despite its fundamental nature, however, we note that the problem of threshold selection has received scant attention in the literature. To the best of our knowledge, this is the first detailed study of this problem.

Key Words: thresholds, delay, delay measurement, VTC, transition time, interconnect, causality

1. Introduction

Logic gates and the interconnect wires used for implementing a digital circuit are inherently analog devices that operate on continuous voltage and current waveforms (see Figure 1-1(a)). In order to specify and design digital systems, these continuous waveforms are abstracted as step (0-1 or logic) waveforms (Figure 1-1(b)). At the functional level, such an abstraction facilitates the use of the mathematical machinery of Boolean algebra to formally specify and design the digital system. In addition, such an abstraction establishes a temporal relationship between the inputs and output of a gate that is captured by the intuitive notion of signal **delay**. For example, the output of the inverter in Figure 1-1(b) changes at time $t_1 + \Delta$ in response to an input change at t_1 and the inverter is said to have a delay of Δ. It is important to note that such a delay is an expression of causality between two related *events* and must, thus, be strictly positive. When dealing with step inputs and outputs, there is no ambiguity in determining when the triggering event at the input and the resultant event at the output occur. Delay in such an ideal world is, accordingly, a well-defined concept.

When dealing with continuous signals it is not immediately obvious when "events" occur or how to define a meaningful delay between such signals. Appealing to the digital nature of the signals under consideration, it is reasonable to preserve the notion of events. Unlike the ideal events of step signals, however, these "real" events are non-instantaneous occurrences that span a finite time interval. This distinction between ideal and real events has several major implications:

- Whereas ideal events are unambiguously identified with the time instant corresponding to an abrupt change in signal value, identifying real events requires the selection of appropriate voltage thresholds that delimit the "significant" portion of a signal. We will refer to these thresholds as the **low** and **high thresholds** V_l and V_h and

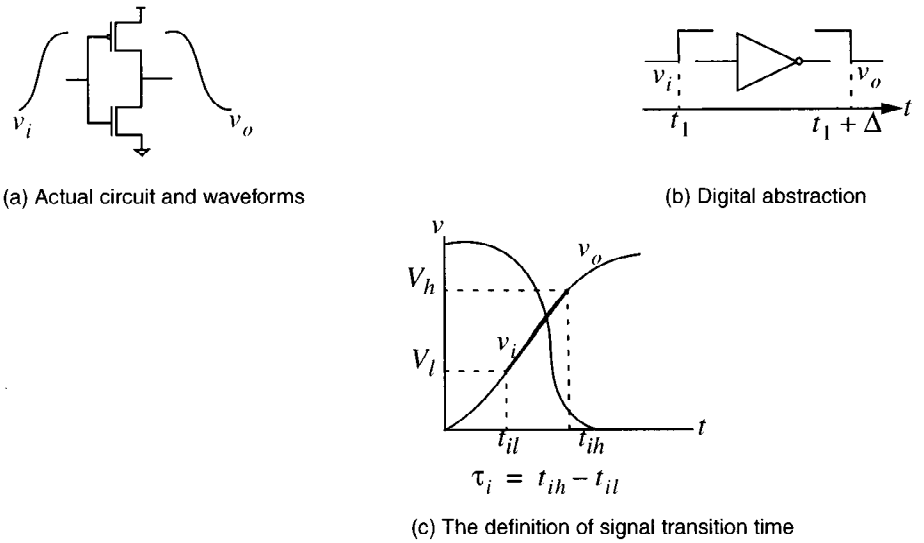


Fig. 1-1. The notion of events and signal delay.

to the voltage interval $[V_l, V_h]$ as the **transition region**.

- The finite duration of an event indicates how long it takes a signal to traverse the transition region, and will be referred to as the signal **transition** or **switching time** τ (see Figure 1-1(c)). When it is necessary to distinguish the transition direction, this duration may be labeled as the **rise** or **fall time**.
- Whereas the choice of reference times for measuring delay between two related non-instantaneous events may not be obvious, any choice of reference times will yield a delay that is a function of the input transition time τ_i. Delay functions will, thus, have the general form $\Delta = f$ (τ_i, circuit and process parameters).

Our goal in this paper is to examine how signal delay is affected by the choice of thresholds used to define it. We study this problem for single- and multi-input gates as well as for simple interconnect structures. This undertaking has both theoretical and practical importance since an improper choice of thresholds can lead to anomalies such as negative delay. For instance, the popular 50% threshold, first suggested in [7], has been shown by several researchers [1, 5, 6, 18, 20, 21] to result in negative delay. Other thresholds, such as the 10%–90%, first proposed in [14], have no theoretical justification and artificially exaggerate the effect of input waveshape on delay. Anomalies related to multi-input gates result not only from poor threshold choices but also from incorrect identification of the "dominant" input; referencing delay measurement to either the first or last changing input can be shown to violate causality.

This paper is organized in five sections as follows. In Section 2, we analyze the problem of threshold selection for inverters, starting from an ideal model of the input and the gate, gradually refining it, and ending with a simulation using physical inputs and gates. Specifically, we seek to establish guidelines for selecting thresholds that preserve the notion of causality and yield strictly positive delays under all operating conditions. Further, we also address the problem of signal transition time measurement and show how the 10%–90% threshold exaggerates the input waveshape effect on delay. In Section 3, we consider multi-input gates—both static and dynamic. The insight gained through inverter analysis is used to address the problem of threshold selection for multi-input gates. In Section 4, we examine delay measurement for point-to-point interconnects. Finally, in Section 5, we conclude the paper with a summary of the principal results.

2. Threshold Selection for Inverters

Before we delve deeper into the issue of threshold selection, it is insightful to discuss the basis for digital abstraction, since delay is a natural consequence of digital abstraction. It is the existence of circuits

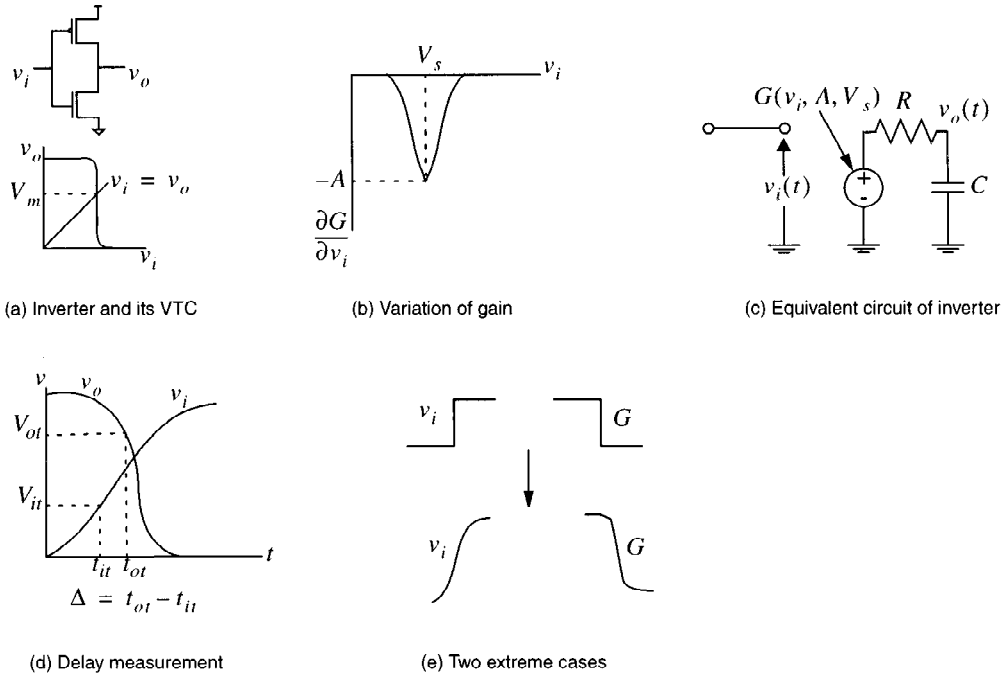


Fig. 2-1. VTC and equivalent circuit of inverter.

that amplify which makes a digital abstraction possible. While some logic functions, for area/speed advantages, can be implemented using pass gates or some other "clever" circuits that do not amplify, however, level-restoring (i.e. amplifying) circuits have to be suitably interspersed in the logic for reliable operation of the complete system. The DC input-output voltage plot, called the voltage transfer curve (or simply the VTC), of these amplifiers, such as the inverter, has the general shape of a deformed letter S (or its mirror image) as shown in Figure 2-1(a). The voltage gain of such circuits is a function of the input voltage and is plotted in Figure 2-1(b). The severe non-linearity exhibited by the inverter partitions the input voltage range into two wide regions where the magnitude of the gain of the amplifier is close to zero, separated by a narrow high gain region. In an ideal digital gate, the width of this narrow region collapses to a single voltage where the gain is infinite, and the gain is zero elsewhere. The existence of these two wide regions where the gain is zero enables us to assign logic levels to these regions and thus makes a digital abstraction possible. Referring to Figure 2-1(a) and (b), we denote the unity DC gain voltage, when $v_i = v_o$, by V_m, the magnitude of the maximum gain by A, and the voltage at which the gain is maximum by V_s. We base the selection of thresholds on the VTC of the circuit since it makes the development sufficiently general and the conclusions valid for any technology.

In order to study the dynamic behavior of the inverter, we introduce the equivalent circuit shown in Figure 2-1(c). The VTC is represented by a voltage-controlled-voltage-source (VCVS), G, parametrized by A and V_s; the resistance R models the output impedance of the inverter and C models the load capacitance as well as the non-linear transistor capacitances of the inverter. The governing differential equation for the output voltage, $v_o(t)$, of the inverter is then:

$$RC\frac{dv_o}{dt} + v_o = G(v_i(t), V_s, A) \tag{2.1}$$

A typical input stimulus and the output response of the inverter is shown in Figure 2-1(d). We denote the time instant when the input crosses the input threshold, V_{it} by t_{it} and the time instant when the output crosses the output threshold, V_{ot}, by t_{ot}. We note that V_{it} and V_{ot} are merely placeholders for actual voltage values which could lie anywhere in the inverter's voltage swing. Referring to the figure, the delay of the

inverter is given by the following template:

$$\Delta = v_o^{-1}(V_{ot}) - v_i^{-1}(V_{it}) \tag{2.2}$$

In the following subsections, we examine this behavior of delay for different choices of V_{it} and V_{ot}, by solving (2.1) for different input and VTC shapes. As shown in Figure 2-1(e), at one end of this spectrum is the ideal input interacting with an ideal gate whereas at the other end is the actual signal interacting with the actual VTC. However, as mentioned earlier, when the input is modeled as a step, there is no ambiguity about the occurrence of the input event and a positive delay can be unequivocally defined. Therefore, as a first step towards approaching realistic waveforms, we model the input by a saturated ramp. In subsection (2.1), we consider a ramp input to an ideal inverter, followed by an analysis of a ramp input to an inverter with a piecewise-linear VTC (the first step towards modeling a physical inverter) in subsection (2.2). In subsection (2.3), the piecewise-linear model of the inverter VTC is refined to a continuous non-linear VTC to mimic the physical VTC and the conclusions reached in subsection (2.2) are confirmed through numerical simulation. Finally, in subsection (2.4), we reconfirm our results using a circuit simulator, for physical signals and VTCs. In the mathematical analysis of subsections (2.1)–(2.3), we assume that all voltages are normalized to lie within $[0, 1]$ and that all times are normalized with respect to the circuit time constant RC. Further, we consider only a rising signal at the inverter input since the reasoning for a falling input is similar.

2.1. A Ramp Input to an Ideal Inverter

As a first step towards modeling an actual signal, we consider a saturated ramp given by:

$$v_i(t) = \begin{cases} \dfrac{t}{\tau_i}, 0 \le t \le \tau_i \\ 1, t > \tau_i \end{cases} \tag{2.3}$$

This signal[1] is applied to the input of an ideal inverter (see Figure 2-2(a)) whose VTC is shown in Figure 2-2(b). Note that for ideal gates we have $V_s = V_m$, and the gain, when $v_i = V_m$, is infinite as shown in Figure 2-2(c). It is easy to see that by composing the ramp input with the ideal VTC, the VCVS in the equivalent circuit, $G(v_i(t), V_m)$, is a step as shown in Figure 2-2(d). Thus, even though the input signal is not ideal, the ideal VTC serves to transform it into an ideal signal. The output response, on solving equation (2.1) with the given input and VTC waveshapes [16], is shown in Figure 2-2(e). The equation for delay (see (2.2)) in this case is given by:

$$\Delta = \tau_i(V_m - V_{it}) - \ln(V_{ot}) \tag{2.4}$$

Referring to Figure 2-2(e), intuitively, an ideal gate implies a choice of $V_{it} = V_m$, since it is only when the input voltage reaches V_m that it causes an output change to occur. With this choice of V_{it}, from (2.4) it is clear that delay is positive for any choice of V_{ot} such that it lies within $[0, 1]$; only the magnitude of delay would vary depending on the choice of V_{ot}. It is also evident that the delay is independent of τ_i. For $V_{it} < V_m$, delay is still positive and monotonically increasing with τ_i; however, we reject this choice since it overestimates delay by incorrectly accounting for causality (since there is no change in the output when $V_{it} < V_m$) and also produces an artificial increase in delay with input slope. Similarly, we reject a choice of $V_{it} > V_m$ since it underestimates delay and could result in negative delay for slow inputs. The behavior of delay for these different choices of thresholds is shown in Figure 2-2(f).

Thus, in summary, the choice of delay thresholds for ideal gates, even when excited by non-ideal inputs, is unambiguous with $V_{it} = V_m$ and $V_{ot} \in [0, 1]$. With this choice of delay thresholds, delay is also independent of the input transition time. However, this does not lead to a consistent choice of delay thresholds. To see why, consider another ideal inverter connected to the output of the inverter under consideration, as shown in Figure 2-2(g). This inverter has a falling transition at its input and going through a similar analysis, we find that we need $V_{it} = V_m$. Therefore, in order to define delay meaningfully for the combination, we need to choose $V_{ot} = V_m$. Thus, for ideal gates we are left with only one reasonable choice of thresholds: $V_{it} = V_m$ and $V_{ot} = V_m$.

2.2. A Ramp Input to an Inverter with Piecewise-Linear VTC

Next we consider a ramp input to an inverter with a piecewise-linear VTC as shown in Figure 2-3(a). The VTC is given by the following set of equations and is

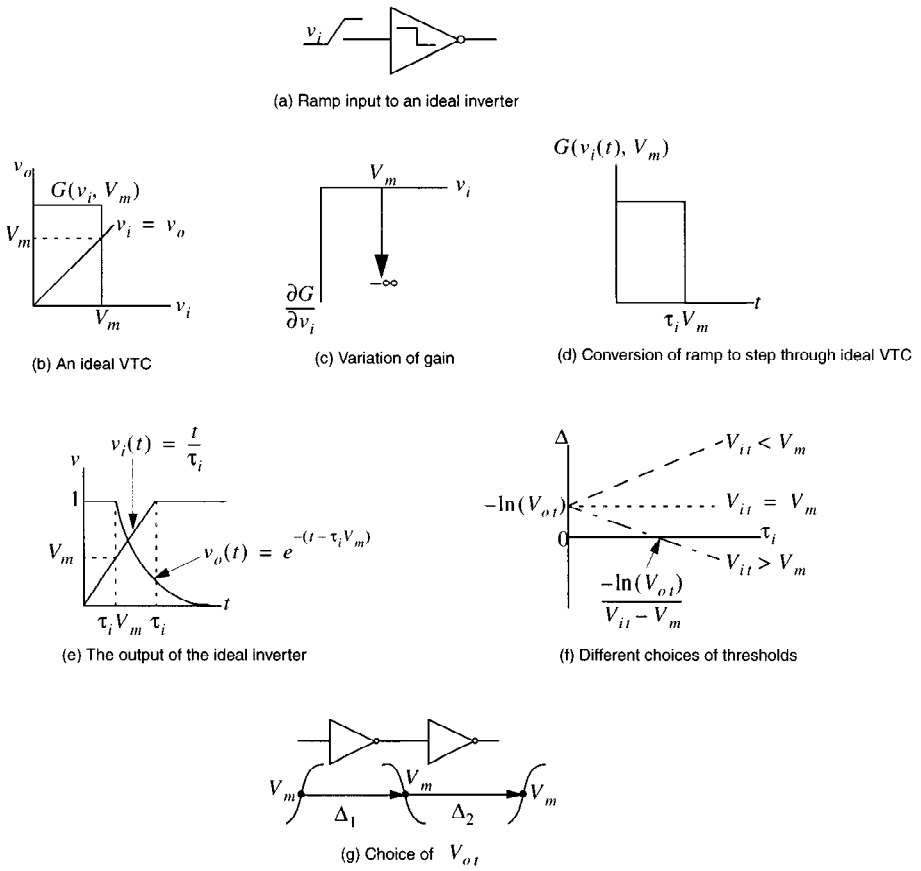


Fig. 2-2. A ramp input to an ideal inverter.

shown in Figure 2-3(b):

$$G(v_i, A, V_s) = \begin{cases} 1, v_i < V_{il} \\ \left(\dfrac{(V_{ih}-v_i)}{V_{ih}-V_{il}} = A(V_{ih}-v_i)\right), V_{il} \le v_i \le V_{ih} \\ 0, v_i > V_{ih} \end{cases} \quad (2.5)$$

Thus, the VTC has a finite but constant gain $A > 1$ between V_{il} and V_{ih} and 0 gain elsewhere, as shown in Figure 2-3(c). It is interesting to note that V_s is not uniquely defined and can be any value between V_{il} and V_{ih}. Unlike the ideal VTC, on composing the ramp input with the piecewise-linear VTC, we are still left with a ramp signal for the VCVS (see Figure 2-3(d)) in the equivalent circuit. Therefore, it is not immediately obvious what choice of delay thresholds would result in a causal definition of delay. The resulting output waveform obtained by solving (2.1) with the given input and VTC parameters is shown in Figure 2-3(e) and consists of two distinct parts.

As a first step towards the selection of thresholds for non-ideal gates, we continue with choices made for ideal gates ($V_{it} = V_m$ and $V_{ot} = V_m$) and investigate the behavior of delay. However, since the output response is composed of two different waveshapes, it is not possible to write an explicit equation for delay. Instead, we break the analysis into two parts: the behavior of delay as $\tau_i \to 0$ (fast inputs) and as $\tau_i \to \infty$ (slow inputs).

Fast inputs: For small values of τ_i, V_B is close to 1 and can be approximated as:

$$V_B = 1 - \frac{\tau_i}{2A} \quad (2.6)$$

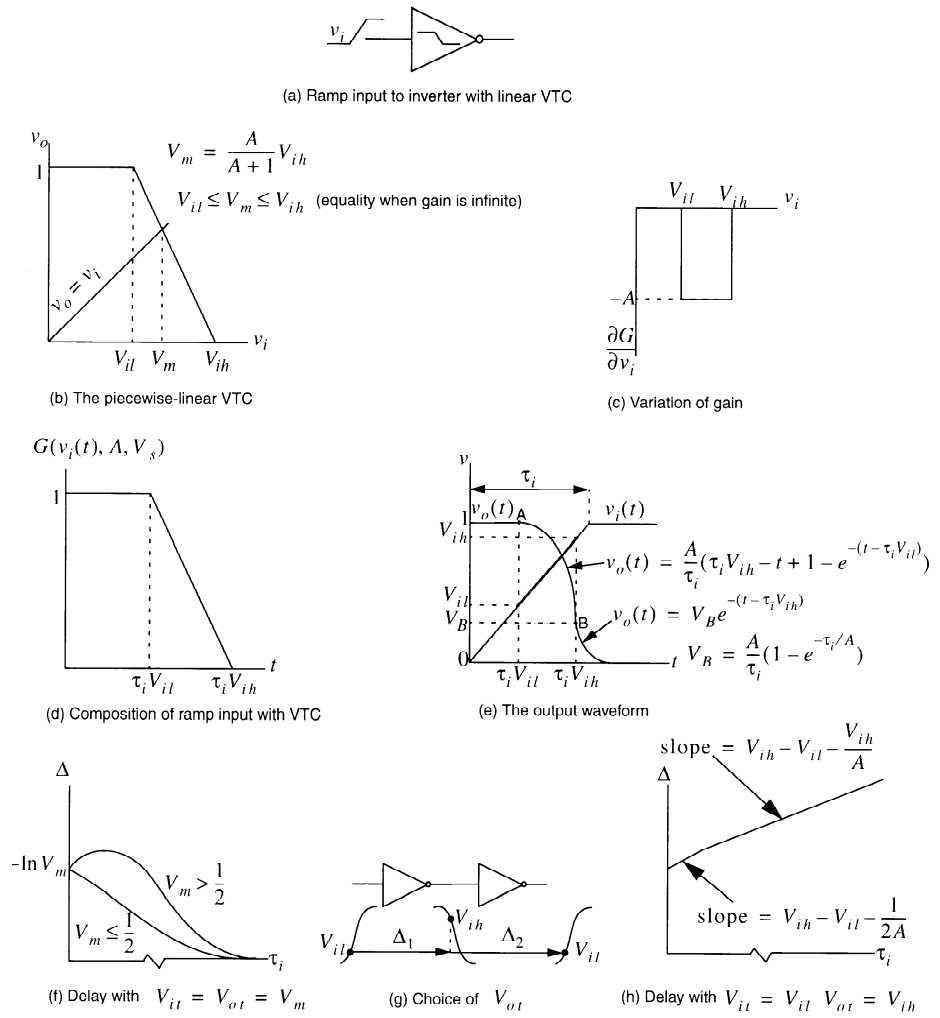


Fig. 2-3. Ramp input to an inverter with piecewise-linear VTC.

and assuming $V_B \geq V_m$, the output voltage is given by:

$$v_o(t) = \left(1 - \frac{\tau_i}{2A}\right) e^{-(t-\tau_i V_{ih})} \tag{2.7}$$

and the delay is given by:

$$\Delta = \tau_i V_{ih} - \ln\left(\frac{V_{ot}}{1 - \frac{\tau_i}{2A}}\right) - \tau_i V_{it} \tag{2.8}$$

It is obvious from this equation that the delay is positive for a step input and is given by $-\ln V_{ot}$ (which confirms our observation with ideal gates and ideal inputs; see Figure 2-2(f)). In order to see its behavior with increasing τ_i, we differentiate (2.8) to get:

$$\frac{d\Delta}{d\tau_i} = V_{ih} - V_{it} - \frac{1/(2A)}{1 - \tau_i/(2A)} \tag{2.9}$$

It follows therefore for $\left.\frac{d\Delta}{d\tau_i}\right|_{\tau_i=0} > 0$ we must satisfy:

$$V_{it} < V_m + \frac{(2V_m - 1)}{2A} \tag{2.10}$$

where V_{ih} has been expressed in terms of V_m (see the relation in Figure 2-3(b)). Substituting $V_{it} = V_m$ in the above inequality we find that delay increases with increasing input transition time if $V_m > 0.5$ and decreases otherwise. It is also clear that the choice of

output threshold does not affect the monotonicity of delay; it only affects the value of delay for step inputs.

Slow inputs: For large values of τ_i, V_B is close to 0 and assuming $V_B \leq V_m$, the output voltage is given by:

$$v_o(t) = \frac{A}{\tau_i}(\tau_i V_{ih} - t + 1 - e^{-(t-\tau_i V_{il})}) \quad (2.11)$$

At the instant t_{ot}, the output voltage V_{ot} is given by:

$$\begin{aligned} V_{ot} &= AV_{ih} - A\frac{t_{ot}}{\tau_i} + \frac{A}{\tau_i} - \frac{A}{\tau_i e^{(t_{ot}-\tau_i V_{il})}} \\ &\cong A\left(V_{ih} - \frac{t_{ot}}{\tau_i}\right) \end{aligned} \quad (2.12)$$

Solving for delay, we have:

$$\Delta = \tau_i \left[(V_m - V_{it}) + \frac{1}{A}(V_m - V_{ot}) \right] \quad (2.13)$$

where again V_{ih} has been expressed in terms of V_m. For a choice of $V_{it} = V_{ot} = V_m$, we find that the delay asymptotes to zero as τ_i tends to infinity.

We can summarize the discussion for this choice of thresholds in Figure 2-3(f), where the behavior for both fast and slow inputs is shown. It is not surprising that this choice of delay thresholds leads to an anomalous behavior of delay. Referring to Figure 2-3(e), observe that the output has already started to change by the time the input reaches V_m. Relating this to our discussion in the Introduction, we are incorrectly assuming the start of input event at the instant the input crosses V_m and thus underestimate delay which results in a zero value of delay for slow inputs.

From (2.13), it is obvious that delay will be positive and increasing with τ_i for slow inputs when $V_{it} < V_m$ and $V_{ot} = V_m$. While we could choose any V_{it} such that it is less than V_m, we find that a choice of $V_{it} = V_{il}$ supports the notion of causality. Again referring to Figure 2-3(e), we find that it is only when the input crosses V_{il} that the output starts to change. By substituting this choice in (2.10), we find that the delay is indeed positive and an increasing function of τ_i for fast inputs as well. Thus, a choice of $V_{it} = V_{il}$ and $V_{ot} = V_m$ appears to be satisfactory, as long as we are considering a single inverter. However, for a combination of two inverters, as shown in Figure 2-3(g), for a choice of $V_{it} = V_{il}$ the only consistent way to define delay is to choose $V_{ot} = V_{ih}$. A quick glance at (2.10) and (2.13), shows that delay is always positive and a monotonically increasing function of τ_i as shown in Figure 2-3(h).

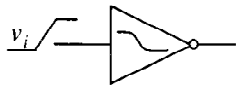
Thus, while a single threshold such that $V_{it} = V_{ot} = V_m$ suffices for ideal gates, we need two thresholds, $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$ when we consider non-ideal gates. However, a single threshold choice of $V_{it} = V_{ot} = V_m$ has been made by some authors ([5, 13, 18, 20]), even for non-ideal gates, which as we saw leads to a non-monotonic behavior of delay with respect to input transition time. This analysis also implies that the *temporally* relevant part of the input waveform is when $V_{il} \leq v_i \leq V_{ih}$, which is shown in bold in Figure 2-3(e). It is therefore reasonable to use $V_l = V_{il}$ and $V_h = V_{ih}$ for measuring the signal transition time.

2.3. A Ramp Input to an Inverter with a Continuous Non-linear VTC

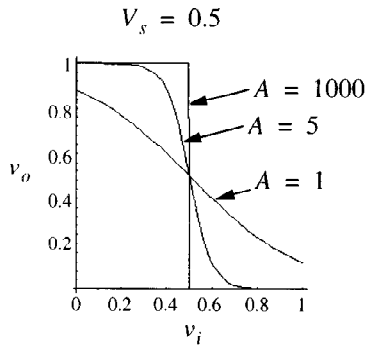
We next consider the ramp input applied to an inverter with a non-linear continuous VTC as shown in Figure 2-4(a). While the preceding analysis with a piecewise-linear VTC provided valuable insight into the choice of delay thresholds, the VTC of a real gate has a smooth shape. In order to mimic the wide variety of VTC shapes in real circuits, we find it convenient to modify equation (2.5) as follows:

$$G(v_i, V_s, A) = \frac{1}{2}\{1 + \tanh[2A(V_s - v_i)]\} \quad (2.14)$$

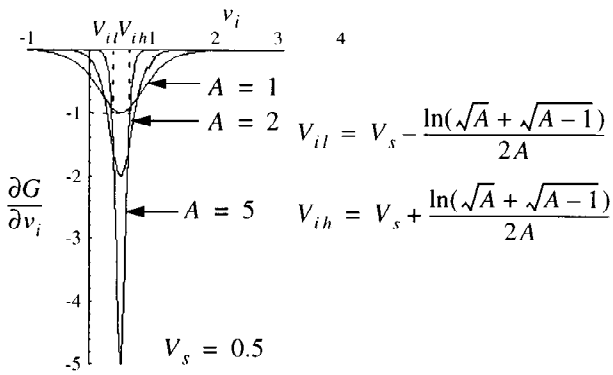
This function is graphed for different values of A in Figure 2-4(b). The variation of gain with v_i is plotted in Figure 2-4(c). The gain is no longer constant and varies with the input voltage. The magnitude of gain is equal to 1 when $v_i = V_{il}$, reaches a maximum of A when $v_i = V_s$, and decreases again reaching a value of 1 when $v_i = V_{ih}$. Therefore, V_{il} and V_{ih} are referred to as the unity differential gain voltages [9]. It is interesting to note the behavior of V_m with V_s in Figure 2-4(d). We note that $V_m = V_s$ only for symmetric VTCs when $V_s = 0.5$; for others V_m is slightly less or greater than V_s. We also observe that though the discontinuities in the curves have disappeared, the essential features of the continuous VTC are the same as the piecewise-linear one. Therefore, we expect the conclusions reached in the preceding subsection to remain valid. In the remainder of this subsection, we restrict ourselves to symmetric VTCs since it avoids the use of V_s in the discussion, keeping it along the same lines



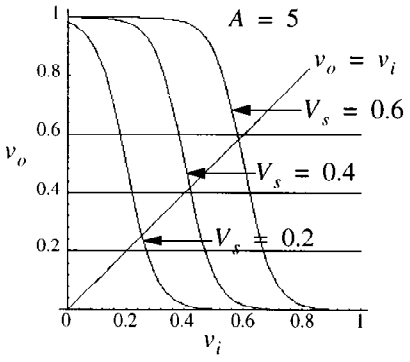
(a) Ramp input to inverter with non-linear continuous VTC



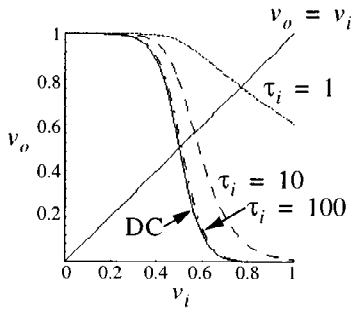
(b) VTC of an inverter for different A



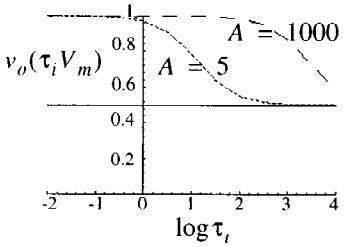
(c) Variation of gain



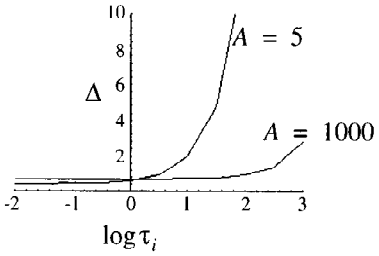
(d) VTC of inverter for different V_s



(e) The transient VTC



(f) The output voltage at $\tau_i V_m$



(g) Delay measured with $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$

Fig. 2-4. Ramp input to an inverter with continuous non-linear VTC.

as before. Note that all the conclusions reached with this assumption remain valid for asymmetric VTCs as well.

Since, we cannot solve (2.1) analytically for the output voltage, we use numerical simulation using *Mathematica* [22] to confirm the results of the previous sub-

section. We first show that a choice of $V_{it} = V_{ot} = V_m$ leads to zero delay as $\tau_i \to \infty$. Since numerical methods have difficulties in determining the asymptotic behavior, we resort to an indirect technique by introducing the notion of a transient VTC[2] in Figure 2-4(e). A transient VTC is obtained by numerically solving for $v_o(t)$ using (2.1) for a given τ_i and plotting it versus $v_i(t)$ for different instants of time, t. It is clear from the figure that a transient VTC approaches the DC VTC as $\tau_i \to \infty$. Therefore, this implies that the output voltage crosses V_m at the same instant as the input does, resulting in zero delay. This is confirmed again in Figure 2-4(f) where we plot the output voltage at the instant the input crosses V_m, versus τ_i, for two different gains. Note that the output voltage at this instant approaches V_m for large τ_i. However, also note that when the gain of the inverter is large, the delay approaches zero slower and in the limit $A \to \infty$, the delay would be a constant positive value, independent of τ_i, confirming our analysis in subsection 2.1 for ideal gates.

However, when we choose $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$, we expect the delay to remain positive. This is because as the transient VTC approaches the DC VTC for slow inputs, the output voltage at the instant the input crosses V_{il} will approach $G(V_{il})$. It is easy to see from the equations for V_{il} and V_{ih} in Figure 2-4(c) that $V_{ih} < G(V_{il})$. In Figure 2-4(g), we show that this choice of delay thresholds never results in negative delay and that the delay is a monotonically increasing function of τ_i. Again, note the relative insensitivity of delay to τ_i when the gain of the inverter is large.

Thus, by a series of steps, starting from an ideal input to an ideal gate and concluding with a ramp input to an inverter whose VTC resembles the actual VTCs of real circuits, we have rigorously analyzed the problem of a proper choice of delay thresholds. From this analysis, it is clear that a choice of $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$ ensures that the delay is always defined such that causality is maintained. This analysis corroborates the same choices made by other researchers [15] without a formal justification. We now confirm the results of this analysis with a physical waveform applied to a physical inverter, in the next subsection.

2.4. Physical Input to a Physical Inverter

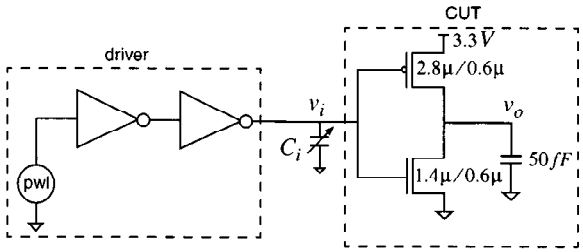
While the analysis so far was based on abstract mathematical models for the inverter and the input, we need to perform experiments using physical inverters and realistic waveforms (see Figure 2-5(a)) in order to conclusively establish the results of the preceding subsections. Consider the experimental setup shown in Figure 2-5(b). In order to excite the circuit-under-test (CUT) by the *characteristic waveform* [3], we drive the CUT by two inverter stages, input to which is a rising ramp. The important thresholds of the CUT in Figure 2-5(b) are shown in the table in Figure 2-5(c), obtained through a DC simulation of the inverter. All simulations described in this subsection (and elsewhere in the paper) were performed using HSPICE [17] with the HP 0.6μm CMOS technology [12] available through MOSIS. Unless stated otherwise, τ_i of the input to the CUT is measured using $V_l = V_{il}$ and $V_h = V_{ih}$ and is changed by varying the capacitance at the input to the CUT.

We begin by showing the inappropriateness of using $V_{it} = V_{ot} = V_m$ as the delay threshold for non-ideal gates and compare it with a choice of $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$. Next, we compare the transition time measurement using the 10%–90% thresholds versus the $V_{il} - V_{ih}$ thresholds.

2.4.1. Delay measurement with $V_{it} = V_{ot} = V_m$ versus $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$. First consider the behavior of delay with $V_{it} = V_{ot} = V_m$. We show the inappropriateness of this choice on two counts: 1) delay going to zero as the input becomes slow, and 2) extreme sensitivity of delay to small variations in the value of V_m. However, since we cannot show the asymptotic behavior of delay as $\tau_i \to \infty$ using circuit simulation, as before we resort to an indirect technique using the transient VTC. The transient VTC for the inverter is shown in Figure 2-5(d). It is obtained by plotting the output voltage versus the input voltage, at various instants of the simulation time. Since the transient VTC asymptotes to the DC VTC for slow inputs, we expect the output to cross V_m at the same instant as the input, resulting in zero delay. This is corroborated further in Figure 2-5(e) where we show the output voltage at the instant the input crosses V_m. As shown in the figure, the output voltage at this instant asymptotes to V_m as the input becomes slower.

Next we show the sensitivity of delay to variations in the value of V_m in Figure 2-5(f). If the value of V_m is incorrectly determined as 1.55V, delay is positive and increasing with τ_i; however, if V_m is incorrectly determined as 1.57V, the delay starts to decrease after a certain point and will eventually become negative. This

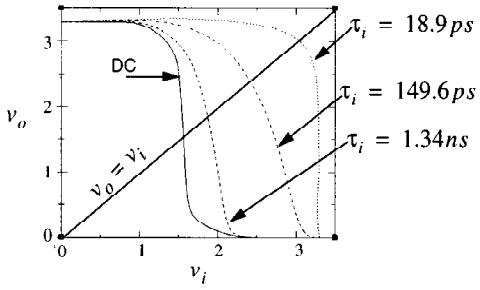
(a) Actual input to a physical inverter



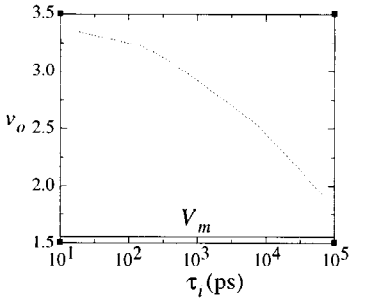
(b) Experimental setup

V_{il}	V_m	V_{ih}
1.250V	1.561V	1.746V

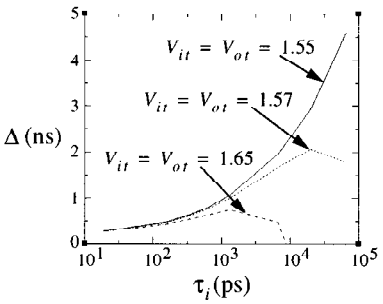
(c) Thresholds of the inverter



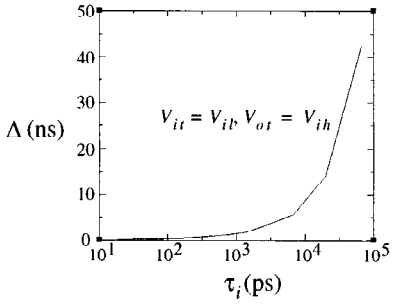
(d) Transient VTC



(e) v_o at instant when $v_i = V_m$



(f) Anomalous behavior of delay



(g) Correct behavior of delay

Fig. 2-5. A physical input to a physical inverter.

result is not surprising if we refer to equation (2.13). It is clear that for $V_{it} > V_m$, $V_{ot} > V_m$, the delay becomes negative and for $V_{it} < V_m$, $V_{ot} < V_m$ the delay remains positive.

We also show the behavior of delay when measured using the popular 50% threshold (which in this case is 1.65V) in Figure 2-5(f). Since for this inverter, the 50% threshold is greater than V_m, this is indeed expected (see (2.13)). In a symmetric inverter, the 50% threshold would equal V_m and its behavior would be similar to the one shown in Figure 2-5(d) and (e). However, when the inverter is designed such that V_m is greater than the 50% threshold, this choice works fine since as predicted by (2.13), the delay remains positive.

The behavior of delay with $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$ is shown in Figure 2-5(g). As predicted by the analysis in the preceding subsections, the delay is always positive and is a monotonically increasing function of τ_i. Unlike the case of V_m, small variations in measuring the value of V_{il} and V_{ih} will not alter the behavior of delay. Even if the V_{il} and V_{ih} values are off a little bit, V_{it} will still be sufficiently smaller than V_m, and since the gain in any practical inverter is large, from equation (2.13) we can see that the delay will still be positive and increasing. Thus, the experimental results confirm our conclusion that $V_{it} = V_{il}$ and $V_{ot} = V_{ih}$ are the appropriate choices for measuring delay. Next we examine the behavior of signal transition time for two different choices of thresholds for measuring it.

2.4.2. Transition time measurement using the 10%–90% thresholds versus the $V_{il} - V_{ih}$ thresholds. If the thresholds for measuring transition time capture the temporally relevant portion of the input, then for a given input transition time, delay of the gate should depend only minimally on the specific input waveshape. We now describe an experiment we performed which shows that this is indeed the case if transition time measurement is done using $V_l = V_{il}$ and $V_h = V_{ih}$ rather than the usual 10%–90% thresholds. The experimental setup used in our experiment is shown in Figure 2-6(a). We first measured the delay through the CUT with the characteristic waveform as the input. We then approximated the characteristic waveform at the input to the CUT by two different waveshapes in turn: the ramp and the exponential, and compared the new delay to the delay due to the characteristic waveform that was obtained earlier (see Figure 2-6(b)). The delay in each case was measured using the $V_{il} - V_{ih}$ thresholds of the inverter. The approximation was done such that the ramp and the exponential had the same transition times as the characteristic waveform they replaced, for two different choices of transition time thresholds: $V_{il} - V_{ih}$, and 10%–90%. This experiment was then repeated a large number of times by randomly varying the parameters of the experimental setup (the range of parameters is shown in Figure 2-6(a)). The percentage error in the delay due to the waveform approximation relative to the delay due to the characteristic waveform is shown in Figure 2-6(c) for the exponential and in Figure 2-6(d) for the ramp waveshapes. The relative errors are plotted as a function of the input transition time normalized to the characteristic waveform delay.

It is clear from the scatter plots that delay is less sensitive to the input waveshape when the input transition time is measured using the $V_{il} - V_{ih}$ thresholds rather than the 10%–90% threshold. It is also interesting to note that in most cases, when the input transition time is measured using the $V_{il} - V_{ih}$ thresholds, the exponential waveshape over estimates the true delay whereas a ramp input underestimates it.

This completes our study of the problem of selecting voltage thresholds for measuring delay and transition time for a single input gate. Summarizing, we find that delay measured using the unity differential gain voltages of the gate is always positive and is a monotonically increasing function of the input transition time. Further, input transition time measured using the same thresholds results in delay that is less sensitive to the input waveshape than the conventional 10%–90% thresholds. We now use the insights gained from this analysis to examine the problem of threshold selection for multi-input gates in the next section.

3. Threshold Selection for Multi-Input Gates

3.1. Static Gates

Simple Gates: The situation is more complicated in a multi-input gate when many inputs switch in close temporal proximity with different transition times (see Figure 3-1(a)). Here the problem is two-fold: not only do we have to identify the voltage thresholds for measuring delay but we also need to identify the correct reference input for delay measurement. In this paper we address only the problem of choosing the correct voltage thresholds; the latter problem is tackled in [4]. As with inverters, delay measured using these thresholds must satisfy causality and must therefore yield a positive value of delay for *all* possible combinations of input transition times and the temporal separations between the inputs. Since the VTC played a critical part in the analysis of the inverter, we once again start with the VTC of the multi-input gate. We illustrate our approach with the three-input NAND gate shown in Figure 3-1(b).

Rather than a single VTC as in the case of an inverter, an n-input gate can have $2^n - 1$ VTCs corresponding to all possible combinations of stable and switching inputs. Figure 3-1(c) shows the VTCs of the NAND gate, obtained by circuit simulation. The V_{il}, V_{ih} and V_m of each VTC are listed in Figure 3-1(d). The VTC for the case when a is switched alone and the VTC

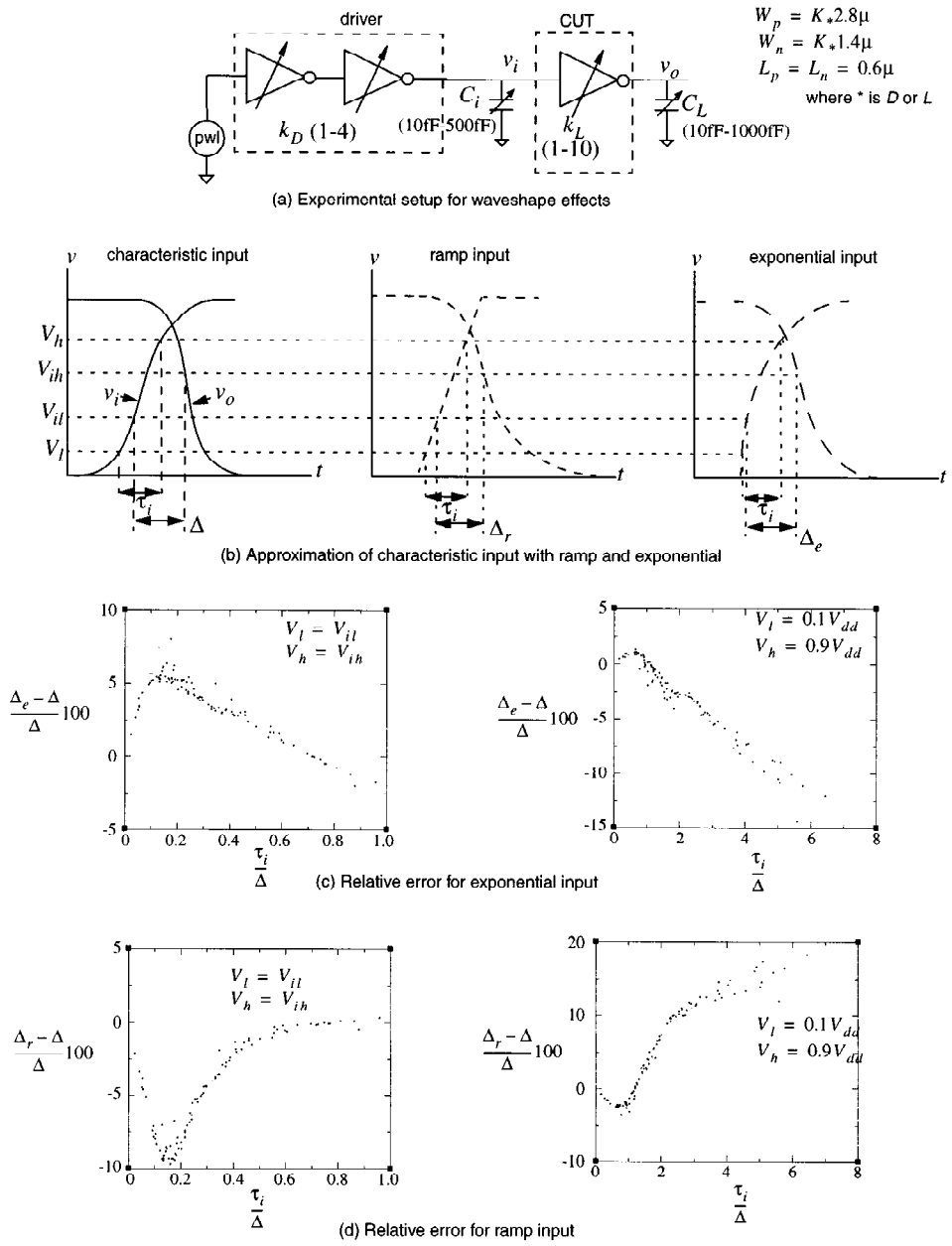
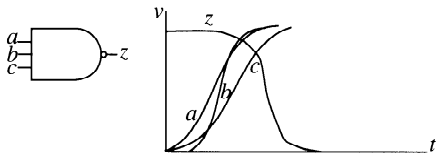
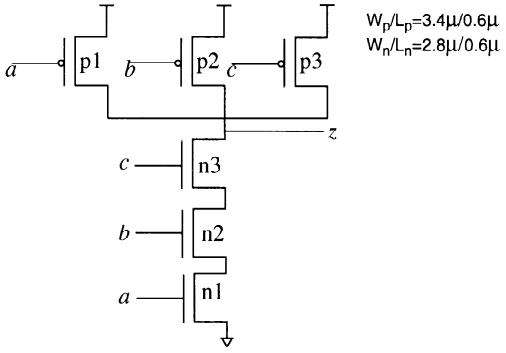


Fig. 2-6. Input waveshape effect on delay for different transition time thresholds.

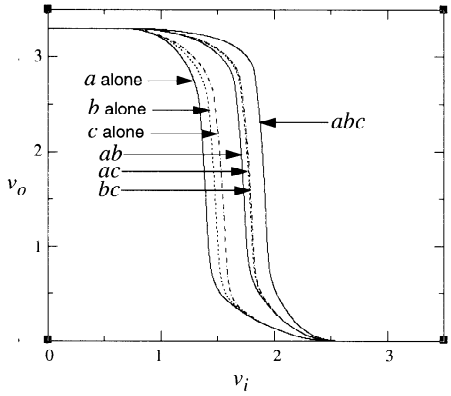
for the case when all of them switch together, are the two extreme cases of this family of curves. Consider the following scenario which illustrates the problem of threshold selection for multi-input gates. Suppose that the three inputs to the gate rise together with the same transition time. Based on our discussion for inverters, it is natural to measure delay using the $V_{il} - V_{ih}$ thresholds obtained from the right most VTC (i.e. *a*, *b*, and *c* tied together) in Figure 3-1(c). Now, consider a different situation; suppose inputs *b* and *c* switch together but input *a* rises *after b* and *c* have finished their transitions. Since the last arriving input *a* causes the output to change, we must measure delay using the $V_{il} - V_{ih}$ thresholds obtained from the left most



(a) Near-simultaneous switching in a multi-input gate



(b) Three-input NAND gate



(c) VTCs of the NAND gate

input	V_{il} (V)	V_m (V)	V_{ih} (V)
a	1.065	1.401	1.585
b	1.161	1.481	1.665
c	1.239	1.545	1.718
a, b	1.482	1.723	2.078
a, c	1.542	1.772	2.085
b, c	1.555	1.78	2.093
a, b, c	1.723	1.9	2.242

(d) Various thresholds for the NAND gate

Fig. 3-1. Threshold selection for a 3-input NAND gate.

VTC (i.e. when a switches alone). Note how we have to move from the thresholds of one VTC to the other VTC depending on the temporal separation of the inputs. It is not clear at what temporal separation of input a from inputs b and c to make the transition from the right most VTC to the left most VTC in Figure 3-1(c). Instead, if we had continued to use the $V_{il} - V_{ih}$ thresholds from the right-most VTC, then we can get negative delays when there is a large temporal separation between input a and inputs b and c (and input a is slow rising). This is so because V_{il} obtained from the VTC corresponding to the three inputs tied together, is greater than the V_m obtained from the VTC corresponding to a switching alone, and as we saw in the

inverter analysis (see (2.13)), this condition can yield negative delays.

To ensure that negative delays never arise and to avoid moving from one VTC to another depending on the separation of inputs, we base our delay measurement on the minimum V_{il} and the maximum V_{ih} from all the VTCs. This will guarantee that $V_{il} < V_m < V_{ih}$ for V_m corresponding to any VTC and will therefore ensure positive delay, for any combination of input transition times and their temporal separations. In general, the lowest V_{il} would be from the VTC obtained by tying the inputs connected to the gates of the n-transistors closest to the ground rail. This is because the source of the transistors is at zero potential whereas the sources of other transistors higher in the series stack will have non-zero source voltage. Consequently a higher gate voltage[3] is required to turn on the transistors higher in the stack resulting in a higher value of V_{il}. Similarly, the highest value of V_{ih} would be from the VTC obtained by tying the inputs connected to the gates of the p-transistors closest to the power rail. Therefore, in case of a NAND gate, the V_{il} chosen would be from the input closest to the ground and V_{ih} would be from the VTC corresponding to all inputs being tied together. In case of NOR gates, the situation is complementary, with V_{il} being chosen from the VTC corresponding to all inputs tied together and V_{ih} being chosen from the input closest to the power rail. The $V_{il} - V_{ih}$ thresholds used for delay and transition time measurement for the example NAND gate are shown shaded in Figure 3-1(d).

Complex Gates: Similar arguments hold in the case of complex gates (see Figure 3-2). While in case of simple gates it was easy to determine what combination of stable and switching inputs during the DC analysis would yield the minimum and maximum thresholds, in case of complex gates, this choice is topology dependent. The guiding principle is still the same: find the input combination that causes the output to fall at the earliest (for minimum V_{il}) and the combination that causes the output to rise at the earliest (for maximum V_{ih}). For example, in the gate shown in Figure 3-2, the minimum V_{il} is determined by switching x_1 and x_2 together and setting x_3 and x_4 to 1. Similarly, for the maximum V_{ih} is determined by switching x_1 and x_4 together and setting x_3 and x_4 to 0. This was further confirmed by a DC simulation of this gate.

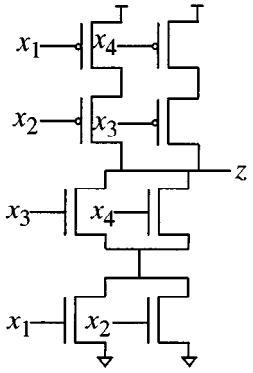


Fig. 3-2. Choosing thresholds for complex gates.

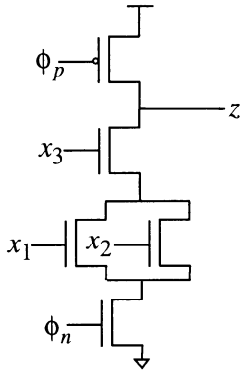


Fig. 3-3. Choosing the thresholds for a dynamic gate.

Dynamic Gates: In case of dynamic gates, there is just one pull-up transistor for the entire pulldown network (see Figure 3-3) and the inputs ϕ_p and ϕ_n are typically connected to the clock signal of the system. Therefore, we examine the topology of only the pulldown network to determine what inputs need to be switching and what inputs need to be stable high or low during the DC analysis to give the minimum V_{il} and the maximum V_{ih}. We then *electrically* connect ϕ_p to the input(s) in the pulldown network that are switching to get a valid VTC from which the thresholds can be found. For example, for the dynamic gate in Figure 3-3, we find through a DC simulation, that the minimum V_{il} is found from the VTC corresponding to inputs x_1, x_2 and ϕ_p switching together (with x_3 and ϕ_n stable high) and the maximum V_{ih} is found from the VTC corresponding to x_1, x_2, x_3, ϕ_n and ϕ_p switching together.

This then completes our discussion of threshold selection for multi-input gates. To summarize, we find

that unlike the inverter, we have not one but a family of VTCs for a multi-input gate. We therefore select the minimum and maximum of all possible V_{il} and V_{ih} values respectively, as the thresholds for delay and transition time measurement. Based on the insight gained from the detailed study of inverters, we conclude that this choice always yields a positive value of delay for all input transition times and their temporal separations.

We note in passing that in a standard cell library based environment, there would be a wide variety of gates. For each gate in the library, we determine the V_{il} and V_{ih} value using the ideas embodied in this paper. We then select the minimum of all the V_{il} values and the maximum of all the V_{ih} values to be the delay and transition time thresholds for the entire system.

This concludes our analysis for logic gates. We next examine the problem of delay measurement for interconnect wires, since with the advent of deep submicron technologies, the temporal modeling of interconnect wires (or simply interconnects) is becoming a major concern.

4. Threshold Selection for Interconnects

In this paper, we shall confine the discussion to only point-to-point interconnect, such as shown in Figure 4-1(a). Unlike logic gates, interconnects are linear, passive (non-amplifying) circuits. Therefore, their VTC is a straight line with slope equal to 1, as shown in Figure 4-1(b).[4] For delay measurement, as in gates, once again we seek thresholds from the VTC to signify the beginning and end of events. However, we note that there are no clear-cut voltages which can demarcate events, since the interconnect VTC has a constant gain over the entire range of the input voltage (see Figure 4-1(c)). Moreover, referring to Figure 4-1(b), intuitively, it appears that the delay would approach zero as input transition time tends to infinity, for any choice of thresholds such that $V_{it} = V_{ot}$, and that delay would never be negative (since interconnects are non-amplifying). However, since interconnects are not isolated circuits and are driven by buffer drivers having a well defined VTC, we use the unity differential gain thresholds (i.e. $V_{il} - V_{ih}$ thresholds) of the driver for measuring delay and transition time thresholds. As shown in Figure 4-1(d), this leads to a consistent definition of delay for a combination of gate and interconnect.

In the following two subsections, we first investigate the behavior of delay with this choice of input thresholds for RC interconnects and then examine the problem for RLC interconnects.

4.1. RC Interconnect

For on chip wires, the inductive effects can be ignored and the interconnect can be treated as a distributed RC network. In the following discussion, for simplicity, we consider only uniform distributed RC interconnect and approximate it by a lumped RC ladder circuit (see Figure 4-2(a)). In the figure, r and c are the per-unit-length resistance and capacitance, l is the length of the interconnect and n refers to the number of lumped segments. While n should be sufficiently large for accuracy, for digital applications $n = 5$ suffices in most cases [10].

We consider a saturated ramp input to the n-segment ladder network. It is well known that the poles of the transfer function of an RC-ladder are all distinct and lie on the negative real axis in the complex frequency domain [8]. Therefore, the impulse response of the ladder network in time domain can be written as follows:

$$h(t) = \sum_{j=1}^{n} k_j e^{-|p_j|t} \tag{4.1}$$

where p_j is the j^{th} pole and k_j is the corresponding residue.[5] Since under DC conditions the output voltage equals the input voltage, we have the following relation between the poles and the residues:

$$\sum_{j=1}^{n} \frac{k_j}{|p_j|} = 1 \tag{4.2}$$

The output response of an RC ladder is known to be monotonic [11] and is obtained by convolving the impulse response given by (4.1) with the ramp input. As shown in Figure 4-2(b), the output response has two parts and the crossover voltage is denoted by V_C. Since it was slow inputs that caused an anomalous behavior of delay in case of logic gates, we begin by examining the behavior of delay for a slow rising ramp input to an RC-ladder.

Slow inputs: We show that the delay approaches zero for any choice of threshold voltage such that $V_{it} = V_{ot}$ as $\tau_i \to \infty$. It can be easily seen from the equation for V_C in Figure 4-2(b) that the cross-over voltage V_C is close to V_{dd} in this case. Therefore we assume that the

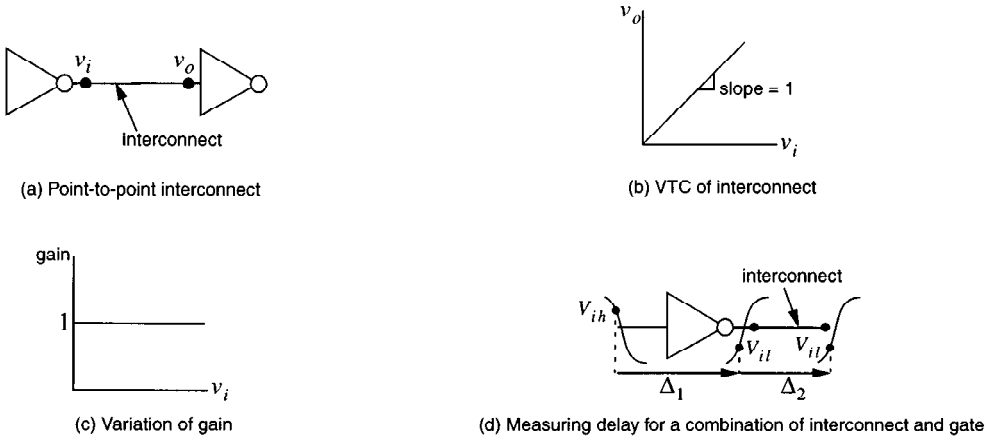


Fig. 4-1. Point-to-point interconnect and its VTC.

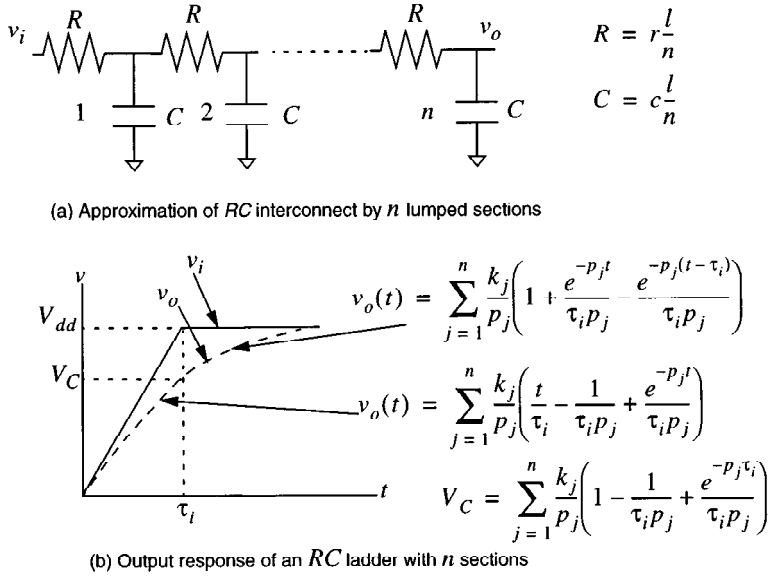


Fig. 4-2. Lumped approximation of *RC* interconnect.

output threshold is less than V_C and the output voltage is then given by:

$$v_o(t) = \sum_{j=1}^{n} \frac{k_j}{p_j}\left(\frac{t}{\tau_i} - \frac{1}{\tau_i p_j} + \frac{e^{-p_j t}}{\tau_i p_j}\right) \quad (4.3)$$

Since this expression cannot be inverted for an explicit equation for delay, we resort to an indirect technique, by examining the output voltage at the instant the input crosses V_{it}. The output voltage at this instant is given by:

$$\begin{aligned} v_o(\tau_i V_{it}) &= \sum_{j=1}^{n} \frac{k_j}{p_j}\left(\frac{\tau_i V_{it}}{\tau_i} - \frac{1}{\tau_i p_j} + \frac{1}{\tau_i p_j e^{p_j \tau_i V_{it}}}\right) \\ &\cong V_{it} \sum_{j=1}^{n} \frac{k_j}{p_j} = V_{it} \end{aligned} \quad (4.4)$$

where use is made of the relation given by (4.2). Therefore, we conclude that delay approaches zero as the input gets slower.

This is further confirmed experimentally using circuit simulation. Consider the circuit shown in Figure 4-3(a) where a ramp voltage source (without loss of generality we use a ramp with $V_l = 0V$ and $V_h = 1V$) is driving an interconnect modeled by five lumped sections. The values for R and C are taken from [11]. In Figure 4-3(b) we plot v_o at the instant v_i crosses V_{it}, as a function of the input transition time for three different threshold values (to mimic the different driver threshold values that could arise in practice). It is clear that the voltage at this instant approaches V_{it} as the input transition time is increased. Unlike gates, delay is never negative even for very slow inputs.

Fast inputs: In this case, V_C is close to zero and the output voltage in the region of interest is given by:

$$v_o(t) = \sum_{j=1}^{n} \frac{k_j}{p_j} \left(1 + \frac{e^{-p_j t}}{\tau_i p_j} - \frac{e^{-p_j (t-\tau_i)}}{\tau_i p_j}\right) \qquad (4.5)$$

It is clear that the delay for a step input is positive since $v_o(0)$ is zero and it takes a finite amount of time for the output to reach the threshold. Unfortunately, it is not possible to infer the behavior (i.e. increasing or decreasing) of delay as a function of τ_i from (4.5). Instead, we experimentally determine the behavior of delay in Figure 4-3(c), where we plot delay versus the input transition time for relatively fast inputs. We find that delay increases with τ_i when V_{it} is less than or equal to the 50% threshold; however, it is interesting to note that it decreases when V_{it} is greater than this threshold. We note that, in general, $V_{il(driver)}$ is less than the 50% threshold for most practical driver circuits and therefore the delay will increase with τ_i for fast inputs.

Thus, as suggested in the intuitive remarks in the beginning of Section 4, while delay never becomes negative, it does asymptote to zero as input transition time approaches infinity. In the next subsection we account for the inductive effects in the interconnect, since inductance can affect delay in board-level signal traces.

4.2. RLC interconnect

If the line resistance is small (which is usually the case for board level interconnect), we cannot approximate a uniform RLC interconnect by a finite number of lumped elements for sufficient accuracy. Also, unlike RC interconnect, the poles of the transfer function for an RLC interconnect are not confined to the negative real axis and are complex. As a result the output could exhibit ringing as shown in Figure 4-4(a), which physically, is due to impedance mismatches in the interconnect circuit [2]. The logic stage connected to the output of the interconnect would then interpret the logic values as shown in Figure 4-4(b). While we define delay and signal transition time, as in the case of RC interconnects, using the driver thresholds, we need an additional parameter, called the **settling time** (denoted by ξ in the figure) to fully characterize the output from a temporal standpoint. From the figure we find that the output of the interconnect can be reliably latched only after $\Delta + \tau_o + \xi$. Using intuitive arguments based on the VTC and by an analysis similar to that of RC interconnects, we can again show that $\Delta \to 0$ as $\tau_i \to \infty$ for any choice of thresholds such that $V_{it} = V_{ot}$.

This completes our discussion of threshold selection for interconnects. In summary, we find that owing to the non-amplifying nature of interconnects, there is no particular voltage with which we can identify the occurrence of events. Hence, to consistently define delay for a combination of gates and interconnects, we use the $V_{il} - V_{ih}$ thresholds from the VTC of the driver to measure the delay of the interconnect. We also showed that the delay asymptotes to zero as input transition time approaches infinity, for any choice of thresholds such that $V_{it} = V_{ot}$. In case of RLC interconnects, we needed an additional temporal parameter, called the settling time, to determine when the output became stable. In the following section, we conclude the paper by summarizing the important contributions of this research and placing them in the proper perspective.

5. Conclusions

In this paper, we have addressed the problem of threshold selection for measuring propagation delay and signal transition time in logic gates and interconnects. The central guiding theme in our study was that delay must be defined so that it reflects the cause and effect relationship between the input and output of a device. As we showed in the paper, non-conformity to this results in physically meaningless values of delay such as negative or zero delay.

We began our study by considering the threshold selection for single input gates. Through a logical, step-by-step development, beginning with a piecewise-linear input to an ideal inverter and concluding with circuit simulation using a realistic input to a physi-

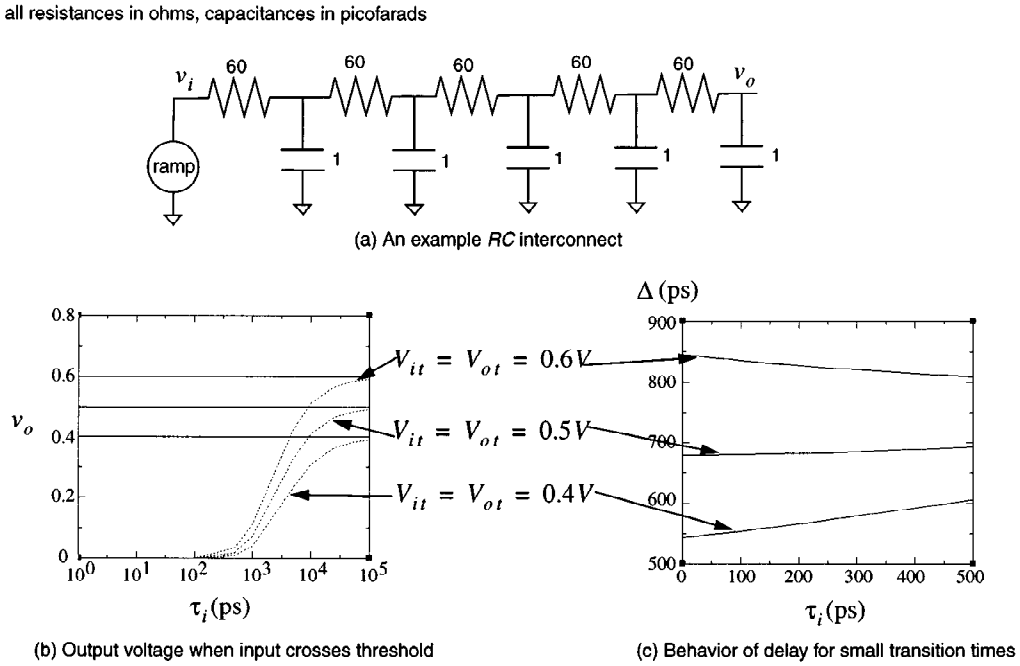


Fig. 4-3. Circuit simulation of a lumped model of RC interconnect.

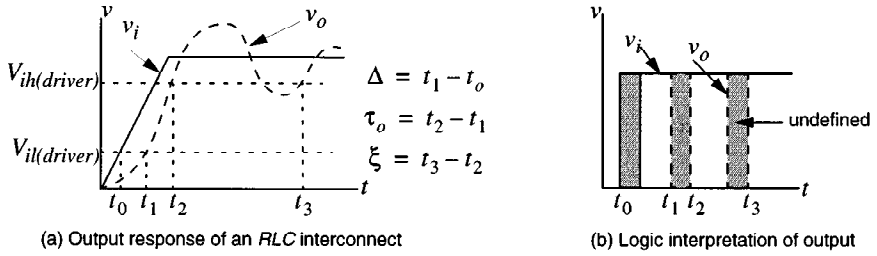


Fig. 4-4. Output response of an *RLC* interconnect.

cal inverter, we found that delay when measured using the unity differential gain thresholds, V_{il} and V_{ih}, from the inverter VTC, is always strictly positive. We also showed that when signal transition time is measured using these thresholds, the delay is relatively less sensitive to input waveshape effects, compared to the transition time measurement using the usual 10%–90% thresholds. Our analysis and subsequent experimental validation showed the inappropriateness of using the popular 50% threshold for delay measurement, since it can give rise to negative delays. We then examined the problem of threshold selection for multi-input gates, both static and dynamic. We found that in case of multi-input gates, we have not one but a family of different VTCs corresponding to the various combination of switching and stable inputs. Based on the insight gained from the inverter study, we found that choosing the minimum V_{il} and the maximum V_{ih} (from the family of VTCs) as the delay and transition time thresholds, ensured a strictly positive delay always. Finally, we examined the problem of threshold selection for simple, point-to-point interconnect structures. Owing to the passive nature of interconnects, we found that there was no clear-cut voltage from the interconnect VTC that would signify the start or end of input and output events. We also showed that while the delay does not become negative, it asymptotes to zero as input transition time approaches infinity for any choice

of thresholds such that $V_{it} = V_{ot}$. In order to define delay consistently for a combination of interconnects and gates, we found it necessary to use the $V_{il} - V_{ih}$ thresholds of the gate driving the interconnect. In case of RLC interconnect, we discovered that the output response could be non-monotonic, and therefore we needed an additional parameter, the settling time, to fully characterize the output temporally.

We believe that this research is of fundamental importance to the accurate delay modeling of gates and interconnects. A careful definition of delay, such as outlined in this paper, paves a natural way for integrating the temporal and functional behavior of a logic gate. Such integrated models are necessary for an accurate and reliable timing analysis at the gate and system level. However, despite the theoretical and practical importance of correct delay measurement, we have not come across a comprehensive treatment of this problem in the literature. To the best of our knowledge, this is the first thorough study of the problem.

Notes

1. Note that in this case $V_l = 0$ and $V_h = 1$. However, any other choice of these thresholds would simply scale the transition time by a constant and would not affect the results of this and subsequent sections.
2. Curves similar to the transient VTC were shown in [13] and were called drive curves. However, they were derived using a model different from ours.
3. Another reason that necessitates a higher gate voltage is the body effect due to the non-zero source to bulk voltage.
4. Interconnects with shunt conductances would have a slope less than 1; however, in most practical interconnects, the shunt conductances are zero and hence we ignore shunt conductances in this paper.
5. These poles and residues can be found by moment matching methods such as AWE [19].

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