THE UNIVERSITY OF MICHIGAN

AFAL-TR-66-169
Supplement I

7274-4-T

ANTENNA SPECTRUM SIGNATURE DATA RECORDING TECHNIQUES

Technical Report
AFAL-TR-66-169
Supplement I

June 1966

Prepared by

J. E. Dute, J. E. Ferris and R. B. Harris

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Contract AF 33(615)-2606
Project No. 4357, Task No. 435703
Contract Monitor, K. W. Tomlinson

Air Force Avionics Laboratory AVWE
Research and Technology Division, AFSC
Wright-Patterson Air Force Base, Ohio 45433

FOREWORD

This report was prepared by the University of Michigan under USAF Contract No. AF 33(615)-2606. The contract was initiated under Project No. 4357, "Electromagnetic Compatibility Techniques" and Task No. 435703, "Interference Measurement Techniques". This was administered under the direction of the Electronics Warfare Division, Air Force Avionics Laboratory at Wright Patterson Air Force Base, Ohio, with Mr. H. M. Bartman as Project Manager and Mr. K. W. Tomlinson as Contract Monitor. This report covers selected phases of the work performed between April 1965 to April 1966. The contractor's report number is 7274-4-T.

This report was submitted by the authors, 2 June 1966.

PUBLICATION REVIEW

This technical report has been reviewed and is approved.

Joseph A. Dombrowski

JOSEPH A. DOMBROWSKI
Lt. Colonel, USAF
Chief, Electronic Warfare Division

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ABSTRACT

This report discusses three techniques that can be employed to obtain analog antenna spectrum signature data in a digital format. The three techniques are: 1) manual, 2) semi-automatic, and 3) automatic. The manual and semi-automatic techniques are discussed briefly. The automatic procedure is discussed in detail along with a system that has been used to obtain data in a digital format. A discussion describing the data format is included to encourage uniformity in the data forwarded to the Electromagnetic Compatibility Analysis Center (ECAC). A discussion of various digital storing mediums that may be employed has been included in Section IV. Typical storage mediums are magnetic tape, punched cards, and punched paper tape. The relative merits of each are discussed along with digitalizing techniques for transferring analog data to a digital format. Section V of the report discusses an automatic system that has been employed by The University of Michigan to obtain data in a digital format usable by ECAC.

I

INTRODUCTION

The Radiation Laboratory and the Radio Science Laboratory of The University of Michigan have been conducting a study for the Avionics Laboratory of Wright-Patterson Air Force Base (WPAFB) to determine an optimum technique for collecting and storing antenna pattern data. The purpose of this study has been to develop a technique that could be employed by the Air Force to collect data to be forwarded to the Electromagnetic Compatibility Analysis Center (ECAC) from which interference predictions would be obtained. During this study, the following digital techniques were considered:

1) Manual
2) Semi-Automatic
3) Automatic

In addition to investigating recording techniques, consideration has been given to the choice of the data format. A data format that has been discussed with both ECAC and the Air Force is presented as a part of this report. Basically this format requires that the data be placed in a digital form on IBM punch cards. The purpose for supplying ECAC with punched cards consisting of raw antenna pattern data is that they can then use this information to perform many different interference analysis programs. This will provide ECAC with a greater degree of flexibility in employing analysis programs when determining interference probabilities.

A brief summary of the recording procedures is presented here to assist the reader in orienting himself as to the various techniques that may be employed to place antenna pattern data in the desired digital format for storage at ECAC.

1.1 Manual

The manual procedure consists of employing an operator to examine the analog plot of the antenna pattern and record the antenna gain, relative to the pattern maximum, at discrete angular increments. In the event the pattern is a wide angle pattern configuration (half-power beamwidth greater than 5^{o}) data is recorded at 1^{o} increments for the full 360^{o} of the pattern. In those cases where the pattern has a narrow beam (half-power beamwidth less than 5^{o}) data is recorded in increments of 0.5^{o}. The relative gain is recorded to the nearest half db. After the pattern data has been recorded, the data sheet is then given to a card punch operator who punches both the angular position and the relative gain onto an IBM punch card. A total of 80 cards are required for each pattern. These cards can then be forwarded to ECAC to become a part of their data base files.

The principal disadvantage to the use of the manual technique is the probability of human errors occurring in the recording of the data. A further disadvantage is that the data collection will be time consuming and costly.

1.2 Semi-Automatic

The second technique investigated was the use of the semi-automatic digital recording procedure. Through the use of the semi-automatic procedure, only one person is required to sample the antenna pattern. Employing this scheme the operator uses a machine to sample the pattern and punch the cards. A computer program is required so that the data collected above can be placed in the proper format for use by ECAC. However, this technique is also laborious and time consuming and the probability of errors is relatively high. Errors are particularly high in those instances where the machine operator is not familiar with antenna patterns.

1.3 Automatic

To overcome the problems for the above techniques, an automatic system to collect antenna pattern data in the proper card format for use by ECAC has been developed. The final results obtained were found to be more accurate and less costly (for large volumes of data) then using either the manual or semi-automatic recording procedures noted above.

There are several techniques that may be employed to obtain data by automatic techniques and these will be discussed in a later section of this report. Several factors must be evaluated when considering an automatic system, e.g. cost, speed with which data may be collected, accuracy of the data, and others that will be discussed later.

Consideration has also been given to the use of commercial equipment to digitalize the data. However, this has been found to be a rather specialized piece of equipment that provides the digital tape as an added feature. Therefore, if the equipment is employed to provide only the digital paper punch tape, it becomes an expensive item for a laboratory to have on inventory. Because of the complexity of the commercial equipment it is not discussed in this report.

II
ECAC DATA FORMAT

During discussions with personnel of ECAC it was learned they prefer antenna pattern data to be in the form of "number pairs". A number pair consists of the antenna gain value and the associated angle (azimuth or elevation) for a given data point. It is felt by ECAC that it is less complicated to write the various programs required for interference prediction for the data assembled in the number pair format. This format relieves a program of the burden of having to search the input data to match a given gain value with its correct angle if data is accidentally placed in the computer in the wrong sequence. Also, if this one data format is adhered to by the Air Force and other services, format variations are eliminated and the ECAC computer programs will perform calculations for statistical analysis of the data much more readily.

ECAC considers cards to be a more desirable form of data storage than magnetic tapes, since they are less susceptible to deterioration or damage and, if partially damaged, may be repunched without difficulty. It is recommended by ECAC that antenna gain values be represented by 4 digits, thus enabling amplitudes to be recorded to .5 db, which is typical of microwave measurement accuracy and is compatible with the recommendations of the report. It is suggested that the angle associated with the antenna gain value also be represented by 4 digits, allowing an increment of 0.5^{o} to be recorded. This is desirable when measuring a high-gain narrow beam antenna, whereas when measuring a low gain wide-beam antenna, an angle increment of 1.0^{o} will suffice.

Considering the above data format, it follows that the card format will consist of 8 columns per number pair. Thus 9 data points are placed on each card, consuming 72 columns. The remaining 8 columns may be used for identification purposes. A total of 80 cards will be required for each antenna pattern. Also, it will be necessary for each set of data forwarded to ECAC to be accompanied with a data sheet describing the card content, i.e. antenna model and type, etc. This data sheet may be a punched card.

III

SEMI-AUTOMATIC DIGITAL RECORDING PROCEDURE

The semi-automatic procedure requires an operator to manually sample a pre-recorded analog antenna pattern. The operator manipulates a pair of cursors on a machine on which the antenna pattern is placed. This machine is manually directed to sample the analog waveform at selected points and to transfer the magnitude of the sampled value to an analog-to-digital converter unit. The converter unit digitalizes the data and feeds a card punching unit which automatically punches the data onto cards. Figure 1 shows a typical setup used in this procedure. The analog to digital converter unit is seen at the left of the photo, the sampling machine ("Oscar" by the Benson-Lehner Company) is shown in the center, and the card punch unit on the right. This semi-automatic procedure has several drawbacks not present in a completely automatic procedure to be discussed in a subsequent section. First, it is doubtful whether this system can conveniently punch the digitalized data onto IBM cards in the format suggested by ECAC (see Section II). Secondly, the analog waveform must be sampled manually by a human operator. A study at The University of Michigan has shown that when the equipment is operated by an individual unfamiliar with antenna patterns, there is a high probability of errors appearing in the digital data. These errors are usually difficult to locate and costly to correct. Third, the curve sampling procedure is tiring to the eyes of the operator and, therefore, increases the probability of errors in the data.

The University of Michigan study has uncovered severe limitations of the semi-automatic technique of data conversion. Such would be the result of work placed with commercial analog-to-digital converter facilities unless the facility was completely automated. The errors introduced into the data by the human operator, if not discovered, would render the data essentially meaningless to the user (ECAC for example). Therefore, if it is necessary to use the semi-automatic procedure, it is suggested that only trained antenna personnel be used as the machine operators.

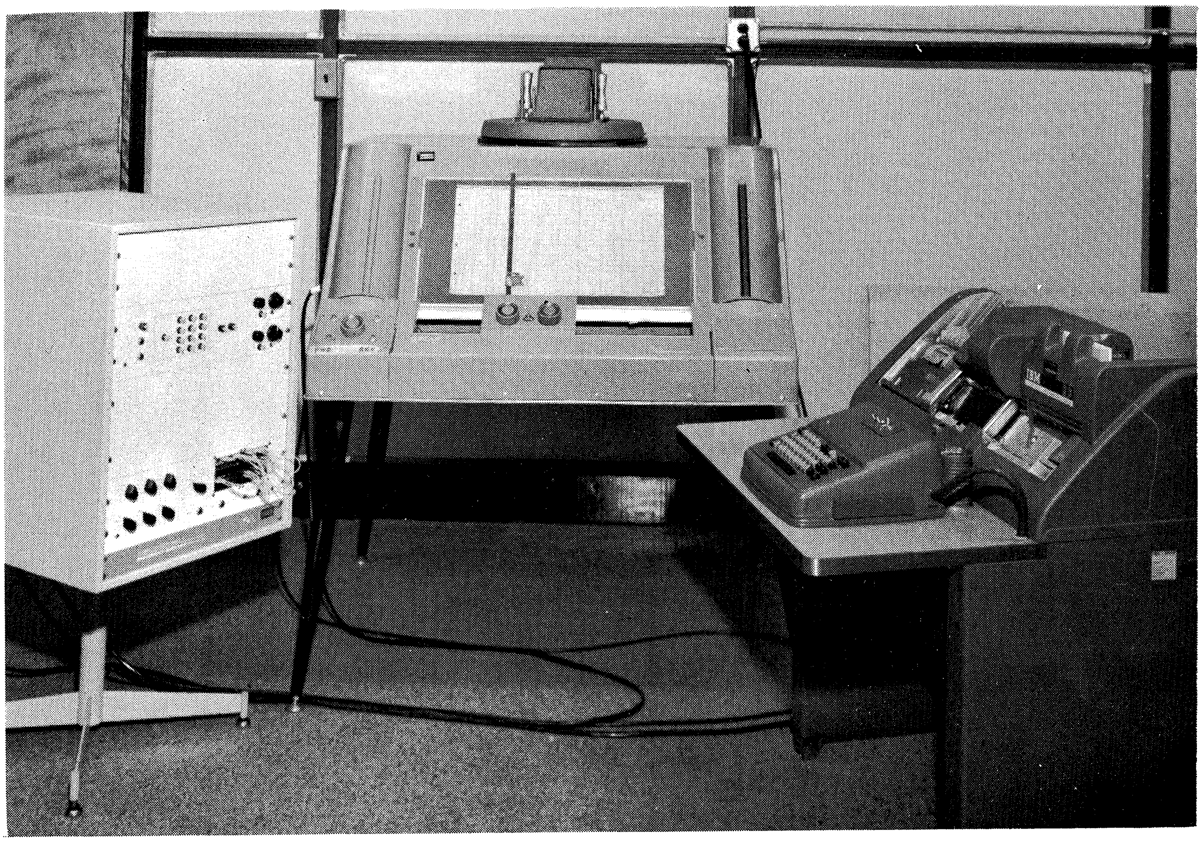


FIG. 1: SEMI-AUTOMATIC DIGITAL RECORDING EQUIPMENT

The results obtained using antenna trained personnel to handle the manual aspects of this procedure have been quite rewarding. However, the optimum procedure for converting antenna data to digital form is to employ the fully automatic system to be discussed in Section IV.

IV

AUTOMATIC DIGITAL RECORDING TECHNIQUES

As a part of the Department of Defense program for the reduction of radio frequency noise, a requirement exists to catalog, in a computer compatible format, the characteristics of a large variety of antennas presently part of or contemplated to be part of the military inventory. As a result of earlier work, The University of Michigan is in position to specify the design of a system for rapidly and readily acquiring antenna pattern measurement data in a form acceptable by a digital computer for purposes of classification and analysis. Prime considerations in the designs to be discussed were cost, reliability, ease of integrating into the existing equipment, ease of operation and compatibility with existing ECAC facilities.

Although the final information storage is to be on punched cards, there are some advantages to utilizing any of several storage mediums at the point where the data is actually gathered, such as magnetic tape, punched cards, and punched paper tape. Magnetic tape may be broken into two subclasses - the better known magnetic incremental tape recorders and the apparently new technique developed by The University of Michigan for their own digital antenna recording system (Section V). The conventional incremental recording technique for recording digital data was rejected for cost reasons and the fact that such equipment is not only sizeable, but difficult to operate in a dirty field environment. The alternate serial magnetic tape technique, while preferable over incremental magnetic tape recorders for cleanliness requirements and cost reasons, is not as well suited for transmission over existing data transmission facilities as is paper tape. Further, this technique requires an additional computer operation to put the antenna data on cards. The punched card technique was rejected on the basis of cost and size considerations for field operations. Another minor weak point of cards is that they must be carefully packed when being transported - whereas, magnetic tape and paper tape are relatively rugged. In the final analysis, the punched paper tape was selected for a number of reasons. These include the availability of paper tape equipment (teletype) in the military inventory, which will simplify logistic and maintenance problems; the inherent durability of this equipment is demonstrated in extensive field operations; the fact that it will be possible in the near future to send the paper tape recorded information over existing military communications facilities; and finally cost. A possible minor drawback of paper tape is that it does require a facility at which the paper tapes can be converted to punched cards. Inasmuch as there are a number of these facilities available on a commercial basis throughout the country, this is not a serious problem. The equipment is relatively small and inexpensive - and could be leased for use at ECAC.

4.1 Digitalizing

Existing antenna pattern recorders have rotating shafts for both the antenna azimuth and the attenuation. The conversion of the analog shaft position to a digital form may be accomplished in a number of ways. The principle ones are: the use of a potentiometer to develop a voltage which is proportional to position and then applying this voltage to an electronic analog to digital converter (ADC); use of a shaft encoder (either brush or optical type); or by the use of a resolver. In the potentiometric method, the brushes are subject to contact wear. Similar comments hold for the brush type shaft encoders. Optical shaft encoders are well suited for this application, however, they are quite expensive; because there is generally a light source involved, they are subject to a minor reduction in reliability. The resolver method of shaft encoding is between the potentiometer/ADC and shaft decoder approaches, from the standpoint of both cost and precision. In the resolver method, the phase shift between the excitation and the output voltage is proportional to rotation. Electronic counter techniques can be used to measure the phase angle and thus shaft position.

The practical limits of accuracy of the potentiometric method are approximately one tenth of a percent or about a third of a degree - this is caused principally by the linearity available from potentiometers. The practical limitation of the resolver type encoder is approximately one tenth of a degree and is apparently limited by phase shifts in the magnetic circuit of the resolver. Optical shaft encoders have been made that are able to resolve 360^o into a million parts or more. Optical shaft encoders are the most expensive as they generally require very precise optical patterns and extensive decoding electronics.

Considering the tradeoffs between shaft loading, required resolution, and reliability, a first choice for this antenna recording system is to use the potentiometric method. However, the system discussed is laid out in such a manner that should it be desirable at a future date to upgrade performance, few changes would have to be made in the logic to incorporate the use of more precise shaft encoding techniques.

4.2 Data Takeoff and Recording

For several reasons punched cards are the most convenient means for storing antenna pattern data at ECAC. A typical format would be for the first eight columns of these 80 column cards to contain alpha-numeric heading identification. The heading information is used to identify test numbers, equipment types, date and the like. The remaining columns make it possible to record nine data words each of which has two four-digit numbers; one number for azimuth and the second for attenuation. Each of the eight heading characters and the 72 data characters occupies one card column.

However, as noted in the introduction of this section paper punch tape will be employed as the storage medium prior to putting the data in card format. The paper punch format has in addition to the data and the heading identification, certain nonprinting symbols. The addition of these symbols makes it possible to generate a data printout by inserting the tape into a teletype page printer. Although these nonprinting format symbols occupy about 23 percent of the punched paper tape, it is believed the advantage of being able to readily monitor the test results is significant. The paper tape required to produce the 80 cards needed to record an entire antenna pattern is 70 feet long. The paper tape supply reels are typically 1000 to 1200 feet in length. The low cost of the tape (about $2/reel) and the relatively small cost of implementing the generation of these format symbols does not discourage their usage.

The Output Programmer, which is discussed in Section 4.4 controls the format (not just the format symbols) of all data to be recorded. Table I indicates what is to be recorded for each of the 25 program sequence steps, and the single non-punching operation. Each complete cycle of the Output Programmer generates the data for one punched card and is defined as a data frame.

Table II shows part of the ASCII eight level paper tape code which is now coming into heavy usage for the transmission of data, numerical machine tool control and computer input/output. The use of the eighth bit, which is an even parity check, is optional.

4.3 Block Diagrams

Figure 2 is a block diagram of the entire recorder system. In this section, only the functional operation of the recording system will be discussed - a detailed discussion of the logic involved in each of the functions is discussed in a subsequent section.

While in many instances it is easier to understand the operation of a system by starting from the inputs and going to the outputs, it is believed that in this case with multiple inputs that the explanation will be appreciably easier to understand by starting at the output and working back to each of the three input sources. Therefore we will start on the right side of the diagram with the eight level paper punch which records the output information in a form compatible for being readily translated into punched cards for final ECAC usage as discussed earlier. In order to record information with punched paper tape recorder, an appropriate set of eight code magnets are energized while a time shaped signal is applied to the clutch which causes the punching, and tape advancing operations. The Output Control block which for the

TABLE IV-1: OUT PROGRAMMER SEQUENCE

Output Programmer Position	Information Type	Symbol	Action
1	None	None	Reset Programmer to start.
2	Format	Line feed	Advances teletype roller.
3	Format	Carriage return	Used with the line feed to start new line.
4	Format	Start of message	Indicates to tape to card converter beginning of data frame.
5	Heading	Alpha/Numeric character	1st digit of heading data
6	Heading	Alpha/Numeric character	2nd digit of heading data
7	Heading	Alpha/Numeric character	3rd digit of heading data
8	Heading	Alpha/Numeric character	4th digit of heading data
9	Heading	Alpha/Numeric character	5th digit of heading data
10	Format	Space	Simplifies reading of page copy
11	Heading	Alpha/Numeric character	6th digit of heading data
12	Heading	Alpha/Numeric character	7th digit of heading data
13	Heading	Alpha/Numeric character	8th digit of heading data
14	Format	Numeric character	Separates heading information and data
15	Data	Numeric character	1st Data Word Subroutine, Word Subroutine is: a) four digits of azimuth data b) space c) four digits of attenuation data d) space
16	Data	Numeric characters	2nd Data Word Subroutine. Etc.
17	Data	Numeric characters	3rd Data Word Subroutine. Etc.
18	Data	Numeric characters	4th Data Word Subroutine. Etc.
19	Format	Line feed	Advances teletype roller.
20	Format	Carriage return	Used with line feed to start new line.
21	Data	Numeric characters	5th Data Word Subroutine. Etc.
22	Data	Numeric characters	6th Data Word Subroutine. Etc.
23	Data	Numeric characters	7th Data Word Subroutine. Etc.
24	Data	Numeric characters	8th Data Word Subroutine. Etc.
25	Data	Numeric characters	9th Data Word Subroutine. Etc.

	1	2	3	Tape Feed	4	5	6	7	8
Line Feed		X		o	X				
Carriage Return	X		X	o	X				X
Start of Message			X	o					X
End of Message	X	X		o					
Space				o			X		X
0				o		X	X		
1	X			o		X	X		X
2		X		o		X	X		X
3	X	X		o		X	X		
4			X	o		X	X		X
5	X		X	o		X	X		
6		X	X	o		X	X		X
7	X	X	X	o		X	X		X
8				o	X	X	X		X
9	X			o	X	X	X		
A	X			o				X	
B		X		o				X	
C	X	X		o				X	X
D			X	o				X	
E	X		X	o				X	X
F		X	X	o				X	X

K = Punched hole

TABLE IV-2: ASCII EIGHT-LEVEL PAPER TAPE CODE

	1	2	3	Tape Feed	4	5	6	7	8
G	X	X	X	o				X	
H				o	X			X	
I	X			o	X			X	X
J		X		o	X			X	X
K	X	X		o	X			X	
L			X	o	X			X	X
M	X		X	o	X			X	
N		X	X	o	X			X	
O	X	X	X	o	X			X	X
P				o		X		X	
Q	X			o		X		X	X
R		X		o		X		X	X
S	X	X		o		X		X	
T			X	o		X		X	X
U	X		X	o		X		X	
V		X	X	o		X		X	
W	X	X	X	o		X		X	X
X				o	X	X		X	X
Y	X			o	X	X		X	
Z		X		o	X	X		X	

K = Punched hole

TABLE IV-2: ASCII EIGHT-LEVEL PAPER TAPE CODE
(Continued)

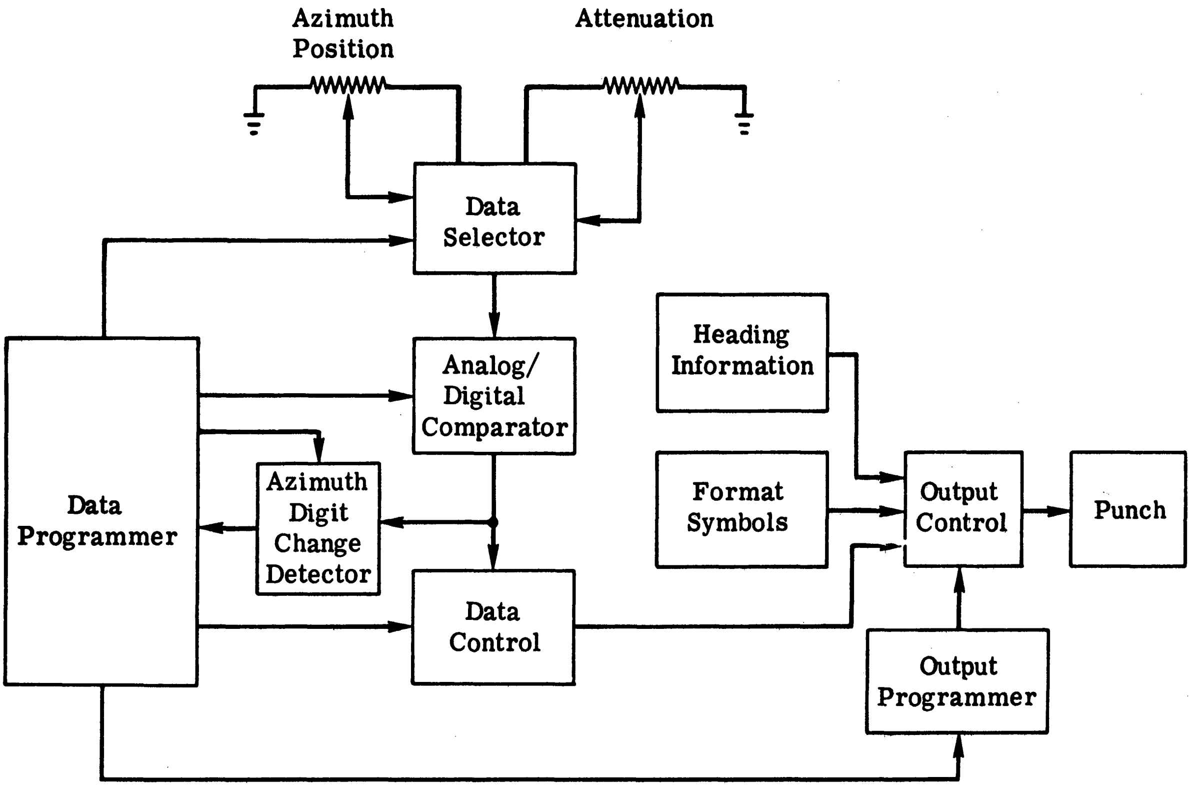


FIG. 2: ANTENNA RECORDER BLOCK DIAGRAM

most part is made up of a number of gates under the control of the Output Programmer, produces the necessary drive signals for the punch. The three sources of data gated by the Output Control are: 1) the heading information, 2) format symbols, and 3) the data to be recorded. The Output Programmer provides the correct gating sequence at the Output Control to cause the recording of the eight digits of heading information and the nine data words (each made up of four digits of azimuth and four digits of attenuation information). Interspersed with these are appropriate format symbols. It may be noted that both the heading information and the format symbols are generated one character at a time, whereas the antenna data words contain two four-digit numbers each. The data sequence is controlled by the elements which occupy the left half of the diagram. The normal position of the Data Selector is such that the antenna position is being digitized in the Analog/Digital Comparator (ADC). When the ADC is operating on azimuth information, its output is applied to the Azimuth Digit Change Detector. If the least significant digit of the azimuth position has not changed, there is no output from the Azimuth Change Detector and the Data Programmer causes the resetting of the ADC to 0 and reperforms its analog to digital conversion of the azimuth position. When the Azimuth Digit Change Detector determines a change has occurred in the least significant digit of the azimuth position, a readout sequence is initiated. The Data Programmer commands the Data Control to read out the azimuth digits one at a time to the Output Control for recording. After the readout of the azimuth data is complete, the Data Programmer causes the Data Selector to switch to the attenuation signal. When this A-D conversion process is complete, the Data Programmer causes the four attenuation digits to be readout by the Data Control into the Output Control for recording. Upon completion of the recording of the last digit of the attenuation information, the Output Programmer advances one step to the next data position and simultaneously resets the Data Selector to monitor the output of the azimuth potentiometer. This process continues until nine data words have been recorded, at which time the Output Programmer resequences and generates heading information for the subsequent data frame.

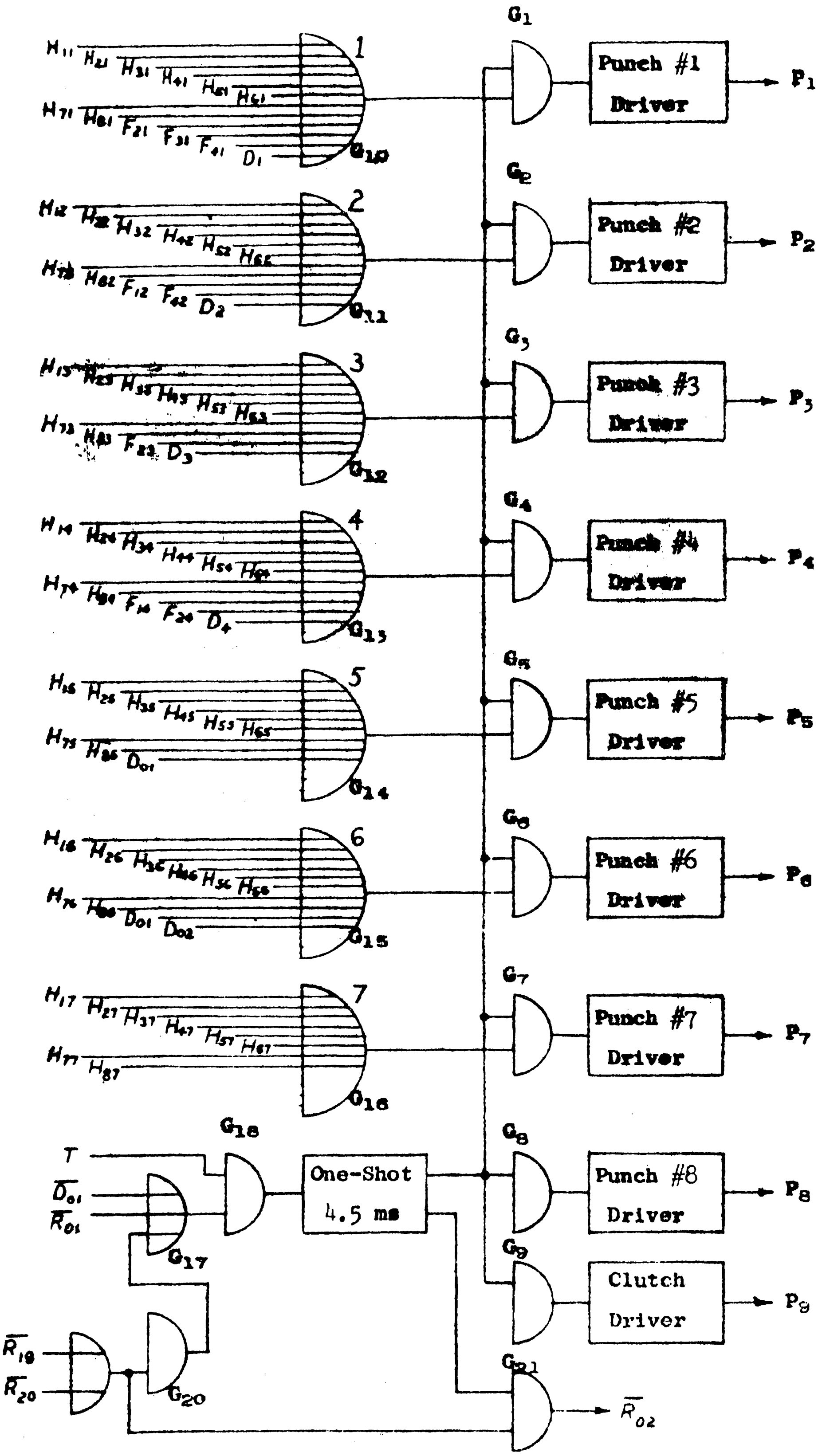
4.4 Logic Diagrams

Figure 3 is a logic diagram of the Output Control. The driver circuits are power stages which have sufficient output to drive the punch code magnets directly. The two input AND gates which precede all of the drivers will cause a hole to be punched at the respective position when an input at any one of the multiple input OR gates and 4.5 ms punching pulse are both present.

The letter designations H., F., or D. of the input signals to the OR gates are heading information, format information, and data respectively. The subscript designations are best explained by the following example: H_{31} is that part of the third heading digit which would occur at punch position 1. A punching operation is initiated each time a signal is present at the out of OR gate 17 and clocked in by gate 19. The sources for the signals which drive the 4.5 ms one-shot will become apparent later.

Figure 4 is a logic diagram of the Heading Data Generators. As the diagram in upper left corner indicates, these are several parallel switches which are activated by the appropriate "R" signals of the Output Programmer. The switches are closed in accordance with the desired alpha-numeric character as shown in Table II and are discussed in the format section.

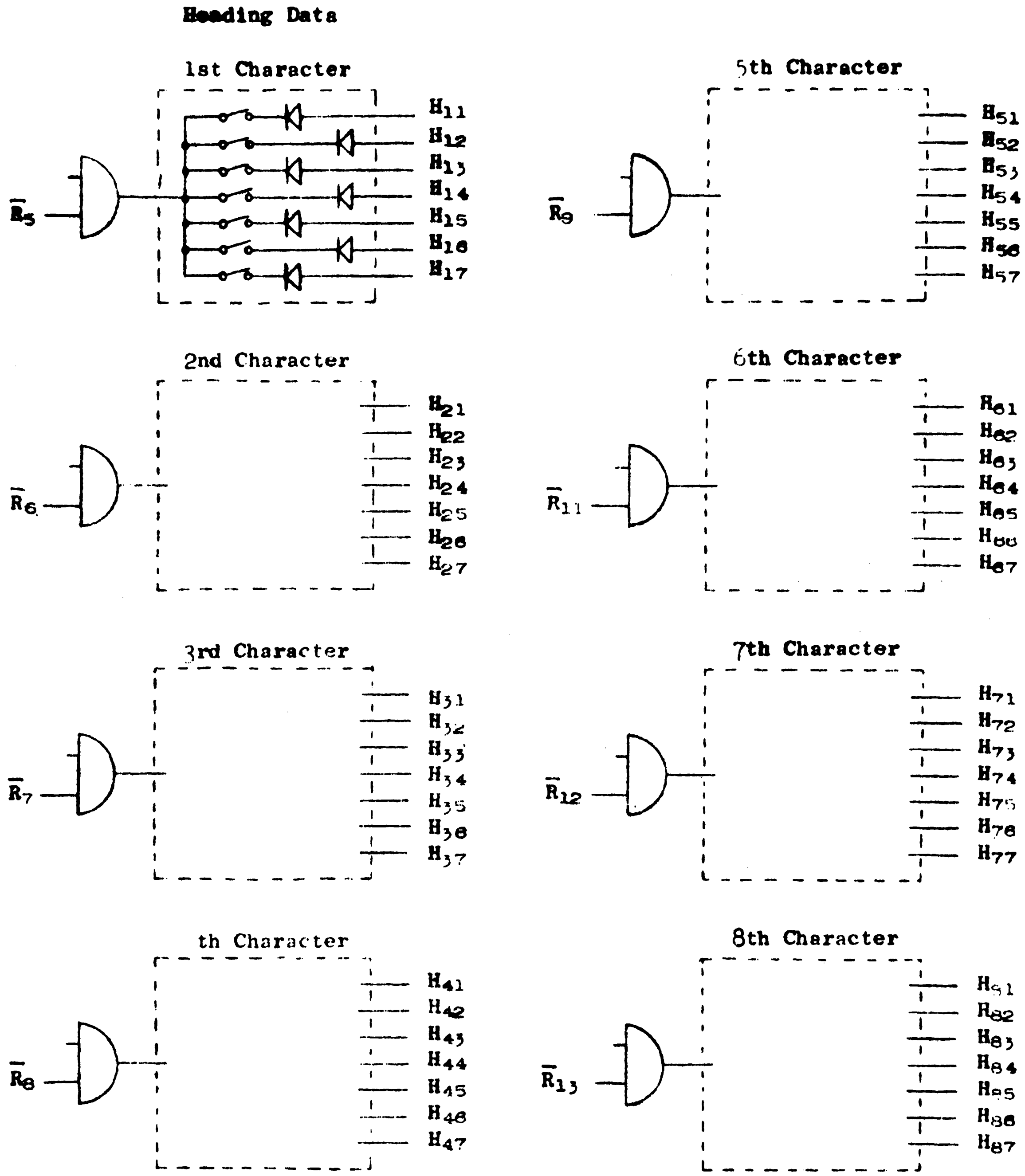
Figure 5 is the logic diagram of the Format Symbol Generator. The format symbols are generated in a manner similar to the heading symbols, but, because they never change, they may be wired permanently rather than requiring switches. With the exception of the space symbols, the "R" signals of the Output Programmer control the generation of individual format symbols. The space symbol is controlled by both the Output Programmer and the Data Programmer since spaces are used for both heading information and data.



Notes:

1. D's from Data Control
2. R's from Output Programmer
3. H's from Heading Data Generators
4. F's from Format Symbol
5. P's to Punch and Clutch Magnetics
6. T from Data Control

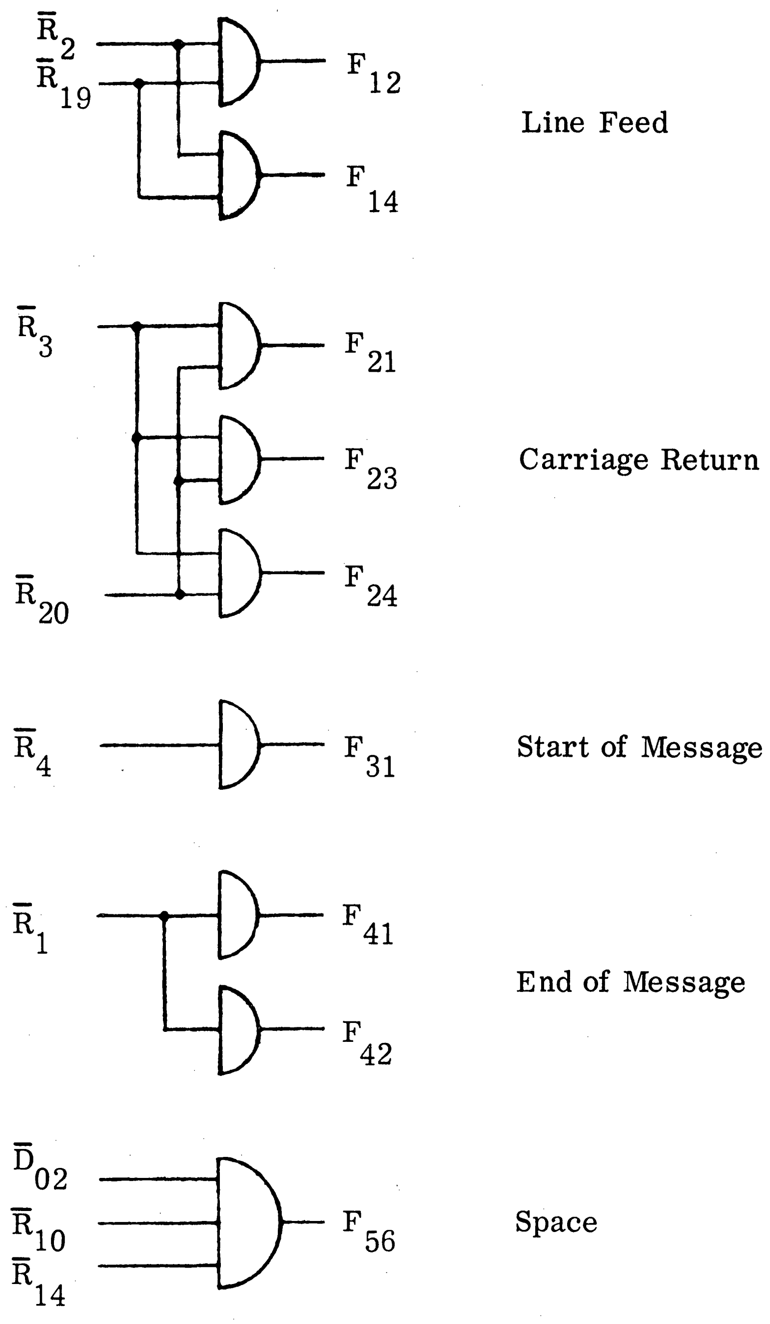
FIG. 3: OUTPUT CONTROL



Notes: 1. Outputs of Heading Data Generators go to OR gates of Output Control.

2. Second digit of letter subscript indicates appropriate OR gate of Output Control.

FIG. 4: HEADING DATA GENERATORS



Notes:

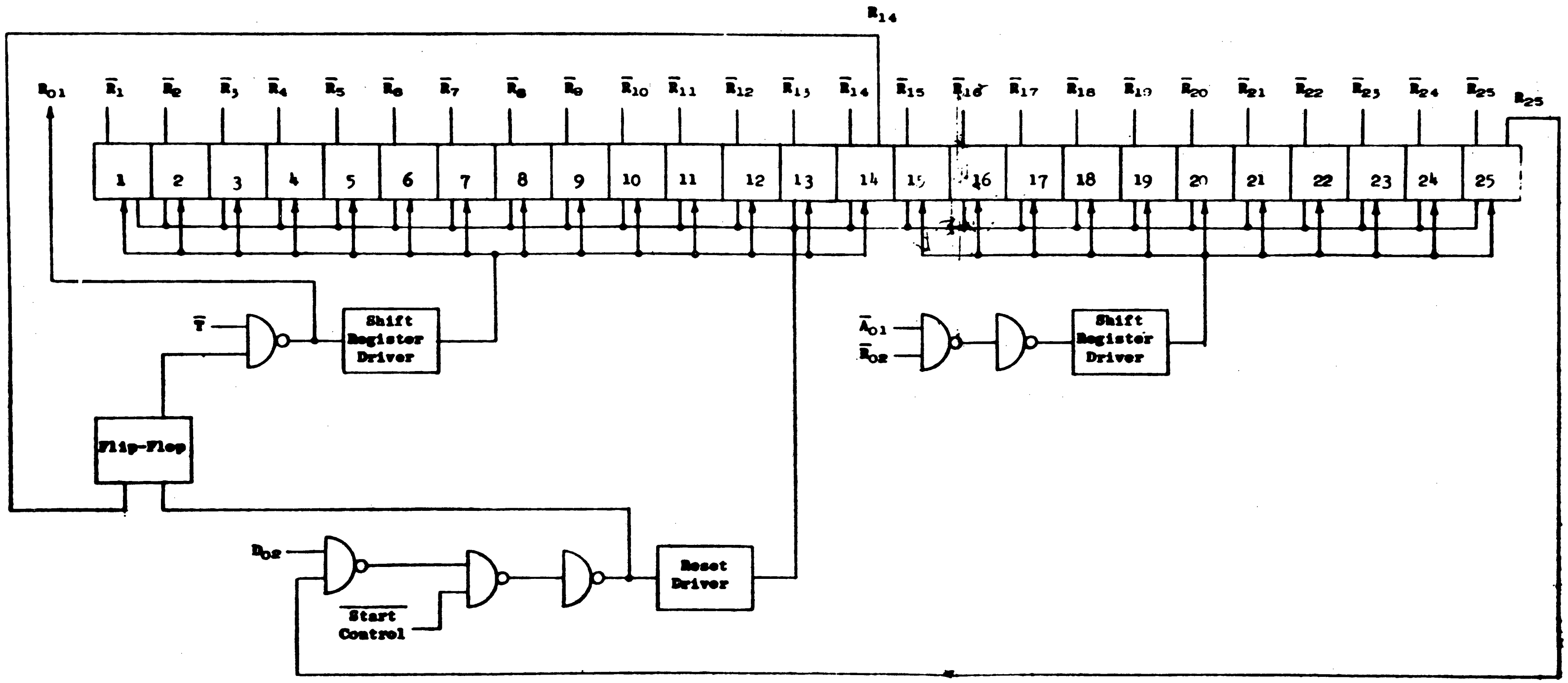
1. F's go to Output Control
2. R's from Output Programmer
3. D's from Data Control

FIG. 5: FORMAT SYMBOL GENERATORS

Figure 6 is the logic diagram of the Output Programmer. Fundamentally, this is a long shift register each stage of which corresponds to a given step of the Output Programmer sequence - shown in the right-hand corner of this figure. The programmer shift register is caused to advance by either of two signals. The register is automatically advanced from position 1 through 14 to record the heading and format information. The register is advanced from position 15 through 23 under the control of the Data Programmer when data words are to be recorded. At the completion of each data word, the register advances one step to the next position in the programmer sequence. Upon completion of the program sequence, the register is automatically reset to position 1.

Figure 7 is the logic diagram for the Data Control. The Data Control causes the four digit output of the ADC to be readout one digit at a time for the recording operation. The six-stage shift register controls the sequencing operation. For each of the first four positions of this register, one digit of data is recorded. As the register moves into each of these four positions, the signal D_{01} is generated which causes the initiation of the punching signal. In position 5, the signal D_{02} is generated which causes the resetting of the Output Programmer (when the Output Programmer register is in its last position). In addition, the signal D_{02} also causes a space signal to be punched (to separate the azimuth and attenuation words); it also indicates to the Data Programmer that a word sequence has been completed.

Figure 8 is the logic diagram of the Analog-to-Digital Converter (ADC). The ADC is made up of a counter (shown near the top of the diagram in four blocks), a Digital-to-Analog (D/A) converter which produces a DC voltage proportional to the instantaneous value of the count, and a comparison amplifier which compares the output of the D-A converter with the output of the signal selector. The divide-by-two counter gives rise to counting in half db steps, or half degree steps as appropriate; the two divide-by-ten counters give rise to the units and tens portion of the word; and



Notes:

1. R's to or from Output Control
2. D's from Readout Control
3. A's from Data Programmer
4. T's from Data Control

FIG. 6: OUTPUT PROGRAMMER

Notes:

1. A_{02} from Data Programmer
2. D_{01} to Output Control
3. D_{02} to Output Programmer And Data Programmer
4. Other D's to Output Programmer and Format Symbol Generator
5. C's from ADC Counter
6. $\overline{T}$ to Output Programmer
7. T to Output Control

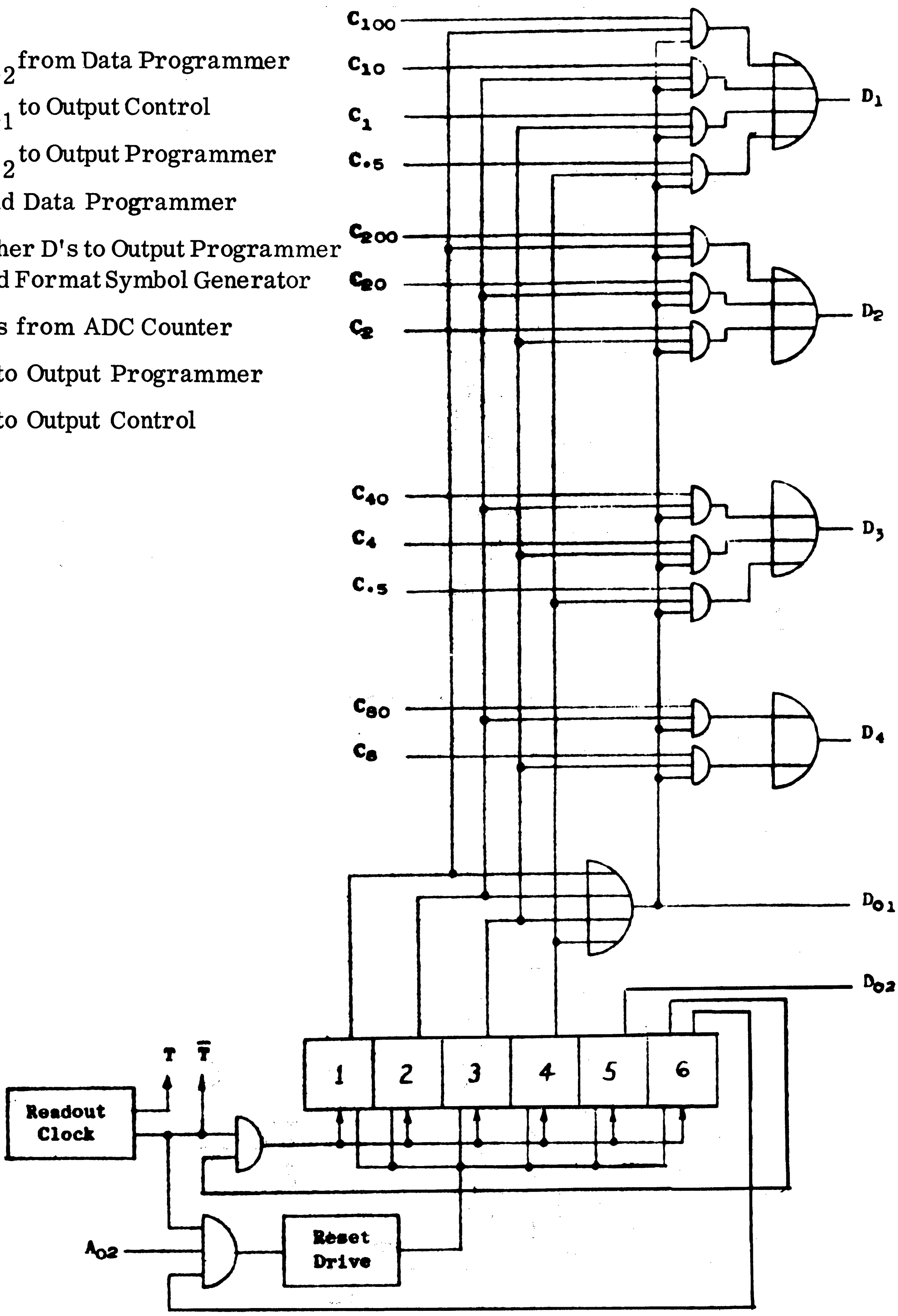
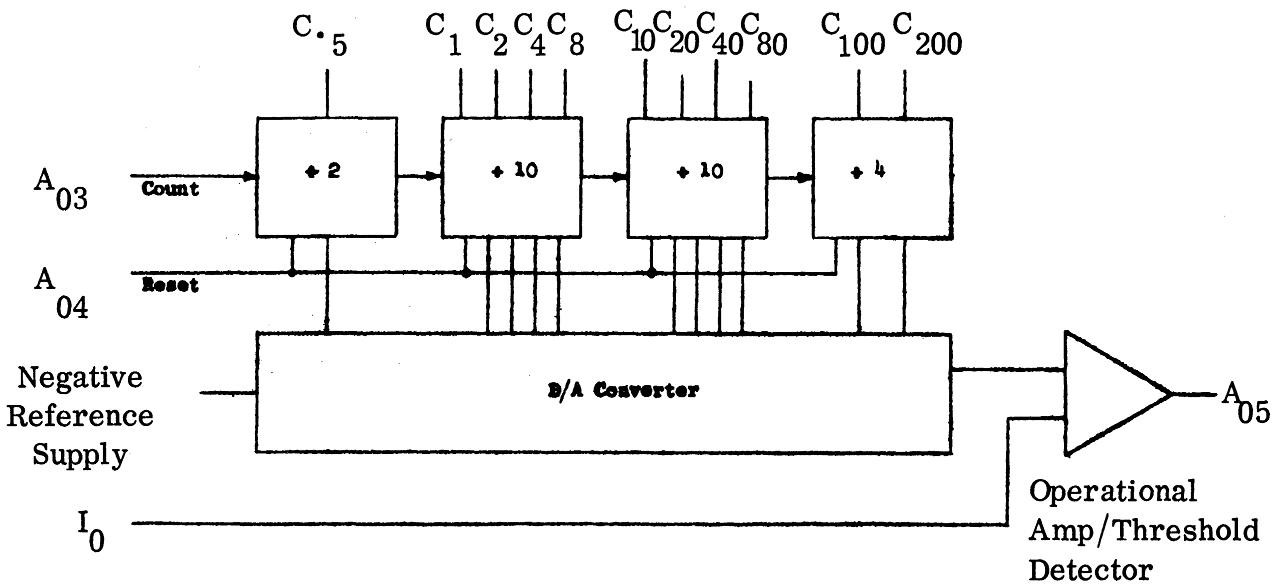


FIG. 7 : DATA CONTROL



Notes:

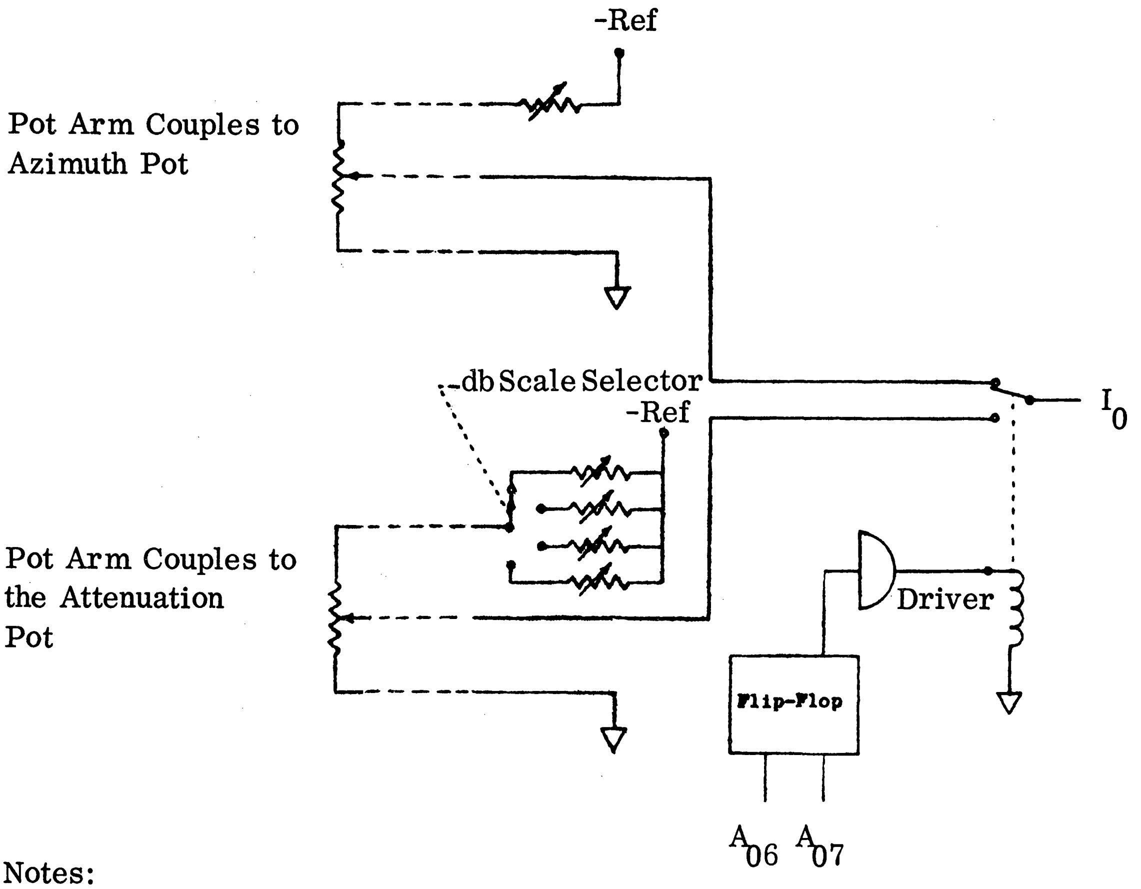
1. A's to or from Data Programmer
2. I_0 Analog Input Signal From Data Selector
3. C's to Data Control

FIG. 8: ANALOG-DIGITAL COMPARATOR

the divide-by-four counter gives rise to the hundreds digit of the word. Inasmuch as the most significant digit cannot go beyond three for 360^{o}, a divide-by-three counter would be sufficient, but a divide-by-four counter is more economical.

Figure 9 is a diagram of the Data Selector. As noted earlier, the normal position of the Data Selector relay is to monitor the azimuth potentiometer. An adjustable resistor in series with the azimuth potentiometer is used to calibrate azimuth position. By supplying both the azimuth potentiometer and the D-A converter receiver with the same voltage, the azimuth position becomes essentially independent of the magnitude of the reference voltage and a function only of the ratio of resistors of the azimuth potentiometer circuit and the D-A circuit. The attenuation db value is determined in a similar manner.

Figure 10 is a logic diagram of the Data Programmer. The essential part of the Data Programmer is an eight-stage shift register. Positions 1 and 2 of this register are used to program the A/D conversion of the azimuth output. In position 1, the ADC counter is reset; in position 2 the clock is gated into the ADC counter until the D/A voltage matches the azimuth potentiometer voltage. Position 3 is used to determine if there has been a change in the least significant azimuth digit. This change is determined by the sign change detector which is discussed in the next paragraph. If no change has occurred, the Sign Change Detector causes the register to be reset to position 1 and the azimuth signal is rechecked. If, on the other hand, there has been a change in the azimuth position, the register is advanced to position 5 which causes the Data Selector to change to attenuation input and the ADC counter is reset. The register then advances to position 6 where the attenuation voltage is digitized. In position 7, as in position 3, the data output of the ADC is recorded. In position 8 the Data Selector is reset to azimuth. The next clock pulse advances the register to 1 and the process is repeated.



Notes:

1. I_0 to Analog-Digital Comparator
2. A's from Data Programmer

FIG. 9: DATA SELECTOR

Notes:

1. A_{06}, A_{07} to Data Selector
2. A_{03}, A_{04}, A_{05} to or from Analog to Digital Comparator
3. A_{02} to Data Control
4. A_{01} to Output Programmer and to Digit Change Detector
5. A_{08}, A_{09}, A_{10} to and from Digit Change Detector

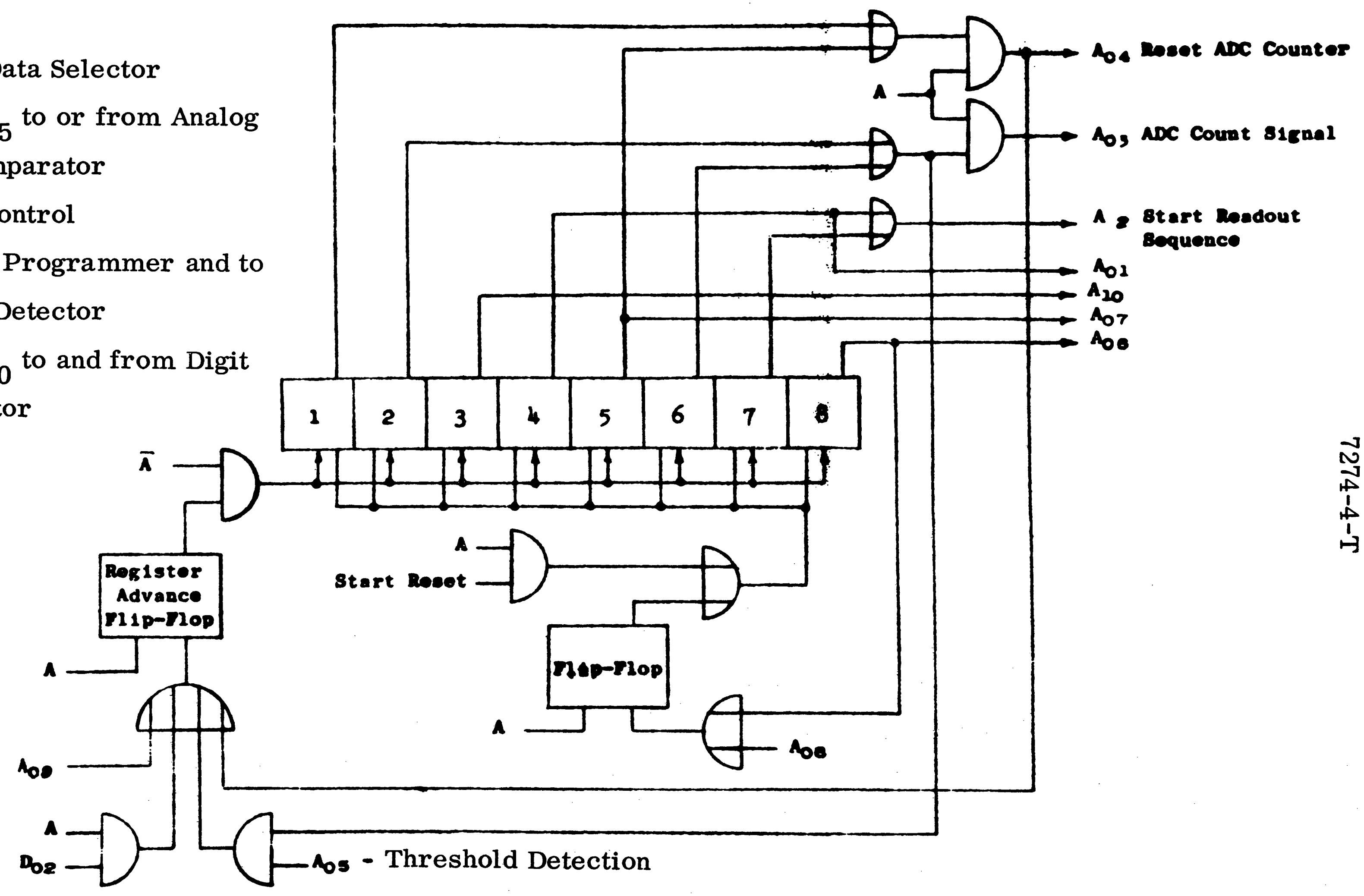


FIG. 10: DATA PROGRAMMER

The Digit Change Detector (DCD) is required to determine if the azimuth has changed by 0.5^{o} since the previous time a data word was recorded. Until it does change, the ADC monitors only the azimuth channel where it continuously tests for a change. As soon as a change is noted, a data word sequence is initiated and both the new azimuth and its corresponding value of attenuation are recorded. To understand the DCD, assume that the flip-flop memory in Figure 11 is in the state so that set output is "1" and the reset output is "0". Further, assume that $C_{.5}$ = "1". These two signals will produce an output from AND gate G_5 which in turn will produce an output from OR gate G_6. When the shift register of the Data Programmer reaches position 3, it generates the signal A_{10} which then will AND with the output of G_6 to produce an output at G_7. This indicates that no digit change has occurred and causes the shift register of the Data Programmer to be reset. As sume that during the next test that $C_{.5}$ has changed to "0". When $C_{.5}$ and its inverse $\bar{C}_{.5}$ are ANDed with the flip-flop outputs in gates G_{14} and G_{15}, there will be no output. This time when the test signal A_{10} comes along, the AND gate G_8 will produce an output which allows the Data Programmer shift register to advance through its data recording sequence. When the Data Programmer reaches position 4, A_{01} is generated allowing the flip-flop to "memorize" the new state of $C_{.5}$ which will be used as a reference in subsequent digit change tests.

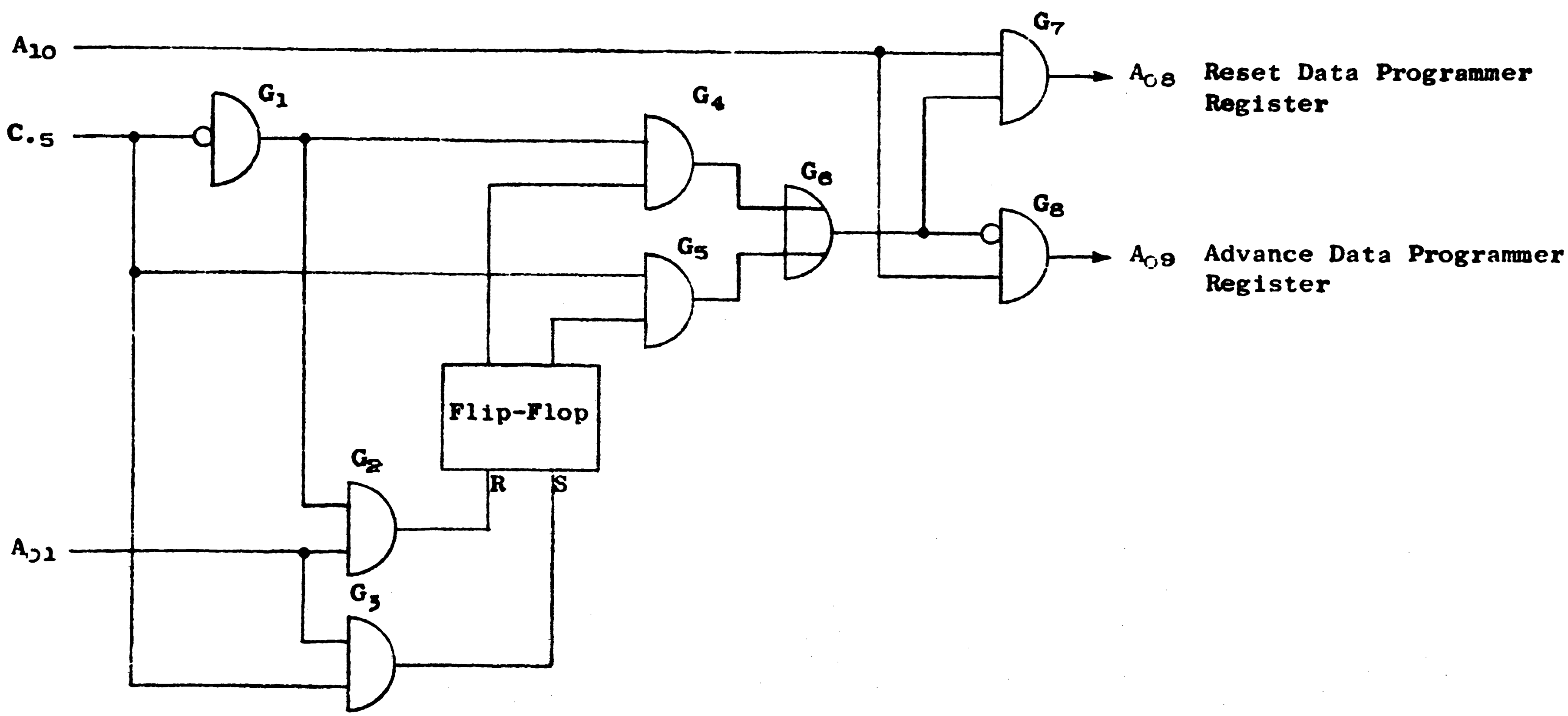


FIG. 11: DIGIT CHANGE DETECTOR

Notes:

1. $C_{.5}$ from Analog to Digital Comparator
2. A_{01}, A_{10} from Data Programmer

V

THE MICHIGAN AUTOMATIC SYSTEM

The instrumentation console presently being used for antenna measurements at the University of Michigan is shown in Fig. 12. Included in the console is a digital antenna pattern recording system which was recently installed as a part of a Spectrum Signature study administered by the Avionics Laboratory of Wright Field.

In the following paragraphs, the design and theory of operation of the digital recording and playback-equipment (see Figs. 13 and 14) is presented. The function of this equipment is to generate a quarter-inch tape recording of antenna pattern data with an amplitude resolution of 121 levels and an angular resolution of one degree. The output format, sequence of logic operation, and design of special circuitry will be discussed.

The pattern data from these tapes are then transferred to half-inch IBM tapes by another analog-to-digital converter and IBM 729 tape deck (see Fig. 15). These IBM tapes, in turn, are processed by an IBM 1401 data processor (see Fig. 16) to produce IBM cards.

5.1 General Description

The function of the equipment is to sample, at one-degree intervals, an analog waveform which represents the field-strength pattern of an antenna which is rotated with respect to the measurement sensor, and to record the magnitude of the sampled value on a general-purpose tape recorder in the form of a binary-coded number. Additional data recorded on the tape are a start pulse for the IBM 729 tape deck, a reference pulse for the IBM 1401 data processor, a start/stop ($\pm 180^{o}$) marker, run number, date, and an identification code.

The analog input to the digital recording equipment is the antenna signal level, taken from a potentiometer which is mechanically gauged to the pen servomechanism of the antenna pattern recorder. Depending on the type of antenna to be tested, different ranges may be used on the analog antenna pattern recorder. Standard chart ranges are 40-, 60-, and 80- decibel logarithmic, and 100- division linear. Of these

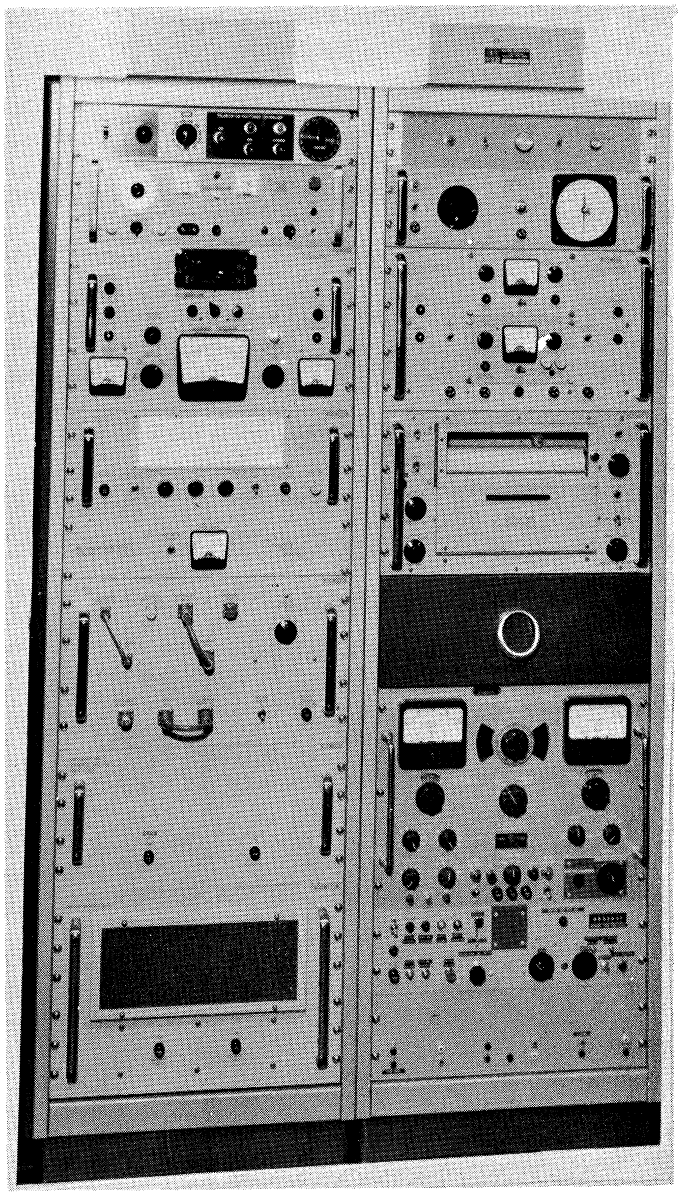


FIG. 12: ANECHOIC CHAMBER INSTRUMENTATION CONSOLE

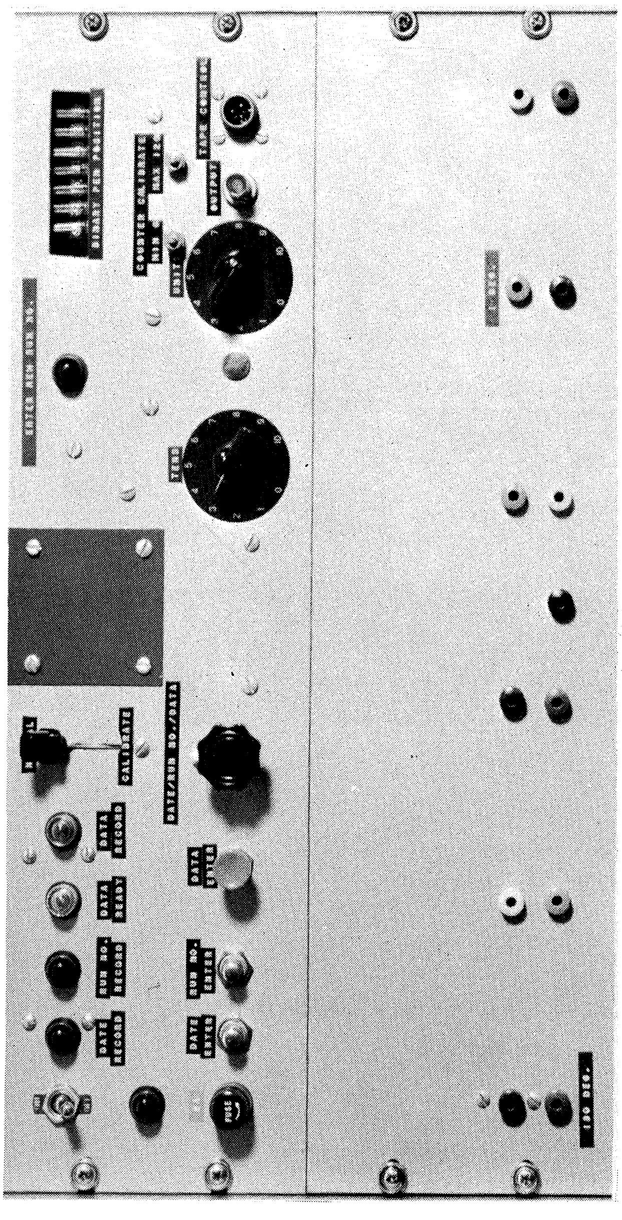


FIG. 13: DIGITAL ANTENNA PATTERN RECORDER CONTROL PANEL

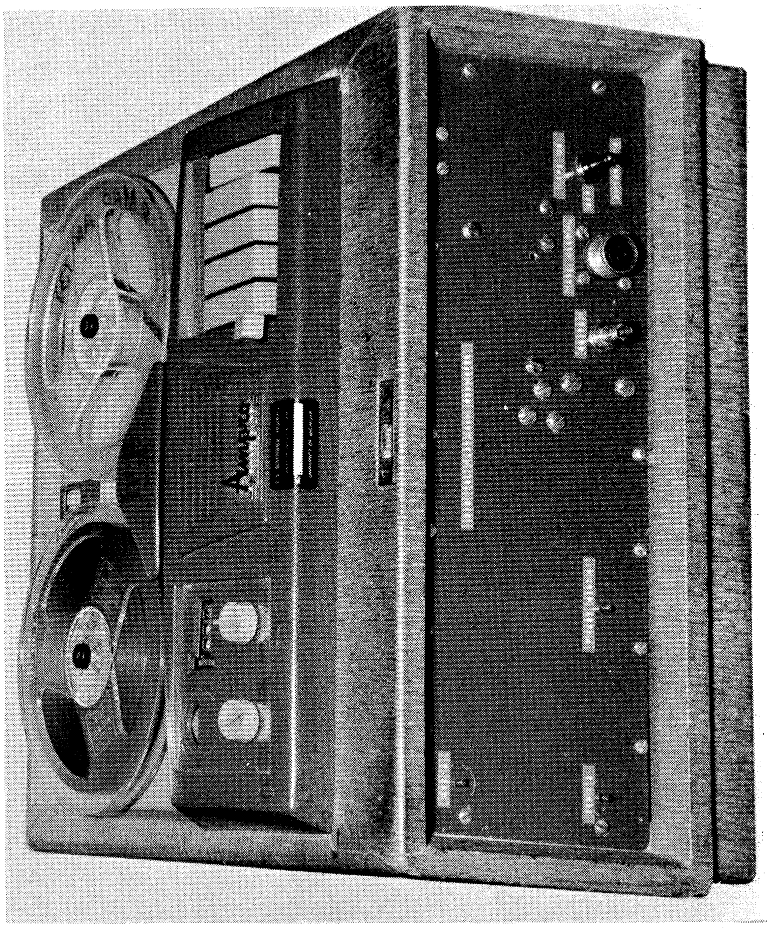


FIG. 14: MODIFIED AMPRO TAPE RECORDER AND PLAYBACK CONTROL PANEL

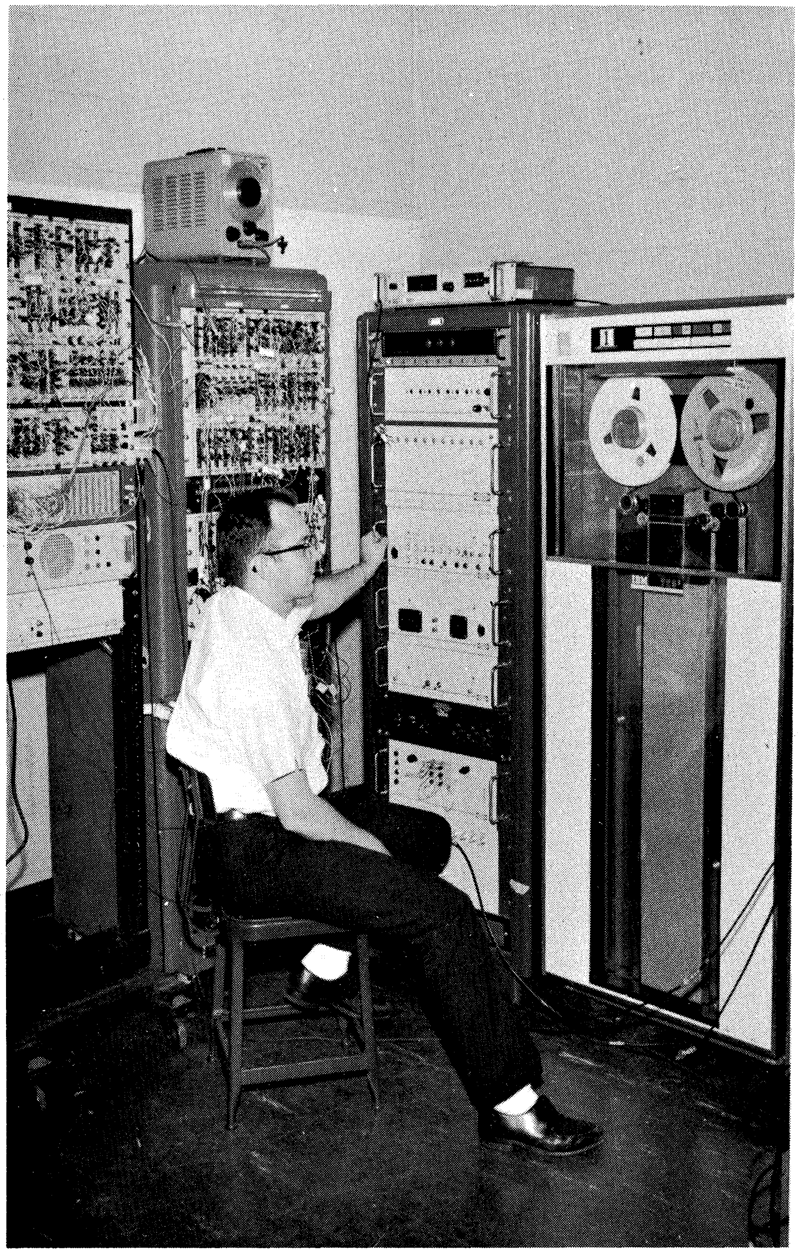


FIG. 15: ANALOG-TO-DIGITAL CONVERTER AND IBM 729 TAPE DECK

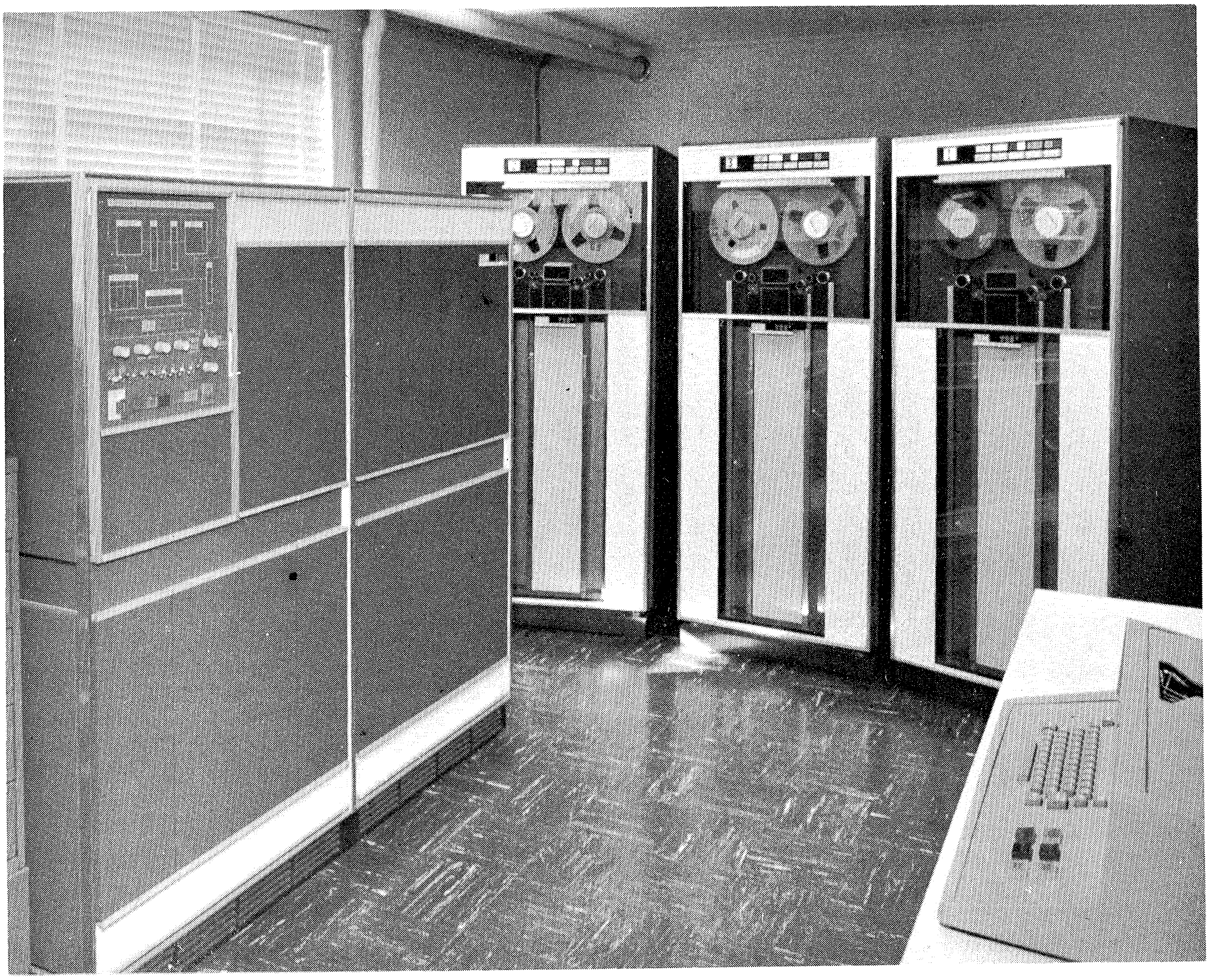


FIG. 16: IBM 1401 DATA PROCESSOR

the 40- and 60-db logarithmic are the most frequently used.

The angular position information is transferred to the digital equipment in the form of pulses derived from photocells, a light source, and two rotating optical gates within the position indicator. Two such inputs are required: the first consists of pulses at one-degree intervals, the second input is a pulse which occurs only at the 180^{o} position.

5.2 Output Format

An output "record" from the digital equipment consists of a group of 12 bi-level pulses, or "bits", -50 millivolts representing a logic "O" and -110 millivolts representing a logic "1". A record consists of a date from 00 to 99, a run number from 00 to 99, or data at one of the sampling points. Two of the record bit positions form an identification code us ed to signify whether the record presents the data, run number, or a data point.

The output pulses have a width of 250 microseconds and are spaced one millisecond apart, corresponding to a frequency of one kilocycle per second. A 1-Kc rate was selected because this frequency is well within the record/playback capabilities of most general-purpose tape recorders. The playback output levels are higher: -6 volts for logic "O", and -12 volts for logic "1", as explained in Section 5.5.

Spacing of records will depend on the rate at which the data is taken, but will never be less than 40 milliseconds. Preceding each twelve-bit record by a nominal time of six milliseconds is a pulse (identical to those representing a logic "1") used for starting the IBM 729 tape deck when transferring the data from the general-purpose quarter-inch tape to the standard half-inch computer tape. The starting time required by the 729 tape deck is approximately three and one-half milliseconds; therefore, this pulse does not appear on the IBM tape.

The entire antenna pattern on either tape consists of 365 records in sequence, called a "file". The file includes the date, run number, and pattern data organized as follows.

5.2.1 Date Format

The first three records of a file representing an antenna pattern will be the date, e.g., 6-1-65. The format of a typical 12-bit date record is shown in Fig. 17. The first bit is always a logic "one", serving as a reference level for the 1401 data processor. The second bit is not used for the date mode, therefore a logic "zero" is placed in that position. The mode code is formed by bit positions 3 and 4; for a date entry the code is 01. The date numbers are placed in the last eight-bit positions: the "tens" digit of a number 00 to 99 is placed in bit positions 5 - 8 in the form of a standard binary number. The most significant bit is in position 5 and the least significant bit is in position 8. The "units" digit is similarly placed in positions 9 - 12 with the most significant bit in position 9 and the least significant bit in position 12. The record shown is that which represents the number "65" of the date.

5.2.2 Run-Number Format

The fourth record of the file is the run number which uses the identical format of the date record with one exception: the mode coding in bit positions 3 and 4 is changed from 01 to 10 to indicate a run number.

5.2.3 Data Format

The data record shown in Fig. 18 employs a slightly different format from either the date or run-number record. The first bit is again a logic "one" reference. The second bit indicates, with a logic "one", the first or last data point. For all other data points, a logic "zero" appears in the second bit position. The mode code in the third and fourth bit positions is 11, representing a data point. A seven-bit binary number which is proportional to the antenna signal level is entered in the last seven-bit positions, with the least significant bit in the twelfth position. Bit position number 5 is not used for data records, so a logic "zero" is entered. Thus, the data record shown represents a data point taken at either the -180^{o} (start) point or the $+180^{o}$ (stop) point and a binary count of 40.

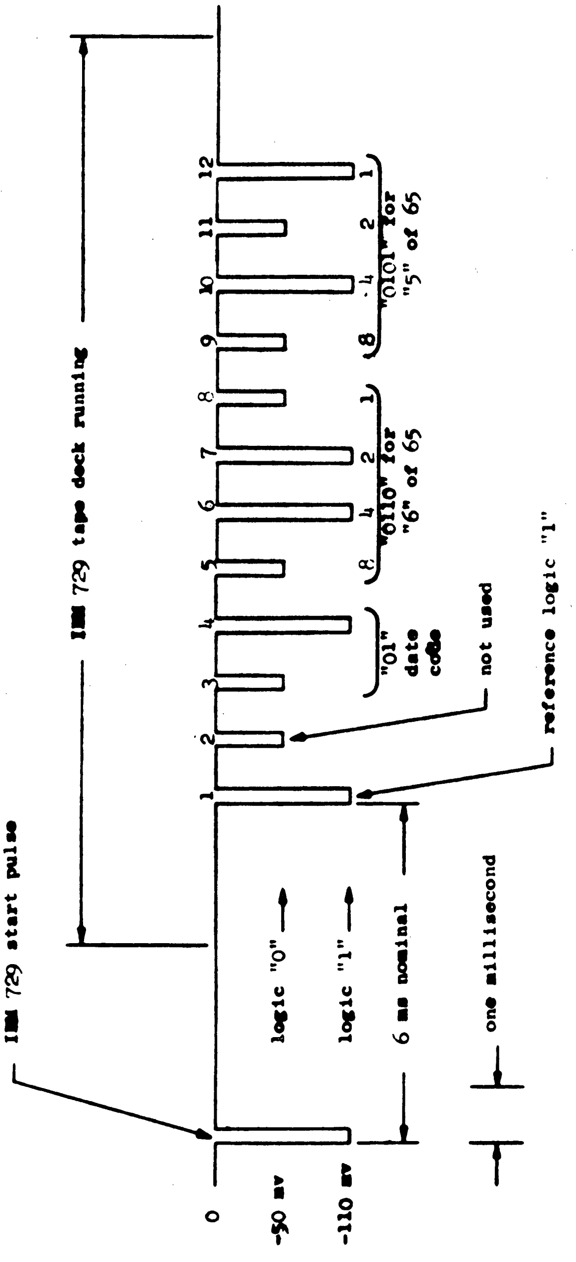


FIG. 17: OUTPUT WAVEFORM FOR A TYPICAL DATE RECORD

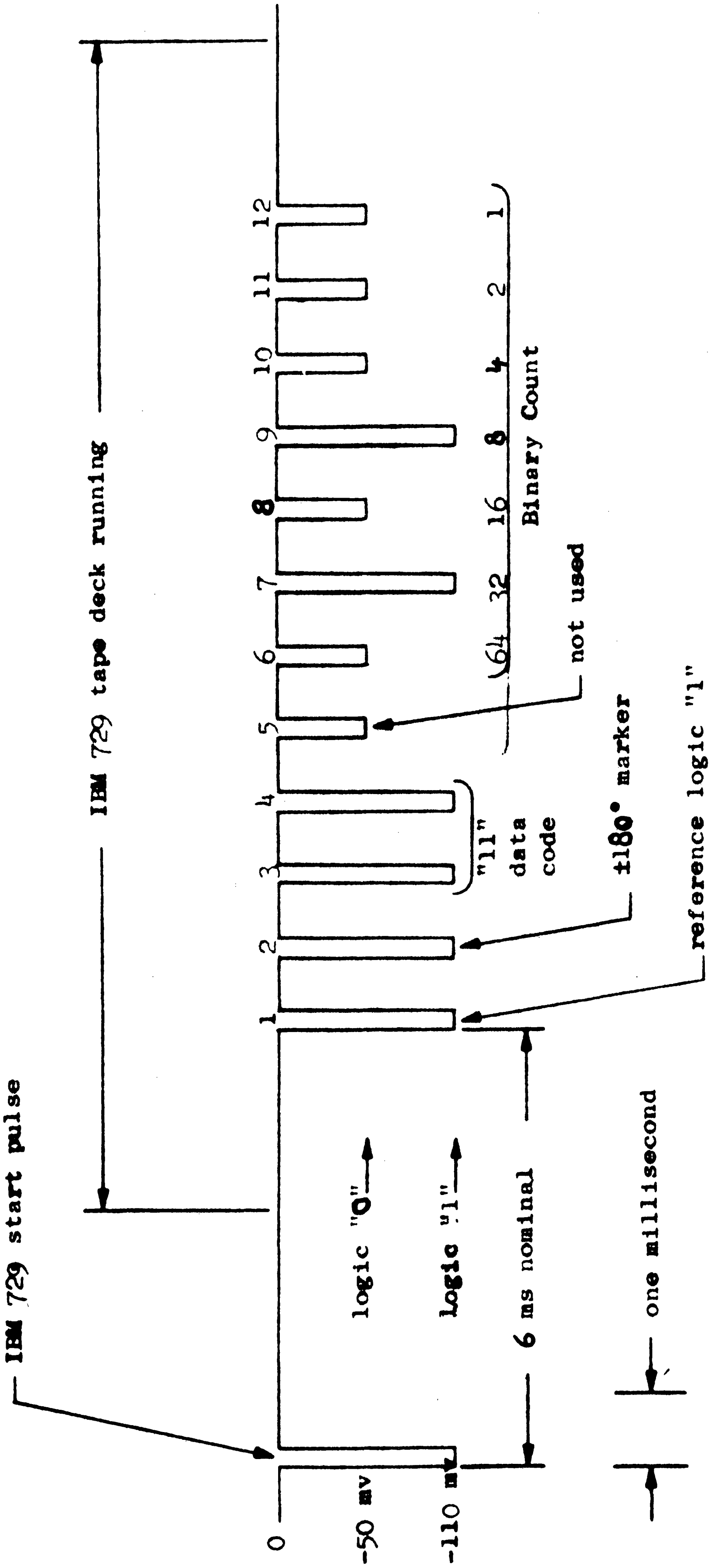


FIG. 18: OUTPUT WAVEFORM FOR ± 180° DATA-POINT RECORD

A total of 361 data points are recorded for one antenna pattern, representing the signal level at one-degree intervals. By counting the number of records between the two 180^o data points, the 1401 data processor can determine if the correct number of data points have been taken. A comparison between the first and last data point, since they should be identical, can provide a cursory check of repeatability.

5.3 System Operation

Figure 19 is a block diagram of the entire system, illustrating the various circuits and their relation to one another. The start signal is channeled through a mode-control circuit which determines the circuits which are active during a particular recording mode.

5.3.1 Date and Run-Number Modes

In either the date or run-number mode, the corresponding "enter" pushbutton sends a signal through the mode-code generator and the date/run number generator to "load" the shift register with the proper logic "zeros" and "ones". At the same time, the tape recorder is started. Then the shift register is read out at a one-kilocycle clock rate. After the record has been clocked out, the tape recorder is stopped and the equipment is ready for another tape entry. The operation of the system is the same for either the date or run-number mode.

5.3.2 Date-Record Mode

The operation of the system in the data mode is different from that of the date or run-number mode previously described. In the data mode the "date record" pushbutton initiates a start signal for the tape recorder as before, but the mode-code generator, the date/run-number generator, and the shift register are inactive at this time. Instead, the signal from the mode-control circuitry is routed to the data control circuits which govern the recording of data. When the control circuits have been enabled by a signal from the mode-control circuitry, the analog-to-digital conversion and recording operations can start when the antenna position indicator

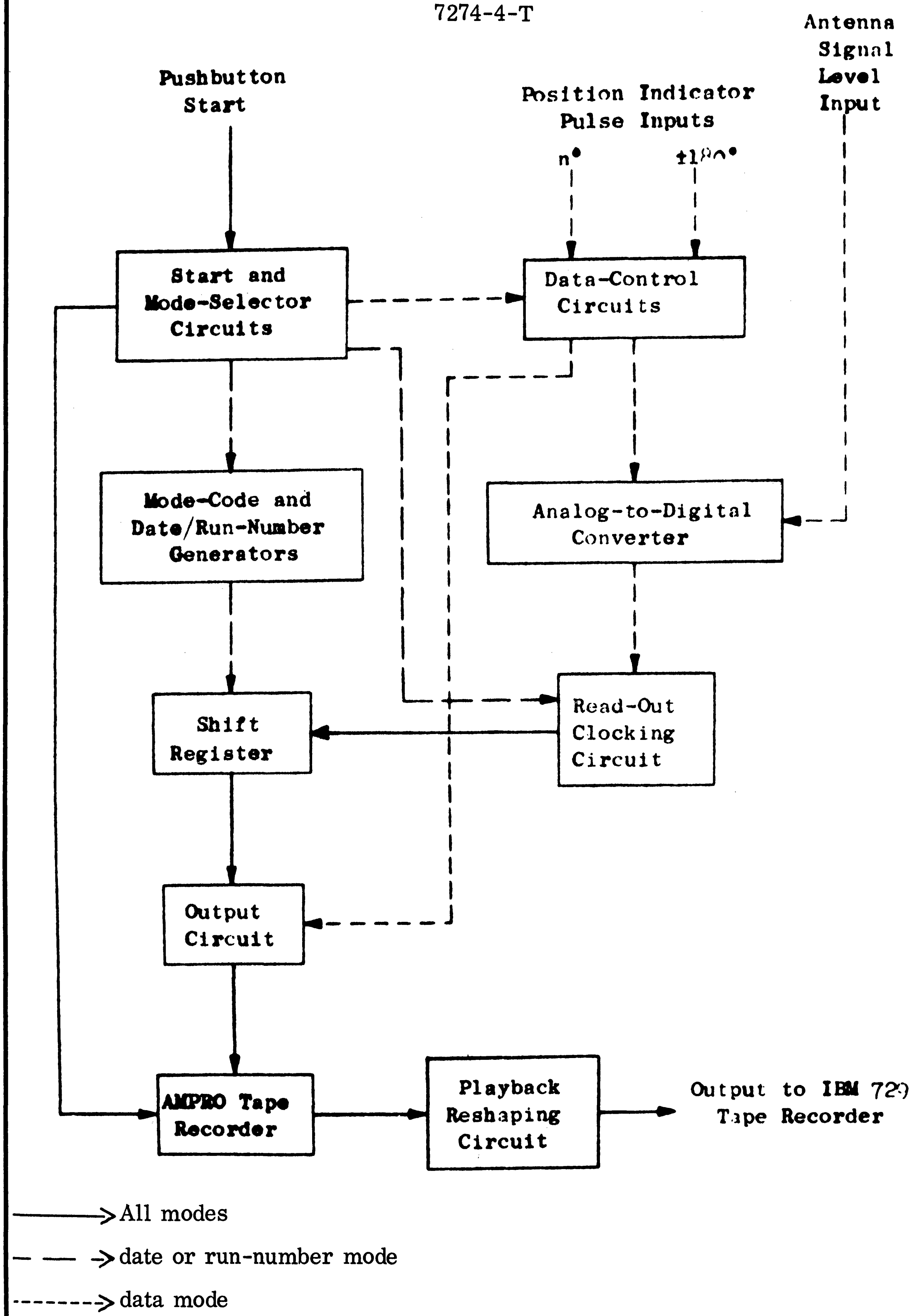


FIG. 19: BLOCK DIAGRAM OF DIGITAL RECORDING/PLAYBACK SYSTEM

reaches the -180^{o} start point. The A/D conversion then proceeds with a binary counter generating a number proportional to the analog input signal. This number is then transferred to the shift register and clocked out, recording the first data point.

Each time an n^{o} pulse appears at the input to the control circuit, a new data point is taken. After the 361st data point, which generates the 365th record on tape, the system stops recording data. The complete file of 365 records is followed by a five-second burst of 500-cps square wave, after which the tape recorder is de-energized. Thus, a complete digitalized antenna pattern has been produced from signals generated with the analog recording system.

The 500-cps tone provides an aural "end of pattern" indication on the quarter-inch tape produced by the above equipment, but is replaced by an "end of file" mark on the final IBM tape.

The system logic is designed so that another data sequence cannot be initiated without first entering a new run number. This feature guarantees the identification of every antenna pattern recorded. The logic does not require repeating the date for each antenna pattern. It can in fact be omitted from even the first pattern recorded. The three-record date is required, however, by the program for the IBM 1401 data process or which reads the half-inch tape to produce IBM cards.

5.4 Detailed Analysis

This section will describe the operation of the system in greater detail to reveal the logic and special-circuit design.

5.4.1 Start and Mode-Selector Circuits

The start and mode-selector circuits are shown in Fig. 20. Depending on the position of the mode switch, the equipment will be set into operation in one of the three previously discussed modes. If the "date enter" button is depressed while the mode selector is in the "date" position, a pulse will be transferred to the SET 1

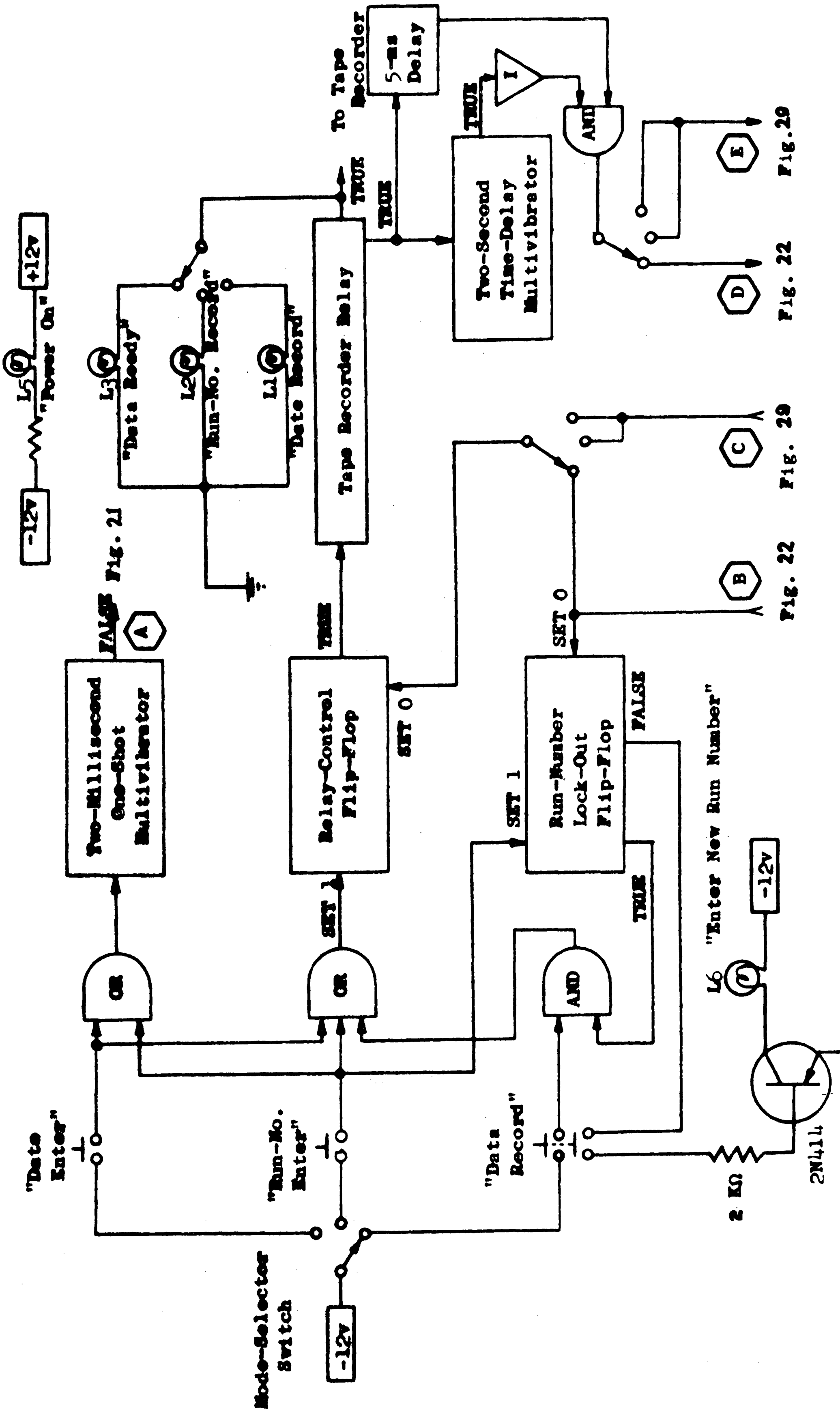


FIG. 20: START AND MODE-SELECTOR CIRCUITS

input of the relay-control flip-flop and to the trigger input of the two millisecond one-shot multivibrator. The "false" output of the one-shot multivibrator serves to load the shift register (Section 5.4.2.7) through the mode-code generator (Section 5.4.1.1) and the date/run number generator (Section 5.4.1.2). Setting the relay-control flip-flop energizes the relay circuit. The contacts of the relay provide a start signal for the tape recorder and a trigger input for the two-second time-delay multivibrator. The two-second time delay allows the tape recorder to attain operating speed before data is recorded.

The rise time of the two-second multivibrator is too poor to trigger succeeding logic elements; a special circuit is needed. The TRUE output of the multivibrator is inverted and applied to an AND gate, along with a "true" signal from the relay, thus producing a "true" signal, after the two-second time delay, at the AND-gate output. The five-millisecond delay is necessary to prevent a premature output. The two-second delayed signal is routed to the input NOR gate of the read-out clocking circuit. The actual clocking operation will be detailed, for the data-record mode, in Section 5.4.2.8.

A pulse from the read-out clocking circuitry is applied to the SET 0 input of the relay control flip-flop after the twelve-bit record has been taped. This de-energizes the relay, stopping the tape recorder. The entire cycle is then repeated twice to record the second and third date numbers.

The run number is recorded next by depressing the "run-number enter" button with the mode selector in the corresponding position. The operation is essentially the same except that the run-number lock-out flip-flop is set in addition to the relay-control flip-flop. It is this lock-out flip-flop which "remembers" the run-number entry, thus allowing the equipment to be operated in the data-record mode next.

The data-record mode is initiated by switching the mode selector to this position and depressing the "data record" button. The resultant pulse will set the relay-control flip-flop through the AND gate which has been opened by the run-number lock-out flip-flop. This starts the tape recorder and the two-second delay multivibrator as in the previous modes. The signal from the output AND gate is then transferred to the SET 1 input of the data-control flip-flop (Section 5.4.2) rather than the clock-out circuit.

5.4.1.1 Mode-Code Generator

The mode-code generator is effected by connecting two sections of the mode selector switch to shift-register inputs 3 and 4, as shown in Fig. 21. The coding is "01" for a data entry, "10" for a run-number entry, or "11" for a data-point entry. A third section of the switch generates the reference logic "one" in the first bit position.

5.4.1.2 Date/Run-Number Generator

A schematic diagram of the date/run-number generator is also shown in Fig. 21. This circuit consists of two four-pole, ten-position rotary switches. These switches generate numbers from 00 to 99 in the form of two 4-bit numbers. The four-bit input for shift-register stages 5 - 8 is obtained from one rotary switch, and represents the "tens" digit of the number selected. Similarly, the input for shift-register stages 9 - 12 is obtained from the second switch, representing the "units" digit.

5.4.2 Data-Control Circuits

The data-control circuits shown in Fig. 22 insure that exactly 361 data points are recorded and that nothing is recorded before the tape recorder has reached operating speed. The control circuits also provide the five-second gating signal for 500 cps end-of-file signal and a reset signal for the start-circuit flip-flop.

When the equipment is operating in the data-record mode, the data-control

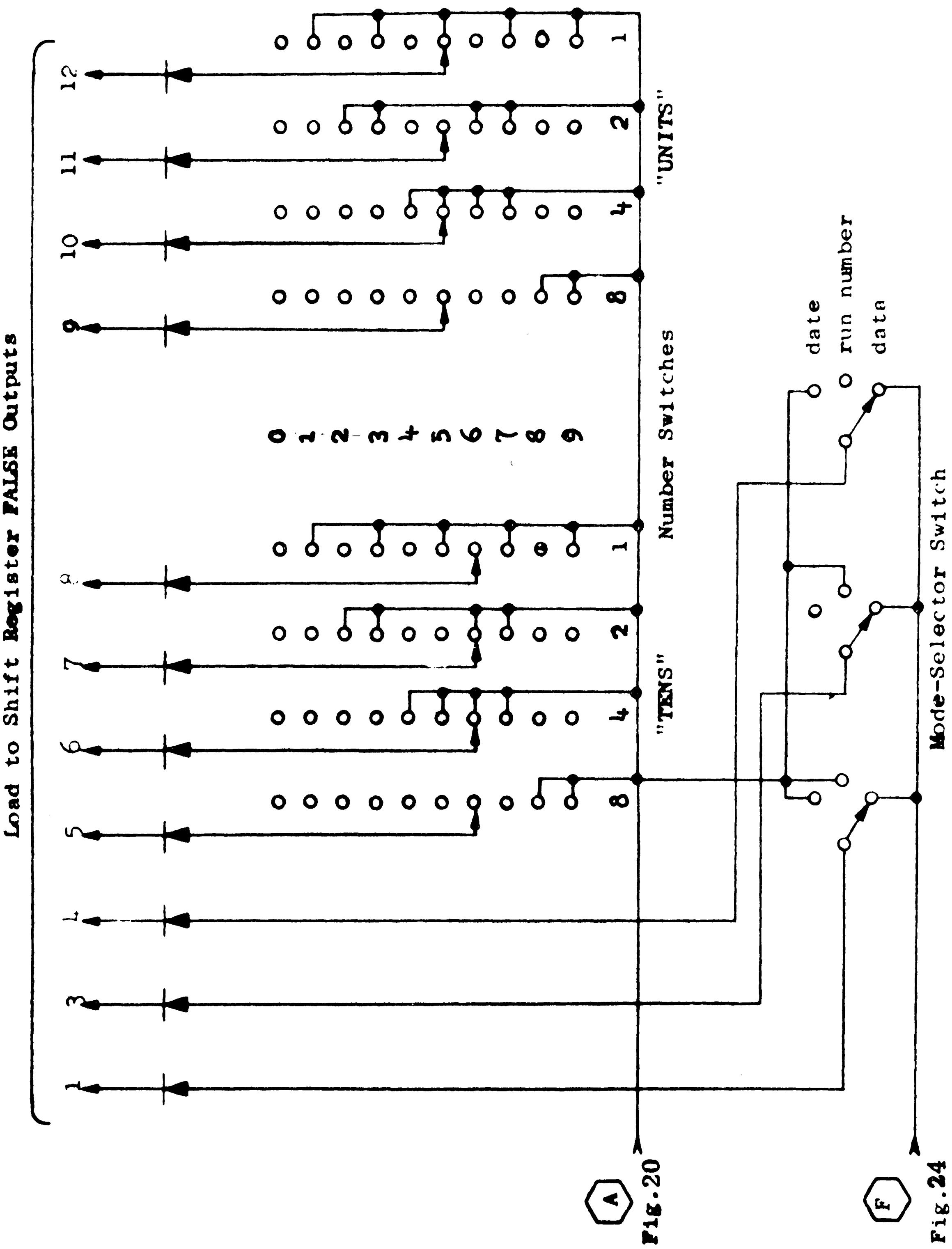


FIG. 21: MODE-CODE AND DATE RUN-NUMBER GENERATORS

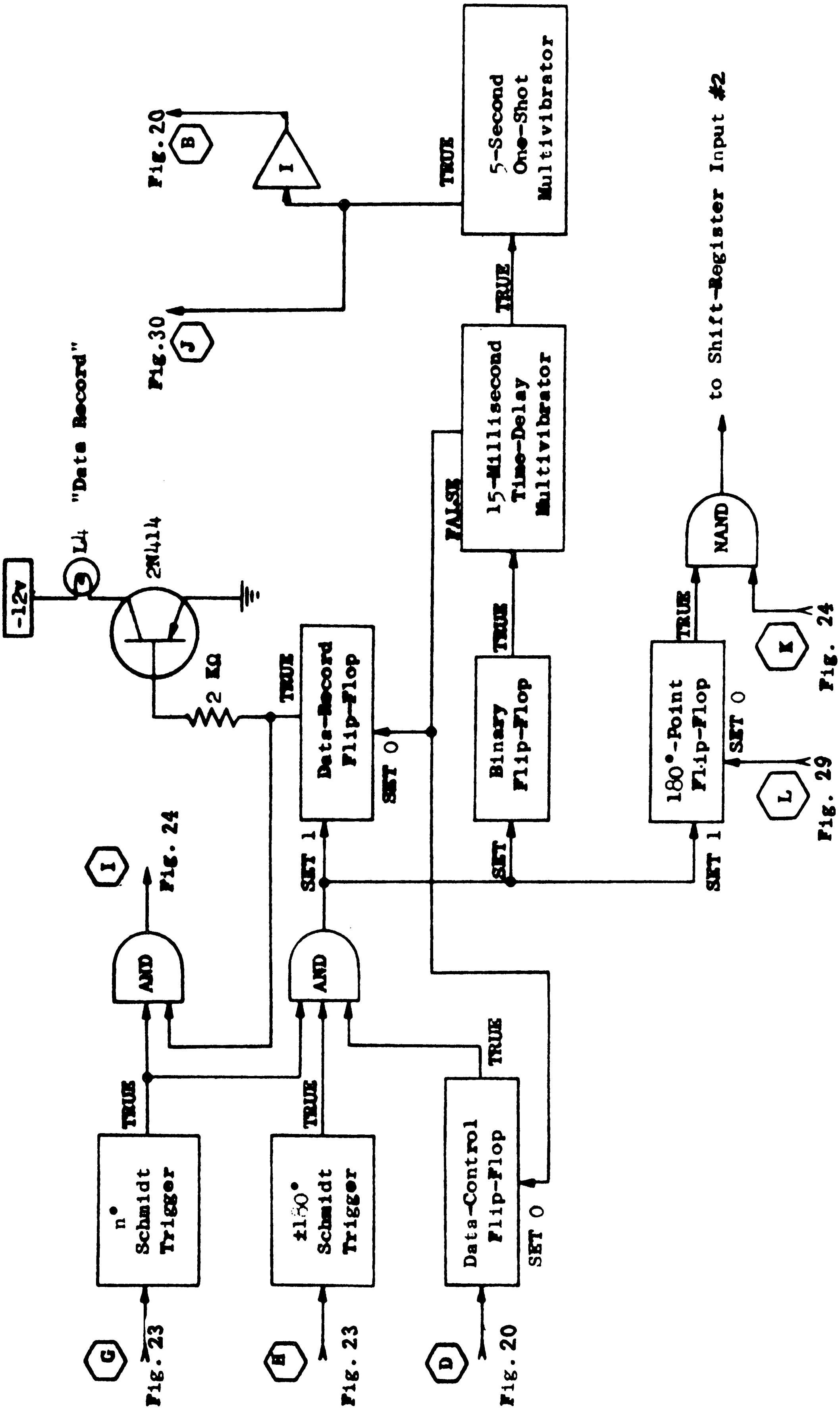


FIG. 22: DATA-CONTROL CIRCUITS

flip-flop is set by the signal from the output AND gate in the start circuit. After the data-control flip-flop has been set, the data-record flip-flop will be set whenever the n^o pulse is accompanied by a 180^o pulse. Both pulses are derived from rotating optical gates between a light source and two photocells within the antenna position indicator (Section 5.4.2.1). The first coincidence of the n^o pulse and the 180^o pulse occurs at the -180^o start position of the position indicator. These pulses are squared by Schmidt triggers and applied to their respective AND gates. When the data-record flip-flop has been set, as indicated by panel lamp L4, the n^o pulses can pass through the second AND gate to drive the analog-to-digital converter circuits (Sections 5.4.2.2 through 5.4.2.6). At the same time the data-record flip-flop is set, the binary flip-flop will also change states.

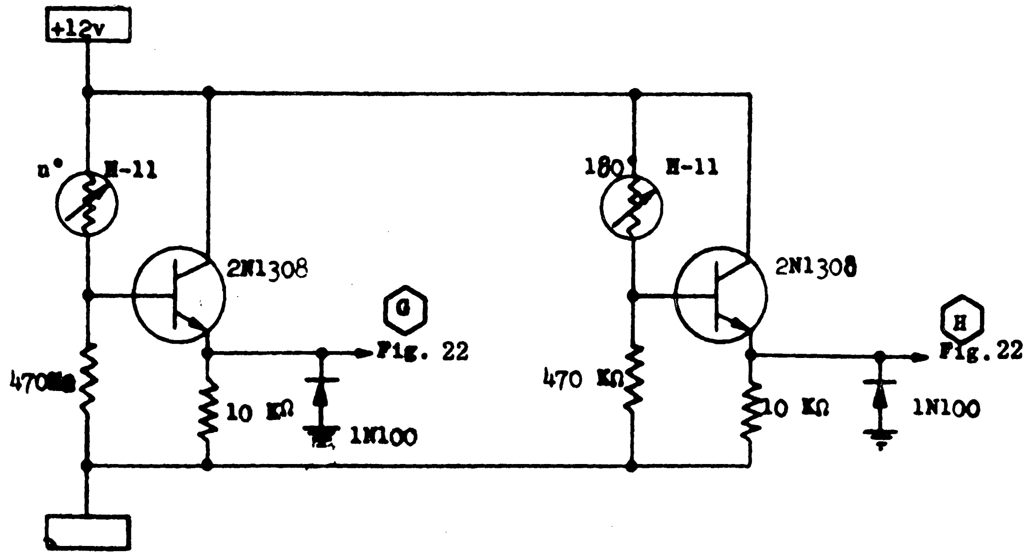
The second time the n^o and $\pm 180^o$ pulses are coincident, which will occur for the 361st data point, or the $+180^o$ stop position of the antenna position indicator, the binary flip-flop will return to its original state and trigger the 15-millisecond time-delay multivibrator. This time delay allows the last data point to be recorded. When the 15-millisecond multivibrator resets itself, the data-control flip-flop and the data record flip-flop will be reset, triggering a five-second one-shot multivibrator which gates the 500-cps end-of-file tone.

After 361 data points have been recorded and the five-second 500-cps note has been placed on the tape to indicate the end of a pattern, a pulse from the five-second time-delay multivibrator is applied to the SET 0 inputs of both the relay-control flip-flop and the run-number lock-out flip-flop in the start circuit (Fig. 20). Thus, the latter has been returned to its original state whereby a new run number must be entered before new data can be recorded. If the "data record" button is depressed while the lock-out flip-flop is in this reset condition panel lamp L6 will be energized since a signal is applied to the base of the lamp driver transistor from the false output terminal of the lock-out flip-flop. This serves as an indication to the operator that a new run number is required. This completes the data-record cycle.

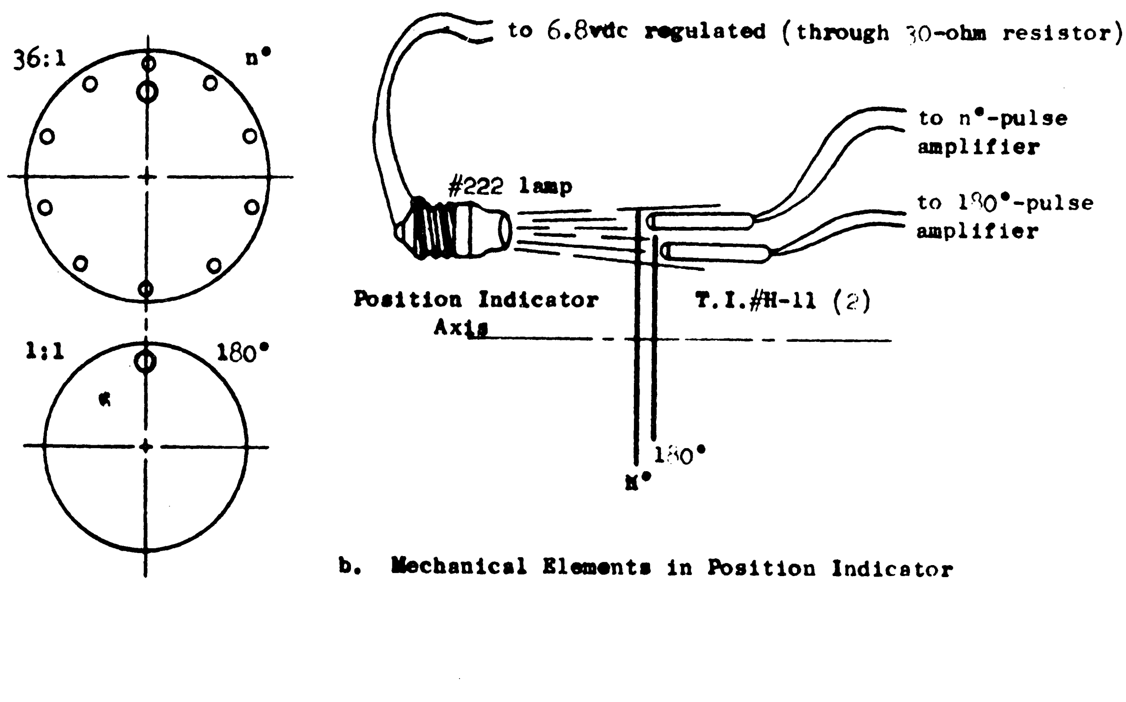
5.4.2.1 Optical Pulse Generator

The n^o and 180^o pulses are generated within the antenna position indicator by a pair of optical gates rotating between a light source and two photocells, shown in Fig. 23a. The indicator contains a dual concentric shaft driven by two synchro receivers electrically "locked" to two synchro transmitters located in the antenna positioner. While one shaft rotates once for each complete rotation of the antenna (positioner), the other shaft rotates thirty-six times or once every ten degrees. A disc is mounted on the latter with ten equally spaced holes near the edge. By placing a light source behind and a photocell in front of this disk, a response is achieved at one-degree intervals. The photocell is connected to the input of a transistor amplifier (see Fig. 23b) located in the antenna positioner controller which houses the position indicator. The n^o pulses are therefore present at the output of the amplifier. Similarly, a second disk (slightly smaller) is placed in front of the first and secured to the other shaft, which rotates once for 360^o rotation of the antenna. A single hole is placed near the edge of this disc at the 180^o position, and a second hole is placed in the corresponding position of the ten-hole disc described above. The two discs form an AND gate which passes a pulse of light to a second photocell and transistor amplifier. Thus, the $\pm 180^o$ pulses are generated.

The $\pm 180^o$ pulses are intentionally made wider, by using larger disc holes than the n^o pulses to guarantee the entry of a logic "one" in bit position 2 of the output signal for the last data point (see Fig. 18). From the logic in Fig. 22, it can be seen that if, for the last data point, the n^o pulse occurs first, the data would be recorded before shift-register stage 2 was loaded by the 180^o point flip-flop. Since the antenna can be driven in either direction, the 180^o pulse is made wider but remains centered with the corresponding n^o pulse. In effect, the 180^o pulse becomes a gating pulse for the n^o pulse which actually triggers the proper circuits.



a. Amplifiers in Positioner Controller



b. Mechanical Elements in Position Indicator

FIG. 23: OPTICAL PULSE GENERATOR

5.4.2.2 Binary Counter

For each n^o pulse emitted by the optical pulse generator, a binary-coded number is produced by the analog-to-digital converter shown in Fig. 24. Each number corresponds to the antenna signal strength at some angular position. The function of each section of the analog-to-digital converter will now be detailed for a single data point.

Once the data-record flip-flop in the data-control circuit has been set, an n^o pulse from the Schmidt trigger will pass through the corresponding AND gate, setting the binary-counter flip-flop. This flip-flop opens a second AND gate which allows the 100-kcs clock signal to drive the seven-stage binary counter. The binary output count begins at zero and increases linearly with time. The "true" outputs of the seven stages are connected to the input of a digital-to-analog converter detailed in the next section.

5.4.2.3 Digital-To-Analog Converter

The digital-to-analog converter is a standard resistive ladder network consisting of 10K-ohm and 20K-ohm, 1 percent resistors. A schematic of this network is shown in Fig. 25. The most significant bit (MSB) is the input closest to the signal output. For maximum stability, the input voltages from the binary counter stages are clamped, by means of 1N4009 diodes, to the -10 volt regulated supply.

The output of the D/A converter is a stair-step signal proportional to the count in the binary counter. The voltage is initially "zero" and increases in a negative direction with the increasing count of the binary counter. The signal is summed with the signal input from the analog antenna pattern recording equipment by the comparator amplifier.

5.4.2.4 Comparator

The comparator circuit, shown in Fig. 26, consists of two amplifiers in a summing arrangement. Each consists of a complementary pair of transistors (NPN

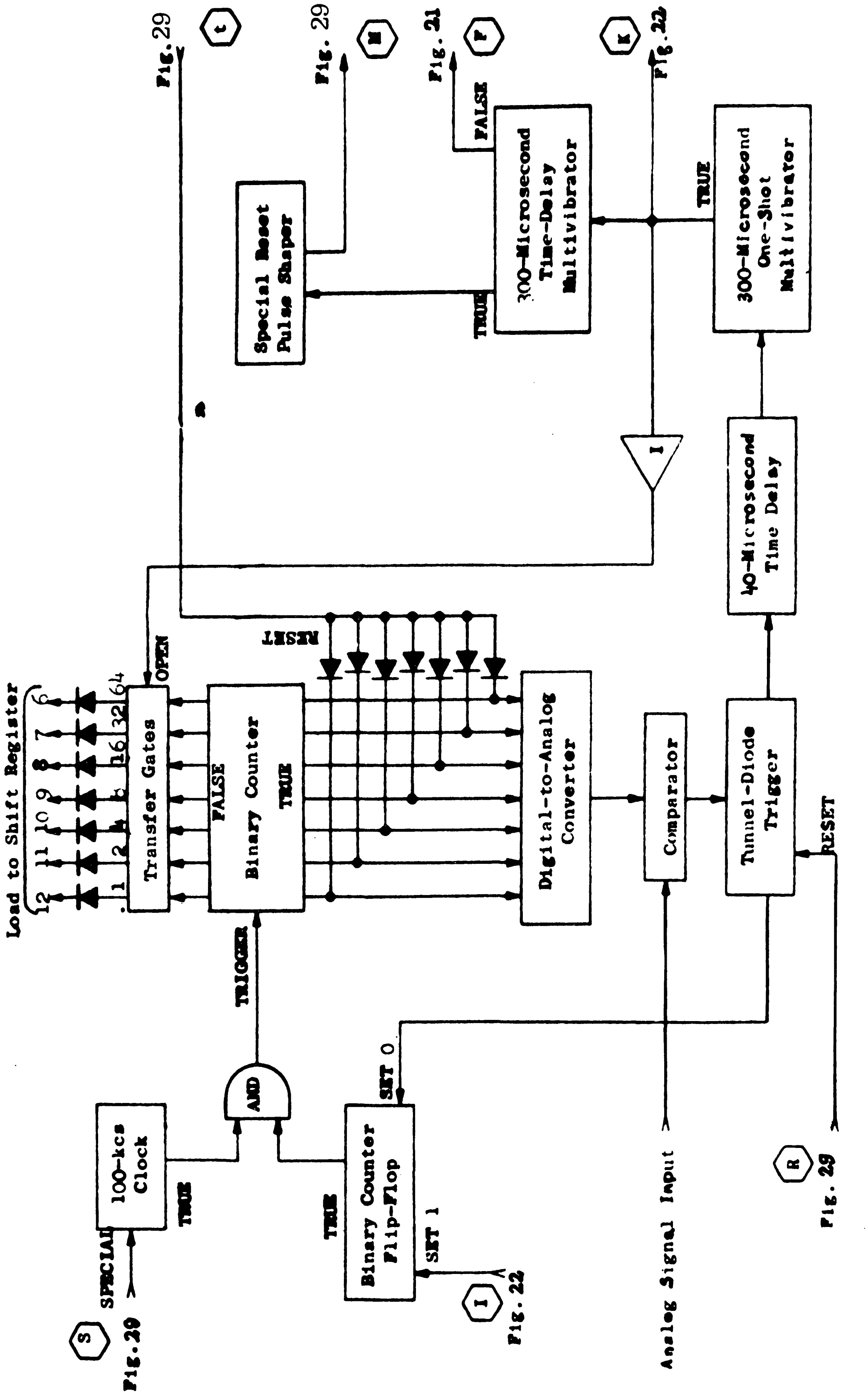


FIG. 24: ANALOG-TO-DIGITAL CONVERTER

Note: All resistors 1% tolerance.

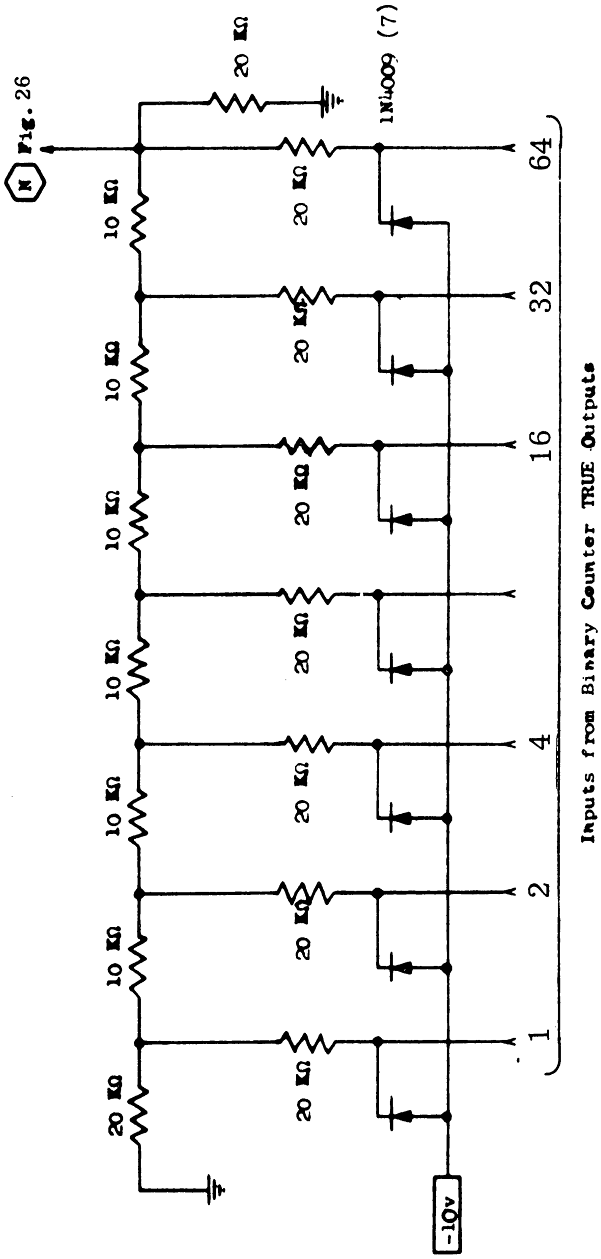


FIG. 25: DIGITAL-TO-ANALOG CONVERTER

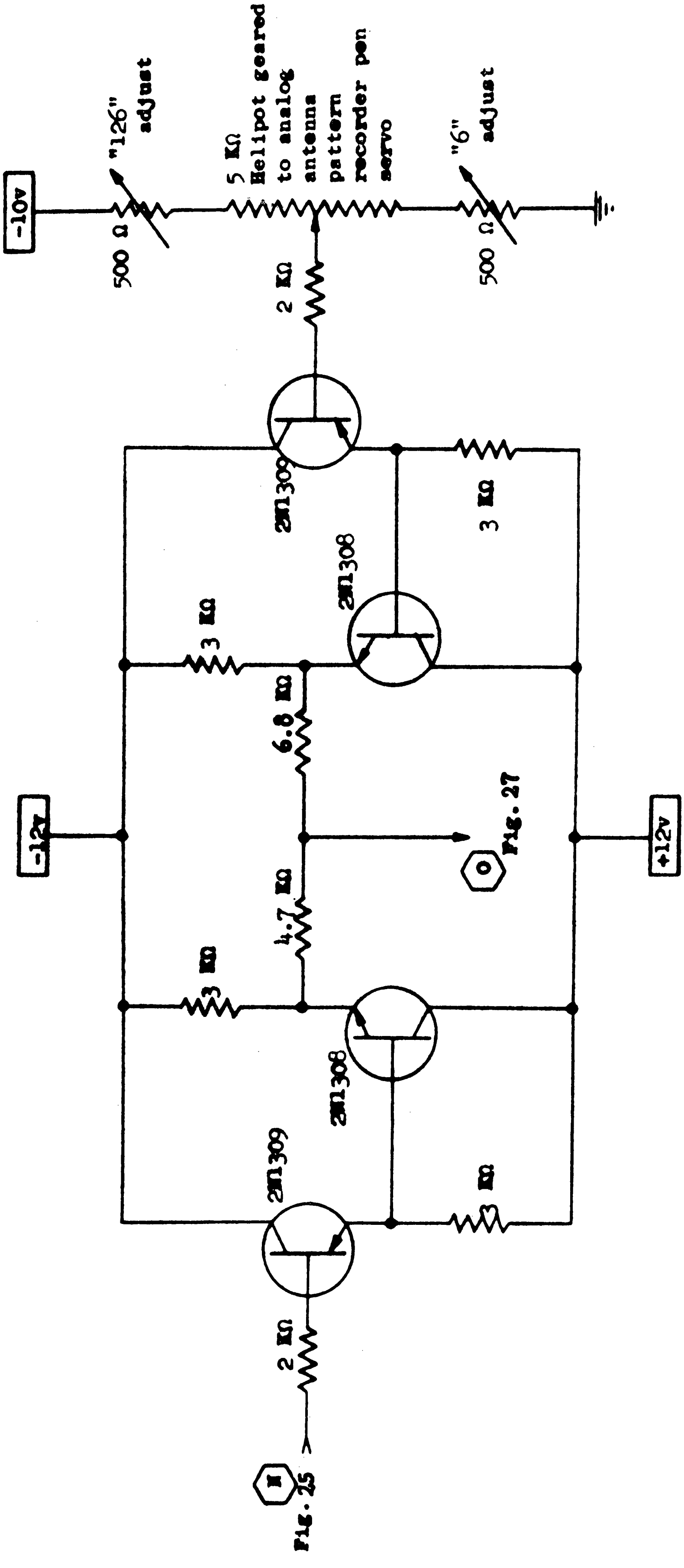


FIG. 26: COMPARATOR

and PNP) in an emitter-follower configuration. The output of the circuit is taken from the junction of the 4.7K ohm and the 6.8K ohm resistors.

The signal input from the recorder is a positive voltage proportional to the pen deflection, while the input voltage from the D/A converter is zero prior to a binary counting operation. The voltage appearing at the output junction is positive due to the input from the recorder. After the binary counter is triggered into operation, the input from the D/A converter increases in a negative direction. The positive voltage at the output junction decreases as the binary counter continues. When the output voltage reaches zero, the zero crossing is detected by the TD trigger circuit.

5.4.2.5 Tunnel-Diode Trigger

The tunnel-diode trigger circuit, shown in Fig. 27, consists of a pair of 2N1991 transistors (Q_1 and Q_2) in a differential-amplifier configuration, and a tunnel-diode trigger consisting of a 1N3713 (1-ma tunnel diode) and a 2N1308 transistor. When the input to the circuit is positive, prior to the binary counting operation, Q_2 is conducting and Q_1 cut off. When the input crosses the zero axis, Q_1 is driven into saturation, turning off Q_2, and the tunnel diode is driven beyond the 1-ma trigger level. Transistor Q_3 is quickly turned on and the collector output voltage changes from a few millivolts negative to -10 volts. This output is applied to the "reset" input of the binary counter control flip-flop, freezing the count. The 0.02-mfd capacitor prevents the high-frequency spikes that are generated in the counting operation from prematurely triggering the tunnel-diode circuit.

5.4.2.6 Analog-To-Digital Converter Calibration

Having seven stages, the counting range of the binary counter is from 0 to 127. As a matter of good practice, extreme counts are avoided in this particular system. A range from 6 to 126 has been experimentally determined as optimum for this equipment from the standpoint of stability and linearity. The range of 120 steps was selected for its convenience when using 40-db or 60-db logarithmic analog recorder chart scales.

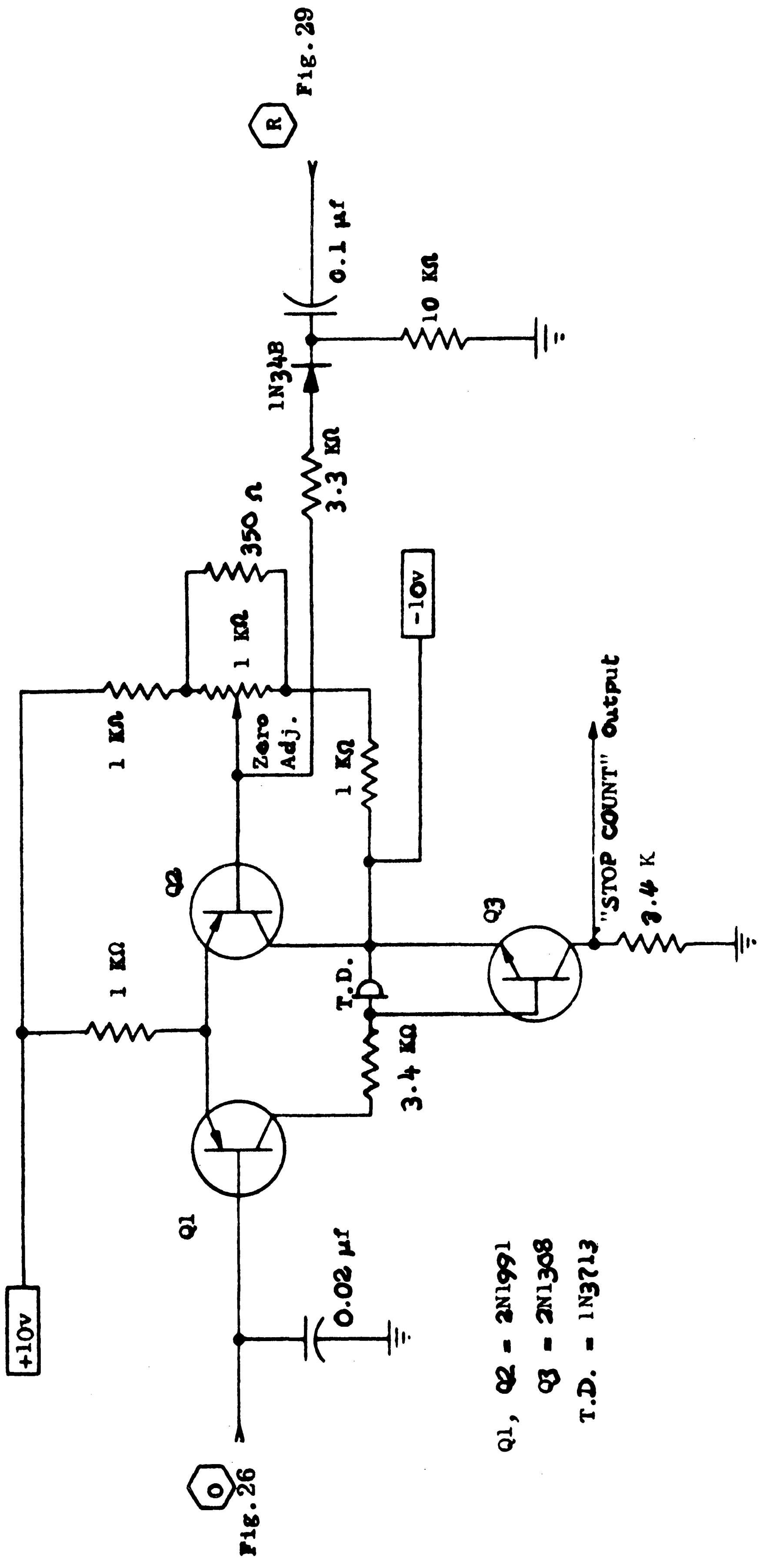


FIG. 27: TUNNEL-DIODE TRIGGER

To facilitate calibration of the binary counter, a pair of miniature potentiometers are located on the front panel of the analog-to-digital converter (see Fig. 13). These potentiometers are connected in series with the potentiometer in the analog antenna pattern recorder, as shown in Fig. 26. The lower potentiometer is adjusted to yield a count of 6 when the recorder pen is manually placed at the lower limit of the chart scale. Similarly, the upper potentiometer is set for a count of 126 when the pen is placed at the upper limit of the chart scale. A sample count can be displayed with the seven indicator lights on the front panel. This is effected by depressing the "calibrate" level switch, which generates a "dummy" n^o pulse and holds the binary count for display.

5.4.2.7 Shift Register

The shift register used in this equipment consists of three standard Wyle logic cards. Each card contains four stages, making a total of twelve to compose the shift register. These stages are interconnected in the usual manner, as shown in Fig. 28. This circuit employs a unique method of parallel loading which is worth mentioning.

The loading operation is accomplished by momentarily grounding the "false" outputs of the appropriate stages, which are at -12 volts in the reset position. This forces the corresponding "true" outputs to turn on, thus setting "ones" into the desired shift-register stages. This is accomplished in the date or run-number modes with the two-millisecond pulse from the one-shot multivibrator (Section 5.4.1). In the data-record mode, the shift register is loaded by a 300-microsecond "data-transfer" pulse from the analog-to-digital converter (explained below). Isolating diodes are used so that the circuits do not interact with each other.

When the binary counter is halted by the TD trigger, the count remaining is proportional to the magnitude of the analog signal input. This digital number is then transferred to the tape recorder by the remainder of the circuits in the analog-to-

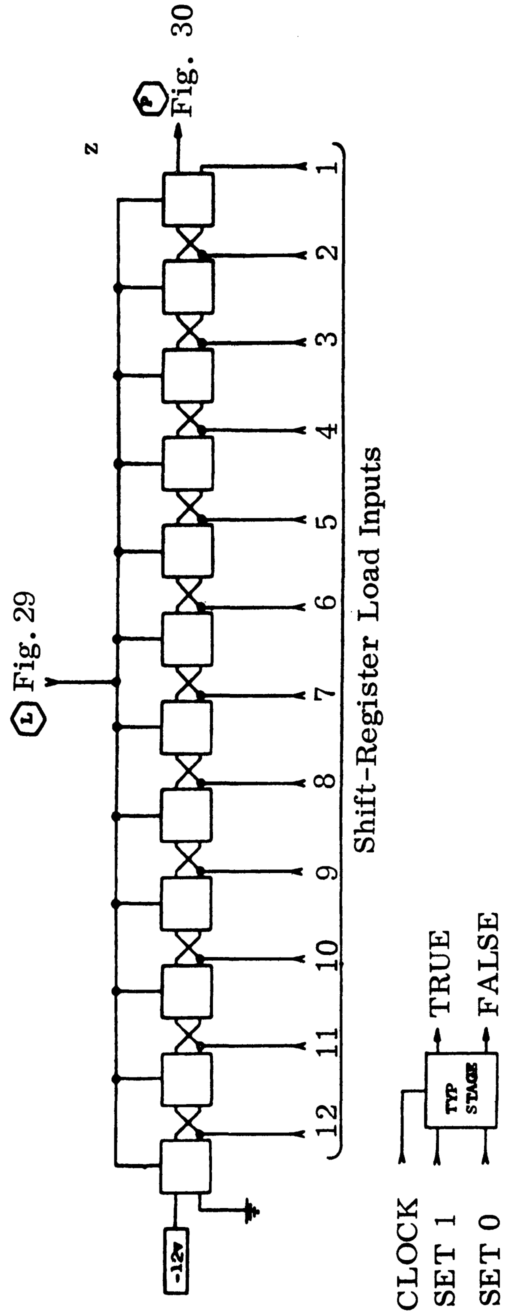


FIG. 28: SHIFT REGISTER

digital converter (see Fig. 24). A 40-microsecond time delay is initiated to allow the counter to stabilize before proceeding. The delayed signal then triggers a 300-microsecond one-shot multivibrator. The TRUE output from the multivibrator is applied through an inverter to the seven transfer gates, thus loading shift-register stages 6 - 12 with the count from the binary counter. The TRUE output also loads a logic "one" into the second stage, if the data point is the first or last ($\pm 180^o$). The 300-microsecond pulse opens an AND gate, connected to the input of shift-register stage 2, which passes the signal from the 180^o point flip-flop in the data-control circuits (Fig. 22).

When the 300-microsecond one-shot multivibrator returns to its original state, a pulse is generated to initiate a 300-microsecond time-delay. The delayed TRUE output is applied to a special reset circuit which generates a 600-microsecond "true" pulse after the 300-microsecond time delay. The delayed FALSE output loads shift-register stages 1, 3, and 4 through the mode-code generator (Section 5.4.1.1). The reference logic "one" is loaded into the first stage; the third and fourth stages receive a logic "one" to indicate the data code.

The 600-microsecond pulse from the special reset circuit is inverted by the NOR gate and applied through isolating diodes to the TRUE outputs of the binary counter, thus resetting the latter for the next data point. At the same time, this "false" pulse is inverted again and applied to the SET 1 input of the timing flip-flop in the read-out clocking circuit.

An alternate input to the NOR gate is the "true" signal from the output AND gate in the start circuit (Fig. 20), which resets the counter prior to read-out clocking during the date and run-number modes to insure starting, with a zero count for the first data point.

5.4.2.8 Read-Out Clocking

The circuit used for read-out clocking is shown in Fig. 29. This circuit pro-

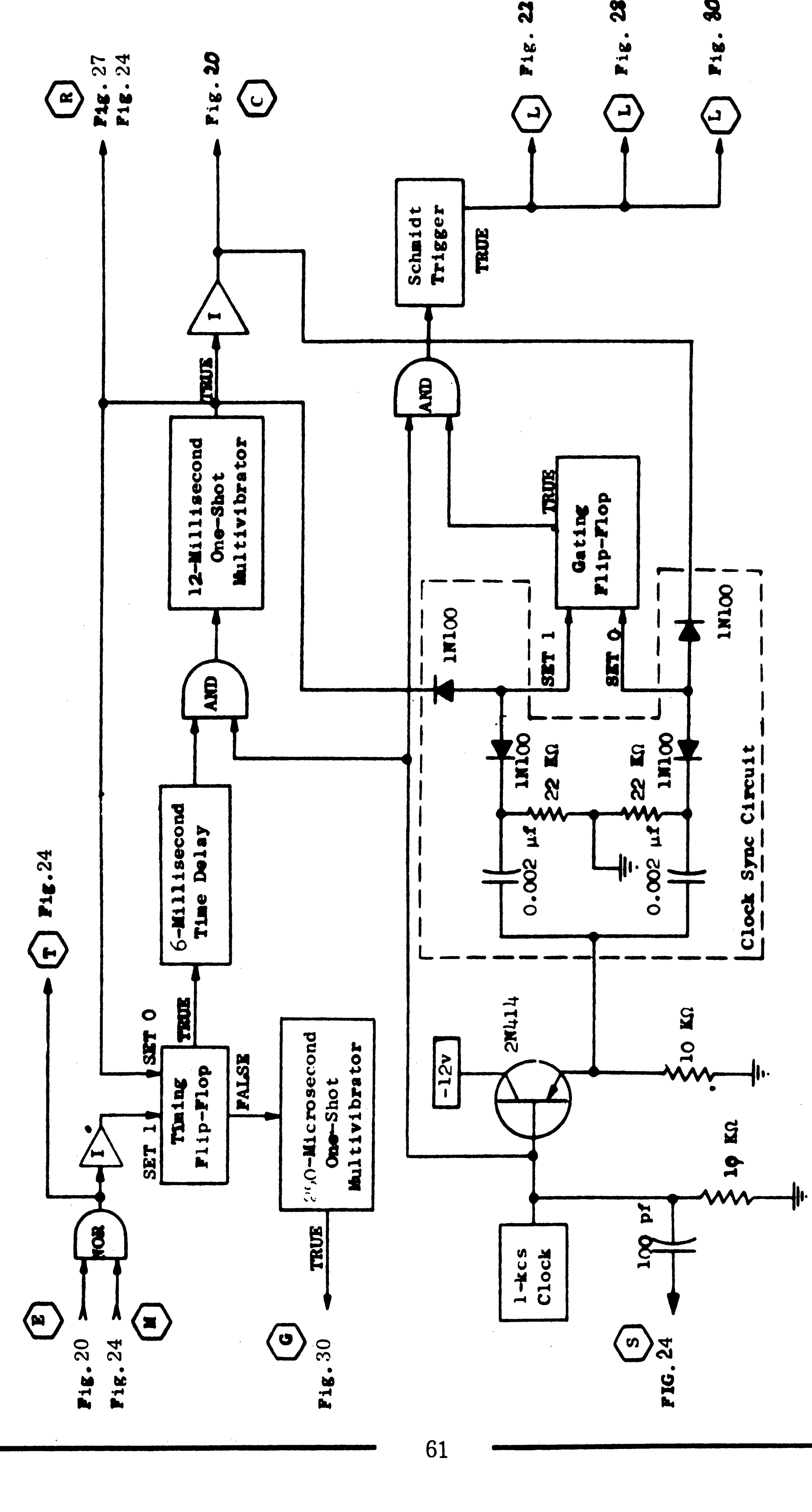


FIG. 29: READ-OUT CLOCKING CIRCUIT

vides a 12-pulse train to the clock input of the shift register. The twelve pulses cause the shift-register load (twelve bits) to appear serially at the output of the first shift-register stage. This bilevel signal (Ov for logic "O", -12v for logic "1") is routed to the output circuit described in the next section. After this read-out operation, the shift-register load consists of twelve logic "zeros" hence it is ready for the next data point.

The read-out clocking must be more complex than simply a one-shot multivibrator controlling an AND gate for the appropriate length of time. The complexity is required to insure that the clock is turned on or turned off between pulses so that the shift register receives twelve full pulses. In the normal (reset) state, the output of the 12-millisecond one-shot multivibrator is zero and the output of the inverter circuit is -12 volts. The output of the clock is a one-kilocycle square wave which alternates between zero and -12 volts. With these voltages applied to the clock-synchronizing circuit, consisting of two differentiating networks and four gating diodes, the differentiated clock pulses are continually applied to the SET 0 input of the gating flip-flop.

There are two ways in which this circuit can be activated. In either the date mode or the run-number mode, the "true" signal produced by the output AND gate in the start circuit is applied to the input NOR gate, indicating that the date or run number has been loaded into the shift register. In the data mode, a 600-microsecond pulse comes from the special reset circuit in the analog-to-digital converter, indicating that the binary count has been transferred to the shift register. Either input sets the timing flip-flop, which in turn activates a six-millisecond tunnel-diode time delay. The purpose of the latter circuit is to delay the actual clock-out operation long enough for the IBM 729 tape deck to reach operating speed when transferring data from the original quarter-inch tape to half-inch IBM tape. The starting pulse (see Fig. 17 or 18) is generated by a 250-microsecond one-shot multivibrator triggered by the FALSE output from the timing flip-flop, and is connected directly into the output circuit (see Section 5.4.2.9).

After the six milliseconds the tunnel diode fires, applying an input to the AND gate. If the clock is "on" at this moment, the 12-millisecond one-shot multivibrator will immediately switch over to the "set" condition. If the clock is "off", the multivibrator will be set when the clock comes on. When the one-shot multivibrator changes states, the TRUE output resets the tunnel-diode trigger for the next counting operation. The output of the multivibrator will be -12 volts and the output of the inverter will be zero. The differentiated clock pulses in the clock synchronizing circuit are then diverted from the SET 0 input to the SET 1 input of the gating flip-flop. The gating flip-flop will change states at the next moment when the clock wave form is negative-going. The gating flip-flop will apply a signal to the AND gate causing clock pulses to occur at the output.

After 12 milliseconds have passed, the one-shot multivibrator will return to its original state. The differentiated clock pulses will be rechanneled into the SET 0 input of the gating flip-flop, which will turn off at the next moment when the clock is negative-going, and the clock pulses will cease to appear at the output. Thus, the purpose of the timing flip-flop is to allow exactly twelve-clock pulses to be produced by synchronizing the gating flip-flop with the clock.

5.4.2.9 Output Circuit

The output circuit shown in Fig. 30 performs two distinct functions. The first is that of level-shifting in which the bilevel output of the shift register is converted to a trilevel system where a logic "0" is represented by -5 volts and a logic "1" is represented by -11 volts. The absence of a signal is represented by zero voltage. The other portion of the output circuit serves as a combination OR gate and emitter follower circuit (two 2N414's) that combines the shift-register output and the 500-cps multivibrator signal at a common output terminal. The system logic is designed so that these signals cannot occur simultaneously.

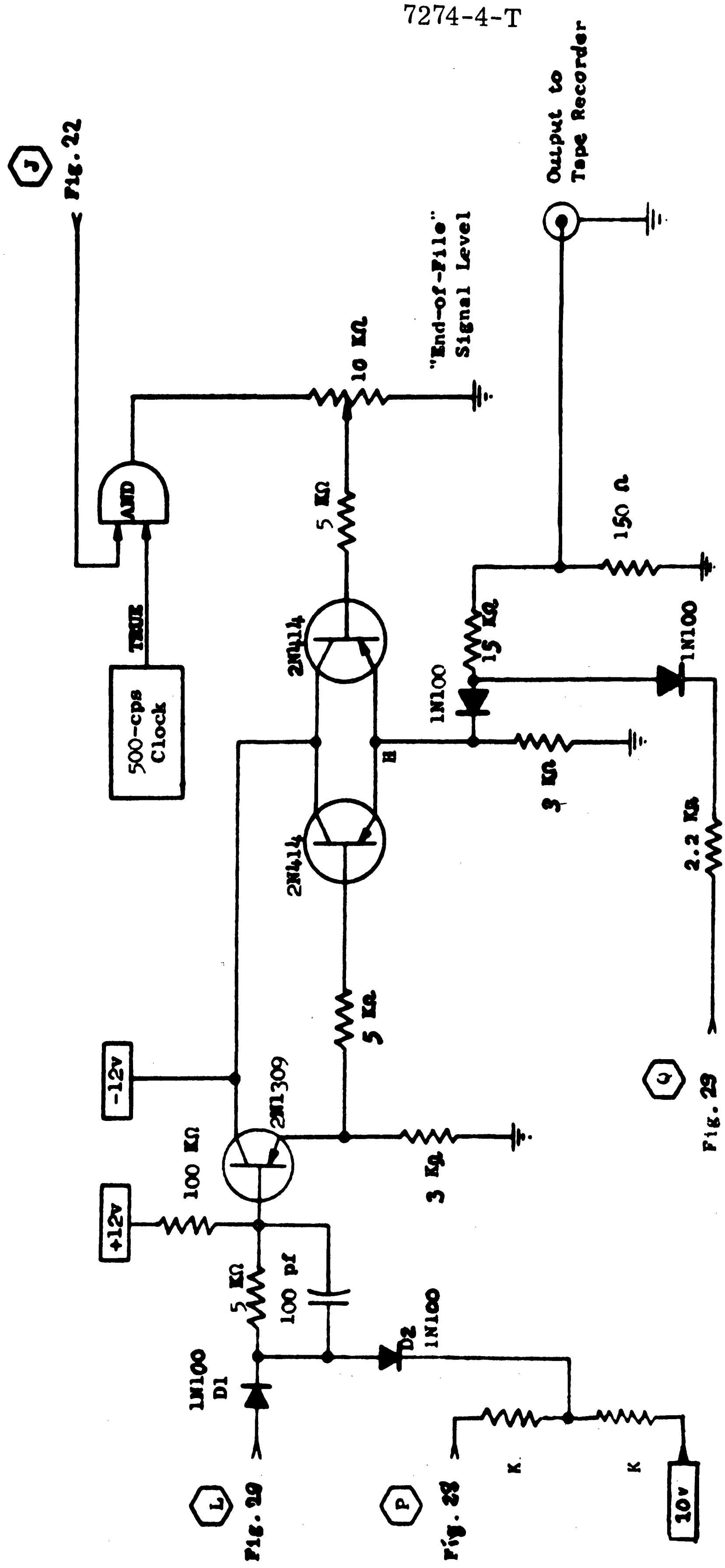


FIG. 30: OUTPUT CIRCUIT

The operation of the level-shift circuit is as follows. The level-shift circuit has two inputs, one from the gated 1-kcs clock signal and the other from the shift-register output. When both signals are at zero, the base voltage of the 2N1309 transistor is clamped to -5 volts by the two 3K-ohm resistors and diode D2. This causes a -5 volt signal to appear at the emitter of the 2N1309, the base of one 2N414, and at terminal H. The voltage at the output connector will be -50 millivolts. When the shift register output is -12 volts, indicating a logic "1", the voltage on the base of the 2N1309 transistor is -11 volts because D2 is now reverse biased. The voltage at the emitter of the 2N1309, the base of the 2N414, and terminal H then becomes -11 volts. The voltage at the output connector will be -110 millivolts.

After the data recording is completed, a signal is supplied to the AND gate from the data-control circuit allowing the 500-cps multivibrator signal to pass through the OR gate to the output. The level of the 500-cps tone at the output connector is adjusted to -25 millivolts by means of the 10K-ohm trimpot so that this signal will not trigger the Schmidt triggers at the input of the playback-reshaping circuit detailed in the next section.

5.5 Tape Recording and Playback

The AMPRO Model 758 "Hi-Fi" tape recorder has been modified for use in this digital recording system. Standard quarter-inch magnetic tape is used on this machine at a speed of 7.5 inches per second.

The signals from the output circuit described above are applied to the "microphone" input of the recorder through a differentiating network as explained below. The volume and tone controls should be set so that the playback-reshaping circuit described below can best differentiate between logic "zeros" and "ones". A four-ohm speaker should be connected to the output of the recorder when "playing" tapes into the IBM 729 tape deck. First, this allows the operator to monitor the individual records which produce short "beeps" and to listen for the 500-cps "end-of-file" signals. Second, the speaker load minimizes distortion because the output stage of the recorder is matched.

Consider now the final output of the converter as shown in Fig. 18. Note that while the DC level during silent periods is zero, there is a nonzero DC level present with an output pulse train representing encoded data. From the beginning of the twelve-pulse train to the end, the "DC level" may vary from one eighth to one quarter of the peak amplitude, depending on the position and number of logic zeros and ones. The fact that there is any DC component input to the recorder renders the recording amplifier unstable, because the amplifier stages are AC coupled. Hence, a low frequency "ringing" occurs (the frequency depends on the time constants of the interstage coupling networks) which is superimposed on the true signal waveform upon playback. This effect, in addition to the inherent phase distortion in an AM magnetic recording process, causes the digital-data waveform to become distorted as shown in Fig. 31. To maintain consistency when the recorded data is converted into IBM format, a circuit is necessary to restore the original waveshape.

A block diagram of the circuit developed to reshape the playback waveform is illustrated in Fig. 32. Two Schmidt triggers are us ed to detect the presence of each logic "1" or "0". The logic "0" Schmidt trigger is set to always detect a pulse, whereas the logic "1" Schmidt trigger fires only when that pulse is a "1". If the input pulse is a logic "1", both Schmidt triggers fire, producing an output pulse whose width is determined by the 250-microsecond one-shot multivibrator. If the input pulse is a logic "0", only the corresponding Schmidt trigger responds. The output pulse in this case will have half the amplitude of that for a logic "1" due to the voltage divider at the output.

Since the waveshape from the playback amplifier has a finite risetime, the 80-microsecond time-delay multivibrator is needed to eliminate a "front-porch" on the

Bits No. 1, 2, 3, 4, 7, and 9 are logic "ones "1 bits No. 5, 6, 8, 10, 11, and 12 are logic "zeros".
Note low-frequency "finging" which masks instantaneous levels.

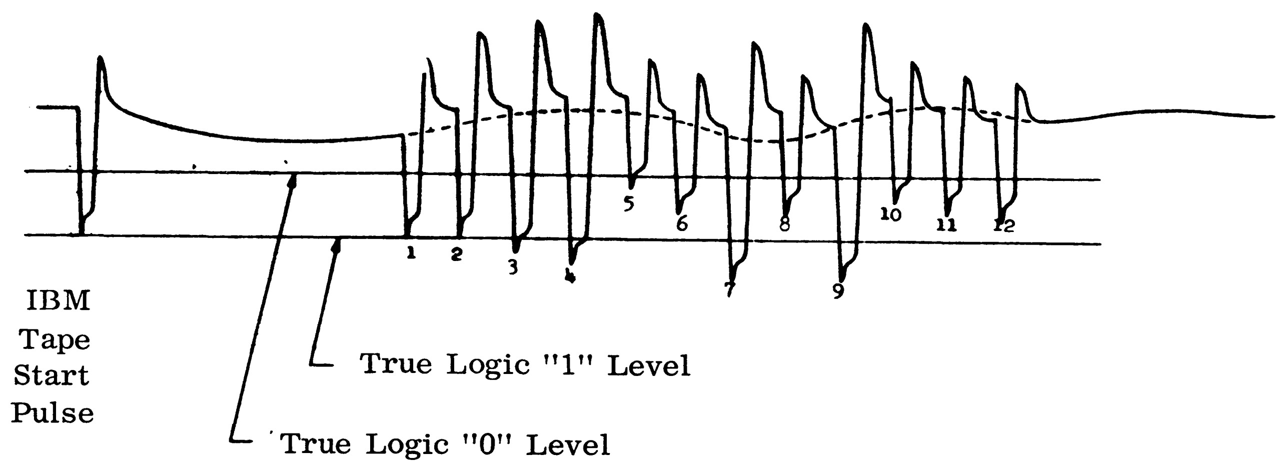


FIG. 31: DISTORTED PLAYBACK WAVEFORM

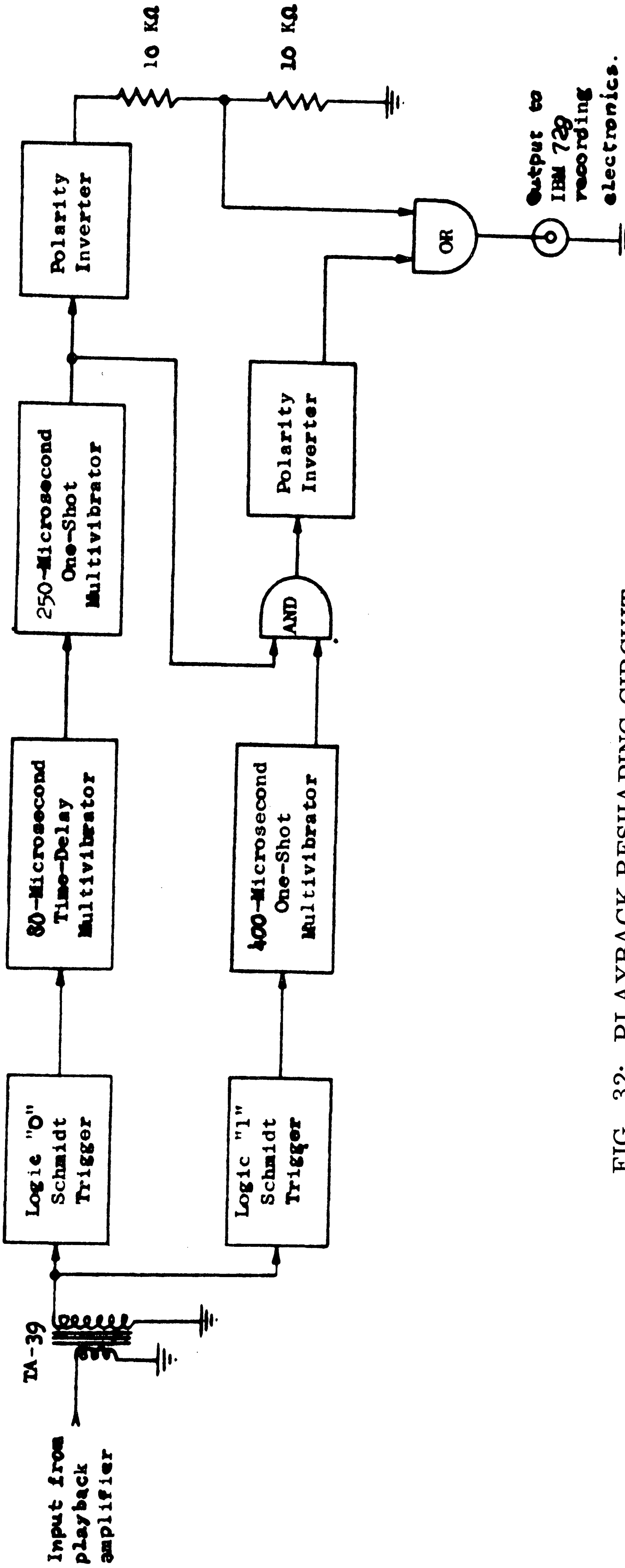


FIG. 32: PLAYBACK RESHAPING CIRCUIT

reshaped waveform of a logic "1". The timing of the second one-shot multivibrator is intentionally longer than that delay time plus the first one-shot time (330 microseconds) to eliminate a back porch on the waveform. The AND gate assures that reconstructed "ones" and "zeros" have the same pulse width.

Because of the low-frequency ringing in the recording amplifier, the ability of the playback-reshaping circuit to differentiate between a logic "0" and a logic "1" was inadequate to guarantee correct reconstruction of the waveform. This problem was eliminated by differentiating the output of the converter prior to recording. The time-constant of the differentiating network was chosen to be 80 microseconds, so that both a negative pulse and a positive pulse are generated for each 250-microsecond pulse. Thus, the average or DC level is always zero, as indicated in Fig. 33. The reshaping circuit above then senses only the proper polarity upon playback. The playback output voltages are -6 volts for a logic "0" and -12 volts for a logic "1". Zero voltage is present between the 250-microsecond pulses.

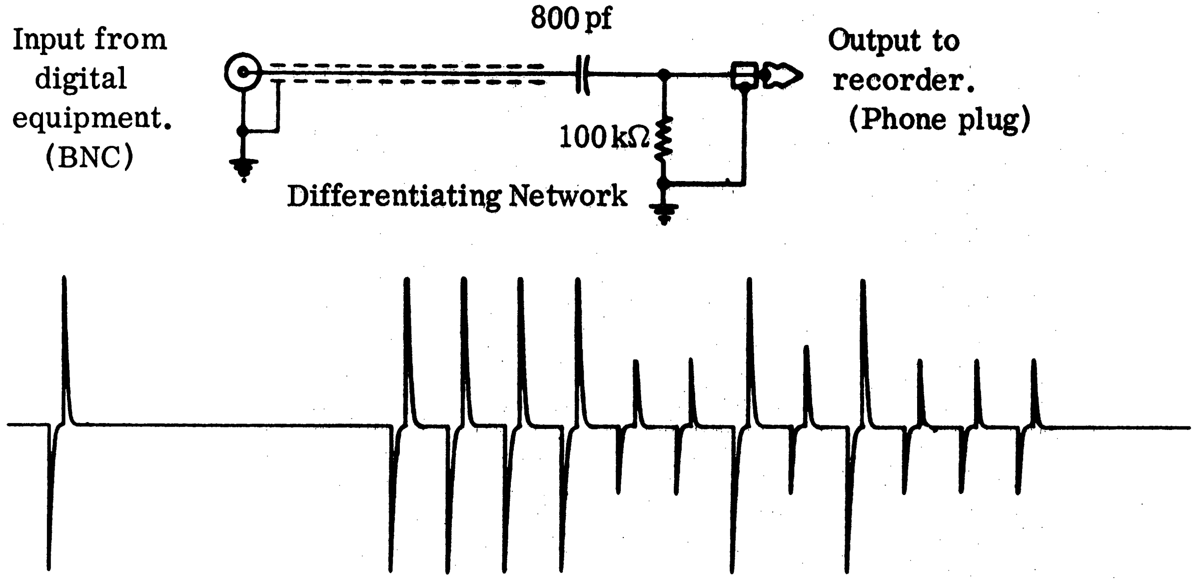


FIG. 33: DIFFERENTIATED OUTPUT WAVEFORM PRIOR TO RECORDING.

VI

CONVERSION TO IBM TAPE

On the ~~IBM tape~~, each "record" consists of forty 36-bit computer "words" (a "header" word, then 39 data words). The header word is merely the number of the record within a "file", as determined by an automatic counting system within the IBM recording electronics at North Campus (see Section V).

A single data word consists of six 15-kcs "samples" of the 12-bit pulse train (record) emanating from the playback system of the AMPRO tape recorder discussed in the last section. Hence, the original 12-bit "digital" signal is treated as analog by the IBM recording electronics.

The time for one record on the IBM tape can be calculated:

$$40 \frac{\text{words}}{\text{record}} \times 6 \frac{\text{samples}}{\text{word}} \times \frac{1}{15} \frac{\text{milliseconds}}{\text{sample}} = 16 \text{ milliseconds/record, which is}$$

sufficient to guarantee the recording of all 12- bilevel pulses from the quarter-inch tape. Note that the first 400 microseconds does not represent actual sampling time, because the header word is substituted.

The input voltage range of the IBM analog-to-digital converter is 0 to -10 volts. Each sample is recorded in the binary numbering system with six-bit accuracy, corresponding to a resolution of 64 levels. If the sample is that of a logic "one" from the original tape, the binary number recorded is 111111, corresponding to the decimal number 63, which is the maximum count. The maximum count is produced by the logic "one" because input voltage (-12 volts from the AMPRO playback reshaping circuit) exceeds the maximum limit of the IBM input range. If the sample is that of a logic "zero" from the original tape, the binary number recorded is 100101, corresponding to the decimal number 37, since the -6 volts from the AMPRO playback reshaping circuit is six-tenths of the -10 volt maximum. If the sample is that of a space between logic pulses, the binary number recorded is 000000, corresponding to the decimal number 00, since the voltage output from the AMPRO playback reshaping circuit is zero.

The half-inch IBM tape is recorded with odd parity and a density of 200 bits per inch at a speed of 75 inches per second. Seven channels are recorded simultaneously: six are used to record the six bits for each sample, while the seventh is used for parity check.

The format for the IBM tape recording for each antenna pattern is:

1. 365 forty-word records, each followed by a "record gap", which constitutes a "file", where:
   a. the first three records give the month, date, and year;
   b. the fourth record gives the run number;
   c. the last 361 records are data points from -180° to $+180^{\circ}$.
2. "End-of-File" mark after each file as above.

The total amount of tape used for one such file will be independent of the rate at which data was originally taken, and can be estimated as follows:

1. Each 16-millisecond "record" uses 1.20 inches of tape.
2. Each "record gap" is a three-quarter inch blank section of tape which includes the tape used during starting and stopping.
3. Therefore, a total of 365 records and record gaps use

$$\frac{365}{12}(1.20 + 0.75) = 59.3 \text{ feet of tape.}$$

Including that tape used for the "end-of-file" mark, approximately sixty feet of IBM tape are required for each antenna pattern.

The time required for the transfer of data to IBM tape is equal to that taken during the original measurement plus equipment setup time and playback monitor checks. A good estimate would be obtained by doubling the actual playing time for the original quarter-inch tape.

VII
CONVERSION TO IBM CARDS

When the IBM tape is placed on the IBM 1401 data processor to transfer the antenna pattern data to IBM cards, a printout of certain data is also obtained (see Fig. 34). The program calls for the file number, the date, the run number, and the antenna signal level (converted back to db) at the first (-180^o) and last ($+180^o$) data points for each antenna pattern to be printed out as the IBM cards are being made. If errors are detected by the 1401 program such as improper record format, which could be caused by transient noise, defective tape, etc., the program calls for an error printout showing the level (logic "zero" or logic "one") of each of the twelve bits of the faulty record, the record number, and the file number (see Fig. 35). The program also instructs the 1401 to leave that record blank on the IBM card, so that the proper numbers can be entered later with a keypunch.

Still another mode of operation can be effected by the operator: The 15-Kc samples for the entire forty-word (240 samples) record can be printed out for complete examination, as shown in Fig. 36. The samples are printed in the octal numbering system, so that a logic "one" appears as the number 77 which corresponds to the decimal number 63, and a logic "zero" appears as the number 45 which corresponds to the decimal number 37 (see Section VI).

The 1401 program requires three consecutive samples in order to "accept" the presence of either a logic "zero" or a logic "one". This eliminates the possibility of confusion should the IBM 729 tape recorder sample the original 12-bit record during a transition from one level to another. Since each bit should remain "on" for 250 microseconds, either three or four identical samples should be obtained.

Each file or antenna pattern on the IBM tape is transferred to a set of fifteen IBM cards. The card has 80 columns of digits 0 - 9 which may be punched as shown in Fig. 37. Three columns are used to record the signal level (converted back to db) for the data point. Twenty-four data points appear on each card (the 361st

-20.0 db

```
FILE =  23

        08/17/65  RUN, FILE, 1ST AND LAST GAIN = 53   023   200   200

FILE =  24

        08/17/65  RUN, FILE, 1ST AND LAST GAIN = 54   024   315   315

FILE =  25

        08/17/65  RUN, FILE, 1ST AND LAST GAIN = 55   025   240   240
```

FIG. 34: IBM 1401 PRINTOUT--ANTENNA PATTERN SUMMARY

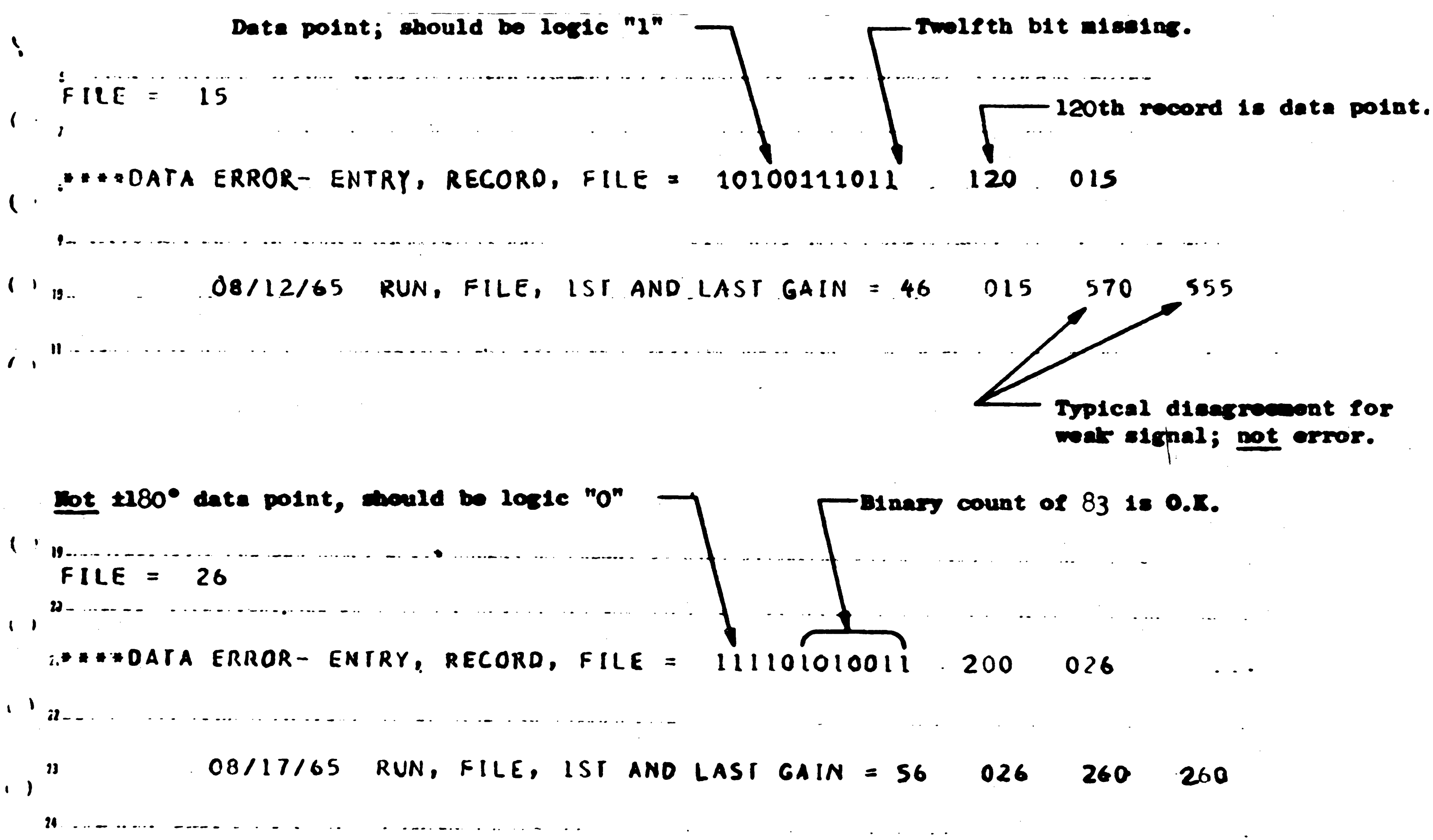


FIG. 35: IBM 1401 PRINTOUT--ANTENNA PATTERN ERRORS

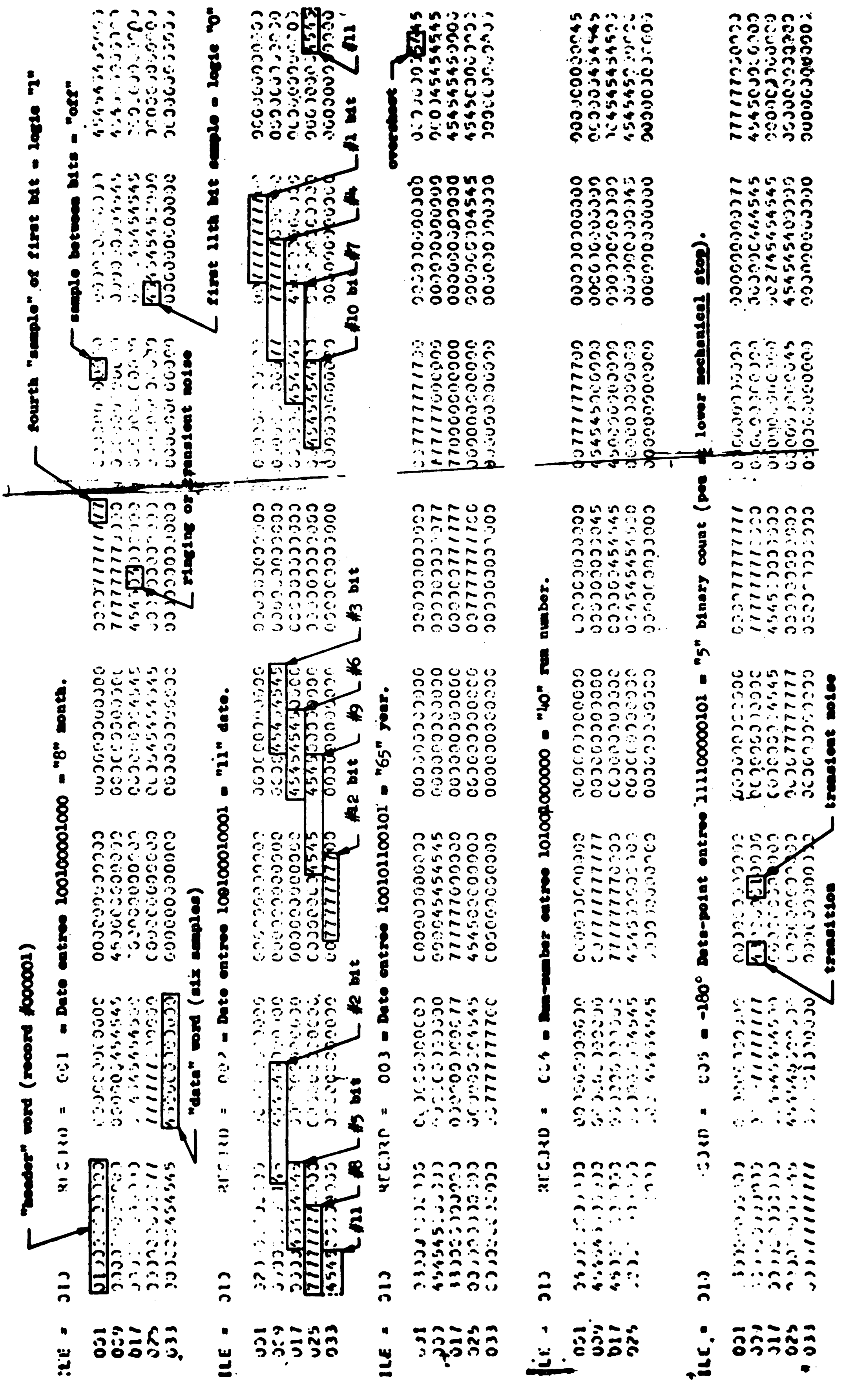


FIG. 36: IBM 1401 PRINTOUT--RECORD DETAIL IN TIME DOMAIN

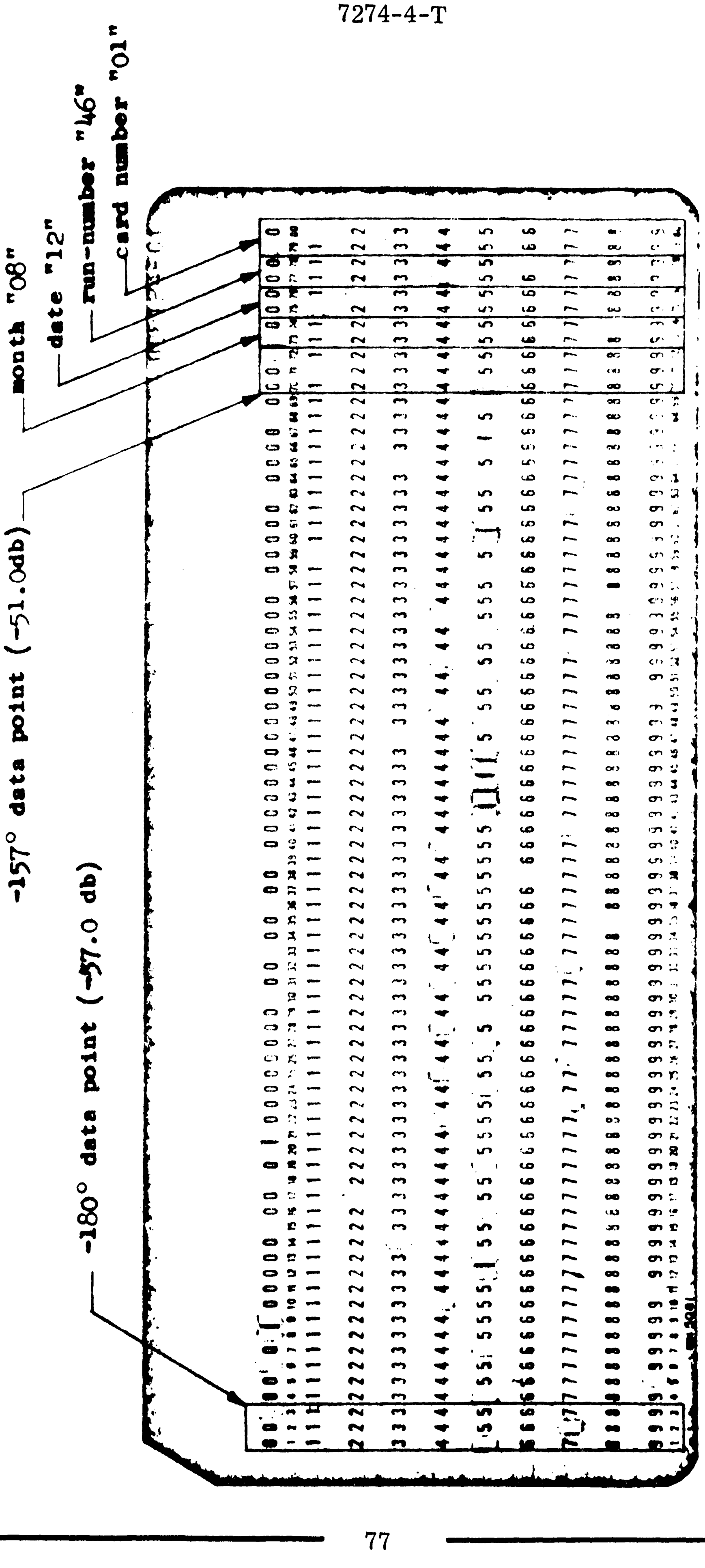


FIG. 37: TYPICAL IBM CARD--ANTENNA PATTERN DATA

data point is dropped): the first 72 columns are thus exhausted. The next four columns, 73 through 76, are used to give the month and the date (the year is dropped). Columns 77 and 78 give the run number, and columns 79 and 80 are used for the card sequence number.

The time required by the data processor to produce one complete set of cards from a tape file is approximately one hundred seconds, once the equipment is operating properly.

A complete file of fifteen cards can then be "interpreted" and printed out in the form shown in Fig. 38 to facilitate manual comparison with the analog antenna pattern recording. Each line shown contains all the information from one card, i.e. twenty-four data points and complete identification.

The fifteen cards for each antenna pattern can finally be processed as desired for further analysis.

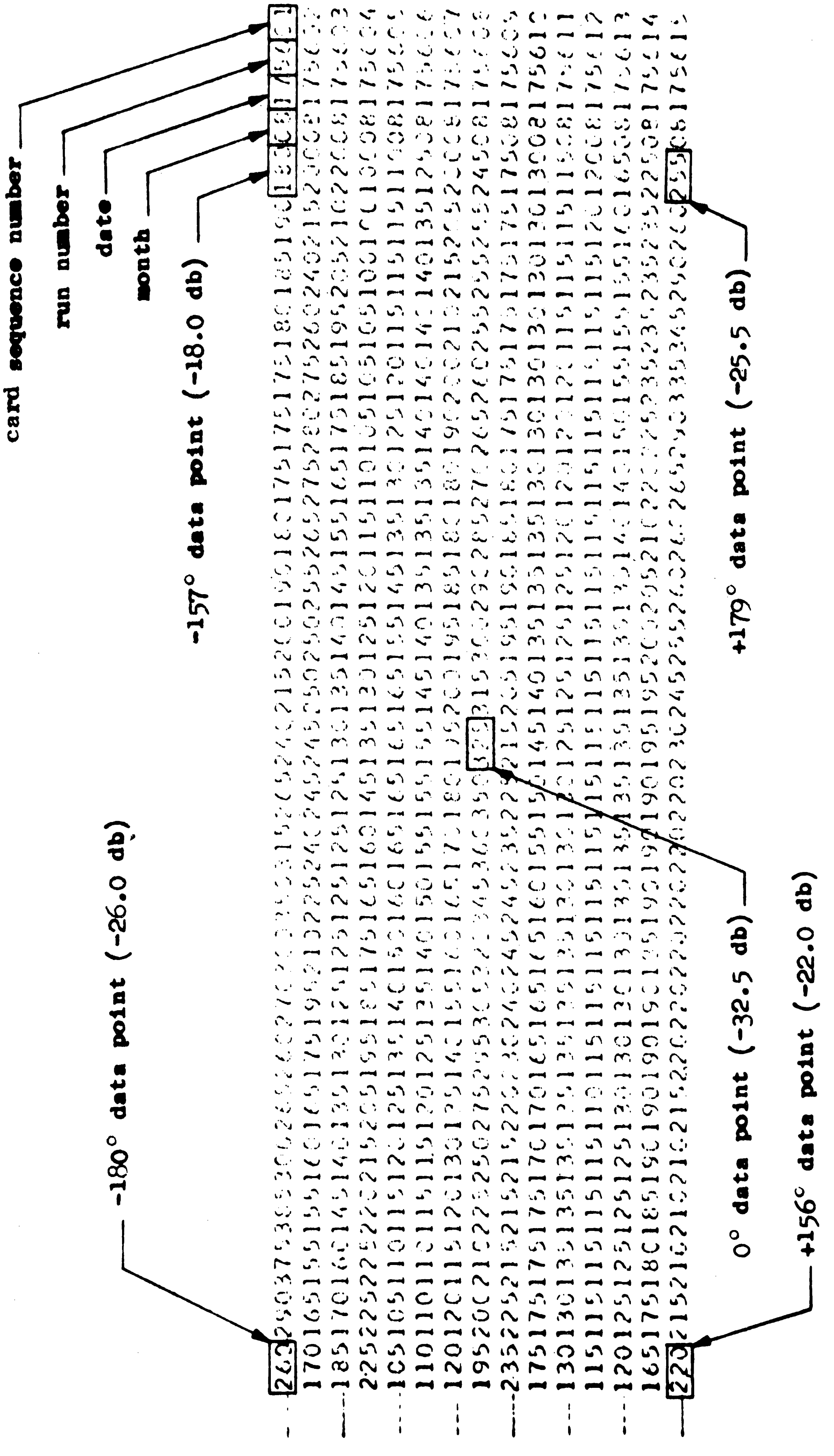


FIG. 38: IBM 1401 PRINTOUT--COMPLETE FILE OF IBM CARDS

VIII

CONCLUSIONS AND RECOMMENDATIONS

This report discusses three recording techniques (manual, semi-automatic and automatic) to obtain antenna spectrum signatures in a digital format. In addition, a format is recommended to ensure that all data forwarded to the Electromagnetic Compatibility Analysis Center (ECAC) is uniform. A major portion of the report is devoted to automatic techniques since it is a more desirable procedure with respect to time, cost and accuracy. It is shown that when employing the manual and semi-automatic procedures human errors are likely to be introduced into the data, thus minimizing its accuracy. However, employing the automatic procedure the probability of human errors occurring in the data is negligible. Therefore, more accurate data can be collected in a shorter period of time at reduced labor costs.

Of major concern to the automatic procedure is the storage medium which should be employed. The three storage mediums evaluated are magnetic tape, punched cards, and a punched paper tape. From this study for field applications, it was concluded that the punched paper tape was the most desirable because of reduced cost, and the availability of recording equipment, and equipment to convert the punched paper tape into the desired punched card format. It has been noted that ECAC prefers punched cards for storage purposes at their facility.

Three techniques applicable to digitalizing the analog data have been considered and are: potentiometers, resolvers and shaft encoders. Because of cost and maintenance factors, the potentiometer and resolver techniques were discarded.

The fourth section of the report discusses a block diagram of an improved automatic system employing the shaft encoding digitalizing technique and a punched paper tape storage medium for the recording of the spectrum data in a digital format. The fifth section of the report discusses in detail the system developed by the University of Michigan and used by them to collect signature data in a digital format. This technique is not as sophisticated as the one presented in Section IV, however, it has been found to operate efficiently and accurately as a breadboard model.

The system discussed in Section V employs a quarter inch magnetic tape as the storage medium and a shaft encoder to digitalize the data. This technique is not recommended for field use since several stages of conversion are required to obtain the data in the proper card format.

As a result of this study, it is recommended that antenna spectrum signature data be collected in a digital format. Further, it is recommended that punched paper tape and a shaft encoder be employed respectively as the storage mediums and digitalizing procedures in the field.

Consideration has been given to the feasibility of using presently available commercial gear for collecting data in a digital paper punch format. Although these are readily available, it is necessary for the using laboratory to purchase considerable additional equipment that is not required to obtain data in the desired digital format. The commercial equipment sells for approximately $10,000 as compared to a cost of $7000 for a custom-built unit that digitalizes the data in the proper format. This may appear as a relatively high price, but it must be remembered this is a custom-built unit and if made on a production basis the cost would in all probability be reduced significantly. Further, one must remember that the commercial equipment requires the use of several pieces of expensive equipment of which only a few circuits are used to effect the digital punch tape and therefore the remaining circuits become a burdensome laboratory investment to be maintained. It is to be noted that most laboratories today are equipped with computer facilities so that once data is obtained in a digital format, it can readily and inexpensively reduce the data into any desired format, therefore, further eliminating the need of elaborate specialized equipment.

UNCLASSIFIED

Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)	2a. REPORT SECURITY CLASSIFICATION
The University of Michigan Radiation Laboratory Department of Electrical Engineering	Unclassified
	2b. GROUP

3. REPORT TITLE

Antenna Spectrum Signature Data Recording Techniques

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Technical Report - June 1966

5. AUTHOR(S) (Last name, first name, initial)

Dute, J. E., Ferris, J. E., Harris, R. B.

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
June 1966	81	

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
AFAL-TR-66-169, Supplement I	7274-4-T
b. PROJECT NO. 4357	
c. 435703	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)
d.	

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11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Air Force Avionics Laboratory AFWE Research and Technology Division Wright-Patterson AFB, Ohio 45433

13. ABSTRACT

This report discusses three techniques that can be employed to obtain analog antenna spectrum signature data in a digital format. The three techniques are: 1) manual, 2) semi-automatic, and 3) automatic. The manual and semi-automatic techniques are discussed briefly. The automatic procedure is discussed in detail along with a system that has been used to obtain data in a digital format. A discussion describing the data format is included to encourage uniformity in the data forwarded to the Electromagnetic Compatibility Analysis Center (ECAC). A discussion of various digital storing mediums that may be employed has been included in Section IV. Typical storage mediums are magnetic tape, punched cards, and punched paper tape. The relative merite of each are discussed along with digitalizing techniques for transferring analog data to a digital format. Section V of the report discusses an automatic system that has been employed by the University of Michigan to obtain data in a digital format usable by ECAC.

14. KEY WORDS	LINK A		LINK B		LINK C	
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