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A CMOS-compatible high aspect ratio silicon-on-glass in-plane micro-accelerometer

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Abstract

This paper presents a post-CMOS-compatible micro-machined silicon-on-glass (SOG) *in-plane* capacitive accelerometer. The accelerometer is a high aspect ratio structure with a 120 μm thick single-crystal silicon proof-mass and 3.4 μm sense gap, bonded to a glass substrate. It is fabricated using a simple 3-mask, 5-step process, and is fully CMOS compatible. A CMOS switched-capacitor readout circuit and an oversampled Σ–Δ modulator are used to read out capacitance changes from the accelerometer. The CMOS chip is 2.6 $\times$ 2.4 mm^2 in size, utilizes chopper stabilization and correlated double sampling techniques, has a 106 dB open-loop dynamic range, a low input offset of 370 μV, and can resolve better than 20 aF. The accelerometer system has a measured sensitivity of 40 mV g^{-1} and input referred noise density of 79 μg Hz$^{-1/2}$. Using the SOG configuration, a post-CMOS monolithic integration technique is developed. The integration technique utilizes dielectric bridges, silicon islands and the SOG configuration to obtain a simple, robust and post-CMOS-compatible process. Utilizing this technique, an integrated SOG accelerometer has been fabricated using the University of Michigan 3 μm CMOS process.

1. Introduction

High precision micro-accelerometers are increasingly needed in applications such as inertial navigation, seismology and micro-gravity measurements [1]. Capacitive micro-accelerometers have several advantages such as high sensitivity, stable dc-characteristics, low drift, low power dissipation and low-temperature sensitivity. One of the important requirements for accelerometers is high resolution [2]. Many *out-of-plane* (z-axis) micro-accelerometers which provide micro-g resolution have been developed [3–6]. In order to reduce noise and increase sensitivity, these sensors utilize full wafer thickness or multiple bonded wafers to form a large proof-mass, and a thin sacrificial layer to form the sense gap. However, it is not practical to easily employ these techniques in *in-plane* (x- or y-axis) sensors that are sensitive to acceleration parallel to the sensor substrate.

Surface-micro-machined accelerometers can be integrated with interface electronics to improve performance. However, due to their small mass they typically have a noise floor of 0.03–1 mg Hz$^{-1/2}$ [7–9]. In order to overcome this limit, bulk micro-machined or SOI (silicon-on-insulator) accelerometers utilizing DRIE (deep reactive ion etching) technology have been developed [10, 11]. These accelerometers utilize 25–70 μm thick single-crystal silicon proof-mass to reduce overall system noise. Nevertheless, these accelerometers either do not provide high enough resolution to satisfy an inertial grade performance or have a complicated fabrication process and large parasitics. In this paper, we report a post-CMOS-compatible high aspect ratio low-noise, high-sensitivity in-plane accelerometer, with a simple fabrication process, which is interfaced with a custom-designed switched-capacitor readout circuit. In the following sections, the structure of the accelerometer and design procedure including sensor performance optimization

Table 1. SOG accelerometer design parameters for performance optimization.

	Parameters	Range	Weight
Mechanical dimensions	Length/width ratio of proof-mass	1.2–20	− −
	Length and width of sense finger	0.2–1 (mm) and 10–25 (μm)	−
	Die size	1–5 (mm^2)	+
Physical characteristics	Quality factor	0.05–0.1	− −
	Cross-axis sensitivity	< -60 (dB)	+
	Shock resistance	> 1000 (g)	+ +
	Operating range	$> \pm 1$ (g)	+ +
Electrical properties	Cut-off frequency	>100 (Hz)	+
	Pull-in voltage	>3 (V)	+
	Sense capacitance	>10 (pF)	+ +
	Stability ($n \cdot k_{ele}/k_{spring}$)	>50	+ + +

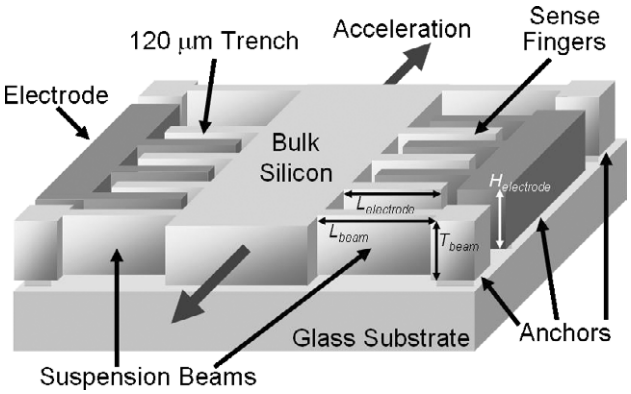

Figure 1. SOG in-plane accelerometer.

are presented first. Micro-machined accelerometer fabrication and associated process issues follow. Then, measurement results of the accelerometer system with CMOS readout circuitry are presented. Finally, we demonstrate a post-CMOS monolithic integration technique using dielectric bridges, silicon islands and SOG configuration [12–14] to obtain a *single-chip* monolithic accelerometer system.

2. Sensor design

Figure 1 illustrates the SOG in-plane accelerometer structure. The accelerometer has a 120 μm thick proof-mass suspended over a glass substrate. This structure is simple and utilizes the well-known lateral combs for sense and force feedback, except that it has a large proof-mass and sense capacitance because of its large thickness and the small sense gap realized by DRIE.

2.1. Design parameter optimization

In order to achieve high sensitivity and low-noise performance, a target object function is defined as (sensitivity/mechanical noise),

$$\frac{\text{Sensitivity}}{\text{Mechanical Noise}} \propto \sqrt{\frac{L_{\text{electrode}}}{H_{\text{electrode}}} \frac{n}{k^2 \cdot d_0}} \cdot M^2 \qquad (1)$$

where n is the number of sense electrodes, k is the spring constant, M is the mass of proof-mass, d_0 is the sense gap, $L_{\text{electrode}}$ and $H_{\text{electrode}}$ are the length and height of an electrode, respectively [13, 15].

The initial design target for mechanical noise density is 10 μg Hz$^{-1/2}$. The thickness of the proof-mass is 120 μm, but it could be made thicker. The target object function is optimized with different design variables to obtain a high performance accelerometer, listed in table 1. In order to perform an efficient optimization process, a customized weight function has been assigned to each parameter to avoid unnecessary trivial minor adjustments. Among the dependent parameters, stability is assigned to be the most significant factor, so as to ensure a stable closed-loop operation. $n \cdot k_{ele}/k_{spring}$ is a measure of stability (k_{ele} is the spring constant of an electrode and k_{spring} is the spring constant of spring beams attached to the proof-mass). This ratio is designed to be larger than 50 to achieve a stable closed-loop operation [16].

Table 2. SOG accelerometer design parameters.

Mass of the proof-mass	0.5 mg
Resonant frequency	2.14 kHz
Thickness of the proof-mass	120 μm
Sense gap	2.0 μm
Sense capacitance	32.1 pF
Spring constant of spring beams	90.4 N m^{-1}
Cross-axis sensitivity	$<0.1\%$
Sensitivity/mechanical noise	(0.78 pF g^{-1})/(10 μg Hz$^{-1/2}$)

Figure 2 shows two three-dimensional (3D) plots of the optimization. The plots illustrate how high sensitivity can be obtained using a mechanical noise of 10 μg Hz$^{-1/2}$ device. Table 2 summarizes the optimized design parameters. Note that the mass of the proof-mass is close to a milligram, which is an order of magnitude higher than that of surface-micro-machined devices. Also, sense capacitance is substantial enough to improve immunity to parasitic capacitances, which enables hybrid assembly with readout electronics.

2.2. Sensor system noise

High sensitivity and low noise are most essential since they determine the input referred noise density (IRND), often called the noise floor. In an accelerometer system, IRND is derived from two components—system gain and output system noise density (OSND):

System gain (V g^{-1}) = (Sensitivity of device)
× (Sensitivity of readout circuitry)

OSND (V Hz$^{-1/2}$)
$$= \sqrt{(N_{\text{mechanical}} \times \text{System gain})^2 + N_{\text{electronic}}^2}$$

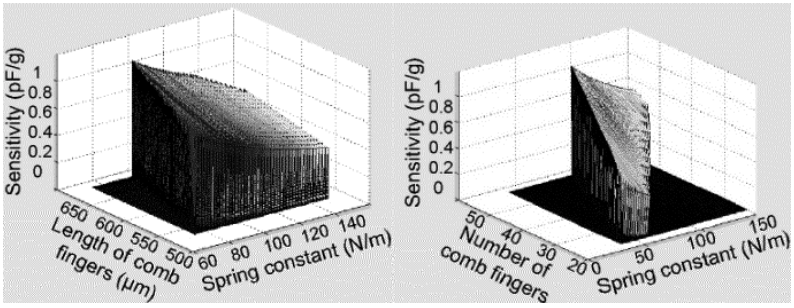

Figure 2. Design parameter optimization.

(where $N_{\text{mechanical}}$ and $N_{\text{electronic}}$ denote mechanical and electronic noise, respectively).

The system gain consists of sensitivities of the accelerometer and the readout circuit. The output system noise density is the addition of noise powers from the mechanical part, multiplied by the system gain, and the electronic part. Note that the noise density indicates not just mechanical noise, but the accelerometer system noise. In this paper, noise represents the overall system noise unless it is stated as mechanical or electronic noise. IRND can be expressed as

$$\text{IRND (g Hz}^{-1/2}) = \text{OSND (V Hz}^{-1/2})/\text{System gain (V g}^{-1}) = \sqrt{N_{\text{mechanical}}^2 + \left(\frac{N_{\text{electronic}}}{\text{System gain}}\right)^2}.$$

Assuming a signal-to-noise ratio (SNR) of 1, the resolution, sometimes called the minimum detectable signal, of the sensor is defined as the multiplication of IRND and the measurement bandwidth. Since the bandwidth is an application-specific parameter, IRND is, generally, the measure of resolution.

To estimate the resolution of the SOG accelerometer system, the contribution from readout electronic noise needs to be taken into account. If we assume a circuit sensitivity of 0.3 V pF^{-1}, a sensor sensitivity of 0.78 pF g^{-1}, and a total output electronic noise of 25 μV over a 100 Hz BW [17], the IRND of the SOG accelerometer system can be estimated as

$$\text{IRND} = \sqrt{(10\,\mu\text{g Hz}^{-1/2})^2 + \left(\frac{25\,\mu\text{V}/\sqrt{100\,\text{Hz}}}{0.78\,\text{pF g}^{-1} \times 0.3\,\text{V pF}^{-1/2}}\right)^2} = 14.6\,\mu\text{g Hz}^{-1/2}.$$

Note that the noise density is strongly dependent on the system gain, which is itself dependent on both device and circuit sensitivities. Since electronic noise increases as circuit sensitivity increases, in order to have a low-noise accelerometer system, it is preferred to use a high-sensitivity and low-noise accelerometer structure.

2.3. FEM verification

Optimized design parameters are verified using FEM simulation. Figure 3 shows the resonant frequencies of the SOG accelerometer. As seen, the first mode (y-axis) resonant frequency is 2.14 kHz, giving a spring constant of 93.5 N m^{-1}. The resonant frequencies for the second and third modes are 14.6 kHz (z-axis) and 22.9 kHz (x-axis) respectively. These are much higher than the first mode, resulting in low cross-axis sensitivity. Sensitivity to off-axis acceleration is also verified by FEM simulation. By definition of sensitivity of any parameter to a second parameter, cross-axis sensitivities are determined by equation (2) (note that y is the sense axis), and shown in table 3. Cross-axis sensitivities for x- and z-axes are estimated as −99 dB and −67 dB, respectively. The x-axis cross-axis sensitivity is much lower than the z-axis due to the larger spring constant:

$$S_{\Delta a_{x,z}}^{\Delta C} = \frac{\Delta C/C}{\Delta a_{x,z}/a_{x,z}}. \quad (2)$$

Shock resistance is also simulated to evaluate if the device is robust enough to sustain external unexpected shocks. For the sense axis (y-axis), the proof-mass movement is constrained by shock stops, thus the sense structures can be protected. For x- and z-axes, a 1000g external shock is simulated. The maximum stresses occur at the edge of the spring beams, and are 10.4 MPa for the x-axis shock and 98.6 MPa for the z-axis shock, respectively. This shows that the sensor should be able to survive under a 1000g shock since the fracture strength for single-crystal silicon is at least 600 MPa [18].

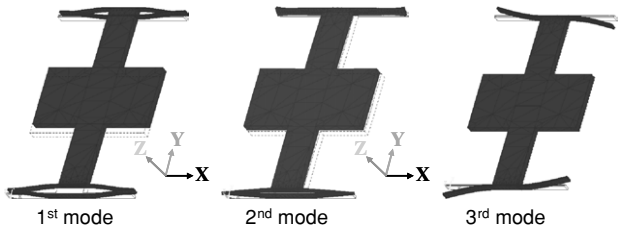

Figure 3. Resonant frequencies of the SOG accelerometer.

Table 3. Cross-axis sensitivities.

	$\Delta x/\Delta y$	$\Delta z/\Delta y$	$\Delta C/C$
x-axis	0.26%	0.02%	−98.88 dB
z-axis	0.008%	2.2%	−67.15 dB

Note that y is the sense axis.

3. Fabrication

The fabrication process has only five steps, requiring three masks as shown in figure 4. The process is simple, requires no special steps other than DRIE, and does not require any high-temperature processing, which is favorable for post-CMOS processing. The glass substrate bonded to the single-crystal silicon is insulating, which reduces parasitics and thereby facilitates interfacing with a hybrid readout circuit.

First, a glass substrate with a shallow recess is prepared for anodic bonding (*a*). Then, a standard silicon wafer (with CMOS circuitry if needed) is anodically bonded to the glass

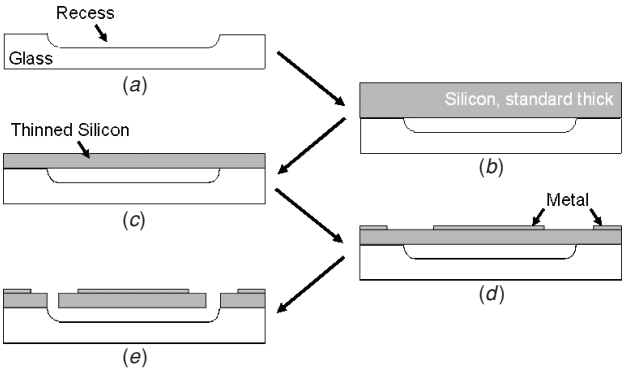

Figure 4. Fabrication sequence.

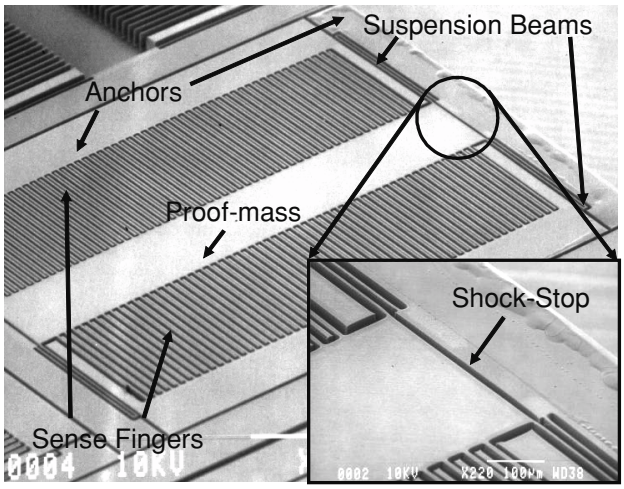

Figure 5. Top view of fabricated SOG accelerometer and shock stop.

substrate (*b*). The silicon wafer is then thinned to 120 μm using standard chemical mechanical polishing (CMP) (*c*). After the CMP step, the metal contacts (Cr/Au) are evaporated and patterned. Finally, the wafer is DRIE etched to define the proof-mass and sense fingers. Figure 5 shows SEM views of the SOG accelerometer, $2.2 \times 3.0 \times 0.12$ mm^3 in size, and a shock stop for preventing excessive proof-mass movement to protect sense fingers from an external shock. There are two critical steps influencing the overall performance; DRIE etch and micro-loading effect. Detailed description and methods to minimize these influences are discussed in the following subsections.

3.1. DRIE technology

DRIE technology is crucial for the SOG accelerometer since it does not only release the device but also determines the sense gap distance. The sense gap is the most important parameter affecting squeeze film damping and sensitivity. The SOG accelerometer is designed to have a 2 μm gap and a depth of 120 μm (60:1 ratio). The etch profile needs to be carefully characterized since a non-vertical sidewall profile introduces non-linearity [19]. To obtain a 60:1 aspect ratio, the pressure inside the etch chamber is initially high and is reduced as the etch proceeds, which helps to remove etch by-products from the deep trench. DRIE etch parameters are listed in table 4. Figure 6 shows a vertical etch profile and sense gap after

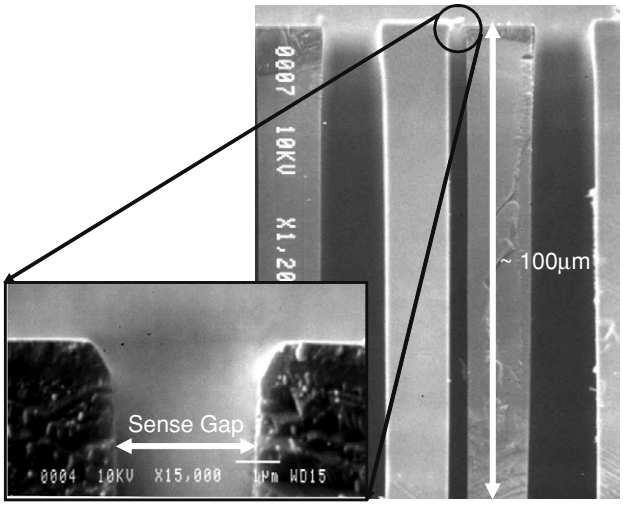

Figure 6. Vertical etch profile of sense fingers and sense gap after 70 min DRIE etch.

Table 4. DRIE etch parameters.

	Time (s)	Flow rate (sccm)	Coil/platen power (W)
Etch	12	SF_6/O_2 (130/13)	80/10
Passivation	6	C_4F_8 (85)	80/0
Pressure	Automatic pressure control, 65–0.6%/min		

70 min DRIE. Although the sense gap is designed to be 2 μm, it becomes wider due to the finite lateral etch during the high aspect ratio etch. This reduces device sensitivity because the sensitivity is proportional to d_0^{-2}.

3.2. Micro-loading effect

The micro-loading effect becomes significant when etching two different width trenches side-by-side [20]. Obviously, SOG devices have different size trenches, which make them vulnerable to this effect. Figure 7 illustrates the micro-loading effect. As the DRIE etch proceeds, a wide trench is etched faster than a narrow trench due to different etch rates. Once the etching of the wide trench is complete, positive ions reach the bottom of silicon through the wide trench, get charged up on the glass substrate, and attack silicon from the bottom side, which results in a thinner structure [21]. The proof-mass from the device is taken and placed upside down to observe the micro-loading effect after finishing the DRIE etch (∼80 min), as is shown in figure 8. Note that the roughness of the sense fingers is due to the non-directional etch from the bottom of silicon through the wide trench. The cross sections of the proof-mass and sense fingers are also shown in figure 8. The thickness of the sense fingers is 100 μm instead of 120 μm, which results in a 20% sensitivity reduction due to the loss of sense area. Moreover, the vertical etch profile is compromised due to the micro-loading effect, which introduces non-linearity.

In order to prevent etching from the backside, a shielding metal layer is placed between the thinned silicon and the glass substrate. In so doing, both silicon and glass have the same electrical potential, which prevents charging up the dielectric substrate [21]. As a result, sense fingers maintain their original

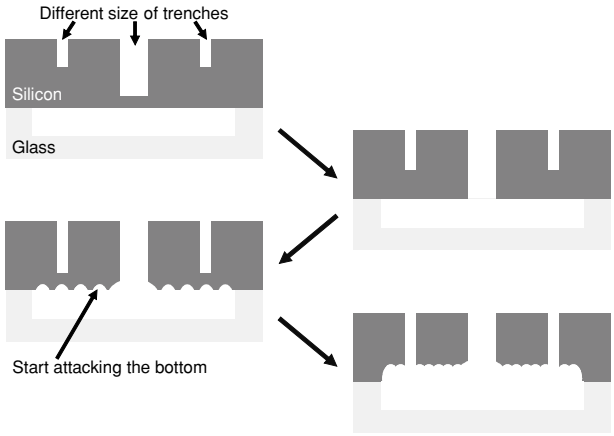

Figure 7. Micro-loading effect [21].

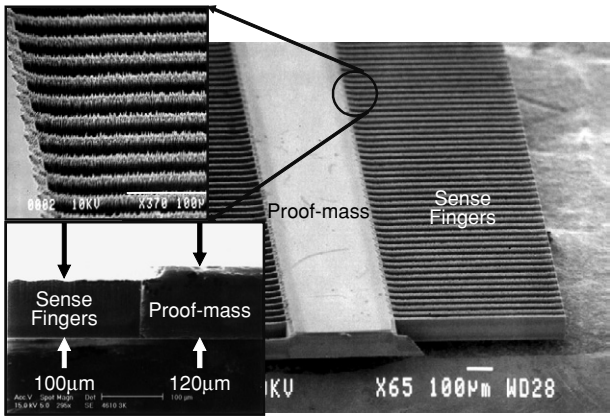

Figure 8. Micro-loading effect on the fabricated SOG accelerometer.

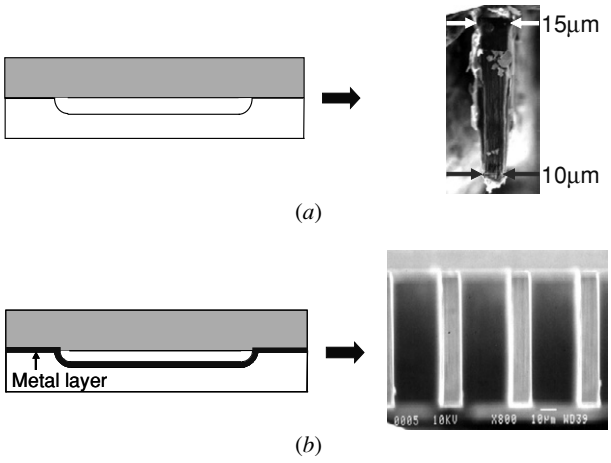

Figure 9. Method to avoid the micro-loading effect: (*a*) damaged sense finger and (*b*) sense finger with an electrical short path.

height and near ideal vertical sidewall profile as shown in figure 9.

4. Test results

4.1. Electrostatic measurement

The fabricated devices are first tested electrostatically and mechanically on a dividing head (precision turn table). The tested accelerometer is designed to have 25 N m^{-1} spring constant, 2 μm sense gap and 16.6 pF sense capacitance, and an estimated pull-in voltage of 1.9 V. Figure 10 shows an electrostatic measurement of the fabricated device. Each left and right side of the electrodes shows smaller capacitances (5.25 $\sim$ 5.4 pF) and higher pull-in voltages (4.5 $\sim$ 4.6 V) than the designed values (8.3 pF and 1.9 V). Assuming the sense area (A), the number of sense electrodes (n) and the spring constant (k) in analytical pull-in voltage of an electrostatic measurement (equation (3)) are not changed much by fabrication variation, the measurement implies that the fabricated device has larger sense gap (d_0) than designed. From the pull-in voltage of 4.6 V, the spring constant can be extracted as 35 N m^{-1}, off by 40% from the designed value (25 N m). It is possible that the discrepancy comes from the non-vertical etch profile of suspension beams. The high aspect ratio etch recipe used for these devices was optimized for deep narrow trenches. Therefore, small features surrounded by wide trenches may not have a very vertical profile:

$$V_p = \frac{2d_0}{3}\sqrt{\frac{2k \cdot d_0}{3\varepsilon \cdot A \cdot n}}. \tag{3}$$

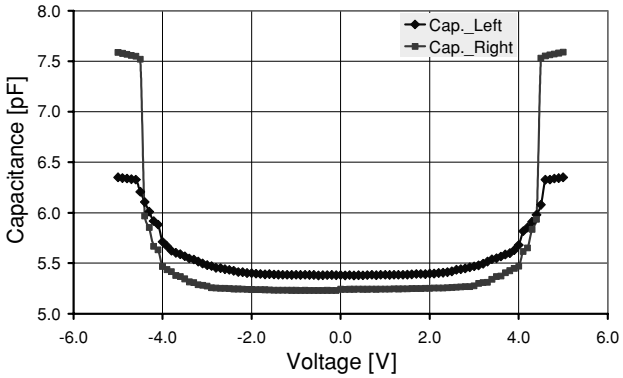

Figure 10. Electrostatic measurement.

4.2. Dividing head (precision turn table) measurement

The measured sense capacitance is approximately 4.8 pF for each side. The designed sense capacitance on one side is 8.3 pF indicating that the fabricated device has larger sense gap, $\sim$3.4 μm. Figure 11 shows the sensitivity measurements by using a dividing head. The sensitivity of the device is 0.15 pF g^{-1}, much smaller than what it is designed to be (0.78 pF g^{-1}). The reduction of sensitivity is due to the larger gap and the stiffer spring. With a 3.4 μm sense gap and 35 N m^{-1} spring constant, the sensitivity is calculated to be 0.19 pF g^{-1}, which is smaller, by a factor of 4$\times$, than expected.

4.3. Hybrid module with switched-capacitor readout circuit

Capacitance changes from the micro-accelerometer are read out by a Σ–Δ switched-capacitor circuit, which can operate either in an open or a closed loop [22]. The circuit includes chopper stabilization and correlated double sampling techniques to cancel $1/f$ noise, and amplifier offset, and compensate for finite amplifier gain. It has 106 dB dynamic

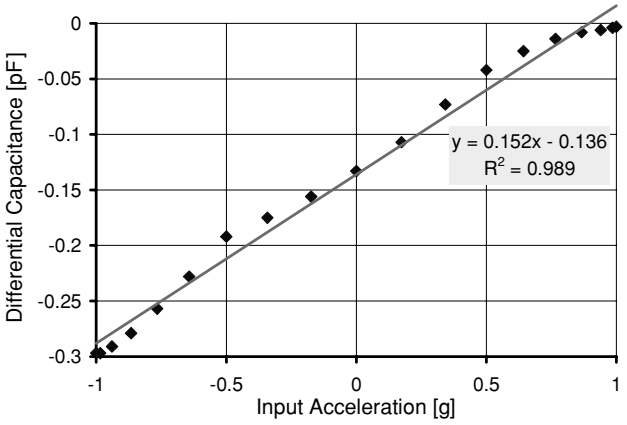

Figure 11. Sensitivity measurement using a dividing head.

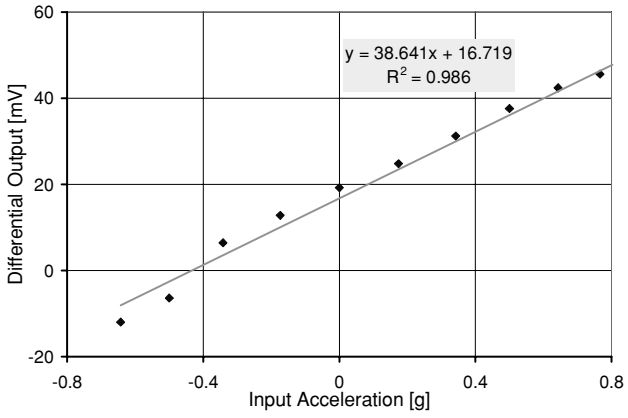

Figure 13. Open-loop test result of the hybrid system.

range, an offset of 370 μV and can resolve better than 20 aF. Figure 12 shows the simplified schematics of the CMOS capacitive interface chip and its hybrid connection to the sensor. Two fixed external reference capacitors are used to establish a full-bridge scheme. The hybrid system is assembled onto a PC board and mounted in a standard 24-pin IC package as shown in figure 12. Note that of the six devices on a die, only one is connected to the circuit for testing.

The hybrid system is tested for sensitivity and noise floor in an open-loop configuration. The open-loop test is performed on a dividing head, in a 1g gravitational field, by changing the acceleration from -1g to $+1$g. Figure 13 shows the open-loop test result for the hybrid system, indicating a sensitivity of $\sim$40 mV g^{-1}. This result matches with the expected value since the device has a sensitivity of $\sim$0.15 pF g^{-1} and the readout circuit has a voltage gain of 300 mV pF^{-1}.

The noise density of the SOG accelerometer system can be estimated as (note that the mechanical noise is reduced to 4.5 μg Hz$^{-1/2}$ due to the enlarged sense gap):

$$\text{IRND} = \sqrt{(4.5\,\mu\text{g Hz}^{-1/2})^2 + \left(\frac{25\ \mu\text{V}/\sqrt{100\ \text{Hz}}}{40\ \text{mV g}^{-1}}\right)^2} = 82.6\,\mu\text{g Hz}^{-1/2}.$$

The measured output noise spectrum of the system (obtained using a dynamic signal analyzer HP3561) is shown in figure 14. The total noise over a bandwidth of 100 Hz is $\sim$22.4 μV, which indicates that the noise density of the current hybrid system is

$$\text{IRND} = \frac{\sqrt{2} \times 22.4\ \mu\text{V}}{40\ \text{mV g}^{-1}} \Big/ \sqrt{100\ \text{Hz}} = 79.1\ \mu\text{g Hz}^{-1/2}.$$

The $\sqrt{2}$ term is added to account for the two output channels of the circuit. As is observed, the calculated output system noise floor matches well with the measured value.

The measured system noise floor of 79.1 μg Hz$^{-1/2}$ is high because of the small gain of the hybrid module (40 mV g^{-1}) and the low sensitivity of the accelerometer. Table 5

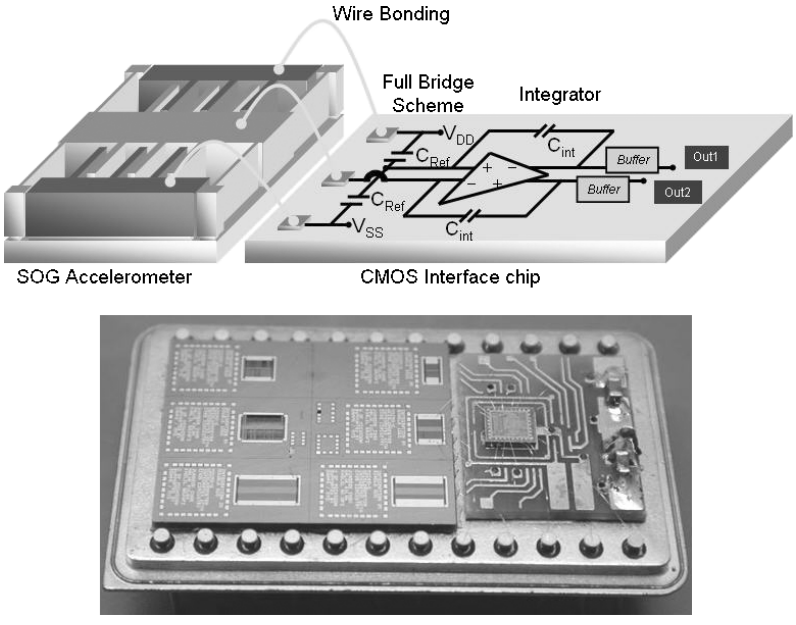

Figure 12. Hybrid accelerometer and readout electronics system in IC package.

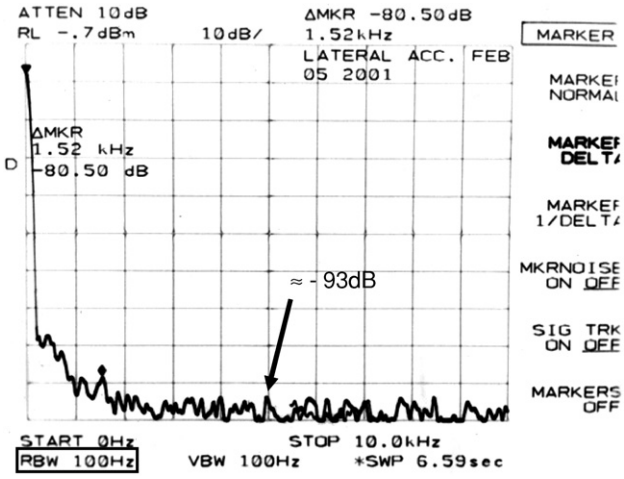

Figure 14. Output spectrum of the hybrid system.

Table 5. Hybrid sensor/circuit module specifications.

MEMS device parameters	
Sensitivity	0.15 pF g^{-1}
Mechanical noise	4.51 μg $Hz^{-1/2}$
Interface readout circuitry parameters	
Sampling clock	30 kHz
Power dissipation	<6.6 mW @ 5 V
Capacitance sensitivity	0.3 V pF^{-1}
Resolution	<20 aF
Offset	2.7 mV (370 μV w/chopper stabilization)
MEMS device and interface circuitry module	
Sensitivity	40 mV g^{-1}
Open-loop noise density	79.1 μg $Hz^{-1/2}$

summarizes accelerometer-interface circuit hybrid module specifications. Table 6 shows the estimated and measured sensitivity, noise floor and the sensitivity/noise ratio of this accelerometer, and compares these values to those of other devices reported in the literature.

5. CMOS compatibility

Surface micro-machining technology has been used extensively for industrial MEMS accelerometer products [23, 24]. One of the biggest advantages of surface micro-machining technology is easy monolithic integration with electronics to achieve small size and improve performance. However, surface-micro-machined devices often do not satisfy the requirements of high performance applications. In order to meet these requirements, devices fabricated using SOI or bulk micro-machining utilizing wafer bonding technologies have been developed [11, 13, 25–27]. The silicon-on-glass (SOG) device, presented in this paper, is one of them. Although these devices offer higher sensitivity and lower noise floor than surface-micro-machined devices, monolithic circuit integration with these devices is a challenge. This is because the sensors often require additional steps before or after standard circuit fabrication process.

We propose a standard post-CMOS monolithic fabrication technique utilizing the SOG configuration. This technique uses dielectric bridges, silicon islands and the SOG configuration to obtain simple, robust and a fully CMOS-compatible MEMS integration process.

5.1. Post-CMOS fabrication

Depending on where the additional steps to build MEMS devices are performed with respect to circuit fabrication, the processes are referred to as pre-CMOS, pre-and-post CMOS [11, 28] and post-CMOS [29]. The post-CMOS technique has been the most popular because it is the most reliable, simple and inexpensive although it is limited to low-temperature process steps to prevent any damage to electronics already fabricated on the wafer [10, 29].

The post-CMOS technique has a few requirements. First of all, as mentioned above, the process steps after circuit fabrication must be performed at low temperature. Second, the interconnection scheme between MEMS devices and the electronics should be robust enough to survive when MEMS devices move. Finally, the additional manufacturing steps after circuit fabrication should be simple because as the post-CMOS fabrication becomes more complicated, the overall yield decreases, and the manufacturing cost increases.

5.2. A monolithic integration technique using SOG configuration

The SOG configuration is a low-temperature process and has simple fabrication steps. In order to obtain robust interconnections, as introduced in the previous section, dielectric bridges and silicon islands are developed and combined with the SOG configuration. Figure 15 illustrates the monolithic integration scheme. A glass substrate supports electrically isolated pieces of silicon defined by DRIE. A metal layer is used for interconnection lines. Although the thickness of silicon is chosen as 120 μm in this work, it can be thicker up to full wafer thickness. It is determined by the capability of DRIE, which is limited only by the required aspect ratio of MEMS structures.

Table 6. Sensitivity/noise ratio.

					SOG	
	ADXL [7]	UCB [9]	CMU [31]	IMI [11]	Estimated	Measured
Sensitivity (fF g^{-1})	0.1	4.5	0.3	102	780	150
Noise Floor (μg $Hz^{-1/2}$)	225	32	50	25	14.6	79.1
Sensitivity/noise floor	0.0004	0.14	0.006	4.1	53	1.9

ADXL stands for Analog Device Inc.'s; UCB stands for University of California at Berkeley; CMU stands for Carnegie Mellon University; IMI stands for Integrated Micro-Instruments.

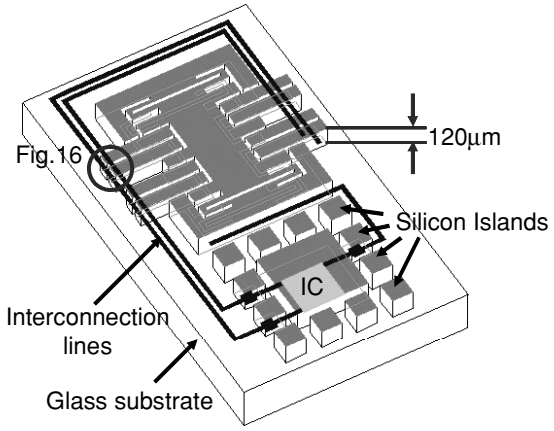

Figure 15. SOG monolithic integration scheme.

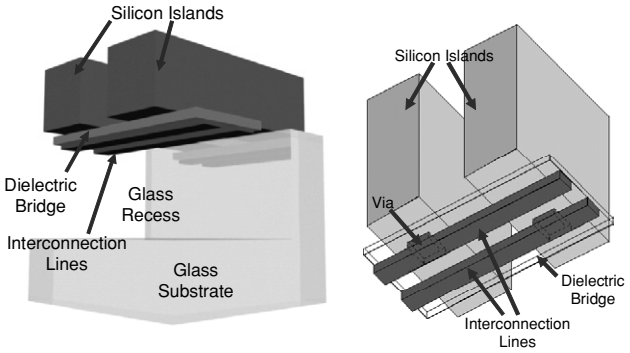

Figure 16. Dielectric bridge and silicon islands.

Figure 16 shows the structure of the dielectric bridge carrying signals between silicon islands. The metal interconnection goes over the silicon islands with the help of the dielectric bridge. The dielectric bridge consists of a number of layers such as thick field oxide and CVD oxide provided by the CMOS fabrication steps. Output pads for connecting to external power supplies, V_{DD} and ground, or for testing and sensor output are formed on the top of the silicon islands.

The SOG monolithic integration process is shown in figure 17. The process is quite similar to the SOG accelerometer presented previously. First, conventional IC fabrication is performed on a silicon wafer. A glass substrate with a recess and a shielding metal is also prepared. The metal is deposited and patterned on the glass substrate not only to avoid the micro-loading effect from the following DRIE, but also to protect the IC from the large electric field during the bonding process. Next, the fabricated silicon IC wafer is anodically bonded to the glass substrate, and is thinned to the desired thickness using CMP. Finally, metal contacts are formed, and DRIE is used to define the MEMS structure, silicon islands and dielectric bridges.

An integrated SOG accelerometer has been fabricated using the University of Michigan 3 μm 2-poly 1-metal CMOS process [30]. Figure 18 shows an optical photograph of a MEMS device integrated with readout electronics before post-CMOS MEMS fabrication steps. Reference capacitors for full-bridge operation, metal interconnections and connection to silicon islands are fabricated on a standard silicon wafer. Figure 19 shows the fabricated chip after the post-CMOS steps, including anodic bonding, CMP, contact metal deposition and DRIE. Each metal pad on top of silicon islands is electrically isolated from the other, and is used to connect to the outside world. Close-up views of the silicon islands, dielectric bridges and interconnection are shown in figure 20.

5.3. Test results

The threshold voltages of nMOS and pMOS transistors were measured to be 0.74 V and 0.49 V, respectively (figure 21). Obviously, the positive pMOS threshold voltage is not what was expected, and results in malfunction of the entire readout circuit. We do not know why the pMOS transistor's threshold voltage was off the target, but nMOS was right on the target. This is likely due to some contamination or a problem in ion implantation.

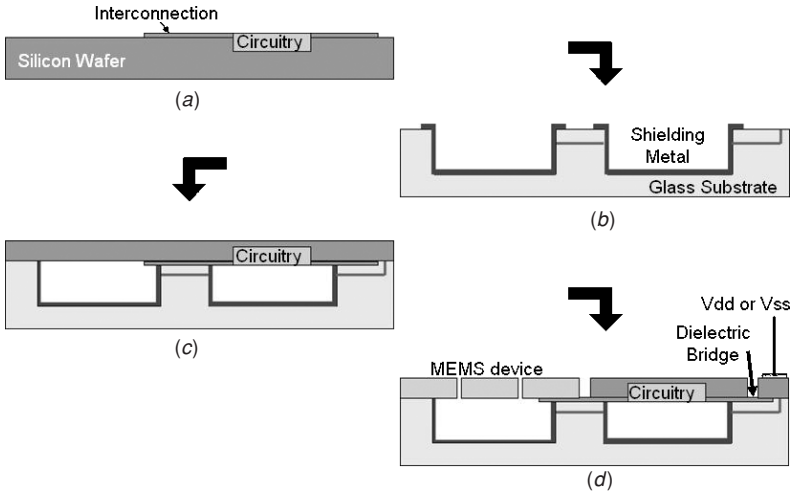

Figure 17. Fabrication sequence of SOG monolithic integration: (*a*) standard CMOS process on a silicon wafer, (*b*) a glass substrate with shielding metal, (*c*) flip the silicon wafer & bond to the glass substrate and CMP the silicon wafer and (*d*) deposit contact metal & DRIE.

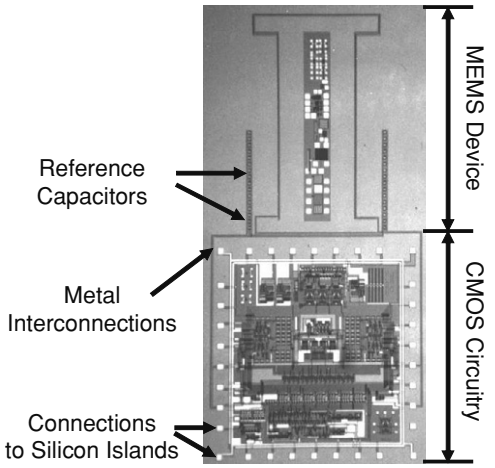

Figure 18. Fabricated integrated MEMS device with readout electronics.

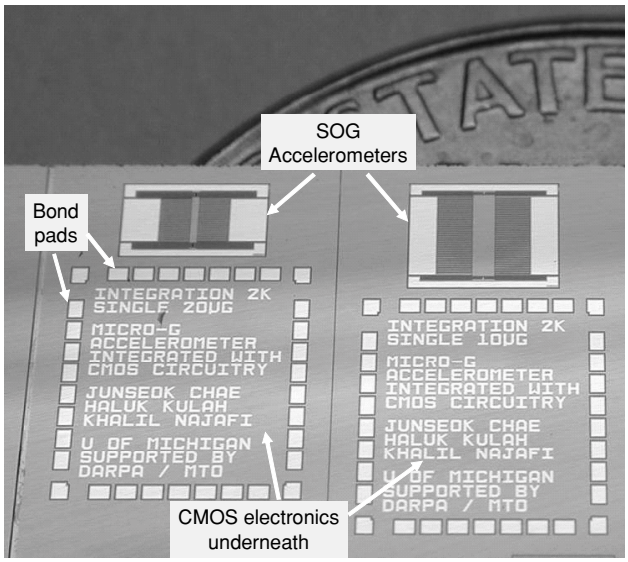

Figure 19. Fabricated chip after post-CMOS process.

Although MEMS devices integrated with CMOS circuit were not realized successfully, the core elements of the integration process have been successfully demonstrated. It has been shown that a standard CMOS wafer can be bonded to glass, polished back, and DRIE etched to form MEMS devices. The dielectric bridge and silicon islands are successfully fabricated and enable signal routing and transfer between the circuits and MEMS devices. The problem associated with the threshold voltage of pMOS transistors can be solved by using standard CMOS wafers from a commercial foundry.

6. Conclusion

In this paper, a fully CMOS-compatible high aspect ratio silicon-on-glass (SOG) configuration micro-accelerometer with CMOS readout circuitry is presented. The SOG configuration uses a high aspect ratio structure with 120 μm thick single-crystal silicon proof-mass and 3.4 μm sense gap, bonded to a glass substrate. The accelerometer has a simple 3-mask, 5-step process, and is fully CMOS compatible. Target sensitivity and noise floor of the SOG accelerometer with readout circuitry are 0.78 pF g^{-1} and 15 μg Hz$^{-1/2}$.

A CMOS switched-capacitor front-end circuit is used to read out the capacitance changes from the micro-accelerometer. The circuit has a 106 dB open-loop dynamic

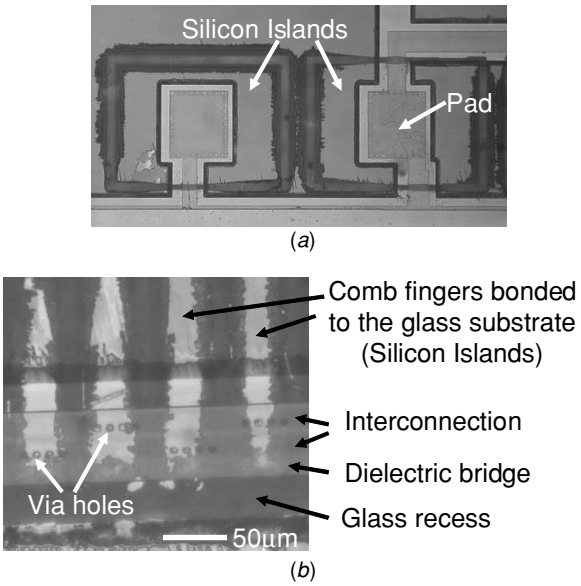

Figure 20. Silicon islands, dielectric bridge and interconnection: (*a*) silicon islands and pad and (*b*) interconnection between comb fingers.

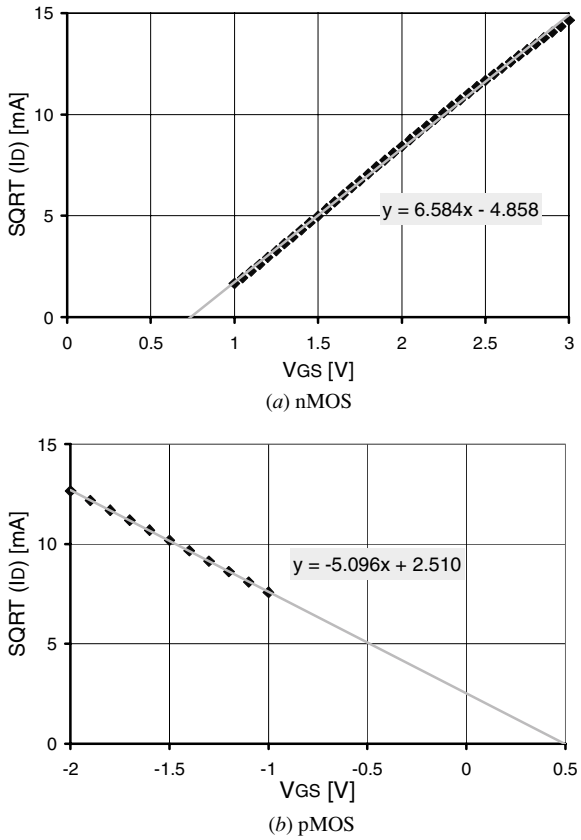

Figure 21. Transistor V_{GS} versus I_D characteristics.

range, a low input offset of 370 μV and can resolve better than 20 aF. A hybrid microsystem consisting of the SOG accelerometer and Σ–Δ switched-capacitor readout circuit provides a measured sensitivity of 0.15 pF g^{-1} and a noise floor of 79 μg Hz$^{-1/2}$. The sensitivity reduction is mostly from an enlarged sense gap due to the finite lateral DRIE etch.

A monolithic post-CMOS integration technique utilizing dielectric bridges, silicon islands and SOG configuration has been developed. This technique is simple, robust and fully post-CMOS compatible. A glass substrate supports the silicon islands and signal routing is provided with the help of the dielectric bridge between the silicon islands. Utilizing this technique, an integrated SOG accelerometer has been fabricated using the University of Michigan 3 μm CMOS process.

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