Active Matrix Organic Light-Emitting Displays: Novel Amorphous Silicon Thin-Film Transistors and Pixel Electrode Circuits

by

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This thesis is dedicated to my beautiful wife, Boyoung, my lovely son, Ian,
and to my supporting parents

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CHAPTER 1

Introduction

1.1 Motivation and Overview

Over last few years, organic light emitting devices (OLED) have attracted significant research interests from both the industries and academia. In near future, they are expected to be used in the solid-state lightings, the plane light-sources for active matrix liquid crystal display (AM-LCD) TVs, and the active-matrix organic light-emitting displays (AM-OLEDs). In general, the OLEDs have following advantages: light-weight, very thin structure, robustness to the external impact, simple fabrication process, high luminous efficiency, and fast response time. Today, it is expected that the AM-OLEDs will become future flat panel displays (FPDs).

Two thin-film transistors (TFTs) competing technologies can be used for active-matrix arrays which are hydrogenated amorphous silicon (a-Si:H) and poly crystalline (poly-Si) TFTs. The a-Si:H TFTs are more matured and well established technology while poly-silicon TFTs have better electrical performance and operational stability. Since Kodak and Sanyo demonstrated first poly-silicon based AM-OLEDs in 1999 [1], several other companies also reported several similar prototypes having different sizes [2-5]. However, due to a poor uniformity issue of poly-Si TFT electrical characteristics over large area, so far the size of the AM-OLEDs could not exceed over 30 inch. Today Sony reported the largest poly silicon based AM-OLED [5] of 27”, and they plan to introduce their 11” poly silicon based AM-OLED into the market in Dec. 2007 [6].

In 2003, Chi Mei Optoelectronics & IBM Japan showed that the a-Si:H TFTs can be also used for a large-area AM-OLEDs [7]. Recently several major display companies started to develop a large size a-Si:H TFT AM-OLEDs. In 2005, Samsung Electronics demonstrated 40" WXGA (1280 × 800 resolution) AM-OLED [8]. Although a-Si:H TFT AM-OLEDs could be fabricated over large area, a-Si:H TFTs electrical stability problem was not solved, and a complicated pixel electrode circuits are needed to compensate for the TFT threshold voltage and mobility variations. Therefore, there is a need for pixel driving methods with a simpler compensation algorithm that could be used in future a-Si:H AM-OLEDs.

In response to this very specific display needs, this dissertation presents research on technical issues relevant to the implementation of an a-Si:H TFT technology to the active-matrix organic light-emitting displays (AM-OLEDs). More specifically, a novel a-Si:H TFT pixel electrode circuits with an optimized and stable operation for high performance AM-OLED display was developed. Also for the first time, novel a-Si:H TFTs with annular or hexagonal shape electrodes for better electrical properties and stabilities were developed. Before details related to these two topics are described, below the voltage and current-driven a-Si:H TFT pixel electrode circuits used in AM-OLEDs are reviewed and compared.

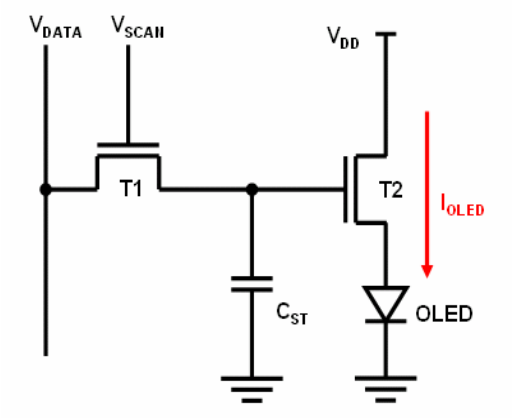
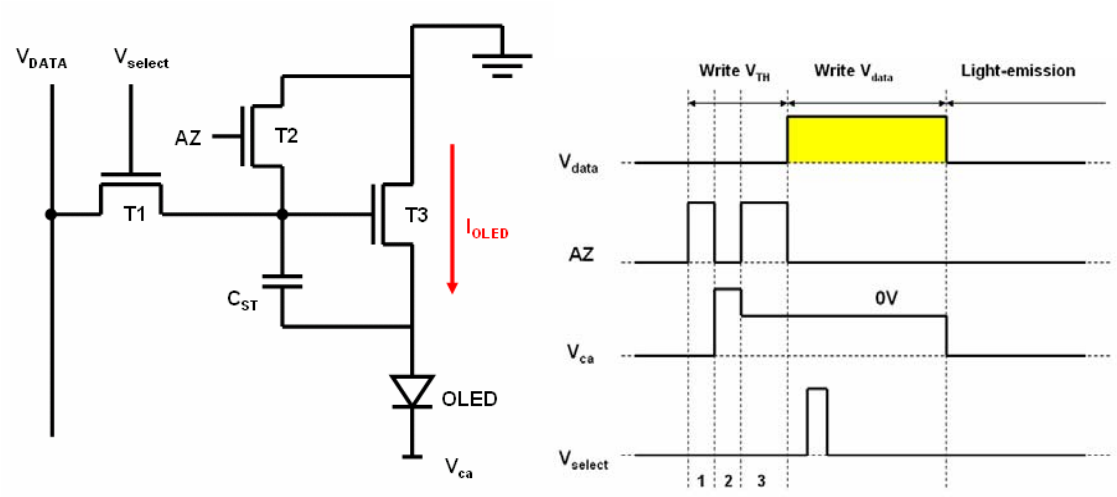


Figure 1.1 Pixel electrode circuit with 2 TFTs for AM-OLED [9].

Figure 1.1 shows a simple voltage-driven pixel electrode circuit with two n-type TFTs [9]; T1 and T2 act as a switching and a driving TFT, respectively. T1 and T2 operate in the linear and in either linear or saturation regimes, respectively. When V_{SCAN} is high (programming state), T1 is ON, and data voltage is stored at the storage capacitor (C_{ST}) through T1. Then the corresponding OLED current (I_{OLED}) flows from V_{DD} through T2 to OLED resulting in the light emission from OLED. When V_{SCAN} is low (driving state), T1 is OFF and the stored voltage at C_{ST} will determine the amount of current flowing through OLED. Therefore, if there is no change in the stored voltage at C_{ST}, the same amount of current is expected from V_{DD} through T2 to the OLED, producing a continuous pixel light-emission with the same brightness. In this simple voltage-driven pixel electrode circuit, the data voltage is equivalent to the summation of T2 V_{GS} and the voltage across the OLED. If there is any change in the turn-on voltage of the OLED or TFTs threshold voltage at a given data voltage, programmed I_{OLED} will change, resulting in non-uniform display light-emission.

To address this problem, another voltage driven pixel electrode circuit has been proposed by Stanford et al [10], which consists of three a-Si:H TFTs, one scan (V_{select}), one control (AZ), and one programmable bias line (V_{ca}) as shown in Figure 1.2 (a). T1 and T2 are switching TFTs, and T3 is a driving TFT. This pixel electrode circuit can compensate for TFT threshold voltage variations with the proper signals and timing as shown in Fig. 1.2 (b). During write V_{TH} period, V_{select} is low, isolating the V_{data} line. The threshold voltage writing (write V_{TH}) involves three steps. During 1st period, the cathode voltage, Vca, is negative and the AZ input is high, turning T2 on, and T3 operates in saturation regime. Current flows from ground through T3 to the OLED and the OLED emits the light. During this short period, the light-emission is not related to the actual data signal and will not affect the display image. During this period, T3 V_{GS},



(a) (b)

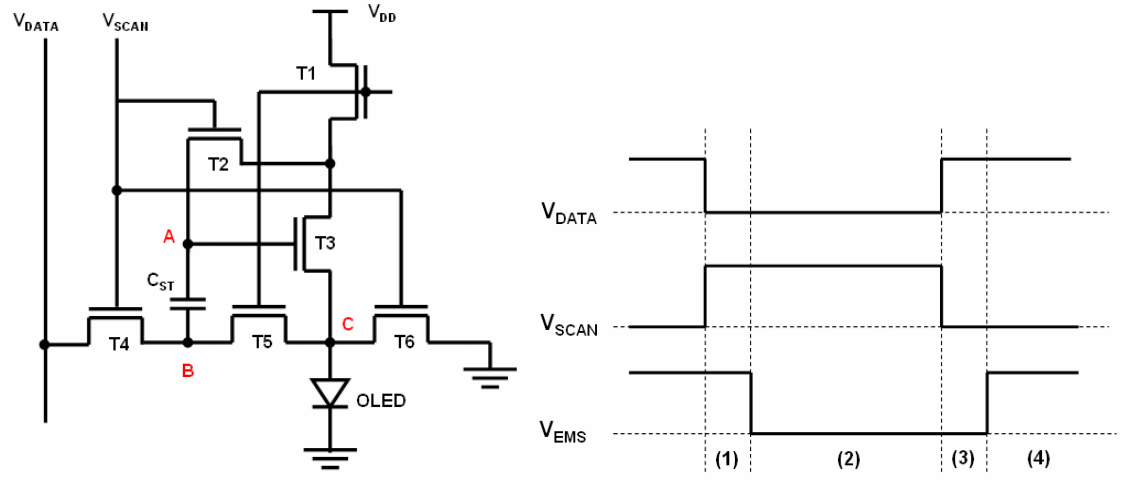
Figure 1.2 Schematics of (a) voltage-driven pixel electrode circuit with threshold voltage compensation, and (b) operational signals [10].

which is larger than T3 V_{TH}, is stored at the storage capacitor (C_{ST}). During 2nd period, V_{ca} is brought to positive voltage and AZ input is low, turning off T2. A reverse bias is applied across the OLED via the reverse conduction of T3. In addition, the gate to drain voltage and T3 drain to source voltage are reversed for removing residual charge induced during normal pixel operation. During 3rd period, V_{ca} is set at 0V and the AZ input is brought high. T3 conducts until the T3 V_{GS} is approximately equal to the T3 V_{TH} at C_{ST}. After this initial threshold voltage establishment, data signals for all pixels are written into each C_{ST} during write V_{data} period. When V_{select} is high and T1 is ON, data voltage is written into each pixel circuit of the selected row. The voltage across C_{ST} is V_{data} + V_{TH} of T3, which is maintained during the rest of the write V_{data} period (V_{select} is low and T1 is OFF). During write V_{data} period, V_{ca} is set to 0V and the AZ input is low. After the data voltage has been written to all the rows in the display, V_{ca} is brought to a negative voltage. Current flows from ground through T3 to OLED and the pixel OLED emits light. The OLED current can be expressed as following,

$$I_{OLED} \propto (V_{GS-T3} - V_{TH-T3})^2 \propto (V_{data} + V_{TH-T3} - V_{TH-T3})^2 \propto (V_{data})^2 \quad (1.1)$$

Since T3 operates in saturation regime, therefore, I_{OLED} is independent of T3 V_{TH} and is proportional to $(V_{data})^2$. In this pixel electrode circuit, AZ and V_{ca} are connected to all the pixels in the display and the pixel OLED emits the light only after the data voltage writing is finished.

J. Lee et al reported the voltage driven a-Si:H pixel electrode circuit that compensates for the a-Si:H TFT threshold voltage shift and OLED turn-on voltage variation [11]. The pixel circuit consists of six a-Si:H TFTs and one capacitor, requiring only one additional signal line V_{EMS} besides V_{data}, V_{scan}, and V_{DD}, Figure 1.3 (a) . The pixel circuit operates in four periods in each frame as shown in Fig. 1.3 (b). The first stage (1) in Fig. 1.3 (b) is a pre-charge period. V_{scan} and V_{EMS} are high so that all TFTs in the pixel are turned on. The gate node of T3 (V_A) would be charged up. During the second stage (2), a data voltage (V_{data}) is applied to node B through T4, and V_{TH} of T3 (V_{TH-T3}) is stored at node A. T1 and T5 are turned off to block a current flow from



(a) (b)

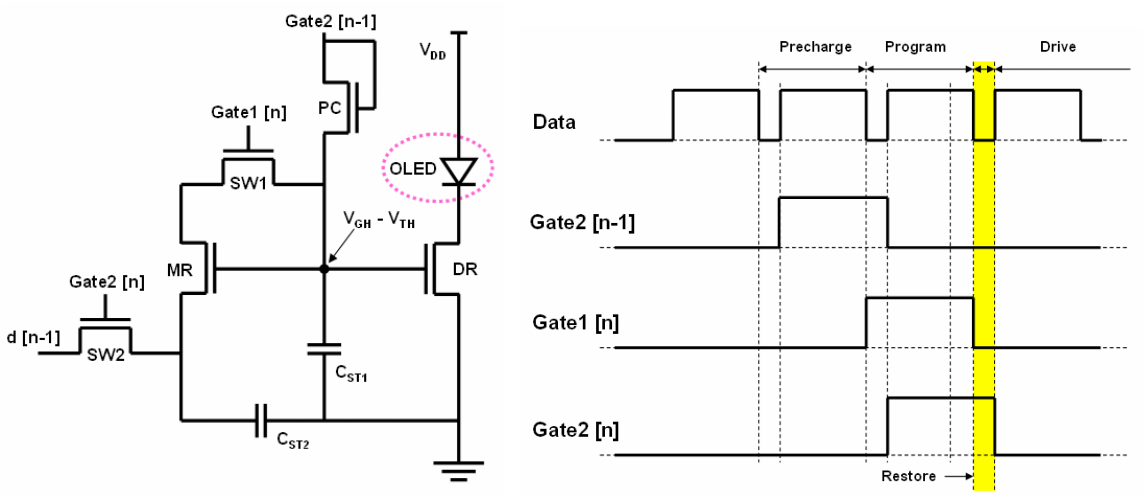
Figure 1.3 Schematics of (a) voltage-driven pixel electrode circuit with 6 TFTs, and (b) timing diagram [11].

V_{DD} and to write V_{data} to node B, respectively. T6 is turned on to block a current flow into OLED because the voltage of node C is equal to V_{SS}. The gate voltage of T3 (V_A) would be discharged through T2 and T6 until T3 was turned off so that the value of V_A would converge into the V_{TH} of T3. Storage capacitor (C_{ST}) stores the voltage difference of $V_{TH\text{-}T3}$ and V_{data}. A stored voltage at the C_{ST}, which is V_{GS} of T3 during the following emission period, should be a positive value so that Vdata should be a negative one. During the period (3), both V_{EMS} and V_{scan} signals are turned off to block the charge injection from V_{DD}. The final stage (4) is the emission period. V_{DD} is connected to the drain node of T3 through T1 and node B is connected to a source node of T3 (node C), so that a current determined by the V_{GS} of T3 would flow through OLED. The C_{ST} holds the voltage ($V_{TH\text{-}T3} - V_{data}$) until the next data is written. The threshold voltage degradation of OLED would not alter an emission current (I_{OLED}) because V_{GS} of T3 in the emission period is fixed as $V_{TH\text{-}T3} - V_{data}$ during the second stage. When the threshold voltage of OLED increases, a gate voltage of T3 also increases because the stored voltage at C_{ST} in not varied until the next data is written. I_{OLED} is the saturation current of T3, and it is independent of the threshold voltage of T3 and OLED but only affected by the data voltage as following,

$$I_{OLED} = k(V_{GS} - V_{TH-T3})^2 = k(V_{TH-T3} - V_{data} - V_{TH-T3})^2 = k(-V_{data})^2 \quad (1.2)$$

where k is (1/2L)×W×C_{OX}, C_{OX} is the gate insulator capacitor, W is channel width, and L is the channel length of T3, respectively.

Kanicki's group also reported the voltage driven pixel electrode circuit with five a-Si:H TFTs as shown in Figure 1.4 (a) [12]. The pixel circuit was developed for top-anode light emitting AM-OLED, and signal time diagram is shown in Fig. 1.4 (b). The programmed OLED current is supposed to be maintained regardless of the a-Si TFT threshold voltage variation by



(a) (b)

Figure 1.4 Schematics of (a) voltage-driven pixel electrode circuit with 5 TFTs, and (b) operational signals and timings [12].

compensating the gate node voltage of the drive TFT. Each pixel is composed of one power line (V_{DD}), two control lines (Gate1, Gate2), two capacitors (C_{ST1}, C_{ST2}) and five TFTs; two switch TFTs (SW1, SW2), a pre-charge TFT (PC), a drive TFT (DR) and a mirror TFT (MR). The pixel circuit operates in four stages; pre-charge, program, restore and drive. During pre-charge stage, previous line gate2 is high (Gate2 [n-1] = V_{GH}), which turns on the pre-charge TFT (PC). The pre-charge TFT with its drain and gate node connected act as a diode with turn-on voltage equal to the threshold voltage of pre-charge TFT (V_{THO}=$V_{TH\text{-}PC}$). Since the anode voltage of this pre-charge diode is relatively high (V_{GH}~*30V*), forcing the diode to be forward-biased, the gate node of drive TFT (DR) is pre-charged to a voltage equal to the gate high voltage minus the TFT threshold voltage (V_{GS}=V_{GH}–$V_{TH\text{-}PC}$). During program stage, previous line gate2 is low (Gate [n-1] =V_{GL}), whereas gate1 and gate2 are high (Gate1 [n] =Gate2 [n] =V_{GH}), and the data signal voltage (D[n] = V_{data}) is applied to the source node of mirror TFT (MR). The first switch TFT (SW1) connects the gate and drain of mirror TFT to form a diode, namely the mirror diode, with

turn-on voltage equal to the threshold voltage of mirror TFT (V_{THO}=$V_{TH\text{-}MR}$). Since (V_{GH} –$V_{TH\text{-}PC}$) was stored in the first storage capacitor (C_{ST1}) during pre-charge stage, and this voltage is typically much higher than V_{data}, the mirror diode is forward-biased. The gate node voltage of drive TFT, or the source node voltage of mirror TFT, is decreased as the storage capacitor is discharged through the mirror diode. The positive node of storage capacitor, or the gate node of the drive TFT, will converge to the applied data voltage plus the turn-on voltage of mirror diode (V_{GS}=V_{data}+$V_{TH\text{-}MR}$). Consequently, the threshold voltage of the mirror TFT is programmed and stored in the storage capacitor. During restore stage, gate1 is low, whereas gate2 is still high, and the data signal voltage is 0V (=*GND*). While the gate voltage of drive and mirror TFT is held at V_{data}+$V_{TH\text{-}MR}$, the source voltage of mirror TFT is decreased from V_{data} to *GND*, and restored in the second storage capacitor (C_{ST2}). The purpose of restoring the source voltage of mirror TFT to *GND* is to make the gate-to-source voltage (V_{GS}) of both mirror and drive TFTs identical for most of the drive period. Our recent studies convey that the amount of threshold voltage shift of a-Si:H TFT depends mostly on the gate-to-source voltage applied rather than to the current applied. Hence, we assume that the threshold voltages of drive and mirror TFTs are the same. During drive stage, gate2 is low, and the drive TFT drives the programmed OLED current. Since we assumed that the threshold voltages of mirror and drive TFTs are identical ($V_{TH\text{-}DR}$=$V_{TH\text{-}MR}$), the voltage stored in the storage capacitor will compensate the OLED current for the variation of drive TFT threshold voltage by canceling out the threshold voltage parameter, as derived in the following equations.

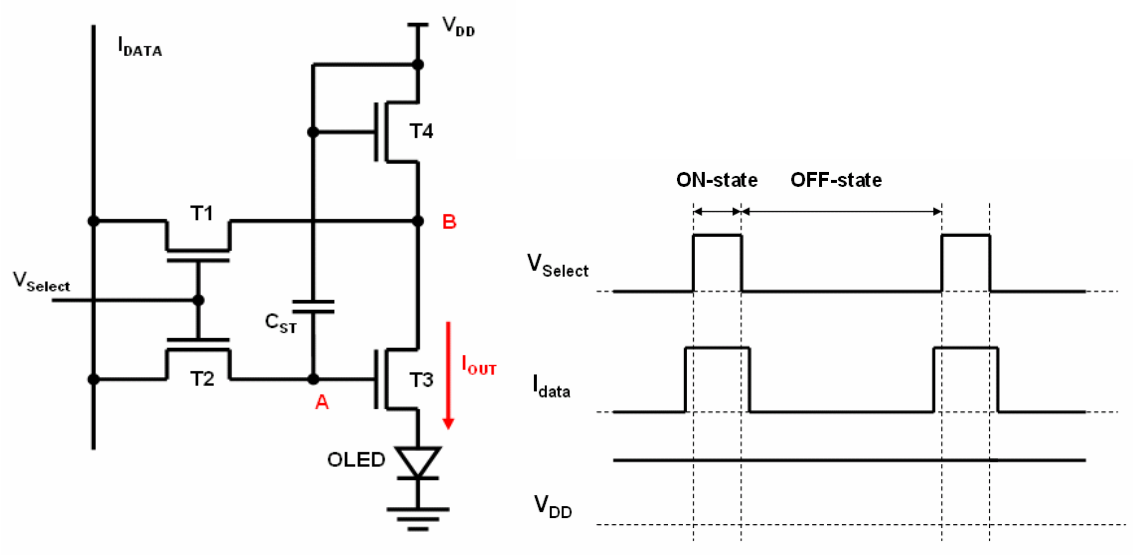
$$I_{OLED} = k(V_{GS} - V_{TH-DR})^2 = k(V_{data} + V_{TH-DR} - V_{TH-T3})^2 = k(V_{data})^2 \qquad (1.3)$$

where k is (1/2L)×W×C_{OX}, C_{OX} is the gate insulator capacitor, W is channel width, and L is the channel length of DR TFT, respectively.

Voltage driven pixel electrode circuit can successfully compensate for the TFT threshold voltage variation during display operation. The OLED threshold voltage variation can also be compensated by operating the driving TFT in the saturation regime, and therefore the OLED current flowing through the driving TFT depends only on V_{GS} not on V_{DS} of the driving TFT. As a result, although any voltage shift occurs in the OLED, it will be automatically compensated by changing V_{DS} of the driving TFT, and the current through the OLED will not change. However, these voltage-driven driving schemes can not fully compensate for the TFT field-effect mobility variations. At the same time, complicated control signals for the five or more TFTs are required to write the threshold voltage information onto each pixel, which could tremendously reduce the pixel aperture ratio in AM-OLEDs.

Alternatively, several current-driven pixel electrode circuits [13 – 16] have been reported to fully compensate for a-Si:H TFT threshold voltage and field-effect mobility variations. In addition, since OLED luminance is directly related to the current flow through the device, the current—driven active-matrix driving method can produce an uniform display brightness by directly writing data current onto each pixel.

The first current-driven a-Si:H pixel electrode circuit was reported by Kanicki's group [13], which consists of four a-Si:H TFTs as shown in Figure 1.5 (a). This circuit has four external terminals: V_{select}, I_{data}, V_{DD}, and ground (GND). The V_{select}. I_{data}, and V_{DD} are provided externally, while the OLED cathode is ground terminal. Figure 1.5 (b) shows an example of the operational waveform that can be used for these signals. When the select line (V_{select}) signal is high, both T1 and T2 are turned on. The data line signal (I_{data}) then passes through T1 and T2 and sets both the drain and gate voltages of T3. Consequently, the potentials at nodes A and B will allow the data current (I_{data}) to pass through T3. The T3 is working in the deep saturation regime, e.g. $V_{DS} > V_{GS}$



(a) (b)

Figure 1.5 Schematics of (a) current-driven pixel circuit with 4 TFTs, and (b) operational signals [13].

– V_{TH}. The V_{DD} is chosen to be lower than the T3 drain voltage to ensure that no current can flow through T4 from V_{DD}. Therefore, in this case, the current flowing through T3 is equal to I_{data}. This current then will turn on the OLED. This is called as ON-state. When the pixel circuit is deselected and the select line signal is low, both T1 and T2 are OFF. The T3 gate voltage, however, is maintained high by the charges stored in the storage capacitor C_{ST} during the ON-state. The drain voltage of T3 will drop very quickly to lower values and consequently T4 will be turned on to maintain the same level of the output current (I_{OUT}). This time current will flow from the V_{DD} to T3 via T4. If the T3 gate voltage is high and the T3 is in the saturation regime, it is expected that $I_{OUT} = I_{data}$. This is called as OFF-state. If the threshold voltage of driving TFT (T3) changes and if this change is not larger than the amplitude of V_{select} during the circuit operation, T3 gate voltage needs to be changed accordingly to ensure the same output current level. This is achieved through automatic adjustment by the current signal (I_{data}) during ON-state. Therefore,

the gate voltage of T3 is always adjusted to maintain the data current (I_{data}) level at the same value, regardless of the threshold voltage value of T3. Hence, the local V_{TH} variation of the driving TFT will not affect the output current (I_{OUT}) level. The threshold voltage shift of other TFTs in this circuit will not have a major impact on the output current level, because they are not used to control the output current.

However, the above described current-programmed pixel circuit, although it can compensate for both TFT threshold voltage, field-effect mobility variations, and OLED threshold voltage shift, has a charging time problem for data current at low gray scales in high-resolution displays. The data current must first charge up all parasitic capacitances formed between data lines and cathode before it is written onto a specific pixel within select time. Therefore, the actual charging process of each pixel might not be completed within select time since the parasitic capacitances value will increase as the number of pixels increases.

To solve this charging time issue of the aforementioned current-programming current driven pixel electrode circuit, Sony Corporation introduced a current-mirror type pixel electrode

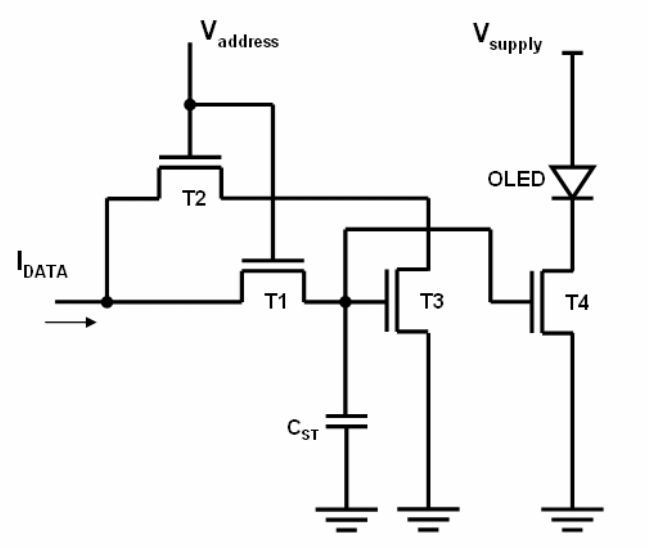


Figure 1.6 The schematic of current-mirror based current-driven circuit with 4 TFTs [15].

circuit with poly-Si TFTs [14]. Based on this concept, Sakariya et al reported the current-driven a-Si:H TFT pixel electrode circuit as shown in Figure 1.6 [15]. The pixel circuit is consisting of four a-Si:H TFTs, where T1, T2, and T3 memorized the input current by storing a voltage on the storage capacitor (C_{ST}), and T4 drives the OLED based on that voltage. T1 and T2 are switches to isolate the pixel from the rest of the array once it has been programmed. This circuit works as long as T3 and T4 have equal shifts of V_{TH}, which is a reasonable assumption since they experience the same V_{GS} stress. When the circuit is being programmed, initially all input current flows through T1 to C_{ST}. As the voltage on the C_{ST} rises, T3 turns on, and the data current is progressively diverted to the path of T2 and T3. The voltage across the C_{ST} keeps rising until all of the data current flows through T3. At that point, the data current is accurately mirrored to the OLED by T4. By setting channel width of T3 larger than that of T4, the data current is larger than the OLED current (I_{OLED}), which makes the write operation fast enough even at a low gray scale. During deselect time, T1 and T2 are turned off, and no current flows through T3. The stored charge in C_{ST} maintains a continuous current flows from V_{DD} through T4 to the OLED during the deselect time. The same amount of I_{OLED} continuously flows through OLED and a continuous light-emission can be achieved since the stored charge in C_{ST} will determine the I_{OLED} level and T4 operates in saturation regime during deselect time. This pixel programming mechanism gives the circuit its excellent stability. As V_{TH} increases, the voltage across C_{ST} is increased to compensate for it, thus keeping the OLED current constant.

Kanicki's group also reported the a-Si:H TFT current-driven pixel electrode circuit with the current scaling function, e.g. fast programming function [16]. The pixel electrode circuit consists of three switching TFTs (T1, T2, T4), one driving TFT (T3) and two storage capacitors (C_{ST1}, C_{ST2}) connected between a scan line and ground with a cascade structure, as shown in

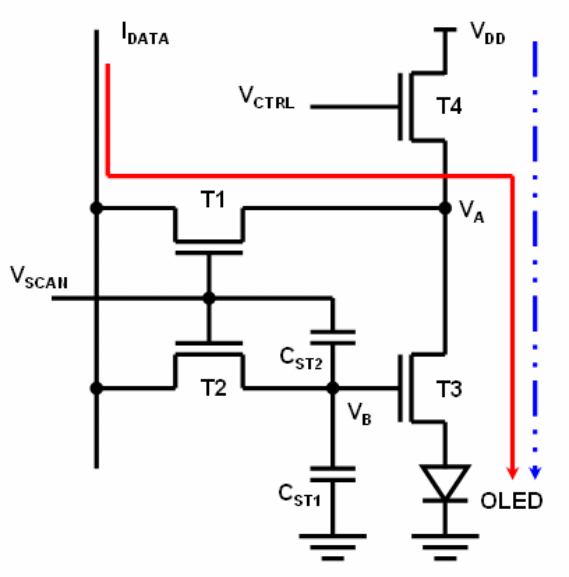


Figure 1.7 The schematic of current-driven pixel electrode circuit with 4 a-Si:H TFTs [16].

Figure 1.7. The operation of the circuit is controlled by four external terminals: V_{SCAN}, V_{CTRL}, I_{DATA}, V_{DD} and ground. The signals of V_{SCAN}, V_{CTRL}, and I_{DATA} are supplied by external drivers while the cathode of OLED is grounded. It should be noticed that to simplify the circuit analysis, one node of C_{ST1} connected to the ground is adopted. The V_{DD} electrode is connected to the external power supply to provide a constant voltage signal to the proposed pixel circuit. During the ON-state, the scan line signal V_{SCAN} turns on the switching transistors T1 and T2. During this time, a data current signal I_{DATA} passes through T1 and T3 to OLED, shown as the solid line in Fig. 1.7, and sets the voltage at the T3 drain electrode (node A). At the same time the voltage at the T3 gate electrode (node B) is set by I_{DATA} passing through T2 (dash line). The control signal V_{CTRL} turns T4 off to ensure that no current flows through T4. Consequently, in ideal case the OLED current in ON-state, $I_{OLED-ON}$, should be equivalent to I_{DATA}. Since the T3 drain and gate electrodes are at the same potential, T3 will operate in the deep saturation region, e.g., $V_{DS} > V_{GS}-V_{TH}$ (threshold voltage) and the V_A and V_B voltages at both nodes are determined

automatically according to equation (1):

$$I_{DATA} = \frac{1}{2} \cdot \mu_{FE} \cdot C_{OX} \cdot \frac{W_3}{L_3} \cdot (V_{GS} - V_{TH})^2 \tag{1.4}$$

where μ_{FE}, C_{OX}, W_3 and L_3 are field-effect mobility, gate oxide capacitance, width and length of TFT(T3), respectively. If T3 threshold voltage changes and if this change is not higher than V_{SCAN} amplitude, the T3 gate voltage, $V_{B\text{-}ON}$, will be adjusted accordingly to ensure the identical I_{DATA} in ON-state. Therefore, $V_{B\text{-}ON}$ is always adjusted to keep I_{DATA} at about the sae value regardless of a-Si:H TFT threshold voltage. The $V_{B\text{-}ON}$ will be stored in both C_{ST1} and C_{ST2} and the voltage across C_{ST2} is V_{SCAN}-$V_{B\text{-}ON}$. When the pixel changes from ON- to OFF-state, V_{SCAN} turns off T1 and T2 and V_{CTRL} simultaneously turns on T4. Because C_{ST2} is connected between the scan line and the node B to form a cascade structure with C_{ST1}, V_{SCAN} change from high to ground state will reduce $V_{B\text{-}ON}$ to $V_{B\text{-}OFF}$ due to the feed-through effect of the capacitors. $V_{B\text{-}OFF}$ can be derived from the charge conservation theory, and is given by Eq. (2), in which ΔV_{SCAN} and $C_{OV\text{-}T2}$ are an amplitude of V_{SCAN} (=$V_{SCAN\text{-}ON}$ − $V_{SCAN\text{-}OFF}$) and the gate-to-source/drain overlap capacitance of T2, respectively:

$$V_{B-OFF} = V_{B-ON} - \Delta V_{SCAN} \cdot \frac{C_{ST2} \parallel C_{OV-T2}}{C_{ST1} + C_{ST2} \parallel C_{OV-T2}} \tag{1.5}$$

A reduced T3 gate voltage, $V_{B\text{-}OFF}$, will be hold in C_{ST1} and C_{ST2} and it will continuously turn on T3 during this time period. Since the overdrive voltage of T4 (=V_{CTRL}-V_A-V_{TH}) is lower than Vdd-V_A, the T4 is working in saturation region. In order to ensure that the V_A is similar to V_{DD} and the T3 is operating in the deep saturation region, the width of T4 should be large enough to reduce the turn-on resistance of T4. A current smaller than I_{DATA} , shown as the dash line in Fig. 1.7, will be generated by $V_{B\text{-}OFF}$ and will pass through T4 and T3 to OLED. Consequently, the

	Voltage-Driven AM-OLED	Current-Driven AM-OLED
Data Signal	Voltage	Current
Data Signal Driver IC	Commercially available from AM-LCD driver IC	Development and standardization is needed.
TFT Threshold Voltage Compensation	Yes	Yes
TFT Field-Effect Mobility Compensation	No	Yes
OLED Threshold Voltage Compensation	Yes	Yes
Slow Charging Time Issue at Low Display Luminance	No	Yes, but can be solved by current-scaling function
Complexity and Pixel Aperture Ratio	Very complicated and very low aperture ratio	Less complicated and higher aperture ratio

Table 1.1 Comparison between voltage- and current-driven pixel electrode circuits for AM-OLED

OLED current in OFF-state, $I_{OLED\text{-}OFF,}$ will be smaller than I_{DATA}. Since the T3 gate voltage decreases from $V_{B\text{-}ON}$ to $V_{B\text{-}OFF}$, the OLED driving current is scale-down from ON- to OFF-state by the storage capacitor cascade structure. Consequently, when a very large data current I_{DATA} is used to charge the pixel electrode and to shorten the pixel programming time, at the same time a smaller driving current $I_{OLED\text{-}OFF}$ can be achieved for lower gray scales.

Although each pixel electrode circuit for AM-OLED has its own advantages and disadvantages, their operation principle can be summarized into two categories; voltage- and current-driven pixel electrode circuits, as shown in Table 1. In both driving scheme, the driving TFT typically operates in the saturation regime to compensate for OLED threshold voltage

variation. The voltage-driven pixel electrode circuit can be easily combined with commercially available AM-LCD data voltage driver IC. However, as aforementioned, it has a limitation of compensating for TFT field-effect mobility variations. In addition, rather complicated control signals are required to have the TFT threshold voltage compensation function in each pixel.

For the current-driven pixel electrode circuit, a specific data current driver IC is required for each pixel electrode circuit configuration. The magnitude of data current depends upon display format and pixel electrode circuit design. Therefore, standardizing data current driver ICs is needed for the commercial applications of the current-driven pixel electrode circuits, which may be very challenging. A slow charging time issue at low display luminance in the current-driven pixel electrode circuit can be solved by introducing a current-mirror or current-scaling function structures. However, a direct writing of data current onto each pixel is a big

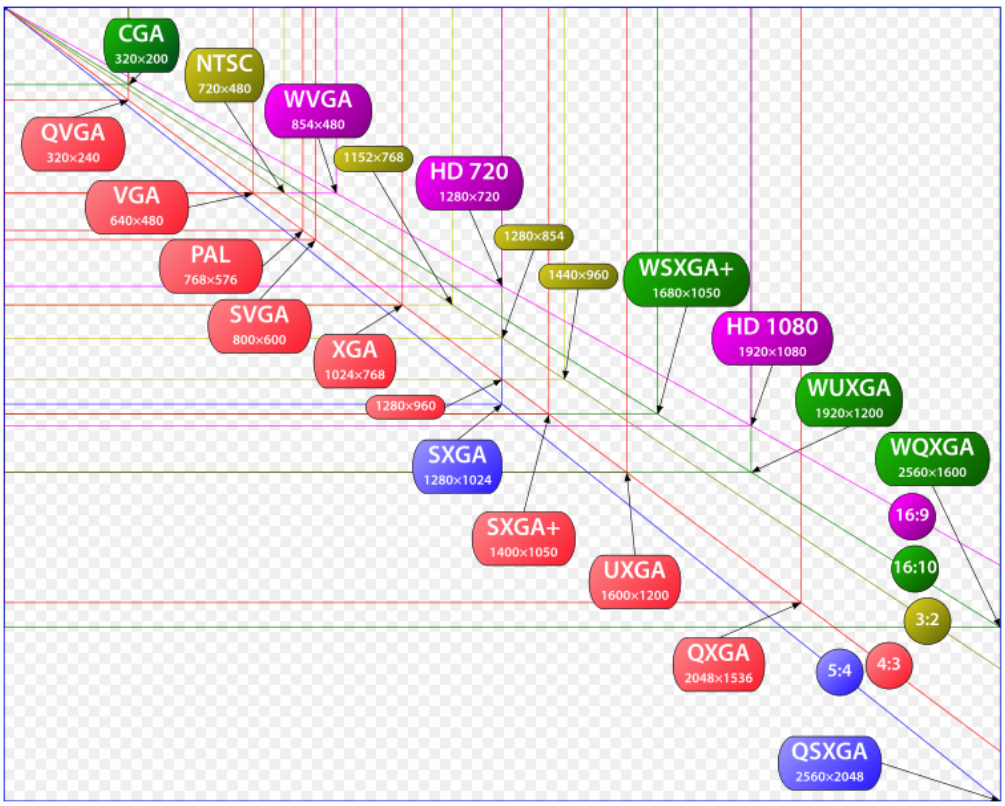


Figure 1.8 The trend of standard display resolutions [17].

advantage for current-driven pixel electrode circuit, which can fully compensate for not only TFT and OLED threshold voltage shifts but also for TFT field-effect mobility variations.

Figure 1.8 shows the trend of standard display resolutions [17], which specify the number of gate and data lines for a certain display resolution. Based on this standard figure, the single pixel size can be calculated for a given display size, and calculated pixel sizes are shown as a function of display size in Figure 1.9. Depending the display size and resolution, the pixel size varies from 50 × 138 μm^2 for 2.2" QVGA display, to 150 × 450 μm^2 for 40" WUXGA display, respectively. Therefore, for 2.2" QVGA display, the pixel area is too small for a-Si:H TFT to be used in the conventional pixel circuits with multiple TFTs mentioned above due to the larger transistor geometry than poly-Si TFT. However, above 10" VGA display, the single pixel

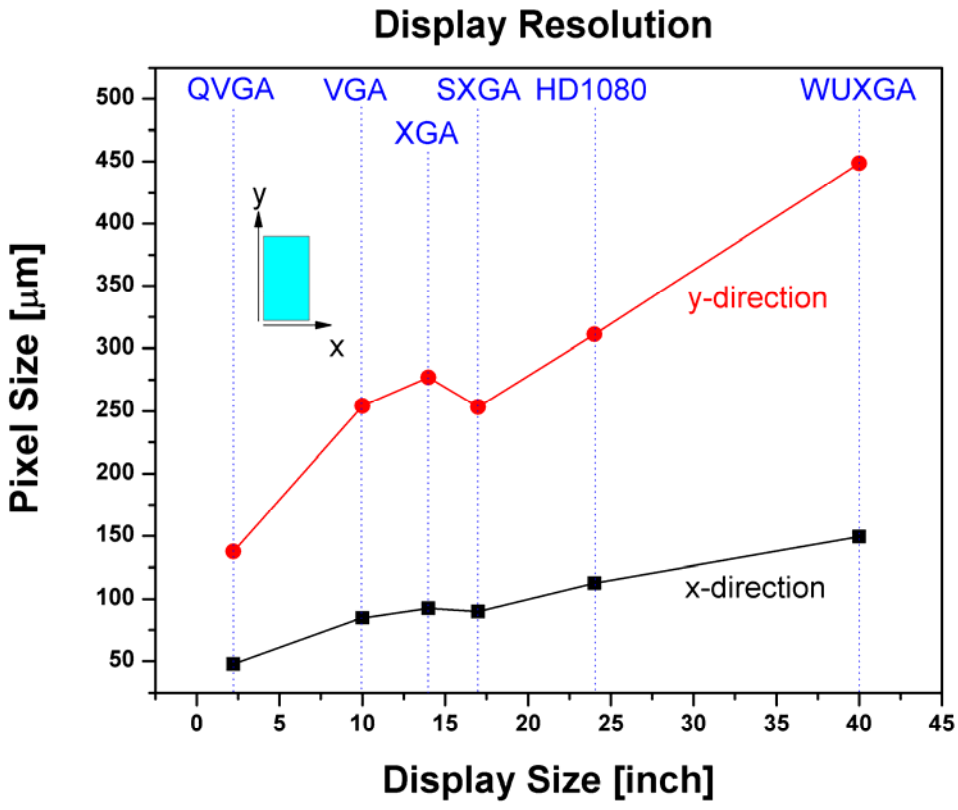


Figure 1.9 The evolution of the pixel size as a function of display size and resolution.

area is large enough so that a-Si:H TFT can be used in any conventional pixel electrode circuit. Yet, since the area per pixel is still limited and voltage-driven pixel circuits often involve complicated signal lines and more than 4 TFTs, the current-driven pixel circuit will be more beneficial to achieve larger pixel aperture ratio.

1.2 Organization of Dissertation

The organization of the thesis is as follows.

Chapter 2 describes amorphous silicon thin-film transistor (a-Si:H TFT) pixel electrode circuit with the current-scaling function that can be used for active-matrix organic light-emitting displays. The current-scaling function of the pixel electrode circuit is based on the cascade-capacitor connected to the driving TFT. In this chapter, we discusses the electrical properties of the fabricated pixel electrode circuit in comparison to the conventional current-mirror and current-driven pixel electrode circuits which were fabricated during the same process steps.

Chapter 3 proposes a novel amorphous silicon thin-film transistor (a-Si:H TFT) pixel electrode circuit with the current-scaling function which is suitable for active-matrix organic light-emitting displays. In contrast to the conventional current-mirror circuit, this circuit with the cascaded storage capacitors can provide a high data-to-OLED current ratio without increasing the a-Si:H TFT size. Moreover, since the number of signal line is reduced in the proposed pixel electrode circuit, the pixel electrode layout and the driving scheme can be simplified in comparison to previously reported cascade capacitor circuit. Finally, the proposed circuit can compensate for the threshold voltage variation of the driving TFT as well as the geometric size mismatch and temperature effect.

In Chapter 4, inverted stagger hydrogenated amorphous silicon (a-Si:H) Corbino thin-flim transistors (TFTs) fabricated with a 5-photomask process used in the processing of the active-matrix liquid crystal displays are described. We have shown that the a-Si:H Corbino TFT has the asymmetric electrical characteristics under different drain bias conditions. To extract the electrical device parameters, we developed asymmetric geometric factors for different drain bias conditions. Current-voltage measurements indicate that the ON-OFF current ratio of Corbino TFT can be enhanced significantly by choosing the outer electrode as the drain while the field-effect mobility and threshold voltage have the identical values when different drain bias conditions are used.

In Chapter 5, inverted stagger Hexagonal hydrogenated amorphous silicon thin-film transistors (HEX a-Si:H TFTs) fabricated with a 5-photomask process used in the processing of the active-matrix liquid crystal displays are proposed. We show that the output current of Hexagonal a-Si:H TFT connected in parallel increases linearly with their number within a given pixel circuit. Current-voltage measurements indicate that a high ON-OFF current ratio and a low sub-threshold slope can be maintained for multiple Hexagonal TFTs connected in parallel while the field-effect mobility and threshold voltage remain identical to a single HEX a-Si:H TFT. Due to a unique device geometry, enhanced electrical stability and larger pixel aperture ratio can be achieved in the multiple a-Si:H HEX-TFT in comparison to standard single a-Si:H TFT having same channel width. These HEX-TFT electrical characteristics are very desirable for active-matrix organic light-emitting displays.

Chapter 6 discusses the dynamic characteristics of normal and Corbino hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs); top- and bottom-gate normal a-Si:H TFTs, and bottom-gate Corbino a-Si:H TFTs were fabricated using a 5-photomask process used

in the processing of the active-matrix liquid crystal displays. The charging time and feed-through voltage (ΔV_P) measurement indicates that the normal a-Si:H TFT shows a similar behavior regardless of its TFT structure. Using a simple C_{GS} model, the dependence of ΔV_P on gate-to-source overlap and storage capacitor has been estimated by analytical calculation. Due to the unique electrode geometry, Corbino a-Si:H TFT shows a small deviation from the analytical model developed for normal a-Si:H TFT. A modified analytical model was developed for Corbino a-Si:H TFT to take into consideration this small deviation. We also developed concepts of its possible application as a switching device to active-matrix organic light-emitting displays.

Finally, the dissertation is concluded and the future work is suggested for high performance a-Si:H TFT based AM-OLED in chapter 7.

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CHAPTER 2

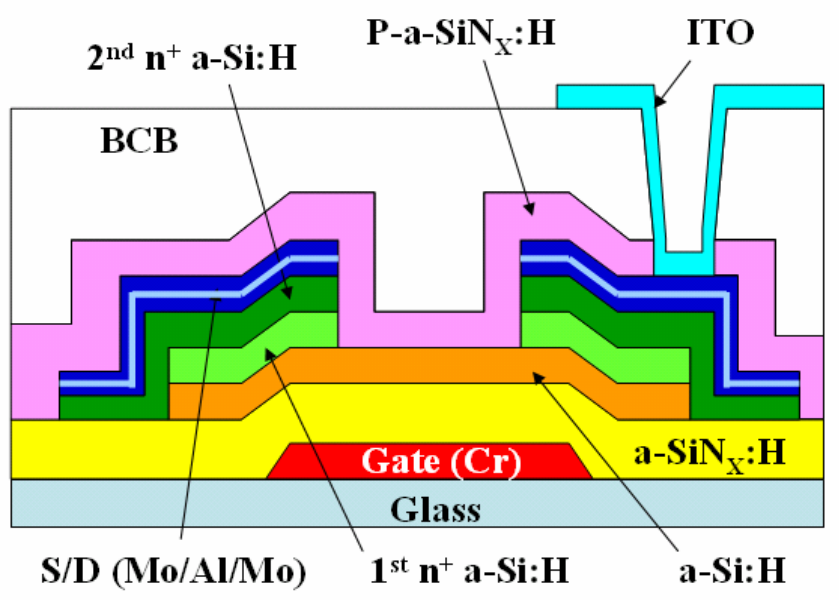
Current-Scaling a-Si:H TFT Pixel Electrode Circuit for AM-OLEDs: Electrical Properties and Stability

2.1 Introduction

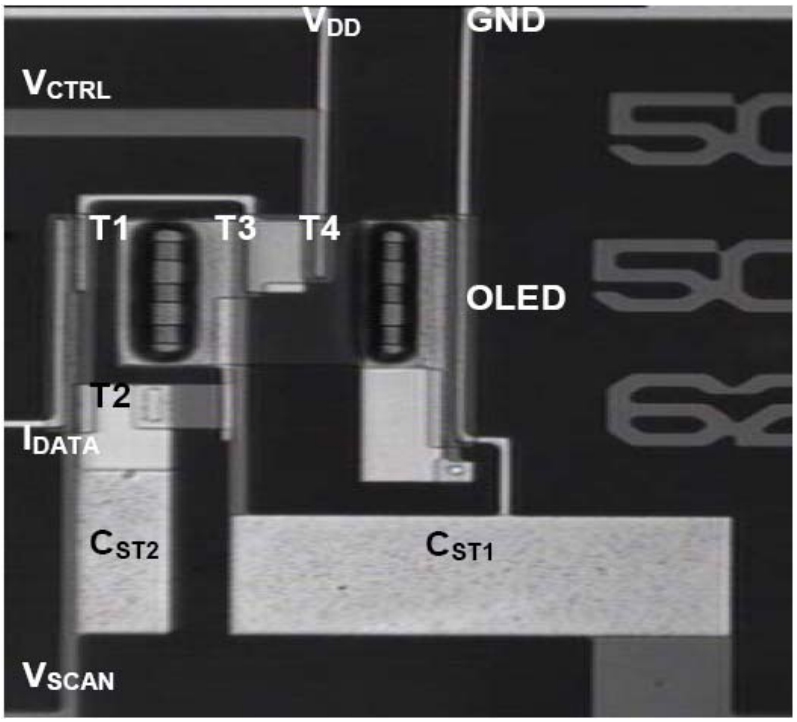
Over last several years, it was shown by several authors [1-5] that the current driving pixel electrode circuits are among the most desirable solutions for active-matrix organic light-emitting displays (AM-OLEDs). However, as display size and resolution increase, a large timing delay can be observed at a low data current and its importance increases with the display size [6]. To address this issue, several solutions have been proposed based on poly-crystalline silicon thin-film transistor (TFT) technology such as current-mirror circuit [7, 8] and series-connected TFT circuit [9]. Besides poly-Si TFTs, Sakariya et al reported the amorphous silicon TFT (a-Si:H TFT) pixel electrode circuit based on the current-mirror circuit [10]. We also proposed a-Si:H TFT based current-scaling pixel electrode circuit to address this problem [6, 11]. In this paper, for the first time, we report on electrical characteristics of the fabricated pixel electrode circuit based on this design, and present its current-scaling function in comparison with the previously published results. We also demonstrate the electrical and thermal stability of the fabricated pixel electrode circuit in comparison to the conventional current-driven TFT circuit.

2.2 Fabrication of Pixel Electrode Circuits

First, chrome layer (Cr, 2000Å) was deposited on glass substrate by a sputtering method, and then was patterned by photo-lithography process using wet-etching CR-7 solution (Mask #1) to define gate electrodes. After soaking in GP:H_2O (1:15), acetone, and methanol, the substrate was rinsed in DI water for 10 minutes, and finally blown dry with the N_2 gas. Tri-layer composed of hydrogenated amorphous silicon nitride (a-SiN_X:H, 3000Å) / intrinsic hydrogenated amorphous silicon (a-Si:H, 1500Å) / first P-doped a-Si:H layer (n^+ a-Si:H, 200Å) was deposited next in multi-chamber plasma-enhanced chemical-vapor deposition (PECVD) system at the substrate temperature of 300ºC. A gas mixture of SiH_4 and NH_3, and SiH_4 and H_2 was used for a-SiN_X:H and a-Si:H layer deposition, respectively. First 200Å thick n^+ a-Si:H layer was used to achieve a good source / drain ohmic contact to a-Si:H. After definition of the device active island by wet-etching (Mask #2), substrate was dipped in HF solution to remove native oxide before deposition of a second n^+ a-Si:H layer (300Å), which was used to realized an ohmic contact to edges of a-Si:H island. Next, molybdenum / aluminum / molybdenum (Mo/Al/Mo, 1000Å/3000Å/1000Å) multi-layer was deposited by thermal coater, and metal source / drain (S/D) contacts were defined by wet-etching (Mask #3). Acetone supersonic solution was used to remove positive photo-resist. Using S/D metal as a mask, the back-channel-etching was performed by reactive ion etching (RIE) to remove exposed n^+ a-Si:H layer between source and drain contacts. Finally, a-SiN_X:H (3000Å) top passivation layer (P) was deposited by PECVD method followed by spin coating of the benzo-cyclo-butene (BCB) planarization layer that was cured in a furnace at 250°C in nitrogen ambient. Planarized a-Si:H TFTs by BCB were already reported previously [12, 13]. The pixel electrode indium tin oxide (ITO) was connected to S/D using via formed through the BCB / P-a-SiN_X:H bi-layer by RIE (Mask #4). ITO (1200Å) was



(a)



(b)

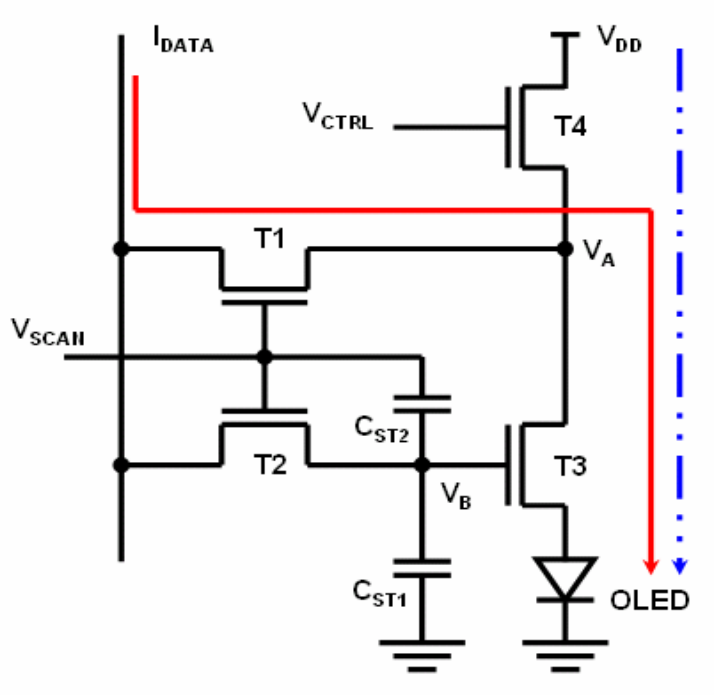
Figure 2.1 The schematic (a) cross-section and (b) top view of the fabricated a-Si:H TFT pixel electrode circuit.

deposited by a DC magnetron sputtering at room temperature, and patterned by wet-etching (Mask #5) in a mixture of HCl, HNO_3, and DI water at 60 ºC [14]. Finally, ITO was thermally annealed at 250 ºC in nitrogen. The cross-section of the a-Si:H TFT is shown in Fig. 2.1 (a).

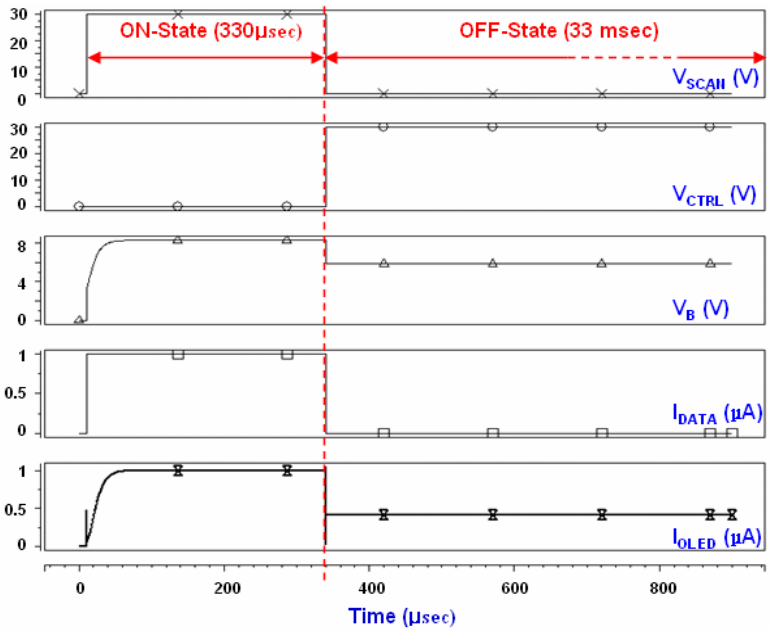
2.3 Operation of the Fabricated Current-Scaling Pixel Electrode Circuits

The fabricated current-driven pixel electrode circuit consists of three switching TFTs (T1, T2, and T4), one driving TFT (T3), and two storage capacitors (C_{ST1}, C_{ST2}) connected between a scan line and ground with a cascade structure, Figure 2.1 (b) and 2.2 (a). The organic light-emitting device (OLED) is represented here by a-Si:H TFT with gate and drain connected together, and device parameters are summarized in Table 2.1 (a). Here we define $I_{OLED\text{-}ON}$ and $I_{OLED\text{-}OFF}$ as the current flowing through OLED during the ON- and OFF-state, respectively. During the ON-state, V_{SCAN} turns on the T1 and T2, and I_{DATA} (=$I_{OLED\text{-}ON}$) passes through T1 and T3 to OLED while the T4 remains turned-off by V_{CTRL}, shown as the solid line in Fig 2.2 (a). When the pixel changes from the ON- to OFF-state, V_{SCAN} turns off T1 and T2, and V_{CTRL} simultaneously turns on T4. Since gate bias of T3 (V_{B_ON}) is reduced to V_{B_OFF} by the ratio of cascaded capacitor ($V_{B\_OFF} = V_{B\_ON} - \Delta V_{SCAN} \cdot C_{ST2} / (C_{ST1}+C_{ST2})$), a scaled-down data current (I_{OLED_OFF}) will flow through OLED, shown as the dashed line in Fig 2.2 (a). To achieve the accurate current scaling by the ratio C_{ST2} and C_{ST1}, we need to consider a parasitic capacitance effect on V_B node potential. Per our previously published discussion [6], When the overlap parasitic capacitance of T2 ($C_{OV\text{-}T2}$) is considered, $I_{OLED\text{-}OFF}$ can be expressed as:

$$I_{OLED-OFF} = \beta(V_{GS} - V_{TH} - V_{offset})^2 = \beta(\sqrt{\frac{I_{OLED-ON}}{\beta}} - V_{offset})^2 \quad (2.1)$$



(a)



(b)

Figure 2.2 Schematic of (a) the cascaded-capacitor pixel electrode circuit and (b) operational wave forms simulated by HSPICE.

$$= I_{OLED-ON} - 2\sqrt{\beta \cdot I_{OLED-ON}} \cdot V_{offset} + \beta \cdot V_{offset}^2$$

$$\text{with } V_{B-OFF} = V_{B-ON} - V_{offset}\text{, where } V_{offset} = \Delta V_{SCAN} \frac{C_{ST2} \parallel C_{OV-T2}}{C_{ST1} + C_{ST2} \parallel C_{OV-T2}} \quad (2.2)$$

where $\beta = (1/2)\mu_{FE} \cdot C_{OX} \cdot W_{T3} / L_{T3}$. As shown in the equation, since the parasitic capacitance of T2 is connected to C_{ST2} in parallel, when the status of TFT (T2) is changed from ON to OFF, a kickback effect can occur. The kickback effect is defined here as the abrupt drop of $V_{B\text{-}OFF}$ originated from the charge sharing between the parasitic capacitance and the storage capacitance. To prevent this effect, we designed and fabricated TFT (T2) as small as possible. Hence, we could minimize this effect in pixel circuit operation. More details analysis of this pixel circuit operation can be found in [6].

2.4 Pixel Electrode Circuit Measurement Details

To analyze the electrical performance of the pixel circuit, we measured $I_{OLED\text{-}ON}$ and $I_{OLED\text{-}OFF}$ flowing through the OLED by applying I_{DATA}, V_{CTRL}, and V_{SCAN} as shown in Fig. 2.2 (b). At the same time, constant DC V_{DD} and ground (GND) were applied. All measurements were done at room temperature, and all signals were applied using HP8110A function generator through a probe station. The time for ON- and OFF-state was set to 0.33 and 33ms, respectively. During ON-state, V_{SCAN} and V_{CTRL} were held at 30 and 0V, respectively while I_{DATA} was swept from 0.2 to 10 μA for each measurement. During OFF-state, V_{SCAN} and V_{CTRL} were changed to 0 and 30V, respectively while I_{OLED} was measured with V_{DD} set at 30V. It should be noted that the I_{DATA} must be turned off when the circuit operation changes from ON- to OFF-state. Otherwise,

Proposed pixel circuit	
W/L (T1, T3) [μm]	50/4
W/L (T2) [μm]	30/4
W/L (T4) [μm]	40/4
W/L OLED [μm]	150/4
C_{ST1} [pF]	2.5
C_{ST2} [fF]	210 / 312 / 625

(a)

Coventional current-driven pixel circuit	
W/L (T1, T2, T3) [μm]	100/4
W/L (T4) [μm]	150/4
W/L OLED [μm]	150/4
C_{ST} [pF]	2.5

(b)

Current-mirror pixel circuit	
W/L (T1, T2) [μm]	100/4
W/L (T3) [μm]	200/4
W/L (T4) [μm]	50/4
W/L OLED [μm]	150/4
C_{ST} [pF]	2.5

(c)

Table 2.1 Listing of the device geometrical parameters used in (a) proposed cascade-capacitor (Fig 1a) (b) convention current-driven (Fig. 5a) and (c) current-mirror (Fig. 5b) pixel electrode circuits.

the measured V_{DATA}, when I_{DATA} is supplied, will increase to high value (>40V) to keep the current flowing when T1 and T2 are turned off, since the probe of I_{DATA} is set to the current supply mode. This high V_{DATA} can result in a large T2 leakage current, which increase the voltage at node B (V_{B_OFF}). Accordingly, the I_{OLED_OFF} will also increase since V_{B_OFF} increases.

Therefore, for proper circuit operation, I_{DATA} should be turned-off during OFF-state as

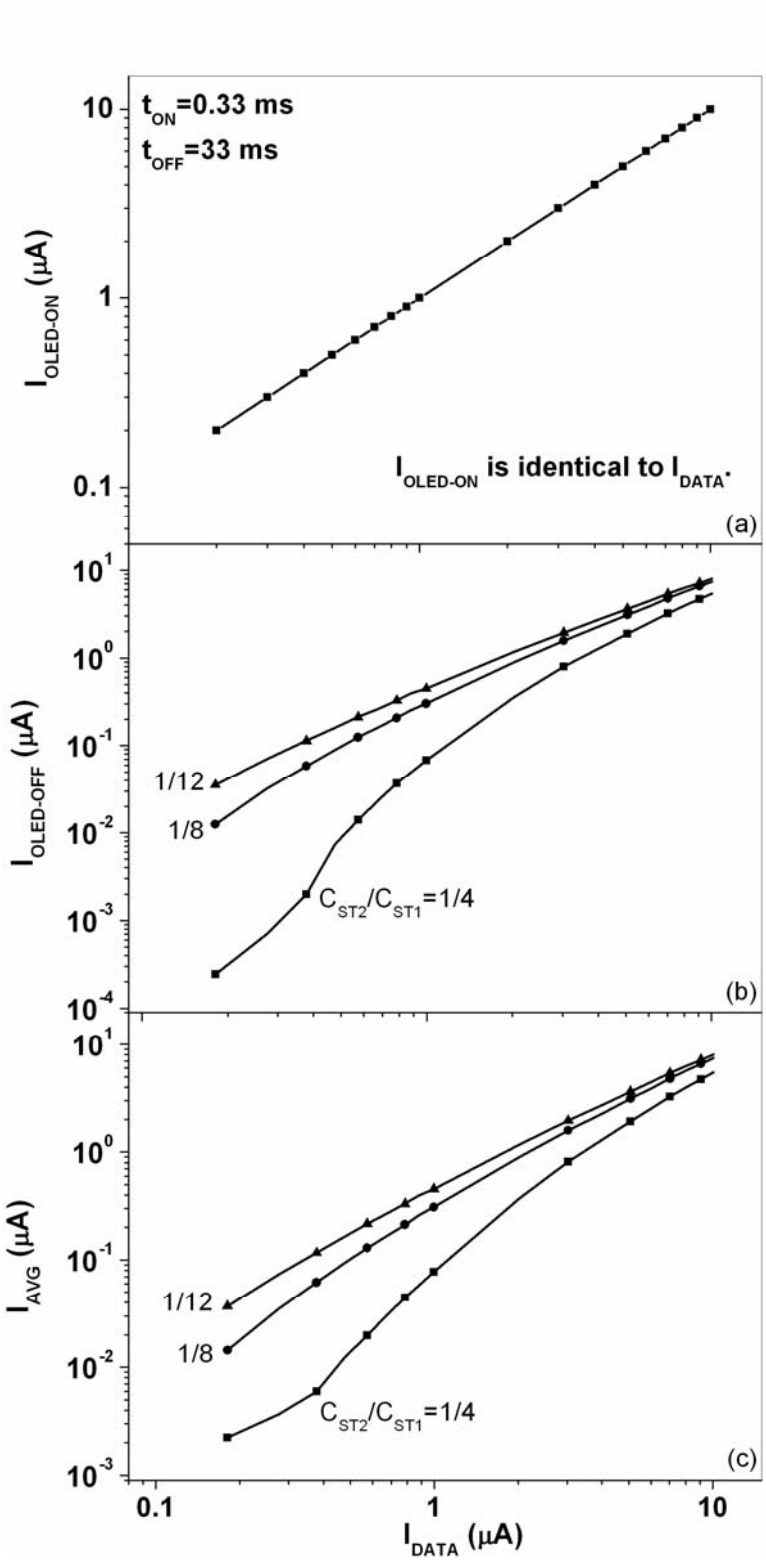
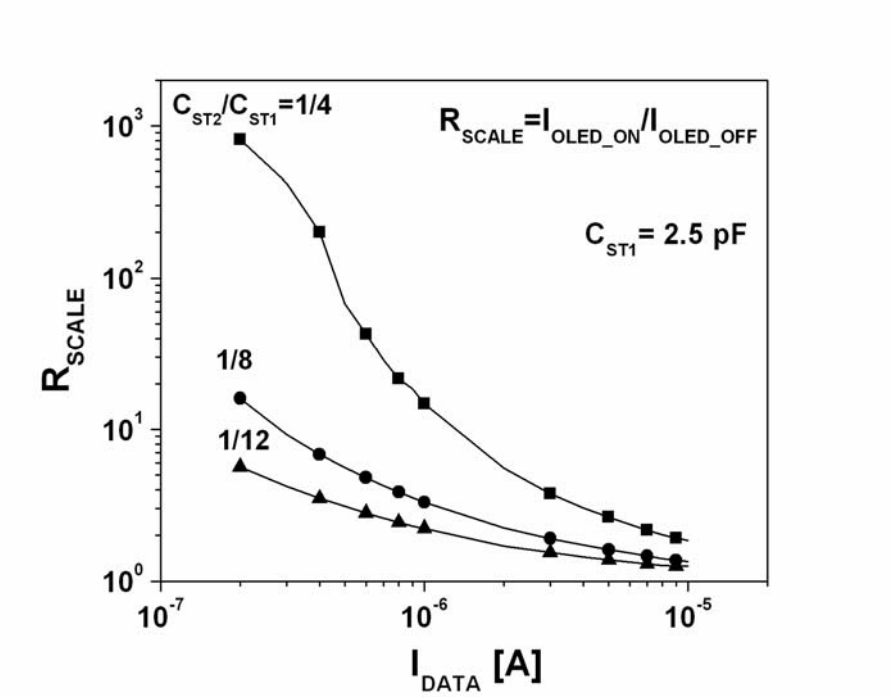


Figure 2.3 Variation of the measured I_{OLED_ON}, I_{OLED_OFF} and I_{AVE} as a function of I_{DATA} (=I_{OLED_ON}) for various C_{ST2}/C_{ST1} ratios.

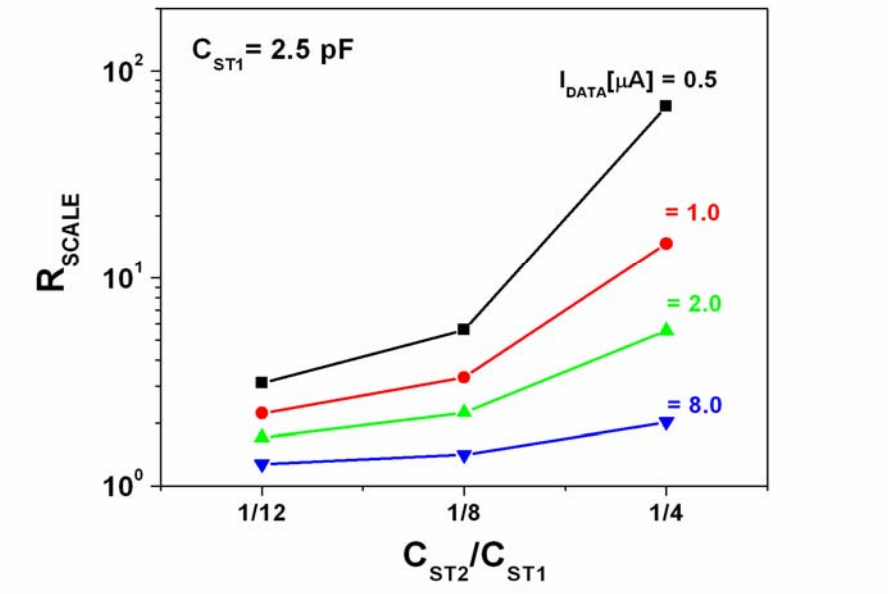
shown in Fig. 2.2 (b). However, even though the I_{DATA} was turned off, the measured I_{OLED_OFF} decreased slightly during OFF-state due to T2 current leakage, which originated from the voltage difference between source and drain electrodes. This current leakage causes the V_{B_OFF} to decrease. To reduce the variation of V_{B_OFF}, the following steps were taken: (i) the value of V_{DATA} during ON-state was measured while supplying DC I_{DATA}. Since the resistance of T1 was very small during ON-state, the voltage at node B (V_{B_ON}) was expected to be the same as measured V_{DATA}. (ii) Then, V_{DATA} obtained in step (i) was applied instead of I_{DATA} on the data line during ON-state. Since the V_{DATA} was same as V_{B_ON} and it would supply the same current as I_{DATA}, the voltage levels during OFF-state between source and drain of T2 could be very similar so that the T2 leakage current was negligible and I_{OLED} was stable during OFF-state. When this pixel circuit is used in a display active-matrix array, in ideal case, the potential of V_B node should not change with the SCAN line addressing. However, in practice, due to the leakage current through TFT (T2), varying V_{DATA} can introduce an variation of V_B resulting in the vertical cross-talk. This effect can be prevented by inserting TFT in series between data line and the common node of T1 and T2 drain.

2.5 Electrical Properties of the Current-Scaling Pixel Electrode Circuit

To investigate the current scaling ratio of the fabricated pixel electrode circuit, we changed the I_{DATA} from 0.2 to 10μA and measured the corresponding I_{OLED_ON} and I_{OLED_OFF} flowing through the diode for different ratios of cascaded-capacitors. In ON-state, the I_{OLED_ON} is identical to the data current (I_{DATA}) since the external driver directly controls the OLED current, Fig. 2.3 (a). When the pixel circuit operates in OFF-state, the diode current (I_{OLED_OFF}) is scaled-



(a)



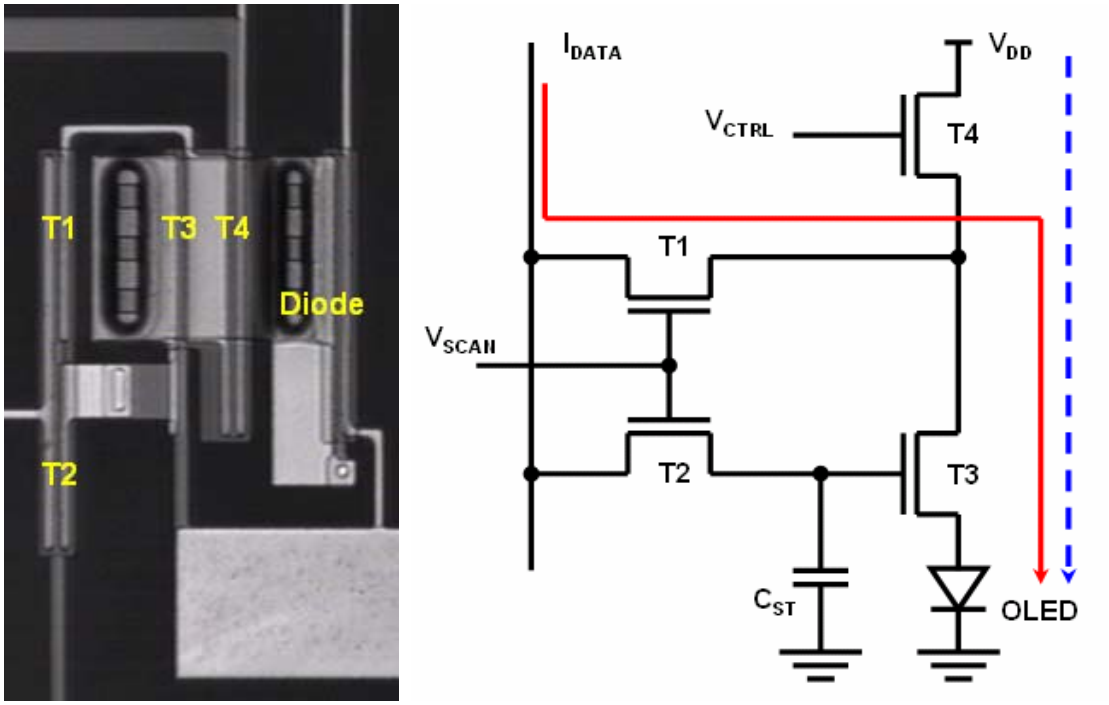
(b)

Figure 2.4 Variation of the measured current scaling ratio as a function of (a) I_{DATA} and (b) ratio of storage capacitances for fabricated cascaded-capacitor pixel circuit.

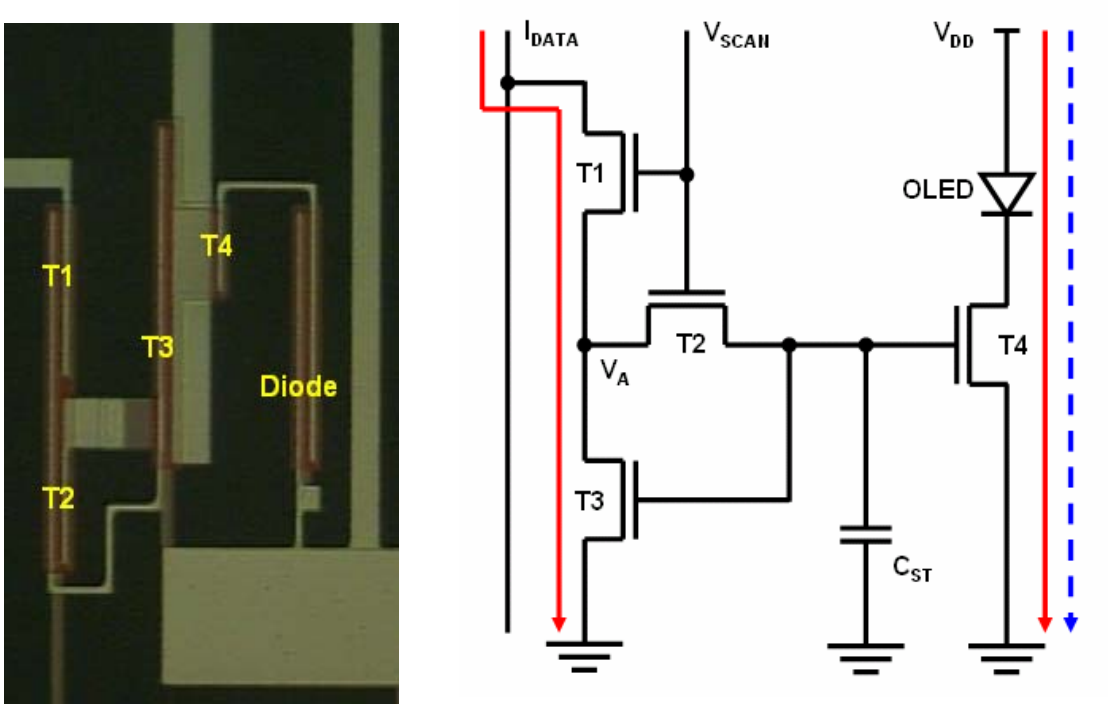
down by the ratio of cascade capacitor as discussed above and in [11]. From Fig. 2.3 (b), it is obvious that the larger C_{ST2}/C_{ST1} results in significant decrease of the I_{OLED_OFF} at lower I_{DATA}. However, as shown previously [11], too large ratio of C_{ST2}/C_{ST1} (> 1/3) resulted in the saturation of I_{OLED_OFF}, which eventually deteriorate the current scaling function.

Since the OLED current value is different during ON- and OFF-state, we define the average OLED current (I_{AVE}) during one frame time [11] as $I_{AVE}= (I_{OLED\_ON} \cdot t_{ON} + I_{OLED\_OFF} \cdot t_{OFF}) / (t_{ON} + t_{OFF})$, where t_{ON} and t_{OFF} is the ON- and OFF- period during the frame time, respectively. The variation of I_{AVE} versus I_{DATA} in one frame period ($t_{ON} + t_{OFF}$) for different C_{ST2}/C_{ST1} ratios is shown in Fig. 2.3 (c). Since the OFF-state period is much longer than ON-state, though I_{OLED_OFF} is very small during OFF-state, it can reduce the I_{AVE} even if the I_{OLED_ON} ($=I_{DATA}$) is large. For example, the fabricated pixel electrode circuit can generate I_{AVE} ranging from 2 nA to 5 μA while I_{DATA} swept from 0.2 to 10 μA. Therefore, during one frame time, we can achieve a very wide dynamic range of OLED current levels by supplying high data current levels.

The evolution of the scaling ratio ($R_{SCALE}= I_{OLED\text{-}ON}/I_{OLED\text{-}OFF}$) for different ratios of C_{ST2}/C_{ST1} as a function of I_{DATA} is shown in Fig. 2.4 (a). In this figure, we can see that for C_{ST2}/C_{ST1}=1/4, R_{SCALE} decreases from 816 to 1.9 as I_{DATA} increases from 0.2 to 10μA, and an ideal non-linearity of R_{SCALE} can be achieved; e.g. a very high R_{SCALE} at low I_{DATA} levels (low gray scales) and a low R_{SCALE} at high I_{DATA} levels (high gray scales) can be produced. The variation of R_{SCALE} with the C_{ST2}/C_{ST1} is also shown in Fig. 2.4 (b). The measured results show that for fixed I_{DATA}, R_{SCALE} increases as C_{ST2} increases from 210 to 625 fF, corresponding to an increase of C_{ST2}/C_{ST1} from 1/12 to 1/4. For constant C_{ST2}/C_{ST1}, R_{SCALE} increases as I_{DATA} decreases as shown in Fig. 2.4 (a). Therefore, for a fixed ratio of C_{ST2}/C_{ST1} calculated for a given pixel



(a)



(b)

Figure 2.5 The top view of fabricated (a) conventional current-driven and (b) current-mirror pixel electrode circuits based on a-Si:H TFTs.

electrode circuit design, we can expect to achieve a certain output OLED current range. These experimental results are in full agreement with the simulated results previously reported [11].

2.6 Comparison with Other Pixel Electrode Circuits

To demonstrate the current-scaling function of the proposed pixel electrode circuit in comparison with both the conventional current-driven [4] and current-mirror pixel circuits [7], we fabricated all three pixel electrode circuits using the same a-Si:H TFT technology as shown in Fig. 2.1 and Fig. 2.5. The device parameters of transistors and capacitors used in different pixel electrode circuits are summarized in Table 2.1. Then we measured I_{AVE} as a function of I_{DATA} for each pixel electrode circuit as shown in Fig. 2.6. Since I_{OLED_ON} for all three circuits was identical to I_{DATA}, the current-driven circuit did not show any current-scaling function. On the contrary, while the current-mirror circuit showed only a fixed current-scaling by the ratio of T4/ T3 over all I_{DATA} range ($I_{OLED} = (W_4 \cdot L_3)/(L_4 \cdot W_3) \cdot I_{DATA}$), the proposed cascaded-capacitor pixel circuit showed non-linear current-scaling function for variable current-scaling ratio depending on I_{DATA}. When I_{DATA} varies from 2×10^{-7} to 10^{-5} A, the proposed cascaded-capacitor pixel circuit with the

ratio of C_{ST2}/C_{ST1}=1/4 can provide I_{AVE} ranging from 2×10^{-9} to 5.4×10^{-6} A. Hence much wider dynamic range of I_{AVE} levels can be achieved by this circuit in comparison with the conventional current-driven pixel circuit (2×10^{-7} to 10^{-5} A) and the current-mirror pixel circuit (10^{-8} to 2×10^{-6} A). At the same time, as shown in the figure, for the given pixel design, e.g. 14" XGA resolution display where a typical single pixel size is 93 μm × 279 μm, the proposed circuit can achieve a

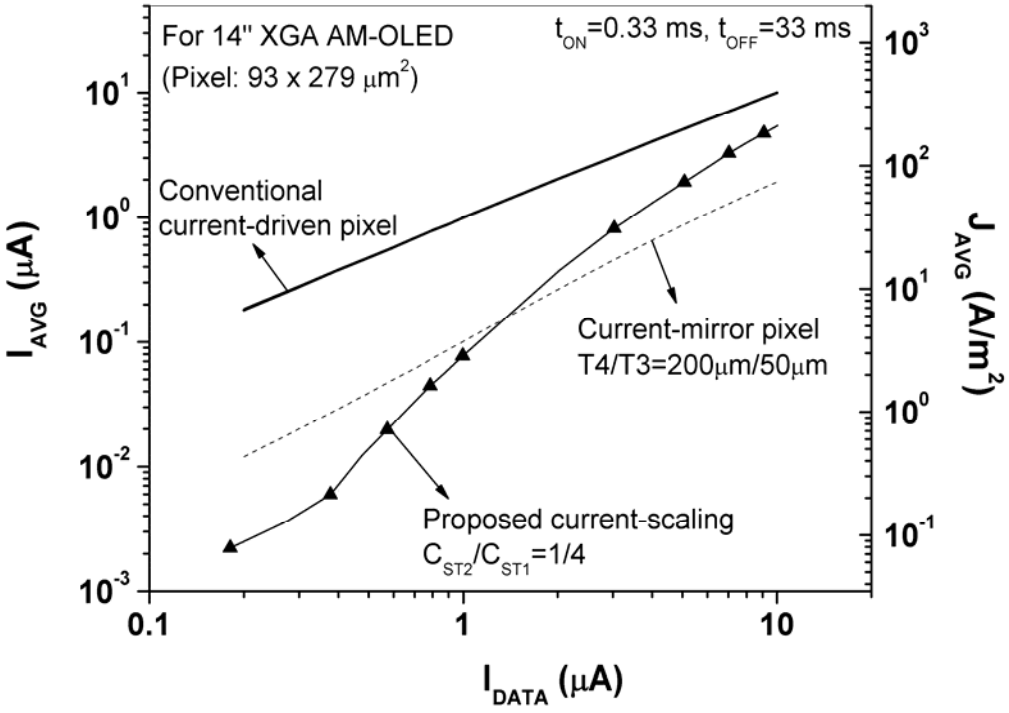


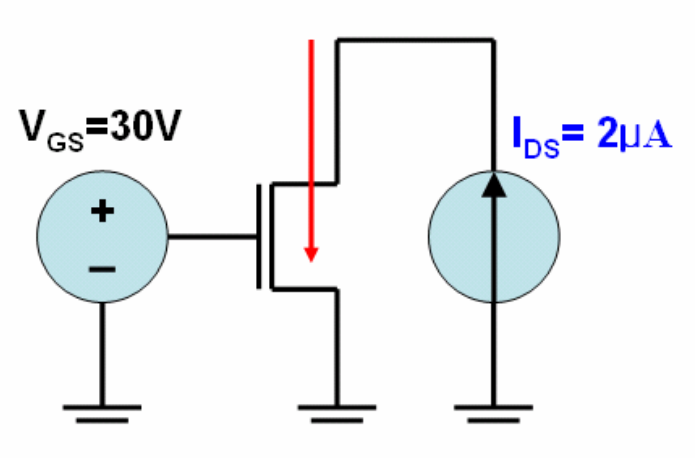
Figure 2.6 Comparison of I_{AVE} and J_{AVE} versus I_{DATA} for conventional current-driven, current-mirror, and proposed pixel circuits.

wide current density (J_{AVE}) range from 0.09 to 210 A/m^2 while the conventional current-driven and current-mirror circuits show a range of J_{AVE} from 7.0 to 387 A/m^2, and from 0.46 to 74 A/m^2, respectively. Therefore, for a given emissive organic material with a fixed emission efficiency (EE), the propose pixel circuit can express much wider luminance levels (gray scale) for given input data current levels without addition power consumption.

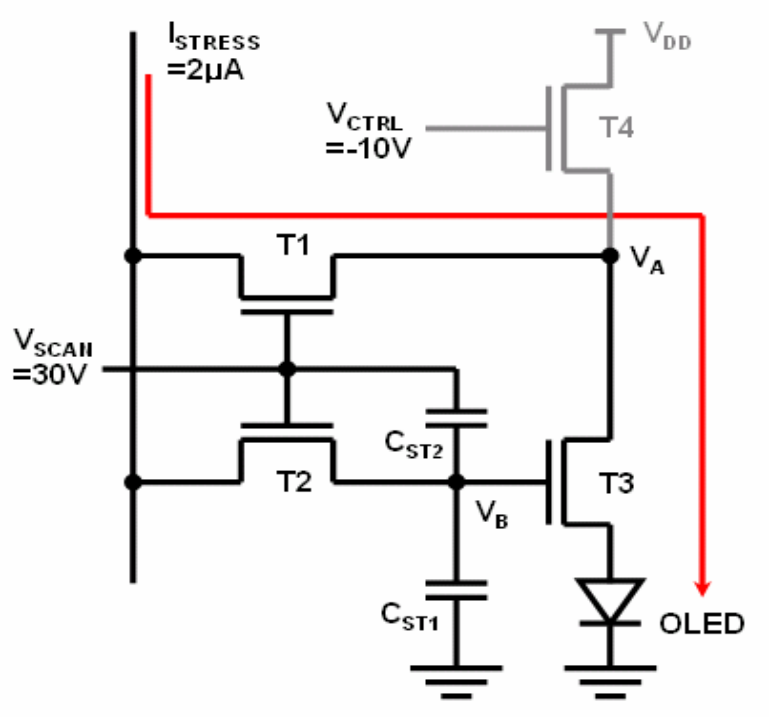
2.7 Electrical Stability of the Fabricated Pixel Electrode Circuit

2.7.1 a-Si:H TFT Stability Measurement

To evaluate the thermal and electrical stability of our fabricated pixel electrode circuit, we



(a)



(b)

Figure 2.7 The schematics of the current-temperature stress measurement set-up used for (a) single a-Si:H TFT and (b) proposed pixel electrode circuit stability study.

performed the current temperature stress (CTS) experiment for both single TFT and pixel electrode circuit, Figure 2.7. For the single TFT CTS measurement, we applied a constant gate bias of 30V (V_{GS}=30V) continuously to the TFT while the drain current was set to 2.0 μA (I_{DATA}=

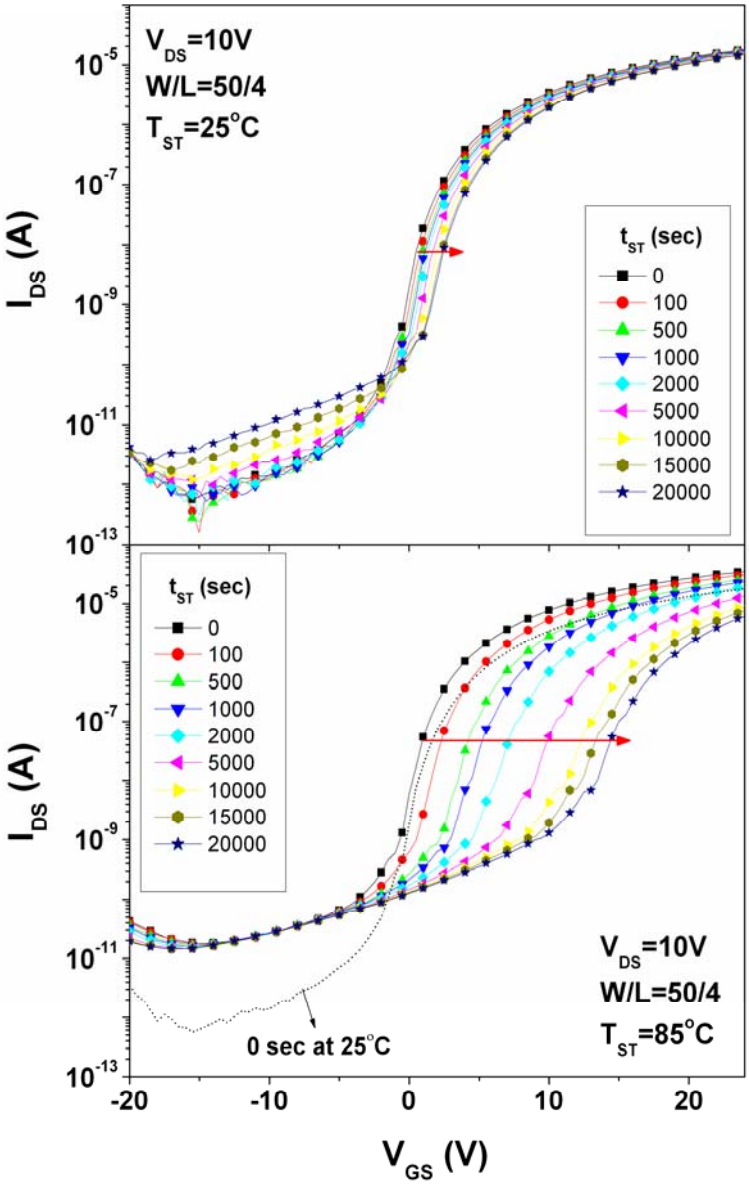


Figure 2.8 The transfer characteristic of TFT (W/L=50/4) after current-stress (I_{DATA}=2μA) as a function of stress time (a) at room temperature (25ºC) and (b) at 85ºC.

2.0 μA), and measured the transfer characteristics of TFT with V_{DS}=10V at the room temperature (25 ºC) for different stressing times (t_{ST}) ranging from 0 to 20000 seconds, Figure 2.8 (a). The stress current value of 2.0μA was determined to achieve the luminance of 500cd/m^2 when the emission efficiency of OLED is 2.5cd/A for the pixel size of 100×100 μm^2. We only stopped device stressing to measure the transfer curves between stress times. We also measured the transfer characteristics of TFT under the accelerated stress condition by raising the stress temperature (T_{ST}) up to 85 ºC, while all bias conditions remained the same (V_{GS}=30V and I_{DATA}=2μA). As shown in Figure 2.8 (b), the transfer curve changes dramatically with the increasing stress time when the temperature is set at 85 ºC. From the transfer characteristics, the threshold voltages are extracted by the maximum slope method [15] for different stressing times and temperatures. As the stressing time increases from 0 to 20000 seconds, the threshold voltage shift (ΔV_{TH}) at 25 ºC increases from 0 to 1.98 V, while ΔV_{TH} at 85ºC increases from 0 to 13.99V, Figure 2.9 (a). At the same time, the field-effect mobility (μ_{FE}) at 85ºC decreases from 0.68 to 0.52 cm^2/V·sec, while μ_{FE} at 25ºC shows small variation from 0.34 to 0.32 cm^2/V·sec with the stress time. It should be noted that the sub-threshold swing at 85ºC shows small variation while it does not change at 25 ºC with the stress time, which can be related to the increase of the interface states at 85ºC with the stress time. The detailed mechanism responsible for these variations of TFT characteristics were discussed in the previous study [16]. All device measurements were done at the stress temperature.

2.7.2 Pixel Electrode Circuit Stability Measurement

Based on the CTS measurement conditions specified above, we evaluated the stability of

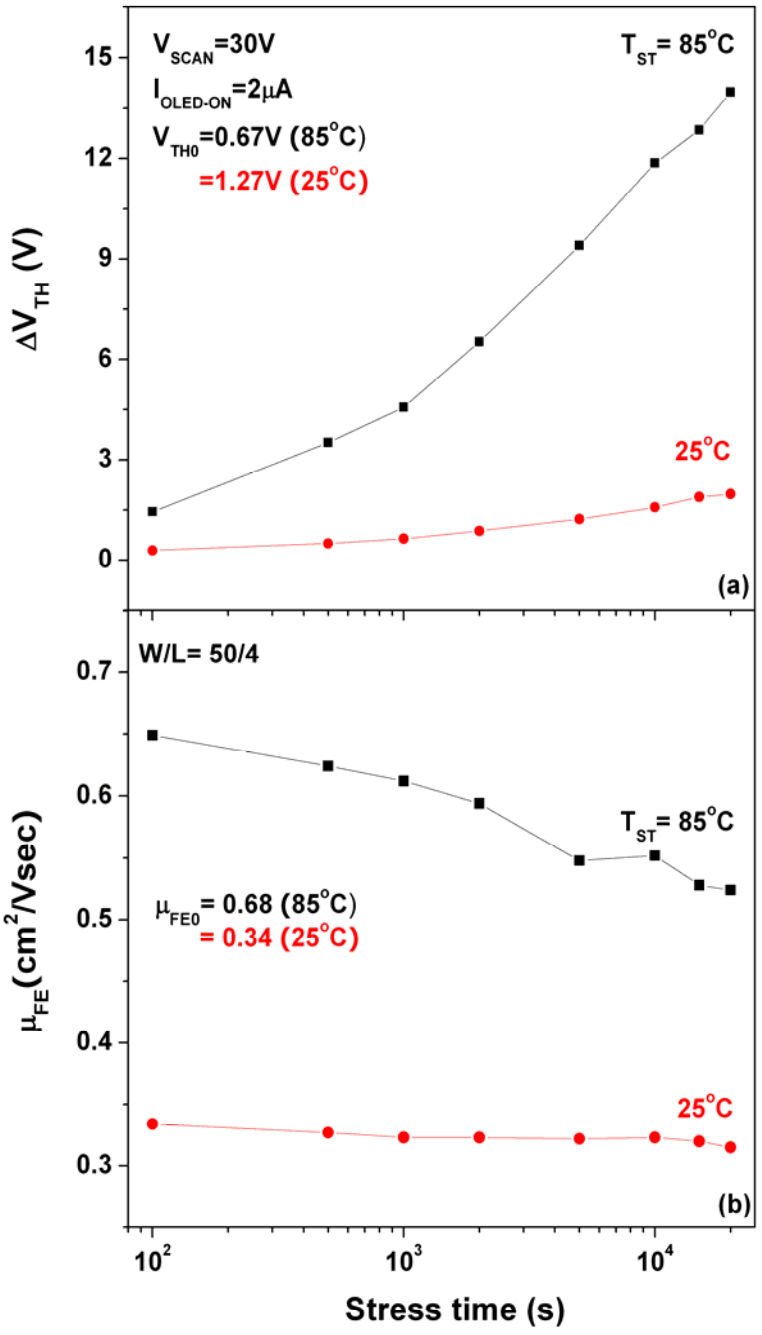


Figure 2.9 Variations of threshold voltage and field-effect mobility of a-Si:H TFT (W/L= 50/4) as a function of stress time at 25 and 85ºC.

the fabricated pixel electrode circuit as a function of the bias stress time. For an accelerating stress condition, the stress temperature of the glass substrate was set up at 85ºC. Then we set the scan and control bias as 30V and -10V, respectively (V_{SCAN}= 30V and V_{CTRL}= -10V). To stress the pixel electrode circuit, the data current (I_{DATA}) of 2μA was supplied to the data electrode during various stress times from 0 to 20000 seconds. After each current stress, we changed the bias condition to the normal measurement set-up described previously, and measured the OLED OFF-current ($I_{OLED-OFF}$) for various data current levels (I_{DATA}= 0.2, 1.0, and 5.0μA) to investigate the stress effect on the OLED current behavior. For the direct comparison, we performed the CTS measurement of the conventional current-driven circuit [4] under the same experimental

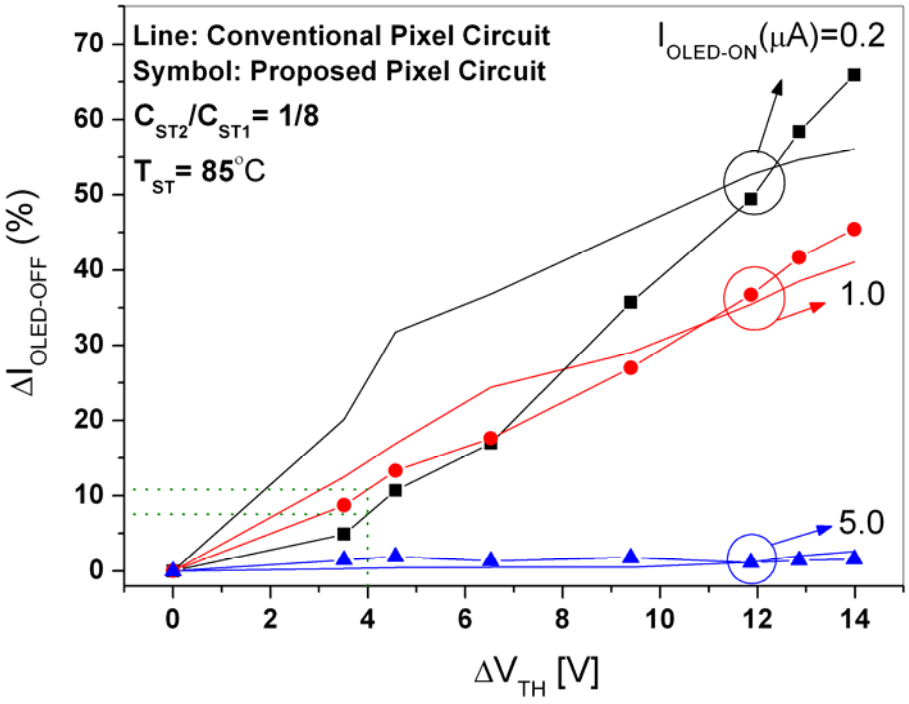


Figure 2.10 Variations of the OLED OFF-current ($\Delta I_{OLED-OFF}$) of the proposed pixel circuit as a function of threshold voltage shift (ΔV_{TH}) at 85ºC in comparison to the conventional current-driven pixel circuit.

conditions. Figure 2.10 shows the variation of $I_{OLED\text{-}OFF}$ ($\Delta I_{OLED\text{-}OFF}$) of the proposed pixel electrode circuit as a function of the threshold voltage shift (ΔV_{TH}) in comparison to the conventional current-driven pixel circuit. In Figure 2.10, the threshold voltage shift (x-axis) is the converted value from the stressing time based on the driving TFT CTS measurement at 85ºC, Figure 2.8 (b).

$$\Delta V_{TH} = V_{TH}(t_{ST}) - V_{TH}(t_{ST} = 0) \tag{2.3}$$

As expected, $\Delta I_{OLED\text{-}OFF}$ of the proposed circuit is very small (< 1.5%) at high data current level (=5.0 μA) regardless of TFT threshold voltage shift. However, as expected, at low current levels (=0.2 μA), the $I_{OLED\text{-}OFF}$ shows a significant deviation (> 40%) as the TFT threshold voltage shift increases over 10V. Nevertheless, if we compare the measured results with the previously published simulated results [6] for the TFT threshold voltage shift ranging from 0 to 4V, they showed a similar variation of the $I_{OLED\text{-}OFF}$ (<10%) for a low data current levels (=0.2 and 1.0μA) as one shown in Figure 2.10. In general, the propose pixel electrode circuit shows a smaller deviation of the $I_{OLED\text{-}OFF}$ ($\Delta I_{OLED\text{-}OFF}$) than the conventional current-driven pixel circuit for the same TFT threshold voltage shift value, which means that the proposed pixel electrode circuits have a slightly better electrical and thermal stability for low I_{OLED} levels in comparison with the conventional current-driven pixel circuit.

The stability issues of the proposed a-Si:H TFT pixel circuit can be further mitigated by adopting novel a-Si:H TFT structures for driving transistor in the pixel electrode circuit such as Corbino a-Si:H TFTs [17]. In Corbino a-Si:H TFT, since the ring-shaped electrode provides a uniform electric field distribution in the channel and eliminates any local electric-field crowding due to sharp corners present in normal TFT, such new TFT has a better electrical stability for a

larger W/L ratio required for driving TFT in comparison to normal TFTs. Therefore, we expect enhanced electrical stability of pixel electrode circuit with the Corbino driving TFT.

2.8 Conclusion

When a low I_{DATA} is used to express a low gray scale, the conventional current-driven pixel circuit has a problem of slow programming time. On the contrary, when a high I_{DATA} is used to express a high gray scale, the current-mirror pixel circuit has a problem of a high power consumption due to a fixed current-scaling ratio. In the proposed pixel circuit, by using cascaded-capacitors connected to the driving TFT, we could produce a non-linear scaling-function that has a high scaling ratio at low current levels and a low scaling ratio at high current levels. Therefore, using such pixel circuit, we expect a reduced power consumption at high current levels and minimized programming time at low current levels, which are ideal characteristics for a high-resolution a-Si:H TFT AM-OLEDs. We also showed experimentally that the proposed pixel electrode circuit has a better electrical and thermal stability than the conventional current-driven circuit under the same experimental current temperature stress conditions.

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CHAPTER 3

Novel Current-Scaling Current-Mirror a-Si:H TFT Pixel Electrode Circuit with Cascade Capacitor for AM-OLEDs

3.1 Introduction

Over last several years, it was shown by several authors [1-3] that the current driving pixel electrode circuits are among the most desirable solutions for active-matrix organic light-emitting displays (AM-OLEDs). However, as display size and resolution increase, a large timing delay can be observed at a low data current and its importance increases with the display size [4]. To address this issue, several solutions have been proposed based on polycrystalline silicon (poly-Si) thin-film transistor (TFT) technology such as current-mirror circuit [5, 6], series-connected TFT circuit [7], and current-mirror circuit with acceleration control line [8]. We also proposed hydrogenated amorphous silicon (a-Si:H) TFT based current-scaling pixel electrode circuit to address this problem [4]. In this report, we present an improved a-Si:H TFT current driving pixel electrode circuit with a enhanced current scaling function. A current mirror circuit with a cascaded storage capacitor is proposed here to achieve a high data-to-OLED current ratio without increasing TFT size in comparison with the conventional current mirror pixel circuit. At the same time, by removing one control signal line, this circuit has a much simpler pixel circuit layout and driving scheme than the previous cascade capacitor pixel electrode circuit.

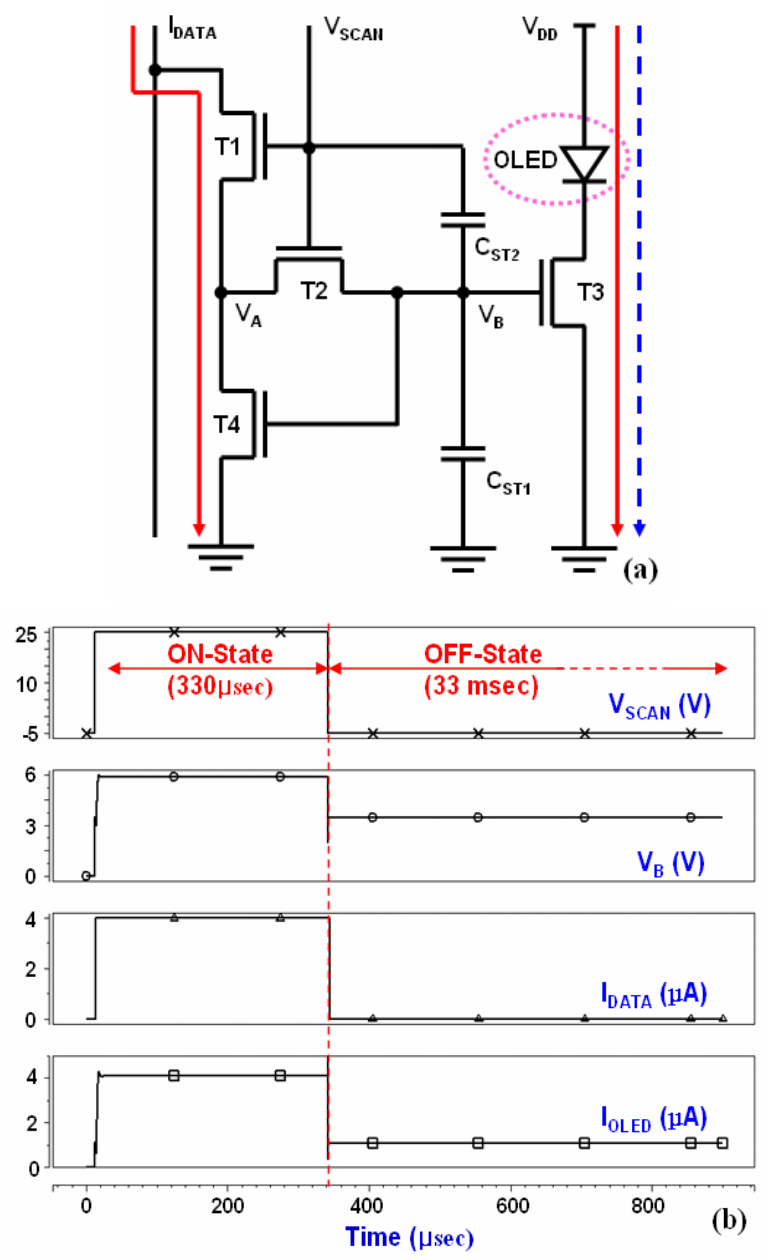


Figure 3.1 Schematic of (a) the cascaded-capacitor current mirror pixel electrode circuit and (b) operational waveforms simulated by HSPICE.

3.2 Operation of the Proposed Current-Scaling Pixel Electrode Circuit

The proposed current-driven pixel electrode circuit consists of two switching TFTs (T1 and T2), one mirror TFT (T4), one driving TFT (T3), and two storage capacitors (C_{ST1}, C_{ST2})

connected between a scan line and ground with a cascade structure, Figure 3.1 (a). The signals of V_{SCAN}, I_{DATA}, and V_{DD} are supplied by the external drivers while the anode of OLED is connected to V_{DD}. In comparison to the cascade capacitor current-scaling pixel electrode circuit reported previously [4], by employing the current mirror TFT structure, the control signal line can be removed to simplify the pixel layout and driving scheme as well as to enable OLED to light up during ON-state even when top anode light-emitting device structure is used.

Here we define $I_{OLED\text{-}ON}$ and $I_{OLED\text{-}OFF}$ as the current flowing through OLED during the ON- and OFF-state, respectively. $I_{OLED\text{-}OFF}$ is also defined as the scaled-down current from $I_{OLED\text{-}ON}$ by the ratio of C_{ST2}/C_{ST1}. The pixel circuit operation mechanism can be described as follow: During the ON-state, V_{SCAN} turns on the T1 and T2, and I_{DATA} (=$I_{OLED\text{-}ON}$) passes through T1 and T4 as the solid line shown in Fig. 3.1 (a), and sets up the voltage at T2 drain electrode (node A). At the same time, I_{DATA} flows through T2 instantly enough to charge up the storage capacitor C_{ST1} and set-up the voltage at T4 gate electrode (node B) to allow I_{DATA} passing through T4. Since I_{DATA} is current source, the gate voltage of T4 is automatically set high enough to allow the fixed I_{DATA} flowing through T1 and T4. In the pixel circuit operation, different from the conventional current-mirror circuit, the current-scaling is not controlled by the geometry ratio of the transistors but by the ratio of capacitors, T3 and T4 are designed to have the same geometries (W=150μm, and L=6μm). The T1 size is set to be large enough (W=150μm, and L=6μm) to reduce the voltage drop over T1 when V_{SCAN} is on, while the T2 size is set to be the small (W=10μm, and L=6μm) to reduce the voltage drop due to the parasitic capacitance when V_{SCAN} turns off. Since T3 and T4 are assumed identical in the ideal case and the gate bias (V_{B_ON}) is common to both TFTs, the same amount of current (I_{DATA}) is expected to flow through OLED to T3 by V_{DD}, which is expressed by (3.1),

$$I_{DATA} = \frac{1}{2}\mu_{FE} \cdot C_{OX} \cdot \frac{W_3}{L_3}(V_{GS} - V_{TH})^2 \tag{3.1}$$

where μ_{FE} and C_{OX} are field-effect mobility and gate oxide capacitance of T3, respectively. The V_{B_ON} will be stored in both C_{ST1} and C_{ST2}, and the voltage across C_{ST2} is V_{SCAN} - V_{B_ON}.

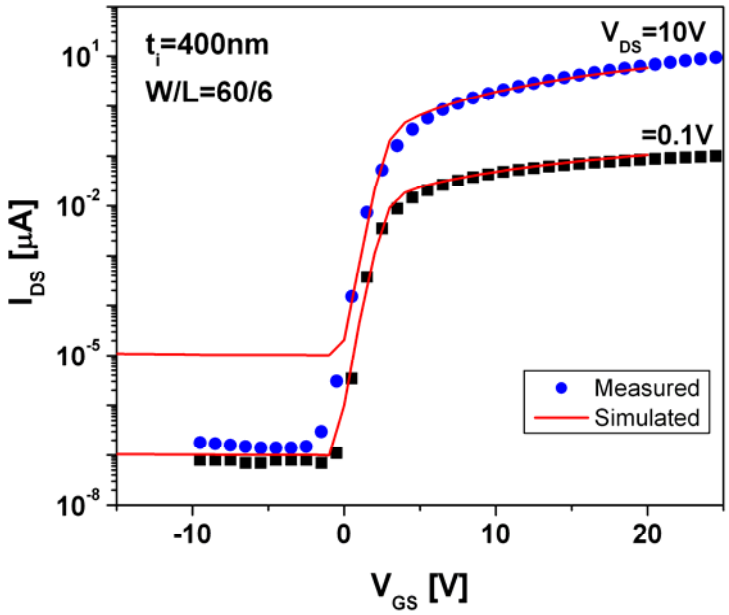
When the pixel changes from the ON- to the OFF-state, V_{SCAN} turns off T1 and T2. Because C_{ST2} is connected between the scan line and the node B to form a cascade structure with C_{ST1}, the change of V_{SCAN} will reduce V_{B_ON} to V_{B_OFF} due to the feed-through effect of the capacitors. V_{B_OFF} can be derived from the charge conservation theory [9] and is given by (3.2)

$$V_{B-OFF} = V_{B-ON} - \Delta V_{SCAN} \cdot \frac{C_{ST2} \parallel C_{OV-T2}}{C_{ST1} \parallel C_{OV-T3} \parallel C_{OV-T4} + C_{ST2} \parallel C_{OV-T2}}. \tag{3.2}$$

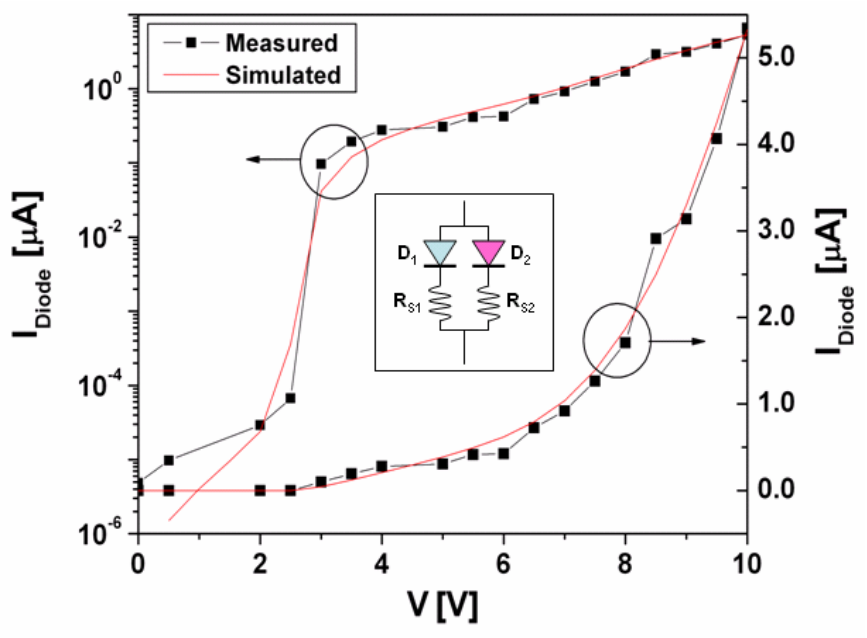
A reduced T3 gate voltage (V_{B_OFF}) will be hold in C_{ST1} and C_{ST2} and it will continuously turn on T3 during the OFF-state. Since gate bias of T3 (V_{B_ON}) is reduced to V_{B_OFF} by the ratio of cascaded capacitor, a scaled-down data current (I_{OLED_OFF}) will flow through OLED, shown as the dashed line in Fig 3.1 (a). Consequently, when a very large data current (I_{DATA}) can be used to charge the pixel electrode to shorten the pixel programming time, a smaller driving current (I_{OLED_OFF}) can be achieved for lower gray scales at the same time.

3.3 Device Parameter Extraction

Synopsis H-SPICE simulation tool with the Rensselaer Polytechnic Institute (RPI) Troy, NY, a-Si:H TFT and diode models [10, 11] were used to simulate the device characteristics and evaluate the proposed pixel electrode circuit. The a-Si:H TFT parameters developed within our group were used in this simulation [3]. To be used for the circuit simulation, we measured the transfer characteristics of the fabricated a-Si:H TFT for different drain bias (0.1 and 10V) by



(a)



(b)

Figure 3.2 Measured and simulated (a) transfer characteristics of a-Si:H TFT (b) current-voltage characteristics of white PLED. The equivalent circuit model of white PLED for simulation is shown in insert.

sweeping the gate bias from -10 to 25V. Then, we simulated the measured transfer curves of a-Si:H TFT for each condition by H-SPICE [12]. The resulted transfer characteristics of a-Si:H TFT are shown in Fig. 3.2 (a). To simulate the behavior of OLED, the conventional semiconductor diode model with the parameters extracted from organic polymer light-emitting diode (PLED) fabricated in our laboratory was used. The electrical property (current versus voltage) of PLED is shown in Fig 3.2 (b) and its opto-electrical properties are described in our previous research [13]. Since the opto-electrical behaviors of white PLED is different from the normal semiconductor diode, two semiconductor diode (D_1 and D_2) with series resistors (R_{S1} and R_{S2}) were used in parallel connection to fit the measured data of white PLED, and its equivalent circuit for the simulation is given in the insert. The a-Si:H TFTs and OLED parameters used for this pixel electrode circuit simulation are given in Table 3.1.

3.4 Simulated Electrical Properties of the Proposed Pixel Electrode Circuit

The proposed current-scaling pixel electrode circuit was evaluated by H-SPICE and an example of waveforms is shown in Fig 3.1 (b). In this specific case, in ON-state, the voltage at node B is set to appropriate level to allow I_{DATA} of 1μA to pass through T3 and T4 while V_{SCAN} and V_{DD} are hold at 30 and 18V, respectively. The time for ON- and OFF-state was set to 0.33 and 33ms, respectively. To investigate the current scaling ratio of the proposed pixel electrode circuit, we changed the I_{DATA} from 0.2 to 5μA and measured the corresponding I_{OLED_ON} and I_{OLED_OFF} flowing through the diode for different ratios of cascaded-capacitors. In ON-state, the I_{OLED_ON} is identical to the data current (I_{DATA}), Fig. 3.3 (a). When the pixel circuit operates in OFF-state, the diode current (I_{OLED_OFF}) is scaled-down by the ratio of cascade capacitor as discussed above and in our previous paper [4]. From Fig. 3.3 (b), it is obvious that the larger

Device parameters of TFT	
W/L (T1, T3, T4) [μm]	50/6
W/L (T2) [μm]	10/6
C_{ST1} [pF]	360
C_{ST2} [fF]	30 ~ 90
ALPHASAT	0.5
EMU [eV]	0.02
EL [eV]	0.1
EPSI	6.9
KVT [V/°C]	-0.01
LAMBDA [1/V]	0.005
M	1.9
MUBAND [m^2/Vs]	0.00015
RD [μΩ]	7000
RS [μΩ]	7000
TOX [m]	3×10^{-7}
VAA [V]	500
VO [V]	0.15
Device parameters of OLED	
n_1	18
n_2	2
R_{S1} [Ω]	7
R_{S2} [Ω]	150
I_{S1} [A]	10^{-8}
I_{S2} [A]	10^{-26}
Supplied signals	
V_{SCAN} [V]	-5 / 25
V_{DD} [V]	18
I_{DATA} [μA]	0.2 ~ 5

* Default values are used for other paramters which are not listed in the table [10]

Table 3.1 Parameters used in pixel circuit simulation.

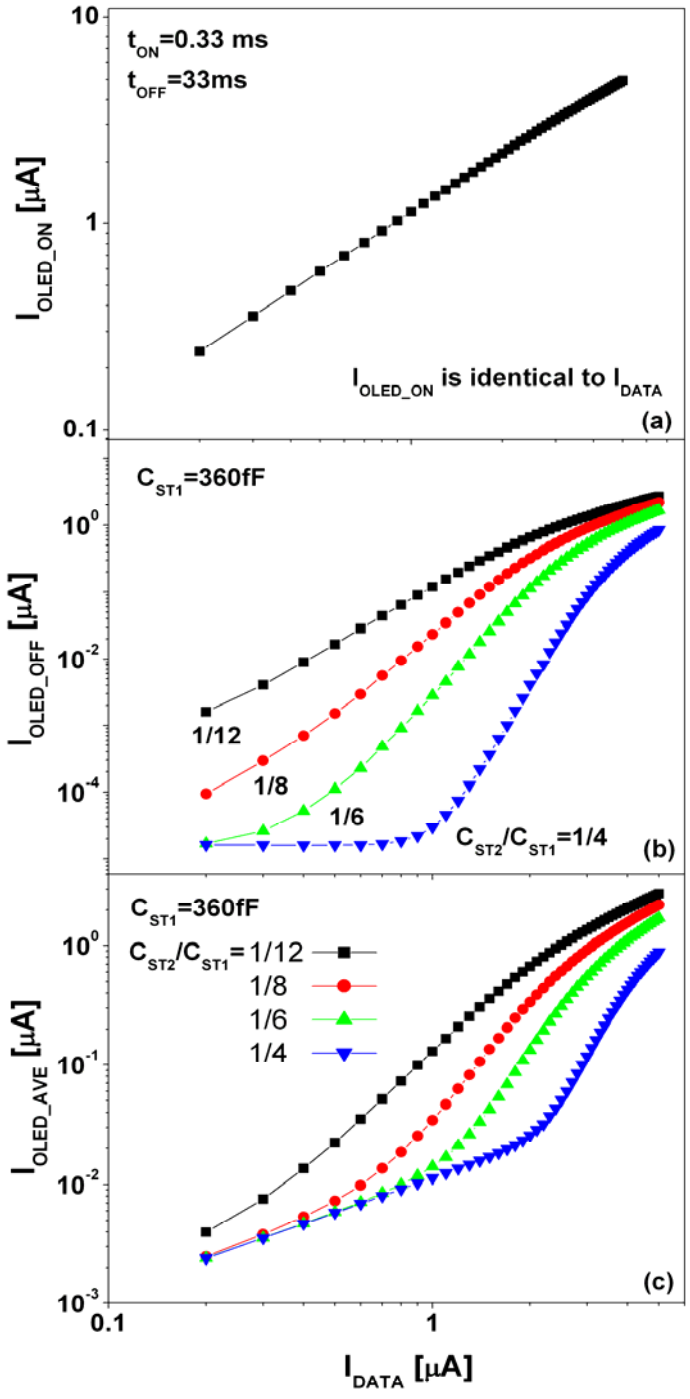


Figure 3.3 Variation of the simulated I_{OLED_ON}, I_{OLED_OFF}, and I_{AVE} as a function of I_{DATA} for various C_{ST2}/C_{ST1} ratios.

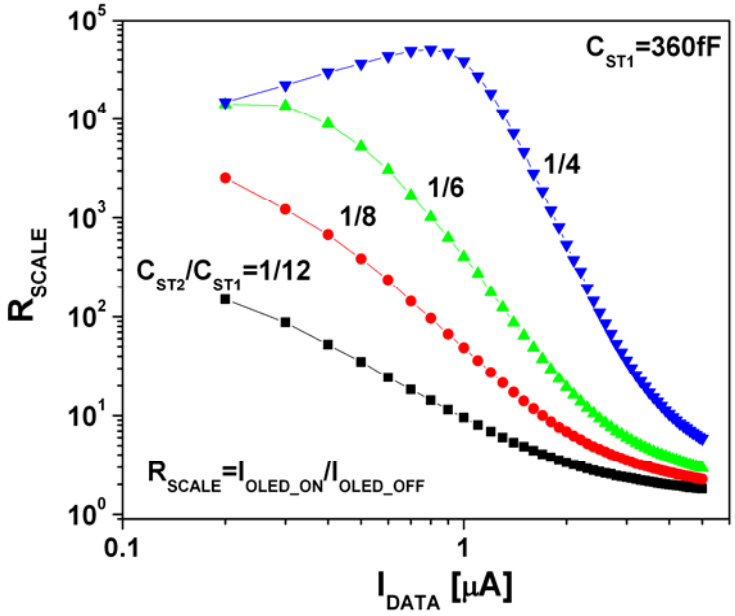
C_{ST2}/C_{ST1} results in significant decrease of the I_{OLED_OFF} at lower I_{DATA}. However, as shown in the figure, too large ratio of C_{ST2}/C_{ST1} (>1/6) can result in the saturation of I_{OLED_OFF}, which eventually can deteriorate the current scaling function.

Since the OLED current value is different during ON- and OFF-state, we define the average OLED current (I_{AVE}) during one frame time,

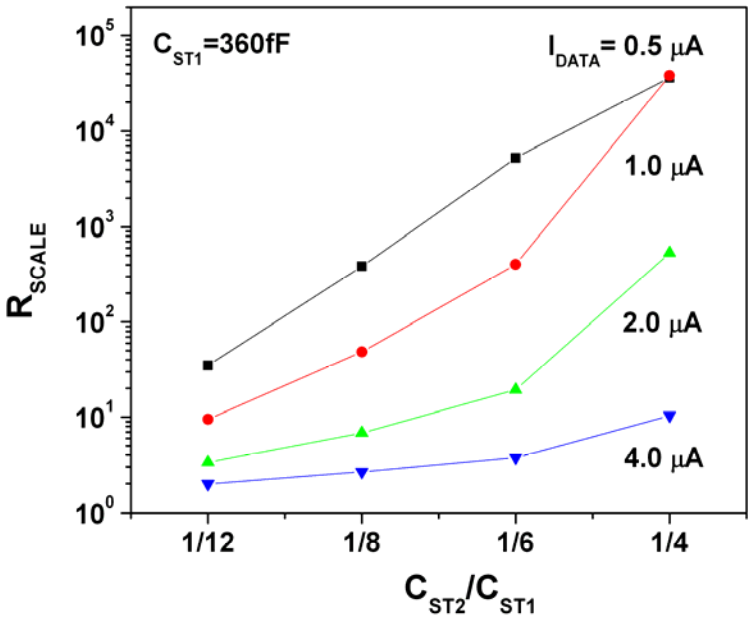
$$I_{AVE} = \frac{I_{OLED-ON} \cdot t_{ON} + I_{OLED-OFF} \cdot t_{OFF}}{t_{ON} + t_{OFF}} \tag{3.3}$$

where t_{ON} and t_{OFF} is the ON- and OFF-period during the frame time, respectively. The variation of I_{AVE} versus I_{DATA} in one frame period ($t_{ON} + t_{OFF}$) for different C_{ST2}/C_{ST1} ratios is shown in Fig. 3.3 (c). Since the OFF-state period is much longer than ON-state, though I_{OLED_OFF} is very small during OFF-state, it can reduce the I_{AVE} even if the I_{OLED_ON} (=I_{DATA}) is large. For example, the pixel electrode circuit can generate I_{AVE} ranging from 2.4 nA to 2.1 μA while I_{DATA} swept from 0.2 to 5 μA. Therefore, during one frame time, we can achieve very wide range of OLED current levels by supplying high data current levels.

The evolution of the scaling ratio (R_{SCALE}= I_{OLED_ON}/I_{OLED_OFF}) for different ratios of C_{ST2}/C_{ST1} as a function of I_{DATA} is shown in Fig. 3.4 (a). In this figure, we can see that for C_{ST2}/C_{ST1}=1/8, R_{SCALE} decreases from 16190 to 2.35 as I_{DATA} increases from 0.2 to 5μA, and an ideal non-linearity of R_{SCALE} can be achieved; e.g. a very high R_{SCALE} at low I_{DATA} levels (low gray scales) and a low R_{SCALE} at high I_{DATA} levels (high gray scales) can be produced. The variation of R_{SCALE} with the C_{ST2}/C_{ST1} is also shown in Fig. 3.4 (b). The simulated results show that for fixed I_{DATA}, R_{SCALE} increases as C_{ST2} increase from 30 to 90 fF, corresponding to an increase of C_{ST2}/C_{ST1} from 1/12 to 1/4. For constant C_{ST2}/C_{ST1}, R_{SCALE} increases as I_{DATA} decreases



(a)



(b)

Figure 3.4 Variation of the current scaling ratio as a function of (a) IDATA and (b) ratio of storage capacitances for the proposed pixel circuit.

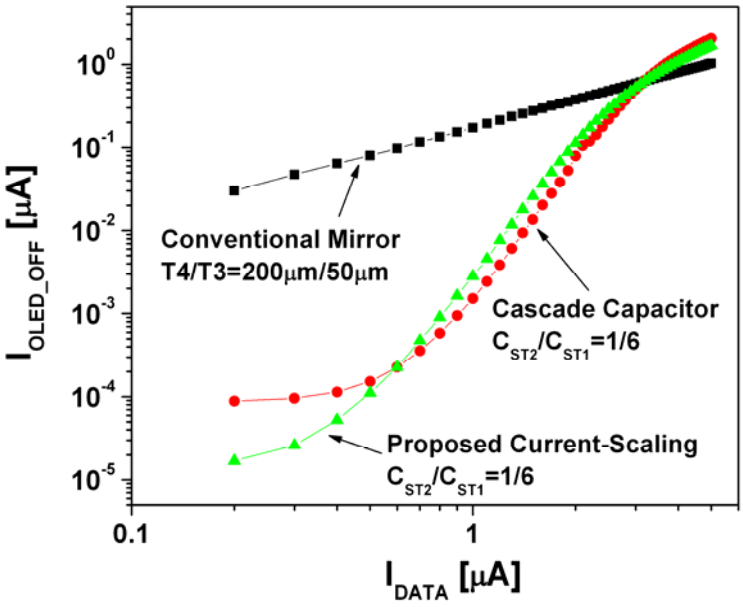


Figure 3.5 Comparison of I_{OLED_OFF} versus I_{DATA} among conventional current-mirror, cascade-capacitor, and proposed pixel electrode circuits.

as shown in Fig. 3.4 (a). Therefore, for a fixed ratio of C_{ST2}/C_{ST1} determined from the pixel electrode circuit design, we can expect certain range of the output OLED current.

3.5 Comparison with Other Pixel Electrode Circuits

To demonstrate the current-scaling function of the pixel electrode circuit in comparison with both the conventional current-mirror [5] and cascade capacitor current-scaling pixel electrode circuits [4], we simulated all three pixel electrode circuits using H-SPICE, and measured I_{OLED_OFF} as a function of I_{DATA} for each pixel electrode circuit as shown in Fig. 3.5. While the conventional current-mirror pixel circuit showed only a fixed current-scaling by the ratio of T4/T3 over given I_{DATA} range, the cascade capacitor current-scaling and the proposed current-scaling pixel electrode circuits showed non-linear current-scaling function for variable

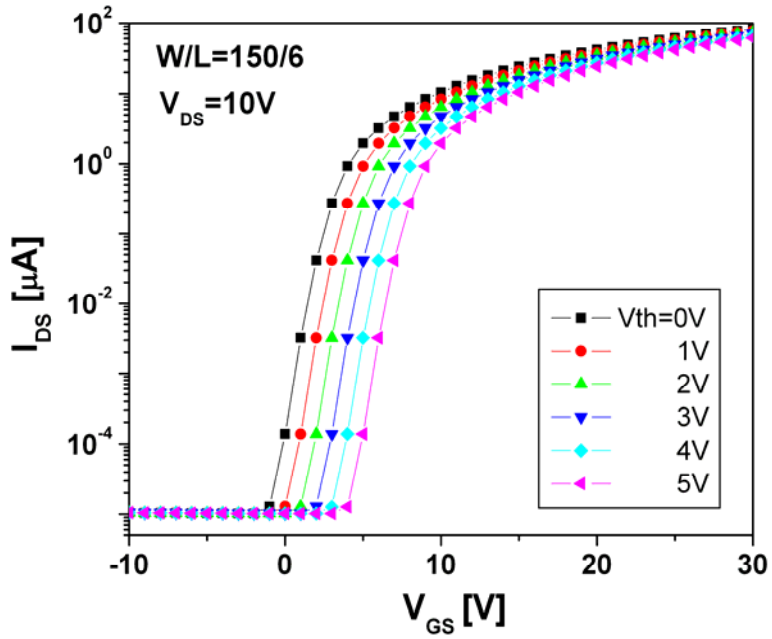
current-scaling ratio depending on I_{DATA}. When I_{DATA} varies from 0.2 to 5.0 μA, the proposed cascaded-capacitor pixel circuit with the ratio of C_{ST2}/C_{ST1}=1/8 can provide I_{OLED_OFF} ranging from 1.7×10^{-5} to 1.7 μA. Hence much wider range of I_{OLED_OFF} levels can be achieved by this circuit in comparison with the conventional current-mirror pixel circuit (3.0×10^{-2} to 1.0 μA). And slightly wider range is obtained in comparison with the cascade capacitor current-scaling pixel circuit (8.8×10^{-5} to 2.0 μA).

3.6 Influence of Threshold Voltage Variation

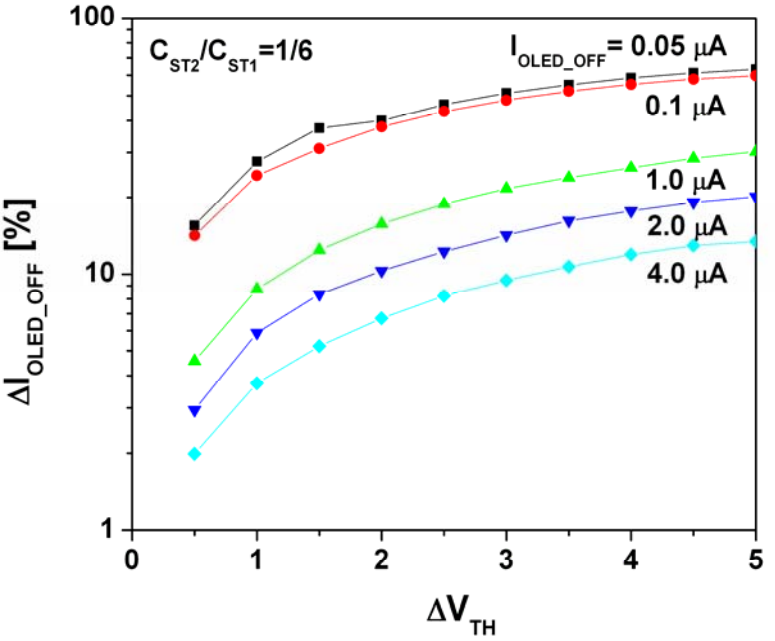
To investigate the influence of the threshold voltage (V_{TH}) variation of T3 and T4 on pixel circuit performance, various threshold voltage deviations (ΔV_{TH}= V_{TH} (after stress) – V_{TH} (initial)) have been used in pixel circuit simulation based on the experimental results reported previously [3]. In the H-SPICE a-Si:H TFT model, the threshold voltage is intentionally varied from 0 to 5V, and it is applied to our a-Si:H TFT model to be used in the pixel circuit simulation. Figure 3.6 (a) shows the change of transfer characteristics of a-Si:H TFT with the threshold voltage variation. In the proposed pixel circuit, since $I_{OLED\text{-}ON}$ is not affected by the threshold voltage variation, the variation of $I_{OLED\text{-}OFF}$ with ΔV_{TH} is used to estimate the influence of ΔV_{TH} on the performance of pixel circuit. For C_{ST2}/C_{ST1}=1/8, the variation of the $I_{OLED\text{-}OFF}$ with ΔV_{TH} can be defined by (3.4),

$$\Delta I_{OLED-OFF} = \frac{I_{OLED-OFF}(\Delta V_{TH}) - I_{OLED-OFF}(\Delta V_{TH}=0)}{I_{OLED-OFF}(\Delta V_{TH}=0)} \tag{3.4}$$

The variation of $I_{OLED\text{-}OFF}$ as a function of ΔV_{TH} is shown in Fig. 3.6 (b). As ΔV_{TH} increases, $\Delta I_{OLED\text{-}OFF}$ also increases from around 4 to 25% when $I_{OLED\text{-}OFF}$ is higher than 1.0μA. In ideal case, $I_{OLED\text{-}OFF}$ of T3 operation in deep saturation regime is independent of ΔV_{TH}. However, since the

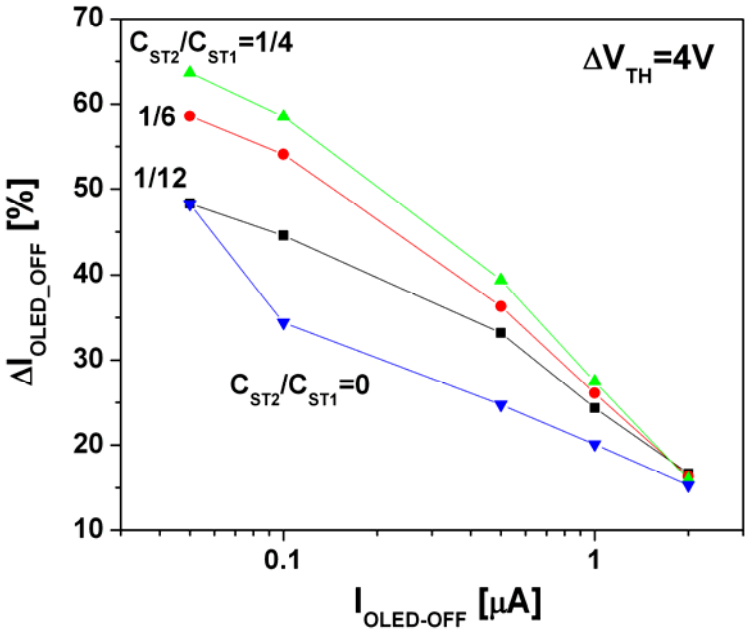


(a)



(b)

Figure 3.6 (a) Changes of transfer curve at V_{DS}=30V, and (b) variation of ΔI_{OLED_OFF} as a function of TFT threshold voltage shift.



(c)

Figure 3.6 (c) ΔI_{OLED_OFF} versus OLED current during display operation OFF-state for different C_{ST2}/C_{ST1} ratios when ΔV_{TH}=4V.

trans-conductance of T3 decreases with the increase of ΔV_{TH}, the drain voltage at T3 decreases as the ΔV_{TH} increases, resulting in the decrease of $I_{OLED-OFF}$ caused by the channel length modulation effect.

Substantial increases of $\Delta I_{OLED-OFF}$ when $I_{OLED-OFF}$ is lower than 100nA is due to the influence of charge injection of switching T2 on V_{B-ON}. Since a small V_{B-ON} will result from a low driving current I_{DATA} at low gray scales, the charge carrier released from T2, when T2 is turned off, can reduce the V_{B-ON}. The variation of V_{B-ON} becomes large when the data current is small since the charge injection effect becomes larger at lower drain voltages. In other words, when the driving transistor (T3) operates just above the V_{TH} for expressing low gray scales, even small V_{TH} shift of TFT can lead to a large change of $I_{OLED-OFF}$. As shown in Fig. 3.6 (c), when large

C_{ST2}/C_{ST1} is used, a significant variation of $\Delta I_{OLED\text{-}OFF}$ at low gray scales is observed in comparison to $C_{ST2}/C_{ST1}=0$. Therefore, smaller storage capacitor is needed to suppress the effect of T2 charge injection. From our data shown in Figs. 3.4(b) and 3.6(c), we can conclude that a large C_{ST2}/C_{ST1} can achieve a high R_{SCALE} but also result in a large $\Delta I_{OLED\text{-}OFF}$.

3.7 Influence of Device Spatial Mismatch and Temperature

Mismatch of TFT geometric size and its operating temperature can also affect the stability of $I_{OLED\text{-}OFF}$. The TFT size mismatch usually can result from device fabrication processes such as over-etching and alignment errors. The heat generated by non-emissive recombination of electron and hole in OLED can also increase the substrate temperature leading to change of the electrical performance of TFTs. From (3.1) and (3.2), the OLED current in OFF-state can be given as

$$I_{OLED-OFF} = \beta(V_{GS} - V_{TH} - V_{offset})^2 = \beta\left(\sqrt{\frac{I_{OLED-ON}}{\beta}} - V_{offset}\right)^2$$

$$= I_{OLED-ON} - 2\sqrt{\beta \cdot I_{OLED-ON}} \cdot V_{offset} + \beta \cdot V_{offset}^2 \qquad (3.5)$$

Where $\beta=\mu_{FE}C_{OX}(W_3/2L_3)$, $V_{offset}=\Delta V_{SCAN}(C_{ST2}||C_{OV\text{-}T2}/(C_{ST1}||C_{OV\text{-}T3}||C_{OV\text{-}T4}+C_{ST2}||C_{OV\text{-}T2}))$. It should be noted that $I_{OLED\text{-}OFF}$ is sensitive to the spatial mismatch due to the V_{offset} in the second and third terms of (3.5) while $I_{OLED\text{-}ON}$ is less affected by this factor. Especially, since T3 and T4 are expected to be identical in the proposed circuit, TFT size mismatch can have critical influence on the pixel circuit performance. If we assume that the T3 width varies from the designed value (W_3=150μm) while the T4 width is fixed, the variation of the $I_{OLED\text{-}OFF}$ with the

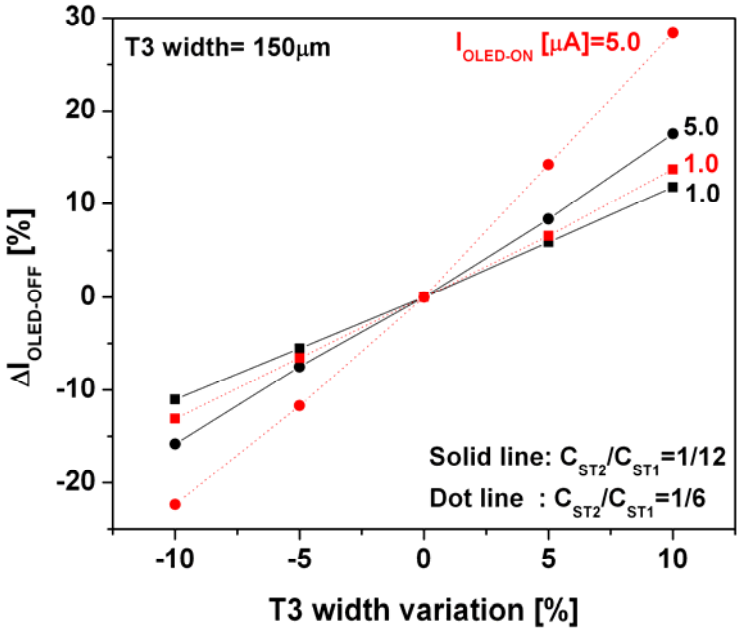


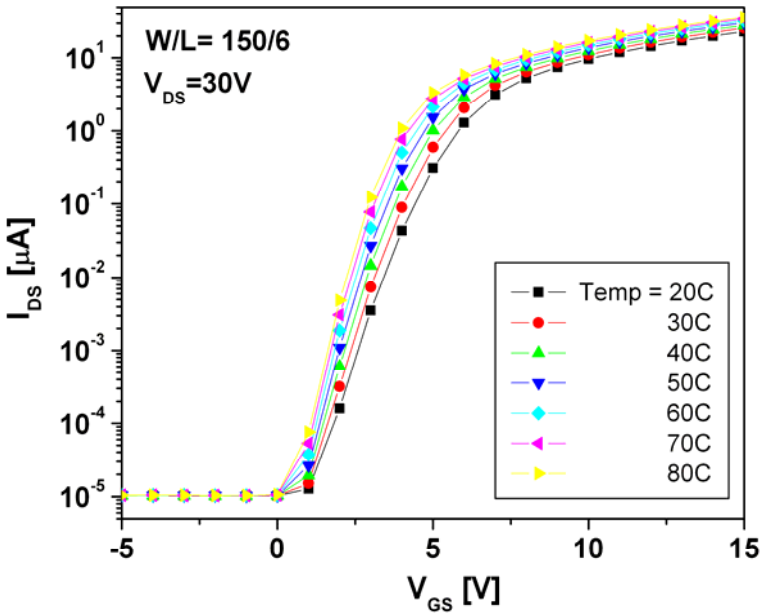
Figure 3.7 Variation of I_{OLED_OFF} as a function of T3 width deviation.

T3 width variation (ΔW_3) can be defined by (3.6), and shown in Figure 3.7.

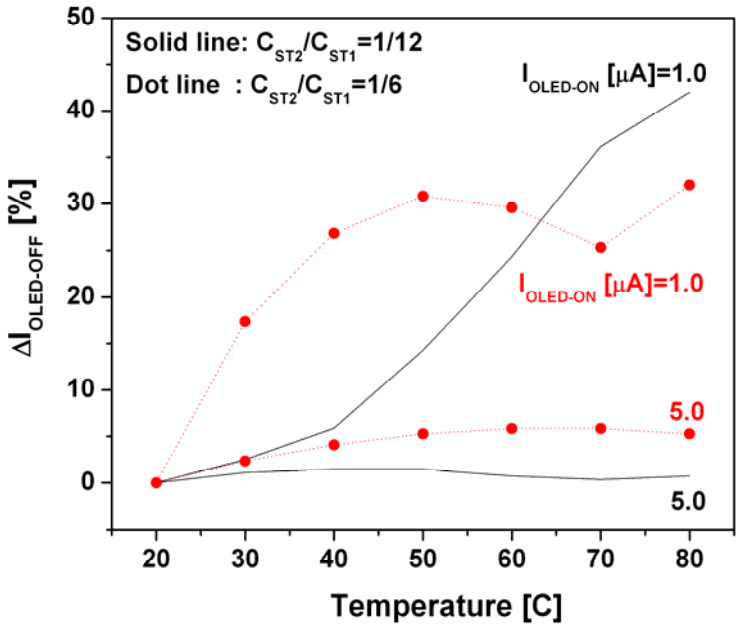
$$\Delta I_{OLED-OFF} = \frac{I_{OLED-OFF}(\Delta W_3) - I_{OLED-OFF}(\Delta W_3 = 0)}{I_{OLED-OFF}(\Delta W_3 = 0)} \tag{3.6}$$

The $I_{OLED-OFF}$ changes by ±25% as the T3 width vary from 135 to 165 μm, corresponding to ±10% deviation. Also, according to (3.5), a higher offset voltage value, associated with a large C_{ST2}/C_{ST1} ratio, will introduce greater deviation of $I_{OLED-OFF}$, Fig. 3.7. The $\Delta I_{OLED-OFF}$ for a high gray level is not as large as for a low gray level since a high driving current can reduce the sensitivity of $I_{OLED-OFF}$ to the geometric size mismatch.

Since it is well known that the field-effect mobility μ_{FE} and threshold voltage V_{TH} in a-Si:H TFT can be influenced by device temperature [14, 15], the increasing temperature will result in higher field-effect mobility and lower threshold voltage thus giving a rise in $\Delta I_{OLED-OFF}$. The



(a)



(b)

Figure 3.8 (a) Changes of transfer curve at V_{DS}=30V as a function of temperature. (b) Influence of operation temperature upon I_{OLED_OFF}.

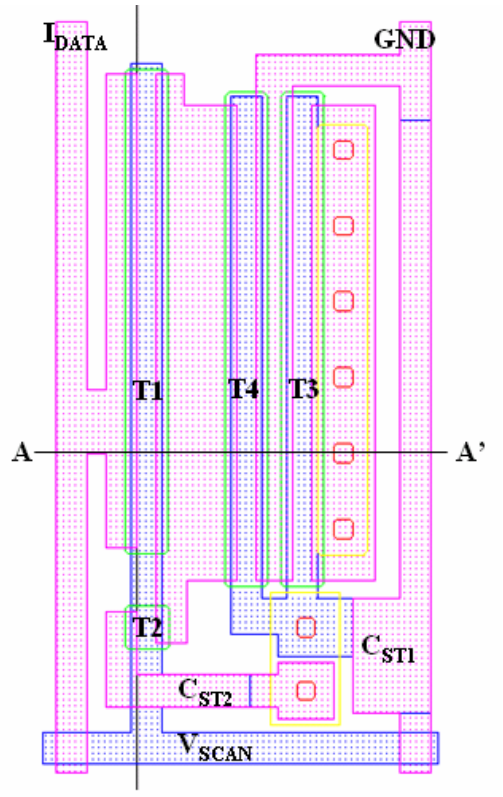
figure 3.8 (a) shows the simulated transfer curves of a-Si:H TFT at V_{DS}=30V when the temperature varies from 20 to 80 ºC. As shown in the figure, as the temperature increase, the mobility also increases from 0.63 to 0.67 cm^2/Vs while the threshold voltage decreases from 2.84 to 0.32V. The variation of the $I_{OLED\text{-}OFF}$ with the temperature (T) can be defined by (3.7), and shown in Figure 3.8 (b).

$$\Delta I_{OLED-OFF} = \frac{I_{OLED-OFF}(\Delta T) - I_{OLED-OFF}(T = 20^{\circ}C)}{I_{OLED-OFF}(T = 20^{\circ}C)} \tag{3.7}$$

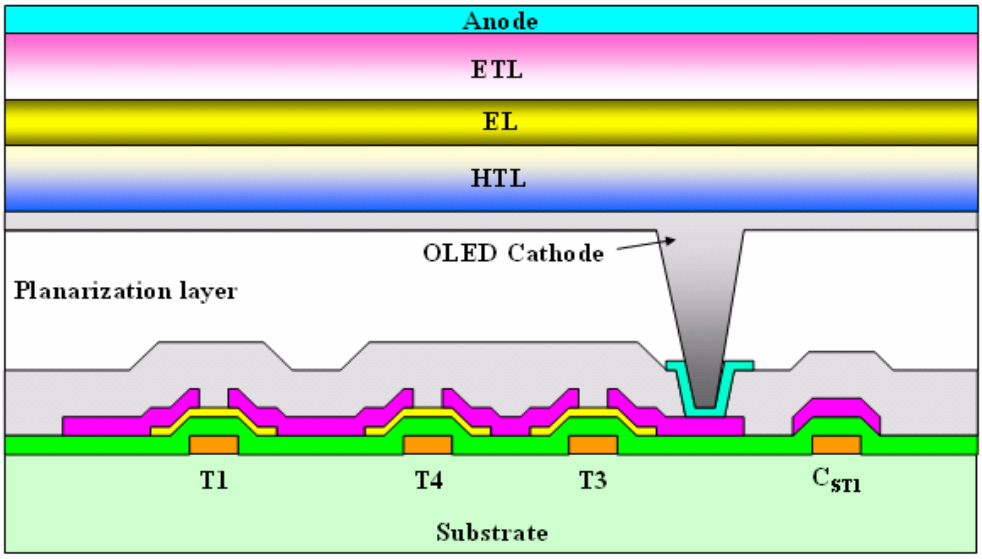
A higher V_{offset} due to a larger C_{ST2}/C_{ST1} ratio can cause an increase of $\Delta I_{OLED\text{-}OFF}$ not only at a low gray level ($I_{OLED\text{-}ON}$=1μA) but also at a high gray level ($I_{OLED\text{-}ON}$=5μA) region. It should be mentioned that as the driving current increases, $\Delta I_{OLED\text{-}OFF}$ becomes smaller as a result of lower sensitivity to temperature achieved by a larger $I_{OLED\text{-}ON}$. Therefore, we can conclude that though the temperature and the device spatial mismatch have impact on the OLED current, the propose pixel circuit can compensate those deviations within acceptable operating error range (<30%).

3.8 Possible AM-OLED Display by the Proposed Pixel Electrode Circuit

Figure 3.9 (a) and (b) presents schematic top views and cross-sections of proposed current-mirror with cascade capacitor pixel electrode circuit that can be used for a top-anode emitting AM-OLED display. The same sizes of TFTs and capacitors as used in the simulation were taken into consideration in the pixel electrode circuit layout. The pixel electrode circuit array layer can be fabricated by using the normal AM-LCD 5-photomask process steps. Then, the planarization layer is deposited before the OLED fabrication. The cathode layer of OLED is made of aluminum (Al) or aluminum alloy coated with the metal thin layer such as magnesium (Mg) or calcium (Ca), and is deposited on top of planarization layer. Then electron-transporting



(a)



(b)

Figure 3.9 (a) Schematic top views and (b) cross sections of proposed a-Si:H pixel electrode circuit.

layer (ETL), organic light-emissive layer (EL), and hole-transporting layer (HTL) are deposited successively over cathode electrode. Finally, transparent thin metal oxide (WO_3 or MoO_3)/ITO or Al bi-layer is deposited as an anode to form a top-emission anode OLED structure.

3.9 Conclusion

When a low I_{DATA} is used to express a low gray scale, the conventional current-driven pixel circuit has a problem of slow programming time. On the contrary, when a high I_{DATA} is used to express a high gray scale, the current-mirror circuit has a problem of high power consumption due to a fixed current-scaling ratio. On the contrary, the cascade-capacitor circuit provides the comparable non-linear current-scaling to the proposed circuit but needs an additional control signal line which could complicate the pixel layout and driving scheme. In the proposed circuit, by employing the cascaded-capacitors connected to the driving TFT, we could produce better non-linear scaling-function than the cascade capacitor circuit, which has a high scaling ratio at low current levels and a low scaling ratio at high current levels. Furthermore, the threshold voltage variation of TFTs can also be compensated by the proposed circuit. The effects of device geometric size mismatch and temperature increase on pixel electrode circuit performance were analyzed. It has been concluded that the resulted deviations of the OLED current are within acceptable range for the operation (< 30%). Therefore, using this pixel circuit, we expect to avoid the unnecessary pixel circuit power consumption at high current levels and minimize the programming time at low current levels with the reduced number of signal lines, which are supposed to be ideal characteristics for a high-resolution AM-OLED based on a-Si:H TFTs.

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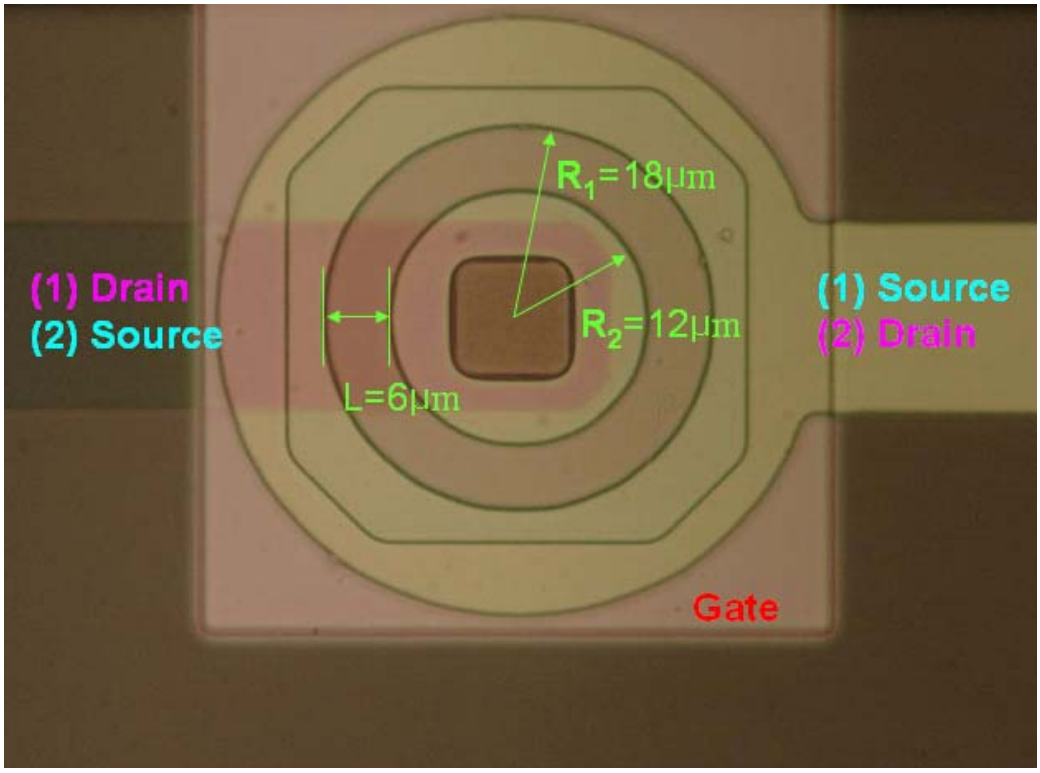
CHAPTER 4

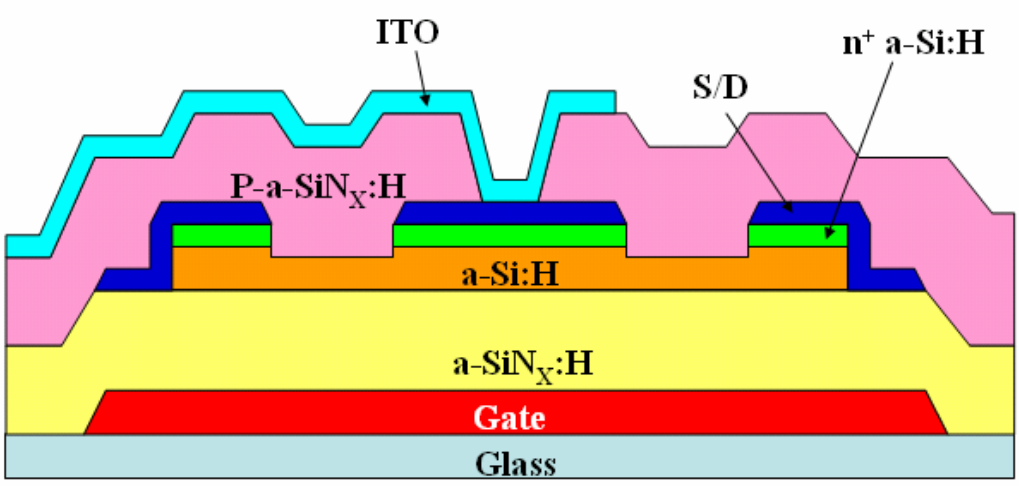
Asymmetric Electrical Properties of Corbino a-Si:H TFTs and Their Applications to Flat Panel Displays

4.1 Introduction

Since Corbino disk was first reported by M. Corbino in 1911 [1], this disk with inner and outer concentric ring contacts has been generally used in magneto-resistance measurement [2], and more recently has also been adopted for organic thin-film transistor (TFT) structures [3]. In hydrogenated amorphous silicon (a-Si:H) TFT, so called, annular shape electrode was first introduced in 1996 to provide a reduced gate-to-source capacitance and a smaller photo-current level that are very important factor to be considered for active-matrix liquid crystal displays (AM-LCDs) [4]. In 1999, to characterize the electrical properties of the silicon-on-oxide wafers by device geometrical factors, ring-shaped and circular electrodes were used in the pseudo-metal oxide semiconductor field effect transistor (Ψ-MOSFET) [5]. Recently, in silicon-based CMOS, annular MOSFET with the concentric circular boundaries was designed to enhance the device electrical reliability by modulating the electric field at the drain end of the channel [6]. However, so far the detailed discussion of the structural effect of Corbino electrode on a-Si:H TFT electrical properties has not been studied.



(a)



(b)

Figure 4.1 (a) The top view configuration and (b) the cross-section of Corbino a-Si:H TFT device.

In this work, we report on Corbino a-Si:H TFTs asymmetric electrical characteristics. More specifically, we studied effects of the drain bias polarity on Corbino TFTs electrical properties. We also investigated the a-Si:H TFT geometric effect on the extraction of key device electrical parameters such as sub-threshold slope, field-effect mobility, and threshold voltage, that are important for AM-LCDs and active-matrix organic light-emitting devices (AM-OLEDs). To our best knowledge, this report represents the first investigation of the asymmetric electrical characteristics of a-Si:H Corbino TFT to be used for AM-OLEDs.

4.2 Corbino a-Si:H TFT Fabrication

The Corbino a-Si:H TFT is consisting of circle-shape inner electrode (radius R_2= 12 μ m) and ring-shaped outer electrode (inner radius R_1=18 μ m), Figure 4.1. Bottom gate electrode is large enough to cover the entire area of device outer and inner electrodes. The Corbino a-Si:H TFT was fabricated using the normal AM-LCD 5-photomask process steps [7]. More specifically, on the Corning Eagle2000 glass substrate, bi-layer of aluminum-neodymium compound (AlNd, 2000Å) and molybdenum (Mo, 500Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet-etching (Mask #1). Following gate electrode definition, hydrogenated amorphous silicon nitride (a-SiN_X:H, 4000Å)/a-Si:H (1700Å)/phosphorous-doped a-Si:H (n^+ a-Si:H, 300Å) tri-layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 ºC to form gate insulator and active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (Mask #2), a chromium (Cr, 1200Å) layer was deposited by sputtering, and source/drain (S/D)

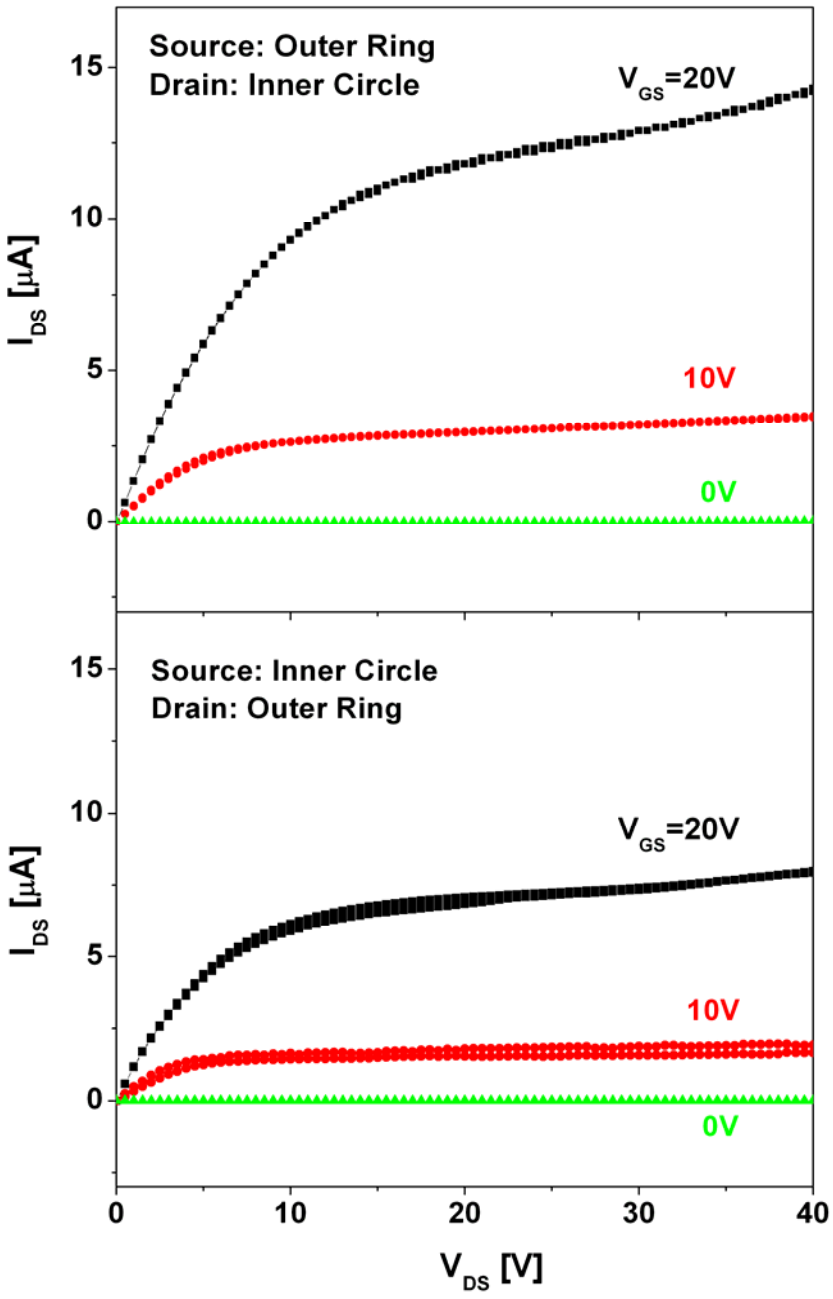


Figure 4.2 Output Characteristics of Corbino a-Si:H TFT

electrodes were patterned by wet-etching (Mask #3). Using S/D metal and photo resist as masks, the back-channel-etching by RIE was performed. Then, we deposited a-SiN_X:H (3000Å) as a passivation layer by PECVD at 300 ºC. To make a contact for the pixel electrode indium tin oxide (ITO) layer, via was formed through the passivation (PVX) layer by RIE (Mask #4). After contact via definition, ITO (500Å) was deposited by a sputtering method at room temperature, and then pixel electrodes were patterned by wet-etching (Mask #5). As a final step, the thermal annealing was performed for an hour at 235 ºC. The cross-section of a-Si:H Corbino TFT structure is shown in Fig. 4.1 (b).

4.3 Experimental Results

To characterize the electronic properties of Corbino a-Si:H TFT, we first measured the output characteristics, Figure 4.2, by applying the drain bias under following conditions: (1) ground was applied on the outer ring source electrode and drain voltage was applied on the inner circle drain electrode; (2) drain voltage was applied on the outer ring drain electrode and ground was applied on the inner circle source electrode. We swept the drain bias from 0 to 40V for various gate voltages (0, 10, and 20V). As shown in the Figure 4.2, at V_{DS}=20V and V_{GS}=20V, the output current for condition (1) (= 11.8 μ A) is 1.73 times higher than for condition (2) (= 6.82 μ A).

Next, we measured the transfer characteristics of Corbino a-Si:H TFT; we swept the gate bias from 15 to -5V, and swept again from -5 to 15V for various drain voltages (0.1, 1, 10, and V_{SAT}). As shown in Figure 4.3, at low drain voltage (V_{DS}=0.1V), the ON-currents are identical for both conditions. However, at high V_{DS} (> 1V), the ON-currents for condition (1) are higher than for

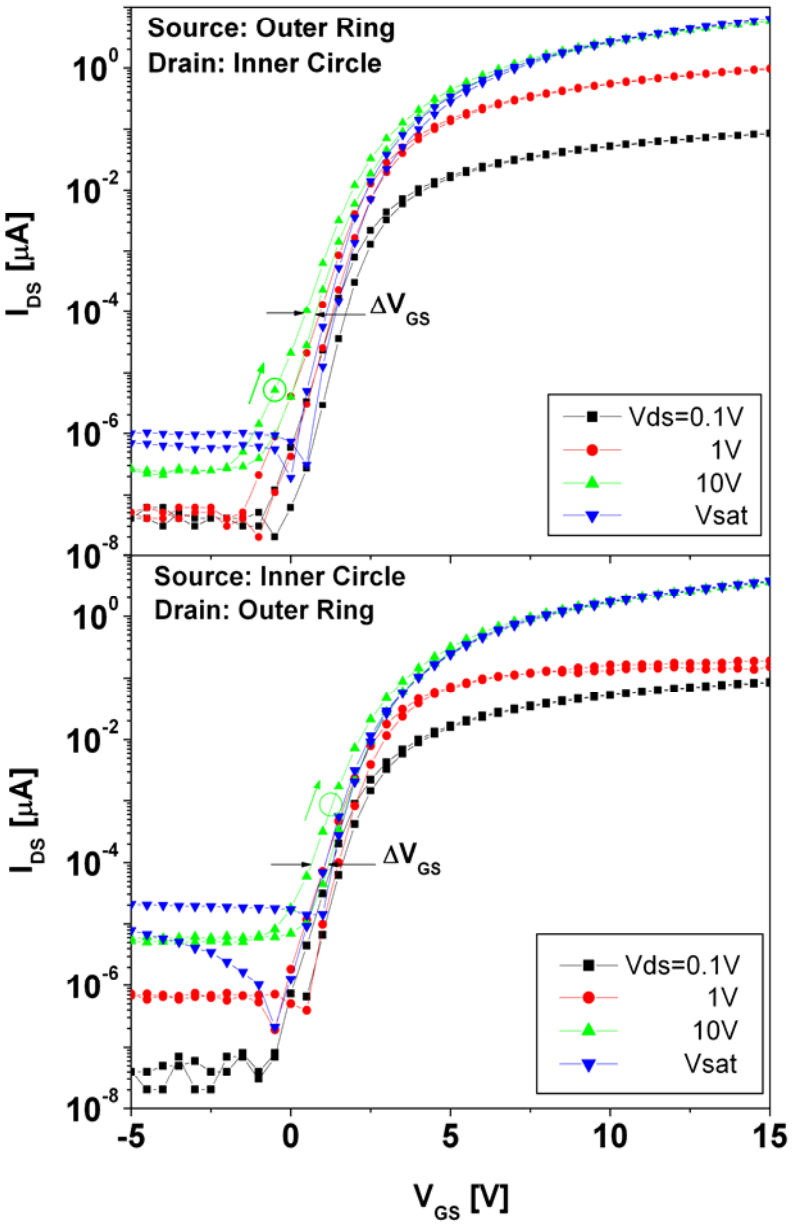


Figure 4.3 Transfer Characteristics of Corbino a-Si:H TFT

condition (2). Therefore, regardless of gate bias and direction of drain bias applied, the ON-currents would be the same for a low drain bias. However, when we apply a high drain bias, the ON-current levels can be increased significantly depending on the drain-bias direction. At the same time, as the drain bias is increased from 0.1 to 10V, the OFF-current for condition (2) increases from ~10^{-14} to ~10^{-12}, while the OFF-current for condition (1) remains low (from ~10^{-14} to ~10^{-13}). During gate bias sweeping, no significant hysteresis in current-voltage characteristics was observed for both conditions; at V_{DS}=10V and I_{DS}=0.1nA, both conditions showed gate voltage variation (ΔV_{GS}= $0.3V_{condition(1)}$, $0.55V_{condition(2)}$) acceptable for AM-LCDs.

4.4 Discussions of a-Si:H TFT Geometry Effect

The asymmetric behaviors of Corbino a-Si:H TFT described above can be explained as follow. As the gate bias increases, a channel is formed in the active a-Si:H layer at the interface with the gate insulator. At low V_{DS} (~1V), since the channel is not affected by the drain voltage, the whole channel layer can be considered as the carrier accumulation layer. Hence, effectively the shape and length of the channel would be the same for both drain bias polarities. Considering the geometrical effect of the channel on the drain current, we adopted the analytical model developed for Ψ-MOSFET [5] for a-Si:H Corbino TFT. The drain current is assumed to be constant at distance *r* from the inner circle and can be expressed as $I_D=2\pi r J_r$, where the current density J_r is a function of radial electric field, E_r, and potential V(*r*): $J_r=\sigma E_r=\sigma dV/dr$. The resulting differential equation for the potential is expressed as,

$$dV = \frac{I_D}{2\pi\sigma} \cdot \frac{1}{r} dr \tag{4.1}$$

where dark conductivity $\sigma=\mu C_{OX}[(V_{GS}-V_{TH})-V_r]$, and μ is the field-effect mobility, C_{OX} is the

oxide capacitance, V_{GS} is the gate bias, and V_{TH} is the threshold voltage of TFT. The integration of eq. (4.1) from R_1 to R_2, yields the potential drop between the source and drain electrodes as,

$$\int_0^{V_{DS}} [(V_{GS} - V_{TH}) - V_r] dV_r = \frac{I_D}{2\pi\mu C_{OX}} \int_{R_1}^{R_2} \frac{1}{r} dr \tag{4.2}$$

Hence, the drain current for both drain bias polarity can be expressed as

$$I_D = f_{g0} \mu C_{OX} [(V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 / 2], \quad \text{where} \quad f_{g0} = \frac{2\pi}{\ln(R_2 / R_1)} \tag{4.3}$$

Thus, instead of using the middle circumference of Corbino a-Si:H TFT as the device effective width, $W_{eff} = \pi(R_1 + R_2)$, the geometrical factor, f_{g0}, should be used in both drain bias conditions to extract the device field-effect mobility and threshold voltage at low V_{DS} (linear regime).

However, output and transfer characteristics at high V_{DS} (>10V) are quite different from those measured at a low V_{DS}. As discussed above, at high V_{DS}, ON-current is higher in condition (1) than condition (2). Assuming the device is ideal crystalline silicon MOSFET and field-effect mobility remains identical for both conditions, the current flowing through TFT can only be strongly dependant on the value of channel width and length. Therefore, at high V_{DS}, we need to define different geometrical factor f_g for each drain bias condition to accommodate the differences in device electrical properties. When TFT is operating in the saturation regime at high V_{DS}, we can assume the channel depletion region at the drain electrode would be increased by a certain value. This change is called as the channel length modulation factor (ΔL). The accumulation layer in the channel will decrease by the same amount. However, in the a-Si:H Corbino TFT, due to the unique geometry of Corbino disk, we can expect that ΔL would be different depending on the drain bias condition; the position of drain and source electrodes [8]. If

the drain bias fully depletes the channel by ΔL from the edge of drain electrode, the electric field at the depletion region edge of drain electrode can be expressed by the gauss' law; the charge contained in a volume (ρ) equals to the permittivity (ε) of a-Si:H times the electric field emanating from the volume.

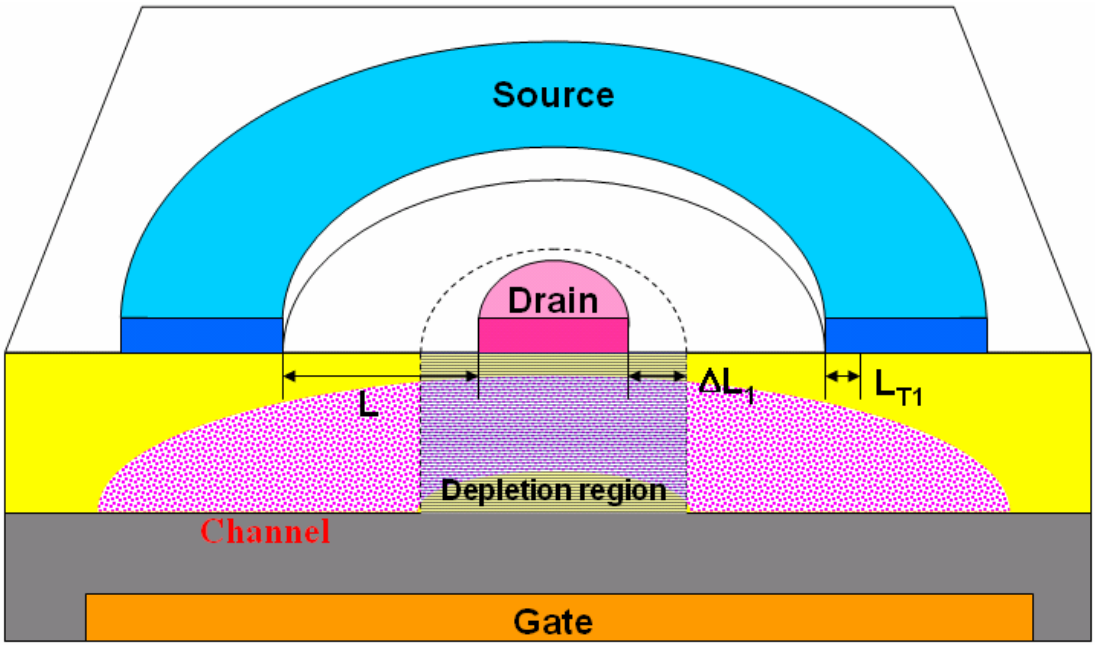
$$\oint \rho dV = \varepsilon_{a-Si} E \tag{4.4}$$

If the drain bias creates the same number of the depletion-region charge per unit area (Q_d) for both drain bias conditions, the electric field for each condition can be expressed by,

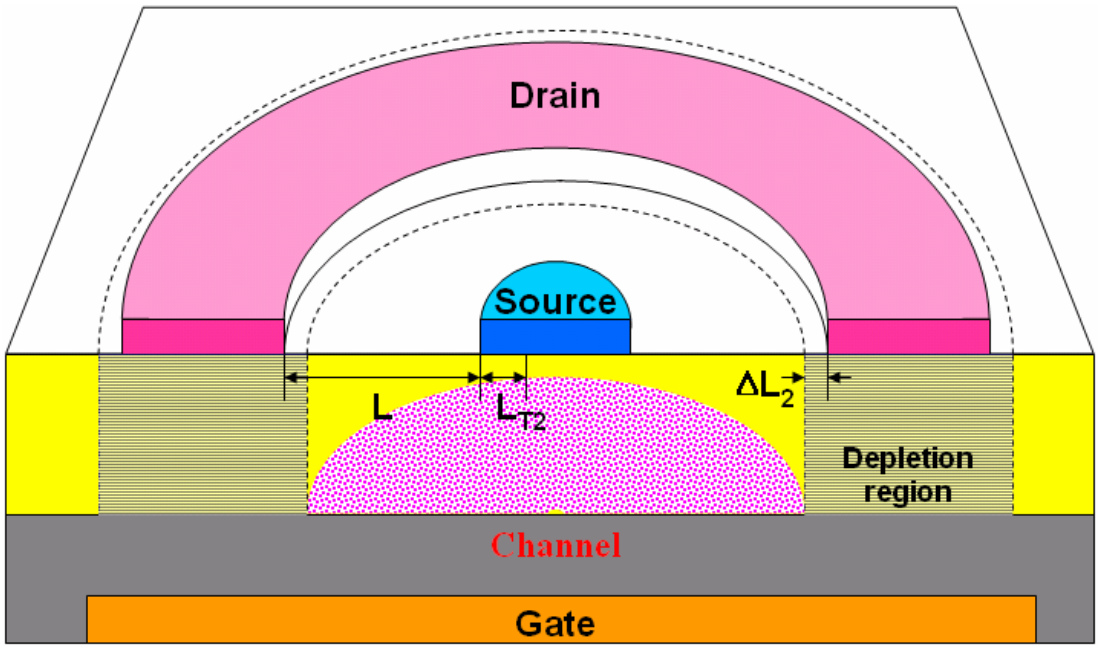
$$E_1 \cong \frac{(Q_d \times x_i \times 2\pi R_1 \times \Delta L_1)}{\varepsilon_{a-Si}} \tag{4.5a}$$

$$E_2 \cong \frac{(Q_d \times x_i \times 2\pi (R_2 - \Delta L_2) \times \Delta L_2)}{\varepsilon_{a-Si}} \tag{4.5b}$$

Therefore, if the electric field at drain electrode edge would be same for both conditions ($E_1=E_2$), since the size of drain electrode is larger for condition (2) than for condition (1) ($2\pi R_2 > 2\pi R_1$), the depletion region at drain side for condition (1) is expected to be larger than for condition (2) ($\Delta L_1 > \Delta L_2$) as shown in Fig 4.4 (a) and (b). From the above, it is expected that the channel length modulation factors will be different, $\Delta L_1=L/6$ for condition (1) and $\Delta L_2=L/10$ for condition (2), respectively. The channel accumulation layer formations for each drain bias condition are also shown in Fig. 4.4 (a) and (b). It should be also noted that due to the unique bottom-gate Corbino TFT structure where the gate electrode covers entire drain and source electrodes, the formed channel is extended even below the source electrode as shown in Figure 4.4. However, it is well known that in a-Si:H TFT, the drain current does not flow through the whole source electrode length but is rather limited to a specific length, so-called TFT characteristic length (L_T) [9] near the electrode edge. Therefore, the characteristic length for each



(a)



(b)

Figure 4.4 The cross-sections of Corbino a-Si:H TFT and the depletion region formation depending on the condition; (a) where the drain bias is applied on inner circular electrode and (b) where the drain bias is applied on outer donut electrode.

drain bias condition can be defined as L_{T1} and L_{T2}, respectively. To estimate L_{T1} and L_{T2}, we measured the channel resistance (r_{ch}) and source/drain contact resistance ($R_{S/D}$) by using four Corbino TFTs with different channel lengths for each drain bias condition. From the measurement data, TFT characteristic length ($=R_{S/D}/r_{ch}$) was calculated as 2 μm ($=L_{T2}$) and 1 μm ($=L_{T1}$), respectively. From the experimental results, we can speculate that L_{T2} is larger than L_{T1} because the size of the electrode acting as an electron source is smaller in bias condition (2) than in bias condition (1).

Based on these assumptions, to derive the equation for the drain current in the saturation regime, the same methodology was applied here as one used for derivation of eq. (4.1); the integration of eq. (4.2) from $R_1+\Delta L_1$ to R_2' ($=R_2+L_{T1}$) for drain bias condition (1) and from R_1' ($=R_1-L_{T2}$) to $R_2-\Delta L_2$ for drain bias condition (2) yields the potential drop between the source and drain electrodes for each case, respectively.

$$\int_0^{V_{DS}} [(V_{GS} - V_{TH}) - V_r] dV_r = \frac{I_D}{2\pi\mu C_{OX}} \int_{R_1+\Delta L_1}^{R_2'} \frac{1}{r} dr \tag{4.6a}$$

$$\int_0^{V_{DS}} [(V_{GS} - V_{TH}) - V_r] dV_r = \frac{I_D}{2\pi\mu C_{OX}} \int_{R_1'}^{R_2-\Delta L_2} \frac{1}{r} dr \tag{4.6b}$$

Hence, since $V_{DS}=(V_{GS}-V_{TH})$ in the saturation regime, the drain current for each condition can be expressed with corresponding geometrical factor f_{g1} and f_{g2}.

$$I_D^{Condition(1)} = f_{g1}\mu C_{OX}(V_{GS} - V_{TH})^2, \text{ where } f_{g1} = \frac{\pi}{\ln[6(R_2')/(R_1 + 5(R_2'))]} \tag{4.7a}$$

$$I_D^{Condition(2)} = f_{g2}\mu C_{OX}(V_{GS} - V_{TH})^2, \text{ where } f_{g2} = \frac{\pi}{\ln((9R_2 + R_1')/10R_1')} \tag{4.7b}$$

As shown in eq. (4.7), in the saturation regime, values of geometrical factor can have direct impact on drain current values. When R_1 and R_2 in eq. (4.7) are replaced with the actual

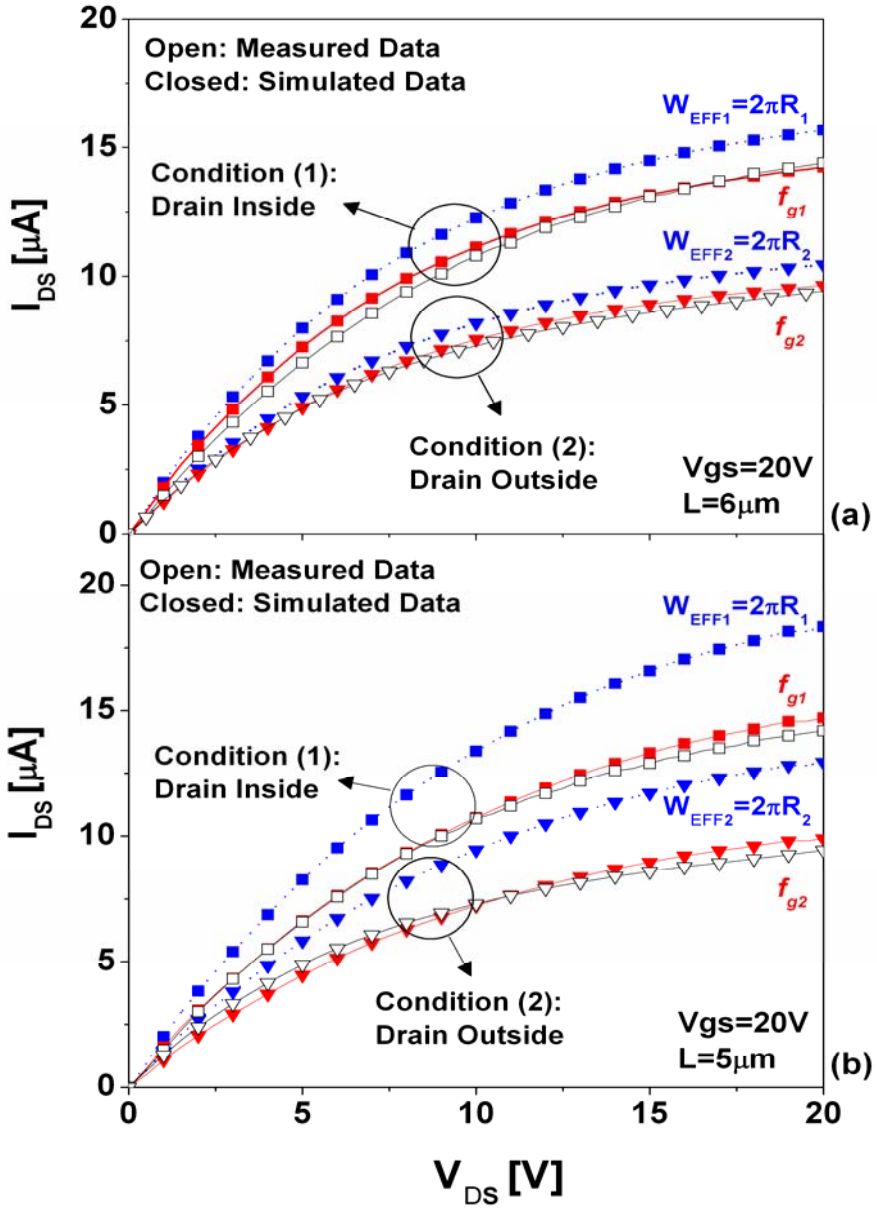


Figure 4.5 Measured (open symbol) and simulated (closed symbol) output characteristics of Corbino a-Si:H TFT; (a) where R2=18 μm and R1=12 μm, and (b) R2=17 μm and R1=12 μm.

measured values (R_1=18 μm and R_2=12 μm), the geometrical factor in condition (1) turns out to be larger than in condition (2) by about 1.6 times. Therefore, the ON-current in condition (1) is also expected to be larger than in condition (2) by the difference in the geometrical factors. To validate this assumption, we calculate the output characteristic of Corbino TFT and compare with the measured data, Figure 4.5. For the asymmetric output current calculation, a conventional rectangular TFT with the same length (width (W) =60 μm and length (L) = 6 μm) was used. Output drain current of conventional standard TFT was measured at V_{GS}=20V, and then normalized with its width over length ratio (W/2L) to be used as a reference value for calculation. Corbino and standard TFT have been fabricated at the same substrate using the same process. We expect that their normalized electrical properties are equivalent and only geometries are different. Therefore, using normalized output drain current of standard TFT, we calculate the output drain current of Corbino TFT for each condition, by multiplying the normalized TFT characteristic by geometric factors shown in eq. (4.7). As shown in the Figure 4.5, we could exactly match the measured output drain current of Corbino TFT for each drain bias condition. It should be noted that when the intuitive channel width is used as the circumference of source electrode ($W_{EFF1}=2\pi R_1$ for condition (1) and $W_{EFF2}=2\pi R_2$ for condition (2)) instead of the defined geometrical factors given by eq. (4.7), the calculated drain current values are much larger than experimental values, Fig. 4.5 (a)! For further validation, we also measured another set of Corbino and standard TFTs with different dimensions; R_1=17μm and R_2=12μm for the Corbino TFT and W=60μm and L=5μm for the standard TFT. Again, the standard TFT is normalized by W/2L to be used as a reference for the calculated current. As shown in Fig. 4.5 (b), though there is a little deviation observed for drain bias condition (1), the measured output drain current of Corbino TFT could be exactly matched by multiplying the normalized drain current of standard TFT for each condition by the defined geometrical factor as defined in eq. (4.7). However, when the

intuitive channel width ($W_{EFF1}=2\pi R_1$ for condition (1) and $W_{EFF2}=2\pi R_2$ for condition (2)) is used instead of the geometrical factor given by eq. (4.7), the calculated output drain current of Corbino TFT shows huge difference from the measured output drain current of Corbino TFT.

The OFF-current in a-Si:H TFT is originated from carriers generated in the depletion region on drain side (at high V_{DS}) when negative gate bias is applied. Under $V_{GS}<0$, the a-Si:H is fully depleted and accumulation of hole will take place near the a-Si:H / a-SiN_X:H interface creating a hole current. The current level is limited by the n^+-a-Si:H source/drain contact regions (these are hole blocking contacts). If we assume that two quasi n^+-p junctions are formed between the drain and source n^+-regions and hole (p) conduction channel, the drain n^+-p junction is under reverse bias ($V_{DS}>0$), which is similar to a n^+-p junction in the OFF-state. Indeed, in a regular n^+-p junction, the OFF-current is carried by minority carrier generated in depletion region. The OFF-current (J_g) in this region can be limited by the generation rate of carriers and the depletion width x_i as in following equation.

$$J_g = \frac{qn_i x_i}{2\tau_o} \tag{4.8}$$

where q is electron charge, n_i is the maximum generation rate, and τ_0 is the life time of excess carrier in the depletion region. If we assume that the width of the depletion region and the generation rate is identical for both drain bias conditions at high V_{DS}, the OFF-current can depend only on the volume of the depletion region (= the area of drain electrode × the depletion width, x_i) for each bias condition. Therefore, since the area of drain electrode is larger in drain bias condition (2) and in drain bias condition (1), the OFF-current of condition (2) can be much higher than for condition (1).

4.5 Device Parameters Extraction

From TFT data shown in Figures 4.2, 4.3 and 4.6, we can extract sub-threshold slope (S), threshold voltage, and field-effect mobility values. We chose the center position (at $I_{DS}=10^{-10}$A) in the transfer curve of log (I_D) vs. V_{GS}, and use the linear fitting by taking two log (I_D) values around the center point to extract S-value.

Field-effect mobility (μ) and threshold voltage can be calculated as follow: from the transfer curve of I_D vs. V_{GS} in Figure 4.6, we chose the value of I_D at V_{GS}=15V. By taking 90 and 10% of this I_D value, we define the fitting range for fitted curves to I_D vs. V_{GS} experimental characteristics. From the slope and x-axis intercept of the calculated curve, the field-effect mobility and threshold voltage have been calculated using eq. (4.3) and (4.7) with different geometrical factors. Extracted device parameters are summarized in Table 4.1 (a) for linear (low V_{DS}) and saturation (high V_{DS}) region, respectively. For the comparison, we also calculated field-effect mobility (μ) and threshold voltage by using maximum slope method [10] which is usually used for crystalline silicon devices. Figure 4.6 shows variations of transconductance ($=dI_{DS}/dV_{GS}$) for each drain bias condition as a function of gate bias for linear (low V_{DS}) and saturation (high V_{DS}) region, respectively. The field-effect mobility is calculated from transconductance maximum (g_m) value using following equations:

$$\mu_{Linear} = \frac{g_{m-Linear}}{f_g C_{OX} V_{DS}} \tag{9a}$$

$$\mu_{Saturation} = \frac{g^2_{m-Saturation}}{f_{g1,2} C_{OX}} \tag{9b}$$

where $g_{m\text{-}Linear}$ is the maximum transconductance at V_{DS}=0.1 V and $g_{m\text{-}Saturation}$ is the maximum

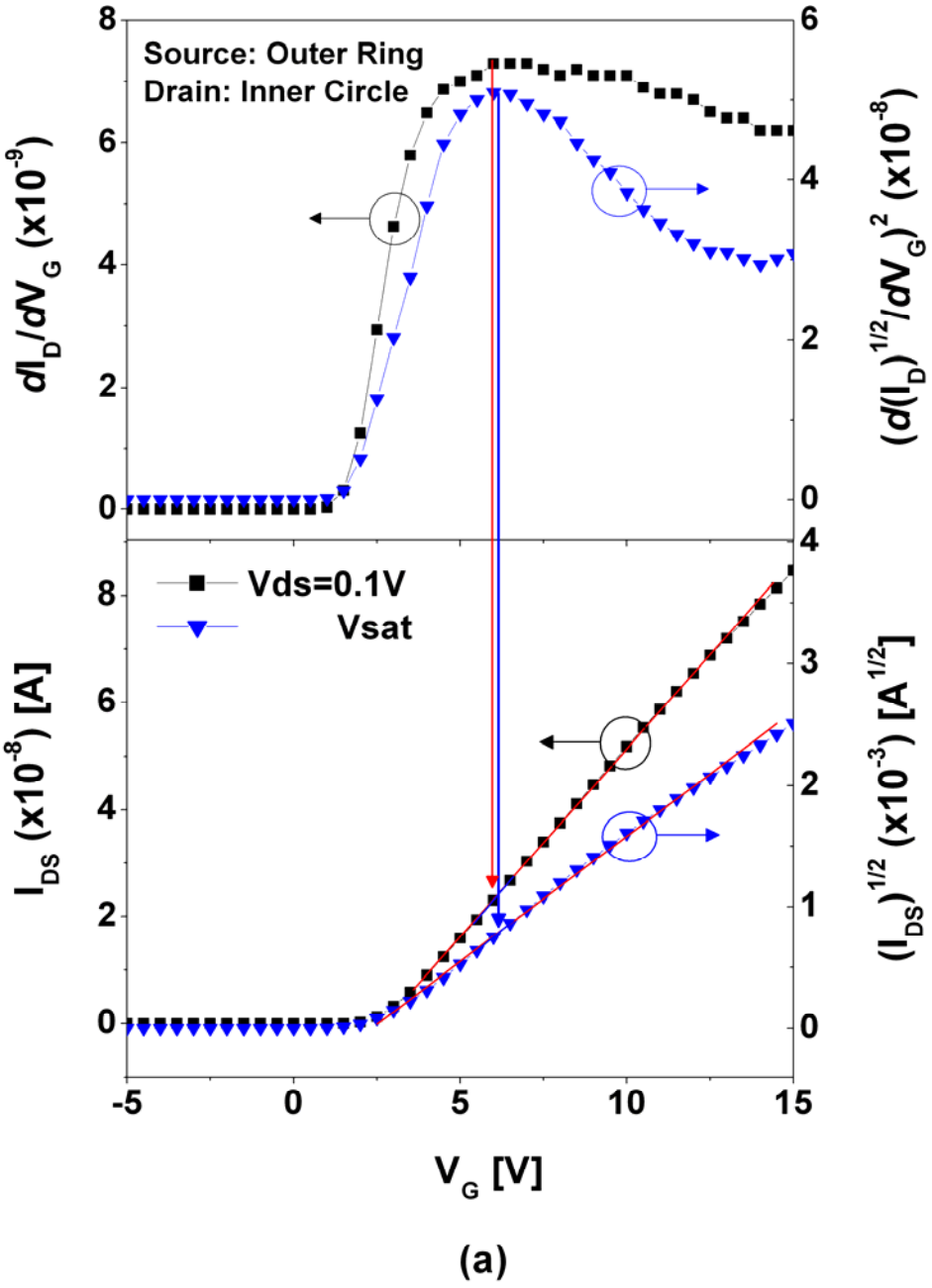


Figure 4.6 Transconductance and corresponding transfer characteristics of Corbino a-Si:H TFT. Curves used for extraction of the threshold voltage and mobility are also shown; (a) where the drain bias is applied on inner circular electrode.

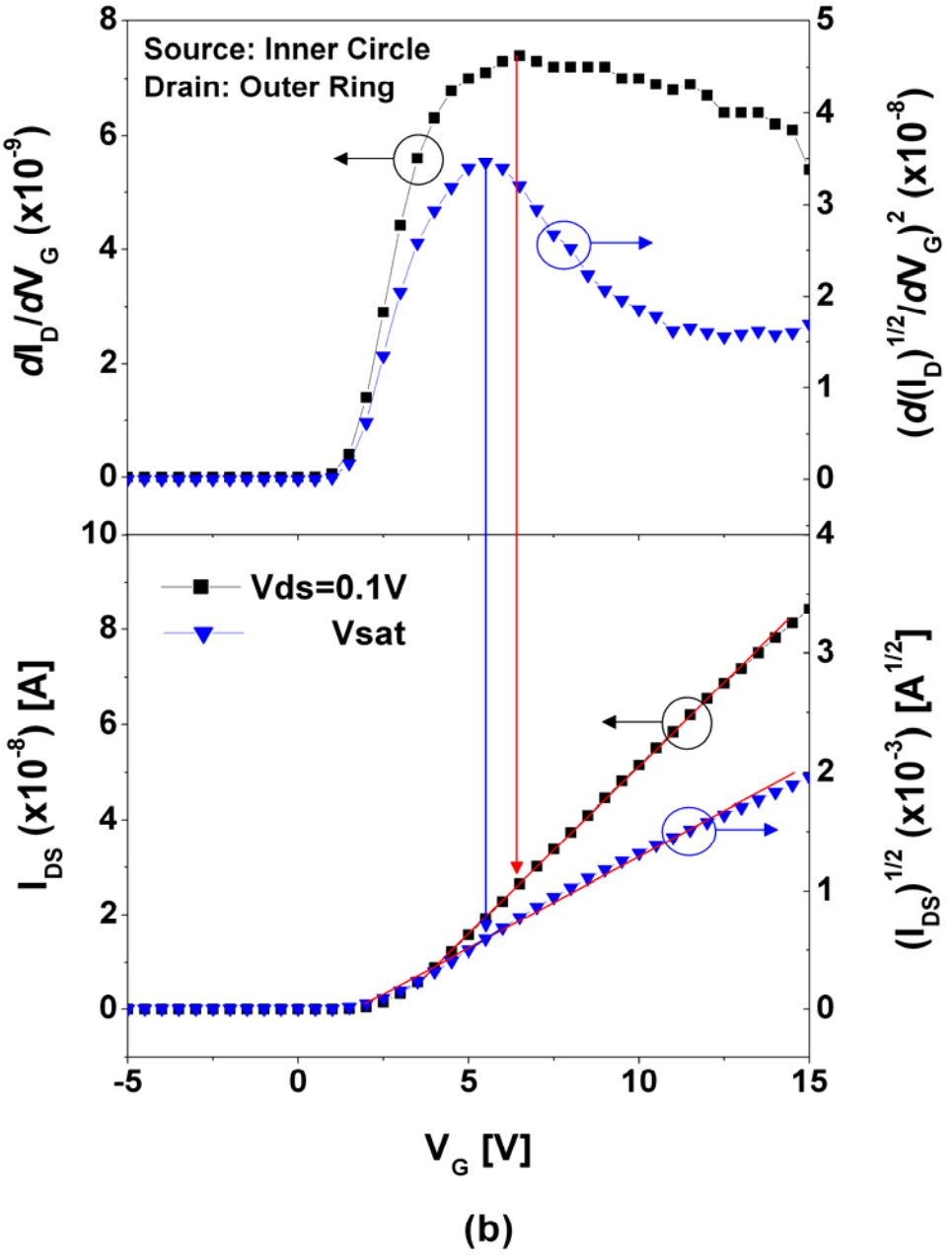


Figure 4.6 Transconductance and corresponding transfer characteristics of Corbino a-Si:H TFT. Curves used for extraction of the threshold voltage and mobility are also shown; (b) where the drain bias is applied on outer ring electrode.

(a)	V_{DS}=0.1V		V_{DS}=V_{sat}	
Condition	(1)	(2)	(1)	(2)
S [mV/Dec]	488	532	416.6	538
V_{th} [V]	2.6	2.7	2.6	2.2
μ [cm^2/V·s]	0.31[a)]	0.32[a)]	0.37[b)]	0.36[c)]

(b)	V_{DS}=0.1V		V_{DS}=V_{sat}	
Condition	(1)	(2)	(1)	(2)
V_{th} [V]	2.6	2.7	2.7	2.3
μ [cm^2/V·s]	0.32[a)]	0.32[a)]	0.39[b)]	0.42[c)]

Geometrical factor a) f_{g0}, b) f_{g1}, and c) f_{g2} is used to extract the parameter.

Table 4.1 Extracted parameters of Corbino a-Si:H TFT by using (a) our method and (b) maximum slope method; condition (1) where the drain bias is applied on inner circular electrode and condition (2) where the drain bias is applied on outer donut electrode

trans-conductance at V_{DS}=Vsat. From the value of V_{GS} corresponding to the g_m as a reference, two closest different gate bias values are chosen so that the straight fitting line is drawn based on these three points in the transfer characteristic curves. The threshold voltage can be estimated from x-axis intercept of this extrapolated line for each drain bias condition, Figure 4.6.

Resulting extracted parameters are summarized in Table 4.1 (b), and it is clear from this

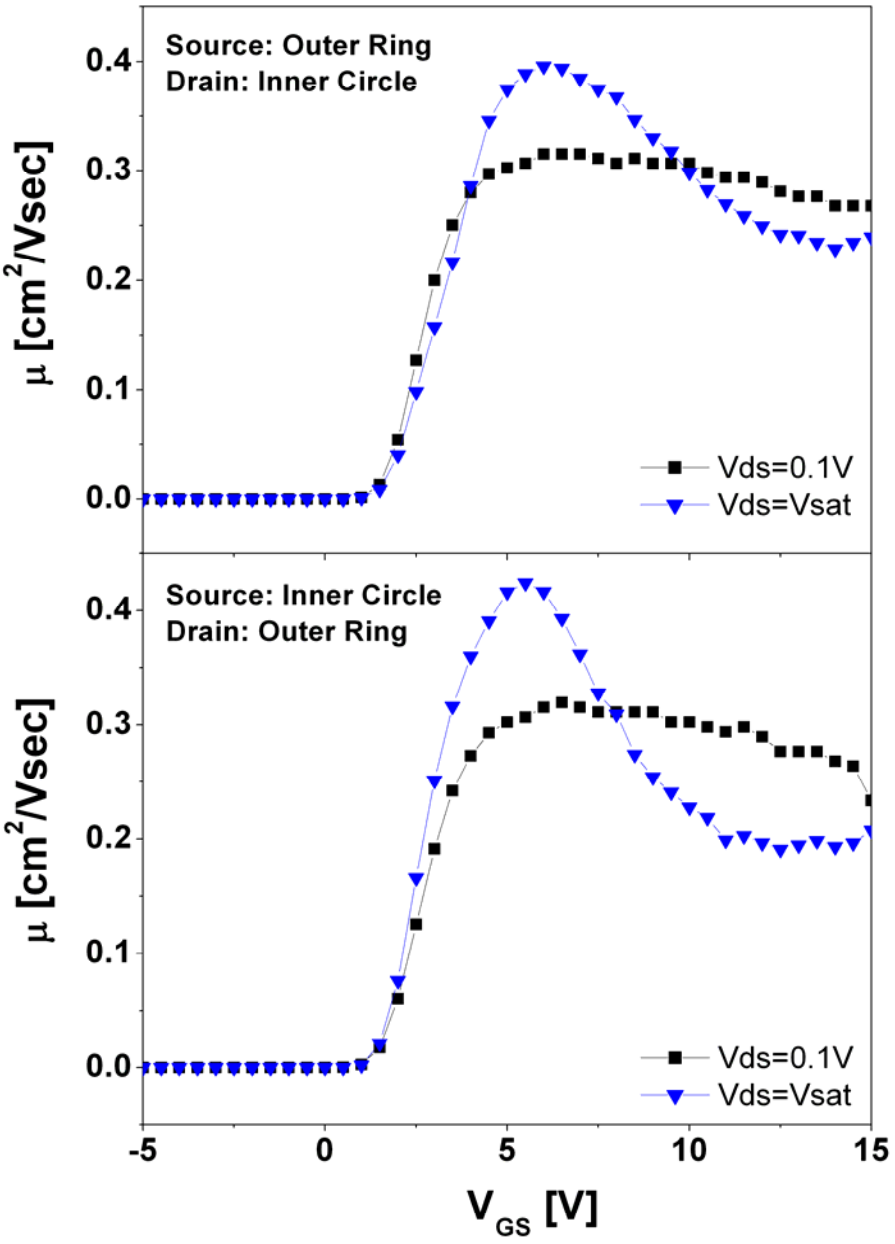


Figure 4.7 Field-effect mobility *of* Corbino a-Si:H TFT as a function of gate bias

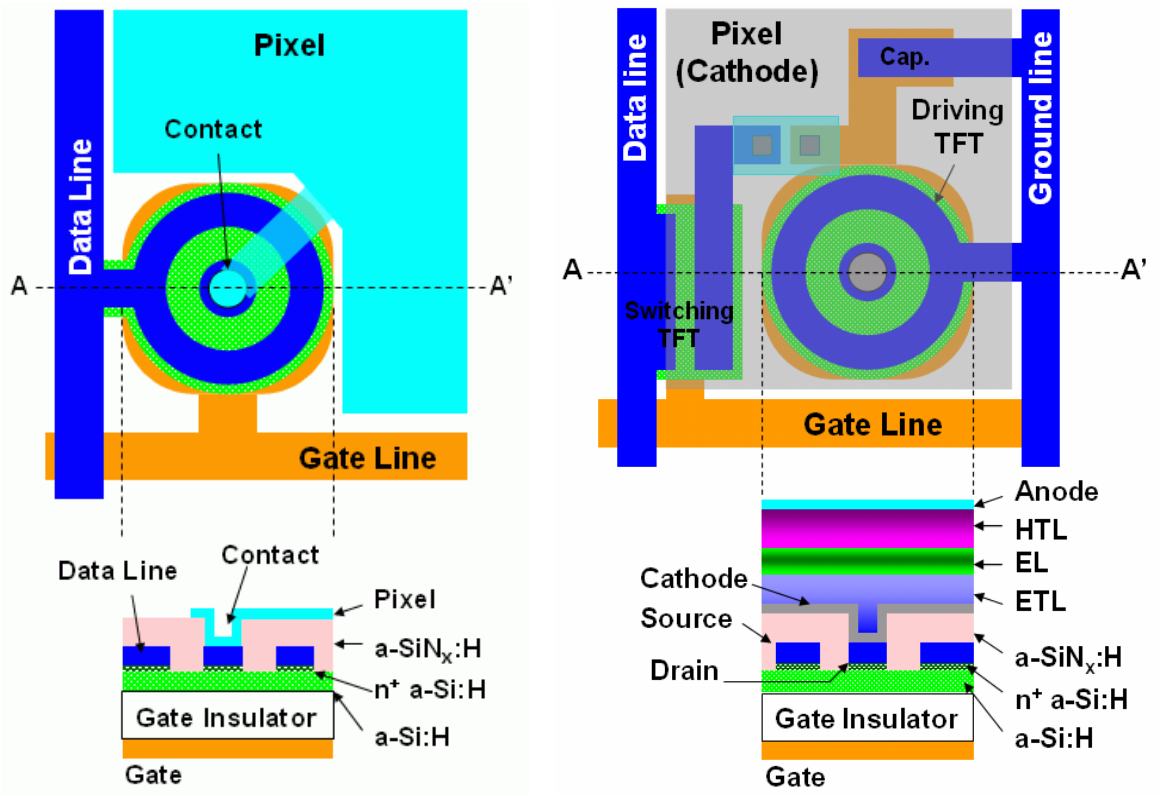
table that those two methods provide very similar mobility and threshold voltage values for a-Si:H TFTs (within experimental error). Figure 4.7 shows the evolution of field-effect mobility by eqn (4.9) for each drain bias condition. In linear regime operation (V_{DS}=0.1 V), the value of field-effect mobility rises very fast from around threshold voltage and saturates with gate bias for both drain bias conditions as in normal MOSFET. In saturation regime operation (V_{DS}=Vsat), the value of field-effect mobility rises very fast from around threshold voltage but decreases with gate bias after the peak due to the scattering effect at the channel interface.

As shown in the table, due to a lower OFF-current, sub-threshold slope is much lower in condition (1), while the field-effect mobility and threshold voltage are similar for each condition. Therefore, asymmetric biasing of the Corbino a-Si:H TFT can change the ON- and OFF-current ratios while the field-effect mobility and threshold voltage remain the same regardless of drain bias conditions. This enhanced ON-OFF current ratio has advantage when device is used as a driving device for AM-OLEDs where the constant current should be applied to organic light-emitting device (OLED) with the minimum leakage current during display operation.

Since the ring-shaped electrode provides a uniform electric field distribution in the channel and eliminates any local electric-field crowding due to sharp corners present in normal TFT, Corbino TFT is expected to have a better electrical stability and larger W/L ratio at the same time in comparison to normal TFTs. This topic will be addressed in more detailed in future publications [11]. Finally, to reduce the pixel electrode parasitic capacitances, the gate electrode can be patterned into a ring-shape to be localized beneath the source and drain contacts.

4.6 Possible Applications of Corbino a-Si:H TFTs

Figure 4.8 (a) and (b) presents schematic top views and cross-sections of Corbino a-Si:TFT that can be used as a switching TFT for a conventional AM-LCDs and a driving TFT for AM-OLEDs, respectively. The storage capacitor is not taken into consideration in these simple pixel electrode schematics. When the device is used as a switching TFT, Figure 4.8 (a), with the minimized overlapped area between the gate and pixel electrode when the pixel electrode is patterned, Corbino TFT has an advantage of having a much smaller parasitic pixel-to-gate capacitance than normal TFT [4]. This will provide a minimum pixel voltage drop (error voltage) with gate pulse in the OFF-state. By achieving a low error voltage, the display quality of the a-



(a)

Figure 4.8 Top views and cross sections of Corbino a-Si:H TFT for (a) AM-LCD (b) AM-OLED.

Si:H TFT AM-LCD can be improved [10]. However, in AM-LCD driving scheme, the polarity of data line bias usually changes from line-to-line with respect to the common (line inversion method); hence the positions of drain and source in TFT should be opposite in odd and even data lines. In such case, as mentioned above, TFTs in the active-matrix array will have different ON- and OFF- current values for different lines. Since ON-current is only used for charging the storage capacitor, asymmetric ON-current does not make any difference in storage capacitor voltage as long as the switch turn-on time is long enough. The switch turn-off time is relatively very long compared with switch-on time in AM-LCD operation. Therefore, due to the asymmetric OFF-current behavior of Corbino a-Si:H TFT, stored charges in storage capacitor may vary between lines, which can cause dramatic change in storage capacitor voltage. This change in storage capacitor voltage can cause the difference in the light transmittance of liquid crystal (LC), and create a possible line MURA defect in AM-LCD [11].

Figure 4.8 (b) shows proposed Corbino a-Si:H TFT to be used as a driving TFT (only driving TFT is considered in this simple pixel electrode circuit) integrated with the top light-emitting anode OLED in AM-OLEDs. The TFT structure is identical to a switching TFT in AM-LCDs. Pixel electrode is, however, made of aluminum (Al) or aluminum alloy coated with the metal thin layer such as magnesium (Mg) or calcium (Ca) instead of ITO since this layer is used as a cathode in OLED. Then electron-transporting layer (ETL), organic light-emissive layer (EL), and hole-transporting layer (HTL) are deposited successively over cathode electrode. Finally, transparent thin metal oxide (WO_3 or MoO_3)/ITO or Al bi-layer is deposited as an anode to form a top light-emitting anode OLED structure. In AM-OLED, the gate of driving n-channel TFT should be always on to supply constant current flowing to OLED. Therefore, pixel voltage is not likely to be affected by the gate-to-drain capacitance of TFT, and we can extend the area of pixel

electrode to maximize the pixel aperture ratio. In addition, since positions of source and drain are always fixed in driving TFT, we can enhance the ON- and OFF- current ratio and minimize the OFF-current by using the outer ring electrode as source in Corbino a-Si:H TFTs. At the same time, such device design provides flexibility to realize the high W/L ratio needed to achieve high ON-current levels.

4.7 Conclusions

In this research, we have studied the asymmetric electrical characteristics of Corbino a-Si:H TFT associated with different drain bias conditions. Due to unique Corbino disk geometry, when source is connected to outer ring electrode, ON-current is about two times higher, and OFF-current is about ten times lower than when source is applied to inner circle electrode at high drain voltages (>10V). However, threshold voltage and field-effect mobility remain same for both drain bias conditions.

We also found that the Corbino a-Si:H TFT might not be adequate switching device for AM-LCD due to the asymmetric OFF-current behavior; the leakage current would vary depending on the drain bias condition. However, at the same time, thanks to its high ON-current and possible enhanced electrical stability, Corbino a-Si:H TFT is a good candidate as a driving TFT for top light-emitting anode AM-OLEDs.

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CHAPTER 5

Hexagonal a-Si:H TFTs, a New Advanced Technology for Flat Panel Displays

5.1 Introduction

Thanks to the spatial uniformity and simple processing, hydrogenate amorphous silicon thin-film transistor (a-Si:H TFT) has been widely used over last 10 years as a active-matrix array backplane for a large area flat panel displays and imaging arrays. However, at the same time, due to its low carrier field-effect mobility, a-Si:H TFT is suffering from a low drain current for a given gate / drain bias which becomes a critical factor for a driving TFT in active-matrix organic light-emitting devices (AM-OLEDs) or in-plane gate drivers [1] for flat panel displays. In a-Si:H TFT, a high drain current can be achieved by simply increasing the channel width for a given length (i) using normal source / drain electrodes, (ii) comb-shaped electrodes [2], or (iii) fork-shaped electrodes [3]. However, it is known that the single transistor with the increased channel width results in the serious TFT threshold voltage variation [4, 5]. Alternatively, Corbino a-Si:H TFT [6] structure can be employed; its unique asymmetric ring shape electrode enables to achieve a high output current, and provide better electrical stability by eliminating sharp corner present in classical devices. However, due to the area limits in pixel electrodes and its unique electrode shape, the channel width of Corbino a-Si:H TFT as a single transistor can not be enlarged enough to achieve a high current required for high resolution flat panel displays or in-

plane gate drivers.

In this chapter, to address above mentioned issues, we are proposing for the first time parallel-connected hexagonal a-Si:H TFTs for a given pixel circuit to achieve a high stable output current over time. We choose the hexagonal shape for multiple a-Si :H TFT structure since it represents an optimum shape to minimize the areal occupation when TFTs are integrated together in parallel in a given circuit. At the same time, we also expect that the multiple hexagonal a-Si :H TFT structure can achieve a higher output drain current with better electrical stability in comparison to other single a-Si :H TFT structures. First we report on single and multiple hexagonal a-Si:H TFTs (HEX-TFTs) electrical characteristics. More specifically, we describe effects of the parallel connection of single HEX-TFTs on overall device performance. We also discuss the impact of number of the HEX-TFT on the extracted key device electrical parameters such as sub-threshold slope, field-effect mobility, and threshold voltage, that are important for active-matrix liquid crystal displays (AM-LCDs) and active-matrix organic light-emitting devices (AM-OLEDs). Then, we compare electrical properties of the multiple HEX-TFT connected in parallel with standard single a-Si:H TFT having different equivalent channel widths. Finally, we present the electrical stabilities and pixel aperture ratio of multiple HEX-TFT in a given pixel area in comparison to single standard a-Si:H TFT. To our best knowledge, this chapter represents the first investigation of the electrical characteristics of single and multiple HEX a-Si:H TFTs and their proposed application to flat-panel displays. We consider this chapter as introduction to a new advanced a-Si:H TFT technology for future flat panel displays.

5.2 Multiple a-Si:H Hexagonal TFT Structure and Fabrication

In this research, a series of a-Si :H TFTs connected in parallel, with a gate length of

Device Name	Channel Length (L)	Number of Multiple TFT	Effective Channel Width (W_{EFF})	
			Linear	Saturation
Hex-1	5 μm	1	285 μm	300 μm
Hex-2	5 μm	2	570 μm	600 μm
Hex-4	5 μm	4	1140 μm	1200 μm
Hex-8	5 μm	8	2280 μm	2400 μm

$W_{EFF\text{-}Linear}$ = Number of HEX-TFT × 6 × (R_1 + L/$3^{1/2}$)

$W_{EFF\text{-}Saturation}$ = Number of HEX-TFT × 6 × R_2

Table 5.1 Device dimensions of various multiple Hexagonal a-Si:H TFTs.

5μm, consisting of octuple Hexagonal TFTs (Hex-8), quadruple Hexagonal TFTs (Hex-4), double Hexagonal TFTs (Hex-2), and a single Hexagonal TFT (Hex-1), were fabricated as listed in Table 5.1. All HEX-TFT structures were constructed of the indentical single Hexagonal a-Si :H TFT as a base unit, and all gate, drain, and source electrodes of the HEX a-Si :H TFTs are connected in parallel, respectively, Figure 5.1. The single Hexagonal a-Si:H TFT is consisting of inner hexagonal electrode (outer side length R_1= 44 μ m) and outer ring-shaped hexagonal electrode (inner side length R_2=50 μ m), Figure 5.2. Bottom gate electrode is large enough to cover the entire area of device outer and inner electrodes. Fig. 5.2 (b) presents the cross-section of single Hexagonal a-Si:H TFT structure. All multiple Hexagonal a-Si:H TFTs were fabricated using the normal AM-LCD 5-photomask process steps [7]. More specifically, on the Corning Eagle2000 glass substrate, bi-layer of aluminum-neodymium compound (AlNd, 2000Å) and molybdenum (Mo, 500Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet-etching (Mask #1). Following gate electrode definition, hydrogenated amorphous silicon nitride (a-SiN_X:H, 4000Å)/a-Si:H (1700Å)/phosphorous-doped a-Si:H (n^+ a-

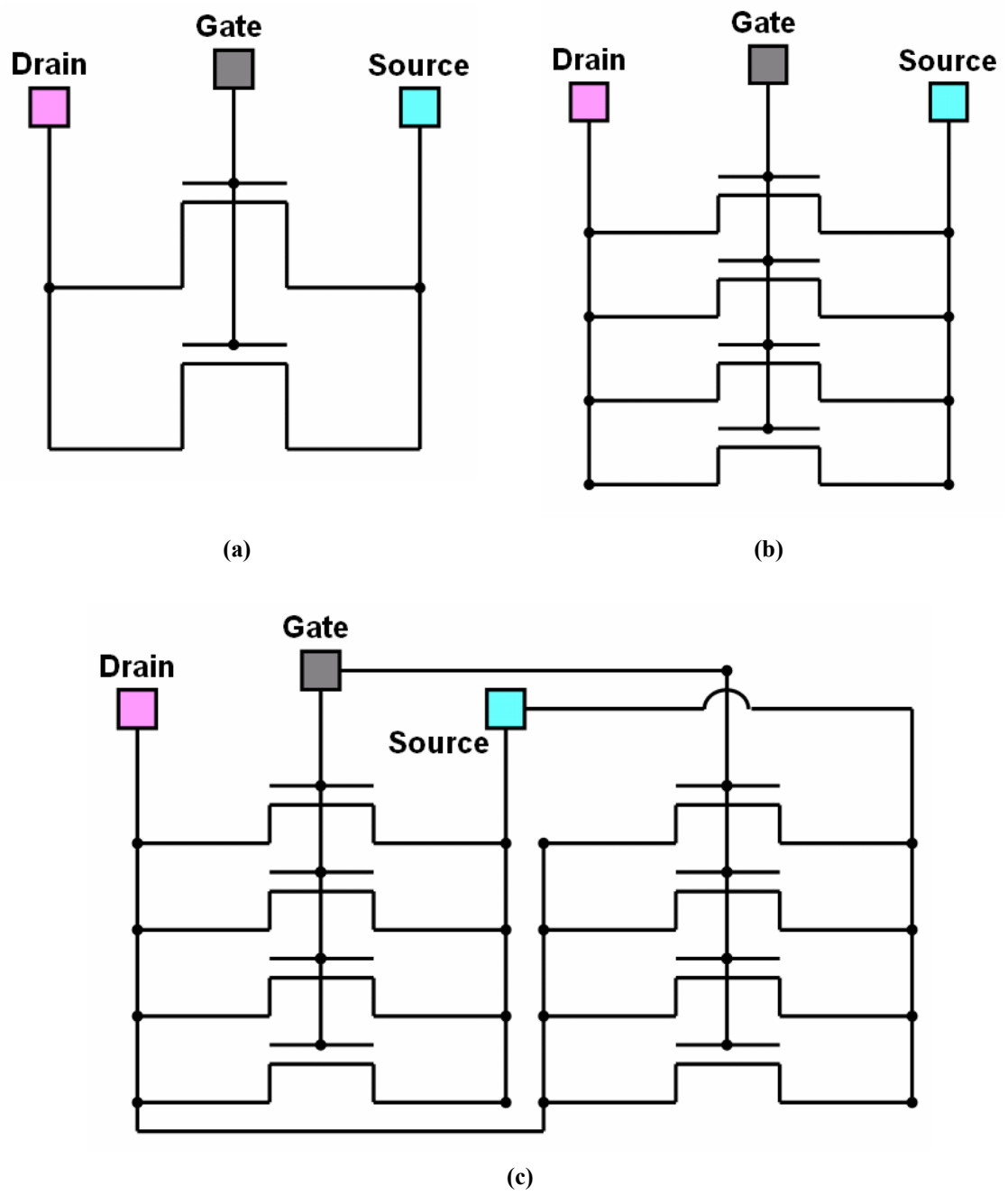
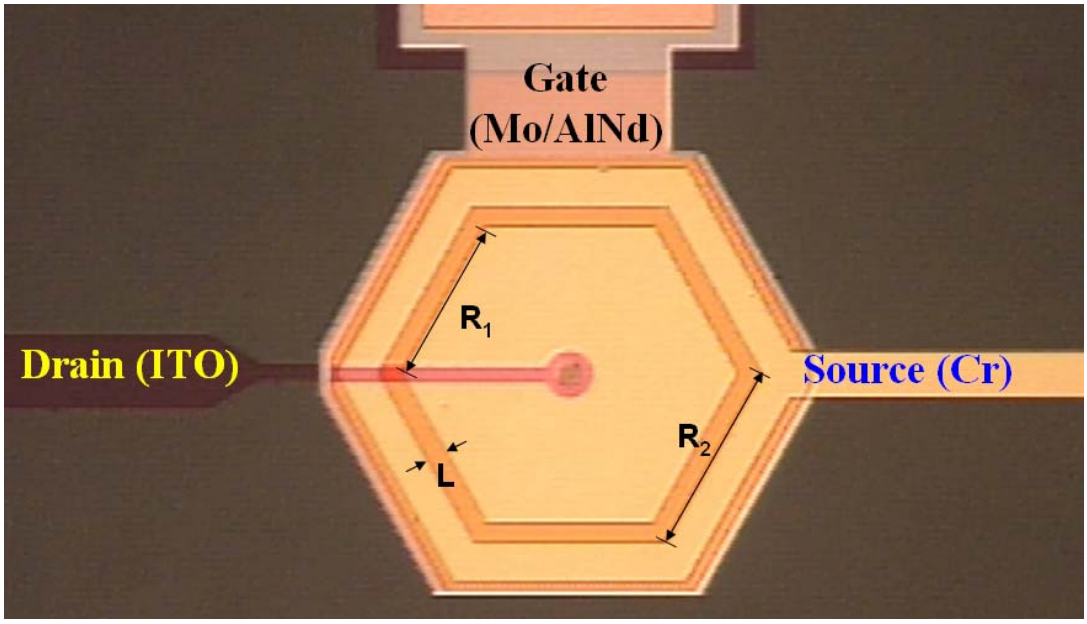
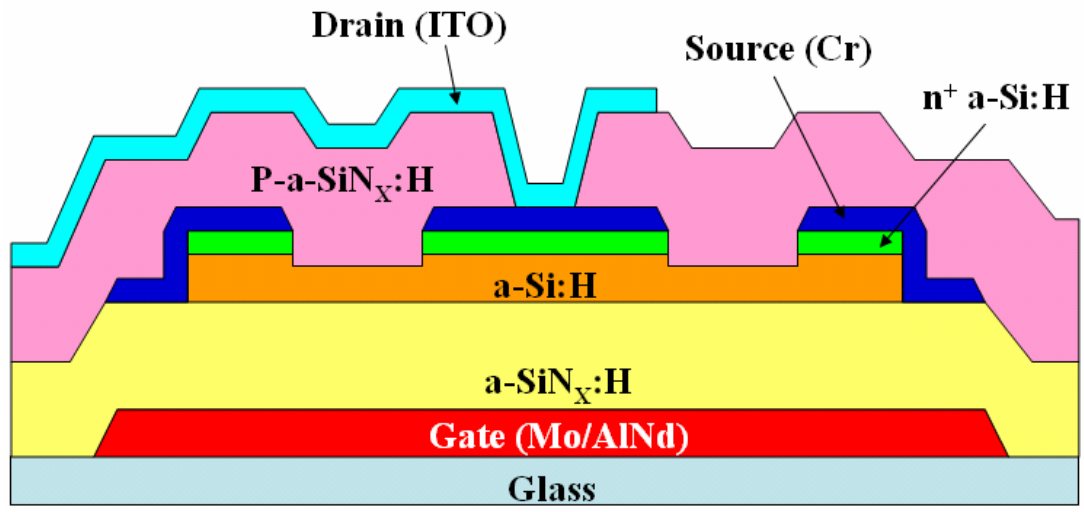


Figure 5.1 The schematics of a-Si:H Hexagonal TFTs connected in parallel; (a) double (Hex-2) (b) Quadruple (Hex-4), and (c) Octuple (Hex-8) a-Si:H HEX-TFTs.

Si:H, 300Å) tri-layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 ºC to form gate insulator and active channel layer, respectively. After defining the device



(a)



(b)

Figure 5.2 (a) The top and (b) the cross-section views of single a-Si:H Hexagonal TFT device.

active island by reactive ion etching (RIE) (Mask #2), a chromium (Cr, 1200Å) layer was deposited by sputtering, and source/drain (S/D) electrodes were patterned by wet-etching (Mask #3). Using S/D metal and photo resist as masks, the back-channel-etching by RIE was performed.

Then, we deposited a-SiN_X:H (3000Å) as a passivation layer by PECVD at 300 ºC. To make a contact for the pixel electrode indium tin oxide (ITO), via was formed through the passivation (PVX) layer by RIE (Mask #4). After contact via definition, ITO (500Å) was deposited by a sputtering method at room temperature, and then pixel electrodes were patterned by wet-etching (Mask #5). As a final step, the device thermal annealing was performed for an hour at 235 ºC; this step is needed to improve ITO optical and electrical properties. It should be noted that all fabricated HEX-TFT were not considered for minimizing the area occupation in the pixel circuit, and this issue will be discussed later in a separate chapter in this paper.

5.3 Experimental Results and Discussions

5.3.1 Electrical Characteristics of Multiple a-Si:H HEX-TFTs

To characterize the electronic properties of multiple HEX-TFT connected in parallel, we first measured the output characteristics for different configurations, Figure 5.3. We have shown in the previous study that the Corbino a-Si:H TFT [6] with the asymmetric electrode geometry could have different electrical properties depending on the drain bias condition. In this study, we fixed the drain bias condition to achieve the highest output drain current level by applying the drain bias on the inner hexagonal electrode and the source (ground) on the outer ring-shaped hexagonal electrode, Figure 5.3. We swept the drain bias from 0 to 20V for various gate voltages (0, 10, 20, and 30V), and the output current of multiple Hexagonal a-Si:H TFTs increases linearly with the increasing number of Hexagonal a-Si:H TFT unit in parallel following equation of given below. To check linearity of the total output current with the number of HEX-TFT, we calculated the total output current value for different multiple a-Si:H HEX-TFT configurations by

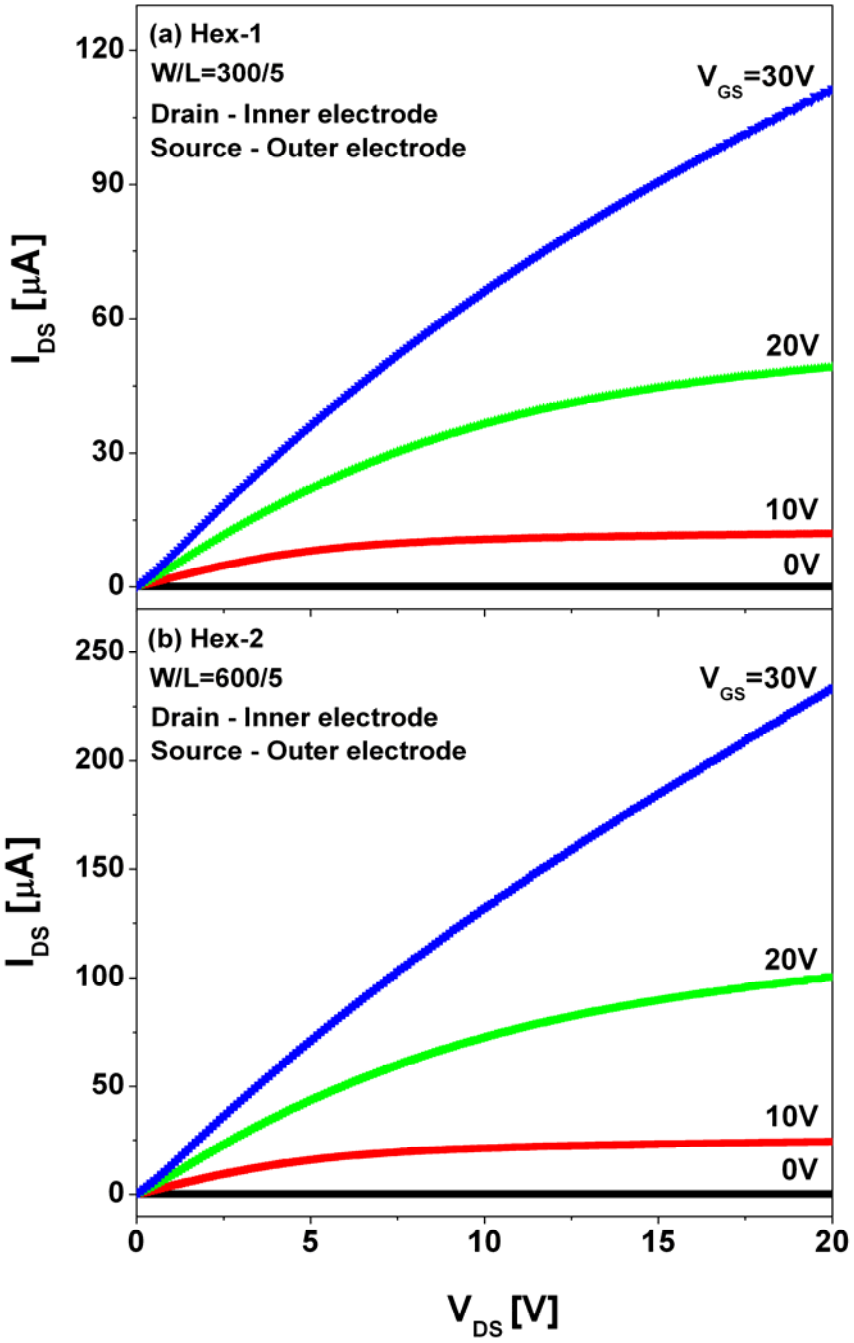


Figure 5.3 Output Characteristics of multiple a-Si:H Hexagonal TFTs; (a) single (Hex-1) (b) double (Hex-2) a-Si:H HEX-TFTs.

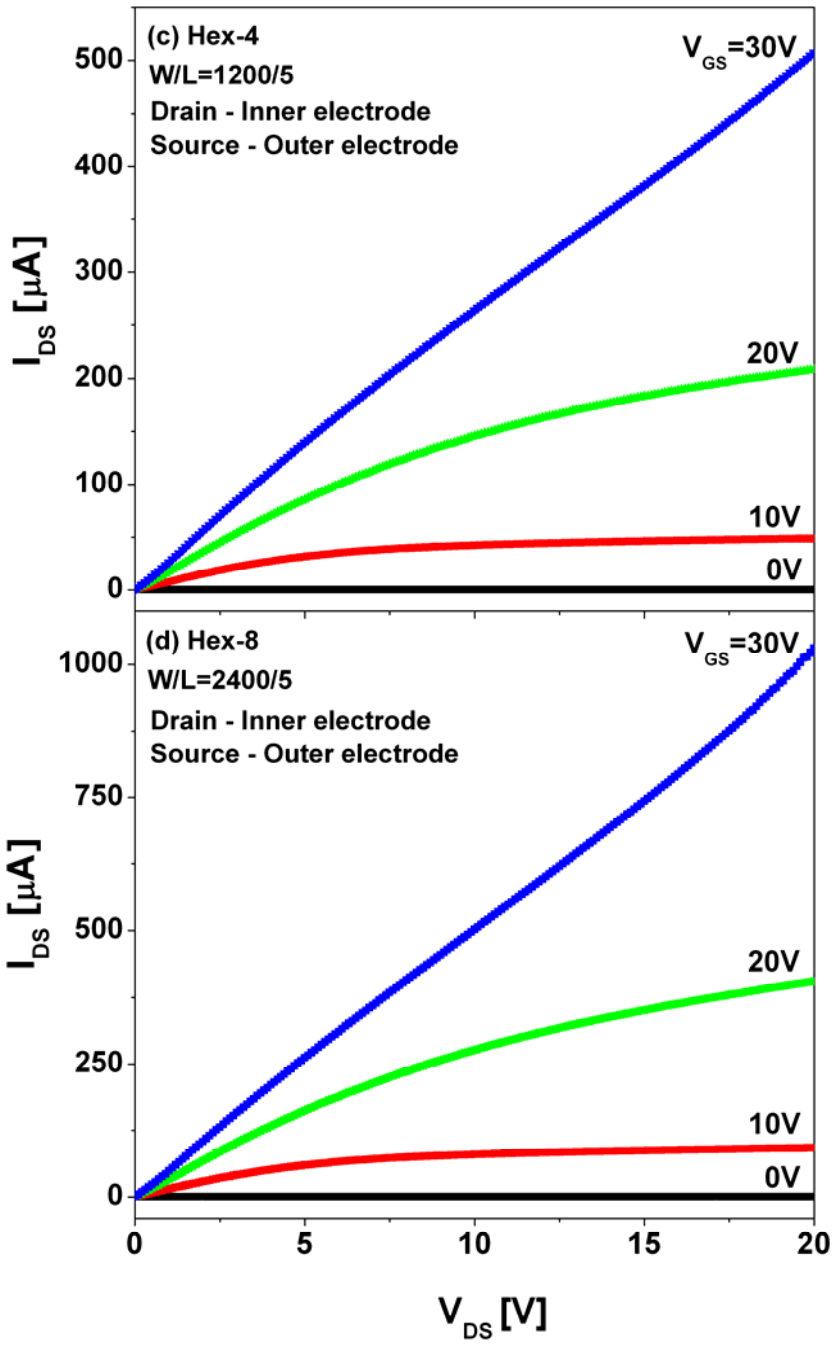


Figure 5.3 Output Characteristics of multiple a-Si:H Hexagonal TFTs; (c) Quadruple (Hex-4), and (d) Octuple (Hex-8) a-Si:H HEX-TFTs.

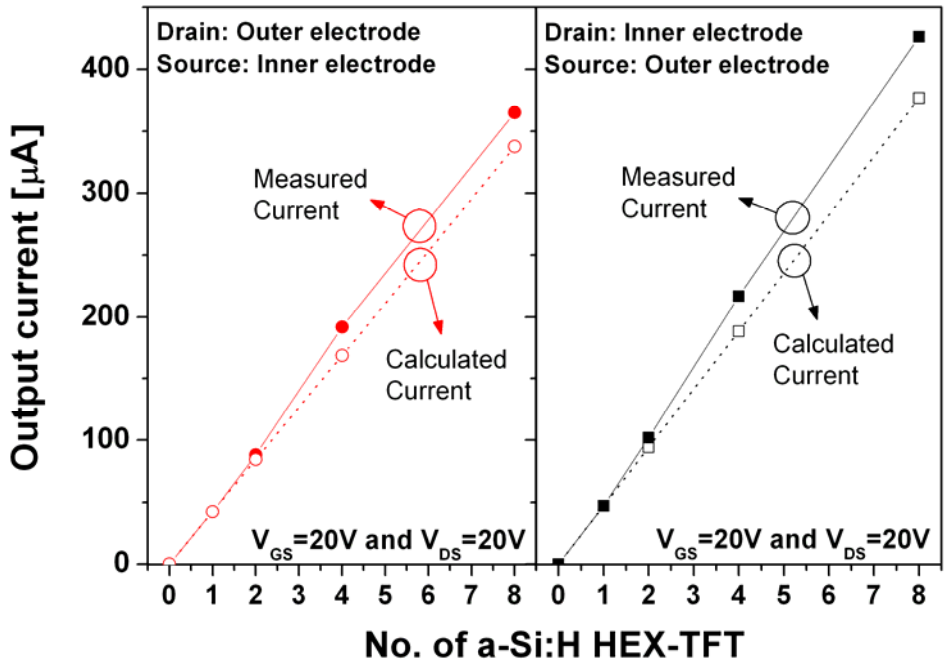


Figure 5.4 Measured (closed symbol) and calculated (open symbol) output current values of multiple a-Si:H HEX-TFTs at V_{GS}=20 and V_{DS}=20V as a function of number of HEX-TFTs; (a) where drain is applied on inner electrode and source is on outer electrode, and (b) where drain is applied on outer electrode and source is on inner electrode.

multiplying the number of HEX-TFTs by the output current of a single a-Si:H HEX-TFT measured at V_{GS}=20V and V_{DS}=20V, and compared calculated values with the actual output current values of multiple a-Si:H HEX-TFTs measured at V_{GS}=20V and V_{DS}=20V, Figure 5.4. As shown in this figure, the measured output current values are only slightly higher (>10%) than the calculated values but shows a very good linearity with the number of multiple HEX-TFTs for both drain bias conditions:

$$I_{out}^{Total} \geq \sum_{i} I_{out}^{i} \tag{1}$$

where I_{out}^{Total} is the total output current for multiple HEX-TFTs and I_{out}^{i} is the output current for a single HEX-TFT used in parallel connected circuit. To verify this relationship, we measured the output current for different bias conditions (V_{DS}=5V, 10V and 15V), and the good linearity of output current was still observed with the number of multiple HEX-TFTs. Therefore, in this unique advanced a-Si:H TFT technology, a desirable output current level can be obtained by adjusting a number of HEX-TFTs used in a given pixel circuit. For example, to achieve desirable output current of 200 μA for a-Si:H TFT AM-OLED, we will need 4 of HEX-TFTs (Hex-4) connected in parallel.

Figure 5.5 shows transfer characteristics of multiple a-Si:H Hexagonal TFTs; we swept the gate bias from -10 to 20V for various drain voltages (0.1, 10, and V_{SAT}), where V_{SAT} is the drain voltage (V_{DS}) when the drain is connected to the gate electrode to keep the transistor in saturation regime ($V_{DS} = V_{GS} > V_{GS} - V_{TH}$). In Fig. 5.5 (a), for V_{DS}=0.1V and V_{SAT}, a single Hexagonal a-Si:H TFT shows sub-threshold slopes (SS) of 348 and 160mV/dec, respectively, and OFF-current levels of 2.0×10^{-13} and 8.5×10^{-13} A, respectively. Here sub-threshold swings for linear and saturation regimes of operation are defined as the inverse values of the steepest slopes of the respective I_{DS}-V_{GS} semi-log plots. By comparing electrical properties of multiple HEX-TFTs, the transfer characteristics reveal that the Hex-8 TFT, Fig. 5.5 (d), has a highest ON/OFF ratio of 8.7×10^{7} at V_{DS}=0.1V, and a smallest SS of 126 mV/dev at V_{DS}=V_{SAT}. It should be noted that when V_{DS}=V_{SAT}, I_{DS} becomes negative as V_{GS} changes to negative values. For this measurement condition, the drain and gate nodes are connected together. Therefore, when gate bias becomes negative, drain node also becomes negative. As a result, the potential at the drain node becomes lower than at the source node, and the current starts flowing from source to drain node (negative current). As shown in Fig. 5.6 (a), the sub-threshold slope for both V_{DS}=0.1V and

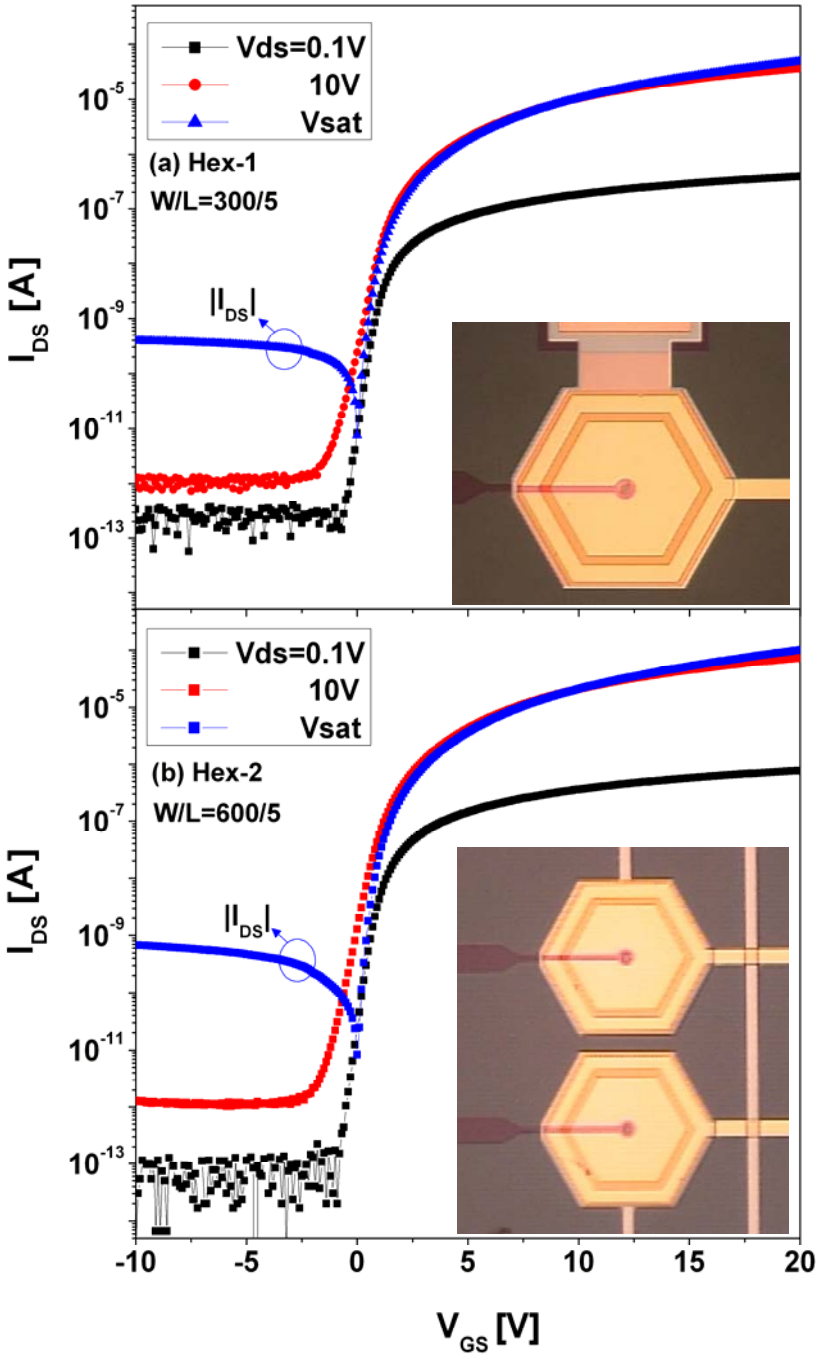


Figure 5.5 Transfer Characteristics and top-views of multiple Hexagonal a-Si:H TFTs where $|I_{DS}|$ represents the negative I_{DS} value; (a) single (Hex-1) and (b) double (Hex-2) a-Si:H HEX-TFTs.

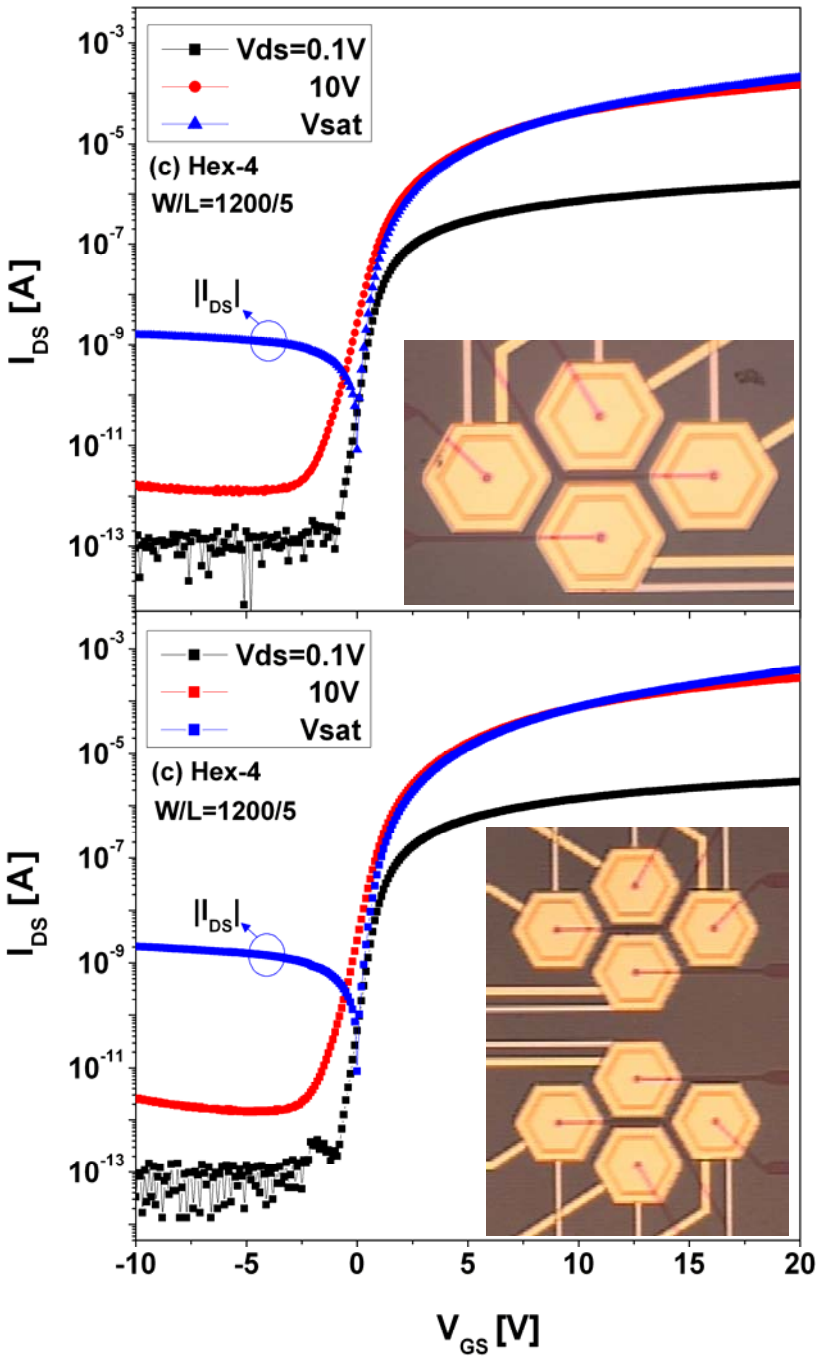


Figure 5.5 Transfer Characteristics and top-views of multiple Hexagonal a-Si:H TFTs where $|I_{DS}|$ represents the negative I_{DS} value; (c) Quadruple (Hex-4) and (d) Octuple (Hex-8) a-Si:H HEX-TFTs.

V_{SAT} decreases with the increasing number of the a-Si:H HEX-TFTs from Hex-1, Hex-2, and Hex-4, to Hex-8 while the OFF-current at V_{DS}=0.1V and 10V remains at the similar level within the error range regardless of the increasing number of HEX-TFTs. It is important to mention that all values presented are means of several separate measurements and the error bars stand for the standard deviation for these values.

Fig. 5.6 (b) shows a variation of the threshold voltage (V_{TH}) and field-effect mobility (μ_{FE}) as a function of number of Hexagonal a-Si:H TFTs. We extracted field-effect mobility (μ) and threshold voltage by using maximum slope method [6, 8] which is usually used for crystalline silicon devices. In this method, the field-effect mobility is calculated from transconductance maximum ($g_m=dI_{DS}/dV_{GS}$) value using following equations:

$$\mu_{Linear} = \frac{g_{m-Linear} \cdot L}{W_{EFF1} C_{OX} V_{DS}} \tag{1a}$$

$$\mu_{Saturation} = \frac{g^2_{m-Saturation} \cdot 2L}{W_{EFF2} C_{OX}} \tag{1b}$$

where $g_{m\text{-}Linear}$ is the maximum transconductance at V_{DS}=0.1V and $g_{m\text{-}Saturation}$ is the maximum transconductance at $V_{DS}=V_{SAT}$. From the value of V_{GS} corresponding to the g_m as a reference, two closest different gate bias values are chosen so that the straight fitting line is drawn based on these three points in the transfer characteristic curves. The threshold voltage is estimated from x-axis intercept of this extrapolated line for each drain bias condition. Based on our previous investigation of the geometrical effect on the a-Si:H TFT characteristics [6], The effective channel widths (W_{EFF1} and W_{EFF2}), for each drain bias condition, are calculated by following equations.

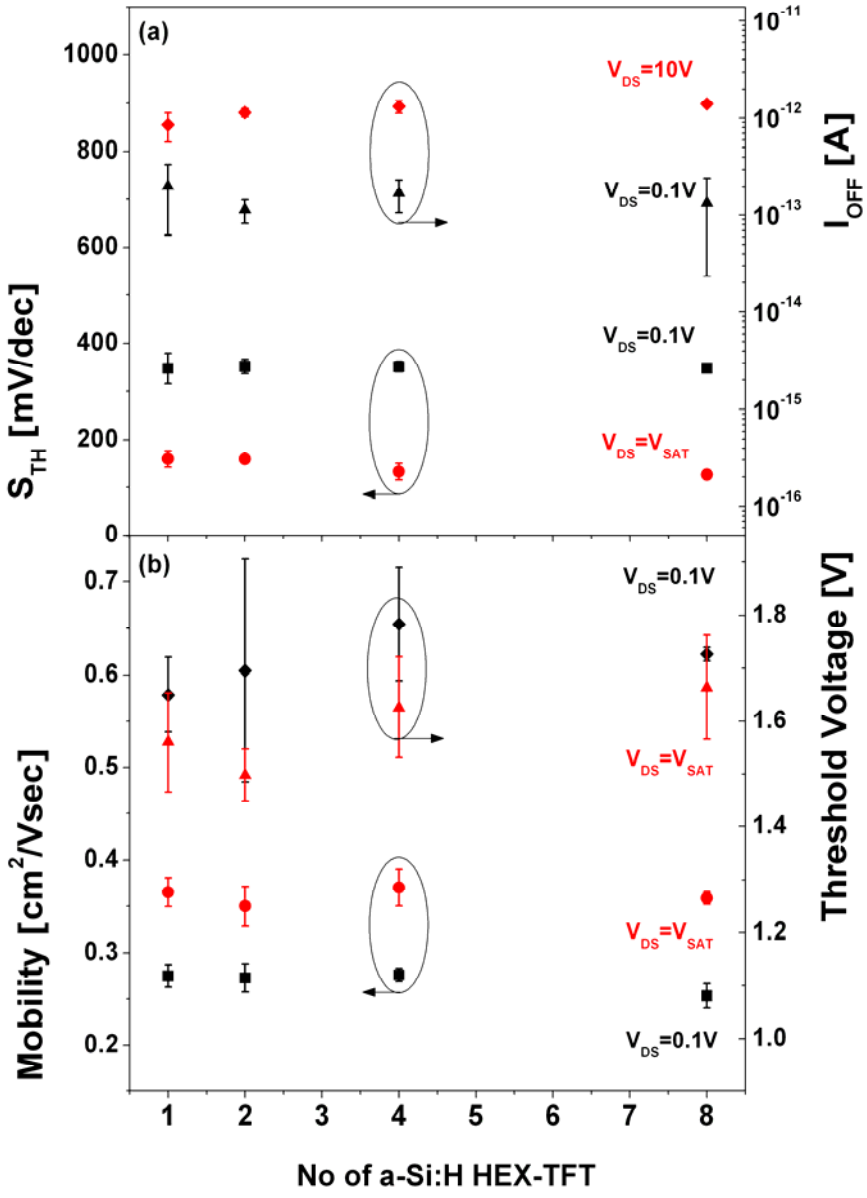


Figure 5.6 The trend of (a) sub-threshold swing and OFF-current, and (b) field-effect mobility and threshold voltage of multiple Hexagonal a-Si:H TFTs as a function of the number of TFTs.

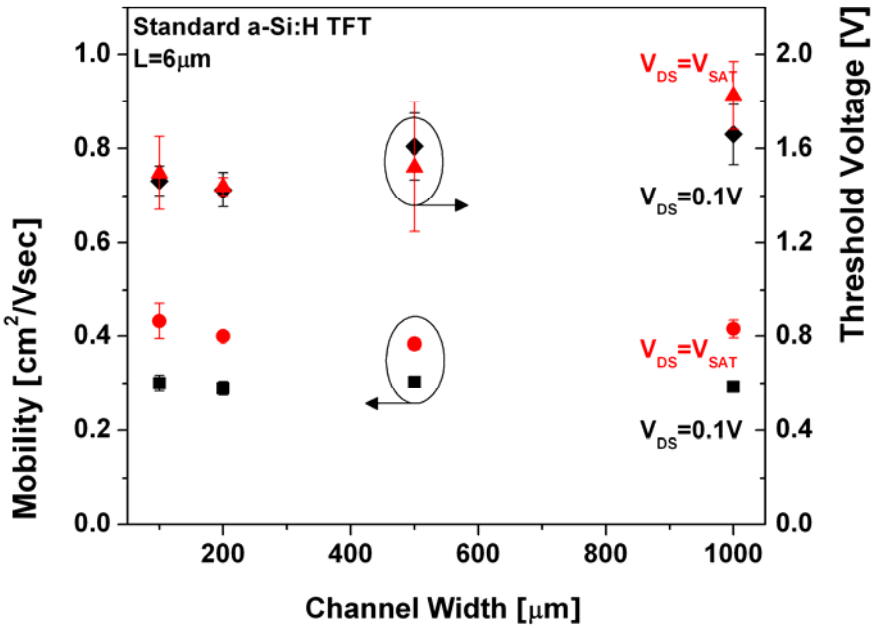


Figure 5.7 The trend of field-effect mobility and threshold voltage of standard TFT as a function of different channel widths.

$$W_{EFF1} = \text{Number of a-Si:H HEX-TFT} \times 6 \times (R_1 + \frac{L}{\sqrt{3}}) \quad \text{(2a)}$$

$$W_{EFF2} = \text{Number of a-Si:H HEX-TFTs} \times 6 \times R_2 \quad \text{(2b)}$$

Where W_{EFF1} is the effective channel width for linear regime operation (V_{DS}=0.1V), and W_{EFF2} is for saturation regime operation (V_{DS}=V_{GS}=V_{SAT}). Experimental results reveal that Hex-1, Hex-2, Hex-4, and Hex-8 a-Si:H TFTs yield almost the same field-effect mobility and threshold voltage values within the error range, indicating that the field-effect mobility and threshold voltage are not affected by numbers of the HEX-TFTs connected in parallel. Such TFT connection will allow increasing overall device channel width and output current at the same time. For the comparison, we also fabricated the standard a-Si:H TFTs with different channel widths, 100, 200, 500, and

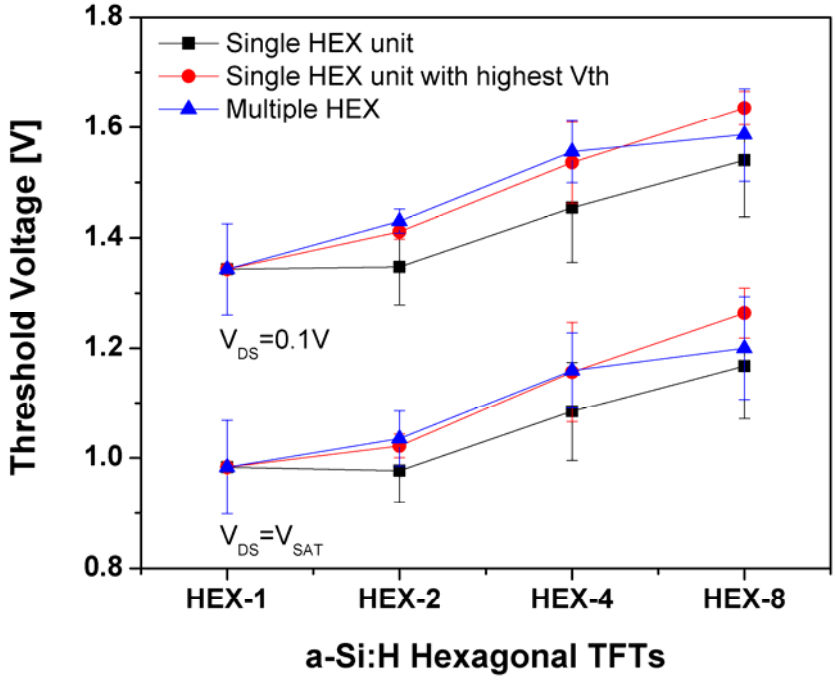


Figure 5.8 The trend of threshold voltage of single HEX-TFT base unit and of multiple HEX-TFTs as a function of number of Hexagonal TFTs.

1000 µm, and channel length L= 5µm. The field-effect mobility and threshold voltage values were calculated using the same method. As shown in Figure 5.7, for standard a-Si:H TFTs, the field-effect mobility does not change but the threshold voltage increases with the increasing channel width. Similar observation was made by others [9]. Hence, we expect that the threshold voltage increase will be more severe if the channel width increases to value higher than 1000 µm to be comparable to the total width of Hex-4 or Hex-8 a-Si:H HEX-TFT, Table 5.1. It should be noted again that all values presented are means of several separate measurements and the error bars stand for the standard deviation for these values.

To see the influences of the variation of the threshold voltage among single HEX-TFTs on the overall performance of multiple HEX-TFTs, we measured the threshold voltage of each

single HEX-TFT base unit in the multiple HEX-TFTs independently, and compared with V_{TH} of multiple HEX-TFTs, Figure 5.8. From the extracted V_{TH} values of single HEX-TFT units from multiple HEX-TFT, the highest V_{TH} was also plotted in the same figure. As shown in the figure, the V_{TH} of multiple HEX-TFTs shows the deviation from the V_{TH} of single HEX-TFT base units but shows a good agreement with the highest V_{TH} values of single HEX-TFT base units. Therefore, it is expected that one specific single HEX-TFT can affect the overall performance of the multiple HEX-TFT circuit. Therefore, this important variation should be considered in designing pixel electrode circuits with a-Si:H HEX-TFT with the optimized process control.

5.3.2 Electrical Stabilities and Pixel Area Occupation of the Multiple a-Si:H HEX-TFTs

To evaluate the thermal and electrical stability of the multiple Hexagonal a-Si:H TFTs for AM-OLEDs, we performed the current temperature stress (CTS) experiment for double (HEX-2) Hexagonal a-Si:H TFT. For the comparison, we chose the standard a-Si:H TFT with W/L=1000/6 and performed the same CTS experiment. For the CTS measurement, we connected gate and drain of TFT together and bias the constant current continuously through the drain to the TFT while the source was set to ground, Figure 5.9. In this way, we can avoid the stress by the gate bias and can investigate the electrical stress on the device only by the drain current. For HEX-TFT structure, the drain bias is applied on the inner electrode, and source is connected to the outer ring-shape electrode. Since all TFTs for the experiment have different W/L ratios, we applied different drain current levels depending on their channel width to maintain the same stress current density ($J_{DS} = I_{DS} / (W \times t_{CH}) = 1667$ A/cm^2), which corresponds to the drain current of 100 and 167 μA for HEX-2 (W/L= 600/5) and standard (W/L= 1000/6) a-Si:H TFTs,

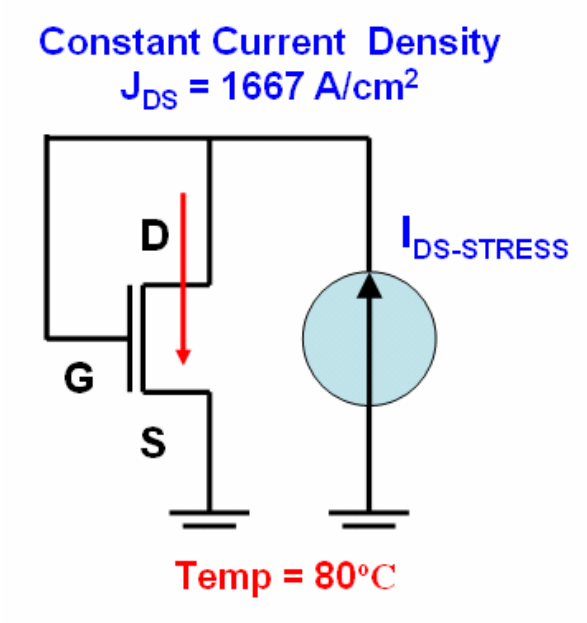


Figure 5.9 The schematics of the current-temperature stress (CTS) measurement set-up used for standard and multiple Hexagonal a-Si:H TFTs**.**

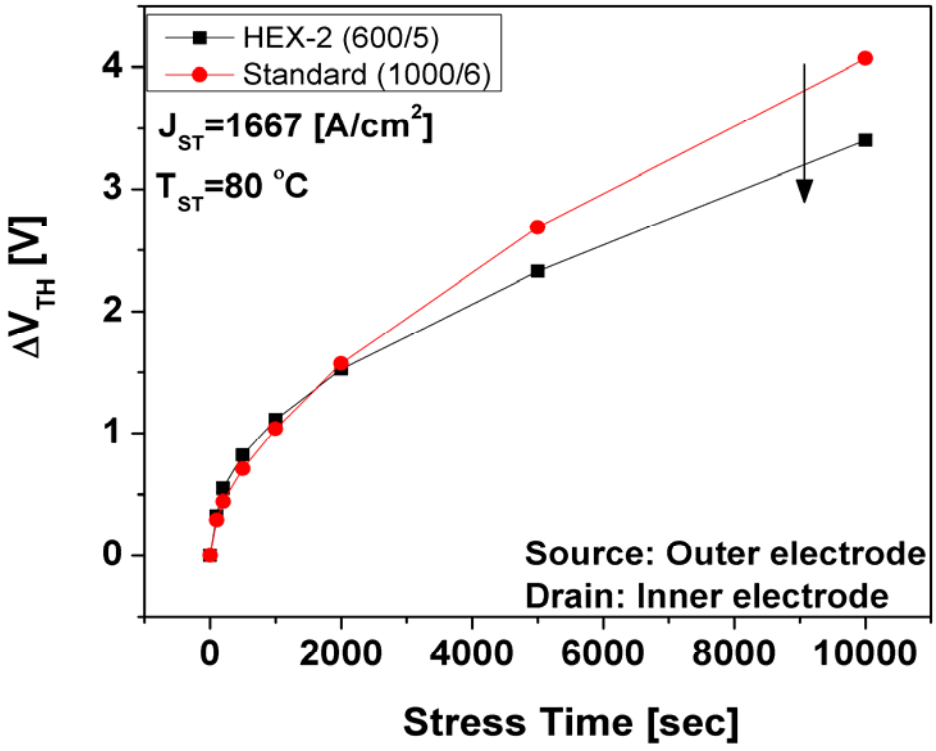


Figure 5.10 Variations of threshold voltage of double (HEX-2) Hexagonal a-Si:H TFT as a function of stress time at 80ºC in comparison to the standard a-Si:H TFT.

respectively. In calculating the channel current density, we assume that its thickness (t_{CH}) is same, 10nm, for all TFT structures. The stress current density value of 1667 A/cm^2 was determined to achieve the drain current of 100 μA from HEX-2 a-Si:H TFT at V_{DS}= V_{GS}= 20V, which corresponds to the luminance of 10000 cd/m^2 when the emission efficiency of OLED is 3.0 cd/A for the pixel size of 300×100 μm^2. All CTS measurements were performed under the accelerated stress condition by setting the stress temperature (T_{ST}) at 80 ºC. We measured the transfer characteristics of TFTs with V_{DS}=V_{SAT} (connected to gate bias) at the stress temperature (80 ºC) for different stressing times (t_{ST}) ranging from 0 to 10000 seconds. We only stopped device stressing for about 60 sec. to measure the transfer curves between stress times. From the transfer characteristics, the threshold voltages are extracted by the maximum slope method [8] for different stressing times. As the stressing time increases from 0 to 10000 seconds, the threshold voltage shift (ΔV_{TH}) of standard a-Si:H TFT increases from 0 to 4.1 V, while ΔV_{TH} of HEX-2 increases from 0 to 3.4 V, Figure 5.10. It means that for the same stress current density, the TFT threshold voltage shift for 10000 sec is reduced by 19.7% for HEX-2 TFT (W/L= 600/5) in comparison to the standard TFT (W/L= 1000/6). Therefore, parallel-connected multiple HEX-TFTs have an enhanced electrical stability in comparison to a single standard TFT with a similar W/L ratio.

It can be easily realized from the honeycomb structure that the hexagonal shape is very desirable in reducing a pixel area occupational space. Hence, by arranging the single Hexagonal a-Si:H TFT in a desirable way, we can expect a tremendous reduction in pixel area occupation for a given circuit design. Figure 5.11 shows layouts of standard TFT, interdigitated electrode TFT, and proposed quadruple Hexagonal TFT (HEX-4) with the same channel width and length (W/L= 330/6). All layouts were drawn in Virtuoso® layout environment using a-Si:H TFT array

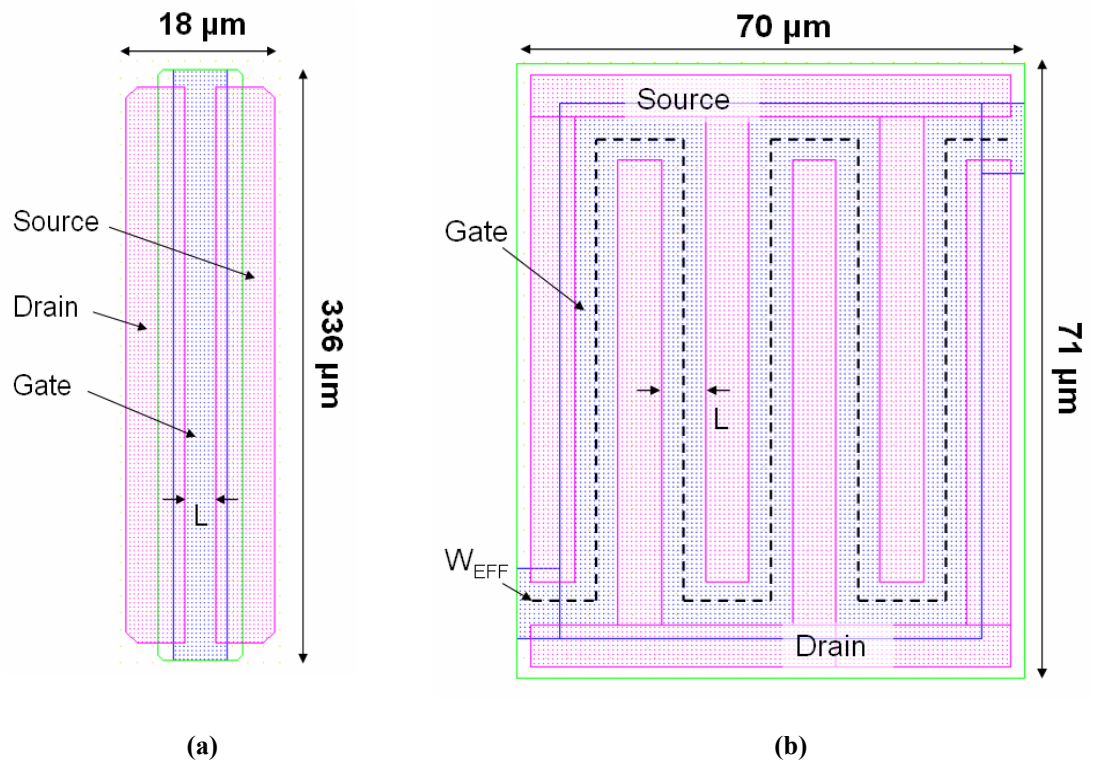
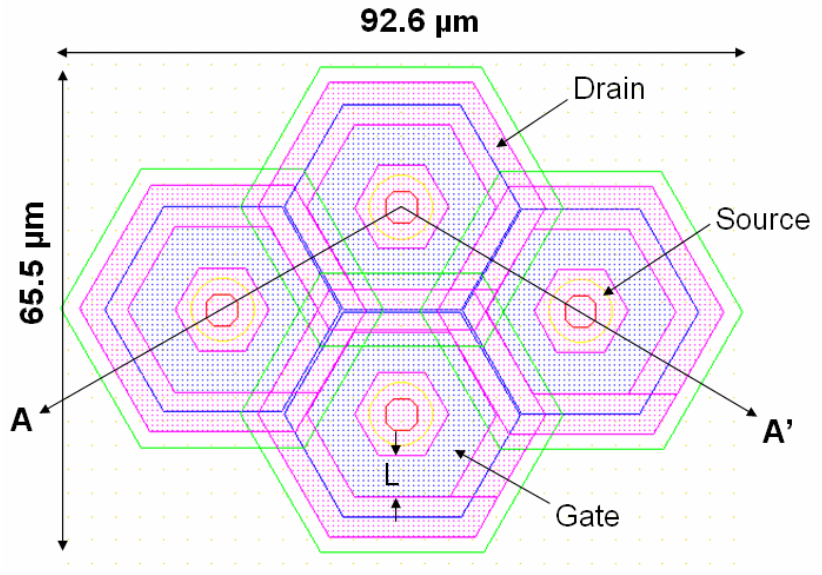
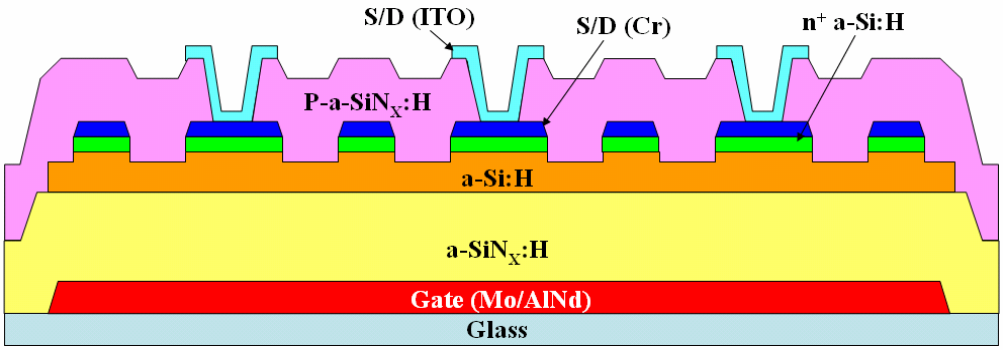


Figure 5.11 Layouts of (a) standard TFT and (b) interdigitated electrode TFT with the same channel width and length (W/L= 330/6). All layouts were drawn in Virtuoso® layout environment.

process design rules, and their respective channel width and length are kept same. For simplicity, we draw only electrodes of gate and source/drain without signal connection lines. Then we calculated the area of each TFT from the layout. Figure 11 (d) shows the cross-sectional schematic of proposed HEX-4 a-Si:H TFT. Same methodology was applied to other Hexagonal TFT structures (HEX-1, HEX-2, and HEX-8) and corresponding standard and interdigitated electrode TFTs. It should be noted that the size of inner electrode of all Hexagonal a-Si:H TFTs decreases to minimize the pixel area occupation and overlap parasitic capacitance. As shown in Figure 5.12 (a), the pixel area occupation ratio is reduced by 37% for HEX-4 TFT in comparison to the standard TFT with same W/L ratio, while a-Si:H TFT with the interdigitated electrode



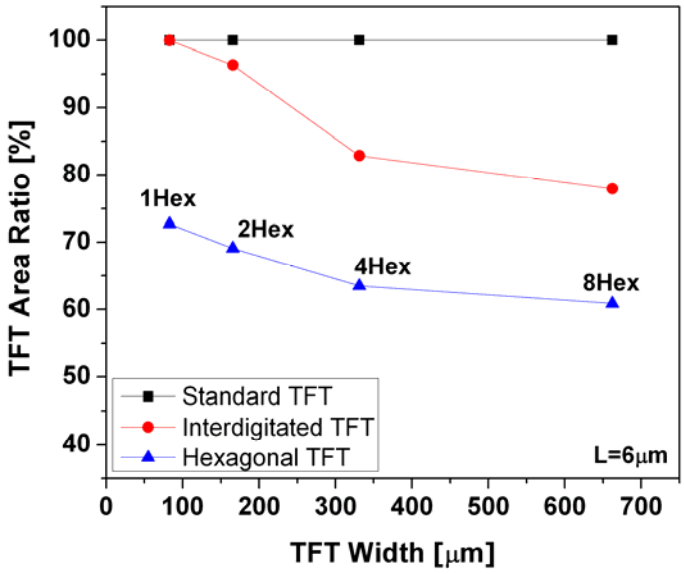
(c)



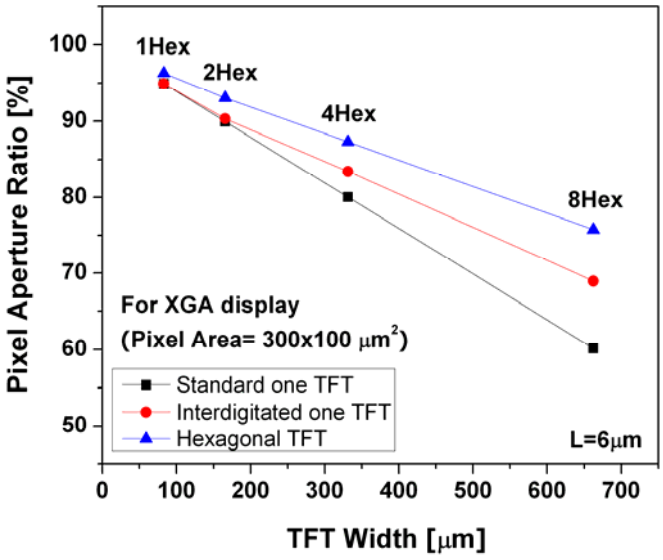
(d)

Figure 5.11 Layouts of (c) our proposed quadruple Hexagonal TFT (HEX-4) with the same channel width and length (W/L= 330/6). All layouts were drawn in Virtuoso® layout environment. (d) The cross-sectional schematic of proposed HEX-4 a-Si:H TFT.

shows a reduction of 17%. This reduction in the pixel area occupation becomes much larger from 27% to 39% as the number of Hexagonal TFT increases. Figure 5.12 (b) shows variation of a pixel aperture ratio as a function of channel width for different TFT structures in XGA display where the pixel area is 300×100 μm^2. The pixel aperture ratio is the ratio between the transmissive portion of a pixel and its surrounding opaque electronics (e.g., the thin-film transistors), expressed as a percentage. In the standard TFT, as the channel width increases, the



(a)



(b)

Figure 5.12 Variations of (a) TFT area occupation ratios and (b) pixel aperture ratios of proposed multiple Hexagonal a-Si:H TFTs in comparison to interdigitated electrode and standard a-Si:H TFTs. TFT area occupation being defined as area occupied by the gate and source / drain electrode of TFT. Pixel aperture ratio is defined as the ratio between the transmissive portion of a pixel and its surrounding opaque electronics for a given pixel area.

pixel aperture ratio decreases from 95% to 60.1%, while the multiple HEX-TFTs based pixel only show a small decrease from 95% to 76%. Therefore, as the device size becomes larger to achieve a higher current needed for AM-OLEDs, a multiple Hexagonal TFT structure has a higher probability for a given design in achieving larger pixel aperture ratio. In addition, since the overlapped area between source and gate electrodes in multiple HEX-TFTs is much smaller than in standard or interdigitated-electrode a-Si:H TFTs with the same channel width, we can expect reduced RC-delay and kick-back voltage in display. For example, if we use quadruple HEX-TFT (HEX-4) with W/L ratio of 330/5, the overlapped area between source and gate electrode is only 241 μm^2 while standard and interdigitated TFT have the overlapped area of 660 and 812 μm^2, respectively, with the same W/L ratio. Per previously published results on Corbino a-SI:H TFT [6], the overlap area between source and gate electrode in HEX-TFT can also be reduced by patterning the gate electrode beneath the source electrode into ring shape. Therefore, a minimal overlapped area between gate and source electrodes can be achieved in multiple HEX-TFTs.

Considering excellent electrical properties of parallel-connected a-Si:H HEX-TFTs, we expect that this new advanced a-Si:H TFT technology is suitable for driving TFTs to be used in future AM-OLED or gate-drivers [1] which require a high ON-current levels and adequate electrical stability. In addition, by substituting one standard a-Si:H TFT with a large channel width by the multiple HEX-TFTs with smaller channel width connected in parallel, we showed that a better electrical stability and much smaller pixel area occupation can be achieved for these new devices to be used for future flat panel displays.

5.4 Conclusions

In this research, we have studied the electrical properties of a single and multiple Hexagonal a-Si:H TFTs connected in parallel. As a number of a-Si:H HEX-TFTs increases, the overall output drain current increases linearly with their number per circuit while the sub-threshold slope decrease. At the same time, the OFF-current, threshold voltage, and field-effect mobility of multiple a-Si:H HEX-TFTs remain same regardless of the number of devices connected in parallel within a given pixel circuit.

Due to a high ON-current, stable field-effect mobility, and threshold voltage, parallel-connected a-Si:H HEX-TFT represents new a-Si:H technology that can be used to realize a high performance stable driving TFTs for future AM-OLEDs and a gate driver for a-Si:H TFT based flat-panel displays. The required output current level can be easily adjusted and controlled by choosing a desirable number of a-Si:H HEX-TFTs per pixel circuit. Finally, we expect that due to a unique device geometry, the multiple a-Si:H HEX-TFT show enhanced electrical stability and larger pixel aperture ratio in comparison to standard single a-Si:H TFT having same large channel width. These properties are required for future success of a-Si:H TFTs in more advanced flat panel displays.

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CHAPTER 6

Dynamic Measurements of Normal and Corbino a-Si:H TFTs for AM-OLEDS

6.1 Introduction

To date, active-matrix organic light-emitting display (AM-OLED) has attracted many interests from both industries and academia due to its superior properties over other flat panel displays such as light weight, thin thickness, high brightness, high contrast ratio, wide view angle, and deep color saturation. From small size displays for portable devices to large size displays for monitors and TV applications, AM-OLEDs are regarded as the next generation display expected to replace existing flat panel displays. Especially, thanks to the well matured active-matrix liquid crystal display (AM-LCD) manufacturing technology, hydrogenate amorphous silicon (a-Si:H) technology is considered as an ideal candidate for active-matrix arrays (so called backplane) for large size high resolution AM-OLED. Today many researchers are trying to develop a more stable backplane pixel electrode circuit with the compensation for the a-Si:H electrical instability. Because of its inherent low field-effect mobility and large parasitic capacitive elements originated from its relatively simple low resolution processing steps in comparison to silicon or poly-silicon technologies, a-Si:H TFT pixel electrode circuits show different dynamic responses from other well established technologies. Historically, in 1990's, several research groups [1 – 3] have reported measurement technique and analysis of dynamic characteristics of a-Si:H TFTs for AM-LCD displays. R. M. A. Dawson et al also showed the transient response of OLED on the

poly silicon based pixel electrode circuits for AM-OLED [4]. However, so far the detailed study in combination with the operational condition and capacitive element effects of on dynamic characteristics of a-Si:H TFT pixel electrode circuit for AM-OLED have not been described.

This chapter will discuss the dynamic characteristics of top- and bottom-gate a-Si:H TFTs that can be used in AM-OLEDs. The device fabrication of top-gate and bottom-gate a-Si:H TFT were described previously and experimental set-up used for dynamic measurement will be described in this chapter. The charging characteristics of top-gate a-Si:H TFTs will be covered in the second part of this chapter. The discussion, in particular, will focus on the effect of storage capacitance and TFT gate-to-source overlap on the switching TFT charging performance. Then the feed-though voltage in AM-OLED pixel electrode circuit and its variation with TFT geometries and driving signal will be discussed. Finally, we will discuss the dynamic characteristics of bottom-gate a-Si:H Corbino and normal TFTs. We will present the feed-through voltage property of a-Si:H Corbino TFT [5] in comparison to normal a-Si:H TFT, and simulate the dynamic characteristics based on top-gate a-Si:H TFT extracted parameters. To our best knowledge, this chapter represents the first investigation for the dynamic electrical characteristics

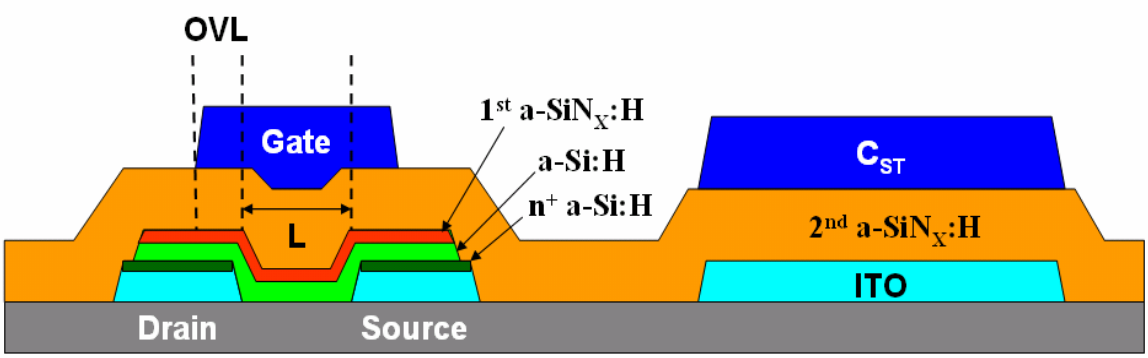
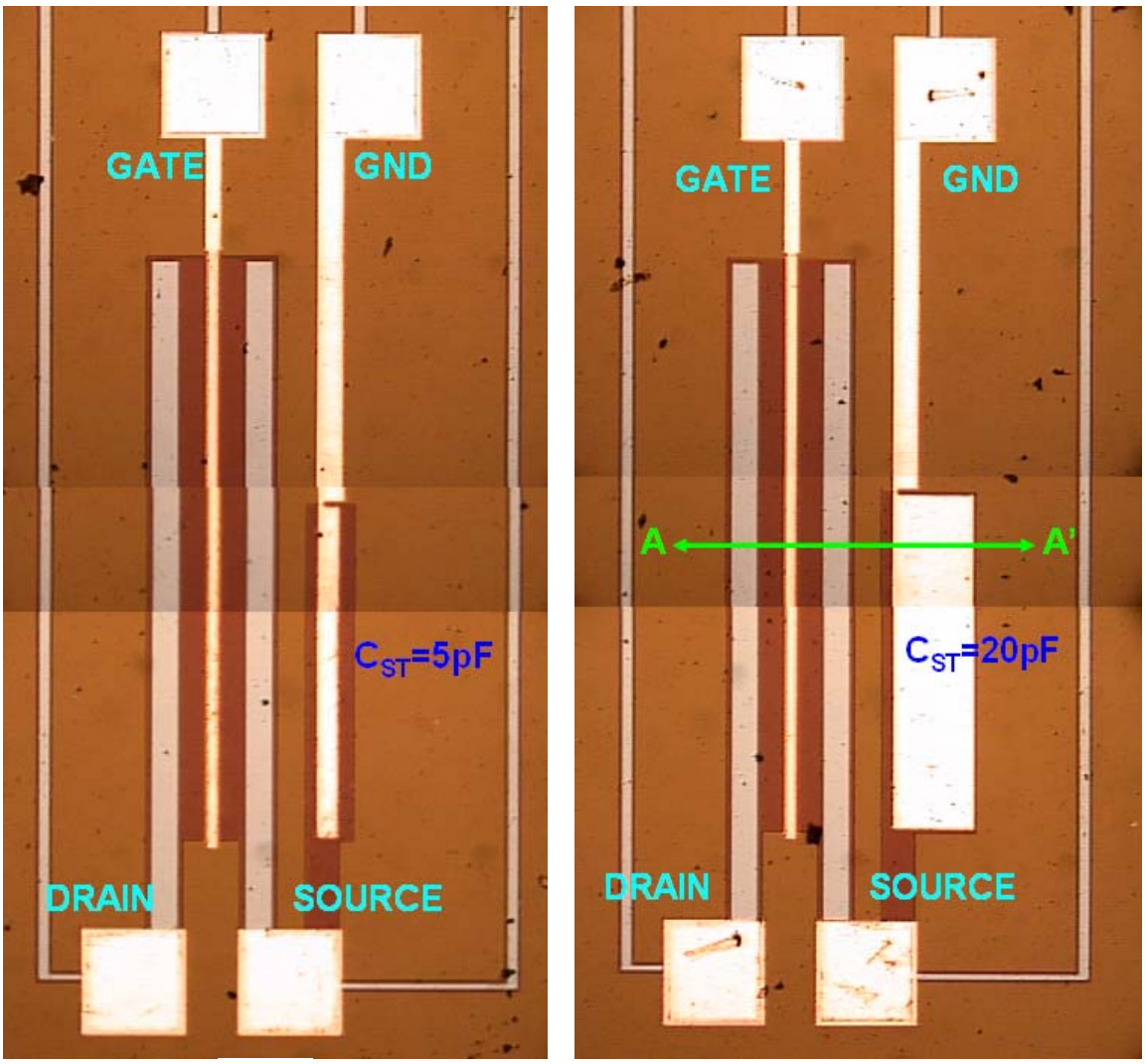


Figure 6.1 The schematic cross-section of top-gate a-Si:H TFT with a storage capacitor of normal and Corbino a-Si:H TFTs on their application to AM-OLEDs.

6.2 a-Si:H TFTs FABRICATION

6.2.1 Top-Gate a-Si:H TFTs

To characterize the dynamic behavior of a-Si:H TFT (charging and hold performance), top-gate a-Si:H TFTs with various storage capacitors are fabricated, Figures 6.1 and 6.2 [6]. For this experiment, a-Si:H TFT with the channel length of 10 μm and the width of 1000 μm is commonly used for various storage capacitors. The overlap between source/drain electrode and



(a) **(b)**

Figure 6.2 The top views of top-gate a-Si:H TFT with a storage capacitor of (a) 5pF, and (b) 20pF.

gate electrode (OVL) is maintained as 4μm. The source electrode of a-Si:H TFT is connected to a storage capacitor. The size of capacitor varies from 5, 10, 20 to 50 pF, which are about 10 to 100 times larger values than the actual storage capacitor used in AM-OLED pixel electrode circuit (~500 fF). Figure 6.1 shows the schematics of the cross section of fabricated top-gate a-Si:H TFTs with a storage capacitor. It is very difficult to monitor the pixel voltage variation when the storage capacitor is less than 2pF, since any perturbation in the probe measurement system can cause significant error. Therefore, to obtain non-perturbed measurement results, it is required to scale-up the storage capacitor size. It should be noted that these capacitor values are subject to the insulator thickness, and the designed capacitance values are obtained from 3300 Å thick a-SiN_x:H insulator. Four different storage capacitance values were achieved by changing the capacitor area as shown in Figure 6.2.

6.2.2 Bottom-Gate a-Si:H TFTs

The bottom-gate Corbino a-Si:H TFTs of different geometries with various storage capacitors have been fabricated to characterize the feed-though voltage behavior of Corbino a-Si:H TFT in comparison to top-gate TFT, Figures 6.3 and 6.4. For this experiment, the channel length of Corbino a-Si:H TFT is fixed at 6 μm while the channel width varies from 88 μm to 245 μm. The sizes of storage capacitors are also fixed at 0.9 and 2.5 pF, which are close to actual values of the AM-OLED pixel electrode design. Due to the unique geometry of Corbino TFT, the overlap between source/drain electrode and gate electrode varies from 5, 8 to 10 μm. The source electrode of a-Si:H TFT is connected to a storage capacitor. For direct comparison, we also fabricated at the same time the normal rectangular a-Si:H TFTs with the same geometries (same channel length and width) to measure the feed-though voltage behavior in comparison to Corbino

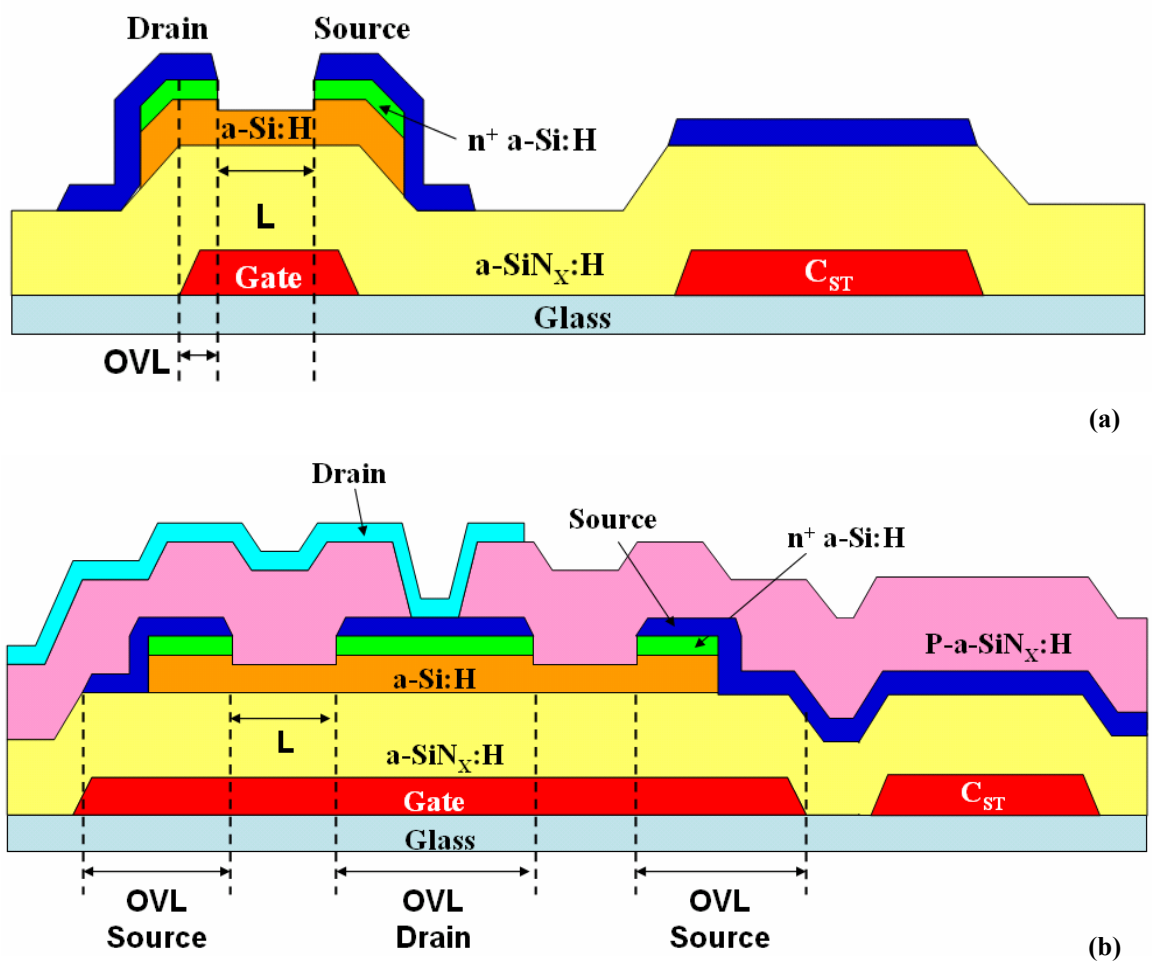


Figure 6.3 The schematic cross-section of (a) normal a-Si:H TFT with a storage capacitor, and (b) Corbino a-Si:H TFT with a storage capacitor.

a-Si:H TFTs, Figure 6.4. As in Corbino a-Si:H TFTs, the sizes of storage capacitors are fixed at 0.9 and 2.5 pF, and the overlaps between source/drain and gate electrode are fixed at 2.5 and 2.0 μm, respectively. Table 6.1 summaries the geometric parameters of different Corbino a-Si:H TFTs and normal rectangular a-Si:H TFTs with various storage capacitors. The schematic cross-sectional views of Corbino and normal a-Si:H TFTs with a storage capacitor are shown in Figure 6.3. All bottom-gate a-Si:H TFTs were fabricated using the normal AM-LCD 5-photomask process steps [7]. More specifically, on the Corning Eagle2000 glass substrate, bi-layer of

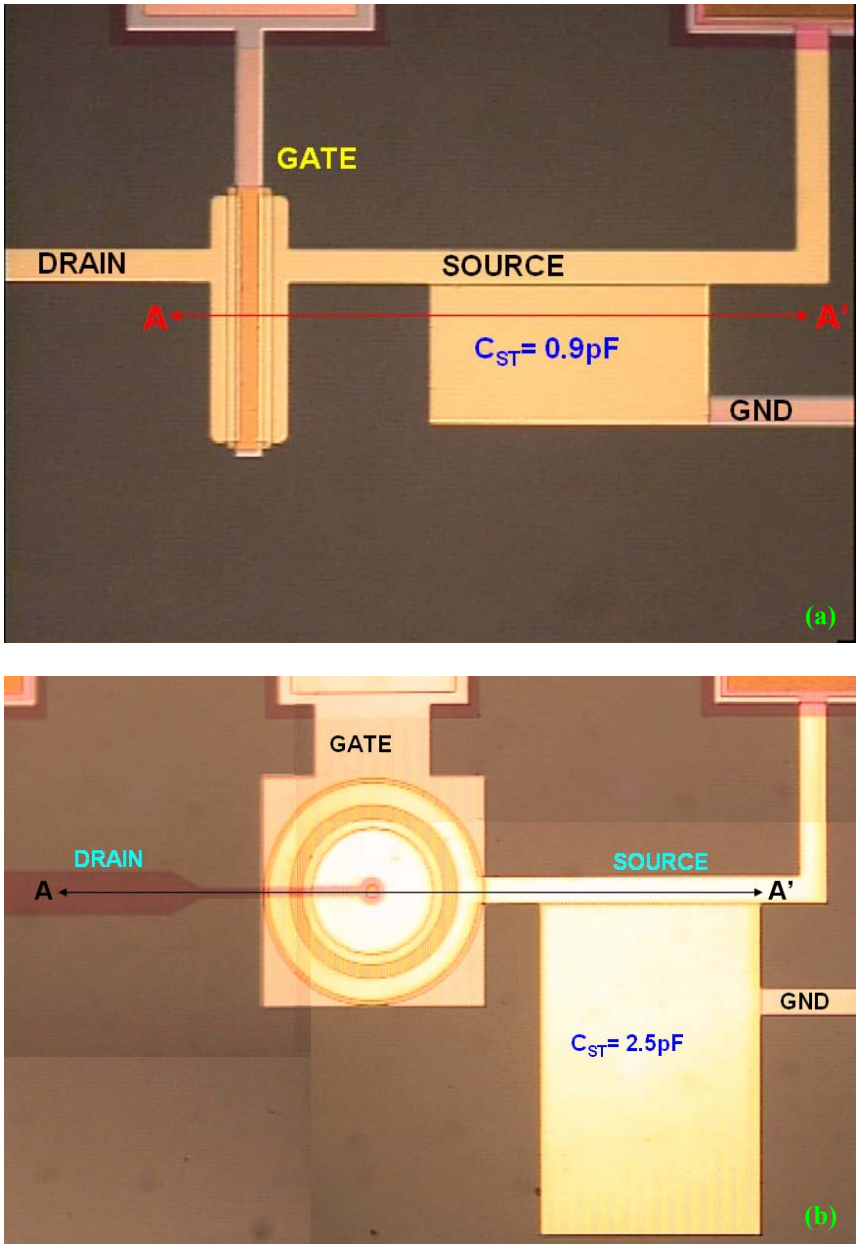


Figure 6.4 The top views of (a) normal a-Si:H TFTs with channel width over length ratio of 88/6 and a storage capacitor of 0.9 pF, and (b) the top views of. Corbino a-Si:H TFT with channel width over length ratio of 245/6 and gate-to-source overlap of 8μm.

aluminum-neodymium compound (AlNd, 2000Å) and molybdenum (Mo, 500Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet-etching (Mask #1). Following gate electrode definition, hydrogenated amorphous silicon nitride (a-SiN_X:H,

Normal	Width [μm]	Length [μm]	C_{ST} [pF]	C_{GSO} [pF]	OVL [μm]
(a)	88	6	0.9	0.026	2.5
(b)	245	6	2.5	0.074	2
Corbino	**Width [μm]**	**Length [μm]**	**C_{ST} [pF]**	**C_{GSO} [pF]**	**OVL [μm]**
(c)	88	6	0.9	0.09	8
(d)	88	6	0.9	0.18	10
(e)	245	6	2.5	0.15	5
(f)	245	6	2.5	0.42	10

Table 6.1 Geometric parameters of normal a-Si:H TFTs and Corbino a-Si:H TFTs with various storage capacitors and gate-to-source overlaps.

4000Å)/a-Si:H (1700Å)/phosphorous-doped a-Si:H (n^+ a-Si:H, 300Å) tri-layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 ºC to form gate insulator and active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (Mask #2), a chromium (Cr, 1200Å) layer was deposited by sputtering, and source/drain (S/D) electrodes were patterned by wet-etching (Mask #3).

Using S/D metal and photo resist as masks, the back-channel-etching by RIE was performed. Then, we deposited a-SiN_X:H (3000Å) as a passivation layer by PECVD at 300 ºC. To make a contact for the pixel electrode indium tin oxide (ITO), via was formed through the passivation (PVX) layer by RIE (Mask #4). After contact via definition, ITO (500Å) was deposited by a sputtering method at room temperature, and then pixel electrodes were patterned by wet-etching (Mask #5). As a final step, the device thermal annealing was performed for an

hour at 235 ºC; this step is needed to improve ITO optical and electrical properties.

6.3 PIXEL OPRATION, EXPERIMENTAL SET-UP, AND MEASUREMENTS

As previously discussed in chapter 2 and 3, in active-matrix organic light-emitting display (AM-OLED) pixel circuit contains at least two thin-film transistors (TFT) with one storage capacitor (C_{ST}) [8]; when switching TFT (SW TFT) is turned on during the programming state, the data signal voltage is stored at the storage capacitor through the switching TFT. Then, when switching TFT is turned off during the driving state, stored data voltage in CST will generate node voltage (VS) at the gate electrode of driving TFT (DR TFT) that will maintain the constant OLED current flow through driving TFT and the light emission from OLED will occur as expressed in eq. (6.1) and in Figure 6.5.

$$I_{OLED} = \beta(V_S - V_{TH})^2 \text{, where } \beta = C_{OX}\mu_{FE}W_{DR}/2L_{DR} \quad (6\text{-}1)$$

Here C_{OX} is gate insulator capacitance, μ_{FE} is the field-effect mobility, W_{DR} is the channel width, and L_{DR} is channel length of driving TFT, respectively. Since the drain voltage of DR TFT (V_{DD}) is a DC bias high enough to make DR TFT working in the saturation regime, the level and shape of OLED current is determined solely by the gate voltage of DR TFT (V_S) during operation as shown in Fig. 6.5. Therefore, here we fabricated various a-Si:H TFT structures with various storage and overlap capacitors as shown in the blocked area in Fig. 6.5 (a), to see the evolution of gate voltage of DR TFT (V_S) under various dynamic operation conditions. By investigating the variation of V_S, the behavior of I_{OLED} during the dynamic pixel circuit operation can be directly estimated from the eq. (6.1) with the extracted device electrical parameters.

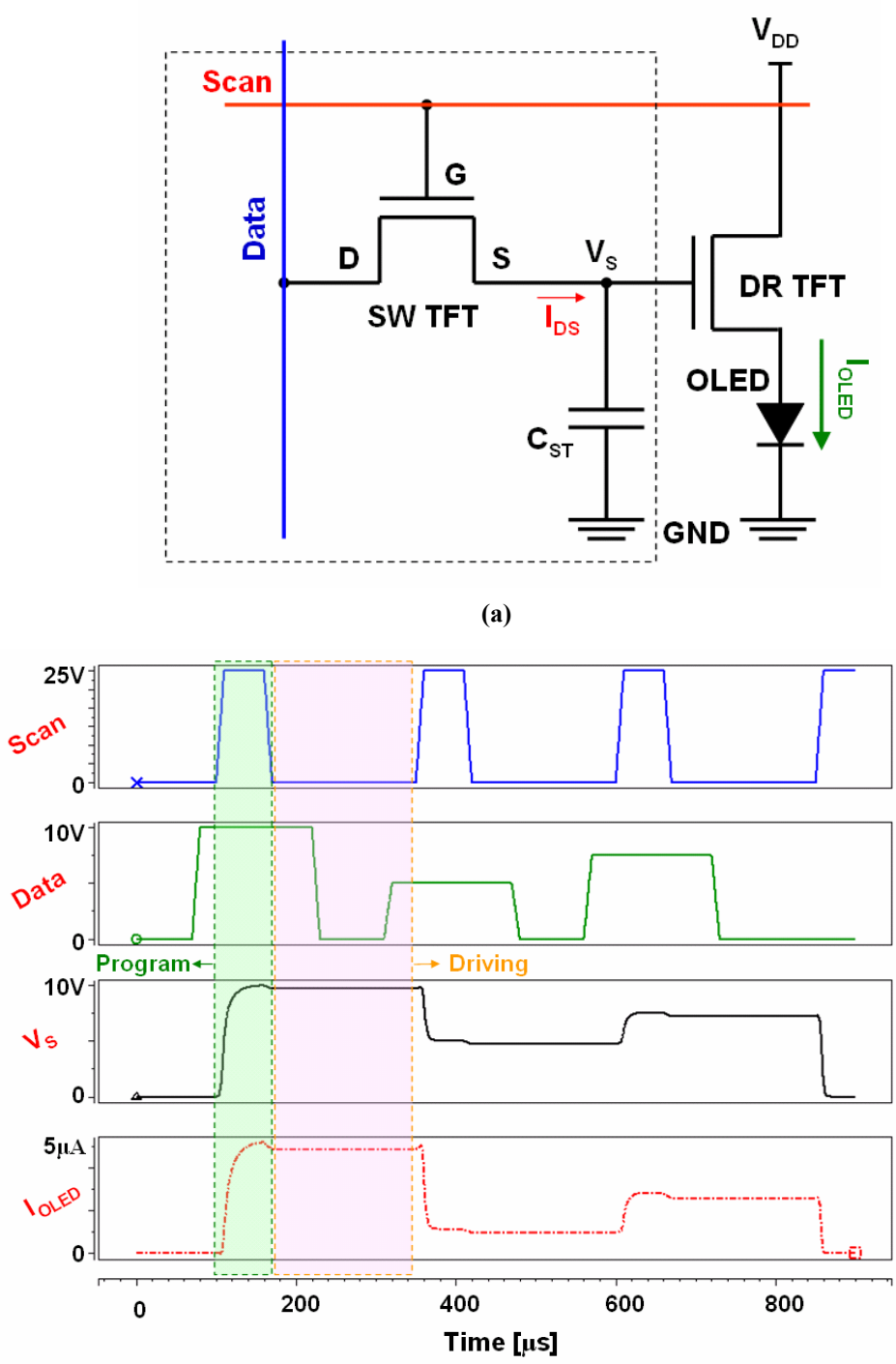


Figure 6.5 (a) Schematic of conventional AM-OLED pixel electrode circuit with two transistors and a storage capacitor [8], and (b) the operational driving signal wave forms simulated by HSPICE during programming and driving states.

Figure 6.6 shows the experimental set-up used for measuring dynamic characteristics of the a-Si:H TFT with a storage capacitor. HP8114A and HP8110A pulse generators are connected to the gate and drain electrodes for applying gate and drain signals, respectively. An active-probe by GGB Industries Inc. (Picoprobe 18B model) is used to measure the voltage variation stored at the storage capacitor by probing source electrode. Since the picoprobe has a very low input capacitance of 0.02 pF and a very high input impedance (input leakage of 10 fA), compared with the designed a-Si:H TFT with a storage capacitor, it has nominally no perturbing effect on the whole circuit. An HP54615B digital oscilloscope with bandwidth of 500 MHz was used to monitor the waveform change during the dynamic operation. A program based on National Instrument Labview virtual instrument commands was used to retrieve the scanned waveform from the oscilloscope. All measurements were done at room temperature.

6.4 EXPERIMENTAL RESULTS

In the dynamic pixel operation, two main properties of transistor are important; the pixel charging performance and feed-through voltage. The charging time of pixel circuit (the time required to charge up the storage capacitor in the pixel electrode circuit to the programmed level) determines the switching speed of switching TFT and programming speed of driving TFT. An insufficient charging of pixel electrode circuit can cause an error either in the OLED brightness or display gray scale resolution as in the active-matrix liquid crystal displays (AM-LCDs) [9]. The importance of TFT charging performance is especially important for high resolution displays, where the available pulse width for the gate signal is relatively short in comparison to the low resolution displays. Therefore, it is necessary for TFTs to have proper electrical characteristics such as high mobility and ON-current that allow to fully charge up the pixel circuits within the

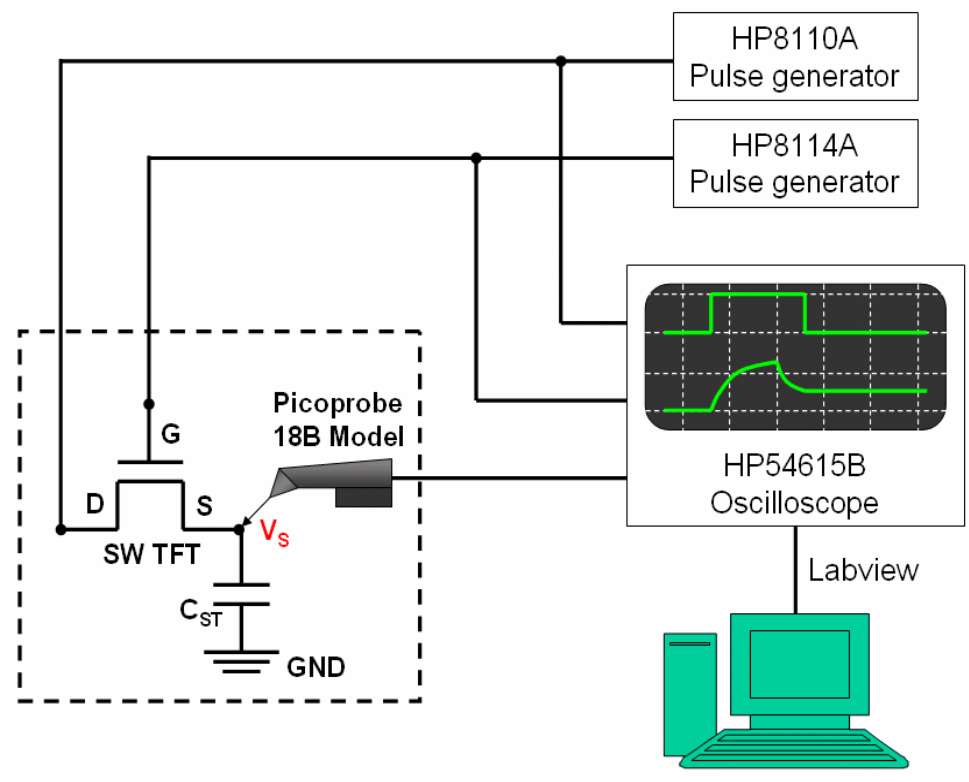


Figure 6.6 Block diagram of the dynamic characteristics measurement set-up.

fixed pulse width or frame time.

The feed-through voltage is another major issue in a-Si:H TFT AM-OLEDs. As mentioned above, during AM-OLED pixel circuit operation, the potential at the gate node of the driving TFT (V_S) is supposed to remain constant and should be maintained at this value by the storage capacitor connected to the gate node during the driving state. This will provide an exact programmed OLED current during pixel driving stage. However, due to the switching TFT dynamic operation, the gate node of driving TFT suffers the potential variation, so-call feed-through voltage due to the parasitic capacitor of switching TFT, Figure 6.5 (b). The presence of the feed-through voltage induces the DC off-set voltage across the driving TFT, and influences the amplitude of OLED current flowing through the driving TFT. This voltage variation can be

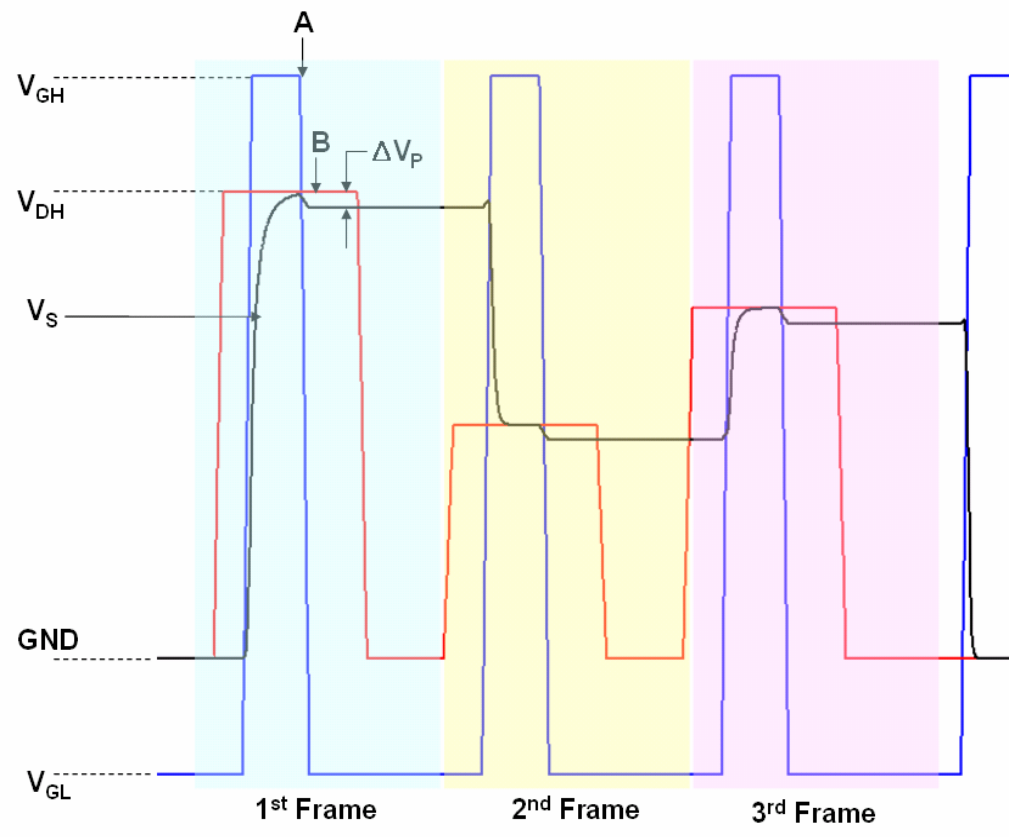


Figure 6.7 Example of signal wave forms used in the dynamic measurement of a-Si:H TFT. A and B represent the time right before and after the falling edge of gate pulse, respectively.

V_{GH}	V_{GL}	V_{DH}	$t_{G\text{-}ON}$	$t_{D\text{-}ON}$
25V	-5V	10V	40 μs	100 μs

Table 6.2 Examples of the driving voltage levels used in the experimental set-up.

estimated in the actual pixel circuit design by considering the geometrical and electrical parameters such as the size of storage capacitor, the size of overlap capacitor between gate and source, and the amplitude of switching TFT gate signal. The detailed discussion on feed-through voltage will be presented in the following section.

Figure 6.7 shows an example of operational wave forms of input signals (VGS and

VDS) and the pixel voltage variation (VS) measured at the storage capacitor, where VGH and VGL are high and low level of gate voltage, respectively, and VDH is the high level of drain voltage. First, the data voltage pulse (Data) is applied to the drain electrode of SW TFT. When the gate voltage pulse is applied to the gate electrode of SW TFT, the SW TFT is turned on and the storage capacitor is charged up to the data voltage during the one frame time. When the gate pulse is removed, the data (or pixel) voltage is stored at the storage capacitor until the next gate and data signals are applied to reset the storage capacitor with a new data voltage for the next time frame. It should be noted that there is voltage drop occurring at the falling edge of gate signal (A). This voltage drop (ΔVP) is caused by the parasitic capacitance of a-Si:H TFT associated with the gate-to-source capacitance (CGS) due to the electrodes overlap, and it will be discussed in detailed in the next section.

Here we focus mainly on influence of the variation of the storage capacitor and signal driving scheme on the charging characteristics of top-gate a-Si:H TFT, while other parameters are kept at the same values; W= 1000 μm and L= 10 μm, and the extracted field-effect mobility and threshold voltage are 0.25 cm2/Vsec and 6.9 V, respectively. Table 6.2 shows the driving voltage levels used in the notation in Figure 6.7. The driving voltage levels were selected for typical AM-OLED driving signals. A gate and drain pulse width are selected as 40 and 100 μs, respectively, to assure sufficient charging time for different experimental conditions. Figure 6.8 shows the pixel voltage (V_S) as a function of charging time for different storage capacitors. As shown in the figure, for fixed TFT geometry and driving signal conditions, the pixel charging time is proportional to the storage capacitance value, while ΔV_P becomes smaller when the C_{ST} becomes larger. We will discuss the ΔV_P behavior in more detail in following section.

In a-Si:H TFT structural design, an important geometrical factor is the gate-to-

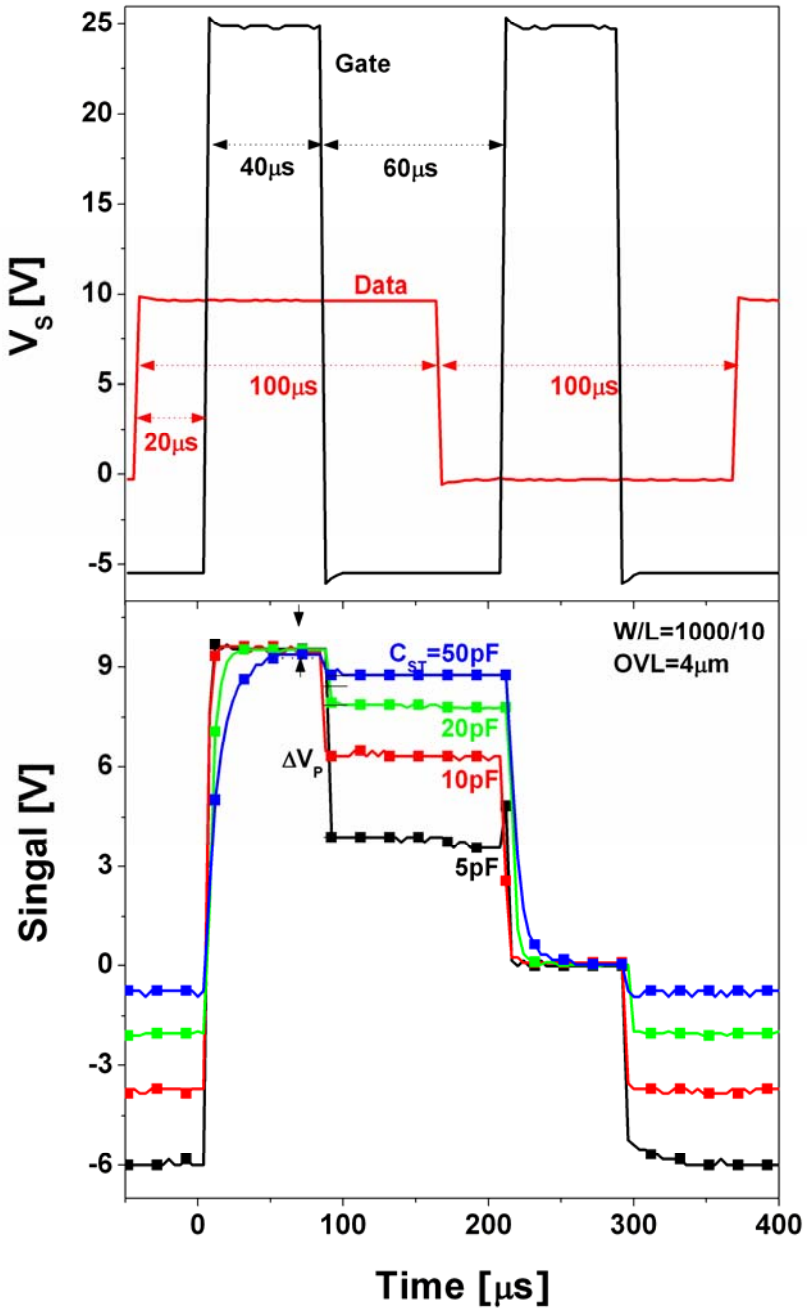


Figure 6.8 Evolution of the measure pixel electrode voltage with the charging time for top-gate a-Si:H TFTs with different storage capacitors and corresponding operational gate and drain signal wave forms.

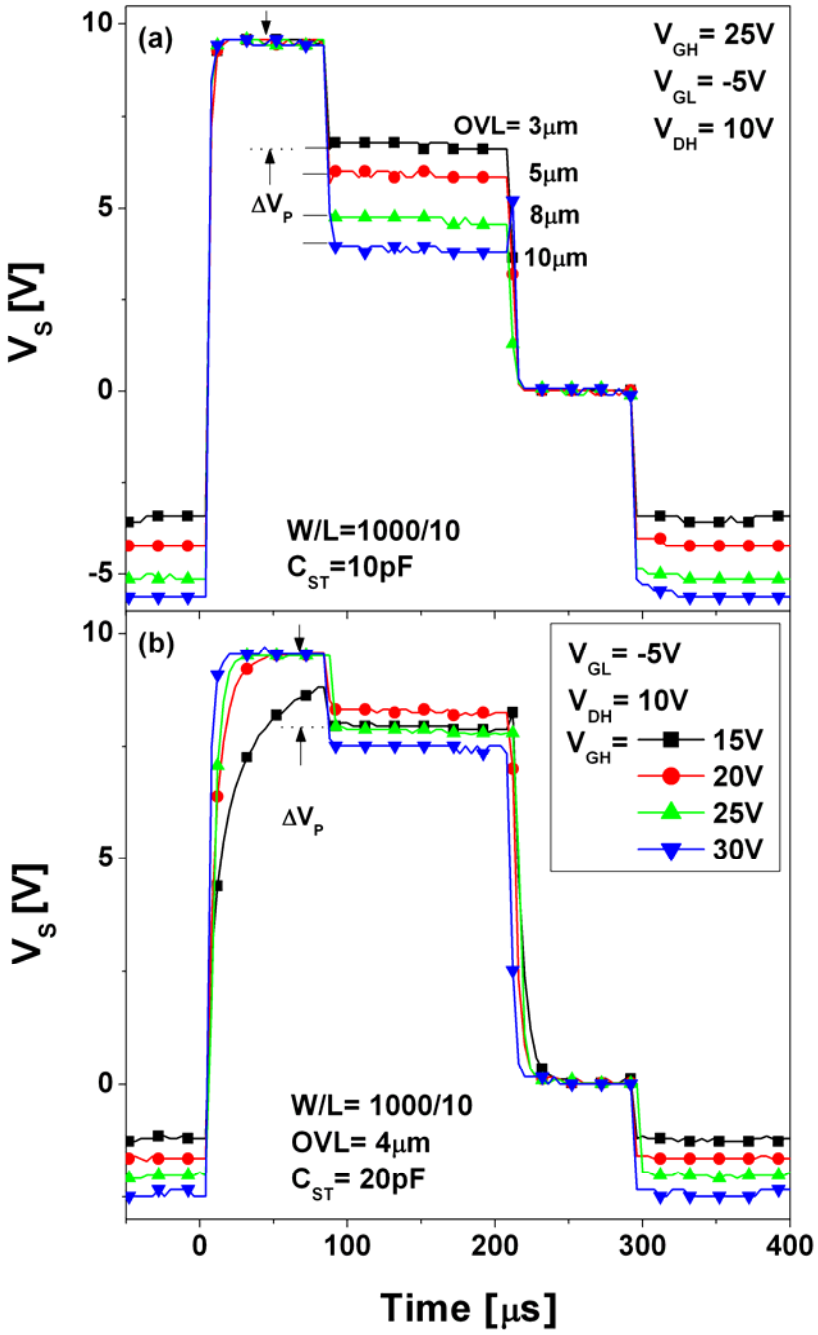


Figure 6.9 Evolution of the measure pixel electrode voltage with the charging time for top-gate a-Si:H TFTs (a) with different gate voltage levels and (b) with different gate-to-source overlaps.

source/drain overlap (OVL). A narrow OVL could induce a current crowding effect at the source/drain contacts which effectively increases the series resistances and reduces the driving capability of a-Si:H TFTs [10, 11]. On the other hand, a large OVL introduces a larger electrode overlap capacitance (parasitic capacitance) which is detrimental to display operation [12]. In addition, a larger OVL occupying a lager pixel area and reduces the overall pixel aperture ratio, which is not desirable especially for high resolution displays. Therefore, it is necessary to optimize the TFT electrode overlap in a-Si:H TFT design. Figure 6.9 (a) shows the pixel charging characteristics of top-gate a-Si:H TFTs with different OVL values of 3, 5, 8, 10 μm for a fixed C_{ST}=10pF. The experimental results indicates that these a-Si:H TFTs have nominally the same switching and driving capabilities while ΔV_P is proportional to OVL values. Figure 6.9 (b) shows the pixel voltage as a function of charging time for different high gate voltages for V_{GL}= -5V. As V_{GH} increases from 20V to 30V, the charging time decreases from 7.2 μs to 2.9 μs.

Base on the experiment and observation above for top-gate a-Si:H TFT with different TFT geometries, we also measured the dynamic response of bottom-gate Corbino a-Si:H TFT. To measure the feed-though voltage of Corbino a-Si:H TFT and normal a-Si:H TFT, the same operational wave forms are used. Figure 6.10 (a) shows the measured pixel voltage for Corbino a-Si:H TFTs with different storage capacitances and overlap capacitances. The overlap capacitance C_{GSO} is calculated from the gate-to-source electrode overlap area and gate insulator capacitance, C_i, which is calculated as 15 nF/cm^2 by considering the dielectric constant (~6.8) and thickness (~4000 Å) of a-SiN_x:H. As shown in the Figure 6.10, as the overlap capacitance increases, the feed-through voltage of Corbino a-Si:H TFT increases for the fixed storage capacitor. At the same time, the larger storage capacitor induces the smaller feed-through voltage of Corbino a-Si:H TFT as in top-gate a-Si:H TFTs described above. Figure 6.10 (b) shows the

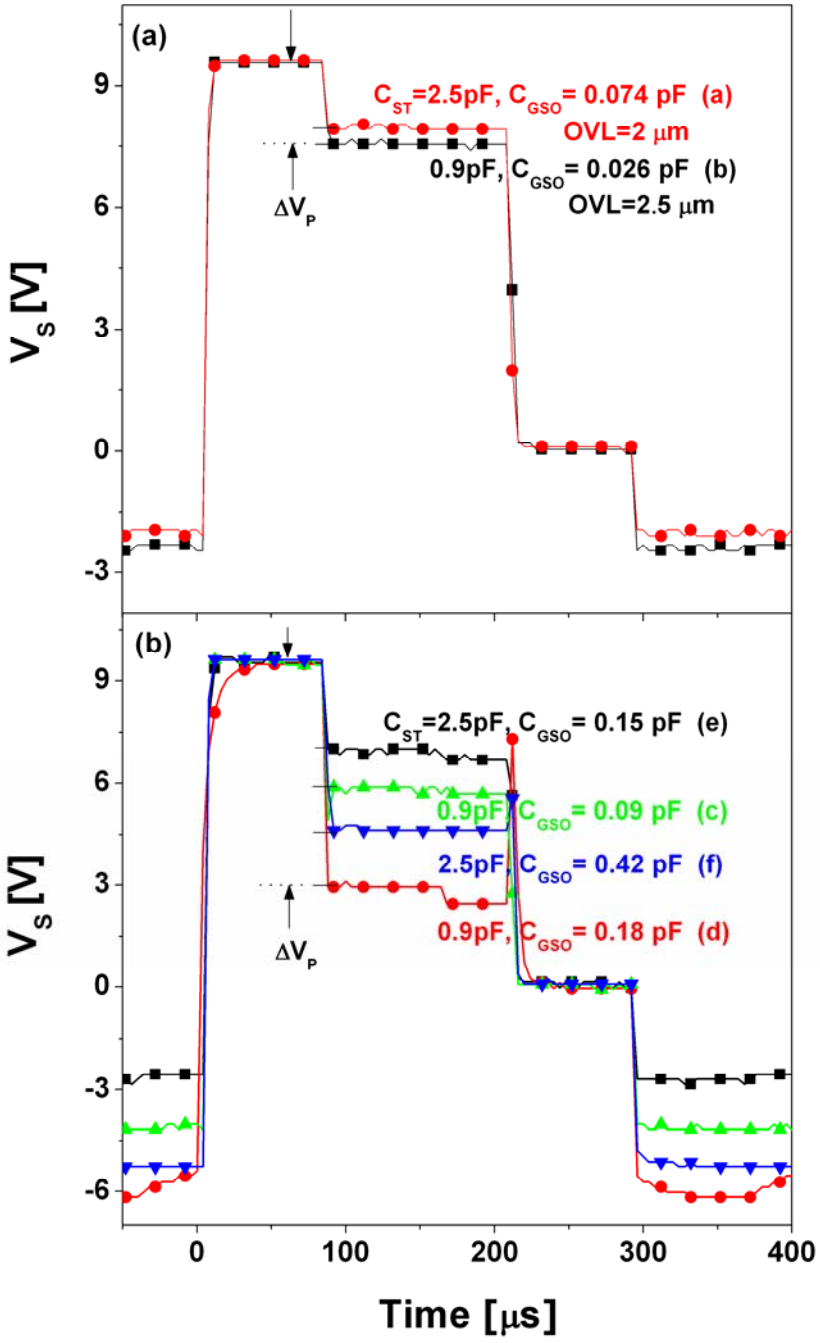


Figure 6.10 The measured pixel electrode voltage for (a) normal and (b) Corbino a-Si:H TFTs with the different storage and overlap capacitance. Detailed device geometry is given in Table 6.1.

pixel voltage variation of rectangular a-Si:H TFT for different storage and overlap capacitors. As shown in the figure, though the overlap capacitance is larger, if the storage capacitor is large enough, the feed-through voltage can decrease. It should noted that all measurements for charging and feed-through voltage characteristics of top- and bottom-gate a-Si:H TFTs used the same operational gate and drain wave forms as shown in Fig. 6.8.

6.5 DISCUSSIONS

6.5.1 Charging Characteristics of the a-Si:H TFTs

From the Figure 6.5 (a), the charging of the storage capacitor can be expressed as

$$C_{ST}\frac{d}{dt}(V_S - GND) = I_{DS} \tag{6.2}$$

where V_S is the gate voltage of DR TFT, GND is the ground, and I_{DS} is the drain current flowing through SW TFT. Assuming a gradual channel approximation, I_{DS} can be described by

$$I_{DS} = \mu_{FE}C_i\frac{W}{L}(V_{GH} - V_S - V_{TH})(V_{DH} - V_S) \tag{6.3}$$

in the linear region where $(V_{DH}\text{-}V_S) < (V_{GH}\text{-}V_S\text{-}V_{TH})$. Here μ_{FE} is the field-effect mobility, C_i is the gate insulator capacitance, W is the channel width, and L is the channel length. From eqs. (6.2) and (6.3), we can define the simplified relationship between Δt and ΔV_S.

$$\Delta t = \frac{C_{ST}\cdot\Delta(V_S - GND)}{I_{DS}} = \frac{C_{ST}\cdot\Delta(V_S - GND)\cdot L}{\mu_{FE}C_iW(V_{GH} - V_S - V_{TH})(V_{DH} - V_S)} \tag{6.4}$$

where $dt \approx \Delta t$ and $d(V_S\text{-}GND) \approx \Delta(V_S\text{-}GND)$ for small variations. If we define the charging time

as the time required to charge the storage capacitor up to 90% of the drain signal level, the charging time t_{CH} can be expressed by

$$t_{CH} = 0.9 \times \Delta t = \frac{0.9 C_{ST} \cdot \Delta(V_s - GND) \cdot L}{\mu_{FE} C_i W (V_{GH} - V_S - V_{TH})(V_{DH} - V_S)} \tag{6.5}$$

Equation (6.5) indicates that the pixel charging characteristics can be determined by the following factors: the storage capacitance (C_{ST}), the TFT geometries (W, L, and C_i), the TFT electrical characteristics (μ_{FE} and V_{TH}), and the signal driving scheme (V_{GH} and V_{DH}). Therefore, for a fixed pixel design and signal driving scheme, the charging characteristics depend on the a-Si:H TFT electrical characteristics; a longer charging time will result for TFTs with a higher threshold voltage at given μ_{FE} and a lower field-effect mobility at a given V_{TH}.

Figure 6.11 shows the charging time variation for different storage capacitor values extracted from Fig. 6.8. We can conclude that the pixel electrode will be charged up much faster when the storage capacitor value is reduced to its minimum acceptable level. We fitted variation of the t_{CH} with C_{ST} using eq. (6.5) shown as the solid line in Fig. 6.11, which shows acceptable agreement with the measured data. Parameters used for this fitting are described in the figure. However, to get precise pixel charging characteristics of the AM-OLED, a more complete modeling will be required for both a-Si:H TFTs and OLED, since the voltage dependence of the OLED was not taken into consideration in the above calculation.

Figure 6.11 also shows the charging time (t_{CH}) variation for different gate voltage values (V_{GH}) and the fitted variation of the t_{CH} with V_{GH} using eq. (6.5) as the solid line. As shown in the figure, it should be noted that when the gate voltage is not high enough (=15V), the charging time becomes very long so that pixel electrode can not be charged up quickly to the programmed voltage value (=10V), which deteriorates the display gray scale. Therefore, in pixel electrode

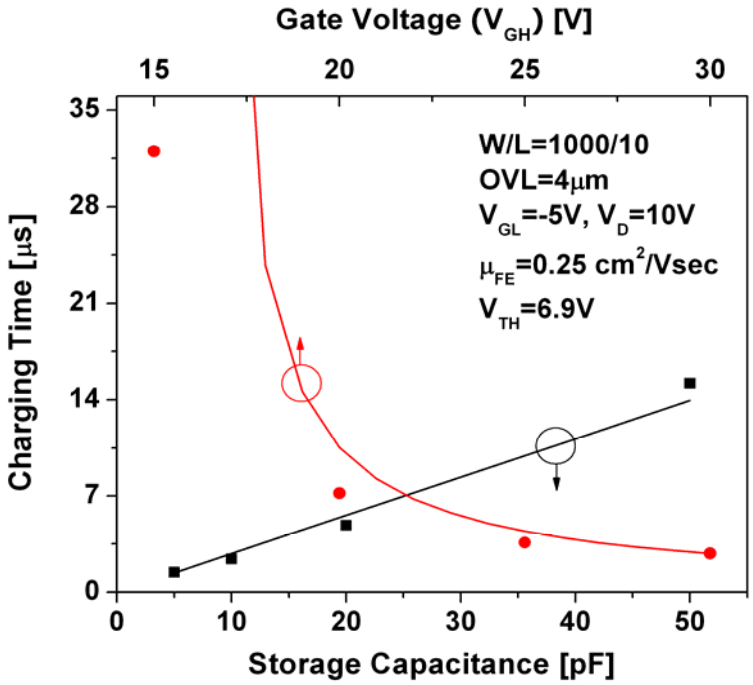


Figure 6.11 Variation of charging time as a function of storage capacitor (C_{ST}) and gate voltage (V_{GH}) for top-gate a-Si:H TFT. The symbols are measured data and solid line is calculated data.

operation, the gate voltage should be set high enough to minimize the charging time to reach the programmed value. However, at the same time, high gate voltage induces high power consumption and large pixel voltage variation (ΔV_P) when the gate voltage of TFT is turned off. Therefore, optimum gate voltage value should be considered in AM-OLED pixel electrode design for a given resolution. It should be noted that the fitted curve in Fig. 6.11 shows acceptable agreement with the measured data for the gate voltage range from 25V to 30V. However, as the gate voltage decreases below 25V, the operation of transistor starts to move from linear to cut-off regime. As a result, the eq. (6.5) becomes invalid and shows the deviations from the measured values.

6.5.2 Feed-Though Voltage of the a-Si:H TFTs

The feed-through voltage (ΔV_P) is the voltage drop of gate node (V_S) of driving TFT during the switching off of the gate signal of switching TFT, Figure 6.7. This voltage drop is mainly due to the existence of SW TFT gate-to-source parasitic capacitance (C_{GS}) which causes the charge redistribution when the SW TFT is turned off by the gate signal. Figure 6.7 shows the schematics of a-Si:H TFT with storage capacitor. In this circuit, the feed-through voltage ΔV_P can be expressed by simple equation:

$$\Delta V_P = \frac{C_{GS}}{C_{GS} + C_{ST}} \Delta V_{SCAN} \quad \text{where} \quad \Delta V_{SCAN} = V_{GH} - V_{GL} \tag{6.6}$$

It should be noted that parasitic capacitors of DR TFT do not have influence on the feed-through voltage or gate potential of DR TFT since they are connected to constant DC bias components (V_{DD} and GND).

The derivation of eq. (6.6) is based on the assumption that C_{GS} is independent of gate bias. However, in reality, C_{GS} is a metal-insulator-semiconductor (MIS) capacitor, which is known to be gate-voltage dependant. Therefore, to obtain the accurate feed-through voltage for a-Si:H TFT, the gate voltage dependence of C_{GS} should be taken into consideration. Figure 6.1 shows the cross-section of top-gate a-Si:H TFT with gate-to-source/drain overlaps (OVL). From Fig. 6.1, the total gate-to-source capacitance, C_{GS} can be approximately divided into the gate-to-source overlap capacitance, C_{GSO}, and the gate-to-source MIS intrinsic capacitance, C_{GSI}:

$$C_{GS}=C_{GSO} + C_{GSI} \tag{6.7}$$

The equivalent circuit for the TFT parasitic capacitances is shown in Figure 6.12, and the overlap capacitance can be expressed as

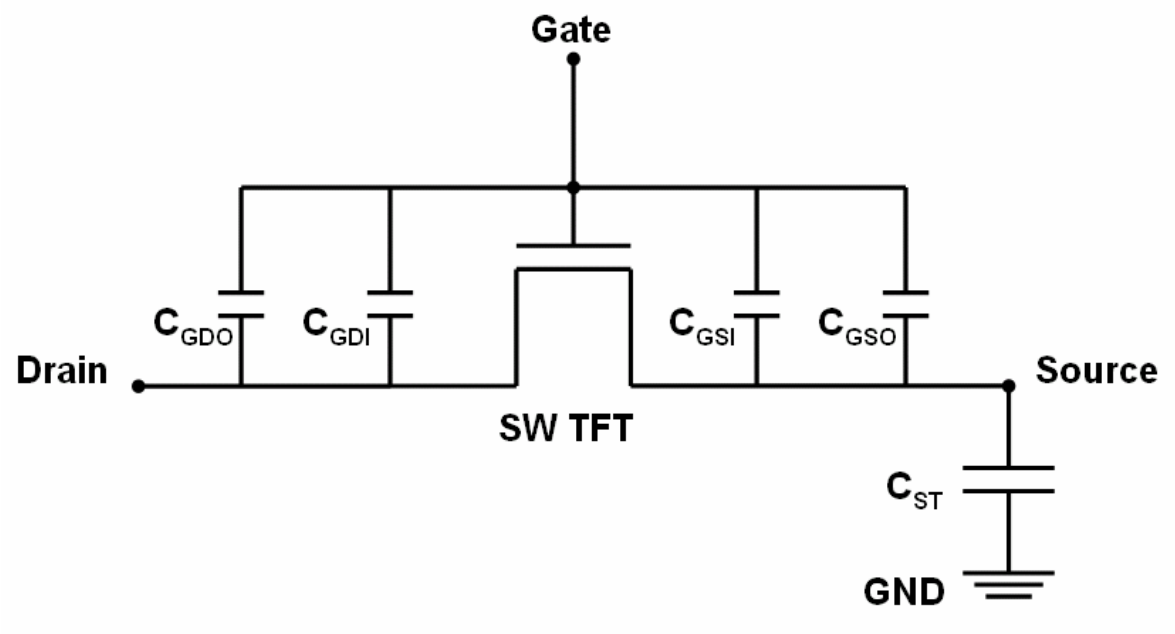


Figure 6.12 The equivalent circuit of a-Si:H TFT with the gate-to-source/drain parasitic capacitances.

$$C_{GSO} = W \cdot OVL \cdot \frac{C_i C_{Si}}{C_i + C_{Si}} \tag{6.8}$$

where W is the TFT channel width, C_i is the gate insulator capacitance, and C_{Si} is the a-Si:H capacitance. For a-Si:H TFTs with thin a-Si:H layer (~300Å), equation can be approximated by

$$C_{GSO} \cong W \cdot OVL \cdot C_i \tag{6.9}$$

Since a-Si:H has a higher dielectric constant (~11) than amorphous silicon nitride (~6.8), and the thickness of amorphous silicon nitride (~3300Å) is much thicker than a-Si:H, this approximation is close to the exact value; the values for C_i and C_{Si} are about 18 and 187 nF/cm^2, respectively. On the other hand, when TFT is in the OFF-state, the a-Si:H layer behaves as an insulator and there is no intrinsic parasitic capacitance,

$$C_{GSI} = 0, \text{ for } V_G - V_S < V_T \tag{6.10}$$

From the above analysis, we can express C_{GS} for the ON- and OFF-states as,

$$C_{GS-ON} = C_{GSO} + C_{GSI} = W \cdot OVL \cdot \frac{C_i C_{Si}}{C_i + C_{Si}} + C_{GSI}, \text{ for } V_G\text{-}V_S > V_T \tag{6.11}$$

$$C_{GS-OFF} = C_{GSO} = W \cdot OVL \cdot \frac{C_i C_{Si}}{C_i + C_{Si}}, \text{ for } V_G\text{-}V_S < V_T \tag{6.12}$$

To derive a more accurate expression of the feed-though voltage, we can use the wave forms shown in Figure 6.7, and the ON- and OFF-state gate-to-source capacitance. The charge stored at the source electrode right before (A) and after (B) the falling edge of gate pulse can be expressed, respectively, as,

$$Q_A = C_{GS-ON}(V_{DH} - V_{GH}) + C_{ST}(V_{DH} - GND) \tag{6.13}$$

$$Q_B = C_{GS-OFF}(V_S - V_{GL}) + C_{ST}(V_S - GND)$$

According to charge conservation, since Q_A=Q_B, we have then,

$$C_{GS-ON} \cdot V_{DH} - C_{GS-ON} \cdot V_{GH} + C_{ST} \cdot V_{DH} - C_{ST} \cdot GND$$

$$= C_{GS-OFF} V_S - C_{GS-OFF} \cdot V_{GL} + C_{ST} \cdot V_S - C_{ST} \cdot GND \tag{6.14}$$

If we add $C_{GS-OFF} \cdot V_{DH}$ term on both sides and organize the equation,

$$(C_{GS-OFF} - C_{ST})(V_{DH} - V_S) = C_{GS-OFF}(V_{GH} - V_{GL}) + (C_{GS-ON} - C_{GS-OFF})(V_{GH} - V_{DH})$$

$$\therefore \Delta V_P = \frac{C_{GS-OFF}}{C_{GS-OFF} + C_{ST}} \Delta V_G + \frac{C_{GS-ON} - C_{GS-OFF}}{C_{GS-OFF} + C_{ST}} (V_{GH} - V_{DH}) \tag{6.15}$$

If we assume m=$C_{GS\text{-}ON}$/$C_{GS\text{-}OFF}$, the equation becomes,

$$\therefore \Delta V_P = \frac{C_{GS-OFF}}{C_{GS-OFF} + C_{ST}} \left[\Delta V_G + (m-1)(V_{GH} - V_{DH})\right] \tag{6.16}$$

Equation (6.16) will be used to verify the experimental data obtained for the staggered a-Si:H

TFTs. It should noted that if $C_{GS\text{-}ON} = C_{GS\text{-}OFF}$, equation is reduced to eq. (6.6).

Figure 6.9 shows the measured pixel voltage for top-gate a-Si:H TFTs with different gate-to-source overlaps. The figure clearly shows that the feed-though voltage increases with increasing gate-to-source overlap widths, and it indicates that an optimum overlap need be defined to minimize the feed-through voltage. However, at the same time, OVL should not degrade the a-Si:H TFT pixel charging performance. The pixel electrode voltage variation for different gate voltage levels is also shown in Figure 6.9. As the gate voltage increases from 15V to 30V, the feed-through voltage becomes larger from 0.9V to 2.2V as predicted by eq. (6.16). Therefore, the optimization of the driving signal should be done based on the consideration of the feed-through voltage effect on display operating performance.

Figure 6.8 shows the measured pixel voltage for a-Si:H TFTs with different storage capacitances. All a-Si:H TFTs have channel width of 1000μm, channel length of 10μm, and a gate-to-source/drain overlap of 4 μm. As shown in the figure, the feed-through voltage increases with the decreasing storage capacitance value.

Figure 6.13 shows the variation of feed-through voltage as a function of ratio of C_{GSO} / (C_{ST} + C_{GSO}). Considering the dielectric constant (~6.8) and thickness (~3300 Å) of a-SiN_x:H, the OFF-state gate-to-source capacitance $C_{GS\text{-}OFF} = C_{GSO}$ = 0.73 pF for the top-gate a-Si:H TFT. By fitting the experimental data (Figure 6.13) with eq. (6.15), we obtained the fitting parameter m = 2.5. It indicates that the ON-state total gate-to-source capacitance $C_{GS\text{-}ON}$= m × $C_{GS\text{-}OFF}$ = 2.5 × $C_{GS\text{-}OFF}$. As in eq. (6.11), since $C_{GS\text{-}ON}$ consists of the gate-source overlap capacitance and intrinsic gate-to-source MIS capacitance, the C_{GSI} for ON-state is about 1.5 × C_{GSO}, which is about half of the total channel intrinsic capacitance, W × L × C_i (≈ 1.8 pF). This result suggests that, for the top-gate a-Si;H TFTs, the ON-state gate-to-drain MIS intrinsic capacitance (C_{GDI}) is

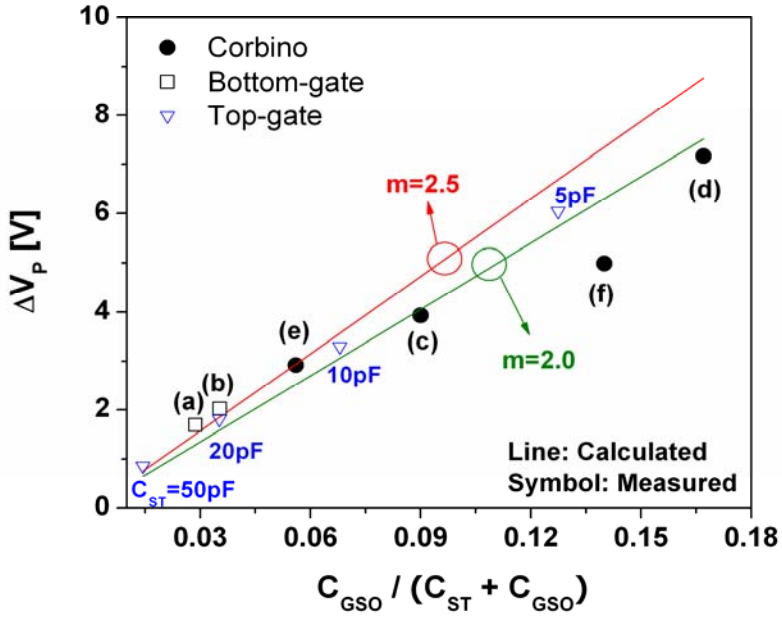


Figure 6.13 Feed-though voltage (ΔV_P) variation for Corbino a-Si:H TFT as a function of ratio of C_{GSO} / (C_{ST} + C_{GSO}) where close symbols are measured values for Corbino a-Si:H TFTs, and open symbols are for rectangular top- and bottom-gate a-Si:H TFTs. The solid lines are calculated values using eq. (6.16) with the fitting parameter m=2.5 and 2.0. Alphabet symbols stand for different Corbino [(a) to (d)] and rectangular bottom-gate a-Si:H TFTs [(e) to (f)] which are summarized in Table 6.2.

also about half of the total channel intrinsic capacitance. This result for top-gate a-Si:H TFT shows a good agreement with the intrinsic capacitance model reported for crystalline MOSFETs, which predicts that when an MOSFET is in linear ON-state, the gate-to-source/drain capacitance is about half of the total channel capacitance [13]. Figure 6.13 also shows the variation of measured feed-through voltage of rectangular top- and bottom-gate a-Si:H TFTs and Corbino a-Si:H TFTs as a function of the ratio of C_{GSO} / (C_{GSO} + C_{ST}). From eq. (6.16), the variation of feed-through voltage for different Corbino a-Si:H TFTs with different storage capacitor values was calculated based on the geometries and operational wave forms. As shown in figure, the

calculated feed-through voltages of rectangular a-Si:H TFT using eq. (6.16) show good agreement with the measured values. This means that eq. (6.16) is valid for both top-gate and bottom-gate a-Si:H TFT structures. However, different from rectangular a-Si:H TFTs, the calculated values for Corbino a-Si:H TFT shows some deviation from the measured values. This deviation can be associated with the unique form of Corbino a-Si:H TFT geometry. Considering fitting parameter $m=C_{GS\text{-}ON}/C_{GS\text{-}OFF}$, due to the large overlap between gate and source electrodes in Corbino a-Si:H TFTs comparing with the normal rectangular a-Si:H TFTs (Table 6.1), the increase in $C_{GS\text{-}OFF}$ (= C_{GSO}) causes the decrease in the fitting parameter, m. Consequently, when we change fitting parameter for Corbino a-Si:H TFT from 2.5 to 2.0 in eq. (6.16), the corrected values show a good agreement with the measured feed-through voltage values. However, it is observed that there is still a small deviation at high C_{GSO} / (C_{GSO} + C_{ST}) ratio, Therefore, more thorough study is needed for Corbino a-Si:H TFT with the different TFT geometries to find out proper fitting parameter m in eq. (6.16) to predict the feed-through voltage variation which is critical in programming the gate voltage for driving TFT to express a large range of gray-scale levels in AM-OLED. Especially for the a-Si:H TFTs with asymmetric shape of electrodes, eq. (6.16) with the modified fitting parameter will be a good approximation to estimate the feed-though voltage variation for designing the operational wave forms and the pixel electrode circuits for AM-OLEDs.

6.6 INFLUENCE OF CORBINO A-SI:H TFTS ON OLED CURRENT

As we described above, the dynamic characteristics (charging performance and feed-through voltage variations) of a-Si:H TFT are closely related to the capacitive elements (the overlapped capacitor and the storage capacitor) and operational signals in the pixel electrode

circuit. In general, as the display resolution of AM-OLED becomes higher, since the pixel area becomes smaller, the size of storage capacitor is pre-determined to be as small as possible to achieve highest possible pixel aperture ratio. The overlapped capacitance is usually predetermined by the TFT processing design rules, and can be hardly changed for a standard rectangular a-Si:H TFT. Operational signal waves are also predetermined depending on the pixel driving circuitry to minimize power consumption for a given AM-OLED gray scale range. Therefore, for a given AM-OLED pixel circuit with standard rectangular a-Si:H TFTs, all these parameters are fixed to designed values, and cannot be changed to reduce the charging time or feed-though voltage.

However, as the AM-OLED pixel circuit becomes complicated with the compensation functions [14, 15], the control of feed-though voltage becomes more necessary since it directly impacts on the OLED current levels during driving state in AM-OLED operation. From Figure 6.1, the OLED current during programming state can be expressed by eq. (6.1). If we assume the feed-through voltage given by eq. (6-16), the OLED current during driving state (after switching TFT is turned off) is expressed as,

$$I_{OLED} = \beta(V_S - V_{TH} - \Delta V_p)^2$$

$$= \beta(V_S - V_{TH} - \frac{C_{GSO}}{C_{GSO} + C_{ST}}\left[\Delta V_G + (m-1)(V_{GH} - V_{DH})\right])^2 \qquad (6\text{-}17)$$

Therefore, for a given pixel circuit design and operational conditions, the variation of OLED current between programming and driving states can be suppressed by minimizing the overlap capacitance of switching TFT, which results in minimized feed-through voltage. Due to an unique geometry of Corbino a-Si:H TFT, the size of source electrode can be minimized in comparison to the drain electrode while the channel width is maintained to designed value.

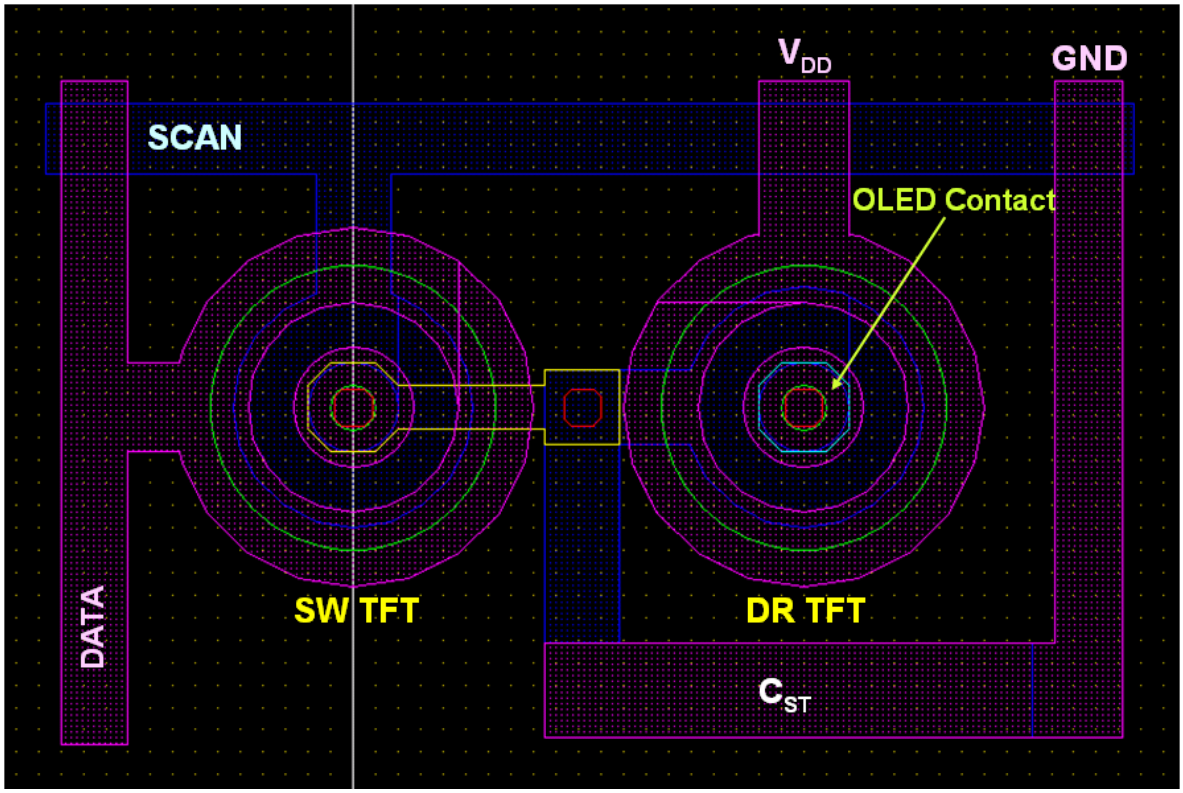


Figure 6.14 The schematic layout of pixel electrode circuit in Fig. 6.5 (a) with Corbino a-Si:H as switching and driving TFTs.

Therefore, the overlapped area between source and gate electrodes is minimized resulting in minimized overlapped gate-to-source capacitance, C_{GSO} in comparison to rectangular TFT with the same channel width. Hence, a relatively much smaller feed-through voltage is expected be achieved for Corbino a-Si:H TFT [5] if used as a switching TFT in AM-OLEDs, Figure 6.14. It should be noted that in AM-OLED operation, the polarity of data signal voltage (gate node of DR TFT) is always positive to make sure the OLED current flowing all the time. Therefore, positions of the drain and source of Corbino TFT are always fixed so that the unique asymmetric geometry does not affect on the OFF-current behavior of Corbino a-Si:H TFT, which would be influenced by line- or dot-inversion method resulting in MURA defect in AM-LCD [16]. In addition, in Corbino a-Si:H TFT, the C_{GSO} can be reduced further by patterning the gate electrode. As shown

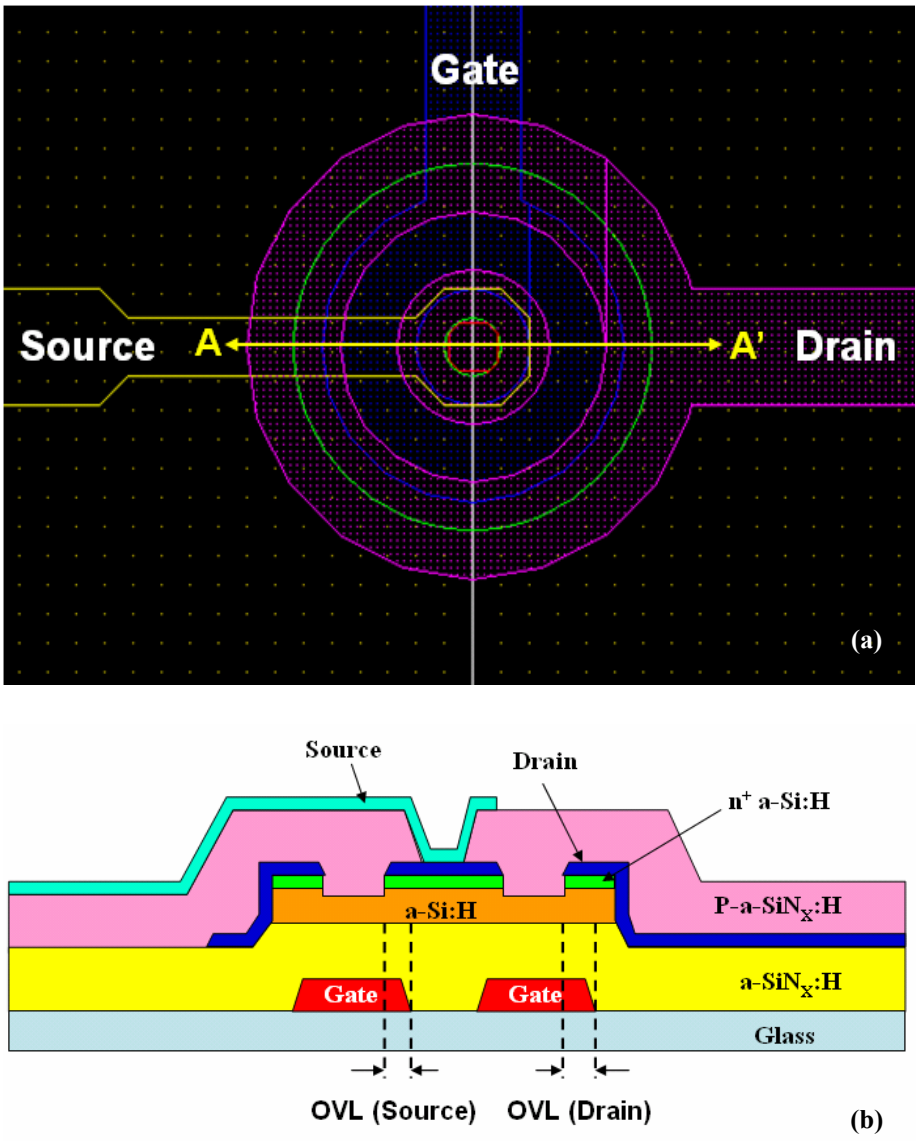


Figure 6.15 The schematics of (a) top-view and (b) cross-section view of Corbino a-Si:H with patterned gate electrode.

in Figure 6.15, the gate electrode can be patterned to minimize the overlapped area with source electrode, which can reduce further the feed-though voltage for a given AM-OLED pixel circuit design. Therefore, by using Corbino a-Si:H TFT in AM-OLEDs, we can expect a better control in OLED current gray scale levels as well as better displays electrical stabilities [5].

6.7 CONCLUSION

In this chapter, the dynamic characteristics of various a-Si:H TFTs are experimentally discussed. The experimental results indicate that the charging performance of a-Si:H TFT depends on the size of storage capacitor connected to the source of TFT and gate voltage level while it is independent of the overlap capacitance. We have also measured that the feed-though voltage characteristics for various top- and bottom-gate a-Si:H TFTs with different TFT geometries. The feed through voltage is shown to be closely related to the value of storage capacitance, overlap capacitance, and operational wave forms. Analytical expressions are also derived to compare the calculated data with the experimental results, and a good agreement between the experimental and calculated results was obtained, for all studied a-Si:H TFTs. Due to the unique geometry, Corbino a-Si:H TFT requires a modification in the fitting parameter of the analytical expression. We believe that derived analytical expressions are very useful tool in the design of the pixel electrode circuits and operational signals for AM-OLEDs. By using Corbino a-Si:H TFT as a switching TFT in AM-OLED pixel circuit, we can expect the feed-through voltage variation can be minimized to maintain the programmed the OLED current.

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CHAPTER 7

Conclusions and Future Work

7.1 Conclusions

In this study, a novel a-Si:H TFT current-driven pixel electrodes for AM-OLED have been demonstrated and their electrical performance have been evaluated. A five photo-mask back-channel etched a-Si:H TFT pixel electrode circuit fabrication technology were developed on the Corning 1737 glass substrate. For the dynamic measurement of different pixel electrode circuits, the different driving schemes have been devised and designed to be used for different pixel electrode circuits for AM-OLEDs. By programming the signal pulse (V_{SCAN}, V_{CTRL}, and I_{DATA}), the OLED current from fabricated different pixel electrode circuits has been measured in time scale as a function of input data current. The effect of different cascade capacitor ratio on the OLED current and scaling-ratio was also investigated during the pixel circuit dynamic measurements.

To address the inherent electrical stability issue of a-Si:H TFT, two novel a-Si:H TFT structures were presented: Corbino and Hexagonal TFTs. It was shown that both a-Si:H Corbino and Hexagonal TFTs have the asymmetric electrical characteristics under different drain bias conditions. To extract the electrical device parameters, asymmetric geometric factors were developed for different drain bias conditions. Current-voltage measurements indicate that the ON-OFF current ratio of the Corbino and Hexagonal TFTs can be enhanced significantly by

choosing the outer electrode as the drain while the field-effect mobility and threshold voltage have the identical values when different drain bias conditions are used. By using multiple Hexagonal TFTs, the output current of the Hexagonal a-Si:H TFT connected in parallel increases linearly with their number within a given pixel circuit. Current-voltage measurements indicate that a high ON-OFF current ratio and a low sub-threshold slope can be maintained for multiple Hexagonal TFTs connected in parallel while the field-effect mobility and threshold voltage remain identical to a single HEX a-Si:H TFT. Due to a unique device geometry, enhanced electrical stability and larger pixel aperture ratio can be achieved in the multiple a-Si:H HEX-TFTs in comparison to standard single a-Si:H TFTs having same channel width.

To evaluate the dynamic response of the a-Si:H TFT pixel electrode circuits and devices, the dynamic measurement setup was developed. The dynamic responses of different a-Si:H TFT structures with the various storage capacitor size were explored for AM-OLEDs. The effect of various storage capacitors and overlap capacitors of TFT on the charging time and feed-through voltage characteristics of the a-Si:H switching TFT were explored. Feed-through voltage behavior of the Corbino a-Si:H TFT also was discussed in comparison to the normal rectangular a-Si:H TFT as a switching TFT for AM-OLEDs. By using Corbino a-Si:H TFT as a switching TFT in AM-OLED pixel circuit, we can expect the feed-through voltage variation to be minimized to maintain the programmed OLED current.

Since, in this work, novel a-Si:H TFT structures with enhanced electrical stabilities and higher ON-OFF ratios were demonstrated for the first time, I believe that this dissertation will have a tremendous impact on the academic and industrial researches in the area of the a-Si:H TFT based AM-OLED. The results presented provide the impetus to expedite development of large area and high resolution AM-OLEDs based on a-Si:H TFT technology.

7.2 Recommendation for Future Work

Although novel a-Si:H TFT structures and pixel electrode circuit for AM-OLED were successfully demonstrated in this thesis, there are still many aspects of the AM-OLED that can be improved.

Novel a-Si:H TFT fabrication of the pixel circuit: Further optimized design and fabrication method of novel a-Si:H TFT pixel electrode circuits are needed to evaluate a high performance a-Si:H TFT characteristics and corresponding pixel electrode circuits. If novel a-Si:H TFTs show better performance in comparison to normal TFT structures, a high driving current can be obtained at lower select and supply voltage. The low operation voltage will reduce the display power consumption and a-Si:H TFT parameter variation during the display operation. At the same time, much better electrical and thermal stability of pixel electrode circuits can be achieved, which is very critical for high resolution and large size a-Si:H based AM-OLEDs.

Pixel circuit implementation in AM-OLED: Optimized design and fabrication of the active-matrix arrays with a novel a-Si:H TFT pixel electrode circuit is needed to evaluate high performance pixel electrode circuits. To improve the display aperture ratio, a top-emission pixel configuration should be used since several TFTs per pixel are needed for current-driven compensating AM pixels. A semi-transparent top-cathode OLED structure can be combined with the developed 4-a-Si:H TFTs pixel electrode circuits to produce top-emission AM-OLED. A transparent top-anode OLED structure is also required for developed current-mirror based current-driven pixel electrode circuit to produce top-emission AM-OLED. Therefore, for the top-emission pixel configuration, an appropriate OLED fabrication process

needs to be first developed for both new top-cathode and top-anode OLEDs.

APPENDIX

List of Publications

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[1] **H. Lee**, C. S. Chiang, and J. Kanicki, "Dynamic Measurement of a-Si:H TFT for AM-OLED Displays," *IEEE Trans. on Electron Devices*, submitted.

[2] **H. Lee**, J. S. Yoo, C- D. Kim, I- J. Chung, and J. Kanicki, "Hexagonal a-Si:H TFTs, a New Advanced Technology for Flat Panel Displays," *IEEE Trans. on Electron Devices*, vol. 55, no. 1, 2008.

[3] **H. Lee**, Y. C. Lin, H-. P-. Shieh, and J. Kanicki, "Current-Scaling a-Si:H TFT Pixel Electrode Circuit for AM-OLEDs: Electrical Properties and Stability," *IEEE Trans. on Electron Devices*, vol. 54, no. 9, pp. 2403-2410, 2007.

[4] J. S. Yoo, **H. Lee**, J. Kanicki, C- D. Kim and I- J. Chung, "Novel a-Si:H TFT Pixel Electrode Circuit for Electrically Stable Top-Anode Light-Emitting AMOLEDs," *J. Soc. Inf. Display*, vol. 15, no. 8, pp. 545-551, 2007.

[5] **H. Lee**, J. S. Yoo, C- D. Kim, I- J. Chung, and J. Kanicki, "Asymmetric Electrical Properties of Corbino a-Si:H TFTs and Concepts of Their Applications to Flat Panel Displays," *IEEE Trans. on Electron Devices*, vol. 54, no. 4, pp. 654-662, 2007.

[6] **H. Lee**, J. S. Yoo, C- D. Kim, I- J. Chung, and J. Kanicki, "Novel Current-Scaling

Current-Mirror a-Si:H TFT Pixel Electrode Circuit with Cascade Capacitor for AM-OLEDs," *Journal of Jpn. Appl. Phys.*, vol. 46, no. 3B, pp. 1343-1349, 2007.

[7] **H. Lee**, A. R. Johnson, and J. Kanicki, "White LED Based on Poly-fluorene Co-Polymers Blend on Plastic Substrate," *IEEE Trans. on Electron Devices*, vol. 53, no. 3, pp. 427-434, 2006.