LOW TEMPERATURE WAFER LEVEL VACUUM PACKAGING USING AU-SI EUTECTIC BONDING AND LOCALIZED HEATING

by

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To Mom, Dad and Grandma.

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ABSTRACT

LOW TEMPERATURE WAFER LEVEL VACUUM PACKAGING USING AU-SI EUTECTIC BONDING AND LOCALIZED HEATING

by

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An Au-Si eutectic wafer-level bonding process and a localized heating process, called differential backside heating, were developed for low-temperature vacuum packaging of MEMS devices.

Using Au-Si eutectic bonding, devices were encapsulated by bonding a silicon cap wafer to a device wafer. Au-Si eutectic bond rings melt at over 363 ºC allowing them to conform over topology such as electrical feed-throughs allowing for a vacuum seal. Detailed specifications are given for achieving uniform/strong bonds to poly-Si and Au bond rings in a bond recipe which includes vacuum pumping, an outgassing step, application of the bond pressure (~2.5 MPa), and heating to 390 °C. Micromachined poly-Si Pirani vacuum sensors were developed, characterized and then packaged in the Au-Si eutectic bonding process in order to measuring vacuum pressures. These packages had cavity dimensions of 2.3×2.3 mm wide with a depth of 90 µm. Yields of 84.6% and

94.1% were achieved in packages with bond ring widths of 100 and 150 µm. With the use of getters and a pre-bond outgassing step, pressures from <3.7 to 23.3 mTorr were achieved. Furthermore, pressures were shown to remain stable to within ±5 mTorr for over 3 years of testing, after 100 hours at 150ºC, and after 50 thermal cycles from -50ºC to 150ºC.

Using differential localized heating, one of the two wafers to be bonded is heated from the backside, and the other is cooled from the backside, so that heat flows through the bond regions while the device regions stay relatively cool. A bonder test setup was built where integrated temperature sensors on the device wafer were used to measure the temperature at different distances from the bond region during Si to glass and Si to Si bond experiments. This technique was proven successful with temperature of 23% and 41% of the bond ring temperature at 250 and 650 µm from the bond rings for bonds to glass and Si respectively. These temperature rises were within 3% and 9% of those predicted by 3-D FEM thermal modeling. In the Si to glass bond, bond rings were heated to 400ºC allowing for a Au-Si eutectic bond.

CHAPTER 1

INTRODUCTION

Only 7 years after the invention of the transistor in 1947, Texas Instruments was selling silicon transistors and by the early 1960's the first computers were made using circuits with small scale integration. Now integrated circuits (ICs) are an integral part of nearly all of the electronics that we use and the semiconductor industry has turned into a $200 billion/year market. In contrast, the first microelectromechanical systems (MEMS) pressure sensors were not commercially available until the 1980s and it was not until the 1990s that MEMS accelerometers were mass produced for automotive crash detection and that Texas Instruments brought DMD (digital micro-mirror devices) to market for projection displays. Despite the fact that MEMS technology is based on the same fabrication and lithographic techniques used for the production of ICs, the commercialization of MEMS devices has lagged behind. One reason for this longer gestation period is the added complexity in packaging MEMS devices which either prevents their commercialization or significantly adds to the cost of manufacturing. Furthermore, packaging often accounts for greater than 50% of the total cost of manufacturing a MEMS device [1-3].

In recent years, the MEMS market has grown significantly with a diverse set of MEMS devices currently on the market including: MEMS microphones which replace standard microphones in cell phones; MEMS pressure sensors used in wide variety of industrial and automotive application; accelerometers and gyroscopes used for traction control, GPS and image stabilization in camcorders and cell phones; and micromirrors which are the heart of Texas Instruments' projection display technology. In the near future we will also see a growing number of RF (radio frequency) switches and micro-resonators used in wireless circuits; MEMS micro-mirrors used as optical cross-connects

in telecommunications networks; and an array of biomedical and micro-fluidics applications including implantable devices, devices for DNA manipulation and MEMS devices for drug delivery. In fact, the MEMS market is currently a roughly $6 billion/year market and is expected to grow to $18 billion by 2015 [4]. In this diverse and growing market, packaging remains the most costly and one of the most prohibitive steps in the manufacturing process.

The goal of this thesis is to offer a *wafer-level vacuum packaging* solution which will help bring more MEMS devices to market. To do this, four major criteria need to be met (Table 1.1): i) the temperature at which the MEMS device is packaged should be low enough not to damage the device (≤400ºC for CMOS processes), ii) electrical connection should be made via feed-through interconnects, iii) the packaging process should be conducted at the wafer-level (which means that all of the devices across a wafer are encapsulated at the same time), and iv) the packaging process should be capable of supporting vacuum pressures of less than ≤10 mTorr. Sections 1.2 through 1.4 discuss the reasons behind these metrics.

Table 1.1: The metrics used in this work for a generic wafer-level packaging process that can be used on a broad set of MEMS devices.

Metrics	Description
Low temperature	The process should be conducted at a low enough temperature not to damage the device (≤400ºC for CMOS processes)
Electrical Connection	Electrical connection should be made via feed-through interconnects
Wafer-level process	The process should be conducted at the wafer-level
Vacuum Compatible	The process should allow for vacuum packaging of MEMS components (vacuum pressures ≤10 mTorr)

In order to fulfill the metrics outlined in Table 1.1, a *Au-Si eutectic wafer-level vacuum packaging* process is detailed in Chapters 2 through 5 and a new technique called *differential localized heating* is introduced in Chapter 6. The *Au-Si eutectic wafer-level vacuum packaging* process meets the metrics shown in Table 1.1 in the following ways: i) it is performed at a relatively low temperature ≤390ºC allowing for bonds to wafers fabricated in CMOS or CMOS-like processes, ii) the Au-Si eutectic layer melts during bonding allowing for bonds over non-planar surfaces such as electrical-feedthroughs, iii) bonds are conducted at the wafer-level so that all devices across a wafer get packaged at

the same time, and iv) with the integration of Nanogetters™ [5, 6], vacuum pressures from <2 to 22.3 mTorr were achieved. Furthermore, because the bond rings are patterned photo-lithographically, they can be as small as tens of microns in width, allowing for a small overall package size. *Differential localized heating* allows for packaging processes like Au-Si eutectic bonding to be performed at their desirable temperatures, but maintain a low temperature where devices are located, thus broadening the scope of devices that can be packaged at the wafer-level.

In the rest of Chapter 1, background on the need for a wafer-level packaging technology are presented, as well as a detailed look at other currently available packaging technology. More specifically, Section 1.1 provides background on IC wafer-level packaging, followed by Section 1.2 which explains the need for wafer-level packaging in MEMS, and their various physical, electrical and thermal requirements. Section 1.3 explains various encapsulation techniques that have been applied and/or investigated by other researchers. Section 1.4 details work done in vacuum packaging. Section 1.5 summarizes the motivation for using *Au-Si eutectic wafer-level vacuum packaging* as well as *differential localized heating*. Finally, Section 1.7 provides the organization of the rest of the dissertation and Section 1.6 presents the contributions of this work to industry and the research community.

1.1 IC Wafer Level Packaging

IC and MEMS packaging generally involve the process steps needed directly after fabrication of the devices on the wafer. Table 1.2 shows how these packaging steps are categorized for the IC industry [7], giving some element and interconnection examples. Level 0 refers to the processes needed for fabrication of the functional IC or MEMS device, Level 1 involves the encapsulation processes and/or integration with a lead-frame package, Level 2 entails the integration of this component with other electrical components, typically on a printed circuit board (PCB), and Levels 3-5 account for assembly of the entire system. References to IC and MEMS packaging usually pertain to levels 1 and 2.

Table 1.2: Package hierarchy for IC's and MEMS devices.

Level	Element	Packaged / Interconnected by
Level 0	Transistor within IC or resonator in a micromachine	IC metallization, wafer-level protection, thin-films
Level 1	ICs, discrete components such as a Si/glass pressure sensor sandwich	Wafer bonded, conventional lead frame packages, multi-chip module packages
Level 2	Single- and multi-chip packages (a pressure sensor in a TO header)	Printed wiring boards
Level 3	Printed wiring boards	Connectors/backplanes (busses), machined chassis or box
Level 4	Chassis or box	Connectors/cable harnesses
Level 5	System itself (a computer or a gas alarm)	

Over the years, the IC industry has evolved towards wafer-level packaging (WLP) processes in order to reduce the costs of level 1 and 2 packaging. The main technical drivers for IC packaging are thermal management and interconnection. Thermal issues generally come into play when attaching the IC chip to a printed circuit board (PCB). Interconnection issues generally involve figuring out ways to deal with higher pin counts and higher signal frequencies. As a result, ICs have evolved toward a technology called wafer-level chip scale packaging (WL-CSP).

One component of WL-CSP is the mini ball grid array (mBGA) technology shown in Figure 1.1 which re-routes bond pads (which are generally at the periphery of an IC) to flip chip pads [8-10]. This is accomplished by depositing two benzocyclobutene (BCB) passivation layers and an aluminum feed-through layer on top of the IC. These feed-throughs electrically connect the closely spaced interconnection pads at the periphery to solder ball joints which are evenly spaced across the die. All of the deposition steps and the electroplating of the solder are done at the wafer-level. Furthermore, the mBGA process allows for wafer-level burn-in and test (WLBT) and wafer-level testing of known good packages (KGP). Such wafer-level testing can reduce testing costs by as much as 50%. [10]. Even an epoxy resin "under fill" layer is applied at the wafer-level to fill the area between the solder joints in order to reduce mechanical stress.

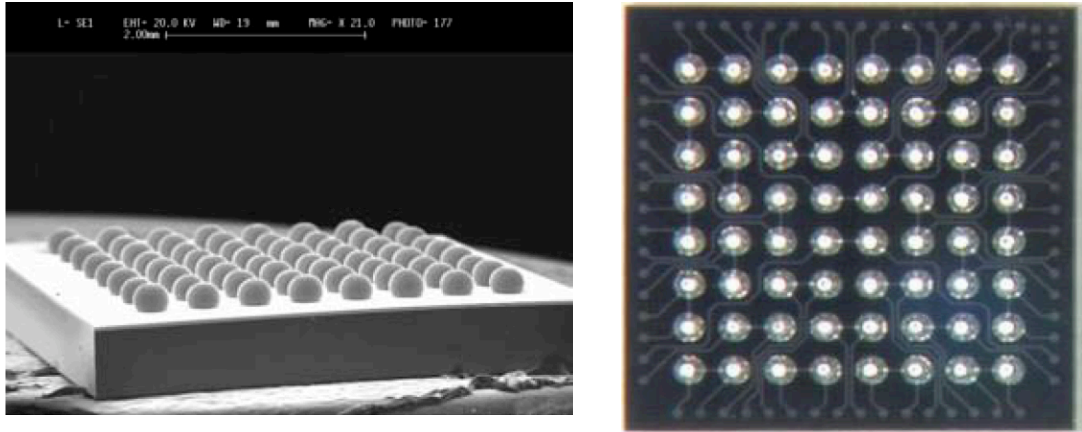


Figure 1.1: An SEM (left) and microscope photograph (right) of mBGAs.

WL-CSP is an exciting set of technologies because they allow for all the IC packaging steps to be done at the wafer-level. This technology has matured, being applied for passive devices, EEPROM, flash memory, DRAM, ASICs and microprocessors [11, 12]. As a further sign of this technology's maturity, several foundries currently offer WL-CSP processing including Flip Chip International and Amkor Technology which are now ship more than a million units per week [11, 13].

1.2 MEMS WAFER LEVEL PACKAGING

Many of the same thermal management and interconnection issues involved in IC packaging also apply to the packaging of MEMS with a whole set of additional challenges. These packaged parts in fact have micro- and nanometer dimension that need to interact with the environment for sensing but need protection from even the smallest particles. Although no one package design is suitable for all applications, in general there are two tracks for packaging MEMS devices: *chip-level* packaging and *wafer-level* packaging. Figure 1.2 shows a typical chip-level packaging sequence in which: i) the device is first diced (sawed from the wafer it was fabricated on), ii) the device is released (etching a film away so that the moving part can move), iii) the device is encapsulated in a dual-in-line (DIP) package or using flip chip in package (FCiP) technology, and iv) the DIP or FCiP is plugged in or soldered onto a PCB to interact with drive circuitry or other components. As labeled in Figure 1.2, steps ii) through iv) are costly because they are done serially on one device at a time. Also, because steps ii) through iv) involve the

handling of un-capped micro-mechanical parts, this approach often results in reliability issues and yield loss.

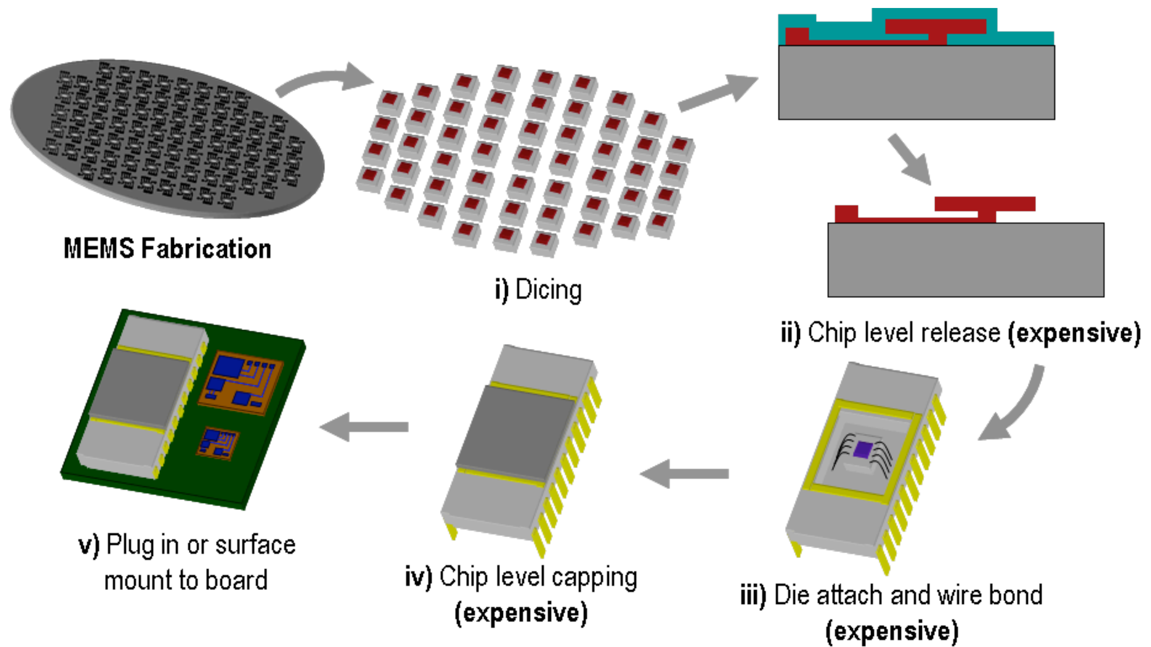


Figure 1.2: A schematic showing the typical packaging steps in a MEMS chip level packaging process.

Figure 1.3 shows a process sequence for the wafer-level packaging approach where devices: i) are released at the wafer-level, ii) encapsulated (using either another wafer or a thin film) while they are still on the wafer, iii) diced, and iv) the package is wire-bonded or flip chipped directly onto the PCB to interact with drive circuitry or other components. In the wafer-level approach all of the devices are released and encapsulated at once (in steps i) and ii)) on the wafer—thus reducing cost. In addition, these processes are done in a clean room environment which potentially increases their reliability. Furthermore, the wafer-level approach reduces overall package size which can help to further reduce the cost of manufacturing.

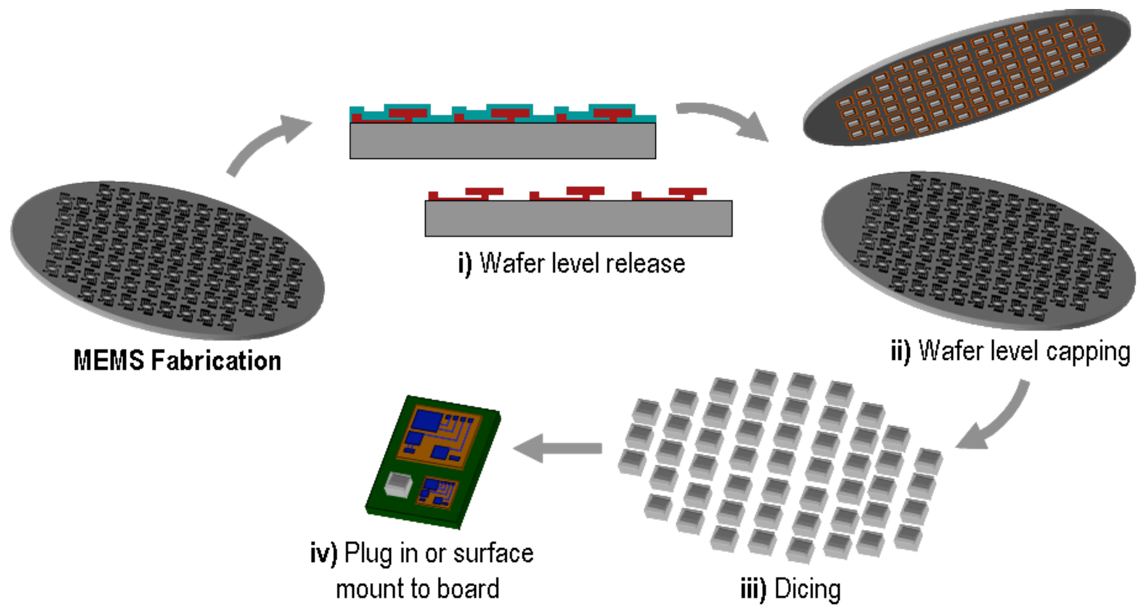


Figure 1.3: A schematic showing the typical packaging steps in a MEMS wafer-level packaging process.

It should be noted that Figures 1.2 and 1.3 are only simplifications of the packaging sequences needed for a MEMS device. Depending on the application, MEMS devices often need high frequency electrical connections, fluidic connections, special non-stick coatings, are often intolerant of high temperatures and need special environments (such as hermetic or vacuum) for operation.

In the rest of this section the physical requirements for MEMS packaging are discussed in detail in Section 1.2.1 and the electrical/interconnection and thermal requirements are then briefly covered in Sections 1.2.2 and 1.2.4.

1.2.1 PHYSICAL REQUIREMENTS

1.2.1.1 Packages with Access to the Environment

Pressure sensors and microphones are two MEMS applications that need access to the environment for sensing but need protection from particulates, corrosion and harsh physical contact. A schematic of NovaSensor's pressure sensor package [14] is shown in Figure 1.4. As shown, the wire bonds, electrical leads and the MEMS device are coated with a silicon gel. The coated device is further encapsulated from physical contact by a metal package which is sealed with a welded joint, where electrical leads run out of the

package providing electrical connectivity. An opening in the top of the package allows for ambient air to enter the package. The silicone gel allows for protection of the metal lead on top of the MEMS device from corrosion while—as an incompressible solid—it transmits the pressure from ambient to the MEMS pressure sensor. Figure 1.5 shows another approach used for access to/protection from the environment used for SiSonic's production of MEMS microphones [15]. In this approach, the MEMS and IC components are encapsulated using FR4 PCB material with an acoustic port which is offset from the MEMS die in order to avoid particle accumulation or physical damage to the die.

For the most part, both pressure sensors and microphones are packaged using chip-level processes.

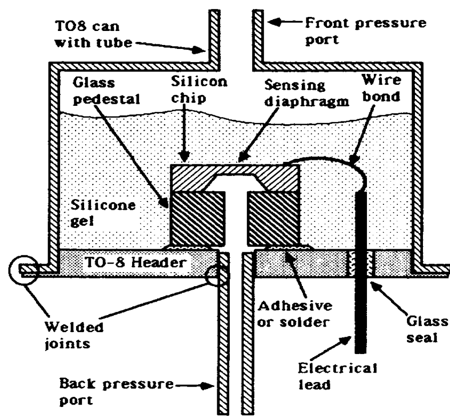


Figure 1.4: A schematic of a MEMS pressure sensor package [14]

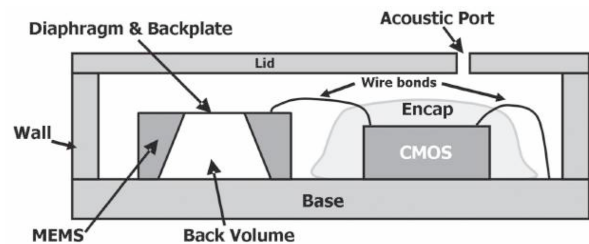


Figure 1.5: A schematic of a MEMS microphone package [15]

1.2.1.2 Stiction and Non-Stick Coatings

Another class of devices require non-stick coatings so that moving parts do not adhere to sidewalls or get damaged when contact is made. At the same time, these devices also need protection from the environment. The iMEMS (integrated MEMS) process used for making Analog Devices inertial sensors [16], RF switches produced by Radent MEMS [17-19] and the Texas Instruments DMD projection displays [20, 21] fit into this category of devices. The non-stick coatings that these devices employ are used to prevent stiction,

which is the permanent adherence of the moving part to a sidewall. Stiction of MEMS devices can occur either during release (etching of the film underneath the MEMS structure) or due to an outside acceleration which can cause the MEMS structure to crash into the sidewall.

Stiction of the MEMS structure to the sidewall can be avoided by (1) making the restoring spring force relatively large, (2) increasing the surface roughness, (3) using "stiction reducing bumps" that reduce the contact area and thus reduce the stiction force [22], (4) using coatings which make the surface hydrophobic, reducing the affinity of water molecules to bond to the surface and thus reducing the stiction force [23] and (5) packaging the devices in an air damped environment (atmospheric pressure).

Where as options 1 through 3 can be accomplished by changing the mechanical structure of the MEMS device without affecting later packaging steps, options 4 and 5 can significantly add to packaging complexity. For instance, depending on the composition of the non-stick coating, it can react or interact with the bond material [16]. Furthermore, when packaging components near atmospheric pressure, it can be difficult to remove all of the moisture from inside of a package. Figure 1.6 shows a packaging method employed by Texas instruments where they encapsulated a special gettering material which reacts with water vapor inside of the package. Dramatic improvements were shown in accelerated temperature/humidity reliability testing of their micro-mirrors using this approach [21].

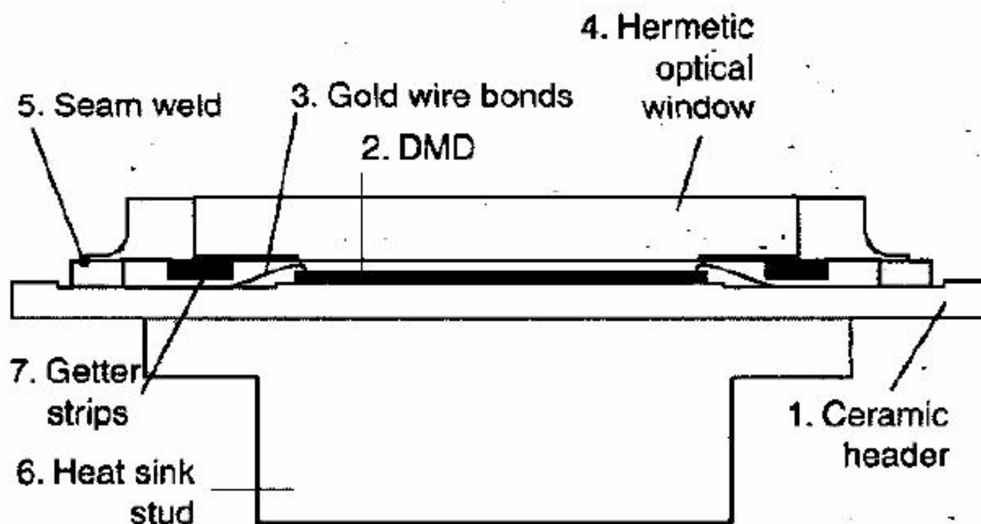


Figure 1.6: A schematic of the encapsulation used for Texas Instruments micro-mirrors [21]

1.2.1.3 Biomedical and Microfluidics Packaging

Biomedical and micro fluidic MEMS are rapidly growing fields for research. Two of the main drivers for implantable bioMEMS are to make smaller packages that will take up less space in the body and on ways to make interconnection to the device from outside of the body. Figure 1.7 shows one such packaging solution developed at the University of Michigan where the device is encapsulated using an anodic bond where power is input and data is acquired using a wireless link [24-26]. Others have investigated MEMS pressure sensors for monitoring artery clogging, neural probes, cochlear implants and MEMS drug delivery systems. These devices, which need to operate inside of the human body, will often require hermetic seals that are resistant to corrosion due to bio-fluids. Furthermore, because many of these devices are fabricated using polymers or polymer substrates, they cannot be exposed to high temperatures during the encapsulation process.

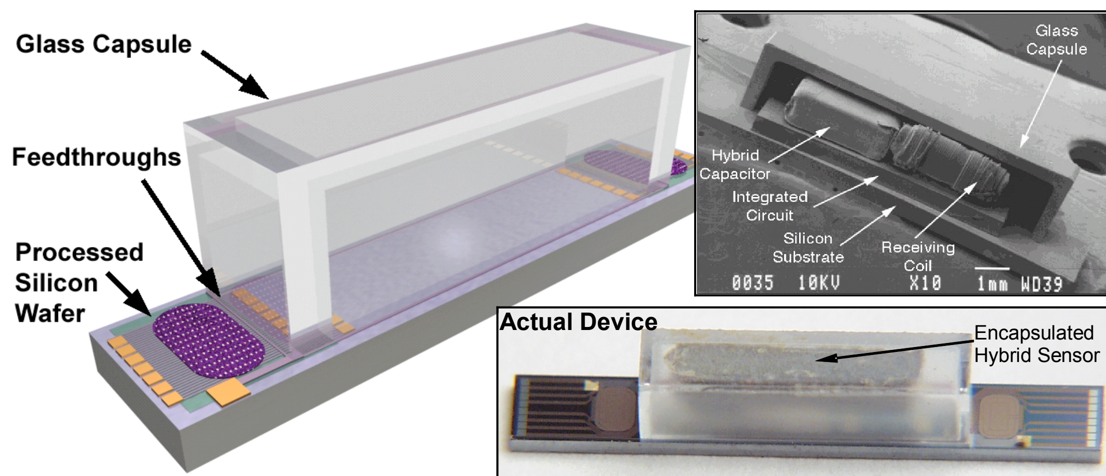


Figure 1.7: An encapsulation approach for implantable devices done at the University of Michigan [26].

1.2.1.4 Vacuum/Hermetic Encapsulation & Protection from the Environment

There are two types of devices which require vacuum for optimal performance: i) resonators and resonant sensors, some of which require the reduced damping of a vacuum environment in order to achieve reasonable oscillation amplitudes; and ii) transducers that require a significant amount of thermal isolation. These include micro-bolometers for infrared imaging (<10 mTorr) [27-29] and micro-resonators used for high accuracy clocks, filters and mixers in a wide range of RF applications (1 μTorr to 760 Torr) [30, 31]. Even applications such as heated micro-columns used for gas chromatography [32,

33] can operate at as much as two orders of magnitude less power at milliTorr pressures. Furthermore, a much wider range of devices simply requires hermeticity or even protection from the environment. This includes most of the devices described in Sections 1.2.1.1,1.2.1.2 and 1.2.1.3.

Motorola was one of the pioneers in wafer-level hermetic encapsulation technology with the development of its patented frit bonding processes in 1994 [34]. In the frit bonding process, a glass frit layer is used to adhere a cap wafer to the device wafer where individual glass frit bond rings encircle the devices (the details of this bond process will be given in Section 1.3.2.4). Motorola and Analog Devices have since used frit bonding for the packaging of many of their commercial inertial sensors [35-38]. Several other companies have used unspecified wafer-level encapsulation processes including Radent MEMS [17-19] (see Figure 1.8) which used wafer-level packaging for hermetically sealing their RF switches and Raytheon which used wafer-level packaging to encapsulate their micro-bolometers (infrared sensors) at below 10 mTorr (a more complete list of vacuum encapsulation data throughout the literature will be given in Section 1.4). Piezoresistive pressure sensors and acoustic microphones (which were discussed in Section 1.2.1.1) also generally require an encapsulated reference volume which is often created using wafer bonding techniques. These reference volumes generally require vacuum levels on the order of 1 Torr.

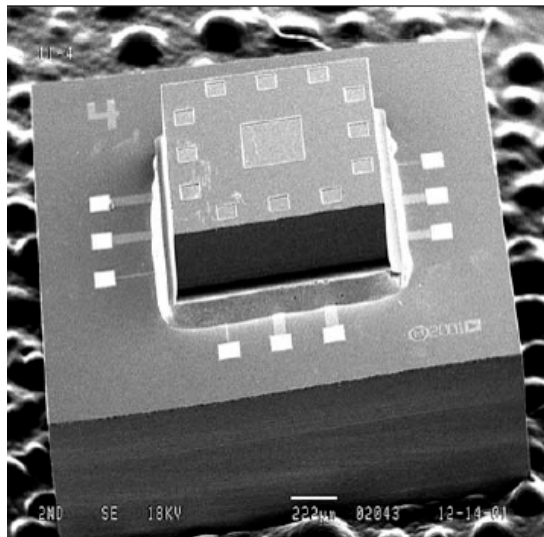


Figure 1.8: A scanning electron microscope (SEM) picture a wafer-level packaged micro-switch manufactured by Radent MEMS [17].

1.2.2 ELECTRICAL CONNECTION & INTEGRATION

As explained in Section 1.2.1.4, nearly all MEMS devices need some kind of encapsulation. This need for encapsulation makes it difficult to provide electrical connectivity. There are two basic approaches used for providing electrical connectivity in a wafer-level packaged device: lateral feed-through interconnects and vertical feed-through interconnects. Lateral feed-throughs can be created using either metals or doped poly-Si in the same thin film processes used for the fabrication of the MEMS device. Figure 1.9 shows a schematic of an encapsulated device in which a bond ring is used to adhere a capping substrate to the device substrate. In the case where the bond ring material is not electrically conductive, the bond ring material can go directly over the electrical feed-through. If the bond ring material is electrically conductive, as is the case with a metal or alloy, a passivation material is required. Lateral feed-throughs are desirable because they often can be integrated into the thin film process used to make the device. On the other hand, because of resistive and capacitive parasitics, they may not be suitable for many high frequency applications such as RF MEMS switches and micro-resonators. The Radant MEMS packaged micro-switch which was shown in Figure 1.8 is one example where lateral feed-throughs were used for electrical interconnection.

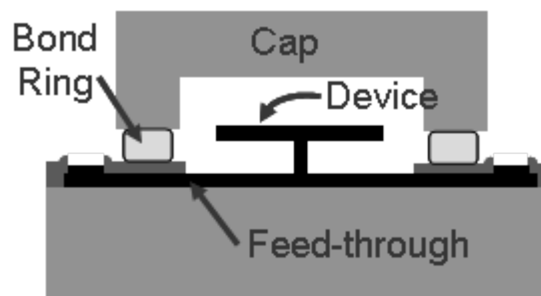


Figure 1.9: A schematic illustrating lateral feed-throughs.

As shown in Figure 1.10, vertical feed-throughs can be created through either the device substrate or the capping substrate. This involves “bulk micromachining” which requires machining of the substrate itself as opposed to thin film deposition and patterning processes. Wet chemistries for creating via holes through Si and glass substrates are cost efficient, but generally require a large amount of substrate area (for

instance etching through a 500μm glass wafer, under the best possible conditions requires more than a 1 mm diameter circular area on the back surface of the glass substrate). Using thinner substrates reduces the amount of surface area needed to accommodate the via hole, but as you reduce wafer thickness below 100 or 200 μm they become fragile and difficult to handle. Deep reactive ion etching (DRIE) can be used to etch through very thick wafers with excellent aspect ratios allowing for holes through 500 μm thick substrates that take up only a few hundred square microns (i.e. on the order of 10×10μm or 20×20μm). After etching the via whole a conductive layer then needs to be evaporated, sputtered and/or electroplated and in the case of Si, this conductive layer needs to be electrically insolated from the Si substrate. Overall, it can be significantly more challenging to design vertical feed-throughs, but as compared to lateral feed-throughs, very low resistances and parasitics can be achieved using vertical feed-through interconnects. Furthermore, such feed-through can allow for flip chip bonding of a die which is desirable for integration with PCBs or other types of substrates. Their main drawbacks are the added complexity to the fabrication process and the potentially large die area the bond pads take up which can limit the number of interconnection lines. Figure 1.11 shows an Analog Devices accelerometer which was packaged using vertical feed-throughs. This packaged device can potentially be flip chipped directly to a PCB.

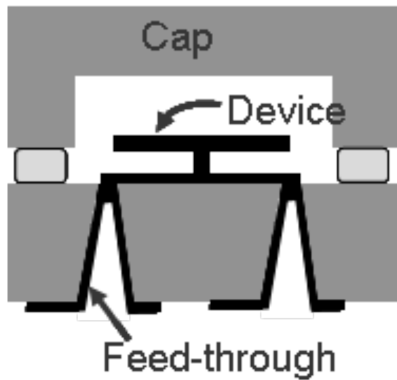


Figure 1.10: A schematic illustrating vertical feed-throughs.

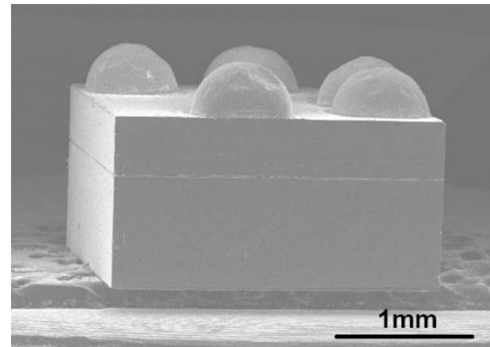


Figure 1.11: An SEM of a packaged accelerometer using vertical feed-throughs by Analog Devices [38].

1.2.3 INTEGRATION

There are two general approaches for integrating a MEMS device with its drive

circuitry: *the two chip solution* and the *one chip solution*. In the *two chip solution* the MEMS device is fabricated on a different wafer and likely in a different process than the drive circuitry. Figure 1.12 shows an example of the *two chip solution* in the packaging of a Motorola accelerometer [39] where the MEMS device is placed in a Ceramic Dual in Line Package (CERDIP) and interfaced with the CMOS drive circuitry via wire-bonds. The advantage of the *two chip solution* is that the processes and materials for the MEMS and CMOS devices can be optimized for each process. As well, the MEMS and drive circuits can be tested and screened before integration so that a known-good-MEMS device is integrated with known-good-drive-circuitry allowing for a higher overall yield. The main disadvantage is a larger overall package size as compared to the 1-chip solution.

Using the *one chip solution* on the other hand, the MEMS device and drive circuit are integrated on the same chip and therefore in the same MEMS process. Figure 1.13 shows the "one chip" solution used by Analog Devices [40] where the device (in this case a gyroscope) is fabricated on the same substrate as the control electronics. Analog Devices then packages these encapsulated dies either in a lead frame chip-scale package (LFCSP) or in a slightly adapted process where solder balls are reflowed through holes in the cap wafer using vertical feed-throughs (as was shown in Figure 1.11). The advantage of the *one chip solution* is its overall smaller size and the clearer electrical signals between electronics and the MEMS device. The disadvantage is that the MEMS process must be compatible with the process for the drive circuitry which strictly limits the design of the MEMS device. Furthermore, the yield of the MEMS and drive circuitry are coupled. In other words, if either the MEMS or drive circuits fails, the whole chip fails, so that the total yield equals the MEMS yield times the CMOS yield.

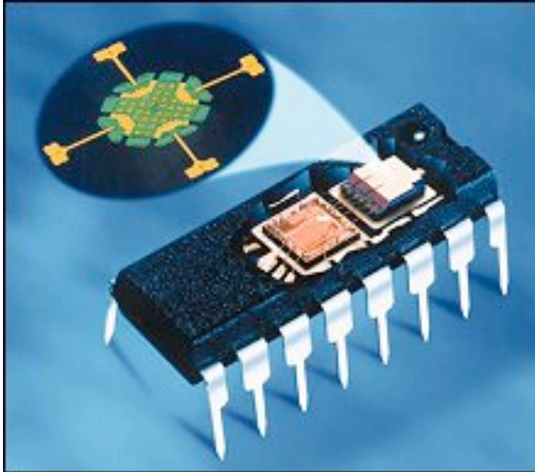


Figure 1.12: A Motorola accelerometer using the 2 chip approach [39].

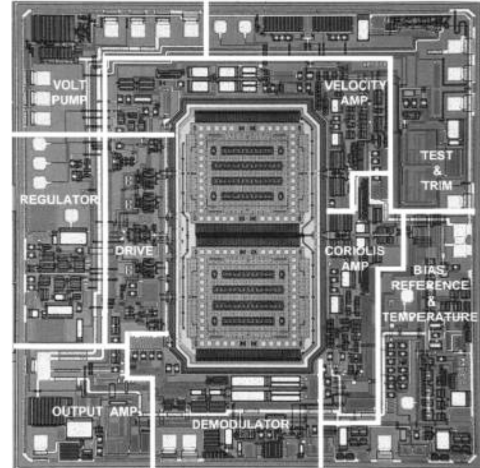


Figure 1.13: An Analog Devices gyroscope using the 1 chip approach [40].

1.2.4 THERMAL REQUIREMENTS

As will be discussed in Section 1.3 (*MEMS Wafer Level Encapsulation Approaches*), an encapsulation process can require temperatures anywhere from near room temperature to around 1000ºC with varying levels of hermeticity and process complexity. This complicates the process since depending on the application, MEMS devices have varying tolerances to high temperatures. For instance, MEMS devices fabricated in CMOS processes generally cannot handle temperatures higher than 400ºC since such temperatures can damage the top aluminum interconnection layer [41, 42]. In fact, the next generation of CMOS processes from 65 nm line widths and smaller will likely require lower and lower temperatures—even as low as 300ºC as CMOS technology continues to advance [42, 43]. Various MEMS processes also incorporate other metals which can inter-diffuse with each other or with other materials at temperature of 200ºC to 400ºC or even lower, compromising the performance of the device. Devices incorporating polymeric materials often have even more stringent temperature requirements and can be potentially damaged at temperature well below 200ºC.

Another challenge in applying high temperatures during an encapsulation processes involves differences in the materials coefficients of thermal expansion (CTE). These CTE mismatches cause the two materials being mated to expand or contract by different

amounts. These expansions and contractions can induce stresses that affect performance or even damage the device and/or package.

1.3 MEMS Wafer Level Encapsulation Approaches

As discussed in Sections 1.2 and 1.3, wafer-level packaging is desirable for both ICs and MEMS mainly because it allows for low cost/high volume production, small size and improved reliability. For the various classes of devices discussed in Section 1.2, nearly every one needs to be encapsulated to either provide vacuum/hermeticity or simple protection from the environment. Furthermore, this encapsulation needs to be achieved at a temperature that will not ruin the device and it needs to be configured in a way that electrical signals can get in and out. To accomplish both integration and vacuum/hermetic encapsulation, two distinct packaging approaches have evolved, the *integrated encapsulation* approach (using thin films) and the *post processing* approach (using wafer bonding). These will be discussed next in Sections 1.3.1 and 1.3.2.

1.3.1 INTEGRATED ENCAPSULATION (THIN FILM PACKAGING)

Figure 1.14 shows an example of the integrated encapsulation approach [44]). In the *integrated encapsulation* approach the devices (and potentially the drive circuitry) are processed first, without etching any sacrificial layers needed for release of the device (Figure 1.14b). Another sacrificial layer is then deposited and patterned atop the device layer (Figure 1.14c). Next, an encapsulation layer is deposited and patterned with a fluid access hole (Figure 1.14d). Finally, after etching of the sacrificial layer (Figure 1.14e), the fluid access holes are sealed under vacuum either using CVD thin films, evaporated metals or solder.

Several authors have used approaches similar to the one shown in Figure 1.14 where phosphosilicate glass (PSG) or SiO_2 were used as the sacrificial material, where hydrofluoric acid (HF) was used to etch the sacrificial layer and low pressure chemical vapor deposited (LPCVD) Si_3N_4 [44-46], deposition of silicon [47, 48] or a combination of poly-Si and aluminum [49] were used as the encapsulation layer. Instead of using a fluidic access port, several authors have used porous poly-Si as the encapsulation

material [50-52]. These poly-Si layers are permeable to HF allowing for etching of the sacrificial layer.

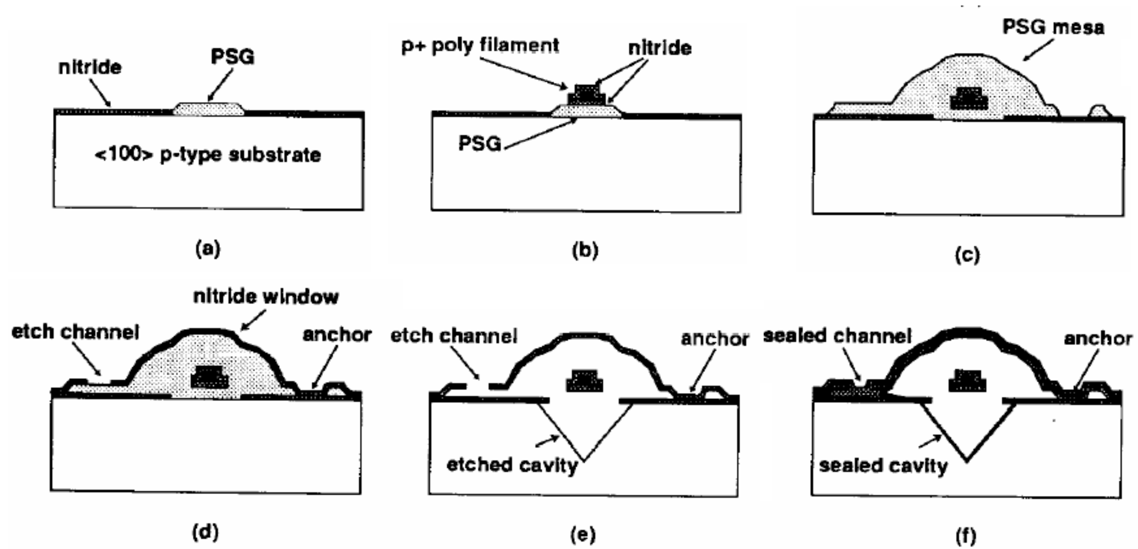


Figure 1.14: A schematic showing the process flow for thin film encapsulation [44]

Using the thin film encapsulation approach, Candler et al. and Kim et al. have demonstrated >1 year of vacuum encapsulation data and implemented extensive reliability testing with no detectible leak [53, 54]. Figure 1.15 shows an accelerometer which was fabricated and packaged using a similar thin film process, demonstrating the size advantage that can be gained using thin film packaging [55].

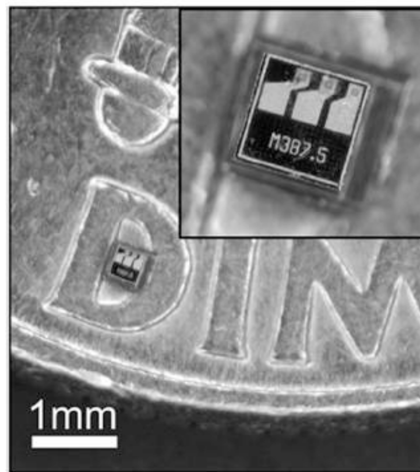


Figure 1.15: A packaged accelerometer developed by Stanford University and Bosch [55]

All of the above LPCVD processes involved relatively high temperature steps (generally >950ºC) either in the deposition of the sacrificial layer that goes over the device, deposition of the capping material or the material used to seal the package. These temperatures are acceptable if the MEMS device process is integrated into those fabrication processes but can provide limitations in the design of the MEMS device.

Others have offered lower temperature processes for device encapsulation. Stark et al. [56, 57] at the University of Michigan used a variation of this approach, using photoresist as the sacrificial layer, an electroplated nickel encapsulation later and lead-tin solder balls for sealing the fluidic access port at 230ºC. The main difficulty in using these thin metal film packages is in the TCE mismatch which causes large mechanical stresses and in the fact that solders tend to outgas, potentially raising the pressure in a vacuum packaging process. Another low temperature approach involved depositing a polymeric encapsulation layer where the sacrificial layer was removed by thermal decomposition [58]. The highest temperatures that devices get exposed to using this process are during the thermal decomposition step at 200 to 300ºC. Similarly with this process there should be issues with outgassing of the polymer which is problematic for vacuum packaging applications.

Overall, the thin film packaging approach has a number of advantages. As was shown in Figure 1.15, there is the potential for minimizing the overall package footprint. This is important for applications that require small packages as well as for making an all around low cost device. Furthermore, when the MEMS process steps can be integrated with a CMOS compatible thin film encapsulation process, it makes it easier to find a manufacturer for the MEMS device since there are a large number of foundries and contract manufactures that can handle CMOS processing. On the other hand, using this approach generally requires long release times since the etchant attacks the sacrificial layer through fluidic access holes and then needs to get flushed out. Furthermore, as mentioned earlier, the device process needs to be compatible with the process temperatures and materials used in the thin film process used for encapsulation.

1.3.2 POST PROCESSING (PACKAGING USING WAFER BONDING)

As compared to the integrated encapsulation approach, the *post processing* approach

can potentially be more flexible and applicable to a wider range of devices. Figure 1.16 shows a schematic of the basic concept behind the post processing approach. In this approach, the device (and potentially the drive circuitry) is processed on one wafer and the cap wafer is fabricated separately. The two wafers are then bonded using either fusion bonding, anodic bonding or an intermediate material such as glass frit, a polymer, a solder or a eutectic. Figuring out how to apply these various bond techniques on a wafer with 100s or 1000s of MEMS devices and achieving successful hermetic and even vacuum tight seals on a high percentage of them can be difficult. As compared to the integrated encapsulation approach, the die size can be significantly larger and in many cases more exotic materials and processes may be needed for implementation.

In Sections 1.3.2.1 through 1.3.3, the various bonding techniques investigated for the post processing approach are discussed.

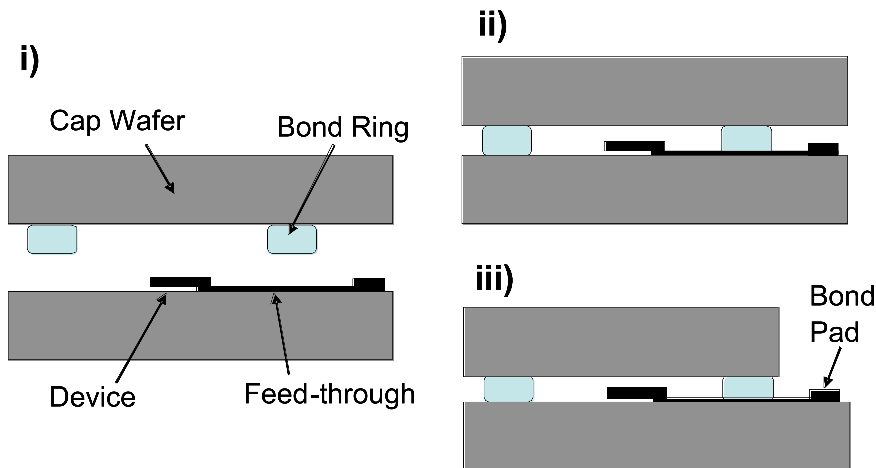


Figure 1.16: One encapsulation scheme using i) a cap wafer and a bond ring where ii) the wafers are bonded and iii) part of the top wafer is removed in order to access a bond pad for interconnection.

1.3.2.1 Fusion (Direct) Bonding

Fusion bonding is known to occur spontaneously when joining two very flat, clean surfaces. Fusion bonds have been investigated between a wide range of material combinations including: GaAs-to-silicon, quartz-to-silicon, silicon-to-sapphire, sapphire-to-GaAs, silicon-to-glass, silicon carbide-to-silicon and silicon-to-silicon both with and without intermediate SiO_2 and Si_3N_4 layers [59-61]. Conventionally, wafers are pre-etched and surface impurities are oxidized and/or desorbed away at elevated temperatures

in a vacuum chamber before bonding. This leaves OH groups at the surface of the wafers, and it is believed that at room temperature the two wafers to be bonded are held together by van der Waals, capillary and electrostatic forces. Once the wafers are brought together, the elevated temperature allows for strong covalent bonds to form. Conventional Si to Si and Si to SiO_2 (on a silicon substrate) bonds require temperatures ranging from 600 to 1200 °C.

Several authors have used another technique called plasma enhanced fusion bonding to achieve lower temperature fusion bonds. With thorough cleaning and application of plasma before the wafers are joined, the wafers are made highly reactive before joining allowing for much lower temperature bonds. Authors have reported plasma enhanced fusion bonds between Si and Si_3N_4 (on a Si substrate) at 300°C [62] and Si and SiO_2 (on a Si substrate) at room temperature [63].

Fusion bonds are widely used for silicon-on-insulator (SOI) wafer production. Although fusion bonds have been applied for fabrication of accelerometers [64] and pressure sensors [65] this bonding technology is not compatible for hermetic/vacuum sealing most MEMS devices. One issue is the 600 to 1200 °C temperatures needed for standard fusion bonds. As of yet, hermetic/vacuum seals have not been demonstrated with the lower temperature plasma enhanced bonding. Another limitation is the requirement for surface roughness of less then 50 Å. Although the surfaces can be planarized to achieve this surface roughness, this adds significant complexity and cost to the device process. Furthermore, fusion bonding is extremely particle intolerant—particles <1 μm in size for instance can result in un-bonded regions of 100 microns. This necessitates the use of stringent cleaning procedures and careful handling before bonding.

1.3.2.2 Anodic Bonding

The anodic bonding process was first patented in 1968 [66], in which a metal to insulator and a semiconductor to insulator bonding process was described. Since then, the most common use of anodic bonding has been between sodium rich Pyrex glass and silicon wafers. In anodic bonding, the substrates are put into contact, heated to a temperature below their softening points and an electric field is applied. With the induced electric field and elevated temperatures, sodium atoms from the glass then

migrate to the Si causing an even larger electric field at the interface. It is believed that the combination of the electric field, the high temperatures, and the diffusion of sodium atoms allow for formation of chemical bonds between the two wafers.

Voltages between 400 to 1500 V at temperatures ranging from 300 to 500°C are generally used depending on the composition and thickness of the substrates being bonded. This technique has also been applied to a wider range of substrates using sputtered and evaporated thin films of glass to form bonds between various substrates and Si at temperatures as low as 135°C [67-69] and to metal surfaces [70-72].

A standard anodic bonding process can be applied at 300ºC with highly reliable hermetic/vacuum seals making them desirable for many applications. Anodic bonding has been applied for vacuum/hermetic encapsulation of a wide range of MEMS devices including pressure sensors [73], gyroscopes [74], accelerometers [74, 75], flow sensors [76] and infrared sensors [77]. The scope of devices which anodic bonding can be applied to is limited by the need for a high electric field and the presence of sodium which can compromise integrated circuits and other device processes. Also, similar to fusion bonding, applications of anodic bonding are limited by its requirement for less then a 300 Å surface roughness.

1.3.2.3 Thermo-compression Bonding

Thermo-compression bonding is applied by coating two wafer surfaces with metal and applying a large amount of force at an elevated temperature, providing enough energy to soften the metals and create covenant bonds. This process is similar to fusion bonding in that it requires two clean and chemically active surfaces but unlike fusion bonding, thermo-compression bonding is intolerant of native oxides. As a result, gold-to-gold bonds are the most common because of the inertness of gold, which makes them resistant to oxidation.

Thermo-compression bonding is attractive because of its simplicity. As a result, it has been used extensively for wire bonding and die attach for ICs but is more difficult to apply to full wafer bonds in MEMS applications. These applications are limited by the need for very high bond pressures of around 100 MPa and temperatures of around 200 to 400°C. Most importantly, as with fusion bonding, thermo-compression bonding requires

extremely planar/low surface roughness surfaces material and is extremely intolerant of particles.

1.3.2.4 Glass Frit Bonding

One of the more commonly used methods for encapsulating circuits and MEMS devices is frit glass bonding. In this process, a glass powder called glass frit is mixed with a paste consisting of solvent and organic binders. The glass frit portion forms the majority of this mixture whereas the paste allows for the material to be screen printed, reducing the coefficient of thermal expansion (CTE) and helping to enhance the mechanical strength. After screen printing the glass frit/paste mixture onto one of the wafer surfaces, the organics are outgassed and the glass melted through a temperature sequence. Finally, at a temperate ≥450°C, the wafers are brought together and the melted glass layer is bonded to the surface of another wafer. The softened glass frit and applied pressure during bonding allow for a hermetic seal. The frit is then cooled and allowed to solidify forming a permanent bond. Many types of glass frit are commercially available with different melting points, CTEs, organic binders, and screen printing properties. Most of the low temperature (~ 450 ^{o} C) frit glass formulations contain some lead.

Glass frit has several advantageous properties. It can be deposited on a wide range of materials, is non-conductive, can be applied directly over electrical feed-throughs and is softened during the bonding process allowing for bonds over non-planar surfaces. Frit bonds have been incorporated into MEMS video scanners [78], resonant density sensors [79] and accelerometer and gyroscopes for automotive applications [35-39, 80]. A vacuum seal has even been demonstrated at the chip level using glass frit bonding by ISSYS corporation using their patented Nanogetters™ to achieve pressures as low as 850 μTorr [5, 6].

The main drawbacks for frit bonding are its relatively high bond temperature of around 450°C which precludes its use in application to CMOS, and the need for screen printing which generally limits the patterning resolutions to no smaller than 150 μm [81]. Another drawback is its lead content which may limit its applications because of impending world wide legislation which will ban the use of lead for most electronics.

1.3.2.5 Spin on Glass (SOG) Bonding

Spin on glass (SOG) bonding is another glass seal wafer bonding technique where silanol (Si–OH) and methyl (CH_3) polymers are dissolved in an alcohol/acetone solvent to form a spin-on material that is often referred to as a sol-gel [82, 83]. After spinning this material onto one of the wafers, the wafer pair is bonded at 250°C-400°C. Typically the wafer pair is then exposed to a second higher temperature step (~1100°C) in order to improve the dielectric breakdown voltages. As with frit bonding, SOG wafer bonding has the advantage of being able to conform over topology such as feed-throughs, but is limited in this respect because of maximum deposition thickness for sol-gel of less then 1µm because of high internal stresses [83]. Furthermore the secondary high temperature step limits its application for most MEMS devices.

1.3.2.6 Polymer/Adhesive Bonding

Another approach to wafer-level encapsulation uses a polymer as an adhesive layer. In general polymers are deposited in liquid form through spin-on coatings and then cured at anywhere from room temperature up to 250ºC. A number of polymers with varying material properties have been used for wafer bonding. They include SU8 [84], BCB (benzocyclobutene) [85, 86], CYTOP (fluorocarbon polymer) [87, 88], PMMA (polymethylmethacrylat)[89], Polyimide [90], MYLAR [91], Parylene (poly-para-xylylene) [92] and many different epoxies and waxes, and liquid crystal polymers (LCP).

The advantage of using polymers is that they melt at low temperatures, allowing them to melt, conforming over features on the wafer. This allows for bonding between two wafers that are not perfectly flat. Furthermore, many polymers can be easily deposited as a viscous liquid through spin-on coating, and then cured at a moderate temperature. Polymers can be deposited on a wide range of materials and are non-conductive, so they can be deposited over electrically conductive feed-throughs. CMOS and CCD devices in fact have been packaged for commercial applications in a glass-Si-glass wafer bond using epoxy [93]. Even so, polymer bonding is generally considered incompatible with vacuum packaging because of outgassing during the curing step or even hermetic encapsulation because of their high permiability. Furthermore polymers are susceptible to water uptake and gas diffusion which leads to delamination at the bond interfaces and

therefore potential reliability problems.

1.3.2.7 Solder/Eutectic Bonding

Similar to frit and polymers, solders and eutectics can be used as an intermediate material to joint two wafers. Solders and eutectics generally are metal alloys that melt at lower temperatures than the pure materials that make them up. Using this type of bonding, the solder or eutectic is melted at above its melting temperature allowing it to conform over non-planar features and form a strong metallic bond between the solder/eutectic and a solder, metal or poly-Si film on another substrate. Various alloys have been developed for the IC industry over the years for die attach and flip chip bonding which have been deposited both at the chip-level and wafer-level. More recently various solders have been investigated for wafer-level vacuum/hermetic encapsulation. These solders and eutectic alloys have a wide range of melting temperatures including Al-Si (577 °C) [94], Au-Si (363 °C) [95-104], Au-Ge (360 °C) [105], Au-Sn (217 °C to 420 °C)[106-108], Pb-Sn (182°C) [109, 110], Sn-Bi (130 °C) [57] and In-Sn (118 °C) [111, 112]. These solders are deposited by evaporating, sputtering and/or electroplating different combinations of metals or alloys. Thin metal films like Ti, Cr, Pt, W, and Au are used as adhesion and seed layers for the solder or metal stack deposition. Various authors have reported the use of unspecified solders for wafer-level vacuum packaging of micro-bolometer for IR imaging [27-29, 113] and gyroscopes [114].

Transient Liquid Phase (TLP) soldering is a type of solder bonding. Using TLP soldering, a low melting temperature metal is sandwiched in between a higher melting temperature metal. The temperature is raised above the lower temperature metal's melting point causing it to soften; allowing it to conform over non-planer surfaces. It then diffuses into the higher melting temperature metal creating a solid metal alloy. This new alloy then has a higher melting temperature than the original low temperature metal. In this way, the final bond joint has a higher melting temperature than the actual bonding temperature. Ni-Sn TLP has been demonstrated at 300ºC (although the lowest theoretical temperature is 232ºC) with packaged vacuum sensors that demonstrate a strong vacuum seal [115-118]. These packages were shown to be able to hold vacuum at temperatures as high as 370ºC.

In eutectic bonding a metal is deposited onto a substrate material and then at an elevated temperature, atoms from the substrate material diffuse into the metal, forming an alloy that melts at a relatively low temperature. This method has been employed by depositing gold onto germanium and onto silicon substrates in order to create Au-Ge [105] and Au-Si [95-104] intermediate layers that melt at 360ºC and 363ºC respectively and using Al deposited onto Si to create an Al-Si intermediate later that melts at 577ºC [94]. The Au-Si system in particular has been investigated by quite a few authors. In particular, in previous publications involving the work reported in this dissertation, a high yield wafer- level vacuum encapsulation process in which a vacuum seal was held for >1 year at pressures below 10 mTorr was demonstrated [104, 119, 120]. Chapters 2 through 5 provide more detail on this work.

Overall, solders and eutectics have the advantage that they allow for wafer bonds at relatively low temperatures and that they conform over non-planar surfaces. Furthermore, metals and alloys are much less permeable to gas and moisture than polymers or glasses, making them very desirable for hermetic and vacuum encapsulation. Despite the desirable qualities and extensive research employed to apply solders and eutectics for wafer-level packaging, there are a number of challenges in implementing these technologies which have stopped them from finding significant commercial use.

One of the major difficulties with solders is the need for a seed layer. These layers and the solders themselves inter-diffuse with each other and other material on the substrate, causing changes in metallurgy which can cause de-adhesion from the substrate, weak solder joints and shorting of electrical lines. One solution is using a “diffusion layer” which prevents the materials to inter-diffuse. Furthermore, currently available wafer bonding systems generally have long heating and cooling rates (on the order of 10s of minutes to an hour) as compared to chip-level bonding systems in which solder flip chip bonding can be performed in minutes. This further exacerbates problems associated with metal inter-diffusion. In general solder bonding methods have a lot of potential for enabling low temperature hermetic/vacuum encapsulation but are still immature technologies.

1.3.3 LOCALIZED HEATING

As has been discussed, the main reason for choosing low temperature bonding techniques is to reduce the exposure of devices to high temperatures which can compromise their performance. One method for achieving this is to use a localized heating method. Using localized heating, heat is generated near the bond joint while maintaining a lower relative temperature near the device. Localized heating methods are desirable so that established high reliability bonding techniques can be employed for the hermetic/vacuum packaging of devices which can not handle those high temperatures. The following sections discuss localized heating methods that have been investigated in the literature which include: resistive heating (Section 1.3.3.1), inductive heating (Section 1.3.3.2), and laser assisted bonding (Section 1.3.3.4).

1.3.3.1 Resistive Heating

Using resistive heating, a current is passed through a conductive material, causing joule heating. Using this method, the resistor can be patterned in the shape of a bond ring in order to encircle the device to allow for encapsulation. Both simulations and experiments have demonstrated that large temperature gradients can be achieved—for instants Cheng et al. was able to get a temperature drop of 700°C to around 50°C over a distance of less than 100μm from the location of the resistive heater [94]. This method has been used for bonding dies using plastic [121], PSG and Indium solder [122], fusion bonding [123], Au-Sn solder [124], and Au-Si eutectic and Al-Si eutectics [94, 123, 125]. In each case, the interface material melts and conforms over the resistive heater and the feed-throughs. In one case, a gold line was used as a resistive heater and as silicon diffused into the gold line the resistive heater acted as the bond interface in a Au-Si eutectic bond [125]. A vacuum package based on localized aluminum/silicon to glass solder bonding technique was even reported [94].

In all of these cases, it was necessary to make electrical contact with the surface of one of the bond surfaces in order to apply a current. It is therefore difficult to apply resistive heating at the wafer-level, and in all of the works described above, this technique was only applied one single dies. One author addressed this issue by proposing to array bond rings across an entire wafer, making electrical contact at the edge of two sides of the

wafer in order to apply a current [126]. This authors attempted to conduct wafer bonding experiments using Au-Sn solder but did not successfully achieve a bond. Even so, this is a promising approach.

1.3.3.2 Inductive Heating

Using inductive heating, a resistor is fabricated out of a ferromagnetic material which forms the bond ring. An inductive coil is then used to create a magnetic field which causes large eddy currents through this ferromagnetic material. These eddy currents cause joule heating. This method can therefore potentially be applied at the wafer-level without having access to the surface of the wafer. Yang et al. [127] used inductive heating to bond a glass wafer to a silicon substrate using a nickel-cobalt layer and was able to achieve a bond strength of 18 MPa. This technique has also been applied for chip level packaging of gyroscopes [128] and for chip-level packaging/assembly in bonds between silicon and steel [129] and for synthesis of carbon nanotubes [130].

1.3.3.3 Electromagnetic Radiation Heating

Large doses of microwave radiation (200 KHz.-20 GHz) in particular very readily heat metals while only marginally heating pure silicon and dielectric materials with low dielectric constants. Microwave heating was successfully applied by Budraa et al. [131] in order to create fusion bond between two 1200Å layer of gold coated substrates at high vacuum. Though this application of microwave heating was not specifically used for localized heating in this application, microwave heating is in fact a potential method for locally heating a bond rings at the wafer-level.

Similarly, Bayrashev and Ziaie used RF radiation to heat a dielectric to achieve wafer bonding [132]. This technique uses a high frequency electric field to impart energy to an insulator. Significant energy can be generated in dielectric molecules by agitating them in an alternating field. In this work, two-inch diameter silicon wafers were bonded via 2-20μm thick polyimide or photoresist intermediate layers. These substrates were joined with high uniformity (> 95% bond area) in less than 7 minutes. Similarly, though this application was not used for localized heating, it has great potential for use in localized heating of bond rings at the wafer-level.

1.3.3.4 Laser Assisted Bonding

Lasers have long been used for welding, and have more recently been used for selective wafer bonding [133-137]. The large energy density of lasers allow for fast and localized heating. One of the main challenges in applying laser assisted wafer bonding is choosing the correct materials. These materials need to be chosen so that the wavelength of the laser is transparent to the substrate but so that the material at the bond ring absorbs the lasers energy.

Researchers have used laser assisted bonding for anodic bonds [133, 134], indium bonds [135] and Pb-Sn bonds [136] in order to join silicon and glass dies. In these cases, 355 or 1064 nm wavelengths were used that were transparent to the glass but not to the material at the bond interface. Spot sizes varying from 20 μm up to 1 mm were achieved. In the case of the 1mm spot size, a mask was used on top of the glass substrate to ensure that only the areas of interest would be heated. In another study, a laser with a wavelength of 10.6 μm was used for joining silicon to silicon wafers using Au-Si and Al-Si eutectics [137]. In each case, reasonably strong bond interfaces were achieved.

One of the main drawbacks of this technique is that it is a serial process, although many emerging systems are capable of scanning large wafers for bonding. The display manufacturing industry in fact uses this technology quite extensively for sealing and packaging of flat panel displays.

1.4 Previous Work in MEMS Vacuum Encapsulation

As was outlined in Section 1.3, there are two distinct packaging approaches: the integrated encapsulation approach (using thin films on a single wafer) and the post processing approach (using wafer bonding). Vacuum packaging results using these two approaches are summarized in Sections 1.4.1 and 1.4.2 respectively.

1.4.1 VACUUM ENCAPSULATION USING THIN FILM PACKAGING

Table 1.3 summarizes the vacuum packaging results reported by various researchers using thin film packaging. Sole use of low pressure chemical vapor deposited (LPCVD) films by these authors allows for aggressive pre-deposition chemical cleans. This allows

for absorbed moisture and hydrocarbons to be removed in the LPCVD chamber directly before sealing at temperatures of 600 to 800°C. These high temperatures allow for removal of a lot of atoms that could potentially outgas into the volume of the thin film package. Even so, as illustrated in Table 1.3 most of these works only achieved pressures in the 100s of mTorr or Torr range. Candler et al. was able to achieve pressures below 7.5 mTorr with a packaging process in which the pressure inside of the package could be changed after packaging by in-diffusing or out-diffusion hydrogen at 300-400ºC. Candler et al. showed that nitrogen and even hydrogen at room temperature did not diffuse back into the package. They also reported on the vacuum integrity after 416 days of testing and showed good performance in their packaged resonators even after >600 cycles from -50 to 80ºC.

Table 1.3: Vacuum packaging results using the thin film packaging.

Author	Institution	Encap-sulation Material	Sealing Temp.	Sensor	Pressure	Leak Rate Data
[53, 138] R. Candler 2006	Stanford & Bosch	LPCVD Oxide	950ºC	Resonator	<7.5mTorr	416 Days
[47]K. Ikeda et al. 1990	Yokogawa Electric Corporation	Epitaxial Si	NR	Resonator	<50mTorr	-
[139] R. He 2007	UCLA	LPCVD Poly-Si	600ºC	Pirani Gauge	130 mTorr	-
[45] L. Lin et al. 1998	Berkeley	LPCVD Nitride	NR	Resonator	300 mTorr	-
[50] K. Lebouitz 1999	Berkeley	Poly-Si	835ºC	Resonator	600 mTorr	-
[56, 57] B. Stark 2004	University of Michigan	60Sn-40Bi Solder	>130ºC	Pirani Gauge	1.5 Torr	160 Days
[51] T. Tsuchiya 2001	Toyota	Silicon Nitride	NR	Resonator	3 Torr	~600 Days
[55, 140] R. Candler et al. 2003 & W.T. Park et al. 2006	Stanford & Bosch	LPCVD Oxide	NR	Resonator (Accelerometer)	5 Torr	-
[46] Guckel et al. 1986	University of Wisconsin	LPCVD Nitride	NR	Transducer	NR	-
[44] C. Mastrangelo et al. 1989	Berkeley	LPCVD Nitride	NR	Pirani Gauge	NR	-
[49] M. Bartek et al. 1997	Delft University, Netherlands	Poly-Si	575ºC	Micro-diode	NR	-
[49] M. Bartek et al. 1997	Delft University, Netherlands	Aluminum	150ºC	Micro-diode	NR	-
[58, 141] P. Monajemi 2006	Georgia Tech.	Polymer & Metal	200-300ºC	Resonator	NR	-

1.4.2 VACUUM ENCAPSULATION USING WAFER BONDING

Table 1.4 summarizes the vacuum packaging results achieved without using getters, using the wafer bonding approach. The materials used in wafer bonding techniques such as anodic, frit and solder bonding, often can not handle the same harsh cleaning procedures as the LPCVD films often used in the thin film encapsulation approach. Material such as frits, solders and electroplated metals also tend to outgas more than LPCVD films. Furthermore, in the case of wafer bonding, sealing takes place in a wafer bonder at 200 to 450ºC as opposed to an LPCVD furnace at 600-900 ºC. These lower temperatures do not facilitate as much outgassing before sealing—and therefore, they are susceptible to more outgassing after sealing. This is why, without using getters, pressures only as low as 0.5 and 1 Torr have been reported using anodic bonding [73, 142], 1 and 1.5 Torr using solder bonding [113, 114] and 0.15 Torr and 1.5 Torr using Frit Bonding [5, 114].

Table 1.4: Vacuum packaging results using wafer bonding, and no getters.

Author	Institution	Wafer/ Chip Level	Encap-sulation Material	Max. Proc. Temp. (°C)	Sensor	Pressure	Leak Rate Data
[80] H.Song 2000	Samsung Advanced Institute of Technology	Wafer	Glass Frit	450	Resonator (Gyroscope)	150 mTorr	-
[73] V. Chavan 2002	University of Michigan	Wafer	Glass-Si Anodic	N.I.	Capacitive Pressure Sensor	~0.5 Torr	-
[142] B. Lee 2003	Seoul National University, Korea	Wafer	Glass-Si Anodic	N.I.	Resonator	1 Torr	-
[113] E. Mottin 2001	LETI LIR, France	Wafer	Au-Sn Solder	N.I.	Bolometer	1 Torr	-
[114] D. Sparks 2001	Delphi Automotive Systems	Wafer	Solder	N.I.	Resonator (Gyroscope)	1.5 Torr	42 days
[143] Wolfgang 2006	Fraunhofer Institute for Silicon Technology	Wafer	Au-Si Eutectic	380-400ºC	Resonator	7.5-12 Torr	-
[144-146] M. Esashi 1994	Tokoku University, Japan	Wafer	Glass-Si Anodic*	400	Infrared and Capacitive Pressure	100-400 Torr	-
[102] Y. Mei 2002	University of Michigan	Wafer	Au-Si Eutectic	>363	None	NR	-

1.4.2.1 Applications of Getters in Micro-Packages

Table 1.5 summarizes the vacuum packaging results achieved with getters using the wafer bonding approach. Non-evaporatable getters (NEGs) were first investigated for micro-packaging in the 1990s [144-146]. Typically NEGs consist of sintered metal particles which are packaged or adhered onto one of the inside surfaces of a vacuum chamber or vacuum cavity. There are two main drawbacks for applications of NEGs for micro-packaging: 1) the need for assembling or depositing sintered metal particle into the micro-cavity and 2) these sintered metal particles can shift inside of the package, interfering with the operation of the MEMS device. To deal with the latter issue, Esashi et al. [144-146] used a configuration similar to the one shown in Figure 1.17. As illustrated, the NEGs are housed in a separate compartment in order to minimize the amount of these particulates which get on the MEMS device. As shown in Table 1.5, using NEGs, Esashi et al. reported vacuum pressures of 10 μTorr. Caplet et al. [147] used a similar configuration and measured a pressure of around 3 mTorr.

Table 1.5: Vacuum packaging results using wafer bonding and getters.

Author	Institution	Wafer/ Chip Level	Encap-sulation Material	Max. Proc. Temp. (°C)	Sensor	Getter	Pressure	Leak Rate Data
[144-146] M. Esashi 1994*	Tokoku University, Japan	Wafer	Glass-Si Anodic*	400	Infrared and Capacitive Pressure	NEG	10 uTorr	-
[5] D. Sparks 2003	Integrated Sensing Systems (ISYSS)	Chip	Glass Frit	N.I.	Resonator	Thin Film (NanogettersTM)	850 uTorr	-
[142] B. Lee 2003	Seoul National University, Korea	Wafer	Glass-Si Anodic	N.I.	Resonator	Thin film (Ti)	1 mTorr	40 Days
[147] S. Caplet	CEA-DRT LETI/LIR, France	Wafer	Glass-Si Anodic	350	Resonator	NEG	3 mTorr	-
[27-29] T. Schimert 2001	Raytheon Electronic Systems	Wafer	Solder	N.I.	Bolometer	N.I.	4 mTorr	~950 Days
This Work	**University of Michigan**	**Wafer**	**Au-Si Eutectic**	**390**	**Pirani Gauge**	**Thin Film (NanogettersTM)**	**1-16 mTorr**	**1000 Days**
[148] News Release	Innovative Micro Technology IMT	Wafer	N.I	N.I	N.I	Thin Film Getter	<10mTorr	N.I.
[94] Y.T. Cheng 2002	University of Michigan	Wafer	Glass-Al	Local-ized 800	Resonator	Ti/Au thin film	25 mTorr	392 Days
[149] B. Lee 2000	Seoul National University, Korea	Wafer	Glass-Si Anodic	N.I.	Resonant Accelerometer	Ti thin film	200mTorr	-
[113] E. Mottin 2001	LETI LIR, France	Wafer	Au-Sn Solder	N.I.	Bolometer	NEG	1 Torr	-

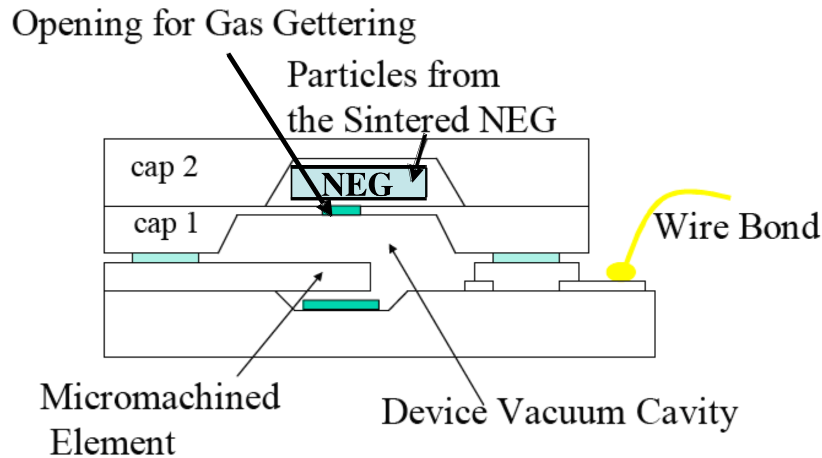


Figure 1.17: In application of NEGs, a separate compartment is often used to house the NEG getters [5].

An alternative to using NEGs is to sputter or evaporate a thin metal film such as Ti

which acts as the gettering material. As opposed to sintered metal particles, thin metal films can be easily deposited and photo-lithographically patterned. As a result, no special configurations are needed to physically separate the getter from the device. Such a thin film can be photo-lithographically formed inside of the micro-cavity for wafer-level packaging. ISSYS corporation first filed for a patent on May of 1999 describing the use of such a thin film getter and it was issued in December of 2002 [150]. It later published several papers reporting pressures as low as 850 μTorr [5, 6] and the application of this packaged getter for the packaging of its flow sensors [5, 6, 79]. ISYSS used glass frit bonding for encapsulation of their devices and a resonant sensor for measurement of vacuum. Researchers at Seoul National University and Samsung also used Ti thin films to achieve pressures as low as 1 mTorr [142, 149] using anodic bonding, where a resonator was used for vacuum measurement. In their study, the pressure was varied from 1mTorr to 1 Torr by varying the surface area of the deposited Ti [142]. Furthermore, the MEMS foundry Innovative Micro Technology (IMT) recently developed a vacuum packaging process for its customers and reports high yields at under 10 mTorr[148].

1.5 SUMMARY & MOTIVATION

The following sections summarize the demand for wafer-level packaging (Section 1.5.1), summarize currently published MEMS wafer-level packaging approaches (Section 1.5.2), and gives motivation for the work done in this dissertation (Section 1.5.3).

1.5.1 DEMAND FOR GENERIC WAFER-LEVEL PACKAGING

Section 1.2 (*MEMS Wafer Level Packaging*) motivated the use of wafer-level packaging, explaining its cost savings and the improved device reliability. Section 1.2.1.4 (*Vacuum/Hermetic Encapsulation & Protection from the Environment*), in particular, explained the physical motivation for vacuum/hermetically packaging MEMS devices. Table 1.6 shows the pressures desired for a number of applications that require vacuum. Most of the devices in Table 1.6 can be fabricated in standard CMOS processes that require temperatures of less than 400ºC. RF MEMS switches on the other hand often

use metals that soften at higher temperatures and therefore can be intolerant of temperatures higher than 200-300ºC. Also shown in Table 1.6 are the current market sizes and the predicted market sizes in 2011 for these MEMS applications [4]. As illustrated, the devices which require or can benefit from vacuum are predicted to represent an approximate $3.1 billion market in 2011.

Table 1.6: Desired vacuum packaging pressures for a number of applications. Also included are the market sizes of each of those applications [4].

	Desired Vacuum Pressure	Current Market Size	2011 Market Size
RF MEMS (Resonators and Switches)	1 mTorr to 760 Torr [30, 31]	$160M	$820M
Accelerometers (Resonant/ Piezoelectric/Capacitive)	100 mTorr to 760 Torr	$780M	$1,400M
Gyroscopes	1-10 mTorr [51, 151]	$620M	$920M
IR MEMS*	1-10 mTorr [27-29]	-	-
Total	**-**	**$1560M**	**$3,100M**

*No good market data

1.5.2 CURRENTLY AVAILABLE TECHNOLOGIES

Given this market demand, quite a few technologies have been developed to provide wafer-level vacuum packaging solutions. These were detailed in Section 1.3 (*MEMS Wafer Level Encapsulation Approaches*) and Section 1.4 (*Previous Work in MEMS Vacuum Encapsulation*). Table 1.7 lists some of the most impressive vacuum packaging results presented in the literature (a more comprehensive list was provided in Section 1.4). In all of these works, pressures below 10 mTorr were achieved. In Table 1.7, for each packaging process, the metrics defined in Table 1.1 (listed at the beginning of the chapter) for achieving a *wafer-level vacuum packaging* process are shown and areas are highlighted where the packaging process does not meet one of these metrics. As illustrated, one of the major issues is process compatibility. For instance Esashi et al. [144-146] and Candler et al.'s [53, 138] processes can only be applied to devices that can be fabricated in certain process flows. The other major issue was the lack of detail presented in many of these works. This is generally the case for companies that publish their packaging work since they are interested in protecting their intellectual property

(IP). In particular, in Schimert et al.'s work [27-29], not only was it be difficult to determine if all of the metrics were met, it would be extremely difficult to recreate their work from their published papers.

Table 1.7: Highlights of applicable packaging process from the literature showing how they fit the metrics defined here needed for a *wafer-level vacuum packaging* process.

Author	Institution	Pressure	Metrics		
			Bond (Temperature ≤400ºC)	Electrical Connection/ Process Compatibility	Wafer Level Process
[144-146] M. Esashi 1994*	Tokoku University, Japan	10 uTorr	400ºC	Glass-Si Anodic (Can not bond over non-planar surfaces)	Wafer
[5] D. Sparks 2003	Integrated Sensing Systems (ISYSS)	850 uTorr	N.I. (Details not specified)	Glass Frit Bonding (OK)	Chip (not wafer-level)
[27-29] T. Schimert 2001	Raytheon Electronic Systems	4 mTorr	N.I. (Details not specified)	Solder (Details not specified)	Wafer
[53, 138] R. Candler 2006	Stanford & Bosch	<7.5mTorr	950ºC	Thin Film Packaging (Not a generic process)	Wafer
This Work (Au-Si Eutectic Bonding)	**University of Michigan**	**1-16 mTorr**	**390ºC**	**Au-Si Eutectic**	**Wafer**

1.5.3 MOTIVATION FOR AU-SI EUTECTIC BONDING & BACKSIDE LOCALIZED HEATING

Using *Au-Si eutectic wafer-level bonding for vacuum packaging,* devices can be packaged at a relatively low temperature (390ºC) in a *wafer-level vacuum packaging* process. Table 1.8 summarizes how the Au-Si eutectic bonding process developed in this work meets the metrics defined in Table 1.1 for a *wafer-level vacuum packaging* process (listed at the beginning of the chapter). *Backside localized heating* on the other hand will allow for packaging processes like Au-Si eutectic bonding to be applied at temperatures from below 200ºC to below100ºC depending on the materials and geometries.

Table 1.8: How Au-Si eutectic bonding fits the metrics defined for *a wafer-level vacuum packaging process* (as defined in Table 1.1) that can be used on a broad set of MEMS devices.

Metrics	Description
Low temperature	Au-Si bonds can be facilitated at a relatively low temperature (≤390ºC), allowing for bonds to wafers fabricated in CMOS or CMOS like processes.
Electrical Connection	The Au-Si eutectic layer melts during bonding allowing for bonds over non-planar surfaces including electrical feed-throughs.
Wafer-level process	Bonds are conducted at the wafer-level so that all of the devices across a wafer get packaged at the same time.
Vacuum compatible	With the integration of Nanogetters™, vacuum pressures <10 mTorr can be achieved.

1.6 Contributions of this Thesis

The major contributions are:

- A comprehensive study on the mechanisms for a high yield, highly reliable wafer-level vacuum packaging process using Au-Si eutectic bonding for MEMS packaging.
    - A fully characterized, low temperature (≤390°C), eutectic wafer-level vacuum packaging process using the Au-Si eutectic system that allows for bonding to poly-Si and Au thin films allowing for wafer level packaging of a wide range of devices.
    - Detailed characterization and analysis of the Au-Si eutectic bond.
    - Comprehensive vacuum testing and methodology for achieving vacuum pressures below 10 mTorr using the Au-Si eutectic process.
    - A new vacuum Pirani gauge designed to measure a wide range of pressures from 760 Torr down to 1 mTorr.
- A new wafer-level localized heating technique called differential localized heating which allows for localized heating of bond rings while the device is only exposed to 25% to 50% of the bond ring temperature.

1.7 Organization of Thesis

The *Au-Si eutectic wafer-level vacuum packaging* process is detailed in Chapters 2 through 5 and a new technique called *backside localized heating* is introduced in Chapter 6.

More specifically, **Chapter 2** gives a detailed background on previous Au-Si eutectic

research and details the bond experiments conducted. From these bond experiments a bond recipe and process design rules are given. Chapter 3 presents the fabrication process for Au-Si eutectic bonding including the cap wafer fabrication and device wafer fabrication. **Chapter 4** presents the design of a new Pirani (vacuum) sensor tailored specifically for characterization of vacuum packages. In **Chapter 5**, the vacuum sensors developed in Chapter 4 were applied for measuring vacuum pressures in the Au-Si eutectic bonding process.

Chapter 6 introduces, analyzes and demonstrates a new wafer-level localized heating approach. Finally, **Chapter 7** concludes the dissertation and suggests future work.

CHAPTER 2

AU-SI EUTECTIC WAFER BONDING

As detailed in Chapter 1, wafer-level packaging technologies are required for a wide range of MEMS devices. Depending on the operating frequency, the geometry and/or the design of the device to be packaged, vacuum pressures ranging from 10 μTorr to 760 Torr can be required and for an even larger scope of devices, hermeticity (the requirement that outside atoms do not penetrate the package) is required. These strict requirements necessitate an excellent seal that is uniform not only across the bond ring, but across a full wafer of packaged part. Characterization of a wafer-level vacuum packaging process is therefore very important.

In this chapter, Au-Si eutectic bond experiment results are presented along with the requirements for achieving a uniform and strong bond. These requirements can be separated into 3 categories as shown in Figure 2.1. They include: a) the material requirements (Section 2.3), b) the bond recipe (Section 2.4), and c) considerations for the Au-Si eutectic viscous flow (Section 2.5). The *material requirements* mainly depended on which materials were selected on the device wafer. As summarized in Figure 2.1a, the device wafer bond ring materials included: un-doped poly-Si; heavily phosphorous doped poly-Si; and sputtered or evaporated Cr/Au. The requirements for the *bond recipe* are summarized in Figure 2.1b were vacuum was first applied, then the outgassing step was applied, then the bond force was applied and finally the bond temperature was applied. The amount of bond force and timing of the bond force turned out to be one of the more critical factors in this bond recipe. As summarized in Figure 2.1c, *Au-Si eutectic flow* during bonding also played an important role in the bond quality and in whether or not devices or other features (such as the getter) would survive the bonding process. As shown in Figure 2.1c, two different types of flow: compressive flow and lateral diffusion

were observed. As well, the etched cavity had an effect on the Au-Si eutectic later flow and in some cases the Au-Si eutectic flowed inside of this cavity, interacting with the getter.

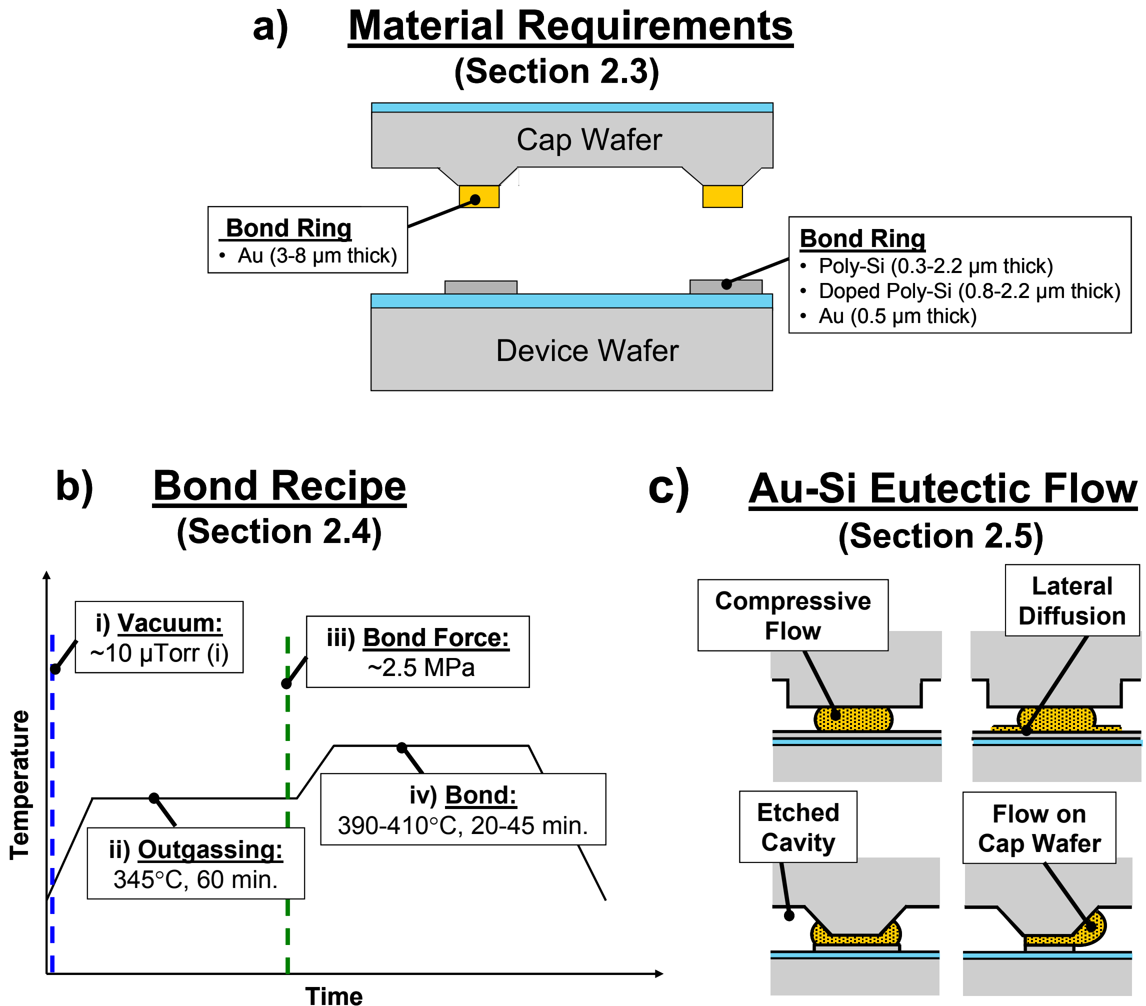


Figure 2.1: A summary of the three sets of bond issues discussed in this chapter for Au-Si eutectic bonding. They are a) the material requirements, b) the bond recipe and Au-Si eutectic flow.

Section 2.1 first gives a background on previous research conducted in Au-Si eutectic bonding for die attach and for wafer-level bonding. Section 2.2 then gives a *brief* description of the metrics for qualifying a uniform/strong bond (Appendix 1 gives a detailed description of these metrics). Section 2.3 details the material requirements (summarized in Figure 2.1b), Section 2.4 justifies the various steps in the bond recipe and Section 2.5 describes some of the ways in which the Au-Si alloy flowed and how this

flow could be controlled. Finally, Section 2.6 gives a brief summary of all of the bond test results.

2.1 BACKGROUND & PREVIOUS WORK

A eutectic reaction involves the formation of a liquid phase from two solid phases upon heating or conversely, the formation of two solid phases from a liquid phase upon cooling. In a binary phase diagram, the eutectic point is at the intersection of the two liquidus lines and is generally at a significantly lower temperature than the melting point of either pure material. Figure 2.2 shows the phase diagram for the Au-Si system [152, 153]. As illustrated, Si and Au have melting temperatures of 1412ºC and 1063ºC. Above the eutectic temperature (shown as 363ºC in Figure 2.2) at the eutectic composition of approximately 18.6±0.5 atomic % Si in Au the Au-Si alloy is in a completely liquid state. Although 363ºC is the generally accepted value for the eutectic temperature [152-155], other authors have measured it at slightly below 360ºC [156] and at 370ºC [157, 158].

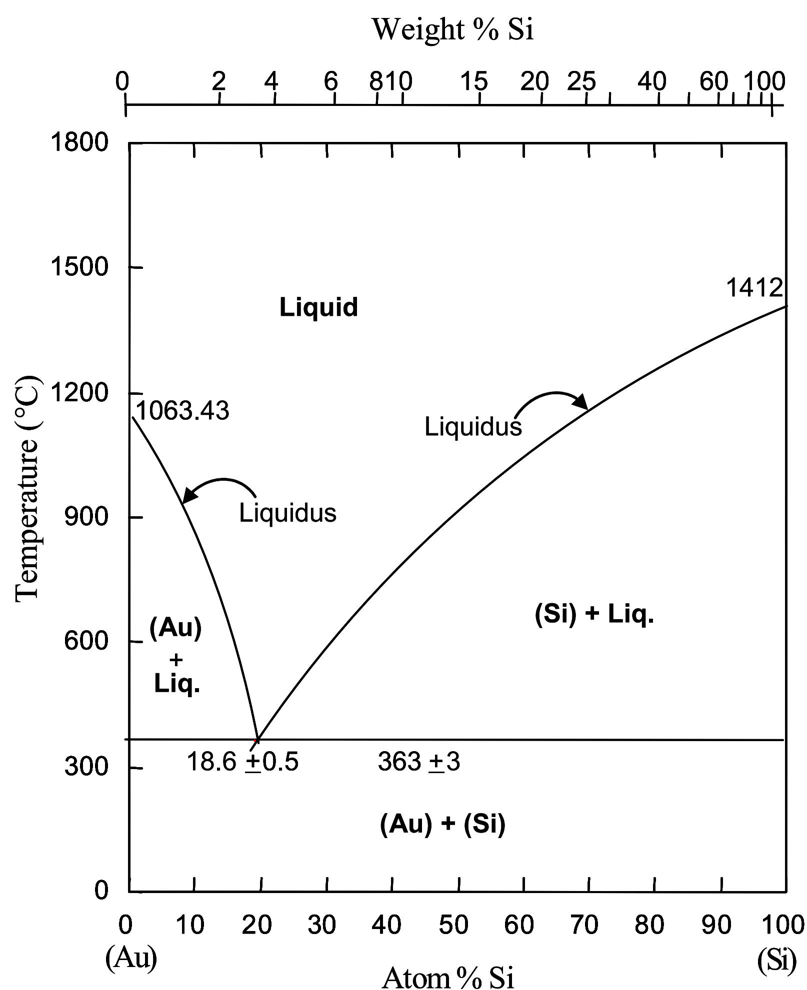


Figure 2.2: The Au-Si eutectic phase diagram [152].

Achieving this liquid state is desirable and/or necessary for strong die and wafer bonds because it conforms over topology and is highly reactive allowing for strong diffusional bonds to some materials. In Figure 2.2 at compositions less than ~18.6 atomic % Si in Au, at temperatures above the eutectic temperature but below the liquidus line, the Au-Si alloy is composed partially of Au-Si eutectic and partially of Au precipitates ((Au) + Liq.). Similarly, at compositions greater than ~18.6 atomic % Si in Au, at temperatures above the eutectic temperature but below the liquidus line, the Au-Si alloy is composed partially of Au-Si eutectic and partially of Si precipitates ((Si) + Liq.). The percentage of Au-Si alloy and that of either Si or Au precipitate depend on the % of Si in Au and on the temperature. This composition can be determined using the lever rule [159]. A detailed discussion on how the Au-Si alloy composition affects bond quality is presented in

Appendix 3.

One method to create such a Au-Si eutectic alloy is to deposit the correct amounts of Au and Si onto a wafer's surface and inter-diffuse them above their eutectic temperature. Another method for achieving this is to deposit the gold layer (with or without an adhesion layer between the gold and bulk silicon) on top of bulk silicon. When going above the eutectic temperature (~363º C), Si from the bulk diffuses into the gold until the eutectic composition is reached. This soft eutectic mixture acts as an adhesive layer, allowing for adhesion to other silicon or metallic surfaces. This method for achieving a Au-Si eutectic bond is generally called Au-Si eutectic bonding.

Understanding how this eutectic layer forms is important and as a result, the literature on Au-Si inter-diffusion and eutectic formation is substantial. In Section 2.1.1 various studies on Au-Si inter-diffusion are presented. This includes a discussion on Au silicide formation, SiO_2 formation on top of Au thin films and a discussion on the atomic structure of Au-Si alloys films. Section 2.1.2 then provides background on previous work done in *Au-Si eutectic bonding for wafer-level vacuum packaging*.

2.1.1 SILICON DIFFUSION INTO AU THIN FILMS

Reactions between Au and Si have been heavily studied because of the extensive use of Au-Si eutectic bonding in the die attach of ICs onto other surfaces such as PCBs. There are two methods generally used for implementation of this die attach method. The first involves placing a Au-Si eutectic preform (a thin film of the Au-Si eutectic mixture) between the IC chip and the surface that it gets mounted too and raising the temperature above the eutectic temperature in order to create a strong bond. Various authors have used this method for die attaching Si substrates [160, 161] and sapphire substrates (with either polysilicon, Au or no coating on the back surface) [100] and even transferring GaAs-AlGaAs structures onto Si substrates [162]. The second method involves depositing Au directly onto a Si surface on the backside of the IC chip and heating it to above the eutectic temperature so that Si diffuses into the Au film in order to create a soft Au-Si eutectic [163]. Samples are generally prepared by first removing the native oxide layer using a hydrofluoric acid (HF) etch and taking the wafers directly to the evaporator or sputter vacuum chamber for Au deposition. In some cases these sample were also

heated inside of the vacuum chamber or treated with an argon plasma in order to remove contamination. The pre-deposition HF etch was necessary because Si oxidizes almost instantaneously when in contact with oxygen—the resulting native oxide can cause bad Au adhesion. This method for die attach where Au and Si are inter-diffused to from a Au-Si eutectic is the most interesting for this work, since our films are formed in a similar manner.

2.1.1.1 Low Temperature Si Diffusion and Silicide Formation

For such die bonding using Au films deposited on a Si substrate, it would seem unlikely that strongly covalently bonded silicon atoms would diffuse out of a bulk Si substrate into the Au thin film at temperatures much lower than the melting temperatures of pure silicon. Several authors have studied how this occurs and how it subsequently enables the formation of Au-Si silicides (silicides are metastable inter-metallic compounds that often form at metallic film interfaces) [96, 97, 101, 156, 164-170]. Okuna et al. conducted experiments where Auger electron spectroscopy (AES) was used to measure the composition of Au films as they were deposited on a (111) oriented Si substrate [164, 165]. They found that films 2 monolayers thick could be heated up to 700ºC without any Au-Si reaction. On the other hand, films thicker than 5 monolayers thick inter-diffused during Au deposition at under 50ºC. Similar (though not as detailed) results were found for gold films on top of (100) oriented silicon substrates [171].

Hiraki suggests that this low temperature silicon diffusion is due to the larger availability of free electrons in thicker Au films allowing for Si atoms to break their strong covalent bonds [165]. Narusawa et al. [166, 167] took this study a step further observing a "diffuse interface" 45 and 20 monolayers thick between (110) and (111) orientated Si and Au which spontaneously forms upon deposition. Nakashimi et al. [167] discovered that in this "diffuse interface" region, metallic Si is formed. This metallic state is generally observed when the Si is in its liquid form and is characterized by a close packed lattice structure (as supposed to its semiconductor state which is characterized by a covalently bonded diamond lattice). The Si atoms are therefore more mobile when they are in their metallic state and can be easily "ejected," diffusing throughout the gold film at relatively low temperatures.

Such low temperature (even room temperature) diffusion through gold films has been evidenced by Au-Si silicide formation on top of Au thin films. Green and Bauer [168, 169] in fact studied Au-Si silicide formation on (100), (110) and (111) oriented silicon substrates for Au thicknesses from 100 Å to 1000 Å. On these substrates, silicide formation was observed and studied at temperature from 250ºC to 300ºC on the top of the Au surface. Such silicide formation was even observed at room temperature on the (111) oriented silicon substrate both at the Au-Si interface and on top of the Au thin film.

2.1.1.2 Oxide Formation on Au Thin Films

The fast diffusion of Si into Au at relatively low temperatures is convenient for the formation of the Au-Si alloy but also provides some challenges in that the Si in the Au-Si silicide readily oxidizes [97, 99, 165, 172-176]. Hiraki for instance observed that heating a 2000Å Au layer on a silicon substrate to 100ºC for 10 minutes resulted in a 1000 Å thick SiO_2 film [165]. This is remarkable in that such growth rates of thermal SiO_2 films on a bare silicon wafer generally requires temperatures in the 700-900 ºC range. The presence of an oxidizing atmosphere and subsequent oxidation in fact has been hypothesized to increase the diffusion of Si into Au [174]. These SiO_2 films that grow on gold surfaces can act as diffusion barriers and can result in non-uniform bonds or can completely disallowing bonds between the Au-Si eutectic layer and the surface it gets bonded too[160].

2.1.1.3 Structure of Au/Si Films after Intermixing

Several authors have also studied the structure of Au and Si at temperatures above and below the eutectic temperature and how this effects Si diffusion into Au [97, 98, 176-178]. Figure 2.3 shows tunneling electron microscope (TEM) photographs taken by Ma et al. [176] of a ~1400Å thick Au film deposited on a (100) silicon surface at 80ºC after sitting in air at room temperature. As illustrated in Figure 2.3a, after 60 days in air, an amorphous Au-Si layer was formed with traces of Au_4Si compound. Figure 2.3b shows that after 150 days, the Au_4Si layer grew further into the Si forming a much less uniform interface (the dotted line in Figure 2.3b shows where the original Au-Si interface was).

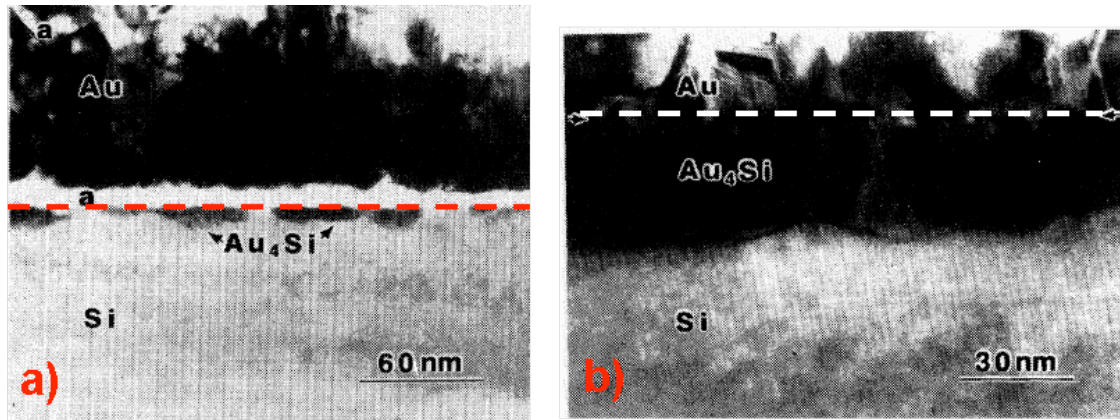


Figure 2.3: A ~1400Å thick film deposited on (100) Si at 80ºC that sat in air at room temperature for a) 60 days and the b) 150 days [176].

Chang et al. [97] took similar TEM photographs on 1500Å thick Au films deposited on (100) silicon surfaces which were subsequently annealed at 275, 300, 350 and 400ºC for 10 minutes in a nitrogen furnace. At 275 and 350ºC very limited Si-Au intermixing was observed whereas at 350ºC some Au_3Si compound formation was observed near the Au-Si interface. At 400ºC on the other hand, Si islands were observed to have grown epitaxially (which means that they have the same orientation and crystalline structure as the substrate) through the Au film. As well, much of the Au thin film was observed to have changed from its original poly-crystalline orientation, growing epitaxially in some places and forming the metastable compound Au_3Si in others. Chang et al. was surprised to observe only 7 atomic % Si in the Au film which according to the phase diagram in Figure 2.2 is well under the eutectic composition. Cros et al. [178] seems to observe similar phenomena. In their experiments, directly after deposition of a 3000Å film, the sample was immediately annealed at 415ºC for 20 minutes. As with Cheng et al., silicon islands were observed in the Au thin film as well as a stable epitaxial Au structure at the Au-Si interface. Next, this sample and another sample which had not been annealed at 415 ºC where heated to 250 ºC. Significantly more oxidation was observed in the sample that *had not* been annealed. Cros' assertion was that the formation of the epitaxial Au interface drastically reduced the Si out diffusion in the Au thin film.

In another interesting study, Waghorne et al. [179] studied the actual structure of the Au-Si eutectic above the eutectic temperature in its liquid state. They observed a close packed structure while in its liquid state. Of most interest for Au-Si eutectic bonding was

that they observed a 1 to 2% expansion of the Au-Si alloy upon solidification.

2.1.2 PAST WORK IN AU-SI EUTECTIC BONDING AT THE WAFER LEVEL

A handful of authors have studied Au-Si eutectic bonding for wafer bonding applications. Wolffenbuttel [101] conducted wafer bonding experiments between two Si wafers, each with 200Å/1000Å of Ti/Au on the front sides of the wafers in a dry oxygen or nitrogen flow at 400, 500, 600 and 800ºC. As expected, Wolffenbuttel found that in an oxygen environment, reliable bonds were not achieved. In vacuum he observed strong bonds at 800 ºC for bond times of 20 and 60 minutes but did not achieve strong bonds at 400ºC even with bond times as long as 60 minutes and could only achieve strong bonds at 500 ºC and 600 ºC for bond times of 60 minutes. Wolffenbuttel presumed that Ti acted as a diffusion barrier reducing the amount of diffusion of Si into Au. He propose that significant Si out diffusion could not be achieved until the silicidation temperature of Si/Ti was reached at around 520ºC. According to Wolffenbuttel's argument, for our application, a Si/Cr silicide would need to be formed in order to achieve significant out diffusion. This conflicts with our results since Cr was used as an adhesion layer for the bond experiments conducted in this work and Si/Cr silicides do not form at temperatures under 450ºC [43]—as will be reported in Sections 2.3 to 2.5, Si diffusion into Au *was* observed here resulting in repeatable bonds at temperatures of 390ºC to 410ºC.

One of the more relevant works was conducted by Mei et al. [102]. In 2002 Mei et al. observed the bond quality for gold-silicon eutectic bonds using the following material combinations: Si/Ti/Au to Si/Ti/Au; Si/Ti/Au to Si; Si/Ti/Au to Si/PolySi; Si/Ti/Au to Si/Oxide; and Si/Ti/Au to Si/Nitride. Of these, the bond quality and uniformity between Au-Au, Au-Si, and Au-PolySi was the best. As illustrated in Figure 2.4, Mei et al. demonstrated the vacuum integrity of bonds to flat 3500Å thick poly-Si thin films using a diaphragm which buckled inwards due to vacuum inside of the cavity. In 2006, Lee et al. used a similar method to create reference cavities for a capacitive absolute pressure sensor [180] using Au-Si eutectic bonding. Very little detail on the bonding process and bond quality was reported in this work. Also in 2006, as was summarized in Table 1.4 of Chapter 1, Wolfgang [143] at Fraunhofer Institute for Silicon Technology reported the use of Au-Si eutectic bonding where inertial sensors were packages and reliability test

data was taken. Wolfgang measured vacuum pressures from 7.5 to 12 Torr using resonators, but did not present any details on the process.

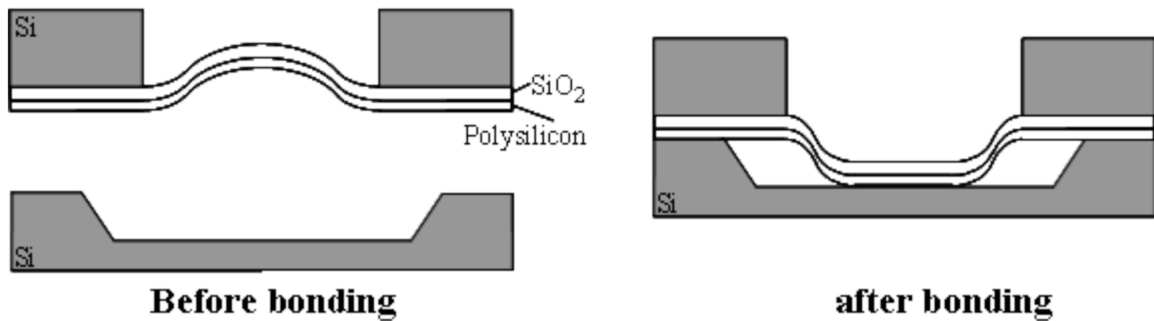


Figure 2.4: Illustrates the method in which Mei [102] used for characterizing vacuum packages.

2.2 Bond Characterization

The uniformity and strength of bonds in this chapter were determined using the razor blade test and the shear test. After bonding, wafers were partially diced (sawed) so that silicon caps were arrayed across the wafer as shown in Figure 2.5. The razor blade test is a destructive test technique which involves wedging off these bonded caps from the device wafer. The uniformity across the bond ring and across the wafer were then determined from inspection of the bond interface. The razor blade test could be applied quickly on bonded chips across the wafer. Using the razor blade test, it could be inferred whether or not a bond would result in a hermetic seal by whether or not either silicon transferred from the cap wafer to the device wafer or some of the thin films or the bulk silicon from the device wafer transferred to the cap substrate *for the entire circumference of the bond*. Figure 2.5b shows a case where silicon has tore from the cap wafer adhering to the device wafer for the entire circumference of the bond. A more detailed discussion of this test technique as compared to other available inspection techniques is detailed in Appendix 1.

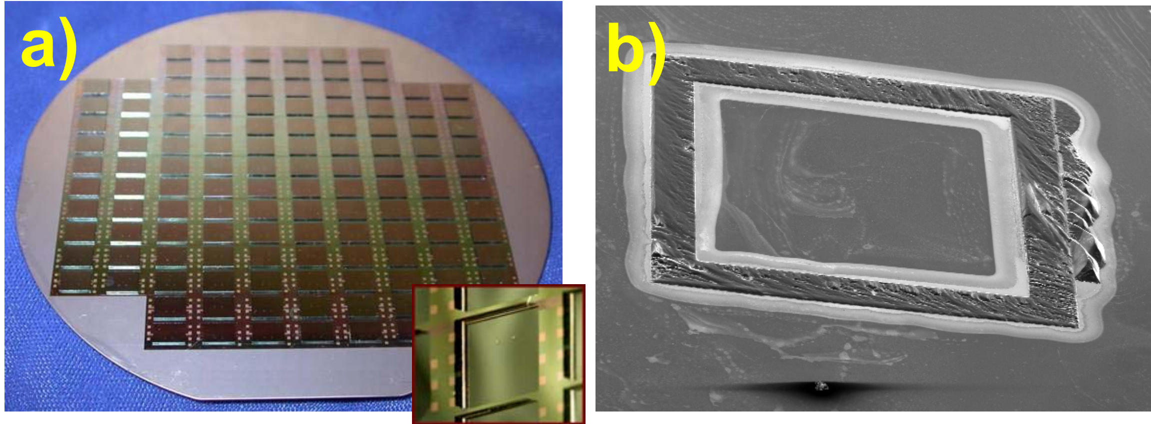


Figure 2.5: a) A picture where a wafer was partially diced so that caps were arrayed across the wafer, and b) a picture of a “dummy” device wafer substrate after a cap was torn off where Si tore for the entire circumference of the bond ring.

The shear test was useful because it was a quantitative method for measuring the strength of bonds. Using the shear test, caps were placed into a specially designed setup where a force was applied perpendicular to the face of the substrate as shown in Figure 2.6a. Figure 2.6b shows one of the caps sitting inside of the test setup where the slider, which applies the shear force, is pressed flush against the side of the cap. A more detailed description of this test setup and test methodology are presented in Appendix 1. Also detailed in Appendix 1 are the military specifications which for the bond areas used in this work specify shear strengths of >6.15 MPa and >12.3MPa as passing. For our bond experiments the more stringent >12.3MPa criterion was used.

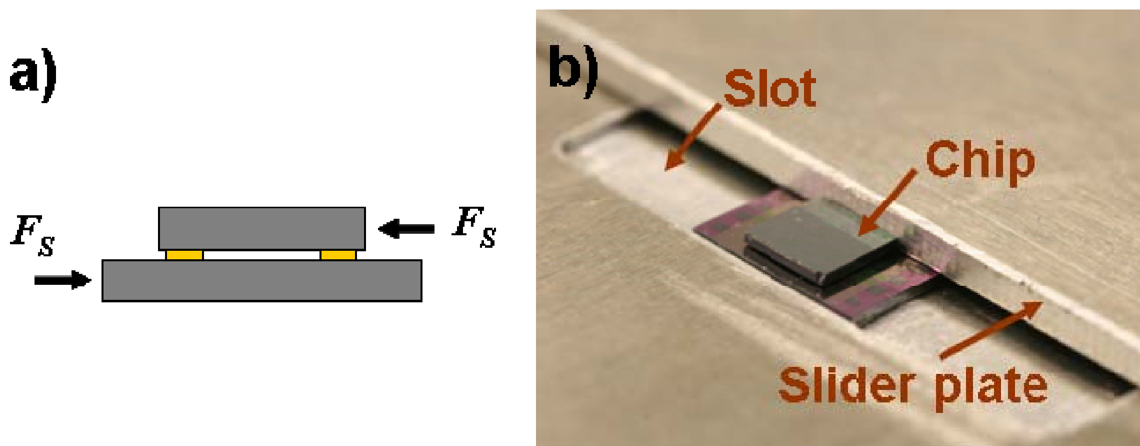


Figure 2.6: a) A schematic of how the shear force is applied and b) a picture of a diced package inside of the shear test setup.

SEM and EDX analysis, on the other hand, were used strictly for failure analysis and helped diagnose issues with the materials used and in the bond recipe.

Table 2.1 summarizes the bond characterization techniques and the criterion used for determining bond quality and bond strength. As explained in Chapter 1, these tests were only used for initial determination of bond quality—the hermeticity of bonds will be determined in Chapter 5 by their ability to hold vacuum.

Table 2.1: Summary of the test techniques and criterion used for determining hermetic/strong bonds.

Test Result	Test Method	Pass Criterion
General Quality	Razor Blade Test	Silicon transferred from cap to device wafer or thin film or silicon transferred from device to cap wafer for entire circumference of the bond
Strength	Shear Test	Shear strength of >12.3 MPa
Failure Analysis	SEMS & EDX	-

2.3 MATERIAL REQUIREMENTS FOR AU-SI EUTECTIC BONDS

This section reports some of the specific requirements for material selection in conducting Au-Si eutectic bonding. Most of the material requirements in executing a uniform/strong bond involved the bond ring material on the device wafer.

Section 2.3.1 first presents the fabrication process for the wafers used for bond experiments. Section 2.3.2 then presents a short discussion on thin film stack that makes up the bond ring on the cap wafer. Finally, bond results are presented for bonds to un-doped poly-Si (Section 2.3.3), heavily phosphorous doped poly-Si (Section 2.3.4) and Cr/Au (Section 2.3.5).

2.3.1 WAFER FABRICATION FOR BOND EXPERIMENTS

Chapter 3 will outline the full Au-Si eutectic bonding process used for device encapsulation. Most of the initial bond experiments conducted in this chapter were fabricated in a significantly simplified version of the process used for device encapsulation. The following sections outline the cap wafer fabrication (Section 2.3.1.1), the "dummy" device wafer fabrication (Section 2.3.1.2) and the wafer preparation for bond experiments (Section 2.3.1.3).

2.3.1.1 Cap Wafer Fabrication for Bond Experiments

Figure 2.7 summarizes the configurations used for the cap wafers used in bond experiments. For fabrication of these wafers, directly after a short buffered hydrofluoric acid (BHF) etching step, 200/5000 Å angstroms of chromium/gold was evaporated on top of bulk silicon using an E-beam Enerjet evaporator at $\sim 2\times10^{-6}$ Torr. The BHF dip preceding the evaporation step was to ensure that the Cr/Au layer was directly in contact with the bulk Si and that a thick native oxide would not prevent inter-diffusion. Generally the wafers were inside of the evaporation vacuum chamber within 15 minutes of the BHF dip. A 15 minute exposure to air should result in approximately 2 Å of oxide [181]. This layer acted as the ***seed layer*** for electroplating.

Next, 10 to 20 microns of AZ 9260 photoresist was deposited and patterned, acting as a mold for the Au electroplating. Electroplating was done using BDT-510 makeup plating solution with a stainless steal cathode on one side of the bath and the wafer on the other side serving as the anode. A current source was used to supply the source current with the cathode attached to the positive side and clips touching the top of the wafer were connected to ground. A current density of $2mA/cm^2$ resulted in a plating rate of around 0.1 µm per minute (the wafers with 300 µm wide bond rings for example had an exposed surface area of $\sim 3.75\ cm^2$ and therefore a supply current of 7.5mA was used). For the device bonds, the electroplated thicknesses ranged from 3 to 8 µm. Half of the electroplating was done with the electrodes connected near the wafer flat and the other half with the wafer flipped around and the electrodes connected near the top edge of the wafer. In some cases, failing to flip the wafers midway through electroplating resulted in bond rings which were 20% thicker near where the electrodes were connected as compared to those on the farthest edge. Flipping the wafers half way through the electroplating process resulted in bond rings with an average bond ring thickness that was consistent across the wafer to with in ±5-10%.

As shown in Figure 2.7b, for some of the bond experiments a cavity was anisotropically etched using Potassium Hydroxide (KOH). This was done by first conducting a 30 second etch in 10:1 H_2O:HF and then placing them in a KOH bath at 90ºC. This resulted in a ~1.1 µm per minute etch rate. Sixty to ninety micron cavities were etched resulting in the sloped sidewalls shown in Figure 2.7b. Because the Cr and

Au are inert to both HF and KOH, they did not need to be masked during this process step. As shown in Figure 2.7c, in other wafers, deep reactive ion etching (DRIE) was used for patterning of the cavities. In these cases, a 10 micron AZ 9260 photoresist was patterned over the bond rings and 90 µm cavities were etched using an STS Multiplex ICP DRIE.

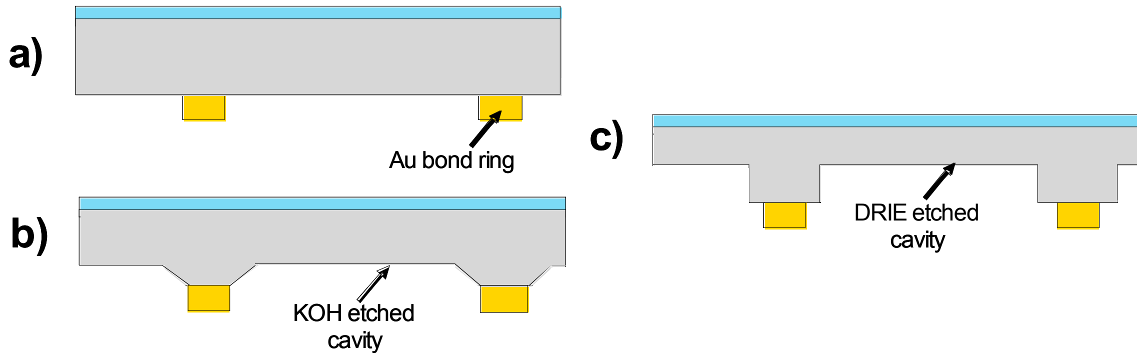


Figure 2.7: Schematics of the cap wafer configurations used for bond experiments in Chapter 2 showing: a) a cap wafer without an etched cavity, b) a cap wafer with a KOH or TMAH etched cavity and c) a cap wafer with a DRIE etched cavity.

2.3.1.2 "Dummy" Device Wafer Fabrication

Figure 2.8 summarizes the materials and configurations used for the "dummy" device wafers used for bond experiments in this chapter. For these wafers, a dielectric layer was deposited followed by the layer to be bonded to (i.e. the *bond-to* layer). The dielectric layer consisted of either 19000 Å of thermal SiO_2 or a 19000Å/3000Å SiO_2/Si_3N_4 stack (with LPCVD deposited Si_3N_4). The latter most closely resembled the material sets in the bond processes which will be outlined in Chapter 3 used for device encapsulation. The *bond-to* layers experimented here were poly-Si and Cr/Au thin films of varying thickness. Poly-Si layers 0.3, 0.8 and 2.2µm thick were deposed and in some cases the bond ring was patterned to 50, 150, 300 or 500µm and in other cases the poly-Si was not patterned at all. Also, in some cases these poly-Si thin films were heavily phosphorous doped. These different configurations are summarized in Figure 2.8a.

For the bonds to Au thin films, a 500/5000 Å Cr/Au thin film was evaporated in an Energet Evaporator or sputtered using an Enerjet Sputter Coater. In some cases the bond ring was patterned to 100, 150 or 300 µm and in other cases the Au was not patterned at

all. These configurations are summarized in Figure 2.8b.

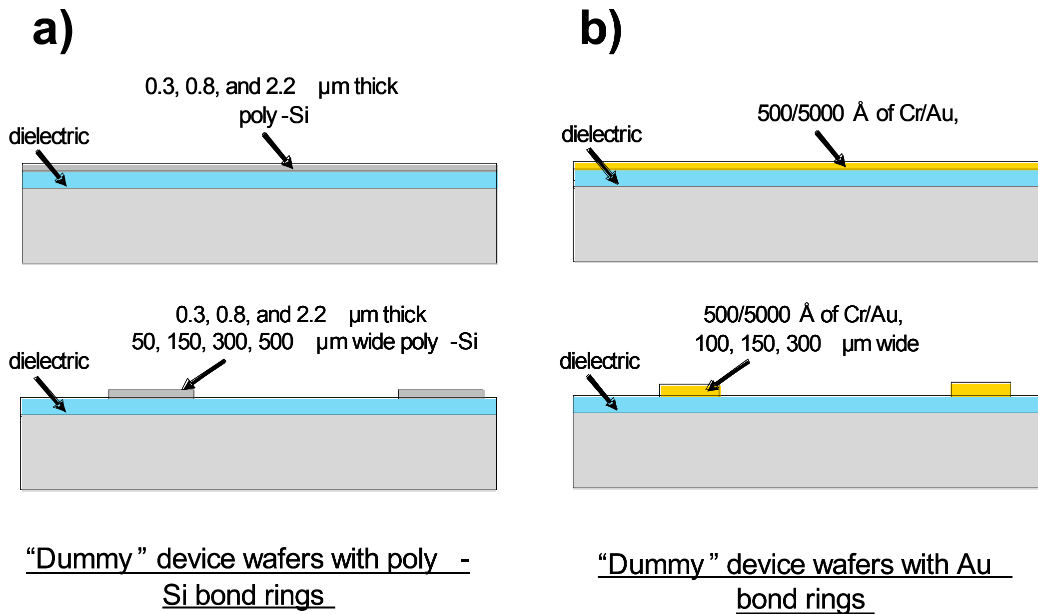


Figure 2.8: Schematics of the different "dummy" device wafer configurations for bonds to poly-Si and Au.

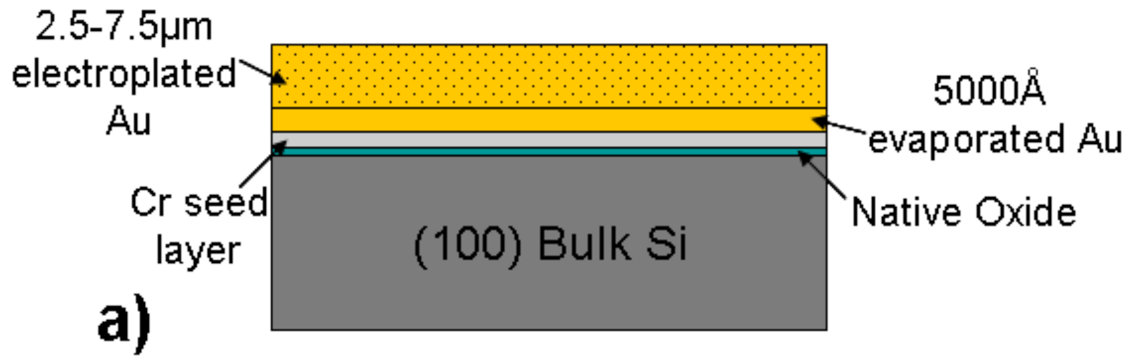
2.3.1.3 Wafer Preparation for Bond Experiments

Directly before each bond, both the cap wafer and "dummy" device wafer were Piranha cleaned (an aggressive chemical clean where the wafers are dipped in an approximately 1 to 1 mixture of sulfuric acid and hydrogen peroxide) for 10 minutes in order to remove organic particles that could compromise the bond quality. For the "dummy" device wafers with poly-Si thin films, after the Piranha clean, the wafers were dipped in BHF in order to remove the native oxide. Bonds were conducted anywhere from several minutes to several hours after this wafer preparation.

In cases where the "dummy" device wafer was patterned, the bond rings on the cap wafer needed to be aligned to these bond rings on the "dummy" device wafer. This was done using a SUSS microTec SB6 wafer alignment system. This alignment system allowed for alignment tolerances anywhere from ±5 to ±100 μm. After the alignment, the wafer which were then clamped into the alignment chuck, where transferred into either the SUSS microTec SB6 or SB6e bond chamber for bonding. More details on this bond chuck and bond chamber are presented in Appendix 2.

2.3.2 A DISCUSSION ON THE CAP WAFER BOND RINGS

One difference in our application as supposed to many of the studies presented in section 2.1 (*Background & Previous Work*) is that in those studies Au was deposited directly on top of the Si substrate. In our application, a 200 Å thick Cr layer was used as an adhesion layer for a 5000 Å thick evaporated Au thin film to ensure excellent adhesion to any native oxide that formed on the surface of the Si wafer. On top of those films, a 3-8µm thick electroplated Au layer was deposited and then etched back by 5000Å (as described in the previous section). As illustrated in Figure 2.9a, this means that Si needs to diffuse through a ~ 2 Å native oxide (the approximate amount of oxide that grows in 15 minutes on a bare (100) oriented silicon wafer [181]) and a 200Å Cr layer to intermix with the evaporated and electroplated Au films.



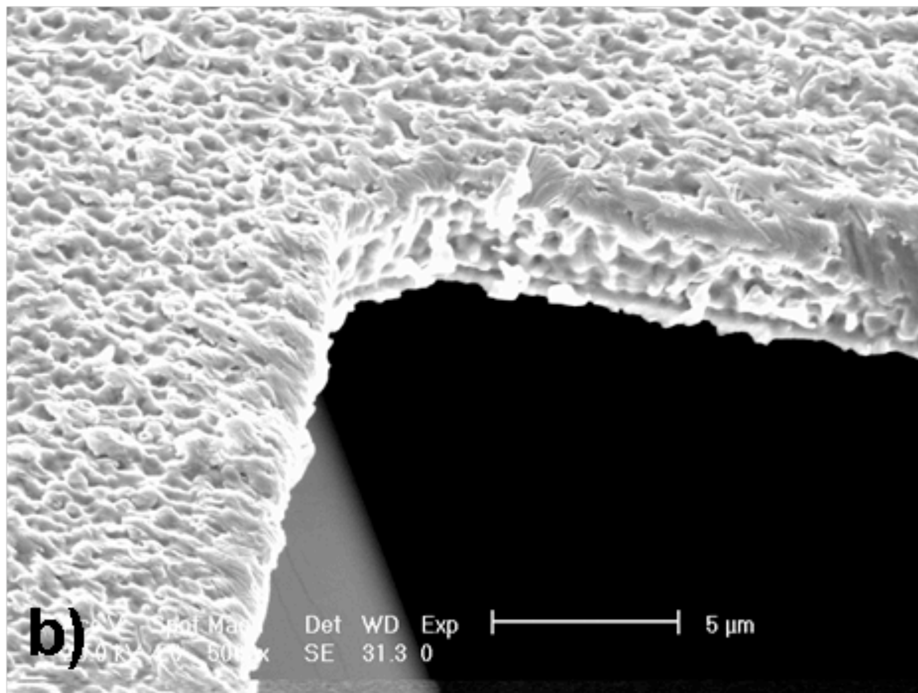


Figure 2.9: a) Schematic of the thin film stack where a native SiO_2 and a Cr layer act as a potential diffusion layer for between the Si and the Au and b) an SEM of the rough electroplated Au layer.

The native SiO_2 and Cr layer do in fact seem to reduce the amount of silicon out diffusion into the Au layer at low temperatures. As was explained in Section 2.1.1.2, a 10 minute exposure at 100 ºC can result in a 1000Å thick SiO_2 layer on top of an evaporated gold film deposited directly on top of a bulk Si layer. In experiments conducted here, evaporated 200Å/5000Å Cr/Au films were heated up to ~315ºC in air for 10 minutes without noticeable discoloration. Furthermore, the wafers were placed on a probe station and probes were placed in contact with the surface of the Au. A multimeter was used to indicate a *short* circuit. This indicated that if there was SiO_2 formation on

this surface, it was not significant—certainly not 1000Å thick. At around 350ºC on the other hand, heating the wafer for several minutes caused it to become "cloudy." This time, probing the wafer with probes from a probe station, a multimeter was used to indicate an *open* circuit. Although not conclusive, these experiments seem to indicate that SiO_2 formation on top of the Au film is not a serious issue until the temperature is raised to near eutectic temperature.

2.3.3 BONDS TO UN-DOPED POLY-SI

There were no processing issues specific to bonds to un-doped poly-Si films. Therefore, only bond results for uniform/strong bonds are presented in this section. There were in fact quite a few bonds to un-doped poly-Si that were problematic. Those technical issues applied for other material sets as well for bonds to un-doped poly-Si and were either caused by the bond recipe or by Au-Si eutectic flow. Those bond results are therefore discussed in Section 2.4 (*The Bond Recipe for Au-Si Eutectic Bonds*) and Section 2.5 (*Au-Si Eutectic Lateral Flow*). All of the bonds described in this section were between a cap wafer with a 300µm wide Au bond ring and a device wafer with either a 0.3 µm or 2.2 µm thick un-doped poly-Si thin film. For each case, the poly-Si film on the "dummy" device wafer was not patterned. Figure 2.10 summarizes the dimensions of the thin films used in these bond experiments.

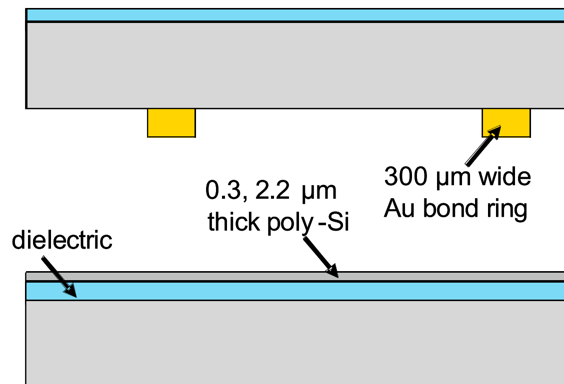


Figure 2.10: The dimensions of the films for bonds from the experiments shown in Table 2.2.

Table 2.2 shows all of the key parameters for these bonds. All of the bonds in Table

2.2 were determined to be high quality by the razor blade test, where bulk Si tore from the cap wafer, adhering to the device wafer for the entire surface area of the bond ring. As illustrated in Table 2.2, quality bonds were demonstrated with and without an intermediate temperature step up to 60 minutes long and at bond temperatures of 410ºC for 40 minutes and 395ºC for 15 to 45 minutes. As also illustrated in Table 2.2, successful bonds were demonstrated with Au bond rings on the cap wafer of 3 to 6 µm thick at bond pressures of 2.1 MPa and 2.7 MPa (1000N and 1300N of force). Bonds using larger and smaller bond forces than these resulted in less consistent results and will be discussed in Section 2.4 (*The Bond Recipe for Au-Si Eutectic Bonds*).

Table 2.2: Summary of hermetic/strong bonds to poly-Si thin films which passed the razor blade test. All of these bonds were with 300 µm wide bond rings.

Au-Si to poly-Si (0.3, 2.2 µm) bond								
Bond #	**Cap Bond ring Thick-ness**	**Poly-Si Thick-ness**	**Bonder**	**Intermediate Temperature Step**	**Bond Temperature Step**	**Bond Force**	**Cavity**	**Pass the Shear Test?**
22	6µm	0.3 µm	EVG	265ºC, 60min	395ºC*, 30min.	2.7MPa (1000N)	-	-
24	3µm	0.3 µm	EVG	265ºC, 40min.	395ºC*, 20min.	2.7MPa (1000N)	-	-
25	5µm	0.3 µm	EVG	-	395ºC*, 40min.	2.7MPa (1000N)	-	-
30	3.5µm	0.3 µm	EVG	-	395ºC*, 15min.	2.7MPa (1000N)	-	-
36	3.5µm	0.3 µm	EVG	-	395ºC*, 40min.	2.7MPa (1000N)	-	5/5 (15.0-20.3 MPa)
39	3µm	0.3 µm	EVG	-	395ºC*, 40min.	2.7MPa (1000N)	-	5/5 (15.0-27.8 MPa)
55	3µm	0.3 µm	EVG	-	395ºC, 45min.	2.7MPa (1000N)	DRIE	-
109	4µm	2.2 µm	SB6e	-	410 ºC, 40min.	2.1MPa (800 N)	-	5/5 (13.0-19.7 MPa)

As summarized in Table 2.2, in the shear tests for wafers #36, #39 and #109 all of the chips tested passed with shear strengths ranging from 13.0 MPa to >27.8 MPa. Tables 2.3, 2.4 and 2.5 show the details of the shear test results from these bonds. As illustrated, for nearly all of the samples from bond #36, #39 and #109, the type of failure is listed as "sheared in the cap or device substrate" which as described in Appendix 1 means that they did not break near the bond ring interface—and as a result the bond interface could not be inspected after the shear test.

Table 2.3: Shear test results for bond #36.

Shear Test Results (Bond #36)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C3-R14	15.0	Sheared in cap or device substrate	Pass
C3-R10	21.3	Sheared in cap or device substrate	Pass
C4-R8	16.6	Sheared in cap or device substrate	Pass
C8-R6	19.7	Sheared in cap or device substrate	Pass
C5-R4	15.0	Sheared in cap or device substrate	Pass
Average Strength: 17.5 MPa			
Standard Deviation: 2.9 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table 2.4: Shear test results for bond #39.

Shear Test Results (Bond #39)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
Unknown	26.1	Sheared in cap or device substrate	Pass
Unknown	15.0	Sheared in cap or device substrate	Pass
Unknown	26.1	Sheared in cap or device substrate	Pass
Unknown	24.5	Sheared in cap or device substrate	Pass
Unknown	>27.8	Not enough force applied for failure	Pass
Average Strength: 23.9 MPa			
Standard Deviation: 5.1 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table 2.5: Shear test results for bond #109.

Shear Test Results (Bond #109)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
Unknown	13.4	Sheared in cap or device substrate	Pass
Unknown	15.0	Sheared in cap or device substrate	Pass
Unknown	19.7	Sheared in cap or device substrate	Pass
Unknown	19.7	Sheared in cap or device substrate	Pass
Unknown	19.7	Sheared in cap or device substrate	Pass
Average Strength: 17.5 MPa			
Standard Deviation: 3.1 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

2.3.4 BONDS TO PHOSPHOROUS DOPED POLY-SI

Most of the bonds in the previous section (Section 2.3.3) where done to 0.3 μm thick un-doped poly-Si. All of the bonds described in this section were between a cap wafer

with a 300μm wide Au bond ring and a device wafer with either a 0.8 μm or 2.2 μm thick poly-Si thin film. In almost all of these bond experiments, the thicker poly-Si layer was *heavily phosphorous doped*. In this section some specific issues involving bonds to heavily phosphorous doped poly-Si films are presented as well as methods for addressing those issues.

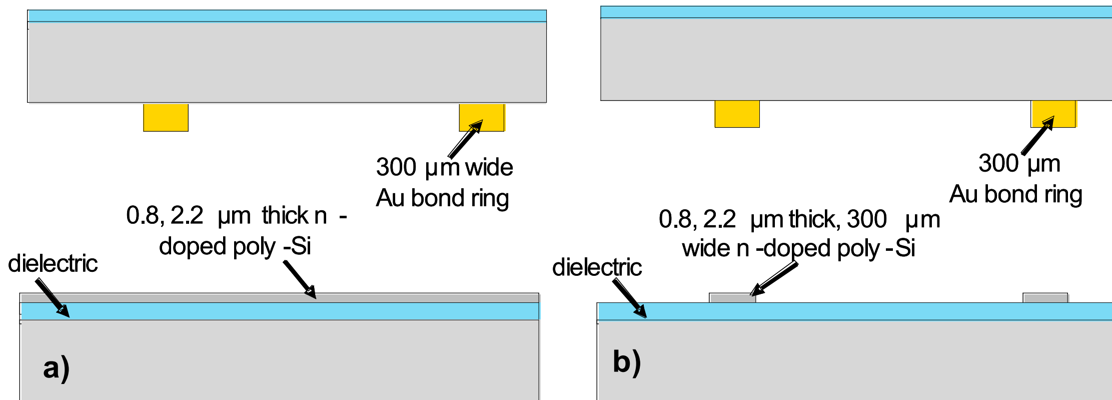


Figure 2.11: The dimensions of the films for bonds from the experiments shown in a) Table 2.6 and b) in Table 2.8.

In an earlier presentation of this work done in 2005, it was hypothesized that bonds to films thicker than 0.3 μm were problematic [104, 119]. In those publications two problems were observed: a more significant lateral flow of the Au-Si alloy and a breaking of the underlying poly-Si at the interface between the poly-Si and the underlying dielectric. Since then, more experiments have been conducted and as will be explained, the heavily phosphorous doping of these poly-Si layers *seems* to cause these phenomena. Table 2.6 shows several bonds conducted to both 0.8μm and 2.2μm thick poly-Si thin films. For each case, the poly-Si film on the "dummy" device wafer was not patterned. Figure 2.11a summarizes the dimensions of the thin films used in these bond experiments.

Bonds #31, #34, and #108 resulted in significant lateral flow of the Au-Si alloy. Figure 2.12a shows the results of one of these bonds after the wafers were pried apart using a razor blade. The dark areas in the figure are where poly-Si tore off the SiO_2 on the device wafer adhering to the cap wafer. Figure 2.12b illustrates this phenomenon schematically, showing poly-Si torn away, adhering to the Au-Si eutectic on the cap

wafer. It is evident from Figure 2.12a that the Au-Si eutectic spread laterally several millimeters during bonding. It is not evident why these heavily phosphorous doped poly-Si films appear to encourage lateral flow of the Au-Si alloy. One potential explanation is that the presence of phosphorous changes the surface tension or some other property of the Au-Si alloy. Furthermore, as evident in Figure 2.12, all of the bond rings across the wafer were easily pulled apart simultaneously when the wafers were pried apart. This qualitatively indicated a very weak bond.

Table 2.6: Bond parameters for bonds conducted between a Au-Si bond ring and a 0.8μm and 2.2 μm thick Poly-Si film on a device wafer that was not patterned.

Au-Si to poly-Si (0.8, 2.2 μm) bonds										
Bond #	**Cap Bond Ring Thick-ness**	**Poly-Si Thick-ness**	**Device Bond Ring Width**	**Bonder**	**Inter-mediate Temp. Step**	**Bond Temp. Step**	**Bond Force**	**Cavity**	**Au-Si Flow**	**Bond Strength**
31	8μm	0.8μm n-doped	No pattern	EVG	-	395℃, 15min.	2.7MPa (1000N)	-	Flow	Very weak
34	2μm	0.8μm n-doped	No pattern	EVG	-	395℃, 40min.	2.7MPa (1000N)	-	Flow	Very weak
108	4μm	2.2μm n-doped	No pattern	SB6e	-	410℃, 40min.	2.1MPa (800 N)	-	Flow	1/5 (9-15MPa)
109	4μm	2.2μm	No Pattern	SB6e	-	410℃, 40min.	2.1MPa (800 N)	-	None	-

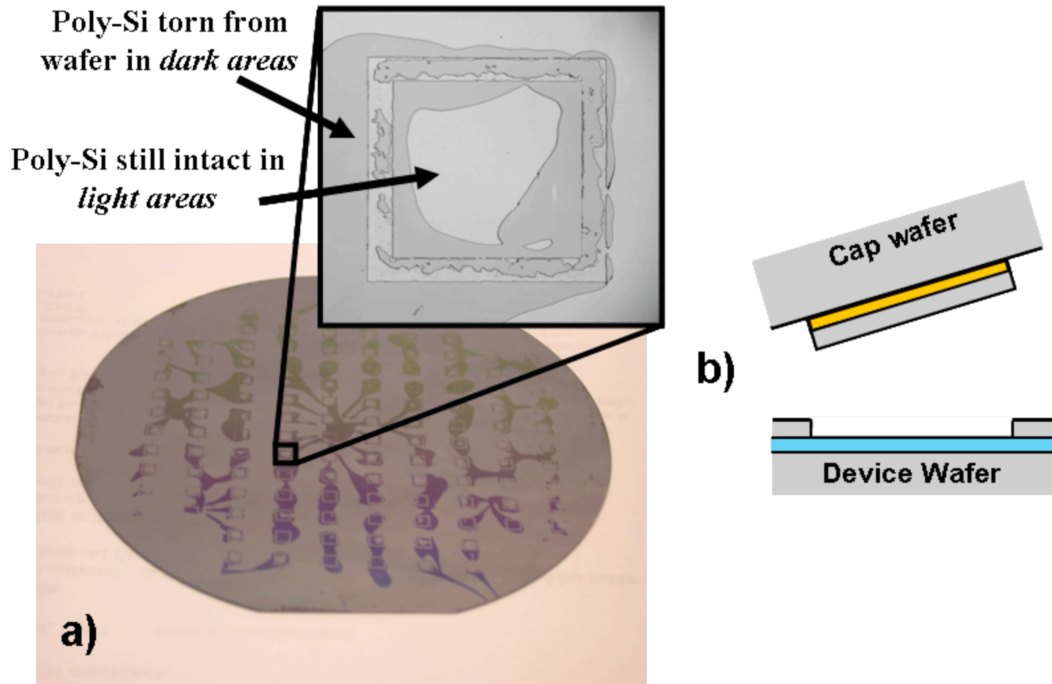


Figure 2.12: a) Photograph of the "dummy" device wafer after pulling the two bonded wafers apart for bond #31 and b) a schematic showing how the poly-Si was pulled of off the underlying dielectric.

Bond #108 stayed well enough intact that chips could be diced allowing for the shear test to be applied. As summarized in Table 2.6, for bond #108 only 1 out of 5 of the packages passed the shear test with shear strengths ranging from 9 to 15 MPa. Table 2.7 shows the details of the shear test results from this bond. Inspecting samples after the shear test, it was evident that poly-Si tore from the device wafer adhering to the cap wafer in the same manner described above and illustrated in Figure 2.12.

Table 2.7: Shear test results for bond #108.

Shear Test Results (Bond #108)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C10-R8	10.2	Sheared in bond ring	Fail
C5-R13	15.0	Sheared in bond ring	Pass
C2-R8	8.7	Sheared in bond ring	Fail
C5-R1	10.2	Sheared in bond ring	Fail
C6-R8	10.2	Sheared in bond ring	Fail
Average Strength: 10.9 MPa			
Standard Deviation: 2.4 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

As a control experiment in Table 2.6, the 2.2 µm thick poly-Si "dummy" device wafer in bond #109 was not phosphorous doped (this bond was also presented in the previous section in Table 2.2). This resulted in a bond in which there was no evidence of any lateral flow and where bulk Si tore from the cap wafer adhering to the device wafer. In shear test results that were detailed in Section 2.3.3 (in the previous section) shear strengths of 13 to 19.7 MPa were achieved where all of the packages passed the shear test. This *seems* to indicate that the excess lateral flow and weakened bond joints in bonds #31, #34 and #108 were due to the heavy doping of the poly-Si layer.

In an attempt to stop lateral flow of the Au-Si alloy in bonds to phosphorous doped films, a number of bonds were conducted where the poly-Si *bond-to* layer was patterned to the same dimensions or to within 200µm of the dimensions of the cap wafer bond ring. Figure 2.11b summarizes these device dimensions and Table 2.8 shows the parameters for these bond experiments. Figure 2.13 shows a bond ring from bond #101 after the cap was torn off using the razor blade test. As illustrated, the 2.2µm thick poly-Si film de-adhered from the device wafer, adhering to the cap side.

Table 2.8: Bond parameters for bonds conducted between a Au-Si bond ring and a 0.8μm and 2.2 μm thick Poly-Si film on the device wafer where the device wafer was patterned to the same dimensions as the cap wafer or to within 100μm of the cap bond ring dimensions.

Au-Si to poly-Si (0.8μm, 2.2 μm) bonds									
Bond #	**Cap Bond Ring Thick-ness**	**Poly-Si Thick-ness**	**Device Bond Ring Width**	**Bonder**	**Inter-mediate Temp. Step**	**Bond Temp. Step**	**Bond Force**	**Cavity**	**Bond Strength**
38	8μm	2.2μm n-doped	500	EVG	-	395°C, 45min.	2.7MPa (1000N)	-	5/5 (20->28MPa)
87	5μm	0.8μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	-	-
93	4.5μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	-	-
101 (Device)	4.5μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	KOH	5/6 (12-25MPa)
102 (Device)	4μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	KOH	-
104 (Device)	4μm	2.2μm n-doped	300	SB6e	345°C, 5min.	410°C, 40min.	9.9MPa (3700N)	KOH	-
107	4μm	2.2μm n-doped	300	SB6e	345°C, 0min.	410°C, 40min.	9.9MPa (3700N)	KOH	5/5 (15-20MPa)

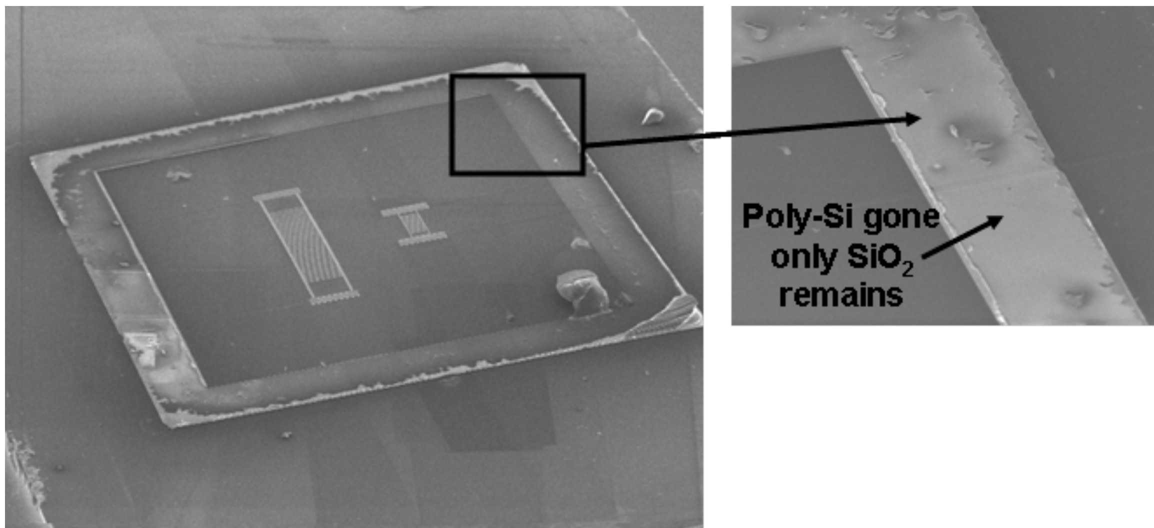


Figure 2.13: An SEM of a bond ring from bond #101 after the cap was torn off of the device wafer.

Even so, shear tests seem to indicate a strong bond. In fact, as shown in Table 2.8, 15 of the 16 packages from bonds #38, #101 and #107 passed the shear test with shear strengths ranging from 11.8 to >27.8 MPa (the one that failed only failed by a small margin with a shear strength of 11.8 MPa). Tables 2.9, 2.10 and 2.11. show the details of

these shear test results. For many of the samples from these bonds, the type of fracture is listed as “Si” which as described in Appendix 1 means that they fractured in the device or cap substrate, not in the bond ring—and as a result, the fracture mode of these devices could not be determined. In several other samples the type of fracture is listed as “bond ring” which meant that cap was sheared off breaking somewhere near the bond ring interface. After inspection, all of these samples fractured in similar ways to the bond shown in Figure 2.13, where the poly-Si tore completely off of the underlying SiO_2 sticking to the Au-Si eutectic layer on the cap.

In addition, no lateral flow of Au-Si was observed for any of these bonds on the device wafer. This is likely because the molten Au-Si alloy does not wet the SiO_2 or Si_4N_3 which surrounded the patterned poly-Si.

Table 2.9: Shear test results for bond #38.

Shear Test Results (Bond #38)			
Position	**Calculated Shear Strength (MPA)**	**Type of Failure**	**Pass/Fail**
C3-R14	22.9	Sheared in cap or device substrate	Pass
C3-R10	22.9	Sheared in cap or device substrate	Pass
C4-R8	22.9	Sheared in cap or device substrate	Pass
C8-R6	19.7	Sheared in cap or device substrate	Pass
C5-R4	>27.8	Sheared in cap or device substrate	Pass
Average Strength: 23.2 MPa			
Standard Deviation: 2.9 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table 2.10: Shear test results for bond #101.

Shear Test Results (Bond #101)			
Position	**Calculated Shear Strength (MPA)**	**Mode of Failure**	**Pass/Fail**
C5-R2	24.5	Sheared in cap or device substrate	Pass
C5-R6	13.4	Sheared in bond ring	Pass
C3-R14	11.8	Sheared in bond ring	Fail
C9-R8	16.6	Sheared in cap or device substrate	Pass
C2-R7	19.7	Sheared in bond ring	Pass
C8-R1	15.0	Sheared in bond ring	Pass
Average Strength: 16.8 MPa			
Standard Deviation: 4.6 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table 2.11: Shear test results for bond #107.

Shear Test Results (Bond #107)			
Position	Calculated Shear Strength (MPA)	type of Failure	Pass/Fail
C5-R14	16.6	Sheared in cap or device substrate	Pass
C5-R8	16.6	Sheared in bond ring	Pass
C4-R2	15.0	Sheared in bond ring	Pass
C10-R8	19.7	Sheared in bond ring	Pass
C2-R8	16.6	Sheared in bond ring	Pass
Average Strength: 16.9 MPa			
Standard Deviation: 1.7 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

2.3.5 BONDS TO AU FILMS

This section presents results for Au-Si bonds to gold thin films. All of the bonds described were between a cap wafer with a 100, 150 or 300µm wide Au bond rings and a device wafer with a 500Å/5000Å Cr/Au film. Figure 2.14 summarizes the dimensions of the thin films used and Table 2.12 summarizes the bond parameters for these bond experiments. In all of the bonds in this table a dehydration bake was used directly before placing the device wafer into the evaporator or sputter tool for the bond ring Cr/Au deposition (details of the deposition process were given in Section 2.3.1). This bake was conducted in an oven at 110ºC for 30 minutes. Results without this dehydration bake are discussed in the next subsection (Section 2.3.5.1).

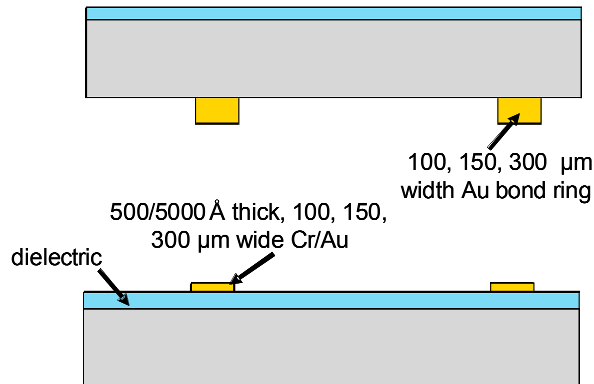


Figure 2.14: The dimensions of the films for bonds from the experiments shown Table 2.12.

As illustrated in Table 2.12, successful bonds were demonstrated with and without a

60 minute intermediate temperature step and at bond temperatures of 410ºC for 40 minutes (as explained in Appendix 1 these bonds were done at 410ºC as opposed to 390ºC because of an error in transferring the recipe to the SB6e bonder). As also shown, Au bond ring thicknesses of 4 and 4.5µm were used on the cap wafer, with bond forces of 1230N, 1850N and 3700N (9.9 MPa of bond pressure in each case because of the differing bond ring widths).

Table 2.12: Bonds to Au thin films where the cap and device wafer had the same dimensions. A dehydration bake was used for each of these bonds.

Au-Si to Au (0.5µm) bonds										
Bond #	**Cap Bond Ring Thick-ness**	**Mat-erial Under Bond Ring**	**Pre-Bake for Au Depo-sition**	**Bond Ring Width**	**Bonder**	**Inter-mediate Temp. Step**	**Bond Temp. Step**	**Bond Force**	**Cav-ity**	**Strength**
95	4.5 µm	Ox/SiN	Yes	300	SB6e	345°C, 60min.	390°C, 40min.	9.9MPa (3700N)	-	-
97	4.5 µm	Ox/SiN	Yes	300	SB6e	345°C, 60min.	410°C, 40min.	9.9Mpa (3700N)	-	-
98	4.5 µm	Ox/SiN	Yes	300	SB6e	-.	410°C, 40min.	9.9Mpa (3700N)	-	5/5 (50-64MPa)
100 (Device)	4 µm	Ox/SiN	Yes	300	SB6e	-	410°C, 40min.	9.9MPa (3700N)	KOH	5/5 (18-21MPa)
103 (Device)	4 µm	Ox/SiN	Yes	150	SB6e	-	410°C, 40min.	9.9MPa (1850N)	KOH	-
105 (Device)	4 µm	Ox/SiN	Yes	100	SB6e	-	410°C, 40min.	9.9MPa (1230N)	KOH	5/5 (30-54MPa)

Table 2.12 also summarized the various shear test results and Tables 2.13, 2.14 and 2.15 show the details of these tests. In bond #100 which had the standard bond ring width of 300µm, all of the devices subjected to the shear test passed with shear strengths of 19 to 22 MPa. Bonds #98 and #105 had bond ring widths of only 100 µm. These bonds broke with roughly the same shear *force*, and because they had smaller bond ring areas, they had higher calculated shear strengths of 50 to 64 MPa and 30 to 54 MPa respectively. Inspecting the bond rings after shear testing, in every case, bulk silicon tore from the cap wafer adhering to device wafers for the entire periphery of the bond.

Table 2.13: Shear test results for bond #98.

Shear Test Results (Bond #98)			
Position	Calculated Shear Strength (MPA)	Mode of Failure	Pass/Fail
C5-R2	49.7	Sheared in bond ring	Pass
C5-R7	63.9	Sheared in bond ring	Pass
C2-R8	54.4	Sheared in bond ring	Pass
C5-R14	68.7	Sheared in bond ring	Pass
C9-R10	63.9	Sheared in bond ring	Pass
Average Strength: 60.1 MPa			
Standard Deviation: 7.8 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table 2.14: Shear test results for bond #100.

Shear Test Results (Bond #100)			
Position	Calculated Shear Strength (MPA)	Mode of Failure	Pass/Fail
C6-R1	18.1	Sheared in bond ring	Pass
C10-R6	18.1	Sheared in bond ring	Pass
C6-R14	21.3	Sheared in bond ring	Pass
C3-R6	18.1	Sheared in bond ring	Pass
C6-R6	18.1	Sheared in bond ring	Pass
Average Strength: 18.8 MPa			
Standard Deviation: 1.4 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table 2.15: Shear test results for bond #105.

Shear Test Results (Bond #105)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C4-R1	54.4	Sheared in bond ring	Pass
C5-R14	54.4	Sheared in bond ring	Pass
C5-R6	30.7	Sheared in bond ring	Pass
C1-R8	59.2	Sheared in bond ring	Pass
C10-R7	44.9	Sheared in bond ring	Pass
Average Strength: 48.7 MPa			
Standard Deviation:11.3 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

The following subsections describe some specific technical issues for bonds to Cr/Au films and for bonds to glass using Cr/Au films.

2.3.5.1 Dehydration Bake

Table 2.16 shows bonds in which a dehydration bake was *not* conducted directly before deposition of the Cr/Au layer in the evaporator or sputter tool. In many cases this resulted in bonds that seem to have a different failure mechanism than the bonds to device wafers that *did* have a dehydration bake. Figure 2.15 shows the results from the razor blade test on bond #92. As illustrated, in some regions, Si transferred from the cap wafer to the device wafer, but in others the Cr/Au layer seems to have delaminated or actually broke in the underlying SiO_2 layer. Similar results were observed for bonds #90 and #91. As shown in the table, in Bond #91 in fact, a different metal stack was used: 500Å/1000Å/5000Å Cr/Pt/Au as opposed to 500Å/5000Å Cr/Au. This change did not seem to affect the outcome of the razor blade test.

Table 2.16: Bonds to Au thin films where the cap and device wafer had the same dimensions and a dehydration bake was not used in several cases. All of the bond ring widths were 300 μm.

Au-SI to Au (0.5 μm) bond										
Bond #	Cap Bond Ring Thick-ness	Mat-erial Under Bond Ring	Pre-Bake for Au Depo-sition	Bonder	Inter-mediate Temp. Step	Bond Temp. Step	Bond Force	Cav-ity	Adhesion to Dielectric	Strength
75	8 μm	Ox	No	SB6	345°C, 60min.	390°C, 40min.	3.5MPa (1300N)	-	Good	-
90	4.5μm	Ox	No	SB6e	345°C, 60min.	390°C, 40min.	9.9MPa (3700N)	-	Bad	-
91	4.5μm	Ox/Cr /Pt/	No	SB6e	345°C, 60min.	390°C, 40min.	9.9MPa (3700N)	-	Bad	-
92	4.5μm	Ox	No	SB6e	345°C, 60min.	390°C, 40min.	9.9MPa (3700N)	-	Bad	5/5 (11.8-26.1MPa)

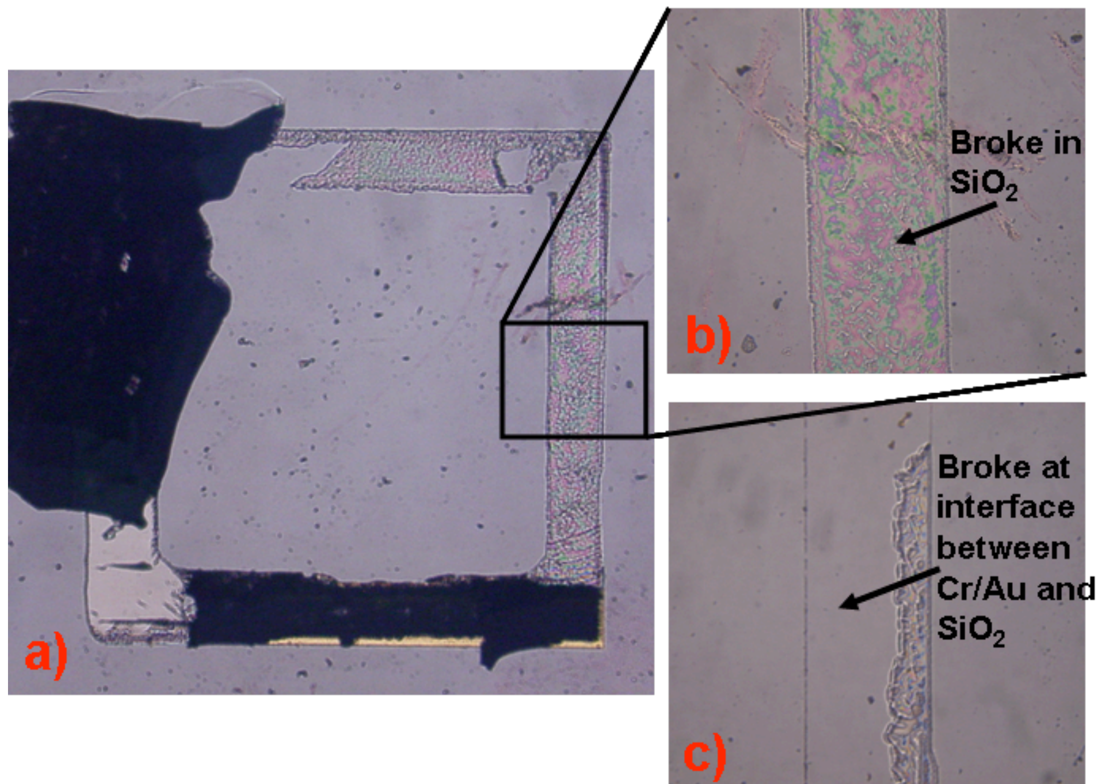


Figure 2.15: Microscope photographs of a) the “dummy” device side of a bond ring from bond #92 where in some parts of the bond ring silicon tore from the other wafer indicating a strong bond, in some parts the Cr/Au delaminated from the wafer and in some parts part of the SiO_2 was pulled off of the device wafer. b) Shows a close of view of an area where oxide was torn off and c) shows an area (on a different bond ring) where the Cr/Au delaminated from the device wafer.

It was presumed that this seeming lack of adhesion of the Cr/Au to the underlying dielectric layer was due to moisture. This is common in deposition of metal films onto glass surfaces (which are similar to SiO_2) and baking out the wafer before thin film deposition is a common method for addressing this problem. It should be noted that Bond #75 in Table 2.16 did not seem to be affected by the lack of a dehydration bake step. It is possible that less moisture collected on the surface of this wafer due to slightly different wafer preparation or that the smaller bond force of 1300N (3.9 MPa) had something to do with this.

Shear tests were conducted on bond #92 as shown in Table 2.16. Table 2.17 shows the details of these shear tests. It is interesting to note that despite the seemingly different failure mechanism; 4 out of 5 of the samples tested passed the shear test with 11.8 to 26.1 MPa shear strengths (the one that failed only failed by a small margin with a shear

strength of 11.8 MPa). Even so, such a failure mechanism could provide a leak path. Furthermore, in bonds to device wafers with Pirani gauges (specifically in bond #100, the vacuum results for this wafer are detailed in Section 5.3.1.2 of Chapter 5), on several dies across the wafer, the feed-through lines were observed to be electrically open. After prying off the caps, they were observed to have broken at the Cr dielectric layer interface or inside the dielectric itself. In some cases, this fracturing actually went through the poly-Si feed-through line themselves. The dehydration bake therefore seemed to be an important step.

Table 2.17: Shear test results for bond #92.

Shear Test Results (Bond #92)			
Position	**Calculated Shear Strength (MPA)**	**Type of Failure**	**Pass/Fail**
Unknown	19.7	Sheared in bond ring	Pass
Unknown	26.1	Sheared in bond ring	Pass
Unknown	19.7	Sheared in bond ring	Pass
Unknown	19.7	Sheared in bond ring	Pass
Unknown	11.8	Sheared in bond ring	Fail
Average Strength: 19.4 MPa			
Standard Deviation:5.1 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

2.3.5.2 Patterning the Au

Table 2.18 shows the parameters for one of the initial bonds to a Au thin film in which a bond was conducted onto a "dummy" device wafer with an un-patterned Au film. Figure 2.16 illustrates the results from this bond. Because of the bad contrast in the photograph, a dotted line was drawn to show the outline of what remains of the bond ring from the cap side. As illustrated in the figure, the Au-Si alloy diffused several millimeters laterally from the bond ring. It was presumed that this lateral diffusion could have adverse effects on the bond quality and therefore the device bond ring was patterned to the same dimensions as the cap wafer bond ring for all experiments following this bond experiment.

Table 2.18: A bond to an Au thin films which was not patterned.

Au-Si to Au (0.5 μm) bond									
Bond #	Cap Bond Ring Thick-ness	Mat-erial Under Bond Ring	Bond Ring Width	Bonder	Inter-mediate Temp. Step	Bond Temp. Step	Bond Force	Cavity	Strength
32	1 μm	Ox	300	SB6	-	395°C, 60min.	5.2MPa (1000N)	-	-

Figure 2.16: The device side of bond #32 where a bond was done to an un-patterned Au thin film. The dotted line shows the location of one of the bond rings.

2.3.5.3 Bonds to Glass

Table 2.19 shows the bond parameters for a bond to a Cr/Au layer deposited on a Pyrex glass wafer. This bond passed the razor blade test and though shear tests were not conducted, it was qualitatively observed to be a strong bond. Subsequently for work published by Lee et al. [182] a similar bond recipe was used for vacuum encapsulating gyroscopes and Pirani gauges in a hybrid bonding process. Therefore, Au-Si eutectic bonding seems to be a viable method for packaging devices fabricated on glass substrates.

Table 2.19: A bonds to a Au thin films on glass.

Bond #	Cap Bond Ring Thick-ness	Mat-erial Under Bond Ring	Pre-Bake for Au Depo-sition	Bonder	Inter-mediate Temp. Step	Bond Temp. Step	Bond Force	Cav-ity	Adhesion to Dielectric	Strength
83	4	Glass	No	SB6	345ºC, 60min.	390ºC, 40min.	3.5MPa (1300N)	-	Good	-

2.4 THE BOND RECIPE FOR AU-SI EUTECTIC BONDS

This section explains each of the steps in the bond recipe used for Au-Si eutectic bonding. Though all of the process steps are explained in this section, most of the technical issues in this section that affected the bond quality involved the amount of bond force and the timing of that applied bond force (Section 2.4.3). In bond experiments three different bonders were used: the EVG 510, the SUSS microTec SB6 and the SUSS microTec SB6e. In some cases, before putting the wafers inside of the bond chamber, they were first aligned to each other in the SUSS microTec SB6 wafer alignment system before going in the SB6 or SB6e bonders. Appendix 2 presents more details on the three bonders used for bond experiments, the temperature calibration of these bond chambers, and the fixturing used for alignment of the wafers.

Figure 2.17 shows a schematic of the bonding process where: i) the bond chamber was pumped down to a pressure of around 10×10^{-6} Torr; ii) both the *bottom heater* and *top heater* were raised to 345ºC and held for 1 hour in the *outgassing step*; iii) physical contact was made between the wafers by removing the spacers, the bond force was applied, and the clamps holding the wafers together were removed; iv) the temperature was raised to the *bond temperature* which ranged from 390 to 410ºC and the temperature was held for a specified amount of time, generally 40 minutes. After running the bond sequence, the wafers were then cooled to below 200ºC at which point they were pulled out of the wafer bonder.

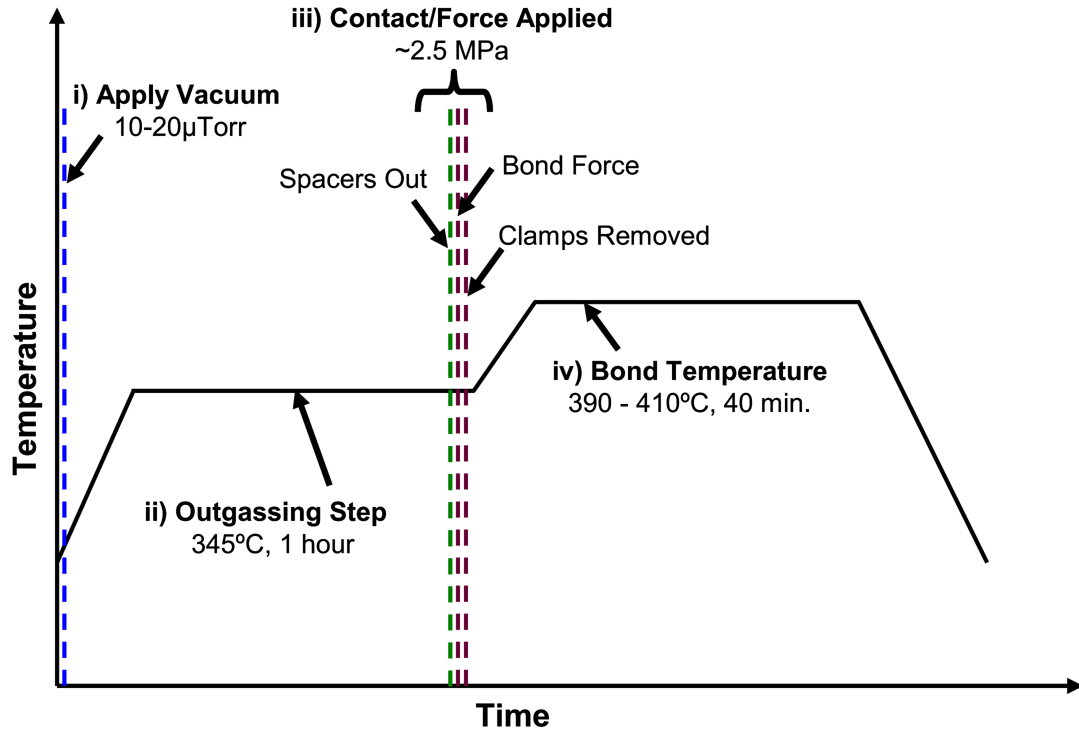


Figure 2.17: The generic bond recipe.

In the rest of this section, these bond steps are discussed in more detail. Sections 2.4.1 and 2.4.2 first present short discussions on the applied vacuum inside of the vacuum chamber (step 1) and the outgassing step (step 2). Section 2.4.3 then presents a discussion on the magnitude and timing of the applied bond force (step 3). Finally, Section 2.4.4 discusses the bond temperature step (step 4).

2.4.1 STEP 1: APPLICATION OF VACUUM

The first step in the bonding processes in Figure 2.17 was the application of vacuum. Inside of the bond vacuum chamber, a pressure of between 10 and 20 µTorr was generally achieved. This step had two motivations. First, one of the goals of this thesis is to develop a vacuum package. Therefore, pulling vacuum and holding the vacuum before the bond and during the bond was a necessary step. Second, this step was useful if not necessary, even for packaging devices that do not need to operate in a vacuum environment. This is because of the of Si diffusion into Au film during bonding. As discussed in Section 2.1.1.2 (*Oxide Formation on Au Thin Films*) SiO_2 formation on top

of Au films have been observed in the literature at temperatures well under the Au-Si eutectic temperature. This SiO_2 formation can act as a diffusion barriers and can result in non-uniform bonds [160]. For devices which need to be packaged at or near atmospheric pressure, one potential option would be to evacuate the chamber with a dry inert gas such as nitrogen or argon.

2.4.2 STEP 2: THE OUTGASSING STEP

The outgassing step shown in Figure 2.17 was used specifically to aid in achieving lower vacuum packaged pressures. During the outgassing step, the wafers were held apart for 60 minutes at 345ºC. As will be discussed in Chapter 5, despite the fact that the vacuum chamber was at a pressure of 10 to 20 μTorr when the packaged cavities were sealed after completion of the bond, the pressures inside of the micro-package where measured at between 2 and 40 Torr without the advent of getters. As will be discussed in Chapter 5, these elevated pressures were likely due to outgassing inside of the micro-cavity after the packages were sealed. The outgassing step was implemented in order to outgas the surfaces of the wafers before the devices were sealed. Because the outgassing rates of materials in a vacuum environment generally reduce over time (even more so at elevated temperature) this outgassing step therefore should help reduce the amount of outgassing inside of the micro-cavity after sealing.

Table 2.20 shows a summary of some of the bonding results presented in Chapter 5. In all of the bonds shown in Table 2.20 getters were used, but only #71 and #78 used the 345ºC, 60 minute long outgassing step. As illustrated, *with* the outgassing step pressures in the single and *tens* of milliTorr were achieved and *without* the outgassing step pressures in the *hundreds* of milliTorr were achieved.

Table 2.20: A summary of the different pressures measured with/without an outgassing step for some of the bonds conducted in Chapter 5.

Bond	Location of Data	Getters	Outgassing Step	Pressure Ranges
#103, #105	Section 5.3.2	Yes	No	77-2400 mTorr
#71, #78	Section 5.3.3	Yes	Yes	<2-23.3 mTorr

2.4.3 STEP 3: WAFER CONTACT & BOND FORCE

As shown in Figure 2.17, after applying the outgassing step, the wafers were brought into contact and the bond force was applied. This entailed removing the spacers which held the wafers apart, applying the bond force and then finally removing the clamps which held the wafers together in the alignment fixture (details on the bond chamber and alignment fixturing are given in Appendix 2). For a majority of the bonds, the bond pressure was around 2.5 MPa. As will be described in the following sections, decreasing the bond pressure to 1.0 MPa (Section 2.4.3.1) and increasing the bond pressure to ~10 MPa (Section 2.4.3.2) decreased the uniformity/strength of the bond. Furthermore, the timing of the applied bond force also affected bond quality (Section 2.4.3.3).

2.4.3.1 Low Bond Pressure Results (~1 MPa)

Table 2.21 shows the bond parameters for a number of bonds conducted with bond pressures 1.0 MPa (a 390 N bond force). All of these bonds involved a 300 μm wide bond ring and were to 0.3μm thick poly-Si. As compared to the bonds from Table 2.2 (the uniform/strong bonds to 0.3 μm poly-Si from section 2.3.3 which were done with bond pressure of 2.7 MPa (a 1000N bond force)), the shear test results conducted on these bonds were not as uniform. In other words, in some parts of the wafer silicon tore from the cap wafer adhering to the device wafer for the entire periphery of the bond ring and in other parts of the wafer, less conformal bonds were observed.

Table 2.21: Summary of bonds to 0.3 µm thick poly-Si thin films (bond parameters summarized in Fig. 2.29), in which a 390 N of bond force was applied.

Bond #	Cap Bond ring Thickness	Bonder	Intermediate Temperature Step	Bond Temperature Step	Bond Force	Cavity	Pass the Shear Test?
51	3.5µm	SB6	345ºC, 10min.	390ºC, 20min.	1.0MPa (390N)	-	-
53	3.4µm	SB6	345ºC, 10min.	390ºC, 35 min.	1.0MPa (390N)	-	4/5 (12-20MPa)
56	8µm	SB6	345ºC, 10min.	390ºC, 35min.	1.0MPa (390N)	DRIE	3/5 (0-23MPa)
58	8µm	SB6	-	390ºC, 40min.	1.0MPa (390N)	-	-

Figure 2.18 shows one of the “dummy” device bond rings from bond #53 after the razor blade test. As illustrated, silicon tore from the cap wafer and adhered to the “dummy” device substrate from some areas of the bond ring but not in others. Figure 2.18 seems to illustrate a non-uniform bond across this bond ring. One likely cause is that the relatively lower bond force was not substantial enough to compress all of the bond rings enough across the wafer so that they all made good contact to the poly-Si on the “dummy” device wafer.

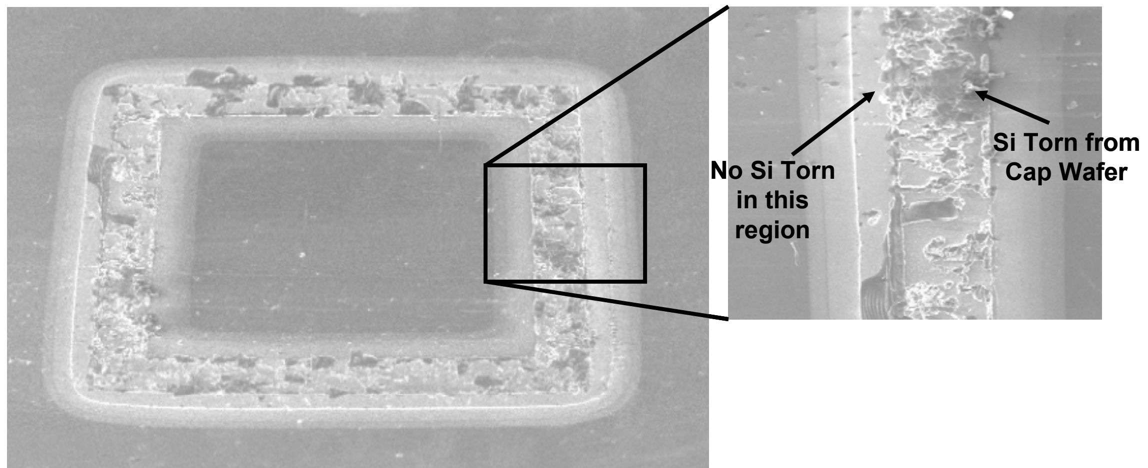


Figure 2.18: The “dummy” device substrate after a cap was sheared off for bond #53.

As illustrated in Table 2.21, 7 out of 10 of the chips from bonds #53 and #56 passed the shear test with shear strengths ranging from 0 to 23 MPa. Tables 2.22 and 2.23 show the details of these shear tests. As shown, the failure mode for all of the bonds are listed as “bond ring,” indicating that all of the packages sheared off at the bond ring interface.

Most of the sheared packages showed similar results to the die shown in Figure 2.18 where parts of the cap wafer adhered to the "dummy" device substrate where as others did not seem to make contact at all.

Table 2.22: Shear test results for bond #53.

Shear Test Results (Bond #53)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
Unknown	13.4	Sheared in bond ring	Pass
Unknown	16.6	Sheared in bond ring	Pass
Unknown	19.7	Sheared in bond ring	Pass
Unknown	11.8	Sheared in bond ring	Fail
Unknown	13.4	Sheared in bond ring	Pass
Average Strength: 15.0 MPa			
Standard Deviation:3.2 MPa			

*Details on the interpretation of this data given in Section 2.2 and Appendix 1.

Table 2.23: Shear test results for bond #56.

Shear Test Results (Bond #56)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C4-R1	16.6	Sheared in bond ring	Pass
C6-R7	8.7	Sheared in bond ring	Fail
C7-R13	15.0	Sheared in bond ring	Pass
C10-R9	0.0	Sheared in bond ring	Fail
C9-R8	22.9	Sheared in bond ring	Pass
Average Strength: 12.6 MPa			
Standard Deviation:8.7 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

2.4.3.2 High Bond Pressure Results (~10 MPa)

Table 2.24 shows the bond parameters for a number of bonds conducted with bond pressure of 10.4 MPa (a 3900 N bond force). All of these bonds involved a 300 μm wide bond ring and were to 0.3μm thick poly-Si. As illustrated in the Table 2.24, none of the chips from bonds #60 passed the shear test with shear strengths ranging from 0 to 12 MPa. Table 2.25 shows the details of these shear tests. Qualitatively from the razor blade test, bonds #61 and #65 seemed to have similar weak bond strengths.

Table 2.24: Summary of the bonds to 0.3 µm thick poly-Si thin films in which a very large bond force was used (3900N), which considered to be hermetic but "weak."

Bond #	Cap Bond ring Thickness	Bonder	Intermediate Temperature Step	Bond Temperature Step	Bond Force	Cavity	Pass the Shear Test?
60	8µm	SB6	-	390°C, 40min.	10.4MPa (3900N)	DRIE	0/6 (0-11 MPa)
61	6µm	SB6	-	390°C, 40min.	10.4MPa (3900N)	DRIE	-
65	8µm	SB6	-	390°C, 40min.	10.4MPa (3900N)	DRIE	-

Table 2.25: Shear test results for bond #60.

Shear Test Results (Bond #60)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C6-R8	0.0	Sheared in bond ring	Fail
C5-R8	5.4	Sheared in bond ring	Fail
C2-R8	11.8	Sheared in bond ring	Fail
C5-R13	0.0	Sheared in bond ring	Fail
C6-R13	8.7	Sheared in bond ring	Fail
C6-R9	5.5	Sheared in bond ring	Fail
Average Strength: 5.2 MPa			
Standard Deviation:5.2 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

As compared to the bonds from Table 2.2 (the uniform/strong bonds to 0.3µm poly-Si from section 2.3.3 which were done with a bond pressure of 2.7 MPa (a 1000N bond force)), these shear test results were very poor. Figure 2.19 shows SEMs of a cross-section of the bond rings from bond #60. Figure 2.19c shows a Dectak profilometery scan of this bond. As illustrated, on the edge of the bond region on either side of the bond, in some places much of the bulk Si from the cap wafer pulled off, adhering to the device wafer; and in other places bulk Si from the device wafer pulled off adhering to the cap wafer. (Because of the scaling in Figure 2.19c, much of the scan is cut off. The portion in the figure labeled "bulk Si adhered to device wafer" and "bulk Si adhered to cap wafer" are in fact 60 and -6.2 µm high indicating that bulk Si in fact did transfer from one wafer to the other). In these areas, enough Au-Si alloy seems to have spread laterally to allowing for bonds outside of the original bond ring area. In the bond region in the center of the scan, there are areas where most if not all of the 0.3 thick poly-Si layer had

been either consumed or pulled completely from the “dummy” device wafer. In Figure 2.19a and Figure 2.19b the dark regions show these areas where the poly-Si was pulled away.

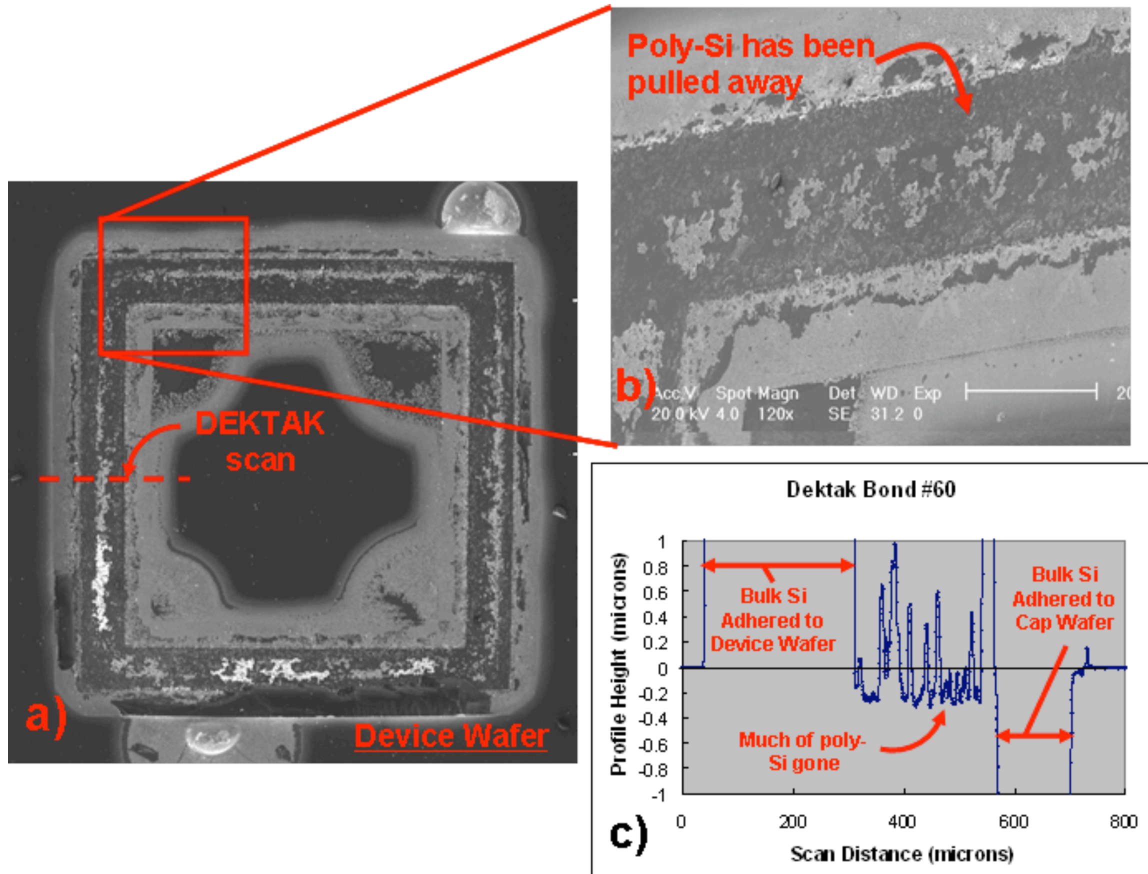


Figure 2.19: For bond #60, an SEM of a) the top view of the bond ring on the “dummy” device wafer after the cap has been pulled off, b) a closer look at the bond ring, and c) a DEKTAK scan of a portion of this bond ring.

Figure 2.20 shows the other side of the bond. As shown in Figure 2.20c, even though the initial Au thickness was 8 μm, it squeezed down to approximately 2.5μm (31.25% of the original bond ring thickness) indicating that much of the Au-Si alloy had squeezed out of the originally 300 μm wide bond ring region. This is also evidenced by the amount of Au-Si alloy which was shown to have spread in Figure 2.19a (the light areas outside of the bond ring region in Figure 2.19a is Au-Si alloy). A more thorough discussion on such Au-Si eutectic flow will be given in Section 2.5.

It is also interesting to note that there is no sign of the poly-Si from the “dummy” device wafer even though it was observed to have been pulled off from the “dummy” device wafer. It seems that the entire 0.3 μm thick poly-Si layer may have been completely consumed during the bond.

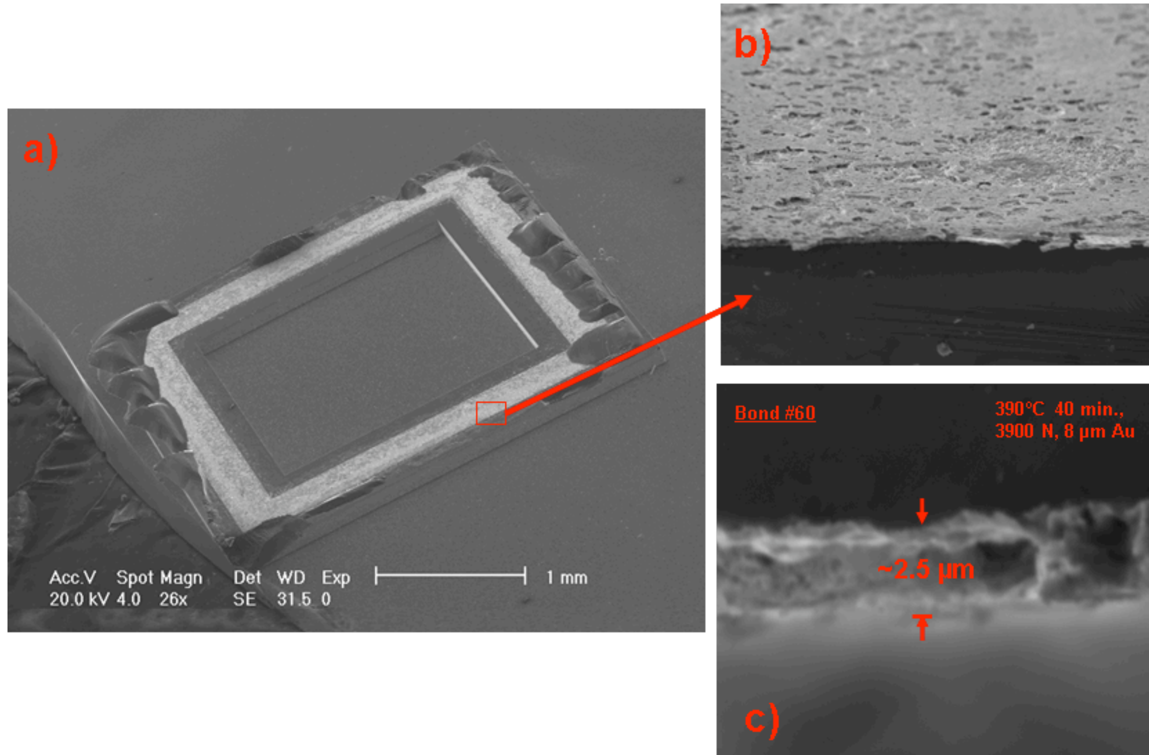


Figure 2.20: SEM of a) the cap side of the one of the bond rings from bond #60, b) a closer look at the Au-Si alloy layer which still adheres to the cap side, and c) a cleaved section which show the thickness of this Au-Si alloy layer.

In summary, the larger applied bond force seems to have been problematic in two ways: 1) it caused significant lateral flow of the Au-Si alloy out of the bond joint and 2) it seemed to reduce the strength of the bond joint. The mechanism of this reduced strength is not known but it could result from either the lateral flow of Au-Si eutectic or from stress put on the bond joint itself due to the large bond force, weakening the bond between the poly-Si layer (or what was the poly-Si layer) and the underlying dielectric. It is important to note that this problem was not observed in bonds to Cr/Au layers. Bond forces of 3700N (a 9.9 MPa bond pressure) in fact were used in most of those bond experiments (Section 2.3.5, *Bonds to Au Films*). The issues described above therefore

may have to do with the properties of the poly-Si in the presence of a large bond force (i.e. a low yield strength or poor adhesion to the underlying SiO_2).

2.4.3.3 Timing of the Applied Bond Pressure

As was shown in Figure 2.17, the general bond recipe involved applying the bond force before going to the bond temperature (that is, before raising the temperature above the eutectic temperature). Table 2.26 shows the bond parameters for several bonds in which the bond force was applied *after* the bond temperature was achieved.

Table 2.26: Summary of bonds to 0.3 μm thick poly-Si in which the bond force was applied after the bond temperature was achieved. These all resulted in bonds that were considered non-hermetic and "weak."

Bond #	Cap Bond ring Thickness	Bonder	Inter-mediate temp.	Bond Temp.	Bond Force	Force applied after Bond temp step?	Cavity Etch	Strength
49 (Device)	3	EVG	-	395°C, 40min.	2.7MPa (1000N)	Yes	TMAH	-
50	3	SB6	345°C, 10min.	390°C, 20min.	1.1MPa (430N)	Yes	TMAH	3/5 (5.5-16.6 MPa)
52	3.5	SB6	345°C, 10min.	390°C, 35min.	1.1MPa (430N)	Yes	KOH	-
54	3.6	EVG	-	395°C, 35min.	2.7MPa (1000N)	Yes	DRIE	-

Figure 2.21 shows SEM photographs of bond #49. As illustrated, an actual device wafer was used in this bond (fabrication for device wafers is described in Chapter 3). DEKTAK profilometery showed that the poly-Si bond ring on the device substrate (Figure 2.21a), remained intact after the cap was pried off. Figure 2.21b shows the cap side where indentations can be seen in the Au-Si eutectic where the feed-throughs made contact. A closer look at this indentation in Figure 2.21c and Figure 2.21d show that the bulk silicon on the cap wafer had pressed flush to the 3000Å high feed-throughs—the highest topology on the device wafer. As evident, nearly all of the Au-Si alloy squeezed out during the bond. What seems to have happened in all of the bonds shown in Table 2.26 is the Au-Si eutectic alloy first formed and then when contact was made, nearly all of this molten liquid got squeezed out of the bond joint. Figure 2.21d shows a schematic of how the silicon from the cap wafer appears to press flush against the bond ring on the device wafer during the bond. This is also indicated in Figure 2.21a where the light areas

show a large volume of Au-Si alloy which has squeezed out of the bond joint.

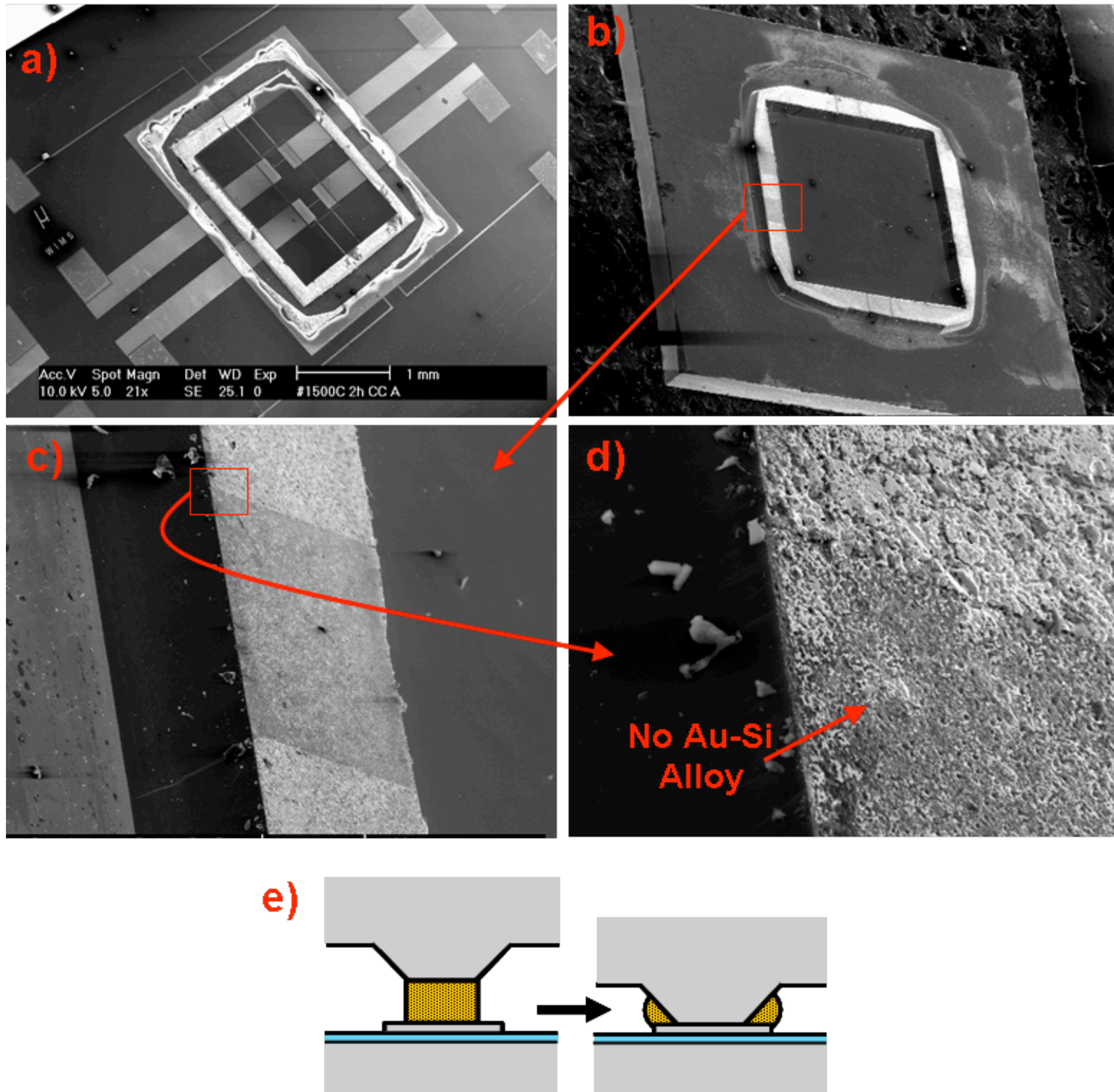


Figure 2.21: SEM of a) the device side of the one of the bond rings from bond #49 where mist of the Au-Si alloy has squeezed out from the bond joint, b) the cap side of bond #49, and c),d) a closer look at one of the feed-through indentations showing that the feed-through had pressed flush against the Si surface of the cap wafer squeezing out nearly all of the Au-Si liquid. e) Shows a schematic of how the silicon from the cap wafer appears to press nearly flush to the surface of the device wafer.

As shown in Table 2.26 shear tests were conducted on bond #50. Table 2.27 shows the details of these shear tests. As shown, the shear strengths ranged from 5.5 to 16.6 MPa with 3 out of 5 of the packages passing the shear test. Inspecting the bond ring interface after the shear test showed similar results as were shown in Figure 2.21 where

the Au-Si alloy appeared to have completely squeezed out of the bond joint.

Table 2.27: Shear test results for bond #50.

Shear Test Results (Bond #50)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C5-R2	16.6	Sheared in bond ring	Pass
C5-R7	8.7	Sheared in bond ring	Fail
C2-R8	15.0	Sheared in bond ring	Pass
C4-R14	13.4	Sheared in bond ring	Pass
C9-R8	5.5	Sheared in bond ring	Fail
Average Strength: 11.8 MPa			
Standard Deviation:4.6 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

2.4.4 THE BOND TEMPERATURE

As was summarized in Figure 2.17, applied temperatures ranging from 390 to 410ºC were used in bond experiments with hold times ranging from 20 to 40 minutes. As detailed in Appendix 2, in the EVG 510 and SB6 bonders, the temperatures sensor used for feedback and control inside of the bonder was not located close enough to the wafers for an accurate temperature measurement. As a result, such long hold times and high temperatures relative the eutectic temperature (~363ºC) were used to make sure that the wafers inside of the bonder had enough time to heat up. As explained in the Appendix 2, in the SB6e bonder this design flaw was addressed with a thermocouple located only millimeters from the wafers during bonding and with a bonder design which allowed for much faster heating and cooling rates. Though not studied here, this would allow for bond tests at closer to the eutectic temperature of ~363ºC with shorter hold times in order to reduce the thermal budget on the packaged device.

2.5 AU-SI EUTECTIC LATERAL FLOW

Appendix 3 presents an analysis on bond cross-sections for a number bonds from the bond experiments described in this chapter. In this analysis, the composition for each of these bond rings was approximately 50 atomic % Si in Au. As calculated in Appendix 3, for a given initial Au bond ring thickness, this additional Si content should increase the

bond ring volume by 2.22 times. As a result, one of the more important issues in designing a bonding process is determining how to manage the resultant lateral flow of the Au-Si alloy. Several parameters affect how the Au-Si alloy flowed including the applied bond force, the initial bond ring width, and the geometry of the cap wafer (i.e. whether or not a cavity was anisotropically etched).

Section 2.5.1 first explains two types of lateral flow observed in bonded samples: compressive flow and diffusive flow. Section 2.5.2 explains the effects of an anisotropically etched cavity on the Au-Si alloy flow. Section 2.5.3 describes how the Au-Si alloy flowed onto the getters in device wafer bonds in several instances. Finally, Section 2.5.4 provides analysis on how to predict the Au-Si alloy flow for a given geometry.

2.5.1 COMPRESSIVE AND DIFFUSIVE FLOW (ANALYSIS OF BONDS #56, #51 AND #36)

Figure 2.22 shows a cross-section of bond #56 (already presented in Section 2.4.1) which was bonded at 390ºC for 35 minutes with a bond force of 390 N and an original Au thickness of 8 µm. At the edge of the fractured bond outside of the bond ring, in Figure 2.22a, the distance between the original cap wafer and device wafer surfaces was measured at 5.1µm—thus inferring that the Au-Si eutectic compressed by around 3.9 µm from the original Au thickness of 8 µm. The dotted line in Figure 2.22b shows approximately where the original Au/cap wafer interface was in the cross-section. As illustrated, the Au-Si eutectic region has expanded into the cap wafer as far as 3µm past the original cap wafer interface. (As was discussed in Section 2.1.1.3, similar effects have been observed in the literature in die attach bond experiments [97, 176]).

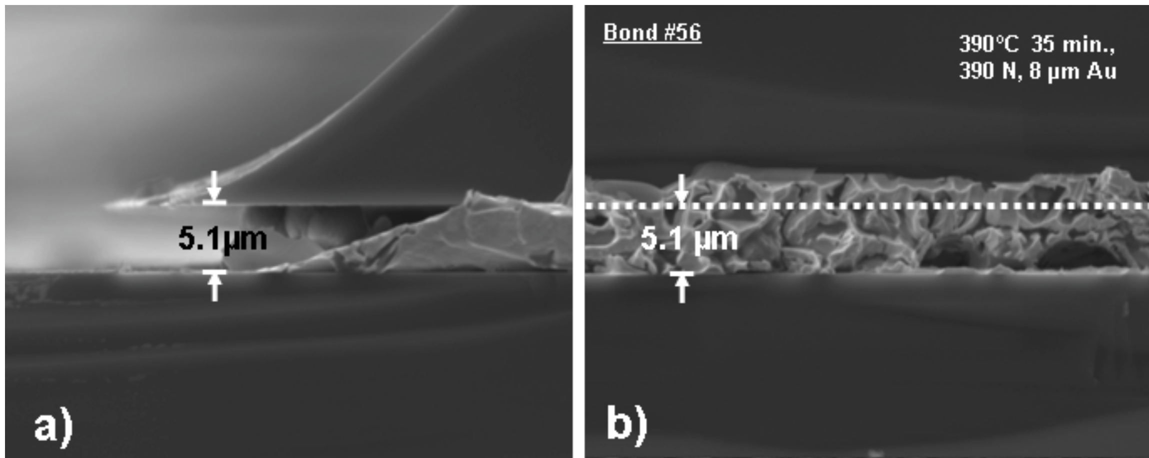


Figure 2.22: SEMS of a cleaved bond ring from bond #56 showing a) the final distance between the original interfaces between the cap and device wafers and b) a cross-section of the bond ring where the dotted line shows the distance between the original interface at the cap wafer and the "dummy" device interface.

Similar analysis was done for cross-sections from bonds #51 and #36 (from Sections 2.4.1, and Section 2.3.3) which had similar bond temperatures, and an original Au bond ring thickness of 3.5µm and bond forces of 390 and 1000 N respectively. Cross-sections and a summary of these bond are shown in Figure 2.23. As illustrated in Figure 2.23a and Figure 2.23b, this resulted in a final distances of 3.1 µm and 3.5 µm from the original bond interfaces on the cap wafer and the "dummy" device wafer's bond interface. As compared to bond #56 which compressed by approximately 2.9µm, the bond interfaces in bonds #51 and #36 seem to have compressed only a fraction of a micron or not at all. The main difference between these bonds and #56 was the original Au thickness. Analysis in Section 2.5.4 will attempt to explain these results.

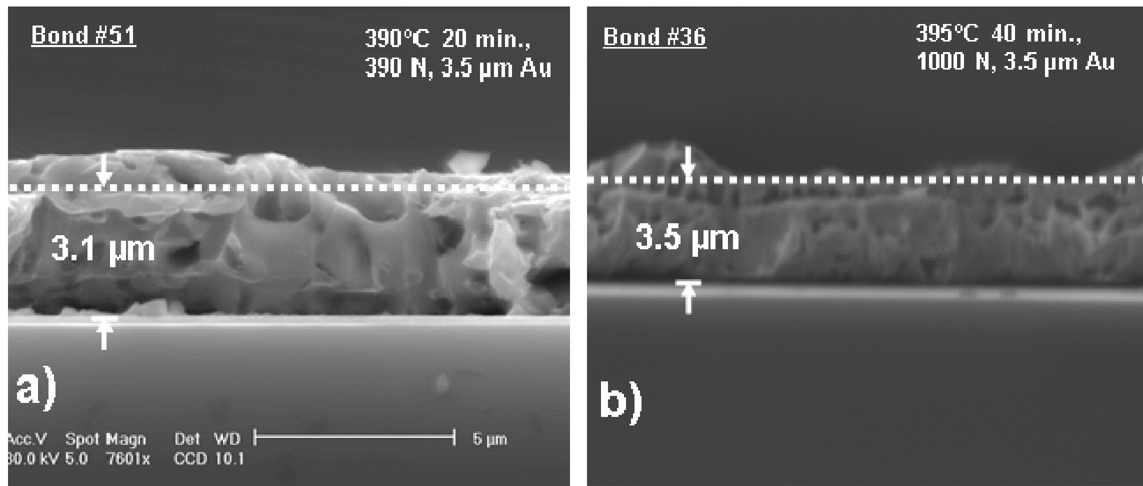


Figure 2.23: SEMS of a cleaved section of bond rings showing a cross-section where the dotted line shows the distance between the original interface at the cap wafer and the "dummy" device interface for a) bond #51 and b) bond #36.

As expected, in each of the cases for bond #56, #51 and #36 (Figures 2.44 and 2.45) a noticeable amount of the Au-Si eutectic alloy actually squeezed out of the bond joint spreading laterally. This lateral spreading occurred both uniformly, where the bond ring width was effectively increased (compressive flow) or diffused/flowed laterally (diffusive flow) forming a thin layer of Au-Si eutectic over the poly-Si. Figure 2.24a and Figure 2.24b illustrated these two types of flow schematically.

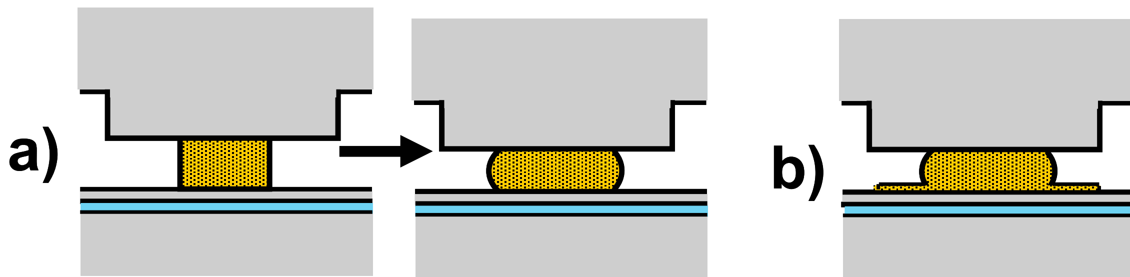


Figure 2.24: A schematic showing how Au-Si alloy a) squeezes laterally, widening the effective bond width for bonds in which the cap wafer was not patterned or was patterned with a DRIE etch. b) Shows Au-Si lateral flow where only a thin layer of Au-Si eutectic spread.

Figure 2.25 shows an example of diffusive flow. In this bond, silicon tore from the cap wafer adhering to the "dummy" device wafer. The light areas in Figure 2.25a and Figure 2.25b are where Au-Si alloy has diffused/flowed more than 100 µm laterally across the poly-Si. Figure 2.25c show a closer view of this Au-Si alloy layer which upon

even closer inspection was shown to be less then 50nm thick. This diffusive flow was only observed on top of poly-Si and did not flow over dielectric layers.

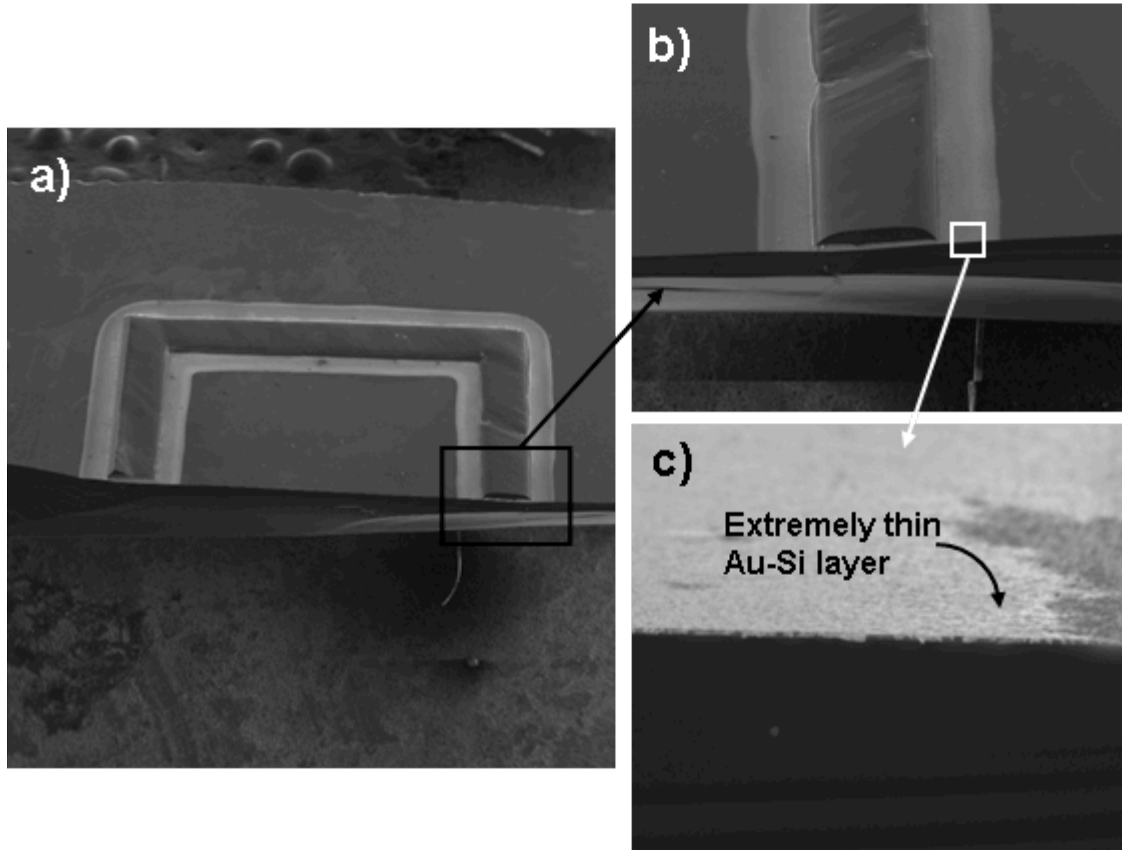


Figure 2.25: a) SEM of a cleaved section of a bond ring from bond #36 showing where Si has torn from the cap wafer and the light area is Au-Si alloy which has spread laterally across the surface. b, c) A closer look at this Au-Si that has spread across the top surface of the poly shows that it is only l0s of nanometers or even angstroms thick.

2.5.2 EFFECTS OF AN ANISOTROPIC ETCHED CAVITY

Figure 2.26 shows a cross-section from bond #71, a device wafer bond which was discussed in Chapter 5. Figure 2.26a shows the anisotropically etched side walls of this cross-section. As shown in Figure 2.26b the Au-Si alloy region compressed from its original thickness of 4 μm down to 1.5μm thick (though the original Au/cap wafer interface could not be discerned as was done in the bonds analyzed in the previous section). This means that the bond ring compressed by 62.5% *or more*. This is significantly more than in bonds #56, #51 and #36 which did not have anisotropically etched sidewalls. Figure 2.26c shows that a relatively large volume of this Au-Si alloy

has squeezed out the sides of the bond. Analysis in Section 2.5.4 discusses these results further.

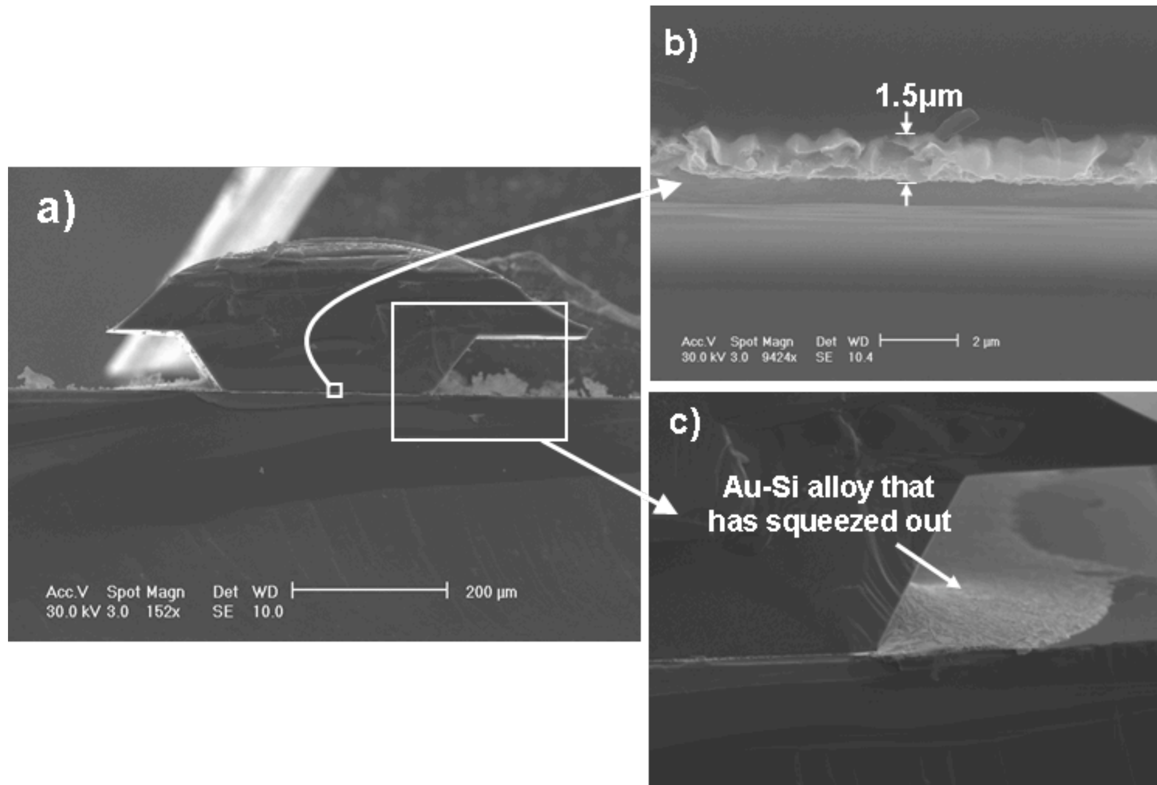


Figure 2.26: a) An SEM of the cross-section of one of the bond rings from Bond #71 which shows the anisotropically etched side walls, b) a closer look showing the bond interface, and c) a look at the right side of the anisotropically etch side wall showing the large volume of Au-Si alloy which has squeezed out.

In bond #71, the Au-Si only flowed laterally, but only where there was poly-Si on the device wafer—in other words, it did not flow onto the parts of the wafer where the top layer was dielectric. This is likely due to the fact that Au-Si alloy (similar to most other solders) does not wet dielectric layers such as SiO_2 or Si_3N_4.

2.5.3 LATERAL FLOW ONTO GETTERS

In several device wafer bonds shown in Table 2.28 the Au-Si alloy flowed on the cap wafer, spreading onto the getter. The bonding results for these wafers were already presented in Section 2.3.4. As was detailed there, the heavily phosphorous doped poly-Si layer on the device substrate was patterned to the same dimensions as those on the cap

wafer. This effectively stopped the flow of the Au-Si alloy on the device wafer, but in bonds #101, #102 and #104 it had a tendency to flow on the cap wafer instead.

Table 2.28: Summary of bonds between cap wafers with 300μm wide bond rings to 2.2 μm thick heavily phosphorous doped poly-Si thin films. All of these were device wafer bonds which were conducted after CPD.

Au-Si to poly-Si (2.2 μm) bonds									
Bond #	Cap Bond Ring Thick-ness	Poly-Si Thick-ness	Device Bond Ring Width	Bonder	Inter-mediate Temp. Step	Bond Temp. Step	Bond Force	Cavity	Bond Strength
101 (Device)	4.5μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	KOH	5/6 (11.9-25MPa)
102 (Device)	4μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	KOH	-
104 (Device)	4μm	2.2μm n-doped	300	SB6e	345°C, 5min.	410°C, 40min.	9.9MPa (3700N)	KOH	-

Figure 2.27 shows one of the caps after bonding from bond #101 where some Au-Si alloy flowed on the cap wafer side. Au-Si alloy did not spread onto the getter on every package in bonds #101, #102 and #104, but in many cases they did. In most cases where the Au-Si alloy made contact with the getter, it diffused across the entire getter and as discussed in the vacuum encapsulation results presented in Appendix 5, this seemed to compromise the effectiveness of the getter for these wafers. This compromising of the getters was not observed in device wafer bonds to un-doped poly-Si or to Au thin films. Since the Au-Si alloy seemed to have a greater tendency to flow laterally on heavily phosphorous doped poly-Si films (see Section 2.3.4), it is possible that the presence of phosphorous encouraged the flow of the Au-Si alloy in these cases. On the other hand, there may have been another parameter which caused this lateral flow and resultant Au-Si eutectic/getter interaction (such as how close the gettering material was patterned on those particular wafers due to shadow mask misalignment). Regardless, making sure that the Au-Si alloy does not interact with the getter is an important consideration in the design.

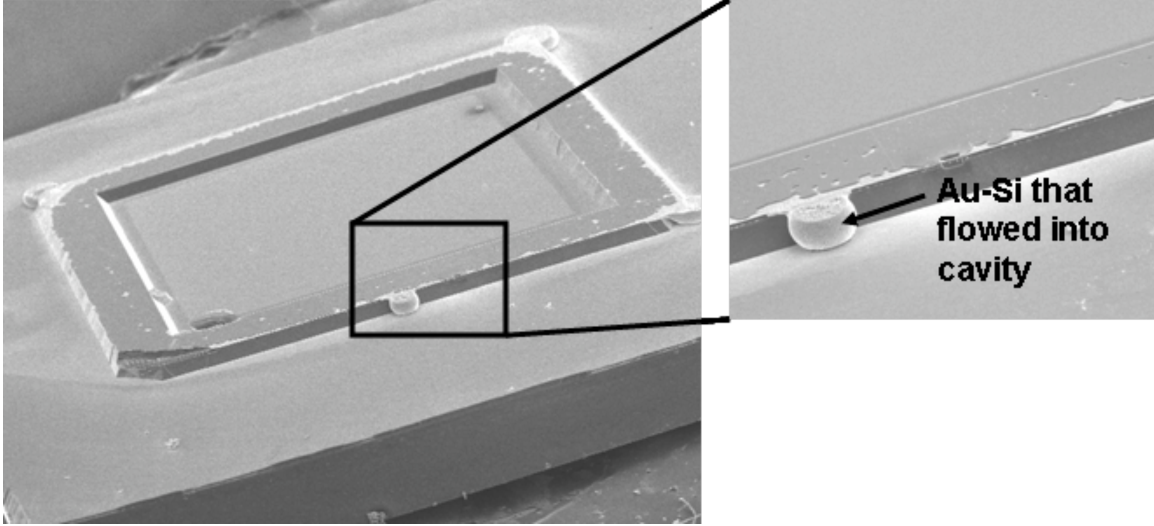


Figure 2.27: An SEM photograph of the cap side of bond #101 where Au-Si alloy has flowed on the cap side.

2.5.4 ANALYSIS OF AU-SI ALLOY FLOW

In Appendix 3, the composition of the bond ring during a bond is discussed, as Si from the cap wafer diffused into the Au bond ring. As is calculated in Appendix 3, even up to 50 atomic % Si in Au, the bond joint should be around 59% eutectic alloy by volume. Therefore, for much of the 40 minutes that the bond ring is held above the eutectic temperature, it is likely viscous and some force should be required to counterbalance the applied bond force in order to reach equilibrium. Figure 2.28 shows how the surface tension of the liquid may provide this counterbalancing force. The schematic in Figure 2.28a shows the melted bond ring, where w is the final width, F_b is the applied bond force, t is the final distance between the cap wafer and the device wafer and ϕ is the contact angle between the liquid and the silicon surface. The length, L, of the bond ring goes into the page. The bond force, F_b, gets distributed across the 124 bond rings spanning the wafer which are each initially 300μm wide, and essentially 10 mm long (the length around the periphery of each square bond ring). As a result, the pressure inside the liquid, σ_L, is given by:

$$\sigma_L = \frac{F_b}{Area} = \frac{F_b}{124 \cdot 0.01 \cdot w} = \frac{F_b}{1.24 \cdot w} \tag{2.1}$$

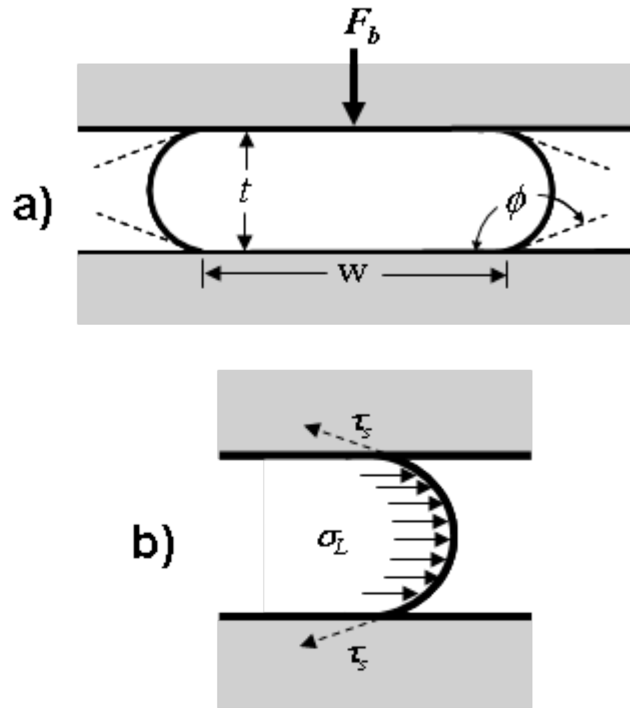


Figure 2.28: a) A schematic showing the different parameters which effect the calculations for achieving static equilibrium in the bond ring, and b) a closer look at how the pressure in the liquid is balanced by the surface tension.

As shown in Figure 2.28b, at the liquid gas interface, the pressure inside the liquid is balanced by the surface tension (strength of the atomic bonds at the surface of the liquid), τ_s, which is a measurable quantity with units of force per length. This force balance equation is:

$$\sum F = \sigma_L t L + 2\tau_s L \cos(\phi) = 0 \qquad (2.2)$$

Combining Equations 2.1 and 2.2, the final thickness to width ratio can be determined as:

$$\frac{t}{w} = -\frac{2.48\tau_s}{F_b}\cos(\phi) \qquad (2.3)$$

Only one reference each was found for the *surface tension* and *contact angle* of Au-Si alloy mixtures. Contact angles where found for molten Au-Si eutectic mixtures on (100) oriented Si by Ressel at el. [183] at temperatures from 400 to 800ºC ranging from 152º to

165º. At 400ºC a contact angle of approximately 152º was measured. Naidich at el. [184] on the other hand measure surface tensions of Au-Si mixtures at a range of compositions at temperatures from just under 400ºC to as high 1600 ºC of 0.7 to 1.1 N/m. Extrapolating from Naidich at el.'s graph of this data, at 50 atomic % Si in gold at 400ºC, the surface tension was approximately 0.85 N/m.

Using these values for the surface tension and contact angle and Equation 2.3, the solid line in Figure 2.29 shows the predicted *t/w* as a function of the applied bond force F_b. Also shown in Figure 2.29, are the measured *t/w* vs. F_b for bonds #36, #51, #56 and #60 and #71. The final thicknesses and widths were measured through SEM photographs analyzed earlier in Section 2.5. These values are summarized in Table 2.29. As illustrated in Figure 2.29, the *t/w* ratios were all a bit higher than predicted by Equation 4.3. This could result from other factors which affect the amount that the bond joint compresses such as Si precipitate formation. These Si precipitates were observed to be as large as 2 μm in diameter. Also shown by the dashed line in Figure 2.29 is the predicted *t/w* assuming a surface tension of 2 N/m. Though this line does not predict the exact t/w ratio, it could be used to better estimate the minimum *t/w* to be expected.

The biggest significance of Figure 2.29 is that there is a correlation between the applied bond force, F_b, and the final *t/w* ratio and therefore, the amount of spreading of the Au/Si eutectic. In cases where there was a lot of compression of the Au-Si bond ring, there was significant lateral flow. Therefore, from Figure 2.29, smaller applied bond forces, or a thinner initial Au bond ring thicknesses clearly resulted in less spreading of the Au-Si eutectic out of the bond joint.

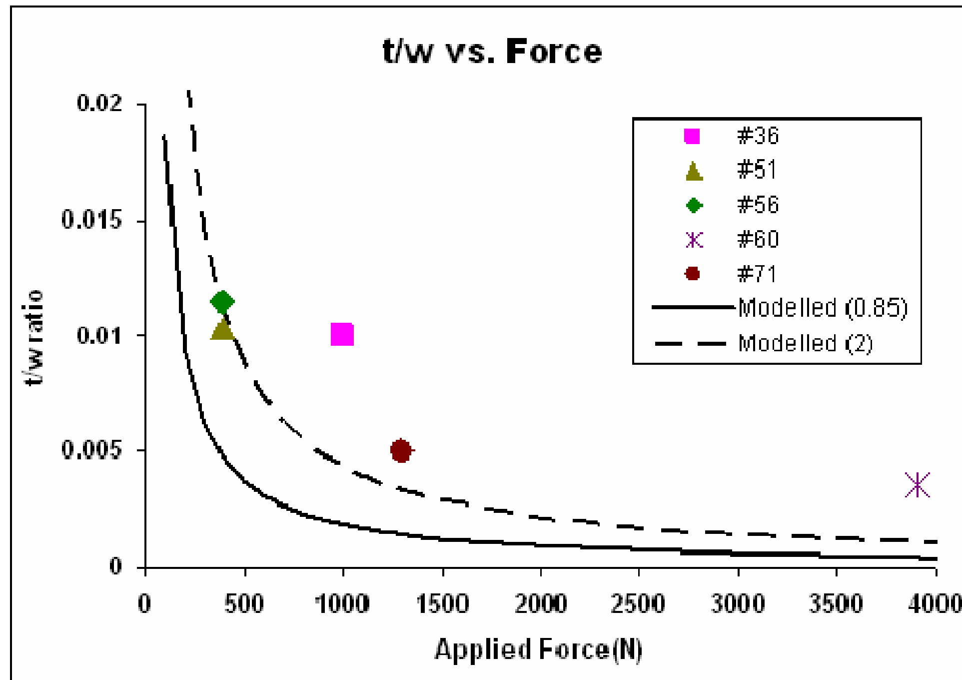


Figure 2.29: A graph of t/w vs. the applied force for several of the bonds discussed in section 2.6.2 and the modeled t/w vs. the applied bond force assuming a contact angle of 152° and a surface tension of 0.85 and 2 N/m.

Table 2.29: The applied bond force and measured thicknesses and widths for bond rings after bonding for the bonds graphed in Figure 2.52.

Bond #	Bond Force	Initial Bond ring Thickness	Final Bond Ring Thickness	Observed final cross-sectional width	thickness/width
36	1000N	3.5 µm	3.5 µm	350 µm	0.01
51	390N	3.5 µm	3.1 µm	300 µm	0.010333
56	390N	8 µm	5.1 µm	445 µm	0.011461
60	3900N	8 µm	2.5 µm	700 µm	0.003571
71	1300N	4 µm	1.5 µm	300 µm	0.005

2.6 Summary of Bond Parameters

The requirements for uniform/strong bonds were discussed in three parts: Sections 2.3 explained the material requirements for Au-Si eutectic bonds, Section 2.4 described the bond recipe, and Section 2.5 explained specific issues in regarding the Au-Si alloy lateral flow.

As was outlined Sections 2.3, cap wafers with Au bond rings were fabricated for bond experiments to: un-doped poly-Si, heavily phosphorous doped poly-Si and gold thin films. Figure 2.30 summarizes some of the material selection and fabrication

films. Figure 2.30 summarizes some of the material selection and fabrication requirements for achieving uniform/strong bonds.

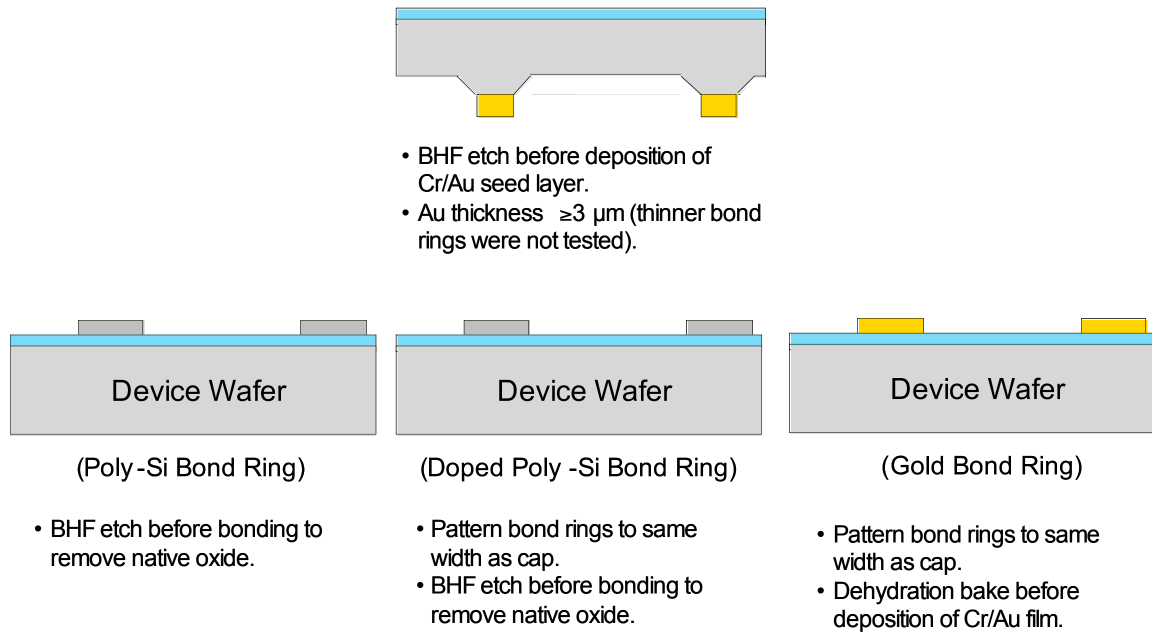


Figure 2.30: A summary of the material requirements for bonds between a cap wafer with a Au bond ring and a device wafer with: an un-doped poly-Si thin film, a heavily phosphorous doped poly-Si thin film and gold thin film.

As was summarized in Section 2.4, there were 4 key steps in the bond recipe: i) vacuum was applied, ii) the wafers were heated up to the outgassing temperature, iii) contact was made and the bond force was applied, and iv) the wafers were heated up to the bond temperature. Figure 2.31 summarizes some of the requirements for each of these steps in the bond recipe.

i) Applied Vacuum	ii) Outgassing Step	iii) Contact/ Bond Force	iv) Bond Temperature
• Needed to prevent SiO_2 formation on Au.	• Needed for achieving lower packaged pressures (more details given in Chapter 5).	• Best results at ~2.5 MPa bond pressure. • Bond pressure should be applied before going above the eutectic temperature	• Good results were achieved with temperatures from 390-410°C. • Lower temperatures and shorter hold times could be investigated.

Figure 2.31: A summary of the important parameters in the bond recipe.

Finally, as was outlined in Section 2.5 the amount of Au-Si eutectic lateral flow depended on several factors including: the thickness of the Au bond ring, the amount of bond pressure applied and the geometry of the bond joint (i.e. whether or not there was an anisotropically etched cavity). The following bullets summarize the important points from that section:

- Larger bond pressures and thicker initial Au bond ring widths cause more lateral compressive flow.
- A thin layer <50nm of Au-Si eutectic was observed to spread hundreds of microns laterally on a poly-Si surface during bonding.
- Au-Si eutectic tended to flow into the adjacent anisotropically cavity causing more compressive Au-Si eutectic flow.
- The amount of Au-Si eutectic flow could be roughly estimated taking into consideration force balance equations involving the surface tension and the contact angle of the Au-Si eutectic.

CHAPTER 3

WAFER LEVEL PACKAGING USING AU-SI EUTECTIC BONDING

This chapter presents the fabrication process for the cap and device wafers used for characterizing the vacuum integrity of packages in the Au-Si eutectic wafer bonding process. The processes outlined in this chapter take into consideration all of the processing constraints laid out in Chapter 2.

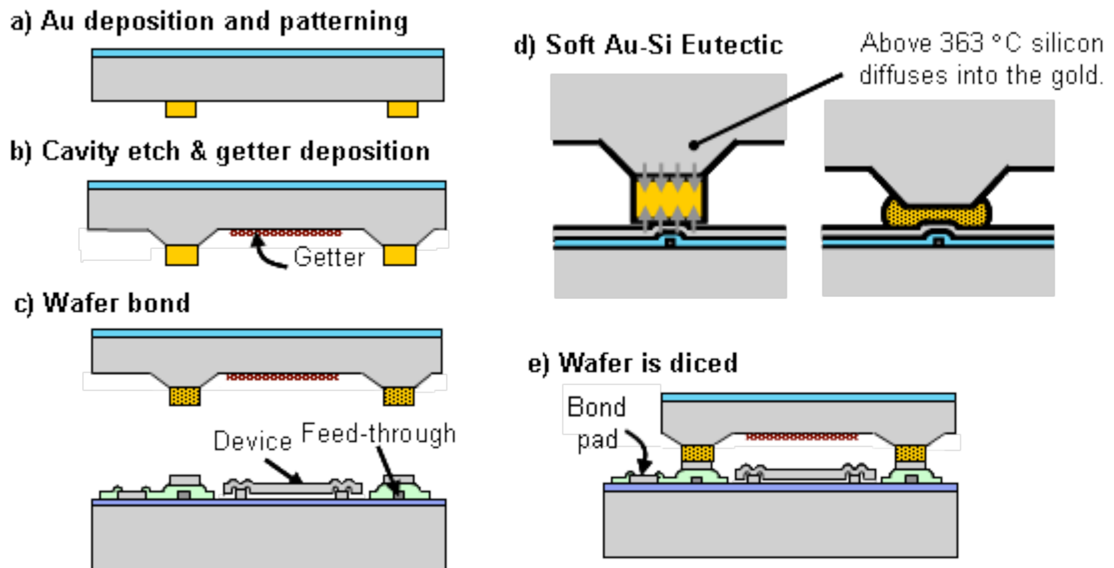


Figure 3.1: The Au-Si Eutectic bonding process.

Figure 3.1 shows the basic steps used in the full Au-Si eutectic packaging process where a gold thin film is first deposited on a silicon substrate via a chromium adhesion layer (Figure 3.1a), a cavity is micro-machined and a thin film getter is deposited inside of the cavity (Figure 3.1b). Next the wafers are brought together (Figure 3.1c) and the

temperature is raised above the eutectic temperature (~363ºC) so that silicon diffuses into the gold layer allowing for the formation of a soft Au-Si eutectic layer (Figure 3.1d). This soft eutectic layer conforms over non-planar features such as electrical feed-through interconnects on the device wafer substrate—thus allowing for a vacuum tight seal. Finally, part of the top wafer is sawed away allowing access to the bond pads for electrical interconnection (Figure 3.1e).

This process allows for encapsulation of devices on a wide range of substrates, including those fabricated in CMOS or CMOS like processes. As an example, Figure 3.2 shows a schematics of the SUMMiT V^{TM} process from Sandia National Laboratories which is a process similar to many CMOS processes. The SUMMiT V^{TM} process consists of multiple stacks of Si_3N_4, SiO_2 and poly-Si thin films, with a top metallization interconnection layer (often aluminum). Figure 3.2b and Figure 3.2c show two approaches for packaging a device fabricated in this process. In the first case as illustrated in Figure 2.2b, bonds could be made directly to one of the poly-Si layers. In the second case, a Cr/Au layer could be deposited onto a device wafer in the last several steps of processing. This approach is particularly desirable because it allows for the packaging of devices fabricated on a wide variety of substrates. Chromium and gold are particularly desirable material sets because both of these materials have negligible etch rates with nearly all common etchants used for device release including hydrofluoric acid (HF), potassium hydroxide (KOH) and xenon difluoride.

In the vacuum packaging experiments conducted here, three different material sets were explored for device encapsulation: 1) bonds between a Au-Si layer and a 0.3 μm un-doped poly-Si thin film, 2) bonds between a Au-Si layer and 2.2 μm heavily phosphorous doped poly-Si thin film and 3) bonds between a Au-Si layer and a Cr/Au thin film. The rest of this chapter outlines the processing done for these wafers used for device packaging.

Section 3.1 outlines the cap fabrication process and Section 3.2 outlines the various device wafer processes. Section 3.3 explains the processes used for device release (additionally

Appendix 4 describes some bond results and yield reduction which resulted from the release process). Section 3.4 presents the bond ring and device wafer layout. Finally,

Section 3.5 explains the bond preparation and reviews the wafer bonding process developed in Chapter 2.

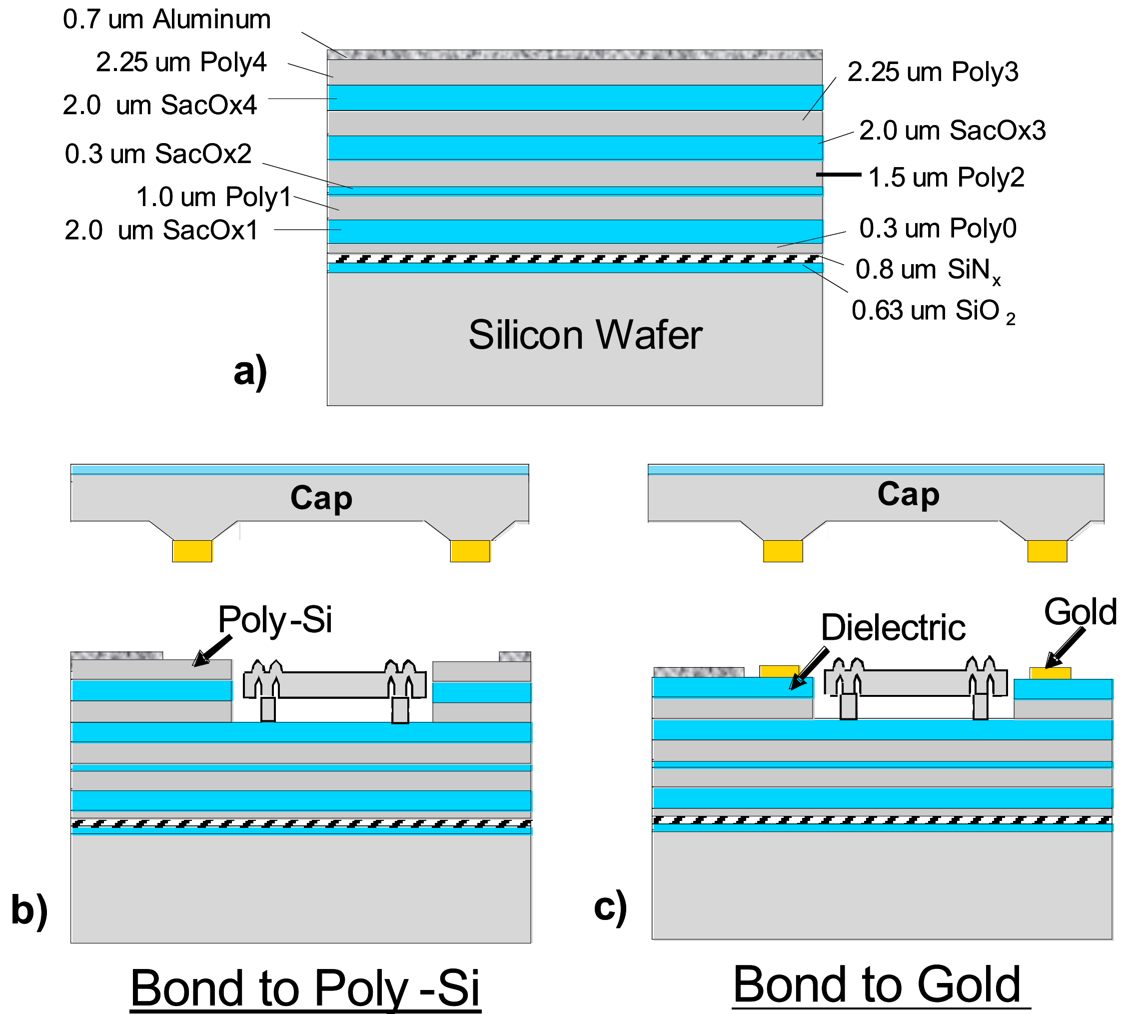


Figure 3.2: a) The SUMMiT V™ thin film stack as an example of a CMOS process, b) bonding to the Poly-Si in this thin film stack and c) bonding to gold layer deposited on top of this thin film stack.

3.1 Cap Wafer Fabrication

Figure 3.3 summarizes the process steps for fabricating the cap wafer. The process begins with growth of a 1.9 µm thick thermal SiO_2. This thermal SiO_2 is removed from the front side of the wafer using BHF (buffered hydrofluoric acid), masking the backside with photoresist. Such a thick SiO_2 layer was used to protect the backside of the wafer from a potassium hydroxide (KOH) etch in a later step. Directly after this BHF etching

step, 200/5000 Å angstroms of chromium/gold was evaporated on top of bulk silicon, acting as the ***seed layer*** for electroplating. These metals were deposited in an E-beam Enerjet evaporator at ~2×10^{-6} Torr. The BHF dip preceding the evaporation step was to ensure that the Cr/Au layer was directly in contact with the bulk Si and that a thick native oxide would not prevent inter-diffusion. Generally the wafers were inside of the evaporation vacuum chamber within 15 minutes of the BHF dip. A 15 minute exposure to air should result in approximately 2 Å of oxide [181].

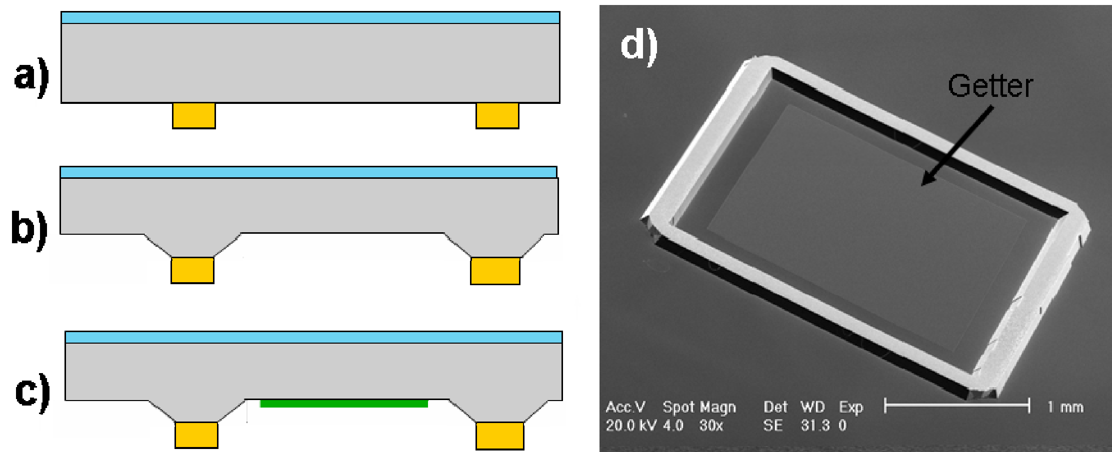


Figure 3.3: A summary of the bond ring fabrication process where a) the bond rings are patterned and electroplated, b) the cavity is KOH etched and c) the getter is patterned and deposited. d) An SEM of a fabricated 150µm which encircles a getter.

Next, 10 to 20 microns of AZ 9260 photoresist was deposited and patterned, acting as a mold for the Au electroplating. Electroplating was done using BDT-510 makeup plating solution with a stainless steal cathode on one side of the bath and the wafer on the other side serving as the anode. A current source was used to supply the source current with the cathode attached to the positive side and clips touching the top of the wafer were connected to ground. A current density of 2mA/cm^2 resulted in a plating rate of around 0.1 µm per minute (the wafers with 300 µm wide bond rings for example had an exposed surface area of ~3.75 cm^2 and therefore a supply current of 7.5mA was used). For the device bonds, the electroplated thicknesses ranged from 4 to 6 µm. This thickness range was determined to be optimum from bond experiments which are detailed in Chapter 2. Half of the electroplating was done with the electrodes connected near the wafer flat and the other half with the wafer flipped around and the electrodes connected near the top

edge of the wafer. In some cases, failing to flip the wafers midway through electroplating resulted in bond rings which were 20% thicker near where the electrodes were connected as compared to those on the farthest edge. Flipping the wafers half way through the electroplating process resulted in bond rings with an average bond ring thickness that was consistent across the wafer to with in ±5-10%.

After electroplating the photoresist mold was removed in PRS2000 and the entire wafer was placed first in Type TFA Au etchant for ~2 minutes and then in CR-14 chromium enchant for ~30 seconds in order to remove the seed layer. The Au etch attacks the electroplated Au at roughly the same rate as the seed layer gold and therefore only about 0.5µm of electroplated Au got etched. Next, directly after a 30 second etch in 10:1 H_2O:HF the cap wafer was placed in a KOH bath at 90ºC resulting in an etch rate of ~1.1 µm per minute. Sixty to ninety micron cavities were etched and the sloped sidewalls shown in Figure 3.3b and Figure 3.3d resulted from this anisotropic etch. Because the Cr and Au are inert to both HF and KOH, they did not need to be masked during this process step. An alternative to KOH etching would be to use deep reactive ion etching (DRIE) for patterning of the cavities.

The final step was the deposition of the getter (Figure 3.3c). Nanogetters™ [5, 6, 150] from Integrated Sensing Systems, Inc. (ISSYS, Inc.) were chosen as the gettering material. This thin layer was deposited and patterned either using a *lift off* or a *shadow mask* process. For the *lift off* process, 20 µm of AZ 9260 was spun on and then patterned. The wafers were then sent to ISSYS, Inc. so that the getter could be deposited. The wafers were then placed in a beaker with acetone and the beaker was placed in an ultrasonic bath for 10 to 20 minutes. This removed the photoresist, pulling off the Nanogetters™ in areas which were not patterned. Using the *shadow mask* method, a separate silicon wafer was patterned and then through wafer etched using an STS Multiplex ICP DRIE. This wafer was then aligned to the cap wafer and clamped using metal clips and given to ISYSS for Nanogetters™ deposition. After the deposition of the Nanogetters™, only solvent cleans could be applied to the cap wafer because of material incompatibility issues with aggressive cleans such as Piranha or an RCA clean.

3.2 DEVICE WAFER FABRICATION

It was desirable to evaluate the bond quality (and eventually vacuum integrity) when bonding to Au and poly-Si bond rings of varying thicknesses and dimensions. To accommodate these materials and differing thicknesses into a process with insulated feed-throughs and a poly-Si device layer, three different processes were developed. In processes #1 and #2, 0.3 and 2.2 μm thick poly-Si bond rings were used, respectively, and in process #3, a 0.5 μm gold bond ring was used. As a result, three different process flows were used for the fabrication of "dummy" device wafers. As shown in Figure 3.4, these processes result in a 3000 Å poly-Si feed-through layer, a poly-Si or Au bond ring layer, a 3000 Å Si_3N_4 layer—which insulates the feed-through layer from the bond ring layer—and a 2.2 μm thick device layer in which Pirani gauges or micro-resonators could be formed.

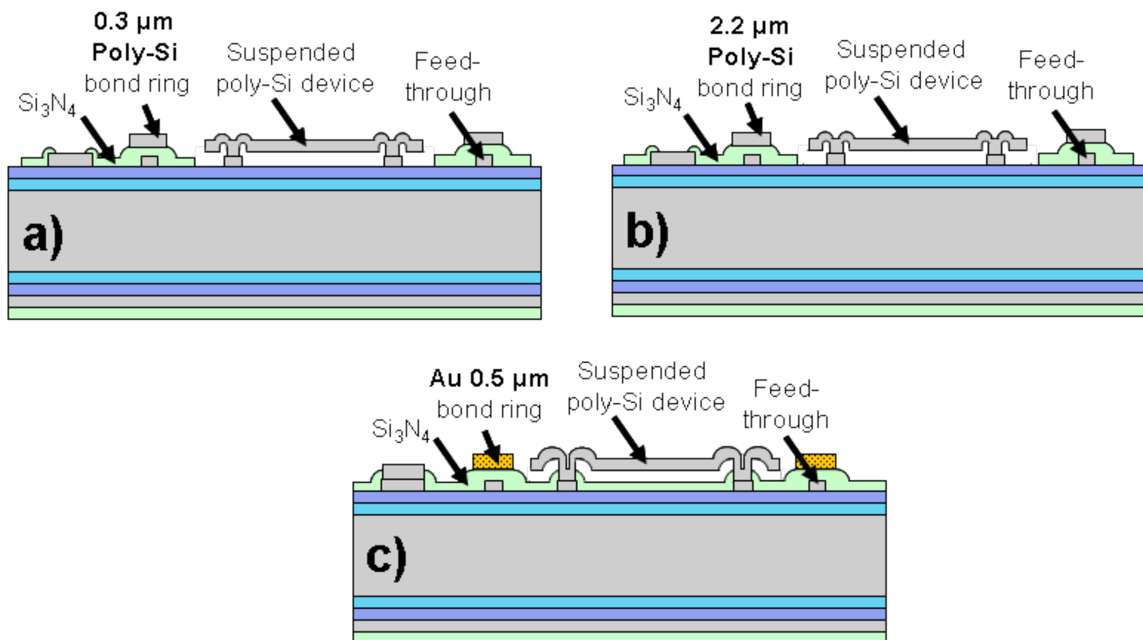


Figure 3.4: The final structure of the device wafers for a) process #1 with a 0.3 μm thick poly-Si bond ring, b) process #2 with a 2.2 μm thick poly-Si bond ring and c) process #3 with a 0.5 μm thick Au bond ring.

Figure 3.5, Figure 3.6 and Figure 3.7 summarize the process steps for processes #1, #2 and #3 including the processing gasses, pressures and growth/etch rates for all of the furnace and etching steps.

Process #1 started with the growth of a 1.9 μm thermal SiO_2 and deposition of 1000 Å of low pressure vapor deposited (LPCVD) Si_3N_4. Such a thick dielectric stack was

chosen because this process was designed to accommodate micro-resonators which need to be well insulated from the Si substrate because of parasitics (micro-resonators were in fact fabricated in this process but not tested). These layers were used for electrical insulation from the substrate. A 3000 Å layer of low stress LPCVD poly-Si was next deposited, followed by a heavy phosphorous doping step. This poly-Si layer was patterned to form the anchors, feed-throughs and bond pads (Figure 3.5, step 1) and had a sheet resistance of approximately 35 Ω/square. Next another 3500 Å of LPCVD Si_3N_4 was deposited for passivation of the feed-through layer and then a 3500 Å layer of LPCVD poly-Si was deposited. The poly-Si layer was then patterned/etched to define the bond ring layer (Figure 3.5, step 2) and then the Si_3N_4 was patterned/etched (Figure 3.5, step 3). After this, a 3 μm layer of LPCVD SiO_2 was deposited (Figure 3.5, Step 4) and patterned to define the sacrificial layer. Next, roughly 2.2 μm of LPCVD poly-Si was deposited, heavily doped and patterned—this defined the device layer (Figure 3.5, Step 5). This layer had a sheet resistance ranging from 14-16Ω per square. Finally, the wafers were soaked in BHF for 30 minutes in order to undercut the poly-Si Pirani gauge structure. (Stoichiometric Si_3N_4 has an etch rate of approximately 9 Å/minute in BHF so that the 3000 Å thickness of Si_3N_4 was more than adequate to hold up to the final 30-minute BHF etch so that the feed-throughs stayed electrically isolated from the bond rings). Without letting the wafers dry, the devices were rinsed, soaked in methanol and then either dried on a hotplate or dried using a critical point drying (CPD), leaving the suspended Pirani gauge structure (Figure 3.5, Step 6). More details on the release process will be given in Section 3.3 (*Device Release*).

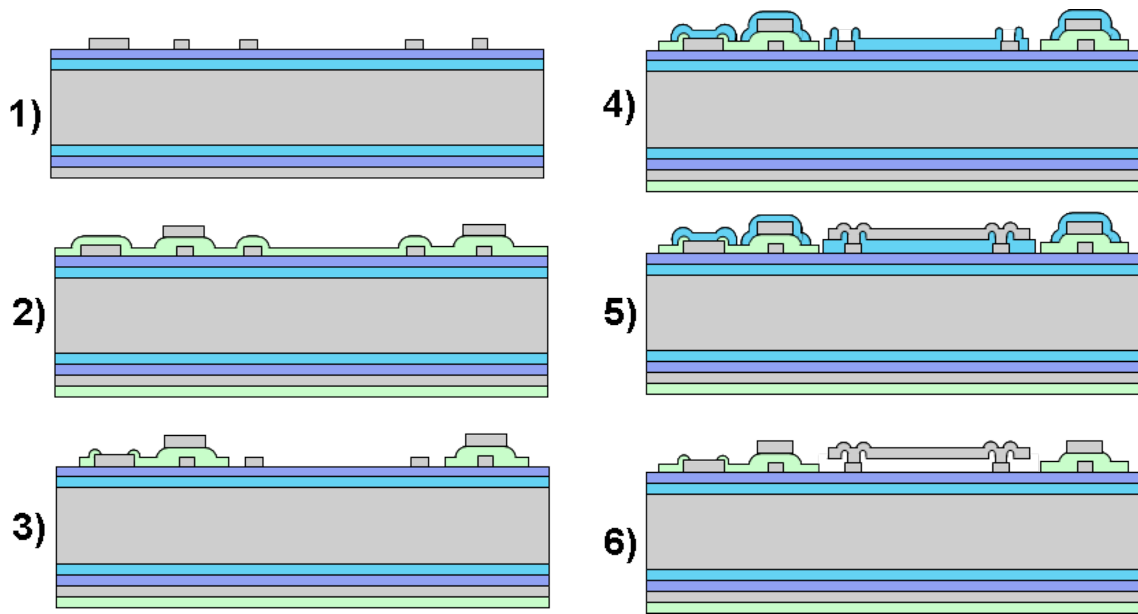


Figure 3.5: The process steps for process 1 with 0.3 μm thick poly-Si bond rings included: 1) the deposition of dielectrics and the poly-Si used for the feed-throughs, 2) deposition of the Si_3N_4 later that insolated the feed-throughs and deposition and patterning of the poly-Si bond ring, 3)patterning of the Si_3N_4 layer, 4) deposition and patterning of the sacrificial layer, 5) deposition and patterning of the device layer, and 6) release of the device.

As shown in Figure 3.6, process #2 is a shorter than process #1 because the poly-Si layer was used for both the device layer and the bond ring. As in Process #1 this process started with a 1.9 μm thermal SiO_2 and 1000 Å LPCVD Si_3N_4 layer is first deposited followed by a 3000 Å layer of low stress LPCVD poly-Si and a heavy phosphorous doping step. This poly-Si layer was patterned to form the anchors, feed-throughs and bond pads (Figure 3.6, step 1). Next both the 3000Å Si_3N_4 insulation layer and the 3 μm SiO_2 sacrificial layer were deposited and patterned in order to open access to the feed-through layer (Figure 3.6, step 2). The 2.2 μm poly-Si device/bond ring layer was then deposited and patterned (Figure 3.6, step 3). Finally, as in process #1, the devices were released by soaking them in BHF for 30 minutes, then rinsed in water, soaked in methanol and then either dried on a hotplate or using CPD (Figure 3.6, Step 4).

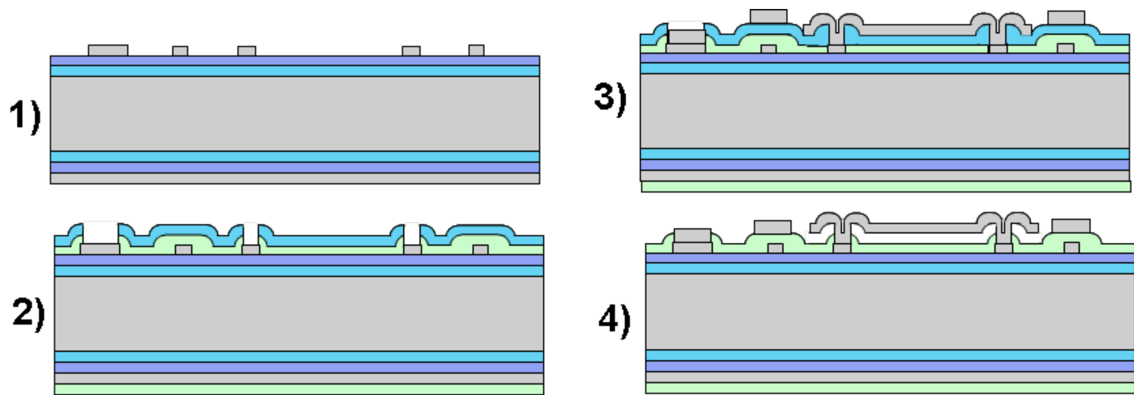


Figure 3.6: The process steps for process 2 with 2.2 μm thick poly-Si bond rings included: 1) the deposition of dielectrics and the poly-Si used for the feed-throughs, 2) deposition and patterning of the Si_3N_4 insulation layer and the SiO_2 sacrificial layer, 5) deposition and patterning of the device layer, and 6) release of the device.

Figure 3.7 shows process #3, in which 0.5 μm thick Au bond rings were used. As illustrated, steps 1 and 2 are identical to those explained for process #2 (Figure 3.7, Steps 1 and 2). Next, the 2.2μm LPCVD poly-Si device was deposited and patterned (Figure 3.7, Step 3). A dehydration bake was then conducted in an oven at 110ºC for 30 minutes (the need for this dehydration bake was explain in Section 2.3.5 of Chapter 2), directly after which the wafers were transferred directly into the Energet Sputter coater for the deposition of 500/5000Å of Cr/Au. After patterning this layer, it was etched using type TFA Au etchant for 2 minutes and Cr-14 Chromium etch for 30 seconds (Figure 3.7, Step 5). These layers were sputtered because bonds were being conducted over top feed-throughs and sputtering is a more conformal deposition process than evaporation. After this, a 10 μm layer of AZ 9260 photoresist was spun over the Cr/Au layer to isolate the Cr/Au layer for the BHF etch. This was used to prevent galvanic etching of the *poly-Si* device. (In one of the first device releases using Au bond rings, after the BHF sacrificial etch, most of the poly-Si devices were etched away. This was observed even though the Au bond rings were not in contact with the poly-Si device.) The final step as in processes #1 and #2 included a BHF etch for 30 minutes, then a water rinse. In process #3 it was next necessary to do a 5 minute acetone soak to remove the photoresist, then a 2 minute soak in isopropanol, then a 2 minute water rinse to remove any acetone scum. Finally, as in processes #1 and #2, the wafers were soaked in methanol. Last, as in the other two processes, the wafers were either dried on a hotplate or using CPD (Figure 3.7, Step 6).

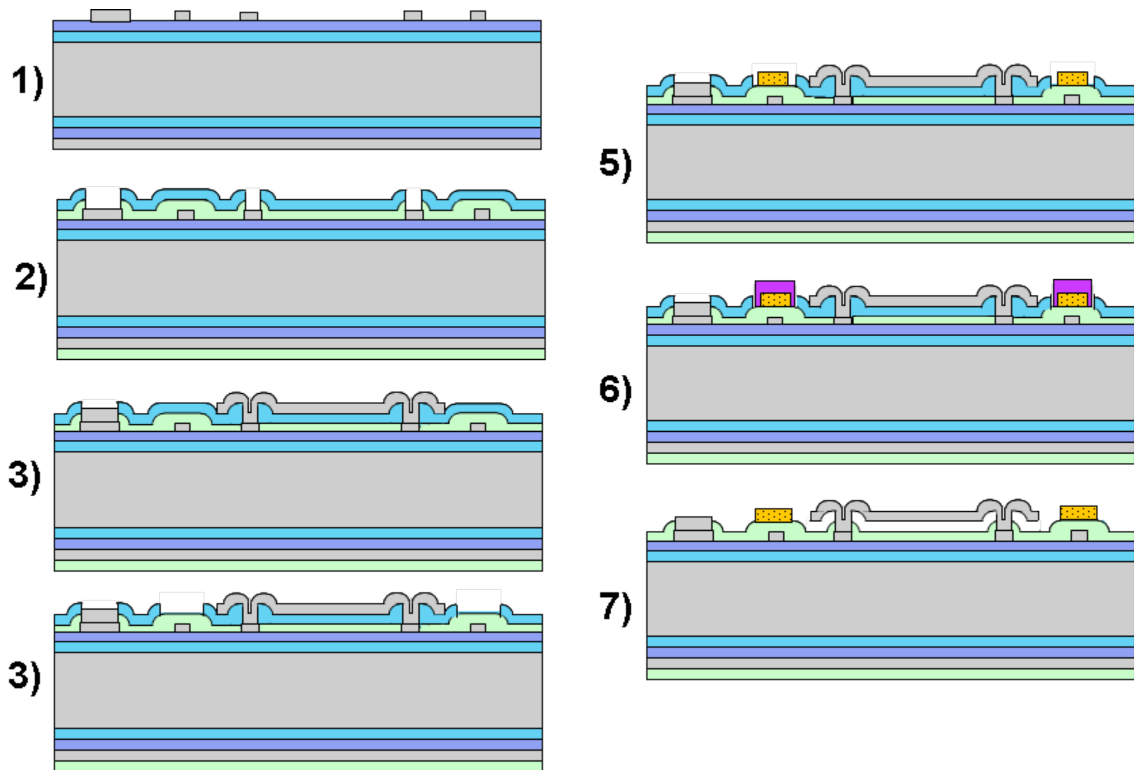


Figure 3.7: The process steps for process 3 with 0.5 μm thick Au bond rings included: 1) the deposition of dielectrics and the poly-Si used for the feed-throughs, 2) deposition and patterning of the Si_3N_4 insulation layer and the SiO_2 sacrificial layer, 3) deposition and patterning of the device layer, 4) another patterning step on the sacrificial layer, 5)deposition of the Cr/Au bond ring, 6) deposition and patterning of a photoresist protective layer and 7) release of the device followed by removal of the photoresist layer.

3.3 Device Release

As described in the previous section, the release process began by first etching away the sacrificial SiO_2 layer in BHF and after a series of steps soaking them in methanol. After this soak, the wafers were either dried on a hot plate or placed in a CPD in order to conduct critical point drying.

3.3.1 HOT PLATE RELEASE

Methanol has a surface tension of around 22.6×10^{-3} N/m as compared to the surface tension of water which is 72.8×10^{-3} N/m. Evaporating away methanol therefore allowed for more fragile structures to stay freestanding as supposed to pulling down and sticking to the substrate because of these lower surface tensions. CMOS grade methanol is

generally more than 99.8% pure. Even so, as shown in Figure 3.8a and Figure 3.8b, if not dried quickly, a residue collected on the surface of the wafer. This resulted in bad bonds and non-functional devices. This residue could consist of the ≤0.2% impurities in the methanol or of impurities that collect in the methanol during processing.

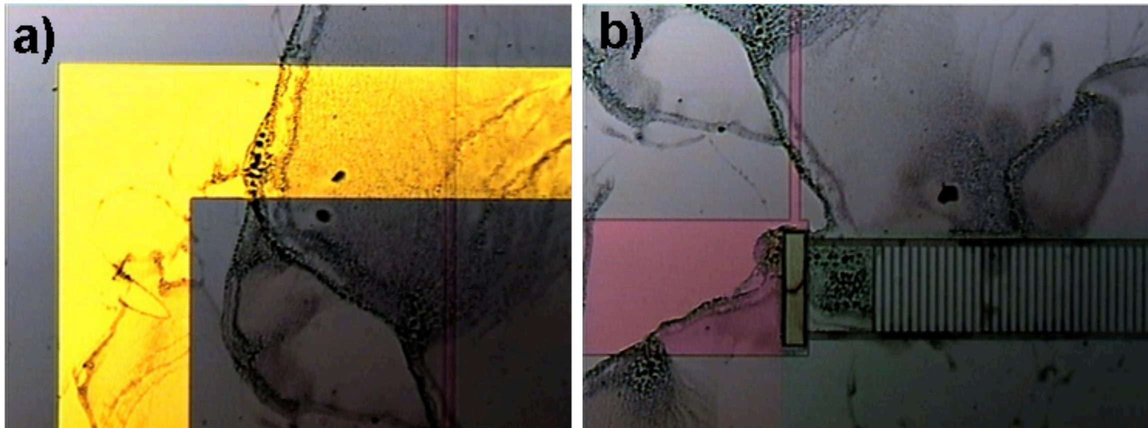


Figure 3.8: Scum left over after the release process on a) a bond ring and b) on a device.

It was observed experimentally that during release, as methanol dissolved from the wafer, this residue tended to accumulate in the last portions to dissolve from the wafer. Therefore, it was desirable to evaporate off methanol from the center of the first. To accomplish this, the device wafer was taken directly out of methanol and placed on a hot plate at 115ºC for about 20 seconds. In order for the methanol to dry quickly from the center of the wafer, very good thermal contact needed to be made between the hotplate and the back surface of the wafer. Therefore, it was necessary to quickly wipe off the backside of the wafer with a wipe before placing it onto the hotplate. If done correctly, methanol scum only accumulated around the periphery of the wafer.

Inevitably using this process, some residue did accumulate on the surface of the wafer.

Appendix 4 discusses how this methanol residue affected the bond quality in several device wafer bonds.

3.3.2 CRITICAL POINT DRYER (CPD) RELEASE

As compared to water or even methanol, liquid CO_2 has an even lower surface tension of around 5×10^{-3} N/m. Soaking devices in liquid CO_2 and taking liquid CO_2 straight to

its gas phase therefore allows for even more fragile devices to get released without pulling down to the substrate. A critical point dryer (CPD) allows for devices to be released in such a manner.

The CPD is a small pressure chamber which allows for liquid CO_2 to be pumped in. When using the CPD for release, dies or wafers were first place inside of the chamber soaking in a small amount of methanol. These soaking dies or wafers were then cooled to below 5ºC at a pressure of 1350 pounds per square inch (psi). Liquid CO_2, which remains in its liquid state at this temperature and pressure, was then pumped into the chamber from a CO_2 cylinder. This liquid CO_2 was used to flush out the methanol. Next, the pressure inside of the chamber was slowly raised so that the CO_2 changed directly to its gas phase.

Initially there were difficulties with an organic, solvent or other residues spreading across the entire wafer when using the CPD. The cause of this residue was not entirely evident. In later release experiments (and subsequent bond experiments) a methodology was developed to eliminate this residue. First, it was important to clean the CPD chamber before releasing devices in case previous users had placed "dirty" wafers (with photoresist or other organic residues) into the tool directly before release. The best way to clean the chamber before use was to run the CPD process with a clean "dummy" wafer. It was also important to orient the wafers upside down inside of the chamber. This was accomplished by placing the wafer face down in the chamber on top of an O-ring. This was necessary because a thin residue (which could be a solvent, organic or other type of residue) was observed to accumulate on the top surface.

Though there were initial problems with cleanliness using CPD, with careful preparation using critical point drier as supposed to a hotplate release actually resulted in a much more repeatable and clean wafer surface to bond to. The bond yield results presented in Chapter 5 reflect this.

3.4 BOND RING & DEVICE LAYOUT

Figure 3.9a shows a wafer with 124 vacuum encapsulated devices and Figure 3.9b show a close up view of one of the packages. Figure 3.9c shows an SEM image of one of these packages which was sawed in half in order to view a cross section of the package.

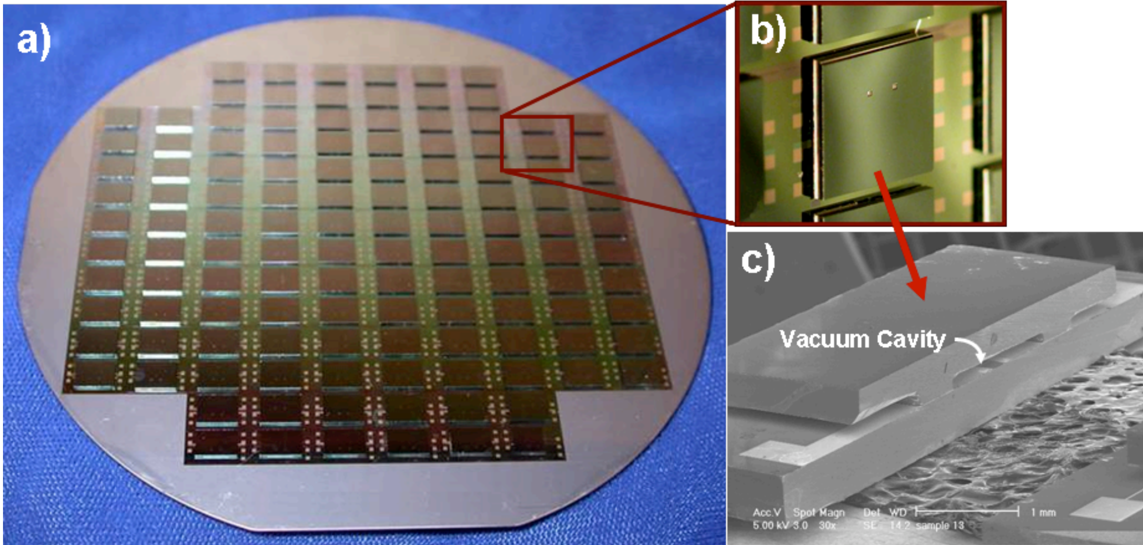


Figure 3.9: a) A wafer with 124 vacuum encapsulated devices, b) a closer view of one of the packages and c) an SEM of a diced package showing the micro-vacuum cavity.

Figure 3.10 shows a close up view of a package where the dotted lines show the location of the 300 µm wide bond ring which encompassed a 2.3 by 2.3 mm area. On the cap wafer, bond rings 300, 150, 100 and 50 µm wide were experimented. For bond tests, in some cases a much wider bond ring was used on the device wafer (500 µm wide) to increase the wafer alignment tolerance. In many cases it was preferable to make the bond ring widths the same on the cap and device wafers (as will be discussed in Chapter 2). The alignment tolerance on the SUSS SB6 bond aligner ranged from ±5 to ±20 µm and therefore was not a significant issue for larger bond ring widths (a more detailed discussion on bond alignment and the fixtures used for alignment and bonding are given in Appendix 2).

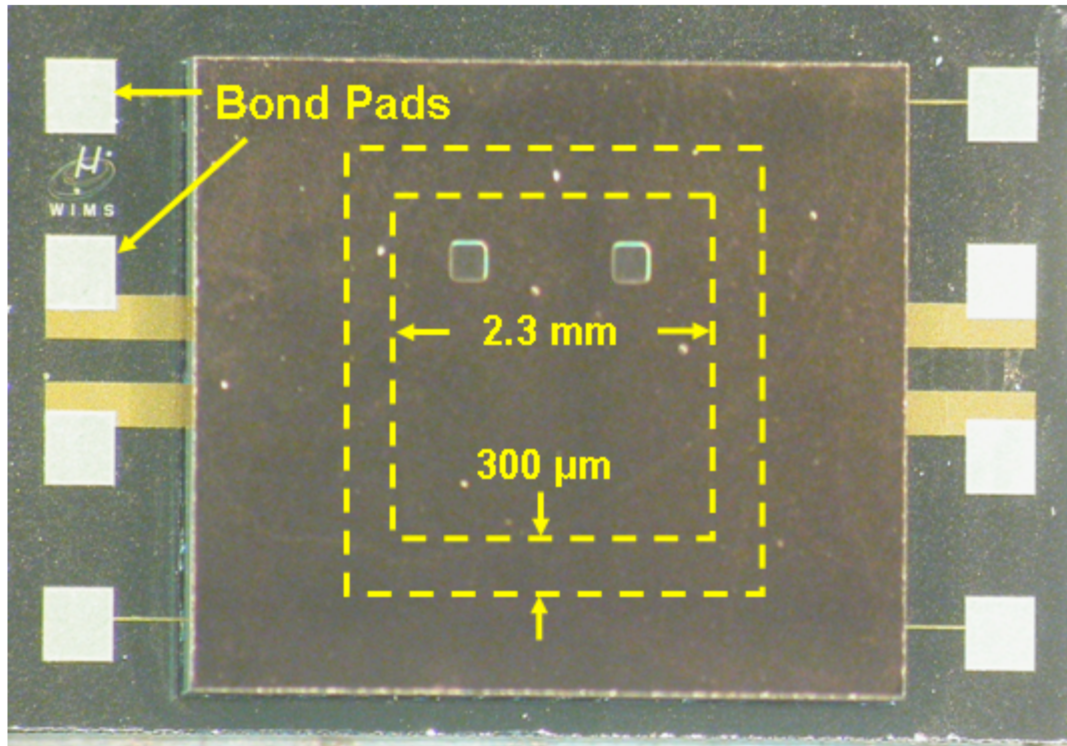


Figure 3.10: a) A top view of one of the caps showing the bond ring dimensions and the bond pads used for interconnection.

Figure 3.11a shows an SEM of a package where the Au-Si eutectic was re-melted on a hot plate and the cap pulled off showing the sensors (Pirani gauges in this case) which the melted bond ring encircled. As shown in the SEM photograph, the feed-through interconnects run underneath the bond ring, electrically connecting the bond pads to the sensors. Figure 3.11b and Figure 3.11c show a close-up of these feed-throughs. As explained in the previous section these feed-through interconnects are insulated by a 3000Å layer of Si_3N_4 which prevents the feed-throughs from electrically shorting to the bond ring.

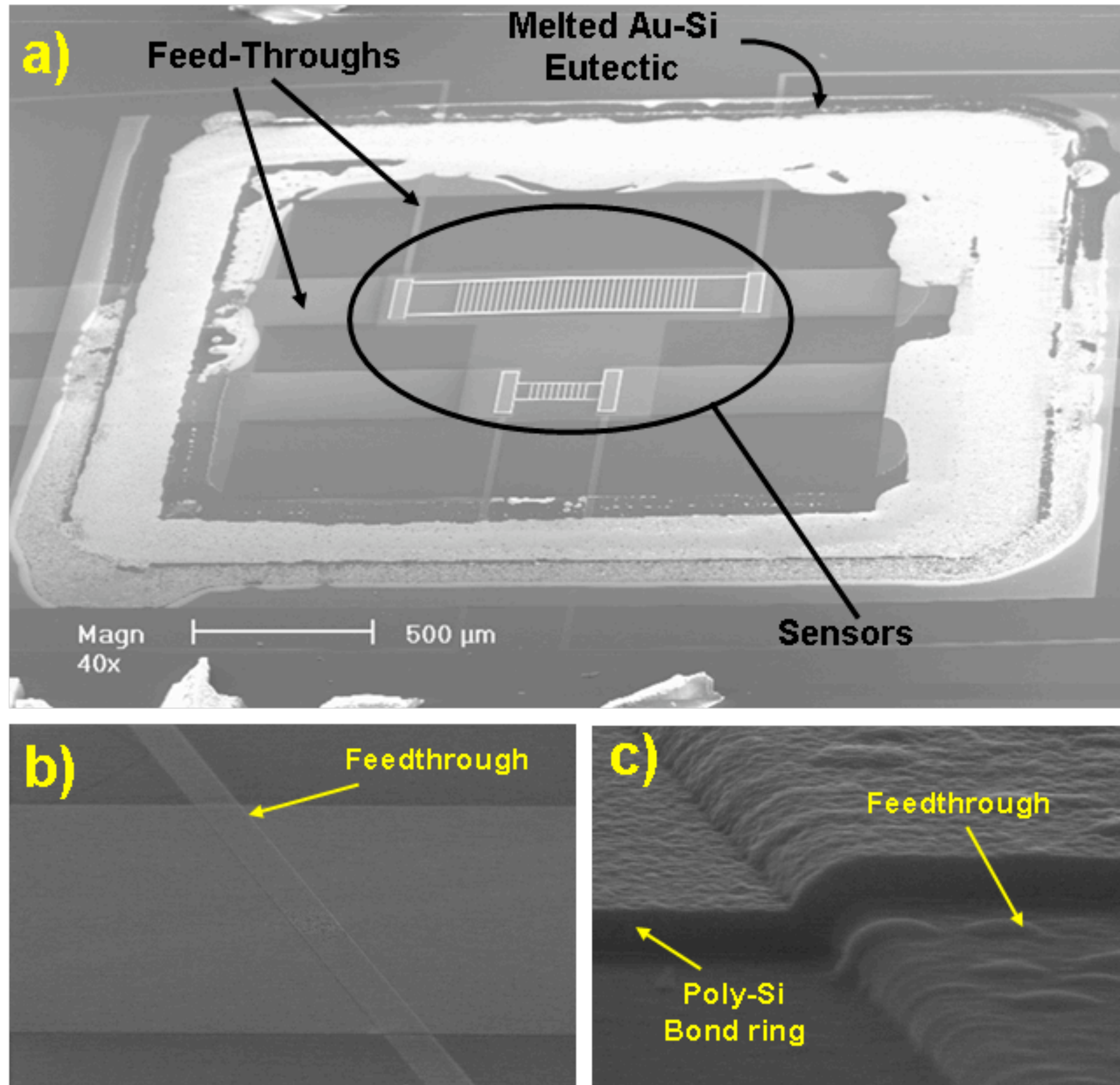


Figure 3.11: a) A closer view where the Au-Si eutectic has been melted in order to remove the cap, b) an SEM of on of the feed-throughs running underneath a feed-through and c) a closer look at one of the feed-throughs.

3.5 Wafer Preparation for Bonding

Directly before each bond, both the cap wafer and device wafers were cleaned. In each case where getters were *not used,* the cap wafers were Piranha cleaned (an aggressive chemical clean where the wafers are dipped in an approximately 1 to 1 mixture of sulfuric acid and hydrogen peroxide) for 10 minutes in order to remove organic particles that could compromise the bond quality. Wafers in which

Nanogetters^{TM} were used on the cap wafer could not be exposed to a Piranha clean because of material incompatibility (as specified by ISSYS, Inc.). A solvent clean instead was used where the cap wafer was first dipped into acetone for 2 minutes, dipped in isopropanol for 2 minutes, rinsed in water for 5 minutes and then dried. It was important to transfer the wafers quickly from the acetone to the isopropanol and then to the water rinse so that a residue did not accumulate from the solvents.

For the device wafers, a Piranha clean was always conducted directly before the release process. In the wafers which had poly-Si bond rings, the native oxide on the poly-Si bond ring got etched during the 30 minute BHF release. Bonds were conducted anywhere from several minutes to several hours after this wafer preparation.

Cap and device wafer alignment was done using the SUSS microTec SB6 wafer alignment system. This alignment system allowed for alignment tolerances anywhere from ±5 to ±100 μm. After the alignment, the wafer which were then clamped into the alignment chuck, were transferred into either the SUSS microTec SB6 or SB6e bond chamber for bonding. More details on this bond chuck and bond chamber are presented in Appendix 2.

Finally, Figure 3.12 summarizes the bond recipe used for vacuum packaging device wafers. This process involved: i) pumping down the bond chamber to around 10×10^{-6} Torr; ii) heating both the *bottom heater* and *top heater* to 345ºC and hold for 1 hour in the *outgassing step*; iii) making physical contact between the wafers by removing the spacers, then applying the bond force was applied, and the clamps holding the wafers together; and iv) raising the temperature to the *bond temperature* which ranged from 390 to 410ºC and holding that temperature for 40 minutes. After running the bond sequence, the wafers were then cooled to below 200ºC at which point they were pulled out of the wafer bonder. In several of the bonds step 2, the outgassing step, was eliminated. The vacuum encapsulation data for these wafers is presented in Chapter 5

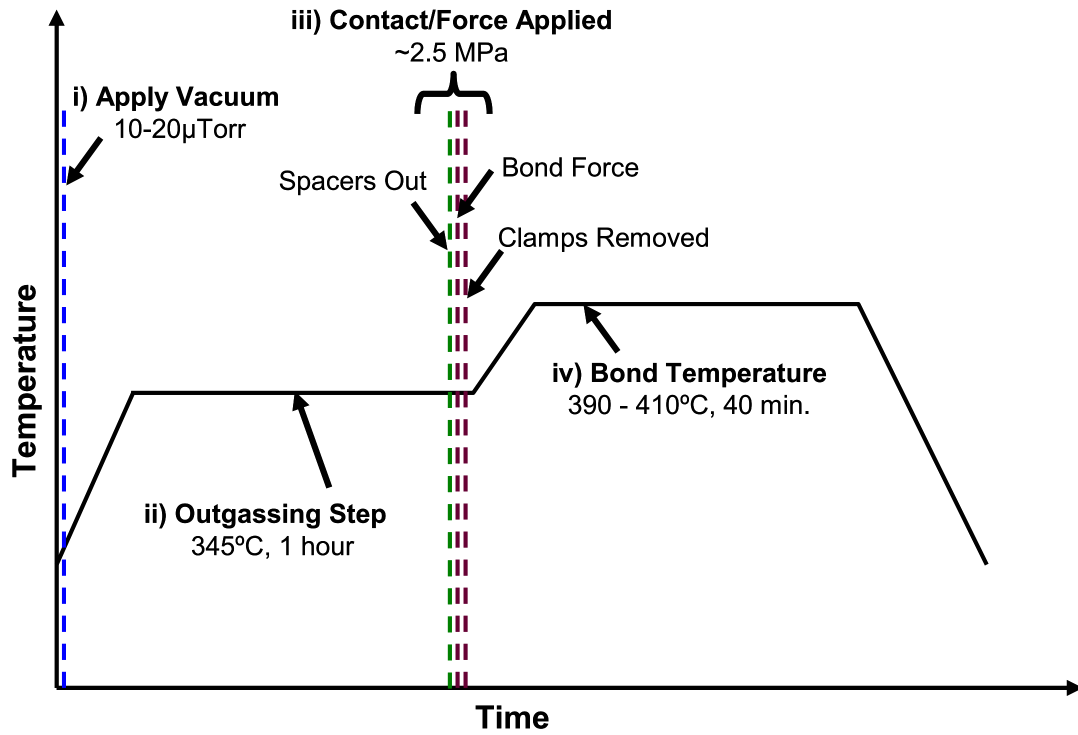


Figure 3.12: The bond process used for vacuum encapsulation of sensors (Pirani gauges) in Chapter 5.

CHAPTER 4

PIRANI (VACUUM) SENSOR DESIGN AND TESTING

This section presents the design and characterization of Pirani vacuum gauges used for characterization of vacuum/hermeticity. In Section 4.1 a brief discussion is presented on the methods available for vacuum/hermeticity characterization and on the motivation for use of Pirani gauges in this application. Section 4.2 provides a background on past Pirani gauge research, Section 4.3 outlines the Pirani gauge design, Section 4.4 explains some fabrication issues specific to these devices and in Section 4.5 the gauges are characterized. Finally, Section 4.6 explains the test methodology used for vacuum characterization.

4.1 METHODS FOR VACUUM/HERMETIC CHARACTERIZATION

4.1.1 LEAK RATE TESTERS

One of the more common methods for characterizing micro-packages involves using a leak detection setup. The specifications for such a leak detection setup are detailed in the Military Specifications titled: Department of Defense Test Method Standard for Microcircuits (Mil-Spec-883F method 1014.11) [185]. There are two types of tests specified, one for fine leak assessment and one for gross leak assessment. For the applications in this work, we are primarily interested in fine leak detection.

The leak test for fine leak assessment is called the Helium leak test. Using this test method the package is generally placed inside of a pressure chamber and pressurized to several atmospheres of pressure with helium and held for 2 to 10 hours. The necessary pressures and hold times are specified depending on the package size (anywhere from 0.5

to 10 cubic centimeters (cc)). The purpose of this He exposure is to force He atoms into the package through a leak path. After sitting inside of the pressure chamber, the packages are placed into another chamber with a He detector. An equation is given for determining the leak rate in MIL-SPEC-883F, for a given package volume, time and pressure inside of the He chamber. Details on the requirements for this test setup up are also given in MIL-SPEC-883F. The pass criterion for this test technique is a leak rate of less than 10^{-9} cc/s at atmospheric pressure and the minimum measurement resolution is generally no greater than 10^{-12} cc/s at atmospheric pressure.

4.1.2 PACKAGED SENSOR

Encapsulating a sensor inside of the micro-package is an alternative to trying to pass gases such as helium through the bond seal. Using this method, the pressure inside of a vacuum cavity is measured over a specified amount of time, *t*. Measuring the change of pressure, ΔP, knowing the volume, V, the leak rate can be determined:

$$Leak \quad Rate = \frac{\Delta P}{760 Torr} \cdot \frac{V}{t} \tag{4.1}$$

Although this takes a significantly more sophisticated package design, this is often practical since the end goal is generally to package some kind MEMS device and in some cases, a pressure sensitive MEMS device.

Resonators, micro-bolometers and Pirani gauges have all been used for micro-package characterization. Resonant devices (which include micro-resonators and gyroscopes) are often pressure sensitive due to squeeze film damping of the molecules in the atmosphere in which they resonate. The pressure sensitivity of the resonant device depends on its geometry and resonant mode. Lower frequency devices generally have larger amplitude vibration and are therefore more pressure sensitive, especially at pressures in the mTorr or even µTorr range. Unfortunately these types of devices can be difficult to calibrate and test.

Both Pirani gauges and micro-bolometers consist of suspended thin film resistors which heat up different amounts depending on how much heat conducts through the ambient air around them. Because micro-bolometer and Pirani gauges are essentially

suspended resistors, they are easy to design for measurement of specific pressure ranges from above atmospheric pressure (760 Torr), to the μTorr range. Pirani gauges are also easy to calibrate and test.

Tables 4.1 and 4.2 compare the resolutions of the He-leak rate test to the use of a packaged sensor. In these tables typical package volumes for several applications ranging from 0.0375 cm^3 down to 2.5×10^{-6} cm^3 are used. For these different package volumes, Table 4.1 shows how fine of a pressure change can effectively be measured in units of Torr/days (converted from a flow rate of cc/s at atmospheric pressure to units of pressure/day for the given package volume). As illustrated, the pressure measurement resolution gets worse as the package dimensions shrink. This is particularly important for applications that require vacuum pressures in the mTorr range. This is significant even for applications that simply require hermeticity where this amount of pressure change can represent a significant amount of moisture or other gasses that can deteriorate device performance.

Table 4.1: Typical package dimensions for different types of devices, and given the leak rate measurement resolution (10^{-12} cc/s) the amount of time it would take for the package to leak by 1 Torr with a leak rate of the 10^{-12} cc/s.

Type of Package	Package Dimensions	Package Volume	Measurement Resolution	Time for 1 Torr change in pressure
Chip Scale Package	5×5×1.5 mm	0.0375 cm^3	10^{-12} cc/s	47.6 days
Gyroscope (wafer-level)	2×2×0.3 mm	0.0012 cm^3	10^{-12} cc/s	1.52 days
Package in this work (wafer level)	**2.3×2.3×0.1 mm**	**5.3×10^{-4} cm^3**	**10^{-12} cc/s**	**0.67 days**
3-D Accelerometer (wafer level)	0.5×0.5×0.3 mm	7.5×10^{-5} cm^3	10^{-12} cc/s	0.10 days
Thin Film Package (wafer level)	0.5×0.5×0.01 mm	2.5×10^{-6} cm^3	10^{-12} cc/s	0.0032 days

Table 4.2 illustrates the advantage of using a sensor for characterization of package hermeticity/vacuum. Table 4.2 shows the same devices and device dimensions as were shown in Table 4.1, but characterized with a sensor that has a 4 mTorr resolution (as was used in much of this work). In each case, much finer leak rates can be detected. As illustrated, for the package dimensions used in this work, a leak rate measurement of 8.0×10^{-13} and 2.24×10^{-17} cc/s at atmospheric pressure can be measured in 1 day and 1

year of measurement respectively. This is several orders of magnitude better than the He leak test. As illustrated in Table 4.2, using a packaged sensor, the leak rate measurement resolution increases as the package gets smaller and as measurements are taken for longer and longer periods of time.

Table 4.2: Typical package dimensions for different types of devices, and given the a pressure measurement resolution (2 mTorr) the leak rate resolution in 1 day and 1 year. Also shown is the time it would take for the package to leak by 1 Torr with this given leak rate measurement resolutions.

Type of Package	Package Dimensions	Package Volume	Leak Rate Resolution (2 mTorr pressure measurement resolution) 1day	1 year	Time for 1 Torr change in pressure (with 1 year of measurement)
Chip Scale Package	5×5×1.5 mm	0.0375 cm^3	5.8×10^{-13} cc/s	$1.59E\times10^{-15}$ cc/s	500 years
Gyroscope (wafer level)	2×2×0.3 mm	0.0012 cm^3	1.83×10^{-14} cc/s	$5.07E\times10^{-17}$ cc/s	500 years
Package in this work (wafer level)	**2.3×2.3×0.1mm**	**5.3×10^{-4} cm^3**	**8.18×10^{-15} cc/s**	**2.24×10^{-17} cc/s**	**500 years**
3-D Accelerometer (wafer level)	0.5×0.5×0.3mm	7.5×10^{-5} cm^3	1.16×10^{-15} cc/s	3.18×10^{-18} cc/s	500 years
Thin Film Package (wafer level)	0.5×0.5×0.01mm	2.5×10^{-6} cm^3	3.87×10^{-17} cc/s	1.06×10^{-19} cc/s	500 years

4.2 Background & Previous Pirani Gauge Research

Micromachined Pirani gauges are now used and applied in both industry and research environments, employing a number of different geometries and materials. As compared with conventional filament based Pirani gauges, these miniaturized versions have the advantage of small size, low power, low temperature operation, fast thermal response and a wide range of operating pressures.

Micromachined Pirani gauges consist of a suspended resistor, where for a given current, the resistor heats up different amounts depending on the heat conducted through the gap, g, between the Pirani gauge and the substrate (Figure 4.1). Structures that allow for more heat conduction through the gas, H_g, as compared to the anchors, H_a, allow for lower pressures to be measured. Heat is conducted through the gas to the substrate as atoms in the gas interact with the suspended bridge. At lower pressure where there are fewer atoms in the gas, the mean free path is much larger that the gap distance, which means the atoms in the gas mostly collide with the bridge and transfer heat from it. Therefore, pressure is less sensitive to gap dimension and more sensitive to the surface

area of the bridge. At higher pressure, the mean free path of gas molecules is quite small and therefore, to increase interaction between the gas and the bridge, the gap has to be reduced. Therefore, structures with smaller gaps between the Pirani gauge and the substrate allow higher pressures to be measured, and structures with larger surface area allow lower pressures to be measured. Therefore, to have the largest possible dynamic range of operation, a gauge should have the largest possible surface area and have the smallest possible gap between this exposed surface area and the substrate. Taking these factors into account, micro-machined Pirani gauges have been fabricated using a variety of processes and geometries. These devices can be grouped into two categories: i) the resistor on dielectric membrane structure and ii) the micro-bridge structure.

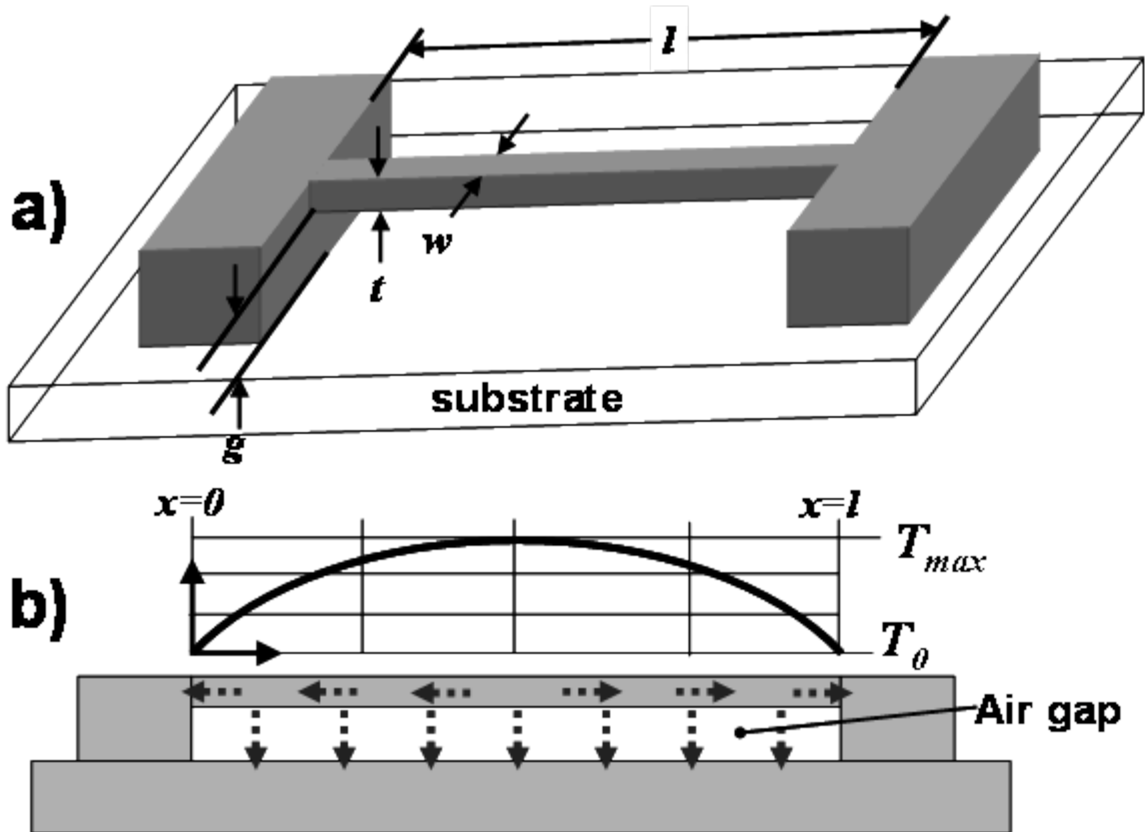


Figure 4.1: a) A single beam micro-bridge structure, b) an illustration of the heat loss through the gas, H_g vs. the heat loss through the anchors, H_a, and the temperature profile across the beam.

In *the resistor on dielectric membrane* structure, a serpentine metal [186-188] or poly-

Si [189, 190] thin film resistor is patterned on top of a dielectric membrane made out of CVD (chemical vapor deposited) Si_xN_y and/or SiO_2. The dielectric is used as a mechanical support and is needed because of the high residual stress of many metal and poly-Si thin films and the low mechanical rigidity the geometry of the resistor. Typically a high temperature coefficient of resistance (TCR) metal such as platinum or nickel is used for the resistor material and the suspended structure is released by a bulk KOH etch (tens of microns deep) of the underlying silicon wafer. Using such a structure, Shie et al. [186] presented a Pirani gauge with a measurement range from 10^{-7} to 1 Torr. Measurement of such low pressures required a constant temperature circuit in order to eliminate piezoresistive effects, as well as thermo-electric temperature stabilization and an integrated reference resistor to correct for ambient temperature fluctuations. Others have created the *resistor on dielectric membrane* structure in a surface micromachining process by undercutting a thin poly-Si layer instead of the bulk silicon [187, 190-192]. This allows for the creation of a smaller gap between the gauge and the substrate and therefore pressure measurement at higher pressure ranges. Chou [187] in particular was able to measure pressures ranging from 10^{-1} up to 10^5 Torr.

The *micro-bridge* structure consists of a suspended beam or coil as was shown in Figure 4.1a. Several researchers have fabricated this type of gauge by first sandwiching a suspended poly-Si layer in between a Si_xN_y or SiO_2 dielectric layer through a series of process steps and then etching the bulk Si underneath using KOH [193-195]. Swart [193] fabricated a 1200 μm long poly-Si coil using such a process in order to measure pressures ranging from 10^{-2} to 10^3 Torr. Quite a few different *micro-bridge* geometries and materials have been used including a suspended platinum beam which was surface micromachined to achieve a 300 nm gap [196]; a 10 μm thick single crystal silicon beam made from a silicon on insulator (SOI) wafer [197]; a heavily boron doped (p++) single crystal silicon coil fabricated in the dissolved wafer process (DWP) [198] and a suspended poly-Si beam fabricated in the Sandia Ultra-planar, Multi-level MEMS Technology 5 (SUMMiT V™) process [199]. In general, the *micro-bridge* structure is very easy to fabricate but because it is not mechanically supported by a membrane, it is difficult to achieve long, thin, thermally isolating structures—therefore it is difficult to measure lower pressures. Table 4.3 summarizes these various results reported in the

literature.

Table 4.3: Summary of Pirani gauges used in the literature.

Researcher/year	Type of Gauge	Pressure Measurement Range
[186] Shie et al., 1995 *	Resistor on dielectric membrane (Platinum)	10^{-7} to 1 Torr* (1.33×10^{-4} to 1.33 Pa)
[187] Chuo et al., 1997 *	Resistor on dielectric membrane (Platinum)	10^{-1} to 10^{5} Torr* (13.3 to 1.33×10^{7} Pa)
[189] Robinson et al., 1991	Resistor on dielectric membrane (Poly-Si)	10^{-2} to 100 Torr (1.33 to 1.33×10^{4} Pa)
[190]Paul et al., 1994	Resistor on dielectric membrane (Poly-Si)	0.75 to 7.5×10^{3} Torr (10^{2} to 10^{6} Pa)
[191] Stark et al., 2003	Resistor on dielectric membrane (Platinum)	10^{-3} to 10 Torr (0.133 to 1.33×10^{3} Pa)
[192] De Jong et al., 2003	Resistor on dielectric membrane (Platinum)	7.5×10^{-2} to 150 Torr (10 to 2×10^{4} Pa)
[196] Swart et al., 1994	Micro-bridge (1200μm long Poly-Si coil)	10^{-2} to 10^{3} Torr (1.33 to 1.33×10^{5} Pa)
[194, 195] Mastrangelo and Muller, 1999	Micro-bridge (1200μm long Poly-Si beam)	7.5×10^{-2} to 75 Torr (10 to 10^{4} Pa)
[196] Dom et al., 2005	Micro-bridge (100μm long platinum beam)	0.75 to 7.5×10^{3} Torr (100 to 10^{6} Pa)
[197] Moelders et al., 2004	Micro-bridge	10^{-2} to 1 Torr (1.33 to 133 Pa)
[198] Chae et al. 2003	Micro-bridge (p++ silicon coil)	20×10^{-2} to 2 Torr (2.67 to 267 Pa)
[199] Stark et al., 2005	Micro-bridge (Poly-Si beam)	10^{-2} to 100 Torr (1.33 to 1.33×10^{4} Pa)

* Used a constant temperature circuit in order to eliminate piezoresistive effects, as well as thermo-electric temperature stabilization and an integrated reference resistor to correct for ambient temperature fluctuations to extend the range of operation.

In this thesis, a new *micro-bridge* Pirani gauge structure is described which allows for pressure measurement from 10^{-3} to 760 Torr with a combination of gauge structures fabricated on the same substrate, in a 1, 2 or 3 mask, CMOS compatible surface micromachined process without post-processing steps such as KOH etching. This is accomplished using the ladder structure shown in Figure 4.2. The ladder structure consists of structural supports that allow for a longer suspended beam lengths and heat spreading across the structural supports. These two effects work together in extending the range of operation into lower pressure regimes. Such a structure can be easily integrated into the process for a number of devices that require vacuum (such as gyroscopes and resonators) for in-situ characterization of vacuum pressure and have been successfully applied in the characterization of micro vacuum packages [119, 120].

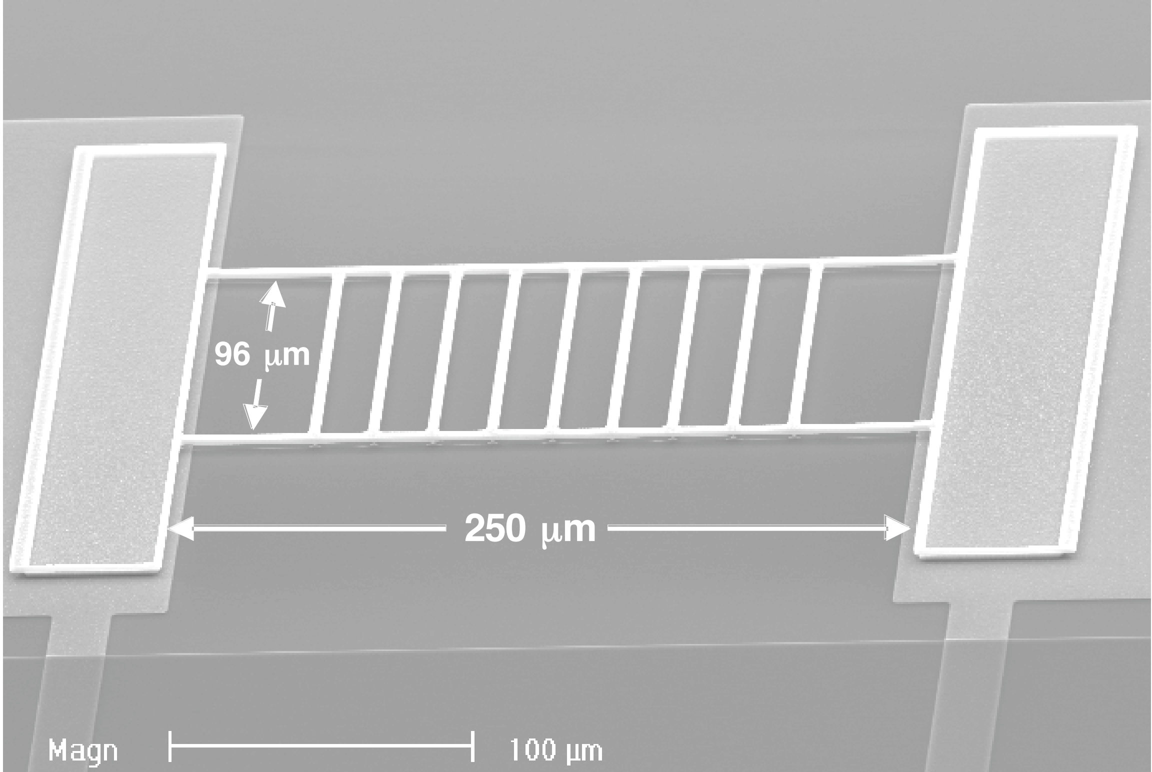


Figure 4.2: An SEM of the design 1 (D1) ladder structure.

4.3 APPROACH AND DESIGN

4.3.1 MODELING OF A SINGLE BEAM PIRANI GAUGE

A single beam micro-bridge Pirani gauge (as was shown in Figure 4.1a) with a width, w, thickness, t, length, l, and a gap between the beam and the substrate, g, has a resistance, R_b that changes as the temperature changes. The fractional resistance change, G_f, is proportional to the average change in temperature across the micro-bridge:

$$G_f = \frac{\Delta R}{R_0} = \frac{R_b - R_0}{R_0} = \xi \Delta T \tag{4.2}$$

where R_0 is the resistance at room temperature and ξ is the temperature coefficient of resistance (TCR). Passing a current, I_b, through the micro-bridge causes its temperature to increase and therefore the resistance to increase. The heat gets dissipated both through the gas separating the micro-bridge from the substrate, H_g, and through the anchors holding the micro-bridge to the substrate, H_a, resulting in a temperature profile similar to

the one that was shown in Figure 4.1b. When the pressure, P, is reduced, less heat dissipates through the gas to the substrate causing the temperature and therefore the measured resistance to increase. The pressure can therefore be measured by measuring the Pirani gauge resistance, R_b.

In operation, the Pirani gauge measures pressures in three different regimes. I) At relatively *high pressures* the mean free path for atoms is smaller than the gap distance, g, thus a very large amount of heat gets transferred through the air gap into the substrate. There is very little change in heat conduction as the pressure changes in this regime. Decreasing the gap distance, g, therefore helps increase the measurement resolution at higher pressures. II) At relatively *moderate pressures* the mean free path for atoms is much larger than the gap distance, g, and the amount of heat transferred through the gas is proportional to the density of atoms (the pressure) around the micro-bridge. The gauge is most sensitive to pressure changes in this regime. III) At relatively *low pressures* a much larger percentage of the heat gets transferred through the anchors, H_a, as compared to that transferred through the gas, H_g. This results in low pressure sensitivity. In order to increase the range of operation into lower pressure regimes, a larger H_g/H_a must be achieved as is the case with longer and more slender (a smaller thickness and width) geometries.

The analytical model derived by Mastrangelo and Muller [194] was used to better understand the operation of the micro-bridge Pirani gauge. In this model, the temperature distribution on a single suspended beam such as the one shown in Figure 4.1a was predicted using a form of the steady state heat equation:

$$\frac{\partial^2 u}{dx^2} - \varepsilon u = \delta \tag{4.3}$$

where u is the micro-bridge temperature, ε is the heat loss through the gas, δ is the ohmic power generation, and x represents the position on a beam spanning from $x=0$ to $x=l$. In modeling the micro-bridge, it was assumed that at the boundaries (x=0 and $x=l$), the temperature was fixed at room temperature, T_0 (as was shown in Figure 4.1b). This is an accurate assumption if heat is sunk efficiently from the beam to the substrate. Mastrangelo and Muller derived the following expression for the micro-bridge resistance,

R_b, as a function of ambient pressure, P:

$$R_b = R_0\left[1+\frac{\delta\xi}{\varepsilon}\left(1-\frac{\tanh(\sqrt{\varepsilon}\,\frac{l}{2})}{\sqrt{\varepsilon}\,\frac{l}{2}}\right)\right] \tag{4.4}$$

where

$$\delta = \frac{I_b^2 R_0}{\kappa_b wlt}, \qquad \varepsilon = \left(\frac{\eta\kappa_g(P)}{\kappa_b gt} - \delta\xi\right) \tag{4.5}$$

and η is a correction factor taking into effect fringing heat flux through the gap and $\kappa_g(P)$ and κ_b are the thermal conductivities vertically through the gas and laterally through the beam. (Refer to Mastrangelo and Muller [194] for a complete derivation and explanation of theory.) The thermal conductivity of highly phosphorus doped poly-Si, the micro-bridge material used in this work, has been measured elsewhere, to be 14.2 $W \cdot m^{-1} \cdot K^{-1}$ (Watts per meter Kelvin) [200]. The thermal conductivity of air, $\kappa_g(P)$ ranges from around 2.2×10^{-2} $W \cdot m^{-1} \cdot K^{-1}$ at 760 Torr (atmospheric pressure) to 2.5×10^{-7} $W \cdot m^{-1} \cdot K^{-1}$ at a vacuum pressure of 10^{-3} Torr (calculated from equations in Mastrangelo and Muller [194]). Because κ_b is so much larger than $\kappa_g(P)$, a relatively long/thin micro-bridge is required to achieve enough thermal conduction through the gas to attain a highly sensitive pressure sensor.

4.3.2 CONFIRMATION OF THE MODEL

The accuracy of the model was tested by comparing the predicted results with that of five Pirani gauges from two different process runs with a width, thickness and length of 4 µm, 2.2 µm and 250 µm and a gap distance of 2 µm (details of the processing and test procedure will be outlined in Section 4.4, *Fabrication of Pirani Gauge Test Structures*). Both in actual devices and the model, increasing the input current, I_b, caused the temperature to increase proportionally to the input power ($P_b=I_b^2R_b$). In testing these devices, a sufficient current was applied so that the maximum fractional resistance change, G_f, between atmospheric pressure and vacuum (10^{-5} Torr in our vacuum chamber) was 1%. In so doing, the measurement ranges of devices with different

material properties and different geometries could be directly compared. Table 4.4 shows the current applied, the measured TCR, the resistivity, average temperature and the power dissipated across each of the micro-bridges. The maximum average temperatures increase across each micro-bridge (measured at 10^{-5} Torr), ranged from 37.8ºC to 62.9ºC and were calculated using Equation 4.2.

Table 4.4: The input currents, initial resistance, TCR, maximum average temperature across the beam, input powers and the correction factors needed for the model to fit the data for each of the 5 single beam Pirani gauges tested.

Measurant	Beam 1	Beam 2	Beam 3	Beam 4	Double Beam
Current (I)	622 μA	545 μA	538 μA	517 μA	739 μA*
Initial Resistance (R_0)	1529.3 Ω	1481.4 Ω	1481.4 Ω	1436.4 Ω	1103.0 Ω*
Measured TCR (ξ)	1.59×10^{-4} ºC^{-1}	2.20×10^{-4} ºC^{-1}	2.24×10^{-4} ºC^{-1}	2.64×10^{-4} ºC^{-1}	1.87×10^{-4} ºC^{-1}
Maximum (Average) Temperature Increase(T_{Ave})	62.9 ºC	45.6 ºC	44.6 ºC	37.8 ºC	53.5 ºC
Power Dissipated	592 μW	440 μW	429 μW	384 μW	301 μW
Modeling Correction Factor	1.539	1.584	1.572	1.658	1.834

*The double beam consisted of two micro-bridge resistors in parallel and was fabricated in a different process run (as detailed in the Fabrication section). The listed input currents and the measured resistance for the double beam structure are the input current and resistance across *each* of the parallel beams.

Figure 4.3 shows that these devices have almost identical G_f vs. pressure behavior. In the modeling results plotted in Figure 3.3, a 622 μA current, a TCR of 1.59×10^{-4} ºC^{-1} and a resistivity of 5.38×10^{-5} Ωm^2 were applied (the parameters for the Beam 1 Pirani gauge shown in Table 4.4). As shown in Figure 4.3 the modeling results for the G_f vs. pressure behavior differ from the test results by a factor of 1.54. Inputting the currents, and the measured TCR's and resistivities for each of the Pirani gauges from Table 4.4 resulted in the model over predicting G_f by factors of 1.54 to 1.84 (the correction factor). This discrepancy could be a result of errors in the assumptions for the model or in the material properties. However, as illustrated in Figure 4.3, multiplying the predicted change in resistance by a factor of 1/(the correction factor), the model results map directly over the test results.

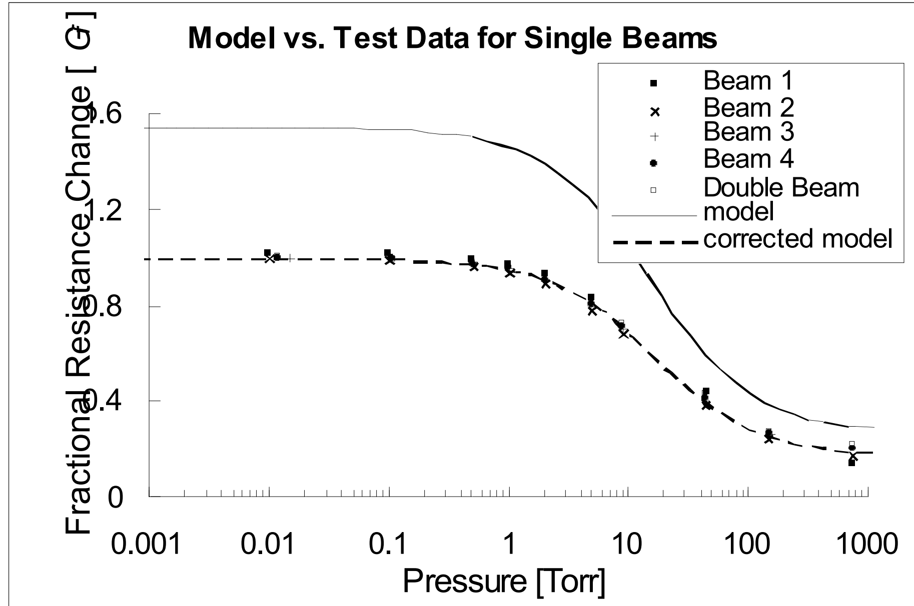


Figure 4.3: The measured data for 4 single 4μm×2μm×250μm micro-bridges and two parallel micro-bridges as compared to the modeling data. Adding a correction factor, the modeling data maps directly over the measured data. * See the note in Table 1 on the double beam structure.

Because of the complexity of the expression for R_b in Equation 4.4, it is not initially evident how the design variables (w, t, l, and g) affect the performance of the device. This can be done numerically. A nominal width, thickness and length of 4 μm, 2.2 μm and 250 μm were chosen, with the input current, TCR, resistivity and correction factor used in the corrected model plotted in Figure 4.3. In the modeling results shown in Figure 4.4, the width and thickness were reduced by a factor of 4 and the length was increased by a factor of 4 in order to show the effects of changing the micro-bridge dimensions, where in each case a current of 155.5 μA (that is the current applied for the nominal case divided by 4) was applied. In so doing, in each case, a maximum average resistance change of 1% was predicted at absolute vacuum. Equation 4.2 therefore predicts that these micro-bridges should have the same average temperature increase as the nominal case. As illustrated in Figure 4.4, for each case the change in resistance decreases from 1% at absolute vacuum, down to 0.01 to 0.2% at atmospheric pressure, where a larger slope indicates better device sensitivity. These plots show that decreasing the width or thickness, or increasing the length shifts the performance curve to the left, indicating higher measurement sensitivities at lower pressures. Increasing the length resulted in the most dramatic change in performance.

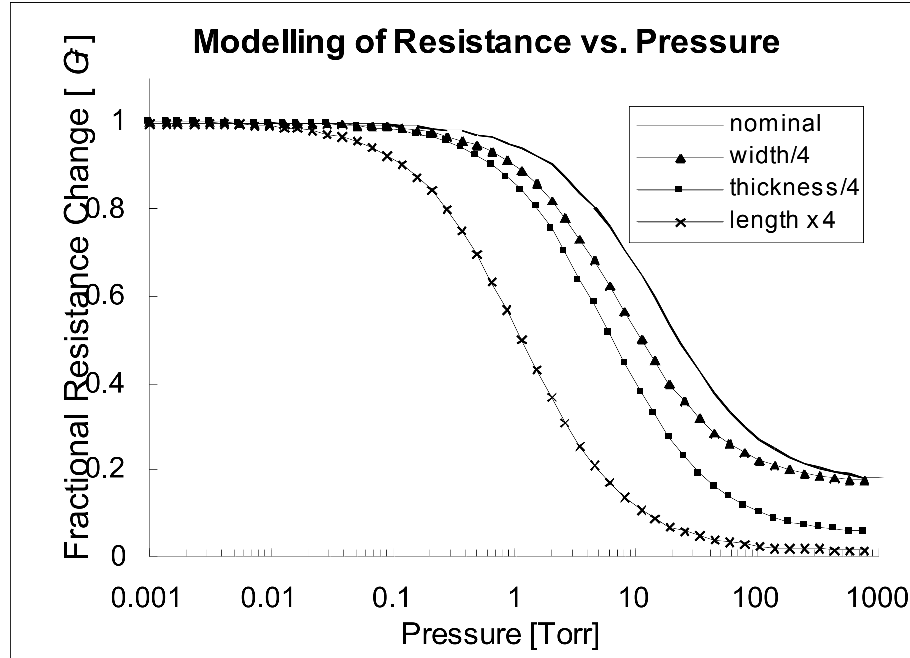


Figure 4.4: Modeling data comparing the nominal case (a single 4µm×2µm ×250µm beam) with a single beam that is a quarter of the width, a quarter of the thickness, or four times the length.

4.3.3 STRUCTURAL RIGIDITY

In the design of a Pirani gauge, structural rigidity must also be considered. Although designing a longer, thinner micro-bridge structure is desirable for measuring low pressures, it results in a decreased stiffness, S_B, in the axis perpendicular to the substrate:

$$S_B = \frac{12Ewt^3}{L^3} \tag{4.6}$$

where E is the Young's Modulus. A structure with a very small stiffness will get pulled down to the substrate during the release process (the details of the release process were discussed in Section 3.3 (*Device Release*) of Chapter 3, and will be discussed specifically in relation to the different Pirani gauge designs in Section 4.4.2 (*Pirani Gauge Structure Release*). Furthermore, in the presence of a compressive stress, buckling is of major concern. The following expression can be used to predict the critical intrinsic stress, σ_{crit}, for *out-of-plane* and *in-plane* buckling respectively:

$$\sigma_{crit} = \frac{\pi^2 E h^2}{3L^2}, \qquad \sigma_{crit} = \frac{\pi^2 E w^2}{3L^2} \tag{4.7}$$

In our 2.2 μm thick poly-Si, a residual stress of roughly 36 MPa was measured. Given t = 2.2 μm and w = 4 μm, Equation 5.7 predicts *out-of-plane* buckling for lengths of ≥266 μm and *in-plane* buckling for lengths of ≥484 μm. Therefore, above 484 μm, a beam should buckle along both axes, causing the micro-bridge to become unstable so that it will collapse to the substrate surface with very little applied force. On the other hand, if the micro-bridge only buckles in the *out-of-plane* direction (and away from the substrate) the beam will bend until enough of the intrinsic stress is relieved to reach static equilibrium. As will be discussed in the fabrication section, beams with sufficient stiffness for release buckled only in the *out-of-plane* direction, always tended to buckle away from the substrate.

The main motivation for using the ladder structure was to prevent horizontal buckling so that when longer and narrower suspended micro-bridge structures were fabricated, they buckled only in the vertical axis. In so, they reached static equilibrium and survived the release process. In using the ladder structure, the structural links were spaced far enough apart so that almost no current passes through them. Therefore, roughly the same amount of heat gets generated across the micro-bridge. Furthermore, some of the generated heat spreads across the structural links, allowing for a larger percentage of the heat to eventually conduct through the gas. This combined with the longer suspended micro-bridge structure allows for a significantly larger H_g/H_a and therefore the ability to measure lower vacuum pressures.

4.4 FABRICATION OF PIRANI GAUGE TEST STRUCTURES

For the development of the Pirani gauge design (which is detailed in Section 4.3), the process flow outlined in Figure 4.5 was used. In this process, a 3000 Å layer of LPCVD Si_3Ni_4 was first deposited to electrically insolate the devices from the substrate. A 3000Å layer of LPCVD poly-Si was then deposited and then heavily phosphorous doped. This poly-Si was patterned to form the *lead/bond pad layer* for the Pirani gauges (Figure 4.5a). A 2 μm LPCVD SiO_2 *sacrificial layer* was next deposited. This layer was then patterned

to allow for anchoring of the device layer to the leads (Figure 4.5b). Finally a 2.2 μm layer of LPCVD poly-Si was deposited and doped with resistivities that ranged from 3.49×10^{-5} Ωm^2 to 5.38×10^{-5} Ωm^2 depending on the process run and position on the wafer. This layer was patterned to form the *device* layer (Figure 4.5c). Finally, the wafers were diced and the dies dipped in BHF (buffered hydrofluoric acid) for 30 minutes to etch the silicon oxide, in order to undercut the micro-bridges (Figure 4.5d). (This release process was described in more detail in Section 3.3 of Chapter 3.)

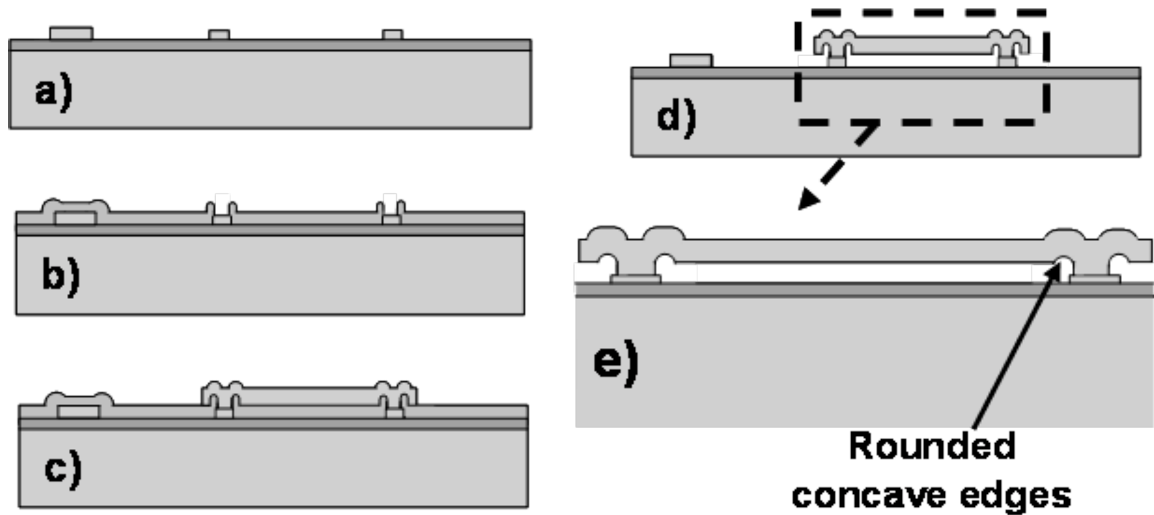


Figure 4.5: Fabrication of the suspended beam structure consists of the deposition and patterning of a) poly-Si which forms the leads and bond pads, b) SiO_2 which acts as a sacrificial layer and, c) a poly-Si structural layer. d) After dicing, the devices are release in buffered hydrofluoric acid (BHF) and then soaked in methanol. e) One possible reason for the tendency of beams to buckle upwards are the rounded concave edges created due to photolithography.

The Pirani gauge structures studied in this section were fabricated on wafers from three different process runs. The four single beam devices tested and one double beam structure (two micro-bridge resistors in parallel) discussed in Section 4.3.2 (*Confirmation of the Model*), were fabricated in *run 1* and *run 2* respectively. Run 1 was fabricated using the full device wafer process (Process #1) outlined in Section 3.2 (*Device Wafer Fabrication*) of Chapter 3 and the devices in this run had resistivities ranging from 5.06×10^{-5} to 5.38×10^{-5} Ωm^2. Run 2 was fabricated using the process outlined above and resistivities ranged from 3.10×10^{-5} to 3.54×10^{-5} Ωm^2 where measured. Despite differences in resistivity and TCRs across all of these devices (as was illustrated in Table

4.4), they demonstrated identical G_f vs. pressure behavior (as was illustrated in Figure 4.3).

Several of the ladder structures designed which will be analyzed in the following sections were also fabricated in run 2. Finally, run 3 was also fabricated in the full device wafer process (Process #1) outlined in Section 3.2 (*Device Wafer Fabrication*) of Chapter 3 and the devices in this run had resistivities ranging from 3.49×10^{-5} to 4.42×10^{-5} Ωm^2. Two of the ladder structure designs which will be analyzed in the following sections were fabricated in this run. As with the single beam and double beam designs, despite minor differences in measured resistivities and TCRs from device to device, specific designs showed nearly identical performances (as will be shown in Section 4.5).

4.4.1 DEVICE LAYOUT

As was demonstrated in section 4.3 (*Approach and Design*), the main factor in the pressure measurement range for a single beam Pirani gauge were the device dimensions (length, width and thickness). For the devices fabricated in this work, the thickness of the device layer remained constant at 2.2μm. Therefore, the length and width of the devices were the predominant factors in determining their measurement ranges. In the ladder structure devices, the size and number of cross-beams also affected the performance of the device. Table 4.5 summarizes the geometries of the various Pirani gauge designs and the release process for each design. In all of the designs shown, except for D3s, the structural links were made with the same width as the cross-beams. Also shown in Table 4.5 is whether or not the devices could be released in methanol or CO_2—these results will be discussed specifically in the next Section 4.4.2 (*Pirani Gauge Structure Release*).

Table 4.5: The dimensions of the different Pirani gauge designs and how or whether or not they released.

Name	Length	Width	Gap	Structural Links		Release
				Width	Number	
S1	250μm	4 μm	2 μm	-	-	Methanol or CO_2
S2	500μm	4 μm	2 μm	-	-	None
S3	1000μm	4 μm	2 μm	-	-	None
D1	250μm	4 μm	3 μm	96 μm	9	Methanol or CO_2
D2	250μm	4 μm	2 μm	384 μm	9	Methanol or CO_2
D3	1000μm	4 μm	2 μm	384 μm	36	CO_2
D3s	1000μm	16 μm	3 μm	384 μm	36	Methanol or CO_2

The last structure shown in Table 4.5, D3s, was designed specifically to be more rigid so that it would release in CO_2 or methanol, so a 16 μm width was used. Because larger structural widths result in significantly larger release times in BHF (very long exposures to BHF can result in significant etching of a Si_3N_4 passivation layer which etches at ~9Å per minute) release holes were design into the D3s structure. Figure 4.6 shows a close up view of the release holes for one of these structures. Two different layouts were used for the D3s structures as shown in Figure 4.7. As illustrated, in Figures 4.7a and 4.7b, these structures had 6 μm square holes with 6 μm spacing and 4 μm holes with 4 μm spacing. In each case, the holes allowed for enough BHF to get underneath the structures so that it would be completely released in less than 30 minutes.

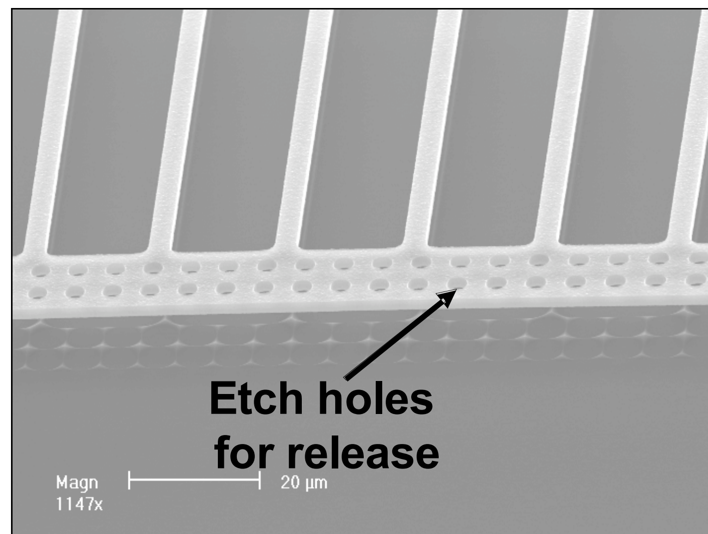


Figure 4.6: A SEMS of one of the D4s structures showing a close up view.

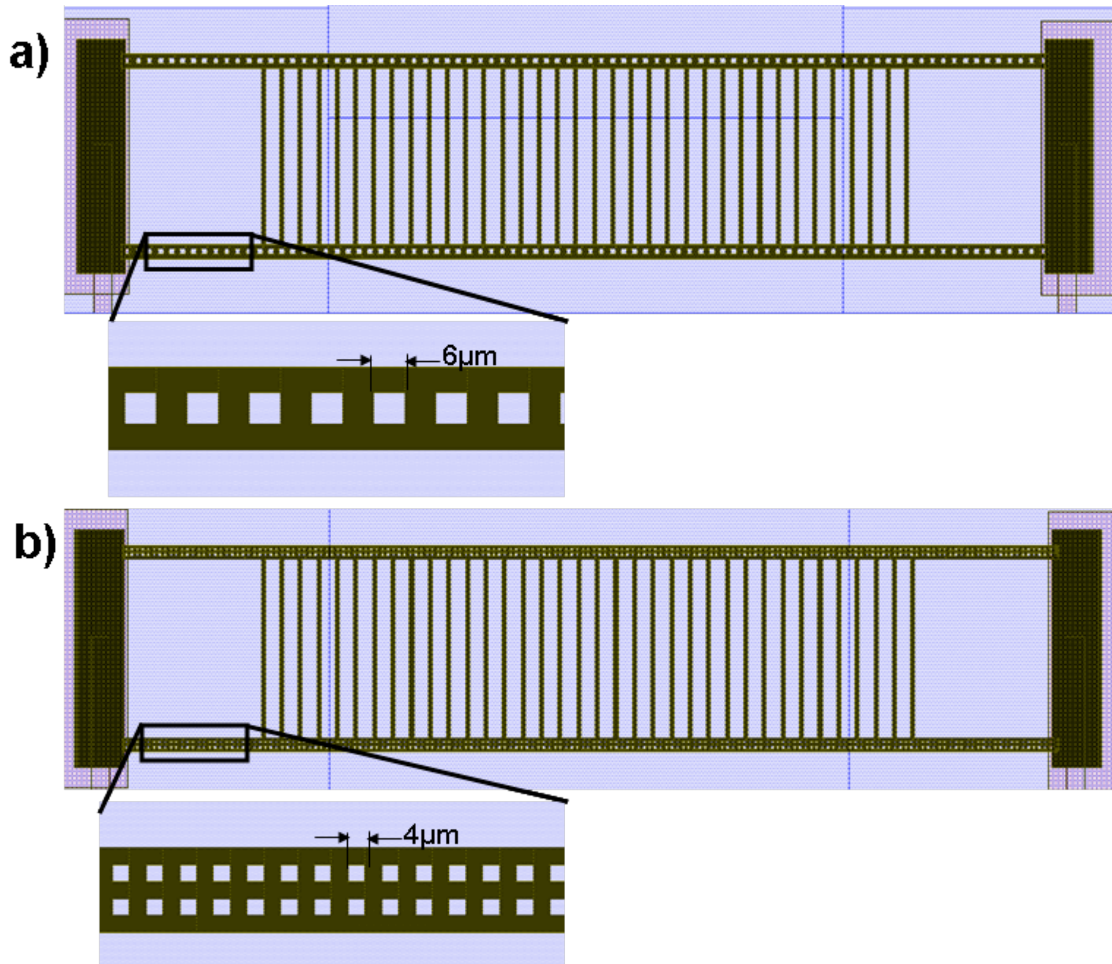


Figure 4.7: Layouts of the two D4s Pirani gauge designs.

4.4.2 PIRANI GAUGE STRUCTURE RELEASE

The device release process was discussed in detail in Section 3.3 of Chapter 3. As was explained in Section 3.3, release was accomplished using either the hot plate release method or using CPD release. Releasing with the CPD allowed for more fragile devices to be released. As was shown in Table 4.5, single 4µmx2.2µmx250µm beams and 4µm×2.2µm×250µm beams with structural links (S1, D1 and D2) were sufficiently rigid not to require CPD for release. On the other hand, the 4µm×2.2µm×500µm and 4µm×2.2µm×1000µm single beam structures (S2 and S3) pulled down to the substrate during release—even with CPD. This is consistent with Equations 5.7 which predicts buckling along both axis (and therefore an unstable structure) at above a 484µm length. Figure 4.8a shows a collapsed 4µm×2.2µm×1000µm single beam structure after release.

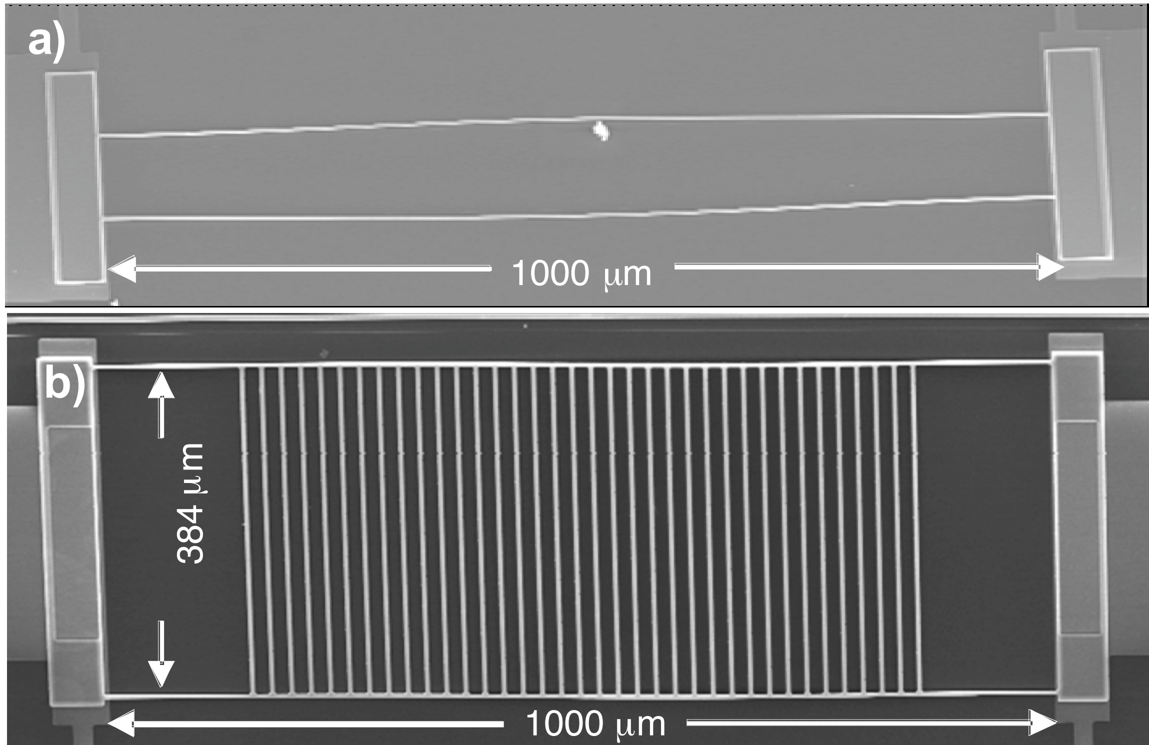


Figure 4.8: a) Parallel 4μm×2.2μm×1000μm suspended beams which buckled along both axis and pulled down to the substrate, and b) the design 3 ladder structure which was successfully released, only buckling in the *out-plane-plane* direction, away from the substrate.

The 4μm×2.2μm×1000μm ladder structure with thirty-six structural links (D3) is also shown in Fig. 3.8b. This structure did successfully and consistently release with CPD. As also shown in Table 4.5, the stiffer 1000 μm ladder structure (D3s) that had a 3 μm gap was successfully released using hot plate release and using CPD release because of its structural rigidity.

All of the ladder structures consistently buckled upwards. In fact, the D3 and D3s structures buckled upwards approximately 6 μm. As was shown in Figure 4.5e, one possible explanation is that the rounded concave geometry on the inside edges of the micro-bridge structure, created (incidentally) through photolithography, give the micro-bridges a tendency to buckle upwards. Another possible explanation is that there may be a stress gradient in the poly-Si. Many thin films tend to have higher stresses in the initial layers due to lattice mismatches and/or changes in pressure or temperature during deposition. The rounded edges at the supports, a stress gradient or a combination of these two effects could cause the tendency for the micro-bridge structure to always buckle

upward.

4.4.3 PROCESS SIMPLIFICATION FOR OTHER APPLICATIONS

For our application, it was desirable to have low profile leads that acted as feed-throughs in a wafer-level bonding process—therefore the *lead/bond pad layer* (Figure 4.5a) and the *device layer* (Figure 4.5c) were deposited and patterned in two different steps. If feed-throughs are not a design concern, *the lead/bond pad layer* and *device layer* can be combined, resulting in a 2 mask process. If the leads and bond pads have much larger dimensions than the Pirani gauge structure, the patterning step for the sacrificial layer can also be removed, making this into a 1 mask process.

4.5 PIRANI GAUGE CHARACTERIZATION

Traditionally a Wheatstone bridge [186-188, 194] is used to monitor the change in Pirani gauge resistance, R_b, during operation. This configuration is well suited for accurate resistance measurements and can be easily integrated with circuitry. An alternative method for Pirani gauge resistance measurement is to use the 4-point probe configuration shown in Figure 4.9 [191, 198, 201]. A 4-point probe consists of 2 leads on each side of the resistor, where a current I_b, is applied across two of the leads, and the voltage drop, V_b, is measured across the other. Since the current is constant from the input to the output, the resistance of the micro-bridge, R_b, can be determined by V_b/I_b independent of the resistances of the leads running to the micro-bridge. The main application for our Pirani gauges were for testing vacuum pressures in micro-vacuum cavities [119, 120] in which testing occurred both using probes on probe stations and wire bonds in DIPs (dual-in-line packages). Through various bond tests and reliability tests, devices where either re-tested on the probe station or repackaged into a DIP causing small changes in the lead resistances which can potentially compromise calibration data if the Wheatstone bridge configuration is used. Therefore, for our application, the 4-point probe configuration was ideal since these lead resistances do not effect the measurement of R_b.

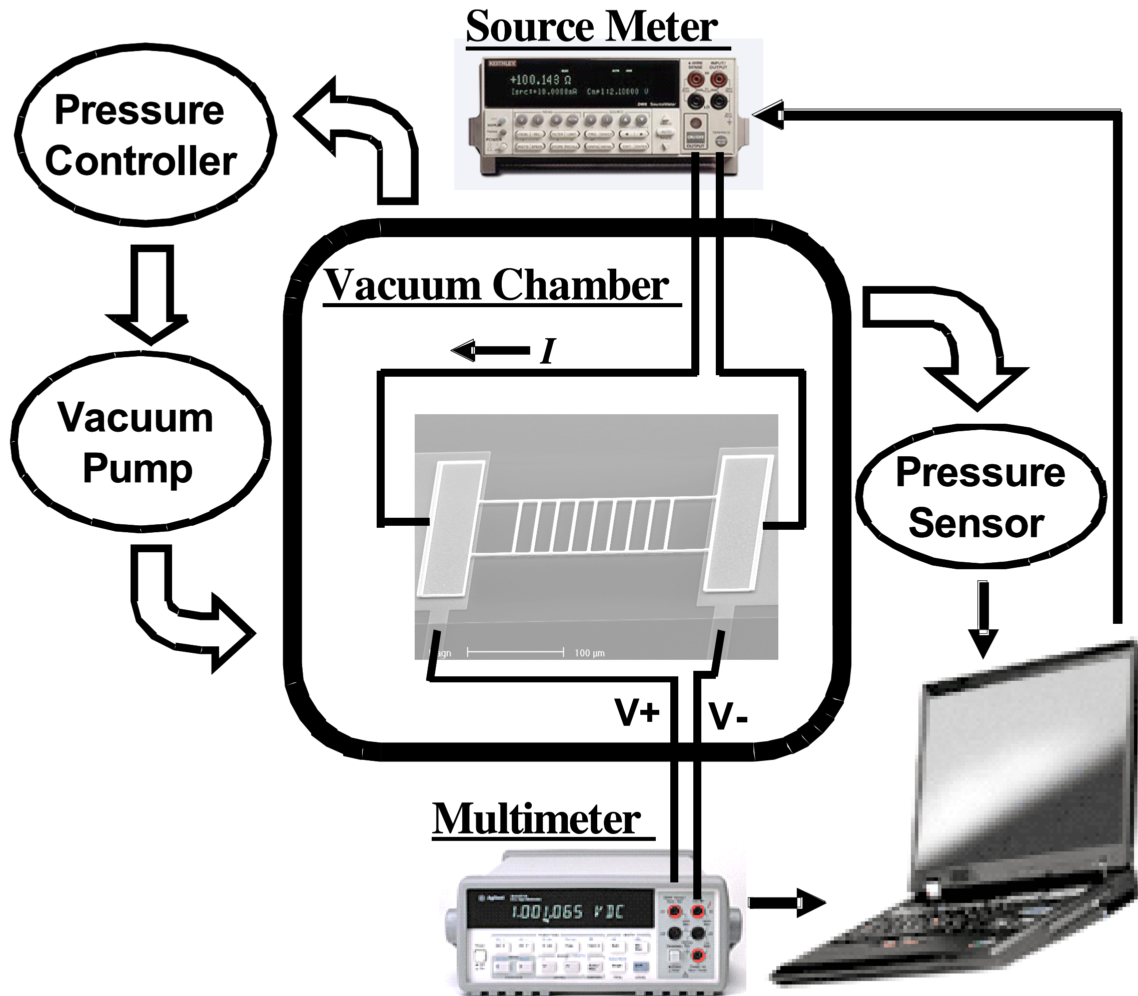


Figure 4.9: A schematic of the test setup where the Pirani gauges were tested in a 4-point probe configuration using a source meter to provide current and a multimeter to sense the voltage drop across the Pirani gauge. The Pirani gauges were tested inside of a vacuum chamber where pressures were dialed in using a pressure controller. A separate pressure sensor was used for measuring the pressures.

Test data for Pirani gauge characterization was obtained using the setup illustrated in Figure 4.9 where the devices were placed in a vacuum chamber and measurements were taken via feed-throughs that ran into the test chamber. During testing the vacuum chamber was backfilled with dry nitrogen and therefore the ambient gas used for calibration was nitrogen. The gas which the gauge is calibrated in is important because, as shown in Equations 4.4 and 4.5, the thermal conductivity affects the performance of the Pirani gauge. Although many commonly used gases (Ar, CO_2, Ne, CO) have almost the same thermal conductivity as N_2, light gases such as He and H_2 have thermal

conductivities 2 and 4 times greater than that of nitrogen [202]. Considering Equations 4.4 and 4.5, such a thermal conductivity change can change the measured pressure by factors of 2.5 and 5, respectively. This should be taken into account in the calibration of the Pirani gauges for applications where the pressure measurement is performed in a predominantly helium or hydrogen environment.

Vacuum pressures were achieved using a Varian SD-301 roughing pump together with a Varian 350 MacroTorr Turbo-V pump. An MKS 600 Series Pressure Controller was used to dial in the desired pressures via a control valve and a MKS Baratron type 627 pressure transducer. These pressures were measured and recorded using a separate pressure sensor: a factory calibrated MKS Series 925C MicroPirani™ Transducer with a reported 10^{-5} to 760 Torr range [203]. Even so, pressures could only be regulated to within ±2 mTorr and the chamber could only be pumped down to as low as 2 mTorr. Because of this, it was difficult to accurately characterize our Pirani gauges below 20 mTorr.

Using a Labview™ program, currents were input using a Keithley 2400 SourceMeter in 500 millisecond pulses and the voltages measured using an HP 34401A multimeter in order to calculate the micro-bridge resistance in the 4-point probe configuration. Holding a substantial current across the micro-bridge for many seconds or minutes caused the substrate to heat and therefore the boundary conditions at each end of the micro-bridge to rise above room temperature. Using 500 millisecond pulses, the substrate did not have enough time to heat up, allowing for predictable results and for the boundary conditions to more closely match the model discussed earlier (Section 4.3).

In determining the TCRs listed in Table 4.4 (in Section 4.3.2, *Confirmation of the Model*) for the micro-bridges, the resistance was measured using the same 4-point probe configuration, but in an oven held at 23ºC, 55ºC and 75ºC. A low current was applied in these resistance measurements so that there was little ohmic heating of the Pirani gauge during the TCR measurement. The slope of G_f (fractional resistance change) vs. ΔT was then used to calculate the TCR via Equation 4.2.

Figure 4.10 shows the G_f vs. pressure for the D1, D2, D3s and D3 ladder structures. As illustrated, the pressure verses resistance data for each design has roughly the same shape on the log-linear graph, but operate in different pressure regimes—this shows that

the Pirani gauges can be designed specifically for a number of different pressure ranges. Going from the 4µm×2.2µmx250µm single beam structure, S1, to the 4µm×2.2µmx250µm ladder structure, D1 (shown in Figure 4.1), there is almost a 5x shift towards lower pressures. This clearly indicates that heat spreading through the structural links allows for measurement at lower pressures as predicted. Looking at the D1 and D2 data, it appears that increasing the structural link lengths from 96 to 384µm only changed the performance of the device slightly. The D3 ladder structure (shown in Figure 4.8b) on the other hand, allowed for pressure measurement 100x lower than that for the 4µm×2.2µmx250µm single beam design and more than 5x lower pressure measurement as compared to that predicted for the 4µm×2.2µmx1000µm structure. This dramatic change in the measurement range is due to both the longer beam length and due to heat spreading across the structural supports. The more rigid D3s gauge operates in a lower pressure range than that predicted for the 16µm×2.2µmx1000µm single beam structure but at nearly 5x higher pressure range then the D3 gauge.

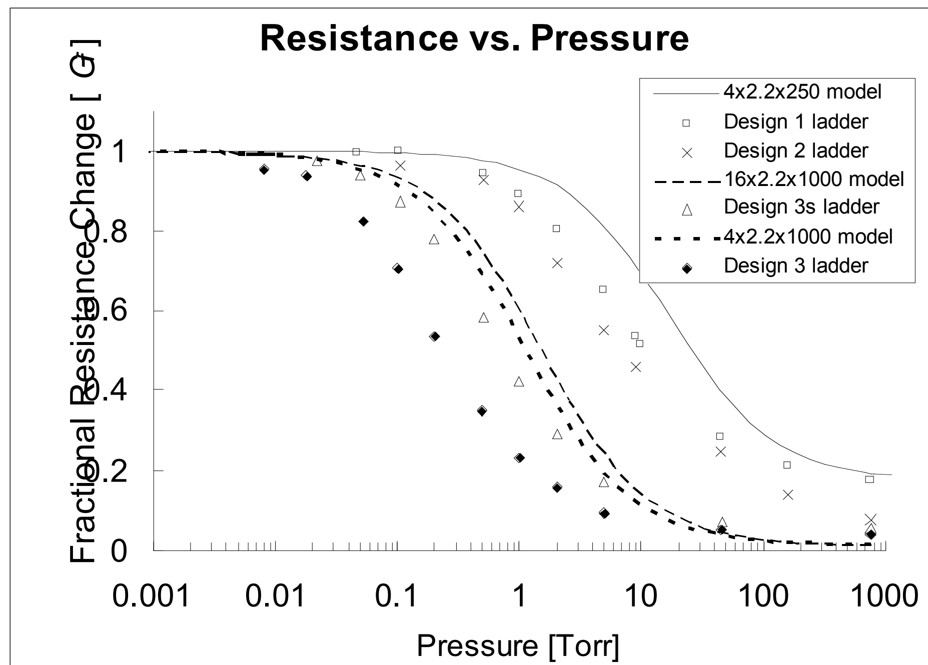


Figure 4.10: A plot of G_f vs. pressure for design 1, 2, 3s and 3 ladder structure Pirani gauges as compared to models of the 4µm×2.2µm×250µm, the 16µm×2.2µm×1000µm and 4µm×2.2µm×1000µm model for single beam Pirani gauges.

The range of operation for these devices is limited by the measurement resolution of the voltage drop across the beam, V_b, for a given input current, I_b ($R_b = V_b/I_b$). To visualize how this affects the measurement range, the data in the plots of G_f vs. pressure in Figure 4.10 are plotted in terms of the change in voltage, ΔV vs. pressure on a *log-log* plot in Figure 4.11—where we define ΔV as the change in the measured voltage from the maximum voltage measured at absolute vacuum, V_{vac}, (in this case <2mTorr):

$$\Delta V = V_{vac} - V_b \tag{4.8}$$

As illustrated, in Figure 4.11, near the lower limit of pressure measurement, there is a linear relation between ΔV and pressure for each of the gauges—this is consistent with ΔV vs. pressure data for Pirani gauges in the literature [186-188]. Several factors limited the range of operation of these gauges. First, as mentioned earlier, in the vacuum chamber, it was difficult to regulate the pressure accurately under around 20 mTorr. The second major factor was our voltage measurement resolution. In Figure 4.11, the horizontal line at 50μV represents approximately the limit of our voltage measurement resolution. It is likely that ambient temperature fluctuation and piezoresitive effects contribute in this voltage measurement error. The measurement range at the upper limit of operation was limited by the voltage resolution in a similar manner resulting in measurement ranges of approximately 5×10^{-2} to 760 Torr, 5×10^{-3} to 100 Torr and 10^{-3} to 50 Torr (2×10^{-5}) for D1, D3s and D3 gauges respectively. Shie et al. [186] was able to extend the operation of their gauge by improving their voltage measurement resolution to better than 1 μV using a constant temperature circuit in order to eliminate the piezoresistive effects, as well as thermo-electric temperature stabilization and an integrated reference resistor to correct for ambient temperature fluctuations. Similar circuitry and thermo-electric temperature stabilization could be used to improve the resolution the Pirani gauges presented here. Assuming that the ΔV vs. pressure would stay linear (as modeling and test data in the literature predict), a 1 μV measurement resolution for instance would allow for pressure measurement below 1×10^{-5} Torr for the D3 gauge.

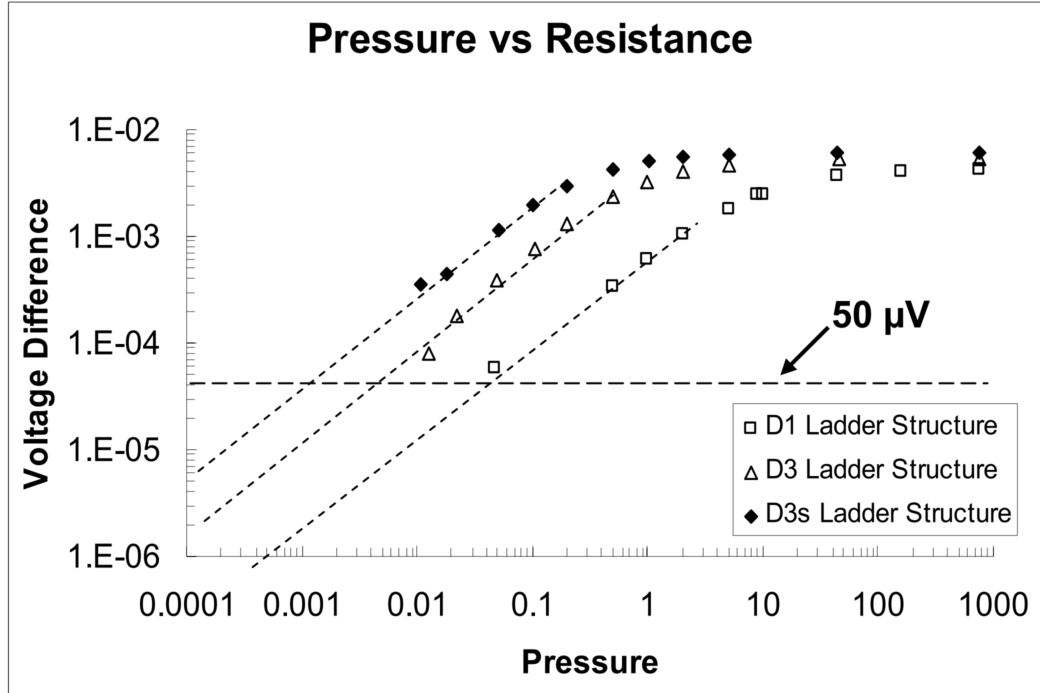


Figure 4.11: The data for the Design 1, 3s and 3 gauges (from Figure 4.10) graphed in terms of ΔV ($\Delta V = V_{max} - V_d$) vs. pressure. As illustrated, as the gauges approach the lower limits of there operation, there is a linear relation between voltage and pressure and therefore the lower limit of operation is limited by the ability to accurately measure voltage.

4.6 IMPLEMENTATION FOR PACKAGE CHARACTERIZATION

4.6.1 TEST METHODOLOGY

Pirani gauges used for package characterization were calibrated by measuring the thermal impedance:

$$T.I. = \frac{T_{avg}}{P_E}, \qquad T_{avg} = \frac{1}{\xi}\frac{R_b}{(R_0 - 1)} \tag{4.9}$$

where P_E is the electrical power and T_{ave} is the average temperature across the microbridge. Here the thermal impedance was used as supposed to measuring the voltage difference, ΔV, from Equation 4.8 which is commonly done in the literature [186-188, 194]. In this application measuring ΔV was not practical for two reasons. First, there was no way to calibrate the devices at the wafer-level before bonding. Ideally, with access to a wafer-level vacuum probe station, each vacuum sensor would be calibrated

before packaging. Second, even with such a calibration, the exposure to wafer bonding temperatures from 345 to 390ºC for 1 ¾ hour can change the resistivity of the gauge (and therefore *ΔV* for a given input current) by as much as a percentage—thus invalidating any pre-calibration. The thermal impedance on the other hand can be measure without pre-calibrating the sensor and is less sensitive to changes in the resistivity of the gauge material. Furthermore, because of the resistivity change of the gauges after bonding, device calibration was conducted *after* packaging. This calibration process will be described in the next section (Section 4.6.2, *Pirani Gauge Calibration*).

To measure the thermal impedance, a range of currents were first applied across the device and the voltage drop was measured in a 4-point probe configuration. Given the TCR of the material, the applied power vs. average device temperature was graphed. (The TCR values though varied from device to device. For simplicity, for package calibration, the TCR was always assumed to be 5×10^{-4}). The slope of this line results in the thermal impedance of the device, where the slope increases as the pressure decreases. Figure 4.12 shows power verses temperature data used for calculating thermal impedances in a D3s gauge. During pressure measurement, currents were applied in 500 ms pulses in succession from 500 μA to 900 μA with 50 μA steps for both the D1 and D3s gauges (the gauges used for almost all of the package characterization).

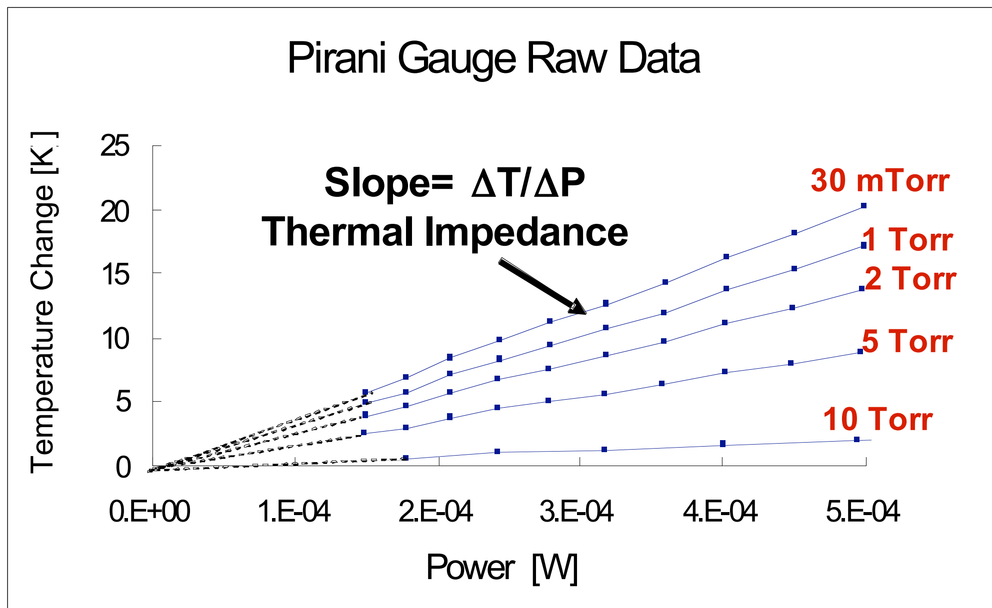


Figure 4.12: Temperature verses power data for a D3s gauge illustrating the acquisition of thermal impedance data for pressure measurement.

Finally, an added advantage of using this method was that 9 measurements were taken (at different currents) for each measurement. This added an averaging affect which increased the precision of the measurement.

4.6.2 PIRANI GAUGE CALIBRATION

4.6.2.1 Pressure Measurement Ranges

For most of the package characterization, the D1 and D3s gauges were used together for measuring pressures ranging from 760 Torr down to around 2 mTorr. Figure 4.13 shows typical plots of thermal impedance vs. pressure for the D1 and D3s gauges. Pressures from 760 Torr to 50 Torr could be estimated using the D1 gauges. Though it was difficult to fit a curve to this area, pressures could be resolved to better than an order of magnitude. For measuring pressures between 2 and 50 Torr, the log-linear region of the D1 gauges was used. As illustrated in Figure 4.14, a logarithmic function could be fit to this part of the curve. Similarly, the log-linear region of the D3s curve could be used for measuring pressures between 0.1 and 4 Torr. The D3s gauge could also be used for measuring pressures below 100mTorr. Figure 4.14 shows a linear plot of the D3s gauge from. As illustrated, from 50mTorr and below the gauge performance is linear. As discussed previously, because of the limitations of the test setup, the pressure chamber could only be consistently pumped down to ~2 mTorr. As a result, the Pirani gauges could not be characterized at lower pressures.

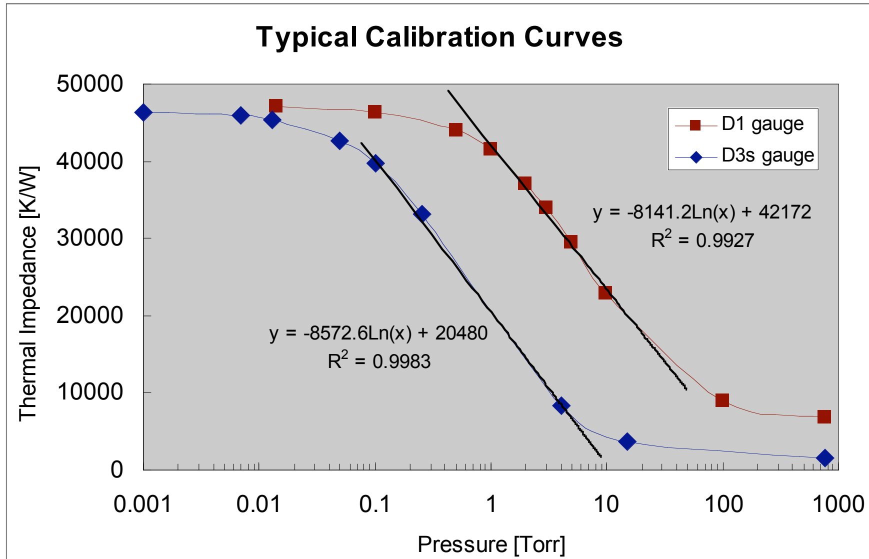


Figure 4.13: Typical D1 and D3s calibration curves.

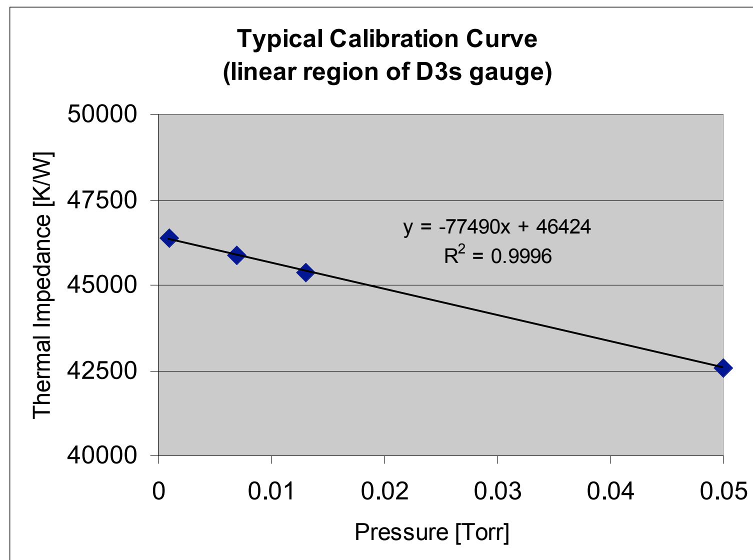


Figure 4.14: The linear portion of the calibration curve from.

4.6.2.2 De-capping for Calibration

As mentioned earlier, packages were calibrated after packaging. To do this, caps where pulled off and the devices put into a dual-in-line package (DIP), wire bonded, and placed in a vacuum chamber (similar as to what was shown in Figure 4.9). Shearing off the caps or using a razor blade to tear of the caps generally caused significant particles which coated the Pirani gauges therefore changing their performance. Drilling a hole

through the cap similarly resulted in particles which coated the Pirani gauges. Instead of either of these two methods for cap removal, caps were pulled of by heating up individual packages on a hot plate to melt the Au-Si alloy and then pulling them off with tweezers. To do this, the hot plate was first heat up to 390ºC. This temperature was measured remotely using a factory calibrated Fluke 66 Infrared Thermometer. The chip was then put onto the hot plate for approximately 30 seconds. In several experiments other dies were exposed to this procedure and no noticeable change in performance was observed. Figure 4.15 shows a package in which the cap was pulled off for calibration.

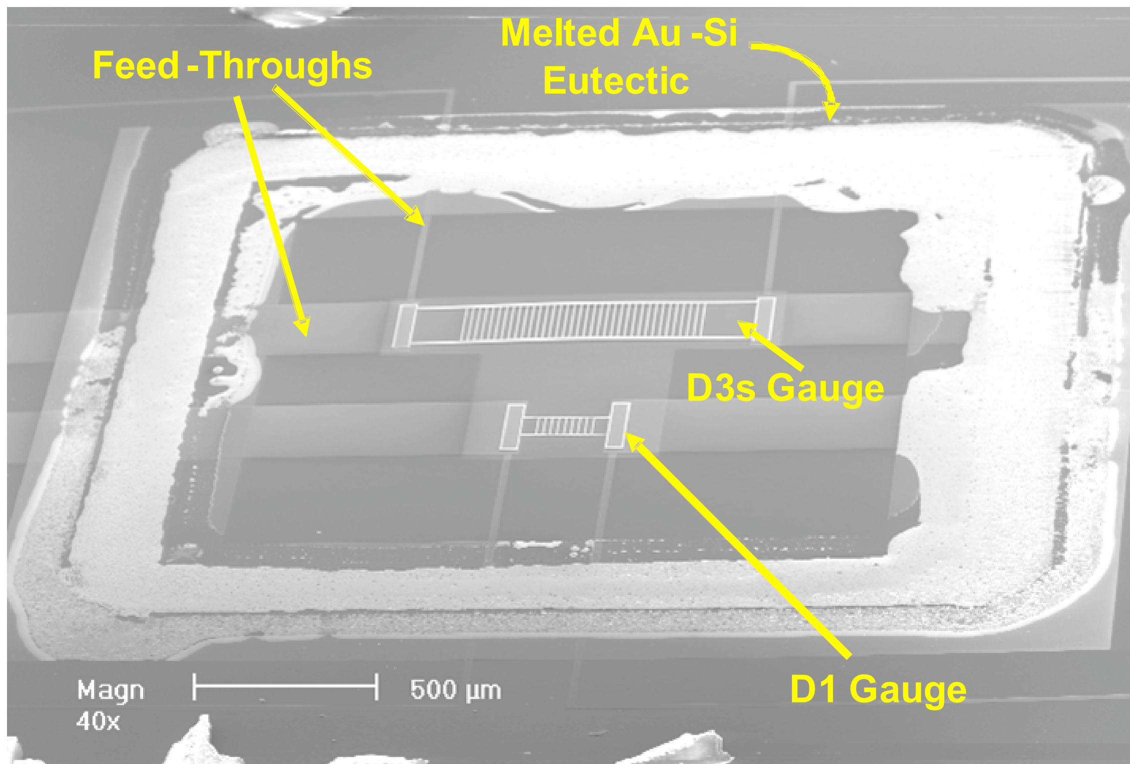


Figure 4.15: Devices after de-capping.

4.6.3 MEASUREMENT ERROR

There are three general types of error that were considered for sensor calibration: accuracy, precision and the temperature sensitivity of the device. These three types of error affected pressure measurement in different ways depending on the pressure range being measured. Section 4.6.3.1 describes the measurement accuracy and its affects in choosing what operation regime of the Pirani gauges to use. Section 4.6.3.2 describes the measurement precision and the resultant measurement resolution. Section 4.6.3.3

explains how the ambient temperature affects the device performance. Finally, Section 4.6.3.4 summarizes the measurement error and the range of operation of the Pirani gauges.

4.6.3.1 Measurement Accuracy

The measurement accuracy was determined predominantly by how well the calibration data matched the performance of the particular gauge being tested. Therefore, for the best measurement accuracy each gauge would have been calibrated. Unfortunately, this was not practical because the de-capping and calibration process was times consuming and because once the devices were de-capped, the packages could no longer be used for reliability or long term testing. It was therefore desirable to test either several gauges from the wafer in which vacuum data was being collected, or from another wafer from the same lot.

Figure 4.16 shows calibration curves from D1 and D3s gauges taken across the wafer for bond #71 (one of the device wafer bonds that will be described in Section 5.3.3.1 of Chapter 5). As illustrated, there is significant variation in performance for different gauges across the wafer. In the log-linear region of the D1 gauge, from 50 to 2 Torr, the predicted pressures for a given thermal impedance vary by approximate ±10 Torr down to approximately ±2 Torr. In the log-linear region of the D3s gauges, from 4 to 0.1 Torr, the predicted pressures for a given thermal impedance vary by approximately ±0.5 down to approximately ±0.05 Torr. Since the exact pressure was not as important as the change in pressure over time, such variation in pressure were deemed acceptable. Therefore, for pressure measurement in these regimes, either several devices from the wafer being tested or several devices from a wafer from the same lot were used for calibration of *all* of the devices across that wafer.

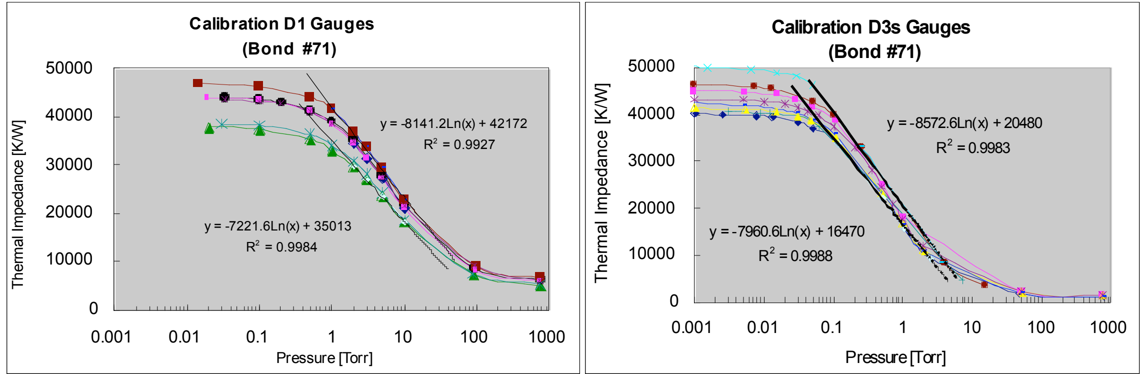


Figure 4.16: Calibration curves across a single wafer for D1 gauges (left) and D3s gauges(right).

Pressure measurement below 100 mTorr on the other hand could not be so easily estimated. Observing the graph of the D3s gauge curves in Figure 4.16, a thermal impedance of 40000 K/W could correspond to a pressure anywhere from <2 mTorr to 100mTorr depending on which Pirani gauge was being tested. This is a difference of 3 orders of magnitude. In this pressure range, it was therefore necessary to calibrate each individual gauge in order to reasonably predict the actual pressure inside of the packaged cavity.

4.6.3.2 Precision

The measurement precision was limited by the measurement error. This *measurement error* resulted in part from noise in the current signal provided from the Keithley 224 source meter and voltage measurement error from the Agilent 34401a multimeter. Other authors have also observed piezoresistive effects, as well as local temperature fluctuations which affect the measurement precision [186].

The measurement precision for D1 and D3 gauges where calculated using the test methodology outlined in Section 4.6.1. These gauges were characterized at different pressures taking 11 successive thermal impedance measurements. The test setup used for this characterization was described in section 4.5 and shown in Figure 4.9. Here the measurement precision was defined by the 99% confidence interval. Using a student T distribution, this 99% confidence interval is 2.718 standard deviation away from the mean. Table 4.6 shows the results for a number of different pressures in the linear and log-linear regions of the D1 and D3s gauges. In Table 4.6 the pressure measurement

resolution was calculated by multiplying the calculated thermal impedance measurement resolution, TI_{res}, by the local slope of the thermal impedance vs. pressure: $TI_{res}\times$slope. Table 4.7 summarizes this data showing the approximate pressure measurement resolutions in different pressure regimes. As illustrated, the pressure measurement resolution is estimated at around 1% and 1-2% respectively of the measured pressure for the D1 and D3s gauges in the log-linear regimes. Below 50 mTorr in the D3s gauge on the other hand, the pressure measurement resolution was relatively constant. The measured resolution was approximately ±2 mTorr. Due to the pressure measurement setup during testing, pressure could only be held to within approximately ±1 mTorr. The pressure measurement resolution below 50 mTorr therefore was likely better than the values shown in Table 4.6.

Table 4.6: The measurement resolution of D1 and D3s gauges at different pressures.

Pressure	Gauge	Region of Graph	Average Thermal Impedance	Thermal Impedance Measurement Resolution (99% Confidence Interval)	Pressure Measurement Resolution
46.0 Torr	D1	Log-linear	16256 K/W	80.22 K/W	±0.44 Torr
9.9 Torr	D1	Log-linear	29781 K/W	57.2 K/W	±0.066 Torr
3.1 Torr	D1	Log-linear	41808 K/W	39.1 K/W	±0.012 Torr
3.0 Torr	D3s	Log-linear	16345 K/W	142.3 K/W	±0.033 Torr
996 mTorr	D3s	Log-linear	30792 K/W	96.33 K/W	±7.5 mTorr
296 mTorr	D3s	Log-linear	49731 K/W	212.5 K/W	±4 mTorr
99 mTorr	D3s	Log-Linear	61159 K/W	266.0 K/W	±2.1 mTorr
30 mTorr	D3s	Linear	66840 K/W	190.9 K/W	±1.8 mTorr
9.9 mTorr	D3s	Linear	68700 K/W	172.2 K/W	±1.7 mTorr
3.0 mTorr	D3s	Linear	69481 K/W	96.3 K/W	±0.95 mTorr

Table 4.7: The measurement resolution of D1 and D3s gauges in different pressures regimes.

Pressure Range	Gauge	Pressure Measurement Resolution
2-50 Torr	D1	±1% of the measured pressure
0.1-4 Torr	D3s	±1-2% of the measured pressure
<0.05 Torr	D3s	±<2 mTorr

4.6.3.3 Error Due to Temperature Fluctuation

Ambient temperature fluctuation was observed to cause changes in sensor performance. This source of error contributes to the pressure measurement error because Pirani gauges use changes in temperature to sense pressure. Overall it would be difficult to integrate a heater and temperature measurement setup into the Pirani calibration setup (described in Section 4.5 and shown in Figure 4.9) for characterizing the drift due to temperature fluctuation. Therefore, the goal of this section was to get a reasonable estimate of the temperature sensitivity of these gauges.

In the log-linear regions of each gauge (from 2 to 50 Torr and 0.1 to 4 Torr for the D1 and D3s gauges respectively) the mathematical model described in section 4.3.1 (*Modeling of a Single Beam Pirani Gauge*) was used to predict changes in the measured pressure. In this model, the temperature was raised and lowered by 2.5ºC and the change in performance was observed.

The model for the 4µm×2.2µm×250µm single beam (S1) was used to estimate the behavior of the 4µm×2.2µm×250µm ladder structure gauge (D1) and the 16µm×2.2µm×1000µm single beam model was used to estimate the behavior of the 16µm×2.2µm×1000µm ladder structure gauge (D3s). In both cases, the model predicted an approximate -0.2% change in the *measured pressure* per 1ºC increase in temperature. Furthermore, the ideal gas law predicts a +0.33% change in the *actual pressure* per 1ºC in a sealed cavity. For package characterization, it was difficult to decouple these two sources of fluctuation in the *pressure measurement* and in the *actual pressure*.

In the linear region of pressure measurement for the D3s gauge (<50mTorr), there was actual test data to analyze the effects of temperature fluctuation on gauge performance. This data was taken during temperature ramping experiments of wafer-level vacuum packaged Pirani gauges (this temperature ramping experiment data is described in more detail in Section 5.4 (*High Temperature Exposure, Thermal Cycling and Burn In*) of Chapter 5). Figure 4.17 shows thermal impedance data vs. temperature data for 5 gauges which were temperature ramped. All of these gauges demonstrated highly regular behavior fitting a 3rd order polynomial fit with an R squared value of greater than 0.9999. Table 4.8 shows all of the base pressures determined after calibration and the slopes of thermal impedance vs. temperature (slope 1) determined from Figure 4.17. Table 4.8

also shows the slope of pressure vs. thermal impedance (slope 2) determined from the calibration curves taken for each of the Pirani gauges (this calibration data is presented in Chapter 5. Multiplying slope 1 times slope 2 (ΔTI/ºC × ΔP/ΔTI) gives an estimate of the temperature sensitivity of the sensor (ΔP/ºC).

Table 4.8 also shows the calculated ΔP/ºC due to the ideal gas law for each gauge which ranged from ±5.5 to ±30 µTorr. The calculated pressure change is therefore around three orders of magnitude lower than the measured ΔP/ºC on each of the Pirani gauges. On the other hand, given the long mean free path length in this pressure regime, the ideal gas law may not apply.

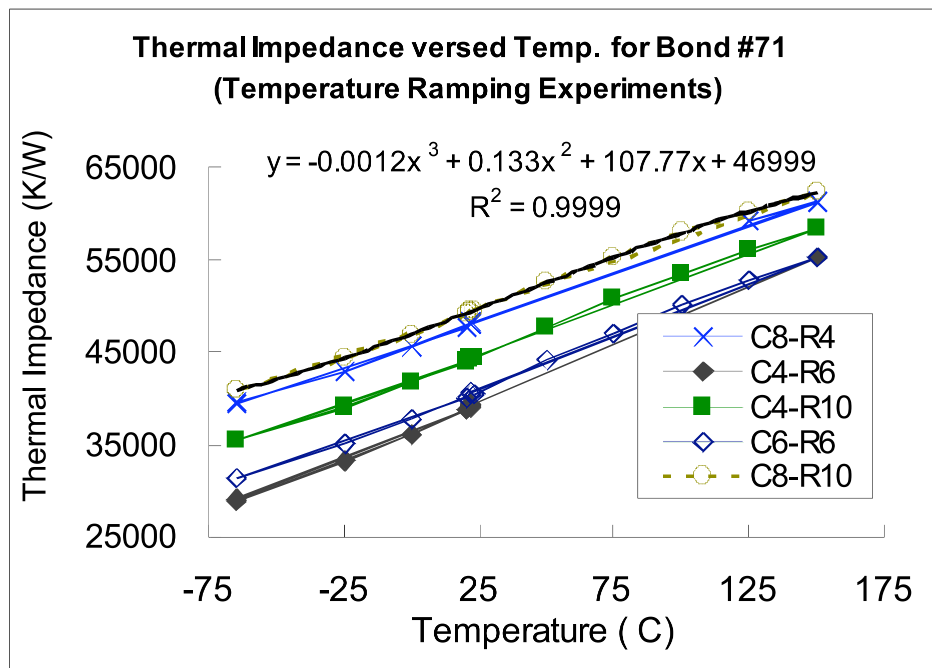


Figure 4.17: Five packaged D3s Pirani gauges which were temperature cycled for reliability testing.

Table 4.8: The drift due to outgassing for D3s gauges at pressures ranging from 1.7 to 9 mTorr.

Gauge	Base Pressure at 23ºC	Slope 1: ΔTI/ ºC at 23ºC (From Figure 3.17)	Slope 2: ΔP/ΔTI at 23ºC (From Calibration Curves in Chapter4)	Total Drift ΔP/ ºC	Calculated ΔP/ ºC due to ideal gas law
C8-R4	7.5 mTorr	102.9	-1.06E-05	-1.3 mTorr	25 µTorr
C4-R6	9 mTorr	122.7	-1.57E-05	-1.9 mTorr	30 µTorr
C4-R10	3.3 mTorr	109.4	-1.50E-05	-1.6 mTorr	11 µTorr
C6-R6	7.8 mTorr	113.9	-1.69E-05	-1.9 mTorr	26 µTorr
C8-R10	1.7 mTorr	101.8	-1.31E-05	-1.3 mTorr	5.5 µTorr

4.6.3.4 Summary of Pirani Gauge Performance

Table 4.9 summarized the performance of the two gauges used for pressure measurement for pressures from <2 mTorr up to 760 Torr. The various sources of error are summarized in this table for the different pressure measurement regimes. Shown are i) the measurement resolution, ii) the pressure change inside of a micro-cavity due to the ideal gas law, iii) the average calculated drift due to temperature fluctuation and iv) the total calculated error from all of these sources.

Table 4.9: The measurement resolution, drift and fluctuation due to the ideal gas law for D1 and D3s gauges in different pressures regimes.

Pressure Range	Gauge	i) Pressure Measurement Resolution	ii) Pressure Change in Due to Ideal Gas Law in a Sealed Cavity	iii) Calculated Drift Due to Temperature Fluctuation	iv) Total Calculated Error (assuming ±1ºC temperature fluctuation)
50-760 Torr	D1	Order of magnitude estimate	-	-	-
4- 760 Torr	D3s	Order of magnitude estimate	-	-	-
2-50 Torr	D1	1.5% of the measured pressure	+0.33% of Pressure/ºC	-0.2% of Pressure/ºC	±0.033 to ±0.82 Torr
0.1-4 Torr	D3s	1-2% of the measured pressure	+0.33% of Pressure/ºC	-0.2% of Pressure/ºC	±4.1 to ±65 mTorr
<0.05 Torr	D3s	<2mTorr Torr	<+50 μTorr/ ºC	-1.7 mTorr/ºC	±3.7 mTorr/ºC

CHAPTER 5

VACUUM CHARACTERIZATION OF MICROPACKAGES

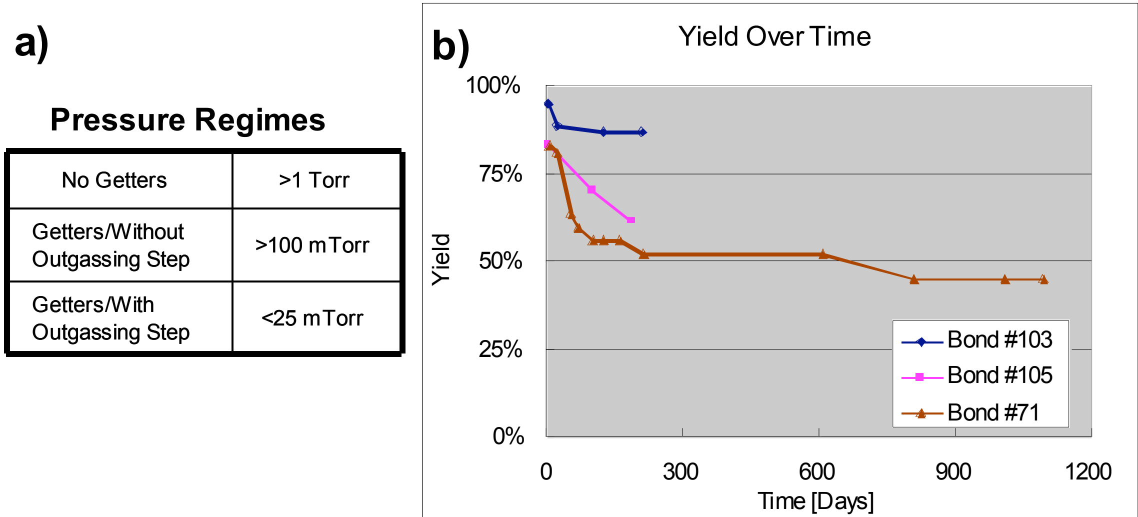
In Chapter 2 bond experiments were conducted in the development of the Au-Si eutectic bonding process. Using these results Chapter 3 presented a process for encapsulating sensors. Chapter 4 then presented the design of Pirani (vacuum) gauges—these Pirani (vacuum) gauges were designed specifically for integration with the Au-Si eutectic bonding process in Chapter 3. This chapter present the vacuum data from these packaged Pirani gauges.

In Chapter 3, three different device wafer processes were outlined: i) a process with 0.3 μm poly-Si bond rings, ii) a process with 2.2 μm heavily phosphorous doped poly-Si bond rings, and iii) a process with 500/5000Å Cr/Au bond rings. Processes i) and iii) produced yields of better than 80%. The vacuum packaging results for devices packaged in these processes are described in detail in the chapter. The vacuum packaging results from process ii) on the other hand resulted in yields from 0-43% (these low yield results resulted in part from Au-Si eutectic lateral flow onto the getters—see Section 2.5.3 for more detail). These vacuum packaging results are presented in .

Figure 5.1 summarizes the data presented in this chapter. As illustrated in Figure 5.1a, three different pressure regimes were achieved: i) pressures of greater than 1 Torr were observed for bonds conducted *without* getters, ii) pressure greater than 100 mTorr where observed for bonds conducted *with* getters but *without* an outgassing step, and iii) pressures below 25mTorr were observed for bonds *with* getters and *with* the outgassing step.

Figure 5.1b shows the estimated yield over time for 3 wafers. As illustrated, bond #71 and #105 had sharp decrease in yield over time whereas bond #103 appeared to have a

relatively flat yield over time. A short discussion is presented at the end of the chapter on the possible processing issues that might cause these different behaviors.



Pressure Regimes

No Getters	>1 Torr
Getters/Without Outgassing Step	>100 mTorr
Getters/With Outgassing Step	<25 mTorr

Figure 5.1: A summary of the data presented in this chapter showing a) the different pressure regimes that were achieved, and b) the yield over time estimated across several wafers.

In this chapter, Section 5.1 first presents background on physical leaks and outgassing and their affect on the pressures inside of micro-packages. Section 5.2 then presents specific attributes of the device layout for the wafers used in bond experiments that were important for device testing. Section 5.3 presents the vacuum packaging and long term testing results. Section 5.4 then presents some high temperature exposure and thermal cycling results. Finally, Section 5.5 presents an overall summary of these vacuum results.

5.1 Physical Leaks and Outgassing

There are two major sources of pressure increase in micro-cavities: 1) through a physical leak path and 2) due to outgassing of molecules from the inside surface. Section 5.1.1 discusses physical leaks and Section 5.1.2 discusses outgassing as background for the pressure measurement results presented later in this chapter.

5.1.1 PHYSICAL LEAKS

A leak generally refers to gas flowing from a high pressure region to a low pressure region through an opening. Physical leak paths are particularly large challenges for MEMS devices packaged at the wafer-level because of their small volumes. Table 5.1 shows the leak rate for several different orifice sizes [204]. Given the smallest leak rate in Table 5.1 of 10^{-10} for a 1 cm long 0.2 μm diameter capillary, Table 5.2 shows the amount of pressure change that should occur for a number of typical package volumes. As illustrated, for the packages used in this work, such a capillary would result in a 163 Torr increase in 1 day. Given the 3.7 to 820 mTorr pressure measurement resolution (depending on the gauge and the pressure range) of the Pirani gauges used in this work (see Table 4.9 of Chapter 4), 1 day of testing should be more than enough to detect any physical leak. Therefore, for package characterization in this chapter, physical leak paths are likely failure mechanisms only in cases where large sudden changes in pressure are observed (on the order of tens of Torr in one 1 day).

Table 5.1: The leak rates calculated for a range of capillary sizes [204].

Leak Rate (torr.Liter.second^{-1})	Equivalent Opening
10^{-3}	Rectangular slit with 1 cm width, 0.1 mm height and 1 cm depth
10^{-4}	Rectangular slit with 1 cm width, 30 μm height and 1 cm depth
10^{-5}	Capillary 1 cm long and 7 μm in diameter
10^{-6}	Capillary 1 cm long and 4 μm in diameter
10^{-7}	Capillary 1 cm long and 1.8 μm in diameter
10^{-8}	Capillary 1 cm long and 0.8 μm in diameter
10^{-9}	Capillary 1 cm long and 0.4 μm in diameter
10^{-10}	Capillary 1 cm long and 0.2 μm in diameter

Table 5.2: The amount of pressure change in 1 day for different package dimensions given a leak rate of 10^{-10} Torr·Liter/second.

Type of Package	Package Dimensions	Leak Rate	Pressure Rise in 1 day
Chip Scale Package	5×5×1.5 mm	10^{-10} Torr·Liters/Second	0.23 Torr
Gyroscope (wafer level)	2×2×0.3 mm	10^{-10} Torr·Liters/Second	7.2 Torr
Package in this work (wafer level)	**2.3×2.3×0.1mm**	**10^{-10} Torr·Liters/Second**	**163 Torr**
3-D Accelerometer (wafer level)	0.5×0.5×0.3mm	10^{-10} Torr·Liters/Second	115 Torr
Thin Film Package (wafer level)	0.5×0.5×0.01mm	10^{-10} Torr·Liters/Second	3456 Torr

5.1.2 OUTGASSING IN MICRO-CAVITIES

Throughout the vacuum science literature, much work has been reported on developing and improving macro-scale vacuum systems and on the study of the effects of outgassing [205-208], but there is very little data to on the behavior of vacuums in micro-cavities ($1x10^{-9}$ to $1x10^{-6}$ liters). Outgassing involves desorption of materials (such as H_2O, H_2, N, O and CO_2 and hydrocarbons) from the inside surface and bulk of vacuum chambers. Extensive investigations have been conducted to determine how to remove these atoms from vacuum systems in order to lower pressures (Figure 5.2a and Figure 5.2b). Typically H_2O is the dominant outgassing molecule [205, 206]. In humid environments (such as a cleanroom), hundreds of monolayers of H_2O can form on the surface of a wafer.

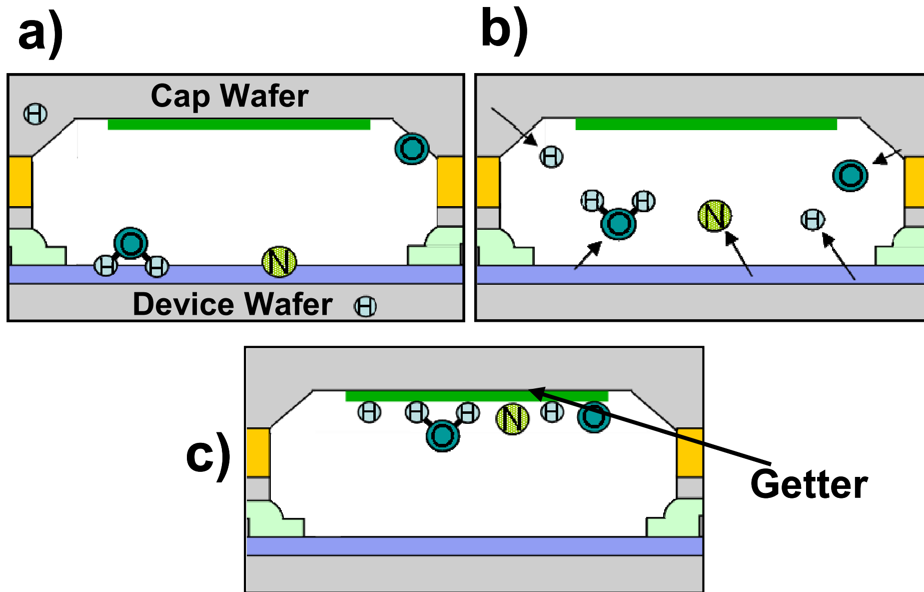


Figure 5.2: An illustration of a) molecules which have adsorbed on the surface or into the bulk of the micro-vacuum chamber, b) molecules that desorb off of the chamber walls to increase the pressure and c) these molecules reacting with the getter to lower the package pressure.

In standard vacuum systems the pressure, p, can be calculated as a function of time:

$$p(t) = \left(p_0 - \frac{\dot{Q}_{in}}{S}\right) \cdot \exp\left(-\frac{S}{V}t\right) + \frac{\dot{Q}_{in}}{S} \tag{5.1}$$

where p_0 is the pressure at the pump, S is the pump speed, V is the volume of the chamber, and $\dot{Q}_{in}$ is the flow rate into the vacuum chamber. This flow rate is generally dominated by outgassing. The flow rate due to outgassing is conventionally modeled as:

$$\dot{Q}_{OUTGAS} = \frac{a_{1h} \cdot A}{\left(\frac{t}{1h}\right)^{\alpha}} \tag{5.2}$$

where A is a geometrical factor, and a_{1h} and α are fitting parameters.

On the other hand, in a sealed micro-cavity, there is only the net flow into the cavity, $\dot{Q}_{in}$. Assuming there is no leak path, the pressure, p, in this micro-cavity can be determined as:

$$p(t) = \int_0^t \frac{\dot{Q}_{OUTGAS}}{V} dt \qquad (5.3)$$

Considering Equations 5.1and 5.3 the pressure inside a sealed micro-cavity will be significantly higher than the vacuum chamber it was sealed in for two reasons: 1) the micro-cavity is not continuously pumped as in the case for Equation 5.1, and 2) Equation 5.3 shows that for a given surface area, smaller volumes will cause higher pressures—thus the larger surface to volume ratio of micro-cavities causes higher pressures.

Another important parameter for outgassing is temperature. In addition to Equation 6.4, the outgassing rate, $\dot{Q}_{OUTGAS}$, is often modeled as a function of the diffusion constant: $\dot{Q}_{OUTGAS} = f(D)$, where D is the diffusion constant of the particular molecule being outgassed from a specified material. This diffusion constant is generally determined from the Arrhenius diffusion equation as [206]:

$$D = D_0 \exp(-\Delta E / RT) \qquad (5.4)$$

where D_0 is a constant, ΔE is the thermal activation energy which is a constant, R is the gas constant, and T is the temperature. As would be expected, the amount of outgassing increases with increased temperature.

There are two important points to consider from this discussion: i) micro-cavities are particularly susceptible to outgassing because of their high surface to volume ratios and ii) increases in temperature should facilitate more outgassing.

5.2 DEVICE LAYOUT CONSIDERATIONS FOR TESTING

Details on the processing of the cap and device wafers were described in Chapter 3 as well as some of the details of the layout and size of the bond rings used. This section describes some specifics of the layout that were important for Pirani gauge testing. Figure 5.3 shows the device layout of each cell for the packages fabricated for this study. As illustrated, each cell consisted of 4 dies which take up a 5.4 by 8.1 mm area. In each die, there are bond pads on the periphery of the die and a bond ring that encircles each device. As shown, there are D1 and D3s Pirani gauges (their design was detailed in Chapter 4) as well as resonators and a test structure. The resonators and the test structure

in fact were not tested in this work. As illustrated, in 3 of the 4 dies, there are D1 Pirani gauges and in 2 of the 4 dies there are D3s Pirani gauges. As explained in Chapter 4 (see Table 4.9), the D1 and D3s gauges were used for accurate pressure measurement from 50 Torr to 2 Torr and 4 Torr to 2 mTorr respectively. Pressures outside of this range were determined using an order of magnitude estimation.

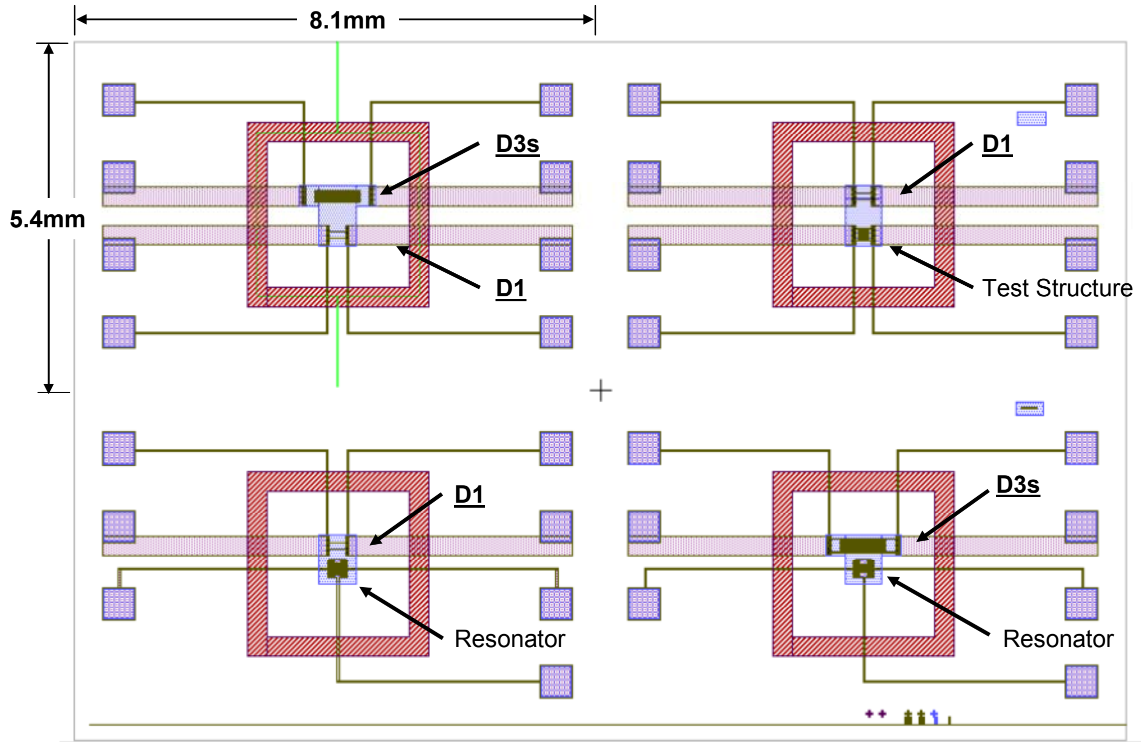


Figure 5.3: Layout of the packaged sensors used for characterization of micro-packages. The resonators and Test structures were not utilized in this work.

Figure 5.4 shows a wafer with 124 packaged devices which were created using the above described layout. As illustrated there are 10 rows and 14 columns. Comparing Figure 5.3 and Figure 5.4, all of the devices which are in an *odd column and an odd row* or an *even column and an even row* have the D3s Pirani gauges. Pressures in the mTorr range could therefore be measured in these packages. On the other hand, the D1 gauges were in all of the packages *except* in those dies in the *even column and even row*. In all of these packages pressure in the Torr range could be accurately measured.

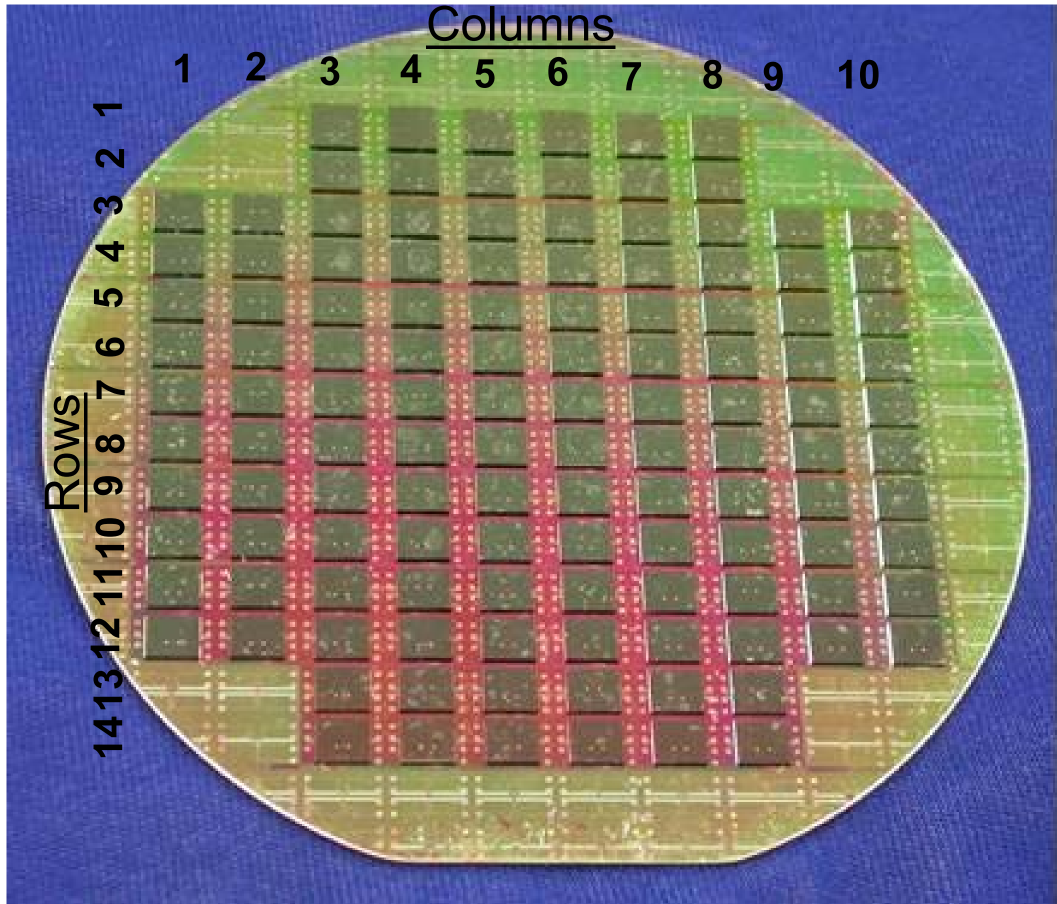


Figure 5.4: A wafer with 124 packaged devices in which there are 10 columns and 14 rows.

5.3 Vacuum Packaging Results

Table 5.3 summarizes the vacuum packaging results across 6 wafers in which Pirani gauges were packages. Including in Table 5.3 is the measured pressure range across the wafer and the initial yield. The initial yield was defined by the packages ability to hold vacuum. In calculating the yield, the pressure necessary for a "passing" package varied depending on the pressure ranges which were achieved across that wafer. As a metric, for packages in vacuum, packages with pressures greater than 3 standard deviations outside of the mean were considered outliers. These outliers were determined to have "failed" and were counted against the yield.

All of the bonds in this section used the bonding process described in Chapter 3 (both with and without the outgassing step). As illustrated in Table 5.3, there were three pressure regimes which were achieved depending on the process parameters: i) pressures

of greater than 1 Torr where observed for bonds conducted without getters, ii) pressures between 100 mTorr and 2.5 Torr where observed for bonds conducted *with* getters but *without* the outgassing step, and iii) pressures below 25 mTorr were achieved *with* getters and *with* the 60 minute, 345ºC outgassing step. Sections 5.3.1 describes the vacuum results for bonds *without* getters, Section 5.3.2 describes the vacuum results for bonds *with* getters but *without* an outgassing step, and Section 5.3.3 describes the vacuum results for bonds *with* getters and *with* an outgassing step.

Table 5.3: Various device bonds with pressures in three different pressure ranges.

Bond #	Bond Ring width	Device Bond Ring (material/ thickness)	Release	Getter	Outagassing Step	Pressure Range	Yield
No getters (>1 Torr)							
67	300 µm	Poly-Si (0.3µm)	Methanol	No	Yes	~1.6-11.8 T*	17/17 (**)
100	300 µm	Au (0.5µm)	Methanol	No	No	2.4-43.5 T	37/46 (80.4%)
Getters/No Outgassing Step (100 mTorr-2.5 Torr)							
103	150 µm	Au (0.5 µm)	CPD	Yes (Shadow Mask)	No	150-980 mT	55/58 (94.1%)
105	100 µm	Au (0.5 µm)	CPD	Yes (Shadow Mask)	No	77-2400 mT	44/52 (84.6%)
Getters/Outgassing Step (<20 mTorr)							
71	300 µm	Poly-Si (0.3µm)	Methanol	Yes (Lift off)	Yes	1.9-16.3 mT	51/63 (81.0%)
78	300 µm	Poly-Si (0.3µm)	Methanol	Yes (Shadow Mask)	Yes	<2 -23.3 mT	16/47 (34.0%)

*Calibrated using devices from other wafers in the same lot.
**Not enough data to calculate approximate yield.

5.3.1 BONDS WITHOUT GETTERS, >1 TORR PRESSURE

As shown in Table 5.3, in bonds #67 and #100 getters were not used. The measured packaged pressures across these wafers ranged from 2-45 Torr. Because pressures were in the Torr range, the log-linear region of the D1 gauges were used for pressure measurement (see Table 4.9 in Chapter 4). Bonds #67 and #100 differ from each other in two ways: the device bond ring material (bond #67 used poly-Si for the device wafer bond rings and bond #100 used Au on the device wafer bond rings) and the use of an outgassing step (bond #67 used an outgassing step and bond #100 did not). Though the bond ring material could potentially affect the yield, it likely would not affect the

packaged pressures.

5.3.1.1 Analysis of Bond #67

The devices used for calibration of bond #67 were taken on D1 gauges from bond #71, since these two wafers were fabricated in the same lot and had similar R_0 (low current resistance) values. Figure 5.5 shows the calibration curves taken from bond #71, where Pirani gauges were taken from the top, bottom, center, left and right sections of the wafer. As a comparison, bond #67 gauges had R_0 values from 485.70-581.78Ω as compared to bond #71 gauges which had R_0 values from 505.21-671.03Ω. Furthermore, for all of the devices probed across bond #67, a measurement at atmospheric pressure was taken before they were packaged. The measured thermal impedances were between 4629-7601 K/W as compared to those used for calibration in bond #71 which were between 5629-7382 K/W.

Figure 5.6 shows the measured thermal impedances across bond #67 (left) and the estimated pressures calculated from those thermal impedances (right). These pressures were calculated using the average of the calculated pressure predicted from the two fit lines in the calibration plot (Figure 5.5). Assuming that the thermal impedance vs. pressure curve of each device fits somewhere between the two fit lines in Figure 5.5, each of the estimated pressures is within ±2 Torr of the actual value. As illustrated, pressures ranging from 2.6±2 to 11.7±2 Torr were measured. Because pressures from only 17 packages were measured, the yield on this wafer was not estimated.

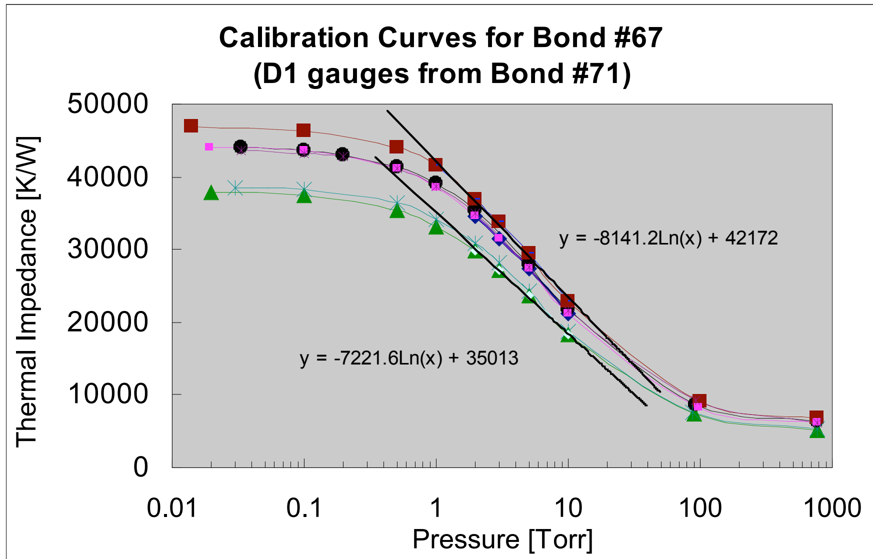


Figure 5.5: Calibration curves for Pirani gauges from D1 gauges from bond #71. Devices from these wafers, fabricated in the same lot, had nearly identical low current resistances and had atmospheric pressure measurements in the same range.

Thermal Impedances (K/W)

	1	2	3	4	5	6	7	8	9	10
1			NM		NM		NM			
2				NM		NM		NM		
3	NM		NM		22385		24851		26457	
4		NM		NM		NM		NM		NM
5	19972		NM		20734		23862		NM	
6		NM		NM		NM		NM		NM
7	NM		NM		23425		24815		25148	
8		NM		NM		NM		NM		NM
9	25951		NM		24481		26193		NM	
10		NM		NM		NM		NM		NM
11	29743		NM		NM		NM		25527	
12		NM		NM		NM		NM		NM
13			31124		28178		31702			
14				NM		NM		NM		

Pressures (Torr)

	1	2	3	4	5	6	7	8	9	10
1			NM		NM		NM			
2				NM		NM		NM		
3	NM		NM		8.6		6.2		5.1	
4		NM		NM		NM		NM		NM
5	11.7		NM		10.6		7.1		NM	
6		NM		NM		NM		NM		NM
7	NM		NM		7.5		6.3		6.0	
8		NM		NM		NM		NM		NM
9	5.4		NM		6.5		5.3		NM	
10		NM		NM		NM		NM		NM
11	3.3		NM		NM		NM		2.8	
12		NM		NM		NM		NM		NM
13			2.8		4.1		2.6			
14				NM		NM		NM		

NM No measurement taken

Bond #67

Figure 5.6: The thermal impedance measured on gauges across bond #67 (left) and the estimated pressures corresponding to these measurements (right).

5.3.1.2 Analysis of Bond #100

Figure 5.7 shows the calibration curves used for estimating pressures in the bond #100

packages. The devices taken for these calibration curves were from bond #100. These gauges were taken from the wafer after packaging and were taken from the top, center and bottom of the wafer (the specific locations for each of these devices are highlighted in Figure 5.8). Figure 5.8 shows the measured thermal impedances across bond #100 (left) and the estimated pressures calculated from those thermal impedances (right). As illustrated, there were quite a few packages which could not be evaluated because of non-functional devices. In most of the packages marked *sensor not functioning* in Figure 5.8, there were problems with the feed-through interconnect lines. This may have resulted from a processing issue described in Section 2.3.5.1 in Chapter 2, from an insufficient dehydration bake before depositing the Cr/Au bond ring on the device wafer.

The pressures listed in Figure 5.8 were calculated using the average of the calculated pressure predicted from the two fit lines in the calibration plot (Figure 5.7). It was assumed that if more gauges had been taken from the wafer for characterization, a larger variance in performance would have been seen. Therefore, the error in the pressure measurement was assumed to be ±2 Torr as was the case in the previous section. As illustrated in Figure 5.8, pressures ranging from 2.4±2 to 43.6±2 Torr were measured. One package had an estimated pressure of approximately 100 Torr. Though this package held vacuum, it was considered an outlier and was counted against the yield. Of the 46 packages tested, 37 where determined to be in an acceptable pressure range (that is, <3 standard deviations from the mean for packages which held some level of vacuum). An initial yield of 80.4% was therefore calculated.

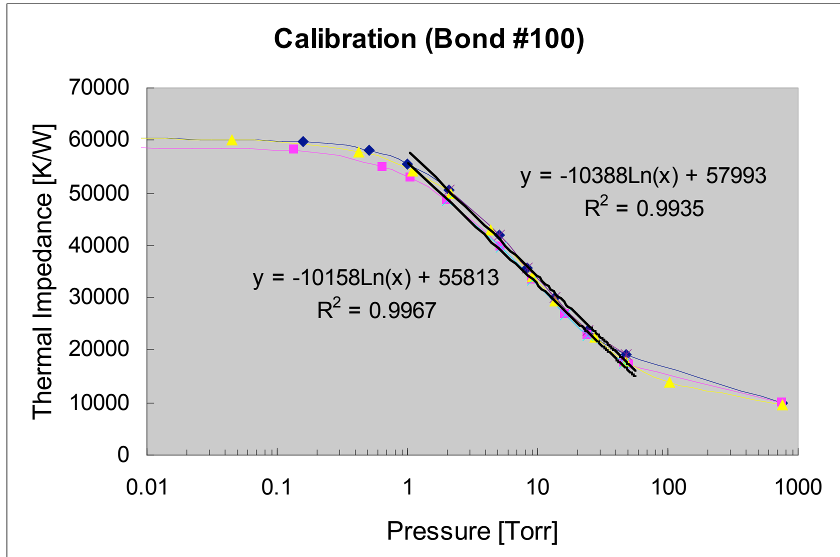


Figure 5.7: Calibration curves for Pirani gauges from D1 gauges from bond #100. The devices used for calibration were taken from the top, bottom and center of the wafer and are highlighted in figure 4.11.

Thermal Impedances (K/W)

	1	2	3	4	5	6	7	8	9	10
1			18789	B	39437	B	40862	B		
2			B		39214		B			
3	B		B	43622	B	12011	39792	B	B	B
4	B		B		42906		16296		B	
5	B	B	B	23232	B	40152	B	840	B	B
6	B		11200		40567		29205		B	
7	B	B	39862	41663	38135	41183	41662	22537	B	
8	B		37983		39584		40406		B	
9	B		8745	42671	21370	41511	42700	B	B	B
10	B		23422		27862		42177		B	
11	B	B	B	49075	41664	46397	46485	B	B	B
12	B		39077		34991		48098		B	
13			B	19288	31569	B	B	B		
14			38584		31272		B			

Pressures (Torr)

	1	2	3	4	5	6	7	8	9	10
1			43.6	B	6.0	B	5.2	B		
2			B		6.1		B			
3	B		B	4.0	B	760	5.8	B	B	B
4	B		B		4.3		100		B	
5	B	B	B	28.4	B	5.6	B	760	B	B
6	B		760		5.4		16.0		B	
7	B	B	5.7	4.8	6.8	5.0	4.8	30.4	B	
8	B		6.9		5.9		5.4		B	
9	B		760	4.4	34.0	4.9	4.4	B	B	B
10	B		27.9		18.2		4.6		B	
11	B	B	B	2.4	4.8	3.1	3.0	B	B	B
12	B		6.2		9.2		2.6		B	
13			B	41.5	12.7	B	B	B		
14			6.5		13.1		B			

(orange)	>50 Torr	(outlined)	Sensor Used for Calibration
B	Sensor not functional		**Bond #100**

Figure 5.8: The thermal impedance measured on gauges across bond #100 (left) and the estimated pressures corresponding to these measurements (right).

5.3.1.3 Long Term Testing for Bonds without Getters

In addition to the initial pressure measurement data, pressures were monitored over

time for the 15 packages tested from bond #67. In Figure 5.9 and Figure 5.10, these pressures were graphed verses time.

Figure 5.9 shows 9 packages with measured pressures ranging from 3 to 12 Torr where the pressure fluctuated from ±0.10 to ±0.51 Torr. Part of this fluctuation may have resulted from measurement error. For the D1 gauge in the 3 to 12 Torr pressure range, the calculated measurement error ranged from ±0.031 to ±0.16 Torr (see Table 4.9 of Chapter 4). This only accounted for some of the observed pressure fluctuation over time. One possible additional source of these measured pressure fluctuations over time may have been from adsorption and desorption of gases to and from the inside cavities (chemisorption and outgassing).

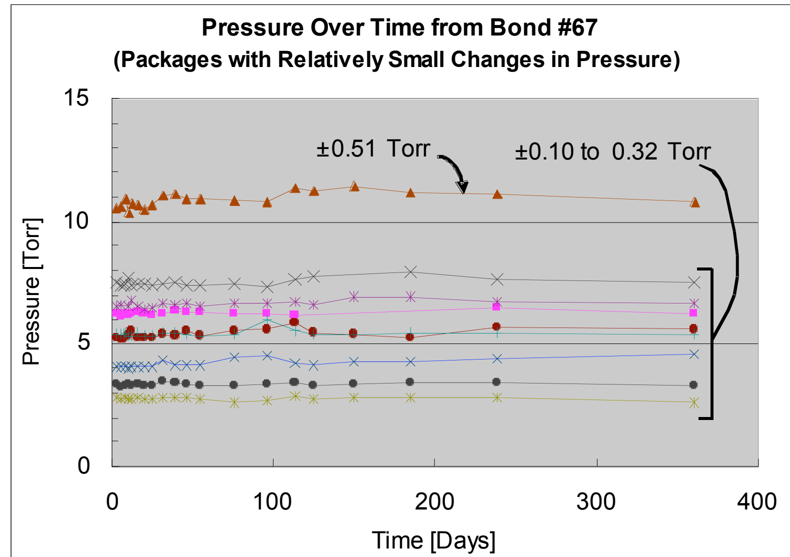


Figure 5.9: Pressures determined from the measured thermal impedances over time using the calibration curves in Figure 5.5 to determine pressures. All of these devices had ±0.5 Torr or less pressure fluctuation over time.

Figure 5.10 shows the 6 packages in which the pressures changed by >3 Torr in 1 month to 1 year of testing. In all of these packages there was a net increase in pressure over time. As illustrated, C1-R5 experienced a sudden change in pressure from 14.5 Torr to approximately 100 Torr in the 39th day of testing. This sudden change in pressure may indicate a physical leak. The pressure for C5-R3 fluctuated up and down with a net increase over time. The other four packages demonstrated a fairly consistent pressure

increase that slowed over time. This slow measured pressure increase over time is likely caused by outgassing.

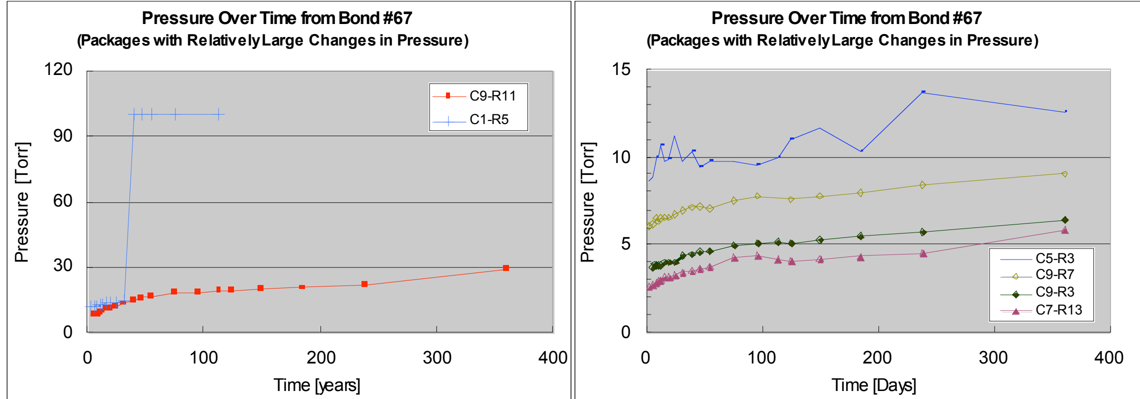


Figure 5.10: Pressures determined from the measured thermal impedances over time using the calibration curves in Figure 5.5 to determine pressures. All of these devices had a >3 Torr pressure change over time.

To observe whether these trends were consistent with typical outgassing trends, the pressures in Figure 5.10 were converted to units of outgassing flow rate per unit area, $\dot{Q}/A$, using the following expression:

$$\dot{Q}/A = \frac{V_{cavity} \cdot \Delta P}{A_{cavity}} \tag{5.5}$$

where V_{cavity} is the volume of the cavity, A_{cavity} is the surface area inside of the cavity, and ΔP is the change in pressure. ΔP was estimated at each time increment by taking the slope of three pressure measurements vs. time in Figure 5.10. This slope was calculated using: the data point taken *directly before* the pressure measurement, P_{t-1}; the data point *at that time* increment, P_t; and the data point taken *directly after* that time increment, P_{t+1}:

$$\Delta P_t = slope(P_{t-1}, P_t, P_{t+1}) \tag{5.6}$$

The resultant graph of $\dot{Q}/A$ vs. time is shown in Figure 5.11. As illustrated on the log-log plots, the calculated outgassing rates for each of the packages demonstrates somewhat of a power law decay over time as would be expected for Outgassing [205-

208].

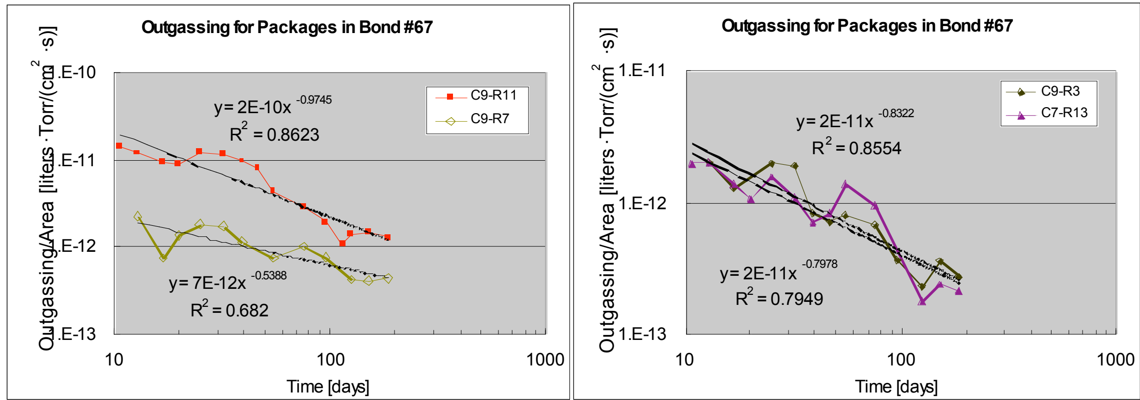


Figure 5.11: The outgassing/area for 4 packages from bond #67.

5.3.2 BONDS WITH GETTERS, >100 mTORR PRESSURE

As was shown in Table 5.3, in bonds #103 and #105 getters were used, and the 345ºC 1 hour long outgassing step was omitted. These bonds resulted in pressures ranging from 100 mTorr to 2.4 Torr. Because pressures were in the hundreds of mTorr, the log-linear region of the D3s gauges were used for pressure measurement (see Table 4.9 in Chapter 4). As compared to many of the other bond tests, thinner bond ring widths of 150 and 100 μm respectively were used in these bonds and in both cases, the bond ring material on the device side was Au.

5.3.2.1 Analysis of Bond #103

Figure 5.12 shows the calibration curves used for predicting the pressures measured in the bond #103 gauges. The devices taken for these calibration curves were from bond #103. These gauges were taken from the wafer after packaging and were taken from the top, center and bottom of the wafer (the specific locations for each of these devices are highlighted in Figure 5.13). Figure 5.13 shows the measured thermal impedances across bond #103 (left) and the estimated pressures calculated from those thermal impedances (right). These pressures were calculated using the average of the calculated pressure predicted from the two fit lines in the calibration plot (Figure 5.12). Assuming that the thermal impedance vs. pressure curve of each device fits somewhere between the two fit

lines in Figure 5.12, each of the estimated pressures is within ±100 mTorr of the actual value. As illustrated in Figure 5.13, pressures ranging from 150±100 to 980±100 mTorr were calculated. One package had a measure pressure of approximately 5.2 Torr. Though this package held vacuum, it was considered an outlier and was counted against the yield. Of the 58 packages tested, 55 where determined to be in an acceptable pressure range (that is, <3 standard deviations from the mean for packages which held some level of vacuum). An initial yield of 94.1% was therefore calculated.

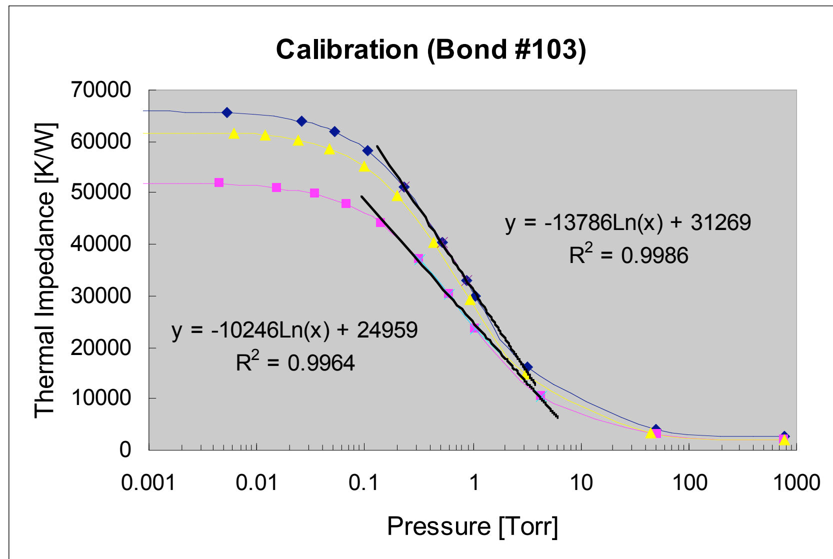
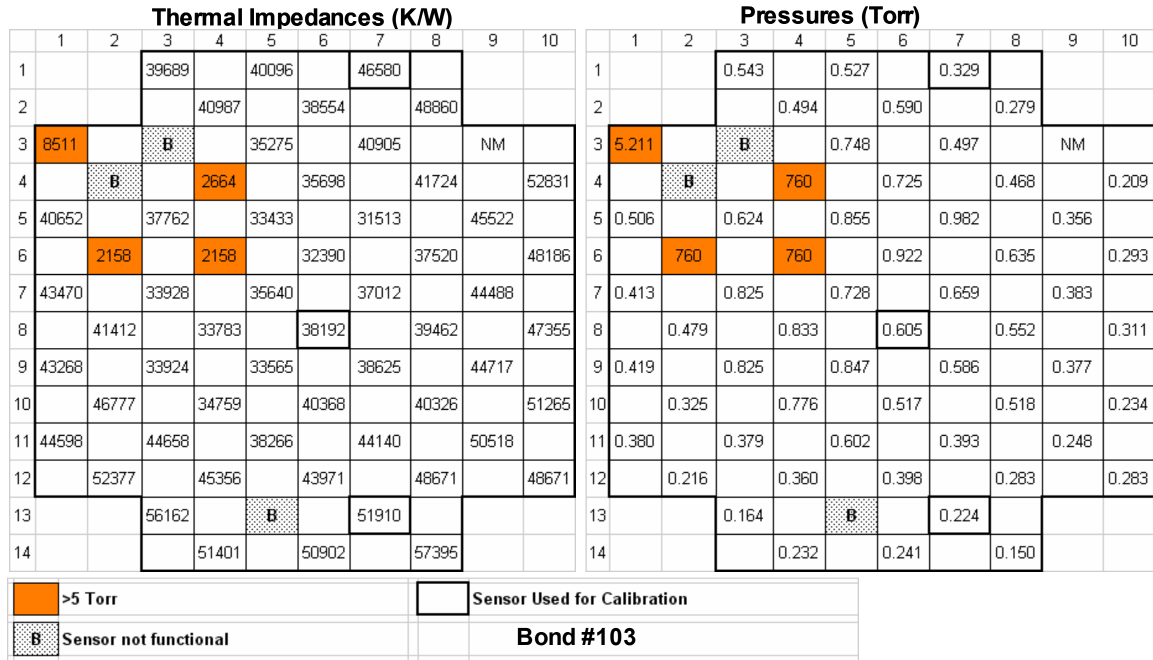


Figure 5.12: Calibration curves for Pirani gauges from D3s gauges from bond #103. The devices used for calibration were taken from the top, bottom and center of the wafer and are highlighted in Figure 5.13.



Thermal Impedances (K/W)

	1	2	3	4	5	6	7	8	9	10
1			39689		40096		46580			
2				40987		38554		48860		
3	8511		B		35275		40905		NM	
4		B		2664		35698		41724		52831
5	40652		37762		33433		31513		45522	
6		2158		2158		32390		37520		48186
7	43470		33928		35640		37012		44488	
8		41412		33783		38192		39462		47355
9	43268		33924		33565		38625		44717	
10		46777		34759		40368		40326		51265
11	44598		44658		38266		44140		50518	
12		52377		45356		43971		48671		48671
13			56162		B		51910			
14				51401		50902		57395		

Pressures (Torr)

	1	2	3	4	5	6	7	8	9	10
1			0.543		0.527		0.329			
2				0.494		0.590		0.279		
3	5.211		B		0.748		0.497		NM	
4		B		760		0.725		0.468		0.209
5	0.506		0.624		0.855		0.982		0.356	
6		760		760		0.922		0.635		0.293
7	0.413		0.825		0.728		0.659		0.383	
8		0.479		0.833		0.605		0.552		0.311
9	0.419		0.825		0.847		0.586		0.377	
10		0.325		0.776		0.517		0.518		0.234
11	0.380		0.379		0.602		0.393		0.248	
12		0.216		0.360		0.398		0.283		0.283
13			0.164		B		0.224			
14				0.232		0.241		0.150		

Figure 5.13: The thermal impedance measured on gauges across bond #103 (left) and the estimated pressures corresponding to these measurements (right).

5.3.2.2 Analysis of Bond #105

Figure 5.14 shows the calibration curves used for predicting pressures in bond #105 packages. The devices taken for these calibration curves were from bond #105. These gauges were taken from the wafer after packaging and were taken from the top, center and bottom of the wafer (the specific locations for each of these devices are highlighted in Figure 5.15). Figure 5.15 shows the measured thermal impedances across bond #105 (left) and the estimated pressures calculated from those thermal impedances (right). These pressures were calculated using the average of the calculated pressure predicted from the two fit lines in the calibration plot (Figure 5.14). Assuming that the thermal impedance vs. pressure curve of each device fits somewhere between the two fit lines in Figure 5.14, each of the estimated pressures is within ±50 mTorr of the actual value. As illustrated in Figure 5.15, pressures ranging from 77±50 mTorr to 2.4±0.05 Torr were measured. Several packages also had pressures of around 50 Torr. Though these packages held vacuum, they were considered outliers and were counted against the yield. Of the 52 packages tested, 44 where determined to be in an acceptable pressure range (that is, <3 standard deviations from the mean for packages which held some level of

vacuum). An initial yield of 84.6% was therefore calculated.

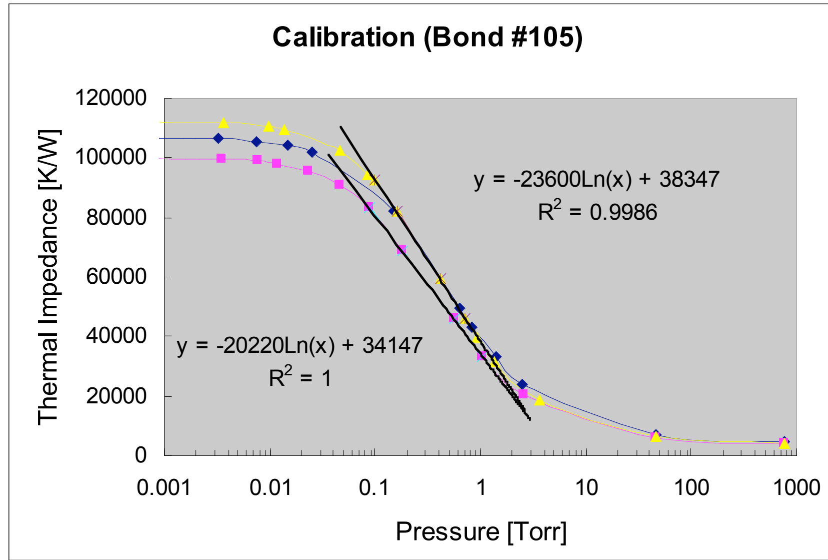


Figure 5.14: Calibration curves for Pirani gauges from D3s gauges from bond #105. The devices used for calibration were taken from the top, bottom and center of the wafer and are highlighted in Figure 5.15.

Thermal Impedances (K/W)

	1	2	3	4	5	6	7	8	9	10
1			55561		78922		92594			
2				70585		17194		89134		
3	B		78348		71797		73371		98925	
4		61892		60418		49530		76171		B
5	B		73452		67082		38397		89685	
6		693		44855		33067		51186		B
7	B		53382		4391		68344		NM	
8		46		151		21382		58393		B
9	18776		58085		54768		65873		82144	
10		73791		67845		38163		4549		B
11	B		78958		70003		72895		13	
12		20993		86005		75923		95955		B
13			46025		3141		47271			
14				81045		91272		79777		

Pressures (Torr)

	1	2	3	4	5	6	7	8	9	10
1			0.482		0.179		0.100			
2				0.255		2.451		0.116		
3	B		0.184		0.242		0.227		0.077	
4		0.369		0.393		0.623		0.201		B
5	B		0.226		0.296		0.998		0.114	
6		760		0.759		1.251		0.580		B
7	B		0.529		50		0.281		NM	
8		760		760		2.052		0.428		B
9	2.292		0.433		0.499		0.312		0.156	
10		0.223		0.287		1.008		50		B
11	B		0.179		0.261		0.231		760	
12		2.086		0.133		0.203		0.087		B
13			0.722		50		0.685			
14				0.164		0.106		0.173		

(orange)	>5 Torr	(outlined)	Sensor Used for Calibration
B	Sensor not functional		**Bond #105**

Figure 5.15: The thermal impedance measured on gauges across bond #105 (left) and the estimated pressures corresponding to these measurements (right).

This calculated yield is approximately 10% lower than that measured for bond #103. One major difference between these two bonds was the bond ring width of 100 µm as opposed to the bond ring width of 150 µm for bond #105. Another difference between these two bonds involved lithography issues in the patterning of bond rings for bond #105. Figure 5.16 shows bond rings from bond #105 in which Au etchant undercut the photoresist pattern during patterning of the Au bond rings. As illustrated in Figure 5.16a, some bond rings were completely compromised, so that the bond ring was no longer contiguous around the device. As shown in Figure 5.16b, other bond rings were only partially compromised. Even so, there did not seem to be a correlation between bond rings which were partially or even fully compromised and those which did not hold vacuum.

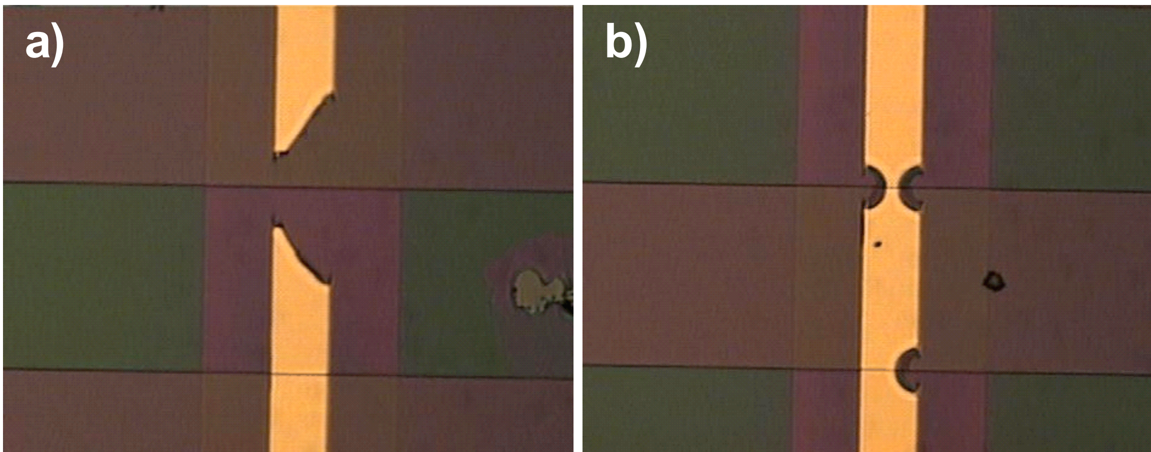


Figure 5.16: a) A bond ring which was completely compromised and b) a bond ring which was partially compromised on the device wafer substrate of bond #105.

5.3.2.3 Long Term Testing for Bonds with Getters but Without an Outgassing Step

Long term testing was conducted on bonds #103 and #105. Figures 5.17 and 5.18 show the pressures measured over time for packages across bonds #103 and #105 which had pressures ranging from 100 mTorr to 2.3 Torr with pressure fluctuations from ±1 to ±25 mTorr over time. For the D3s gauge in the 100 mTorr to 2.3 Torr pressure range, the calculated measurement error was ±4.1 to ±33 mTorr (see Table 4.9 in Chapter 4). This measurement error could account for much or all of the pressure fluctuations in many of the packages. Pressure fluctuations could also result in part from adsorption and

desorption of gases to and from the inside cavities of the package through outgassing as well as through various chemical reactions with the getters.

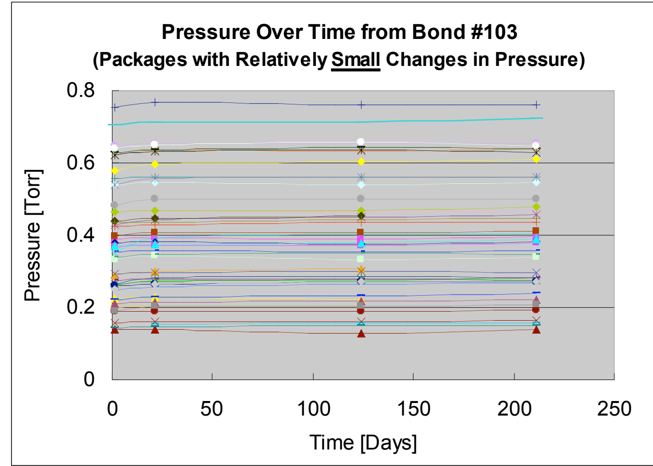


Figure 5.17: Packages from bond #103 which demonstrated changes of pressure from ±1 to ±25mTorr. These pressures were determined from the measured thermal impedances on bond #103 over time using the calibration curves in Figure 5.12.

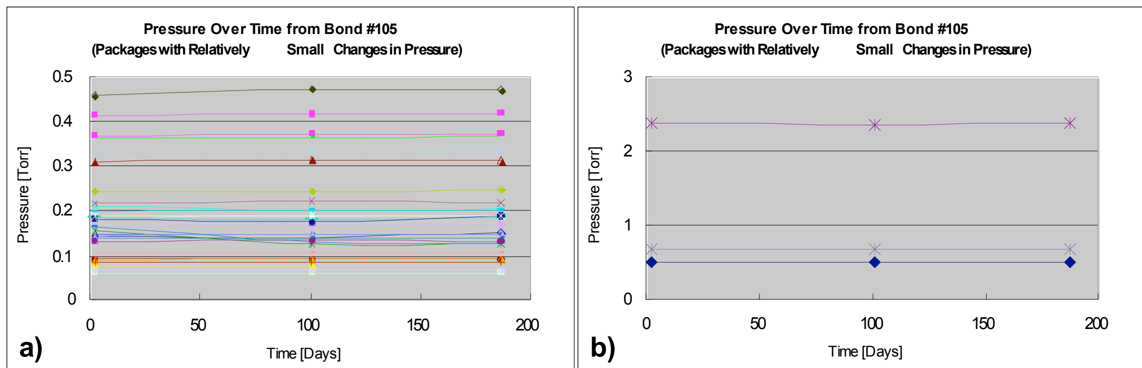


Figure 5.18: Packages from bond #105 which demonstrated changes of pressure from ±1 to ±25mTorr. These pressures were determined from the measured thermal impedances on bond #105 over time using the calibration curves in Figure 5.14.

Figures 5.19 and 5.20 show data for packages from bonds #103 and #105 with >1 Torr of pressure change over time. As illustrated in Figure 5.19, 3 of the 4 packages in bond #103 that demonstrated large changes in pressure went all of the way to atmospheric pressure. The fourth package showed a slow rise in pressure from around 10 Torr to around 30 Torr by the 124th day. As shown in Figure 5.20 on the other hand, there were quite a few more packages with significant pressure fluctuations in bond #105. Figure

5.20a shows two of these packages which appeared to go all of the way to atmospheric pressure and two more that ended up around 30 Torr. Furthermore, Figure 5.20b shows several packages with pressure changes from +0.25 to +1.5 Torr. As mentioned previously, the main difference between bond #103 and #105 were their bond ring widths of 150 and 100 μm respectively and photolithographic issues in the patterning of bond #105 bond rings. Both of these factors may have played a role in the number of packages which showed significant changes in pressure over time.

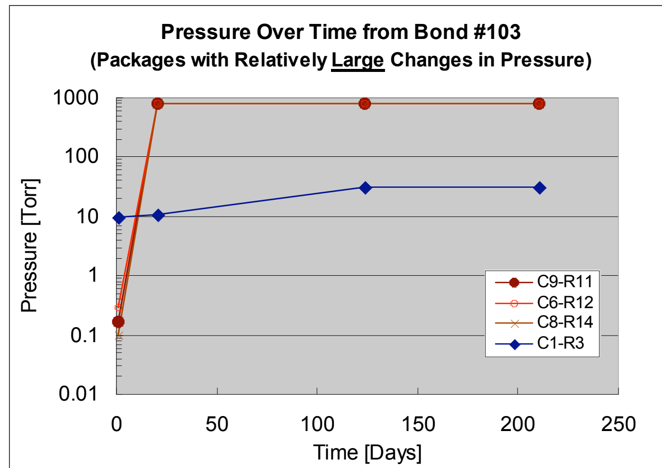


Figure 5.19: Packages with relatively large changes in pressure from bond #103. These pressures were determined from the measured thermal impedances on bond #103 over time using the calibration curves in Figure 5.12.

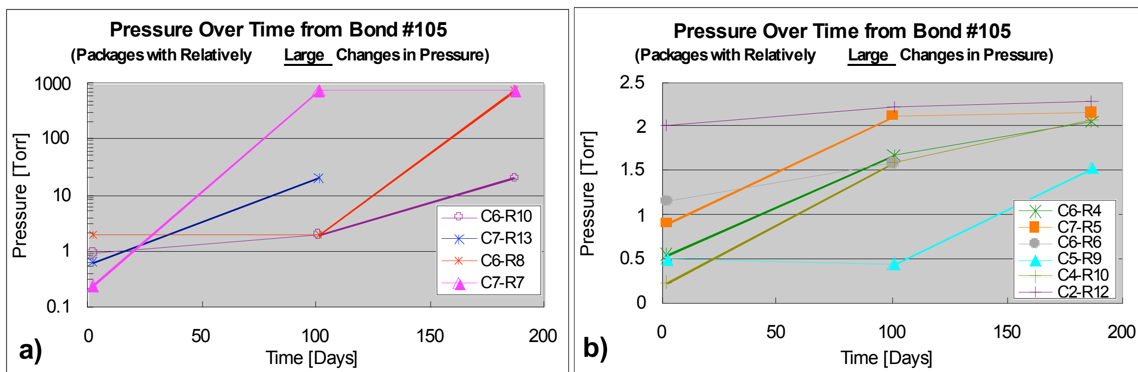


Figure 5.20: Packages with relatively large changes in pressure from bond #105. These pressures were determined from the measured thermal impedances on bond #105 over time using the calibration curves in Figure 5.14.

In summary, for each of the packages in bonds #103 and #105, the measured pressures either remained stable to within ≤±25 mTorr over time, or their was a 1 to 760 Torr increase in pressure in successive measurements. In estimating the yield over time, packages which remained stable to within ±25 mTorr "passed." Packages with pressure increases greater than 1 Torr were determined to have "failed." The failed packages counted against the yield. This given, Figure 5.21 shows the yield over time for bonds #103 and #105. As illustrated, they started with yields of 94.1% and 83% and ended up with yields of 86.8% and 61.5% after around 200 days of testing.

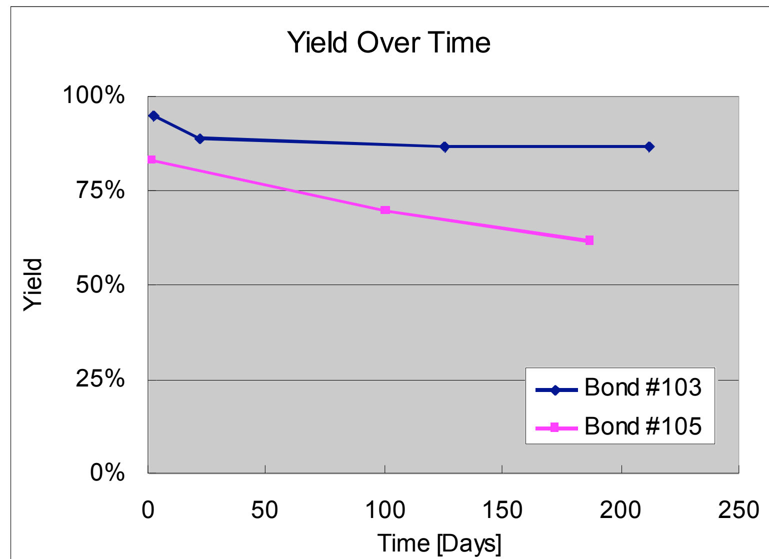


Figure 5.21: The yield over time for bond #103 and #105.

5.3.3 BONDS WITH GETTERS, <25 mTORR PRESSURES

As was shown in Table 5.3 in bonds #71 and #78, getters were used along with a 345ºC, 1 hour long pre-bond outgassing step. Because many of the packages across these wafers demonstrated pressures below 25 mTorr, the linear region of the D3s gauges were used for pressure measurement (see Table 4.9 in Chapter 4). As was discussed Chapter 4, for accurate pressure measurement in the 0 to 50 mTorr pressure range, each individual Pirani gauge needed to be calibrated for package characterization.

5.3.3.1 Analysis of Bond #71

Figure 5.22a shows the calibration curves for the 8 Pirani gauges calibrated across

bond #71 (the specific locations for each of these devices are highlighted in Figure 5.23). These gauges were taken from the wafer after packaging. Figure 5.22b shows the linear portions of calibration curves for each of the gauges in the 0 to 50 mTorr pressure range. Figure 5.23 shows the measured thermal impedances across bond #71. Underneath many of the listed thermal impedances are the pressures determined from the calibration curves. These pressures were determined in three different ways depending on the measured thermal impedance. For packages with thermal impedances from 0 to 5000 K/W, order of magnitude approximations were used to estimate the pressures using the calibration curves in Figure 5.22a. For packages with thermal impedances from 5000 to 23120 K/W the average of the two log-linear curve fits in Figure 5.22a were used. Finally, for packages with pressures from 36882 K/W to 60300 K/W it can be seen from Figure 5.22a that the pressures should *likely* be under 100mTorr. For these packages the linear portion of the calibration curve for each device in Figure 5.22b was used for calibration. (As discussed in Section 4.6.2 (*Pirani Gauge Calibration*), for accurate pressure measurements in this pressure regime, each gauge needed to be calibrated individually after packaging.)

Packages with thermal impedances ranging from 0 to 23120 K/W were determined to have pressures ranging from 760 down to 0.7 Torr. Though many of these packages held vacuum, they were considered outliers and were counted against the yield. For the packages with thermal impedances from 36882 to 60300 K/W, 8 were randomly de-capped and calibrated—as mentioned earlier, these calibration curves are shown in Figure 5.22. As illustrated from Figure 5.23, the calculated pressures for these packages ranged from <3.7 to 16.3 mTorr. (A pressure of 1.9 mTorr was calculated for C8-R10 but because of the measurement error of ±3.7 from Table 4.9 in Chapter 4 the pressure was estimated at <3.7mTorr).

Of the 63 packages tested, 51 demonstrated thermal impedances from 36882 K/W and 60300 K/W. As mentioned above, looking at the graphs in Figure 5.22, these packages were *likely* to have pressures under 100mTorr. Furthermore, all of the 8 packages in which were de-capped and calibrated demonstrated pressures from <3.7 to 16.3 mTorr. Defining “passing” devices as those with pressures *likely* under 100 mTorr, the initial yield was calculated to be 81.0%.

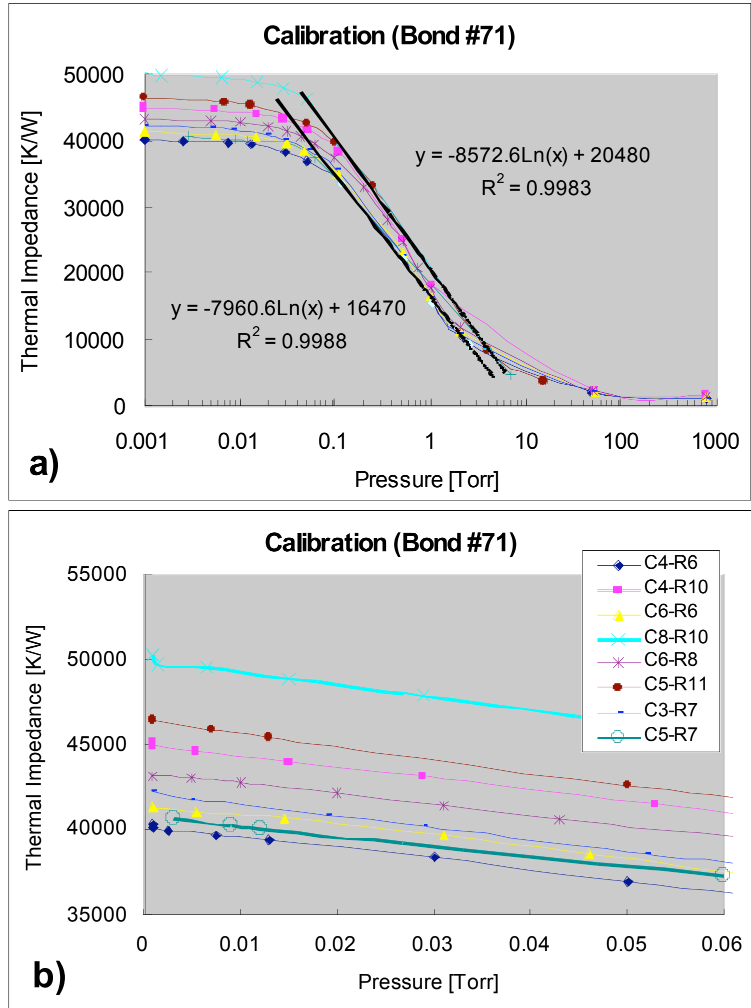


Figure 5.22: Calibration curves for Pirani gauges from D3s gauges from bond #71 showing a) the entire plot on a log-linear plot and b) the linear portion of each of the 8 calibrated Pirani gauges.

Thermal Impedances (K/W) & Pressures

	1	2	3	4	5	6	7	8	9	10
1			36822		43731		53961			
2				37879		8703 (3.9T)		5823 (5.5T)		
3	B		39966		41371		47430		60166	
4		4495 (~10T)		39273		42430		48576		58019
5	3809 (~50T)		39213		40371		45966		4428 (~20T)	
6		39813		39544 (9.9mT)		40904 (6.8mT)		47053		56178
7	40583		41065 (16.3mT)		40369 (9.4mT)		46818		56016	
8		42101		40004		42992 (4.9mT)		46597		23120 (0.7T)
9	41345		42977		43014		48730		8119 (4.2T)	
10		47614		44801 (3.3mT)		45531		50003 (<3.7mT)		633 (760T)
11	59429		49146		45851 (5.9mT)		51429		59590	
12		6920 (4.9T)		49570		49181		53063		60300
13			7635 (4.7T)		1678 (760T)		56469			
14				55702		54764		2118 (760T)		

>100mTorr

Sensor Used for Calibration

B Sensor not functional

Bond #71

Figure 5.23: The thermal impedance measured on gauges across bond #71 and the estimated pressures corresponding to several packages which were de-capped and calibrated.

5.3.3.2 Analysis of Bond #78

Figure 5.24a shows the calibration curves for the 4 Pirani gauges calibrated across the bond #78 (the specific locations for each of these devices are highlighted in Figure 5.25). Figure 5.24b shows the linear portions of the calibration curves for each of the gauges in the 0 to 50 mTorr pressure range. Figure 5.25 shows the measured thermal impedances across bond #78.

Similar to the analysis of bond #71, for packages with thermal impedances from 0 to 5000 K/W the calibration curve in Figure 5.24a was used to make an order of magnitude approximation of the pressure and for thermal impedances from 5000 to 32007 K/W the average of the two log-linear curve fits in Figure 5.24a were used to calculate the packaged pressure. Finally, for packages with pressures from 36882 and 47959 K/W it

can be seen from Figure 5.24a that the pressures should likely be under 100mTorr. For these packages the linear portion of the calibration curve for each device in Figure 5.24b was used for calibration. (Once again, as discussed in Section 4.6.2 (*Pirani Gauge Calibration*), for accurate pressure measurements in this pressure regime, each gauge needed to be calibrated individually after packaging.)

Packages with thermal impedances ranging from 0 to 32007 K/W were determined to have pressures ranging from 760 down to 0.253 Torr. Though many of these packages held vacuum, they were considered outliers and were counted against the yield. For the packages with thermal impedances from 36882 and 47959 K/W, 4 were randomly de-capped and calibrated—as mentioned earlier, these calibration curves are shown in Figure 5.24. In Figure 5.24b the dashed lines show the thermal impedances measured for Pirani gauges in packages C4-R8, C7-R9 and C8-R8. Each of these thermal impedances is slightly higher than that measured during calibration at 2 mTorr. As discussed in Section 4.6.2 (*Pirani Gauge Calibration*), the calibration setup could not be pumped down below around 2 mTorr. The Pirani gauges therefore could not be characterized at lower pressures. Furthermore, from Table 4.9 in Chapter 4 the total measurement error was estimated at ±3.7 mTorr. As result, as shown in Figure 5.25, the thermal impedance is listed as <3.7 mTorr. Package C2-R10 on the other hand had a packaged thermal impedance of 48354 K/W and therefore from the calibration curve, a calculated packaged pressure of 23.3 mTorr.

Of the 47 packages tested, 16 demonstrated thermal impedances from 36882 and 47959 K/W. As mentioned above, looking at the graphs in Figure 5.22, these packages were *likely* to have pressures under 100mTorr. Furthermore, each of the 4 packages which were de-capped and calibrated demonstrated pressures from <3.7 to 23.3 mTorr. Defining "passing" devices as those with pressures *likely* under 100 mTorr, the initial yield was calculated to be 34.0%.

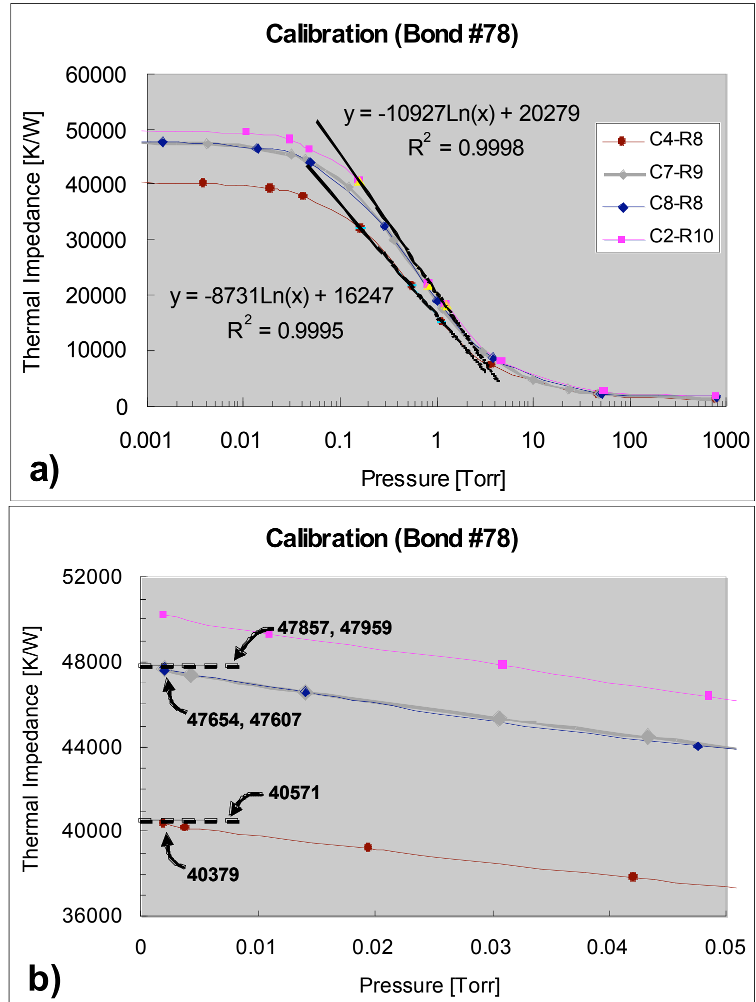


Figure 5.24: Calibration curves for Pirani gauges from D3s gauges from bond #78 showing a) the entire plot on a log-linear plot and b) the linear portion of each of the 4 calibrated Pirani gauges. The dotted lines show the measured thermal impedance while the device was still capped for C4-R8, C7-R9 and C8-R8.

Thermal Impedances (K/W) & Pressures

	1	2	3	4	5	6	7	8	9	10
1			B		B		B			
2				42684		46833		2549 (~40T)		
3	1666 (~760T)		3959 (~15T)		45656		B		1856 (~760T)	
4		B		40461		7863 (2.8T)		2837 (~25T)		3962 (~15T)
5	1547 (~760T)		42594		15322 (1.3T)		B		B	
6		32007 (253mT)		38938		5293 (3.7mT)		47836		2257 (~50T)
7	B		42040		2037 (~60T)		B		B	
8		B		40571 (<3.7mT)		28494 (359mT)		47959 (<3.7mT)		4982 (~5T)
9	1948 (~50T)		45087		43152		47857 (<3.7mT)		B	
10		48354 (23.3mT)		44463		44484		14249 (1.5T)		266 (~760T)
11	636 (~760T)		1161 (~760T)		1520 (~760T)		38526		B	
12		B		1982 (~50T)		47 (~760T)		B		292 (~760T)
13			1894 (~50T)		1023 (~760T)		1859 (~760T)			
14				2185 (~50T)		2097 (~50T)		205 (~760T)		

>100mTorr

Sensor Used for Calibration

Bond #78

B Sensor not functional

Figure 5.25: The thermal impedance measured on gauges across bond #78 and the estimated pressures corresponding to several packages which were de-capped and calibrated.

5.3.3.3 Long Term Testing for Bonds with Getters and With an Outgassing Step

Long term testing was conducted on packages from bond #71. As was discussed previously, for most of the packages across this wafer, packages needed to be de-capped and the Pirani gauge inside needed to be calibrated in order to accurately measure the packaged pressure. Figure 5.26 shows the pressures measured over time for the 8 packages which were de-capped and then calibrated after day 23, 70 and 215 of testing. Figure 5.26a shows the packages which had ±2 mTorr or less variation in pressure over time. Figure 5.26b shows a package where the pressure increased by 35 mTorr on day 215 of testing.

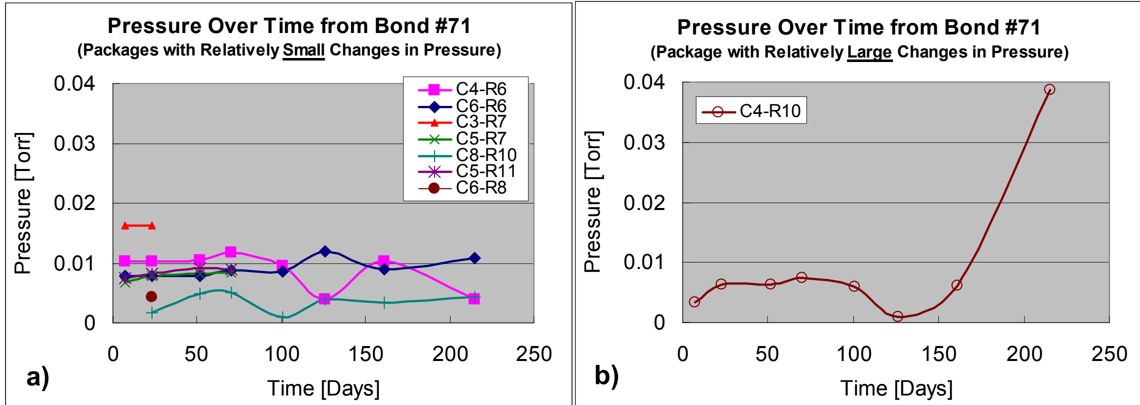


Figure 5.26: Graphs of pressures over time for packages which were individually de-capped and calibrated where Figure 5.22 shows the calibration curves. a) Shows packages with changes in pressure over time of ±2 mTorr or less and b) shows one package in which the pressure increased to around 40 mTorr at the 215 day of testing.

Besides de-capping devices for calibration, many packages were also taken for reliability testing (these reliability tests will be detailed in Section 5.4). Figure 5.27 shows log for day 7, 161, 810 and 1095 for which packages were taken out for de-capping and reliability tests. As can be seen in Figure 5.27, 15 packages total were taken for de-capping even though only 8 were used for calibration. The other seven were damaged during the de-capping process and their calibration curves could not be used. Also shown in Figure 5.27 are the packages which failed over time. Packages with >5 mTorr increase over time were determined to have failed. The methodology for determining whether or not these packages had significant pressure changes is discussed below.

The pressures and the change in pressure over time for un-calibrated packages with pressures *likely* <100 mTorr (the packages with initial thermal impedances from 36882 K/W and 60300 K/W from Section 5.3.3.1) were estimated assuming an initial pressure, P_i, and assuming a thermal impedance vs. pressure slope, S_i. The following equation was then used for estimating the pressure in these packages, P_E:

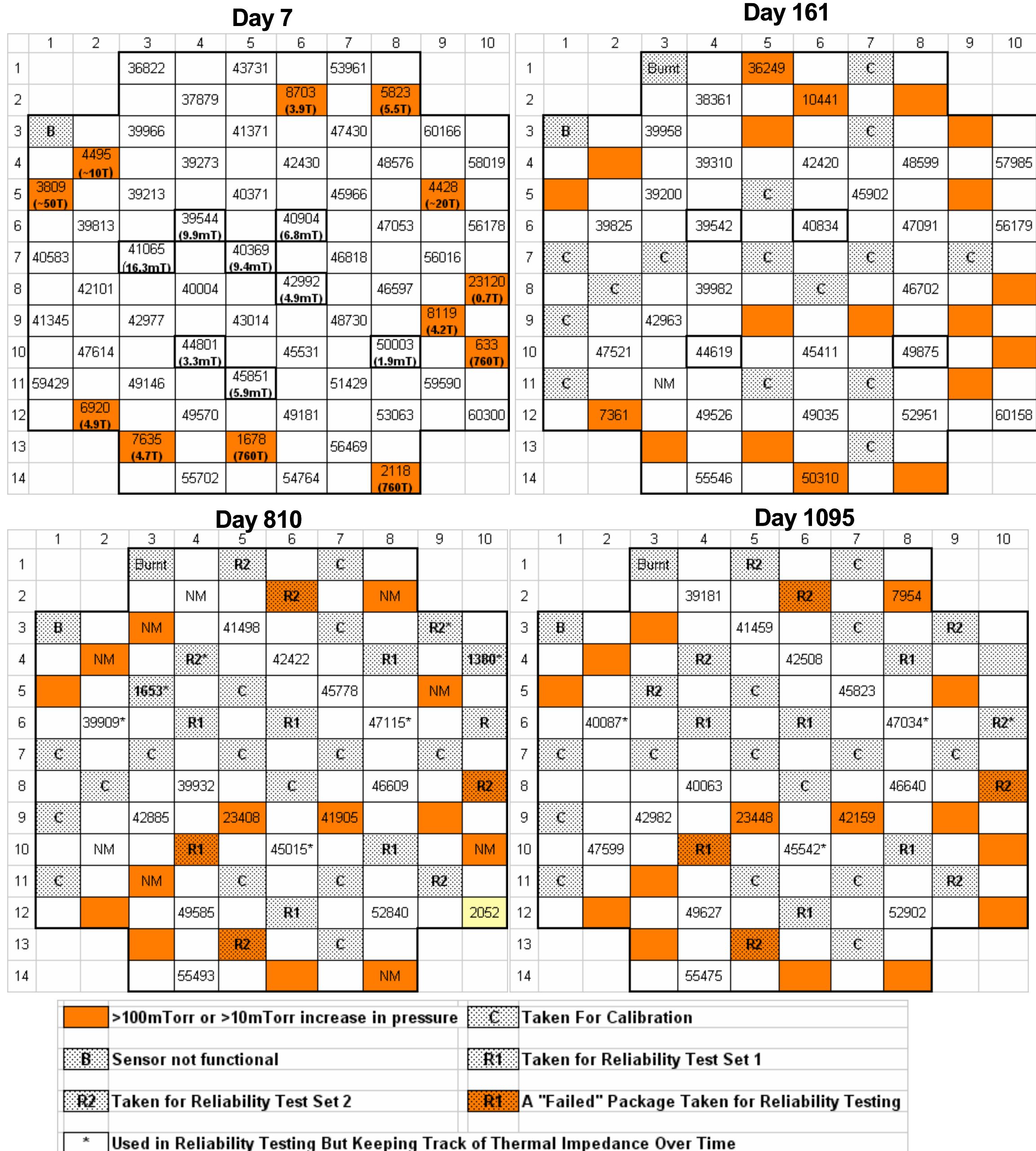
$$P_E = (TI - TI_i) \cdot S_i + P_i \tag{5.7}$$

Where, TI_i was the initial thermal impedance and TI was the thermal impedance at each time after the initial thermal impedance measurement. Looking at Equation 5.7, P_i is the

estimated pressure for the first thermal impedance measurement. Every estimated pressure after that measurement depends on the relative change in thermal impedance, ($TI - TI_i$), times the slope of thermal impedance vs. pressure, S_i.

In Equation 5.7, an initial pressure, P_i, of 7.5 mTorr was chosen because this was the average initial pressure calculated from the 8 packages which were de-capped across bond #71 (Section 5.3.3.1). Similarly, a pressure vs. thermal impedance slope, S_i, of 1.5×10^{-5} Torr·W/K was assumed since this was the average slope of the calibration curves taken from bond #71 (see Figure 6.24b in Section 5.3.3.1). These values were used in the following equation for estimating package pressure:

$$P_E = (TI - TI_i)\cdot 1.5\times10^{-5} + 0.0075 \qquad (5.8)$$



Day 7

	1	2	3	4	5	6	7	8	9	10
1			36822		43731		53961			
2				37879		8703 (3.9T)		5823 (5.5T)		
3	B		39966		41371		47430		60166	
4		4495 (~10T)		39273		42430		48576		58019
5	3809 (~50T)		39213		40371		45966		4428 (~20T)	
6		39813		39544 (9.9mT)		40904 (6.8mT)		47053		56178
7	40583		41065 (16.3mT)		40369 (9.4mT)		46818		56016	
8		42101		40004		42992 (4.9mT)		46597		23120 (0.7T)
9	41345		42977		43014		48730		8119 (4.2T)	
10		47614		44801 (3.3mT)		45531		50003 (1.9mT)		633 (760T)
11	59429		49146		45851 (5.9mT)		51429		59590	
12		6920 (4.9T)		49570		49181		53063		60300
13			7635 (4.7T)		1678 (760T)		56469			
14				55702		54764		2118 (760T)		

Day 161

	1	2	3	4	5	6	7	8	9	10
1			Burnt		36249		C			
2				38361		10441				
3	B		39958				C			
4				39310		42420		48599		57985
5			39200		C		45902			
6		39825		39542		40834		47091		56179
7	C		C		C		C		C	
8		C		39982		C		46702		
9	C		42963							
10		47521		44619		45411		49875		
11	C		NM		C		C			
12		7361		49526		49035		52951		60158
13							C			
14				55546		50310				

Day 810

	1	2	3	4	5	6	7	8	9	10
1			Burnt		R2		C			
2				NM		R2		NM		
3	B		NM		41498		C		R2*	
4		NM		R2*		42422		R1		1380*
5			1653*		C		45778		NM	
6		39909*		R1		R1		47115*		R
7	C		C		C		C		C	
8		C		39932		C		46609		R2
9	C		42885		23408		41905			
10		NM		R1		45015*		R1		NM
11	C		NM		C		C		R2	
12				49585		R1		52840		2052
13					R2		C			
14				55493				NM		

Day 1095

	1	2	3	4	5	6	7	8	9	10
1			Burnt		R2		C			
2				39181		R2		7954		
3	B				41459		C		R2	
4				R2		42508		R1		
5			R2		C		45823			
6		40087*		R1		R1		47034*		R2*
7	C		C		C		C		C	
8				40063		C		46640		R2
9	C		42982		23448		42159			
10		47599		R1		45542*		R1		
11	C				C		C		R2	
12				49627		R1		52902		
13					R2		C			
14				55475						

(orange)	>100mTorr or >10mTorr increase in pressure	C	Taken For Calibration
B	Sensor not functional	R1	Taken for Reliability Test Set 1
R2	Taken for Reliability Test Set 2	R1 (orange)	A "Failed" Package Taken for Reliability Testing
*	Used in Reliability Testing But Keeping Track of Thermal Impedance Over Time		

Figure 5.27: A snap shot of the log for the testing of packages from bond #71 over time on day 7, 161, 810 and 1095. The legend at the bottom of the figure shows which packages failed over time (increased by >5mTorr), which packages were taken for calibration and which packages where taken for reliability testing.

Using Equation 5.8 for estimating the pressure and the pressure change over time, Figure 6.31 shows 11 packages which maintained pressures to within ±5 mTorr over 3 years of long term testing. The total measurement error for the D3s gauges in the 0 to 50 mTorr range was approximately ±3.7 mTorr (see Table 4.9 in Chapter 4). This

measurement error could account for much or all of the pressure fluctuations in many of these gauges. Pressure fluctuations could also have resulted from adsorption and desorption of gases to and from the inside cavities of the package through outgassing as well as through various chemical reactions with the getters.

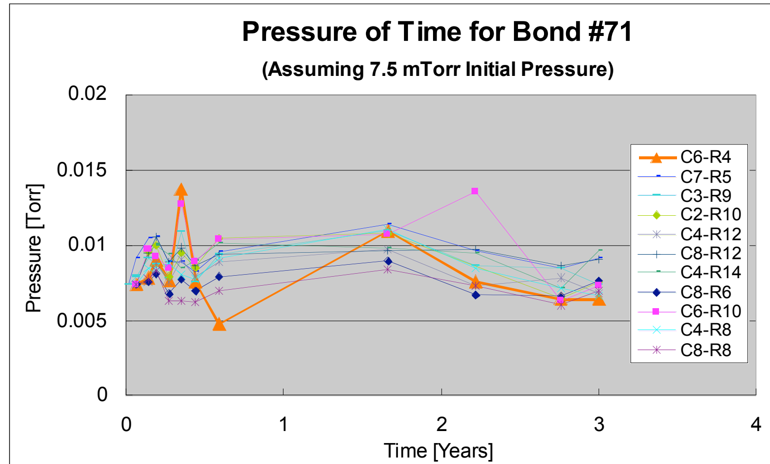


Figure 5.28: The estimated pressure over time for 11 packages which maintained pressures to with in ±5 mTorr over 3 years of testing.

Figure 5.29 shows 7 packages where there was a significant increase in pressure over time. The packages in Figure 5.29a demonstrated pressure increases ranging from 29 to 77 mTorr. These relatively small changes in pressure over a relatively large amount of time are likely from outgassing. The packages in Figure 5.29b showed increases in pressure all of the way to atmospheric pressure. These changes in pressure could have been either from outgassing overtime or from a sudden catastrophic physical leak. Figure 5.30 shows 5 packages which had an initial increase in pressure and then a subsequent pressure reduction. These packages appeared to experience some outgassing over time followed by gettering (or chemisorption of atoms in to the getter). As will be reported in the reliability tests in Section 5.4 (*High Temperature Exposure, Thermal Cycling and Burn In*), similar phenomena was observed with exposure to high temperatures.

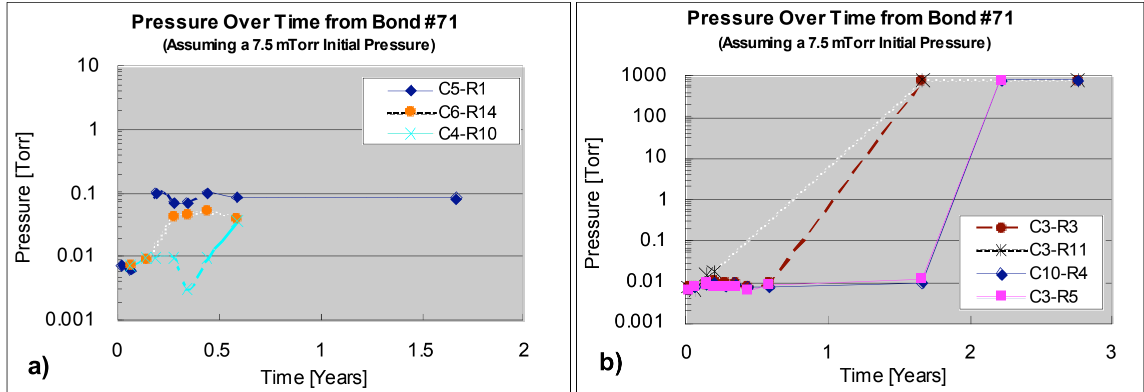


Figure 5.29: The estimated pressure over time for 7 packages which had significant changes in pressure over time.

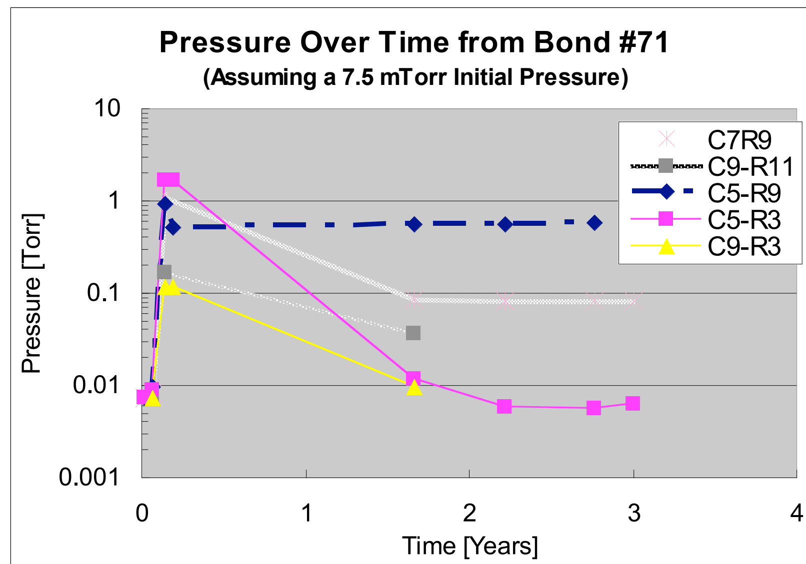


Figure 5.30: The estimated pressure over time for 5 packages which had an initial increase then decrease in pressure.

For each of the packages in bond #71 that had estimated pressures of <100 mTorr, the measured pressures either remained stable to within ±5 mTorr over time, or there was a 29mTorr to 760 Torr increase in pressure overtime. In estimating the overall yield, packages which maintained pressures within ±5 mTorr were determined to have "passed," where as packages with greater than 29 mTorr of pressure increase were determined to have "failed." These "failed" packages were counted against the yield. Since quite a few packages were removed over time for de-capping and for reliability tests the yield could not simply be calculated by the total number of "passing" devices

divided by the total number of devices tested. This is because the un-tested devices (those which were taken out for de-capping or reliability tests) were packages which could have potentially failed over time. Therefore, to estimate the yield over time the following equation was used:

$$Y_n = Y_{n-1} - \frac{\#Failed}{\#Tested} \tag{5.9}$$

where Y_n was the current measurement, Y_{n-1} was the yield in the previous measurement, *#Failed* was the number of packages which failed *in that set of measurements* and *#Tested* was the number of devices *still available for testing*. In this way, the % failure rate was subtracted from the previous yield. This given, Figure 5.31 shows the yield over time for bond #71. As illustrated, there is initially a sharp drop that leveled off after around 7 months.

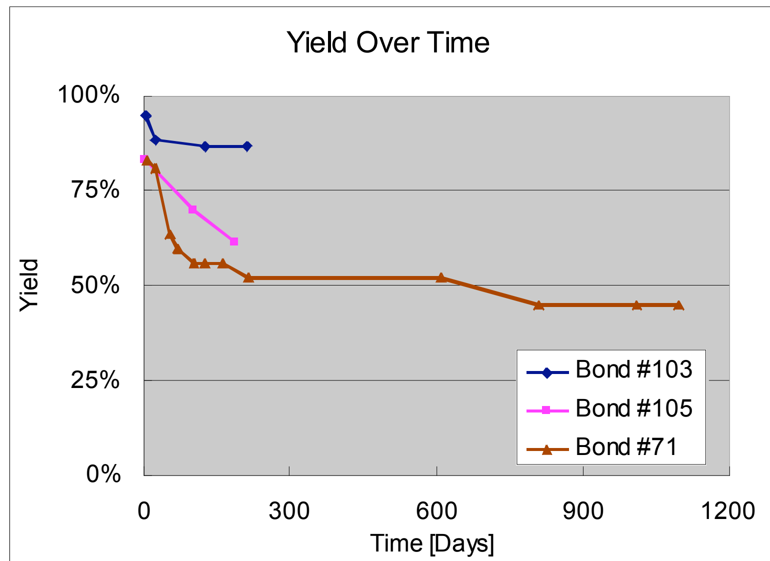


Figure 5.31: The yield over time for bond #71.

5.4 High Temperature Exposure, Thermal Cycling and Burn In

This section reports test results on packages exposed to elevated temperatures, reduced temperatures and thermal cycling. The main objective of these experiments was to better understand how the vacuum pressure changed under harsh conditions. Five packages from bond #71 were first transported from Ann Arbor, Michigan to Albuquerque, New

Mexico in order to conduct tests at Sandia National Laboratories (SNL). This transport included a 40 minute car ride which exposed devices to 40ºC temperatures, low frequency vibration and high humidity. After transport and testing, these devices were de-capped and calibrated. The following sections describe the measured pressure variation after transporting the devices to Sandia Nation Laboratories (Section 5.4.1.1), after temperature ramping experiments (Section 5.4.1.2) and thermal cycling (Section 5.4.1.3). Finally, Section 5.4.1.4 summarizes these results.

5.4.1.1 Pressures after Transit

As shown in Figure 5.32, after transit, on days 272 through 288 (in Albuquerque, New Mexico), pressures increased from 1.3 to 5.2 Torr on *all* five packages. In packages C4-R10, C6-R6 and C8-R10 this initial pressure increase was followed by a subsequent decrease in pressure to near their original values of 16.3 mTorr, 4.4 mTorr and 1.9 mTorr respectively.

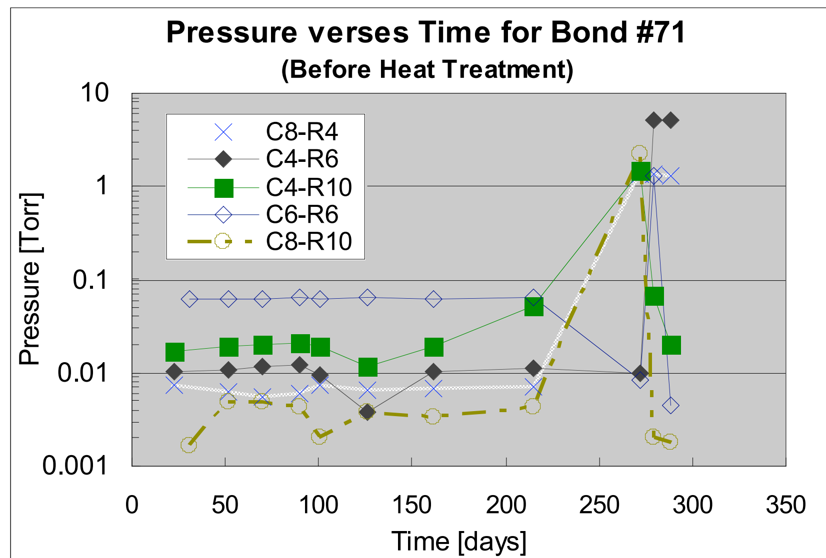


Figure 5.32: Five packages which were taken out of the controlled environment (after 215 days). Large pressure fluctuations were observed.

5.4.1.2 Temperature Ramping Experiments

Next, these 5 devices were put through temperature ramping tests inside of a Tenney Temperature Benchtop oven/refrigeration system. A schematic of the test setup is shown

in Figure 5.33. Individual packages were mounted and wire bonded to dual-in-line packages (DIPs). During testing, these DIPs were plugged into a high temperature PC board which sat inside of the oven (shown schematically in Figure 5.33). Leads from the PC board ran to a switch box, which allowed for individual testing of each of the 5 vacuum packages. Vacuum pressures were determined using a computer controlled program to direct currents across the Pirani gauges while measuring the voltage drop across them. From this data, the thermal impedances were measured.

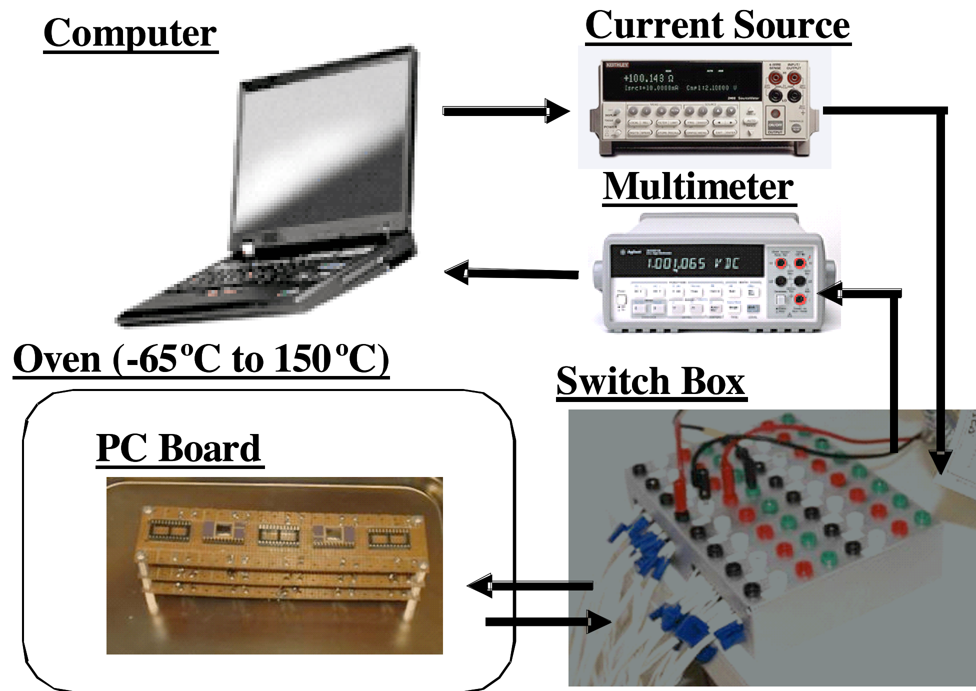


Figure 5.33: Packaged vacuum sensors were tested inside of an oven using a Labview program, a current source, a multimeter and a switch box to test each sensor during and ever ramping cycles.

Table 5.4 shows the temperatures that the 5 packages were held at for the temperature ramping experiments. As shown, in steps #1-#4, temperatures were first raised to 50, 75, 100 and 125°C and held for 2 hours. Next, in step #5, they were held at 150°C for 100 hours and then brought back down to room temperature in step #6. In steps #7 and #8, the packages where held at 0 and -25ºC for 2 hours. Finally the packages where held at -65°C for 6 hours.

Table 5.4: The times at each temperature at which gauges at which packages were held at for the high/low temperature exposure tests.

Step	Temperature	Exposure Time
0	23°C (Room Temperature)	-
1	50°C	2 hours
2	75°C	2 hours
3	100°C	2 hour
4	125°C	2 hours
5	150°C	100 hours
6	22°C (Room Temperature)	1 hours
7	0°C	2 hours
8	-25°C	2 hours
9	-65°C	6 hours

Figure 5.34 shows the results of the temperature ramping experiments for the 5 packages. It is important to note that Figure 5.34 shows the thermal impedances at each temperature step, not the pressure. The thermal impedances are graphed because the measured thermal impedance has a strong dependence on the ambient temperature—the elevated temperatures therefore make the thermal impedance vs. pressure calibration curves (from Section 5.3.3.1) inaccurate.

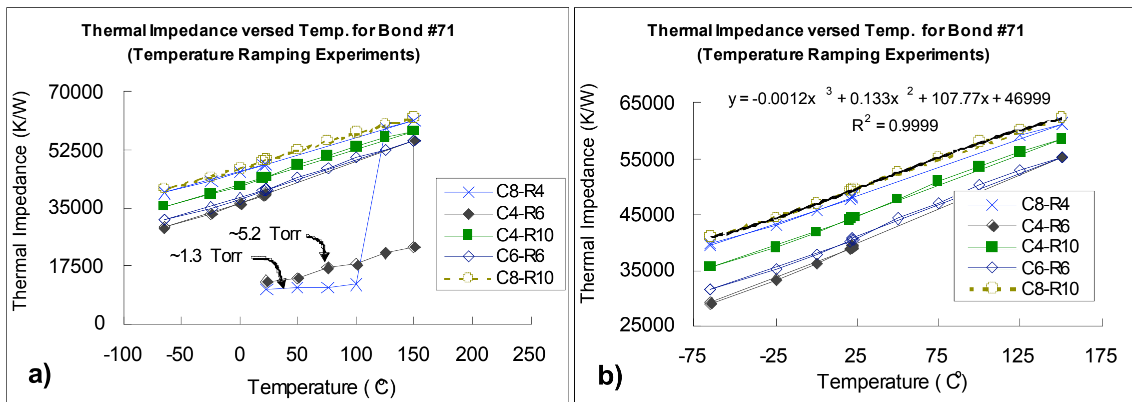


Figure 5.34: Thermal Impedance vs. temperature for the 5 packages taken through high/low temperature exposure tests. a) Shows a plot of each data point in the temperature ramping and b) shows a plot without the initial data points for C8-R4 and C4-R6.

As was shown in Figure 5.32 and discussed above, packages C4-R10, C6-R6 and C8-R10 returned to near their original packaged pressures before beginning the temperature ramping experiments. This corresponds to thermal impedances in Figure 5.34 of 43347,

40344 and 49169 K/W at 23ºC (room temperature). At the beginning of the temperature ramping experiments, packages C8-R4 and C4-R6 had pressures of 1.3 and 5.2 Torr, which corresponds to thermal impedances in Figure 5.34a of 10410 and 12835 K/W. As illustrated, in Figure 5.34a, between the 100 and 125ºC temperature steps, package C8-R4 had a large increase in thermal impedance (and therefore decrease in pressure). Package C4-R6 held a relatively low thermal impedance until it was held at 150ºC (step 5) for 23 hours. At 23 hours, there was a similar large increase in thermal impedance. Figure 5.34b shows this same thermal impedance vs. temperature graphs but without the data for the first 4 and first 6 temperature steps for packages C8-R4 and C4-R6. All of the packages in Figure 5.34b show a consistent trend. As illustrated, a 3rd order polynomial is curve fitted to package C8-R10 with a root mean squared (R-squared) value of 0.9999. The other 4 packages also demonstrated 0.9999 R-squared values in 3rd order polynomial curve fits.

The temperature sensitivity of these Pirani gauges could be estimated from the slopes of the 3rd order polynomials at room temperature. Table 5.5 shows the slope of thermal impedance vs. temperature (TI/ºC) for each Pirani gauge. Using the calibration curves for each gauge, the slope of pressure vs. temperature (mTorr/ºC) could then be calculated as shown in Table 6.4. This data was used in Section 4.6.3.3 (*Error Due to Temperature Fluctuation*) for the estimation of the temperature sensitivity of the D3s Pirani gauges below 50 mTorr. More detailed calculations and discussion were presented in Section 4.6.3.3.

Table 5.5: Slopes of thermal impedance and mTorr vs. the change in temperature.

Step	Thermal Impedance/ºC	mTorr/ºC
C8-R4	102.9	1.33
C4-R6	122.9	1.93
C4-R10	109.4	1.64
C6-R6	113.9	1.93
C8-R10	101.8	1.33
Average:	**110.6**	**1.63**

5.4.1.3 Thermal Cycling Tests

After the temperature exposure tests the packages where thermal cycled from -65 to 150°C for 50 thermal cycles. These tests were done in accordance with MIL-SPEC-883F Method 1010.8, test condition C for thermal cycling. The calculated pressures after thermal cycling tests did not change by more than ±2 mTorr.

5.4.1.4 Summary of Tests Conducted at Sandia National Laboratory

Figure 5.35 shows a summary of the heat treatment results. As shown, the pressures for all of the packages tested stabilized either before or during the 150ºC 100 hour temperature exposure. Even after exposure to -65ºC for 7.5 hours and 50 thermal cycles from -65 to 150°C, the measured packaged pressures remained stable to within ± 2mTorr. Though this data is not conclusive, these experiments may indicate the need for a "burn in" step where packages are initially exposed to an elevated temperature in order to stabilize the pressures inside of the package.

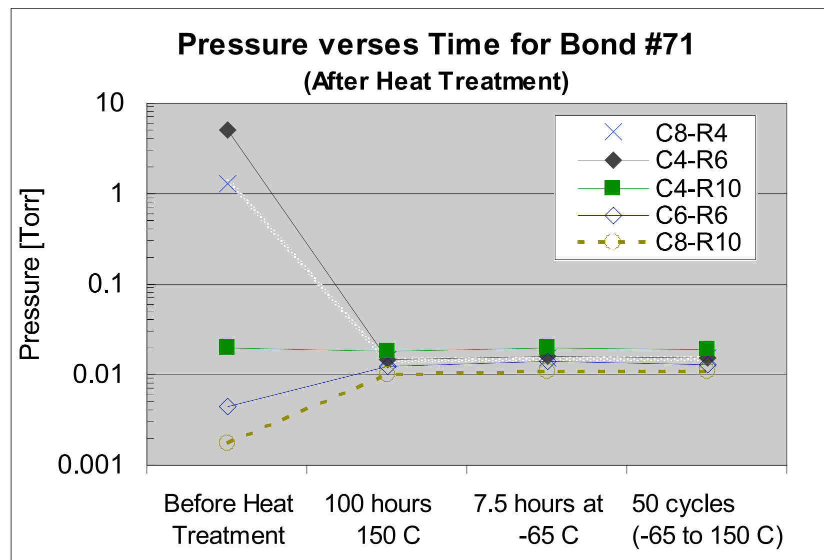


Figure 5.35: A summary of the results through various heat treatment steps.

5.5 SUMMARY OF VACUUM TESTING RESULTS

There were several significant results reported in this chapter regarding i) the package pressure, ii) the initial yield, iii) the pressure stability over time and iv) heat treatment and

burn-in.

Package Pressure

The minimum pressures achieved depended on whether or not a getter was used and whether or not an outgassing step was used. As summarized in Table 5.6: i) pressures of greater than 1 Torr were observed for bonds conducted *without* getters, ii) pressures between 100mTorr and 2.4 Torr were observed for bonds conducted *with* getters but *without* the 60 minute outgassing step, and iii) pressures below 25mTorr were observed for bonds *with* getters and *with* the 60 minute outgassing step.

Table 5.6: A summary of the different pressures measured with/without getters and with/without an outgassing step.

Bond	Location of Data	Getters	Outgassing Step	Pressure Ranges
#67	Section 5.3.1.1	No	No	1.6-11.8 Torr
#100	Section 5.3.1.2	No	Yes	2.4-43.5 Torr
#103, #105	Section 5.3.2	Yes	No	77-2400 mTorr
#71, #78	Section 5.3.3	Yes	Yes	<2-23.3 mTorr

Initial Yield

The yield across each wafer was estimated in order to quantify the bond quality. The initial yield was defined by the package's ability to hold vacuum and there were different standards depending on the pressure ranges which were achieved across the bond. As a metric, packages with pressures greater than 3 standard deviations outside of the mean were determined to have "failed." These packages were counted against the yield. Table 5.7 shows the yields for 5 wafers discussed earlier in this chapter. As shown, bonds #78 and #100 had the lowest initial yields at 30.4%, 80.4% and 81%. In all of these bonds the hot plate method was used for device release (Section 3.3.1 of Chapter 3).

Appendix 4 discusses how this residue seems to reduce bond uniformity depending on the amount of residue observed.

For bonds #105 and #103 on the other hand, initial yields of 84.6% and 94.1% were observed. In all of these bonds, critical point drying (CPD) was used for device release (see Section 3.3.2 of Chapter 3). As discussed

Appendix 4, a visibly "cleaner" bonding surface resulted using CPD once the process

had been refined. These higher yields were achieved despite the fact that bond ring widths of 100 and 150μm were used. The initial yield in bond #105 in fact could likely have been reduced also by issues with the patterning of the bond ring as described in Section 5.3.2.2.

Table 5.7: A summary of the different pressures measured with/without getters and with/without an outgassing step.

Bond	Location of Data	Bond Ring Width	Release Method	Pressure Range	Yield
#78	Section 5.3.3.2	300 μm	Hot Plate	<2-23.3 mTorr	30.4%
#100	Section 5.3.1.2	300 μm	Hot Plate	2.4-43.5 Torr	80.4%
#71	Section 5.3.3.1	300 μm	Hot Plate	2-16 mTorr	81.0%
#105	Section 5.3.2.2	100 μm	CPD	77-2400 mTorr	84.6%
#103	Section 5.3.2.1	150 μm	CPD	100-500mTorr	94.1%

Pressure Stability over Time

In each of the three bonds in which pressures were monitored over time, a certain number of packages from each wafer had a significant increase in pressure. These increases in pressure ranged from +29 mTorr to +760 Torr in bond #71 and from +1 Torr to +760 Torr in bonds #105 and #103. In each of these bonds, package pressures in some cases rose slowly over time (likely caused by outgassing) and in other cases they seemed to go straight to atmospheric pressure (which could be the result of outgassing or a sudden catastrophic physical leak). Several packages from bond #71 also demonstrated fluctuations in pressure in which there was an initial increase but subsequent decrease in pressure. Such behavior could be caused by outgassing followed by chemisorption of molecules into the getter. As summarized in Table 5.8 the packages which were defined as stable did not vary in pressure by more than ±5 or ±25 mTorr respectively. Table 5.8 and Figure 5.36 compare how the yield over time for these three bonds decreased.

As shown, in the first 6 months of testing, bonds #71 and #105 both had a significant drop in yield. As discussed above, these yield losses could likely be due to residue left from the release process and patterning of the bond ring respectively for these two bonds. In bond #103 on the other hand, there was a small initial yield loss which appeared to level off after 4 months of testing.

Table 5.8: A summary of the different pressures measured with/without getters and with/without an outgassing step.

Bond	Location of Data	Measured Pressure Fluctuation for "Stable Package"	Yield after 6 months
#71	Section 5.3.3.3	<±5 mTorr	52.1%
#105	Section 5.3.2.3	<±25 mTorr	84.6%
#103	Section 5.3.2.3	<±25 mTorr	86.8%

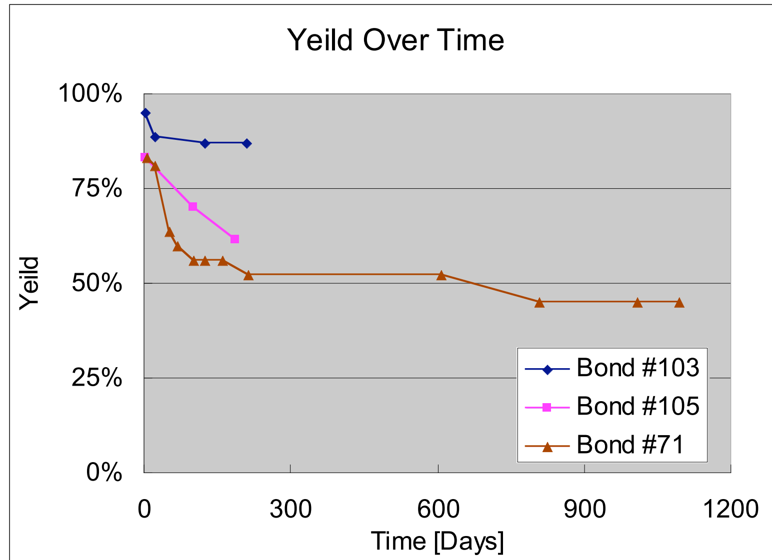


Figure 5.36: A summary of the yields over time for bonds #103, #105 and #71.

Heat Treatment and Burn-In

The reduced yields in Figure 5.36 over time can potentially be a big problem in the application of Au-Si eutectic wafer-level packaging to commercial products where such yield loss over time would not be acceptable. In Section 5.4, a number of packages experienced pressure increases of 1.3 to 5.2 Torr after a 23 hour car ride. After heat treatment at 150ºC for 23 hours, the pressures in these packages remained stable for the remaining 77 hours at 150ºC and through 50 thermal cycles from -65ºC to 150 ºC. Although this data was not conclusive, these test results seem to indicate that a "burn-in" step could be applied for stabilizing packaged pressures. Furthermore, such a burn-in step could be used to more quickly cause packages to fail—thus avoiding package and subsequent device failures in the field.

CHAPTER 6

DIFFERENTIAL LOCALIZED HEATING

Most of the wafer-level encapsulation techniques discussed in Chapter 1 require relatively high temperatures for their implementation. The most widely applicable methods for such encapsulation include frit bonding (≥450ºC), Au-Si eutectic bonding (~390ºC), and thin film encapsulation (≥600ºC). Many emerging applications, including MEMS biomedical devices and RF micro-switches, incorporate materials such as polymers, biological coatings, metals and piezoelectric materials that cannot withstand these temperatures. For this reason, researchers have investigated bonding methods using polymers and low temperature solders. Another option is to use a well established high temperature bonding method and use localized heating to heat the bond region to a relatively high temperature while maintaining a relatively low temperature where devices are located. Section 1.3.3 of Chapter 1 explained some of these localized heating methods. As explained there, most of these methods are difficult to implement at the wafer level and none have directly measured the temperatures of encapsulated devices in order to explicitly gauge the effectiveness of their localized heating techniques.

This chapter presents a new wafer-level localized heating approach called *differential localized heating*. Figure 6.1 shows the concept for *differential localized heating* where heat is applied on the backside of the cap wafer and then gets pulled through a bond ring towards a heat sink and away from the device. In this way, large bond ring temperatures can be achieved while maintaining a relatively low temperatures at the device location.

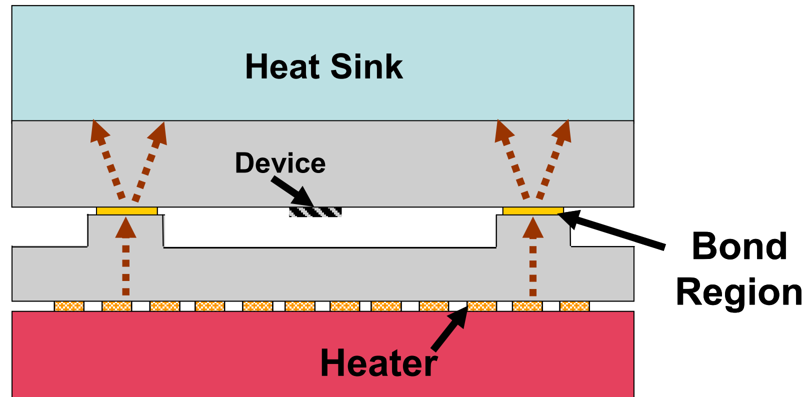
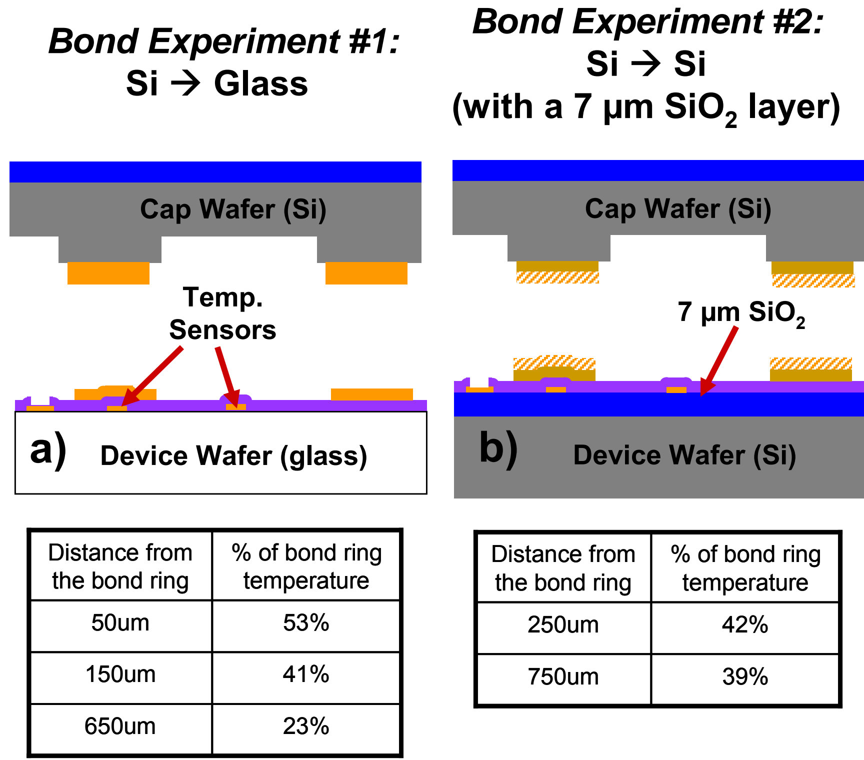


Figure 6.1: A schematic illustrating the concept behind *differential localized heating* where heat gets pulled through the bond rings towards the heat sink, heating up the bond ring while keeping the device relatively cool.

Figure 6.2 shows the bond experiments that are presented in this chapter which include: i) a bonds between a Si and glass wafer (*bond experiment #1*) and ii) a bond between a Si wafer and a Si wafer with a 7µm thick SiO_2 layer (*bond experiment #2*). These material sets were chosen specifically so that there was a low thermal conductivity near the bond ring on the device wafer—as will be discussed, this was an important parameter for achieving good thermal isolation inside of the bond ring. For bond experiment #2, the 7 µm thick SiO_2 layer was chosen to roughly mimic the various thin films in a CMOS process. For example, Sandia National Laboratory's SUMMIT V^{TM} process, shown in Figure 3.2 of Chapter 3, has 6.5 µm of SiO_2, 0.8 µm of SiN_x, and 6.25 µm of poly-Si.



Distance from the bond ring	% of bond ring temperature
50um	53%
150um	41%
650um	23%

Distance from the bond ring	% of bond ring temperature
250um	42%
750um	39%

Figure 6.2: A schematic of the bond experiments conducted in this chapter along with the measured temperatures relative to the bond ring temperatures for each of these bond experiments.

As shown in Figure 6.2, temperature sensors were also fabricated underneath the bond ring and at different distances from the bond ring in order to quantify the effectiveness of this localized heating technique. As shown in the tables directly under each schematic in Figure 6.2, in each of the bond experiments, a reasonable amount of thermal isolation was achieved inside of the bond ring. In fact, the temperature was observed to be 23% of the minimum bond ring temperature at 650 μm from the bond ring in bond experiment #1, and to be 41% of the minimum bond ring temperature at 250 μm from the bond ring in experiment #2.

The rest of this chapter provides a more in depth discussion of the test setup, the modeling results and the test results. More specifically, Section 6.1 presents the modeling results which helped in choosing the materials and the dimensions used in the bonding experiments. Section 6.2 describes the fabrication process for the wafers used in the bond experiments and Section 6.3 presents the bonder setup used for the bond experiments. Section 6.4 explains the bond experiment results and Section 6.5

summarizes the modeling and bond experiment results. Finally, Section 6.6 presents some parametric analysis which will aid in the application of this work in the future and analysis on residual stress induced from this bonding technique.

6.1 Modeling & Analysis

This section presents some key concepts in the thermal design and choice of materials for the implementation of *differential localized heating*. ANSYS® multiphysics analysis software was also used to help determine the materials and geometries used for bond experiments. Section 6.1.1 first explains some key concepts for the choice of the materials and geometries used in wafer bonding experiments and Section 6.1.2 presents a 1-D circuit analogy describing the wafer bonding test setup. Section 6.1.3 then presents the modeling results for several different material combination using the materials and geometries of the test setup described which will be described later (in Section 6.3). Finally, Section 6.1.4 presents summarizes these results and presents data which will later be used for comparison to the test results.

6.1.1 MATERIALS AND THERMAL DESIGN

Figure 6.3 shows the structure of the test setup that will be presented in Section 6.3. The models presented in the following sections use the same materials and dimensions as those in the test setup. As shown in Figure 6.3, the test setup and the model consist of the following substrates: i) a thermally insulating Cogetherm^{TM} plate (10.5 mm thick), ii) a glass heater substrate with on-chip resistive heaters (550µm thick), iii) a silicon cap wafer (550µm), iv) a device wafer (modeled as either silicon or glass, 550µm thick), v) a copper plate heat sink substrate on top of the device wafer (3.1 mm thick), and vi) a steel weight providing the bond force (modeled as 14 mm thick). In each of these models, 100 µm wide bond rings that encompassed 2.3x2.3mm^2 areas were used. (These are the same dimensions as some of the bond experiments reported in Chapter 2 and Chapter 5). Furthermore, 90 µm cavities inside of the bond rings were also modeled.

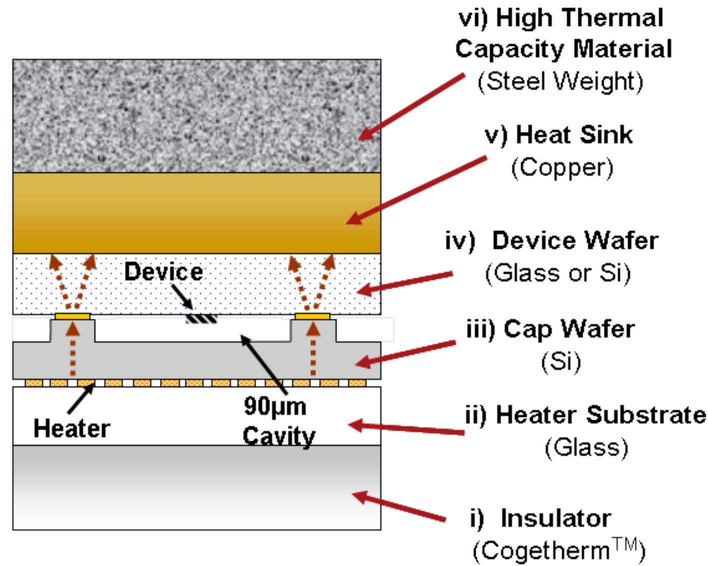


Figure 6.3: Shows the layers in the test setup which will be described in Section 6.3.

Table 6.1 shows the thermal conductivities of the various materials used in modeling the test setup. Cogetherm™ (i) is a composite that was chosen because of its low thermal conductivity in particular in the z-axis (the direction that the heat flows in Figure 6.3). Glass (ii) was also chosen for its low thermal conductivity. These materials have thermal conductivities in the vertical to the plane axis of 0.3 $W{\cdot}m^{-1}{\cdot}{}^{o}C^{-1}$ and 1.4 $W{\cdot}m^{-1}{\cdot}{}^{o}C^{-1}$ respectively. The single crystal Si (iii), on the other side of the heater, on the other hand has a thermal conductivity of around 141 $W{\cdot}m^{-1}{\cdot}{}^{o}C^{-1}$—this relatively high thermal conductivity allowed a larger percentage of the heat to go up towards the bond rings instead of down towards the glass and Cogetherm™ plate. In Figure 6.3, the heat gets pulled through the cap and device wafer towards the copper heat sink. Copper was chosen because of its exceptionally high thermal conductivity of 385 $W{\cdot}m^{-1}{\cdot}{}^{o}C^{-1}$ which encouraged heat conduction away from the device wafer. Though the steel weight only had a moderately high thermal conductivity of 55 $W{\cdot}m^{-1}{\cdot}{}^{o}C^{-1}$, it provided a very large thermal mass.

Table 6.1: The thermal conductivities for the various materials used in the model of the test setup.

	Materials	Thickness	Thermal Conductivity
vi)	Steel	14 mm	55 $W \cdot m^{-1} \cdot {}^oC^{-1}$
v)	Copper	3.1 mm	385 $W \cdot m^{-1} \cdot {}^oC^{-1}$
iv)	Glass	550 μm	1.4 $W \cdot m^{-1} \cdot {}^oC^{-1}$
	Single Crystal Si	550 μm	141 $W \cdot m^{-1} \cdot {}^oC^{-1}$
	SiO_2	7 μm	1.4 $W \cdot m^{-1} \cdot {}^oC^{-1}$
iii)	Single Crystal Si	550 μm	141 $W \cdot m^{-1} \cdot {}^oC^{-1}$
	Air	90 μm	0.0263 $W \cdot m^{-1} \cdot {}^oC^{-1}$
ii)	Au (heater)	0.75 μm	320 $W \cdot m^{-1} \cdot {}^oC^{-1}$
	Glass	550 μm	1.4 $W \cdot m^{-1} \cdot {}^oC^{-1}$
i)	Cogetherm™	10.5 mm	3 $W \cdot m^{-1} \cdot {}^oC^{-1}$ (0.3 in z direction)

Because of the large thermal mass of the steel block, long heating times and high input powers were required to raise the temperature. To estimate the heating rate of the 50lb weight, the lumped capacitance method can be used given the relation between heat flux, *q,* and the thermal heat capacity:

$$q = mc_p \frac{dT}{dt} \tag{6.1}$$

where m is the mass of the material and c_p is its specific heat capacity. Assuming that all of the heat generated by the heater gets pulled through the bond ring into the heat sink and then into the steel block, a heater power of 200 W results in a heat flux, q, into the steel weight of 200 $J \cdot s^{-1}$. Given the mass of the steel block of 50 lb (22.7 kg) and its specific heat capacity (419 $J \cdot kg^{-1} \cdot {}^oC^{-1}$), Equation 6.1 predicts a worst case temperature increase into the steel weight of 1ºC per 47 seconds. This was important because all of the bond experiments conducted in Section 6.4 use input powers lower than 200W and most of them were conducted for less than 1 minute. This allowed for the assumption of a 23°C (room temperature) boundary condition at the far edge of the steel plate in the model presented in section 6.1.3.

6.1.2 A 1-D CIRCUIT ELECTRICAL EQUIVALENT MODEL

Figure 6.4 shows a simple 1-D circuit electrical equivalent model for how the heat

flow, q, goes from the heater, through the bond ring, to the heat sink. These thermal resistances, R_T are estimated using the lumped sum approach, where each resistance is calculated using:

$$R_T = \frac{\Delta z}{k_T A} \tag{6.2}$$

where Δz is the distance which the heat needs to flow through the material, k_T is the thermal conductivity of the material and A is the cross sectional area of the material.

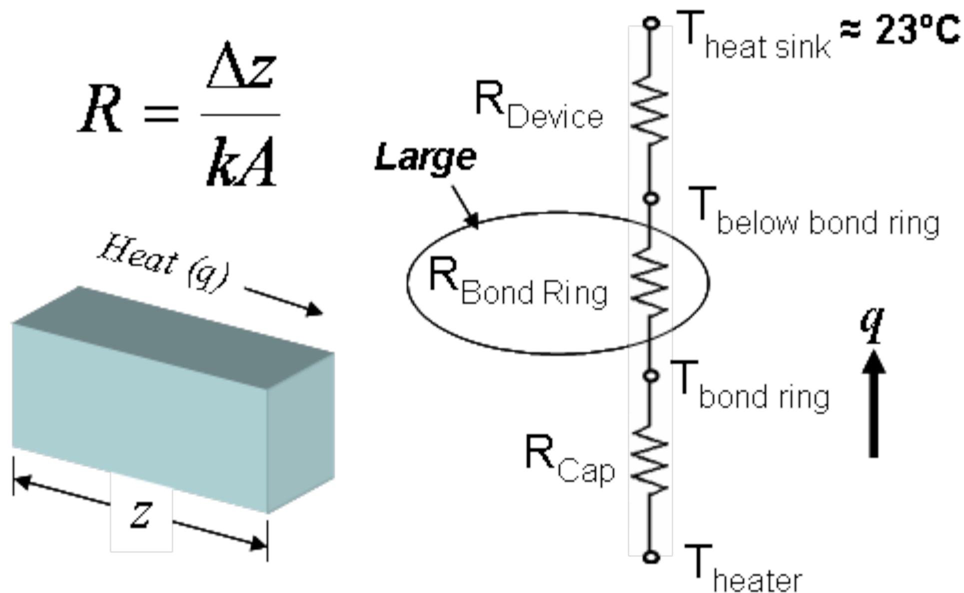


Figure 6.4: The 1-D representation of how heat flows from the heater through the bond rings to the heat sink.

In Figure 6.4, the heat flow starts at the heater where the temperature is T_{heater}. As the heat flows through each resistive element, the temperature drops until it gets to the heat sink, $T_{heat\ sink}$. Ideally $T_{heat\ sink}$ is at or near 23ºC (room temperature). Larger thermal resistances result in larger temperature drops. There is a relatively small temperature drop through the cap wafer, $R_{Cap},$ since the thermal conductivity of Si is very high. Given that the thermal conductivity of air (at atmospheric pressure) is roughly 5000 times lower than that of Si, almost all of the heat conducts through the bond ring. This heat flow is therefore focused through the bond ring towards the device wafer. In the models

presented in the following section (Section 6.1.3), this device wafer is made of glass, Si and Si with a 7 μm thick SiO_2 layer. When this device wafer is glass, the thermal conductivity directly above the bond ring, $R_{Bond\ ring}$, is extremely large as compared to the other thermal resistances. Considering equation 6.2, this is because of: i) the relatively small cross-sectional area at the bond ring, A_B, and ii) the small thermal conductivity, k_{Tg}, of glass. This large thermal resistance directly underneath the bond ring, $R_{bond\ ring}$, is desirable for two reasons: 1) it causes a relatively large temperature drop under the bond ring and laterally towards the device, which is necessary for thermal isolate of the device; and 2) a large thermal resistance directly under the bond ring allows for better thermal isolation of the heater from the heat sink, which means less input power is needed to achieve a given temperature at the bond ring. As a result, it can be difficult to achieve good thermal isolation of a device when bonding directly to a very thermally conductive material such as Si. This will be demonstrated in the models presented in Section 6.1.3. As will also be demonstrated in Section 6.1.3, using a low thermal conductivity thin film such as SiO_2 on top of a Si wafer can drastically improve the thermal isolation inside of the bond ring.

6.1.3 A 3-D MODEL OF THE TEST SETUP

As will be described in Section 6.3, in the test setup, 4 bond rings are heated at a time during bond experiments. Figure 6.5 shows the structure of the "test setup model." As shown in Figure 6.5, in this model, there is symmetry along the planes perpendicular to the x and y axes (adiabatic boundary conditions) so that the model represents a quarter of the actual assembly. Because of this quarter symmetry, the model in Figure 6.5 represents a single heater that heats up 4 bond rings at the same time. The picture of the assembly in Figure 6.5 was made transparent to allow a view of a quarter of the 0.75×10500×13300μm heater. Adjacent bond rings are also shown in the figure. As will be described, these bond rings affected how the heat flowed through the assembly.

Because of the large number of nodes in this 3-D model, a transient model would have been difficult to execute and as a result the model was run assuming steady state conditions. In simulating the model, a steady state solution was found by applying a uniform power density across the 0.75 μm thick heater, while the top of the steel weight

and the bottom of the insulator plate were held at 23ºC (room temperature). As explained in the Section 6.1.1, this assumption was made because the large thermal mass of the 50 lb steel weight made for a slow heating rate in that material. In the following subsections, Si to glass (Section 6.1.3.1), Si to Si (Section 6.1.3.2), and Si to Si with a 7 µm SiO_2 layer (Section 6.1.3.3) bonds are analyzed.

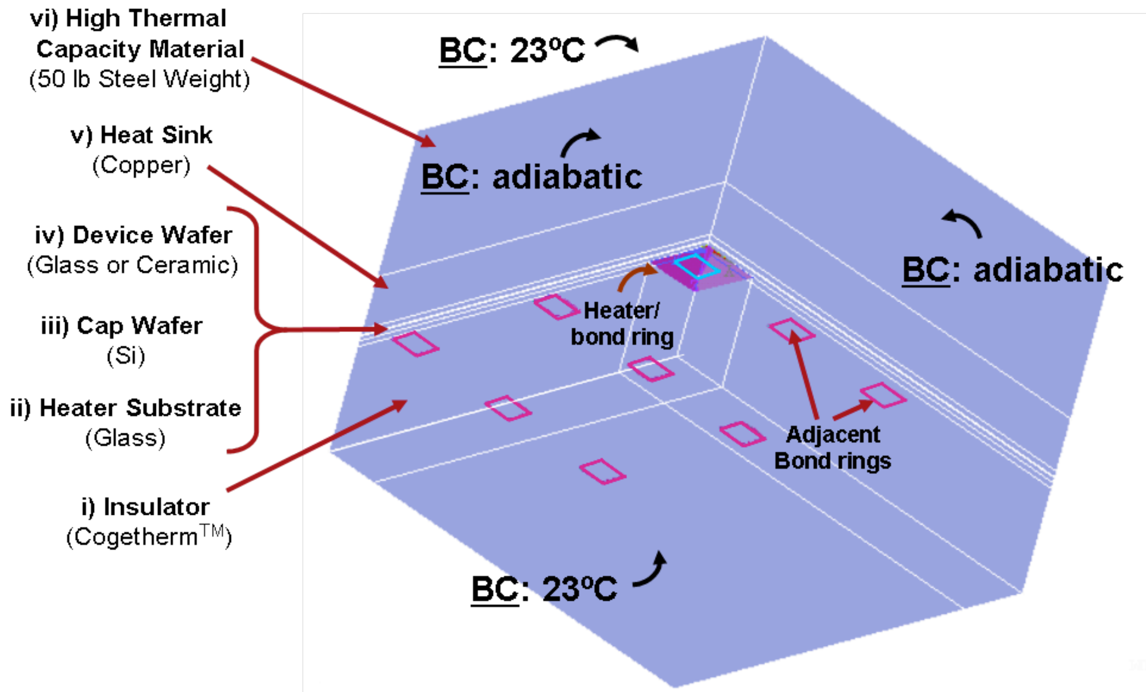


Figure 6.5: The structure of the model used for modeling the test setup.

6.1.3.1 Si to Glass Bonds

Figure 6.6 shows the case where an input power of 26.8 Watts/bond ring was needed to achieve a minimum 400ºC bond ring temperature for the modeling of a Si to glass bond. In Figure 6.6, slices of the model have been taken vertically across the bond ring to show a cross-sectional view (Figure 6.6a and Figure 6.6b), laterally across the heater (Figure 6.6c) and laterally through the bond ring (Figure 6.6d). In the cross-sectional view shown in Figure 6.6a, the location of the heater substrate, cap wafer, device wafer and heat sink are labeled. Also, the location of the heater is denoted by a dotted line. As illustrated in the cross-sectional view, heat is pulled towards the heat sink, but also laterally towards the adjacent bond rings. This causes a large temperature gradient

laterally across the assembly. Figure 6.6c illustrates the resultant temperature gradient across the heater itself. Since this is a quarter symmetry model, in Figure 6.6c, the hottest point at 501ºC is in the center of the heater and the temperature reduces at distances farther and farther away from the center. This results in the temperature profile shown in Figure 6.6d across the bond ring where the temperature ranges from 400ºC to 461ºC. On the other hand, at 500 μm away from the bond ring the temperature was only 134 ºC (29% of the minimum bond ring temperature) and at the center of the bond ring the temperature was around 75ºC (14% of the minimum bond ring temperature). Therefore, despite the non-uniformity of the heating, there is significant thermal isolation inside of the bond ring.

A more ideal model is presented in Section 6.6 where the heater encompasses all of the bond rings across a wafer. In this case their temperature across the wafer and each bond ring is uniform and less power per bond ring is needed since heat is not pulled away from adjacent bond rings. Those modeling results will be discussed in Chapter 7 in the context of future work to be done.

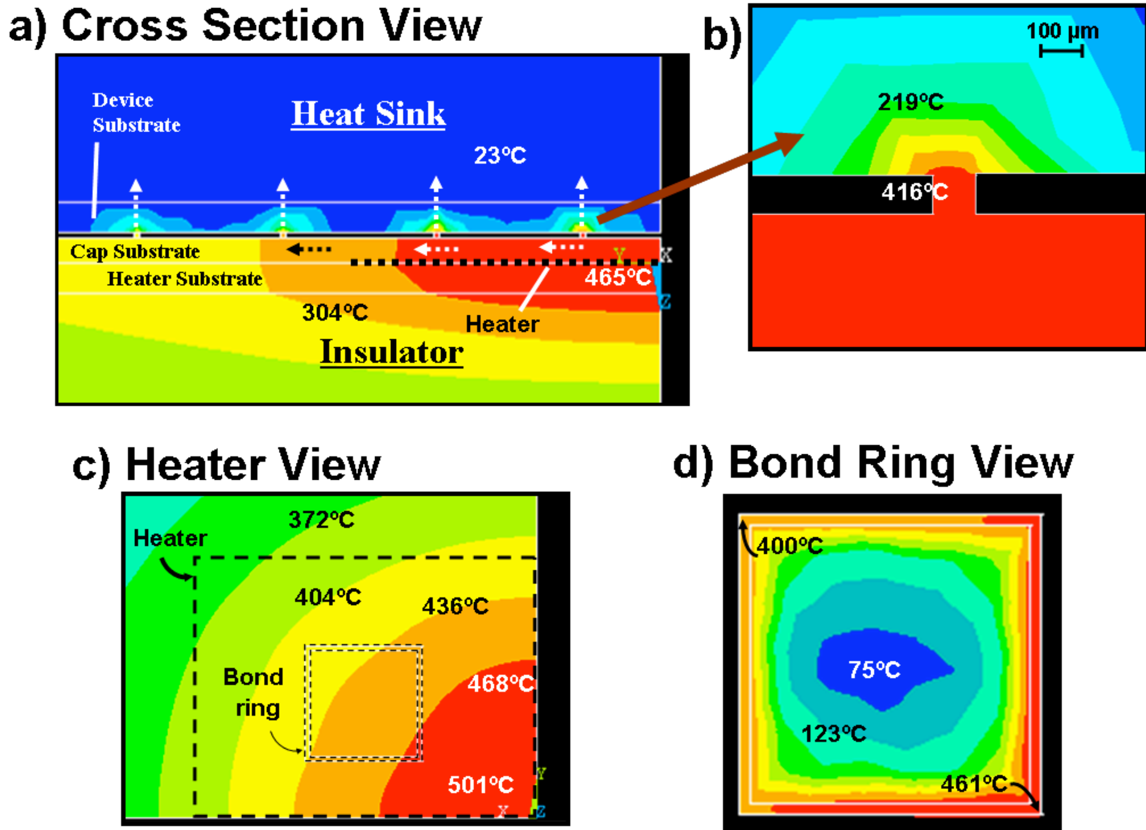


Figure 6.6: Results from the "test setup model," for a *Si to glass bond* showing a) a cross-section view showing how the heat flows into the heat sink, b) a closer look at the cross-section of the bond ring, c) a section of the heater, and d) the heat distribution across the bond ring and inside of the bond ring.

6.1.3.2 Si to Si Bonds

Figure 6.7 shows the case where an input power of 463 Watts/bond ring was needed to achieve a minimum 400ºC bond ring temperature for the modeling of a Si to Si bond. In Figure 6.7, slices of the model have been taken vertically across the bond ring to show a cross-sectional view (Figure 6.7a and Figure 6.7b), laterally across the heater (Figure 6.7c) and laterally through the bond ring (Figure 6.7d). Once again, as illustrated in the cross-sectional view, heat is pulled towards the heat sink, but also laterally towards the adjacent bond rings causing a large temperature gradient laterally across the assembly. As illustrated in Figure 6.7c, the hottest temperature again is at the center of the heater and is 1652ºC. It would be difficult to choose a heater material and substrate materials

which could handle such high temperatures. Furthermore, as illustrated in Figure 6.7d the minimum temperature inside of the bond ring of 318ºC (81% of the minimum bond ring temperature) is not significantly lower than the bond ring temperature.

As was explained in Section 6.1.2, the high necessary input power and bad thermal isolation inside of the bond ring resulted from using a highly thermally conductive device substrate.

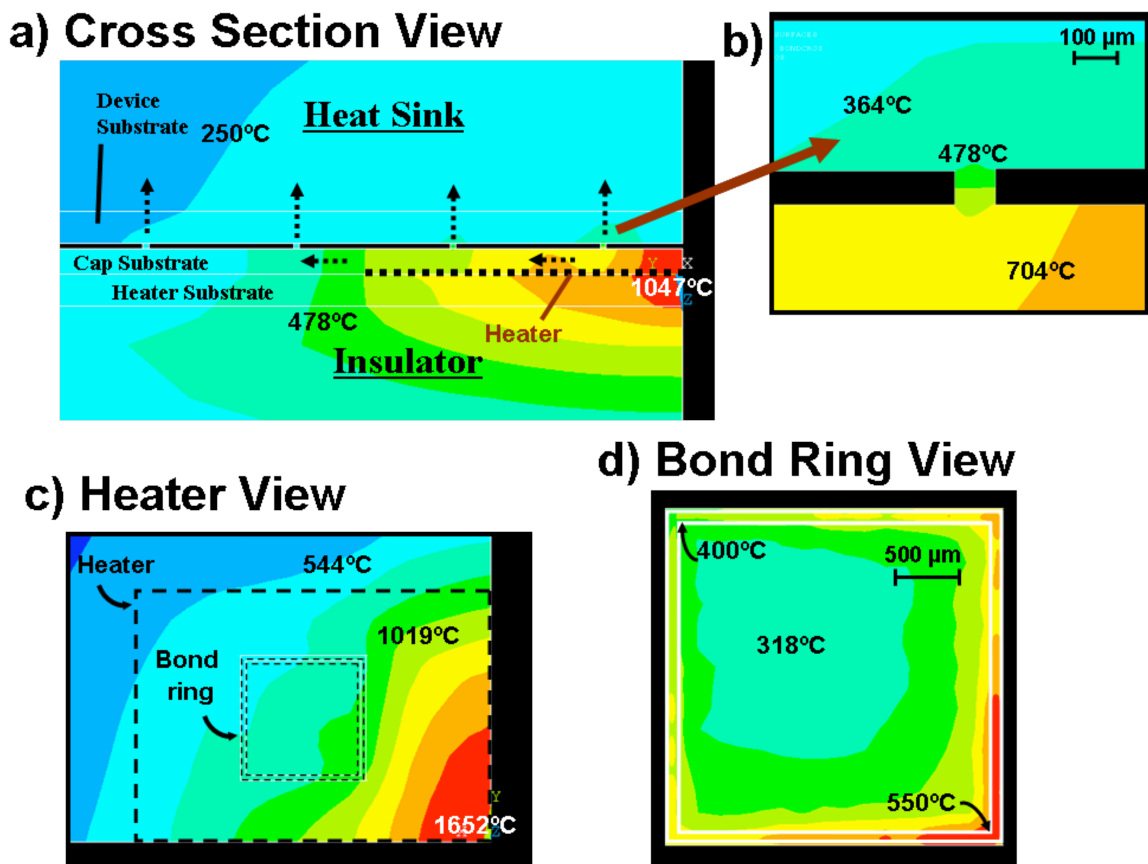


Figure 6.7: Results from the "test setup model," for a *Si to Si bond* showing a) a cross-section view showing how the heat flows into the heat sink, b) a closer look at the cross-section of the bond ring, c) a section of the heater, and d) the heat distribution across the bond ring and inside of the bond ring.

6.1.3.3 Si to Si Bonds with a 7 μm Thick Surface Oxide

Given the analysis in Section 6.1.2, using a less thermally conductive material at the bond ring interface should lower the necessary input power and allow for better thermal

isolation of the device. A 7 μm thick SiO_2 layer was chosen for this purpose. As explained at the beginning of this chapter, this thickness was chosen to roughly mimic the various thin films in a CMOS process.

Figure 6.8 shows the case where an input power of 166 Watts/bond ring was needed to achieve a minimum 400ºC bond ring temperature for the modeling of a Si to Si (with a 7 μm thick SiO_2 layer) bond. In Figure 6.8, slices of the model have been taken vertically across the bond ring to show a cross-sectional view (Figure 6.8a and Figure 6.8b), laterally across the heater (Figure 6.8c) and laterally through the bond ring (Figure 6.8d). Once again, as illustrated in the cross-sectional view, heat is pulled towards the heat sink, but also laterally towards the adjacent bond rings causing a large temperature gradient across the assembly. As shown in Figure 6.8b, the temperature drops significantly through the SiO_2. As discussed earlier, this significant temperature drop is necessary for achieving good thermal isolation inside of the bond ring. As illustrated in Figure 6.8c, the hottest temperature is at the center of the heater and is 920ºC. Though this temperature is still relatively high, and would make material selection difficult, it is much closer to a reasonable value than for the Si to bare Si bond described in the previous section (Section 6.1.3.2). One option for this material set is to lower the necessary bond ring temperature by using a lower temperature bonding method.

Finally, Figure 6.8d shows the temperature profile across the bond ring where the temperature ranged from 400ºC to 540ºC. Despite this large range in temperatures, the model predicts a relatively constant temperature inside of the bond ring where 500 μm away from the bond ring the temperature was only 146ºC (33% of the minimum bond ring temperature).

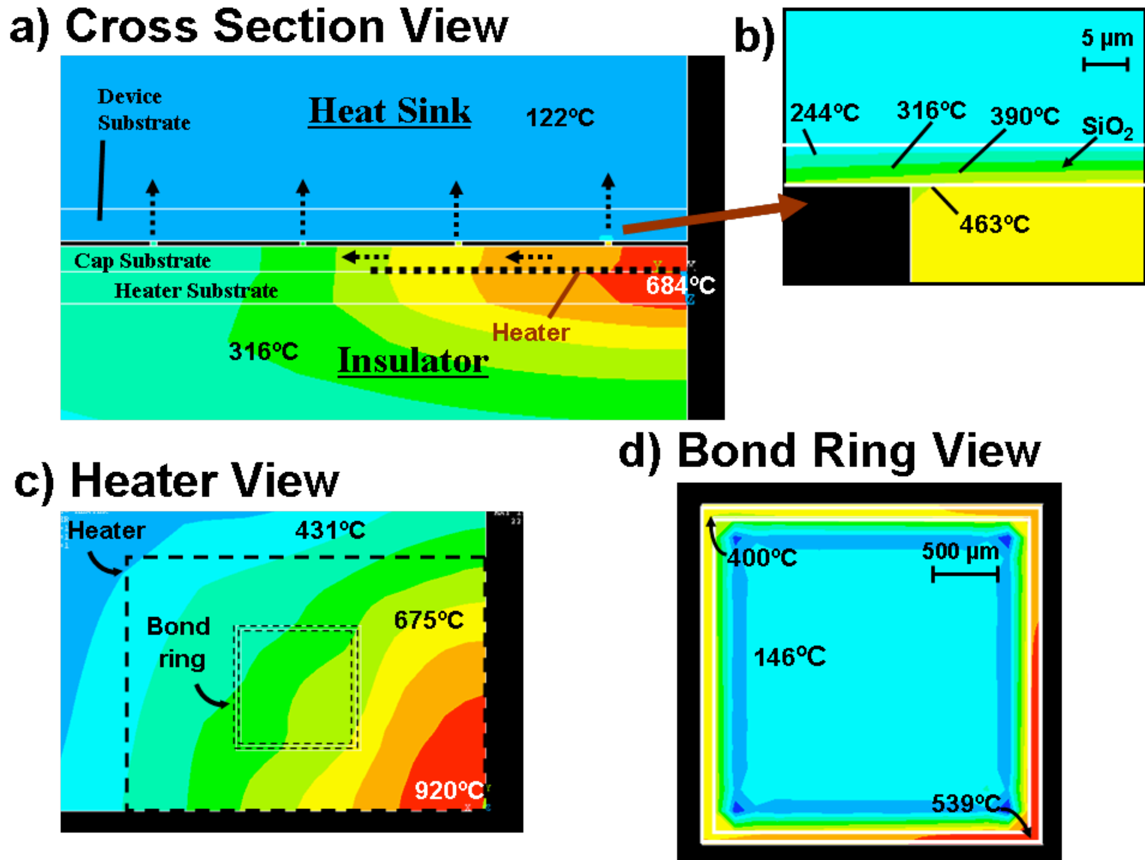


Figure 6.8: Results from the "test setup model," for a *Si to Si bond with a 7 µm thick SiO_2 layer* showing a) a cross-section view showing how the heat flows into the heat sink, b) a closer look at the cross-section of the bond ring, c) a section of the heater, and d) the heat distribution across the bond ring and inside of the bond ring.

6.1.4 SUMMARY OF MODELING RESULTS

The analysis and modeling results presented in this section (Section 6.1) demonstrated the need for a non-thermally conductive device wafer material in order to facilitate *differential localized heating*. As a result, two material combinations were chosen for bond experiments: Si to glass wafer bonds (bond experiment #1), and Si to Si wafer bonds with a 7 µm thick SiO_2 layer (bond experiment #2).

In the models presented in and Section 6.1.3, a large enough power was applied in each case so that the minimum bond ring temperature, T_{Bmin}, was at least 400ºC. Because all of the temperatures in these models varied linearly with the power input to the heater,

all of the temperatures could be represented as ratios of the minimum bond ring temperature, R_{BR}. Table 6.2 summarizes some of the modeling results showing the important R_{BR} values. As illustrated, the model predicts an R_{BR} value of 29% at 500 μm away from the bond ring for bonds to glass and 33% at 500 μm away from the bond ring for bonds to Si wafers with a 7μm thick SiO_2 layer. These numbers illustrate good thermal isolation inside of the bond ring. On the other hand, for bonds to a bare Si wafer, the R_{BR} value was 94% indicating bad thermal isolation.

Table 6.2: Summary of the modeling results showing the R_{BR} values (temperature relative to the minimum bond ring temperature) on the heater and at 500μm from the bond ring on the device wafer. All of the simulations were done using the "test setup model" with bond ring widths of 100 μm.

Device wafer material	R_{BR} Bond Ring	R_{BR} Maximum at Heater	R_{BR} at 500 μm from Heater
Glass Wafer (Bond Experiment #1)	100%	127%	**29%**
Si Wafer with 7 μm SiO_2 (Bond Experiment #2)	100%	239%	**33%**
Bare Si Wafer	100%	328%	**81%**

It is also important to compare the R_{BR} values for the maximum heater temperatures. This is important because material selection for the heater becomes difficult at very high temperatures. More specifically, the Au thin film heaters used in the test setup (which will be described in Section 6.3) were observed to burn out at around 500ºC. As illustrated in Table 6.2, for bonds to glass, the maximum R_{BR} on the heater was 127%. Because of this relatively low R_{BR} value, for Si to glass bonds (*bond experiment #1*) a Au-Si eutectic bond could be applied using this bonding technique. Au-Si eutectic bonding was already studied in detail in Chapters 2 through 5 and can potentially be achieved at temperature just above 363ºC.

On the other hand, for bonding a Si wafer to a Si wafer with a 7μm thick SiO_2 layer (*bond experiment #2*), the maximum R_{BR} on the heater was 239%. Therefore, Au-Si eutectic bonding could not be applied since temperatures ≥363ºC across the entire bond ring would require the heater to withstand a temperature of 835ºC according to the model. Therefore, for *bond experiment #2*, a Sn-Ag solder bond was attempted. The eutectic temperature for Sn-Ag solder at its eutectic composition is only 221ºC. The model

therefore predicts that the heater would have to withstand a temperature of only 496ºC.

Table 6.3 summarizes some of the modeling results showing the important input power parameters for the "test setup model." As shown, for bonds between Si and glass (*bond experiment #1*), there was an increase in heater temperature of 3.9°C for every Watt of input power while the minimum bond ring temperature increased by 3.5°C/W. For bonds between a Si and a Si wafer with a 7 µm SiO_2 layer (*bond experiment #2*), a significantly larger amounts of power was needed. The heater temperature increased by 0.89°C/W while the minimum bond ring temperature increased by only 0.57°C/W.

Table 6.3: Summary of the modeling results showing the average heater temperature per input power and the minimum bond ring temperature per input power. All of the simulations were done using the "test setup model" with bond ring widths of 100 µm.

Device wafer material	Average Heater Temperature/Input Power	Minimum Bond Ring Temperature/Input Power
Glass Wafer (Bond Experiment #1)	3.9 K/W	3.5 K/W
Si Wafer with 7 µm SiO_2 (Bond Experiment #2)	0.89 K/W	0.57 K/W
Bare Si Wafer	0.49 K/W	0.20 K/W

6.2 WAFER FABRICATION FOR BOND EXPERIMENTS

Two sets of bond experiments were conducted: i) between a Si cap wafer and a glass device wafer (*bond experiment #1*) and ii) between a Si cap wafer and a Si device wafer with a ~7 µm SiO_2 layer (*bond experiment #2*). As was explained in the previous section (Section 6.1), these materials were chosen for the device wafer substrates because of their low thermal conductivities which helped to provide better thermal isolation inside of the bond ring.

The *bond experiment #1* wafers were prepared to facilitate a bond between an Au-Si eutectic layer on the Si cap wafer and a Au thin film on the glass device wafer. This is shown schematically in Figure 6.9a. The Au-Si eutectic bonds reported in Chapters 2 though 5 were conducted at 390 to 410ºC and could potentially be done at as low as the Au-Si eutectic temperature of 363ºC. At these temperatures, Si diffuses from the cap wafer into the Au bond ring allowing for the formation of the Au-Si eutectic. This

material set was chosen since the Au-Si eutectic bonding method was already characterized in Chapters 2 through 5.

For *bond experiments #2*, wafers were prepared to facilitate a bond between a Ni/Sn/Ag layer on the Si cap wafer and a Sn/Ag layer on the device wafer. This is shown schematically in Figure 6.9b. Sn-Ag solder has a melting temperature of around 221ºC at its eutectic composition of 3.5 weight % of Ag in Sn. This composition was achieved by electroplating 6 μm of Sn on the cap and device wafer and evaporating 3000Å of Ag on the cap wafer. For Sn-Ag solder bonding, the temperature is simply raised above the melting temperature of the solder, allowing for Sn-Ag inter-diffusion and softening. The Ni layer acted as a diffusion barrier to stop the Sn-Ag solder from inter-diffusing with the seed-layer which was made out of Cr/Au. As explained elsewhere [116], such inter-diffusion can cause delaminating of the film and therefore bad adhesion. This material set was chosen because of the relatively higher maximum heater temperature of around 237% of the minimum bond ring temperature predicted from the modeling for this material set. This higher heater temperature would cause the heater to fail at the ≥363ºC necessary bond ring temperature in the Au-Si eutectic bond.

Section 6.2.1 explains the fabrication process for the cap wafers and Section 6.2.2 explains the fabrication process for the device wafers used in *bond experiment #1* and *bond experiment #2*.

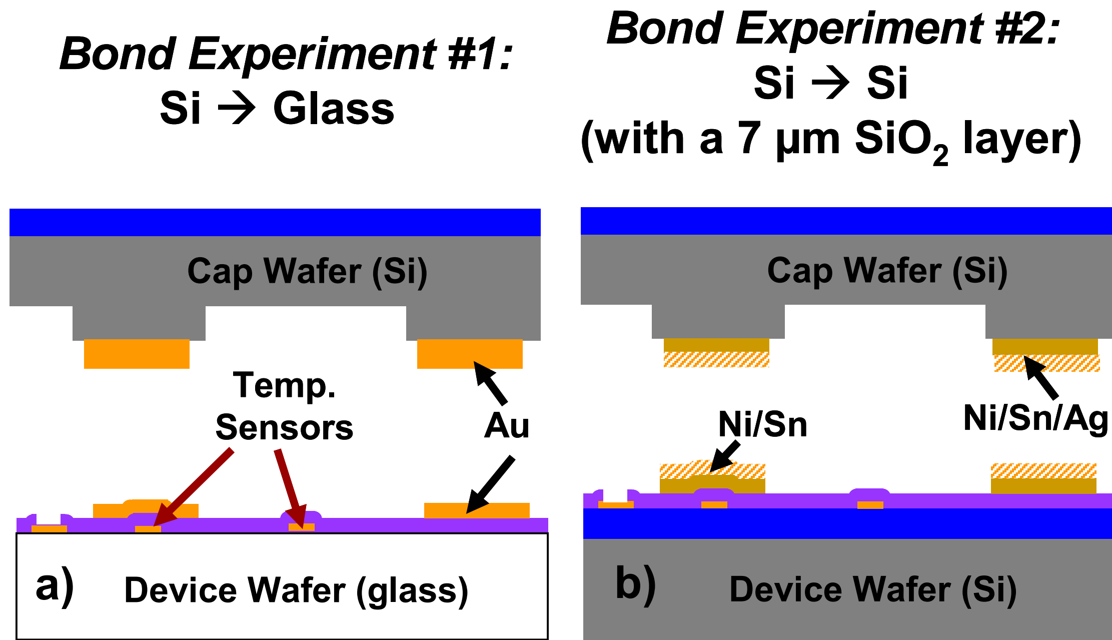


Figure 6.9: Schematics of the cap and device wafers fabricated for bond tests for a) the Si to glass bonding process and b) the Si to Si wafer with 7 µm of SiO_2.

6.2.1 CAP WAFER FABRICATION

Figure 6.10 shows the fabrication processes for the bond experiments #1 and #2 cap wafers. Fabrication of each set of cap wafers began with growth of a 1.9 µm thick thermal SiO_2 layer. This thermal SiO_2 was removed from the front side of the wafer using BHF (buffered hydrofluoric acid) and masking the backside with photoresist as shown in Figure 6.10a and Figure 6.10d. This SiO_2 layer was used to electrically isolate the Au coils on the heater which made direct contact with the backside of the cap wafer (See Section 6.3 for a full description of the test setup). Such a thick SiO_2 layer was needed because of the up to 300 V applied to this heater in the bond experiments that will be presented in Section 6.4 (*Results & Discussion*).

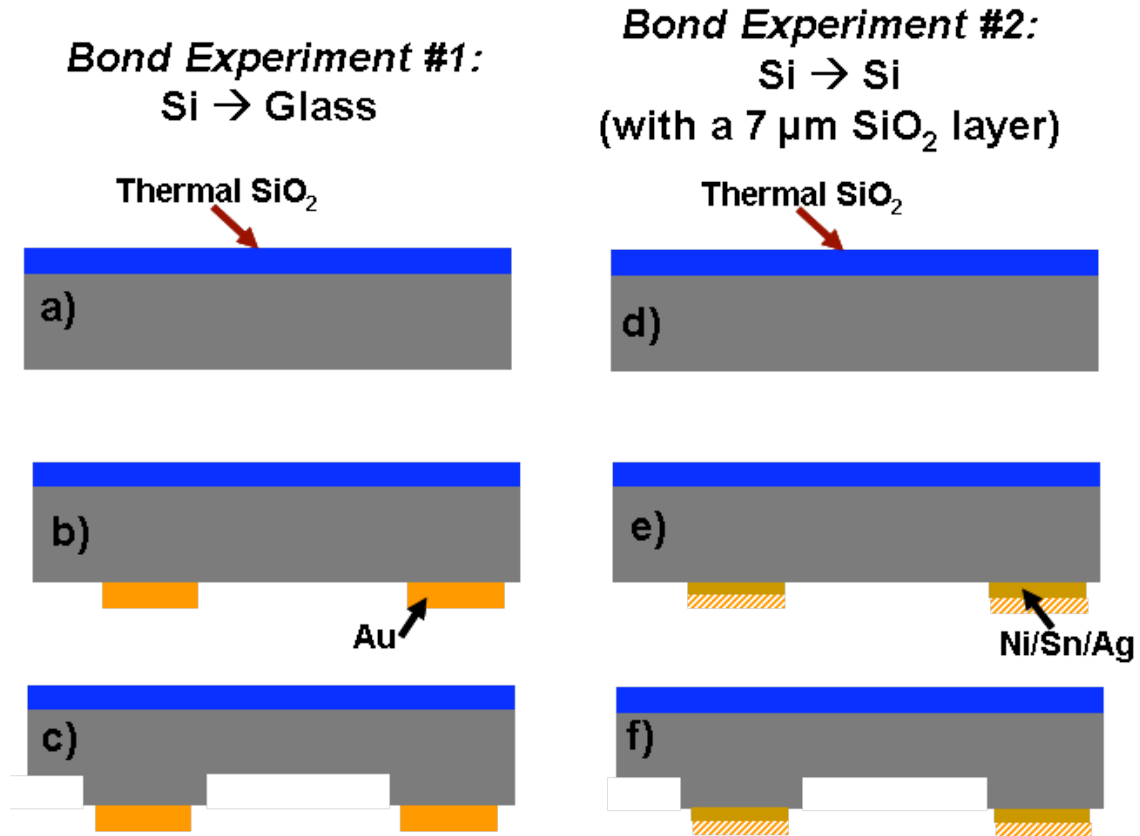


Figure 6.10: The fabrication process for cap wafers for a-d) Si to glass bonds and e-h) Si to Si bonds with a 7 μm thick oxide layer.

Figure 6.10b shows the 4 μm thick Au bond ring layer deposition and patterning step used for *bond experiment #1*. In defining this layer, directly after the BHF etching step, 200/5000 Å of Cr/Au was evaporated on top of bulk silicon, acting as the ***seed layer*** for electroplating. These metals were deposited in an E-beam Enerjet evaporator at $\sim 2\times 10^{-6}$ Torr. As was explained in Section 3.1 of Chapter 3 this BHF dip preceding the evaporation step is used in the Au-Si Eutectic bonding process to ensure that the Cr/Au layer was directly in contact with the bulk Si and that a thick native oxide would not prevent inter-diffusion. This inter-diffusion is necessary for creation of the liquid Au-Si eutectic needed to facilitate the Au-Si eutectic bond. Next, as in Section 3.1 of Chapter 3, 10 microns of AZ 9260 photoresist was deposited and patterned, acting as a mold for Au electroplating. Electroplating was done using BDT-510 makeup plating solution with a

stainless steal cathode on one side of the bath and the wafer on the other side serving as the anode. A current source was used to supply the source current with the cathode attached to the positive side and clips touching the top of the wafer were connected to ground. The wafers were electroplated at 50ºC with a current density of 2mA/cm^2 resulted in a plating rate of around 0.1 µm per minute (these wafers had 96, 100 µm wide bond rings and therefore an electroplated surface area of ~0.97 cm^2 and a supply current of 1.9mA). The bond ring was electroplated to a thickness of 4 µm. Finally, the photoresist mold was removed and the then the seed layer (the Cr/Au layer) was etched away using TFA Au etchant for approximately 3 minutes and then CR-14 Cr etchant for 30 seconds.

Figure 6.10e shows the 3µm/7µm/0.3µm Ni/Sn/Sg bond ring layer deposition and patterning step used for *bond experiment #2*. In defining this layer, 200/5000Å of Cr/Au was first evaporated on top of the bulk silicon. This layer acted as the ***seed layer*** for electroplating. (It was not important in this process to go directly from the BHF etch to the evaporator since the Au-Sn bond does not use Si diffusion for creation of a eutectic.) Next, 20 µm of AZ 9260 photoresist was deposited and patterned, acting as a mold for the Ni/Sn electroplating. Nickel electroplated was done at 50ºC in a sulfate based electroplating solution with a current density of 21mA/cm^2 for 10 minutes resulting in the 3 µm thick Ni film. Directly before tin electroplating, the wafer was next placed in dilute (~10%) hydrochloric (HCL) acid in order to remove the nickel oxide to improve adhesion. The Sn layer was electroplated at room temperature in Bright Tin Electroplating Solution at 30 mA/cm^2 for 10 minutes resulting in the 7 µm thick Sn film. Next, the 0.3 µm Sg layer was evaporated on top of this metal stack in an Energet Evaporator. The wafers were then placed in acetone in order to remove photoresist. Next 20 µm of AZ 9260 photoresist was patterned over the bond rings in order to protect the bond ring materials from the seed layer etch. The Cr/Au seed layer was then etched away using TFA Au etchant for approximately 3 minutes and then CR-14 Cr etchant for 30 seconds. This photoresist layer was left on for the next process step.

The final process step for each of the cap wafers was the Deep Reactive Ion Etch (DRIE) step used to define the cavity. This step is shown in Figure 6.10c and Figure 6.10f. For *bond experiment #1,* 10 µm of AZ 9260 photoresist was first patterned over

the bond rings (as mentioned in the last paragraph, for *bond experiment #2* the photoresist mask from the previous patterning step was left on.) For both processes, the wafers were next placed in a STS Multiplex ICP DRIE etcher in order to etch the 90 µm deep cavities. Finally, the photoresist mask was removed. Directly before the cap and device wafers were aligned for bonding, the cap wafers were solvent cleaned (soaked in acetone, then isopropanol and then DI water).

6.2.2 DEVICE WAFER FABRICATION

Figure 6.11, shows the fabrication processes for the device wafers for *bond experiments #1 and #2*. Fabrication of the *bond experiment #2* wafers (Figure 6.11e) began with the deposition of a 7 µm PECVD SiO_2. Next, for both the *bond experiment #1 and #2* wafers, the temperature sensor layer was deposited and patterned as shown in Figure 6.11a and Figure 6.11e. Definition of this layer began with the patterning of a 1.5 µm thick SPR220 photoresist. A 100Å/1000Å Cr/Pt layer was then evaporated in the E-beam Enerjet evaporator at $\sim 2\times10^{-6}$ Torr, over top of the patterned photoresist. Acetone was then used to remove the photoresist in a lift off process leaving the Cr/Pt lines which defined the temperature sensors, feed-throughs and bond pads. Chromium was used because it acted as an adhesion layer for the platinum and the platinum was chosen for the temperature sensor material because of its chemical inertness and its high TCR.

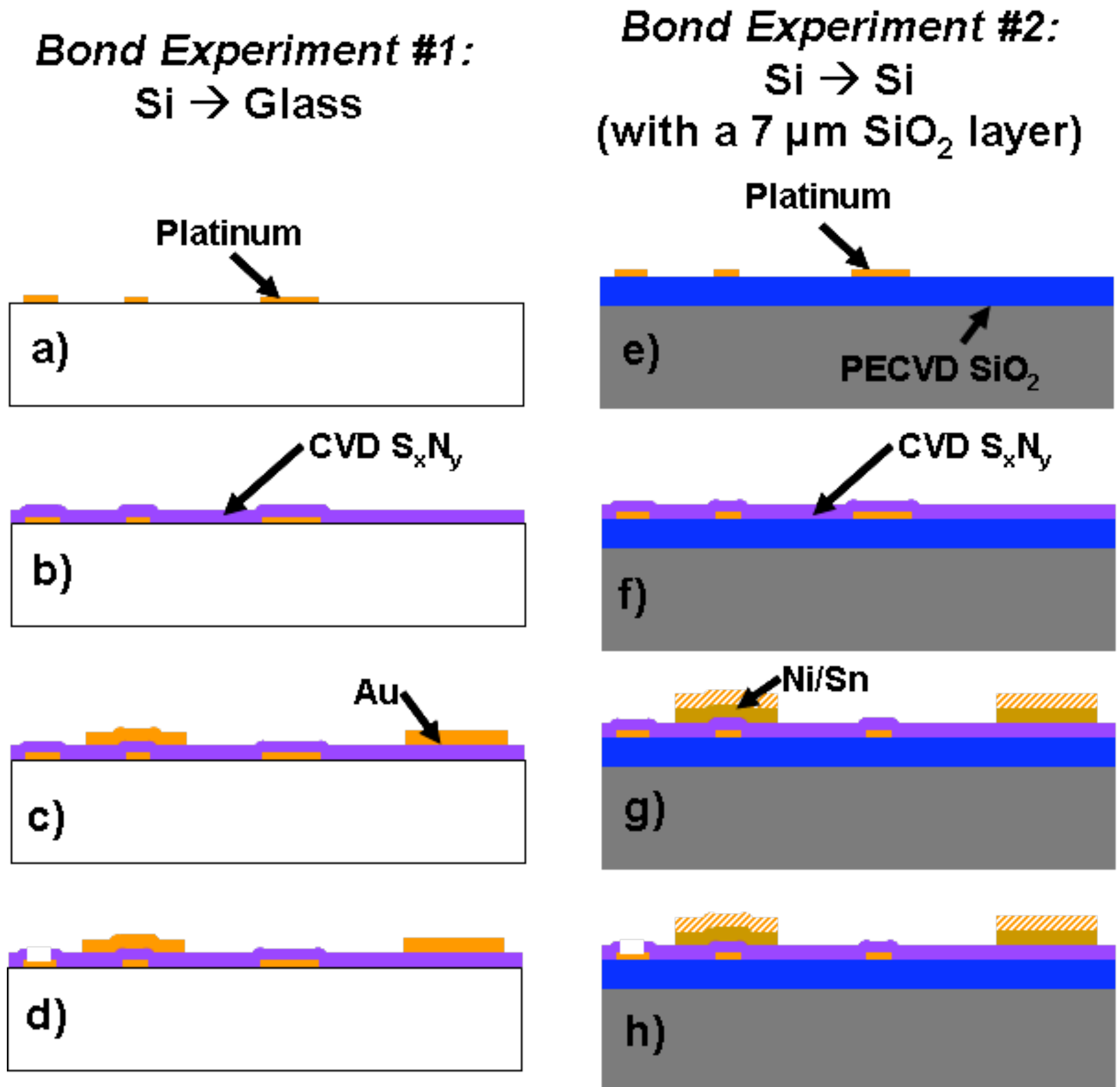


Figure 6.11: The fabrication processes for the cap and device wafers for a-d) Si to glass bonds and e-h) Si to Si bonds with a 7 µm thick oxide layer.

Next, a 5000Å layer of PECVD Si_xN_y was deposited as shown in Figure 6.11b and Figure 6.11f. This layer served an electrical insulating layer. Silicon nitride was chosen because its thermal conductivity (14 W/m·K) is roughly 10 times that of SiO_2 (1.4 W/m·K). As a result, given its relatively larger thermal conductivity and the thickness of this layer relative to that of the 7 µm SiO_2 (in bond experiment #2), according to Equation 6.2 there should be approximately 1/140th of the temperature drop through this

layer as compared to the SiO_2 layer.

Next, the bond ring layer was deposited as shown in Figure 6.11c and Figure 6.11g. On the *bond experiment #1* wafers, a 200Å/5000Å Cr/Au layer was sputtered on using an Enerjet Sputter Coater. This layer was patterned and then etched using TFA Au etchant for approximately 3 minutes and then CR-14 Cr etchant for 30 seconds. On the *bond experiment #2* wafer, the 3µm/7µm Ni/Sn layer was deposited using the same process steps outlined in the previous section (Section 6.2.1) using a photoresist mold and electroplating both the Ni and Sn layers.

Finally as shown in Figure 6.11d and Figure 6.11h, on both sets of wafers, using a 1.5 µm thick SPR220 photoresist mask, the Si_xN_y layer was etched in BHF (buffered hydrofluoric acid) for 10 to 15 minutes to open up the bond pads for electrical access.

6.3 TEST SETUP DESIGN & ASSEMBLY

Appendix 2 describes the wafer bonders which were used for the bond experiments outlined in Chapter 2 and Chapter 5. These wafer bonders included: an EVG 510 wafer bonding system, an SB6 semi-automated wafer bonding system and an SB6e semi-automated wafer bonding system. Unfortunately these wafer bonder systems could not be easily adapted for applying the *differential localized heating* wafer bonding method for three reasons. First, it was desirable to have temperature sensors underneath the bond rings and at different distances from the bond ring on the surface of the device wafer during bond tests. These sensors allowed for the temperature profiles inside of the bond rings to be monitored during bonding in order to gauge the effectiveness of this bonding technique in thermally isolating potential devices. Adapting the fixturing for the EVG, SB6 and SB6e bonders and providing electrical interconnection through the vacuum chambers in these bonders would have been difficult. Second, as was discussed in Section 6.1 (*Modeling & Analysis*), a relatively large amount of power is needed to heat bond rings up to 200 to 400ºC when applying differential heating with the dimensions and materials used here. The EVG, SB6 and SB6e bonders were not designed for applying such large powers or sinking large amounts of heat. Third, because of how time consuming it was to fabricate the temperature sensors and integrate them into the test setup, it was desirable to conduct several bond experiments for each bonded pair of

wafers. This could be done by only heating up small portions of the wafer at a time. The heaters in the EVG, SB6 and SB6e bonders on the other hand were only designed to allow for heating of the entire wafer all at once. As a result, a special wafer bonder setup was designed and build for evaluating the *differential localized heating* method.

In the rest of this section, the components of this test setup are described in detail. Section 6.3.1 describes overall test setup design and Section 6.3.2 explains the general layout of the device wafer in relation to the test setup. Section 6.3.3 then explains how the test setup was assembled for testing. Finally, Section 6.3.4 and Section 6.3.5 describe the temperature sensor and heater designs and how they were calibrated and tested during bond experiments.

6.3.1 TEST SETUP DESIGN

The bonder setup described in this section included: 1) an array of micro-machined heaters which allowed for 200 W or more of power to be applied to a 10.5 x 13.3 mm^2 area on the backside of a cap wafer; 2) as supposed to a pneumatic force or a spring force system (as is used in the EVG, SB6 and SB6e bonders) a 50 lb weight was used for apply the bond force, 3) a passive heat sink made of copper and a 50 b steel weight, and 4) fixturing which allows for access to temperature sensors on the device wafer for measurement of temperatures at and near the bond ring during bond tests.

Figure 6.12 shows schematics of the *differential localized heating* bonder setup which accommodated all of these features. As illustrated in Figure 6.12, this test setup consisted of i) a Cogetherm™ plate (Cogetherm™ is a special high temperature insulating composite manufactured by Jaco Products) which functioned both as a mechanical backing plate and a thermal insulator; ii) the heater substrate made out of glass on top of which the Au thin film heater sat atop; iii) the cap wafer substrate which made direct physical contact to the heater; iv) the device wafer which made physical contact with the bond rings on the cap wafer and on the backside, physical contact with the heat sink; v) the copper heat sink; and vi) the 50 lb steel block which provided the bond force and provided a large thermal mass which aided in the heat sinking.

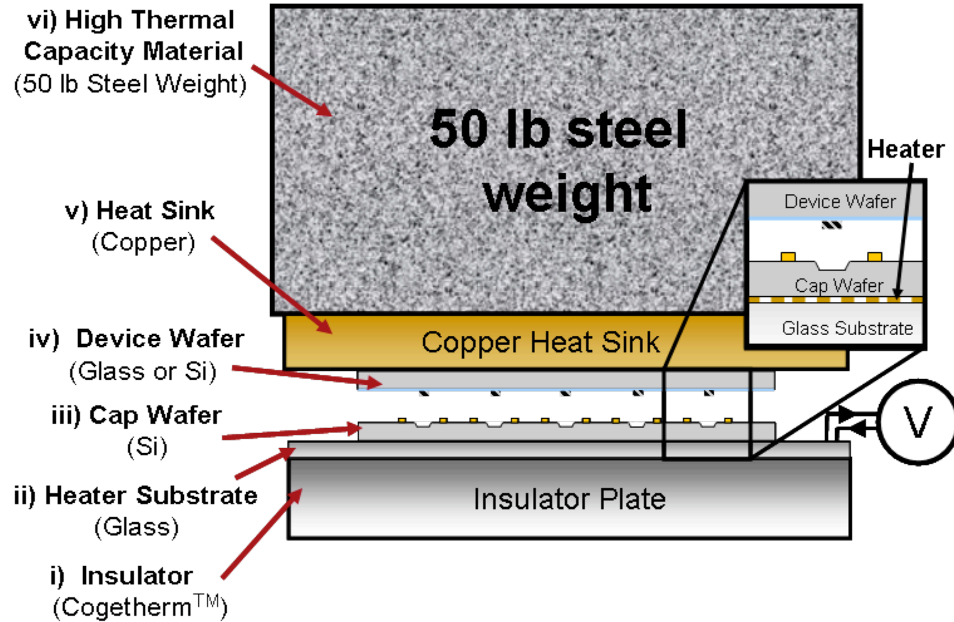


Figure 6.12: Schematics showing cross-sections of the test setup.

6.3.2 LAYOUT OF THE DEVICE WAFERS

Figure 6.13 shows a schematic of the device wafer. The fabrication process for these device wafers were detailed in Section 6.2 (*Wafer Fabrication for Bond Experiments*). The exploded views in Figure 6.13b and Figure 6.13c show the layout of the bond rings and feed-throughs. These bond rings were made out of Au or Ni/Sn, were 100µm wide and encompassed a 2.3×2.3 mm^2 area (as was the case for the bond rings used in many of the bond experiments conducted in Chapter 2 and Chapter 5). Temperature sensors were fabricated underneath some of these bond rings and at different distances from them on the surface of the wafer. The schematic in Figure 6.13c shows 3 temperature sensors, one located directly underneath the bond ring and the other two located at 250 and 750 µm away from the edge of the bond ring. As illustrated in Figure 6.13b, there are four electrical interconnection lines for each temperature sensors making a 4-point probe. In so, the temperature sensors functioned in a similar manner to the Pirani gauges described in Chapter 4. Details on how these sensors were operated and calibrated are presented in Section 6.3.4. The feed-through interconnection lines ran from the temperature sensors themselves out to bond pads at the periphery of the wafer as shown schematically in Figure 6.13a.

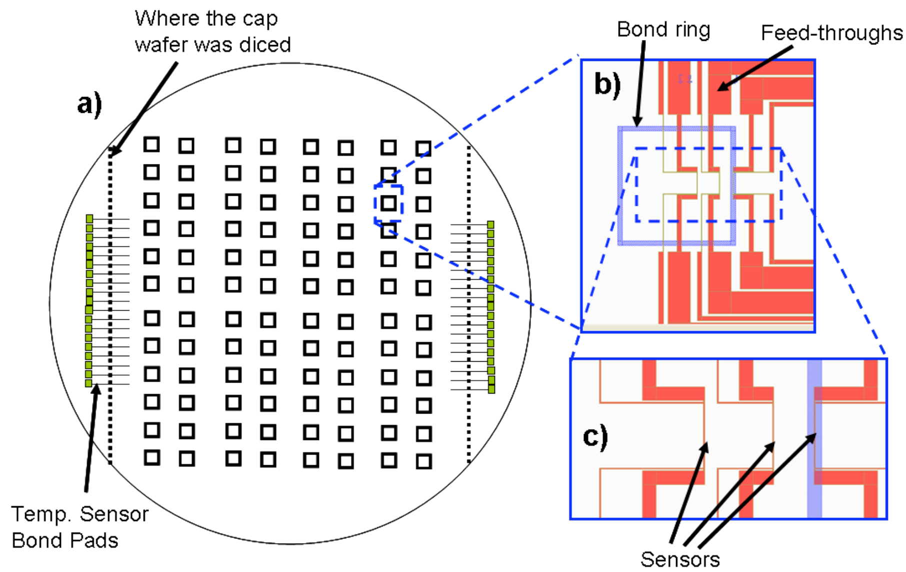


Figure 6.13: A schematics showing how the temperature sensors were laid out across the wafer.

6.3.3 ASSEMBLY OF THE TEST SETUP

As described below, the test setup was assembled in 4 steps: 1) device and cap wafer alignment (Section 6.3.3.1), 2) integration of the copper heat sink (Section 6.3.3.2), 3) incorporation of the heaters (Section 6.3.3.3), and 4) assembly of the entire setup (Section 6.3.3.4).

6.3.3.1 Step 1: Device and Cap Wafers Alignment

The device wafer was aligned to the cap wafer which had bond rings with same dimensions and spacings as the device wafer. This wafer had 90 µm etched cavities (as was shown schematically in Figure 6.12b). Also, before aligning these two wafers part of *cap wafer* on the left and right sides were diced away to allow access to the bond pads on the *device wafer*. The relative location of where this cap wafer was diced is shown schematically in Figure 6.13a. Figure 6.14a shows the device and cap wafer after they had been aligned and clamped together. These wafers were aligned in an SUSS MicroTec SB6 wafer alignment system. While still clamped into the SB6 alignment chuck the clamps shown in Figure 6.14a were applied on the outside edge of the wafer as shown. The wafers were then taken out of the SB6 alignment chuck. Figure 6.14b shows

an exploded view of the area on left side of these aligned wafers where the top cap wafer was diced away. As shown, the bond pads on the device wafer can be accessed because of this diced away region.

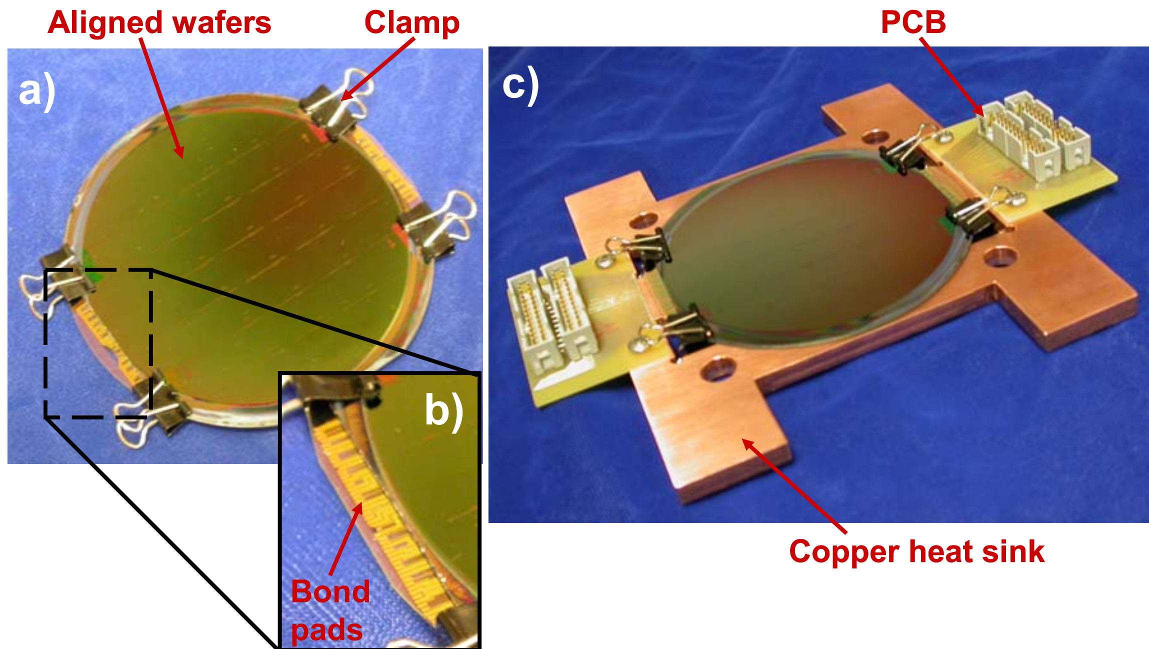


Figure 6.14: a) The aligned cap and device wafers which were held together using clamps, b) a closer look at the edge of these aligned wafers showing how the diced away portion of the cap wafer allows access to bond pads on the device wafer that run to temperature sensors, and c) the aligned wafers that sit on top of the copper heat sink. PCBs on either side of the wafer pair were wire bonded to the bond pads on the device wafer in order to access the temperature sensors near the bond ring.

6.3.3.2 Step 2: Integration of the Copper Heat Sink

Figure 6.14c shows the wafer pair after they were placed on top of the copper heat sink. Two PCBs were screwed into the copper heat sink so that wire bond connections could be made to the PCBs from the 48 bond pads on either side of the wafer (96 total) that ran to temperature sensors at various locations on the wafer. The copper plate itself was finely polished in order to allow for good thermal connection to the backside of the device wafer. As shown in Figure 6.15a there were several other slots and wholes machined into the copper plate. The two large slots at the top and bottom of the plate in Figure 6.15a allowed for electrical connection to the heaters—the orientation of the copper plate with the heater substrates will be described in more detail in Steps 3 and 4. The four slots closer to the center of the plate allow clearance for the clamps (as can also

be seen in Figure 6.14c). Figure 6.14c above showed how this clamped wafer pair fit onto the copper plate. Finally, the four circular holes in Figure 6.15a were used to mate the copper plate with the Cogetherm^{TM} plate in the final assembly.

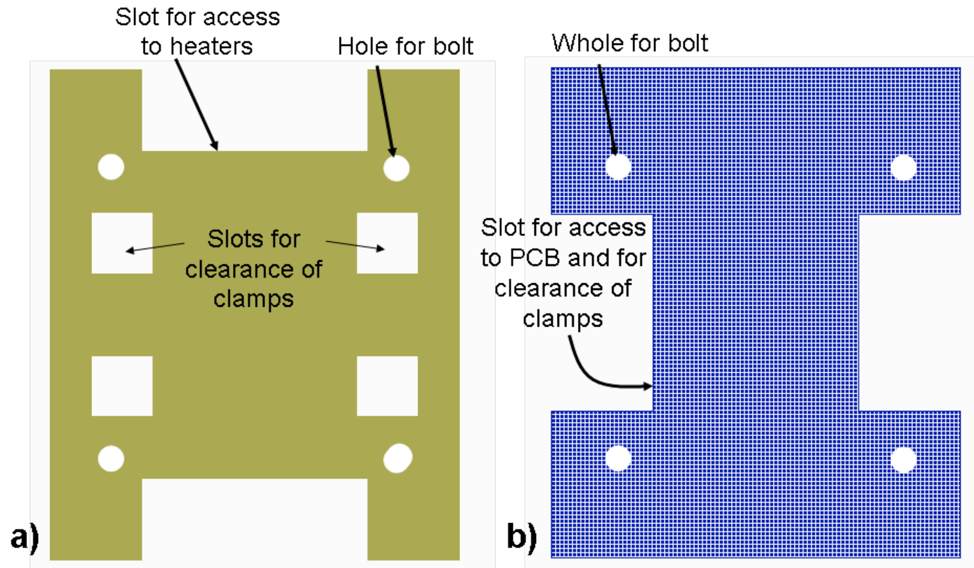


Figure 6.15: The layout of the a) copper heat sink and b) Cogetherm^{TM} insulator plate.

6.3.3.3 Step 3: Integration of the Heaters Substrate & Cogetherm^{TM} Plate

Figure 6.16a shows one of the heater substrates. One full 4" glass wafer was used for the fabrication of each of the heater arrays and then diced to form the 70 x 76 cm rectangular heater substrate shown in Figure 6.16a. Each heater substrate consisted of a 3×5 array of heaters with two leads running from each heater to bond pads at the periphery of the substrate. During testing, wires were soldered to these bond pads and connected to a power supply in order to power the heaters. More detail on the heater design and operation will be given in Section 6.3.5. Two of these heater substrates where need to encompass the bond rings across one full wafer. Figure 6.16b shows two of these heater substrates placed on a Cogetherm^{TM} insulator plate. Figure 6.15b above shows the layout of the machined Cogetherm^{TM} plate. The two large slots at the right and left of the plate in Figure 6.15b allowed for clearance for the PCB. These slots are also oriented to allow for clearance of the clamps holding the wafers together. Finally, the four circular holes in Figure 6.15b were used to mate the Cogetherm^{TM} plate with the copper plate in

the final assembly.

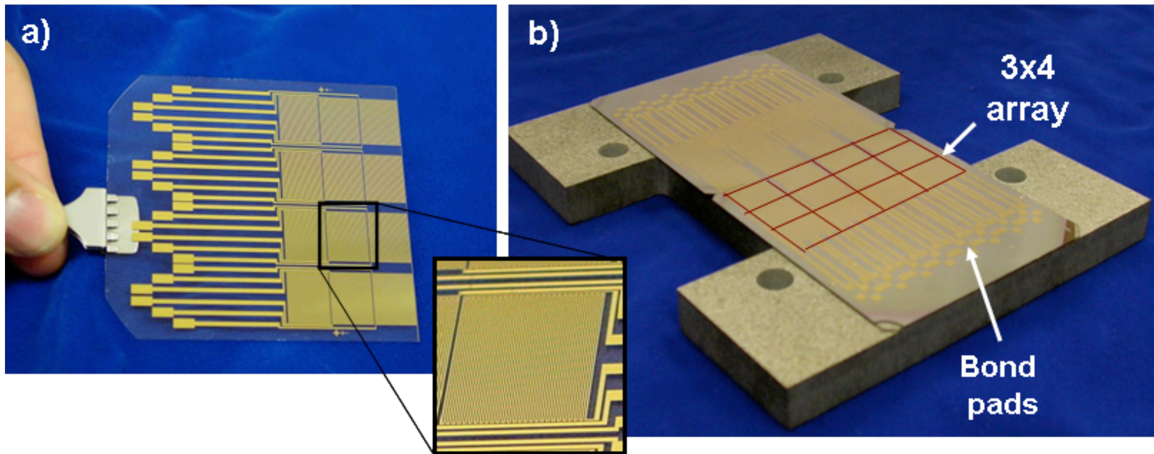


Figure 6.16: a) A heater substrate and b) two heater substrates placed on the Cogetherm™ plate.

6.3.3.4 Step 4: The Final Assembly

Figure 6.17a shows the total assembly where the copper plate and the Cogetherm™ plate sandwiched the heater and the wafer pair. Three eighths inch diameter bolts were put through the circular holes in the copper and Cogetherm™ plates in order to clamp them together. Figure 6.17a also shows wires that were soldered to bond pads on the heater substrate for providing power to the heaters as well as the PCBs which allowed interconnection to the temperature sensors on the device wafer. Figure 6.17b shows this total assembly with the 1×4×4" steel block and the 50lb steel weight which sat atop this assembly. The steel block and 50lb steel weight served three functions: i) they provided a force so that the heaters made good thermal contact with the cap wafer and so that the copper heat sink made good thermal contact with the device wafer; ii) they provided a larger thermal mass which aided in heat sinking, and iii) they provided a bond force so that the cap wafer bond rings and device wafer bond rings pressed together in order to encouraging diffusion between the cap wafer bond rings and the device wafer bond rings. For the bond force, the 50 lb weight was distributed across the 96 bond rings on the cap and device wafers. The pressure across each one of these bond rings was 2.5 MPa. (This was one of the bond pressures determined in Chapter 2 to result in strong bonds for the Au-Si eutectic process. See Section 2.6 for more detail).

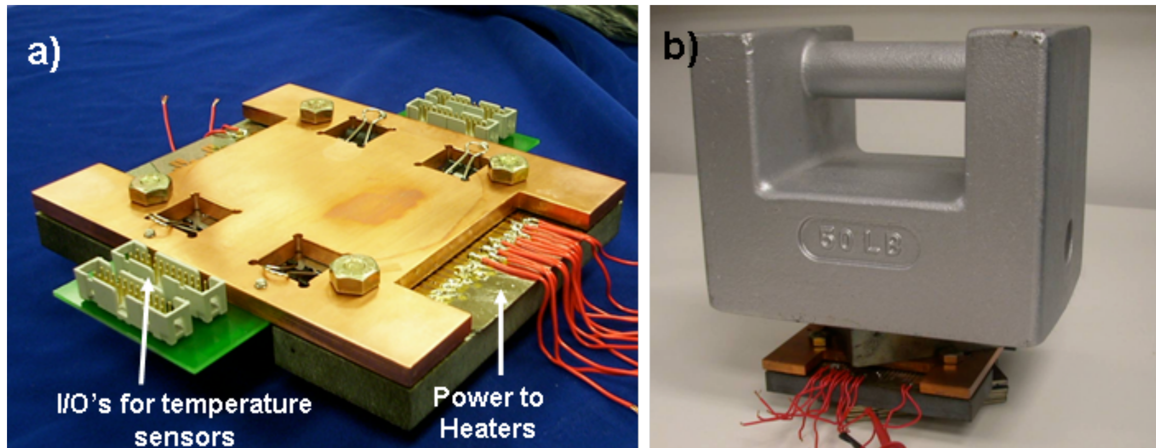


Figure 6.17: a) The entire assembly where the copper plate and the Cogetherm™ sandwiched the heaters and the wafer pair and, b) a 1× 4 × 4" steel block and a 50lb weight on top of this assembly.

Finally, Figure 6.18 shows a schematic of how the heater substrates lined up with the bond rings after the entire assembly was put together. As shown, each heater encompassed 4 bond rings so that the two 3×4 heaters encompass a total of 96 bond rings across the wafer. Furthermore, the heater substrates protruded several millimeters from the slots in the Cogetherm™ plate as could be seen in Figure 6.16b. Because the heater substrate was transparent (glass) this allowed for macro scale alignment marks (2×2mm crosses) to be aligned to the wafer pair in the alignment of the total assembly. In this way the heater substrates were aligned to the cap and device wafer to within approximately ±250 µm.

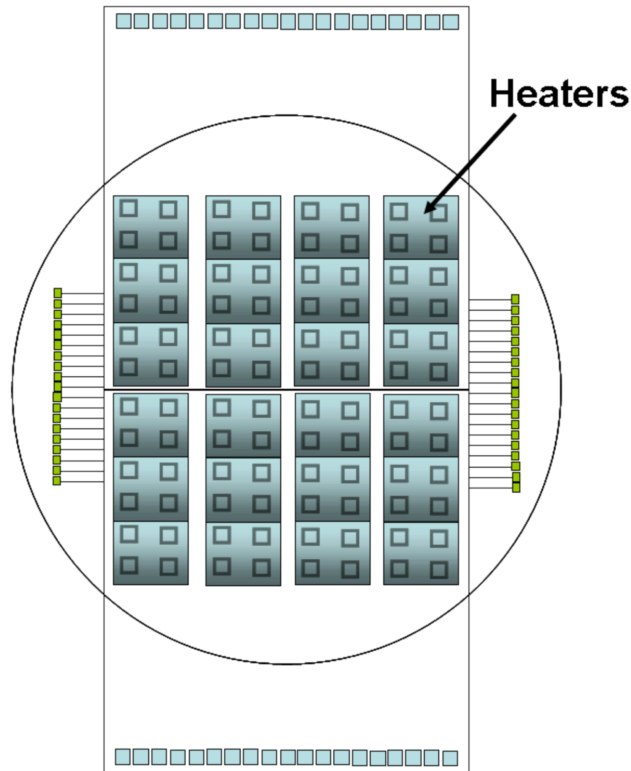


Figure 6.18: A schematic showing how the heaters lined up with the bond rings across the wafer.

6.3.4 TEMPERATURE SENSOR DESIGN & CALIBRATION

As explained previously, the temperature sensors functioned in a similar manner to the Pirani gauges described in Chapter 4. As was the case for those Pirani gauges, there were four interconnection lines that connected to each sensor in a 4-point probe configuration. Two of these interconnection lines on either side of the sensor were used for applying a current, I_R, and the other two were used for measuring the voltage drop, V_R, across the resistor. Since the current is constant from the input to the output, the resistance of the resistor, R_R, can be determined by V_R/I_R independent of the resistances of the leads running to the resistor. The resistor itself consisted of a 100/1000Å thick Cr/Pt layer that was 10 µm wide and 470 µm long. Currents of 1 mA were input using a Keithley 2400 SourceMeter and the voltages were measured using an HP 34401A multimeter. These currents were small enough so that ohmic heating was negligible. The change in temperature, ΔT, across the sensor was determined from:

$$\Delta T = \frac{1}{\xi}\frac{\Delta R}{R_{RT}} = \frac{1}{\xi}\frac{R_R - R_{RT}}{R_{RT}} \tag{6.3}$$

where ξ is the TCR of the of the resistor and R_{RT} is its resistance at room temperature (23ºC). The temperature of the temperature sensor, T_S, was therefore:

$$T_S = \frac{1}{\xi}\frac{R_R - R_{RT}}{R_{RT}} + 23^{\circ} C \tag{6.4}$$

From equation 6.4, in order to calibrate each temperature sensor, ξ and R_{RT} needed to be determined. The R_{RT} value was determined by measuring the resistance of the resistor, R_R, at 23ºC. Similar to the method for determining the TCR for the Pirani gauges in Chapter 4, R_R was next measured at 55ºC and the 75ºC, inside of an Espec Su-240 temperature chamber, and the slope of $(R_R-R_{RT})/R_{RT}$ vs. temperature was calculated in order to determine the TCR.

6.3.5 HEATER DESIGN & CALIBRATION

The heaters were fabricated on top of 4" diameter 500mm thick Pyrex glass wafers in a single mask process. A 200Å/7500Å thick Cr/Au layer was first evaporated onto the wafer in an Energet Evaporator. The wafer was then patterned and then etched using TFA Au etchant for approximately 3 minutes and then CR-14 Cr etchant for 30 seconds. Figure 6.19a shows one of the heaters which consisted of coils with 100 µm wide lines, that had 53 winds and encompassed a 10.5 x 13.3 mm^2 area. Each coil had a total length of approximately 70 cm. This geometry was chosen to achieve a heater resistance of around ~250Ω at room temperature and ~500 Ω at 427 ºC (these projected resistance were calculated using the geometry of the heaters and the book values for the resistivity of Au at 23ºC of 2.71×10^{-8} Ω/m and its resistivity at 427ºC of 6.28×10^{-8} Ω/m). These heaters were designed to allow for an input power up to 200 W at an average temperature of 427ºC. To achieve this power at 427°C (and therefore with a resistance of ~500 Ω), a current of ~0.72 A and a voltage of ~390 V were required.

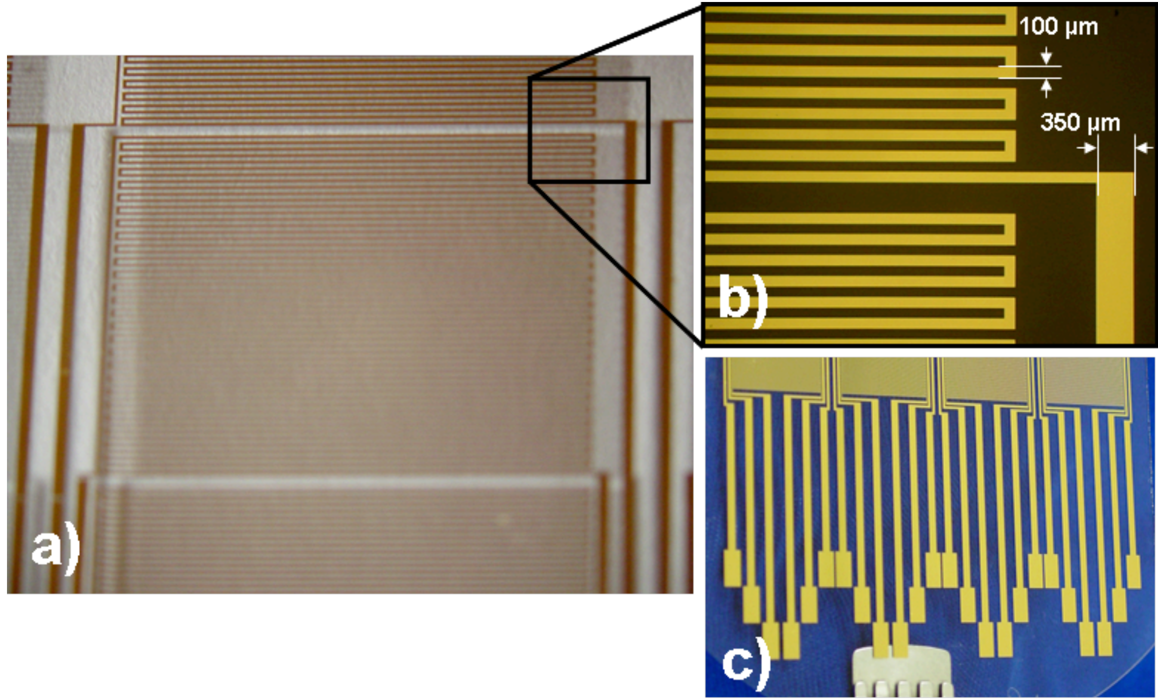


Figure 6.19: Shown is a) a heater, b) a closer look at some of 100 µm wide coils in one of these heaters and the 350 µm wide lead running from the heater, and c) the portion of the leads running to the bond ring which were 1000 µm wide.

The leads that ran to the heaters were an important part of the design. Two leads per heater ran out to bond pads at the periphery. As shown in Figure 6.19b, these leads were 350 µm wide near the heating area and as shown in Figure 6.19c, they expanded to 1000 µm wide near the bond pads. The amount of power dissipated in the heater and in the leads can be determined considering the following equation for the joule heating per unit length, δ [209]:

$$\delta = \frac{I_R^2 R_R}{\kappa_R t_R w_R l_R} = \frac{I_R^2 \rho_R}{\kappa_R t_R^2 w_R^2} \tag{6.5}$$

where κ_R is the resistor's thermal conductivity, ρ_R is the resistivity of the material and t_R, w_R and l_R are the thickness, width and length of the resistor. The joule heating per unit length, δ, is therefore proportional to the inverse square of the width of the lines. As a result, the 350 and 1000 µm segments of the leads should experience 8.1 and 1% of the joule heating per unit length, as the 100 µm wide coils.

Table 6.4 shows the lengths, widths and resistances of the heater coil and the two

different segments of the leads. Given those values Table 6.4 shows that the heater resistance accounts for 99.0 to 99.2% of the total resistance. Also shown are the percentage of the total calculated ohmic heating accounted for by the heater and each segment of the leads (from Equation 6.5)—as illustrated, the heater resistance should account for 99.7 to 99.8% of the total ohmic power generation.

Table 6.4: Calculations for the percentage of the total resistance and the power dissipated in the heater and in the leads.

Portion of heater/leads	Length	Width	Resistance	% of total Resistance	% of total Power Dissipated
Heater	700 cm	100μm	526Ω*	99.0-99.2%	99.7-99.8%
350 μm section of leads	3 to 5.2 cm	350μm	2.4-4.1Ω**	0.4-0.8%	0.1-0.2%
1000 μm section of leads	4.0 to 6.4 cm	1000μm	1.2-1.9Ω**	0.2-0.3%.	<0.1%

*Calculated at 427ºC

**Calculated at 23ºC (assuming to neglibable ohmic heating or heat spreading in the leads)

Because the resistances and ohmic power generation resulting from these leads were so small as compared to that of the heater, a simple two point probe was used for simultaneously inputting a power and measuring temperature. For temperature measurement, a voltage, V_H, was applied across the heater and the output current, I_H, was measured. Since the current is constant from the input to the output, the resistance of the heater, R_H, could be determined by V_H/I_H. The applied voltages and currents were measured by two separate HP 34401A multimeters. The temperature of the heater could then be calculated using the following equation:

$$T_S = \frac{1}{\xi}\frac{R_H - R_{RT}}{R_{RT}} + 23^\circ C \qquad (6.6)$$

It is important to note that the resistivity of each portion of the heater changes linearly with temperature. Therefore, T_s represents the average temperature across the heater for a heater with a non-uniform temperature.

From equation 6.6, in order to calibrate each heater for temperature measurement, ξ and R_{RT} needed to be determining. The R_{RT} value was determined by measuring the resistance of the resistor, R_H, at 23ºC. Similar to the method for determining the TCR for the Pirani gauges in Section 4.5 of Chapter 4, R_H was next measured at 55ºC and the

75ºC, inside of an Espec Su-240 temperature chamber, and the slope of $(R_H-R_{RT})/R_{RT}$ vs. temperature was calculated in order to determine the TCR. These R_H values were taken with a 1 mA current and were input using a Keithley 2400 SourceMeter and the voltages measured using an HP 34401A multimeter. These currents were small enough not to cause significant ohmic power generation.

6.4 RESULTS & DISCUSSION

Bond experiments were conducted between a Si cap wafer and a glass device wafer (*bond experiment #1*) and a Si cap wafer and Si device wafer with a 7 um PECVD SiO_2 (*bond experiment #2*). The *bond experiment #1* wafers were designed to facilitate a Au-Si eutectic bond at above 363ºC and the *bond experiment #2* wafers were designed to facilitate a Sn-Ag bond at above 221ºC. Using the test setup described in detail in Section 6.3, power was input into the heaters and the temperatures of the heaters and temperature sensors were monitored. The input power, and temperatures of the heaters and sensors were compared with the modeling results described in Section 6.1 (and summarized in Section 6.1.4).

6.4.1 BOND EXPERIMENT #1 (Si TO GLASS)

6.4.1.1 Heater Characterization

As was explained in Section 6.3.5 (*Heater Design & Calibration*), the heaters were designed to allow for the average temperature across the heater to be measured. Figure 6.20a shows the average measured temperature over time for one of the heaters tested in bond experiment #1 for a number of different input powers. As illustrated, the temperature quickly ramps up and begins to level off. In Figure 6.20b the temperature vs. power is graphed for two different heaters. For characterizing the temperature vs. input power for the heaters, the temperature was measured after holding a specified power across the heater for 10 seconds. As illustrated in Figure 6.20 the temperature vs. power behavior for these two heaters are similar and they both demonstrate very linear behavior with an average slope of 3.5 K/W. This is comparable to the temperature vs. power behavior predicted by the model in Section 6.1 (and summarized in Table 6.3) of 3.9

K/W.

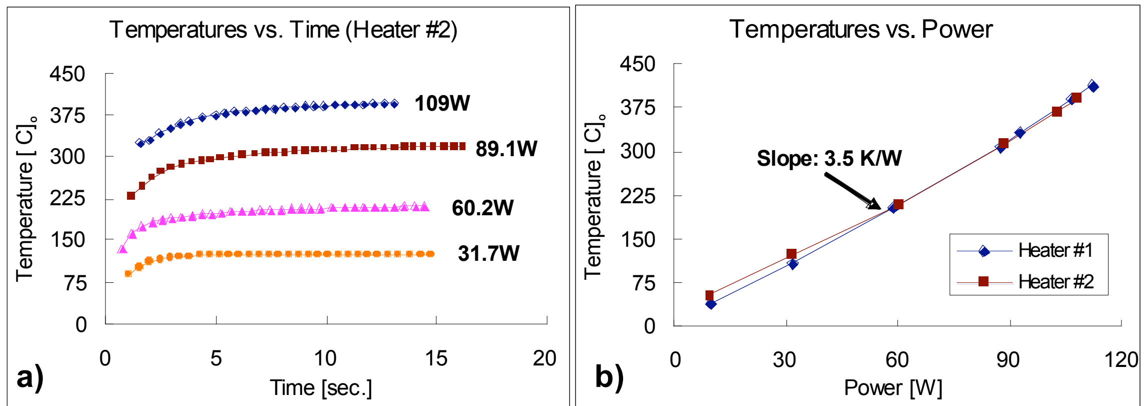


Figure 6.20: a) The average measured temperature across one of the heaters for different powers and b) the temperature vs. power (after holding power for 10 seconds) for two different heaters that were tested in bond experiment #1.

Figure 6.21a shows the temperature vs. power behavior of two heaters which failed—resulting in an open circuit. In each case, after inspection, a portion of the heater was observed to have burnt. As illustrated, heater #1 failed after holding a power of 112 W for 16 seconds and heater #2 failed after holding a power of 109 W for 955 seconds. The measured temperatures across these heaters at failure were 430ºC and 440ºC respectively. Considering the modeling for *bond experiment #1*, there should be a large temperature gradient across the heater. Figure 6.21b shows the modeled temperature profile for the case which was presented in Section 6.1.3.1 where there was a heater input power of 107 W (26.8 W/bond ring), resulting in an average heater temperature of 442ºC and a maximum temperature of 501ºC. Considering the average temperatures across heaters #1 and #2 at failure (of 430ºC and 440ºC), the model therefore predicts that heaters #1 and #2 should have had a maximum temperature near 500ºC.

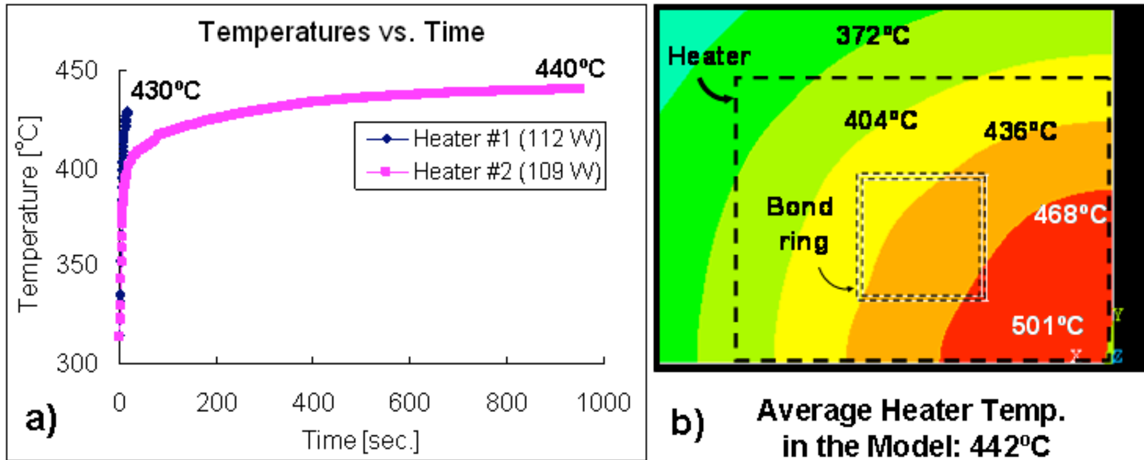


Figure 6.21: a) The temperature vs. time for two heaters that failed with applied powers of 112 and 109 W at temperatures of 430ºC and 440ºC respectively and, b) the case which was modeled in Section 6.1.3.1 where there was an average temperature of 442ºC for *bond experiment #1*.

6.4.1.2 Temperature Sensor Measurement

As was explained in Section 6.3 (*Test Setup Design*), temperature sensors were fabricated so that they would be located underneath the bond ring and at 250 and 750 µm from the edge of the bond ring. In *bond experiment #1* the device and cap wafer were misaligned by 100 µm along the vertical axis. Figure 6.22 shows a view from underneath the glass device wafer for one of the bond rings encompassed by heater #2. As shown in Figure 6.22, this resulted in the three sensors being 50µm (S1 sensor), 150µm (S2 sensor) and 750µm (S3 sensor) from the bond ring during the bonding experiments.

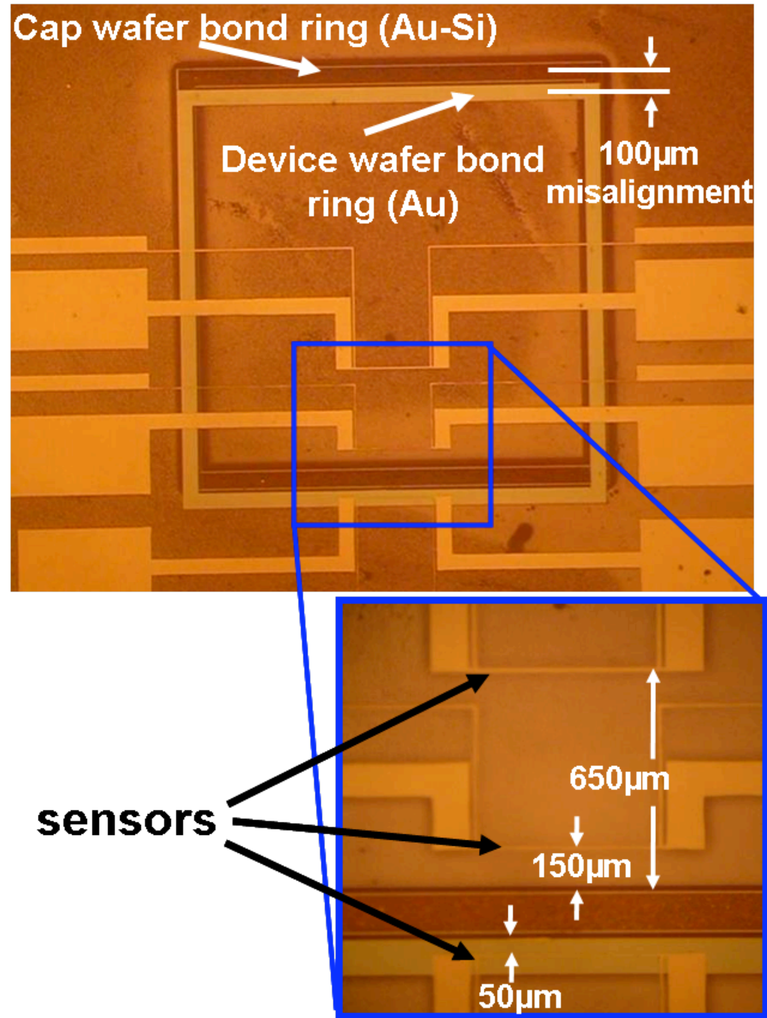


Figure 6.22: The aligned cap and device wafers as seen through the backside of the glass device wafer in *bond experiment #1*. As illustrated, these bond rings were misaligned vertically by 100 µm resulting in the temperature sensors being 50, 150 and 650 µm from the edge of the bond ring.

Figure 6.23a shows a plot of the modeled temperature distribution across the bond ring which was presented in Section 6.1.3.1. Instead of showing specific temperatures, the temperatures in Figure 6.23 are listed as a percentage of the minimum bond ring temperature, R_{BR}. Figure 6.23a shows the locations of each of the sensors schematically and the R_{BR} values modeled at each of these locations.

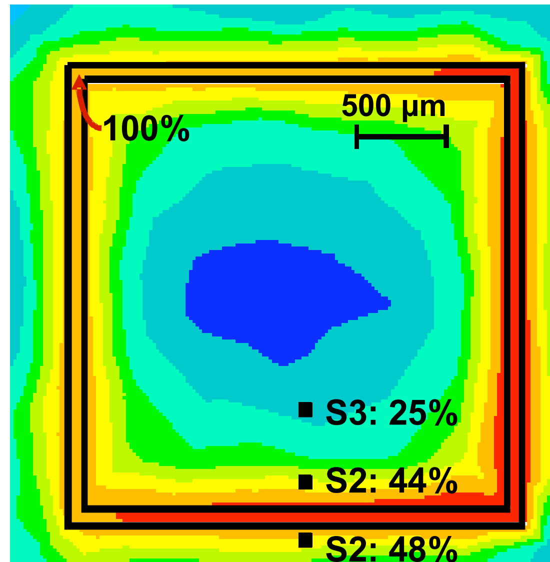


Figure 6.23: The modeled temperature profile showing the temperatures relative to the minimum bond ring temperatures (R_{BR}) at different distances from the bond ring for *bond experiment #1*.

Figure 6.24 shows a plot of the average heater temperatures, T_{Have}, along with the temperatures measured at the S1, S2 and S3 temperature sensors for the misaligned bond ring that was shown in Figure 6.22. In order to compare the modeling results with the measured results, the average heater temperature, T_{Have}, was assumed to have an R_{BR} of 111% as was the case in the model (In other words, the average heater temperature, T_{Have}, was assumed to be 1.11 times the minimum bond ring temperature, T_{Bmin}. This assumption was made because T_{Bmin} could not be directly measured). This given, the dashed and dotted lines in Figure 6.24 show the modeled data for the minimum bond ring temperature, T_{Bmin}, and the modeled data at each of the temperature sensor locations. Table 6.5 summarizes these results comparing the modeled R_{BR} values with the average measured R_{BR} values at each of the temperature sensors. As illustrated, for a given heater temperature the model does a good job of predicting temperatures near the bond ring. Furthermore, *bond experiment #1* seems to indicate good thermal isolation inside of the bond ring with the temperature 650µm from the bond ring measured at 23% of the minimum bond ring temperature.

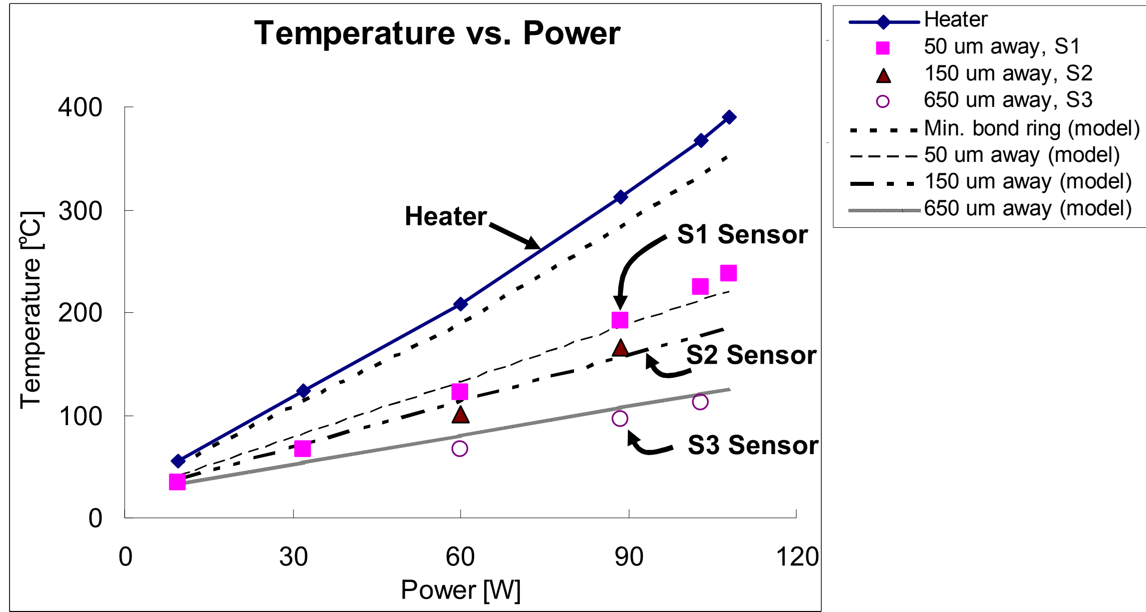


Figure 6.24: A comparison of the measured heater temperature and the temperatures at different distances from the bond ring to the modeling results for *bond experiment #1*.

Table 6.5: A comparison of the modeled and measured temperatures relative to the minimum bond ring temperatures (R_{BR}) at different distances from the bond ring.

Location	Modeled R_{BR}	Measured R_{BR}
Heater (Average Temp.), T_{Have}	111%	111%*
Bond Ring (Minimum Temperature), T_{Bmin}	100%	-
Bond Ring (S1)	48%	53%**
250 µm Away (S2)	40%	41%**
750 µm Away (S3)	25%	23%**

*The average heater temperature was assumed to be at 111% of the minimum bond ring temperature as in the model.

**The average of the R_{BR} values measured at each temperature sensor assuming that T_{Have} was 111% of T_{Bmin}.

Finally, Figure 6.25 shows the heater temperature overtime along with the temperature at each of the temperature sensors. In Figure 6.25, a 89 W power was held for around 15 seconds. The temperatures inside of the bond ring (at 250µm and 750µm from the bond ring) seemed to maintain their R_{BR} values (their temperatures relative to the bond ring temperature) for the short duration of the temperature ramping tests.

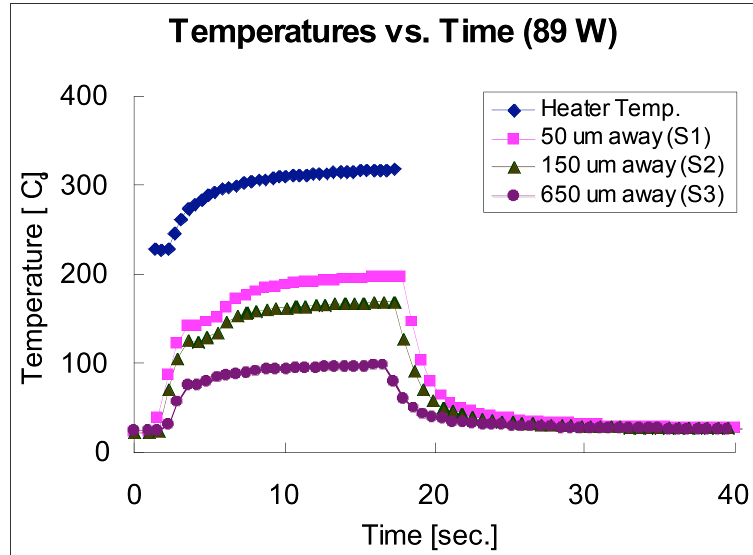


Figure 6.25: The temperature over time for one of the temperature ramping tests from bond experiment #1 showing the temperatures at each one of the temperature sensors.

6.4.1.3 Au-Si Eutectic Bonding Using Localized Heating

As was discussed in the Section 6.2 (*Wafer Fabrication for Bond Experiments*), for *bond experiment #1*, Au bond rings were fabricated on the cap wafer to facilitate a Au-Si Eutectic bond to a Au film on the device wafer. After the temperature ramping experiments described in the previous sections, the cap and device wafer were pulled apart and the bond rings were inspected. As was shown in Figure 6.21a of Section 6.4.1.1, heater #2 achieved its maximum average temperature of 440ºC when it was held at a power of 109 W for around 15 minutes. Figure 6.26a shows the modeled temperature profile across this bond ring, assuming a heater temperature of 440ºC. Figure 6.26b shows a picture of the device wafers substrate after the wafers were pulled apart for one of the bond rings encompassed by heater #2. As shown in Figure 6.26a, for an average applied temperature of 440ºC, according to the model, the entire bond ring should be above 398ºC—well above the Au-Si eutectic temperature. As shown in Figure 6.26b this resulted in a bond where the Au-Si eutectic bond was strong enough to tear Si from the cap wafer so that it adhered to the device wafer after the wafers were pulled apart. (It is important to remember from Figure 6.22 in Section 6.4.1.2 that the cap and device wafers were misaligned along the vertical axis so that the bond rings only made contact on the left and right edges of the bond ring). This seems to indicate that this

bonding method could be applied for Au-Si eutectic bonding.

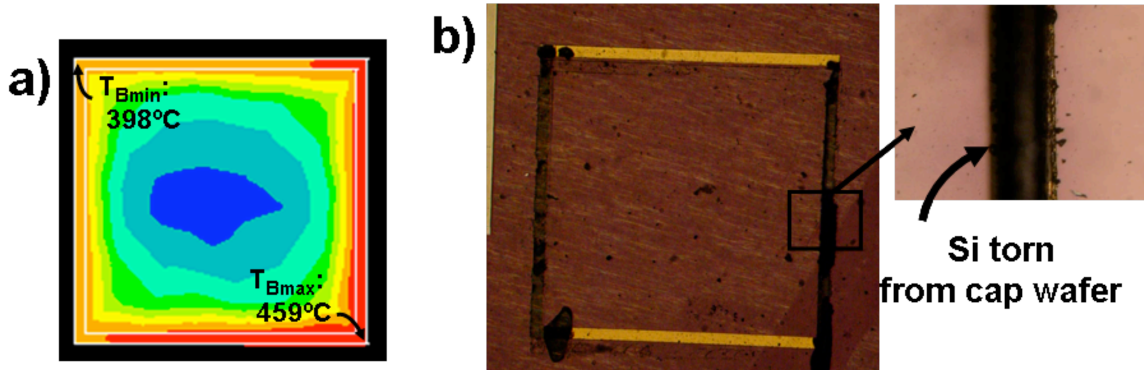


Figure 6.26: a) Modeling results for the case where the average heater temperature is 440°C and b) one of the bond rings under heater #2 after the cap and device wafers were pride apart after the bond experiments.

6.4.2 BOND EXPERIMENT #2 (Si TO Si WITH A 7 μm SiO_2 LAYER)

6.4.2.1 Heater Characterization

Figure 6.27a shows the average measured temperature over time for one of the heaters tested in *bond experiment #2* for a number of different input powers. Similar to the experiment #1 bond tests, when power was applied to the heater, the temperature quickly ramped up and started to level off. For applied powers of greater than 100 W in some initial heater tests for *bond experiment #2* bonds, the heaters appeared to be damaged either in the initial heating step or once power was cut and rapid cooling took place. In those experiments, the glass heater substrate was observed to have cracked. It was presumed that rapid heating and/cooling caused large strains in the glass due its temperature coefficient of expansion (TCE), causing large stresses. To avoid damaging the heaters in this way, as shown in Figure 6.27a, at powers greater than 100W the power was slowly ramped up and slowly ramped down.

In Figure 6.27b the temperature vs. power is plotted for four different heaters. For characterizing the temperature vs. input power for the heaters, the temperature was measured after holding a specified power across the heater for 10 seconds, as was the case in *bond experiment #1* tests. As illustrated, the temperature vs. power behaviors for each of the heaters are similar to each other and demonstrate very linear behavior with

power behavior predicted by the model in Section 6.1.3.3 (and summarized in Table 6.3). The source of this discrepancy is not evident and indicates that more heat his pulled away from the heater in the model as compared to the actual test setup. One possible explanation for this is that there was not good thermal contact between the bond rings on the cap and device wafers because of the roughness and/or non-uniformity in the electroplated Ni/Sn layers. Such bad thermal contact would make the heater more thermally isolated from the heat sink, allowing it to heat up with smaller amounts of power.

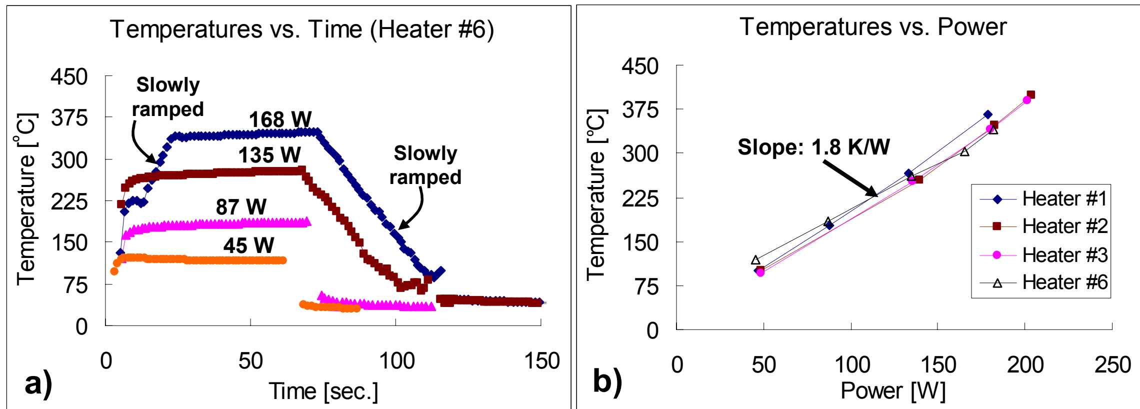


Figure 6.27: a) The average measured temperature across one of the heaters for different powers and b) the temperature vs. power (after holding power for 10 seconds) for four different heaters that were tested for *bond experiment #2*.

Figure 6.28a shows the temperature vs. power behavior of three heaters which failed—resulting in an open circuit. In each case, after inspection, a portion of the heater was observed to have burnt. As illustrated, heaters #1 and #7 failed after holding powers of 181 and 200 W for 15 and 21 seconds with maximum temperatures of 374 and 347 ºC respectively. Heater #5 on the other hand survived an input power of 200W for 207 seconds and failed at a temperature of 416ºC. Figure 6.28b shows two other heaters which were held at 200W for around 50 seconds each without failure. Considering the modeling for *bond experiment #2*, there should be a large temperature gradient across the heater. Figure 6.28c shows the modeled temperature profile across the heater for a bond between a Si wafer and a Si wafer with a 7 µm SiO_2 layer presented Section 6.1.3.3. In the modeled case shown in Figure 6.28c a power was applied so that the average heater temperature, T_{Have}, was 400ºC. In this case the maximum heater temperature was 556ºC.

temperature, T_{Have}, was 400ºC. In this case the maximum heater temperature was 556ºC. Assuming that during testing the heater had a similar temperature profile, the five heaters tested in Figure 6.28a and Figure 6.28b would have seen temperatures ranging from 490ºC to 565ºC.

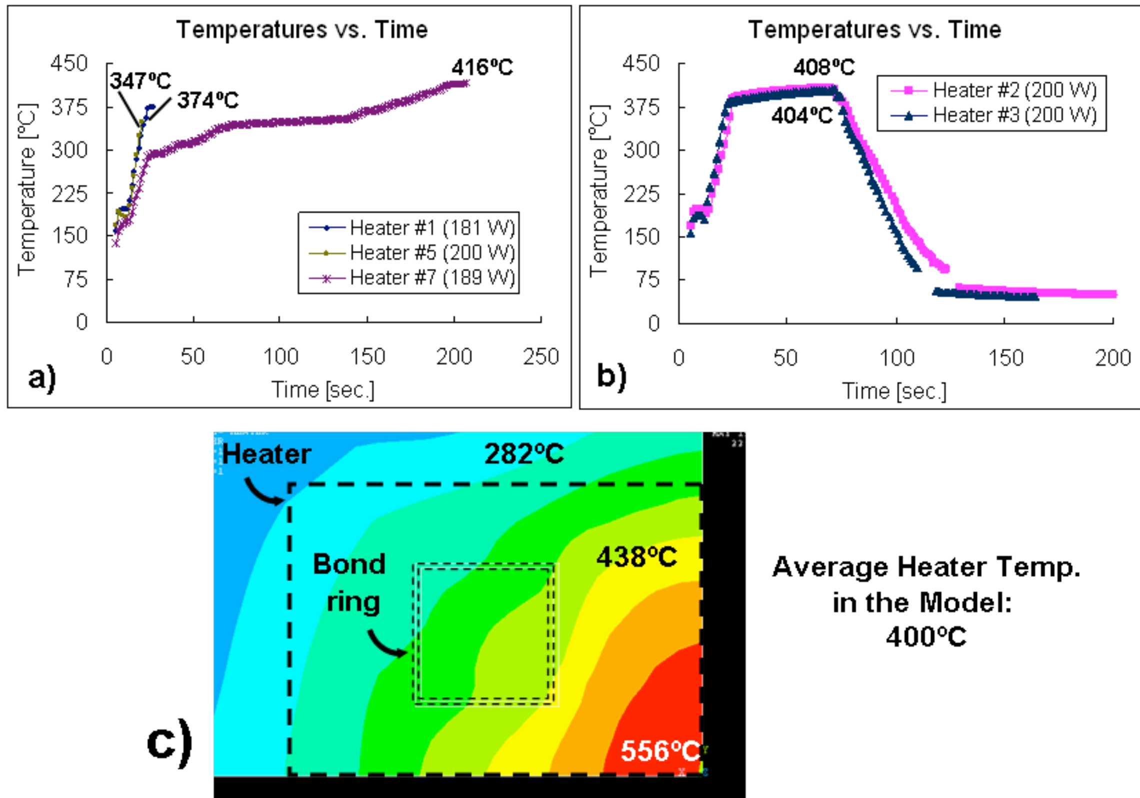


Figure 6.28: a) The temperature vs. time for three heaters that failed with applied powers of 181, 200 W and 189 W at temperatures of 374, 357 and 416ºC respectively, b) two heaters that did not fail with applied powers of 200W and, c) a plot of the modeled case from Section 6.1.3.3 with an assumed average heater temperature was 400ºC.

6.4.2.2 Temperature Sensor Measurement

In bond experiment #2, the cap and device wafers were aligned with no observable misalignment so that the S1, S2 and S3 sensors were located underneath the bond ring and at 250 and 750 µm from the bond ring.

Figure 6.29a shows a plot of the modeled temperature distribution across the bond ring which was presented in Section 6.1.3.1. Instead of showing specific temperatures, the temperatures in Figure 6.29 are listed as a percentage of the minimum bond ring temperature, R_{BR}. Figure 6.29a shows the locations of each of the sensors schematically and the R_{BR} values modeled at each of these locations.

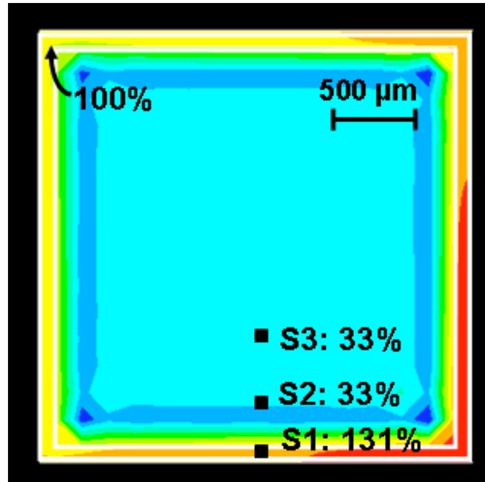


Figure 6.29: The modeled temperature profile showing the temperatures relative to the minimum bond ring temperatures (R_{BR}) at different distances from the bond ring for *bond experiment #2*.

Figure 6.30 shows a plot of the average heater temperatures, $T_{Have,}$ along with the temperatures measured at the S1, S2 and S3 temperature sensors for one of the bond rings encompassed by heater #6. In this plot, in order to compare the modeling results with the measured results, the average heater temperature, T_{Have}, was assumed to have an R_{BR} of 157% as was the case in the model. (In other words, the average heater temperature, T_{Have}, was assumed to be 1.57 times the minimum bond ring temperature, T_{Bmin}. This assumption was made because T_{Bmin} could not be directly measured). This given, the dashed and shaded lines in Figure 6.24 show the modeled data for each of the temperature sensors.

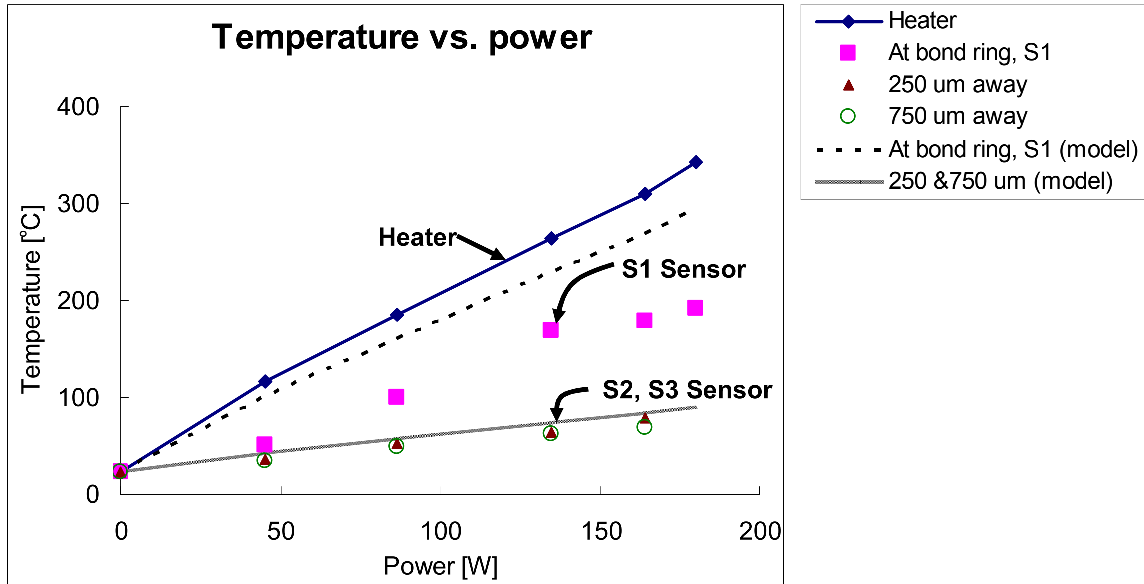


Figure 6.30: A comparison of the measured heater temperature and the temperatures at different distances from the bond ring to the modeling results for the experiment #2 bond tests.

As illustrated in Figure 6.30, for a given heater temperature, the model does not accurately predict the temperature at the bond ring where the S1 sensor is located. Once again, a possible explanation for this, is that there may not have been good thermal contact between the Ni/Sn/Ag on cap wafer and the Ni/Sn on the device wafer because of a high surface roughness (as was also mentioned in regards to the discrepancy between the measured and modeled heater temperatures in the previous section). This bad thermal contact could cause a larger than expected temperature drop at the bond ring interface resulting in a lower temperature just under the bond ring where that temperature sensor was located. Regardless, it is evident that the measured heater temperature was not a good indicator of the minimum bond ring temperature, $T_{BRM,}$ since it did not accurately predict the temperature at S1. In order to better gauge the amount of thermal isolation inside of the bond ring, in Table 6.6, R_{BR} is estimated assuming that the temperature at S1, is 131% of the minimum bond ring temperature, as is the case in the model. In other words, instead of using the heater temperature for comparing the bond results to the model, the temperature at S1 is used to compare the measured results to the modeled results. As shown in Table 6.6, assuming that the temperature at S1 accurately predicts the minimum bond ring temperature, the measured R_{BR} values of 42% and 39% at 250μm

and 750μm from the bond ring are higher than those predicted by the model. Even so, this does represent a reasonable amount of thermal isolation inside of the bond ring.

Table 6.6: A comparison of the modeled and measured temperatures relative to the minimum bond ring temperatures (R_{BR}) at different distances from the bond ring.

Location	Modeled R_{BR}	Measured R_{BR}
Bond Ring (Minimum Temp.)	100%	-
Bond Ring (S1)	131%	131%*
250 μm Away (S2)	33%	42%**
750 μm Away (S3)	33%	39%**

*The measured bond ring temperature at S1 was assumed to be at 131% of the minimum bond ring temperature as in the model.
** The average of the R_{BR} values measured at each temperature sensor assuming that T_{S1} was 131% of T_{Bmin}.

Finally, Figure 6.31 shows the heater temperature overtime along with the temperature at each of the temperature sensors. In Figure 6.31 a 165 W power was held for around 60 seconds. As in bond experiment #1, the temperatures inside of the bond ring (at 250μm and 750μm from the bond ring) seemed to maintain their R_{BR} values (their temperatures relative to the bond ring temperature) for the short duration of the temperature ramping tests.

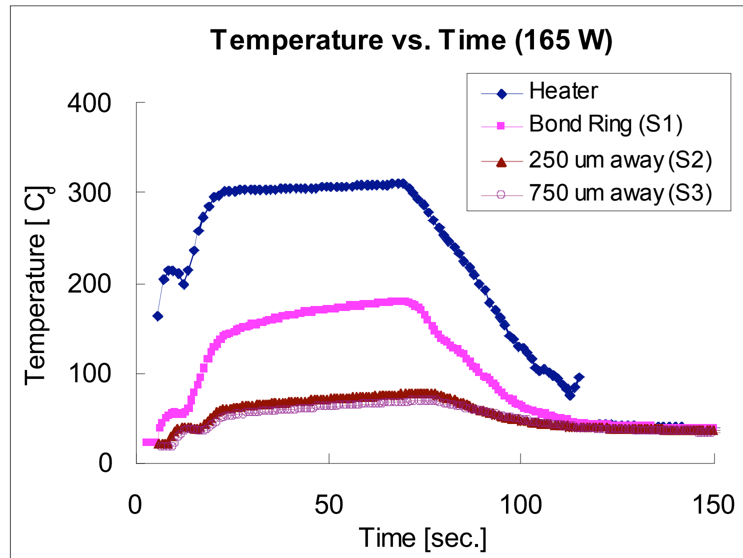


Figure 6.31: The temperature over time for one of the temperature ramping tests from bond experiment #2 showing the temperatures at each one of the temperature sensors.

6.4.2.3 Sn-Ag Solder Bonding Using Localized Heating

As was discussed in Section 6.2 (*Wafer Fabrication for Bond Experiments*), for bond experiment #2, Ni/Sn/Ag bond rings were fabricated on the cap wafer to facilitate a Sn-Ag solder bond to a Ni/Sn film on the device wafer. After the temperature ramping experiments described in the previous sections, the cap and device wafers were pulled apart and the bond rings were inspected. Unlike *bond experiment #1*, strong enough bonds were not achieved to observe tearing of the Si from the cap wafer and subsequent adhesion to the device wafer. On the other hand, Sn-Ag intermixing was observed. Figure 6.32a shows one of the Ni/Ag bond rings on the device wafer which was not heated up and Figure 6.32b shows one of the bond rings from heater #3 which was. As illustrated the film in Figure 6.32b has become darker seeming to indicate Sn-Ag intermixing. Furthermore, the rounded bubbles give some indication that a liquid eutectic was formed.

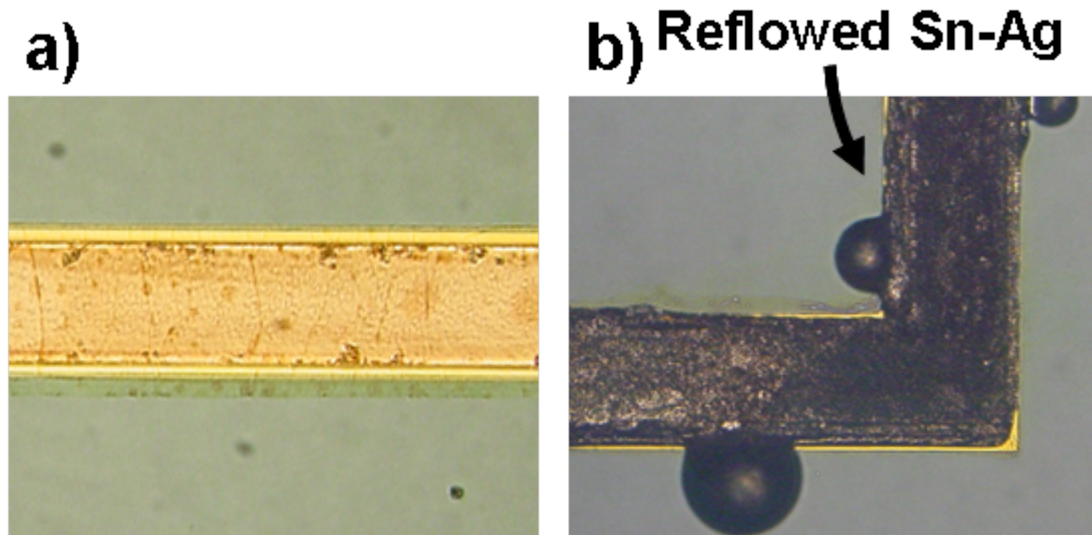


Figure 6.32: a) A Ni/Sn film on the device wafer which was not heated up, showing no evidence of Sn-Ag intermixing, and b) another bond ring which has darkened and flowed seeming to indicate Sn-Ag intermixing and viscous flow.

Figure 6.33 shows the modeled temperature profile across a bond ring which was encompassed by heater #6 and one encompassed by heater #3 (for the highest heater temperature that was applied) and pictures of the device wafer substrates after the wafers were pulled apart for these bond rings. For heater #6, a power of 180 W was applied for around 1 minute with a maximum heater temperature of 348ºC. For heater #3 a power of

200 W was applied for 1 minute with a maximum heater temperature of 404ºC (as was shown in Figure 6.26a). For heater #6, the maximum temperature measured at the bond ring, T_{S1}, was 198ºC. Given the R_{BR} values that were shown in Figure 6.29, this T_{S1} temperature was used to estimate the temperature profile across the bond ring as shown in Figure 6.33a. As illustrated, the model predicts that none of the bond ring should be over the melting temperature of Sn-Ag solder of 221ºC. Even so, in Figure 6.33b, there does appear to be Ag-Sn intermixing. The darker areas in the lower right hand side of the bond ring seem to indicate more intermixing where the model predicts higher temperatures.

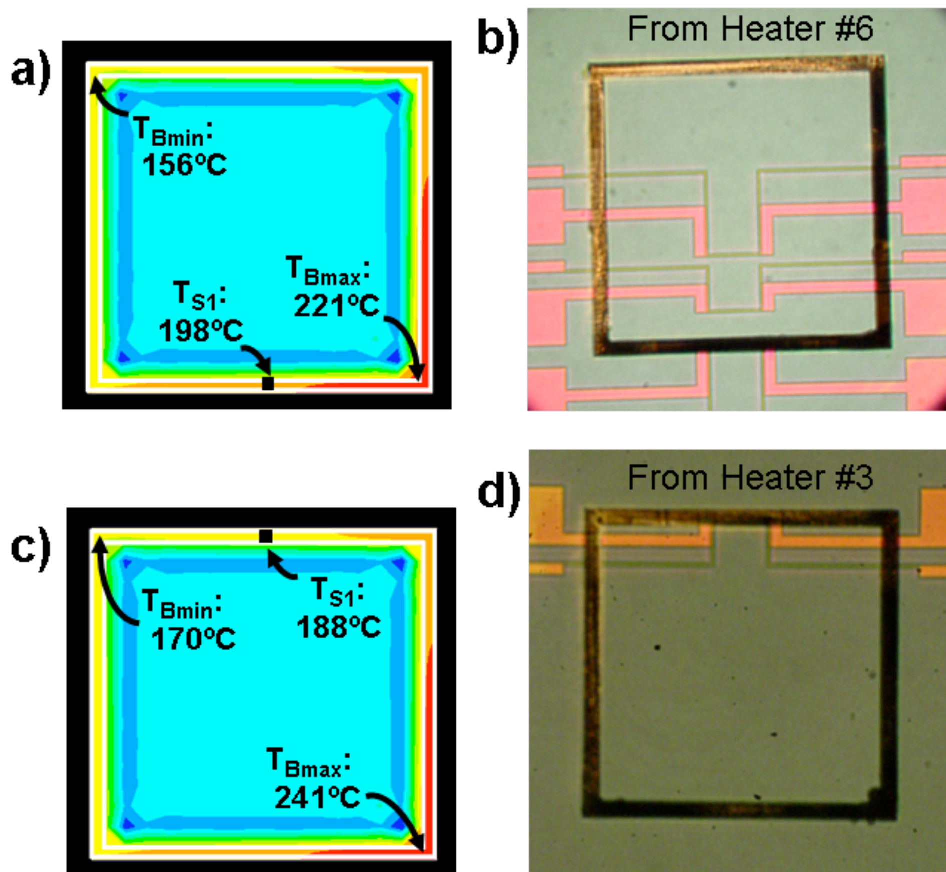


Figure 6.33: a) The modeled temperature profile for the bond rings under heater #6 for the maximum applied temperature, b) a bond which was encompassed by heater #6 after the bond tests, c) the modeled temperature profile for the bond rings under heater #3 for the maximum applied temperature and d) a bond which was encompassed by heater #3 after the bond tests.

For heater #3, the maximum temperature measured at the bond ring was 188ºC and as

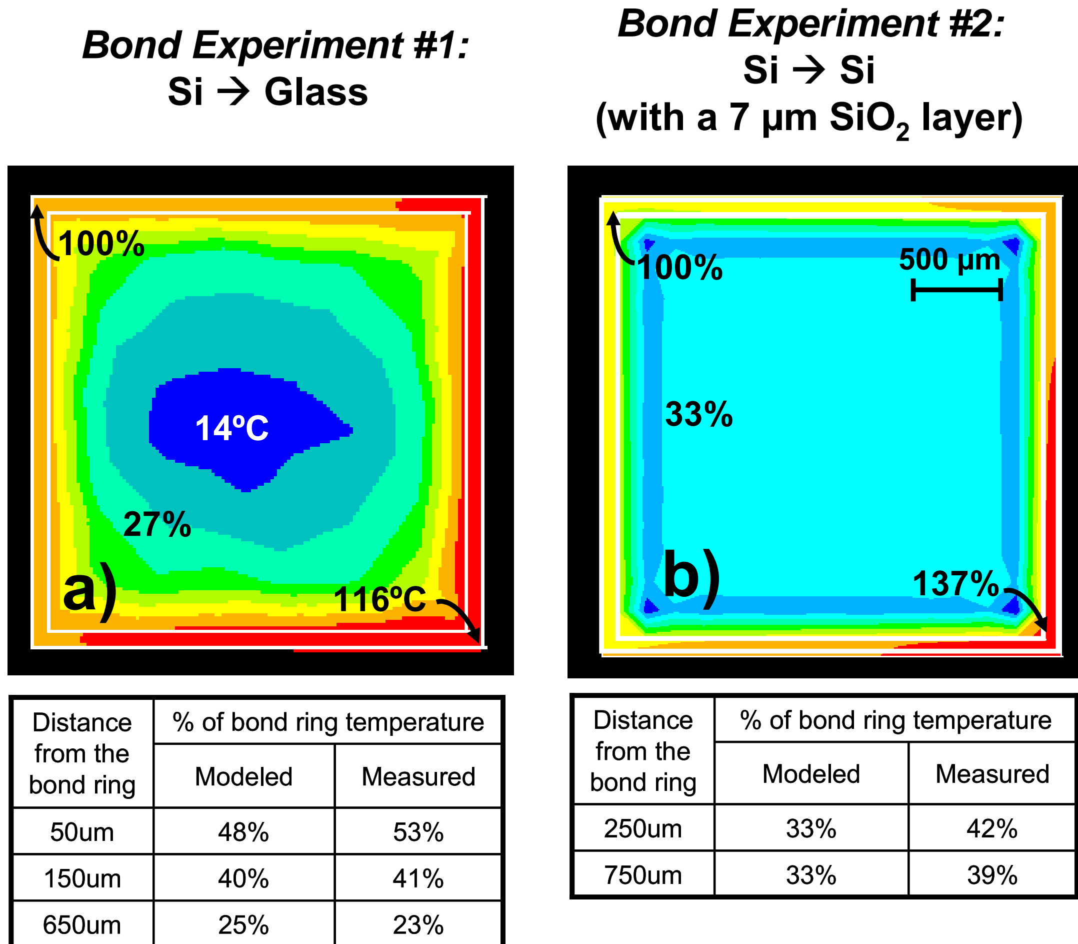
supposed to the heater #6, this sensor was located at the top of the bond ring—on the edge farthest from the center of the heater. Once again, the sensor temperature, T_{S1}, was used as a reference for determining the temperature profile shown in Figure 6.33c. As illustrated, the model predicts that the lower right hand corner should have gone above the melting point of Sn-Ag solder which is 221ºC. Figure 6.33d shows a bond ring which was encompassed by heater #3 where some flow seems to have occurred—Figure 6.32b in fact showed a close up view of the lower right hand corner. This evidence of viscous flow may indicate that eutectic solder did in fact form at above its melting temperature.

6.5 CONCLUSION

A new method for localized heating of a bond region has been developed and tested for bonding two wafers, while maintaining a low temperature where sensitive devices are located. Using a 3D ANSYS thermal model, the needed input power and temperature distributions were predicted for silicon to glass and silicon to silicon bonds. Integrated temperature sensors were used in this study to measure temperatures at different distances from the bond region in order verify the model and the bonding technique.

Figure 6.34 summarizes some of the modeling and test results for the two sets of experiments that were conducted: i) a bond between a Si and glass substrate (*bond experiment #1*) and ii) a bond between a Si wafer and a Si wafer with a 7µm thick SiO_2 layer (*bond experiment #2*). These models and bond experiments were conducted in order to gauge the effectiveness of the *differential localized heating* technique. Figure 6.34a and Figure 6.34b show plots for the modeled temperature profiles for bonds conducted in bond experiment #1 and #2. Each of these plots demonstrate a reasonable amount of temperature drop inside of the bond ring. The tables underneath each plot compare the modeling results with the test results. For bonds to glass, in *bond experiment #1*, very good agreement is shown between the modeling and test results with differences in the temperature relative to the minimum bond ring temperature of less than 3%. On the other hand, for bonds to a Si wafer with a 7 µm SiO_2 layer, in *bond experiment #2*, a 6-9% higher temperature relative to the minimum bond ring temperature was measured as compared to the modeling results. Even so, good thermal isolation inside of the bond ring was observed. In fact, the temperature was observed to be 23% of

the bond ring temperature at 650 μm from the bond ring in bond experiment #1, and to be 41% of the bond ring temperature at 250 μm from the bond ring in bond experiment #2. Furthermore, a Au-Si eutectic bond was successfully implemented using *differential localized heating* for a Si to glass bond in bond experiment #1.



Distance from the bond ring	% of bond ring temperature	
	Modeled	Measured
50um	48%	53%
150um	40%	41%
650um	25%	23%

Distance from the bond ring	% of bond ring temperature	
	Modeled	Measured
250um	33%	42%
750um	33%	39%

Figure 6.34: a plot of the temperature profile modeled for a) bond experiment #1 and b) bond experiment #2. Underneath each plot is a comparison of the modeled and measured relative temperatures at different distances from the bond ring.

6.6 Considerations for Application of Differential Localized Heating

This section provides parametric analysis to determine the effects of bond ring width and the device wafer thickness on differential localized heating. An analysis on the stress that results from differential localized heating is also presented. The ANSYS model presented in Section 6.1.3 was made specifically to predict the temperature distribution

across bonded wafers in the bond tests presented in Section 6.4. In these bond tests, bond rings were heated up 4 at a time instead of heating all of the bond rings across the wafer at once. For simplicity, in the final application of differential localized heating it would be advantageous to apply this bonding method on a full wafer of bond rings all at once. Therefore, for analysis of the application of differential localized heating, a "full wafer bond model" is presented in order to conduct parametric analysis.

Section 6.6.1 first presents the structure of the "full wafer bond model". Section 6.6.2 then presents parametric analysis for the Si to glass bond and for the Si to Si bond with a 7 μm thick SiO_2 layer. Finally, Section 6.6.3 presents analysis on the stresses induced from backside localized heating.

6.6.1 THE FULL WAFER MODEL

In the "full wafer bond model," shown in Figure 6.35, a single bond ring was modeled with a heater that encompassed the span of the model. This heater area, 5.4×8.1 mm^2, was the same area as a single die from the test setup. All 4 lateral sides of this model had adiabatic (symmetric) boundary conditions—thus assuming that bond rings in all directions are being heated with the same amount of input power. As a result, the heat flowed in the z-axis, through the bond ring and did not flow laterally in the x or y directions.

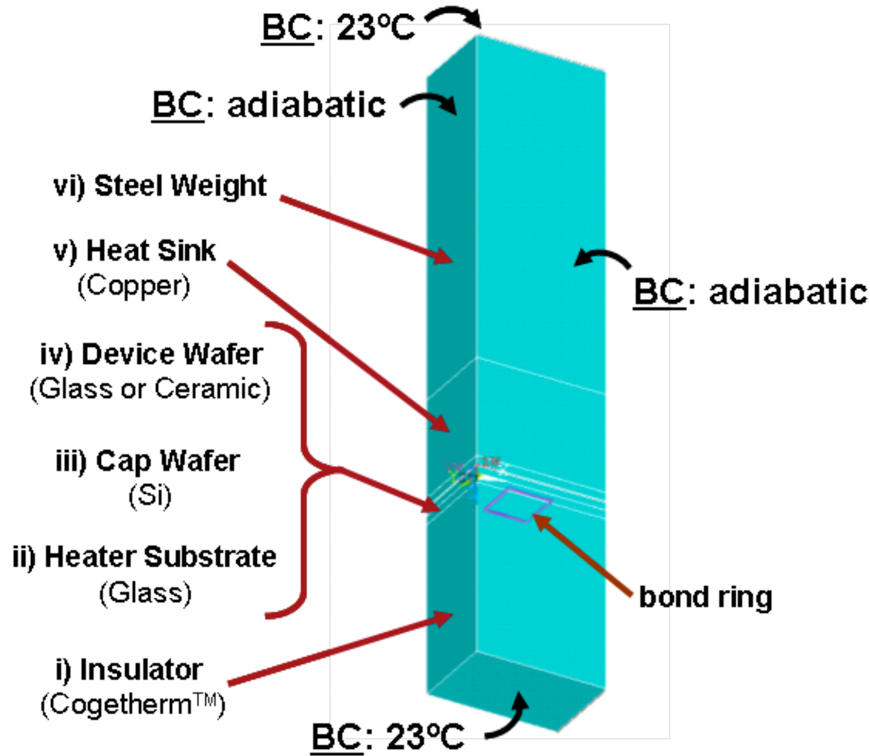
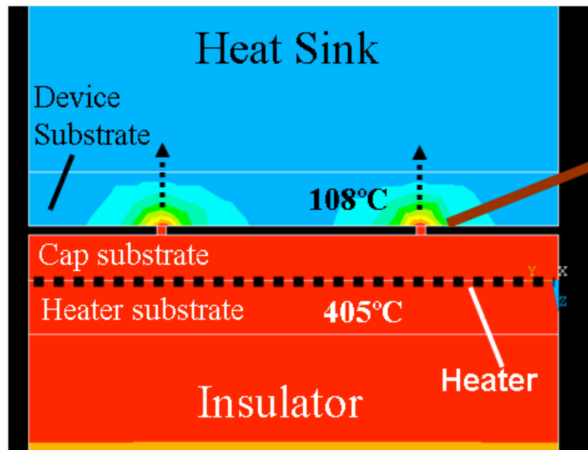


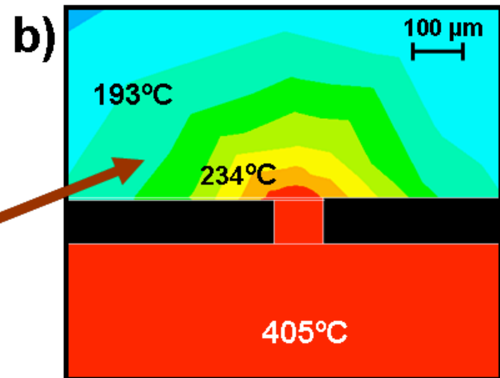
Figure 6.35: The structure of the model used for "full wafer model."

In simulating the model, a steady state solution was found by applying a uniform power density across the 0.75 µm thick heater, while the top of the steel plate and the bottom of the insulator plate were held at 23ºC. As was explained in Section 6.1.1, this boundary condition was chosen assuming that their was a large enough thermal mass that far a way from the bond ring the temperature remains at 23 ºC. The material used for the device substrate in this model was glass.

Figure 6.36 shows the case where an input power of 6 Watts is applied. In Figure 6.36 slices of the model have been taken vertically across the bond ring to show a cross-sectional view (Figure 6.36a and Figure 6.36b) and laterally through the bond ring (Figure 6.36c). In the cross-sectional view, the location of the heater substrate, cap wafer, device wafer and heat sink are labeled. Also, the location of the heater is denoted by a dotted line. A zoomed in view of the cross-section in Figure 6.36b shows a dramatic temperature drop in the device wafer, just above the bond ring. Furthermore, Figure 6.36c shows that a uniform temperature of 400ºC was achieved at the bond ring. On the other hand, inside of the bond ring the temperature drops significantly. In fact, at 500 µm

away from the bond ring the temperature was only 134ºC and at the center of the bond ring the temperature was around 98ºC.





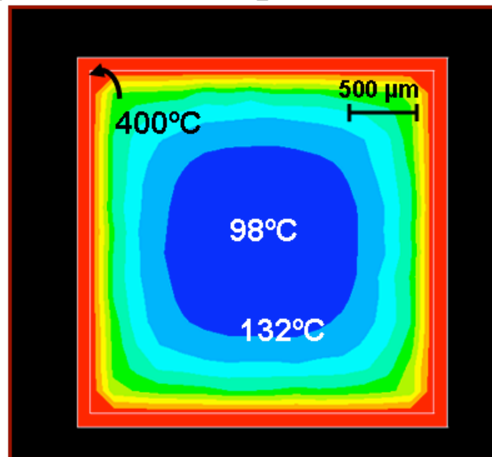


Figure 6.36: Results from the “full wafer bond model,” showing a) a cross-section view showing how the heat flows into the heat sink and b) a closer look at the cross-section of the bond ring and c) the heat distribution across the bond ring and inside of the bond ring.

6.6.2 PARAMETRIC ANALYSIS

Two parameters were analyzed to determine their effects on the effectiveness of localized heating: 1) the width of the bond ring and 2) the thickness of the device wafer substrate. In the nominal case described in Section 6.6.1 a 100 µm wide bond ring (on

the cap wafer) and a standard 550µm thick device wafer were used. In this section, 50, 200 and 300 µm wide bond rings and 100, 250 and 1000 µm thick bond rings are also modeled and analyzed.

6.6.2.1 The Si to Glass Bond

Figure 6.37 shows the results of parametric analysis for a Si to glass bond where the temperature at different distances from the center of the bond ring are graphed for changes in the bond ring width and the device wafer thickness. In each case enough power was input so that the bond ring heated up to 400ºC. As illustrated in Figure 6.37a, increasing the bond ring width causes an increase in the temperature inside of the bond ring. The dotted line shows where the temperature was at 60% of the bond ring temperature (which is around 250ºC). Assuming that the device being packaged requires a temperature under 250ºC, Table 6.7 lists the required distance from the bond ring and the resultant increase in package size in both dimensions (along the x and y planar axis). As illustrated, the over all increase in package size due to packaging increases from 501 µm with a 100 µm bond width to 686 and 895 µm going to 200 or 300 µm (it should be noted that a significant part of this increase is due the increased area that the bond ring itself takes up). As also shown, there is a slight increase in the necessary input power as well when increasing the bond ring width.

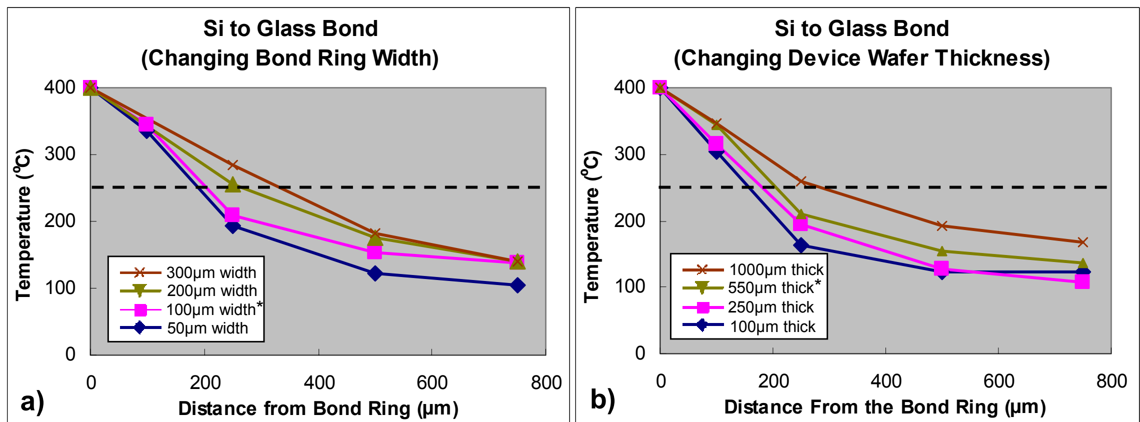


Figure 6.37: Results from the parametric analysis for a Si to glass bond showing a) changes in bond ring width and b) changes in the device wafer thickness. (*Indicates the nominal case.)

Table 6.7: The distance from the center of the bond ring where the temperature drops to 60% of the bond ring temperature, the resultant increased die size due to packaging and the necisary input power for a bond ring width of 50, 100, 200 and 300 µm.

Bond Ring Width	Distance from bond ring needed for 250ºC temperature	Increased Die Size in Each Dimension Due to Packaging	Necissary Input Power per Bond Ring
50 μm	190 μm	430 μm	5.5 W
100 μm (nominal case)	201 μm	502 μm	6 W
200 μm	256 μm	712 μm	6.75 W
300 μm	330 μm	960 μm	7.5 W

As illustrated in Figure 6.37b, decreasing the device wafer thickness decreases the temperature inside of the bond ring by a small amount. The dotted line shows where the temperature was at 60% of the bond ring temperature (which is around 250ºC). Assuming that the device being packaged requires a temperature under 250ºC, Table 6.8 lists these required distances from the bond ring and the overall increase in package size in both dimensions (along the x and y planar axis). As illustrated, the over all decrease in package size due to packaging decreased only from 502 µm with a 550 µm thick device wafer to 424 µm going down to a 100 µm thick device wafer. As also shown, the necessary input power doubles going from a 550 µm thick device wafer down to a 100 µm device wafer.

Table 6.8: The distance from the center of the bond ring where the temperature drops to 60% of the bond ring temperature, the resultant increased die size due to packaging and the necisary input power for a device wafer thickness of 50, 100, 200 and 300 µm for a Si to glass bond.

Bond Ring Width	Distance From Bond Ring Needed for 250ºC Temperature	Increased Die Size in Each Dimension Due to Packaging	Necissary Input Power per Bond Ring
1000 μm	289 μm	678 μm	5 W
550 μm (nominal case)	201 μm	502 μm	6 W
250 μm	181 μm	462 μm	8.5 W
100 μm	162 μm	424 μm	12 W

6.6.2.2 The Si to Si Bond with a 7 µm thick SiO_2 Layer

For the Si to Si bond with a 7 µm thick SiO_2 layer significantly larger input powers

where needed to achieve a 400ºC bond ring temperature. As a result, when applying this technique to a full wafer, an extremely large power needs to be applied. Initial modeling results with only a passive heat sink in the "full wafer bond model" therefore did not result in very low bond ring temperatures inside of the bond ring because the heat was not efficiently sunk from the backside of the device wafer. The model presented in Section 6.6.1 was therefore slightly modified to simulate an active heat sink. For the active heat sink model, the steel plate was replaced with water at a temperature of 23°C with a convection coefficient of 5000 $W/m^2 \cdot K$. This convection coefficient is well in the range of those that can be achieved using forced liquid cooling [217].

Figure 6.38 shows the results of parametric analysis where the temperature at different distances from the center of the bond ring are graphed for changes in the bond ring width and the device wafer thickness. In each case enough power was input so that the bond ring heated up to 400ºC. As illustrated in Figure 6.38a, increasing the bond ring width causes an increase in the temperature inside of the bond ring. The dotted line shows where the temperature was at 60% of the bond ring temperature (which is around 250ºC). Assuming that the device being packaged requires a temperature under 250ºC, Table 6.9 lists these required distances from the bond ring and the overall increase in package size in both dimensions (along the x and y planar axis). As illustrated, the over all increase in package size due to packaging increases from 460 µm with a 100 µm bond width to 992 and 1224 µm going to 200 or 300 µm. As also shown, there is a slight increase in the necessary input power as well when increasing the bond ring width. As expected these necessary powers are significantly higher than those for the Si to glass bond case because of the presence of an active heat sink.

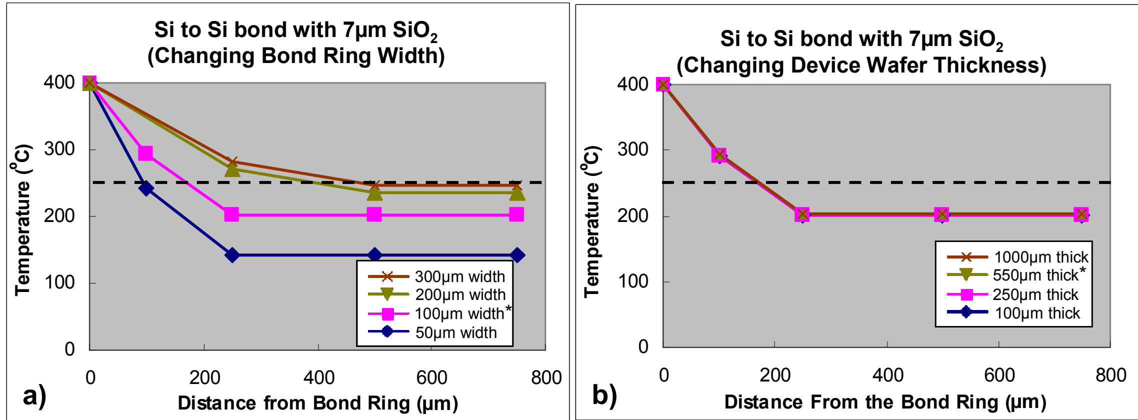


Figure 6.38: Results from the parametric analysis for a Si to Si bond with a 7 µm SiO_2 layer showing a) changes in bond ring width and b) changes in the device wafer thickness. (*Indicates the nominal case.)

Table 6.9: The distance from the center of the bond ring where the temperature drops to 60% of the bond ring temperature, the resultant increased die size due to packaging and the necisary input power for a bond ring width of 50, 100, 200 and 300 µm for a Si to Si bond with a 7 µm SiO_2 layer.

Bond Ring Width	Distance from bond ring needed for 250ºC temperature	Increased Die Size in Each Dimension Due to Packaging	Necissary Input Power per Bond Ring
50 µm	95 µm	240 µm	47 W
100 µm (nominal case)	180 µm	460 µm	59 W
200 µm	396 µm	992 µm	74 W
300 µm	462 µm	1224 µm	84 W

As illustrated in Figure 6.38b, decreasing the device wafer thickness has almost no effect on the temperature seen inside of the bond ring. Once again, the dotted line shows where the temperature was at 60% of the bond ring temperature (which is around 250ºC). Table 6.8 lists these required distances from the bond ring and the overall increase in package size in both dimensions (along the x and y planar axis).

Table 6.10: The distance from the center of the bond ring where the temperature drops to 60% of the bond ring temperature, the resultant increased die size due to packaging and the necisary input power for a device wafer thickness of 50, 100, 200 and 300 μm for a Si to Si bond with a 7 μm bond ring.

Bond Ring Width	Distance from bond ring needed for 250°C temperature	Increased Die Size in Each Dimension Due to Packaging	Necissary Input Power per Bond Ring
1000 μm	180 μm	460 μm	58 W
550 μm (nominal case)	180 μm	460 μm	59 W
250 μm	180 μm	460 μm	60 W
100 μm	180 μm	460 μm	60 W

6.6.2.3 Summary of Parametric Analysis

Overall, for the Si to glass bond, changing the bond ring width and the device wafer thickness only marginally affected the necessary die area needed for packaging. On the other hand, for the Si to Si bond with a 7 μm SiO_2 layer, the necessary die area was a strong function of the bond ring width. In fact, the necessary die area increased from 460 μm on a side to 1224 μm going from a 100 μm wide to a 300 μm wide bond ring. This represents a 7 times increase in necessary die area. The device wafer thickness on the other hand had virtually no effect on necessary die area.

6.6.3 EFFECTS OF CTE MISMATCH

Using differential localized heating, the cap and device wafers are heated to different temperatures and then after bonding occurs, they are cooled down to room temperature. After bonding these two wafers are adhered together and the difference in the amount that each wafer contracts because their different temperatures and coefficients of thermal expansion (CRE) can cause a residual stresses. In uniaxial expansion the stress on the device wafer, σ_{Device}, can be determined from:

$$\sigma_{Device} = E\varepsilon = \left(E_{Cap}\Delta T_{Cap}\alpha_{Cap} - E_{Device}\Delta T_{Device}\alpha_{Device}\right) \tag{6.7}$$

where E and ε are the Young's Modulus and strain; E_{Cap} and E_{Device} are the Young's Modulus for the cap and device wafer; α_{Cap} and α_{Device} are the coefficients of thermal expansion for the cap and device wafer; and ΔT_{Cap} and ΔT_{Device} are the changes in

temperature during cooling (after the bond) for the cap and device wafers. Given Hooke's Law for biaxial strain (in the plane of the wafer) the term $E/(1-v)$ can be substituted for the Young's Modulus [210] and the above equation therefore becomes:

$$\sigma = E\varepsilon = \left(\left(\frac{E_{Cap}}{1 - v_{Cap}} \right) \Delta T_{Cap} \alpha_{Cap} - \left(\frac{E_{Device}}{1 - v_{Device}} \right) \Delta T_{Device} \alpha_{Device} \right) \tag{6.8}$$

where v_{Cap} and v_{Device} are Poisson's ratios for the cap and device wafer.

For estimating the changes in temperature on each wafer, the "full wafer bond model," from Section 6.6.1 was used. Figure 6.39 shows the results from this model when heating up the bond ring to 400ºC for a Si to glass and a Si to Si bond with a 7 µm thick SiO_2 layer. As a result, as summarized in Table 6.11, after bonding, the cap wafer will cool by 385ºC and 470ºC, and the device wafer will cool by 83ºC and 176ºC for the Si to glass and Si to Si bond respectively. Table 6.11 also shows Poisson's ratio, Young's Modulus and the CTE values used for both the cap (Si) and device (Si or glass) wafers. As shown, the glass wafer was assumed to have a CTE of 3.25×10^{-6} K^{-1} which is the value given by Corning Corporation, the manufacturer of the Pyrex® borosilicate glass wafers used in these bond experiments. The Si value for the cap wafer on the other hand was the average of the CTE values measured elsewhere [218] in the 23-400ºC temperature range for the cap wafer in the Si to glass bond; in the 23-500ºC temperature range for the cap wafer in the Si to Si bond; and 23-200ºC temperature range for the device wafer in the Si to Si bond.

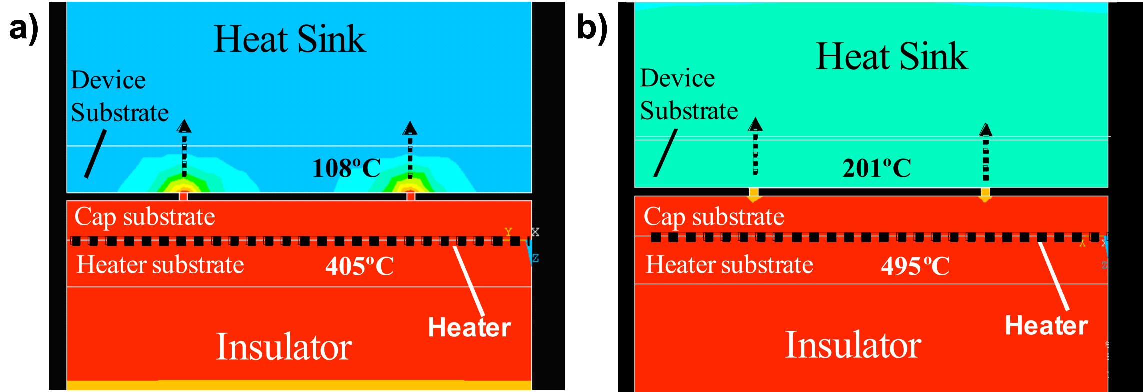


Figure 6.39: The modeling results using the "full wafer bond model" where enough power was input to heat up the bond ring to 400ºC in a) a Si to glass bond and b) a Si to Si bond with 7 μm thick SiO_2 layer.

Table 6.11: The variables used in Equation 6.8 for calculating the stress from bonding.

Variables	Cap Wafer	Device Wafer
Young's Modulus	161 GPa (Si)	64 GPa (glass) 165 GPa (Si)
Poison's Ratio	0.22 (Si)	0.2 (glass) 0.22 (Si)
Average CTE	3.30×10^{-6} K^{-1} (Si to glass bond) 3.35×10^{-6} K^{-1} (Si to Si bond)	3.25×10^{-6} K^{-1} (Si to glass bond) 3.05×10^{-6} K^{-1} (Si to Si bond)
Temperature Change	-385ºC (Si to glass bond) -470ºC (Si to Si bond)	-83ºC (Si to glass bond) -176ºC (Si to Si bond)

Entering the values from Table 6.11 into Equation 6.8 results in a residuaul stress of 247 MPa and 222 MPa for the Si to glass and Si to Si bonds respectively. The Si substrates should be able to handle a fracture stress as high as 7 GPa [219], so the Si substrates in both cases should be more than strong enough to hold up to such stresses. A fracture stress of 270 MPa [220] on the other hand has been measured for Pyrex glass which is problematic since it is on the same order of magnatidute as the residual stress predicted from the model. Furthermore, many thin films such as SiO_2 and Si_3N_4 used in MEMS fabrication have similar fracture stresses. In application of differential localized heating it is therefore important to design the bond so that the residual stress is minimized. This can be done in three major ways: 1) using a lower temperature bonding material such as solder that will melt and bond at 200-300ºC, thus allowing for a lower temperature on the cap wafer and therefore a smaller ΔT in the cap wafer; using a material on the device wafer with a higher CTE so that it shrinks more after cooling; and choosing a material on the cap wafer other than Si that has a lower CTE so that it shrinks

less after cooling.

CHAPTER 7

CONLUSION

An Au-Si eutectic wafer-level vacuum packaging process and a localized heating process called differential backside heating were developed for the packaging of MEMS devices. A summary of this work is presented in Section and the

7.1 DISSERTATION SUMMARY

Chapters 2 and 3 outlined and summarized the Au-Si eutectic bonding process for the encapsulation of MEMS devices. A detailed bond recipe and list of guidelines were presented for achieving strong bonds to substrates with poly-Si or Au surfaces at temperatures of 390 °C or potentially lower. The requirements for achieving uniform and strong bonds were separated into 3 categories: a) the material requirements (Section 2.3), b) the bond recipe (Section 2.4), and c) considerations for the Au-Si eutectic viscous flow (Section 2.5). The *material requirements* mainly depended on which materials were selected on the device wafer. The materials used in the device wafer included: un-doped poly-Si; heavily phosphorous doped poly-Si; and sputtered or evaporated Cr/Au. The *bond recipe* involved first pulling vacuum inside of the bond chamber, then conducting an outgassing step, applying the bond force and finally, applying the bond temperature. The amount of bond force and timing of the bond force turned out to be one of the more critical factors in the bond recipe. The way in which the *Au-Si eutectic flowed* during bonding played an important role in the bond quality and in whether or not devices or other features (such as the getter) would survive the bonding process. Two different types of flow were observed: compressive flow and lateral diffusion. As well, the etched cavity had an effect on the Au-Si eutectic later flow and in some cases the Au-Si eutectic

flowed inside of this cavity, interacting with the getter.

Chapter 4 presented the design for a Pirani (vacuum) sensor which was specifically design for characterizing pressures in the Au-Si eutectic bonding process. This micro-Pirani gauge employed a ladder shaped structure with two parallel bridges and cross-links in between. This design enhanced the physical performance of the gauge by increasing structural rigidity, thus allowing for longer beams and a wider selection of materials and by allowing for better heat distribution across the sensor—therefore improving the full scale range of sensor response. Two poly-Si Pirani gauge designs in particular were characterized specifically for characterizing the Au-Si eutectic bonding process. The D1 design was used for measuring pressures between 50 and 2 Torr with an estimated measurement error of ±0.033 to ±0.82 Torr respectively, and the D3s design was used for characterizing pressures between 0.005 and 4 Torr with a measurement error between ±0.0037 to ±0.065 Torr. Furthermore, order of magnitude estimations of pressure were made using the D1 and D3s gauges in the 50 to 760 Torr and 4 to 760 Torr ranges respectively.

In Chapter 5, data for the packaged Pirani gauges was presented. Depending on whether or not getters were used and whether or not a 1 hour 345 ºC outgassing step was used, three different pressure regimes were achieved: i) pressures of greater than 1 Torr were observed for bonds conducted *without* getters, ii) pressures greater than 100 mTorr where observed for bonds conducted *with* getters but *without* an outgassing step, and iii) pressures below 25mTorr were observed for bonds *with* getters and *with* the outgassing step.

The yield across each wafer was also estimated in order to quantify the bond quality. In estimating the yield, as a metric, packages with pressures greater than 3 standard deviations outside of the mean were determined to have "failed." These packages were counted against the yield. Initial yields of 30.4%, 80.4%, 81%, 84.6% and 94.1% were observed. The 84.6% and 94.1% yield results were achieved in bonds with bond ring widths of 100 and 150μm respectively. In three of the above mentioned wafers, the pressures were also measured over time and in each case, a certain number of packages from each wafer had a significant increase in pressure. These increases in pressure ranged from +29 mTorr +760. In each of these packages, pressures in some cases rose

slowly over time (likely caused by outgassing) and in other cases they seemed to go straight to atmospheric pressure (which could be the result of outgassing or a sudden catastrophic physical leak). The yield drop across these wafers ranged from 10 to 29% after 6 months of testing. Furthermore, in one series of experiments, a number of packages experienced pressure increases of 1.3 to 5.2 Torr after a 23 hour car ride. After heat treatment at 150ºC for 23 hours, the pressures in all of these packages remained stable for the remaining 77 hours at 150ºC and through 50 thermal cycles from -65ºC to 150 ºC. Although this data was not conclusive, these test results seem to indicate that a "burn-in" step could be applied for stabilizing packaged pressures.

In Chapter 6, a new wafer-level localized heating approach called *differential localized heating* was introduced where heat is applied on the backside of the cap wafer and then gets pulled through a bond ring towards a heat sink and away from the device. In this way, large bond ring temperatures can be achieved while maintaining a relatively low temperature at the device location. A localized differential heating bonder test setup was built in order to conduct bond experiments to test the viability of this technique. Bond experiments were conducted between: i) a Si and glass wafer (*bond experiment #1*) and ii) a Si wafer and a Si wafer with a 7μm thick SiO_2 layer (*bond experiment #2*). These material sets were chosen specifically so that there was a low thermal conductivity near the bond ring on the device wafer—as determined from the modeling and analysis, this was an important parameter for achieving good thermal isolation inside of the bond ring. For bond experiment #2, the 7 μm thick SiO_2 layer was chosen to roughly mimic the various thin films in a CMOS process. For example, Sandia National Laboratory's SUMMIT V^{TM} process, shown in Figure 3.2 of Chapter 3, has 6.5 µm of SiO_2, 0.8 µm of SiN_x, and 6.25 µm of poly-Si. In both of these bond experiments, temperature sensors were fabricated underneath the bond ring and at different distances from the bond ring in order to quantify the effectiveness of this localized heating technique. The temperature was observed to be 23% of the minimum bond ring temperature at 650 μm from the bond ring in bond experiment #1, and to be 41% of the minimum bond ring temperature at 250 μm from the bond ring in experiment #2.

7.2 SUGGESTIONS FOR FUTURE WORK

7.2.1 THE AU-SI EUTECTIC BONDING PROCESS

The bond experiments in Chapter 2 and the vacuum encapsulation data in Chapter 5 demonstrated a highly uniform, high strength and high yielding process for encapsulating MEMS sensors. The next step for this work is its application for wafer-level hermetic/vacuum packaging of commercial sensors. As was explained in Chapter 1, there are several MEMS devices which are good candidates for packaging using Au-Si eutectic bonding including: RF MEMS resonators, MEMS accelerometers, MEMS gyroscopes and IR MEMS (including micro-bolometers and thermopiles). Nearly all of these devices can be completely sealed from the environment and only need electrical connection which can be accomplished either through lateral or vertical feed-throughs. Many of these devices as well can benefit from or need vacuum levels <10 mTorr.

In Chapter 5 yield data was presented for one wafer where an initial yield of 94.1% was achieved, and after 6 months it dropped and seemed to level off at 86.8%. This is encouraging data, in particular from an academic laboratory, and the next step is to convert this process into one compatible with large scale production facilities in which repeatable yields can be achieved on hundred or thousands of wafers per year. One of the goals in this process development might be to push the bond ring dimensions as small as possible in order to take up as little die area as possible. This reduces the overall package size and the unit cost of manufacturing. This would allow Au-Si eutectic bonding to potentially replace glass frit bonding (which Motorola and Analog Devices have used for the packaging of many of their inertial sensors [35-38]) in many applications since bond ring dimensions of less than 150μm are generally not attainable using frit glass bonding.

7.2.2 VACUUM PACKAGING AND MEASUREMENT

In this work, using Nanogetters™ and a 60 minute, 345 ºC outgassing step, pressures from <3.7 mTorr to 23.3 mTorr were achieved. As is generally the case for the Au-Si eutectic process, making sure that vacuum pressures all remain stable below a certain value is mostly a mater of process development. In many applications, pressures below <10 mTorr or potentially <1 mTorr may be desirable. As was demonstrated in Chapter 5,

the use of an outgassing step at an elevated temperature reduced the pressures inside of cavities from the 100 mTorr range down below 25 mTorr and in some cases <3.7 mTorr. Therefore one of the main methods for continued reduction in pressure is increasing the time of the outgassing step. Another important factor is improving the process so that each wafer is cleaned well so no residues coats any part of the wafer. Organic residues in particular are know to have high outgassing rates.

An important part of characterizing a process with a low vacuum pressures is the design of the vacuum sensor which can measure pressures in that range with a reasonable resolution. One of the limitations in this work was the inability to measure pressures below <3.7 mTorr. This will become more and more important as the pressure in the cavities are reduced. One of the sensors, the D3 Pirani gauge from Chapter 3 had a 5 times lower pressure range than either of the pressure sensors used for package characterization. In addition, Shie et al. [186] reported pressure measurements between 1 Torr and $1{\times}10^{-7}$ Torr using a different Pirani gauge design with constant temperature circuitry and thermo-electric temperature stabilization.

7.2.3 DIFFERENTIAL LOCALIZED HEATING

One of the main challenges in implementing differential localized heating is figuring out how to conduct bonds on a full wafer at a time. In Section 6.6 a full wafer model was presented in which it is assumed that all of the bond rings across a wafer are heated uniformly. In this model, using the same bond ring dimensions and wafer thicknesses as were used in the modeling and testing in Chapter 6, it takes a 6 Watts/bond ring to achieve a bond ring temperature of 400ºC for a Si to glass bond. This means for instance that to heat up 200 bond ring across a wafer, 1200 Watts of power would be needed. Heat sinking this much power is the main technical challenge. As in the discussion presented in Section 6.1.1 (*Materials and Thermal Design*), the model presented in Section 6.1.3 as well as the model presented in Section 6.6 assumes a 23ºC (room temperature) boundary condition in the massive steel block connected the heat sink. This assumption can only be met if the steel block is very massive. Given the calculation presented in Section 6.1.1, a 50 lb steel block with a 1200 Watts input power would heat up a 50 lb steel block at a rate of 1ºC per 7 seconds. There are several possible

approached in order to address this technical challenge. One is too make a larger thermal mass and or active cooling in order to pull heat out of the system. Another is to pulse heat so that the bond rings have time to heat up but so that there is not enough time for the large thermal mass to heat up significantly. Finally, heater arrays could be used, as were used in this work, so that different parts of the wafer are heated at once.

APPENDICES

APPENDIX 1

BOND CHARACTERIZATION

Bond characterization was done predominantly using two test methods: the razor blade test and the shear test. Section A1.1 presents the various methods available for characterization bond quality and provides a justification for the use of the razor blade test. Similarly, Section A1.2 describes the shear test used for the characterization of bond strength. Next, Section A1.3 describes the use of the scanning electron microscope (SEM) and energy dispersive X-ray (EDX) analysis for analysis of bond metallurgy and failure mechanisms. Finally, Section A1.4 provides an overall summary of the bond test methodology.

A1.1 CHARACTERIZATION OF BOND QUALITY

Two non-destructive inspection techniques were considered for wafer bond inspection: infrared inspection (IR) and ultrasonic imaging. A destructive inspection technique called the razor blade test was also evaluated for wafer bond inspection. As will be described in this section, the razor blade test was the most desirable out of these bond evaluation techniques because more information could be gathered on the actual failure bond mechanism. Section A1.1.1 and A1.1.2 describe each of these evaluation techniques, motivating the use of the razor blade test.

A1.1.1 NON-DESTRUCTIVE INSPECTION TECHNIQUES

Figure A1.1a and Figure A1.1b show a bond which was determined to be strong and one which was determined to have failed by IR inspection. A Research Devices Inc. Infrared Microscope was used for taking the infrared pictures shown in the Figure A1.1.

Using this technique, infrared radiation passes through silicon and dielectric layers but reflects off of metals such as gold. Using the infrared microscope, images could either be taken observing the IR light that passes through the wafer stack using a camera underneath the microscope or the light reflected back up to a camera above the sample. The image in Figure A1.1a shows a bond ring where the Au-Si eutectic was formed and had clearly spread. In Figure A1.1b on the other hand, one of the bond rings either did not form a Au-Si eutectic or did not make good contact with the device wafer and spread laterally. In this way, it could be determined if the Au-Si alloy had formed and flowed. The main drawback of this technique was that voids or other indications of bad adhesion could not be determined from the images gathered. This is because IR does not transmit through the Au-Si alloy and the Au-Si alloy is present all of the way around the bond ring regardless of whether or not a void exists. As a result, not much information was yielded from most of the IR imaging.

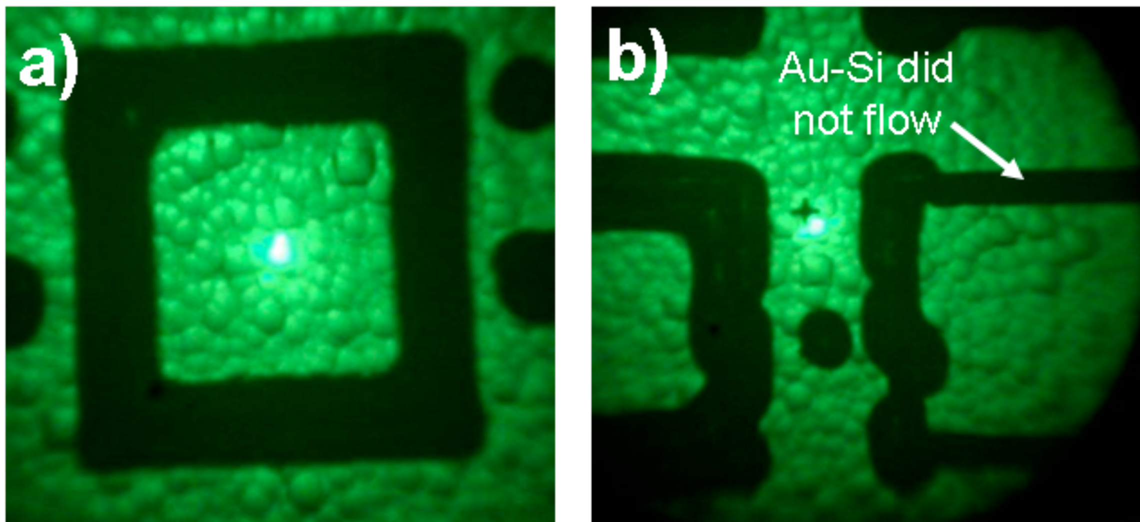


Figure A1.1: IR images of a) a bond ring in which a Au-Si eutectic has formed and spread, and b) where one of the bond rings either did not form a Au-Si eutectic or did not make good contact with the device wafer and spread laterally.

Ultrasonic images were taken using Sonix UHR-2001 scanning acoustic microscope. Using ultrasonic imaging, wafers were placed in a bath of water in which high frequency ultrasonic waves were pulsed through one side of the wafer pair and a detector on the other side measured the ultrasonic waves that got transmitted through. Since a very small

percentage of the ultrasonic waves pass through air, voids can be easily detected. Depending on the wavelength of the ultrasonic signal and the scan speed, spatial resolutions as small as 2 μm could be resolved. Figure A1.2a shows an image of a void free bond ring and Figure A1.2b shows one where multiple voids were detected (these voids could be caused by any number of parameters such as a residue or bad planarization across the wafer during the bond due to an insufficient bond force causing air gaps at the interface of the bond). Voids can provide a path for leaks and reduce the bond strength. Although useful for void detection, the main drawback of this method is that it does not allow for the determination of the source of the voids or failure mechanisms.

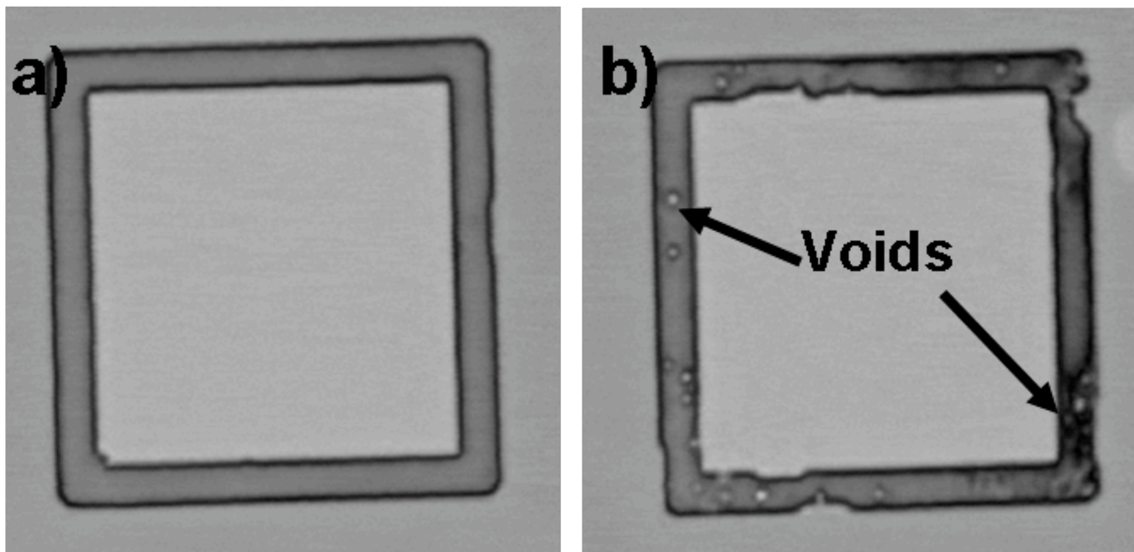


Figure A1.2: Ultrasonic images of a) a bond ring in which no voids seem to exist, and b) one where multiple voids are detected.

A1.1.2 THE RAZOR BLADE TEST

The razor blade test is a destructive means for tearing the two substrates apart after bonding in order to analyze the bond interface. Using the razor blade test, the bonded wafers were first prepared by partially dicing away the cap wafer (in the same way in which the *device* wafers were diced as described in Chapter 3) so that packages were arrayed across the wafer as shown in Figure A1.3a. A razor blade was then used to wedge caps off across the wafer. Bond quality was determined by inspecting the bond

interface. Figure A1.3a shows a SEM of a bond where Si was torn from the cap wafer, adhering to the device wafer for the entire circumference of the bond ring. This indicates that the Au-Si eutectic bond is very strong. Figure A1.3b shows a microscope photograph of a bond ring where part of the cap wafer tore off, but in other parts of the bond ring, either the bond ring delaminated from the device wafer or it tore in the oxide layer. As a result, a lot of information was gathered from this particular razor blade test allowing for more successful future bonds. A number of different types of failure modes were in fact determined as is discussed in Chapter 2.

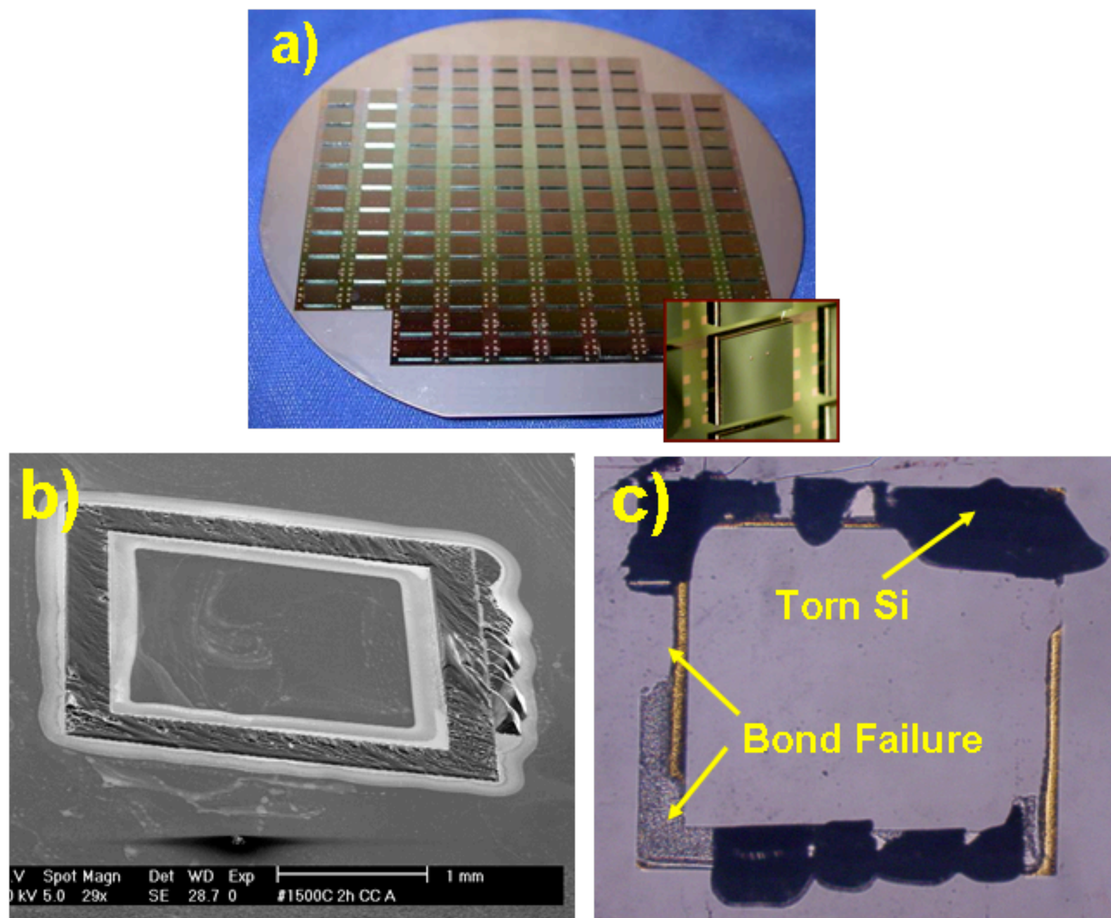


Figure A1.3: a) A wafer after dicing that is ready for the razor blade test, b) An SEM of a bond where Si was torn from the cap wafer adhering to the device wafer and c) one where in some places Si tore from the cap wafer and in others either the bond ring delaminated from the device surface or SiO_2 tore from the device wafer.

A1.2 CHARACTERIZATION OF BOND STRENGTH: THE SHEAR TEST

In the Military Specifications Titled: Department of Defense Test Method Standard for Microcircuits (Mil-Spec-883F method 1014.11), pull strength tests (Method 2011.7) and shear strength tests (Method 2019.7) are defined for determining the strength of bonds between die substrates to other substrates such as PCBs [185]. Although our application is different than that of die attached chips, the concepts are similar in that a solder or eutectic can be used for adhering two substrates together. These bond evaluation techniques were therefore considered for our application.

Figure A1.4 shows how force is applied using the *pull test* and the *shear test* on die attached chips and on a cap bonded to a device wafer. In application of the *pull test* to die attached chips, an axial Force, F_A, is applied to the chip by pulling it perpendicularly away from the substrate. The axial stress, $\sigma_{A,}$ seen on the bonded area, $A_{d,}$ is:

$$\sigma_A = F_A / A_d \tag{A1.1}$$

By Mohr's theory [210], the maximum shear stress due to this axial force is at 45º from the direction which the force is being applied and is:

$$\tau_A = \sigma_A / 2 \tag{A1.2}$$

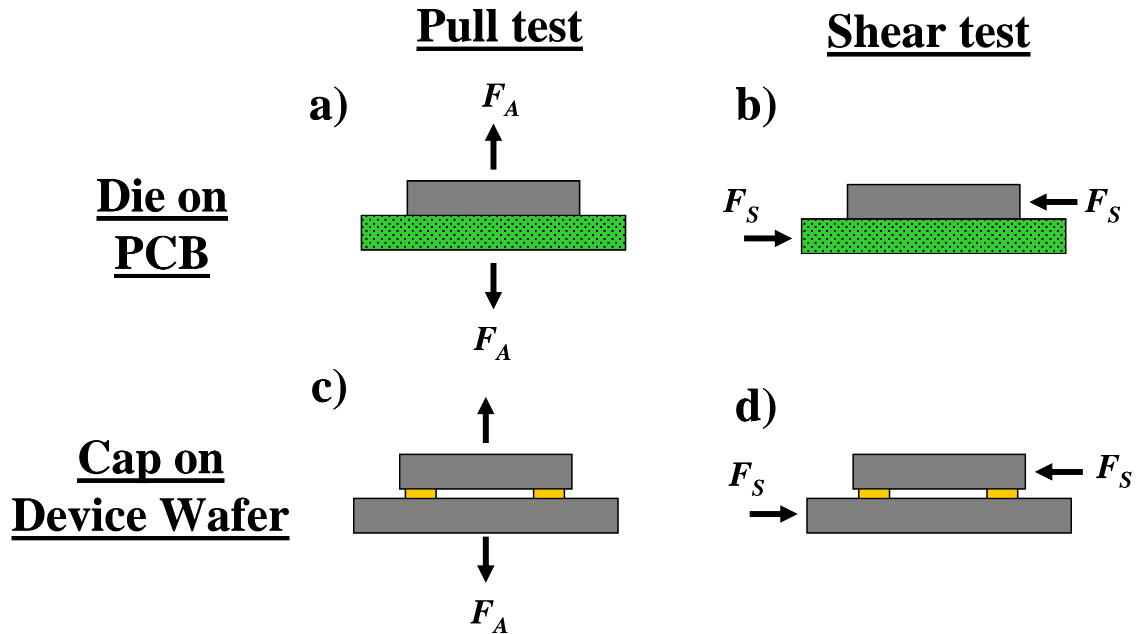


Figure A1.4: The a) pull test and b) shear test for a die on a PCB, and c) the pull test and b) shear test for a cap on a device wafer.

In application of the *shear test* a transverse force, F_S, is applied on the chip by applying a force parallel to the substrate. Figure A1.5 shows a schematic from MIL-SPEC-883 showing how the force is applied perpendicular to the edge of the die using a wedge to apply the force. The resultant shear stress, τ_S, seen on the bonded area, A_d, is:

$$\tau_S = F_S / A_d \tag{A1.3}$$

By Mohr's theory, the maximum axial force due to this shear force is at a 45º from the direction in which the shear force is being applied and is:

$$\sigma_S = \pm \tau_S \tag{A1.4}$$

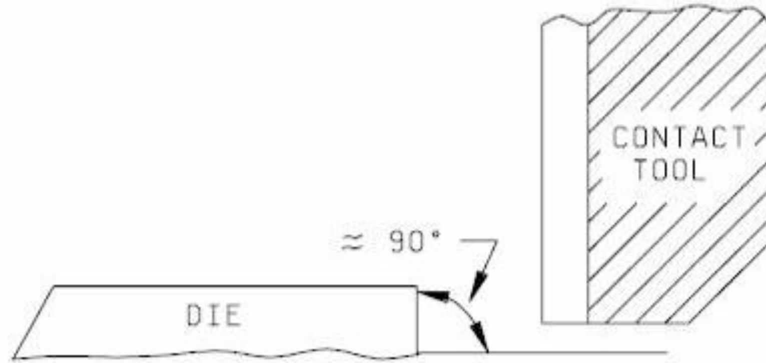


Figure A1.5: A schematic from MIL-SPEC-88F, Method 2019.7 illustrating the application of force to a die 90º to the edge of the sample [185].

Brittle failures generally occur due to *axial stresses* whereas ductile failures generally occur due to *shear stresses*. Therefore failures which are initiated in the bulk Si (which are brittle failures) would likely be due to *axial stresses*, where as failures in the Au-Si eutectic (which could be brittle or ductile) may happen due to either *shear* or *axial stresses*. As illustrated in Equations A1.1 through A1.4, both the pull test and the shear test impart axial and shear stresses.

Although the pull test is briefly mentioned in Method 2011.7 of MIL-STD-883F for testing solder or eutectic die attach bonds, it is mostly directed towards wire bond strength evaluation. Shear testing of solder or eutectic die attach bonds on the other hand is covered in detail in MIL-SPEC-883F, Method 2019.7 and has been used extensively in the literature for evaluating polymer and epoxy bonds [211-214], solder bonds [163, 215] and Au-Si eutectic bonds [163].

Table A1.1 summarizes some of the shear strengths measured using a number of different bonding materials. Because the shear test is detailed in the military specifications and because of its extensive use in prior studies, it was chosen for evaluating bond strength in this work.

Table A1.1: Shear strength data from the literature taken using the Mil-specifications using a number of different adhesive materials.

Shear Strength for Die Attached Chips		
Material	**Shear Strength**	**Comments**
Polymide [211]	4.2 to 8.9 MPa	Varied depending on material bonded too.
Epoxy [211]	2.9 to 46< MPa	Varied depending on composition and material bonded too.
Silver/Resin Mixture [212]	0.6 to 1.1 MPa	Varied depending on composition
In-Au Solder [216]	2.5±2 17.5±3 MPa	Varied depending on the bond recipe
Au-Si Eutectic [163]	12.5 to 15 MPa	Depending on bond recipe at bond temperature.

The failure criteria specified in MIL-SPEC-883F were used for evaluation of our packages. As shown in Figure A1.6, three different standards are defined for determining if a chip passed the shear test. In the first case, when silicon from the die breaks, adhering and covering more than 50% of the other substrate, the pass/fail criteria is determined as 1.0x the minimum bond strength defined in the figure. When less than 50% of the die substrate broke and adhered to the other substrate, 1.25x the minimum strength was used and when 10% of the die substrate broke and adhered to the other substrate 2.0x the minimum strength was used.

To be conservative, in this work the 2.0x minimum strength criteria was used. Considering the slope of the line for the 2.0x, the minimum strength the bond needs is a ~12.3 MPa. For our application, with 300, 150 and 100 μm wide bond rings with bonded areas of approximately 0.03, 0.15 and 0.01 cm^2 resulted in minimum applied shear forces of 37.2 N (3.8 kg), 18.6 N (1.9 kg) and 12.4 N (1.3 kg) respectively.

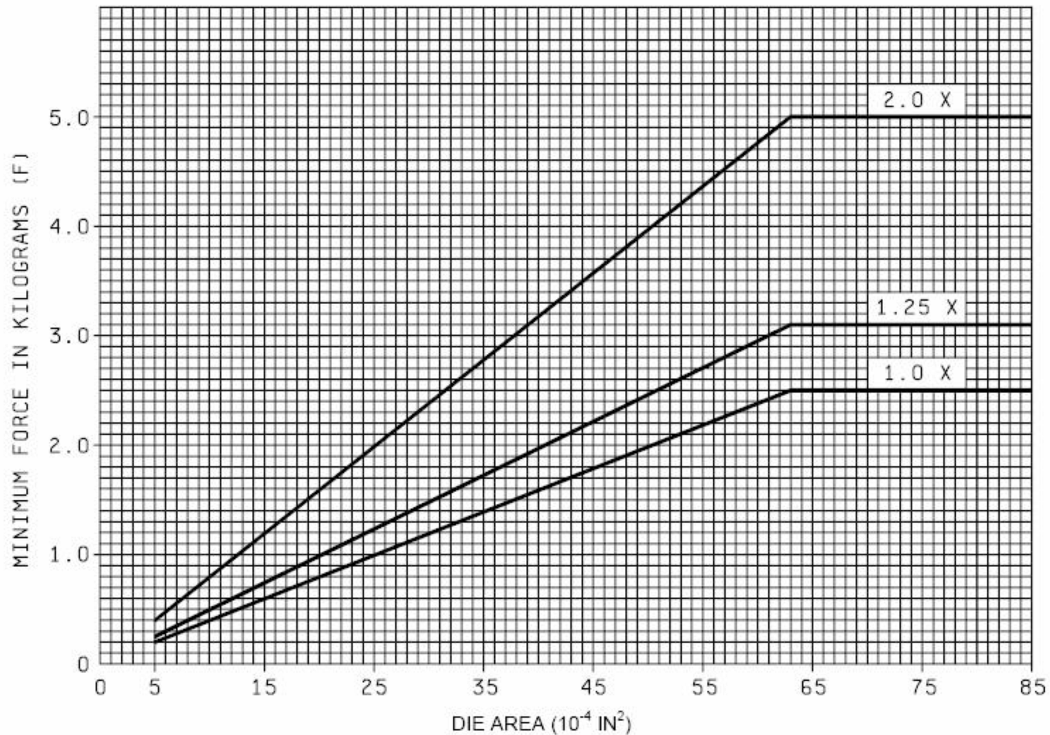


Figure A1.6: A schematic from MIL-SPEC-883F showing the pass/failure criteria for 3 different classes of failed die bonds[185].

A1.2.1 THE SHEAR TEST SETUP

Figure A1.7 shows a schematic of the shear test setup that was built for characterizing the shear strengths of bonded/diced chips. As shown in the side and top views, an aluminum slider plate sits on top of a larger aluminum base plate. A bolt is screwed through a slot in the slider plate to keep the slider plate from going out of plane and to make sure that it moves perpendicular to the chip. As also shown in the figure, a 1 kg weight is placed on top of the slider plate to further prevent out of plane movement. Using thin polymer coated stainless steal wire (fishing wire), weights were placed in a bucket which hung off of the edge of the base plate in order to apply a specified force onto the slider plate. As shown in the zoomed in portion of the side view, the chip sits inside of a 24 mil (~560μm) deep square slot. As also shown, the slider plate applies force perpendicular to the edge of the cap in order to shear it off. The edge of the base plate was also beveled in order to reduce the friction of the wire that slides over the edge of the base plate. Figure A1.8 shows a photograph of a chip sitting in the test setup.

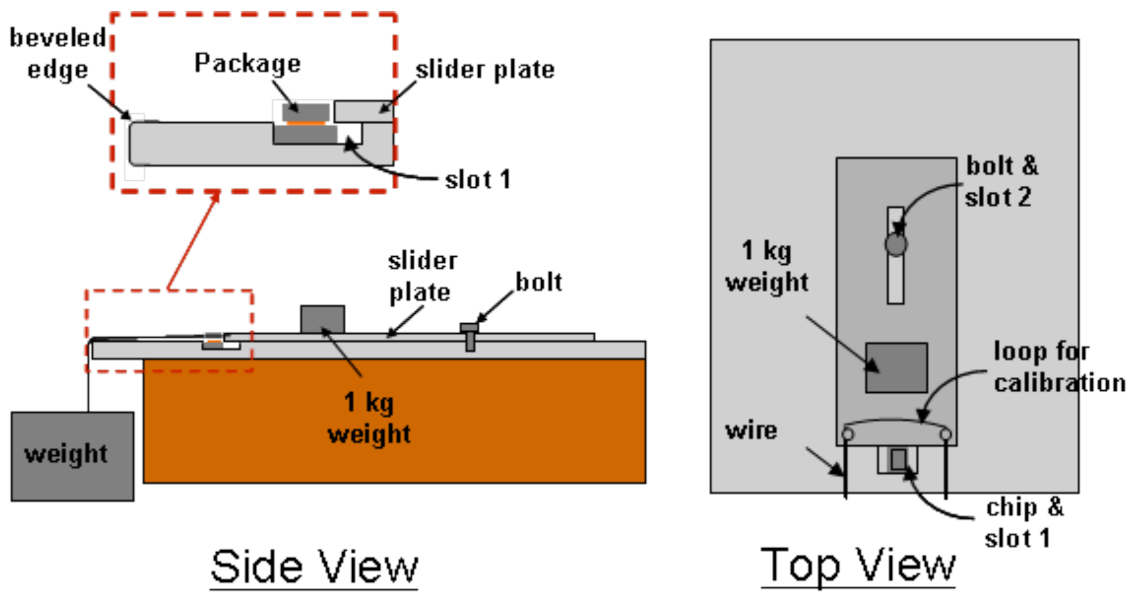


Figure A1.7: A schematic of the shear test setup.

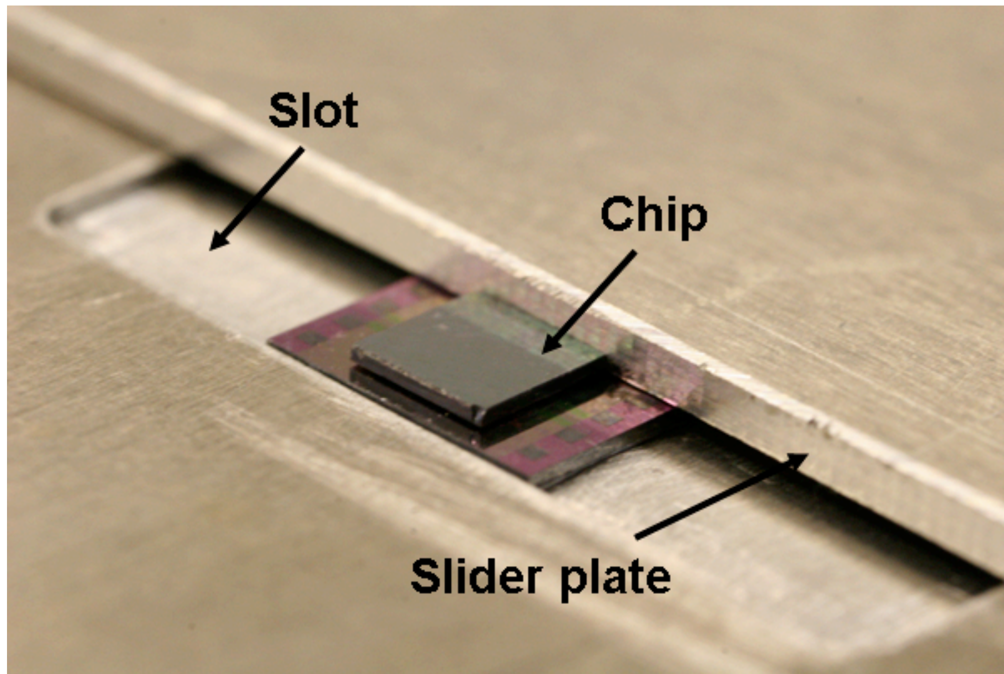


Figure A1.8: Photograph of the shear test setup.

A1.2.2 CALIBRATION OF THE SHEAR TEST SETUP

In the shear test setup, there were two sources of friction. As a result, the amount of weight applied, F_{appied}, at the end of the wire was not the same force seen at the slider plate, F_{acting}. Both of these friction forces are static friction forces since the plate does not move until the package actually fails. The first source of friction was from the 1 kg weight which sits atop the slider plate in Figure A1.7. This friction force, F_1, is:

$$F_1 = \mu_1 \cdot (1 \text{ kg}) \qquad \text{(A1.5)}$$

where μ_1 is the static friction coefficient between the slider plate and the base plate. This friction force is constant because the 1 kg weight is the only force which acts to press the slider plate into the base plate. To measure the magnitude of F_1, the 1 kg weight was placed on top of the slider plate without placing a chip into slot 1 in Figure A1.7. Water was then poured into the bucket until the slider moved (water was used for this measurement because water could be applied in small increments and measuring the volume of the water allowed for very precise weight measurement). The friction force was determined to be 0.5±0.05 kg.

The second source of friction was from the wire which slid over the beveled edge of the base plate. This friction force, F_2, is:

$$F_2 = \mu_2 \cdot (F_{appied}) \qquad \text{(A1.6)}$$

where μ_2 is the static friction coefficient between the wire and the beveled edge. This force was linear as shown in Equation A1.6 because the force pressing the wire into the base plate increases linearly as F_{appied} increases. This force was determined using an Accu-weight Model T50 force gauge. One end of the force gauge was hooked around the wire loop tied through the slider plate (shown in Figure A1.7) and the other side was hooked to the base of a table. Weights were then place into the bucket. Figure A1.9 shows a graph of the results from this experiment. The friction coefficient, μ_2, was determined from the slope of the line in Figure A1.9. This slope was determined to be 0.734 with an error of approximately ±0.025. Subtracting the friction forces from the

force applied at the end of the wire gives the approximate force actually seen by the chip:

$$F_{actual} = (0.734\pm0.025) \cdot (F_{appied}) - 0.5\pm0.05 \quad \text{(A1.7)}$$

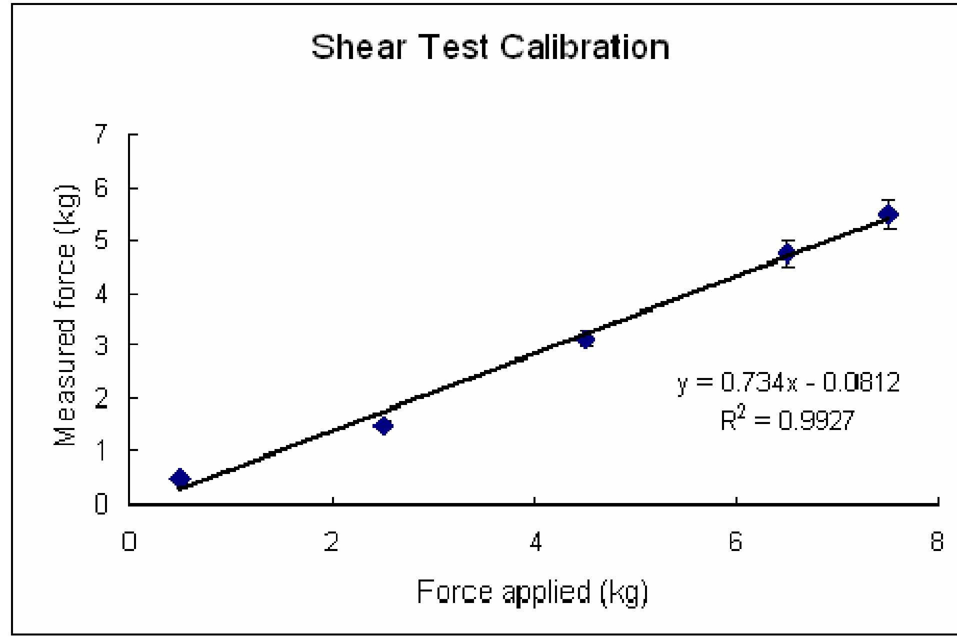


Figure A1.9: A graph of the calibration plot for the shear test setup.

A1.2.3 SHEAR TEST METHODOLOGY

Using the test setup shown in Figure A1.7, 0.66 lb weights were placed in the bucket one at a time until package failure. For the final 0.66 lb weight placed in the bucket, it was not evident whether or not the entire 0.66 lb weight was needed for failure or if some fraction of that weight would have been sufficient. Therefore, for estimating the actual amount of weight needed for failure, the final weight was counted as 0.33 lbs with a ±0.33lb error bar. Incorporating this into Equation A1.7, the weight that the chips saw during fracture was determined as:

$$F_{actual} = (0.734\pm0.025) \cdot (0.66 \cdot (W_n-1) + 0.33\pm0.33) - 0.5\pm0.05 \quad \text{(A1.8)}$$

where W_n was the number of weights needed for either the cap to shear off or for the package to break in the substrate or cap (but not in the bond ring). The sources of error

shown in Equation A1.8 were from the error in the applied force discussed above and from the calibration setup (discussed in Section A1.2.2). Considering Equation A1.8 this error sums too:

$$\textit{Shear Force Measurement Error} = \pm\, 0.0183 \cdot F_{actual} \pm 0.335 \text{ kg} \qquad \text{(A1.9)}$$

Generally, for the characterization of each bond, five or more caps were used for shear tests from the top, bottom, center, right and left quadrants of the wafer. Table A1.2 shows sample shear tests results. Shown in the table are: i) the position of the chip tested (columns and rows), ii) the calculated shear strength (calculated using Equation A1.8), iii) the mode of failure, iv) whether or not each package passes the military specification (>12.3 MPa shear strength), and v) the average and standard deviation of the shear strengths. Figure A1.10 shows the positions for each of the packages from the sample data in Table A1.2.

Because of the limits of the capacity of the test setup, the maximum force that could be applied was 12.3 kg and therefore, according to Equation A1.7, A1.8 and A1.9, the maximum force that could be applied to the actual chip, F_{actual}, was 8.5±0.53 kg. For chips with 300 μm bond rings (which had a 0.03 cm^2 bonded area), this resulted in a 27.8±1.8 MPa maximum applied shear stress that could be applied to each package. As shown in the sample table, Table A1.2, for packages that were stronger than this and could not be broken, the type of failure they is listed as "Not enough force applied for failure" and the shear strength is listed as >27.8 MPa. In some samples as well, the failure did not occur near the bond ring itself, but in the package or cap. In these cases the type of failure was listed as "Sheared in cap or device substrate." This could result from a slight misalignment in mounting the specimens or in the geometry of the specimen causing the substrate to break before enough shear force was applied to shear the bond ring interface. Regardless, because enough force is not applied in these cases for the bond ring to shear off, the failure mechanism of the bond can not be determined. Lastly, in the case where the sample broke in the bond ring itself, the type of failure was listed as "Sheared in bond ring." In these cases the bond ring could be inspected after shearing to see the failure mechanism. For each bond in which the shear test was conducted in

Chapter 2, a table similar to Table A1.2 is presented along with a discussion on the implications of those shear test results.

Table A1.2: Example shear test results.

Sample bond Results (*This is not real data)			
Position	Calculated Shear Strength (MPA)	Type of Failure	Pass/Fail
C5-R8	15.8	Sheared in bond ring	Pass
C6-R2	>27.8	Not enough force applied for failure	Pass
C2-R8	17.4	Sheared in bond ring	Pass
C9-R8	5.5	Sheared in bond ring	Fail
C5-R13	15.8	Sheared in cap or device substrate	Pass
Average Strength: 16.5 MPa			
Standard Deviation: 7.9 MPa			

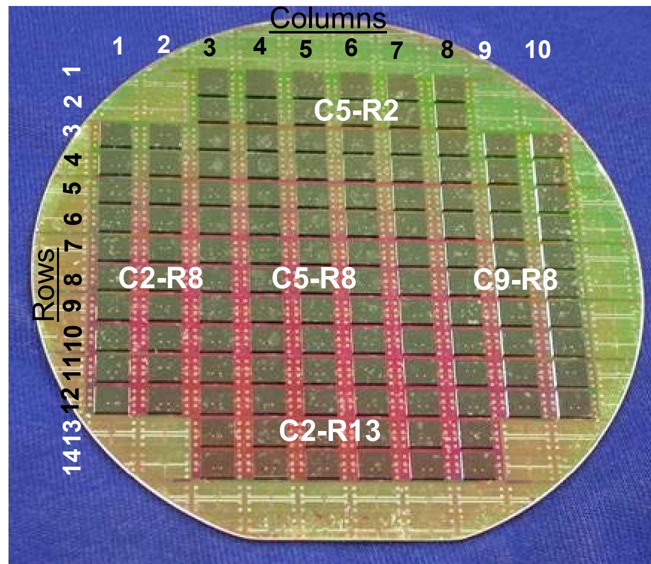


Figure A1.10: The rows and columns of packages in the wafer and the packages selected for shear tests from the sample data shown in Table A1.2.

A1.3 SEMS Photograph and EDX Spectroscopy Analysis

Scanning electron microscope (SEM) photographs were taken from cross-sections of many of the bonds in order to better understand the bond quality and mechanisms for failure. Two different tools were used for taking SEMs: the XL30 FEG SEM Philips and the Quanta 200 3D. For each of these tools a high energy electron beam is focused and rastered across the sample. The SEM image is compiled from data collected at a detector

which measures electrons that reflect off of the sample. The resolution of the images collected depends on a number of factors including sample preparation, the materials used, the settings of the SEM software, and user expertise.

For preparation of samples for SEM photographs of cross sections, most of the samples were cleaved. Cleaving allowed for a minimal amount of change to the cross-section. Dicing the sample in order to look at the cross section on the other hand generally caused smearing of Au-Si eutectic layer.

Energy dispersive X-ray (EDX) spectroscopy was used for compositional analysis of bond joints and was conducted in the XL30 FEG SEM Philips and the Quanta 200 3D. In EDX analysis, an SEM scan was first taken to get an image of the specimen to be analyzed. The electron beam used for making SEM images was then either focused at a particular area or rastered across the sample to get a map of the composition across the entire area of the image. Energy from the electrons in this beam hit various atoms in the cross-section and the incident electrons then loose a certain amount of energy. As a result, these atoms are ionized by the excitation of the electrons to higher energy states and an inner shell vacancy is created. These ionized atoms can then loose energy in a number of ways, one of which is for an outer shell electron to jump into the vacant inner shell. This loss of energy can result in X-ray photons which are measured using an X-Ray detector mounted inside of the vacuum chamber of the SEM tool. The spatial resolution of the measurement is dependant on the electron beam spot size and the amount of scattering of the incident electrons through the material.

A1.4 SUMMARY OF THE METHODOLOGY FOR BOND CHARACTERIZATION

Although nice images could be acquired using infrared microscopy and ultrasonic imaging (Section A1.1.1), more useful information on bond integrity and failure mechanisms were determined using the destructive razor blade test (Section A1.1.2). Furthermore, as supposed to the shear test, the razor blade test could be applied quickly on bonded chips across the wafer. As a result, the razor blade test was the primary method for determining bond quality. Using the razor blade test, it could be inferred whether or not a bond would result in a hermetic seal by whether or not either silicon transferred from the cap wafer to the device wafer or some of the thin films or the bulk

silicon from the device wafer transferred to the cap substrate *for the entire circumference of the bond*.

In several cases the criteria for quality bonds via the razor blade test were passed, but the bond strength was very weak because of reduced adhesion in one of the underlying films on the device substrate. In these cases the shear test was useful for determining whether or not the cap wafer had adequate adhesion to the device substrates. Furthermore, the shear test is more quantitative. Because shear tests were more time consuming it was only conducted on select bonds.

SEM and EDX analysis, on the other hand, were used strictly for failure analysis and helped diagnose issues with the materials used and in the bond recipe.

Table A1.3 summarizes the bond characterization techniques and the criterion used for determining bond quality and bond strength. As explained in Chapter 1, these tests were only used for initial determination of bond quality—final determination of hermeticity of bonds will be determined in Chapter 5 by their ability to hold vacuum.

Table A1.3: Summary of the test techniques and criterion used for determining hermetic/strong bonds.

Test Result	Test Method	Pass Criterion
General Quality	Razor Blade Test	Silicon transferred from cap to device wafer or thin film or silicon transferred from device to cap wafer for entire circumference of the bond
Strength	Shear Test	Shear strength of >12.3 MPa
Failure Analysis	SEMS & EDX	-

APPENDIX 2

WAFER BONDERS & BOND RECIPE

In the course of experiments, 3 different bond chambers were used: an EVG 510 wafer bonding system, an SB6 semi-automated wafer bonding system and an SB6e semi-automated wafer bonding system. Before bonding, the wafers were aligned using alignment marks on the front side of one of the wafers (generally the cap wafer) to align to alignment marks on the backside of the other wafer (generally the device wafer). When conducting bonds in the EVG 510, an EVG 620 bond aligner was used for the wafer alignment and in conducting bonds in the SB6 and SB6e, a SUSS microTec MA6 bond alignment system was used.

After alignment with either the EVG 620 or the SUSS microTec MA6, the wafers were clamped into a special fixture and transported to the bond chamber. Figure A2.1 shows the configuration inside of the bond chamber, where the two wafers sit on top of the *bottom heater*. As illustrated, these two wafers are separated by three 100µm spacers which were initially used to hold the wafers apart.

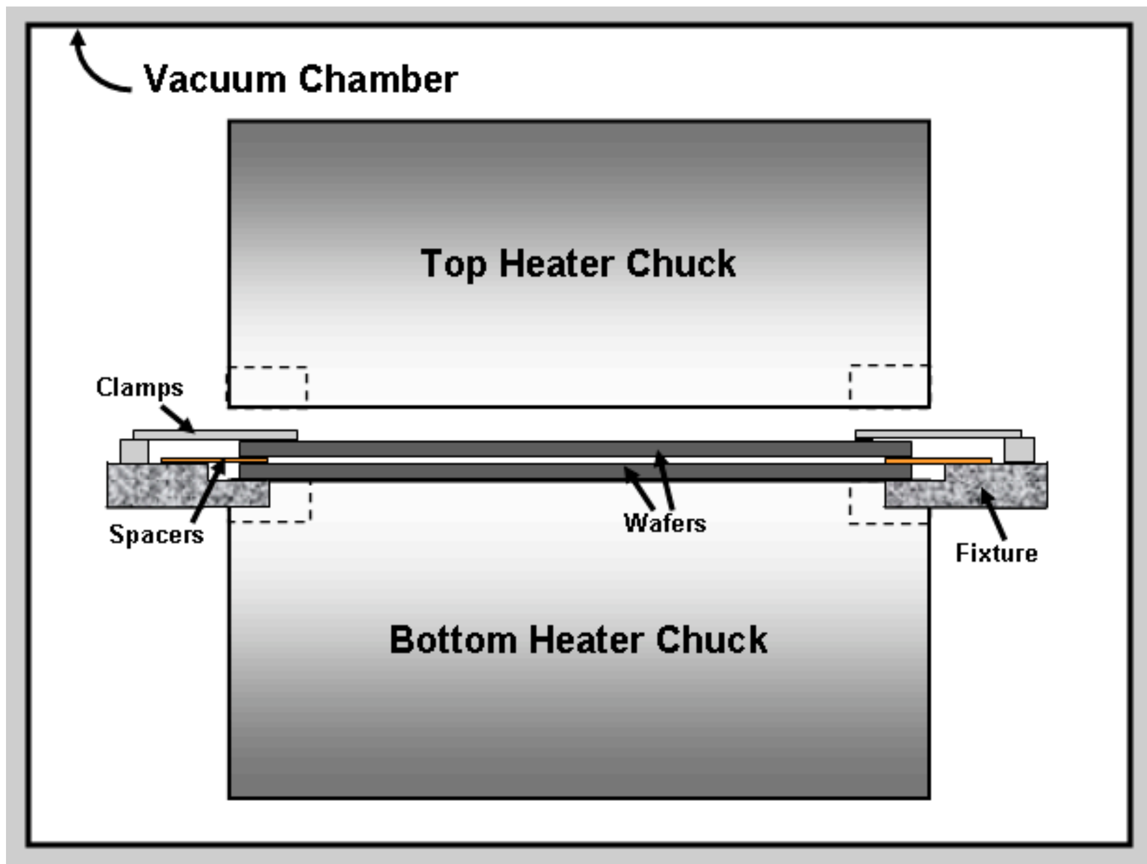


Figure A2.1: A schematic of the vacuum bond chamber where initially the wafer position is maintained using clamps and held apart with spacers.

Figure A2.2 shows a schematic of the bonding process where: i) the bond chamber was pumped down to a pressure of around 10×10^{-6} Torr; ii) both the *bottom heater* and *top heater* were raised to an *intermediate temperature* of 345ºC and held for 1 hour; iii) physical contact was made between the wafers by removing the spacers, the bond force was appied, and the clamps holding the wafers together were; iv) the temperature was raised to the *bond temperature* which ranges from 390 to 410ºC and the temperature was held for a specified amount of time, generallt 40 minutes. After running the bond sequence, the wafers were then cooled to below 200ºC at which point they were pulled out of the wafer bonder.

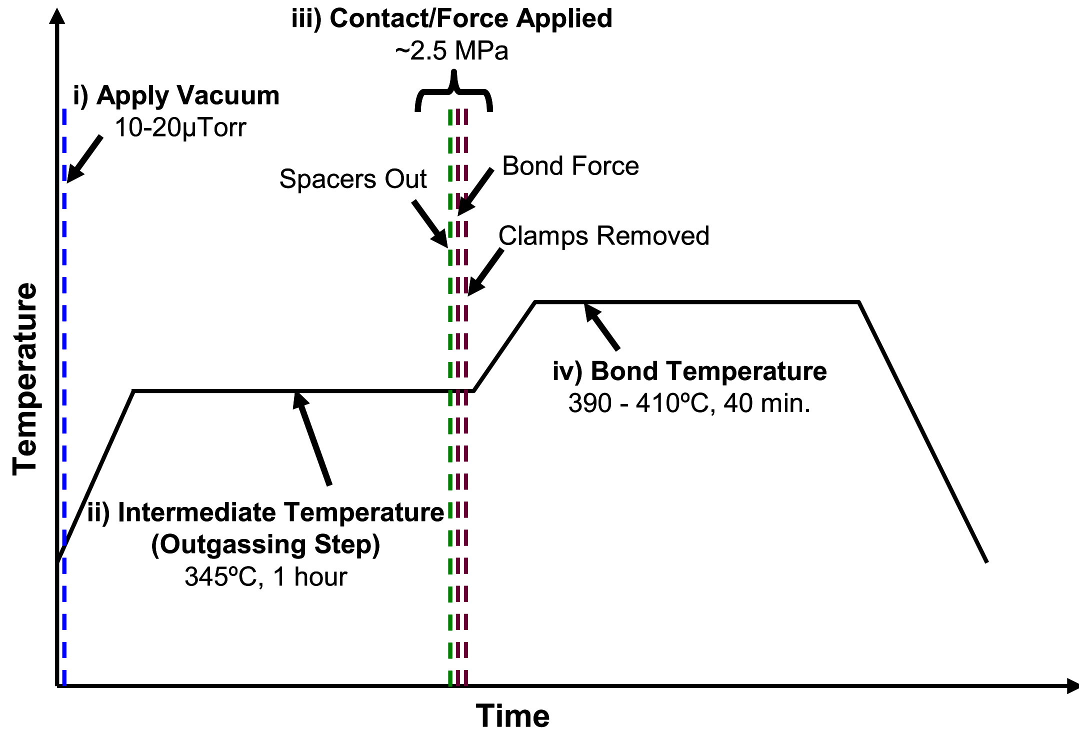


Figure A2.2: The generic bond recipe.

In Timothy Harpster's PhD Dissertation [26], the temperature was calibrated for both the EV501 and the SB6 bonders. Both of these bonders use thermocouples embedded in the bottom and top chucks (the bottom and top chucks were shown schematically in Figure A2.1) for temperature feedback control. Figure A2.3, right and left, shows experiments Harpster ran where the set temperatures were ramped and the wafer temperatures were measured for the EVG and SB6 respectively. An integrated thermistor fabricated on a Si wafer was used in the EVG501 and a thermocouple embedded near the wafer in the bottom chuck of the SB6 bonder was used for measuring the wafer temperatures. Figure A2.3 shows the difference between the temperature measured by the bonder and that measured near the wafer, ΔT (the rise temperature), and time which it took for these to temperatures to equal out, Δt (the rise time). (The end of the *rise temperature* and *rise time* was defined by when the temperature of the integrated thermistor or thermocouple came within 1% of steady state). Table A2.1 shows the *rise temperature* to *rise time* ratio (ΔT/Δt) and the temperature offset for both of these bonders. As illustrated, the EVG and SB6 bonder both had large ΔT/Δt ratios (which

means that it took a long time for wafer temperature to equal the temperature measured by the bonder for feed-back and control) of 7.9 and 7.0 ºC/minute respectively. In addition, the EVG bond had an approximate 12% overall temperature offset, where as the SB6 bonder had less than a 0.5% temperature offset.

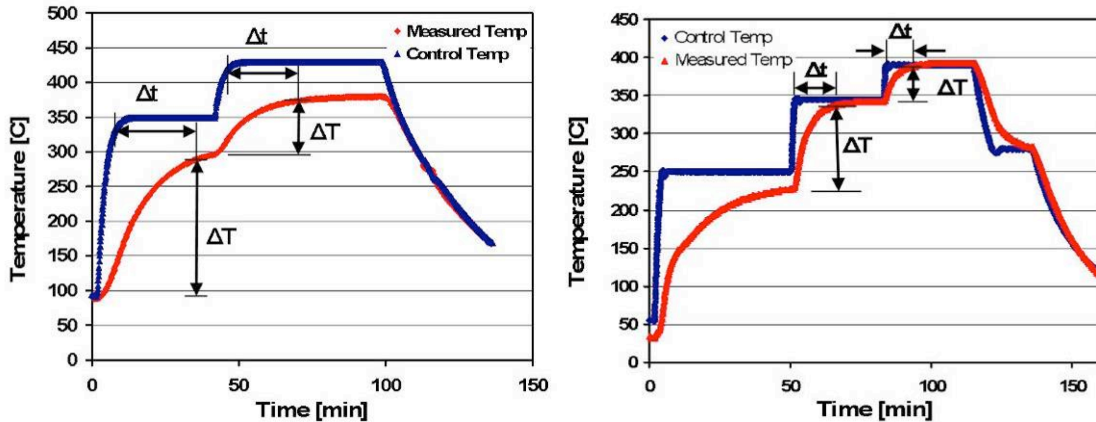


Figure A2.3: Comparison of control temperature and actual wafer temperature of wafers (in vacuum) in the SB-6 bonder (left) and EV-501 bonder (right)

Table A2.1: Measured rise time and steady state temperature offset for the SB-6 and EV-501

	EV bonder	SB-6 bonder	SB-6e bonder
Temp Offset	12%	<0.5%	~ 0%*
ΔT/Δt	~7.9ºC/min.	~7.0ºC/min.	~ 0*

*The temperature offset and ΔT/Δt were near 0 because the thermo-couple used for feed-back and control was positioned very close to the wafer. Therefore the difference between the temperature measured during bond and that seen by the wafer was very small.

To offset the effects of the large offset in temperature seen in the EVG bonder, much higher set temperatures were used. In the presentation of the bond results (Chapter 2) the temperature offsets shown in Table A2.1 are factored in. For all of the bonds conducted in the EVG bonder, set temperatures of 450ºC were used which corresponded to actual temperatures of 395ºC at the wafer according to the calibration curves presented above. For both the EVG and the SB6 bonders, the initial temperature step in combination with a long hold time at the bond temperature were used in order to compensate the large ΔT/Δt.

In the SB6e on the other hand, a thermocouple a few millimeters away from the wafer was used for feedback and control. Because of this feedback, the temperature sensed was essentially the temperature on the wafer. Figure A2.4 shows a typical run using the

feedback from this thermocouple. In addition to having more accurate temperature feedback, as illustrated in Figure A2.4, the heating times were much faster than in the EVG or SB6 bonders. As a result, there was no need for a longer lead time for bonding. It should be noted, that because of an error in transferring the recipe from the SB6, in several of the bonds conducted in the SB6e in Chapter 2 the bond temperature was set at 410ºC instead of 390ºC. As will be discussed, this did not appear to affect bond quality.

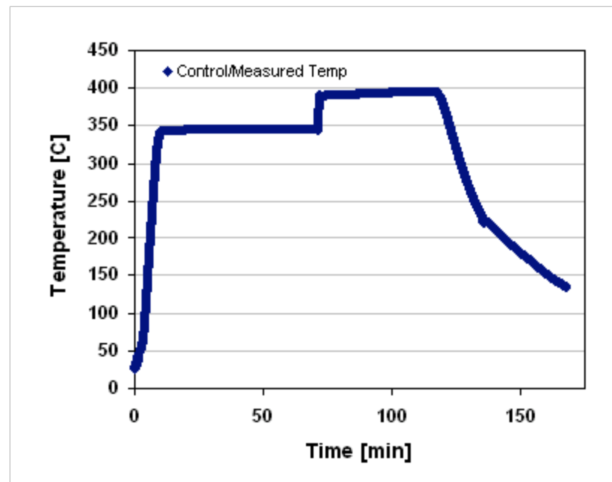


Figure A2.4: The temperature profile for the bottom chuck for the SB6e which was controlled and measured by a thermocouple near the surface of the wafer.

APPENDIX 3

AU-SI EUTECTIC BOND METALLURGY

Most of the research in Au/Si reactions described in Section 2.1 (*Background & Previous Work*) of Chapter 2 was conducted for applications of Au-Si eutectic bonding applied to chip-level die attach. In this section some of those reports are put into the context of Au-Si eutectic bonding for wafer-level packaging. Furthermore, the metallurgy of some of the Au-Si eutectic bonds conducted here are investigated.

A3.1 BOND UNIFORMITY

In Au-Si eutectic bonds applied for die attach a non-uniform bond is acceptable if a large enough percentage of the surfaces bond. For instance, consider a 5×5mm chip in which only 50% of the back surface makes a strong bond to metal on a PCB. If the bonded area of the backside of this chip has an ultimate strength of 120MPa (the ultimate strength of Au), it would take an approximately 2880 N (269 kg) axial force or a 1440 N (134kg) shear force to tear the chip off the board. Such a bond would easily pass the shear test military specifications described in Appendix 1. On the other hand, for wafer-level vacuum/hermetic packaging, one small 100 to 300μm diameter void in any of the 100s of bond rings across a wafer will ruin that bond ring's hermeticity and ability to hold vacuum. Furthermore, as supposed to bonding two relatively flat surfaces, in wafer bonding application there are generally topologies such as feed-throughs to bond over. It is therefore more important that the soft eutectic should be formed so that it can conform over this topology. Therefore, in wafer bonding applications, it is much more important that the soft Au-Si eutectic is formed around the entire bond ring and in bond rings across the entire wafer.

The phase diagram shown in Figure A3.1 shows a simplified representation of the composition of a gold thin film deposited onto a silicon substrate at above 390ºC over time. The dotted line in Figure A3.1a shows the percentage of Si in Au as Si diffuses into the bond ring. As the Si content increases, a larger percentage of this mixture becomes Au-Si eutectic. As shown in Figure A3.1b, according to the phase diagram, at above ~18.32% the film becomes 100% Au-Si eutectic. At above ~18.47%, the phase diagram predicts that the film should be partially Au-Si eutectic and partially Si precipitate. As the percentage of Si increases, a larger percentage of the film becomes Si precipitate. In the next subsection (Section A3.2) the composition of the Au-Si eutectic bonded film from this work are analyzed and discussed.

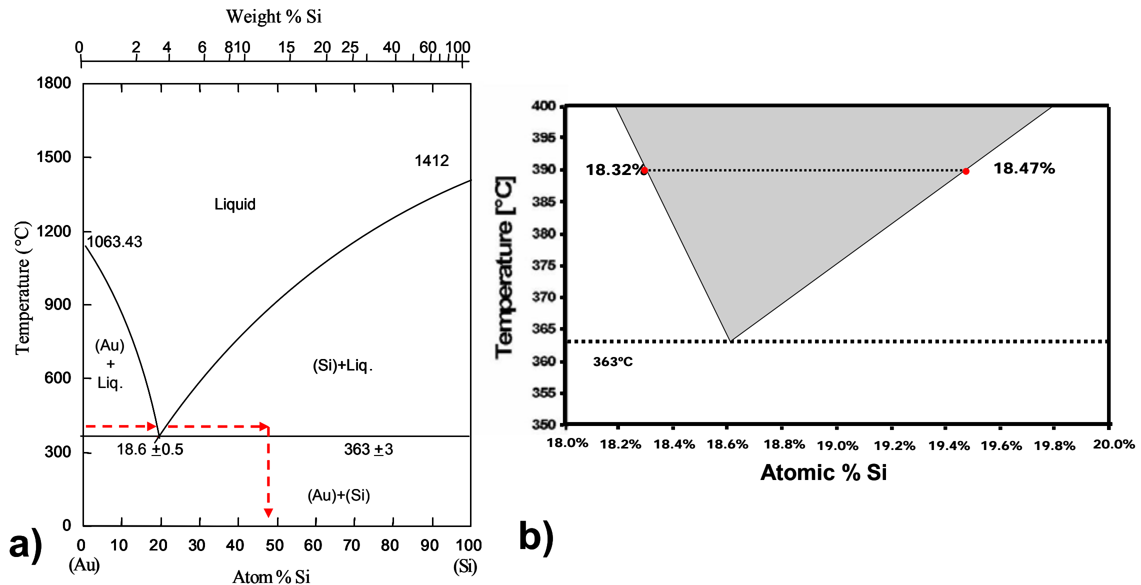


Figure A3.1: a) The dashed arrow shows how the composition of the Au film changes as Si diffuses in and b) a zoomed in view near the eutectic point. [152].

A3.2 BOND COMPOSITION

To better understand what happens in the bond ring during a bond, SEM images of the cross sections of several bonds were taken as well as EDX spectroscopy for compositional analysis. Table A3.1 shows some of the bond parameters for the bond rings that were analyzed (more details on the bond recipe and material parameters for each of these bonds are presented in Sections 2.3.3 and 2.5.2). Figure A3.2a shows and

SEM photograph of the cleaved edge of bond #56 (one of the bonds shown in Table A3.1). Figure A3.2b and Figure A3.2c show EDAX scans of the cross-section in Figure A3.2a that graphically illustrate the relatively densities of Si and Au atoms in the cleaved cross-section. Comparing Figure A3.2b and Figure A3.2c, there are pockets in the bond region in which there are relatively high densities of Si and relatively low densities of Au. As shown in Figure A3.2a, a more focused EDAX scans in one of these pockets showed 91 atomic % Si. Though these EDX measurements did not show this area to be 100% silicon, considering the phase diagram, it is likely that this area is silicon precipitate. As also shown in Figure A3.2 outside of this Si pocket, in a wider area scan, 45 atomic % Si was measured. Similarly EDX analysis was conducted on bonds #36 and #71. In those EDX scans small silicon rich areas were also observed and as shown in Table A3.1, in wider area scans 42 and 55 atomic % Si in Au was measured respectively.

Table A3.1: Bond experiments from which SEM cross-sections and EDX analysis were taken. More details on the recipes of these bonds are presented in Sections 2.3.3 and 2.5.2.

Bond #	Intermediate Temperature Step	Bond Temperature Step	Bond Force	Comments	Discussion of Bond Experiment	Composition
51	345ºC, 10min.	390ºC, 20min.	1.0MPa (390N)	Good bond in some areas	Section 2.3.3	42 atomic% Si
56	345ºC, 10min.	390ºC, 35min.	1.0MPa (390N)	Good bond in some areas	Section 2.3.3	45 atomic% Si
71 (Device)	345ºC, 60min.	390ºC 40 min.	3.5MPa (1300N)	High yield device bond	Section 2.5.2	54 atomic% Si

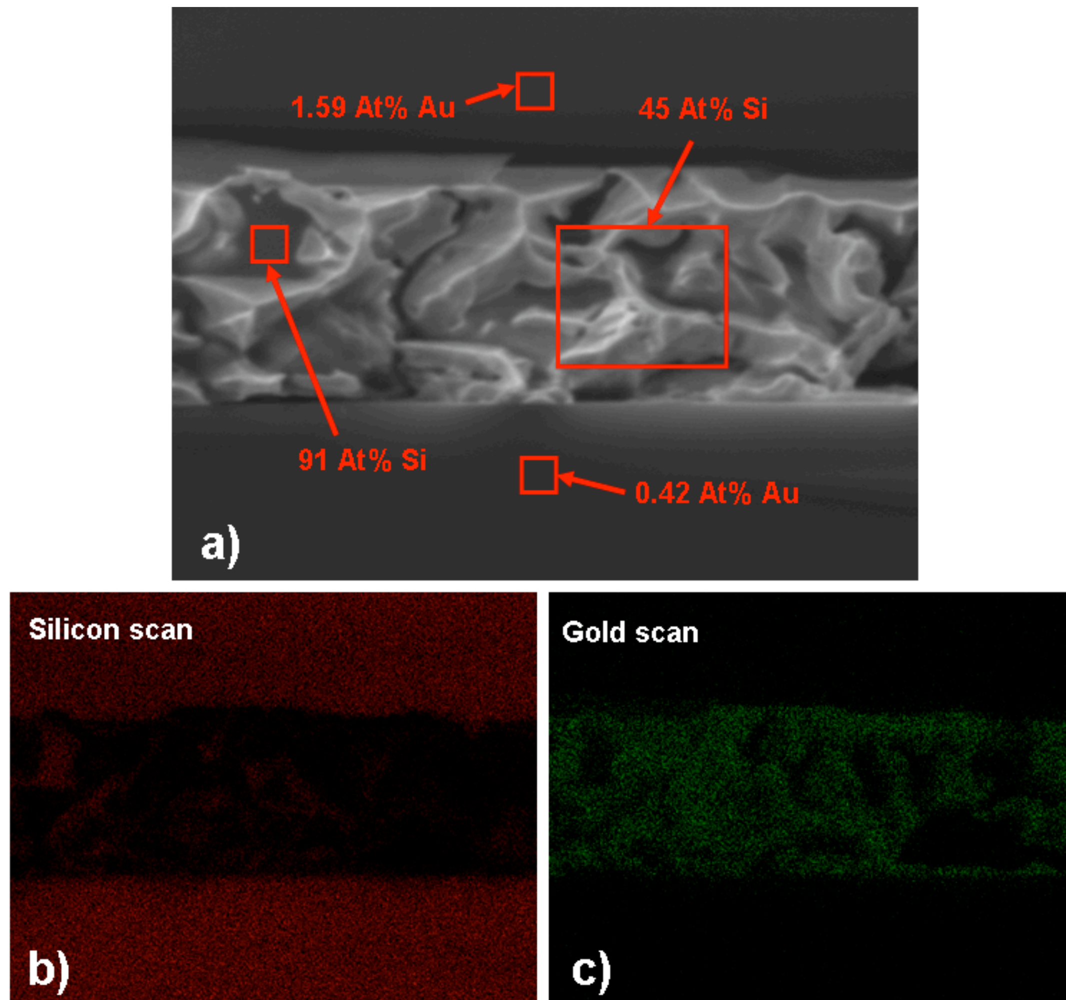


Figure A3.2: a) A cross-section of bond #56 showing the concentrations of Au and Si in different parts of the bond. A map showing the relative concentrations of b) Si and c) Au in throughout this cross-section.

In each of the cross-sections that were analyzed, a composition of around 50% atomic Si in Au was observed. At around 50 atomic %Si (12.5 weight %), using the lever rule [159] on the phase diagram in Figure A3.1, the bond ring should be approximately 59 atomic % (90.4 weight %) of the *Au-Si eutectic composition* and 41 atomic % (9.6 weight %) *pure Si.* Given this calculation of the amount of Au-Si eutectic and pure Si (Si precipitate) in the bond ring after the bond, the increase in volume can then be calculated. Table A3.2 shows the values needed to make this calculation. The values for the molar mass and molar volume of the Si and Au are the book values and those for the Au-Si eutectic were calculated using the rule of mixtures. Table A3.3 shows the calculations for determining the overall increase in volume of the bond ring assuming 50 atomic % Si

in Au for a bond ring that is originally 4μm thick, 300μm wide and encompasses a 2.3×2.3 mm area (the typical dimensions used in our bond experiments). As summarized in Table A3.3, the bond joints volume increases by 2.22 times where 61.5% of the bond joint is composed of Au-Si alloy and 45.5% is composed of Si precipitate by volume. As explained in section 2.1.1.3, there is in fact an increase in volume of the Au-Si eutectic portion of 1 to 2% [179] so that our total estimated volume increase is actually around 2.24 times. This volume increase is an important consideration and can potentially contribute to lateral flowing of the Au-Si alloy which can compromise the bond and/or the device being packaged. Such flowing of the Au-Si alloy is discussed in more detail in Section 2.5 (*Au-Si Eutectic Lateral Flow*).

Table A3.2: Constants need for calculation of the increase in volume of the bond ring during bonding.

Constants	Au	Si	Au-Si Eutectic
Molar Mass(kg/mole)	0.19697	0.02808	0.161
Molar Volume (m3/mole)	1.02E-05	1.21E-05	1.06E-05

Table A3.3: Calculations for the volume increase of the bond joint.

Constituents of the Bond Ring	Mass		Moles		Volume	
	(Kg)	% of initial	(unitless)	% of initial	(m^3)	% of initial
Au Bond Ring (before bonding)	1.20E-11	100%	6.09E-11	100%	6.22E-16	100%
Au-Si Eutectic (after bonding)	1.24E-11	103%	7.70E-11	126%	8.16E-16	131%
Si Precipitate (after bonding)	1.32E-12	11%	4.70E-11	77%	5.66E-16	91%
Total After (after bonding)	1.37E-11	114%	1.24E-10	203%	1.38E-15	**222%**

APPENDIX 4

THE EFFECTS OF THE RELEASE PROCESS ON BOND QUALITY

Table A4.1 shows three bonds to device wafers. These bonds were between cap wafers with 300 µm bond rings and device wafers with 0.3 µm thick poly-Si. Besides the added process steps for the feed-through interconnects and the Pirani gauges, the main differences in the processing of these wafers were: the cap wafers were anisotropically KOH etched and the device wafers were processed using a methanol hot plate release. The effects of having an anisotropically etched cap wafer are mostly in how the Au-Si alloy flows laterally from the bond joint because of this difference in geometry. This is described in more detail in Sections 2.5.2 (*Effects of an Anisotropic Etched Cavity*). On the other hand, as discussed in Section 3.3.1 (*Hot Plate Release*), hotplate release left a residue after evaporating away the methanol in some parts of the wafer and not in others. It was presumed that this residue could affect bond quality. Table A4.1 summarizes the bond parameters and Table A4.2 and detail the shear test results for bonds #71 and #78. As shown, for bond #71, 5 out of 6 of the samples passed the shear test with shear strengths ranging from 5.5 to 26.1. In this wafer, only a marginal amount of methanol residue was observed on the periphery of the wafer in pre-bond inspections. It is important to note that C10-R10, the package which did not pass was at the lower right edge of the wafer (see Figure A1.10 in Appendix 1 for a map of the packages across the wafer). For bond #78 on the other hand, only 2 out of 6 of the packages passed the shear test with shear strengths ranging from 0 to 22.9 MPa. As compared to bond #71, after pre-bond inspections on this wafer, a large amount of residue was observed across many parts of the wafer. The results from bonds #71 and #78 correlate well with vacuum data from these wafers which is presented in Section 5.3.3 of Chapter 5.

Table A4.1: Summary of bonds between cap wafers with 300µm wide bond rings to 0.3 µm thick poly-Si thin films. All of these were device wafer bonds which were conducted after a hot plate methanol release.

Au-Si to poly-Si (0.3 µm) bonds							
Bond #	**Cap Bond ring Thickness**	**Bonder**	**Intermediate Temperature Step**	**Bond Temperature Step**	**Bond Force**	**Cavity**	**Pass the Shear Test?**
67 (Device)	4µm	SB6	345°C, 60min.	390°C 40 min.	3.5MPa (1300N)	KOH	-
71 (Device)	4µm	SB6	345°C, 60min.	390°C 40 min.	3.5MPa (1300N)	KOH	5/6 (5.5-26.1MPa)
78 (Device)	4µm	SB6	345°C, 60min.	390°C 40 min.	3.5MPa (1300N)	KOH	2/6 (0-22.9MPa)

Table A4.2: Shear test results for bond #71.

Shear Test Results (Bond #71)			
Position	**Calculated Shear Strength (MPA)**	**Type of Failure**	**Pass/Fail**
C8-R14	26.1	Sheared in bond ring	Pass
C8-R13	14.9	Sheared in bond ring	Pass
C2-R4	22.9	Sheared in bond ring	Pass
C2-R3	26.1	Sheared in bond ring	Pass
C10-R10	5.5	Sheared in bond ring	Fail
C10-R9	15.0	Sheared in bond ring	Pass
Average Strength: 18.4 MPa			
Standard Deviation: 8.1 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table A4.3: Shear test results for bond #78.

Shear Test Results (Bond #78)			
Position	**Calculated Shear Strength (MPA)**	**Type of Failure**	**Pass/Fail**
C7-R11	22.9	Sheared in bond ring	Pass
C9-R9	19.6	Sheared in bond ring	Pass
C4-R1	11.8	Sheared in bond ring	Fail
C4-R2	11.8	Sheared in bond ring	Fail
C3-R5	3.9	Sheared in bond ring	Fail
C3-R4	0.0	Sheared in bond ring	Fail
Average Strength: 11.7 MPa			
Standard Deviation: 8.8 MPa			

*Details on the interpretation of this data are given in Section 2.2 and Appendix 1.

Table A4.4 and Table A4.5 show the parameters for several more device wafer bonds

to both 2.2 μm thick heavily phosphorous doped poly-Si and 0.5 thick Au thin films respectively. For each of these bonds, the cap wafers were also anisotropically KOH etched. The main difference in the processing of the wafers is that a CPD release (detailed in 3.3.2, *Critical Point Dryer (CPD) Release*) was used as supposed to a hot plate release. For all of these bonds, this resulted in no observable residue in pre-bond inspections. As summarized in Table A4.4 and Table A4.5 nearly all of the packages tested from these wafer passed the shear test (except for one from bond #101 which failed by only a small margin with a shear strength of 11.9 MPa).

Overall, from inspection, using the CPD process detailed in Section 3.3.2 seemed allow for a more consistently residue free device wafer surface. This appeared increase the uniformity of bond quality as compared to using hot plate release.

Table A4.4: Summary of bonds between cap wafers with 300μm wide bond rings to 2.2 μm thick heavily phosphorous doped poly-Si thin films. All of these were device wafer bonds which were conducted after CPD.

Au-Si to poly-Si (2.2 μm) bonds									
Bond #	Cap Bond Ring Thick-ness	Poly-Si Thick-ness	Device Bond Ring Width	Bonder	Inter-mediate Temp. Step	Bond Temp. Step	Bond Force	Cavity	Bond Strength
101 (Device)	4.5μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	KOH	5/6 (11.9-25MPa)
102 (Device)	4μm	2.2μm n-doped	300	SB6e	345°C, 60min.	410°C, 40min.	9.9MPa (3700N)	KOH	-
104 (Device)	4μm	2.2μm n-doped	300	SB6e	345°C, 5min.	410°C, 40min.	9.9MPa (3700N)	KOH	-

Table A4.5: Summary of bonds between cap wafers with 300μm wide bond rings to 0.5 μm thick Au thin films. All of these were device wafer bonds which were conducted after CPD.

Au-Si to Au (0.5 μm) bonds										
Bond #	Cap Bond Ring Thick-ness	Mat-erial Under Bond Ring	Pre-Bake for Au Depo-sition	Bond Ring Width	Bonder	Inter-mediate Temp. Step	Bond Temp. Step	Bond Force	Cav-ity	Strength
100 (Device)	4 μm	Ox/SiN	Yes	300	SB6e	-	410°C, 40min.	9.9MPa (3700N)	KOH	5/5 (18-21MPa)
103 (Device)	4 μm	Ox/SiN	Yes	150	SB6e	-	410°C, 40min.	9.9MPa (1850N)	KOH	-
105 (Device)	4 μm	Ox/SiN	Yes	100	SB6e	-	410°C, 40min.	9.9MPa (1230N)	KOH	5/5 (30-54MPa)

APPENDIX 5

LOW YEILD VACUUM RESULTS

In this section the yield was defined as the percentage of packages which held vacuum. Table A5.1 summarizes various bonds in which yields of less than 50% were achieved. All of these bonding results were made using processes which were determined in Chapter 2 to result in low quality bonds. Table A5.1 shows several of the important bond parameters, the approximate pressure ranges for successfully sealed devices, and the calculated yields.

Table A5.1: Bond Results where the Au-Si eutectic layer reacted with the getter.

Bond #	Device Bond Ring material		Bond Temperature	Getter	Release	Approximate Pressure Range	Yield
101	300 μm wide	2.2μm doped Poly-Si	345°C 0min. 410°C 40min.	Yes	CPD	~100-500mT*	24/55 (43.6%)
102	300 μm wide	2.2μm, doped Poly-Si	345°C 0min. 410°C 40min.	Yes	CPD	~50-4000mT*	11/39 (28.2%)
104	300 μm wide	2.2μm, doped Poly-Si	345°C 0min. 410°C 40min.	Yes	CPD	-	0/52 (0%)

*Calibrated using devices from other wafers in the same lot.

In bonds #101, #102 and #104, getters were used. In these bonds, there were issues with Au-Si eutectic spreading laterally onto the getters. This problem is described in Section 2.5.3 of Chapter 2. Because pressures were in the 100s of mTorr, the D3s gauges were used for pressure measurement. Figure A5.1 shows the calibration curves from bond #105 which were used for estimating the pressures across these wafers (these calibration curves are also shown and used in Figure 5.14 of Section 5.3.2 for the calibration of devices across bond #105). The plots in Figure A5.1 were taken from devices from the top, center and bottom of the bond #105 wafer. Bond #105 was

processed in the same lot as bonds #101, #102 and #104 and had similar R_0 (low current resistance) values.

Figure A5.2 shows the measured thermal impedances across bond #101 (left) and the estimated pressures calculated from those thermal impedances (right). The pressures listed were calculated using the average of the calculated pressure predicted from the two fit lines in Figure A5.1. Assuming that the thermal impedance vs. pressure curve of each device fits somewhere between the two fit lines in Figure A5.1, each of the estimated pressures were within ±50 mTorr of their actual value. As illustrated in Figure A5.2, the pressure range for successfully sealed devices was between 120 and 448 mTorr. Most of the devices though were at around atmospheric pressure. In all of the packages at atmospheric pressure which were later torn apart, it was observed that Au-Si alloy had spread laterally onto the getter. Similar results were observed for bonds #102 and #104. As shown in Table A5.1, these bonds demonstrated even lower yields.

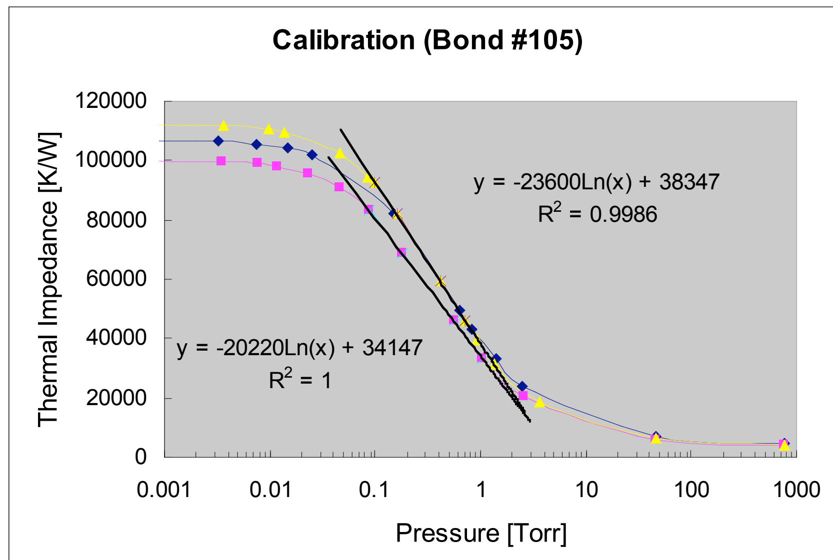
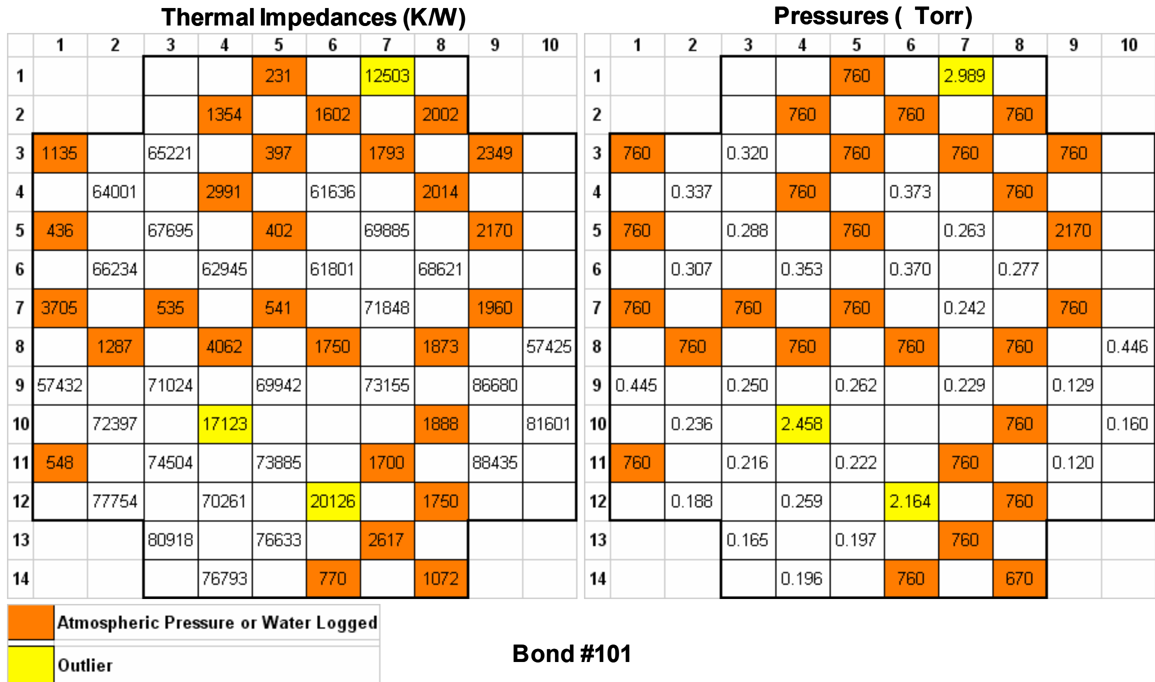


Figure A5.1: Calibration curves for Pirani gauges from D3s gauges from bond #105. The devices used for calibration were taken from the top, bottom and center of the wafer and are highlighted in Figure 5.15.



Thermal Impedances (K/W)

	1	2	3	4	5	6	7	8	9	10
1					231		12503			
2				1354		1602		2002		
3	1135		65221		397		1793		2349	
4		64001		2991		61636		2014		
5	436		67695		402		69885		2170	
6		66234		62945		61801		68621		
7	3705		535		541		71848		1960	
8		1287		4062		1750		1873		57425
9	57432		71024		69942		73155		86680	
10		72397		17123				1888		81601
11	548		74504		73885		1700		88435	
12		77754		70261		20126		1750		
13			80918		76633		2617			
14				76793		770		1072		

Pressures (Torr)

	1	2	3	4	5	6	7	8	9	10
1					760		2.989			
2				760		760		760		
3	760		0.320		760		760		760	
4		0.337		760		0.373		760		
5	760		0.288		760		0.263		2170	
6		0.307		0.353		0.370		0.277		
7	760		760		760		0.242		760	
8		760		760		760		760		0.446
9	0.445		0.250		0.262		0.229		0.129	
10		0.236		2.458				760		0.160
11	760		0.216		0.222		760		0.120	
12		0.188		0.259		2.164		760		
13			0.165		0.197		760			
14				0.196		760		670		

Figure A5.2: The thermal impedance measured on gauges across bond #101 (left) and the estimated pressures corresponding to these measurements (right).

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