Vacuum and Hermetic Packaging of MEMS Using Solder

by

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To Kate: Your love, dedication, and support made this possible.

To Connor (and everyone else with a curious mind): The key is to never stop asking questions.

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Chapter 1

INTRODUCTION

Micro-Electro-Mechanical Systems (MEMS) research started in the 1960s with a resonant gate transistor [1]. Researchers used a suspended bridge to modulate the current flowing through a transistor gate. Being the first to combine a moving mechanical structure with electronic components on the microscale, they broke ground in what was to become a fertile field of research.

MEMS are a system of mechanical, electrical, and other components that interact with physical and chemical aspects of the outside world and interface with integrated circuits (IC). Almost 50 years after the resonant gate transistor, MEMS have found their way into a variety of products spanning markets from national defense to automotive to consumer electronics. Figure 1.1 shows that the MEMS market is currently worth more than $6 Billion and projected to double in the next 5 years.
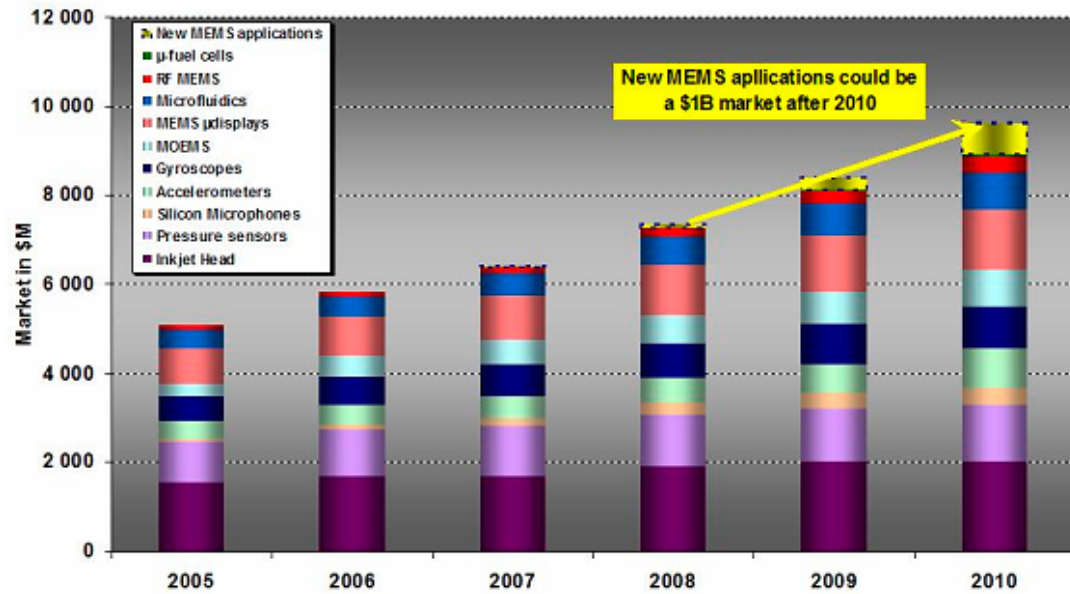
Figure 1.1: MEMS historical and projected sales by market segment [2].

Packaging is a critical component of the continued commercial success of MEMS devices. However, MEMS packaging is not a standardized process. Unlike ICs, which use very similar materials and contain no moving parts, MEMS devices rarely use the same materials and often have moving parts. This complexity results in specific custom packaging solutions that are only compatible with a certain process. With further research into MEMS packaging there is an opportunity to invent new packaging processes that are compatible with a wide range of devices and standardize MEMS packaging.

To that end, this research has explored the use of solder as a means of advancing the state of the art in MEMS wafer-level packaging (WLP). Figure 1.2 illustrates an overview of this work. Three processing technologies were developed: standard solder bonding, transient liquid phase (TLP) solder bonding, and a novel solder transfer technique. These process technologies were used to create two packaging systems: a wafer bonded vacuum package and transferred thin-film package.

Process Technologies   Packaging Systems

Standard Solder Bonding
Chapter 2

Wafer Bonded Vacuum Package
Chapter 4

Transient Liquid Phase (TLP) Solder Bonding
Chapter 3

Transferred Thin Film Package
Chapter 5

Solder Transfer Technique
Chapter 5
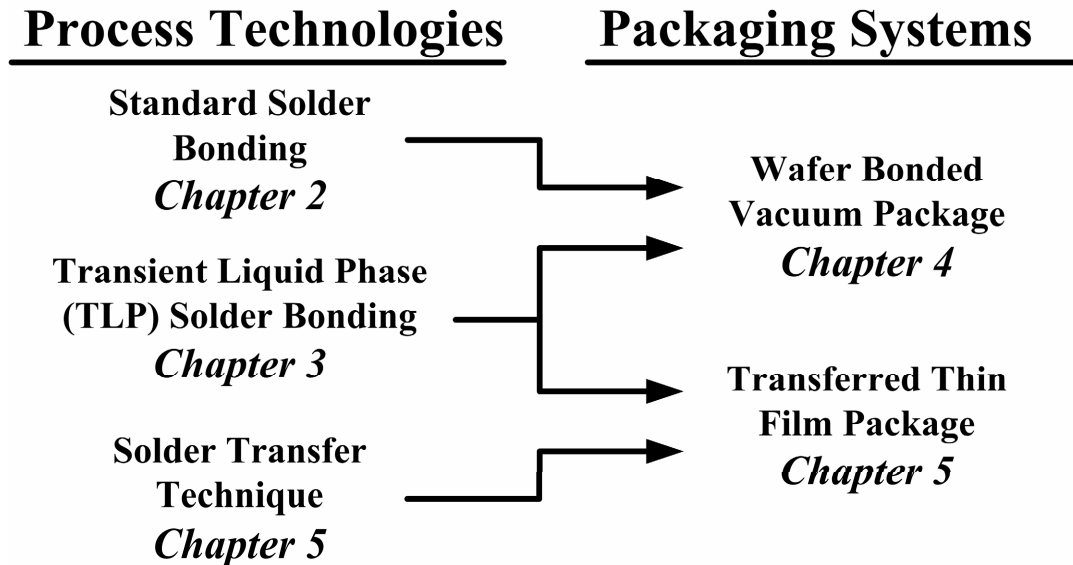
Figure 1.2 Visual Overview of the research presented in this thesis.

Solder has several attributes, such as its planarization capabilities, low permeability, and low processing temperature, which make it an attractive material for MEMS vacuum WLP. In this work, solder was used to develop two processes. The first is a wafer bonding process that uses solder as an attachment and sealing method. The second uses

solder as a method for transferring structures from one wafer to another. These two processes were used to create wafer level approaches for MEMS vacuum packaging.

The major contributions of this thesis are:

- A Au-Sn standard solder wafer bonding process technology compatible with commercial wafer bonding systems.
- Advanced solder bonding process technologies, transient liquid phase (TLP) solder bonding, based on Ni-Sn, Au-Sn, and Au-In material systems.
- Detailed characterization and understanding of standard solder bonding and TLP solder bonding that are presented as a set of design rules.
- Wafer-level MEMS vacuum packages created with standard and TLP solder bonding that have internal pressures lower than 20 mTorr and 10 months of vacuum data.
- Characterization of titanium thin-film getters at low activation temperatures.
- A novel solder-transfer technique that enables a transferred thin-film package technique with potential as a low-profile modular MEMS wafer-level vacuum package.

These results achieve three firsts for MEMS packaging:

- The lowest maximum temperature (200 °C) MEMS wafer bonded vacuum packaging process with integrated getters reported.
- The first application of TLP solder bonding to MEMS vacuum packaging.
- The first use of solder de-wetting as a transfer technique for MEMS structures.

The rest of this chapter provides a brief introduction to MEMS packaging process, typical packaging requirements, and three general packaging approaches. Then, several reasons for using solder in a vacuum packaging process. To close the chapter, the organization of the thesis is outlined.

1.1 MEMS Packaging

Micro-Electro-Mechanical Systems (MEMS) are the integration of mechanical structures and electronics on the μ-scale through μ-fabrication technology. With the addition of mechanical components to the electronics, the complexity of the system has increased exponentially because it has entered the multi-physical domain. The complexity of MEMS packaging has grown correspondingly to meet the new demands of the MEMS devices. A MEMS package serves four functions listed below:

1. Protect the device from the external environment
2. Provide the internal environment necessary for reliable operation
3. Allow it access to the information it needs to collect
4. Interface it with the other components

Figure 1.3 is an illustration of areas critical to MEMS packaging that highlights packaging of integrated circuitry, micromachined devices, and electrical and fluidic interconnects. The hermetic coatings and hermetic/vacuum-sealed cavity provide the necessary protection for the circuits and micromachined devices. The cavity also goes one step further: it not only protects the micromachined device from the outside environment, but also provides the necessary internal environment (in this case a vacuum) for reliable device operation. The integrated sensor outside the hermetic/vacuum-sealed cavity with the hermetic coating presents another common packaging challenge. It needs access to the outside environment as well as protection from it. A special hermetic coating over the sensor is needed to allow access to what it needs to measure while still protecting it from any contaminants in that environment. Finally, the electrical and microfluidic connects interface the system to the outside world.
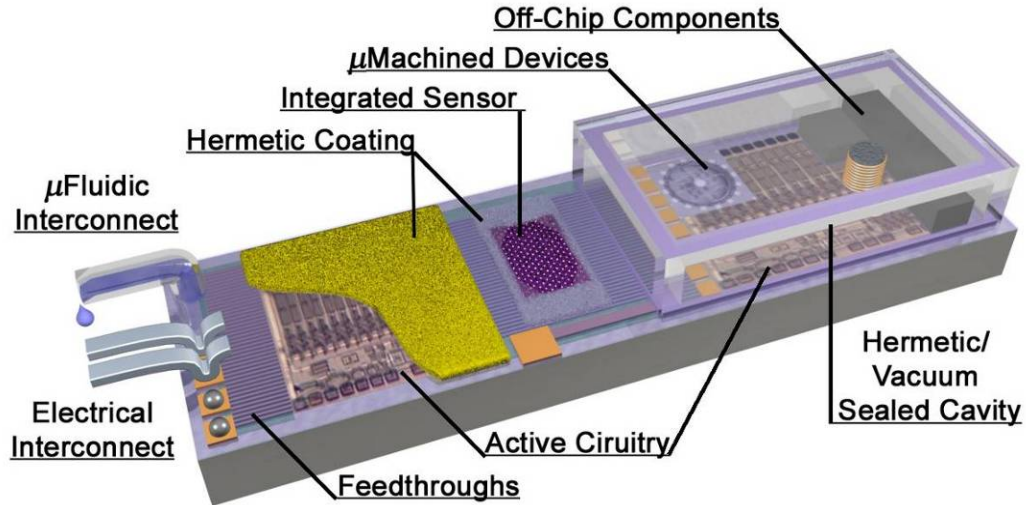
Figure 1.3 Illustration of a generic MEMS device [3].

This level of complexity, integrated electronics and several micromachined devices with feedthroughs is typical for MEMS. The package process design must balance the differing package requirements from each sub-part of the overall system to arrive at the optimal design. It is imperative that this design be considered from the beginning in order to ensure all the packaging requirements are met while maintaining process compatibility. Inevitably, some tradeoffs are necessary to satisfy all of the requirements. However, some flexibility is afforded the packaging engineer because not all the packages are created in a single step; packaging is a process with several steps and a hierarchy.

1.1.1 Packaging Process

The inherent complexity in MEMS packaging presented in the previous section can be simplified by breaking the packaging process down into distinct steps. Table 1.1 shows the packaging hierarchy for ICs with an added column describing a MEMS analogy. By splitting the packaging requirements into different hierarchical levels, the packaging engineer can limit the compromises that must be made to integrate the packaging and device process flows.

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Table 1.1 IC and MEMS Packaging Hierarchy (adapted from [4]).

Level	IC Element	MEMS Analogy	Packaged / Interconnected by
Level 0	Single transistor within an IC	Single valve in a MEMS	IC metallization, wafer-level protection, thin-films
Level 1	Complete IC	microGas Chromatography (µGC) separation column with integrated valves on the same chip	Wafer bonded, conventional lead frame packages, multi-chip module packages
Level 2	Single- and multi-chip packages	µGC column/valve chip integrated with chemical sensor chip	Printed wiring boards, microfluidic substrates, WIMS Cube
Level 3	Printed wiring boards	Printed wiring boards	Connectors/backplanes (busses), machined chassis or box
Level 4	Chassis or box	Chassis or box	Connectors/ cable harnesses
Level 5	System itself (a computer or a gas alarm)	Complete handheld µGC system	Connectors/ cable harnesses

The first three packaging steps are where most of the differences lie. This is because after Level 2, ICs and MEMS are almost indistinguishable black boxes of packaged chips with interconnections. Current MEMS packaging research is focused on the first three levels of the packaging hierarchy because it is in these first critical levels that the four MEMS packaging functions are achieved.

As mentioned previously, the first MEMS packages were made from off-the-shelf IC packages to save cost and time. Over time, as IC packages improved, MEMS packages also improved as they adopted the latest and greatest IC packaging developments (See Figure 1.4).
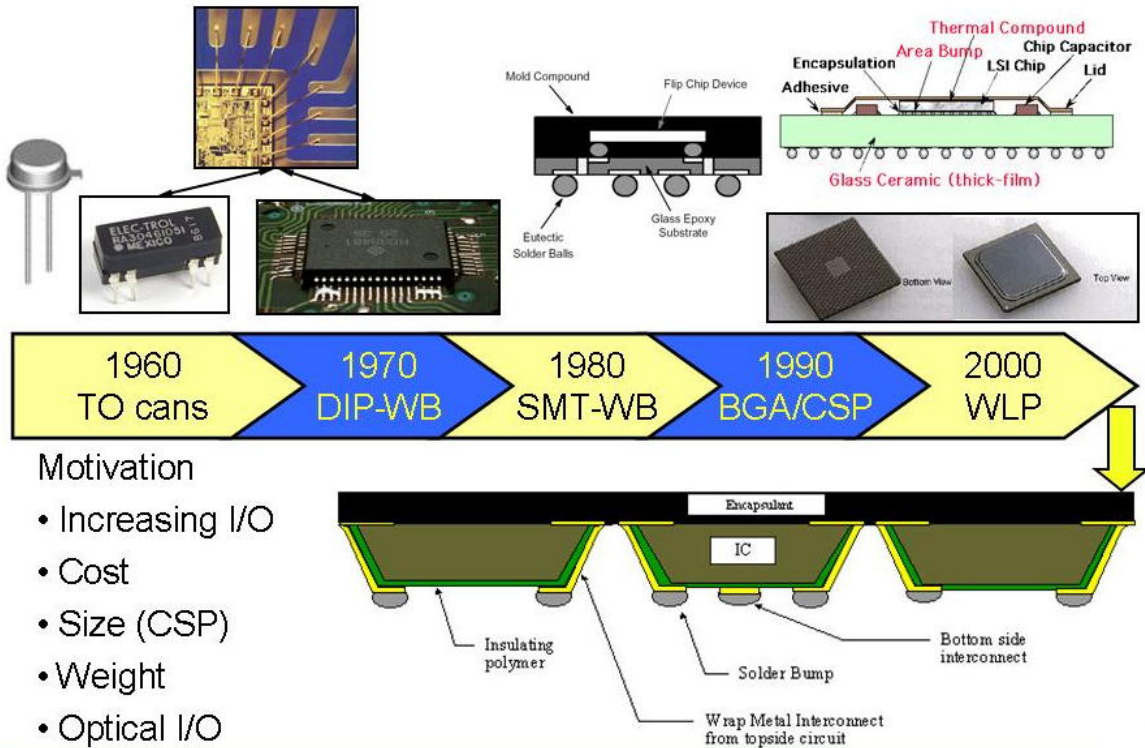
Figure 1.4 History of the evolution of IC packaging techniques [3].

The IC package developments were driven by cost savings through greater parallel processing as well as improved performance through higher input/output counts and better thermal performance. Over the years, these improvements had an impact on IC cost and performance; however, little of that impact translated to similar improvements for MEMS due to the added complexity of MEMS packaging. The greatest improvement for MEMS packaging came with wafer-level packaging (WLP). The shift of the early packaging steps (Levels 0 and 1), from individual die to when the wafer is still whole, has enormous benefits by reducing cost and size and increasing the performance of MEMS devices. This is evident when a process where singulation is performed before these early packaging steps is compared to a process where they are performed at the wafer level.
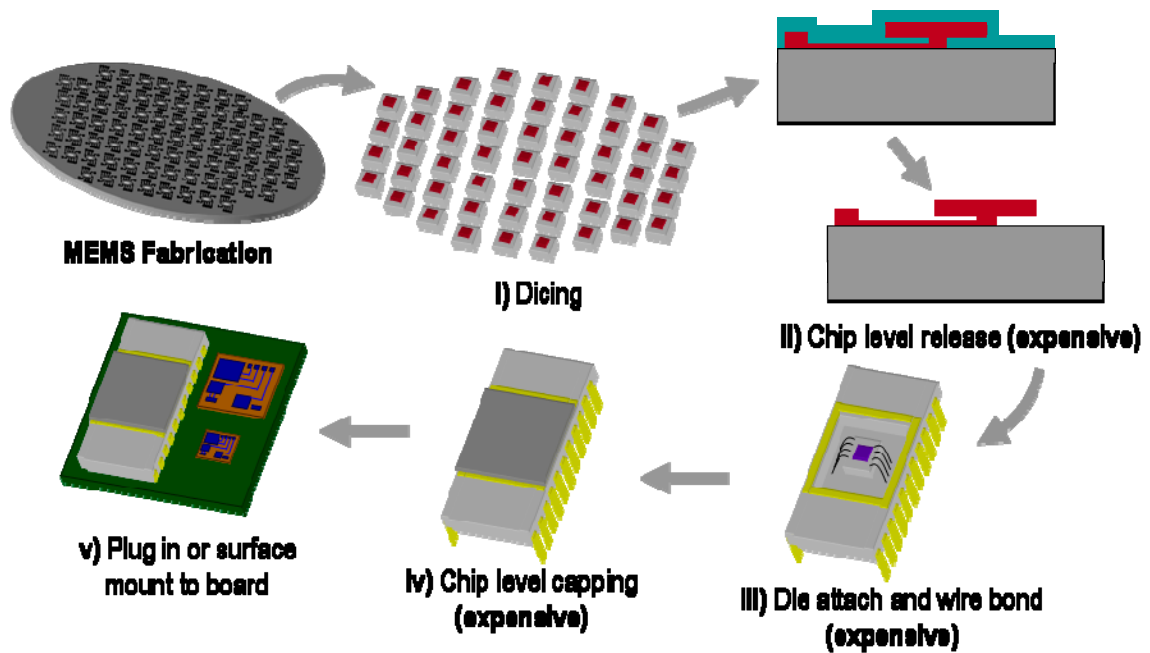
Figure 1.5 A singulation first package process [5].

Figure 1.5 illustrates a process where the dicing step precedes the release step. Right after the MEMS fabrication steps are complete, the wafer is sawed into individual die. After dicing, the individual dies are released. The release step must be performed after dicing or the water from the dicing saw would ruin any released MEMS device. Since release steps typically require long etches in a vaporized acid or an acid bath, the individual die can be released at the same time with special multi-die handling equipment. All the subsequent steps, however, are serial because only one die can be handled at a time. Performing these steps individually for each die increases the cost of MEMS packaging. Parallel processing is one of the greatest strengths of IC processing. With so many MEMS parts fabricated simultaneously, each expensive process step is divided by a large number to calculate the cost for an individual die, which brings the die cost down to a sustainable level. This advantage and cost savings is lost once the wafer is sawed into individual die because all the subsequent processing steps must be individually performed on each die. Another disadvantage of this processing technique is the large package size. The individual dies are usually placed in a package such as a metal can or a dual in-line package (DIP) (See Figure 1.4), which precludes their use in next generation cell phones and other handheld devices. For a release-first packaging process, the dicing step is delayed until much later in the process after each of the first two packaging levels

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has been completed. This delay produces a big cost savings and reduction in package size.

The release-first package process starts after the MEMS fabrication is completed, but instead of dicing the wafer next, all of the devices are released simultaneously while the wafer is still whole (See Figure 1.6).
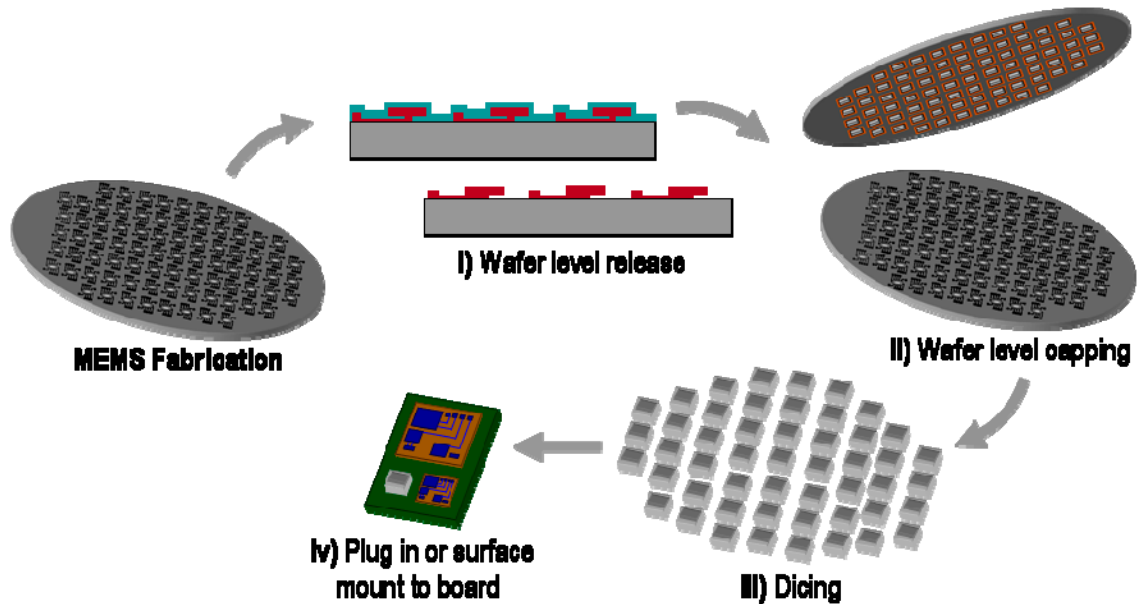
Figure 1.6 A release-first packaging process [5].

The released devices are then protected using a WLP technique such as wafer bonding or thin-film encapsulation. Next, the wafer can be singulated without concern for the fragile released MEMS devices; the encapsulation provided by the WLP technique protects them from the harsh environment during dicing. After dicing, the chips are mounted on a board similar to the chip-level packages. By using a release first packaging process, more of the packaging steps occur in parallel to all of the dies at once, instead of one by one as in a singulation first package process.

The cost and size advantages of the release-first process are balanced by the technical challenges of integrating a WLP technique with MEMS processes. There is great amount of research into wafer-level packaging techniques that can be integrated with MEMS processes and serve the four functions of MEMS packages.

1.1.2 Package Design Considerations

All of the different requirements, from process integration issues to final package specifications need to be addressed from the beginning of the packaging process. If the whole picture is not in view from the beginning, a problem could arise late that could require rethinking of the entire packaging approach. It is important that the packaging engineer be mindful of all of the issues that could arise during the process so they can be addressed with a packaging plan from the beginning.

PACKAGE SPECIFICATION REQUIREMENTS

Interconnections

One of the 4 main functions of MEMS packaging presented earlier was to interface the device with the outside world; interconnect or feedthrough are the generic terms applied these objects. Interconnects provide a path for charge or fluids to move from one place to another. With electrons, interconnects are usually made of metals or highly doped semiconductors that provide a conductive path into the package. The best materials for creating electrical interconnects are those with low resistivity. Metals such as aluminum or gold are widely used because they are excellent conductors.

Aside from electrons, fluids, such as gases in µGCs or liquids in DNA analysis chips, must also be transported from one region to another. Microfluidic interconnects provide the path for these fluids to move from one part of the system to another. These interconnects create a challenge not present in electrical interconnects because the fluids flowing down the interconnect are so varied. The materials for these interconnects should be chosen carefully to prevent any interaction between the interconnect walls and the fluid they are transporting. Another big issue with microfluidic interconnects is leakage, therefore, the quality of this seal is very important. There is plenty of research into different materials for microfluidic interconnects and creating leak-free seals. Be they electrical or fluidic, there are two major schemes for creating interconnects: the interconnects can be created laterally into the package by putting the interconnect on the surface of the wafer or, alternatively, they can be created through the bulk of the chip in a vertical manner.

Vertical or lateral, electrical or fluidic, interconnects provide communication between the packaged devices and the outside world. The required performance and process integration issues need to be considered by the engineer during the package design process.

Internal Environment

Another of the four functions of MEMS packages is to provide the internal environment necessary for the device to operate reliably. This requirement varies from device to device. It can be as simple as keeping the internal environment the same as the external environment or as difficult as creating a high vacuum inside the package cavity.

The most common requirement of the internal environment is to keep it moisture-free. Water vapor causes many reliability problems for MEMS and electronics components. Many MEMS devices cannot tolerate any water vapor at all and those that can need a constant level of water vapor to limit drift. To achieve this, the internal environment of the package must be isolated from the external environment with a hermetic seal. An effective hermetic seal will prevent the varying water vapor concentrations in the outside environment from making it inside the package and causing problems with the devices inside. A hermetic seal is also required to create a vacuum environment inside the package. The hermetic seal prevents the atmosphere from leaking into the package and raising the pressure inside. Creating a vacuum package is much more difficult that just creating a moisture-free environment. The challenges mainly lie in removing all the outgassing that occurs off of packaging materials during package formation. Vacuum packaging, its motivation, and its challenges are covered in great detail in Chapter 4 since they are such a large part of this dissertation.

The internal environment is an important consideration in the package design process. Most devices need a dry, inert environment to operate with long-term reliability and some even need a more stringent vacuum environment, but both these devices need a hermetic seal to preserve their necessary environments.

Size

Market demands are driving consumer devices smaller and thinner while still offering the same features. The package size is critical if MEMS are going to be deployed in these applications.

There are two main aspects of the size issue that need to be addressed when developing a packaging process: area and profile. The area of the package is the extra area needed outside of the MEMS device it takes to provide the four functions of a MEMS package. This could be due to die space reserved for bond rings if the package is created using wafer bonding, or, it could be needed to accommodate the bond pads necessary on a thin-film packaging approach. A disadvantage of extra area is cost. In wafer-level packaging, if you need to reserve die space to place the bond rings for a wafer bonded package, that space costs money. If you can reduce the space necessary for the bond rings by reducing the size of the bond rings, the overall die size becomes smaller so you can fit more die on each wafer. There is much research into wafer-level packaging techniques that reduce the size reserved for bond rings or use a thin-film approach, which does not need a bond rings at all and further reduces the added area from the package.

Another major aspect of the package size is its height. At Level 0 or Level 1 in the packaging process, there are still many packaging steps left that need to be able to fit around any packaging steps performed at these first levels. If the package used for Level 0 or Level 1 is very thick or tall, then the subsequent packaging steps must accommodate this thickness by being even thicker. If the package used for Level 0 and Level 1 can be fabricated with a low-profile technique, it keeps more packaging options open for the later steps while still keeping the overall package size thin.

Size, in terms of added area and profile, is an important aspect of package design. It can affect the cost of the packaged devices by using up precious die area or complicate subsequent package steps by creating extra thickness. Pushing the limits to scale packages smaller and smaller such that they barely add any size to a MEMS device is a major goal of packaging research.

External Environment

The environment that the package must sit in will drive many of the choices in the packaging process plan. There are many different environments, each with special requirements that necessitate different packaging approaches.

MEMS have many interesting application opportunities inside the human body. There have already been devices that can measure a single neuron firing, devices that monitor blood pressure inside an artery stent, and devices that monitor ocular pressure are under development [6]. The human body is a unique environment that necessitates careful package design [3]. The materials used to fabricate this type of package must be able to withstand the chemicals present inside the body. Long soak tests have shown that saline in the body can dissolve common MEMS materials, such as polysilicon [7]. Not only must the packages survive the harsh environment inside the body without failing, they also must avoid causing any harm to the body. There has been a large research effort to determine what materials are bio-compatible, such that they can be implanted without any adverse effects to the host.

Other environments are not as sensitive to the packages themselves, they cannot be harmed by them; however, they are much more harsh than a hot saline bath to the packages. Oil and gas exploration as well as automotive applications are two such environments. The package materials must be able to survive this harsh environment, as well as protect the sensors and electronics. Other applications in automotive, such as pressure and temperature sensors deployed inside an engine cylinder, can create similar temperatures and pressures as well as harsh chemical byproducts. Research into silicon carbide and other harsh packaging approaches is trying to address these issues [8].

Access to the Measurand

For a MEMS device to operate properly, it must have access to what it is supposed to measure. Sometimes, as in the case of RF or other electrical signals, the signals can be brought in with a feedthrough which shifts the packaging challenges to creating the interconnect. In other cases, as in a MEMS microphone, the sensor must have access to

the pressure levels outside the package, which can greatly complicate the package design.

Microphones need to be able to measure high frequency pressure components from the atmosphere and convert them into electrical signals. To do this, the microphone needs to be exposed to the atmosphere to measure the pressure signals. The issue is that elements of the atmosphere where microphones are typically deployed can be harsh and change often. There are contaminants, such as particles, water vapor, and harsh chemicals, which can lead to reliability issues for these microphones. Also, the atmospheric pressure changes constantly: absolute barometric pressure changes with the weather as well as the humidity. Both of these changes can cause drift or reliability problems if the package is designed improperly. If they are included in the packaging plan from the beginning, however, there are several packaging techniques that can solve or alleviate these problems.

Cost

As mentioned previously, packaging costs make up a significant fraction of the overall MEMS device cost. This is because a new MEMS package needs to be developed for almost every new device. This fraction has come down in recent years as some packaging processes become standard; however, there are still aspects of the MEMS packaging process that should be considered to keep packaging costs low.

Wafer-level packaging is the key to keeping packaging costs low. By splitting the large costs of MEMS fabrication among many die, the individual die costs remain low. Serial processes, such as wire-bonding, metal can packages, and others that occur at the die level, will increase the packaging costs significantly.

Another aspect of the cost issue lies in the die yield from the wafer. The yield can be defined as the number of die that pass a performance metric, known as good die, divided by the total number of die on the wafer. Yield loss causes cost increases in two ways: 1) if it is a failed die, you cannot sell it 2) if the yield is not 100% you must test every die to find the failed ones or risk shipping poor quality parts that need to be returned. For high volume applications, it is more cost-effective to forego testing each device and cope with

the issues surrounding shipping bad parts. To keep the costs associated with this tactic to a minimum, yield losses must be reduced to the order of parts per million.

Process Integration

MEMS device and package processing is based on CMOS processes developed by the IC industry. However, MEMS uses many materials not found in IC fabrication. There is very little set order to the steps, and there are moving structures present in the finished chips. All these factors add up to create many challenges in combining a MEMS packaging process flow with a MEMS device process flow. Two major challenges, thermal budget and release compatibility, are covered below.

Since there are many non-CMOS materials used, such as metals, there is a large constraint put on the temperatures that can be used for fabrication. Metals such as gold and aluminum react with silicon to form a eutectic combination at relatively low temperatures below 400°C. Even before reaching the eutectic temperature, solid-state diffusion between common CMOS materials and metals can cause unwanted electrical effects, such as shorts and opens that would destroy a circuit. Aside from metal-semiconductor interaction, exotic materials such as low-k dielectrics and polymers are also reducing the maximum temperature CMOS circuits can survive. Depending on the polymer used, the maximum temperature for a CMOS die will be reduced to 320 °C or possibly even lower [9].

The mechanical structures used in MEMS need to be released before they can work properly. This step usually involves a long wet-acid etch or dry etch to dissolve away a sacrificial layer that frees the mechanical layers. Typically the processing steps after the release step are limited because the released mechanical structures cannot tolerate any wet process steps due to stiction effects. Combining this release step with the package materials can be a challenge since many of the materials that are used for packaging are not compatible with long wet-acid etches. Either the packaging materials need to be able to withstand the long release in acid or they have to be added after the release step.

The wide range of different devices and their packaging needs makes it impossible to standardize the MEMS packaging process. However, a majority of packaging processes can be classified as one of three general approaches: integrated thin-film sealing, wafer bonding, and transferred thin-film. Table 1.2 compares the relative merits of the three generic approaches across several different metrics.

Table 1.2 Comparison of three generic packaging approaches.

Metric	Thin-Film Sealing	Wafer Bonding	Transferred-Thin Film
Process Integration	Difficult	Flexible	Flexible
Package Size	Small	Large	Small
Cost	Low	High	Low
Die Area Used	Low	Large	Medium
Further Packaging Complexity	Minimized	Low to High	Minimized

Integrated Thin-Film Sealing

The integrated, thin-film sealing packaging approach uses a thin film of material that is deposited over the device to encapsulate it. However, it is challenging to achieve this for a MEMS device because there needs to be a cavity for the MEMS device to operate in. This is accomplished with thin-film packaging by depositing a sacrificial material before the thin-film package is deposited. Figure 1.7 illustrates a typical process flow. After depositing and patterning the thin-film package layer, the sacrificial material can be removed through a hole in the thin-film package. This hole is then plugged using another thin-film deposition step. There have been many demonstrations of thin film packaging techniques over the years that have found unique ways to create packages with several different thin-film materials deposited with different methods [10].

1. Start with the device wafer   2. Deposit and pattern sacrificial material   3. Deposit and pattern thin-film package

4. Release by removing sacrificial material   5. Seal package with second film deposition
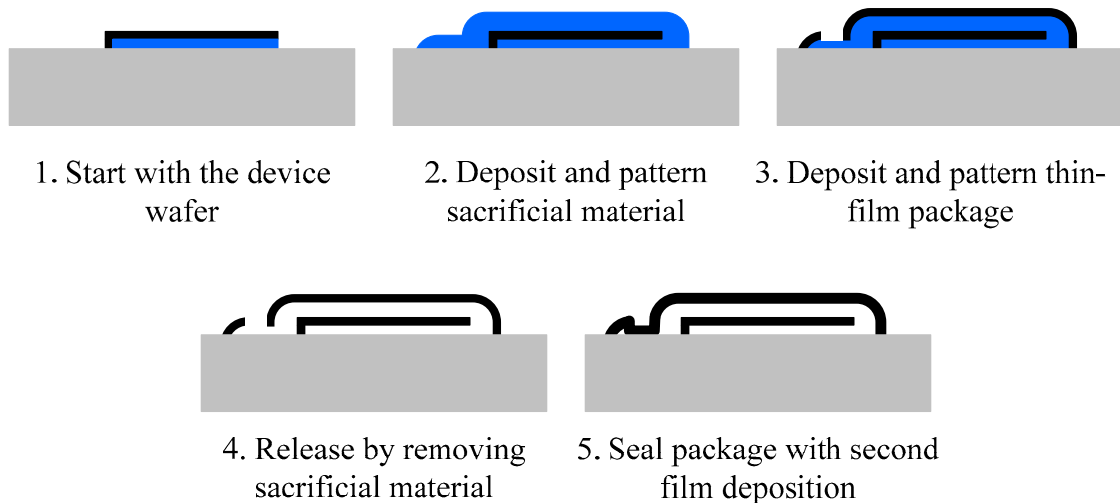
Figure 1.7 Generic process for integrated thin-film packaging.

Thin-film packaging has many features that make it an attractive choice for Level 0 packaging of MEMS. Recall from Table 1.1 that the Level 0 packaging is the step that packages individual devices. Individual MEMS devices can be very small, as small as tens of μms on a side. Thin-film packaging is appropriate for this size because it does not add much extra area for bond rings. A thin-film package requires only a ring approximately 10 μm wide surrounding the device to package it [10]; this is a substantial savings compared to a typical wafer bond ring size of several hundred. Thin-film packaging also maintains a low profile after completion. The thin film is typically 20-40 μm thick [11]; compare this to a wafer-bonded package, which has a 5-10 μm tall bond ring plus several hundred μms of wafer on top of it, making the package orders of magnitude taller. The low profile of thin-film packages enables much simpler integration of the packaged devices into total systems with subsequent packaging steps.

Thin-film packaging suffers from some disadvantages; most notably, it is a very process-specific packaging solution. The deposition of the thin film is typically a high temperature process that can only be integrated with certain process flows. The rest of the process needs to be adapted to the packaging step instead of adapting the packaging step to the process flow. This limits its use in many MEMS packaging solutions. For instance, CMOS circuits cannot be present on the wafers for the thin-film packaging achieved at higher temperatures because the elevated temperature causes the dopants to diffuse into

unwanted areas in the circuits. Even low-temperature, thin-film packaging processes suffer from process incompatibilities. Getters that are typically used in vacuum packaging are difficult to integrate into thin-film package processes because they need to be deposited on the package ceiling. If it can be integrated into process flow without compromising device performance, integrated thin-film sealing offers many size and cost advantages over other packaging techniques.

Wafer Bonding

The general approach for wafer bonding vacuum packaging is shown in Figure 1.8. The process starts with two wafers, one wafer with the devices on it and another blank wafer that will serve as the cap. Next, bonding material is formed on one or both wafers. Then a recess, or cavity, is etched into the top wafer that will form the final cavity housing the MEMS device. Finally, depending on the bonding technique used, the two wafers are bonded together by applying heat, pressure, and/or voltage.
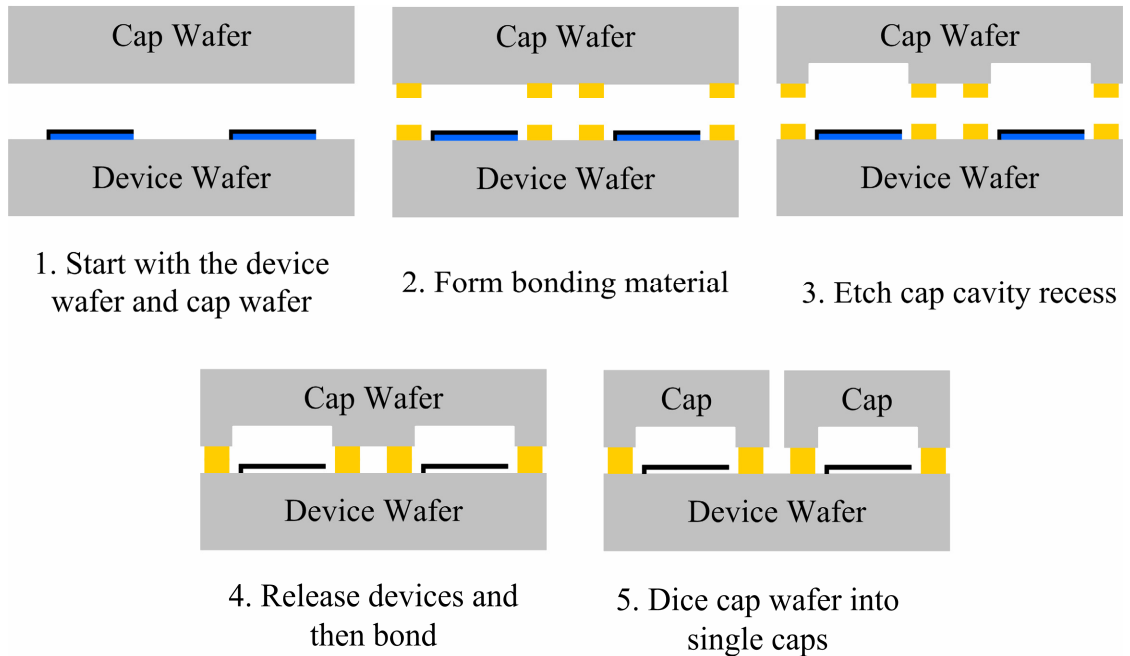
Figure 1.8 Generic process for wafer bonding packaging.

There are many different types of wafer bonding approaches available that can provide the protection or integration necessary for MEMS packaging applications (see Table 1.3). For some wafer bonding techniques, it is as simple as electroplating a few thin films onto

each wafer, integrating the getter, and then bonding the wafers together. The large number of bonding techniques at a range of temperatures give the package engineer some design flexibility when choosing a technique for the packaging process flow. The modular wafer bonding packaging approach offers much more flexibility compared to thin-film packaging which requires high-temperatures and a dedicated process flow.

Table 1.3 Comparison of different wafer bonding techniques.

Bonding Type	Temperature	Planarization	Hermeticity	References
Anodic	Medium-High	Poor	Fair	[12]
Fusion	High	Poor	Good	[13]
Eutectic	Medium-High	Good	Good	[12],[14]
Solder	Low-Medium	Good	Good	[12],[14]
Glass Frit	Medium-High	Good	Fair	[12],[15]
Polymer	Low	Good	Poor	[16]
Thermocompression	Low-Medium	Fair	Good	[17],[18]

All these techniques have been used to bond wafers together; however, not all of them are suitable for vacuum packaging. All polymers and some glasses are too permeable to provide the hermetic seal necessary for vacuum packaging over typical MEMS scales (see Figure 1.9), so wafer bonding for vacuum packaging has usually been achieved with anodic, fusion, glass frit, and metal bonding. More details on the different wafer bonding approaches are covered in Section 2.1.
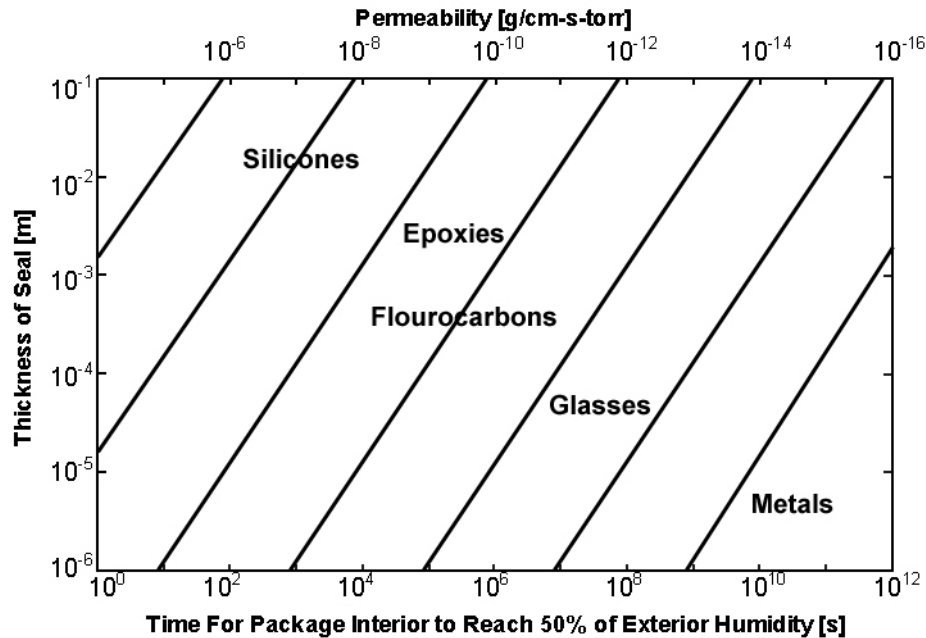
Figure 1.9 Hermetic performance of different material classes [4].

Wafer bonding vacuum packaging is a very flexible process that is easier to integrate into a process flow, but it suffers from some drawbacks: The bond rings take up a large amount of die area and the final product is a large multi-wafer stack. Also, the proven wafer bonding techniques, such as anodic, glass frit, and eutectic bonding, all require temperatures of 350 °C or higher. There is need for further research into lower temperature wafer bonding techniques for packaging thermally-sensitive devices.

Transferred Thin-Film

A newer packaging approach that combines some of the advantages of each of the two major packaging approaches has received some research attention lately [19]. A transferred thin-film package offers the low-profile of the thin-film packaging approach with the process flexibility of the wafer bonding approach. Unlike previous thin-film packaging approaches, a transferred thin-film package can accommodate getters in the process flow and can be realized with many low temperature bonding techniques.

Figure 1.10 shows a generic process flow for a TTF packaging approach. The process starts with the device wafer and a carrier substrate that will hold the package caps before they are transferred. A release layer is prepared on the carrier wafer. Then the package

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caps are created on top of the release layer. Next, a bond ring is prepared on the device wafer and/or the carrier wafer full of packages. Finally, the packages are bonded and transferred to the device wafer using a wafer-bonding technique combined with a package transfer technique.

1. Start with the carrier wafer and cap wafer

2. Deposit the release/ sacrificial material

3. Form the package caps on the carrier wafer

4. Form the bond material and then release devices

5. Bond and transfer package caps
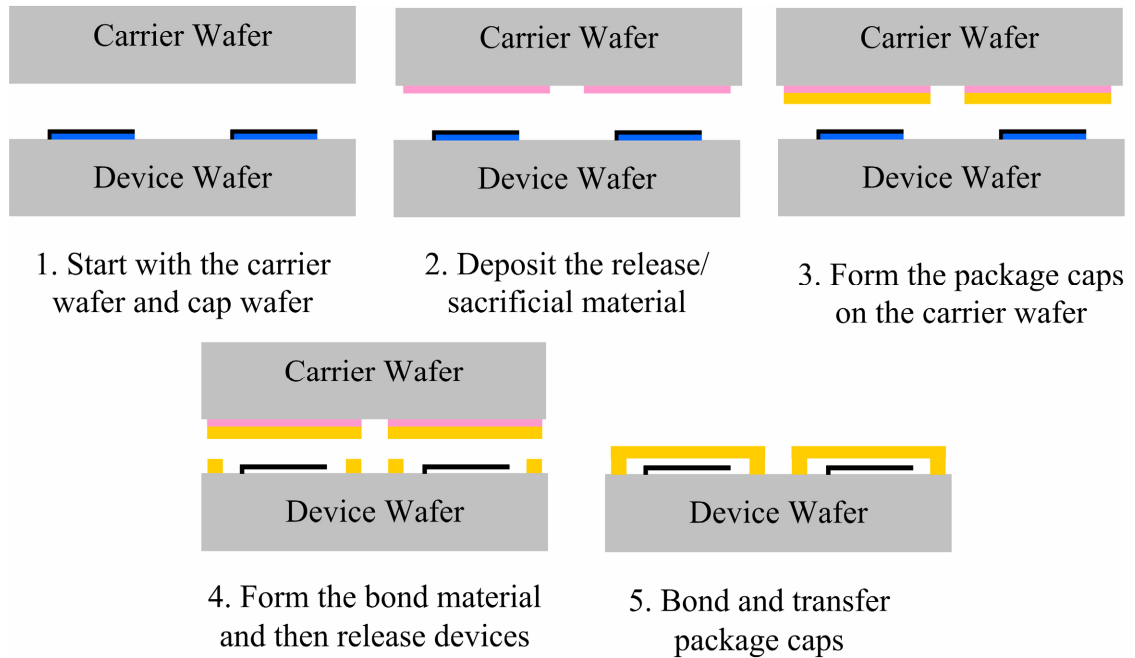
Figure 1.10 Generic process for transferred thin-film packaging.

Transferred thin-film packaging is an excellent candidate for 0-level MEMS packaging. It builds upon the inherent advantages of thin-film packaging, namely a low-profile and small size, by adding the modularity of wafer bonding. A transferred thin-film package can be adapted to many process flows to provide protection for MEMS devices, but much work needs to be done. Transferred thin-film packaging is an unproven technology. More research is needed to integrate getters, characterize different sealing bonds, and test the reliability of the packages. Solder has some interesting properties that make it an attractive material for accomplishing both the wafer bonding and transfer necessary for a transferred thin-film packaging process.

1.2 Solder for Vacuum Packaging

Solder is a low melting point metal alloy (< 450 °C), typically containing tin or indium, which is used to join two metal surfaces together [20]. The solder acts as metal "glue"

that adheres to each metal surface and holds them together. Solder has several advantages that make it a good material for MEMS vacuum WLP.

First, there are many different solder alloys that melt at temperatures ranging from near room temperature to several hundred degrees Celsius (Table 1.4). The range of solder melting temperatures offers some thermal flexibility to the designer of a packaging process. As mentioned previously, all of the wafer bonding processes require temperatures of 350 °C or higher. There are many solders that melt at temperatures well below 350 °C that could be used as wafer bonding techniques.

Table 1.4 Several widely used low melting point solder alloys [20].

Composition, wt %							Eutectic
Ag	Bi	In	Pb	Sn	Au		°C
…	49.0	21.0	18.0	12.0	…		57
…	57.0	…	…	43.0	…		139
3.0	…	97.0	…	…	…		144
…	…	99.4	…	…	0.5		156
…	…	…	38.0	62.0	…		183
3.5	…	…	…	96.5	…		221
…	…	…	…	20	80		278

Second, solders can planarize over wafer topography similar to the industry standard technique glass frit. A major source of topography in MEMS packaging is lateral feedthroughs that provide interconnection to the packaged MEMS. Direct bonds, like anodic and fusion, cannot seal over any topography greater than 100 Å. Bonds that are liquid or semi-fluid during the bonding process will flow over and conform to topography, which is a major advantage for a bonding technique if it will be used for packaging.

Third, solders are made of the best material for creating vacuum packages, metal. Figure 1.9 shows that as a material class, metals provide the greatest hermetic capability per unit thickness. This is advantageous for creating MEMS vacuum packages with scaleable bond rings. Metals will still provide the hermetic seal that is necessary to maintain good pressure levels for MEMS vacuum packages even as the bond ring widths get very small. No other material class is as effective at providing hermetic seals.

For these reasons, different solder processes were developed and applied to create MEMS vacuum packages in this these. The next section gives an overview of the material presented as part of this research.

1.3 Thesis Organization

The goal of this thesis is to investigate uses of solder as a MEMS vacuum WLP material. The results from this effort are organized in the following manner:

Chapter 2 presents the background science of solder and the development of a solder wafer bonding process that is compatible with a commercial wafer bonder. The lessons learned from these wafer bonding efforts led to a successful implementation of a Au-Sn solder bond with good strength and hermeticity results.

Chapter 3 presents an advanced type of solder bonding, called transient liquid phase (TLP) solder bonding. This bonding technique is more compatible with the long thermal time constants of commercial wafer bonders and was therefore more successful than the standard solder bond in producing vacuum results. The Au-Sn, Ni-Sn, and Au-In TLP solder material systems were all investigated as wafer bonds for MEMS vacuum packages. Their strength, hermetic, and re-melting results are all presented as well as a section detailing the design rules for TLP solder bonding.

Chapter 4 covers the use of the standard and TLP solder bonds in creating vacuum packages. The motivation for vacuum packaging several classes of MEMS devices is covered. Some of the background science that explains the difficulties in creating MEMS vacuum packages, such as outgassing and getters, is reviewed. Two different Pirani gauges were used to make the pressure measurements in the vacuum packages. Finally, the vacuum data and some interesting low-temperature getter activation data are presented.

Chapter 5 explains a novel solder transfer process and its application in a transferred thin-film packaging process. The transfer process is combined with a TLP solder bond to transfer thin electroplated films from a carrier wafer to a device wafer. Several challenges

in creating a vacuum package with this technique are covered, including process integration challenges and thermal coefficient of expansion stress issues.

Chapter 6 includes the conclusion and outlines proposed future work in MEMS vacuum packaging with solder.

Chapter 2

WAFER BONDING USING STANDARD SOLDER

Solder has been used since antiquity to bond two metal surfaces to one another at relatively low temperatures (150-300 °C). Modern electronics make use of solder as a bonding mechanism at many points during the assembly process: solder is used to form the interconnections and mechanical attachment between a chip and a PC board with a ball grid array, between dual-inline packages (DIP) and a PC board, and to attach wires in electronic systems. Despite solder's widespread use in electronics manufacturing, it has only recently been used for MEMS packaging [10]. As mentioned in the introduction, solder has several properties that make it an interesting candidate for MEMS wafer-level packaging research. Its low melting point, planarization capabilities, and low permeability give solder several advantages over other wafer bonding techniques for creating low-temperature scalable vacuum packages. The following sections discuss the fundamentals of a typical soldering process, some challenges that were faced in using it to create wafer bonds, and results from a wafer-level Au-Sn solder bonding process.

Section 2.1 briefly reviews wafer bonding technologies and compares them to solder bonding technologies. There are many different types of wafer bonding that can be used to create vacuum packages, but solder bonding offers several advantages that make it a unique approach among all others.

Section 2.2 reviews the basics of general solder bonding theory, such as wetting, intermetallic formation, and fluxless soldering. The process details of a standard solder bonding process are also covered, such as the reflow profile and bonding environment.

Section 2.3 covers the solder bonding experiments that were carried out as part of this work, including the shortcomings of the wafer bonding equipment used in the experiments. The results are summarized in Table 2.1. The long thermal-time constant of

standard commercial wafer bonding tools made applying standard solder bonding techniques to MEMS processes challenging. Several materials were explored to achieve reliable solder bonding on the wafer scale. In the end, only Au-Sn solder proved to be a reliable, robust wafer-level solder bonding technique that is suitable for MEMS vacuum packaging.

Table 2.1 Summary of experimental results for standard solder bonds. Only the Au-Sn solder bond shows promise for MEMS wafer level vacuum packaging with standard commercial wafer bonders.

Exp. #	Solder	Metallization	Hermeticity	Strength	Notes
1	Pure-Tin	Cr-Ni-Au	N/A	N/A	Bond failed due to nickel consumption
2	Pure-Tin	Cr-Ni-Au	N/A	Stronger than Pyrex™	Thicker electroplated nickel layer survived bond cycle
3	Pure-Tin	Cr-Mo-Au	N/A	N/A	Solder de-wetted molybdenum
4	Gold-Tin	Cr-Au	$1.5 \cdot 10^{-15}$ atm·cc·s^{-1}	28.0 MPa Shear	Bond Successful

2.1 Wafer Bonding Techniques

Wafer bonding is an important process in creating MEMS structures. Over the past decades, there has been a great deal of research effort into various wafer bonding techniques. The major techniques are compared in Table 2.2. In the following sub-sections, those techniques that are suitable candidates for vacuum packaging are briefly described along with their corresponding advantages and shortcomings.

Table 2.2 Comparison of various wafer bonding approaches across several metrics.

	Anodic	Fusion	Glass Frit	Eutectic	Solder	Parylene	PDMS
Bond Strength	Very Strong	Excellent	Strong	Strong	Strong	OK	Weak
Hermeticity	Good	Excellent	Good	Excellent	Excellent	Poor-OK	Poor
Temperature							
Formation	250-400 °C	200-1000 °C	400-500 °C	> 363 °C	57-400 °C	230 °C	R.T. – 90 °C
Service	> 400 °C	> 1000 °C	< 400 °C	< 363 °C	<< formation	<< 230 °C	< 90 °C
TCE Mismatch	OK	Good	OK	OK	Poor	OK	OK
CMOS Compatible	OK	Poor	OK	OK	Good	Good	Good
Planarization Capability	Poor	Very Poor	Good	Good	Good	Good	Good
Maturity	Decades	Many Years	Many Years	Many Years	Years	New	Years
Cost	$	$$$	$$	$$$	$$	$$	$

2.1.1 Anodic Wafer Bonding

An anodic bond is formed between a glass wafer, usually Pyrex™ type 7740, and a silicon wafer. The wafer pair is heated and then a large electric field is applied across the wafer stack. The heat increases the mobility of sodium ions in the glass, which will then move because of the applied electric bias. The mobile sodium ions at the interface between the glass and silicon leave behind an unsatisfied bond that is filled by a silicon atom from the silicon wafer.

Anodic bonding is a very mature bonding technology that produces uniform, reproducible, robust bonds [21]. The resulting bonding strength is limited by the fracture toughness of the Pyrex™ wafer, making it one of the strongest wafer bonding methods available.

For all of its advantages, it is limited as a vacuum packaging technique because of the constrained material choices and poor planarization capabilities. For an anodic bond to take place, the bonded wafer pair must include a glass layer. Glass is not optimal for creating scaleable vacuum packages because of its relatively high permeability (Figure 1.9). Also, anodic bonding has difficulty conforming to wafer topography. There is a small amount of planarization capability afforded by the large forces from the applied electric field, but the capability is not great enough to create a hermetic seal over typical lateral electrical feedthrough dimensions, which are usually > 1000 Å thick. An advanced

hybrid anodic gold-silicon eutectic bond approach has been developed to provide more planarization during the anodic bonding process to accommodate lateral feedthroughs [3].

2.1.2 Fusion Bonding

A fusion bond creates an uninterrupted bond between two silicon wafers or a silicon and glass wafer [22]. The surface of each wafer is activated either chemically [23] or with a plasma treatment [24], then placed in contact with one another and heated. The wafers are heated to 1000 °C for chemically-activated fusion bonds and the wafers are heated to approximately 400 °C for plasma-treated bonds.

Fusion bonds create excellent hermetic seals because, as long as there is no wafer topography and the wafers are completely flat, there is a continuous single-crystal material across the bond joint. Fusion bonding is even worse at conforming to topography then anodic bonding because there is not an extra force from an applied electric field forcing the wafer surfaces together as there in anodic bonding. Fusion bonding is rarely used in MEMS wafer-level packaging due to its lack of planarization capabilities and high temperature requirements.

2.1.3 Glass Frit Bonding

Glass frit is a low melting-point glass paste mixture that is used as an adhesive to attach two wafers to one another [25]. The frit is applied to one of the wafers using a screen printing method, then it undergoes several thermal treatments to remove all the organic solvents and form a continuous glass film. The wafer with the frit is then aligned with the other wafer and both are heated to the transition temperature of the glass frit while some force is applied to the bond stack. The frit softens from the heat and forms to the second wafer's topography from the force. The wafer stack is then cooled down to complete the bond.

Glass frit is a reliable, robust, reproducible wafer bonding technique that has become the industry standard for MEMS vacuum and hermetic packaging [25]. It is so widely used because glass frit creates a robust bond that can conform to wafer topography, allowing for the use of lateral feedthroughs in and out of the package. Given that frit is an

insulating material, another major benefit is that there is no need to deposit a separate dielectric over the conductive feedthroughs to insulate them from the bond ring. This greatly simplifies the manufacturing of the packages compared to other bonding techniques that need an extra insulating layer between the bond ring and lateral feedthroughs.

Glass frit is presently the industry standard, however, there are several limitations that will make it a less attractive technique in the future. Most of the low melting-point glass frits contain lead to reduce their melting point [26]. The inclusion of lead is a major drawback because it generates environmental concerns. Currently, there is legislation in the European Union and Japan that bans the importing of any electronic materials with lead used in the manufacturing process [27]. Also, low melting-point glass frit still requires relatively high temperature process steps, sometimes as high as 600 °C. There are many future applications that cannot tolerate such temperatures. Lastly, scaling glass frit bond ring widths is challenging for two reasons: the application method, screen-printing, is limited to about 150 μm for high-yield bonding [26] and creating a vacuum package with such thin layers of glass is not feasible due to the permeability of glass (Figure 1.9).

2.1.4 Eutectic Bonding

A eutectic bond is named for the eutectic composition of silicon-gold (3.9 wt%) that melts at 363 °C. It is formed by depositing gold onto a wafer with a source of silicon, which could be in a single crystal form from the same wafer, another wafer, or in the form of polysilicon or amorphous silicon. The silicon is put in contact with the gold by putting the two wafers together and the whole assembly is heated past the eutectic point. Once everything reaches the eutectic temperature, the silicon diffuses into the gold and vice-versa to form the molten eutectic compound. The liquid eutectic flows over wafer topography, such as feedthroughs and particles, and attaches the two wafers to one another. Upon cooling, the eutectic composition forms the majority of the phases left in the joint and acts as metal "glue" holding the two wafers together.

Many advances have been made recently in using a eutectic bond as a wafer-level

vacuum packaging technique [3]. It is well suited for this purpose because, just like many solders, it can form a hermetic seal with very small dimensions as well as flow over and seal topographies. The two major limitations of eutectic bonding are its rigid temperature requirements and its need for a dielectric to insulate the conductive bond ring from electrical feedthroughs.

2.1.5 Solder Bonding

Solder bonding has found use as a wafer bonding mechanism only recently [10]. It is very similar to eutectic bonding, in that it acts as metal "glue" holding the two wafers together. Unlike eutectic bonding, however, there are many different solder bonds that melt at a range of temperatures spanning from 50 to 300 °C. This makes solder unique among bonding techniques. It is the only *low-temperature* wafer bond that can conform to wafer topography as well as create high-quality hermetic seals with small dimensions.

There are many challenges to creating a quality wafer bond using solder. The following sections present an overview of a solder-bonding process, discuss some challenges and results from applying it to wafer bonding, and present some results from the one alloy that yielded positive results, Au-Sn Solder.

2.2 Solder Bonding Theory

A typical soldering process starts with three separate materials in contact: material A, the solder alloy, and material B (see Figure 2.1). When the whole assembly is heated, the solder melts and spreads over, or wets, the surfaces of material A and material B. In its molten state, the solder also reacts with those materials to form intermetallic compounds (IMC). After the solder wets both surfaces, the assembly is cooled down and the solder bond is complete. The low melting point alloy still exists in the solder joint, so the service temperature of the assembly cannot exceed the bonding temperature (i.e. the melting temperature of the solder) or the solder will melt again and compromise the integrity of the joint. The following sections discuss how to achieve good wetting without fluxes, under bump metallizations, a typical solder bonding profile, and the bonding environment.
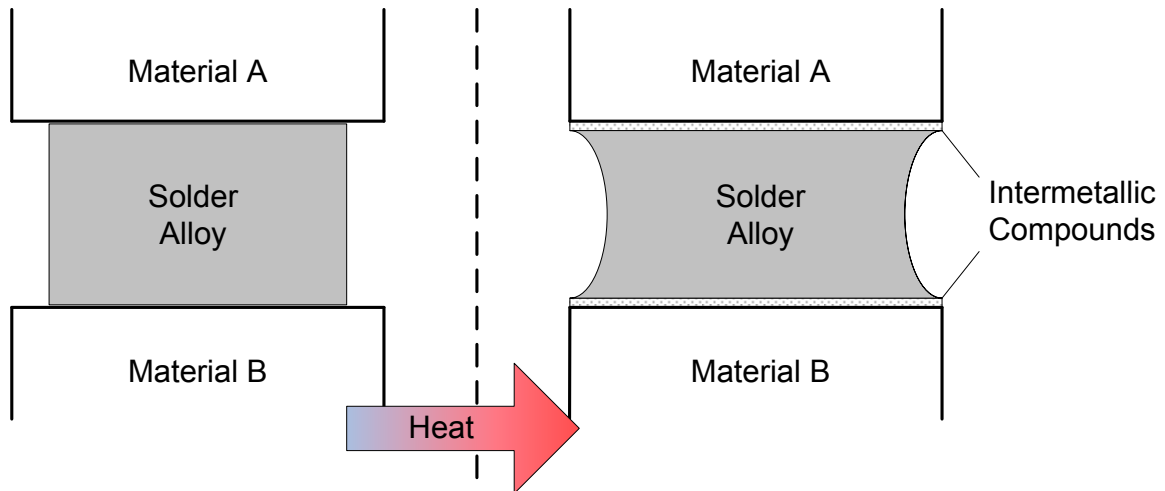
Figure 2.1 Illustration of the solder bonding concept. Heat applied to the solder causes it to melt and spread over Materials A&B.

2.2.1 Achieving Good Wetting without Fluxes

WETTING

To understand the behavior of solder, it is necessary to understand how it behaves as a liquid. Most of the action in a soldering process happens during its liquid state. The behavior of the solder in its liquid state is dependent on the surface energies of the materials present in the solder joint. Good wetting occurs when the relative surface tensions of the solder and solder parent metal interface create a force that causes the liquid solder to spread across the surface of the solid.

Each material has a certain surface energy that is determined by the free energy from the unsatisfied bonds of the atoms on the material's surface [20]. This surface energy creates a surface tension force that keeps the liquid together. Consider the case of a drop of liquid sitting on a solid surface in a vacuum (Figure 2.2). The relative surface tensions of the materials determine the contact angle and spreading characteristics of the droplet. A contact angle of 180° means the droplet of liquid is sitting as a perfect sphere on the solid surface. The surface tension of the solid (γ_{SV}) is much less than the surface tension of the solid-liquid interface (γ_{SL}) in this case because the drop has spread over the surface to form a contact angle of less than 90°. A contact angle of 0° means the liquid is spread infinitely thin and covers the entire surface of the solid. The definition of 'to wet' for

soldering purposes is a contact angle of less than 90°. The lower the contact angle, the greater the spreading effect. This contact angle and spreading effect during bonding will determine the quality of the final solder joint because the solder must uniformly spread over the surfaces of the materials to form a strong bond to them.
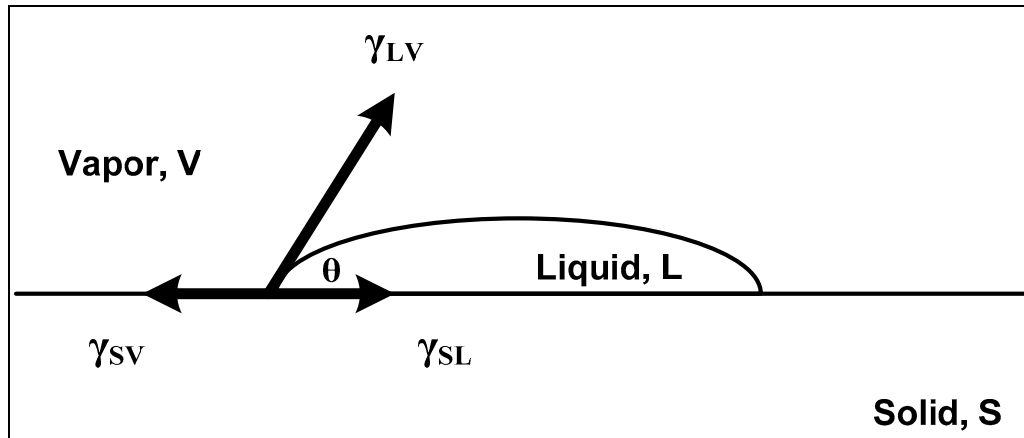
Figure 2.2 The relative surface tensions of the solid, liquid, and solid-liquid interface will determine the contact angle of a drop of liquid on a solid surface.

FLUXES

Many pure metals have a high surface tension (γ_{SV}), but their oxides do not. If molten solder is in contact with many pure metals it will easily spread over the surface of that metal and form a good bond. However, most metals react with the oxygen in the atmosphere to create native oxides on their surface that prevents good wetting [20]. Fluxes are highly reactive materials that are used in almost all soldering processes to ensure good wetting. During the soldering process, fluxes remove the native oxide and other contaminants from the bonding surface as well as the surface of the solder. Once the oxide and contaminants are removed, good wetting is possible because the pure metal surface is exposed to the solder and the pure metal's high surface tension ensures good wetting.

Fluxes are a good method to achieve proper wetting and a reliable solder joint, but they are not compatible with MEMS processing. First, the liquid flux can cause stiction issues with released MEMS devices. The liquid could flow into tiny gaps between the released MEMS device and the substrate, thereby ruining the device. Second, fluxes

leave residues. Figure 2.3 shows a picture of the residue left behind after the solder process has been completed. This reside will cause major long-term reliability problems for MEMS devices by outgassing that would ruin a vacuum and corroding metal layers. Therefore, only flux-free soldering processes are compatible with MEMS vacuum packaging processes.
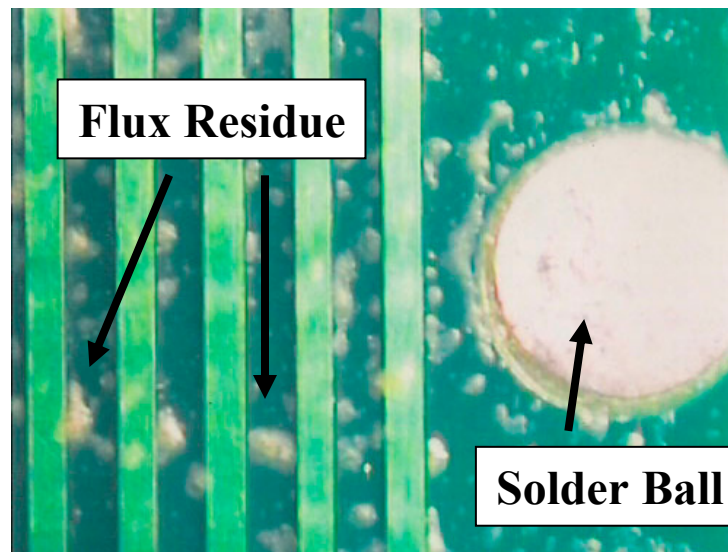
Figure 2.3 Fluxes are normally used in solder processes, but the residues they leave behind preclude their use in a MEMS soldering process [20].

FLUXLESS SOLDERING

There are several fluxless soldering processes. One approach, plasma assisted dry soldering (PADS) [28], uses plasma pre-treatment to alter the chemistry of the metal's native oxide to make it solderable without a flux. This approach has been proven in the laboratory, but it requires specialized equipment to perform the plasma treatment. Another drawback is that the surface treatment is only temporary; after some time, the surface must be treated again, which may cause problems in a manufacturing environment, where long shelf times may be needed.

Another fluxless soldering technique was described in [29]. The technique is simple: remove the metal native oxide then coat the metal with a thin noble metal to prevent further oxidation. The noble metal layer does not oxidize and will prevent the oxidation of the metal beneath it. Many solder alloys will rapidly consume noble metals, such as

platinum, gold, or palladium during a normal solder process to reveal the clean metal surface underneath. Some process development is necessary to choose a compatible metal native oxide etch. Also, care must be taken to limit the re-growth of the native oxide between the etch step and the noble metal deposition. In addition, it is important to limit the amount of some noble metals, such as gold, to prevent any negative mechanical effects from the IMC [20]. There is a design tradeoff between longer shelf times (thicker noble metal layers) and good mechanical properties of the final joint (thinner noble metal layers). Using this noble metal to create a fluxless solder bonding process is part of designing a proper under bump metallization (UBM).

2.2.2 Under Bump Metallizations

The UBM is a stack of thin-film metals that sit between the solder and the material it is bonding. UBMs are required when using solder to bond materials that are not normally solderable because the solder will not wet them. Since typical MEMS wafers, such as silicon and glass, are not wettable by solder, a UBM is required for the solder to bond them together.

For reliable soldering to thin films of metal, several different materials need to form this thin-film stack. Figure 2.4 illustrates a generic UBM on top of a lateral feedthrough.
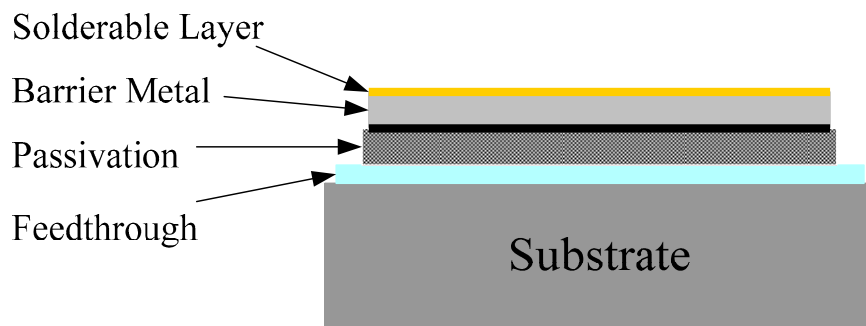
Figure 2.4 Illustration of the various layers in a UBM that is necessary for a solder bond over a lateral electrical feedthrough.

Each layer in the stack performs a specific function. The topmost layer, the solderable layer, is usually a noble metal such as gold or platinum that does not form a native oxide. With no native oxide, the solder will easily wet and spread over this layer. Below the

solderable layer, the barrier metal is usually a refractory metal, like nickel or cobalt that reacts with the solder slowly. The barrier metal prevents the solder from consuming the entire UBM during the soldering process. If the entire stack consisted of just the solderable layer, the high dissolution rates of the metals that are typically used for the solderable layer would constrain the total bonding time to sub-second times; if the solder were molten longer than that, it would completely consume the solderable layer and dewet the layer beneath it, resulting in a poor bond. Underneath the barrier metal is the passivation layer that provides insulation between the conductive feedthrough and the conductive bond ring. Several different UBMs were explored in this work and are presented in Section 2.3.2.

2.2.3 Solder Temperature Reflow Profile

Solder forms a bond to the parent metals by melting and spreading over the UBM. For this to happen, the wafer pair must be heated past the melting temperature of the solder. There are four stages to the heat cycle as shown in Figure 2.5: 1) initial heating 2) dwell 3) reflow and 4) cooling.
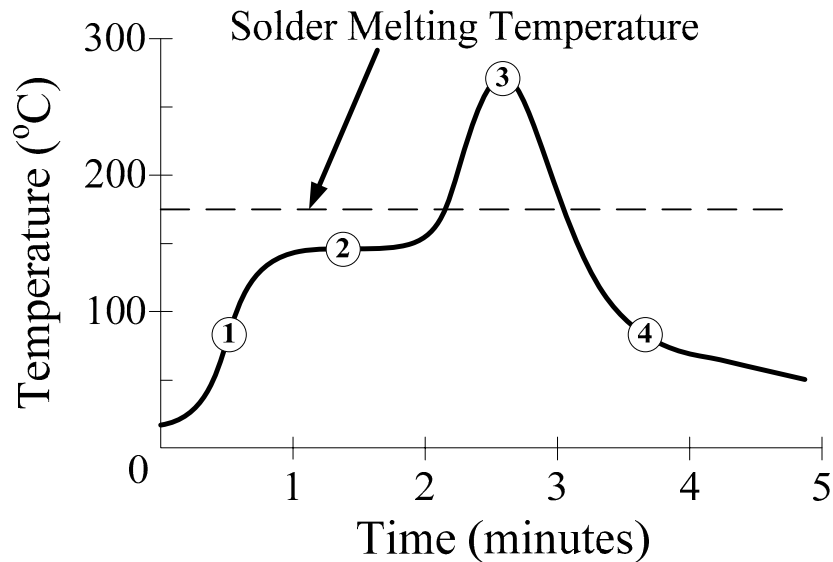
Figure 2.5 Typical solder reflow profile for Pb-Sn Solder. The profile proceeds through 4 stages: 1) initial heating 2) dwell 3) reflow and 4) cooling [20]

In theory, the initial heating stage should be performed as quickly as possible to limit

adverse reactions between the solder and the parent materials before the solder melts. In practice, however, it is difficult to achieve rapid heating rates because of large thermal gradients or poor heat conduction between the wafers and heat source in reduced pressure atmospheres. A typical approach rapidly heating to a temperature below the melting point of the solder, then holding at that temperature for an extended period of time to allow the wafers to thermally equilibrate.

The dwell stage should only last for a few minutes to allow the entire assembly to reach the same temperature and to flush the water vapor out of the joint. If the wafers are held at this elevated temperature for too long, the adverse material reactions that were prevented by the high heating rate in Stage 1 will still take place. After the dwell stage, the assembly is heated above the melting point of the solder in the reflow stage.

It only takes a small amount of heat to raise the temperature of the assembly above the melting point of the solder because the dwell stage temperature was chosen to be slightly less than the melting point of the solder. The maximum temperature of the bonding process is determined by metallurgical constraints of the solder and parent metals. The temperature should be well above the melting point of the solder because it is difficult to maintain precise control over the solder metallurgy, especially when bonding with very small volumes of solder as those used in wafer bonding. Depending on the solder metallurgy chosen, the melting point could vary widely with small changes in composition. Some properties of the solder, such as viscosity and wetting ability, increase with increasing temperature. Typically, the higher temperature above the melting point, the better the solder is able to wet and spread between the joints. For this reason, the maximum temperature of the solder joint is usually chosen to be 50 °C to 100 °C above the melting point of the solder. This extra temperature above the melting point of the solder is known as the superheat. There is a tradeoff in choosing the superheat because too much heat will accelerate the adverse material reactions between the molten solder and parent metals. The amount of these reactions that is tolerable varies between different solders and different parent metals. Another way to reduce these reactions is to minimize the amount of time the assembly spends above the melting point of the solder. In general, the faster the assembly can be heated and cooled, the higher the superheat can be applied

because the rapid heating and cooling allow the total time that the solder is molten to be minimized. For certain heating methods, such as those done in reduced pressure atmospheres, it is difficult, if not impossible, to apply sufficient superheat without causing detrimental solder-parent metal reactions.

After the reflow stage, the assembly is cooled to ambient temperature. Usually this cooling rate is limited by the thermal mass of the assembly and the heat removal path. In vacuum atmospheres, large thermal masses can cause long cooling times because of the difficulty in maintaining good thermal contact to the assembly.

2.2.4 Bonding Environment

For fluxless soldering, the entire reflow process must take place in a reducing atmosphere, inert atmosphere, or vacuum. The atmosphere must be free of oxygen so that the parent metals, and more importantly the solder, do not grow any native oxides during the soldering process. A vacuum environment ensures that there is not any oxygen available to form native oxides on any of the materials in the assembly. An inert atmosphere of argon, nitrogen, or helium will displace any oxygen. A reducing atmosphere with forming gas, such as H_2 or NH_3, also allows for fluxless soldering by removing native oxides or by growing a film on surfaces that can be removed by the solder as it reflows. For MEMS vacuum packaging, a vacuum environment is already required to create the vacuum packages and it is therefore an obvious choice for a fluxless soldering process.

2.3 Solder Bonding Experiments

The typical solder bonding process that was described in the previous section is difficult to implement as a wafer bonding method. Many challenges arise from scaling the bonds to micron dimensions as well as using commercial wafer bonding equipment to apply the heat. In this section, an overview of the wafer bonding equipment is given, the details of several solder bonding experiments are presented, and the challenges faced with solder bonding are discussed.

2.3.1 Wafer Bonding Equipment

The wafer bonder used for these experiments is the SB-6e made by the Karl SUSS Corporation. The bonder is a vacuum chamber with equipment inside for heating the wafers, keeping them separated, and applying force, all while maintaining good alignment (< 10 μm) between the top and bottom wafers. The bond chamber with the lid open is shown in Figure 2.6.

WAFER BONDING SEQUENCE

A wafer bond starts with loading the wafers into the fixture. This can be performed with a high-precision mask aligner configured to handle the fixture or it can be performed by hand under a microscope. The bottom wafer is loaded first, next a spacer can be placed between the wafers to keep them separated, and then the top wafer is loaded and the clamps engage to keep the wafer aligned during loading of the fixture into the bond chamber.
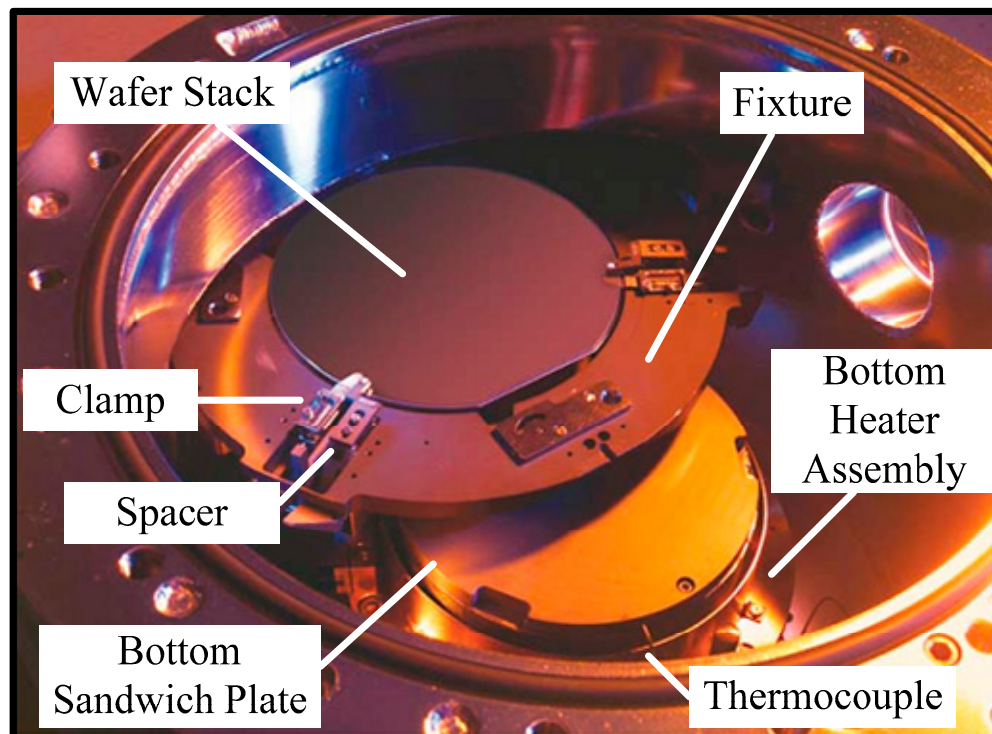
Figure 2.6 Photograph of the inside of a SUSS SB-6e wafer bonder chamber as the fixture is loaded into the chamber. A great deal of equipment is needed to produce a well aligned bond [30].

Once the fixture is loaded into the chamber, it sits directly on the bottom sandwich plate. The bottom sandwich plate is made of silicon carbide for its strength and high thermal conductivity. There is a thermocouple welded directly into the bottom sandwich plate. This thermocouple provides a direct measurement of the bottom sandwich plate to the control software to give the tool precise control over the bottom sandwich plate temperature. Below the bottom sandwich plate is the bottom heater assembly. This assembly contains the resistive heaters that generate the thermal energy to heat the wafers as well as a motor that moves the whole bottom assembly up and down to transfer the fixture to and from the loading arm during loading.

The lid and top assembly would block the view and are therefore not shown in Figure 2.6. The top assembly is very similar to the bottom assembly. There is a top sandwich plate that is also made out of silicon carbide similar to the bottom sandwich plate; however, there is not a thermocouple directly welded into the top sandwich plate because large voltages on the top plate during anodic bonds will short down the thermocouple lead to the bonder chassis. Instead, the temperature for the top plate is measured at the resistive heat source in the top assembly. The measurement of the top plate temperature is very inaccurate because it is not taken at the sandwich plate. There is no motor in the top heater assembly; however, there is another pressure chamber that is used to apply force to the wafers. Once the wafers are in contact with the top plate, the pressure in the chamber behind the top plate can be regulated versus the bond chamber pressure so that a force equal to the tool pressure multiplied by the top sandwich plate area is applied to the wafers. An illustration of the side view of the bonder is shown in Figure 2.7.
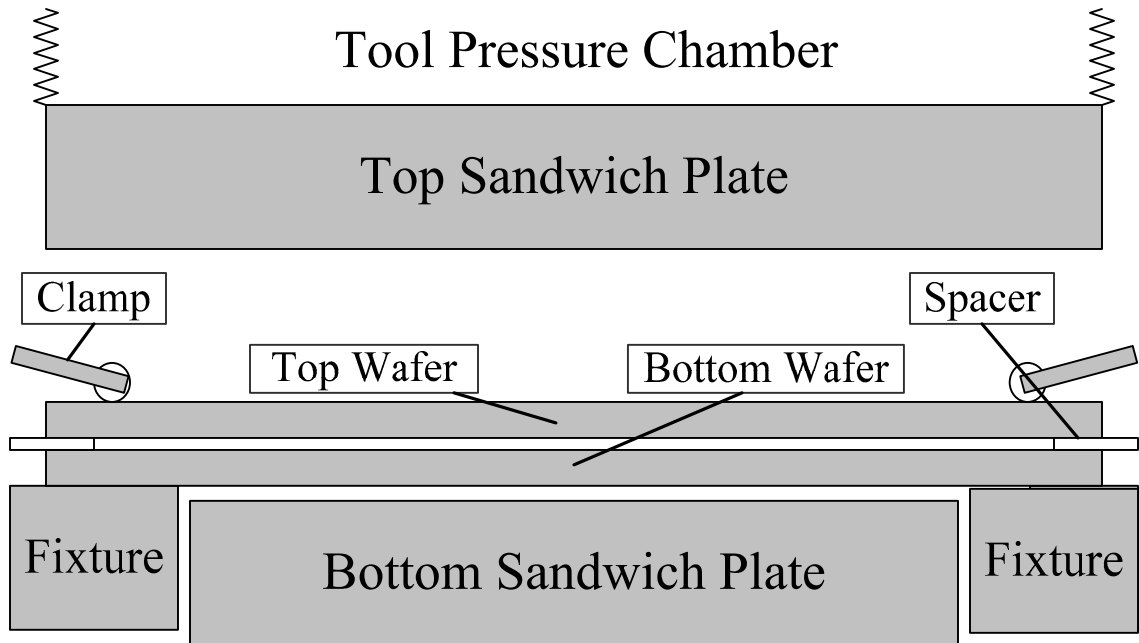
Figure 2.7 Illustration of the side view of the inside of the bond chamber detailing all the components used to create well aligned bonds. All of this thermal mass must be heated and cooled during a bond, which takes a long time in a vacuum environment.

LIMITATIONS OF COMMERCIAL WAFER BONDERS

There are several limitations of this tool configuration that impact solder bonding processes, the greatest of which is the thermal time constant of the system. The thermal time constant of this system determines the greatest heating and cooling rates that can be achieved by the control software. This configuration produces a very large thermal time constant for several reasons. First, there is a lot of material used in the design. The fixture, bottom and top sandwich plates all need to be heated and cooled along with the wafers. This is a much larger thermal mass compared to just the wafers themselves, larger by several orders of magnitude. More thermal mass means there needs to be more heat moved into the system and more removed to change the temperature. Second, getting heat in and out of this system is a challenge, especially when the bond chamber is pumped down to a vacuum atmosphere. This is because the system relies on thermal conduction across long distances to heat the fixture and wafers. The heaters used to generate the heat are not placed right next to the wafer stack; they are placed well below the sandwich plates in the heater assemblies. The heat has to travel through all of the material between the heaters and wafers to cause any temperature rise in the wafers. To

complicate matters, there are several air gaps in the system as well. The gaps are very small and located between the sandwich plate and the heater assembly as well as between the sandwich plate and the wafers. These gaps are very small so heat is conducted across them at a similar rate to solid conduction when the bond chamber is at atmosphere. However, if the bond chamber is pumped down to a vacuum environment, these gaps become very good thermal insulators. Any extra thermal resistance in the heating and cooling path will lead to a larger thermal time constant and longer heating and cooling times. These factors add up to long thermal cycles when using a commercial system for wafer bonding experiments.

There are other bonders that do not suffer from long-thermal time constants, but they are targeted for die-level bonding and therefore not equipped to handle large silicon wafers. This equipment is not capable of producing vacuum packages at the wafer level while the silicon wafer is still whole. To maintain a major advantage of MEMS manufacturing, large parallel processing, all of the bonding experiments were carried out at the wafer level.

2.3.2 Solder Experiments

Several experiments were run to test solder processes in the SUSS SB6e wafer bonder. The first two solder reflow experiments were designed with a generic solder process in mind. The designs of the UBM and reflow sequence were developed so that many different types of solder alloys could be used. To that end, the experiments used a pure tin solder, to which different materials, such as copper, silver, and bismuth, could be added to change the melting temperature, mechanical properties, and other metrics of the solder. Two UBMs were investigated, one with a nickel barrier layer and another with a molybdenum barrier layer. In addition, another solder wafer bonding experiment was designed for a specific solder that is widely used in semiconductor manufacturing, eutectic Au-Sn solder.

As mentioned previously, one of the big advantages of using solder as a wafer bonding technique lies in the fact that there are many different types of solder alloys available. The properties of these alloys can vary significantly over metrics such as reflow

temperature, mechanical strength, and thermal coefficient of expansion, to name a few [20]. There are many varied MEMS bonding needs, some of which would benefit from the different advantages of the many alloys of solders. To that end, several solder reflow experiments were conducted that tested standard solder UBMs in a commercial wafer bonder solder process. Pure-tin was used as the solder because it is a good representative of a generic solder, since tin is a major component in the most common solder alloys.

NICKEL AS THE UBM BARRIER LAYER

A standard UBM in typical solder reflow experiments uses gold as the solderable layer, nickel as the barrier layer, and titanium or chromium as an optional adhesion layer [31]. This UBM was investigated as a generic UBM for a solder wafer bonding technique.

The experiment was conducted by fabricating the UBM onto two wafers, one wafer contains only the UBM and the other has the UBM and then electroplated tin on top of it. The fabrication starts with creating a bond ring pattern on one silicon wafer with photoresist. The UBM of 500 Å Titanium / 2000 Å Nickel / 4000 Å Gold was deposited by electron beam evaporation in a single vacuum cycle. It is important to perform this step without breaking vacuum to keep the titanium and nickel from oxidizing. The gold layer must be thick enough to prevent oxidation after vacuum is broken. Several thousand angstroms of gold is sufficient to prevent oxidation for several months, if the gold is a high-quality film like those deposited by PVD [20]. The film is patterned into a square bond ring by sacrificing the photoresist in acetone and lifting off the metal UBM stack. The same UBM stack is deposited on another wafer by physical vapor deposition (PVD) without any photoresist on it. After UBM deposition, photoresist is exposed with the same bond ring pattern on the substrate. The photoresist forms an electroplating mold. The wafer is then put into a stannous tin electroplating bath and 5 μm of pure-tin is electroplated into the photoresist mold to form the solder layer. After electroplating the solder, another photoresist layer is spun on the wafer and patterned with a clear field mask to form a protective layer over the solder layer. This photoresist protects the tin layer during the various wet etching steps that remove the UBM from areas of the wafer where there is no solder. The gold is removed in gold wet etchant GE-8148, the nickel in

10% nitric acid, and the titanium in 5% BHF solution. It is necessary to remove as much excess UBM area as possible so that the solder does not spread over the entire wafer it was deposited on. The final cross-section of the wafers just prior to reflow in the wafer bonder is illustrated in Figure 2.8.
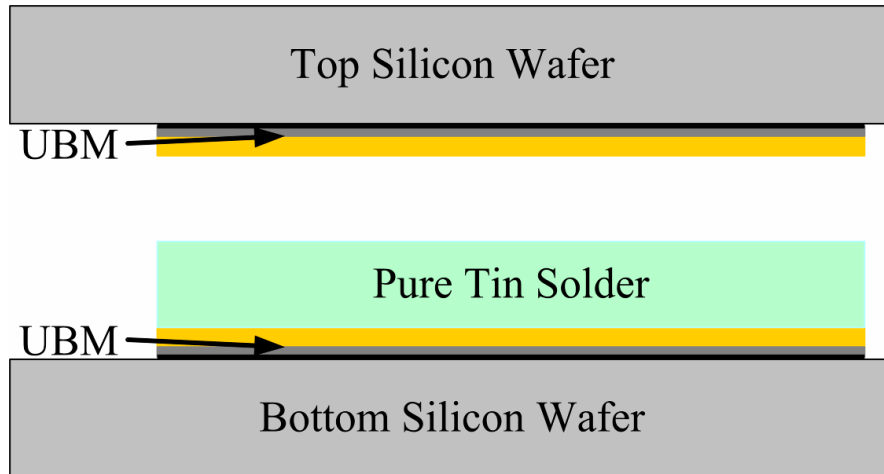
Figure 2.8 Illustration of the cross-section of the nickel UBM solder reflow experiment. This standard solder UBM (Ti-Ni-Au 500Å-2000Å-4000Å) does not create good solder wafer bonds because of the extended heating cycles of commercial wafer bonders.

The silicon wafers were aligned and bonded in the SUSS SB6-e. The wafers were loaded into the bonder and then the chamber was pumped down to vacuum. The chamber remained at vacuum for the entire soldering sequence to keep the process fluxless. The reflow heating profile was modeled after the typical solder reflow profile illustrated in Figure 2.5, but modified to fit the thermal time constant of the SB6-e. Figure 2.9 shows the actual temperatures of the wafer bonder top heater and bottom sandwich plate during the reflow sequence.
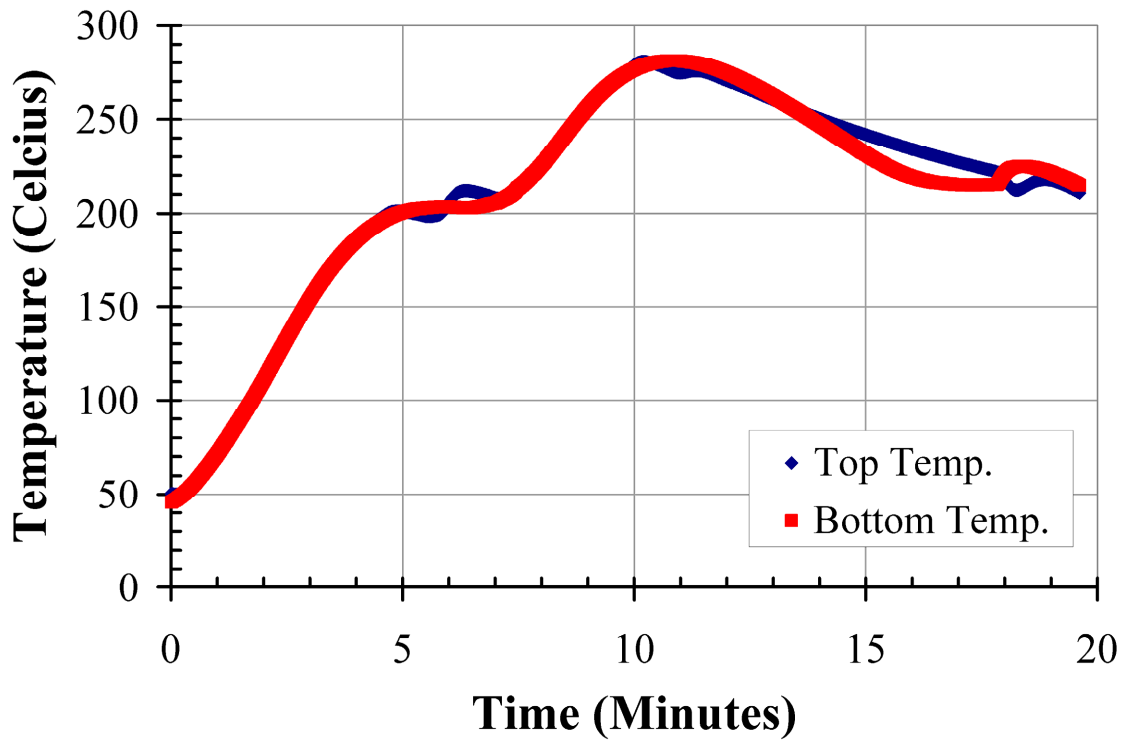
Figure 2.9 Temperatures of the top heater and bottom sandwich plate in the SB6-e during the nickel UBM solder reflow experiment. This reflow sequence is > 6 times longer than a typical solder reflow process.

After the bonding sequence, the wafers were taken from the bonder and inspected. Immediately after taking the wafers from the bonder they became detached from one another. The small force exerted by the tweezers used to unload the wafers was enough to break the bond holding the two wafers together. A picture of one of the bond rings from the bottom wafer is shown in Figure 2.10.
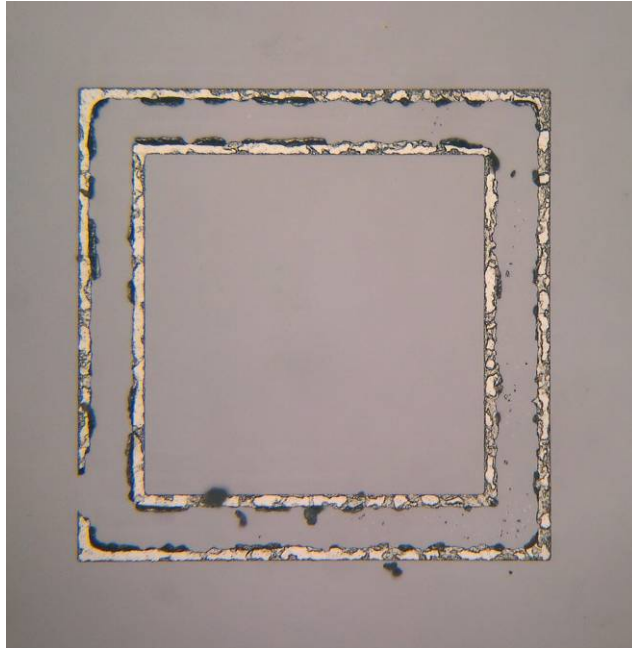
Figure 2.10 Picture of the remnants of a bond ring from the bottom wafer of the nickel UBM experiment. The pure-tin solder consumed the nickel barrier wafer and the rest of the UBM during the reflow sequence.

The solder completely consumed the UBM during the reflow process. The nickel layer in the UBM stack was not of sufficient thickness to survive the extended thermal cycle. The solder reflow profile in Figure 2.9 shows that the solder was above its melting temperature for 438 seconds (> 8 minutes). Compared to a typical soldering process where the solder is molten for less than 30 seconds, the solder was molten a factor of ~15 longer in this reflow experiment. During this extended molten period even nickel, which is the slowest of typical solder materials (Figure 2.11), was completely consumed. The consumption rate of a fresh nickel layer (without Ni-Sn IMC) by molten pure-tin is ~ 0.3 μm/min [32]. As the IMC layer grows, this rate goes down.
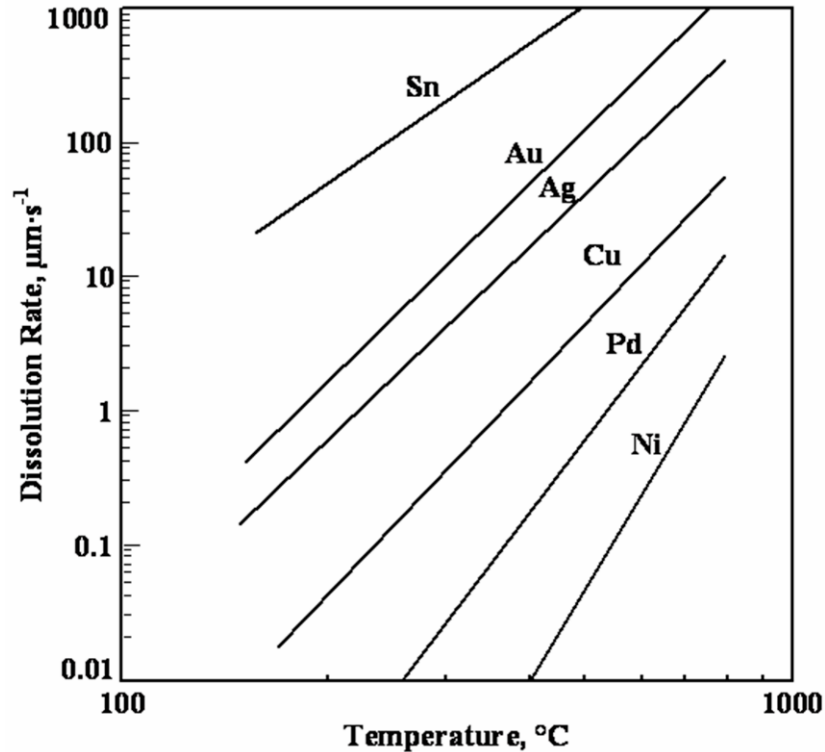
Figure 2.11 Dissolution rates of various metals in eutectic lead-tin solder. These rates are underestimates of the dissolution rates for lead-free solders because of the higher tin content in lead-free solders.

One solution to the consumption problem could be to make the nickel layer thicker, because a thicker nickel layer would not be completely consumed during the reflow process. Another experiment was conducted similar to this experiment, but a thicker nickel barrier layer was used. A different method was necessary to deposit the nickel film because 2000 Å is approaching the limit of evaporable nickel thin films. The stress in the deposited film causes thicker layers to delaminate from the wafers. It was determined experimentally that anything above 2000 Å suffered from poor adhesion to the wafers. To deposit thicker layers, a 1 μm thick electroplated nickel layer was used as the barrier layer in the UBM. This technique was used to create successful solder bonds.

The wafers used were a Pyrex™ wafer and a double-sided silicon wafer. Each wafer was individually processed and then bonded. The top wafer processing begins with a clean double-side polished silicon wafer. First, the electroplating seed layer for the nickel rim was deposited on the front side of the wafer (titanium 300 Å/ nickel 2000 Å). A thick

layer of photoresist was spun on top of the seed layer and patterned to provide the mold for electroplating. The bond ring was electroplated into the mold with a Nickel Sulphamate electrolytic process to a thickness of 1 μm. After forming the rim, the thin-film solderable layer was deposited. First, the nickel oxide was etched in a diluted hydrochloric acid etch. Then, the wafers were rinsed in DI water for two minutes and quickly dried. Next, the wafers were loaded into an evaporation system and it was pumped down. It was important to minimize the time between the completion of the oxide etch in HCl and the evacuation of the evaporation system in order to reduce the oxide growth on the nickel bond ring. The gold solderable layer was evaporated (nickel 1000 Å/ gold 1000 Å) and patterned by a liftoff process. The photoresist electroplating mold for the rim was removed in acetone, leaving the solderable layer deposited only on top of the rim. A similar process was used to create the same UBM on a Pyrex™ wafer. An illustration of the cross-section of wafers prior to bonding is shown in Figure 2.12.
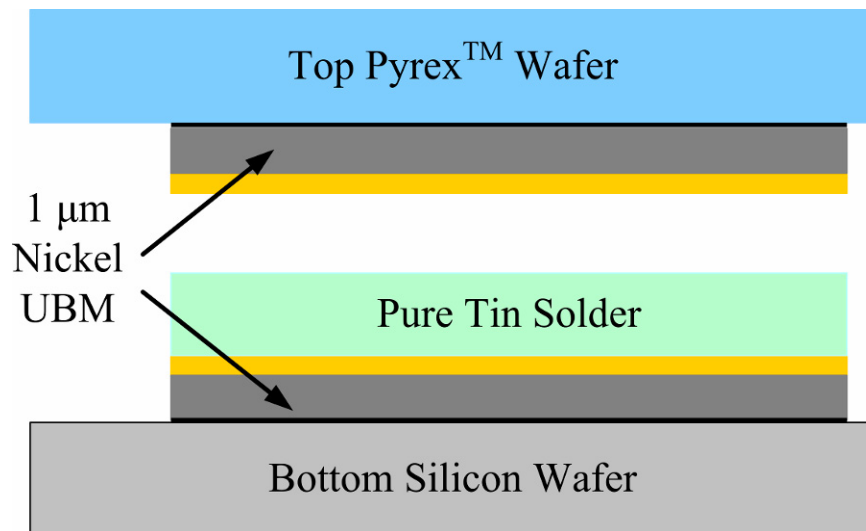
Figure 2.12 The cross-section of the thick nickel UBM solder bond experiment right before bonding. The thicker nickel can survive the longer bond sequences in commercial wafer bonders.

The wafers were bonded in a vacuum environment with the same reflow profile as in Figure 2.9. After bonding, the wafers were unloaded from the bonder and were well adhered to one another. The force from the tweezers holding the wafers was not enough to separate the two. A larger force was used to try and pry the wafers apart with a razor blade. The razor blade force was sufficient to separate the two wafers from one another.

The bond strength of the solder bond was very high, because the bond failed by breaking the glass wafer. A portion of the Pyrex™ wafer remained adhered to the solder bond ring as can be seen in Figure 2.13. This indicates that the solder bond was stronger than the fracture strength of a Pyrex™ wafer.
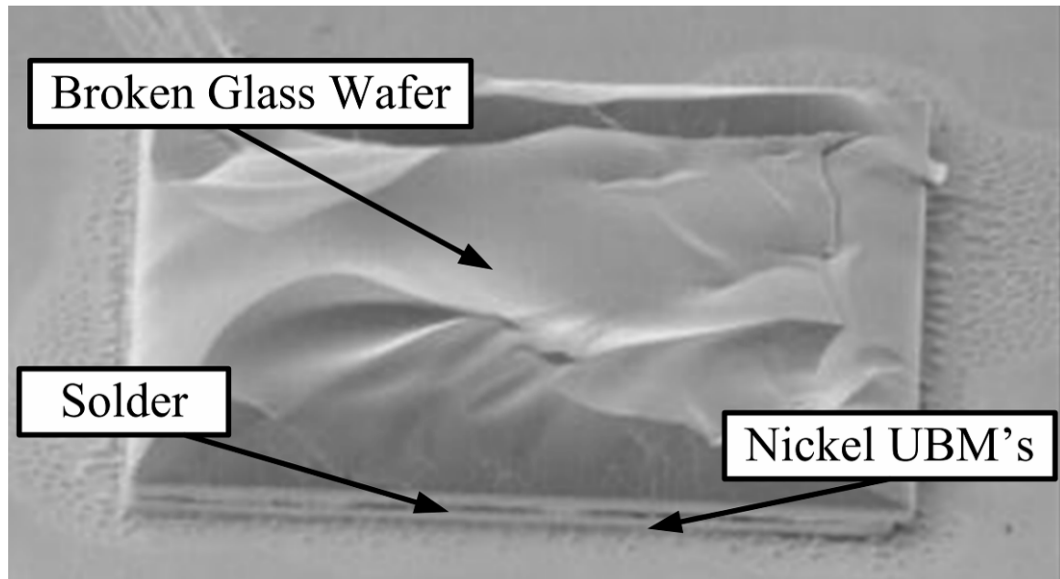
Figure 2.13 Remnants of the wafer bond strength test. The solder bond was stronger than the fracture strength of the glass wafer, so the bond failed by fracturing the glass wafer instead of pulling the solder bond apart.

Successful, lead-free solder bonds can be created with a thick nickel barrier layer UBM. However, there are other detrimental effects from the long thermal time constants that made pursuing other UBM metallizations attractive. Most notably, thick intermetallic layers, especially nickel-tin intermetallics, will reduce the shear strength of the solder bond [31]. The intermetallic phases that are formed from the reaction of solders and the parent metals are typically brittle and do not adhere well to other phases in the solder [20]. Although there are exceptions, such as AgSn intermetallics in silver-tin solder, most intermetallic layers decrease the quality of the solder bond. Moreover, the thicker the intermetallic layer, the more detrimental the effect on the solder bond quality [31]. For this reason, barrier layers other than nickel were explored as solder bonding UBMs.

MOLYBDENUM AS THE UBM BARRIER LAYER

There are other materials aside from those shown in Figure 2.11 that have been used

as the barrier layers in UBMs. Some research has been done in UBM barrier layers that can survive contact with molten solder during its entire service time. Many of the refractory metals, such as niobium, tungsten, and molybdenum, are consumed at a rate of nearly zero by tin solders because of their limited formation of IMCs [33]. That makes these materials interesting candidates as barrier layers in a UBM that has to survive the long reflow times inherent in commercial wafer bonder solder processes.

A simple bonding experiment was prepared to examine the feasibility of molybdenum as a barrier layer in a robust UBM. A silicon and Pyrex™ wafer with the UBMs and solder were prepared using physical vapor deposition and electroplating as with the previous experiments. However, for this experiment the UBM was deposited using sputtering instead of evaporation because the high melting point of molybdenum makes it difficult to deposit with electron beam evaporation. The UBM is made up of Cr/Mo/Au (500 Å/2500 Å/1000 Å) and the solder layer is 10 µm thick. The cross-sections of the wafers prior to bonding are shown in Figure 2.14.
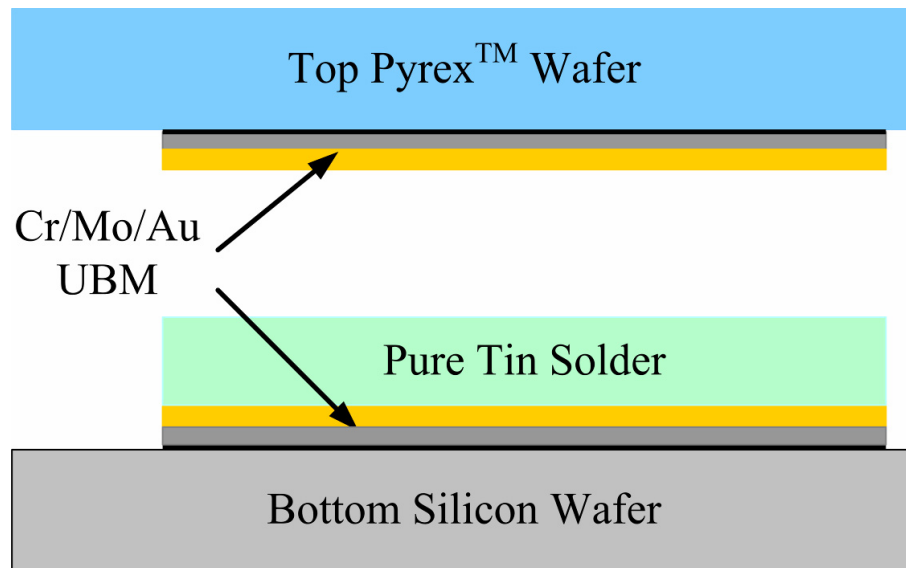
Figure 2.14 Cross-section of the molybdenum barrier layer UBM experiment prior to bonding. Molybdenum does not form intermetallics with molten tin and therefore has a consumption rate of zero during a solder reflow process.

The wafers were bonded in a vacuum environment with the same reflow profile as in Figure 2.9. After bonding, the wafers were unloaded. The force from the tweezers

unloading the wafers was not enough to separate the wafers. However, simply inserting a razor blade between the wafers without applying much force caused the wafers to completely separate. The pictures from Figure 2.15 provides some insight as to why the bond strength was so low.
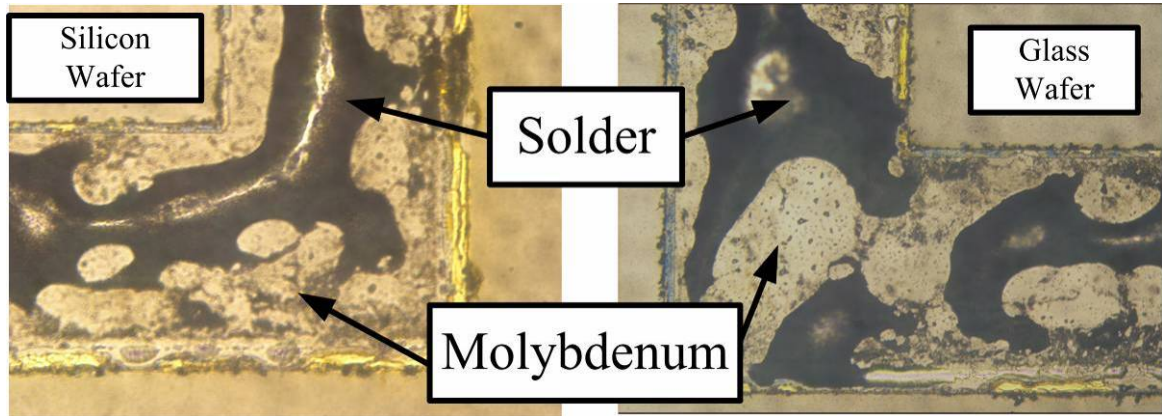
Figure 2.15 Pictures of the bond rings from the Pyrex™ and silicon wafers from the molybdenum UBM experiment. The solder did not wet the molybdenum despite the use of a solderable layer of gold.

The solder did not consume the molybdenum layer during the soldering process. In that regard, molybdenum is a good barrier layer. However, the solder in the photographs has not wet the molybdenum barrier layer. The gold solderable layer has been mostly consumed from each bond ring (there is only a little bit of gold left near the edge). This indicates that the solder covered the entire bond ring at one point during the reflow process. However, once the solder has consumed the gold solderable layer it reveals the molybdenum underneath. At this point, the interfacial surface tension between the solder and molybdenum (γ_{SL}) is higher than the surface tension of the molybdenum (γ_{SV}) so the solder dewets the molybdenum and pools into isolated islands of solder on both wafers. The bond strength of the solder between the molybdenum and solder is very low because of this dewetting.

The molybdenum was investigated as a barrier layer because it is not consumed by molten solder. The molybdenum survived, but it is not a good candidate for the UBM barrier layer because the solder did not wet it and therefore did not create a strong bond. The reason it did not wet the molybdenum is, unfortunately, the very reason molybdenum

50

was chosen to investigate as a potential barrier layer: its low dissolution rate. The dissolution of parent metals by solder is caused by intermetallic formation, which will cause problems for long soldering reflow times. However, the reaction between the solder and the parent metal that forms intermetallics releases energy, the extra energy available from this intermetallic formation promotes further wetting of the parent metals by the solder. The intermetallic formation between molten solder and many parent metals can produce as much as twice the spreading force as from just the difference in surface tensions alone [20]. This extra force enhances the spreading of solder over barrier layers that it consumes, such as nickel and copper. Unfortunately, the reason for investigating molybdenum (it's near zero dissolution by molten tin) as a barrier layer also precludes its use as one.

There are some alloys of refractory metals, such as titanium-tungsten that may be another area of interesting UBM research. Titanium is a wetting promoter used in some solders [20] for active soldering of materials with low surface energies, such as oxides and other dielectrics. Combining it with a refractory metal such as tungsten may achieve the balance that is needed to create a UBM that can survive long contact times with molten solder without getting consumed by it.

Another interesting way to combat the limitations of a long thermal time constant inherent in commercial wafer bonders is to use a solder with a low ratio of the materials responsible for consuming the barrier layer of UBM. Gold-tin solder only contains 20% tin by weight (~ 29% atomic), compared to over 90% by weight for other common lead free solders.

GOLD-TIN SOLDER

Gold-tin solder has been used in the semiconductor industry for die-attachment and creating hermetic seals for ceramic semiconductor packages [34]. The alloy is hard and moderately brittle because the major phases that make up the joint, Au-Sn and Au_5Sn, are intermetallic phases [20]. Figure 2.16 shows the binary phase diagram. The solder composition is typically near the eutectic point at a concentration of 20% Sn by weight. There are two major advantages for using a gold-tin solder alloy as a MEMS wafer

bonding technique. First, its low tin content reduces its dissolution rate of UBM barrier layers such that the UBM barrier layers commonly used in soldering processes are compatible with the long-thermal cycle times of standard wafer bonders. Also, it is simple to make gold-tin soldering a fluxless process because gold is a common solderable layer in UBMs, therefore little extra processing is needed to make the bond a fluxless process. For these reasons, gold-tin solder was investigated as a wafer bonding technique for MEMS vacuum packaging.
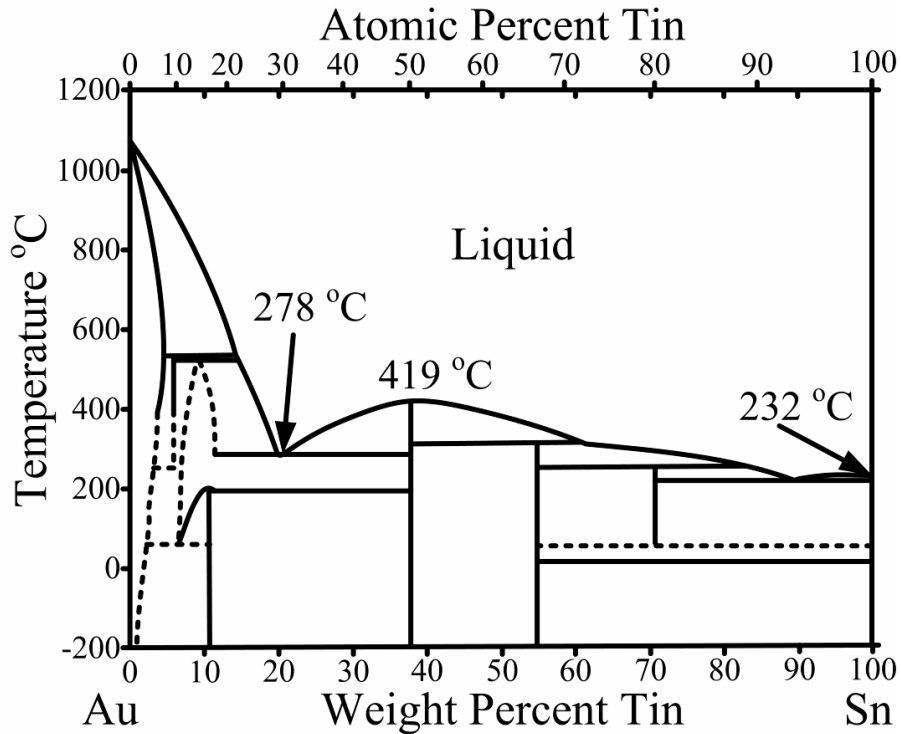
Figure 2.16 Gold-Tin binary phase diagram. The most common gold-tin solder composition is the 20% tin by weight eutectic composition.

A gold-tin solder bond can be created by electroplating gold to a certain thickness, then electroplating pure tin on top of it to a thickness that is 66% of the gold thickness. These thicknesses will result in a near eutectic composition in the bond joint. The melting temperature at this composition is ~ 280 °C. Gold-tin solder is usually bonded at 320-350 °C, which is 50-70 °C of superheat to promote wetting and spreading by the solder. Two wafers were bonded with this Au-Sn solder to test its wafer bonding capability.

Fabrication started with two double-side polished silicon wafers. A seed layer of 1kÅ

Cr / 5 kÅ Au was deposited onto both wafers by sputtering PVD. Next, both wafers were electroplated with gold to a thickness of 7 μm. The tin thickness required to create the eutectic composition should be the total gold thickness (electroplated thickness plus the sputtered seed layer thickness) divided by 1.5, which is a tin thickness of 5 μm on both wafers. After the tin electroplating, the bond rings are protected with a photoresist layer while the seed layer is etched in gold and chrome etch baths. The final cross-section of the bond joint is shown in Figure 2.17.
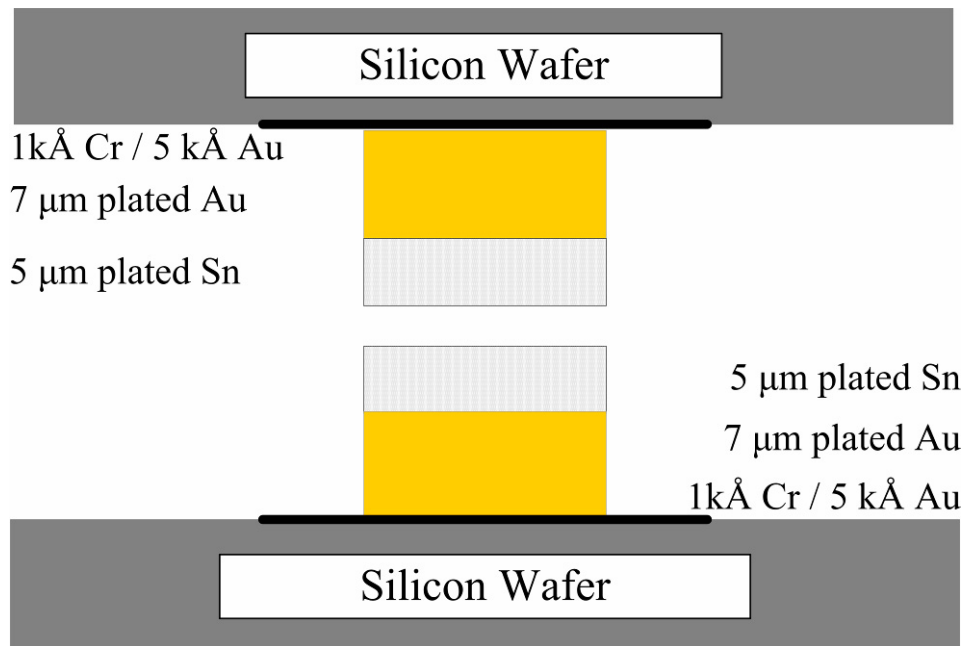
Figure 2.17 Cross-section for the Au-Sn solder wafer bond directly before bonding.

The wafers were aligned in a BA-6 bond aligner then loaded into the SB-6e wafer bonder for the bond cycle. The cycle begins with pumping the chamber down to vacuum to remove all the oxygen from the chamber and enable fluxless soldering as well as creating vacuum packages. After pumping down, the top assembly is brought into contact, the clamps are removed, the spacers are removed, and then the wafers are heated to the bonding temperature. The minimum possible force, 200 Torr (26 kPa), is applied to the wafers during the bond sequence, which equates to a pressure of 0.4 MPa at the bond rings. The bonding temperature for the Au-Sn solder was 300 °C. The temperature profile for the bond sequence is shown in Figure 2.18.
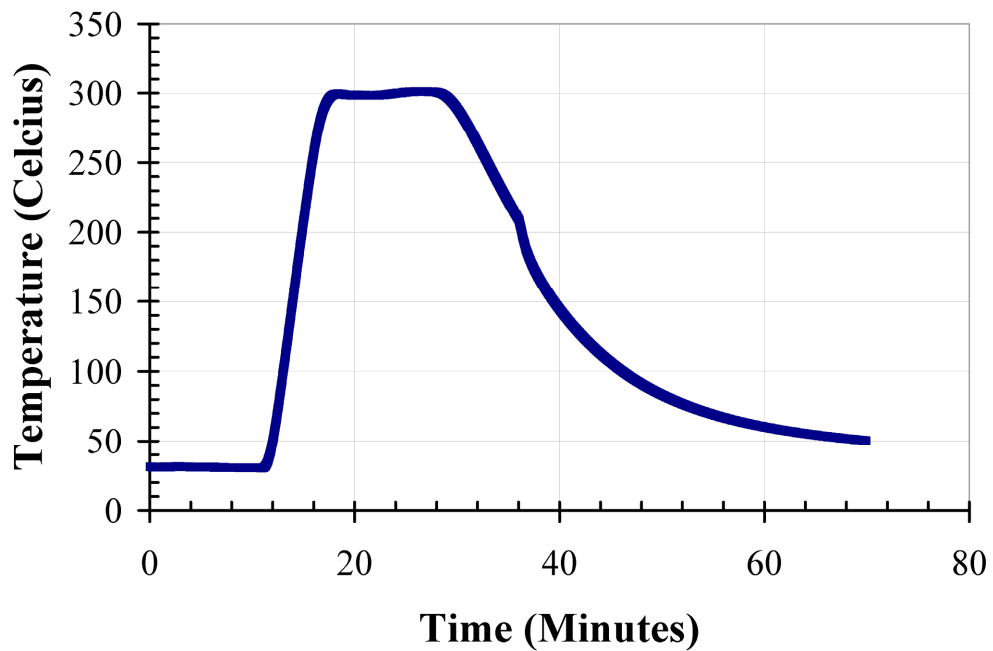
Figure 2.18 Bond Temperature Profile for a Au-Sn solder bond.

The wafers were held at the bond temperature for 10 minutes, which is much longer than normal reflow times, to ensure good wetting. The extra reflow time was done promote good wetting because of the small superheat of only 20 °C [20]. The combination of waiting time at the bond temperature and the heating and cooling cycles make the total bond time approximately 1 hour. After the wafers had cooled past the eutectic temperature of the Au-Sn solder (280 °C), the bonder chamber was vented to atmosphere to speed up the cooling rate. Once the wafers cooled to room temperature, they were removed from the bonder, inspected with a SEM, and tested for shear strength and hermetic capabilities.
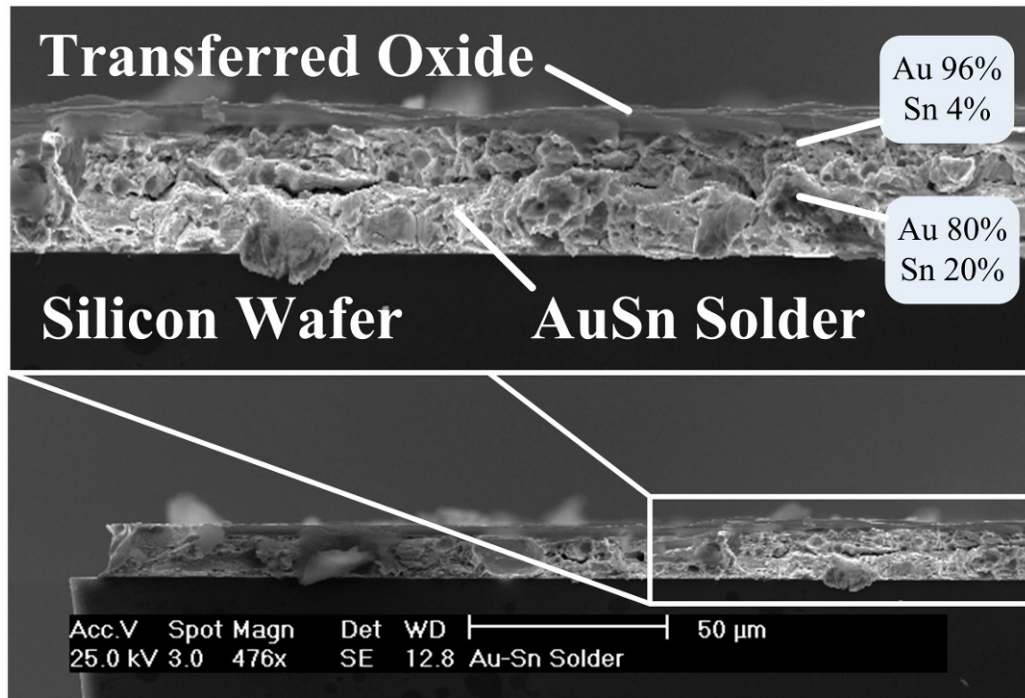
Figure 2.19 SEM image of the cleaved Au-Sn Solder bond cross-section. The Au-Sn ratio in the center of the bond is near the eutectic composition and gold-rich near the edge of the wafer bond as measured by X-ray dispersive element analysis.

Figure 2.19 shows a SEM image taken of the cross-section of a cleaved bond ring. The inset shows a magnified view highlighting the transferred oxide from the failed bond as well as the material composition as measured by EDAX element analysis. The element analysis showed that the majority of the bond is the eutectic composition of 20% Sn by weight. Near the edge of the bond joint, the solder composition becomes more gold-rich (only 9% Sn by weight), probably due to the extra gold available from the seed layer deposition. The visual inspection of the cross-section of the wafer bond shows that there are not any obvious voids and the transfer of the silicon oxide film indicates that the bond has good mechanical characteristics. More quantifiable data was measured on the Au-Sn solder using methods that are described in detail in Section 3.4; the results are summarized and discussed here.

Table 2.3 Data summary for the Gold-Tin solder bonding technique.

Metric	Test Methodology	Result
Hermeticity	Long-term vacuum data	$1.5 \cdot 10^{-15}$ atm·cc·s^{-1}
Strength	Shear Test	28.0 MPa
Re-melting Temperature	from Solder Theory	~ 280 °C

Table 2.3 summarizes the measured metrics for the Au-Sn solder bonding technique. The Au-Sn bond exhibited very robust mechanical characteristics. The shear strength was the highest of any bonding technique investigated in this work at 28.0 MPa. A majority of over 20 die tested could not even be broken by the shear stress setup. The largest stress that can be applied by the shear test setup on these wafer bonds was 28.9 MPa. Every single die tested passed the most stringent MIL-STD specifications for die shear strength.

Au-Sn solder wafer bonding also exhibited good hermetic capabilities. The bonding technique has shown that it can seal a very small vacuum cavity (< 0.5 µL) for over 3 months with a stable pressure inside. The worst case leak rate into the packages is $1.5 \cdot 10^{-15}$ atm·cc·s^{-1}, which has been calculated from the pressure sensor error. There is no visible long-term leak in the package data. As more data is taken, the worst case leak rate will decrease.

The low tin content in the Au-Sn eutectic enables this solder to remain above its melting temperature for many minutes without the adverse effects that are seen when pure-tin solders are molten for such long times. This makes Au-Sn an excellent candidate for MEMS wafer bonding in commercial wafer bonders. However, the melting point of Au-Sn solder is relatively high for solder at 280 °C. In this work, the required bonding temperature for this solder was 300 °C and would be difficult to reduce the temperature any lower because of the corresponding reduction in wetting. If lower temperature solders are to be used as a MEMS wafer bonding technique, another method of applying the heat other than a commercial wafer bonder should be used. The next section covers several other heating techniques that could be investigated as techniques for creating pure-tin solder bonds for MEMS wafer bonding because they use localized heating technology that does not suffer from the long thermal time constants of commercial wafer bonders.

2.3.3 Localized Solder Bonding Methods

There are other methods of applying the heat necessary to melt the solder that do not suffer from the long thermal time constants inherent in commercial wafer bonders pumped down to high vacuum levels. Normal soldering reflow times are possible with these techniques because the solder is heated directly while limiting the temperature rise of the surrounding material. This reduces the thermal mass that must be heated and cooled so that a typical reflow profile is possible, even in a vacuum environment. These methods could overcome the challenge of finding a suitable barrier layer that is wettable by the molten solder without getting consumed during the reflow cycle.

LOCALIZED LASER REFLOW

Y. Tao, used a CO_2 laser to reflow eutectic PbSn for a solder wafer bonding technique [35]. The laser type was chosen because a large portion of the energy at the wavelength of the laser (10.6 μm) is transmitted by the silicon (40%) compared to the amount absorbed (20%). The solder was electroplated or screen printed over a copper/titanium UBM to form the sealing ring around a cavity. The wafers were loaded into a vacuum chamber, then the laser moved across each bond ring to raise the temperature of the solder briefly above the melting point so it reflows and seals the bond ring. This method results in a solder that is only molten for a brief instant in time, reducing the dissolution of the parent metals to a minimum. Other researchers have reported similar techniques for indium bonding [36], Si-Au eutectic bonding [37], and direct glass to silicon bonding [38].
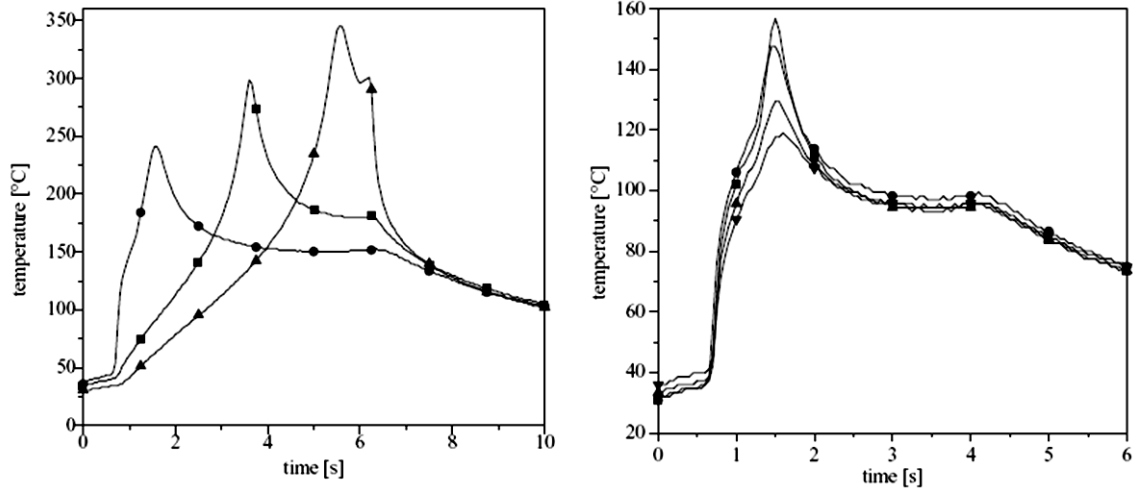
Figure 2.20 Temperature profiles from a Nd:YAG laser reflow process. Laser reflow techniques produce quick temperature cycles. However, their serial nature makes them an expensive wafer bonding technique [36].

Figure 2.20 shows the type of reflow profiles that are possible using localized laser bonding, which can be completed much faster than a wafer bonder approach. However, the serial nature of this process could lead to long processing times for wafers with many bond rings. This is directly opposed to a major advantage of MEMS processing: parallel, cost-saving processing. Another technique utilizes induction heating to locally heat bond rings in parallel.

LOCALIZED INDUCTIVE HEATING

Induction heating works by creating magnetic loops of material underneath the solder on the wafers. If the loops are placed into a changing magnetic field, the induced electrical current in the loops will cause joule heating that raises the temperature of the bond rings and melts the solder. Compared to the serial nature of laser reflow, induction heating can raise the temperature of all of the bond rings at the same time so it can still be a parallel processing technique.

H. Yang used a NiCo layer underneath a PbSn solder to inductively heat a solder wafer bond [39]. The nickel cobalt layer was electroplated onto a chrome-copper seed layer, and then the solder was electroplated on top of the NiCo spacer layer. The whole wafer assembly is placed onto a loop through which a high-frequency power supply

creates a changing magnetic flux that induces current flow in the spacer layer. Most of the heat is generated in the spacer layer, which is right next to the solder layer. Since the heat generation is localized, the temperature on other places of the wafer does not get as hot as the solder and the total bond time is less than 1 minute (See Figure 2.21).
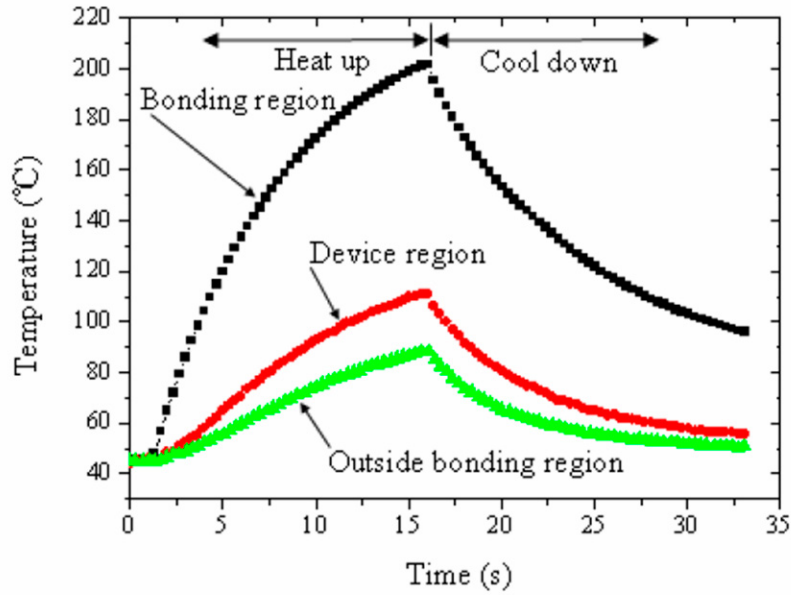
Figure 2.21 Reflow temperature profile for a localized induction solder bond. The overall bond time is short because the majority of heat is generated right next to the solder itself so it heats and cools quickly [39].

One issue with inductive heating is unwanted heating of other structures from the large varying magnetic flux. Other metals, aside from the spacer used underneath, will be exposed this flux and could heat up from it. A long, thin ferromagnetic structure that is well thermally isolated from the substrate could experience a lot of heating from the magnetic flux used to heat the solder. Also, other structures that are designed to be magnetic sensors or actuators need to be able to withstand the large fluxes present during the bond sequence. This issue of unwanted effects from the magnetic flux could complicate or preclude the use of this technique with certain MEMS devices. The localized inductive heating technique has been reported for wafer bonding of silicon to steel [40], anodic bonding [41], and lead-free solder [42].

2.3.4 Standard Solder Bonding Conclusion

There are ways to overcome the challenges in using a commercial wafer bonder for solder bonding. Specific alloys with low tin content, such as Au-Sn solder, solve the problem because the low tin content reduces the parent metal dissolution rates below a critical value that allows the parent metals to survive the long bonding process. This specific alloy works, but this removes one of the great advantages of solder bonding: the temperature flexibility offered because the engineer can select from a range of solder alloys. The gold-rich, Au-Sn eutectic solder melts at 280 °C and is typically bonded at temperatures above 300 °C. There are many other solder alloys that melt at a range of temperatures well below 300 °C that are difficult to use for such long bonding times because of their high tin content.

Generating heat in a localized manner for wafer bonding could also overcome the challenges of selecting a suitable barrier layer for the UBM by reducing the total time the solder is molten. However, these techniques require specialized structures on the wafer or specialized equipment to generate the heat. Furthermore, there are other steps that require thermal energy to produce MEMS vacuum packages that will increase the total thermal budget. Getters are integrated pumps that are necessary for producing the low pressures in MEMS packages (Getters are covered in more detail in Section 4.2.2). The getters need to be activated at elevated temperatures to produce the pumping action that removes contaminating gasses. If this heat is not applied locally, there will be unwanted effects from parent metal dissolution at the elevated temperatures that could ruin the wafer bond.

There is an advanced type of solder bonding technique, called Transient Liquid Phase (TLP) solder bonding that offers several advantages that address the limitations of the traditional solder bonding processes when used with a commercial wafer bonder. Chapter 3 covers TLP solder bonding in depth.

Chapter 3
WAFER BONDING USING TRANSIENT LIQUID PHASE SOLDER

A transient liquid phase (TLP) solder bond is formed by sandwiching a low-melting point interlayer between two parent metals. To form the bond, the assembly is heated above the melting point of the interlayer. The molten interlayer flows to fill any gaps in the bond joint and reacts with the parent metals to form a higher melting point IMC layer; this reaction with the parent metals consumes the interlayer. The bond joint becomes completely solid without reducing the temperature as the last of the liquid interlayer is transformed into the solid IMC layer.

TLP solder bonds are very similar to the standard solder bonds discussed in the previous Chapter. A TLP solder bond is made entirely of metals, just like a standard solder bond. Also, the lower temperature TLP solder bonds (those formed below 300 °C) feature metals that are typically found in standard solder bonds, such as indium and tin. TLP bonds can also planarize over wafer topography just like a standard solder bond because a liquid phase exists during the bonding process that will flow over, and conform to, topology. However, unlike a standard solder bond, this liquid phase exists only temporarily during the bonding cycle, hence the name *Transient* Liquid Phase solder bonding. During a TLP solder bond the liquid phase is transformed into a solid by material interactions; this transformation makes TLP solder bonds unique from standard solder bonds. Unlike standard solder bonds, the service temperature of a TLP solder bond is higher than the formation temperature because there is not any low-melting point phase is left in a TLP bond once it is finished. A standard solder bond will re-melt if the assembly is heated back up to the soldering temperature because there are still low-melting point phases present in the standard solder joint after it is completed. For a TLP bond, all of the low-melting point phases present at the beginning of the bond are transformed into higher-melting point intermetallic phases by material reaction during the

bonding process. This difference makes TLP an ideal technique for solder bonding with commercial wafer bonders because it is compatible with the long thermal time constant inherent in these tools.

Three TLP solder bond material systems were investigated in this work: Au-Sn TLP, Ni-Sn TLP, and Au-In TLP. The bond parameters and experiment results are summarized in Table 3.1.

Table 3.1 Overview of the material families investigated in this work and their results.

Material System	Bond Temp.	Hermeticity	Bond Strength	Re-melt Temp.	Notes
Gold-Tin	300 °C	N/A	Stronger than Pyrex ™	419 °C	Rapid IMC formation created many voids in the bond
Nickel-Tin	300 °C	$1.10^{-15} cc \cdot atm \cdot s^{-1}$	12.1 MPa Shear	> 450 °C	Gold-free, hermetic
Gold-Indium	200 °C	$1.10^{-16} cc \cdot atm \cdot s^{-1}$	28.0 MPa Shear	> 450 °C	Low temperature, strong, hermetic

Section 3.1 discusses the previous work in TLP and TLP solder bonding. A TLP-style bond has been recorded as early as the 16th century. Since then, it has been used for many other applications in industries that span from aerospace to titanium bonding.

Section 3.2 presents an overview of the TLP solder bond process. The process can be broken into four discreet stages. Each stage is covered in detail with discussion of the important design parameters and equations that predict the changes in the materials as the bond proceeds.

Section 3.3 details all of the TLP solder bond experiments performed as part of this work. The process flow for each bonding technique is described, and then a summary of the bonding results are presented and discussed.

Section 3.4 explains the tests used to quantify the capabilities of the TLP solder bonding techniques. The hermeticity, shear strength, and re-melting temperature were characterized for the different material families. The data for the Au-Sn solder bond is

also presented in this section so that it can be compared and contrasted to the TLP solder bonding techniques.

Section 3.5 articulates a design process for TLP solder bonds. The advantages and disadvantages of the different material systems are compared and contrasted. Then a design process is covered that calculates design parameters like layer thicknesses, bond joint areas, and bonding process parameters.

3.1 Previous Work in TLP Solder Bonding

Transient Liquid Phase bonding can be traced back to a publication by Cellini in the sixteenth century describing a method called granulation that used copper oxide paint as an interlayer to fasten small gold balls onto another gold piece [43]. Since then, TLP bonding has been used to bond titanium [44], nickel superalloys [45], dissimilar metals such as: zircaloy 2 to 304 stainless steel [46], and in semiconductors [47].

The most relevant techniques for this work are TLP bonds that use low-melting point interlayers, such as tin and indium, to form robust bonds at low processing temperatures. Table 3.2 lists some reported material systems with their reported process times, temperatures, and re-melting temperatures. All of the bonds are formed at temperatures below 300 °C and the bonds that use indium are formed at or below 200 °C. Even though they are formed at low temperatures, the bonds can survive much higher temperatures. The largest difference between process and re-melting temperatures are for the bonds that use silver (from 175 °C to 880 °C for Silver-Indium and from 250 °C to 600 °C for Silver-Tin.)

Table 3.2 The formation and melting temperatures of some TLP material systems (adapted from [20]).

Material System	Process Time and Temp.	Re-melt Temp.
Copper-Indium	4 min at 180 °C	> 307 °C
Copper-Tin	4 min at 280 °C	> 415 °C
Silver-Tin	60 min at 250 °C	> 600 °C
Silver-Indium	120 min at 175 °C	> 880 °C
Gold-Tin	15 min at 260 °C	> 278 °C
Gold-Indium	0.5 min at 200 °C	> 495 °C
Nickel-Tin	6 min at 300 °C	> 400 °C

C.C. Lee . has investigated many different material systems for TLP solder bonds targeted for die attachment of high-power electronics devices, including AgSn [48], AgIn [49], and CuIn [50]. The parent metals and interlayers were deposited using a combination of physical vapor deposition and/or electroplating and then bonded in a home-built vacuum chamber. The results include detailed material analysis with EDAX, re-melting experiments, and strength measurements, but does not include hermeticity data. Bosco . did an in-depth investigation into creating void-free TLP solder bonds with the CuSn material system [51]. They determined that there is a minimum critical interlayer thickness that is necessary to create void-free bonds. If the interlayer thickness is larger than this critical thickness, then the joint will be void-free. If not, then there is a large chance for voids to form in the bond joint. The conclusions from their work were used to develop design rules for hermetic TLP solder bonds. Humpston . presents an excellent overview of TLP solder bonding in [20], but refer to it as diffusion soldering. They have also published and in depth study of the AgSn material system [52].

TLP solder bonding has been reported for many different uses in semiconductor and MEMS fabrication. However, information has not been reported using TLP solder bonding as a vacuum packaging process. The first reported vacuum TLP solder bonding results are presented in Chapter 4.

3.2 TLP Solder Bond Process

Many efforts have been made to model TLP bonding [51]. Several models based on the thin-film diffusion [53] and thick-film diffusion [54]equations try to model the whole

bonding process at once, but fail because the equations do not accurately predict material interactions as layers change from solid to liquid and back again. Another model, the discreet stage model, splits the bonding process into distinct stages where assumptions can be made about the status of the layers in the bond and concentration of different phases in each layer [43]. Different sets of equations are used based on these assumptions to predict bonding times and layer thicknesses throughout the bonding process. This model is a step in the right direction for accurately describing the TLP solder bonding process; however, the kinetics for the growth of the various phases during the bonding process have been modeled as diffusion controlled processes. For some systems, such as copper-tin, there is clear evidence that this is the case. However, a better model that accurately describes the complex growth of the various phases throughout the bonding process is needed to model other material systems that are not governed by diffusion phase growth. An overview of the four discreet stages is shown in Figure 3.1. Each stage is discussed in detail in the next sections. The important bonding process parameters are discussed and some of the modeling efforts are presented. The references contain more detailed information regarding the various modeling processes.
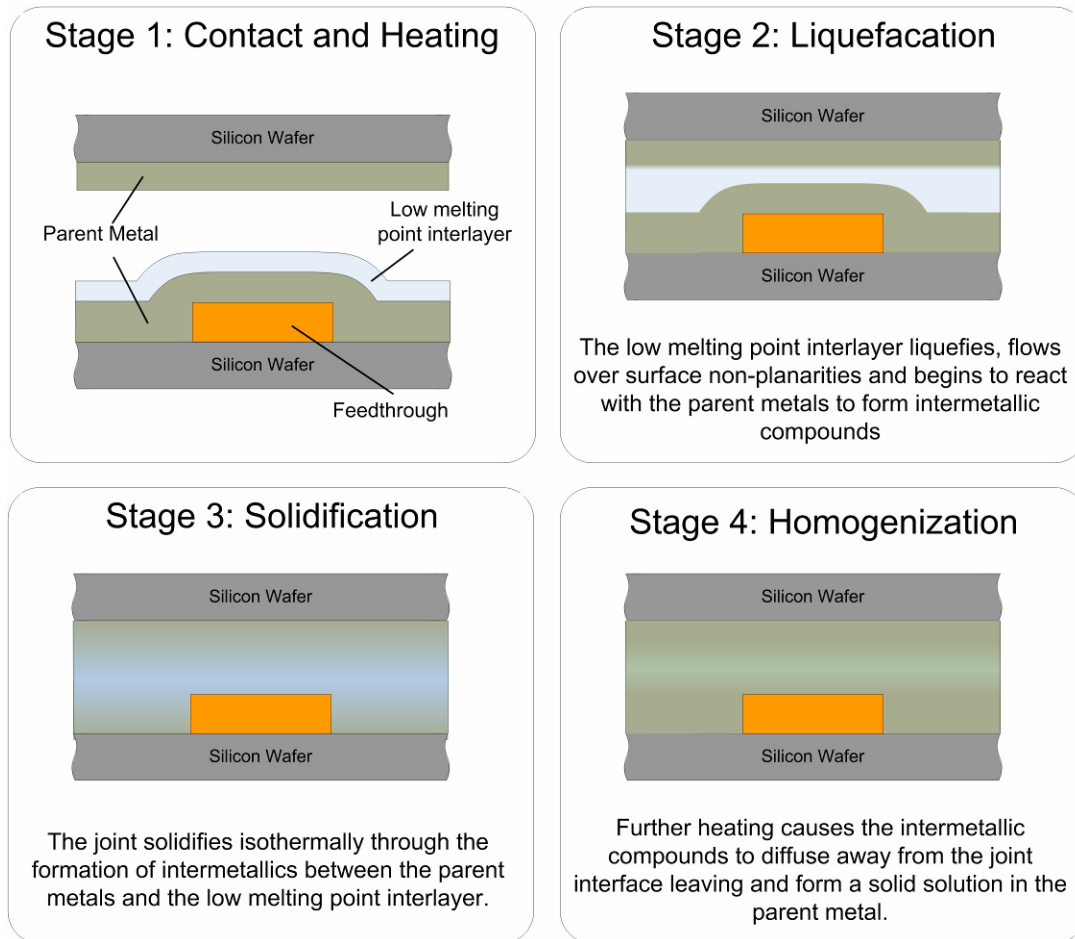
Figure 3.1 The four stages of a TLP bond.

3.2.1 Stage 1: Contact and Heating

After fabrication of the bond joint is finished, the two parts to be bonded are put into contact and heated above the interlayer's melting point. As the assembly is heated, the extra thermal energy promotes the growth of IMCs. Limiting the growth of these compounds is important in the design of the bonding sequence for this stage. Other critical parameters for this stage are the heating rate, bonding temperature, and the clamping force.

CLAMPING FORCE

The clamping force for TLP solder bonds needs to be higher than what is typically used for a solder bond, but not as high as the force used for solid-state diffusion bonds. The applied force is typically between 0.5 to 2 MPa [20]. This force ensures that the

assembly is in good contact across all the bond joints. Another reason for applying a clamping force is to create a good TLP solder bond without fluxes. The force is used to break the native oxide on the interlayer in a similar manner as in standard solder bonds. A high clamping force will break the native oxide on the low melting point interlayer. As long as the bond is created in a vacuum environment, the underlying interlayer should not oxidize and will wet the other parent metal, resulting in a good bond. The force required for breaking the native oxide is much higher than the force needed for the bond itself, so the force is increased to a maximum (~ 5 MPa) at the beginning of the bond cycle to break the native oxide, then reduced to the TLP solder bond value for the rest of the bond. This is the approach typically used when tin is the low melting point interlayer.

BOND TEMPERATURE

The bond temperature obviously must be greater than the melting point of the interlayer for a successful TLP solder bond, exactly how much greater depends on other aspects of the bond. One reason for a higher bonding temperature is to increase the wetting ability of the low melting point interlayer. The superheat, or extra heat above the melting point, increases the wetting force for liquid metals [20]. The larger the wetting force, the greater the spreading of the low melting point interlayer over the surface of the parent metals and, therefore, the greater the bond uniformity. Another reason for a higher bonding temperature would be to accommodate a temperature overshoot from the rapid heating rate of the wafers. As described in the next paragraph, a high heating rate is desirable for TLP solder bonds. It is necessary to overdrive commercial wafer bonders to achieve the optimal heating rate, which leads to overshoots of 10-20 °C. The typical bonding temperature for TLP solder bonds varies, but it is usually between 30-50 °C above the melting point of the interlayer.

HEATING RATE

The heating rate is the most critical parameter of the entire TLP bonding process because it will determine if the joint contains voids or not. The whole assembly should be heated as quickly as reasonable to create high-quality, void-less bonds. The maximum heating rate is limited in commercial wafer bonders by their large time constant when

bonding in a vacuum environment; for a SUSS SB6e it is ~ 60 °C per minute. For other bonders, the heating rate can be limited by unwanted thermal gradients in the assembly or how the heat is generated and applied. The heating rate is extremely important because common TLP solder interlayers react with parent metals even in the solid state. This reaction rate is also dependent on temperature. If the heating rate is too slow, the assembly will spend too much time at elevated temperatures before reaching the melting point of the interlayer. If this occurs, the interlayer can be entirely transformed to higher melting point phases before it can melt. The higher melting point phases will not melt during the bonding process, so there will not be any liquid layer during the bonding process if the heating rate is too low. If there is not a liquid phase during the bonding process, there will be nothing to flow and fill the gaps in the bond joint, resulting in many voids across the bond interface. To understand how the heating rate controls the intermetallic phase thickness, the basics of intermetallic phase growth should be understood so that a final thickness can be predicted based on the temperature profile of this stage.

SOLID-STATE INTERMETALLIC PHASE GROWTH MODELING

Intermetallic phase formation is a complex material reaction that is highly dependent on the material system. Different material systems will produce intermetallics of different shapes at different rates. An all-encompassing model that explains intermetallic growth for all material systems does not exist. Therefore, to understand intermetallic growth kinetics for a TLP solder bond, the specific material system reactions should be studied. Furthermore, most intermetallic phase growth results are reported for isothermal conditions. To predict a final intermetallic phase layer thickness at the end of Stage 1, the intermetallic phase growth kinetics need to be understood over a temperature range. For some systems, assumptions can simplify the calculations. In the rest of this section the generic reactions are described then simplified into two cases based on simple assumptions that can be used to estimate the intermetallic phase thickness for linear temperature profiles. Also, a recent model, called the dual phase lag model, is presented and shows promise for accurately modeling the growth.

A generic representation of the interface between the interlayer and parent metal is presented in Figure 3.2.
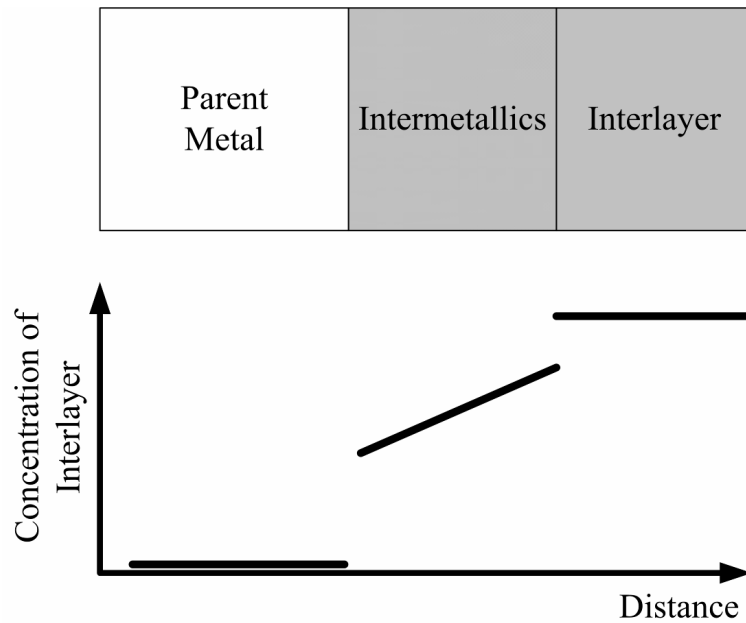
Figure 3.2 Illustration of the interface between the parent metal and interlayer. Generally, intermetallic growth falls into one of two cases: diffusion limited growth and interfacial reaction limited growth.

Dybkov studied the growth of chemical compound layers at the interface between a binary system, which is directly applicable to the growth of intermetallic layers in a TLP solder system [55]. He theorized that there are two reactions that need to take place for the chemical compound layer to grow: 1) One (or both) of the elements in the binary system must diffuse across the chemical layer compound that separates them and 2) once across, the element must react with the other element to produce more chemical compound and increase the layer thickness. If we assume that only the interlayer is diffusing through the IMC to react with the parent metal on the other side, then Equation (3.1) shows the relationship between IMC layer thickness and time.

$$dt = \left(\frac{x}{K_{diffusion}} + \frac{1}{K_{reaction}} \right) dx \qquad (3.1)$$

Where t is time, x is the intermetallic layer thickness, $K_{diffusion}$ is the diffusion rate

constant, and $K_{reaction}$ is the interfacial reaction rate constant. Equation (3.1) can be split into two separate equations that represent the time it takes for the diffusion and interfacial rate reaction to take place:

$$dt_{diffusion} = \frac{x}{K_{diffusion}} dx$$
(3.2)

$$dt_{reaction} = \frac{1}{K_{reaction}} dx$$
(3.3)

In some cases, one of these two reactions will be the rate-limiting step for a given material system at the dimensions of interest in MEMS wafer bonding, which allows for some simplification of the analysis.

If the diffusion of the interlayer through the IMC layer is much faster than the interfacial reaction between the interlayer and the parent metal, then the interfacial reaction rate is the limiting step. When this is the case, the growth rate of the IMC layer is constant with time. A constant growth rate means that the thickness is linear with time because the growth rate does not depend on the thickness of the IMC layer. The interfacial reaction rate is usually the rate limiting steps in material systems with high interlayer atomic diffusivities in the IMC layer, such as gold-indium [56], or if the IMC layer is very thin. Equation (3.4) shows the relationship between the IMC layer thickness, h_p, and time, t.

$$h_p = k_l \cdot t$$
(3.4)

The growth rate constant, k_l, is related to temperature by an Arrhenius relationship shown in Equation (3.5):

$$k_l = k_{lo} e^{\left(\frac{-E}{kT}\right)}$$
(3.5)

Where k_{lo} is the growth rate pre-exponential factor, E is the activation energy, k is

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Boltzmann's constant, and T is the temperature.

On the other hand, if the interfacial reaction rate is much slower than the diffusion of the interlayer atoms through the IMC layer, then the diffusion time dominates the growth rate. When this occurs, the growth rate of the IMC layer is dependent on the thickness of the layer itself and therefore not constant with time. As the layer gets thicker, the interlayer atoms have a longer distance to diffuse across before they can react with the parent metal so the growth rate slows down. The thickness of the IMC layer can be calculated from Fickian diffusion equations and it will exhibit the characteristic square root dependence on time. Material systems such as nickel-tin exhibit this type of solid-state intermetallic growth, where the thickness, h_p, versus time, t, is given by Equation (3.6) [57]:

$$h_p = \sqrt{2k_p t} \tag{3.6}$$

The parabolic growth rate constant, k_p, is related to temperature by the Arrhenius relationship in Equation (3.7):

$$k_p = k_{po}\, e^{\left(\frac{-E}{kT}\right)} \tag{3.7}$$

Where, k_{po} is the pre-exponential factor, E is the activation energy, k is Boltzmann's constant, and T is the temperature.

IMC growth experiments are usually performed under isothermal conditions; the solder and parent metals are held at a constant temperature and the IMC layer thickness is logged at several time intervals. All of the constants governing both interfacial limited growth and diffusion limited growth are extracted from this data. Using the constants to predict the final IMC thickness under non-isothermal conditions, such as the temperature ramp during Stage 1, requires some further assumptions and simplifications because the integral of the growth rate equations over a temperature ramp does not have a closed form solution.

Shewmon discusses an effective diffusion constant that can be used to model diffusion kinetics during the heating and cooling stages of material processing [58]. Since the growth rate factors used to predict IMC growth are governed by the same Arrhenius type relationships as the diffusion, the same approach can be used to calculate an effective growth rate constant for linear and parabolic IMC growth during the heating period of Stage 1. This technique was first applied to TLP bonding by MacDonald and Eagar [43]. The effective growth rate constant, k_{eff}, is calculated by integrating the growth rate equation over the time period of the heating cycle then dividing by the total cycle time, t_o, as shown in Equation (3.8):

$$k_{eff} = \frac{\int_0^{t_o} K(t)}{t_0}$$

(3.8)

The temperature during the ramp rate is given by Equation (3.9).

$$T = \tau \cdot t + T_i$$

(3.9)

Where T is the temperature, τ is the heating rate, t is the time, and T_i is the initial temperature. To find the total cycle time, the final temperature T_f is substituted for T then Equation (3.9) is solved for time to give Equation (3.10):

$$t_0 = \frac{T_f - T_i}{\tau} = \frac{\Delta T}{\tau}$$

(3.10)

Replacing the final time, t_o, with Equation (3.10) and integrating over time instead of temperature gives Equation (3.11), which can be used to predict the final intermetallic thickness at the end of the heating cycle of Stage 1:

$$k_{eff} = \frac{\tau}{\Delta T} \int_{T_i}^{T_f} k_0 \, e^{\left(\frac{-E}{kT}\right)} \frac{dT}{\tau}$$

(3.11)

It is interesting to note that the effective growth rate constant is independent of the

heating rate. However, the heating rate will affect the final IMC layer thickness because a slower heating rate will increase the amount of time it takes to heat to the melting point of the interlayer. The integral in this equation does not have a closed form solution. A slowly converging series expansion of this integral can be used to estimate the growth rate [43]. Shewmon found that the majority of diffusion takes place as the sample is heated from 80% of the bonding temperature until the bonding temperature [58]. In this work, the integral was numerically approximated across these boundary conditions using MATLAB(TM) software. The results of this modeling are presented in the TLP Solder Design Rules section, Section 3.5.

There are some material systems where neither of the previous cases applies so the growth rate is neither linear nor proportional to the square root of time. Several models have been proposed to predict the intermetallic phase compound growth rate for these systems. Erickson modeled the intermetallic phase growth for pure tin on copper using a variable diffusion coefficient and Fick's law[59], but this approach is an empirical curve fitting and lacks a theoretical foundation. Another model, called the Dual Phase Lag Diffusion model, was reported by Chen for modeling IMC growth [60]. The DPLD model is based on the Fick's Law, but a phase lag is added to the mass flux vector *(j)* and density gradient *(∇p)* to yield Equation (3.12):

$$\bar{j}\left(\bar{r}, t + \tau_j\right) = -D\nabla p\left(\bar{r}, t + \tau_p\right)$$ (3.12)

Where *r* is the position vector, *t* is the time, and τ_j and τ_p are the phase lags associated with the mass flux vector and density gradient. The phase lags, τ_j and τ_p, correspond to the finite time it takes for the chemical reactions at the interface and interdiffusion between two dissimilar materials to occur, respectively. The model is very versatile and has been applied to many complex problems, such as thin-film growth [61] and heat conduction [62]. With more experimental results that can determine the phase lags for TLP solder systems; the DPLD model has the potential to accurately predict IMC growth for the heating during Stage 1.

Stage 1 is the most critical of all four stages. The selection of the bonding parameters

for this stage will have the greatest effect on the successful outcome of a TLP solder bond. A sufficient clamping force and superheat will promote good wetting without fluxes. If the heating rate is high enough then the assembly should proceed to Stage 2 before the IMC layer is too thick to prevent the formation of a void-less bond. If careful attention is paid to designing this part of the process, the bond will successfully proceed to Stage 2 where the interlayer melts.

3.2.2 Stage 2: Liquefaction

As the temperature of the assembly reaches the melting point of the interlayer, the interlayer liquefies. As a liquid, it will flow over wafer topography to seal structures such as lateral feedthroughs. It is important that there is enough interlayer between the intermetallic phases growing from each parent metal left in the bond joint after the heating cycle from Stage 1. If there is not any interlayer left between the non-melting intermetallic phases growing from each parent metal, the touching intermetallic phases will prevent the two wafers from moving closer to one another such that the gaps created by wafer topology will not seal. There is a minimum interlayer thickness that can be calculated from the intermetallic growth rate, the intermetallic morphology, the heating rate from Stage 1 and mass balance equations. Bosco . studied the copper-tin material system to determine the minimum interlayer thickness required to produce void-free bonds between planar surfaces [51]. This critical interlayer thickness can be calculated from Equation (3.13).

$$h_c = h_p \cdot C_p \left(\frac{\rho_p}{\rho_l} \right)^2 \Omega \qquad (3.13)$$

Where h_c is half the critical thickness, h_p is the thickness of the intermetallic phase, C_p is the mass fraction of interlayer in the intermetallic phase, ρ_p is the intermetallic phase density, ρ_l is the interlayer density, and Ω is a correction factor for the non-planar growth of the intermetallic phase. The Ω factor is necessary because some intermetallic phases, such as copper-tin, do not grow in a planar manner with phase boundaries parallel to the original boundary. Instead copper-tin intermetallics grow in a scalloped shape, with

a height greater than their width. Figure 3.3 illustrates the differences between planar and scalloped intermetallic phase growth as well as when the interlayer thickness exceeds and does not exceed the critical thickness of $2\,h_c$.
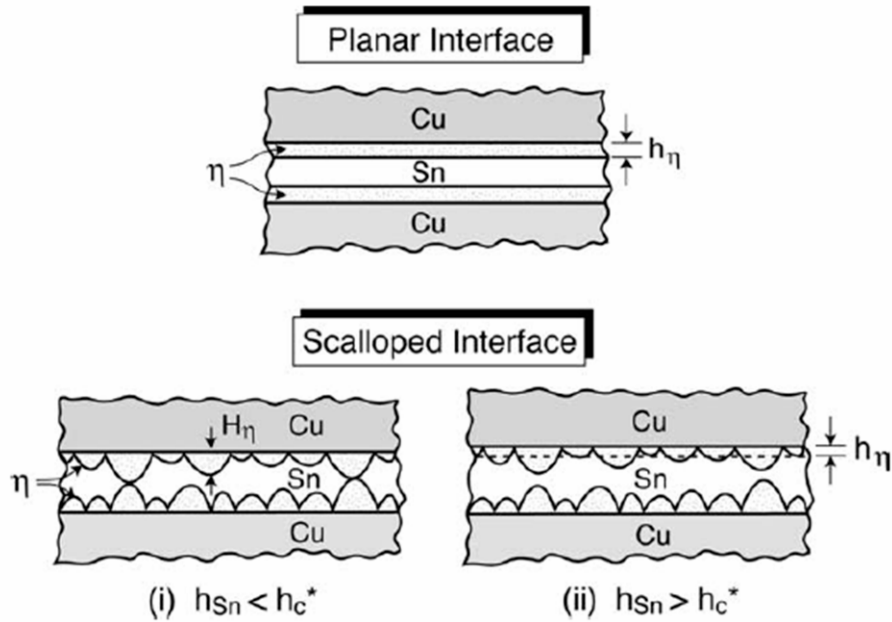
Figure 3.3 Illustration of TLP bond cross-sections with planar and scalloped intermetallic phase morphology and interlayer thicknesses that exceed (Case (ii)) and fall short (Case (i)) of the critical thickness [51].

Calculating the critical interlayer thickness from Equation (3.13) is not trivial. Values for C_p, ρ_p, and ρ_l can be found in a good quality material science reference book. However, h_p and Ω are not easily calculated or found. Bosco performed a series of experiments to study the growth of the Cu-Sn intermetallic phase under different heating rates and then extracted the values for h_p and Ω from the experiments. Due to the complex nature of intermetallic phase growth that is material system specific, it is difficult to predict these two values without repeating the same intermetallic growth rate studies for all materials systems of interest. That being said, a rough calculation of the critical interlayer thickness for various material systems is possible by making assumptions about the intermetallic growth kinetics and morphology from published data. An approach based on the equations from the previous section is presented and an

example is given in Section 3.5 that discusses TLP solder bond design rules.

3.2.3 Stage 3: Solidification

At this point, the liquid interlayer has melted and flowed into any joints in the bond gap. In its molten state, the IMC formation rate between the interlayer and the parent metals is much higher than when the interlayer is solid. Table 3.3 compares reported reaction rates between two materials systems when the interlayer is molten and in the solid state. The actual growth rate will vary based on the thickness of the IMC layer that is already present, but for small layer thicknesses (< 1 µm) this effect is negligible. The growth rate increases more than a factor of 10 in the case of gold-indium intermetallic formation and over 50 times for the nickel-tin material system. Some of the rate increase is undoubtedly due to the increase in temperature. However, the magnitude of the increase cannot be explained by extra thermal energy alone.

Table 3.3 Intermetallic formation rates for selected materials systems when the interlayer is solid versus when it is liquid at similar temperatures.

Material System	Solid State Growth Rate	Liquid Interlayer Growth Rate	Reference
Gold-Indium	0.736 µm/h @ 150 °C	10.67 µm/h @ 225 °C	[56, 63]
Nickel-Tin	0.0833 µm/h @ 220 °C	4.61 µm/h @ 278 °C	[57, 64]

The high intermetallic growth rate during this stage coupled with the thin interlayer thicknesses typically used in MEMS wafer bonding (< 5 µm) means that the liquid layer does not last long and rapid isothermal solidification will take place. Once the last of the interlayer has been consumed by intermetallic formation, the joint becomes two parent metals sandwiching a layer of IMCs. Since there is no interlayer left in the entire joint, the melting temperature of the joint has risen from the melting point of the interlayer (typically ~160-230 °C) to the lowest melting point of all the phases present in the joint. This new melting point varies with the material system, but is typically in the range of 400-600 °C. Once the joint has solidified, the TLP solder bond can be complete depending on the final target microstructure. If the presence of the intermetallic phases left over at the end of this stage is OK for the design of this joint, then the bonding is complete. If the target final microstructure is a pure parent metal joint with the interlayer

in solid solution, more heat needs to be applied to cause joint homogenization in Stage 4.

3.2.4 Stage 4: Homogenization

Not only can TLP solder bonds survive higher temperatures than their formation temperature, they also improve the longer and hotter they are heated (provided that the temperature never exceeds the melting temperature of the IMCs present in the joint). The extra thermal energy promotes the diffusion of the intermetallic phases away from the center of the joint further into the parent metals. For systems with a large solid-state solubility of the interlayer in the parent metal, it is possible to achieve a completely uniform bond joint cross-section comprised of pure parent metal with the interlayer dispersed in solid solution. If this is the targeted terminal phase of the joint, the re-melting temperature approaches the melting temperature of the parent metal itself.

The amount of heat and time it takes to create such quality joints may preclude the material systems use as a cost effective MEMS packaging approach. This is because the transformation from the intermetallic phases that are left after the joint solidifies in Stage 3 to a pure parent metal with the interlayer in solid solution is orders of magnitude slower than the liquid to intermetallic phase transformation that took place in Stage 3. For the copper-tin TLP bonding investigated by Bosco , the shortest calculated time was several hundreds of minutes at the relatively high temperature of 500 °C [51].

Aside from a higher melting temperature, another big benefit of heating the joint to the terminal solid solution phase is an increased joint strength [20]. As mentioned previously in Section 2.3.2, intermetallic phases tend to be brittle and adhere poorly to other phases in a solder joint [31]. This makes most TLP solder bonds much weaker mechanically versus comparable solder bonds. For most MEMS packaging applications, a high bonding strength is not required because other steps in the packaging process will provide mechanical support, such as epoxy overfills [4]. However, for some applications where a very high mechanical strength is needed, it may be worthwhile to expose the chip to such high temperatures for a long time to make the terminal phase the pure parent metal that has good mechanical properties.

3.3 TLP Bonding Experiments

Several TLP bonding experiments were performed with the goal of producing a void-free, thermally-robust wafer bond at low temperatures. To achieve this goal, the following material systems were investigated: Gold-Tin, Nickel-Tin, and Gold-Indium. Each material family is split into a separate sub-section where the experiment details are presented as well as images of the bond cross-sections and discussion of the results. More quantifiable results that test hermeticity, bond strength, and re-melt temperature are presented for all of the solder bonding techniques in Section 3.4.

3.3.1 Gold-Tin TLP Solder Bonding

A gold-tin solder bond was previously reported as a wafer bonding technique in Section 2.3.2. In this section, a gold-tin TLP bond is presented. The difference between the two bonds lies in the difference in the phases left in the bond cross-section after the bond has been completed. For the Au-Sn TLP solder bond, there will be much less tin (< 4% by weight) in the bond joint cross-section than the Au-Sn solder bond (~ 20% by weight). This is because the ratio of tin to gold that started in the bond joint is much less for the Au-Sn TLP solder bond (10:1 Au to Sn for the TLP solder bond versus 3:2 Au to Sn for the solder bond). The gold-tin phase diagram highlighting two overall joint concentrations is shown in Figure 3.4. The gold-tin TLP solder bond is formed by intermetallics instead of a eutectic composition as in a standard solder bond.
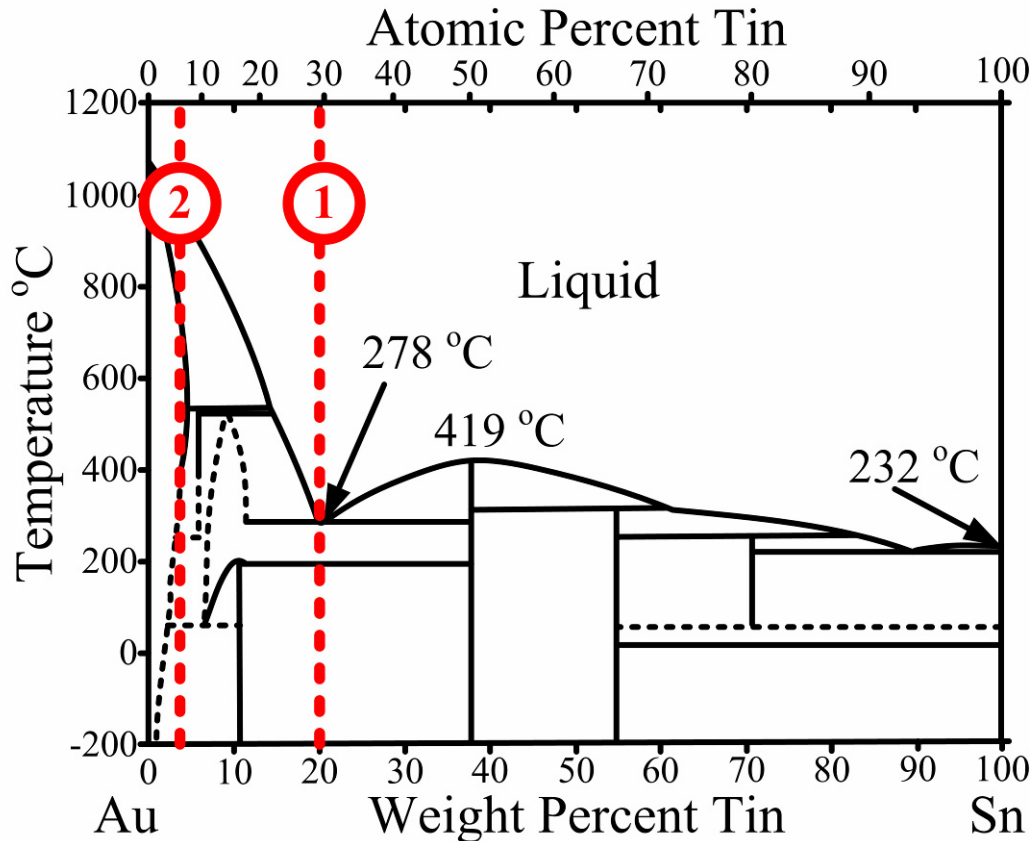
Figure 3.4 Gold-Tin binary phase diagram. Dotted Line #1 represents the joint composition for a Au-Sn solder bond and Dotted Line #2 is the joint concentration for the Au-Sn TLP solder bond presented in this section.

The Au-Sn material system was investigated as an exploratory TLP solder bonding technique because of the processing convenience of using these materials. Gold is a common material used in MEMS fabrication, especially for electroplating the thick layers that are necessary for TLP solder bonding. Tin is not as common; however, it has a low melting temperature (232 °C) that enables this bond to be formed at relatively low temperatures. Another benefit is that gold does not form a native oxide, so it is simpler to make this a fluxless process than if another metal was used as the parent metal. This bond was performed before much of the TLP solder bond theory was known so many of the bonding parameters were not optimized for quality results. The results are presented here to illustrate what a non-hermetic TLP solder bond looks like and discuss the factors that led to such a poor outcome.

The bond is formed between a silicon wafer and Pyrex™ wafer. A seed layer of 500 Å Titanium / 2000 Å Gold is evaporated onto both wafers. Next, photoresist forms the mold for electroplating 300 μm wide bond rings. Gold electroplating increases the thickness of the bond rings on both wafers to 5 μm. A 5 kÅ layer of tin is evaporated onto the gold bond ring on the Pyrex™ wafer, then patterned by liftoff. The cross-section right before bonding is shown in Figure 3.5
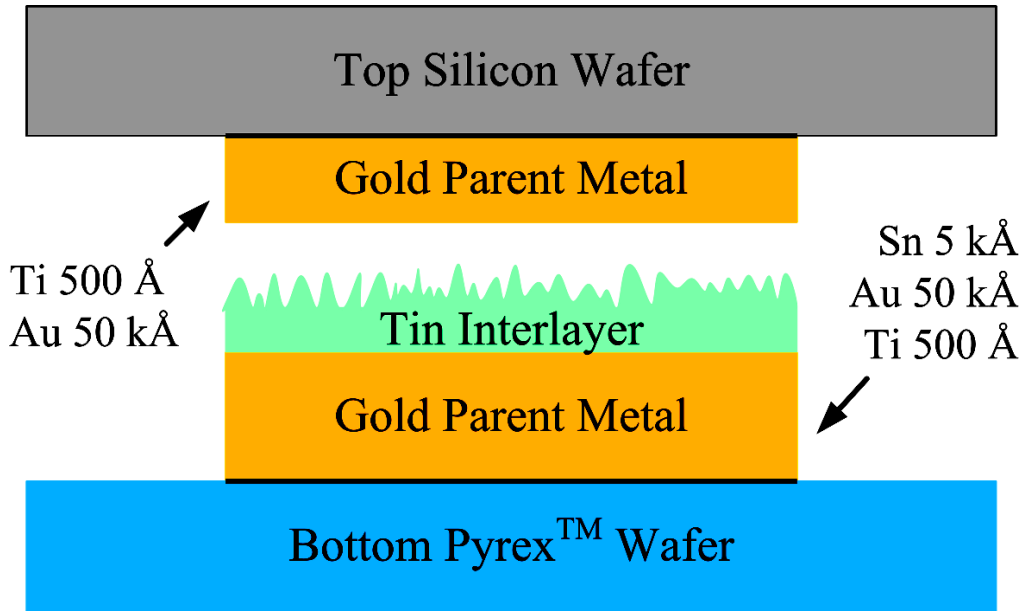
Figure 3.5 Illustration of the cross-section of the Gold-Tin solder TLP experiment before bonding. The tin layer had an average roughness of 2.5 kÅ, which is typical for tin or indium evaporated onto un-cooled substrates [65].

The wafers were bonded in a SUSS SB-6 bonder, which is an older, similar, model to the SB-6e. The wafers were heated at a rate of 60 °C/min to a bonding temperature of 300 °C. The tool pressure was 500 kPa, which results in a pressure of 8 MPa at the bond rings because the area of the tool plate is 63 cm^2 and the bond ring area was ~ 4 cm^2. The wafers were held at the bond temperature in vacuum for 1 hour, then the chamber was vented, the wafers cooled to room temperature, and unloaded.

After unloading, the strength of the wafer bond was tested by forcing a razor blade between the two wafers to attempt to break the bond. When the wafers separated, the bond had broken in the Pyrex™ wafer, indicating that the Au-Sn TLP solder bond was stronger than the fracture strength of the glass. Figure 3.6 shows a picture of a bond ring

with transferred Pyrex™ taken through a microscope.
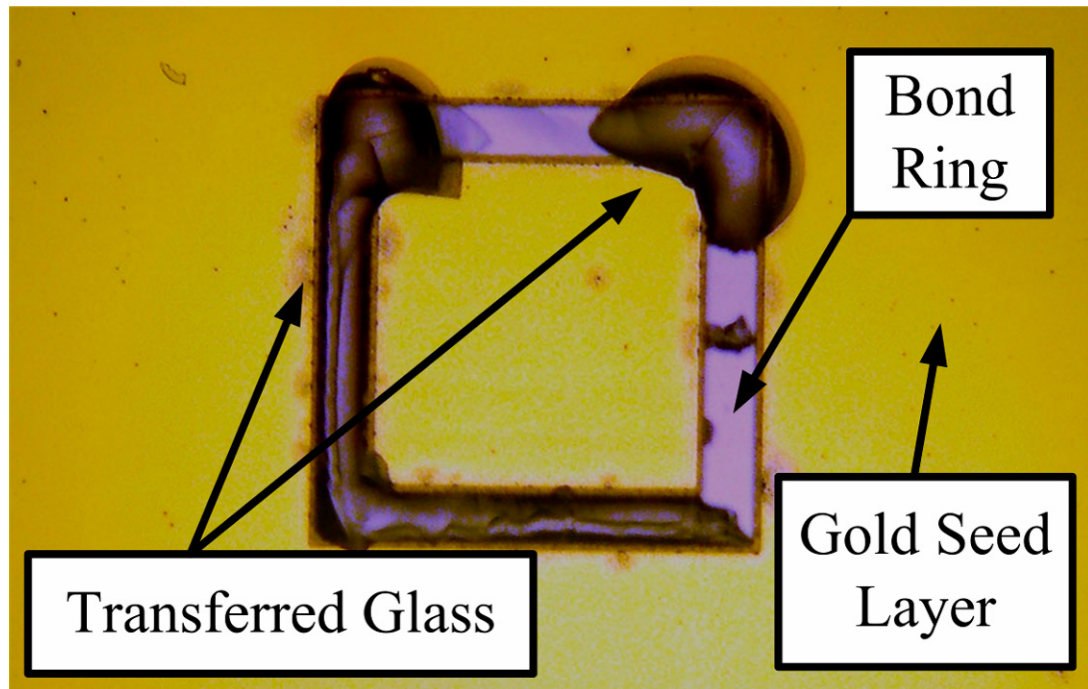
Figure 3.6 Picture of a Au-Sn TLP solder bond ring after the wafers were separated. The bond strength was high enough to fracture the Pyrex™ wafer as pieces of it remained attached to the bond ring.

The bond strength of the Au-Sn TLP solder bond seemed adequate, but a visual inspection of the bond cross-section revealed deficiencies in its hermetic sealing capability. The wafer was sawed into individual die, and then a single die was cleaved across a bond section for closer inspection with a Scanning Electron Microscope (SEM). The SEM image of the cross-section is shown in Figure 3.7.

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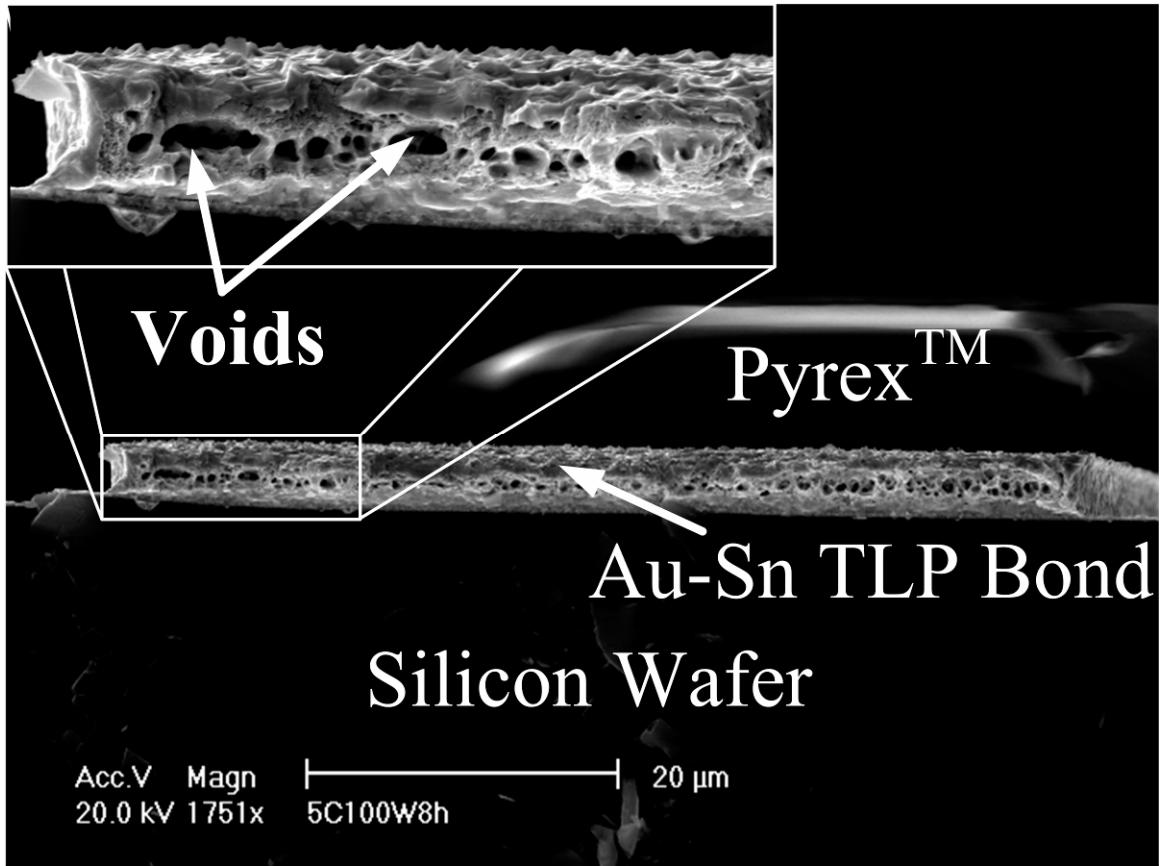
Figure 3.7 A Gold-Tin TLP bond full of voids caused by a combined low heating rate, high gold-tin intermetallic formation rate, and small interlayer thickness.

It was unknown at the time, but Au-Sn is a challenging material system to use as a TLP solder for wafer bonding. The IMC formation rate for the Au-Sn material system is very rapid (on the order of 0.6 µm/min at 150 °C) [66]. This high IMC formation rate prevented the tin interlayer from melting and filling in the gaps in the joint. As the wafers were heated up in the bond chamber, the gold reacted with the tin so quickly that the tin was completely transformed into high melting IMC before the wafers could be heated past 232 °C. Detailed calculations are presented in Section 3.5: Design Rules for TLP Solder Wafer Bonding. From those calculations, it would take a heating rate of 345 °C/s for a successful TLP solder bond with these materials at these thicknesses, which is an impossible feat for any wafer bonder. Another way to create a successful Au-Sn TLP solder bond in the SB-6 wafer bonder would be to increase the thicknesses of the tin and gold layers to 9.3 µm and 180 µm, respectively.

Au-Sn TLP solder wafer bonding is a good method for applications where only attachment is needed and not hermetic sealing. The materials are common in MEMS manufacturing and the gold layer makes this an effortless fluxless bonding process. The bond strength is higher than the fracture strength of a Pyrex™ wafer, which is high enough for many wafer bonding and die attachment applications [67]. However, the voids left in the bond cross-section that result from rapid IMC growth preclude the use of this bonding technique for creating hermetic seals in standard wafer bonders unless a thicker tin interlayer is used to reduce the required heating rate.

3.3.2 Nickel-Tin

Another material system, Ni-Sn, was investigated as a TLP solder bonding system. Nickel-tin also uses common MEMS manufacturing materials. However, the IMC formation rate is orders of magnitude lower than the IMC formation rate for gold-tin, which reduces the heating rate requirement for void-free TLP solder bond formation. This occurs because it will take longer for the IMC to consume the interlayer during the heating in Stage 1. Also, a nickel-tin process has the potential for becoming a completely gold-free wafer bonding process. Gold is a major contaminant for IC manufacturing and therefore not a welcome material in some large MEMS foundries that also produce ICs. A wafer bonding process that is gold-free, can planarize over wafer topography, and is performed at low-temperatures is attractive for wafer-level hermetic sealing in a manufacturing process with stringent cleanliness requirements. The disadvantage for using a nickel-tin TLP solder bond process is that it loses the effortless flux-free capability that a gold parent metal provides, because unlike the gold, the nickel forms a native oxide when exposed to atmosphere. With proper joint design and an extra processing step, the nickel-tin TLP solder bond can also be a flux-free process.
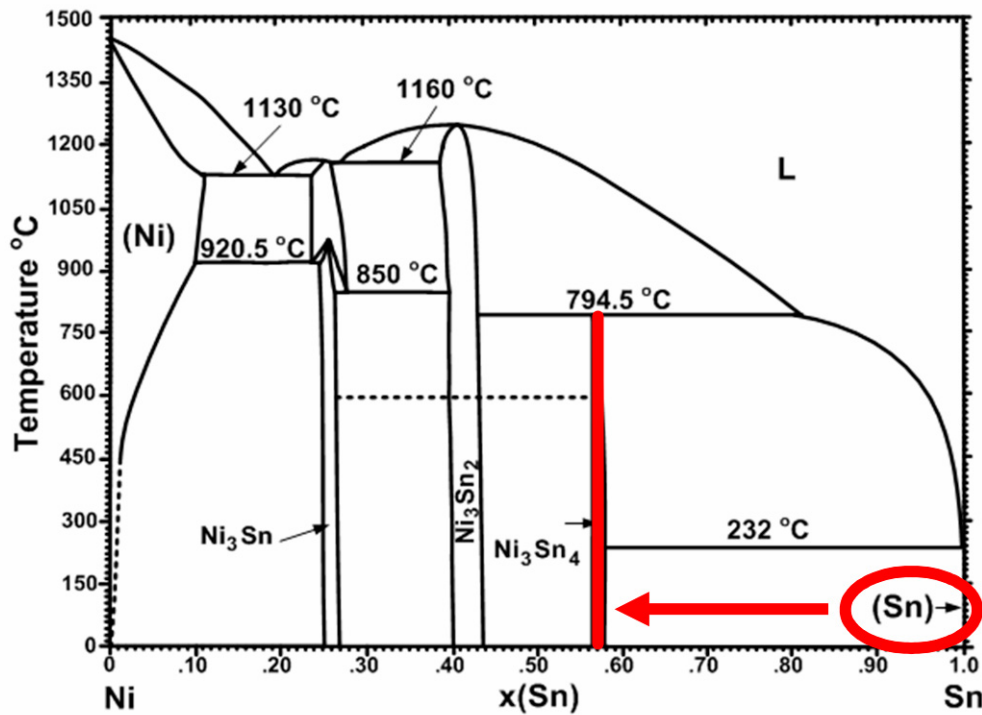
Figure 3.8 The nickel-tin phase diagram. The transformation of the pure tin interlayer to the nickel-tin IMC is highlighted in red.

Figure 3.8 shows the nickel-tin binary phase diagram with the phase transformation from pure tin to the terminal IMC highlighted in red. The interlayer is deposited as pure tin, which melts at 232 °C. After the Ni-Sn TLP solder bond is completed, the bond joint will consist of Ni_3Sn_4 IMC sandwiched by pure nickel. The re-melting temperature of the bond should approach 800 °C.

The wafer bond was created by bonding a silicon wafer to a Pyrex™ wafer with a Ni-Sn TLP solder bond. The process starts by sputtering a chrome/gold (1kÅ/2.5kÅ) seed layer onto both wafers. Next, a photoresist mold is patterned on both wafers. Then both wafers undergo two plating steps to create the 300 μm wide bond rings (5 μm of nickel and 3 μm of tin). Next, a protective photoresist layer is spun over both wafers and patterned to be 20 μm wider than the bond ring. Then the seed layer is etched on both wafers. Figure 3.9 shows the cross-section of the wafers prior to bonding.
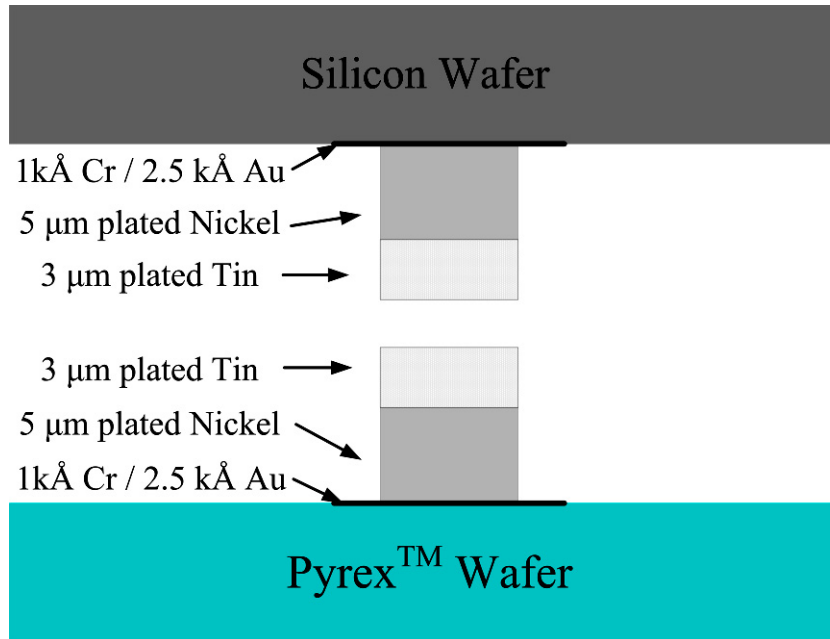
Figure 3.9 Illustration of the cross-section of the Ni-Sn TLP solder bond directly before bonding. The tin interlayer is deposited on both sides of the bond joint to prevent the nickel parent metal from oxidizing.

Unlike previous flux-free, solder-based bonding processes that used a thin film of gold to prevent the nickel barrier layer from oxidizing (Section 2.2.2), this bonding process uses the tin interlayer itself as a barrier layer to prevent oxidation. The tin also forms a native oxide, but this oxide is easily broken by the tool force applied by the wafer bonder once the tin is molten.

Before any heating, the chamber is pumped to vacuum and a pressure of 100 kPa is applied to the wafers (resulting in a pressure of 5 MPa at the bond rings). The wafers are bonded at 300 °C with a heating rate of 60 °C/min, just as the gold-tin TLP solder wafers were heated. The wafers were held at the bonding temperature for 1 hour, and then cooled to room temperature. The entire bond sequence, from room temperature to unloading the completed wafers, lasts approximately 1.5 hours.

The bonded wafers were pried apart with a razor blade to qualify the strength of the Ni-Sn TLP solder bond. Similar to the Au-Sn TLP solder bond, the bond strength was higher than the fracture strength of the Pyrex™ wafer. A SEM picture of the transferred Pyrex™ is shown in Figure 3.10.
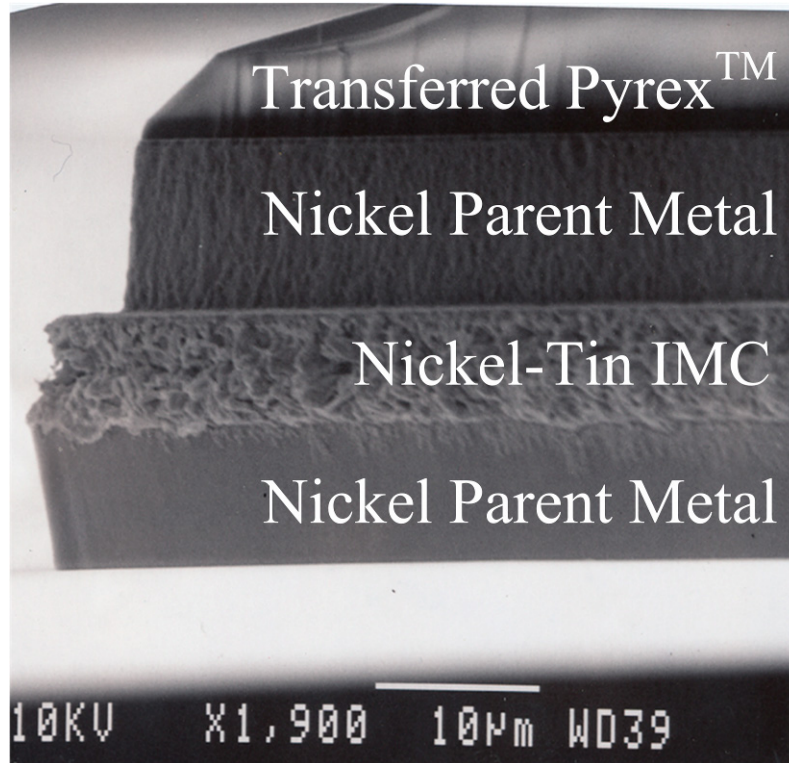
Figure 3.10 SEM image of a Ni-Sn TLP solder bond. The bond is stronger than the fracture strength of a Pyrex™ wafer.

The cross-section of the Nickel-Tin bond was inspected by dicing through one of the bond cross-sections. The dicing saw was used because the ductility of the Nickel-Tin TLP solder bond was too tough to allow for cleaving of the cross-section as was done for the Gold-Tin TLP solder bonded wafers. A SEM image of the cross-section with Energy Dispersive X-Ray (EDX) elemental analysis is shown in Figure 3.11.
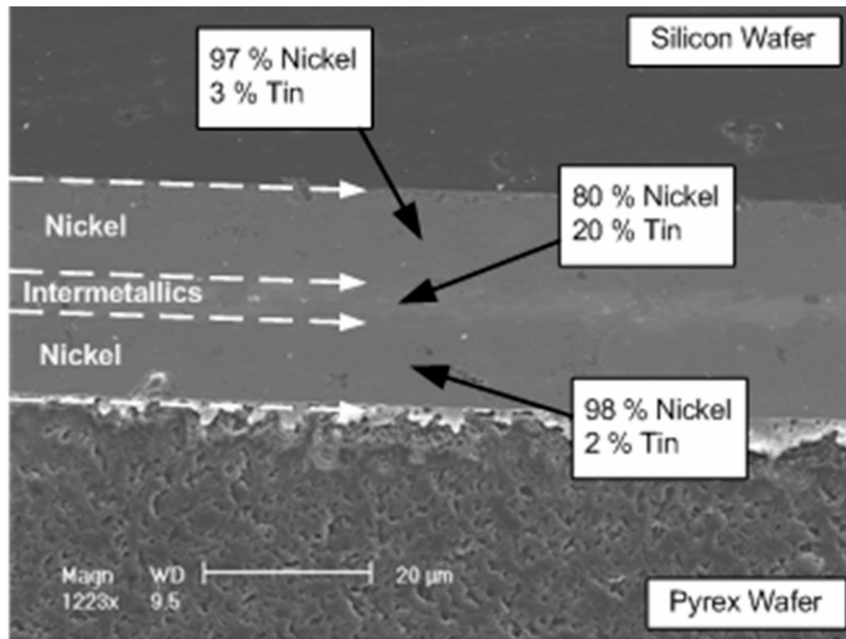
Figure 3.11 A void-less Nickel-Tin TLP solder bond. A thicker interlayer and lower intermetallic formation rate combined to create a quality TLP solder bond without voids.

It is evident from the picture that the Ni-Sn bond joint is free from voids. The intermetallic layer is distinguishable from the nickel parent metal as the lighter gray section in the middle of the bond joint. The interlayer was further identified with EDX analysis, which showed an element ratio of 80% nickel and 20% tin, which closely corresponds to the Ni_3Sn intermetallic phase on the binary nickel-tin phase diagram. Other much thinner bond joints on the wafer, as thin as 50 μm, showed similar void-free results (Figure 3.12).
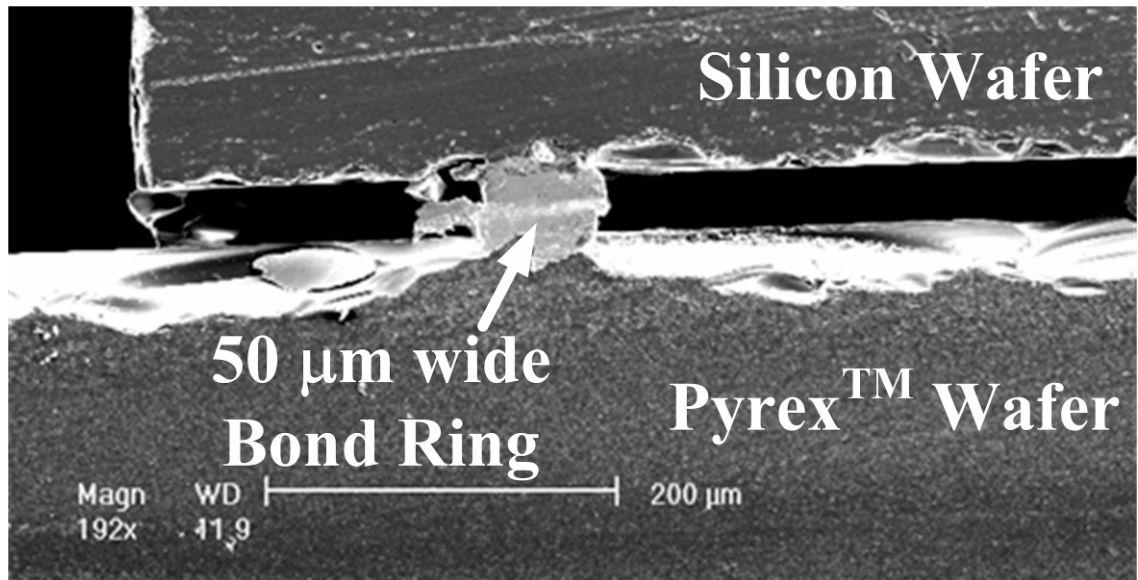
Figure 3.12 A 50 µm wide nickel-tin TLP solder bond joint. The minimum thickness for a TLP solder bond joint is more limited by the shear strength than the hermetic capabilites of the bond.

The nickel-tin TLP solder bonds showed the void-free quality that is necessary for creating a wafer-level hermetic bond. The thicker electroplated tin interlayer and slow nickel-tin IMC formation rate enabled some tin interlayer to remain unaffected by IMC growth during the heating in Stage 1 of the TLP solder bonding process. The pure interlayer then melted in Stage 2, filling the gaps in the bond cross-section and forming a void-free bond joint. This wafer bonding technique was used to produce wafer-level vacuum packages that are reported in detail in Chapter 4. The hermeticity, shear strength, and re-melting temperature testing data were measured from these vacuum packages. The hermeticity is discussed in detail in Chapter 4. The shear strength and re-melting temperature are discussed at the end of this Chapter in Sections 3.4.2 and 3.4.3. The results from these tests for the Nickel-Tin TLP solder bond are summarized in Table 3.4.

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Table 3.4 Test results for Nickel-Tin TLP solder wafer bonding.

Metric	Test Methodology	Result
Hermeticity	Long-term vacuum data	$1.7 \cdot 10^{-15}$ atm·cc·s^{-1}
Strength	Shear Test	12.1 MPa
Re-melting Temperature	Hotplate	> 450 °C

3.3.3 Gold-Indium

In the interest of reducing the bonding temperature even further, the Au-In TLP solder bonding system was investigated. Indium is the other common low-melting point interlayer (aside from tin) that is used for low-temperature TLP solder bonding. Indium melts at an even lower temperature (156 °C) than tin (232 °C), which enables bonding temperatures of 200 °C and lower. Gold was chosen as the parent metal because it does not form native oxide and is therefore easily wet by molten indium without any fluxes. One advantage to the Au-In system compared to the Au-Sn system is that the IMC formation rate is much slower (< .3 µm/hr at room temperature for Au-In versus ~ 13 µm/hr at room temperature for Au-Sn) [56]. Also, the wafers require less time heating up to the melting temperature of an indium interlayer bond compared to a tin interlayer bond because indium's melting point is lower than tin's, so there is less time for IMC growth during Stage 1 heating. There are several disadvantages of choosing indium over tin as the TLP solder bond interlayer. Indium is a rare, expensive metal. The price of indium has fluctuated between $500 and $1000 per kilogram over the last few years [68]. Compared to the price of tin, which has skyrocketed to the lofty price of $12 per kilogram this year [69], indium is prohibitively expensive for some soldering applications. That being said, a very small amount of indium is used per wafer bond (only ~ 14 g per wafer was used in the very inefficient evaporator for this experiment) so the solder costs are small compared to other MEMS processing costs. Another disadvantage of indium is its stubborn native oxide. In_2O_3 has a free energy of formation at 25 °C of -620 kJ/mol, which is almost a factor of 2 higher than SnO (-260 kJ/mol) [20]. The stability of the indium oxide necessitates a different approach from that used with tin interlayers to create a fluxless process. A simple solution is to apply a thin layer of gold directly onto the indium in-situ during the indium deposition. If the indium is deposited using e-beam evaporation or sputtering, this can be done by changing pockets or targets and putting

down a quality film on top of the Indium. If electroplating is used to deposit the Indium, it is much more challenging to deposit this layer. The indium must be removed from the electroplating bath and placed into the vacuum chamber for physical vapor deposition without exposing the indium surface to an oxidizing environment. For these two reasons, Au-In should only be used as a wafer bonding method if the wafer cannot tolerate the higher temperatures used for the tin-interlayer techniques presented in this work.

Gold and indium can form several IMCs that are stable to temperatures around 500 °C (Figure 3.13). The IMC that melts at the coolest temperature is the Au-In phase, at 509 °C, giving the Au-In TLP solder bonding technique a theoretical melting temperature of over 500 °C.
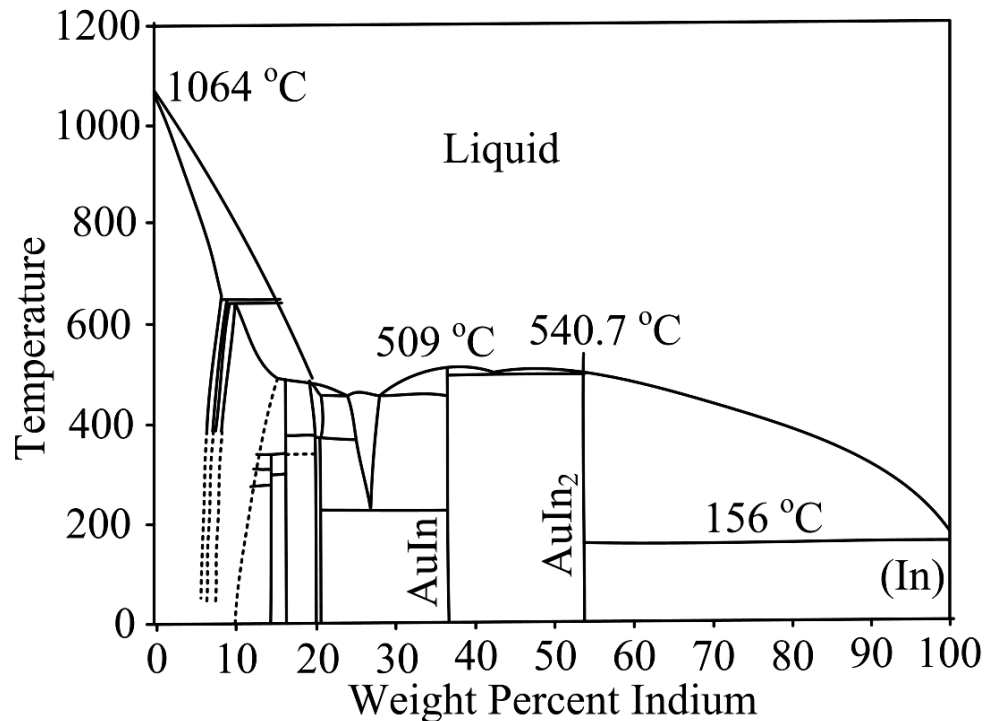
Figure 3.13 The gold-indium binary phase diagram (Adapted from [70]). Au-In is the lowest melting point phase left in the completed Au-In TLP solder bond joints, giving this bond a theoretical re-melting temperature of over 500 °C.

The wafer bonds were created between two silicon wafers. First, a seed layer (1kÅ Cr – 2.5 kÅ Au) is sputtered over both wafers. A photoresist mold masks the seed layer for the 300 μm wide, 5 μm thick gold bond rings that are electroplated onto each wafer. Next,

a 2 μm thick indium layer is evaporated onto the bond rings on one wafer, followed in-situ by a 1 kÅ layer of gold that forms a protective layer of gold-indium intermetallics. This step prevents indium oxidation and enable the fluxless TLP solder bonding. The indium-gold metal stack is patterned by a liftoff process. The cross-section of the two wafers directly before bonding is shown in Figure 3.14.

Figure showing cross section with labels:

Silicon Cap Wafer

1kÅ Cr / 2.5 kÅ Au
5 μm plated Au
20 kÅ In – 1 kÅ Au

5 μm plated Au
1kÅ Cr / 2.5 kÅ Au

Silicon Device Wafer
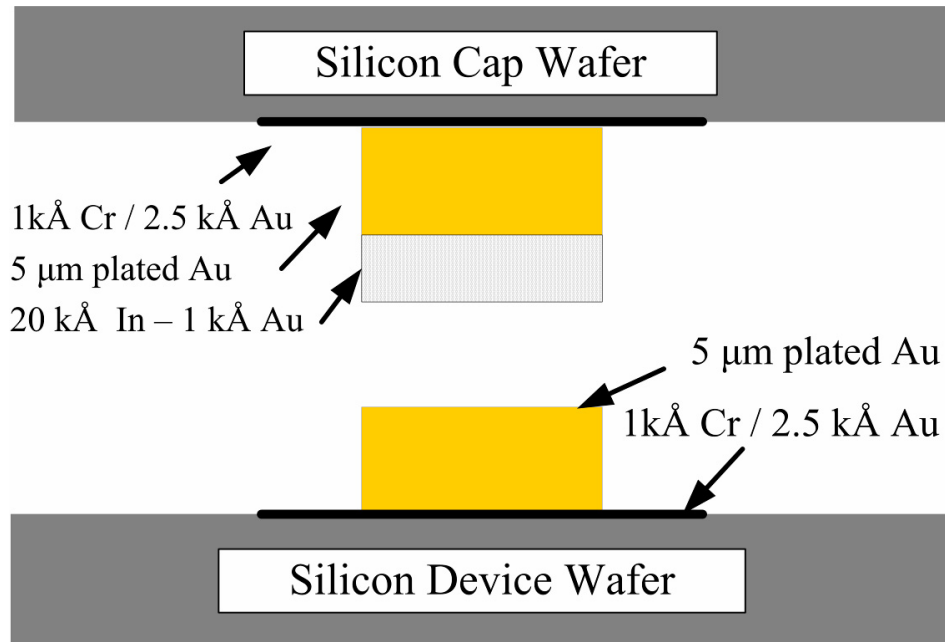
Figure 3.14 Cross-section of the Au-In TLP solder bond directly before bonding. 1 kÅ of gold is deposited in-situ on top of the indium interlayer so the process can be flux-free.

The wafer pair is then aligned and bonded. The heating rate for this bond is ~ 60 °C/min. After heating to 200 °C, the wafers are held for 1 hour to complete the bond. During the bond process, a tool pressure of 500 kPa (8 MPa at the bond rings) was applied to the wafer stack to ensure the thin gold-indium oxidation prevention layer is broken to reveal fresh molten indium during the bond. The entire bond cycle, from room temperature to unloading the finished wafer pair, takes 1.25 hours. Once the wafers were finished and unloaded, a bond ring was cut with the dicing saw to inspect the cross-section. A SEM image of the cross-section is shown in Figure 3.15.
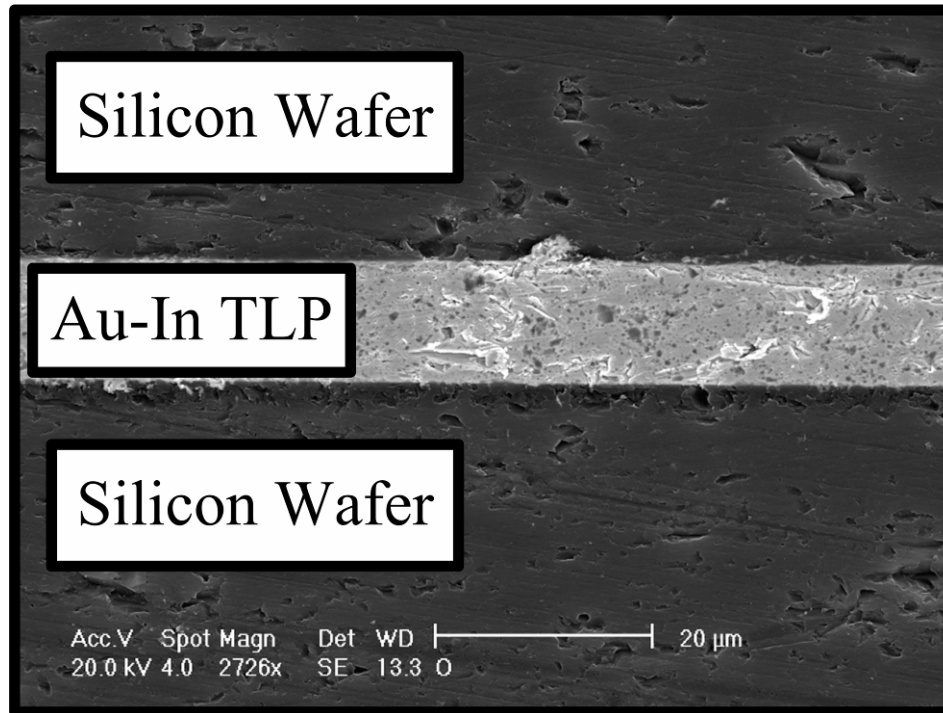
Figure 3.15 SEM image of the cross-section of a Au-In TLP solder bond. The bond is formed with a maximum temperature of 200 °C.

The gold-indium TLP solder bonds showed the void-free quality that is necessary for creating a wafer-level, hermetic bond. The slow gold-indium IMC formation rate enabled some indium interlayer to remain unaffected by IMC growth during the heating in Stage 1 of the TLP solder bonding process. The pure indium interlayer then melted in Stage 2, filling the gaps in the bond cross-section and forming a void-free bond joint. The hermeticity, shear strength, and re-melting temperature testing data were measured from these vacuum packages. The shear strength and re-melting temperature are discussed at the end of this Chapter. The results from these tests for the Gold-Indium TLP solder bond are summarized in Table 3.5. This wafer bonding technique was used to produce wafer-level vacuum packages that are reported in detail in Chapter 4. The hermeticity is discussed in detail in Chapter 4.

Table 3.5 Test results for Gold-Indium TLP solder wafer bonding.

Metric	Test Methodology	Result
Hermeticity	Long-term vacuum data	$1 \cdot 10^{-16}$ atm$\cdot$cc$\cdot$s^{-1}
Strength	Average Shear Strength	24.4 MPa
Re-melting Temperature	Hotplate	> 450 °C

3.4 Testing the Wafer Bonds

There are several properties of wafer bonding techniques that are important to characterize if these bonding approaches are to be used for a wafer-level MEMS vacuum packaging process. First, the hermeticity of the bonds should be characterized. This is difficult to measure because the standard hermetic testing techniques, like helium leak-rate testing, cannot be applied for MEMS packages due to their stringent leak rate requirements. Also, the strength of the bonding technique is important for designing the minimum bond area necessary to keep the package lid attached throughout the rest of the assembly process. The shear strength of each bonding technique was characterized using a home-built shear testing setup. Lastly, for TLP solder bonding only, the re-melting temperature of the bonding techniques was characterized by placing the bond on a hotplate and then testing for bond failure. Each test is explained in its own section and the results for each bonding technique (Au-Sn solder, Au-Sn TLP solder, Ni-Sn TLP solder, and Au-In TLP solder) are presented here for discussion.

3.4.1 Hermeticity Testing

Testing the hermeticity of packages with such small internal volumes is difficult, if not impossible with the industry standard helium leak-rate test. A helium leak-rate test begins by exposing the package to several atmospheres of helium pressure to force helium atoms into it. After the helium is forced into the package, the package is placed in a reduced atmosphere and a helium detector measures the amount of helium coming from the package. Typically, helium leak-rate testing is used as the standard for measuring the leak-rates of everything from electronic packages to pressure chambers to bubble packs used in the pharmaceutical industry; it is also the standard for qualifying packages for the United States Military [67]. Because it is an industry standard, helium leak-rate testing is widely reported in the literature as verification of hermetic capabilities. However, most

data published for MEMS packaging is questionable unless the reported package volume is larger than 1 μL. This is because even the best helium testers can only measure a minimum leak-rate of 10^{-12} atm·c.c.·s^{-1} [71]. A leak of this magnitude would allow all the helium in such a small volume to escape during the transfer between the helium bomb chamber and the vacuum chamber. If there is not any helium inside the package, the helium detector will not register a leak and therefore the minimum leak will be reported when it is in fact much higher. This problem was reported by researchers investigating BenzoCycloButene (BCB) as a hermetic wafer bonding technique [72]. A much more reliable method was used to characterize the hermeticity of the wafer bonding techniques in this chapter.

The hermeticity of the wafer bonds were tested by creating vacuum packages with integrated vacuum sensors. The details of the leak rate measurement technique are presented in Chapter 4, but the results for the different bonding techniques are summarized here in Table 3.6.

Table 3.6 Leak rates for the wafer bonding techniques presented in this chapter. Details of the measurement technique are presented in Chapter 4.

Bond Type	Bond Temperature	Days of Vacuum Data	Leak Rate
Au-Sn Solder	300 °C	93	$1.5 \cdot 10^{-15}$ atm·cc·s^{-1}
Au-Sn TLP Solder	300 °C	0	very high
Ni-Sn TLP Solder	300 °C	220	$1.7 \cdot 10^{-15}$ atm·cc·s^{-1}
Au-In TLP Solder	200 °C	184	$1 \cdot 10^{-16}$ atm·cc·s^{-1}

All of the bonding techniques show good hermeticity, except for the Au-Sn TLP solder bond. Standard commercial wafer bonders were incapable of meeting the heating rate requirements for creating a void-less Au-Sn TLP solder, therefore there were many gaseous conduction paths throughout the bond cross-section. All of the other bonding techniques confirm the fact that metals are the best materials for creating hermetic seals due to their extremely low permeability. The leak rates reported in this section are based on the worst-case line that will fit in the long-term vacuum measurement of the packages; there is not an observable leak. Therefore, as more data is taken over time, the leak rate will decrease.

3.4.2 Strength Testing

The bond strength is an important metric for wafer bonding technologies. There are many different ways of testing bond strength, including: the razor blade test [73], burst-pressure testing [3], shear or pull testing [5], and the micro-chevron test [74]. Since the wafer bonds in this thesis are being used to create MEMS packages, the shear/pull test was chosen as the testing method because it provides the most useful information for wafer bonds that create MEMS packages.

The military specification (MIL-STD-883F) for testing micropackages is commonly cited as the preferred method for qualifying package quality across many metrics [12]. In those specifications, two strength tests are covered: pull strength tests (Method 2011.7) and shear strength tests (Method 2019.7). The pull test covered in Method 2011.7 of MIL-STD-883F is presented as a technique for testing wirebonds. To apply this testing technique to measure the strength of wafer bonds would require the design of a pull test jig that can grab one side of the wafer bond (the package cap) and apply enough axial force to rip the wafer bond apart. Usually this is performed with a gripper or epoxy, but it can be a challenge to grip or attach with sufficient force to break strong bonds. Because of its limited coverage in the military testing specifications and the difficulty in designing the test setup, the shear test method was used to measure the strength of the wafer bonds. The shear test is covered in detail in MIL-SPEC-883F, Method 2019.7.

The shear test works by applying a transverse force, F_S to the chip parallel to the substrate. Figure 3.16 shows how the force is applied perpendicular to the edge of the die by a contact tool, or wedge. The shear stress, τ_S, seen on the bonded area, A_d, is therefore:

$$\tau_S = F_S \big/ A_d \tag{3.14}$$

Once the transverse force creates a shear stress that exceeds the shear strength of the wafer bond, the wafer bond will fail and the package cap shears off.
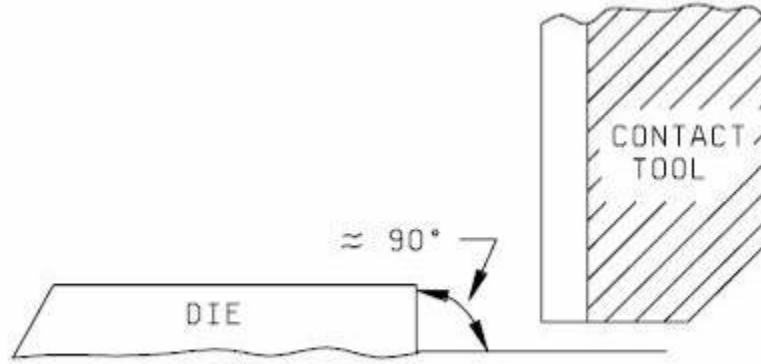
Figure 3.16: A drawing of a partial shear test setup from MIL-SPEC-88F, Method 2019.7. [67].

The military testing specifications contain failure criteria that were used to evaluate the packages. Figure 3.17 illustrates three different standards for testing die shear.
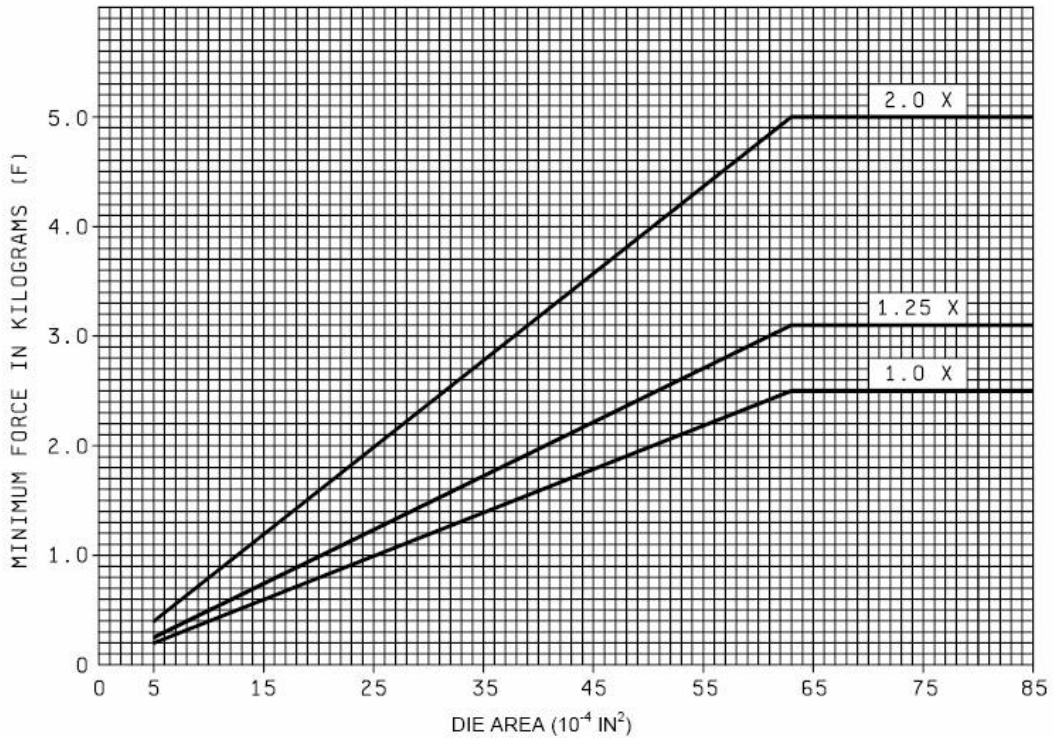
Figure 3.17: The shear strength failure criteria from MIL-STD 883 for three separate cases. The most stringent (2.0 X) was used for qualifying the wafer bonds in this work [67].

The first curve, 1.0 X, applies to a failure where 50% of the material stays adhered to

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the die after the bond is broken. If less than 50% of the material transfers, then the 1.25 X curve should be used. The 2.0 X curve applies to cases where less than 10% of the bond area is covered by transferred material. The most conservative of the three cases, 2.0 X, was used to define PASS/FAIL criteria for these packages. The 2.0 X curve corresponds to shear strength of 12.3 MPa, the package passes if the shear strength of the wafer bond is higher than this value. The next section discusses the design and operation of the shear test setup.

THE SHEAR TEST SETUP

The shear test setup was conceived, designed, and constructed in cooperation with another PhD student in our research group, Jay Mitchell. His thesis contains more information on the theory of shear testing and the shear test setup [5].
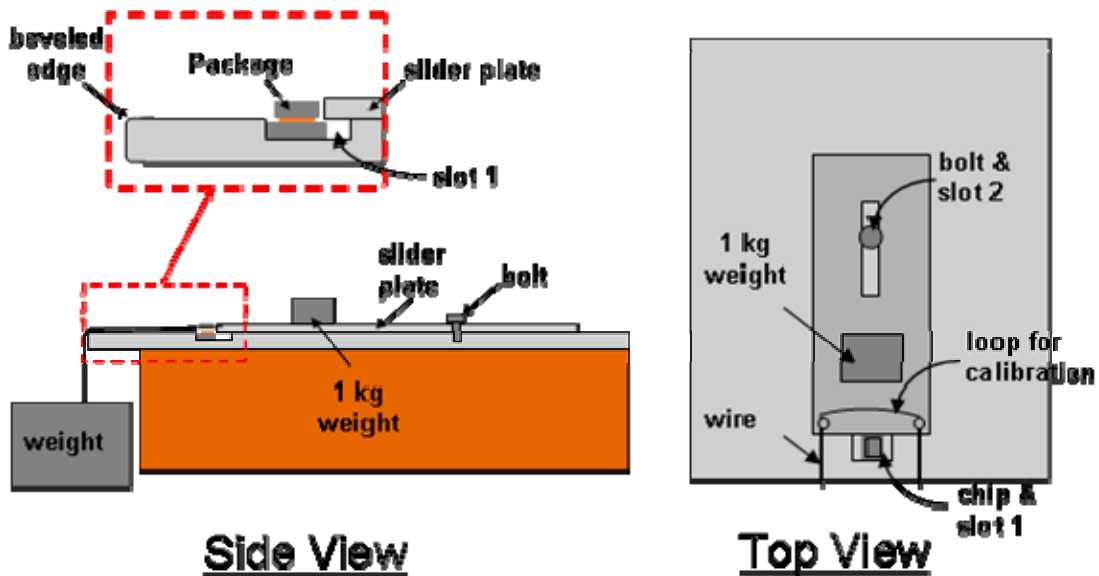
Figure 3.18 Illustration of the shear test setup [5].

An illustration of the shear test setup is shown in Figure 3.18. The shear force is applied by weights acting on a thin aluminum slider plate that moves parallel to the package surface (see Side View inset). The slider plate sits on top of a larger base plate for support. Slot #1 in the base plate holds the package under test. The slot is machined to a depth of 560 μm, which is ~ 60-100 μm deeper than the bottom wafer of the package. The weights are attached to the slider plate with polymer-coated, stainless steel wire. The

top view of the test setup shows slot #2 in the slider plate. This allows for a safety bolt to be threaded through the slot into the base plate. The bolt provides a safety stop that keeps the aluminum plate from sliding away after the package shears. A 1 kg weight is placed on the slider plate to keep it flush with the base plate to prevent the package from rotating during testing. Figure 3.19 is a photograph showing a package sitting in slot #1 with the slider plate applying a force perpendicular to the edge of the package cap.
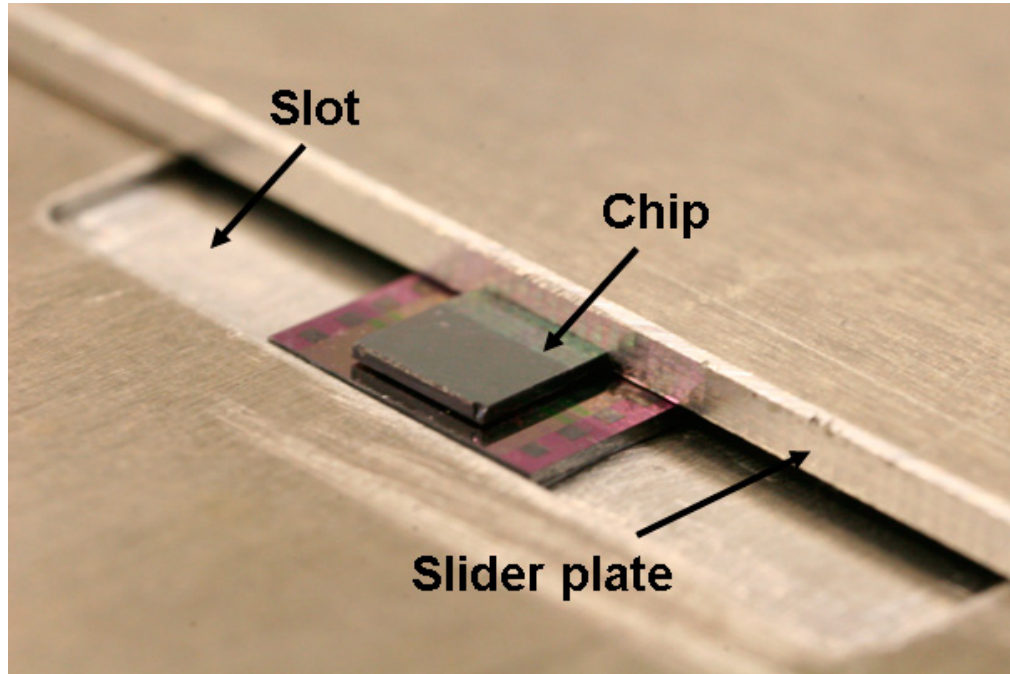
Figure 3.19 Photograph of a package sitting in the shear test setup. The slot and slider plate apply the shear force perpendicular to the package cap edge.

The tests were conducted by adding 0.66 kg weights to the wires attached to the slider until the package broke or the capacity of the test setup was reached. The force that the aluminum slider plate applies to the package was calculated by calibrating the shear test setup. Equation (3.15) shows the formula used to calculate the force from the aluminum slider plate:

$$F_{applied} = ((0.734) \cdot (0.66 \, \text{kg} \cdot W_n - 0.33 \, \text{kg}) - 0.5 \, \text{kg}) \cdot 9.8 \, \text{m}/\text{s}^2 \qquad (3.15)$$

Where, W_n is the number of weights in the setup when the package fails. Only half of the final weight (0.33 kg) is counted towards the total weight, because it cannot be known

how much of the final weight was needed to cause the failure. This uncertainty is counted as an error of ± 0.33 kg. The total error in the measurement from the weight uncertainty, friction forces, and calibration error is ± 0.64 kg, which corresponds to a force of 6.27 N [5]. The shear stress is calculated by dividing the applied force by the bond area, which is 0.030 cm^2 for all packages tested.

PACKAGE TESTS

Wafer pairs full of packages from the Au-In TLP solder, Ni-Sn TLP solder, and Au-Sn solder bonding technologies were tested by selecting 20-30 packages from various parts of the wafer and shearing off the package caps. The packages were placed in the setup and weights were added until the package broke or the capacity of the setup was reached. The packages failed in one of two ways. In the first, the package cap sheared cleanly away from the bottom wafer without a transfer of material or fracturing of either wafer. It is clear in this case that the shear strength of the wafer bond has been exceeded because it was the only thing that failed. In the second case, which typically happened when large shear forces were applied, the bond remained intact but one or both of the silicon wafers fractured. In this case, it is not clear if the shear strength of the wafer bond has been exceeded because the bond remained intact. A third outcome of the test is that the capacity of the test setup was reached. The maximum number of weights the setup can hold is 20, which corresponds to shear strength of 28.9 MPa. This is well over twice the most conservative criteria from the military testing specifications. The outcome of the test is included in the reported data: sheared, not-sheared, or not broken to indicate which of the three outcomes occurred for each die. The data includes: the number of weights, the applied force, the shear stress, the test outcome, and a PASS/FAIL indication. The die passed if the shear strength exceeded 12.3 MPa.

The shear strength data from the wafer bonds is summarized in Table 3.7. The data shows that the Au-Sn solder bond is the strongest, followed closely by the Au-In TLP solder bond, and then the Ni-Sn TLP solder bond is the weakest.

Table 3.7 Summary and comparison of the shear strength data from all tested wafer bonding techniques.

	Ni-Sn TLP Solder Bond	Au-In TLP Solder Bond	Au-Sn Solder Bond
# of Die	24	29	26
PASS	46%	97%	100%
FAIL	54%	3%	0%
Average	12.1 MPa	24.4 MPa	28.0 MPa
Median	10.1 MPa	25.8 MPa	28.9 MPa
St.Dev.	9.0 MPa	5.1 MPa	2.1 MPa
Max	28.9 MPa	28.9 MPa	28.9 MPa
Min	0.0 MPa	11.7 MPa	21.1 MPa

Nickel-Tin TLP Solder Bond Strength Results

The Ni-Sn TLP solder bond was the weakest of the three wafer bonding techniques tested. Less than 50% of the package dies passed the most stringent of the MIL-STD testing requirements. This result is not surprising given the reported results of other strength testing of solder bonds. Se-Hoon studied the effect of Ni-Sn intermetallic phase growth on the shear strength of solder bumps [31]. They found that thicker IMC layers formed by extended heating cycles caused a marked reduction in the shear strength of the solder bonds. The brittle nature of the intermetallic phases and their poor adhesion to other phases in the joint leads to this low shear strength [20].

The low shear strength of the Ni-Sn TLP solder technique is a concern if it is to be used as a wafer-level MEMS vacuum packaging process. However, there is potential for shear strength improvement by process optimization. The large standard deviation of the strength measurements indicates that there were many die strong enough to satisfy the test requirements. With more understanding of the bonding process, and why some die were so much stronger than others, would lead to an improvement in the bond design and its shear strength.

Gold-Indium TLP Solder Bond Strength Results

The Au-In TLP solder bond showed much higher bond strength than the Ni-Sn TLP solder bond; it was the strongest TLP solder bond investigated in this work. Only 1 die out of the 29 tested failed the most stringent military standard for die strength. One

reason for the much larger strength for Au-In TLP solder compared to Ni-Sn could be due to the shorter time it takes for Au-In TLP solder bonds to homogenize as the IMC diffuse away from the bond joint during Stage 4. It has been reported that the homogenization rate is proportional to the IMC compound formation rate [51]. Since the Au-In IMC formation rate is much faster than Ni-Sn, it will reach its final microstructure faster as the IMC diffuse away from the center of the bond leaving behind a pure Au metal bond. The strength of the Au-In TLP solder bond was high, but not as high as the Au-Sn solder bond.

Gold-Tin Solder Bond Strength Results

The Au-Sn solder bond showed the highest shear strength of the three wafer bonding techniques tested. All the die tested passed the MIL-STD specification. Furthermore, very few of them actually even broke in the setup because most of the die were stronger than the maximum stress that could be applied by the test setup (28.9 MPa). Most of the bond joint cross-section is formed by the eutectic composition of Au80Sn20, which has a very high shear strength [34]. The shear strength for the Au-Sn solder measured here agrees well with other published data.

The standard solder bond was the strongest of the three bonds because the bond joint is made up of mostly the eutectic composition of Au-Sn instead of brittle intermetallics. For applications with high strength requirements, Au-Sn solder is optimal. For other applications that have more demanding thermal requirements, such as high service temperatures, the TLP solder bonds are better suited due to their higher re-melting temperature than bonding temperature. The re-melting temperature for Au-In and Ni-Sn TLP solder bonding is reported in the next section.

3.4.3 Re-melting Temperature Test Results

One of the major advantages of TLP solder bonding is a higher service temperature than its formation temperature. A higher service temperature is a big advantage in MEMS vacuum packaging because the bond used to create the vacuum package is the first in a long line of bond steps that it takes to assemble the MEMS into other systems. After the

vacuum package bond, the chip is heated up to 220 °C at least one more time for solder bonding to the PC board. The bond that is used to create the vacuum seal is required to survive this bond. The current solution uses high temperature solders as the first bonds, and then steps down to lower melting point solders for the subsequent bonds. Lower melting point solders must be used for the final assembly steps because the temperature cannot approach the eutectic temperature of the solders already present in the assembly. Au-Sn is a standard solder for these early solder bonding steps, like vacuum seals, because it is formed at 350 °C and will not re-melt until 280 °C. Au-Sn is acceptable, if the MEMS structures can tolerate such a high temperature. TLP solder bonds, like Au-In, do not have the risk of re-melting once they are formed, so the temperature reduction steps are not necessary if they are used as the front-end bonds in a packaging sequence. This means that the maximum temperature of the entire packaging process has been reduced because the Au-In TLP solder bond replaces the high melting point solder normally used as a front-end bonding mechanism. Both Au-In and Ni-Sn TLP solder bonds were tested on a hotplate at 400 °C. The packages were measured to quantify their vacuum level and then they were placed on the hotplate at 400 °C for 5 minutes and measured again. If the pressure level inside the packages had risen after the hotplate test, the bond failed. Both Au-In and Ni-Sn packages survived the hotplate test.

3.5 Design Rules for TLP Solder Wafer Bonding

3.5.1 Choosing a material family

The advantages and disadvantages of the three TLP solder material families investigated as part of this work are presented below. Attributes of each material family limits their use to certain applications.

GOLD-TIN

Au-Sn TLP bonding is a simple fluxless technique that is best applied as a die attach method where hermeticity is not needed. Au-Sn TLP solder bonding is simple to make fluxless since gold is a noble metal that is easily wet by molten tin. This is true especially compared to a material system like Au-In TLP solder bonding, which requires gold on the indium interlayer to make it fluxless. Tin does not need a gold layer on top of it to

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prevent tin oxidation because the tin oxide is easily broken by the force from the wafer bonder when the tin interlayer is molten. Au-Sn TLP solder bonding is also attractive compared to Au-In TLP solder bonding because tin is not nearly as rare as indium and therefore less costly. Although it was not quantified, Au-Sn TLP solder bonding should also have high shear strength as evidenced by the Pyrex™ fracture during its qualitative strength testing. All of these positive attributes are overshadowed by the difficulty in using Au-Sn TLP solder as a hermetic bonding technique. The IMC formation rate between Au and Sn is so rapid that it takes extraordinary heating rates (> 300 °C/s) or very thick joints (> 80 μm) to produce void-free TLP solder bonds. Ni-Sn or Au-In TLP solder bonding material systems are better suited for applications that require hermetic seals.

NICKEL-TIN

Ni-Sn TLP solder bonding can provide a hermetic seal. It is also uses the most economical materials of all of the approaches here. Nickel is a commonly found metal used in a large number of industrial processes, and therefore least costly because of its abundance and economies of scale. Nickel electroplating solution costs 1/6 the price of a similar volume of gold electroplating solution. Combining nickel with the cheaper of the two interlayers, tin, produces the most economical TLP solder bond. A Ni-Sn TLP solder bond also relaxes the heating rate demands placed on the wafer bonding equipment used to produce the bonds because of the low IMC formation rate between nickel and tin. Ni-Sn TLP solder may be attractive to some large scale manufacturers because it can be made into a gold-free process, which is a cleanliness requirement for many major foundries. The biggest drawback in using Ni-Sn TLP solder is its low shear strength. The presence of a large Ni-Sn IMC layer weakens the bond joint; such that only half the die tested passed the MIL-STD specification for die shear strength. For some applications where other materials provide the mechanical strength for the package, like an epoxy overmold, this low shear strength may not be an issue.

GOLD-INDIUM

In many ways, Au-In TLP solder is the best technique of the three for creating MEMS

vacuum packages. It can create a hermetic seal at the lowest bonding temperature of 200 °C. It showed the highest shear strength of any of the TLP solder bonding techniques. Also, the process is not as complicated to create a fluxless bond. It is, however, the most costly of the three systems studied because it uses the most expensive parent metal, gold, and interlayer, indium. Also, the indium oxide can complicate processing if the indium is not deposited by physical vapor deposition where a gold layer can be applied in-situ over the indium to prevent oxidation. Despite these drawbacks, Au-In TLP solder shows the most promise as a wafer-level MEMS vacuum packaging technique.

3.5.2 Process Design

Once the material system has been chosen, design parameters like the joint layer thicknesses, bond ring area, interlayer deposition technique, and bond process settings can be calculated and chosen. The next several sections treat each parameter separately and demonstrate the calculations necessary to design a successful TLP solder. The constants necessary to calculate the parameters for the other two families are presented as well.

DETERMINE THE INTERLAYER THICKNESS

The first parameter that needs to be calculated is the interlayer thickness. This thickness will determine much of the rest of the bond joint and process design, such as the parent metal thickness and total bonding time.

To calculate the interlayer thickness, the planarization requirements and bonder heating rate must be known. The planarization needs could be a feedthrough thickness or other topography. Typical feedthrough thicknesses are several thousand angstroms, but could be as high as microns for low resistance feedthroughs. The heating rate should be as quick as is reasonable for the bonder used to apply heat to the wafers. For the SB6e used in this work, the heating rate was 60 °C/min, but other techniques that apply heat locally could heat the wafers much faster.

First, the heating rate should be used to calculate the thickness of IMC that grow during the heating of Stage 1 of the TLP solder bonding process. Section 3.2.1 presents

the background theory and equations that govern IMC layer growth during Stage 1. For many TLP solder bond systems, the IMC growth can be classified as interfacial rate limited or diffusion limited. A different equation is used to calculate the layer thickness for each growth rate type. For diffusion limited growth, Equation (3.16) applies:

$$h_p = \sqrt{2k_{eff}t} \tag{3.16}$$

For interfacial rate growth, Equation (3.17) applies:

$$h_p = k_{eff} \cdot t \tag{3.17}$$

Where the effective rate constant is calculated from Equation (3.11) using a T_i of 80% of the bonding temperature *in Kelvin*.

$$k_{eff} = \frac{1}{\Delta T} \int_{T_i}^{T_f} k_0 \, e^{\left(\frac{-E}{kT}\right)} dT \tag{3.18}$$

The IMC thickness is used to calculate the critical interlayer with Equation (3.19):

$$h_c = h_p \cdot C_p \left(\frac{\rho_p}{\rho_l}\right)^2 \Omega \tag{3.19}$$

Where, C_p is the mass fraction of Sn in the IMC, ρ_p and ρ_l are density of the IMC and interlayer, and Ω is a corrective factor for non-planar IMC growth. The thickness of the interlayer should be greater than twice this critical thickness. The parameters for the calculations in this section are shown for all material families in Table 3.8.

Table 3.8 Material constants used to calculate the critical interlayer thicknesses for the TLP solder material systems. The order of the reference numbers in the final column corresponds to the material family column (i.e. the first reference is for Au-Sn, second is for Ni-Sn, etc.).

Parameter	Au-Sn TLP Solder	Ni-Sn TLP Solder	Au-In TLP Solder	Reference
Limiting rate	diffusion	diffusion	interfacial	[66][75][56]
k_0	$5 \cdot 10^4 \ \mu m^2/s$	$3.2 \cdot 10^9 \ \mu m^2/s$	$3.417 \ \mu m/s$	[66][75][56]
E	0.607 eV	1.326 eV	0.321 eV	[66][75][56]
T_f	505 K	505 K	473 K	[66][75][56]
T_i	404 K	404 K	378 K	[66][75][56]
C_p	38%	57%	53%	Phase Diagram
ρ_p	$19.72 \ g/cm^3$	$8.64 \ g/cm^3$	$10.2 \ g/cm^3$	[76][77][78]
ρ_l	$7.31 \ g/cm^3$	$7.31 \ g/cm^3$	$7.31 \ g/cm^3$	[79]
Ω	3	3	3	[51]

The material constants listed above were used to calculate the effective growth rate over the temperature range (from 80% to 100 % of the bond temperature). The integral from Equation (3.18) does not have a closed form solution, so MATLAB™ was used to numerically calculate the integral. The effective growth rates for each material family are presented in Table 3.9. It is interesting to note that the effective growth rate is independent of the heating rate.

Table 3.9 Effective growth rate constants calculated by numerical approximation of the integral in Equation (3.18) with MATLAB™.

Material System	Initial Temperature	Bond Temperature	Calculated k_{eff}
Au-Sn TLP Solder	404 K	505 K	$0.0135 \ \mu m^2/s$
Ni-Sn TLP Solder	404 K	505 K	$2.8813.10\text{-}5 \ \mu m^2/s$
Au-In TLP Solder	378 K	473 K	$6.0528.10\text{-}4 \ \mu m/s$

The effective growth rate can be substituted along with the heating time from 80% of the bond temperature (calculated from the heating rate) into Equations (3.16) and (3.17) to calculate the IMC layer thickness at the end of Stage 1. This thickness is substituted into Equation (3.19) to calculate the critical interlayer thickness. The critical interlayer thicknesses for the three material systems for a range of heating rates are plotted in Figure 3.20.
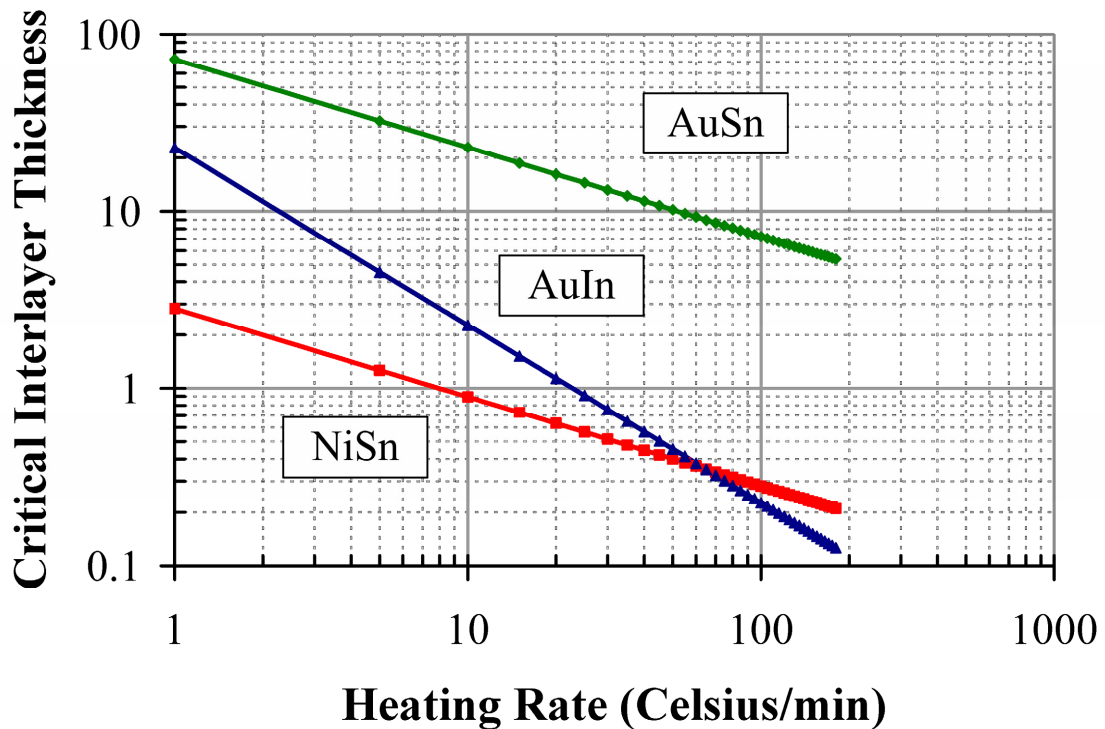
Figure 3.20 Plot of the calculated critical interlayer thickness for the three TLP solder material systems studied in this work. The heating rate used for these bonds was 60 °C/min.

From the graph in Figure 3.20, the critical interlayer thickness for a given heating rate can be found for the material family. Note that the Au-Sn TLP solder material system requires very thick interlayers to produce void-free bonds at reasonable heating rates. For the heating rate of 60 °C/min used in this work, the critical interlayer thicknesses are 9.3 μm, 0.36 μm, and 0.38 μm for the Au-Sn, Ni-Sn, and Au-In TLP solder bond material systems, respectively. With this heating rate, these critical layer thicknesses are the *minimum* necessary to create a void-free bond without having to planarize over any feedthroughs or other topology. The topology thickness should be added to this minimum calculated value. Therefore, for a feedthrough that is 2000 Å thick, the *minimum* interlayer thicknesses become 9.5 μm, 0.56 μm, and 0.58 μm for the Au-Sn, Ni-Sn, and Au-In TLP solder bonds.

DETERMINE THE PARENT METAL THICKNESS

Once the interlayer thickness is known from the calculations in the previous section,

the parent metal thickness can be calculated from the binary phase diagram for the material system in use. The target terminal bond composition will determine the amount of parent metal needed; therefore, there is some design latitude in selecting the parent metal thickness. If the bond requirements can tolerate a large proportion of IMC in the final bond joint, then a thick parent metal may not be necessary. However, if the target final microstructure is a solid solution of the interlayer dispersed among the parent metal, then a thick layer of parent metals is needed. Figure 3.21 shows the Au-In binary phase diagram. If the indium is < 5 % by weight of the final joint then it will eventually (with enough heating) be dispersed as a solid solution among the gold parent metal.
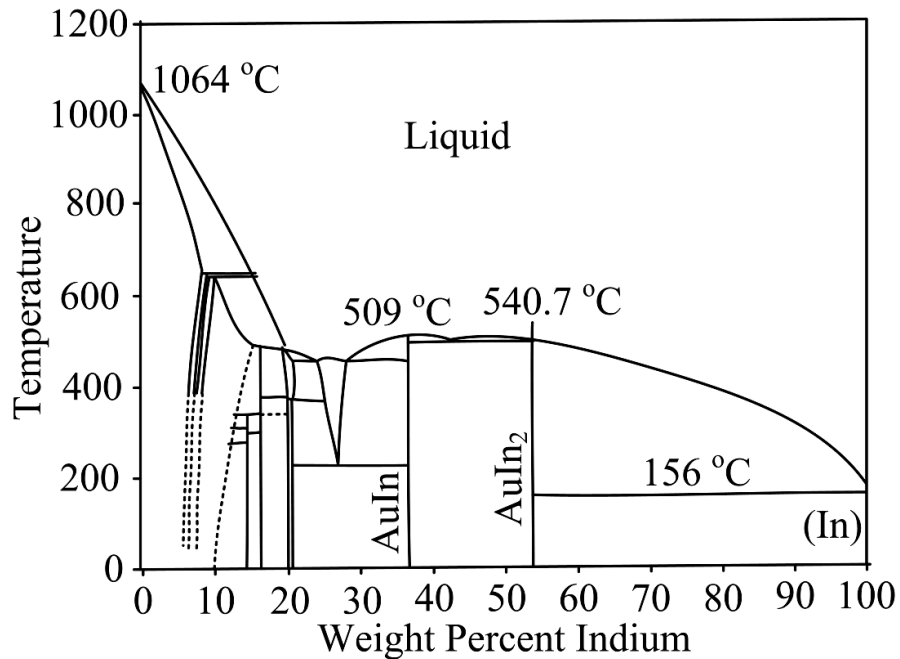
Figure 3.21 Au-In binary phase diagram.

A graph of the ratio of the parent metal thickness to the interlayer thickness necessary to produce a final cross-section of a certain weight percentage interlayer is shown in Figure 3.22. The plot was calculated using Equation (3.20):

$$\frac{h_{PM}}{h_{IL}} = \frac{\rho_{IL}}{\rho_{PM}}\left(\frac{1}{wt\%}-1\right)$$

(3.20)

Where h_{PM} and h_{IL} are parent metal and interlayer thicknesses, ρ_{PM} and ρ_{IL} are the

parent metal and interlayer densities, and *wt%* is the weight percent of the interlayer in the final joint.
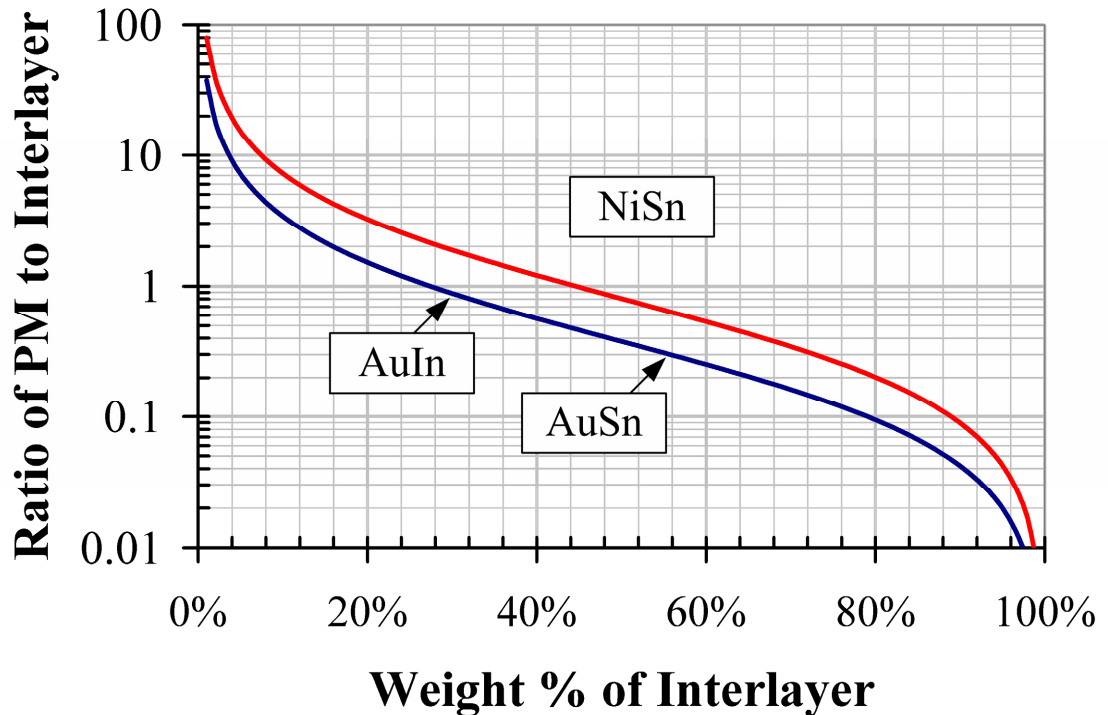
Figure 3.22 Plot of the ratio of parent metal thickness to interlayer thickness required to produce a final microstructure that contains a certain weight percentage of interlayer.

The densities of indium and tin are both 7.31 g·cm^{-3} so the curve for both material families is the same. To use the plot, search for the wt% of the interlayer for the target composition then find the ratio of parent metal to interlayer that will produce that composition. For example, for a solid solution of indium dispersed in a gold parent metal the wt% of indium should be less than 5% which corresponds to a ratio of approximately 7 on the plot of gold thickness to indium thickness. For an indium interlayer thickness of 1 μm, the total gold thickness in the joint should be 7 μm bringing the total joint thickness to 8 μm.

Reducing the total bond joint thickness

Some MEMS bonding applications require a thin bond joint. Applications like low-profile packaging, or bonds that are used to join material layers that are already thin themselves, such as thin layers of piezoelectric materials, require very thin bond joints. If the total bond joint thickness calculated in this section needs to be thinner for this application, there are several options. The option with the biggest impact will be increasing the heating rate of the bonding technique. A higher heat rate will reduce the thickness of the IMC layer at the end of Stage 1, and therefore reduce the amount of interlayer required. Another way to reduce the total bond joint thickness would be to increase the ratio of interlayer left in the final microstructure. If a higher concentration of interlayer is tolerable (meaning that more of the joint contains intermetallic compounds) in the bond joint, the parent metal thickness can be reduced, making the overall bond joint much thinner. Lastly, if the two techniques above still result in a bond joint that is too thick, another material family such as Ni-Sn TLP solder should be considered. The Ni-Sn IMC formation rate in the solid state is very small compared to other material systems. Therefore the Ni-Sn IMC layer thickness at the end of Stage 1 will be much thinner than other material systems for the same heating rates.

CHOOSE THE DEPOSITION TECHNIQUE

The deposition technique for the interlayer is an important part of the design process. The two most common ways of depositing the metals used in MEMS processing is physical vapor deposition and electroplating. The parent metal thickness is typically around 5 μm, which makes electroplating a better choice since it is difficult to use PVD to create parent metals layers thicker than 1 μm or even 0.2 μm for high stress materials, like nickel. Ironically, electroplating also produces higher quality interlayers than PVD. Tin and indium are very difficult to deposit with PVD because the morphology of the films during deposition leads to very rough surfaces (~ 1 μm RMS roughness). Cooling the substrate to -40 °C during deposition can create higher-quality films [65], but this requires specialized equipment. Therefore, electroplating is the deposition technique of choice for material systems that use a tin interlayer. Indium is not as simple, however. Electroplating indium will create a higher-quality film, but as discussed in Section 2.2.1,

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indium oxide is much more stable than tin oxide and therefore prevention measures must be taken to prevent its formation. The simplest way is to deposit a thin layer of gold over oxide-free indium. This is easy to do if the indium was deposited with PVD, because the gold can be deposited on top of the indium without breaking the vacuum of the system. With electroplating, however, the wafer must be removed from the electroplating bath and moved to a PVD system without allowing the oxide to form. Choosing the proper deposition technique for indium must weigh the merits of the high film quality possible with electroplating compared to the simple processing afforded by PVD.

FLUXLESS DESIGN RULES

A MEMS bonding process must be fluxless. To create a fluxless process, the native oxides that form on the metals used in the bond joint must be managed. If gold is used as the parent metal, this is easy since gold does not form a native oxide. Other metals, like indium, nickel, and tin require some process design.

Indium oxide is very stubborn so its growth must be prevented during processing. This can be performed by depositing a thin layer of gold on top of the indium layer in-situ. Tin oxide is not as rigid as indium oxide so it does not require a thin layer of gold to prevent its formation. Tin oxide can be handled by applying sufficient force during the bonding process to fracture the tin oxide. The nickel oxide cannot be handled in a similar manner because the nickel underneath the oxide is never molten as the tin is. With a rigid support underneath, the oxide is difficult to fracture without damaging the underlying metal. Therefore, nickel oxide must also be prevented. This can be accomplished by covering it with a layer of gold or another metal, such as tin, to prevent nickel oxide growth. Since the tin oxide can be handled by applying sufficient force during the bonding sequence, as long as all the nickel surfaces are covered with a layer of tin the nickel oxide will be prevented by the tin layer.

Chapter 4

WAFER-LEVEL VACUUM PACKAGING WITH SOLDER BONDING

A vacuum is an enclosed space filled with gas at pressures that are less than atmospheric pressure [80]. The pressure region of interest for typical MEMS vacuum packaging spans the range of 100 mTorr to < 1 mTorr.

This chapter covers the use of the wafer bonding techniques presented in Chapters 2 and 3 as methods to create wafer-level vacuum packaging. The motivations for vacuum packaging, which include increased thermal isolation, reduced squeeze film damping, and a rarefied atmosphere, are briefly reviewed in Section 4.1. Section 4.2 presents the major leaks that must be designed for with a MEMS vacuum package as well a way of pumping out gasses to reduce the pressure. Section 4.3 presents and discusses previous vacuum packaging approaches. Many different types of wafer bonding have been used to create MEMS vacuum packages, but they all require temperatures above 350 °C to do so. Section 4.4 presents data on all of the packaging experiments, including the vacuum measurement technique, long-term data on, and low-temperature titanium getter activation results (A summary of the data is provided in Table 4.1). The Au-In TLP solder technique is a vacuum packaging approach that has obtained pressures as low as 20 mTorr without exceeding 200 °C.

Table 4.1 Summary of the wafer bonding MEMS vacuum package data.

Bonding Technique	Temp./Time	Pirani Gauge	Pressures	Leak Rate	Notes
Au-Sn Solder	300 °C/20 mins.	Poly.	0.6-0.2 Torr	$1.5 \cdot 10^{-15}$ atm$\cdot$cc$\cdot$s^{-1}	Shortest bond cycle
Ni-Sn TLP Solder	300 °C/1 hour	Poly.	30-1 Torr	$1.7 \cdot 10^{-15}$ atm$\cdot$cc$\cdot$s^{-1}	Cheapest materials
Au-In TLP Solder	200 °C/1 hour	Poly.	10-.2 Torr	$1 \cdot 10^{-16}$ atm$\cdot$cc$\cdot$s^{-1}	Lowest temperature
Au-In TLP Solder	200 °C/25 hours	Platinum	0.5-0.02 Torr	-	24 hours at vacuum before bond cycle

4.1 Motivation

There are several reasons for vacuum packaging MEMS devices. The next sections describe major motivations for MEMS vacuum packaging and provide basic analysis of the physics behind these motivations.

4.1.1 Thermal Isolation

Some MEMS devices precisely measure temperature from infrared radiation or need to be heated to accelerate a chemical analysis. To achieve high temperature sensitivities or keep their power consumption small, these devices need to be thermally insulated from the ambient temperature. This is easily accomplished at macroscopic distances because air is an excellent thermal insulator at this scale. At MEMS dimensions, however, the thermal conductivity of air at atmospheric pressures conducts large amounts of heat. This conduction can be reduced by lowering the pressure of the air surrounding the device. Exactly the magnitude of the required reduction in pressure is dependant on many factors, including the device dimensions, the desired thermal insulation, and the types of gas inside the package. The following analysis provides a brief summary of the theory that determines the pressure levels required to achieve sufficient thermal isolation for typical MEMS dimensions. A more rigorous treatment of the equations and theory governing the thermal conductance of gas versus pressures has been extensively covered in the literature [81].

Heat is lost from a MEMS structure via three methods (see Figure 4.1): solid conduction through the supports attaching it to the substrate (G_{solid}), conduction through the gas (G_{gas}) surrounding the device, and radiation ($G_{radiation}$).
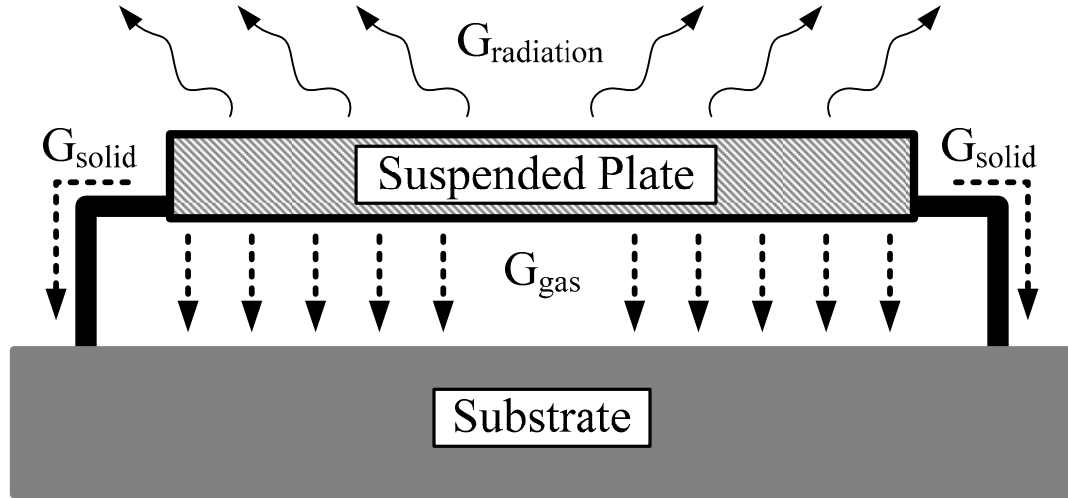
Figure 4.1 Illustration of the thermal losses from a heated plate suspended over a substrate.

Equation (4.1) shows the total thermal conduction G_{total} is equal to the sum of these three loss mechanisms:

$$G_{total} = G_{radiation} + G_{solid} + G_{gas} \tag{4.1}$$

If we assume that the temperature of the device remains close to room temperature, the heat lost by radiation can be neglected. The heat conducted through the solid supports is determined by the geometry of those supports and the materials they are made out of, which do not change with pressure, therefore the heat lost through solid conduction represents a the maximum thermal isolation of the structure. The thermal conductivity of a gas is more complex.

The thermal conductivity of a gas is given by:

$$\kappa = \frac{1}{3} m \, \lambda \, \eta \, \upsilon_{ave} \, c_v \tag{4.2}$$

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Where: κ is the thermal conductivity, m is the molecular mass, λ is the mean free path, η is the molecular density, v_{ave} is the molecular velocity, and c_v is the specific heat of the gas [82]. It is interesting to note that the thermal conductivity of the gas, as a material property, is independent of pressure. As the pressure decreases, the mean free path, λ, increases inversely proportional to pressure. At the same time, the molecular density, η, decreases with pressure. The effects of these two dependencies cancel, thus removing any pressure dependence from the thermal conductivity equation.

However, equation (4.1) no longer applies when you consider the gas as part of a system. This is because the system constrains the gas into a space of limited distance. Inside this space, the maximum mean free path of the gas is restricted by the dimensions of the system. As the mean free path approaches those dimensions, any further decrease in pressure cannot increase the mean free path. Since the molecular density still drops with pressure while the mean free path stays constant, the thermal conductivity of the gas becomes proportional to the drop in pressure.

The thermal conductivity for a gas enclosed between two plates can be approximated by Equation (4.3)[83]:

$$\kappa_{air} = \kappa_{air,0} \frac{1}{1 + \dfrac{7.6 \cdot 10^{-5}}{P \times d / T}} \tag{4.3}$$

Where $\kappa_{air,0}$ is the thermal conductivity of air at room temperature and pressure (0.0284 W/mK)), P is the pressure in Torr, T is the average temperature of the two plates in Kelvin, and d is the distance between the plates in meters. In this equation, the distance, d, is the critical dimension that reduces gaseous thermal conductance by constraining the mean free path as the pressure drops.
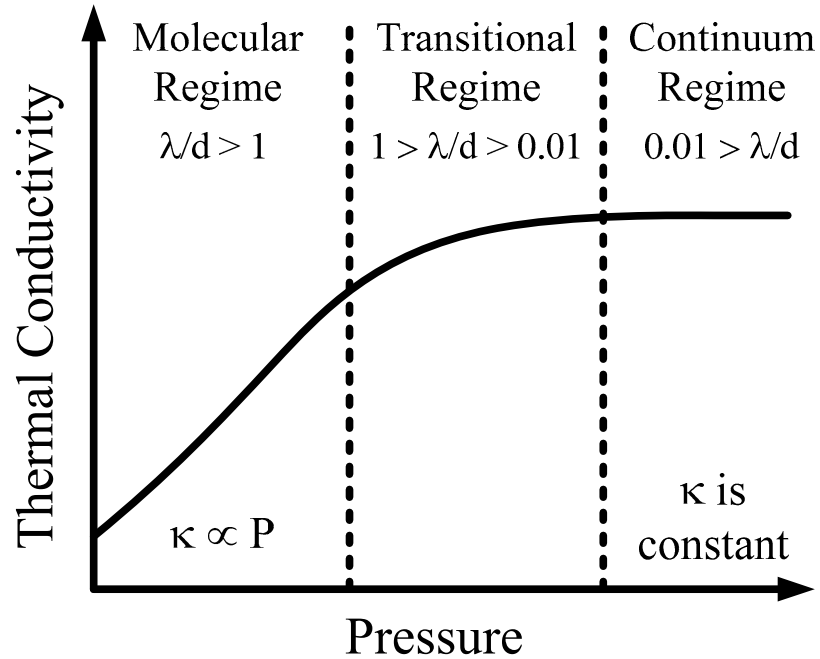
Figure 4.2 Illustration of the pressure dependence of gaseous thermal conductivity.

Figure 4.2 illustrates the three regimes of gaseous conduction, highlighting their dependence on the ratio of the mean free path of the gas to the critical dimension of the system. In the continuum regime, the mean free path is much smaller than the critical dimension and is therefore able to become larger as the pressure drops and cancel out the drop in molecular density. In the transitional regime, the mean free path is approaching the critical dimension and does not completely cancel out the drop in molecular density so there is a slight dependence on pressure. In the molecular regime, the mean free path is completely constrained by the critical dimension so the thermal conductivity is proportional to the pressure because the mean free path does not cancel the reduction in molecular density.

Combining the pressure dependence of gaseous thermal conductivity with the solid thermal conduction losses, the total thermal losses vs. pressure are plotted in Figure 4.3.
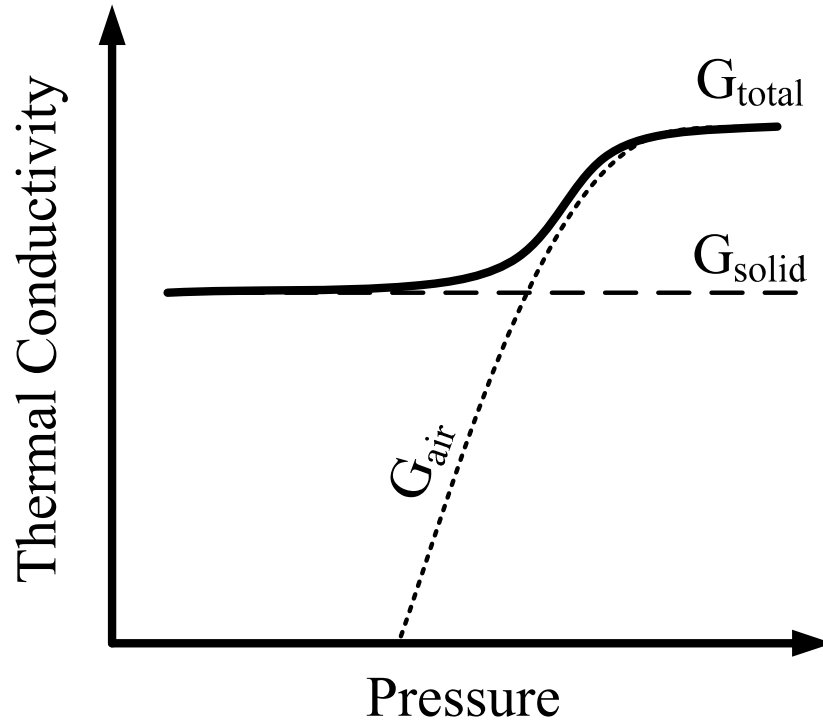
Figure 4.3 Illustration of the total, gas, and air thermal conductivities versus pressure.

At higher pressures, the conductance of heat through the gas dominates the total heat loss from the system. Reducing the pressure reduces the thermal conductivity of the gas as it enters the molecular range and therefore the total thermal losses also drop. As the pressure continues to drop, the thermal conductance from the gas continues to drop until is becomes less than the thermal losses from solid conduction down the supports. At this point, further pressure reduction does not decrease the thermal losses from the system because losses down the solid supports dominate.

Several conclusions can be drawn from these rough calculations that are useful when designing a system that require vacuum packaging for thermal isolation:

1. The minimum possible thermal losses for the system are determined by conduction down the solid supports (and radiation at extreme thermal isolations).

2. At or near atmospheric pressure, gaseous conduction of heat across small gaps is too large to be ignored in MEMS systems.

3. The vacuum level required to achieve optimal thermal isolation depends on the thermal losses through solid conduction. The lower the loss of heat through solid conduction, the lower the vacuum level that is required to reach the point where solid conduction dominates.

Uncooled thermal bolometers are a good example of a MEMS device that benefits from vacuum packaging. Uncooled bolometers can create an image that displays very small changes in measured ambient temperature, but they require vacuum packaging to operate [84]. The bolometers sense the changes in temperature by adsorbing infrared photons and measuring the thermal energy of each photon. This is only possible by having a very well isolated thermal platform. The larger the thermal isolation, the larger temperature difference each incident photo will create on the platform as it is adsorbed. Without a vacuum environment, the temperature increase would be conducted away from the platform by the gas molecules before the temperature increase is registered.

4.1.2 Reducing Viscous Fluid Losses

Reducing viscous fluid losses is another reason for vacuum packaging MEMS devices. Many MEMS devices use a resonating structure for various sensing and actuating applications. Resonant structures have been used to sense pressure, fluid viscosity, inertial movement, and many other physical phenomena [8]. They can also be used as frequency references, filters, and other signal processing functions that are widely used in radio frequency communications and timing applications [85]. All of these applications require a quality factor that is as high as possible to maximize device performance, whether it be the angular rate sensitivity of a gyroscope or the phase noise of a frequency reference.

The quality factor is defined by:

$$Q = 2\pi \frac{Energy\ Stored\ per\ Cycle}{Energy\ Lost\ per\ Cycle} \qquad (4.4)$$

To maximize the Q, the resonator design should maximize the energy stored per cycle, while minimizing the energy lost. The energy stored per cycle depends largely on factors that are dictated by other aspects of the design, such as the resonant frequency and spring stiffness, which may not leave much design latitude to increase the energy stored per cycle without considerably deviating from the original device design. However, one of the major loss mechanisms, viscous fluid damping, is largely dependent on the pressure of the gas surrounding the resonator, making vacuum packaging an important factor to consider when designing high-Q resonant structures. The next paragraphs cover the basics of viscous fluid damping in resonators and how vacuum packaging can minimize the losses.

The two major types of viscous fluid damping mechanisms illustrated in Figure 4.4. Squeeze film damping occurs when a plate moves perpendicular to a stationary surface. The gas trapped inside the gap is compressed and begins to squeeze out the sides of the gap to equalize the increase in pressure. The work performed by the plate to move the gas out of the gap is lost energy. Squeeze film damping is the major source of energy loss for resonant MEMS [86]. Slide film damping occurs as a plate moves parallel across a surface. There is not a pressure change in this gap as there was with squeeze film damping. However, there is a velocity gradient across the gap since the gas closest to the moving plate moves with the same velocity as the plate, while the gas near the substrate is stationary. The energy loss mechanism for slide film damping is from viscose shear motion near the surface [87]. Slide film damping causes much less energy loss compared with squeeze film damping [86].
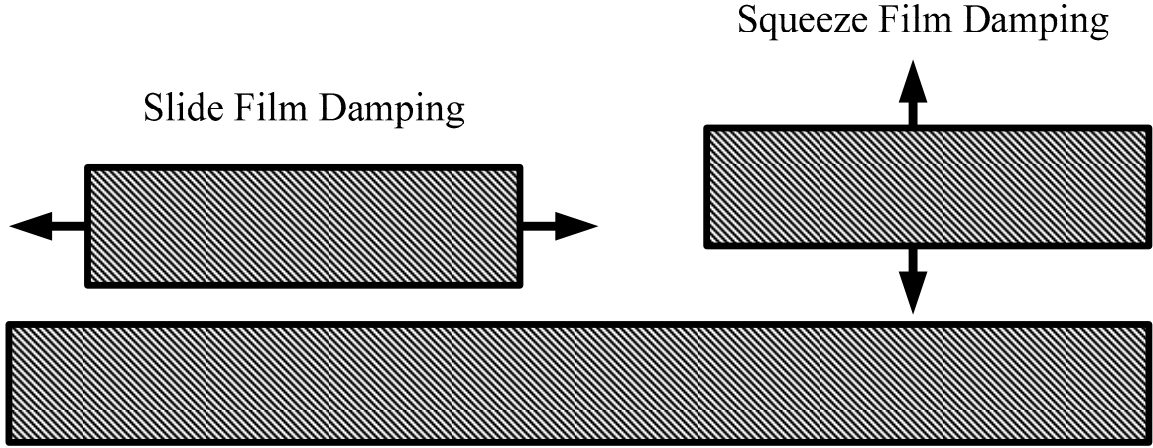
Figure 4.4 Illustration of the two types of viscous fluid damping.

The energy losses due to viscous fluid damping are too complex to calculate for any practical MEMS structure. There are many research efforts focused on developing techniques for simulating both types of film damping on MEMS resonator Q's and how they vary with pressure level [86]. Despite the fact that numerical methods are required for complete understanding of the interaction, equations that only approximate the losses are still useful for a general intuition of viscous damping and how it relates to important design parameters as well as the pressure.

Slide film damping of a plate moving parallel to the surface of a stationary plate can be modeled by Equation (4.5) [88]:

$$\xi = \frac{\eta \, A_P}{d} \left(\frac{1}{1 + 2 \, K_n} \right) \tag{4.5}$$

Where ξ is the damping factor, η is the gas viscosity, d is the gap between the plates, and K_n is the Knudsen number defined in Equation (4.6) as the ratio of the mean free path of the gas, λ, divided by the gap between the plates, d.

$$K_n = \frac{\lambda}{d} \tag{4.6}$$

Equation (4.5) is valid for sliding plates that are moving so slowly that the gas velocity gradient across the gap is linear and it is a Couette flow; other references cover more

complicated flow cases [89]. Upon first inspection of Equation (4.5), it isn't apparent how the pressure level surrounding the plate affects the slide film damping coefficient. However, recall that the Knudsen number is the ratio of the mean free path of the gas over the gap between the plates. As the pressure surrounding the moving plate is lowered, the mean free path increases, thus the Knudsen number increases and the overall damping coefficient is minimized.

Squeeze film damping is slightly more complicated than slide film damping because it does not always act as just a damper. Depending on the size of the gap, the resonant frequency of the system, and the pressure of the gas in the gap, a squeezed film can act as a damper for the system or as a spring. Equation (4.7)

shows the calculation of a squeeze number, which determines if the squeezed film should be modeled as a spring or a damping component in the system.

$$\sigma = \frac{12 \, \eta \, A_S \, \omega}{P \, d^2} \tag{4.7}$$

Where σ is the squeeze number, η is the gas viscosity, d is the gap between and A_s is the area of the plates, P is the pressure, and ω is the resonant frequency.

The reason squeeze film damping can act as a damper or a spring lies on the physical explanation of the gas movement as it is getting squeezed. If the movement of the gap is slow enough such that the gaseous molecules can escape from between the gap, the squeezed film is acting as a damper. On the other hand, if the gap is changing too quickly for the gas to escape, the squeezed film acts as a spring. This spring/damper duality is captured in the squeeze number equation. For low squeeze numbers, implying one to all of the following: a small plate, low resonant frequency, low pressure, or a large gap between the plates, the gas is able to flow freely between the plates during the resonant cycle. Work is required to move the gas from in between the plates, thus energy is lost from the system and the squeezed film acts as a damper. If the squeeze number is less than 10, then the squeezed film is acting a damper for the system and should be modeled with equation (4.8).

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$$\xi = 0.035 \frac{P A_S \sigma}{\omega d} \tag{4.8}$$

For high squeeze numbers, which implies one to all of the following: large plate area, high resonant frequency, high pressure, or a small gap, the gas is not able to flow from within the gap during a resonant cycle [90]. Instead of flowing from in between the plates, the gas is compressed by the moving plate. The compression of the gas stores energy from the moving plate, which it returns to the system as it decompresses when the plate moves away from the surface. Since no energy is lost, only stored, the squeeze film acts as another spring in the system. If the squeeze number is much greater than 10, then the squeezed film is acting as an extra spring for the system and will affect the resonant frequency as shown in Equation (4.9).

$$\omega = \sqrt{\frac{1}{m}\left(k_{si} + \frac{C P A_S}{d} \right)} \tag{4.9}$$

Reducing the pressure has many positive effects on the outcome of squeeze film damping on Q reduction. First, reducing the pressure increases the squeeze film number. The higher the squeeze film number, the more the squeezed film is acting as a spring instead of a damper and the less energy it removes from the system per cycle. Second, reducing the pressure reduces the magnitude of the squeeze film damping coefficient because the coefficient is proportional to the pressure level. Third, the reduction in pressure reduces the effect of the squeezed film has as a spring in the system as well.

The resonant frequency of the resonators plays a role in determining the vacuum level required to reduce squeeze film damping to levels that produce an acceptable Q. It can be read in the literature that devices with lower resonant frequencies, in the kHz range, require higher vacuum levels than other resonators with higher resonant frequencies to achieve high Q's. Resonators in the GHz range have reported high Q's at atmospheric pressure. The reason for this can be seen in the equation (4.7)

The squeeze film number is proportional to the resonant frequency, so that high frequency resonators (even though they have much smaller gaps) will have orders of

magnitude higher squeeze film numbers compared to other lower frequency resonators. This means that squeezed films for high frequency resonators cannot flow in and out of the gap during one resonant cycle, thus no energy is lost to squeeze film damping and the Q remains high even in atmospheric pressures.

Vacuum packaging is important for resonant devices that need high Q's for optimal performance. Viscous fluid damping in the form of squeeze film and slide film damping can rob resonators of energy every cycle and lower the Q. Creating a vacuum environment lessens the magnitude of squeeze film and slide film damping as well as shifting the squeezed film effect from a damping loss effect to a spring stiffening effect, which lowers its negative effect on the Q resonator. Vacuum packaging is much more critical for resonators with lower resonant frequencies, as the squeezed film effect acts more as damper for slower moving plates. [80].

4.1.3 Other Motivations for Vacuum Packaging

Aside from thermal isolation and reducing viscous fluid damping, vacuum packaging is also used to create a rarefied atmosphere for electron emitting devices and as a Brownian noise reduction technique for low-noise sensors.

Some of the first vacuum packaged devices were vacuum tubes. Vacuum tubes use thermionic emission to create a stream of electrons that can be controlled by varying electric fields to amplify, switch, and otherwise control electric signals [91]. It is important for these tubes to operate in vacuums because the electrons must travel unimpeded between the anode and cathode for optimal operation. If the pressure is too high, the electrons would run into, and ionize, the gas molecules present, ruining the operation of the tube. Vacuum packaging and its corresponding long mean free path is needed for all devices that rely on unimpeded electron flow in free space for their operation. Vacuum tubes, while once the workhorse of electronics, have been supplanted by transistors and are only used in niche applications, such as audiophile stereo equipment [91]. However, there are other MEMS electron emitting devices, such as field-emitters, that require vacuum packaging [92].

Another benefit of a vacuum environment with MEMS applications is lowered Brownian noise. The random movement of particles is known as Brownian motion [93]. The Brownian motion of gas particles surrounding very sensitive physical sensors will cause an increase in the noise floor of the sensor. The gas particles randomly strike the sensor and transfer some of their momentum causing an unwanted signal output. By reducing the pressure surrounding the sensor with vacuum packaging, the number of gas particles surrounding the sensor drops and there is a corresponding decrease in the noise level contributed by the Brownian motion of the particles. Very low noise accelerometers and high precision MEMS tunable lasers can benefit from vacuum packaging by the reduction in Brownian noise levels seen from removing most of the gaseous molecules from the package [94].

4.2 Creating Vacuum inside a MEMS Package

Vacuum packaging is the package of choice for many MEMS devices based on all the advantages discussed in the previous section. However, despite its widespread need and corresponding engineering efforts, it is still challenging to create vacuum packaged MEMS devices. The next sections cover two important aspects of creating a vacuum package on the micro-scale: leaks and pumps.

4.2.1 Leaks

A leak in the traditional sense of the word means gas flowing from a high pressure region to a low pressure region through an opening. In MEMS packaging, there are many other sources of gas that can raise the pressure without flowing through an open orifice that are classified as virtual leaks. They are not leaks in the traditional understanding of the word, but they are just as effective at ruining a vacuum package. The main sources of leaks, real and virtual, are illustrated in Figure 4.5.
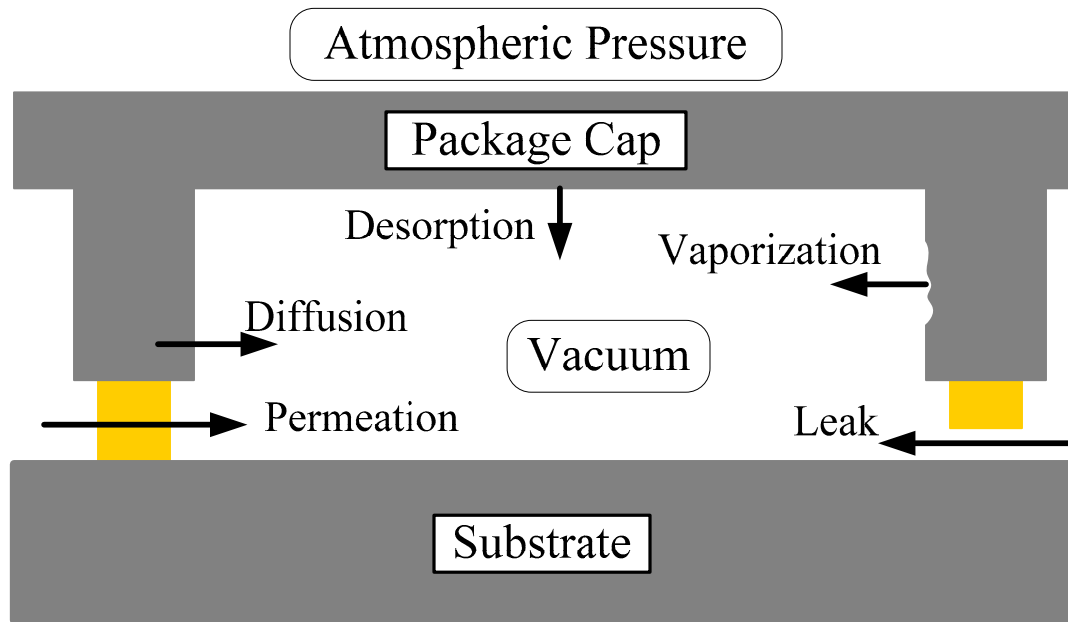
Figure 4.5 Sources of gas inside a vacuum-sealed microcavity.

VAPORIZATION

Vaporization is the thermally stimulated movement of molecules from the solid or liquid phase into the vapor phase. The molecules will only enter the vapor phase if the pressure is below the vapor pressure for that material at its temperature. The vapor pressure curves for different metals are given in Figure 4.6. Vaporization is not a concern for most MEMS packaging materials. Almost all metals have very low vapor pressures at the service temperatures of MEMS packages. Some other materials, such as glasses and polymers may have vapor pressures that are high enough at the package service temperature to cause problems with the vacuum level inside the package.
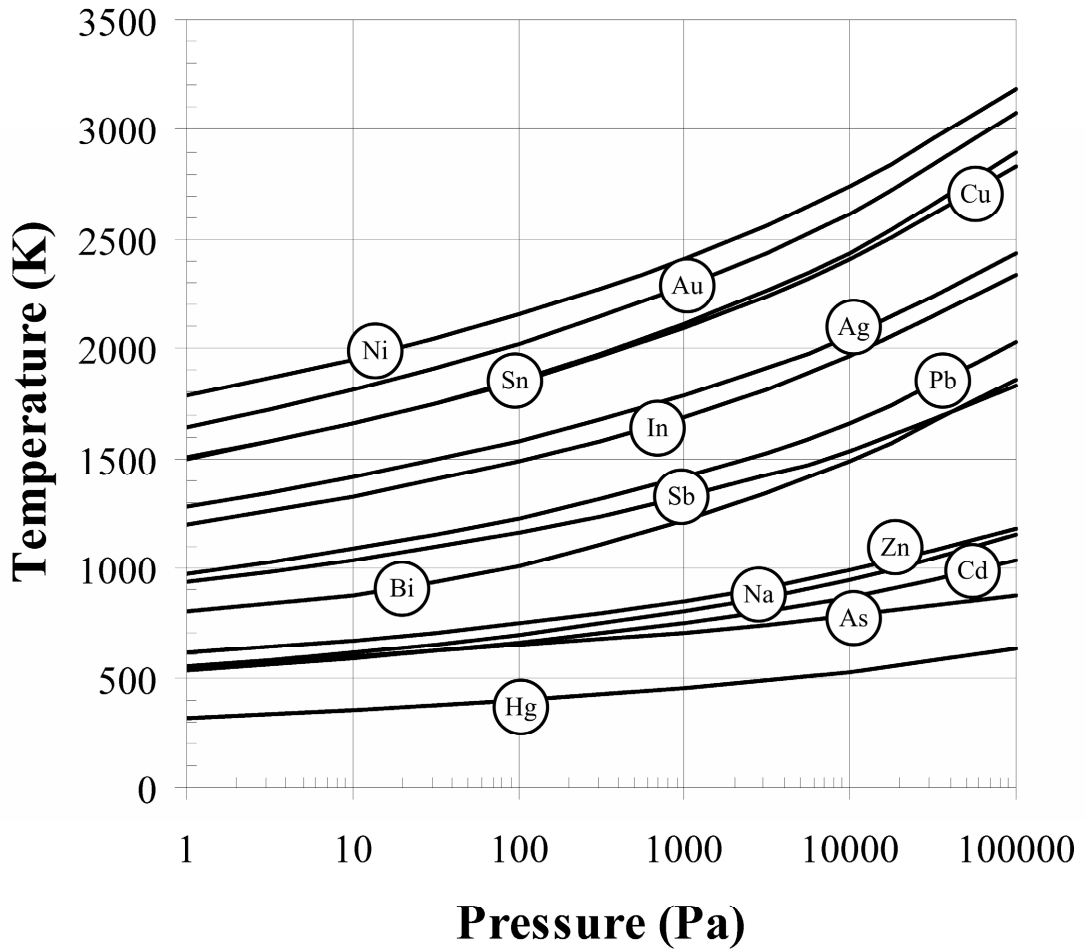
Figure 4.6 Vapor pressures for several metals that might be used in MEMS packaging. The most common metals must be heated very hot (> 1000 K) for their vapor pressures to reach 1 Pa (7.5 mTorr) [81].

REAL LEAKS

Real leaks are a much larger concern for MEMS vacuum packaging, because even the smallest real leak can rapidly ruin a vacuum package. The leak rate for several different orifice sizes is given in Table 4.2.

Table 4.2 Real leak rates for different sized leak paths (Adapted from [95]).

Leak Rate (torr.Liter.second^{-1})	Equivalent Opening
10^{-3}	Rectangular slit with 1 cm width, 0.1 mm height and 1 cm depth
10^{-4}	Rectangular slit with 1 cm width, 30 μm height and 1 cm depth
10^{-5}	Capillary 1 cm long and 7 μm in diameter
10^{-6}	Capillary 1 cm long and 4 μm in diameter
10^{-7}	Capillary 1 cm long and 1.8 μm in diameter
10^{-8}	Capillary 1 cm long and 0.8 μm in diameter
10^{-9}	Capillary 1 cm long and 0.4 μm in diameter
10^{-10}	Capillary 1 cm long and 0.2 μm in diameter

To approximate the pressure rise from these real leaks, we first start with:

$$\frac{dp}{dt} = \frac{Q}{V} \qquad (4.10)$$

Where dp/dt is the pressure rise, Q is the leak rate, and V the package volume. Integrating both sides with respect to time and solving for the pressure yields:

$$P = \frac{Q}{V} t \qquad (4.11)$$

Equation (4.11) is valid as long as the leak rate Q is constant with pressure, which is valid for small internal package pressures (< 100 Torr) because the conductance through the leak path is approximately constant for those pressures.

If we consider a typical MEMS package cavity with dimensions: 5 mm wide by 5 mm long and 200 μm high (a volume of 2.5 μL), the pressure rise versus time from equation (4.11) due to these leak rates is plotted in Figure 4.7.
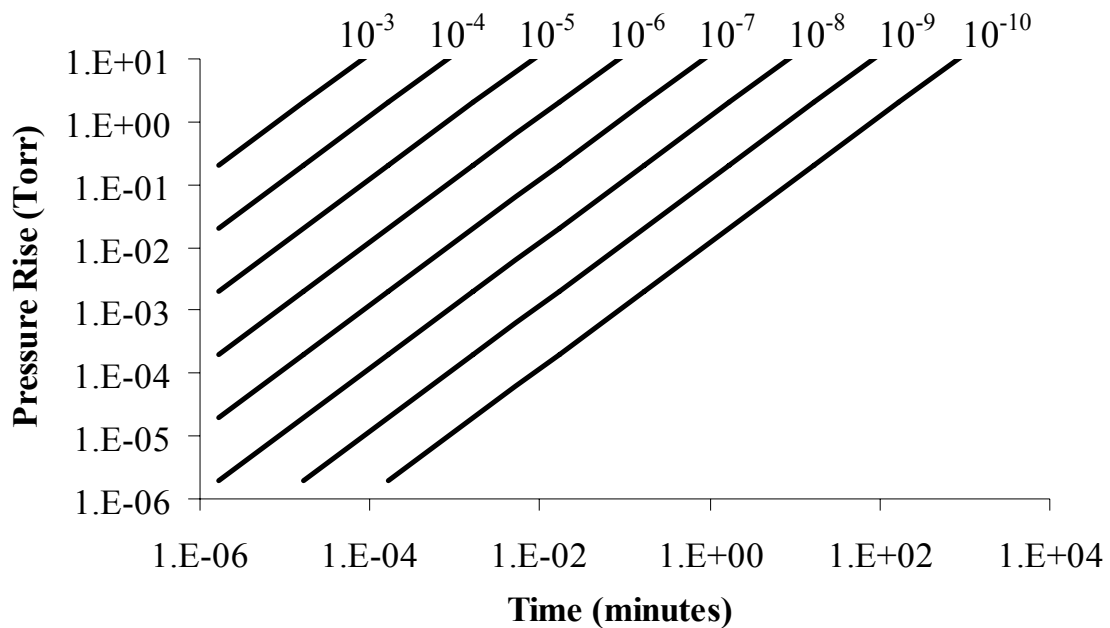
Figure 4.7 Approximate pressure rise for a MEMS package with a volume of 2.5 μL for various leak rates labeled in torr·liter/sec [95].

For the smallest leak rates, $1*10^{-10}$ Torr·Liter/Second, the pressure inside a MEMS package will rise over 1 mTorr/minute. The leak rate of $1*10^{-10}$ Torr.Liter/Second corresponds to a capillary twice as long as the package is wide and only 200 nm in diameter. This pressure rise is unacceptable for even the minimum MEMS vacuum packaging specifications. If the package started at 1 mTorr, it would rise to 17 Torr by the end of the first day. The reason for this large pressure rise is that MEMS packages have small volumes, such that even small fractions of a mole of gas will move the pressure well out of the mTorr vacuum range. The effect of real leak rates on the pressure level could be mitigated by increasing the package volume, but this solution directly counteracts one of the biggest advantages of MEMS, their small size.

PERMEATION

Permeation is a virtual leak that will also ruin a MEMS vacuum package if not accounted for in the design. Permeation occurs when a gas molecule adsorbs on the outside of a wall of the package, diffuses through the width of that wall, then desorbs on the inside of the package. Figure 1.9 shows the relative permeability of several classes of

materials that have been used in previous vacuum packages.

Similar to a real leak, scaling the package size down to MEMS volumes limits the materials that can be used in a MEMS vacuum package to those with small permeability. This is evident by a simple inspection of how permeability scales with volume. The leak due to permeation through the cavity walls is given by [81]:

$$Q_{PERM} = P \cdot \frac{A}{d} \cdot (p_1 - p_2) \qquad (4.12)$$

Where P is a constant depending on the material and gas, A is the cross-sectional area, d is the thickness of the wall, and $p_1 - p_2$ is the differential pressure across the wall. Removing the constants, we can simplify to:

$$Q_{PERM} \propto \frac{A}{d} \qquad (4.13)$$

The differential pressure increase in a cavity due to leaking is given by:

$$dp/dt = Q_{PERM}/V \qquad (4.14)$$

Substituting the permeation leak rate proportionality:

$$dp/dt \propto \frac{A}{d \cdot V} \qquad (4.15)$$

Substituting the unit dimensions and simplifying yields:

$$dp/dt \propto \frac{1}{m^2} \qquad (4.16)$$

Equation (4.16) shows that as the dimensions of the package get smaller, the leak rate due to permeation increases as the inverse square. This explains why light bulbs and vacuum tubes can use a thin shell of glass as a barrier between the atmosphere and their vacuum environment, whereas a MEMS package must use different materials or a much thicker layer of glass.

Jourdain, et. Al reported on the hermetic capabilities of a polymer, Benzocyclobutene (BCB) [72] used as a wafer bonding technique to create wafer-capped packages. The permeability of the polymer was so high that all of the helium used in MIL spec fine leak test had escaped the package before the package could be transferred from the bomb chamber to the vacuum chamber. The small size of MEMS packages and their sealing layers limits the materials that can be used for vacuum packages to metal films, single crystal materials, and thick layers (100's μm) of glass.

This is evident by looking at the permeability of hydrogen and helium through these materials. Hydrogen and helium have the high permeability in common packaging materials because of their small size and solubility. The partial pressures of helium and hydrogen in the atmosphere are 4 mTorr and 0.4 mTorr respectively. An estimate of the leak rate can be calculated using hydrogen permeation through a nickel bond ring that is 10 μm tall, 4800 μm in perimeter, and 300 μm wide. The leak rate can be calculated from Equation 4.17:

$$q_{perm} = \frac{K_p\left(P_2^{1/2} - P_1^{1/2}\right)}{d} \tag{4.17}$$

Where q_{perm} is the leak rate due to permeation, K_p is a parameter dependent on the material and the gas, P_2 is the pressure outside the package, P_1 is the partial pressure inside the package, and d is the distance of permeation. For hydrogen through nickel, K_p is $2 \cdot 10^{-10}$ m^2.Pa$^{1/2}$.s^{-1} [80]. Substituting the bond ring dimensions along with this value gives:

$$q_{perm} = \frac{2 \cdot 10^{-10} \frac{\text{m}^2 \text{Pa}^{1/2}}{\text{s}}\left((0.05\,\text{Pa})^{1/2} - 0\right)}{300\,\mu\text{m}} = 1.49 \cdot 10^{-7} \frac{\text{m}^3 \text{Pa}}{\text{s} \cdot \text{m}^2} \tag{4.18}$$

To calculate the maximum pressure rise over time, the leak rate must be multiplied by the bond ring cross sectional area and divided by the package volume:

$$\Delta P = q_{perm} \frac{\text{Area}}{\text{Volume}} = 1.49 \cdot 10^{-7} \frac{\text{m}^3 \text{Pa}}{\text{s} \cdot \text{m}^2} \cdot \frac{4 \cdot 10 \text{um} \cdot 1200 \text{um}}{5 \cdot 10^{-10} \text{m}^3} = 0.10 \frac{\mu \text{Torr}}{\text{s}} \quad (4.19)$$

This is the pressure rise over time for a 0.5 μL package with no hydrogen inside. As the pressure of hydrogen inside the package increases, the permeation leak rate will go down. Therefore, the calculation above is the worst case leak rate. Despite the worst case scenario, this calculation indicates that for reasonable deployment times of several years, any package sealed with these dimensions and materials would see a pressure rise due to the permeation of hydrogen that would be very near the partial pressure of hydrogen in the atmosphere.

The small volumes of MEMS packages combined with the permeability of hydrogen through metals and helium through glasses makes the partial pressures of these gasses the theoretical minimum pressure attainable with each sealing material. Therefore for a metal sealed package, the theoretical limit for minimum package pressure is 0.4 mTorr and for a glass sealed package the theoretical limit is 4 mTorr [80].

DIFFUSION AND DESORPTION

Leaks due to diffusion and desorption are the most difficult to mitigate because even good hermetic materials like glass and metal will contribute virtual leaks. Moreover, the magnitude of diffusion and desorption leaks is proportional to the surface area of the inside of the package [80]. Therefore, as the size of the package shrinks, this leak type has a larger negative impact on the package pressure.

In 1962, Benajmin B. Dayton published the paper "Outgassing Rate of Contaminated Metal Surfaces", which first identified the major source of diffusion and desorption leaks, or outgassing, in vacuum systems [96]. H_2O is the major contaminant that contributes to outgassing in vacuum systems. Water molecules get adsorbed on the surface and in the bulk of the native oxides of metals, and then later diffuse to the surface and desorb into the package cavity. The total amount of water contained on the surface and in pores of the metal oxide amounts to an equivalent of 100 monolayers of H_2O molecules. As the pressure at this surface drops, the physically adsorbed water breaks free from the metal

surface and enters the vapor phase. As long as there is a pump to remove the new water vapor, the pressure will remain constant or keep dropping depending on the pumping speed. After the physically adsorbed water has entered the vapor phase, the chemisorbed water dissolved in the oxide diffuses to the surface and then into the vapor phase. Over time, the outgassing rate from the water vapor drops as the water molecules are removed. The sum of all these outgassing sources leads to an outgassing rate, which for metals can be modeled by Equation (4.20):

$$K_n = \frac{K_I}{t_h^\alpha} \tag{4.20}$$

K_n is the outgassing rate in torr.liters.second^{-1}.cm^{-2}, K_I is a constant fit to experimental data (approximately 10^{-7} Torr.liter. second^{-1}.cm^{-2}), α is another experimental constant that is between 0.7 to 2 and normally close to 1, t_h is the time after pump down in hours. Figure 4.8 plots the outgassing rate versus time for typical metals.
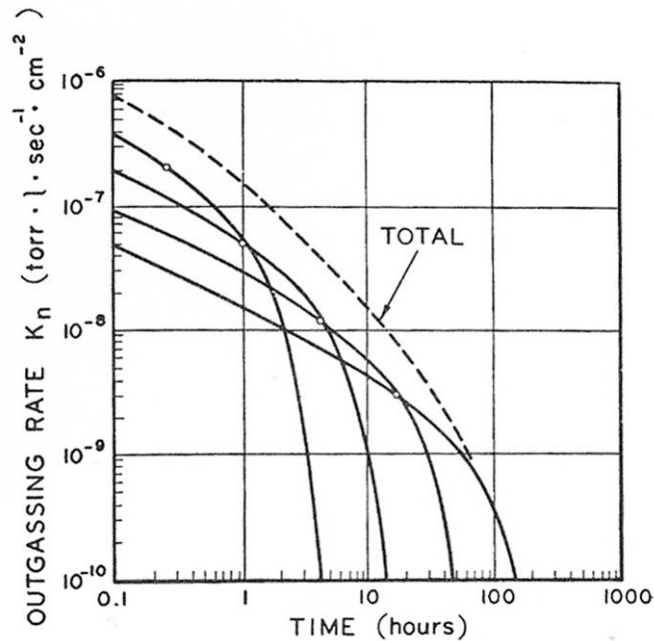
Figure 4.8 Typical outgassing curve vs. time for a metal surface in a vacuum [96].

Since the outgassing rate is a physical phenomena, it also varies with temperature. Figure 4.9 illustrates the theoretical change in outgassing rates from the same initial

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conditions at different temperatures.
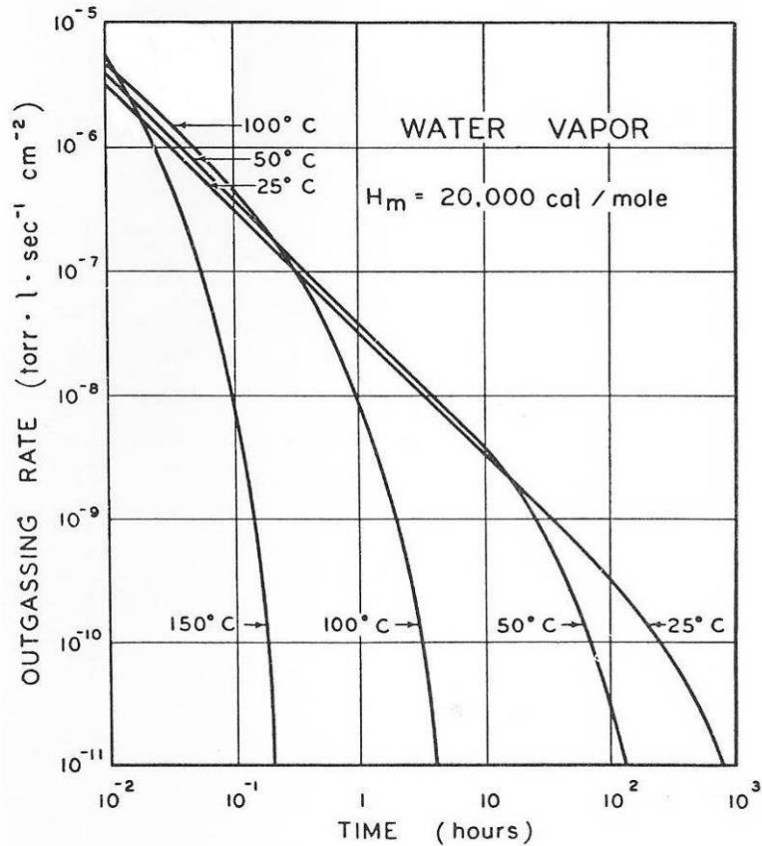
Figure 4.9 Theoretical outgassing curves for water vapor at different temperatures [96].

The curve at 25 °C is the same curve as the summation curve in Figure 4.8. As the temperature is increased from room temperature, the outgassing rate goes up as would be expected from a physical process. The initial higher rate removes the chemisorbed and physically adsorbed water much quicker than the room temperature rate, so the outgassing rate begins to fall off of the maximum rate more quickly than if it was outgassing at room temperature. For the 100 °C curve, the outgassing rate is approximately twice as high as the room temperature curve at the beginning, but after just 12 minutes the outgassing rate is the same as the room temperature curve. The rates are the same at this point; however, much more water vapor has been released for the 100 °C outgassing curve. Two important conclusions can be made from this data:

- Outgassing rates increase with an increase in temperature.
- The increased outgassing rate depletes the stored water vapor more quickly than outgassing at a lower temperature.

Outgassing is a major virtual leak that has a large impact on MEMS vacuum packaging, especially as package sizes scale to smaller sizes. Water vapor forms the largest percentage of outgassing contaminants in vacuum systems, including MEMS vacuum packages. The outgassing rate is highly dependent on the temperature of the package. An increase in temperature causes an increase in the outgassing rate. This increased rate depletes the amount of adsorbed water vapor quicker than rates at cooler temperatures; therefore the outgassing rate reduces more rapidly for higher temperature outgassing.

Pumps are the only way to eliminate leaks that cannot be mitigated by package design and material choices. The next section reviews pumps and presents a class of pumps that are easily integrated into MEMS vacuum packages, thin-film getters.

4.2.2 Pumps

There are several classes of pumps that create low pressure atmospheres, including: positive displacement, kinetic, and capture vacuum pumps [81]. However, only a few of the capture vacuum pumps can be integrated into a MEMS vacuum package, such as thin-film, non-evaporable getters (NEG) and sputter-ion pumps. These types of pumps have been the focus of research into pumping for MEMS vacuum packaging. The more widely used of these two types is the thin-film NEG pump. The next sections cover the operation and physics of thin-film NEG pumps as well as presenting applications of thin-film NEGs in MEMS vacuum packaging.

THIN-FILM NEG PHYSICS AND OPERATION

Thin-film NEGs are thin films of metal alloys that will capture gaseous molecules under certain conditions, which results in the net reduction of pressure inside a package cavity. Thin-film NEGs can be distinguished from other getter pumps because they remain in the solid state during the pumping process; there is not evaporation or

sputtering of the getter material in order to capture the gaseous species. Thin-film NEGs rely on mostly surface phenomena and bulk diffusion in order to capture and pump gaseous materials.

When a gaseous molecule strikes a solid surface, several things can occur. The two surface phenomena of interest in capture getter pumps are physical adsorption and chemisorption. Physical adsorption takes place when an impinging molecule hits the solid surface and remains physically stuck to the surface, without reacting with it. The whole gas molecule remains intact and weakly bound to the surface of the solid through Van der-Walls forces. If enough energy, in the form of thermal energy or energy from another impinging molecule, is supplied to a physically adsorbed molecule, it will break free from the surface and enter the gas phase again. Physical adsorption is a reversible process, i.e. the gaseous molecule is not trapped for a long time because it is easy for it to enter the gaseous phase again. Chemisorption, on the other hand, is not a reversible process. Chemisorption takes place when the impinging molecule reacts with the solid surface to form another compound. This can require disassociation of the gas molecule into atoms, which then react with the getter material to form new chemical compounds. The resultant chemical compounds are very stable and therefore the binding energy is much higher for chemisorption compared to physical adsorption. It takes large amounts of thermal or physical energy to break a chemisorbed bond; the gaseous molecule can be considered permanently removed into the solid state for almost all MEMS getter applications. The capture rate of gas molecules, or pumping speed, is represented by Equation (4.21):

$$S = \frac{s\,p}{\sqrt{2\,\pi\,m\,k\,T}} \qquad\qquad (4.21)$$

Where s, is the sticking coefficient of the gas, p, is the pressure of the gas, m is the mass of the gas molecule, T is the temperature in Kelvin, and k is Boltzmann's constant. The pumping speed maximizes when there are many surface sites for the gas molecules to land. As pumping takes place, these sites begin to fill up. Once the surface is completely covered in gaseous molecules, the pumping speed will drop to almost zero. The only way to increase the pumping speed again is to drive the surface molecules into the bulk with

diffusion and 'activate' the getter.

After a long period of time, all of the available sites on the surface of the getter are covered with physisorbed and chemisorbed molecules. These covered sites need to be opened up for more gaseous molecules to attach to so the pumping speed can be increased again. One way to do open up covered sites is to drive the chemisorbed and physisorbed atoms into the bulk of the getter with diffusion. Equation (4.22), shows the diffusion equation.

$$D = D_0 \, e^{\left(\frac{-E}{RT}\right)} \tag{4.22}$$

Where D is the diffusion, D_0 is the pre-exponential factor, E is the activation energy, R is the gas constant, and T is the temperature in Kelvin. By heating up the getter, the sorbed gas molecules are moved from the surface of the getter into the bulk, thereby freeing up new sites on the surface of the getter for more pumping to take place. The rate of diffusion of the sorbed gas molecules into the bulk is highly dependant on temperature and time. Usually a high temperature, such as 400 °C, is used for short periods of time to activate the getter. Activation can take place, so long as the molecules on the surface can be driven into the bulk to reveal fresh surface sites for pumping. After many activations, it becomes difficult to drive the same number of surface molecules into the bulk because the bulk has reached capacity. Therefore, the pumping speed after each activation will not reach the same maximum as it did for previous activations. This effect can be seen in Figure 4.10.
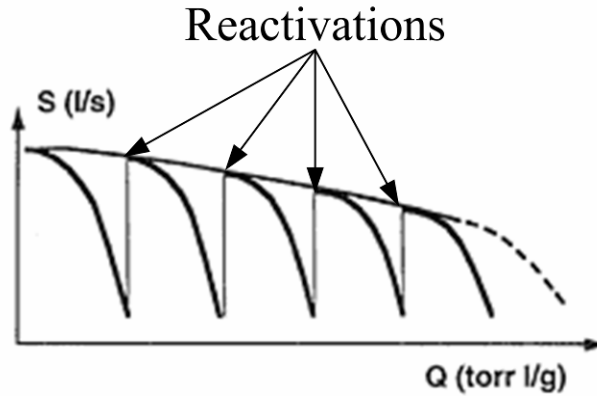
Figure 4.10 Plot of pumping speed versus sorption capacity for a common thin-film NEG [81].

For the first curve, the pumping speed starts at a maximum since all the surface sites are free for gas molecules to attach. As more gas is pumped (moving in the positive x direction on the plot), the free sites become occupied and the pumping speed will decline until reaching a minimum when all the sites are filled. At this point, the getter is reactivated with thermal energy, which drives the surface atoms into the bulk thereby freeing up more sites for pumping. With more sites free for pumping, the pumping speed is increased again, although not as high as the previous curve. Each subsequent reactivation will increase the pumping speed from the minimum, but not as high as the previous maximum since it becomes more difficult to drive the surface atoms into the bulk as it reaches its solubility limit.

Thin-film getters are typically deposited by sputtering or evaporation to a coating on the order of μms thick. Once the vacuum of the deposition technique is broken, the getter surface becomes quickly covered in gaseous molecules. Therefore, before the getter can pump any gas out of the package, it must be 'activated' by raising the temperature and driving the surface contaminants into the bulk. The activation frees up new sites on the surface of the getter for gaseous molecules to become physisorbed or chemisorbed.

APPLICATIONS OF THIN-FILM NEGS IN MEMS VACUUM PACKAGING.

Several getter systems have been reported for MEMS vacuum packaging: Titanium, Ti-Zr-V, and Nanogetters™.

Thin-film titanium NEG is the simplest of the three. It is not an alloy and therefore easily thermally evaporated. It is also widely available as a clean room material because of its use as an adhesion layer for other thin-film depositions. It has been reported as a thin-film getter for the packaging of resonators [97] and gyroscopes [98]. Titanium getters are usually activated at 400 °C [81].

An alloy of titanium-zirconium-vanadium has shown the best performance of the three getters. The deposition of the alloy is offered as a commercial service by SAES Getters corporation and has been widely reported on by the same. It offers better pumping speeds for certain gases and a lower activation temperature of 300 °C compared to a titanium thin-film NEG [99].

Nanogetters™ are a proprietary getter compound available from ISSYS Corporation. Little information on the pumping speed or film chemistry has been reported. However, it has been capable of achieving sub mTorr cavity pressures with activation temperatures of > 400 °C [25]. Thin-films of titanium and Nanogetters™ were used as getters for vacuum packaging in this work.

4.3 Previous Wafer Bonding Vacuum Packaging Approaches

Anodic, eutectic, and glass-frit have been demonstrated as excellent wafer bonding techniques for MEMS wafer-level vacuum packaging. Table 4.3 presents an overview of some published results, which are discussed briefly in the following paragraphs.

Table 4.3 Overview of selected wafer bonded MEMS vacuum packages. *The Al-Si to glass bonding was achieved with a localized heating bonding technique.

Packaging Approach	Bonding Temperature	Getters	Initial Vacuum	Leak Rate (days)	Ref.
Anodic Bonding	400 °C	Zr-V-Fe	10 µTorr	30	[100]
Glass Frit	> 400 °C	Nanogetters™	850 µTorr	121	[25]
Solder Bonding	?	?	4 mTorr	960	[101]
Au-Si Eutectic	400 °C	Nanogetters™	5 mTorr	360	[102]
Anodic Bonding	400 °C	Titanium	8 mTorr	40	[21]
Al-Si to Glass	800 °C*	none	25 mTorr	392	[103]

Esashi used anodic bonding in combination with a Zr-V-Fe NEG to achieve a vacuum package with an internal pressure of 10 µTorr that was stable for > 30 days [100]. The getter was not a thin-film getter. It was cut by hand from a large piece of bulk getter and housed in a separate cavity from the vacuum cavity. The pressure measurement was achieved with a differential capacitive measurement, where the pressure on one side of the cavity is controlled with a pump and the other side is the vacuum cavity. The error for this measurement was not reported and it is not clear how such a small pressure level could be measured by the force it applies on a capacitive plate. However, there is little doubt the pressure is well below 1 mTorr. This package represents some of the best early vacuum results using chip-level packaging.

Sparks used a glass frit bonding approach with Nanogetters™ to achieve a chip-scale MEMS vacuum package with an internal pressure of less than 1 mTorr as measured by resonating tubes [25]. The package showed excellent long-term pressure stability in storage at elevated and reduced temperatures. This technique was the first instance of the use of a thin-film getter integrated into a vacuum packaging process. By using a thin-film deposited getter instead of a bulk NEG as in the previous approach, the particles from bulk NEGs were reduced as well as allowing the package to be fabricated with clean room compatible processes at the wafer level. The wafer bonding temperature was not reported in the paper, but glass frit wafer bonding is achieved well above 400 °C and routinely even higher than 500 °C.

Schimert used an unknown solder alloy as a wafer-level bonding technique to vacuum

package IR bolometers below 10 mTorr for over 3 years [101]. Very little detail of the wafer bonding process was reported. No information on process flow, solder alloy type, getter type, or bonding conditions were included in the publication. The internal pressures were measured by using the bolometers as Pirani gauges.

Mitchell used a Au-Si eutectic solder to encapsulate polysilicon Pirani gauges at 400 °C with integrated Nanogetters™ to achieve 5 mTorr vacuum levels [102]. The vacuum levels have been stable for over three years and show leak rates of less than 2 mTorr/year. The bonding process takes ~ 1 hour with a maximum temperature of approximately 400 °C. The yield of the bonding process was high, greater than 80%.

Lee used anodic bonding with a thin-film titanium getter to package resonators at 8 mTorr for 40 days [21]. No information on the bonding temperature was included, but anodic bonding is typically achieved above 350°C and quite often at 400 °C. The pressures inside the cavities varied by the area of the titanium getter included in the package. For the packages with the most getter area (5 times the rest), the pressures were 8 mTorr as measured by resonating MEMS.

Cheng used a localized heating approach to achieve an aluminum-silicon to glass bond with internal cavity pressures of 25 mTorr [103]. This is the lowest wafer-bonded vacuum package pressure reported without the use of getters. Getters were not needed due to the careful control of the outgassing from the wafer during the bonding process. First, the cap wafer was baked at 150 °C for over 24 hours, and then covered with a shielding metal layer to prevent the outgassing of helium. Second, the localized nature of the bonding technique limited the temperature rise of any material not directly next to the bond rings. Since the outgassing rate is highly dependent on temperature (Section 4.2.1), the outgassing was minimized by keeping the temperature low. This technique requires a specialized bond ring design to achieve localized heating.

Many different types of wafer bonding have been used to create vacuum packages at the chip and wafer-level. Anodic, glass-frit, and eutectic solder have all demonstrated their capability at creating very low pressures inside MEMS vacuum packages if they are

integrated with a getter. Another approach to creating low pressures inside vacuum packages without getters is to use a localized bonding method and metal shield to minimize outgassing inside the package. For all the success in MEMS vacuum packaging, there is still a need for a generic wafer bonding approach that can create a MEMS vacuum package at low temperatures. The next section discusses the application of solder bonding technologies to achieve a generic wafer-bonded, low-temperature MEMS vacuum package.

4.4 Vacuum Packaging with Solder Wafer Bonding

Solder bonds have the potential to create MEMS vacuum packages at low temperatures. The next sections cover the effort to apply the solder bonding techniques presented in Chapters 2 and 3 to create MEMS vacuum packages. Two different Pirani gauges were used to measure the vacuum packages, a polysilicon and platinum gauge; their theory, fabrication, and performance are presented in Section 4.4.1. Table 4.4 summarizes the results from Section 4.4.2, which presents all of the packaging experiments. Finally, in Section 4.4.3, some interesting results on the low-temperature activation of titanium thin-film getters are presented.

Table 4.4 Summary of the MEMS vacuum packaging experiment results.

Bonding Technique	Temp./Time	Pirani Gauge	Pressures	Leak Rate	Notes
Au-Sn Solder	300 °C/20 mins.	Poly.	.6-.2 Torr	$1.5 \cdot 10^{-15}$ atm·cc·s^{-1}	Shortest bond cycle
Ni-Sn TLP Solder	300 °C/1 hour	Poly.	30-1 Torr	$1.7 \cdot 10^{-15}$ atm·cc·s^{-1}	Cheapest materials
Au-In TLP Solder	200 °C/1 hour	Poly.	10-.2 Torr	$1 \cdot 10^{-16}$ atm·cc·s^{-1}	Lowest temperature
Au-In TLP Solder	200 °C/25 hours	Platinum	.5-.02 Torr	No long-term data	24 hours at vacuum before bond cycle

4.4.1 Vacuum Measurements

There are many ways to measure vacuum levels in the range of 1 mTorr to 10 Torr [80]. The two most common methods for MEMS packages are the Q of resonant devices

and Pirani gauges. As covered in Section 4.1.2, the Q of resonant devices is highly dependent on the squeeze film damping effect, based on a change in pressure. To use a resonator as a vacuum sensor, the Q of the device is measured while the pressure is changed. Once the calibration curve is taken, the Q measured from the packaged resonator can be compared to the calibration curve to determine the pressure inside the package and monitor it versus time. Pirani gauges are used in a similar manner; however, they measure the thermal conductivity of the gas instead of the squeeze film damping effect. Pirani gauges were chosen as the vacuum measurement technique for this work since they are simpler to fabricate and measure.

A Pirani gauge works by measuring the thermal conductivity of a gas. Recall from Section 4.1.1, that the thermal conductivity of a gas is determined from Equation (4.2):

$$\kappa = \frac{1}{3} m \lambda \eta \upsilon_{ave} c_v$$

The thermal conductivity of a gas is constant with pressure because the change in mean free path, λ, and molecular density, η, with pressure cancel each other out. However, a Pirani gauge constrains the mean free path by suspending a platform a distance, d, above a substrate. Once the pressure level in this gap reaches a level where the mean free path is 10 times greater than the gap distance, the thermal conductivity of the gas becomes proportional to pressure. A Pirani gauge measures this thermal conductivity by creating a known amount of heat on the platform, and then measuring the temperature rise. Dividing the temperature rise of the platform by the heat created on it will give the thermal conductivity of the system. By measuring the thermal conductivity of the gauge over the pressure range of interest, a calibration curve can be generated. The measurement of the packaged gauge can be compared to this calibration curve to determine the pressure inside the cavity and monitor it over the long term. More detail on the operation of Pirani gauges, including more mathematical analysis, is covered in [5].

Two Pirani gauges, a polysilicon gauge and a platinum gauge, were used to measure the vacuum level inside the packaging techniques presented in this chapter. Their

fabrication sequence, measurement technique, and error estimate are presented in the next sections.

POLYSILICON PIRANI GAUGES

The polysilicon Pirani gauges were fabricated using a surface polysilicon micromachining process. The process was developed by Jay Mitchell and is described in detail in [5]. The ladder structure of the Pirani gauges adds extra area where heat is conducted from the gauge through the gas to the substrate. Adding the ladder rungs increases the sensitivity of the gauge by roughly a factor of two [5]. The basic process and Pirani gauge performance are summarized here.

The process starts with a single-sided silicon wafer. A 2 μm thermal oxide is grown, followed by a LPCVD silicon nitride film 3000 Å thick. Next, the first polysilicon feedthrough layer (3000 Å) is deposited and patterned. A passivation layer (silicon nitride 3000 Å) and sacrificial layer (silicon dioxide 2 μm) are next deposited by LPCVD. The anchors are opened in the oxide/nitride stack down to the first polysilicon layer with dry etching. Finally, the second layer of polysilicon (2 μm), which forms the Pirani gauges, is deposited and patterned to finish the Pirani gauge process. At this point, the wafers are ready for the bond ring to be fabricated on top of them. The bond ring must be able to survive the release step, which is 40 minutes in a buffered hydrofluoric acid etch. Or alternatively, a photoresist layer should cover the bond rings to protect them from the BHF etc. After the oxide layer is removed, the wafers are dried by critical point drying, and then they are ready to be packaged. Figure 4.11 shows SEM images of the two types of poly-Pirani gauges used in this work, the short and long types, after release and drying.
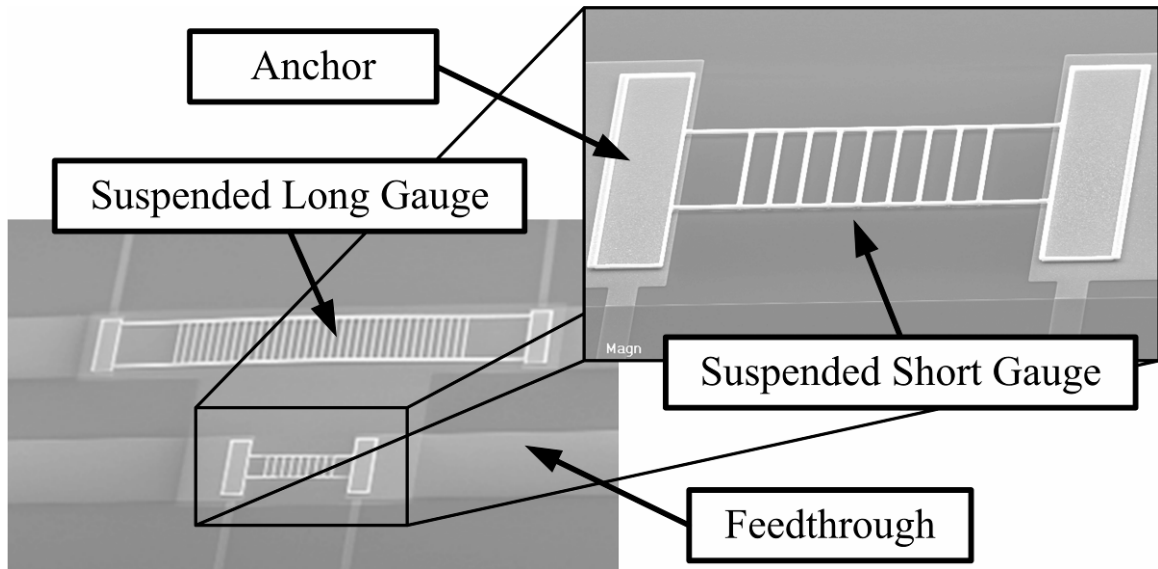
Figure 4.11 SEM images of the short and long surface micromachined Pirani gauges [5].

The Pirani gauges are measured by a four-point probe method. Current is driven through the gauge and the voltage is measured from anchor to anchor. Dividing the voltage by the current gives the resistance of just the suspended gauge, which is the only part of the structure that is suspended. Since it is the only part suspended, it is the only part that is thermally isolated from the substrate and therefore the only part of the structure that heats up.

The thermal impedance of the gas between the suspended bridge and substrate is measured by flowing increasing amounts of current through the bridge. As the current increases, more joule heating occurs in the bridge and the temperature of the bridge rises. This temperature rise can be measured by measuring the change in resistance of the bridge versus a null value taken at very small currents where joule heating has not occurred. The temperature of the bridge from the TCR of the polysilicon can be plotted versus the power generated from the joule heating in the bridge structure. The slope of this line is the thermal impedance of the gas in the gap between the bridge and substrate. Several of these thermal impedance measurements were taken as the pressure was varied across the two gauges to produce a characterization profile of the gauges (Figure 4.12). The dynamic range of the two gauges is from 1 mTorr to 30 Torr for the long gauge and from 100 mTorr to 100 Torr for the short gauge.

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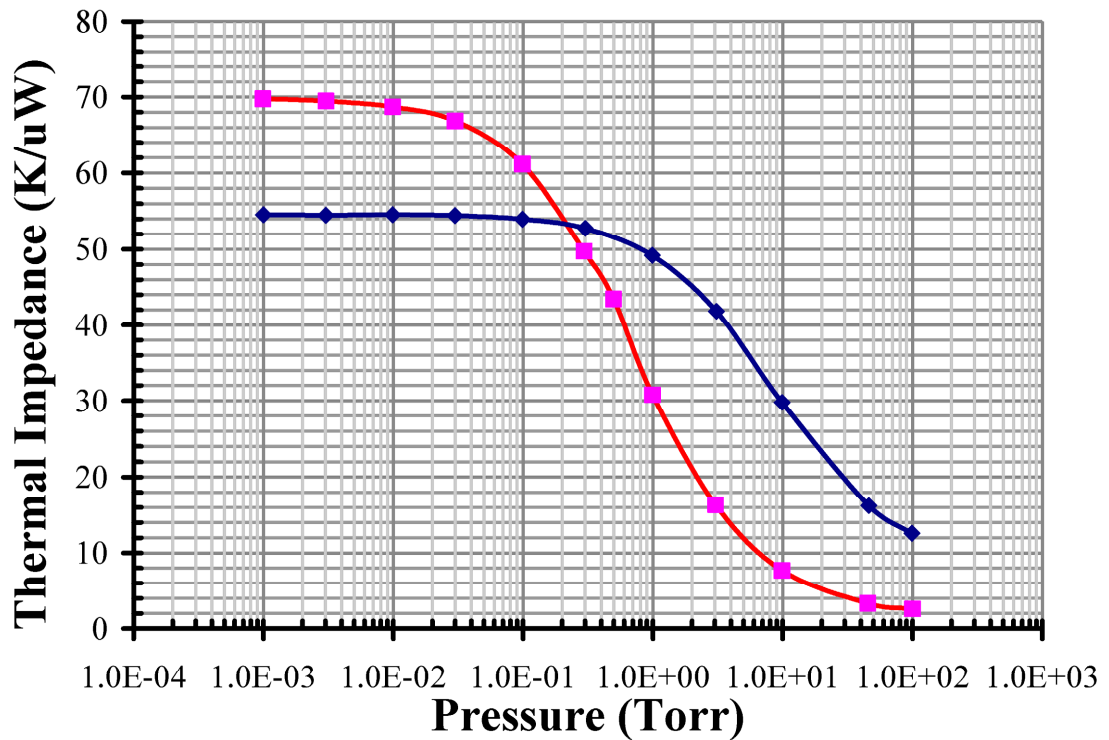
Figure 4.12 Characterization plot of the short and long Pirani gauge types. The short gauge's maximum thermal impedance is 55 K/µW while the long gauge's maximum is 70 K/µW.

The error of the pressure measurement can be calculated by taking many measurements at the same pressure, then taking the standard deviation and averages of the measurements to use in a confidence integral to calculate the error in thermal impedance, which can then be used to estimate the pressure error. The confidence integral is found using the Student's T-distribution because the sample size is small (< 40 measurements) [104]. Table 4.5 shows the data taken for the long polysilicon gauge. More information on the resolution and sources of pressure measurement error are given in [5].

Table 4.5 Pressure measurements and statistical analysis based on Student's T-distribution for the long polysilicon Pirani gauge.

Pressure	Avg. T.I.	Sigma T.I.	# of Measurements	99% C.I. Factor	99% T.I. Error	
					Upper	Lower
0.00099	69761	61	11	3.169	69821	69699
0.00303	69482	35	11	3.169	69517	69446
0.0099	68700	63	11	3.169	68763	68636
0.03	66840	70	11	3.169	66910	66769
0.099	61159	37	11	3.169	61195	61122
0.296	49732	98	11	3.169	49829	49633
0.499	43452	61	11	3.169	43513	43390
0.993	30792	78	11	3.169	30870	30713
3.04	16345	35	11	3.169	16380	16309
9.9	7696	52	11	3.169	7748	7643
45.2	3331	64	11	3.169	3395	3266
100	2574	60	11	3.169	2633	2514

PLATINUM PIRANI GAUGE

Another Pirani gauge fabrication technique was developed to investigate a different release technique. The fabrication and characterization data are presented in the next few paragraphs.

The fabrication begins with a single-sided silicon wafer. A 0.5 µm thermal oxide is grown on the wafer, which will serve as the support for the thin-film of platinum. Next, the thin-film of platinum is deposited on top of the oxide. The same layer of platinum serves as the feedthroughs and Pirani gauge. The platinum is patterned by a liftoff process. Next, a 1 µm passivation stack of PECVD oxide, nitride, and oxide is deposited. The films are deposited in that sequence to minimize the formation of pinholes that are continuous throughout the stack. After the passivation layer is deposited, the passivation and oxide are etched completely down to the silicon to define the Pirani gauge platform and supports. At this point, the package bond rings are created by the various electroplating, PVD, and etching steps that are specific to each solder bonding technique. After the bond ring is fabricated, the Pirani gauge is released in a XeF_2 etch tool. The silicon wafer itself acts as the sacrificial material for this Pirani gauge. XeF_2 etches

silicon with excellent selectivity to almost any other material, which makes this a particularly attractive technique for sensitive manufacturing processes. Another advantage of the XeF$_2$ release step is that it is a dry process; therefore critical point drying is not necessary to keep the Pirani gauge from sticking to the substrate. Figure 4.13 shows a SEM image of the completed Pirani gauge. The support beams are 110 µm long and 6 µm wide.
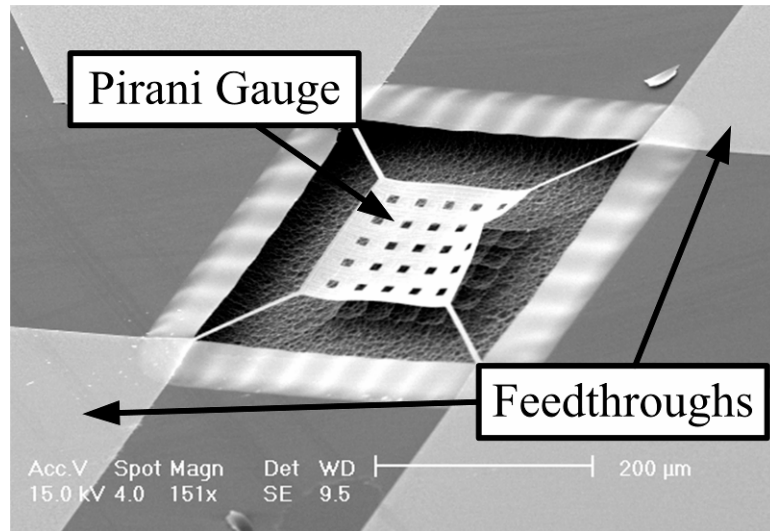
Figure 4.13 SEM image of the platinum Pirani gauge.

The platinum Pirani gauges are measured in the exact manner as the polysilicon gauges. The calibration curve for the gauge is shown in Figure 4.14. The dynamic range of this gauge extends from 1 mTorr to 10 Torr just as the long polysilicon gauge.
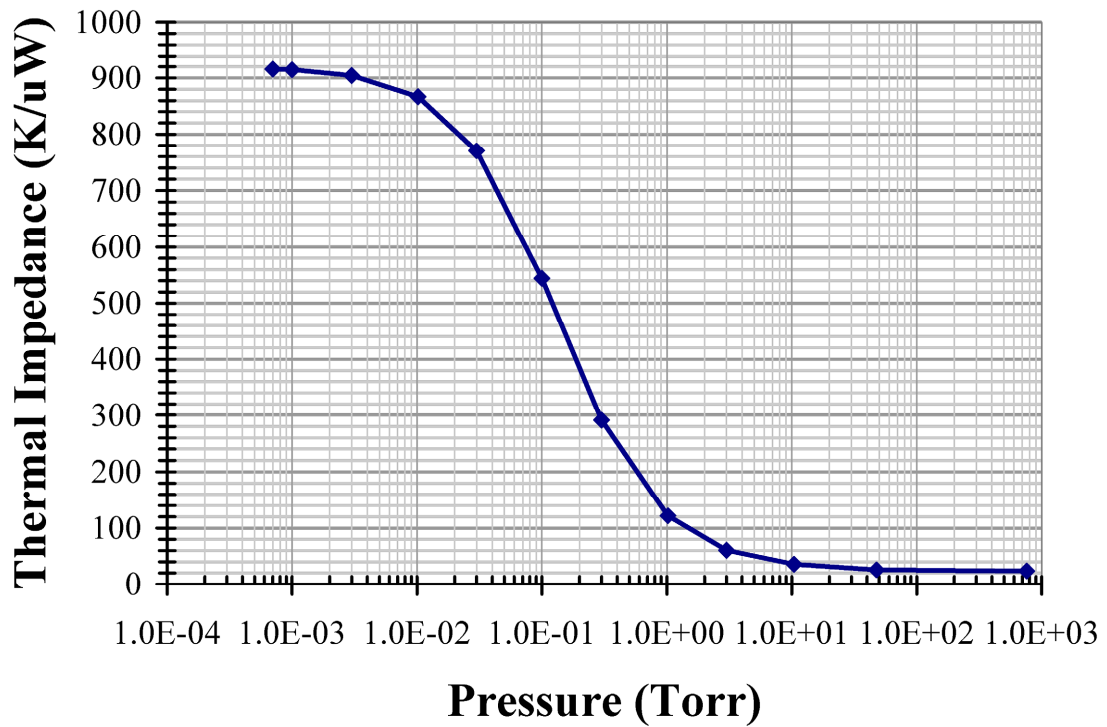
Figure 4.14 Platinum Pirani gauge characterization plot.

The same error estimate method as the polysilicon Pirani gauges was also used to estimate the measurement error for the platinum Pirani gauges. Table 4.6 shows the data taken from one platinum Pirani gauge. Fewer measurements were taken than the polysilicon Pirani gauges, only 3 instead of 11. The pressure error data for the pressure range of interest in MEMS vacuum packaging is included for the platinum Pirani gauges in the final column. For pressures less than 300 mTorr, the error for the calibrated gauge was less than 1 mTorr.

Table 4.6 Characterization data for the thin-film platinum gauge. Three measurements were taken at each pressure.

Pressure (Torr)	Avg. Thermal Impedance	Sigma Thermal Impedance	99% C.I. Factor	Thermal Impedance Error	Pressure Error (mTorr)
0.0007	915695	116.0	9.925	814	0.157
0.001	914519	152.4	9.925	1070	0.206
0.003	904166	84.9	9.925	596	0.115
0.0102	866593	300.9	9.925	2112	0.407
0.03	770355	258.6	9.925	1815	0.326
0.1	544434	357.5	9.925	2509	1.393
0.3	291150	2.6	9.925	19	0.037
1.02	122002	45.4	9.925	319	-
3.01	60724	96.7	9.925	679	-
10.4	35737	35.2	9.925	247	-
47.7	25629	1.2	9.925	8	-
760	23523	15.9	9.925	111	-

Both the polysilicon and platinum Pirani gauges were packaged using the bonding techniques presented in Chapters 2 and 3 to determine the vacuum and hermetic capabilities of those bonding methods. The next sections present the details of the fabrication for each package as well as SEM images and pressure measurements from each package.

4.4.2 Packaging Experiments

Three different bonding techniques were used to create wafer-level MEMS vacuum packages: the Au-Sn standard solder bond, Ni-Sn TLP solder bond, and Au-In TLP solder bond. All the bonding techniques demonstrated the hermetic sealing capability necessary to create MEMS vacuum packages. Two different getters were used for the packages. For some of the packages Nanogetters™ from ISSYS Corporation were deposited on the ceiling of the package and, for others, a thin-film of titanium was sputtered or evaporated on the ceiling of the package. The getter used for each package is listed in its respective process flow.

AU-SN STANDARD SOLDER BONDING

The polysilicon Pirani gauges were used to test the hermeticity and vacuum capability

of the standard Au-Sn solder bond. After the polysilicon gauges were fabricated according to the process flow described previously, the package fabrication began.

The packages were made from two wafers: a silicon cap wafer and the Pirani gauge device wafer. First, both wafers had the electroplating seed layer deposited (1kÅ Cr / 2.5 kÅ Au) by sputtering PVD. Next, both wafers were electroplated with 7 μm of gold, then 5 μm of tin into a photoresist mold that forms the bond rings. The photoresist mold is then stripped and a new photoresist layer is deposited to protect the bond rings on both wafers for the next steps that are separate for each wafer.

For the cap wafer, the photoresist is patterned such that it is 20 μm wider than the bond ring. The seed layer is etched in gold and chrome wet etchants. The wafer is then put into a deep reactive ion etch (DRIE). The DRIE selectively thins the cap wafer throughout except the bond rings (and 20 μms on either side of them). This creates clearance for the Pirani gauge and dicing saw during the final singulation steps. If the package cap was not thinned with DRIE, the Pirani gauges would reach the ceiling of the package cap. Also, the precision on the height setting of the dicing saw blade is too coarse to cut the top cap wafer without cutting the bottom device wafer if the bond ring is the only structure separating the two. Therefore, the DRIE step is needed to make the cap thinner. After the DRIE step, the titanium getter was deposited and patterned by a liftoff process.

For the device wafer, the photoresist serves to protect the bond ring material during the seed layer etch and from the buffered hydrofluoric (BHF) acid etch that is used to sacrifice the silicon dioxide layer beneath the Pirani gauges. After the seed layer is etched in gold etchant and chrome etchant, the gauges are released. The release etch takes approximately 40 minutes in BHF. After the gauges are released, the photoresist protecting the bond rings is stripped in acetone and IPA, then left to soak in methanol for 20 minutes, *all without letting the wafer dry*. Care must be taken to prevent the gauges from sticking to the substrate when the wafers dry. After the methanol soak is complete, the wafers are dried in a critical point dryer (CPD) to prevent stiction. The final wafer cross-section directly before bonding is shown in Figure 4.15.
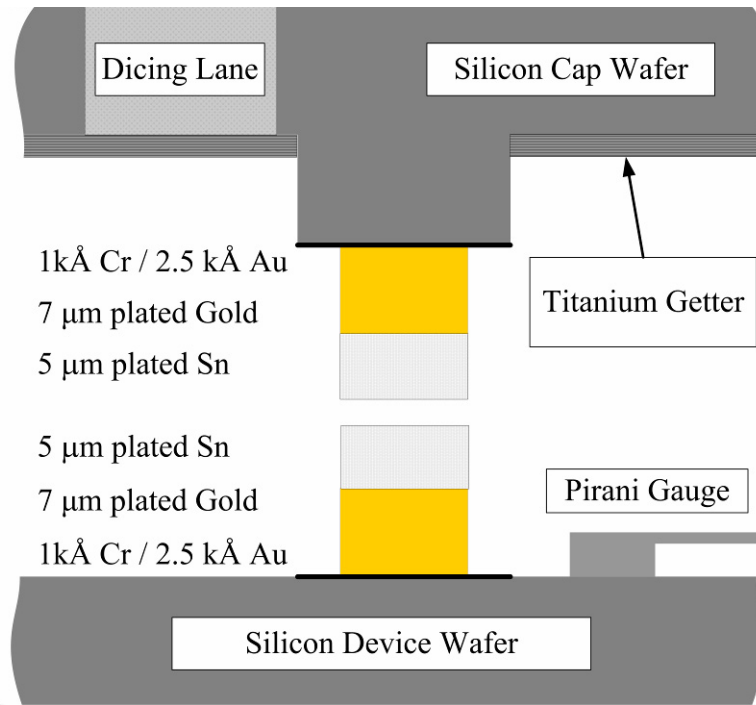
Figure 4.15 Cross-section of the wafers directly before performing the Au-Sn standard solder bond.

After the fabrication is complete, the wafers are aligned and bonded in the SUSS SB6e wafer bonder. The same bond profile that was used to create the Au-Sn standard solder bond in Chapter 3 is used to create the Au-Sn solder bond for the wafer packages. The bonder chamber is first pumped to high vacuum (10 µTorr), to removing all the oxygen from the chamber and enabling a fluxless soldering process. Once the chamber reaches high vacuum, the wafers are heated to the bonding temperature (300 °C) and held there for 10 minutes. The bonding force was kept to a minimum value of 150 Torr. The force necessary to create a quality Au-Sn standard solder bond is less than TLP solder bonds because most of the Au-Sn standard solder bond is molten for the entire bond cycle, instead of just a small percentage of the bond joint as is the case for TLP solder bonds. As the wafers reach the Au-Sn eutectic temperature, the solder melts and seals the package cavities. This means that all of the outgassing that happens during the rest of the bond cycle is trapped inside the package cavities. After the holding period is over, the wafers are allowed to cool past 220 °C before the chamber is vented to atmosphere and the bond is complete. Illustrations of the bond cycle are shown in Figure 4.16.
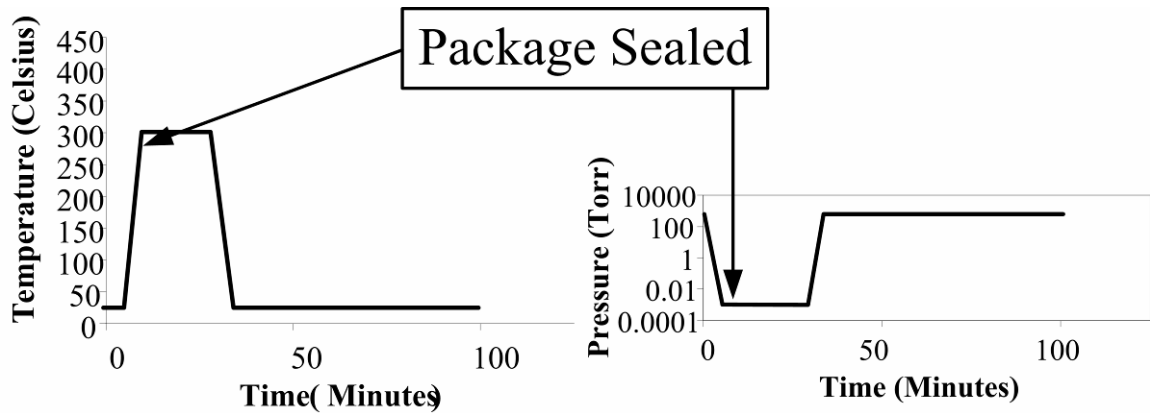
Figure 4.16 Bond cycle temperature and pressure profiles for the Au-Sn standard solder bonded packages. The bond cycle requires approximately 30 minutes.

Once the bond was complete, the wafers were removed and underwent several tests. First, a package was deliberately broken with a razor blade to inspect the bond cross-section. Once the package was broken, the cap side was cleaved across the bond ring. The cleaved section was inspected with a scanning electron microscope. The results are shown in Figure 4.17.
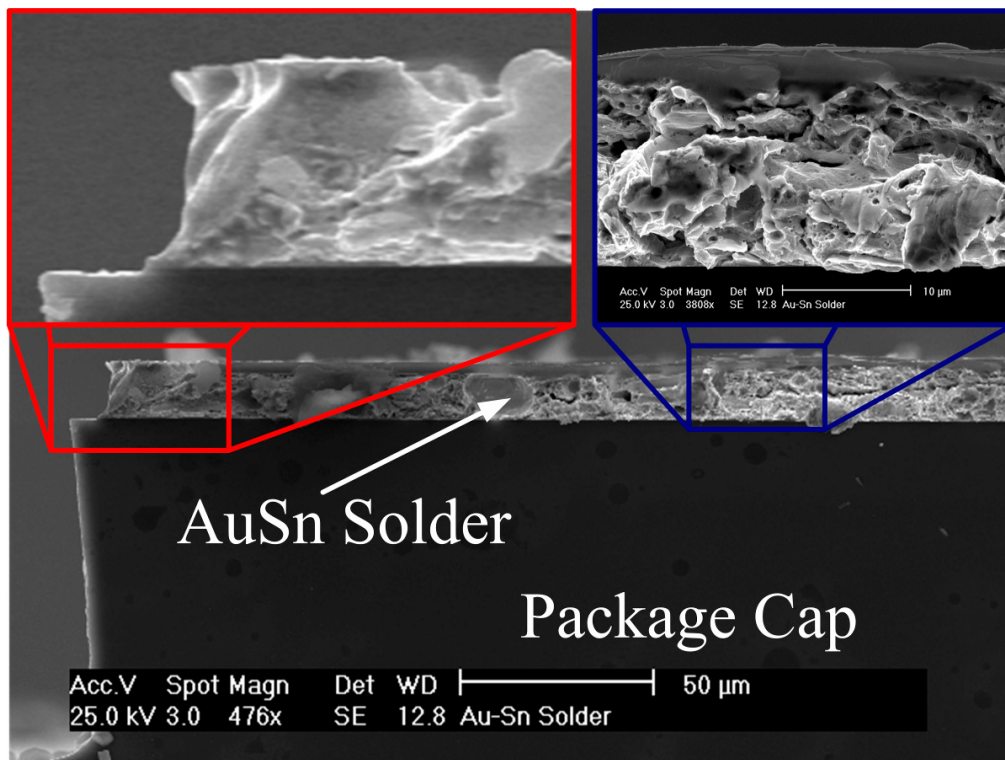
Figure 4.17 SEM image of the Au-Sn bond from the package. The insets show magnified views of the Au-Sn solder layer.

The SEM image in Figure 4.17 shows the Au-Sn solder sitting on the package cap. The magnified inset in the upper left-hand corner of the image shows the Au-Sn solder clearly wetting the seed layers on both wafers. This indicates that, despite the long bond cycle time, the Cr-Au seed layer survived the bond cycle without getting completely consumed by the tin layer. This is the major advantage of the Au-Sn standard solder bond; the low tin content allows standard UBMs, like gold-chrome, to withstand contact with molten solder for extended thermal cycles. The inset in the upper right-hand corner shows that the morphology of the Au-Sn solder bond does not contain voids and therefore can provide a good hermetic seal. The hermeticity of the Au-Sn solder seal is evident in the vacuum data presented in Figure 4.18.
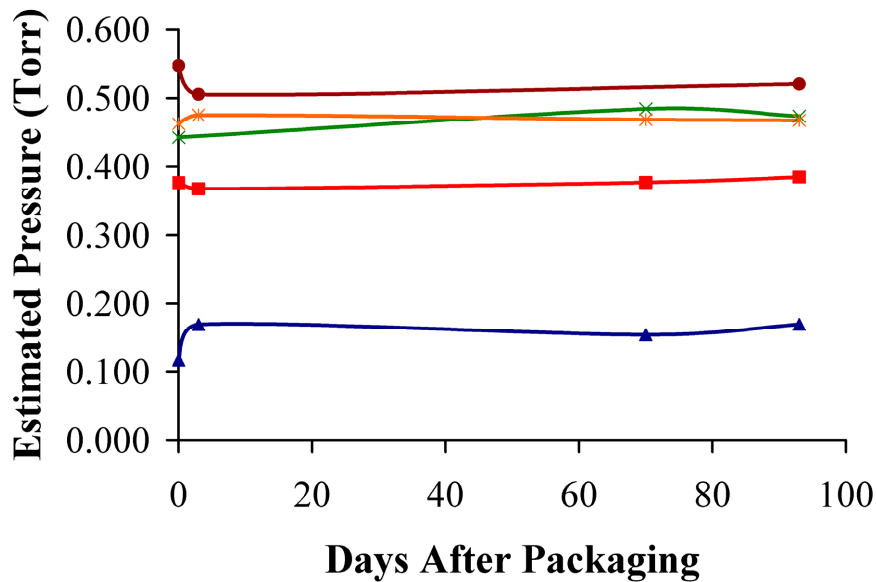
Figure 4.18 Long-term vacuum data for the Au-Sn solder bond with fully activated getters. The pressures inside the packages varied from 600 mTorr to 200 mTorr and have remained stable over 90 days.

The Pirani gauges inside the packages were monitored over 90 days. The pressures inside the cavities range from 200 mTorr to 600 mTorr and have been stable for over 90 days. The estimated pressures show no observable leak-rate trends; however, a worst-case line can be fit within the measurement error of the pressure measurement (Figure 4.19).

Estimated Pressure (Torr)

0.600

0.550

0.500

0.450

0.400

Worst case leak rate
71 mTorr/year

0   20   40   60   80   100

Days after Packaging
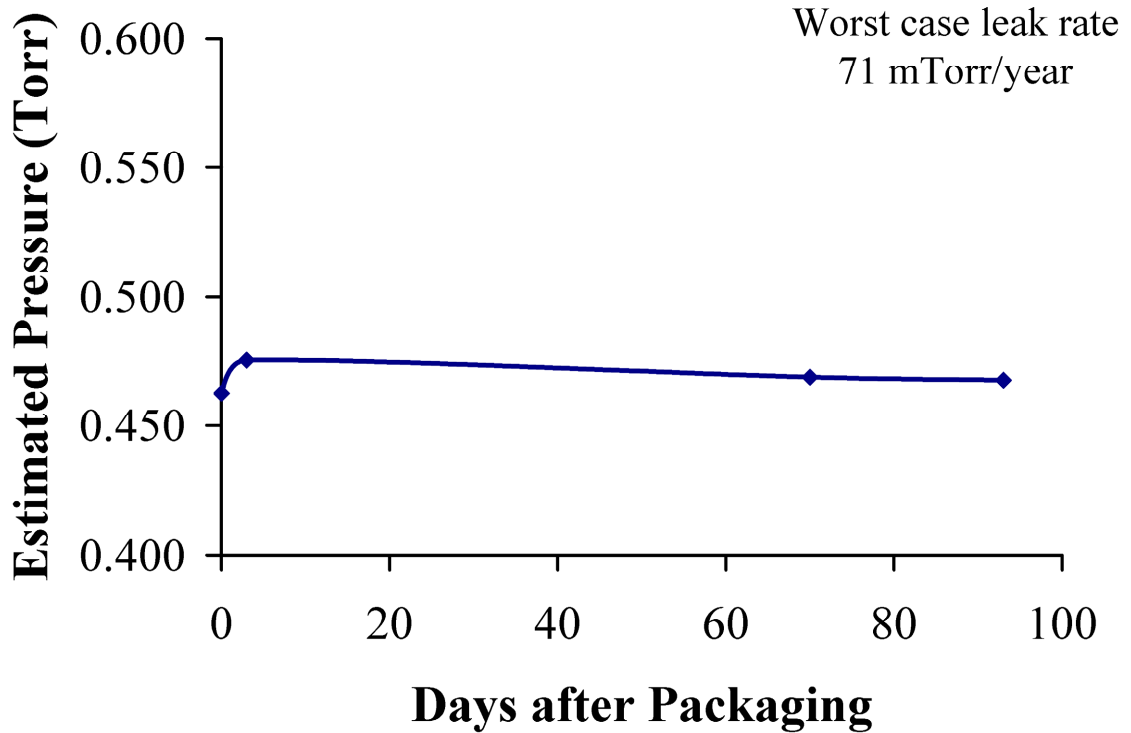
Figure 4.19 Magnified view of the pressure data for a package from the Au-Sn standard solder bonded wafer. The worst-case leak-rate that fits within the pressure measurement error for the Au-Sn Solder bonded packages is 71 mTorr/year (1.5·10^{-15} atm·cc·s^{-1}).

The worst case leak rate trend shows a leak rate of 71 mTorr/year, which corresponds to a leak rate of 1.5·10^{-15} atm·cc·s^{-1} for a package volume of 0.5 µL. Since this leak rate estimation is based on the worst case fit of a trend line through the pressure measurement error, the leak rate will decrease as more data is taken over a longer time. This is expected because there is not an observable trend in the vacuum data that would indicate a larger leak rate than this worst case estimate.

The Au-Sn standard solder bonded packages were also tested for strength. The details of the measurement are covered in Chapter 3, but the summary of all the tests for Au-Sn standard solder bonding are presented in Table 4.7.

Table 4.7 Summary of package testing data for the Au-Sn standard solder bond.

Metric	Test Methodology	Result
Hermeticity	Long-term vacuum data	$1.5 \cdot 10^{-15}$ atm$\cdot$cc$\cdot$s^{-1}
Strength	Shear test	28.0 MPa
Re-melting Temperature	From solder theory	~ 280 °C

Ni-Sn TLP Solder Bonding

The Ni-Sn TLP solder bond was used to package the polysilicon Pirani gauges. After the Pirani gauge fabrication process was complete, the package was created in a similar fashion as the Au-Sn standard solder bonded packages by bonding a cap wafer to the Pirani gauge device wafer.

The packages were created with two double-side polished silicon wafers. The silicon device wafer contains the aforementioned Pirani gauges and the silicon cap wafer serves as the package cap. Both wafers had a seed layer of 1kÅ Cr / 2.5 kÅ Au deposited on them by sputtering PVD. A Cr-Ni seed layer is another option that can be used for packaging processes that need to be gold-free. A large benefit in using a gold seed layer, and the major reason it was used in this process, is that gold simplifies the nickel electroplating step because it does not form a native oxide and therefore special chemical treatments are not necessary before electroplating. If a nickel seed layer was used, a dilute hydrochloric acid dip directly before electroplating will remove the native oxide from the nickel seed layer and ensure quality adhesion between the electroplated nickel and the seed layer. After the seed layer is deposited, a photoresist mold is formed to pattern the electroplating steps that create the bond ring. Two electroplating steps form the bond ring, and they are identical for both the package cap wafer and the device wafer. A 5 μm layer of nickel is electroplated, followed directly by 3 μm of tin on top of it. The tin layers serve two functions: they are the interlayer for the TLP solder bond and also enable fluxless processing of the bond. The tin makes the process fluxless by preventing the underlying nickel from growing a native oxide. The tin native oxide is not a concern for fluxless processing, because it can be broken once by the bond force once the tin is molten. After the electroplating steps, both wafers are covered with a photoresist layer that will protect the bond rings during further processing.

The cap wafer is further processed by patterning the protective photoresist to cover the bond rings and a space of 20 μm on either side of them. This photoresist allows the seed layer to be etched in Au and Cr wet etchants without damaging the electroplated bond ring. After the seed layer is removed, the cap wafer is thinned by DRIE and the titanium getter layer is deposited and patterned by liftoff. This completes the cap wafer processing.

The device wafer is further processed by patterning the protective photoresist in the same manner as the cap wafer. The seed layer is also etched in the same way. The photoresist is left after the seed layer removal to protect the bond rings during the Pirani gauge release step. The Pirani gauges are released in a BHF acid etch for 40 minutes, followed by removal of the protective photoresist in acetone, cleaning in IPA, and a methanol soak. After soaking in methanol for 20 minutes, the device wafer is loaded into the CPD tool to complete the release. A 5 minute oxygen plasma ashing step removes any methanol residue left over from the CPD release. The final cross-section of the wafers is shown in Figure 4.20.
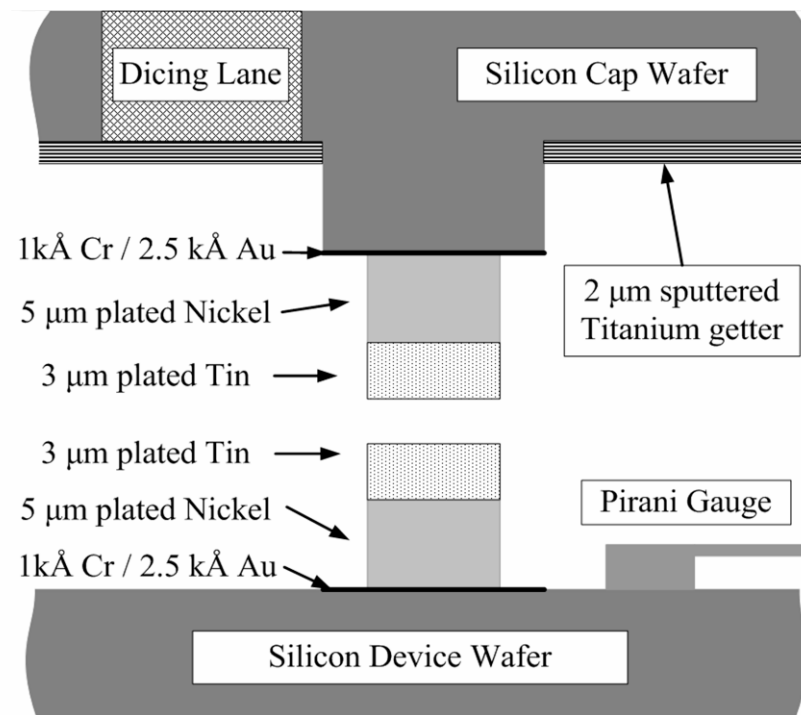
Figure 4.20 Cross-section of the Ni-Sn TLP solder bonded wafers directly before the bond cycle.

After the wafer fabrication is complete, the wafers are aligned in a SUSS BA-6 aligner and then bonded in a SUSS SB6e wafer bonder. The same process that was used to create the Ni-Sn TLP solder bonds in Chapter 3 was used to create these packages. First, the bonder chamber is pumped to a high vacuum level (< 10 µTorr) to reduce the final pressure inside the packages and, more importantly, remove as much of the oxygen as possible from the bond chamber to enable fluxless processing. If there were oxygen in the bond chamber during the bond cycle, a clean molten tin surface would never develop in the bond joint, which would inhibit good wetting and thus a strong bond. After the bonder chamber reaches high vacuum, the wafers are heated to the bond temperature. The bond temperature for the Ni-Sn TLP solder bond is 300 °C and the wafers are held there for 1 hour to complete the bond. After one hour, the wafers are cooled to room temperature and unloaded from the bond chamber. Figure 4.21 illustrates the temperature and pressure levels inside the bond chamber during the bond cycle. Note that the packages are sealed within the first ten minutes of the bond cycle as the temperature passes 230 °C and the tin interlayer melts.
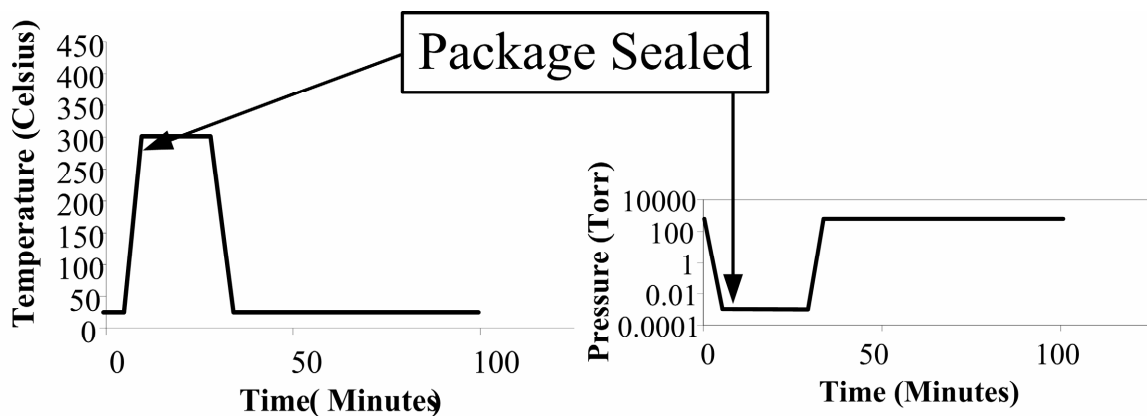
Figure 4.21 Bond cycle for the Ni-Sn TLP solder bonded vacuum packages. The packages are sealed at the beginning of the bond cycle.

After the bond cycle is complete, the wafers were removed from the bonder and singulated using a dicing saw. There are two cuts that need to be made to create the final package. The first pass only cuts through the cap wafer (without touching the device wafer) and removes all of the cap wafer between each package, leaving only a small margin of silicon hanging over the edge of the bond ring. The second pass cuts entirely through to separate the device wafer into individual die. A picture of the wafer was taken

after the first dicing pass, but before the second dicing pass (Figure 4.22) that shows the wafer with the majority of the cap wafer cut away but before the wafer is separated into individual die. The inset of the picture shows the wafer in a later state after one of the package caps was deliberately removed with a razor blade to show the detail of the Pirani gauge inside the package.
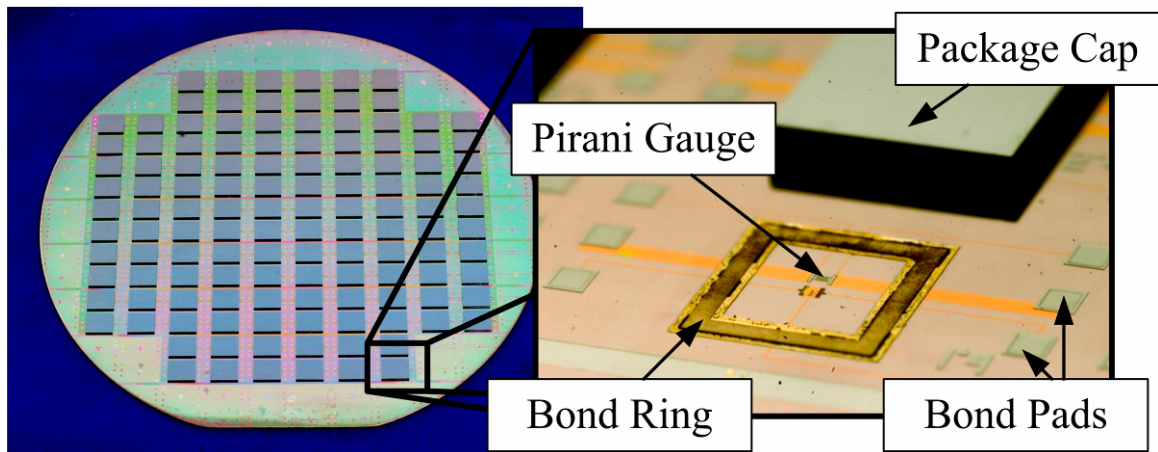
Figure 4.22 Photo of Ni-Sn TLP solder bonded wafer. Inset shows a magnified view of a package cap, bond ring, and a polysilicon Pirani gauge.

The polysilicon Pirani gauges were measured to determine the pressures inside the package cavities over the long term. The pressures ranged from 20 Torr to less than 250 mTorr and have remained stable for over 220 days. Figure 4.23 plots the pressure levels inside a sampling of the package versus time. The error bars indicate a 99% confidence integral that was calculated using a Student-T distribution. The wide range of pressure levels inside the cavities is believed to be due to the differences in outgassing and getter activation levels across the wafer. To further investigate these effects, some experiments on post-packaging getter activation were performed; the results are presented in Section 4.4.3.
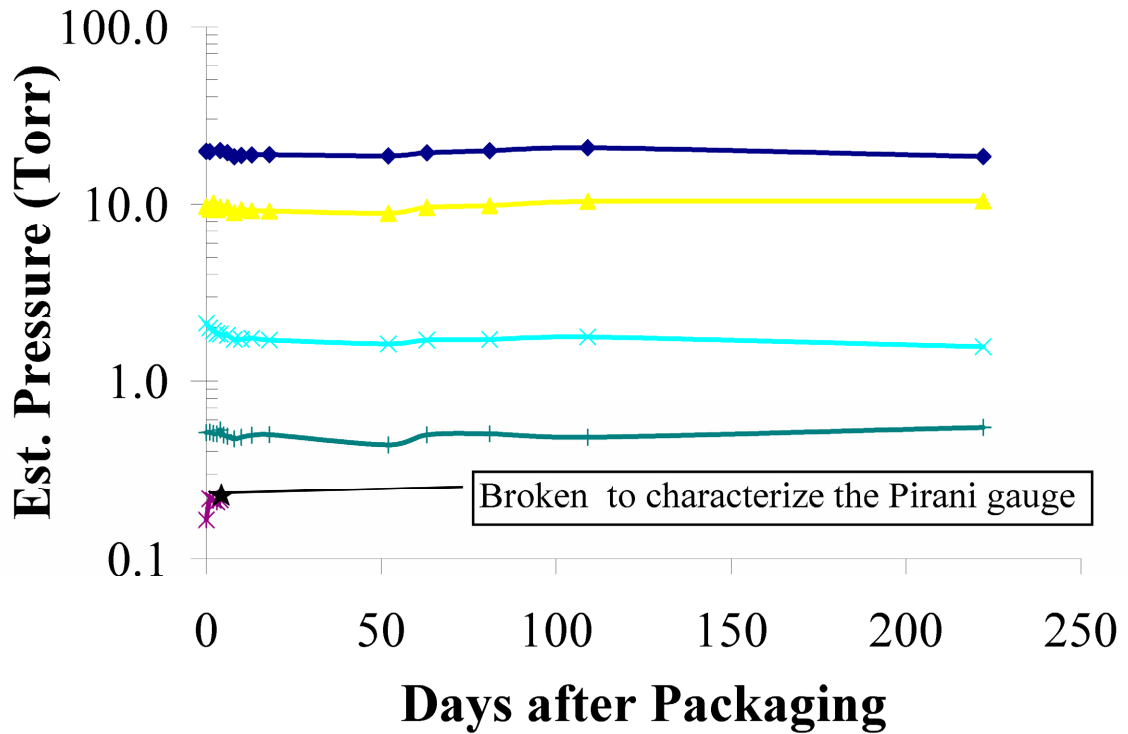
Figure 4.23 Estimated long-term pressure data for the Ni-Sn TLP Solder bond. The pressures varied from 10s of Torr to 200 mTorr.

No observable leaks were found in any of the sealed packages. To estimate a leak rate for this bonding technology, the data from one package was inspected more closely (Figure 4.24). The plot shows a zoomed view of the package pressure data and illustrates the worst case leak rate that can be fit inside the 99% confidence integral error of the pressure measurement data. The worst case estimation of the pressure rise is 81 mTorr/year, which corresponds to a leak rate of $1.7^. 10^{-15}$ cc·atm·s^{-1} for a package volume of 0.5 μL.
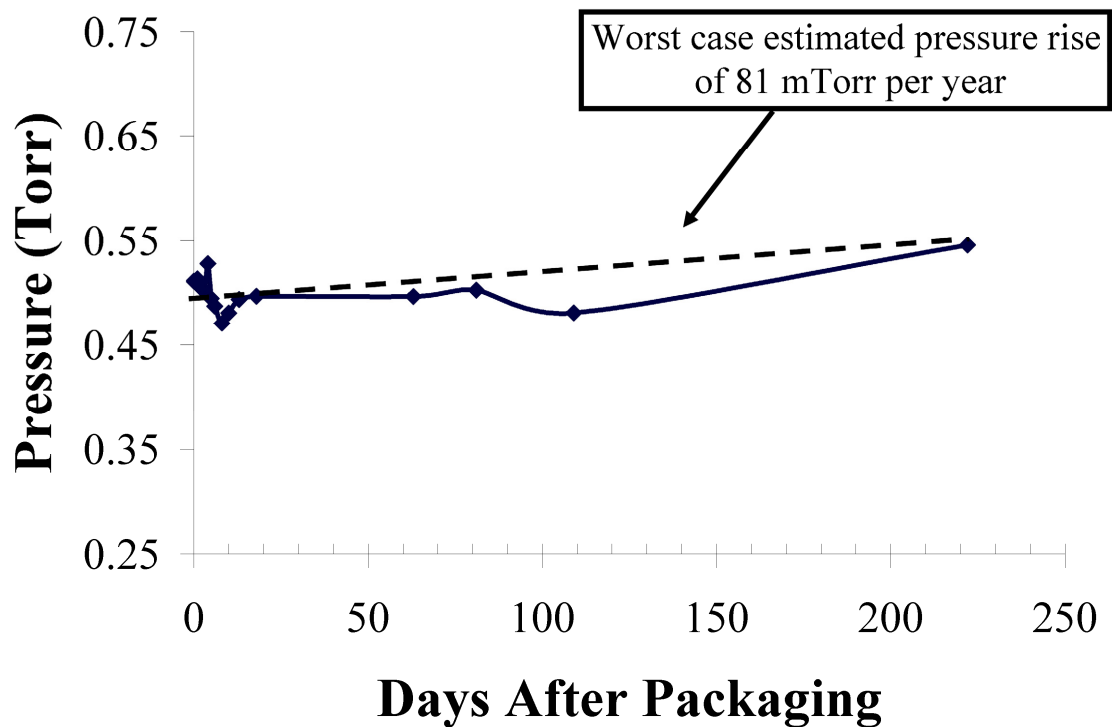
Figure 4.24 Magnified view of the pressure of one die over time. The worst case leak rate for the Ni-Sn TLP solder bond was 81 mTorr/year (1.712·10⁻¹⁵ cc·atm·s⁻¹).

The packages were also tested for shear strength using an in-house shear strength test setup as well as tested for thermal robustness on a hotplate. The details of the tests and data are presented at the end of Chapter 3 in Sections 3.4.2 and 3.4.3. A summary of the data is provided in Table 4.8 for quick reference.

Table 4.8 Summary of data from the tests on Ni-Sn TLP solder bonded packages.

Metric	Test Methodology	Result
Hermeticity	Long-term vacuum data	1.10^{-15} atm·cc·s⁻¹
Strength	Shear Test	12.1 MPa
Re-melting Temperature	Hotplate	> 450 °C

AU-IN TLP SOLDER BONDING

Au-In TLP solder bonding was combined with the polysilicon Pirani gauges to determine its capability as a wafer-level vacuum packaging technique for MEMS. Au-In

TLP solder bonding is interesting because it occurs at 200 °C, which is almost 200 °C lower than any other reported wafer-level MEMS vacuum packaging technique. The packaging approach was very similar to the Au-Sn standard solder and Ni-Sn TLP solder bonds reported in the previous sections.

Two double side polished silicon wafers were used to create the packages: one wafer is the silicon cap wafer that will form a cavity for the polysilicon Pirani gauges on the other wafer, the silicon device wafer. After the Pirani gauge fabrication process is complete, a seed layer of 1kÅ Cr / 2.5 kÅ Au is deposited onto both the cap and device wafers. A photoresist layer is patterned on both wafers that will serve as the electroplating mold for the bond ring fabrication. A layer of gold is electroplated into each mold to a thickness of 5 μm to form the bond rings. An extra layer of 2 μm In / 1 kÅ Au is deposited on top of the bond ring mold on the cap wafer. This indium will serve as the interlayer for the Au-In TLP solder bond. Evaporation of the indium was chosen over electroplating due to the processing convenience. Electroplating indium creates a higher quality film compared to evaporation, but it is more difficult to prevent the indium from oxidizing if the indium is deposited by electroplating. Evaporation allows for the deposition of a thin layer of gold directly on top of the indium during the same vacuum cycle. This thin layer of gold prevents the underlying indium from oxidizing and enables a fluxless process. The indium/gold interlayer stack is patterned by sacrificing the bond ring photoresist mold in acetone. Next, both wafers are covered with a layer of photoresist that will protect each bond ring during the subsequent processing steps.

Cap wafer fabrication continues with the patterning of the protective photoresist to a dimension 20 μm wider than bond ring. Next, the seed layer is removed in Au and Cr wet etchants, and then the cap wafer is thinned using DRIE. Nanogetters™ from ISSYS Inc. were chosen as the getter material, which were patterned using liftoff of the bond ring protective photoresist. This completes the fabrication of the silicon cap wafer.

The silicon device wafer's protective photoresist is patterned in the same manner as the cap wafer's, to a dimension of 20 μm wider than the bond ring. The seed layer is removed in Au and Cr wet etchants and then the polysilicon Pirani gauges are released in

a BHF etch for 40 minutes. After the release step, the protective photoresist is removed in acetone, and then the wafer is cleaned in IPA, and left to soak in methanol for 20 minutes. After the methanol soak, the wafer is dried by CPD to prevent stiction from ruining the gauges. Finally, the residue left from the CPD is removed with a 300 W O_2 plasma etch. The cross-section of the wafers directly before bonding is shown in Figure 4.25.
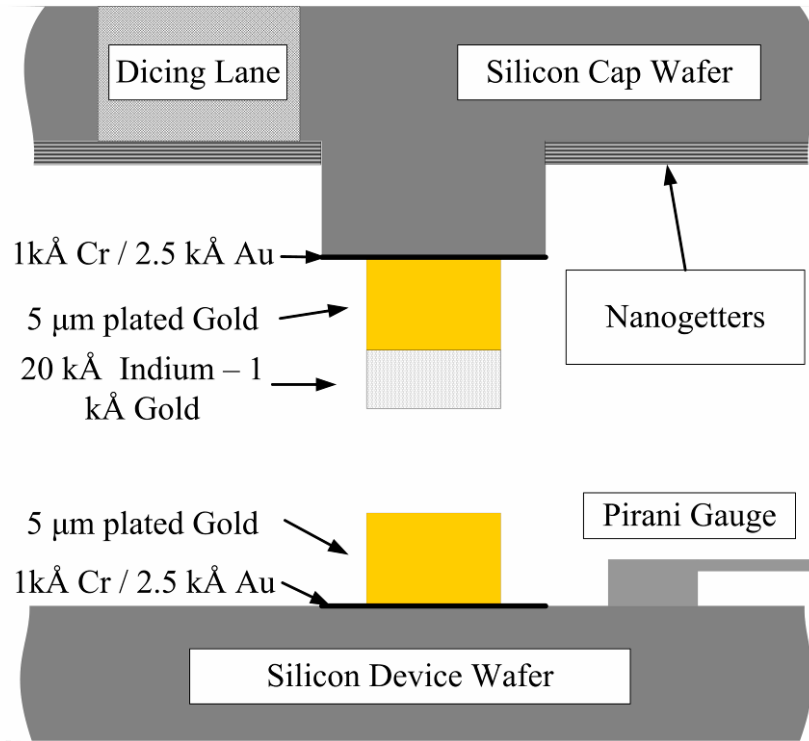
Figure 4.25 Cross-section of the wafers directly before bonding.

The wafers are aligned in a SUSS BA6 and then bonded in a SUSS SB6e. The bond cycle proceeds in the same manner as the two previous bonds; the chamber is pumped to high vacuum (< 10 μTorr) to remove any oxygen and reduce the final pressures inside the package cavities. Once a high vacuum level has been reached, the wafer pair is heated to the bond temperature (200 °C) as rapidly as the system will allow (60 °C/min) to form a quality TLP solder bond without voids. The wafer pair is held at the bond temperature for 1 hour to allow the bond to complete, then the chamber is vented back to atmosphere. Note that the packages are sealed as soon as the temperature passes 156 °C, where the indium melts and flows into any gaps between the bond rings. Normally, the process would be complete after the bond chamber has been vented and the wafers cooled down.

However, an extra getter activation step was included in this bond cycle to forgo activating the getters die-by-die. The complete bond cycle is illustrated in Figure 4.26.
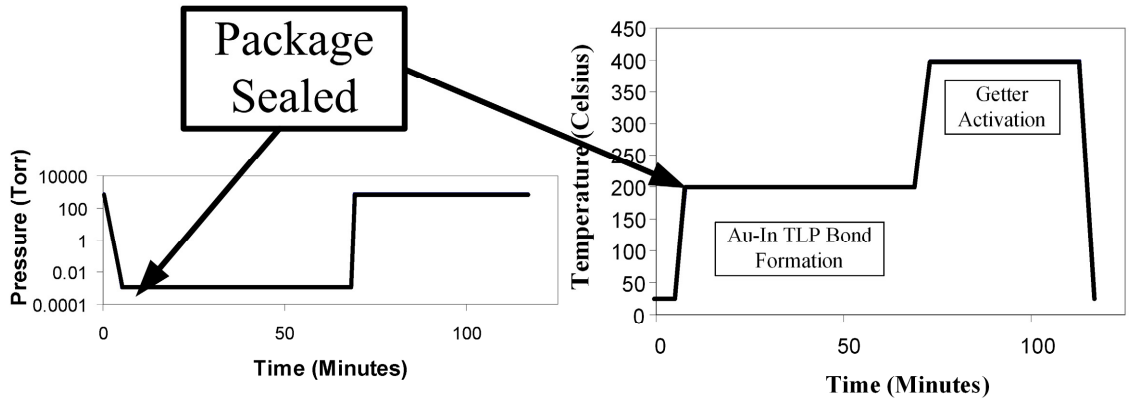
Figure 4.26 Bond cycle for Au-In TLP solder. The package is sealed a few minutes into the vacuum cycle, therefore all the outgassing during the bond cycle is trapped inside the package.

After the bond cycle is completed, the wafers are unloaded and cut with the dicing saw to form the package caps and singulate the wafer into die. The same two-step dicing process as described for the Ni-Sn TLP solder bond was used to form the caps. The dicing saw was also used to cut through one of the packages to take a SEM image of the cross-section (Figure 4.27).
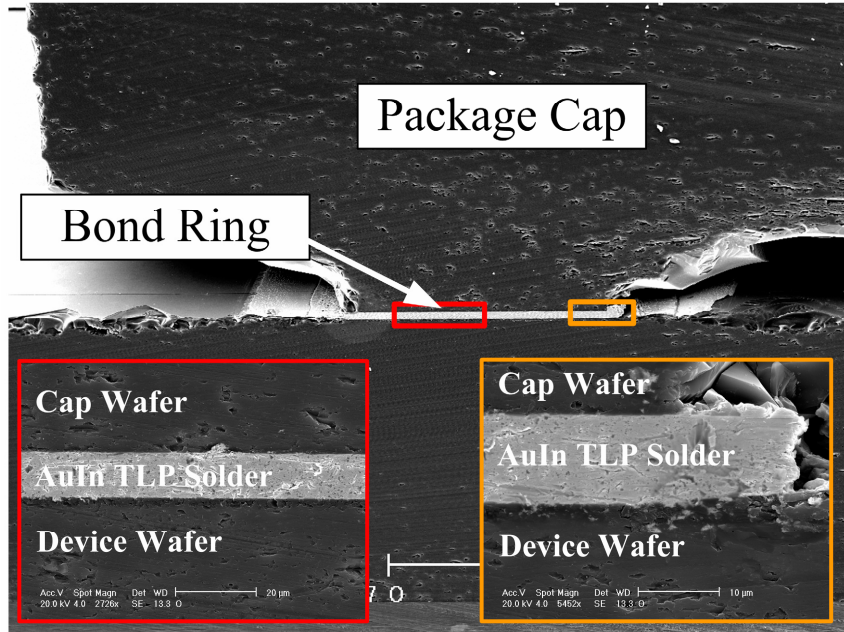
Figure 4.27 SEM image of the Au-In TLP Solder bonded vacuum package.

The SEM image clearly shows the bond ring, recessed package cavity, and device wafer. The insets show a magnified view of parts of the bond ring that indicates that the Au-In TLP solder bond is high-quality and void-free. Several other tests were performed to determine the hermetic, strength, and thermal capabilities of the bonding technology.

Hermetic capability was determined by measuring the polysilicon Pirani gauges over a long period of time. The pressure measurement results are presented in Figure 4.28. The pressure ranges inside the packages varied from several Torr to 200 mTorr. The pressure level ranges for this wafer are much more uniform compared to the Ni-Sn TLP solder, which ranged from 20 Torr to 250 mTorr. It is believed that the extra getter activation step at 400 °C for the Au-In TLP solder bond reduced the magnitude of the range of pressures by pumping out the outgassed molecules.
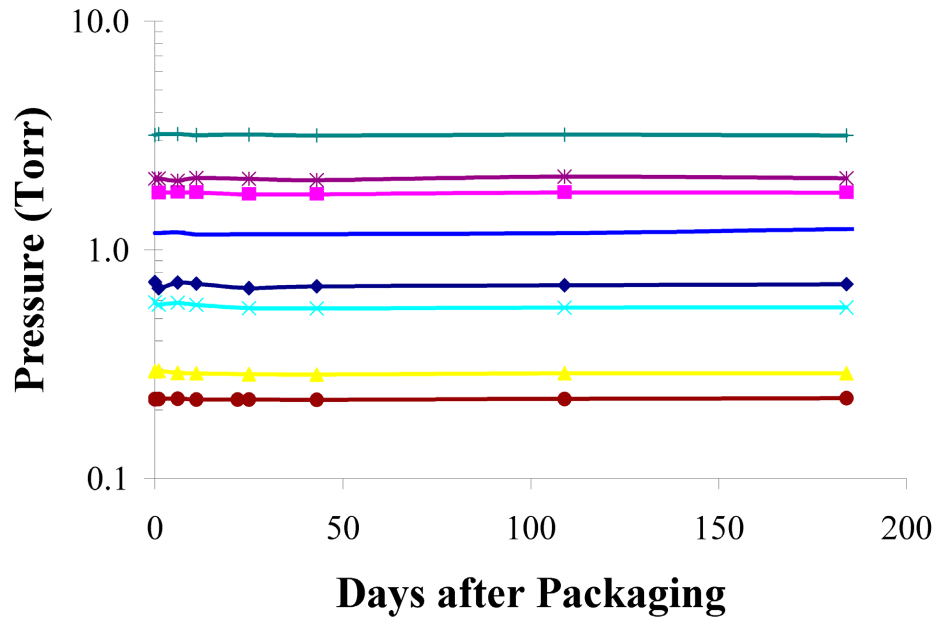
Figure 4.28 Estimated long-term pressure data for the Au-In TLP solder bonded vacuum packages. The pressures ranged from several Torr to 200 mTorr after getter activation.

The hermeticity of the package technique was determined in the same manner as the other bonding techniques. The long-term pressure data from a single die was closely inspected for any leak rate trend. Similar to the other bonding technologies, there was not an observable pressure rise trend for the Au-In TLP solder bond. A worst case estimation of the pressure rise (16 mTorr/year) was fit within the error of the pressure measurement for a single die. This pressure rise corresponds to a leak rate of $9.6^{.}10^{-17}$ atm$^{.}$cc$^{.}$s^{-1} for a package volume of 05 μL.
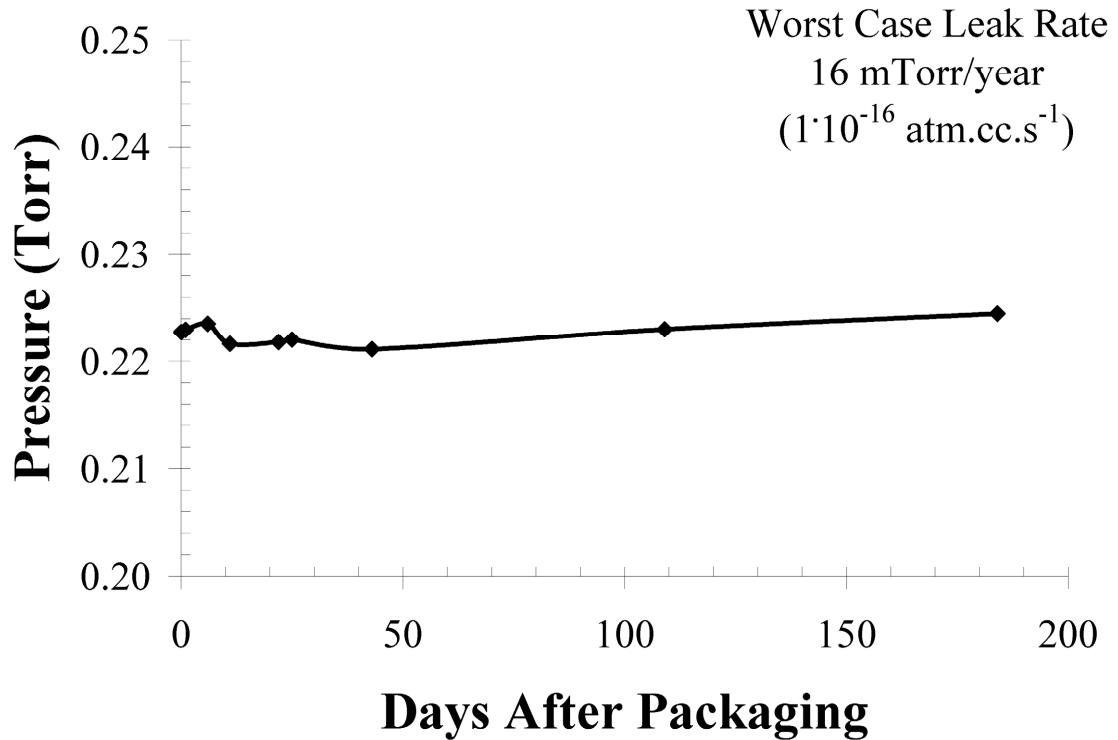
Figure 4.29 Magnified view of a single die from the Au-In TLP solder bonded MEMS vacuum packages. The worst case leak rate that fits within the error of the pressure measurements is 16 mTorr/year ($9.6 \cdot 10^{-17}$ atm·cc·s⁻¹).

The bonding technology was also measured for shear strength and re-melting temperature using techniques described in Sections 3.4.2 and 3.4.3. A summary of the testing results are presented in Table 4.8.

Table 4.9 Summary of data from the tests on Au-In TLP solder bonded packages.

Metric	Test Methodology	Result
Hermeticity	Long-term vacuum data	$1 \cdot 10^{-16}$ atm·cc·s⁻¹
Strength	Average shear strength	24.4 MPa
Re-melting Temperature	Hotplate	> 450 °C

MODIFIED AU-IN TLP SOLDER BOND

All of the bonding techniques featured internal cavities with pressures above 200 mTorr. This minimum pressure might be low enough for some low thermal isolation

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vacuum packaging applications, but it is not low enough for high thermal isolation applications or squeeze-film damping reduction applications. A modification to the Au-In TLP solder bonding process was investigated to reduce this minimum pressure to levels that are useful for a wider range of vacuum packaging applications.

One drawback of all the bonding techniques previously reported is that the packages are sealed at the beginning of the process when the temperature of the wafer exceeds the melting temperature of the solder. At this temperature, the solder melts and flows into any gaps, sealing off the package for the rest of the bond cycle. This negatively impacts the pressure inside the cavity, because by sealing it at the beginning of the cycle, all of the outgassing that occurs during the rest of the cycle is trapped inside the package. This effect is exacerbated by the fact that the outgassing phenomena is highly dependent on temperature, and since the package is sealed at the beginning of the thermal cycle, the majority of the increased outgassing rate is captured inside the package cavity.

The most optimal bond sequence would be one where the wafers are heated to a temperature hotter than the bond temperature *before* they are sealed. This way, the extra outgassing from the rise in temperature would not be trapped in the package, but pumped out of the chamber by the vacuum pump. If the wafers were then cooled down to the bond temperature and sealed, the outgassing rate would be much lower and therefore less gas molecules would be trapped inside the package and have to be pumped out by the getters.

Unfortunately, using this approach is not compatible with TLP solder bonds. If a TLP solder bond were heated past the melting temperature of the interlayer to a temperature that was higher than the bond formation temperature, the bond would be unsuccessful. This is because the interlayer needs to be in contact with the bond ring from the opposite wafer in order to seal the package. If the wafers are not in contact, such that all of the outgassing molecules can be pumped out of the package, then the interlayer is not in contact with the opposite bond ring and cannot seal the package. The result of this approach would be an interlayer that reacted with only one bond ring to form intermetallics.

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Another approach was explored to reduce the pressures inside the package cavities. Instead of heating above the bond temperature then cooling back down to complete the bond, the wafers were held inside a vacuum chamber at high vacuum for an extended period of time to remove a majority of the outgassing molecules. Figure 4.30 shows the bond cycle that was used for this experiment. The wafers sat at < 10 μTorr for 24 hours before heated up to the bond temperature.
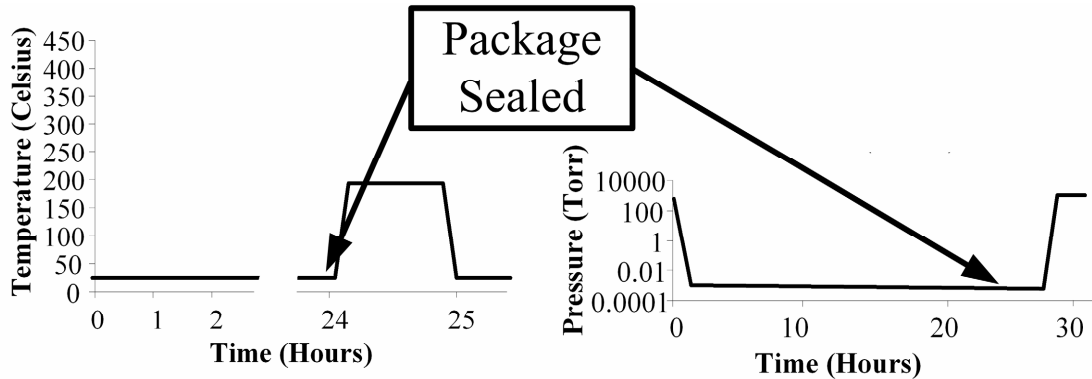
Figure 4.30 Modified Au-In TLP solder bond cycle. The package sits in a vacuum environment for 24 hours before the bond is performed. This results in a much lower pressure inside the packages due to the reduction in the outgassing rate.

The Au-In TLP solder bond was integrated with platinum Pirani gauges to use this bond cycle as a method for reducing the final pressures inside the packages. The package processing for this experiment is exactly the same as the polysilicon process. The major difference is in the Pirani gauge release. Instead of using oxide as a sacrificial layer for the Pirani gauges, the silicon wafer itself served as the sacrificial material. Therefore, the release of the Pirani gauges was performed with XeF_2 silicon etching instead of BHF. XeF_2 is an attractive release technique because it is a dry process and therefore does not suffer from the stiction issues that plague wet release processes. Once the release process is finished, the cross-section of the wafers is exactly the same as that depicted in Figure 4.26. The wafers are bonded using the bond cycle in Figure 4.30. After bonding, the wafers are diced with the two pass process to create the wafer depicted in Figure 4.31.
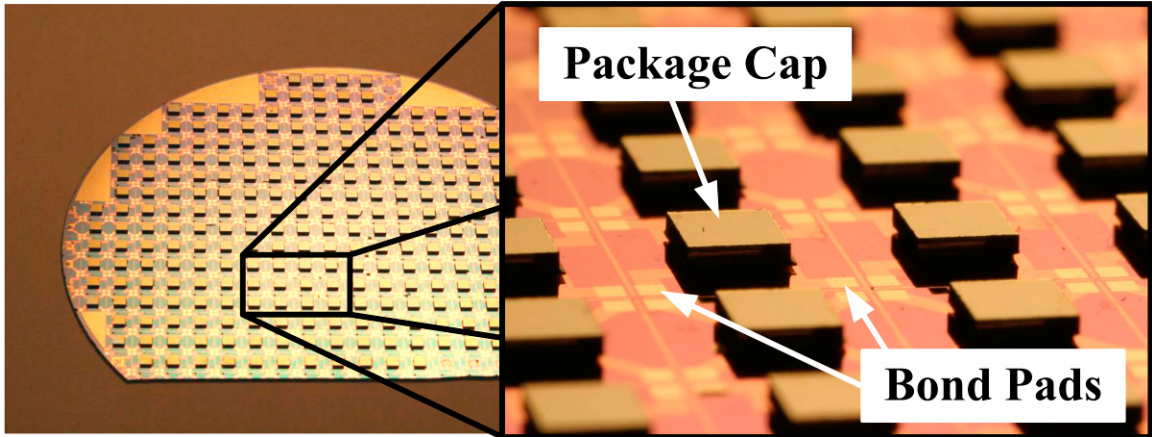
Figure 4.31 Picture of the completed Au-In TLP solder bonded wafer with a magnified view inset.

The pressures inside the cavities were monitored by the platinum Pirani gauges. The internal pressures *for the packages with inactivated getters* varied from several Torr to 200 mTorr. The resulting pressures were much lower than those reported for bond cycles where there is not extended outgassing period before bonding. The pressures were stable for several days before the getters were activated.
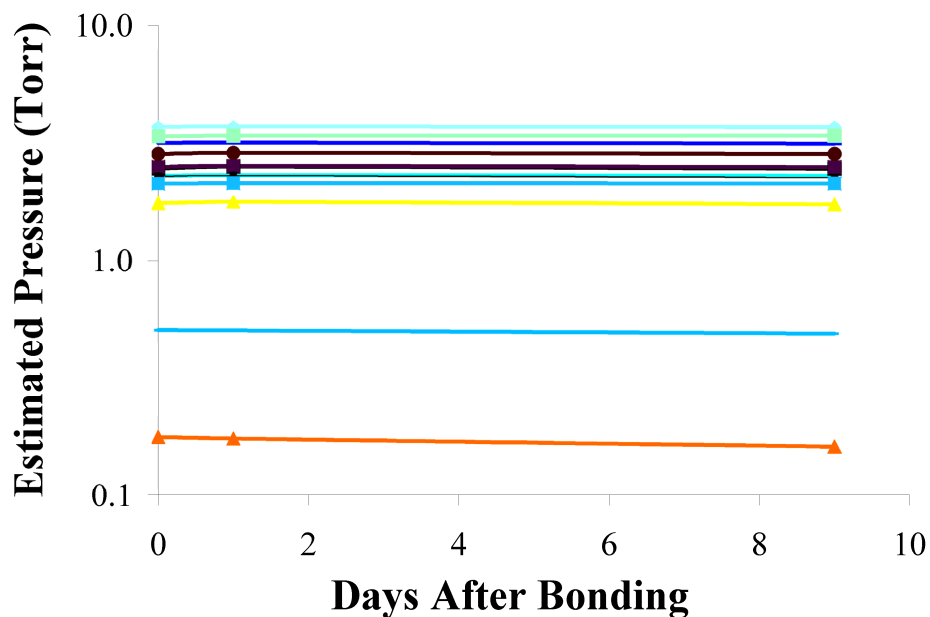
Figure 4.32 Pressure data from the modified Au-In TLP solder bond sequence. The 24 hours at vacuum reduced the outgassing rate, such that the pressures before the titanium getters were activated are the same as the previous wafer after the getters had been activated.

One of the interesting aspects of Au-In TLP bonding is that the low temperature allows for the measurement of the pressures inside the packages before the getter has been appreciably activated. The activation of the titanium getter was studied at various temperatures and times with some interesting results that are presented in the next section. The final results of the getter activation experiments are presented in summary form in Figure 4.33. The reduction of the pressure from before and after getter activation was very similar for each die, in that the ratio of pre-activation pressure over post-activation pressure was greater than, but close to 10. This means that the getters pumped over 90% of the gas molecules left in the package after bonding. A more detailed explanation and analysis of the getter activation is presented in Section 4.4.3.
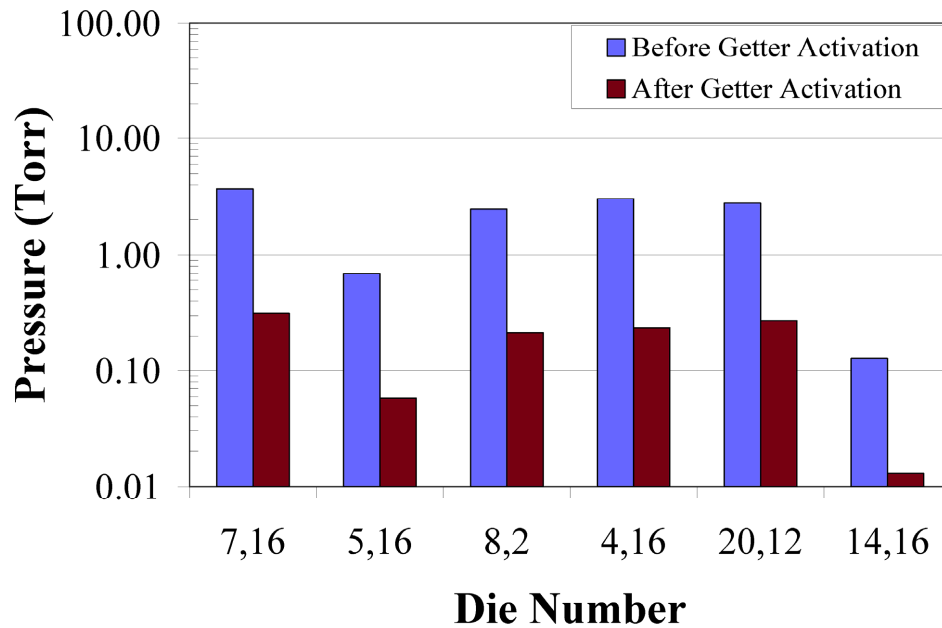
Figure 4.33 Pressures for various die from the modified Au-In TLP solder-bonded packages before and after getter activation on a log scale plot. The extended outgassing sequence at high vacuum for 24 hours before bonding resulted in an internal pressure of less than 20 mTorr after getter activation.

The extended outgassing step at high vacuum resulted in much lower post-activation pressures, as expected from outgassing theory. The final pressures were all below 500 mTorr and some even well below 100 mTorr. The lowest pressure, 20 mTorr, is low enough for most thermal isolation applications and is beginning to become useful for

reducing squeeze film damping, especially if the resonant structure has small gaps and a high resonant frequency.

The long outgassing step that precedes the bonding portion of the bond cycle is an obstacle if this technique is to be used in a production level wafer bonding process. There are several methods that could be used to reduce the amount of time that needs to be spent outgassing the wafers before they are bonded. The first is to raise the temperature of the wafers close to the bonding temperature before they are bonded. The extra thermal energy would increase the initial outgassing, and thus deplete the amount of adsorbed and absorbed gas molecules, which would reduce the outgassing rate much faster than if the wafer remained at room temperature. This could be performed with a bonding technique like Au-Sn solder with little issue. However, this would be a tricky method to implement with TLP solder boding since the increased temperature would also cause the interlayer to react with the parent metal and form IMC. This initial heating cycle would increase the critical interlayer thickness for producing void-free bonds. Other methods that are more compatible with TLP solder bonding, include photo-stimulated desorption, plasma assisted desorption, and electron stimulated desorption.

4.4.3 Titanium Getter Activation

TLP solder bonds offer a unique advantage that allows more information to be collected from the MEMS vacuum packaging process. Since TLP solder bonds can withstand higher temperatures than their formation temperature, the packages can be sealed without fully activating the getters. This allows a measurement of the pressure inside the cavity *before* the getters are activated. Taking a measurement before and after the getters are activated reveals more information on the getter activation process as it applies to MEMS vacuum packaging.

The titanium getters used inside the Ni-Sn TLP solder packages were tested. After the bonding process was finished, the getters inside the packages had been exposed to a temperature of 300 °C for an hour during the bond sequence. Several packages were measured for 5 days to establish a baseline pressure, and then the packages were heated to a higher temperature than the bond temperature to activate the getters. The packages

were placed on a hotplate and heated to 400 °C for 5 minutes, then allowed to cool slowly to room temperature and then the pressure was monitored over a long period. The pressures inside the cavities are plotted in Figure 4.34. The extra thermal energy caused the gas molecules adsorbed on the surface of the titanium getter to diffuse into the bulk, which freed more capture sites on the surface of the film to capture more gas molecules. The pumping action reduced the pressures inside the cavities by approximately a factor of 5. This is the first example of an in-situ measurement of the thin-film getter effect in MEMS vacuum packages.
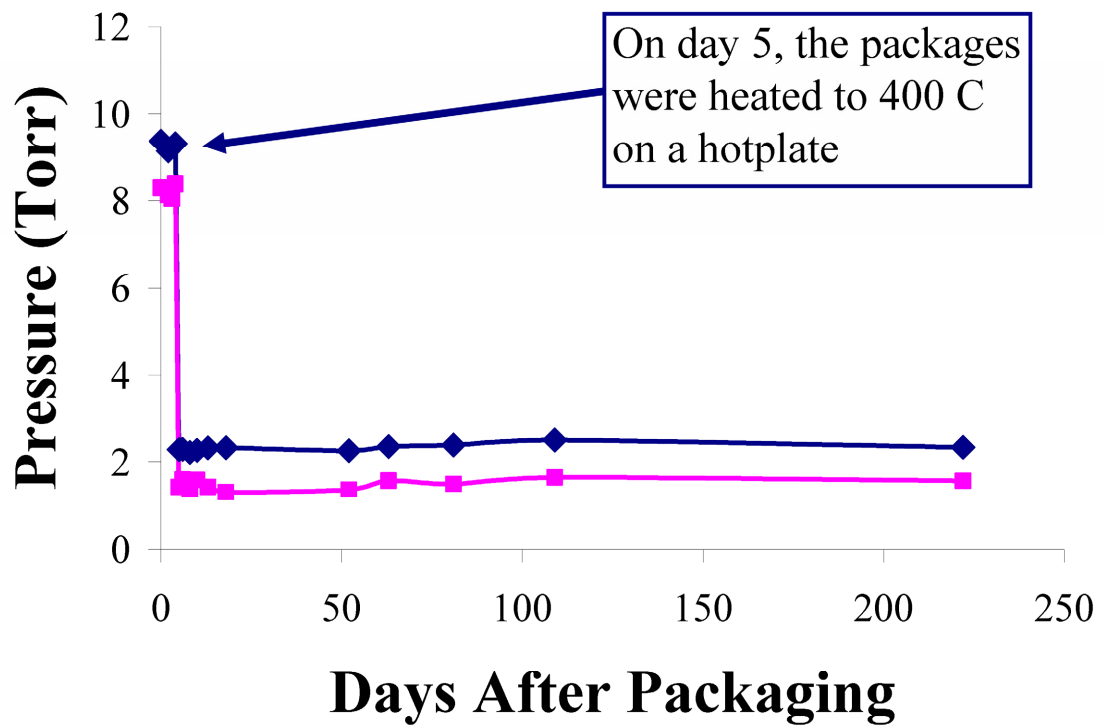
Figure 4.34 Activation of titanium getters with a Ni-Sn TLP solder bond. The packages were heated to 400 °C on day 5, which activated the getters and dropped the pressure by a factor of 5.

A similar experiment was conducted with the modified Au-In TLP solder bond. However, for this experiment the temperature of the getter activation step was also varied. Instead of activating the getters at only 400 °C, cooler temperatures of 200 °C and 300 °C were also used to activate the titanium getters.

The lower temperature of the Au-In TLP solder bonding process allows more temperature information about the getter activation process to be collected. Since the maximum bond temperature for the Au-In TLP is 200 °C instead of 300 °C, the getters are less activated at the end of the bond cycle. To study the effects of the getter activation, the pressures in several packages were measured, then the getters activated at temperatures of 200 °C, 300 °C, and 400 °C for different time intervals with pressure measurements between each activation step. The results are shown in Figure 4.35.
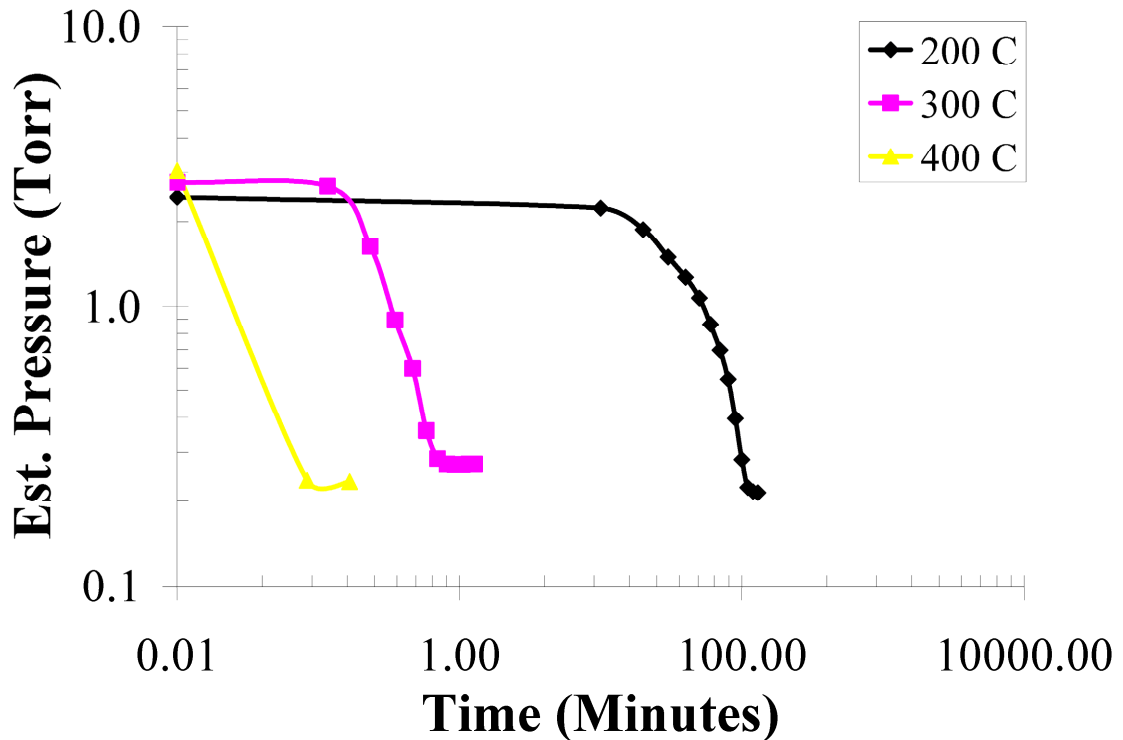
Figure 4.35 Plot of pressure versus activation time for titanium getters. Titanium getters can be activated at temperatures as low as 200 °C, although the activation time increases substantially for lower temperature activation.

Several interesting conclusions can be drawn from this getter activation step. First and most applicable to this work, is that titanium getters can pump with activation temperatures as low as 200 °C, which is 200 °C lower than previous reported temperatures [81] and 100 °C lower than recommended activation temperatures of other more exotic getter alloys [105]. This is very important for low-temperature vacuum packaging because even though it was shown that good hermetic seals could be created at

low temperatures with the Au-In TLP solder bond, the maximum temperature would have been dictated by the getter activation temperature, which was reported as 200 °C hotter than the bond temperature. By demonstrating that titanium getters are able to pump out 90% of the gaseous molecules inside a package in a reasonable amount of time, it is feasible to keep the maximum temperature for the entire packaging process at or below 200 °C. This activation procedure is compatible with a production environment since only heat is needed to activate the getters; even if it takes 2 hours per wafer, an entire lot (25 wafers) could be loaded in an oven at once to activate the getters on all wafers at the same time. This reduces the per wafer getter activation time to under 6 minutes.

It is unclear what determines the minimum pressure that can be produced by the titanium getter pumping. For all of the activations, regardless of the temperature, the getter could only pump approximately 90% of the gas from the packages. There could be a couple of reasons why the getters stop pumping.

One possibility is that the getter film could be completely saturated, meaning that all of the titanium atoms reacted with gaseous molecules leaving no more open sites for reaction. A quick calculation shows that this is unlikely: the titanium getter film is 1000 μm by 1000 μm by 2 μm, giving it a volume of $2 \cdot 10^6$ μm^3. Titanium has a molecular density of $9.4 \cdot 10^{-2}$ mol.g^{-1}, which means there are $1.13 \cdot 10^{17}$ titanium molecules in the getter film. If we assume that the product of oxygen gettering is titanium dioxide the 100% oxygen capacity of the getter film is $2.27 \cdot 10^{17}$ atoms. For a 0.5 μL package volume at standard temperature and pressure, this corresponds to well over 1 atmosphere of oxygen. This makes getter saturation an unlikely cause of the minimum pressure.

Another more likely reason is that there is a gas, or combination of gasses, that cannot be pumped by the titanium getter. All the noble gases, helium, argon, krypton, etc. are difficult to pump with getter films. Hydrogen is also difficult to permanently capture with getter films. Measurements of the gasses trapped inside the packages with a mass spectrometer would shed more light on this subject.

Chapter 5

TRANSFERRED THIN-FILM PACKAGES WITH A SOLDER TRANSFER LAYER

Aside from two bonding techniques, the unique behavior of solder can be used as a novel transfer method [106]. With the understanding of wetting and intermetallic formation, a solder joint can be designed between a structure and a wafer that will get weaker as the bonding process occurs. At the same time, one of the bonding techniques mentioned previously can be used to strengthen a bond between the structure and another wafer, such as a standard solder bond or a TLP solder bond. During the bond cycle, the structure becomes weakly attached to one wafer while strongly attached the other wafer. When the wafers are separated, the structure is transferred from one wafer to another. The weakening process is described in Section 5.1 and a process to create a transferred thin-film packaging solution is presented in Section 5.2.

5.1 Solder as a Transfer Material

The bond weakens when the solder dewets the surface it was well attached to previously. This can be accomplished by using an under bump metallization that is designed to be consumed by the solder during the bonding process. When the thin film is completely consumed, the underlying material is exposed to the molten solder. If the underlying material has a low surface tension, the solder balls up and dewets the surface (See Figure 5.1). Two conditions must be satisfied for the bond to weaken: 1) the solder must completely consume the under bump metallization; 2) the underlying surface must have a low surface tension.
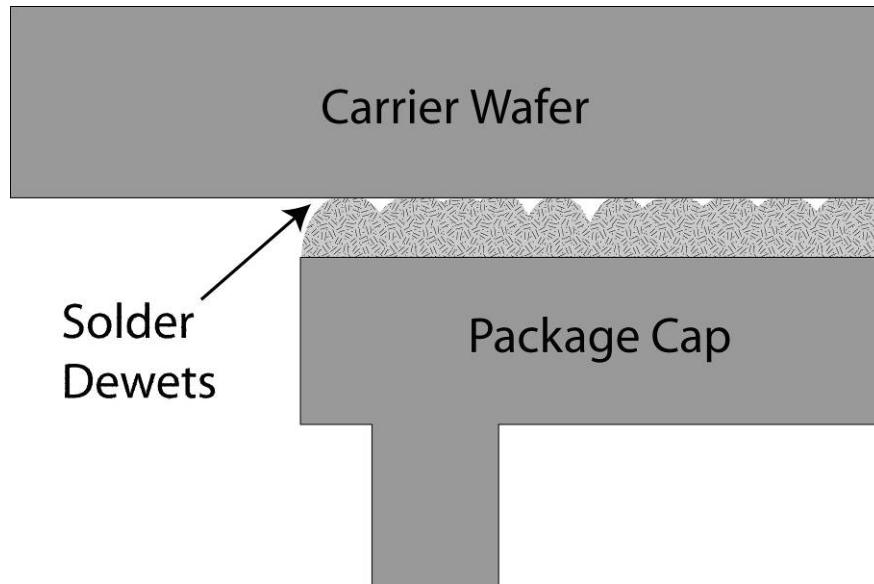
Figure 5.1 Illustration of the solder transfer process. The solder consumes the seed layer it was electroplated on, and then dewets the carrier wafer.

These requirements are simple to satisfy with a silicon wafer, a thin-film deposition tool, and two electroplating baths. First, a thin film of titanium-gold is deposited onto the silicon wafer. Gold is a good choice for this thin film because it is rapidly consumed by most solder alloys due to their high tin content. A photoresist mold is then patterned that will form the transferred structures. Next, a thin layer of the transfer solder is electroplated into the mold. The solder must be thick enough to consume the thin layer underneath it, but not too thick that it will affect the mechanical properties of the structural layer. Next, the structural material is electroplated directly onto the solder. The structure can be as thick as the electroplating mold will allow. The solder layer must be compatible with the structural electroplating bath. If not, the solder must be covered with another thin film that is compatible with the bath chemistry. This somewhat complicates the process, but is necessary to maintain the operability of the structural electroplating bath. Finally, the photoresist is removed and the structures are bonded and transferred to another substrate. This process was used to create transferred thin-film packages.

5.2 Wafer-Level Packaging with Transferred Thin-Film Packages

As mentioned in the introduction, there are several general packaging approaches that can create wafer-level vacuum packages. The transferred thin-film approach combines

the modularity of a wafer-bonded package with the low-profile of a thin-film package approach. This combination of modularity and low-profile is particularly advantageous for packaging steps that are early in the packaging and assembly process (Level 0 or Level 1). The previous approaches for transferred thin-film packaging are presented below.

5.2.1 Previous Transferred Thin-Film Packaging Approaches

Maharbiz created a thin-film package out of LPCVD polysilicon and transferred it with a room temperature thermocompression bond [19]. The polysilicon was deposited over a PSG sacrificial layer and then gold tethers were electroplated overtop of the poly. Next, the PSG was sacrificed in HF and only the tethers held the poly thin film in place. The device wafer contained a sealing ring of gold electroplated around the resonators. The gold tethers and gold bond ring were attached by thermocompression bonding to form the seal. The vacuum level was verified by the deflection of the thin-film layers. This approach is a good demonstration of the feasibility of transferred thin film packaging, but it leaves additional investigation. The research lacked proof that the vacuum level inside the cavity is sufficient for most MEMS vacuum packaging needs and the long-term reliability was not measured. The thickness of the poly cap is also limited by the deposition rate of the LPCVD furnace to a couple of microns. More expensive processes, such as epitaxial reactors, can be used to create thicker caps with this process, but other cheaper means are available. Also, the particles left over from breaking the gold tethers during the transfer process could cause contamination issues in large volume manufacturing processes.

Pan used electroplating, a cheaper alternative to high temperature furnaces, to create thin-film packages out of nickel and transferred them with a polymer bond [107]. The transfer technique was a novel approach based on a passivated nickel seed layer. The seed layer for the electroplating was deposited by evaporation and then heated inside an oven with a specific temperature profile. The heating cycle passivated the seed layer by forming a layer of nickel oxide. This oxide weakens the adhesion between the electroplated nickel and the seed layer. The caps were transferred to a device wafer by a

photoresist bond. The weakened adhesion between the electroplated cap and its seed layer makes it easy to transfer the caps from the carrier wafer to the device wafer. This technique showcases a unique transfer method that could solve many MEMS packaging problems, but it could not be used for vacuum packaging applications. The permeability of polymers is much too high to serve as a good gas barrier at micron dimensions (Figure 1.9). Only a metal, or possibly a glass bond, can provide the permeability barrier necessary for vacuum packaging at the micro scale. A transferred thin-film packaging process that combines electroplated packages with a metal seal bond is presented in the next section.

5.2.2 Process Flow for Solder Transferred Thin-Film Packaging

Fabrication begins on the carrier wafer by evaporating a thin titanium (50 Å) – gold (500 Å) electroplating seed layer (see Figure 5.2). Gold is used for the seed layer because it is rapidly dissolved by tin-based solders and it does not oxidize, making it easy to electroplate other materials on top. The lead-tin or pure-tin sacrificial solder is electroplated onto this seed layer into a photoresist mold. Next, the nickel cap is formed directly on the sacrificial solder by electroplating into the same photoresist mold. After the lid is formed, more photoresist is spun on top of the old resist and the package rim is defined by photolithography. The nickel oxide that formed on the cap is removed in a diluted HCl solution before electroplating the rim to ensure good adhesion. This completes the fabrication on the carrier wafer.
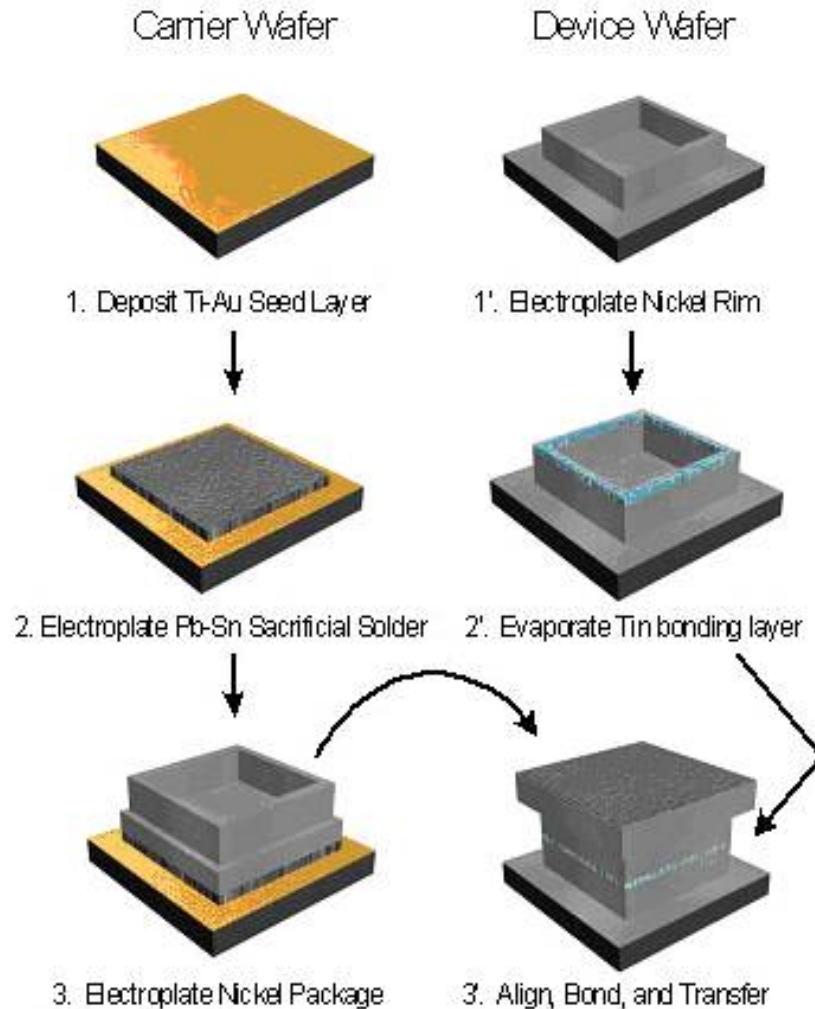
Figure 5.2 Illustration of the process flow for transferred thin-film packaging with a novel solder transfer technique.

The device wafer fabrication starts with the deposition of a titanium (300 Å) – nickel (1500 Å) seed layer. A photoresist mold is created on top of the seed layer to define a bond ring around the device. A dip in diluted HCl removes the nickel oxide from the seed layer before electroplating to ensure good deposit adhesion. After the bond ring is electroplated, a layer of tin (1.5 μm) is evaporated or electroplated onto the wafer. The evaporated tin is patterned by sacrificing the electroplating mold, thereby removing the tin from the entire wafer except for the top of the bond rings. The electroplated tin is patterned by the photoresist mold as it is deposited.

Finally, the wafers are aligned and bonded in a SUSS SB-6 wafer bonder. The wafers

are loaded and the chamber is pumped down to vacuum (~5 µTorr) then heated to 300 °C. After 1 hour, the wafers are allowed to cool to 50°C under vacuum then the chamber is vented and the wafers removed.

After bonding, the carrier wafer and device wafer are weakly bound together by the sacrificial solder and package cap. This bond is easily broken with the tip of a razor blade and the top wafer removed leaving the caps bonded to the device wafer.

5.2.3 Package Results

Two different runs were tried with two different transfer layers and interlayer deposition techniques. The first was a lead-tin transfer layer with an evaporated tin interlayer. The second was a pure-tin transfer layer and electroplated tin interlayer.

LEAD-TIN TRANSFER LAYER AND EVAPORATED TIN INTERLAYER

The process was run with two different substrates for the device wafer: Pyrex™ and silicon. The transferred and non-transferred caps were counted after bonding to measure the yield. In each case, the yield was greater than 99%. The yield was slightly lower with Pyrex™ as the device wafer (1192 out of 1200 caps transferred) vs. silicon (1200 out of 1200 caps transferred). This could be accounted for by the slight thermal mismatch between silicon and Pyrex™. A picture of a silicon substrate with transferred caps is shown in Figure 5.3.
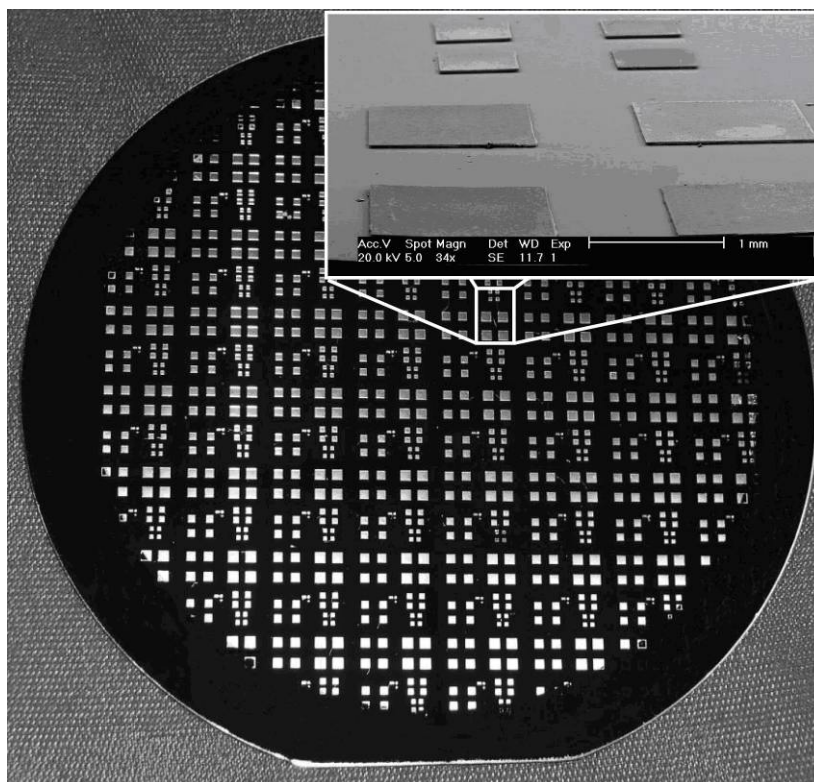
Figure 5.3 Silicon substrate full of transferred thin-film packages.

SEM images were taken of the profile of the transferred thin-film packages (Figure 5.4).
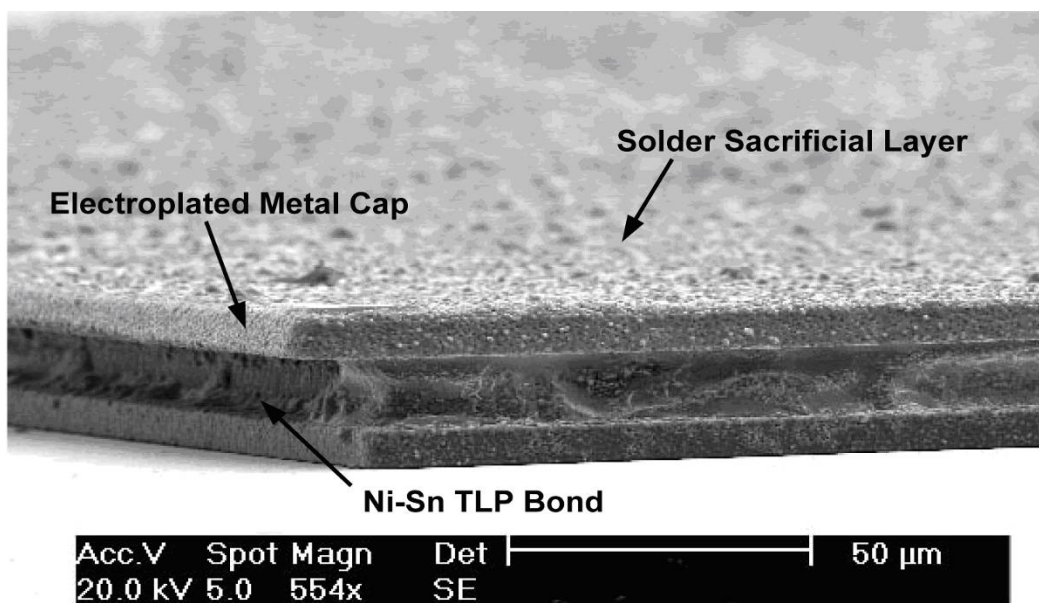
Figure 5.4 SEM image of the profile of a transferred thin-film package.

After bonding, the Ni-Sn TLP solder bond composition was analyzed in a scanning electron microscope with energy dispersive spectroscopy capabilities. A picture of the bond and the varying composition is shown in Figure 5.5. The formation of intermetallics was confirmed by the changing ratio of nickel to tin across the interface. The nickel composition starts at 97% on the top, and then goes to about 50% nickel / 50% tin near the bond joint, then goes back to 96% on the bottom.
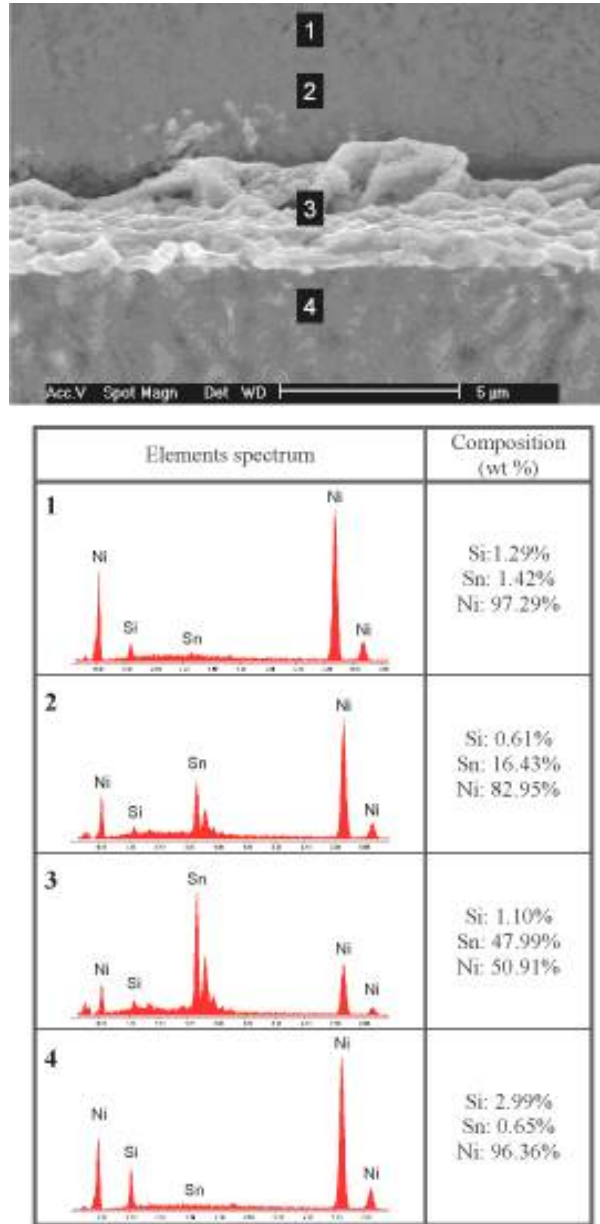
Figure 5.5 Magnified view of the Ni-Sn TLP bond and EDAX elemental analysis across the bond joint.

The thickness of the TLP low melting point interlayer and heating rate play an important role in the planarization capabilities mentioned previously in Section 3.5.2. If the interlayer is too thin or the heating rate is too low, the low melting point interlayer can be consumed by the parent metal before it transforms into a liquid phase. The intermetallic formation reaction between the parent metal and interlayer can be rapid enough at low temperatures to completely consume a thin interlayer before it can melt. The interlayer thickness becomes the most important parameter in vacuum bonding applications because it is difficult to increase the heating rate with such high thermal isolation between materials at low pressures. Without air molecules to conduct the heat from the bonding chuck to the wafers, it takes time to heat up the wafers for bonding. The thickness of the interlayer must be increased to better planarize the bond interface. In this process, the interlayer was evaporated onto the bond ring on the device wafer. The maximum allowable thickness was limited to 2 μm by the size of the crucible in the deposition system. For the next experiment, electroplating was used to deposit the interlayer, which does not suffer from such small thickness limitations.

The selection of the solder used for the transfer layer is a critical part of the package design. This solder defines the seed layer that is needed and the package materials that are available to ensure a reliable transfer. The solder must dissolve the seed layer much faster than the package material for a successful transfer. The solder layer must also serve as an electroplating seed layer for the package material, therefore it becomes part of the final package. It completely consumes the seed layer and transfers, along with the package, to the device wafer and forms the outer surface of the completed package. To comply with much of the pending legislation banning the use of lead in electronic components, a lead-free process is presented in the next sub-section.

PURE-TIN SOLDER TRANSFER LAYER AND ELECTROPLATED TIN INTERLAYER

Another process using the same general solder transfer technique was performed. But instead of a lead-tin solder transfer layer and evaporated tin interlayer, the second process used a lead-free, pure-tin solder transfer layer and a thicker electroplated tin interlayer. The process flow remained exactly the same for the second packaging approach, save for

the solder transfer deposition and interlayer deposition. For the lead-free process, the solder transfer layer was electroplated pure-tin deposited to a thickness of 2 μm and the interlayer was electroplated tin deposited to a thickness of 2 μm on both the rims on the package cap and bond rings on the device wafer. A SEM image of the transferred caps is shown in Figure 5.6.
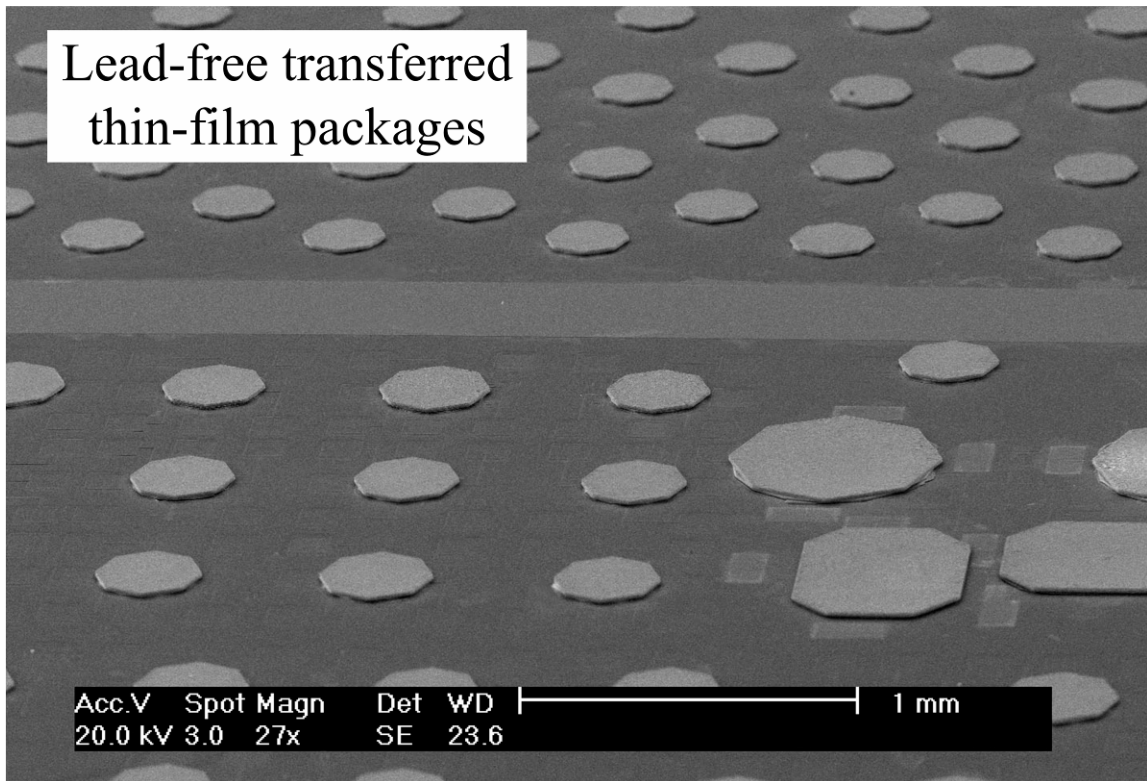
Figure 5.6 SEM image of lead-free transferred thin-film packages.

The caps were transferred to a device wafer filled with disc resonators. Figure 5.7 shows a SEM image of a de-capped package with a disc resonator inside.
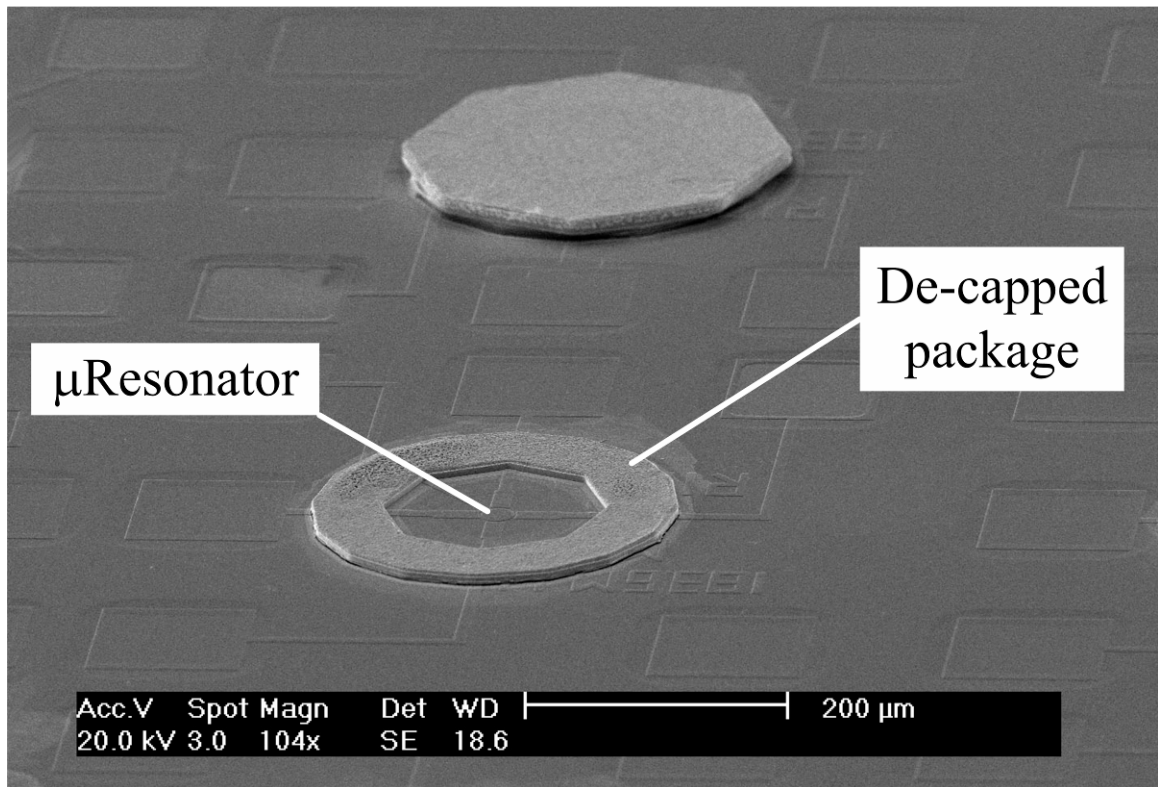
Figure 5.7 Magnified view of a transferred thin-film package and a de-capped package showing a μ-disk resonator inside.

This process demonstrates that the transferred thin-film process can comply with worldwide legislation banning the use of lead in electronics products.

5.2.4 Design Guidelines for Solder-Transferred Thin-Film Packages

There are several limits to the design of the transferred thin-film package dimensions that are imposed by the geometry of the packages and the process parameters. The ratio of the transfer to bond force, stress from CTE mismatch, and ambient pressure force on the cap will all limit the maximum size of the transferred thin-film cap.

A transfer yield of over 99% as shown in the previous data indicates that the solder dewetting results in a large reduction in the adhesive force between the package caps and carrier wafer. The adhesion between the package cap and carrier wafer was much smaller than the tensile strength of the bond rings for the package caps for the size of the caps that were transferred in the experiments. However, as the packages get larger, the adhesion between the package cap and carrier wafer does not scale the same as the tensile

strength of the bond rings. Therefore there may be issues when using large transferred caps because the adhesion force between the package cap and wafer could be comparable to the bond rings since they do not scale at the same rate. This would impose an upper limit on the size of caps that could be transferred using this method. However, other effects, such as the force from the pressure difference across the caps, will impose more strict size limits.

The stress from the differences in the thermal coefficient of expansions (TCE) for the package caps and silicon substrate is an important effect that dictates the choice of materials and bond parameters.
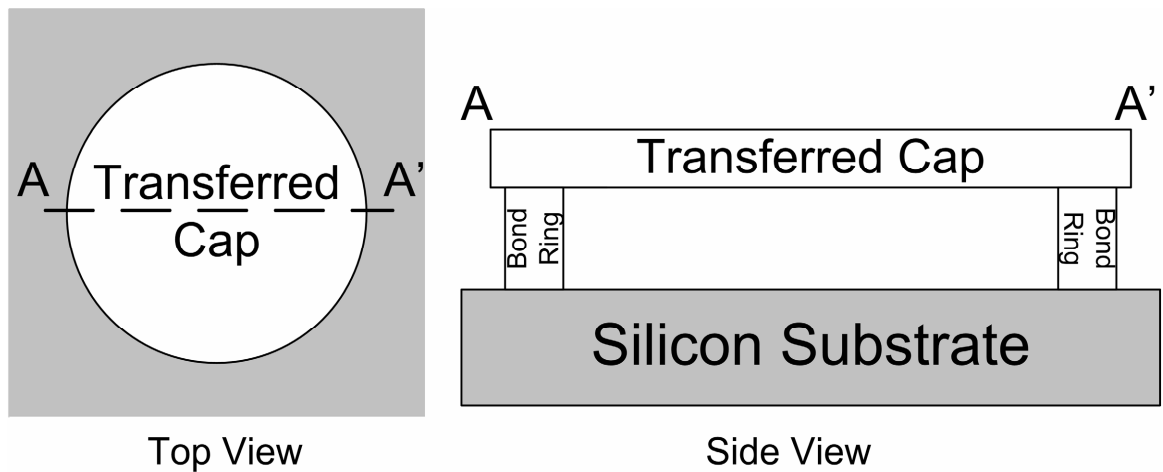
Figure 5.8 Illustration of the top view and side view of a transferred cap.

Figure 5.8 is an illustration of the top and side view of a transferred cap. The stress in the package cap from TCE mismatch between the package cap and wafer materials can be calculated from Equation 5.1:

$$\sigma_{cap} = E \cdot \left(T_{bond} - 23\,K\right)\left(\alpha_{cap} - \alpha_{wafer}\right) \qquad (5.1)$$

Where σ_{cap} is the cap stress, E is the Young's Modulus of the package cap, T_{bond} is the bond temperature, α_{cap} is the TCE of the cap material, and α_{wafer} is the TCE of the silicon wafer. This stress will result in a shear force at the bond ring given by Equation 5.2:

$$F_{shear} = \sigma_{cap} \cdot 2\pi \cdot d \cdot t \qquad (5.2)$$

Where F_{shear} is the shear force, d is the circular cap diameter, and t is the thickness. The force is calculated by multiplying the package cap stress by the area of the edge face of the cylindrical cap. This shear force will result in a shear stress on the bond rings given by Equation 5.3:

$$\sigma_{shear} = \frac{F_{shear}}{\text{Bond Ring Area}} = \frac{F_{shear}}{\dfrac{\pi\left(d^2 - (d-w)^2\right)}{4}} = \frac{E \cdot (T_{bond} - 23\,K)(\alpha_{cap} - \alpha_{wafer}) \cdot 8 \cdot d \cdot t}{(2dw + w^2)} \qquad (5.3)$$

Where w is the width of the bond rings. If the shear stress from the CTE mismatch exceeds the shear strength of the bonding technique used to attach the package caps to the substrate, then the CTE mismatch stress will break the bond. Figure 5.9 shows calculated shear stress for package caps made of nickel and gold that are 10 μm thick, have bond rings 50 μm wide, and are bonded at 200 °C and 300 °C:
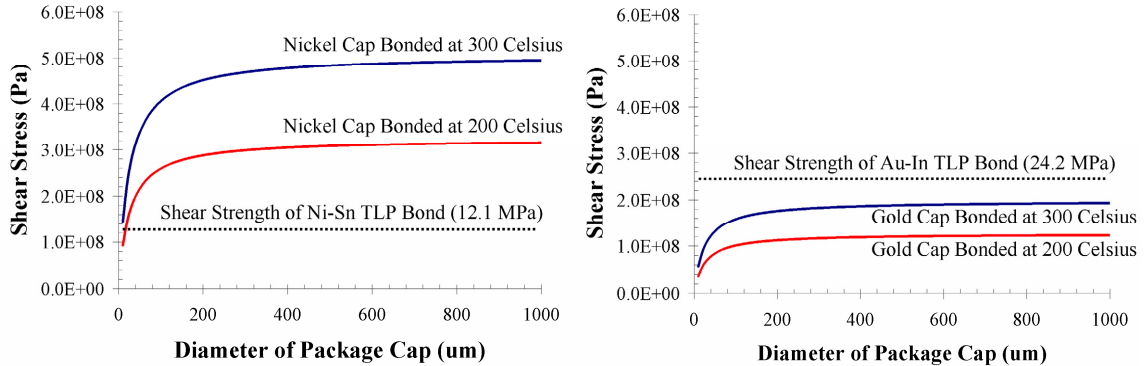
Figure 5.9 Calculated shear stress from CTE mismatch for gold and nickel package caps that are 10 μm thick, with 50 μm bond rings. If the shear stress exceeds the bond strength, the package caps will fail.

The dotted line on each plot indicates the measured shear strength of the Ni-Sn TLP solder bond technique for the nickel cap plot and Au-In TLP solder bond technique for the gold cap plot. The shear stress put on the bond ring is much lower for the gold package caps because gold has a much lower Young's modulus than nickel.

The nickel package cap and a Ni-Sn TLP solder bond were poor material choices for

the transferred thin-film package process. The packages would have to be smaller than 10 μm in diameter to reduce the CTE mismatch shear stress below the shear strength of the Ni-Sn TLP solder bonding technique. Gold package caps and the Au-In TLP solder bond are much better choices due to the lower Young's modulus of gold and larger shear strength of the Au-In TLP solder bonding technique. For cap thicknesses of 10 μm, the shear strength of the Au-In TLP solder technique is larger than the CTE mismatch stress for any size cap up to and even larger than 1 mm in diameter. Since the CTE mismatch stress scales linearly with package cap thickness, the thickness of the gold package caps bonded at 200 °C could be increased to 20 μm without exceeding the shear strength of the Au-In TLP solder bond. For a gold package cap and Au-In TLP solder bond, the CTE mismatch stress would not limit the maximum size of the package caps.

The biggest factor that limits the scaling of the transferred package caps is the deflection caused by the pressure difference across the cap. For a clamped circular diaphragm the maximum deflection is given by Equation 5.4:

$$w_{max} = \frac{P \cdot r^4 \cdot 12(1 - v^2)}{64 \cdot E \cdot t^3} \tag{5.4}$$

Where w_{max} is the maximum deflection in μm, P is the pressure in Pa, r is the radius in μm, v is Poisson's ratio for the package cap material, E is Young's modulus in Pa for the package cap material, t is the package cap thickness. The practical maximum thickness for a transferred gold cap is 20 μm due to the shear stress limitations discussed in the previous paragraph. The maximum deflection calculation for a gold cap of this thickness and other smaller thicknesses are shown in Figure 5.10.
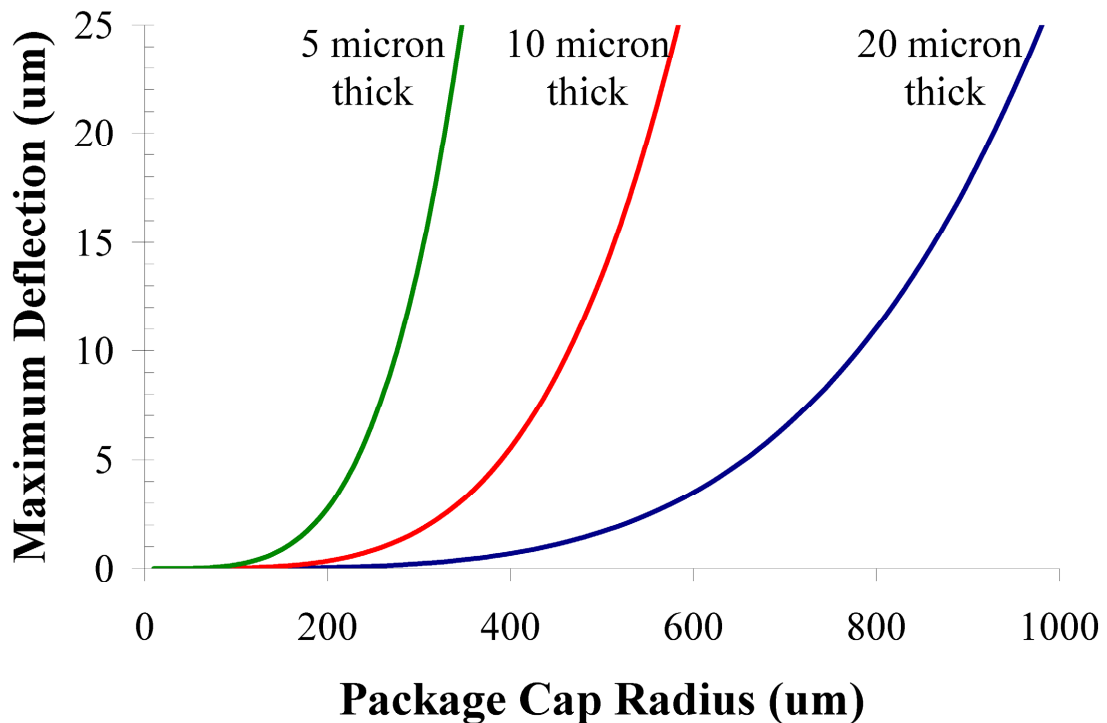
Figure 5.10 The maximum deflection for 5, 10, and 20 μm thick gold transferred thin-film caps.

The plot in Figure 5.10 indicates that for a tolerable maximum deflection of 1 μm, the cap can have a radius of no larger than ~ 160 μm, 270 μm, and 440 μm for a cap thickness of 5 μm, 10 μm, and 20 μm respectively. If larger cap sizes are needed, it is possible to tolerate larger maximum deflections by increasing the thickness of the bond rings such that the center deflection does not impede the movement of the MEMS inside the package.

There are several aspects of the transferred thin-film cap geometry that will limit the material choice and scalability of this packaging technique. Gold package caps and a Au-In TLP solder bond are the best choices for creating a package cap. The practical limits for scaling the caps with these choices are limited to a thickness of ~ 20 μm and a package size of 900 μm in radius for a circular shaped package. These limits are acceptable for most applications that would utilize solder transferred thin-film packages. This packaging technology is best suited for small single devices distributed across a die instead of as a whole die packaging technology.

5.2.5 Conclusion

A method of transferring thin-film metal packages with a novel solder transfer layer has been developed. The method allows packages to be electroplated on a separate wafer and later, simultaneously, transferred and bonded to a device wafer. This modular approach adds fabrication flexibility to the packaging and the device processes that is not available in a standard thin-film packaging approach. The transfer is accomplished by selective dewetting of a solder transfer layer and the formation of TLP bond between the package cap and device wafer. The TLP bond did not provide a hermetic seal due to the low strength of the Ni-Sn TLP solder bond and large stress from the thermal coefficient of expansion (TCE) mismatch of the nickel cap and silicon substrate (see Figure 5.11), but the attachment strength was high enough to transfer more 99% of the caps from the host wafer to the device wafer.
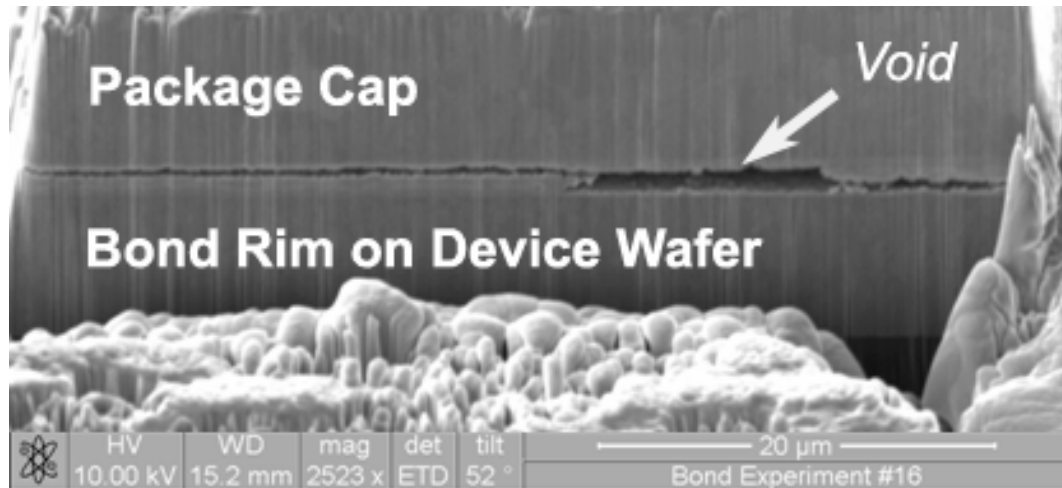
Figure 5.11 SEM image of a fractured bond ring. The low shear strength of the Ni-Sn TLP solder bond combined with the stress in the transferred cap broke the bond and resulted in an unsealed package.

Chapter 6

CONCLUSIONS AND FUTURE WORK

Solder is an interesting material for vacuum packaging MEMS devices at the wafer-level. It has good hermetic capabilities, can be processed at low temperatures, and planarize over topography. This thesis investigated its use as a wafer-bonding technique and as a novel transfer technique. A brief review of the results, conclusion, and future work are presented in the next sections.

6.1 Conclusion

Several different standard solder processes were applied to a wafer bonding process using commercially available wafer bonding equipment. The large thermal time constant of the commercial wafer bonders presented a challenge in reproducing the temperature profiles of standard soldering processes. A standard solder bond cycle lasts only 4 minutes and the solder is only molten for 30 seconds. The commercial wafer bonder, pressed to its limits, can produce a cycle time of 22 minutes where the solder is molten for 438 seconds. Solders that are molten for such a long time will completely consume even very thick (> 100 μm) layers of metals like Au, Cu, Ag, Pt. Therefore different combinations of solders and under-bump metals were investigated to determine if any were compatible with commercial wafer bonders. The only successful solder was Au-Sn solder, which, due to its low tin content, does not consume metals as rapidly as other solders. The Au-Sn solder bond is formed at 300 °C, with a process time of less than 1 hour. The bonding technique provides shear strength of 28 MPa, hermeticity of $1.5^{.}10^{-15}$ atm.cc.s^{-1}.

An advanced type of solder bonding, called transient liquid phase (TLP) solder bonding, was investigated because it is more compatible with the long thermal time

constants inherent in commercial wafer bonders. Unlike standard solder bonding, TLP solder bonding relies on the IMC formation between a low-melting point interlayer, which is usually tin or indium, and a parent metal. This allows TLP solder bonds to withstand long times at high temperatures that can even exceed the bonding temperature. Several different material systems were investigated, including Au-Sn, Au-In, and Ni-Sn TLP solder bonding. All three bonds were tested, but only the Au-In and Ni-Sn material systems proved capable of providing a void-free joint within the design constraints. The Au-In and Ni-Sn bonds, which are formed at 200 °C and 300 °C, showed shear strengths of 24.4 and 12.1 MPa and hermeticity of $1.0^{.}10^{-16}$ and $1.7^{.}10^{-17}$ atm$^{.}$cc$^{.}$s^{-1}, respectively. A design process for TLP solder bonds based on equations that govern intermetallic formation was presented.

The three hermetic wafer bonding techniques, Au-Sn standard solder, Au-In TLP solder, and Ni-Sn TLP solder, were used to create wafer-bonded MEMS vacuum packages. The packages were created by bonding two wafers together, one wafer contained Pirani gauges to monitor the long-term pressure level and the other wafer created a recessed cavity with integrated thin-film non-evaporable getters. The package pressures varied by a wide range, from 200 mTorr to 20 Torr, due to differences in outgassing in getter rates across the first package runs. A later package run used a long outgassing step (24 hours) at high vacuum to remove as much adsorbed gas from the package before sealing it. This resulted in fully activated package pressure of well below 0.5 Torr and as low as 20 mTorr. Several methods for further reducing this pressure are included in the future work section. Due to the low bonding temperature of Au-In TLP bonding (200 °C) the titanium thin-film getter activation process was able to be investigated. The un-activated package pressures were monitored over 5 days to determine a baseline pressure, and then the titanium getters were activated at different temperatures for set intervals while the pressure was monitored. The understanding gain through this investigation enabled a wafer-bonded MEMS vacuum package to show an internal pressure of < 20 mTorr with a maximum process temperature of 200 °C.

Solder was also investigated as a transfer mechanism. A novel solder transfer technique was developed that enables structures to be transferred from a carrier wafer to a

device wafer without any particles from broken tethers. The transfer process is designed by creating a solder layer between the structure to be transferred and the carrier wafer that will melt and dewet the carrier wafer during the bonding process. This technique was used to transfer electroplated thin-film nickel packages using a lead-based and lead-free transfer process. There was no evidence of a hermetic seal because the Ni-Sn TLP solder bond fractured after transfer. This is believe to be due to the high stress in the transferred package caps, which can be reduced in several ways that are outlined in the future work section.

6.2 Future Work

There are several potential improvements to the work presented in this thesis. The pressure levels inside the wafer-bonded packages could be reduced by several methods and the stress from the transferred thin-film packages could be reduced to prevent the TLP solder bond from fracturing.

6.2.1 Lower Pressure Wafer-Bonded Packages

The pressure level in the wafer-bonded packages was sufficient for some MEMS vacuum packaging needs, but an improvement would make it useful for more stringent requirements of applications like high-Q, low frequency gyroscopes and field emitting devices. Some ideas are discussed in the next sub-sections.

USE LOCALIZED ACTIVATION OF THE GETTERS

The heat that is used to activate the getters also increases the outgassing rate of the adsorbed gas on the inside of the package walls. From Figure 4.9, it is evident that an increase in temperature releases more adsorbed gas from the walls of the MEMS package. Therefore, when the getters are activated with thermal energy, to pump more contaminants from the package, gas is also being driven from the walls of the MEMS package. If the getters could be thermally isolated from the substrate, the heat could be applied locally with two benefits. The first benefit is a reduced outgassing rate from the inside walls of the package because they do not heat up during the getter activation process. The second is that the getters could be heated to a high temperature (> 500°C) to

increase the pumping rate without harming any temperature sensitive devices on the MEMS device wafer.

<div align="center">CHANGE THE PACKAGE CAVITY GEOMETRY</div>

The outgassing rate is proportional to the surface area of the inside of the package. The pressure rise from outgassing is inversely proportional to the volume. These reasons combine to make scaling vacuum packages to MEMS dimensions difficult. Therefore, an easy, but compromising, way to reduce the pressure inside the cavity is to increase the enclosed volume. This increase should reduce the pressure inversely proportional to the ratio of the new volume to the old volume. For the packages presented in this work, the cap wafer was thinned by 100 μm to create the cavity. Thinning the cap wafer by 200 or 300 μm should reduce the pressure by a factor of 2 or 3.

6.2.2 Transferred Thin-Film Packages with Vacuum

As shown in Figure 5.11, the stress from the TCE mismatch of the transferred nickel cap and silicon substrate causes the weak Ni-Sn TLP bond to fracture as the wafers cool down. There are several material changes that could reduce the TCE mismatch stress and increase the TLP solder bond strength. If the cap and bond rings were made out of gold instead of nickel and the interlayer were indium instead of tin, the TCE mismatch stress would be less and the TLP solder bond would be stronger. Gold has a slightly higher TCE than nickel (14.8 ppm vs. 13.4 ppm) but a lower Young's modulus by over a factor of two (78 GPa vs. 200 GPa) [79]. These facts alone lower the resulting mismatch stress considerably. Other benefits, including a lower bonding temperature of 200 °C and a higher shear strength for Au-In TLP solder bonding compared to Ni-Sn TLP solder bonding (28 MPa vs. 12.4 MPa) also make gold and indium better choices for transferred thin-film packaging.

Appendix A: Raw Data from Shear Strength Tests

Table 6.1 Shear strength raw data for the Nickel-Tin TLP solder bonded wafer.

Row	Col.	# of Weights	Calculated Applied Force (N)	Shear Strength (MPa)	Failure Mode	Pass/Fail
1	4	10	40.2	13.2	Sheared	PASS
1	6	1	0.0	0.0	Sheared	FAIL
2	6	6	21.2	7.0	Sheared	FAIL
1	12	5	16.5	5.4	Sheared	FAIL
2	12	9	35.5	11.7	Not Sheared	FAIL
4	13	19	82.9	27.3	Sheared	PASS
3	6	10	40.2	13.2	Sheared	PASS
5	10	4	11.7	3.9	Sheared	FAIL
6	8	6	21.2	7.0	Sheared	FAIL
5	6	7	26.0	8.6	Sheared	FAIL
5	5	4	11.7	3.9	Sheared	FAIL
3	2	13	54.4	17.9	Not Sheared	PASS
5	1	4	11.7	3.9	Sheared	FAIL
6	1	4	11.7	3.9	Sheared	FAIL
8	3	14	59.2	19.5	Not Sheared	PASS
8	6	14	59.2	19.5	Sheared	PASS
8	14	3	7.0	2.3	Sheared	FAIL
8	12	20	87.7	28.9	Sheared	PASS
9	12	13	54.4	17.9	Sheared	PASS
9	6	15	63.9	21.1	Not Sheared	PASS
9	3	13	54.4	17.9	Sheared	PASS
10	5	4	11.7	3.9	Sheared	FAIL
10	7	4	11.7	3.9	Sheared	FAIL
9	5	20	87.7	28.9	Sheared	PASS

Table 6.2 Shear strength raw data for the Gold-Indium TLP solder bonded wafer.

Row	Col.	# of Weights	Calculated Applied Force (N)	Shear Strength (MPa)	Failure Mode	Pass/Fail
1	5	20	87.7	28.9	Sheared	PASS
1	6	9	35.5	11.7	Not Sheared	FAIL
1	9	20	87.7	28.9	Not Sheared	PASS
1	10	15	63.9	21.1	Not Sheared	PASS
1	11	13	54.4	17.9	Not Sheared	PASS
1	12	20	87.7	28.9	Didn't Break	PASS
3	7	17	73.4	24.2	Not Sheared	PASS
3	8	13	54.4	17.9	Not Sheared	PASS
3	9	10	40.2	13.2	Not Sheared	PASS
3	13	15	63.9	21.1	Not Sheared	PASS
3	14	20	87.7	28.9	Not Sheared	PASS
4	2	20	87.7	28.9	Not Sheared	PASS
4	7	14	59.2	19.5	Not Sheared	PASS
4	13	15	63.9	21.1	Not Sheared	PASS
5	4	17	73.4	24.2	Not Sheared	PASS
5	8	20	87.7	28.9	Didn't Break	PASS
5	14	20	87.7	28.9	Not Sheared	PASS
6	1	20	87.7	28.9	Didn't Break	PASS
6	7	20	87.7	28.9	Didn't Break	PASS
6	12	15	63.9	21.1	Not Sheared	PASS
7	1	17	73.4	24.2	Not Sheared	PASS
7	7	20	87.7	28.9	Didn't Break	PASS
7	12	18	78.2	25.8	Not Sheared	PASS
8	1	18	78.2	25.8	Not Sheared	PASS
8	8	20	87.7	28.9	Didn't Break	PASS
8	14	20	87.7	28.9	Not Sheared	PASS
10	3	16	68.7	22.6	Not Sheared	PASS
10	7	20	87.7	28.9	Didn't Break	PASS
10	12	14	59.2	19.5	Not Sheared	PASS

Table 6.3 Shear strength raw data for the Gold-Tin solder bonded wafer.

Row	Col.	# of Weights	Calculated Applied Force (N)	Shear Strength (MPa)	Failure Mode	Pass/Fail
2	3	16	68.7	22.6	Not Sheared	PASS
2	7	15	63.9	21.1	Not Sheared	PASS
2	12	20	87.7	28.9	Not Sheared	PASS
3	1	18	78.2	25.8	Not Sheared	PASS
3	13	20	87.7	28.9	Didn't Break	PASS
4	1	20	87.7	28.9	Didn't Break	PASS
4	7	20	87.7	28.9	Didn't Break	PASS
4	14	20	87.7	28.9	Not Sheared	PASS
5	2	20	87.7	28.9	Didn't Break	PASS
5	7	20	87.7	28.9	Didn't Break	PASS
5	13	20	87.7	28.9	Not Sheared	PASS
6	1	20	87.7	28.9	Didn't Break	PASS
6	7	20	87.7	28.9	Didn't Break	PASS
6	14	20	87.7	28.9	Didn't Break	PASS
7	1	20	87.7	28.9	Didn't Break	PASS
7	6	20	87.7	28.9	Not Sheared	PASS
7	13	20	87.7	28.9	Didn't Break	PASS
8	1	20	87.7	28.9	Not Sheared	PASS
8	8	20	87.7	28.9	Didn't Break	PASS
8	14	20	87.7	28.9	Not Sheared	PASS
9	3	20	87.7	28.9	Didn't Break	PASS
9	8	20	87.7	28.9	Didn't Break	PASS
9	12	20	87.7	28.9	Not Sheared	PASS
10	3	20	87.7	28.9	Didn't Break	PASS
10	7	19	82.9	27.3	Not Sheared	PASS
10	12	17	73.4	24.2	Not Sheared	PASS

Bibilography

[1] H. C. Nathanson, W. E. Newell, R. A. Wickstrom and J. R. Davis Jr., "The resonator gate transistor," *IEEE Trans. Electron Devices,* vol. ED-14, pp. 117-133, 03. 1967.

[2] J. C. Eloy, "MIS 07 - status of the MEMS industry report," Yole Development, Lyon, France, 2007.

[3] T. J. Harpster, "Hermetic Packaging and Bonding Technologies for Implantable Microsystems," 2005.

[4] R. R. Tummala and E. J. Rymaszewski, *Microelectronics Packaging Handbook.* New York : Chapman & Hall, 1997,

[5] J. Mitchell, "Low Temperature Wafer Level Vacuum Packaging Using Au-Si Eutectic Bonding and Localized Heating," 2007.

[6] K. Takahata, A. DeHennis, K. D. Wise and Y. B. Gianchandani, "A wireless microsensor for monitoring flow and pressure in a blood vessel utilizing a dual-inductor antenna stent and two pressure sensors," in *Maastricht MEMS 2004 Technical Digest,* 2004, pp. 216-19.

[7] M. Dokmeci and K. Najafi, "Glass-silicon hermetic micro packages for implantable biomedical microsystems," in *Vehicle Displays and Microsensors '99. 6th Annual Strategic and Technical Symposium, 22-23 Sept. 1999,* 1999, pp. 159-64.

[8] R. G. Azevedo, D. G. Jones, A. V. Jog, B. Jamshidi, D. R. Myers, L. Chen, Xiao-an Fu, M. Mehregany, M. B. J. Wijesundara and A. P. Pisano, "A SiC MEMS resonant strain sensor for harsh environment applications," *IEEE Sensors Journal,* vol. 7, pp. 568-76, 04. 2007.

[9] Wen-Lung Huang, Z. Ren and C. T. -. Nguyen, "Nickel vibrating micromechanical disk resonator with solid dielectric capacitive-transducer gap," in *Proceedings of the 2006 IEEE International Frequency Control Symposium and Exposition,* 2006, pp. 9.

[10] B. H. Stark and K. Najafi, "A low-temperature thin-film electroplated metal vacuum package," *J Microelectromech Syst,* vol. 13, pp. 147-157, 2004.

[11] W. Park, J. Cho, H. Li, T. W. Kenny, R. N. Candler, H. J. Li, A. Partridge, G. Yama and M. Lutz, "Wafer scale encapsulation of MEMS devices," in *2003 International Electronic Packaging Technical Conference and Exhibition, Jul 6-11 2003,* 2003, pp. 209-212.

[12] W. H. Ko, J. T. Suminto and G. J. Yeh, "Bonding techniques for microsensors," in *Micromachining and Micropackaging of Transducers.* 1985, pp. 41-61.

[13] W. P. Maszara, "Silicon-on-insulator by wafer bonding. A review," *J. Electrochem. Soc.,* vol. 138, pp. 341-347, 1991.

[14] A. Singh, D. A. Horsley, M. B. Cohn, A. P. Pisano and R. T. Howe, "Batch transfer of microstructures using flip chip solder bump bonding," in *Tech. Dig. Transducers'97, 9th Int. Conf. Solid-State Sensors and Actuators,* 1997, pp. 265.

[15] L. Ristic, *Sensor Technology and Devices.* Boston : Artech House, 1994, pp. xiv, 524.

[16] V. L. Spiering, J. W. Berenschot, M. Elwenspoek and J. H. J. Fluitman, "Sacrificial wafer bonding for planarization after very deep etching," *J Microelectromech Syst,* vol. 4, pp. 151-7, 1995.

[17] L. Parameswaran, V. M. McNeil, M. A. Huff and M. A. Schmidt, "Sealed-cavity microstructure using wafer bonding technology," in *Tech. Dig. Transducers'93, 7th Int. Conf. Solid-State Sensors and Actuators,* 1993, pp. 274-277.

[18] T. Yagi, Y. Shimada, T. Ikeda, O. Takamatsu, H. Matsuda, K. Takimoto and Y. Hirai, "A new method to fabricate metal tips for scanning probe microscopy," in *Proceedings IEEE the Tenth Annual International Workshop on Micro Electro Mechanical Systems. an Investigation of Micro Structures, Sensors, Actuators, Machines and Robots, 26-30 Jan. 1997,* 1997, pp. 129-34.

[19] M. M. Maharbiz, M. B. Cohn, R. T. Howe, R. Horowitz and A. P. Pisano, "Batch micropackaging by compression-bonded wafer-wafer transfer," in *Proceedings of the 1999 12th IEEE International Conference on Micro Electro Mechanical Systems, MEMS, Jan 17-21 1999,* 1999, pp. 482-489.

[20] G. Humpston, *Principles of Soldering.* Materials Park, OH : ASM International, 2004, pp. xii, 271.

[21] B. Lee, S. Seok and K. Chun, "A study on wafer level vacuum packaging for MEMS devices," *J Micromech Microengineering,* vol. 13, pp. 663-669, 2003.

[22] M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation," *Proc IEEE,* vol. 86, pp. 1575-1585, 1998.

[23] P. W. Barth, "Silicon fusion bonding for fabrication of sensors, actuators and microstructures," *Sens Actuators A Phys,* vol. 23, pp. 919-926, 1990.

[24] V. Dragoi and P. Lindner, "Plasma activated wafer bonding of silicon: In situ and ex situ processes," in *Semiconductor Wafer Bonding 9: Science, Technology, and Applications - 210th Electrochemical Society Meeting,* 2006, pp. 147-154.

[25] D. Sparks, S. Massoud-Ansari and N. Najafi, "Reliable vacuum packaging using NanoGetters [trademark] and glass frit bonding," in *Reliability, Testing, and Characterization of MEMS/MOEMS III, Jan 26-28 2004,* 2004, pp. 70-78.

[26] R. Knechtel, "Glass frit bonding: An universal technology for wafer level encapsulation and packaging," *Microsystem Technologies,* vol. 12, pp. 63-68, 2005.

[27] M. Pecht, Y. Fukuda and S. Rajagopal, "The impact of lead-free legislation exemptions on the electronics industry," *IEEE Transactions on Electronics Packaging Manufacturing,* vol. 27, pp. 221-232, 2004.

[28] N. Koopman, S. Bobbio, S. Nangalia, J. Bousaba and B. Piekarski, "Fluxless soldering in air and nitrogen," in *1993 Proceedings of the 43rd Electronic Components and Technology Conference, Jun 1-4 1993,* 1993, pp. 595-605.

[29] G. Humpston and D. M. Jacobson, "Fluxless soldering processes," *Advanced Materials and Processes,* vol. 162, pp. 35-37, 2004.

[30] Anonymous "SUSS MicroTec: SB6/8e Semi-Automated Wafer Bonding System," vol. 2007,

[31] S. Park and Y. Kim, "Intermetallic formation between sn-ag(-cu) solder bumps and Au/Ni/Ti UBM and it's effects on the shear force of the solder bumps," in *PRICM 5: The*

Fifth Pacific Rim International Conference on Advanced Materials and Processing, 2005, pp. 1881-1884.

[32] M. N. Islam, Y. C. Chan, M. O. Alam and A. Sharif, "Comparative study of the dissolution kinetics of electrolytic Ni and electroless NiP Layers by molten Sn3.5Ag solder alloy," *Transactions of the ASME. Journal of Electronic Packaging,* vol. 127, pp. 365-9, 12. 2005.

[33] J. F. Li, S. H. Mannan and M. P. Clode, "Lifetime of solid metals in contact with liquid solders for high-temperature liquid solder assemblies," *Scr. Mater.,* vol. 54, pp. 1773-8, 05. 2006.

[34] Thang Tak-Seng, D. Sun, Huck-Khim Koay, M. -. Sabudin, J. Thompson, P. Martin, P. Rajkomar and S. Haque, "Characterization of au-sn eutectic die attach process for optoelectronics device," in *2005 International Symposium on Electronics Materials and Packaging,* 2005, pp. 118-24.

[35] Y. Tao, A. P. Malshe and W. D. Brown, "Selective bonding and encapsulation for wafer-level vacuum packaging of MEMS and related micro systems," *Microelectronics Reliability,* vol. 44, pp. 251-258, 2004.

[36] C. Luo, L. Lin and M. Chiao, "Nanosecond-pulsed laser bonding with a built-in mask for MEMS packaging applications," in *Proceedings of 11th International Conference on Solid State Sensors and Actuators Transducers '01/Eurosensors XV,* 2001, pp. 214-17.

[37] U. M. Mescheder, M. Alavi, K. Hiltmann, C. Lizeau, C. Nachtigall and H. Sandmaier, "Local laser bonding for low temperature budget," in *Proceedings of 11th International Conference on Solid State Sensors and Actuators Transducers '01/Eurosensors XV,* 2001, pp. 218-21.

[38] M. J. Wild, A. Gillner and R. Poprawe, "Advances in silicon to glass bonding with laser," in *MEMS Design, Fabrication, Characterization, and Packaging,* 2001, pp. 135-41.

[39] Hsueh-An Yang, M. Wu and W. Fang, "Localized induction heating solder bonding for wafer level MEMS packaging," *J Micromech Microengineering,* vol. 15, pp. 394-9, 02. 2005.

[40] B. D. Sosnowchik, L. Lin and A. P. Pisano, "Rapid silicon-to-steel bonding using inductive heating," in *2006 ASME International Mechanical Engineering Congress and Exposition, IMECE2006,* 2006, pp. 7.

[41] B. D. Sosnowchik, L. Lin and A. P. Pisano, "Rapid silicon-to-steel bonding using inductive heating," in *2006 ASME International Mechanical Engineering Congress and Exposition, IMECE2006,* 2006, pp. 7.

[42] C. Hu, S. Wen, C. Hsu, C. Chang, C. Shih and H. Lee, "Solder bonding with a buffer layer for MOEMS packaging using induction heating," *Microsystem Technologies,* vol. 12, pp. 1011-1014, 2006.

[43] W. D. MacDonald and T. W. Eagar, "Transient Liquid Phase Bonding," *Annual Review of Materials Science,* vol. 22, pp. 23-46, 1992.

[44] J. F. Lynch, L. Feinstein and R. A. Huggins, "Brazing by diffusion-controlled formation of liquid intermediate phase," *Welding Journal,* vol. 38, pp. 85-89, 1959.

[45] G. Hoppin and T. F. Berry, "Activated Diffusion Bonding," *Journal of Welding,* vol. 49, pp. 505-509, 1970.

[46] W. A. Owczarski, "Eutectic Brazing of Zircaloy 2 to Type 304 Stainless Steel," *Journal of Welding,* vol. 41, pp. 78-83, 1962.

[47] L. Bernstein, "Semiconductor joining by the solid-liquid interdiffusion (SLID) process. I. The systems Ag-In, Au-In and Cu-In," *J. Electrochem. Soc.,* vol. 113, pp. 1282-1288, 12. 1966.

[48] J. S. Kim, T. Yokozuka and C. C. Lee, "Fluxless bonding of silicon to copper with high-temperature ag-sn joint made at low temperature," in *IEEE 56th Electronic Components and Technology Conference,* 2006, pp. 1706-1711.

[49] R. W. Chuang and C. C. Lee, "Silver-indium joints produced at low temperature for high temperature devices," *IEEE Transactions on Components and Packaging Technologies,* vol. 25, pp. 453-458, 2002.

[50] Y. Chen and C. C. Lee, "Indium - copper multilayer composites for fluxless oxidation-free bonding," *Thin Solid Films,* vol. 283, pp. 243-246, 1996.

[51] N. S. Bosco and F. W. Zok, "Critical interlayer thickness for transient liquid phase bonding in the Cu-Sn system," *Acta Materialia,* vol. 52, pp. 2965-2972, 2004.

[52] G. Humpston, D. M. Jacobson and S. P. S. Sangha, "Diffusion soldering for electronics manufacturing," *Endeavour,* vol. 18, pp. 55-60, 1994.

[53] R. R. Wells, "Microstructural Control of Thin-Film Diffusion Brazed Titanium," *Weld J (Miami Fla),* vol. 55, pp. 20-27, 1976.

[54] J. Crank, *The Mathematics of Diffusion.* Oxford University Press, 1975,

[55] V. I. Dybkov, "Reaction diffusion in heterogeneous binary systems. I. Growth of the chemical compound layers at the interface between two elementary substances: one compound layer," *J. Mater. Sci.,* vol. 21, pp. 3078-84, 1986.

[56] M. Millares, B. Pieraggi and E. Lelievre, "Reaction/diffusion in the Au-In system," *Solid State Ionics,* vol. 63-65, pp. 575-580, 1993.

[57] W. J. Tomlinson and H. G. Rhodes, "Kinetics of intermetallic compound growth between nickel, electroless Ni-P, electroless Ni-B and tin at 453 to 493 K," *J. Mater. Sci.,* vol. 22, pp. 1769-72, 05. 1987.

[58] P. G. Shewmon, *Diffusion in Solids /.* Warrendale, Pa. : Minerals, Metals & Materials Society, 1989; 1989,

[59] K. L. Erickson, P. L. Hopkins and P. T. Vianco, "Solid state intermetallic compound growth between copper and high temperature, tin-rich solders. Part II. Modeling," *J Electron Mater,* vol. 23, pp. 729-734, 1994.

[60] J. K. Chen, J. E. Beraun and D. Y. Tzou, "A dual-phase-lag diffusion model for predicting intermetallic compound Layer growth in solder joints," *Transactions of the ASME. Journal of Electronic Packaging,* vol. 123, pp. 52-7, 03. 2001.

[61] J. K. Chen, J. E. Beraun and D. Y. Tzou, "Dual-phase-lag diffusion model for predicting thin film growth," *Semiconductor Science and Technology,* vol. 15, pp. 235-241, 2000.

[62] R. Quintanilla, "Exponential stability in the dual-phase-lag heat conduction theory," *J. Non Equilib. Thermodyn.,* vol. 27, pp. 217-227, 2002.

[63] Y. M. Liu and T. H. Chuang, "Interfacial reactions between liquid indium and Au-deposited substrates," *J Electron Mater,* vol. 29, pp. 405-10, 04. 2000.

[64] T. Ishida, "Rate of Dissolution of Solid Nickel in Liquid Tin under Static Conditions," *Metallurgical Transactions B (Process Metallurgy),* vol. 17B, pp. 281-289, 1986.

[65] E. Lugscheider, K. Bobzin and A. Erdle, "Solder deposition for transient liquid phase (TLP)-bonding by MSIP-PVD-process," *Surface and Coatings Technology,* vol. 174-175, pp. 704-707, 2003.

[66] S. R. Cain, J. R. Wilcox and R. Venkatraman, "A diffusional model for transient liquid phase bonding," *Acta Materialia,* vol. 45, pp. 701-7, 02. 1997.

[67] Department of Defense, *MIL-STD-883E, Test Method Standard, Micro-Circuits, Method 1014.9.* March 14th, 1995,

[68] Anonymous "Indium Advocate News @ Basics/Mines," vol. 2007,

[69] Anonymous "The IPC Solder Products Value council feels compelled to clearly articulate the current global situation regarding the global supply of two crucial metallic elements to the Electronics Industry," vol. 2007,

[70] ASM International., ASM International. and ASM International., *ASM Handbook.* Materials Park, Ohio : ASM International, 1992; 1992,

[71] Y. Tao and A. P. Malshe, "Theoretical investigation on hermeticity testing of MEMS packages based on MIL-STD-883E," *Microelectronics Reliability,* vol. 45, pp. 559-66, 03. 2005.

[72] A. Jourdain, P. De Moor, S. Pamidighantam and H. A. C. Tilmans, "Investigation of the hermeticity of BCB-sealed cavities for housing (RF-)MEMS devices," in *Fifteenth IEEE International Conference on Micro Electro Mechanical Systems,* 2002, pp. 677-80.

[73] Xiao Ying-Ying, Wang Jian-Hua, Huang Qing-An and Q. Ming, "Measurements of the bond strength for wafer bonding," *Chinese Journal of Electron Devices,* vol. 27, pp. 360-5, 06. 2004.

[74] M. Petzold, H. Knoll and J. Bagdahn, "Strength assessment of wafer-bonded micromechanical components using the micro-chevron-test," in *Reliability, Testing, and Characterization of MEMS/MOEMS, Oct 22-24 2001,* 2001, pp. 133-142.

[75] W. J. Tomlinson and H. G. Rhodes, "Kinetics of intermetallic compound growth between nickel, electroless Ni-P, electroless Ni-B and tin at 453 to 493 K," *J. Mater. Sci.,* vol. 22, pp. 1769-1772, 1987.

[76] D. Kim, J. Kim, G. L. Wang and C. C. Lee, "Nucleation and growth of intermetallics and gold clusters on thick tin layers in electroplating process," *Materials Science and Engineering A,* vol. 393, pp. 315-319, 2/25. 2005.

[77] Mona, A. Kumar and Z. Chen, "Influence of phosphorus content on the interfacial microstructure between Sn-3.5Ag solder and electroless Ni-P metallization on Cu substrate," *IEEE Transactions on Advanced Packaging,* vol. 30, pp. 68-72, 2007.

[78] C. K. Saw and W. J. Siekhaus, "Thermal expansion of AuIn2," *Scripta Materialia,* vol. 53, pp. 1153-1157, 11. 2005.

[79] Anonymous "Chemistry: WebElements Periodic Table," vol. 2007,

[80] J. F. O'Hanlon, *A User's Guide to Vacuum Technology.* Hoboken, N.J. : Wiley-Interscience, 2003, pp. xviii, 516.

[81] J. M. Lafferty, *Foundations of Vacuum Science and Technology.* New York : Wiley, 1998, pp. xxv, 728.

[82] L. G. Carpenter, "Vacuum Technology," *Vacuum,* vol. 20, pp. 253, 06. 1970.

[83] General Electric, *Fluid Flow Databook.* Genium Publishing, 1982,

[84] M. H. Unewisse, K. C. Liddiard, B. I. Craig, S. J. Passmore, R. J. Watson, R. E. Clarke and O. Reinhold, "Semiconductor film bolometer technology for uncooled IR

sensors," *Proceedings of the SPIE - the International Society for Optical Engineering,* vol. 2552, pp. 77-87, /. 1995.

[85] J. R. Clark, W. Hsu, M. A. Abdelmoneum and C. T. -. Nguyen, "High-Q UHF micromechanical radial-contour mode disk resonators," *J Microelectromech Syst,* vol. 14, pp. 1298-1310, 2005.

[86] M. Bao and H. Yang, "Squeeze film air damping in MEMS," *Sensors and Actuators A (Physical),* vol. 136, pp. 3-27, 05/01. 2007.

[87] L. C. Chow and R. J. Pinnington, "Practical industrial method of increasing structural damping in machinery, II: Squeeze-film damping with liquids," *J. Sound Vibrat.,* vol. 128, pp. 333-347, 1989.

[88] Young-Ho Cho, B. M. Kwak, A. P. Pisano and R. T. Howe, "Slide film damping in laterally driven microstructures," *Sensors and Actuators A (Physical),* vol. A40, pp. 31-9, 01. 1994.

[89] J. Kang, Z. Xu and A. Akay, "Inertia effects on compressible squeeze films," *J Vib Acoust Trans ASME,* vol. 117, pp. 94-102, 1995.

[90] B. H. Stark, Y. Mei, C. Zhang and K. Najafi, "A doubly anchored surface micromachined pirani gauge for vacuum package characterization," in *IEEE Sixteenth Annual International Conference on Micro Electro Mechanical Systems, Jan 19-23 2003,* 2003, pp. 506-509.

[91] K. R. Spangenberg, *Vacuum Tubes.* McGraw-Hill, 1948,

[92] K. Kakushima and H. Fujita, "MEMS application to characterization of field emitters and biomolecules," in *MEMS, MOEMS, and Micromachining,* 2004, pp. 82-8.

[93] I. Karatzas, *Brownian Motion and Stochastic Calculus.* Springer, 1991,

[94] D. Huber, P. Corredoura, S. Lester, V. Robbins and L. Kamas, "Reducing Brownian motion in an electrostatically tunable MEMS laser," *J Microelectromech Syst,* vol. 13, pp. 732-6, 10. 2004.

[95] A. Roth, *Vacuum Technology. Second, Revised Edition.* North-Holland, 1982, pp. xiv+532.

[96] B. Dayton, "Outgassing Rate of Contaminated Metal Surfaces," *Trans.8 thNational Vacuum Symposium and 2 ndInternational Congress on Vacuum Science and Technology, Washington, DC,* 1961.

[97] Min Seog Choi and Sung Hoon Choa, "Experimental reliability estimation and improvement for a wafer level vacuum packaged MEMS device," in *Asian Pacific Conference for Fracture and Strength (APCFS'04),* 2005, pp. 588-93.

[98] S. H. Choa, "Reliability of vacuum packaged MEMS gyroscopes," *Microelectronics Reliability,* vol. 45, pp. 361-369, 2005.

[99] M. Moraja, M. Amiotti and H. Florence, "Chemical treatment of getter films on wafers prior to vacuum packaging," in *Reliability, Testing, and Characterization of MEMS/MOEMS III, Jan 26-28 2004,* 2004, pp. 87-93.

[100] M. Esashi and K. Minami, "Packaged micromechanical sensors," in *Proceedings of the 1994 IEEE Symposium on Emerging Technologies & Factory Automation, Nov 6-10 1994,* 1994, pp. 30-37.

[101] T. Schimert, N. Cunningham, G. Francisco, R. Gooch, J. Gooden, P. McCardel, B. Neal, B. Ritchey, J. Rife, A. J. Syllaios, J. Tregilgas, J. Brady, J. Gilstrap and S. Ropson, "Low cost, low power uncooled 120x160 a-si-based micro infrared camera for law

enforcement applications," in *Enabling Technologies for Law Enforcement and Security, Nov 5-8 2000,* 2001, pp. 187-194.

[102] J. Mitchell, "Encapsulation of vacuum sensors in a wafer level package using a gold-silicon eutectic," pp. 928, 2005.

[103] Y. Cheng, W. Hsu, K. Najafi, C. T. -. Nguyen and L. Lin, "Vacuum packaging technology using localized aluminum/silicon-to-glass bonding," *J Microelectromech Syst,* vol. 11, pp. 556-565, 2002.

[104] G. W. Hill, "Student's *t*-distribution," *Commun ACM,* vol. 13, pp. 617-19, 10. 1970.

[105] M. Moraja, M. Amiotti and R. Kullberg, "New getter configuration at wafer level for assuring long term stability of MEMs," in *Reliability, Testing, and Characterization of MEMS/MOEMS II, Jan 27-29 2003,* 2003, pp. 260-267.

[106] W. C. Welch III and K. Najafi, "Transfer of metal MEMS packages using a wafer-lelel solder sacrificial layer," in *18th IEEE International Conference on Micro Electro Mechanical Systems (MEMS): Miami MEMS 2005 Technical Digest, Jan 30 - Feb 3 2005,* 2005, pp. 584-587.

[107] C. T. Pan, "Selective low temperature microcap packaging technique through flip chip and wafer level alignment," *J Micromech Microengineering,* vol. 14, pp. 522-9, 04/. 2004.