MIMIC Mixer/Multiplier

Faculty: Linda P.B. Katehi and Jack East
Graduate Students: Steve Robertson and Fred Brauckler

Quarterly Report

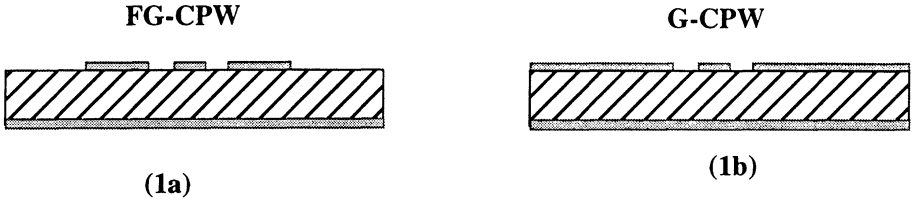
This is a quarterly progress report on the MIMIC Mixer/Multiplier Project. As we discussed during our review at Michigan, as an initial step we have concentrated on the design of a MIMIC circuit which carries the first of the two desired functions of the Mixer. We have focused on the design of a MIMIC circuit which in the transmit mode performs as a doubler with a desired bandwidth of a least 2 GHz and with about 7 dBs of conversion loss.

For this doubler circuit we decided to use finite-ground coplanar waveguides to allow for easy integration of the Schottky diodes and eliminate the undesirable parasitic effects associated with microstrip as well as regular coplanar waveguide. These unwanted mechanisms are parasitic coupling and parasitic radiation in the form of substrate modes. The presence of these effects substantially increase loss and limit performance.

At the present time we have been able to design, fabricate and measure the performance of all the passive components required for the doubler and we found that these components have demonstrated excellent performance. Our next step is to integrate the diodes in the circuit and measure its performance. The purpose of this report is to briefly review what we discussed during our first project review and report on our progress since then.

As it has been mentioned above, the transmission line geometry considered for this project is the finite ground coplanar waveguide (FGCPW) shown on figure 1a. The coplanar arrangement is important to allow for the integration of the diodes with minimal inductive parasitics. The finite grounds are necessary to insure suppression of the parallel plate waveguide mode which dominate the performance of the conventional grounded coplanar waveguide, shown on figure 1b, and introduce substantial parasitic coupling and parasitic radiation loss.

FIGURE 1. Coplanar Waveguide Geometries



(1a) (1b)

Theoretical studies of the FG-CPW line were performed early-on in the project and using both point matching method (PMM) and a finite element method (FEM) of the 2-D geometry shown in figure 2. The analysis showed that this line can propagate a single, almost dispersionless, quasi-static mode up to 135GHz thus allowing for excellent performance in the frequency ranges of interest (up to 115 GHz). Figure 3 shows indirectly the cut-off frequency of the second mode by the abrupt change of the relative effective dielectric constant of the line. Using the same analysis, the characteristic impedance and the effective dielectric constant of the FG-CPW line vs. the slot aperture (figure 1a and 2) have been computed and are plotted in figure 4. The FEM analysis provided a 2-D mapping of the field intensity seen in Figure 5. Both methods have provided useful design information on the performance of the proposed line.

As a next step in the theoretical modeling, a stepped impedance low-pass filter was designed and analyzed with a finite difference time domain code (FDTD) code. The filter has five stages and high/low impedance values of 94 W and 21 W respectively. Figure 6 shows an FDTD simulated response of the filter, which has a cutoff frequency of approximately 40 GHz with better than 15 dB out-of-band rejection. For the

doubler application, the filter can be scaled to pass the 47 GHz input and block the 94 GHz output.

The FDTD analysis was also used to study the air-bridge structures which are to be incorporated in the diode mounting structure for the doubler. The air-bridge structures will be extended from the center conductor of the FG-CPW out towards the ground planes as shown in figure 7. The diodes will be incorporated in the upper ground planes, with the ground metallization serving as the anode. The air-bridge structures will contact the tops of the diodes to form the cathode, and the diode bias voltage will be provided thought the center conductor of the FG-CPW line. Figure 8 shows the insertion loss of four diode mounting fingers with different lengths. These preliminary results indicate that the mounting structure can be modeled by a series LC combination in shunt with the transmission line.

With the completion of the theoretical modeling. the emphasis was sifted to the fabrication of the passive circuit components necessary for the doubler and the verification of their performance through measurements. The fabrication process of FG-CPW circuits can be broken into a number of steps (see figure 9). First the GaAs sample is thinned to 100μm by lapping, then via holes are etched, if needed, and the backside is metallized. Next the diodes and the air-bridges are formed. Finally, the circuits are defined and metallized.

Early in this project we suspected that the FG-CPW circuits will require the use of vias in the feeding ports of the doubler. That led us into fabricating circuits with vias in the input and output ports. Formation of diodes, air bridges and circuits has been obtained on prior projects. However, a via hole process and the lapping and handling techniques of the thin semiconductor material were required. Non-uniformity of the via holes across the sample was a problem for the first several attempts (see figure 10), but with the proper agitation, uniform vias were obtained. The lapping and handling were made possible by temporarily bonding a second substrate to the semiconductor sample. With these techniques, the fabrication of circuits became possible.

The first circuits which were fabricated included two low-pass filters shown in figure 11. The larger in size was designed for a cut-off frequency of 32 GHz (figure 11b) and the smaller in size for a cut-off frequency of 60 GHz (figure 11a). The rest of the lines were calibration standards for a TRL calibration. The TRL calibration set was designed with several delay lines for use from 1GHz to 120GHz (see figure 11). A

second set of circuits was also fabricated and measured. In addition to the previous circuits components, this second mask included matching stubs, required for the doubler, and some diode mounting structures. Measurements performed on these two sets of circuits indicated that via holes were not working well and that they introduced very strong parasitic resonances. At that time we decided to remove the vias from the circuit masks, fabricate the circuits again and measure them to verify performance.

As a next step the previously described two sets of circuits were fabricated without vias and their performance was measured. The measurements were performed in our 40GHz probe station and showed excellent performance. Figure 13 shows the measured loss for a through line to be 0.81 dB/λg at 40 GHz. The whole performance from 5GHz to 40 GHz indicated that most of the loss comes from conductor losses which in dB/λg vary as the inverse of the square root of the frequency. As a result, the loss at 47GHz and 94GHz is expected to be approximately 0.74 dB/λg and 0.528 dB/λg respectively for a structure which scales appropriately.

The very low-loss performance was also confirmed by the response of an open-end FG-CPW stub (figure 12c) which is plotted in figure 14 and shows an S_{21} of less than -23 dB at the resonant frequency. The final two measurements which indicated the low-loss performance of the FG-CPW provided the performance of the two low-pass filters included in the mask. The longest filter with a 32 GHz cut-off frequency exhibited a 2db conductor loss in the pass-band due to its longer features (see figure 15), and a return of less than -15 dB with a rejection of -15db at 40 GHZ, as it has been predicted by the theory (scaled version of filter in figure 6). The low-pass filter with 60 GHz cut-off frequency exhibited a much lower loss, less than 0.5 dBs in the pass band (see figure 16) and a much lower return, less than -30dB in the pass band. The rejection band of this filter will be measured in the W-band probe station at NASA Lewis Research Center.

In addition to the above, a harmonic balance analysis program has been used to determine a range of impedances that can be used for good performance in a varactor multiplier. By trading varactor performance for better impedance matching, an input Q~-2.5 and output Q~1 with impedance near 50 Ω can be obtained. In this range, a varactor diode can still operate at a reasonable efficiency and output power. These impedances are being used to determine the best matching network for the multiplier circuits (see figure 17). Measurements of the above circuits on a W-band

probe station at the facilities of NASA Lewis Research Center will be performed within the next few weeks. However, all measurements indicate that the circuits performed as expected and predicted by the theory.

At this point we are ready to proceed with the fabrication and measurement of the doubler to verify its performance. We will be able to provide update you with more measurement data in one to two months.

2-D Geometry of FGCPW

- Use PMM and FEM to analyze FGCPW

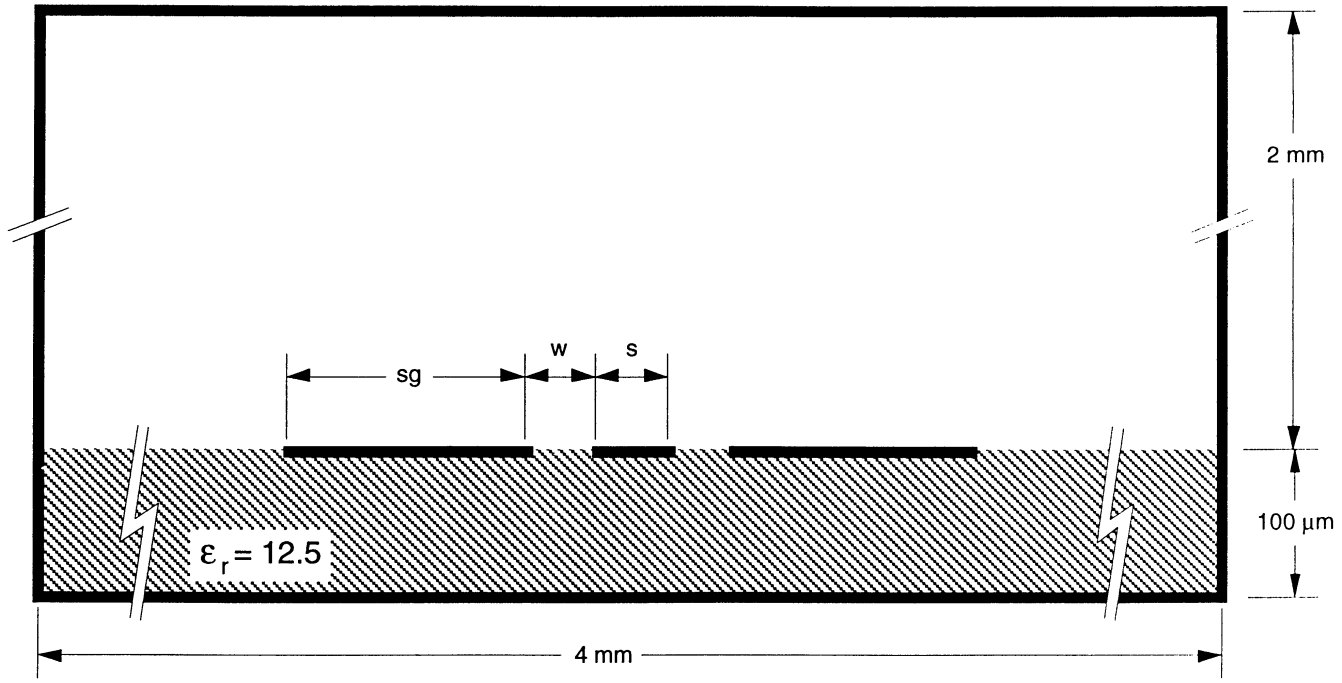


Figure 2

FDTD Analysis of FGCPW

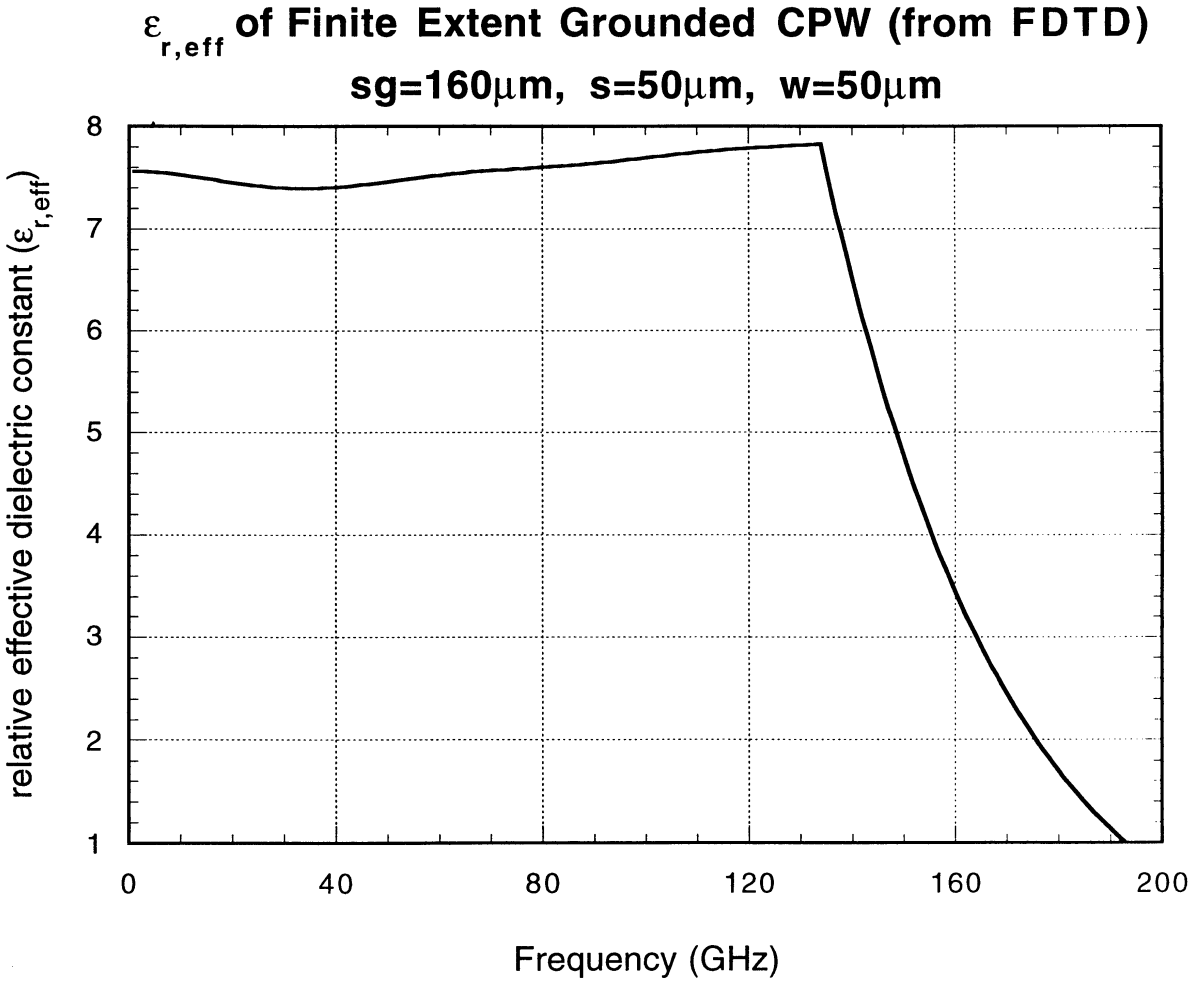


Figure 3

Results of PMM Analysis

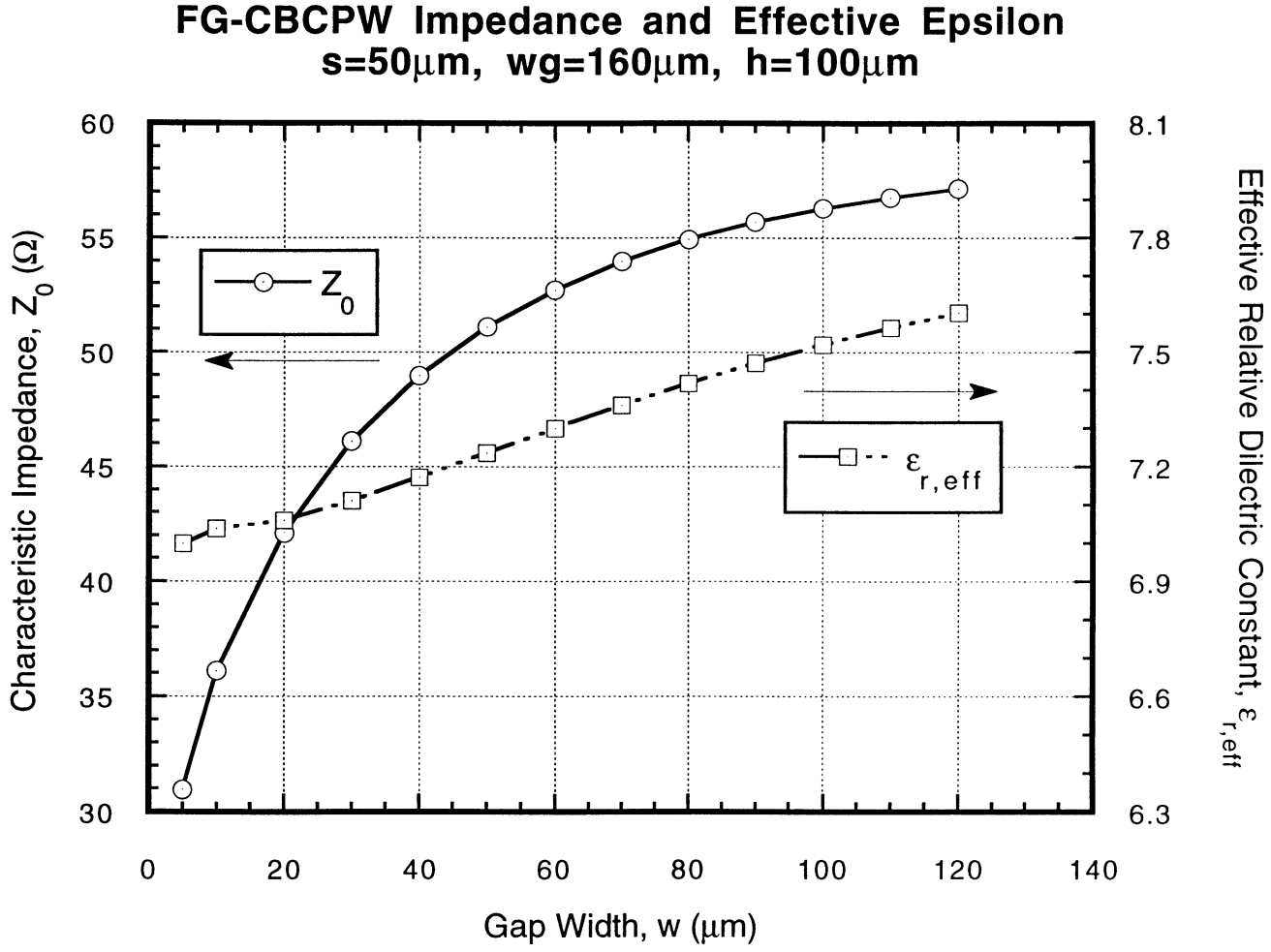


Figure 4

Results of 2-D FEM Analysis

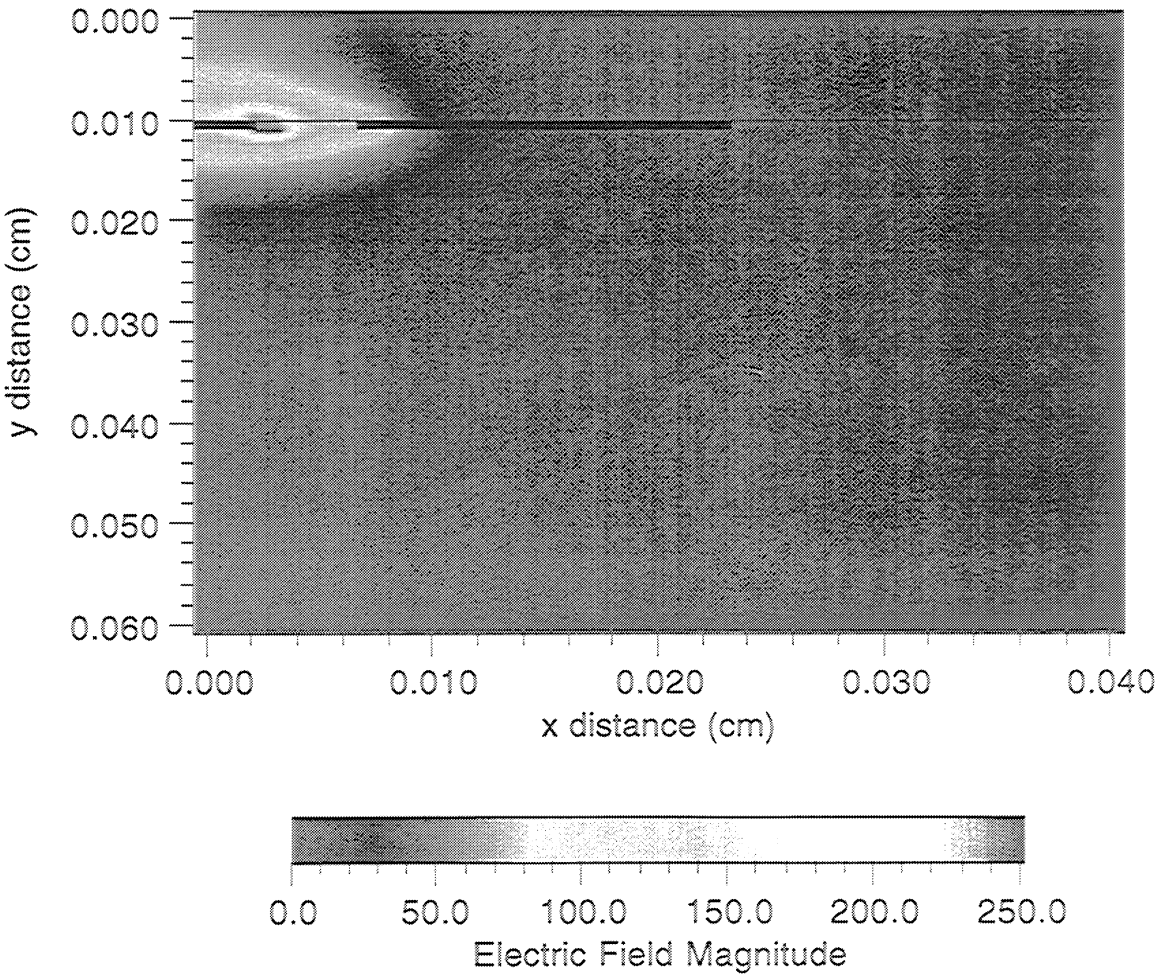


Figure 5

Modeled Filter Performance

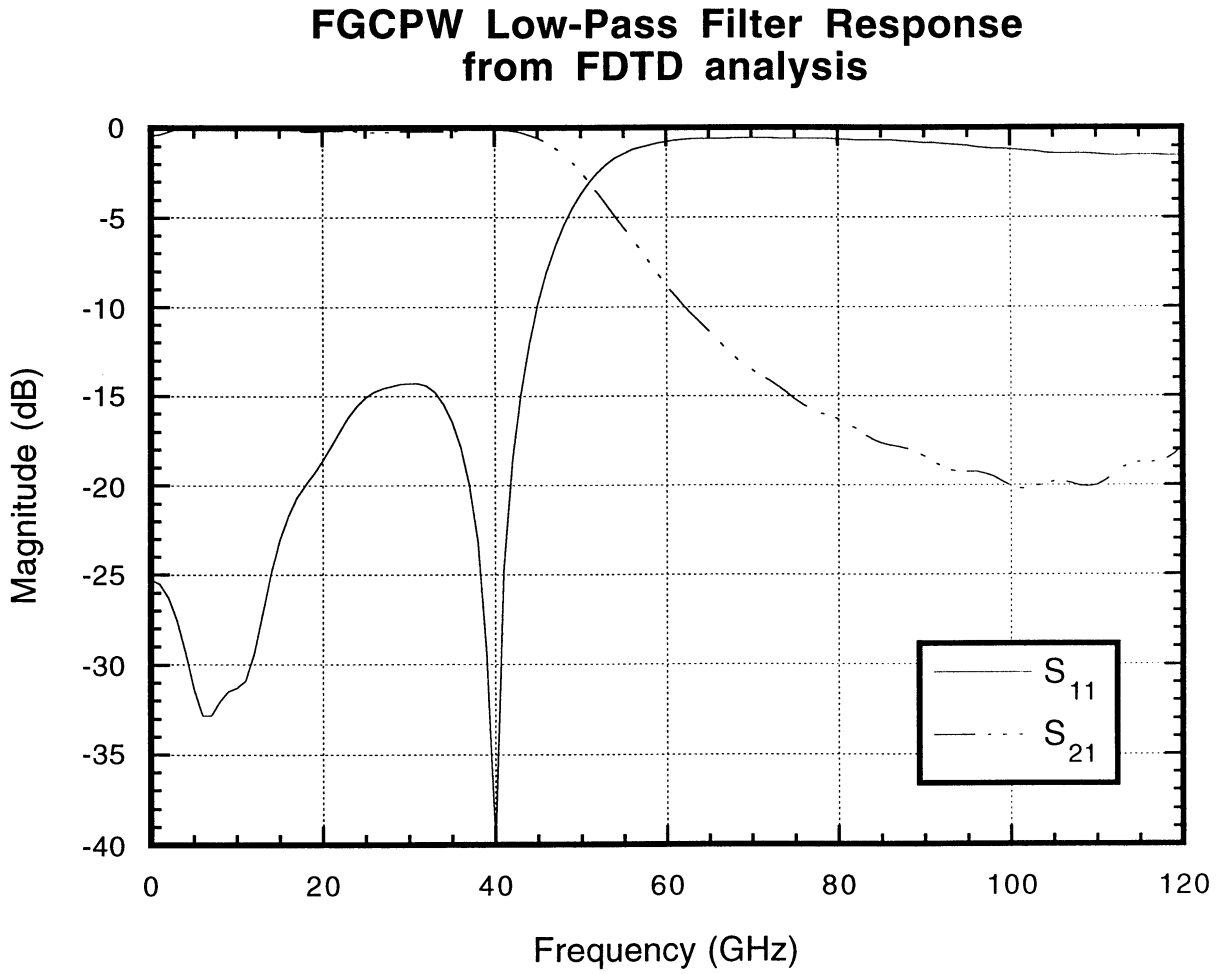
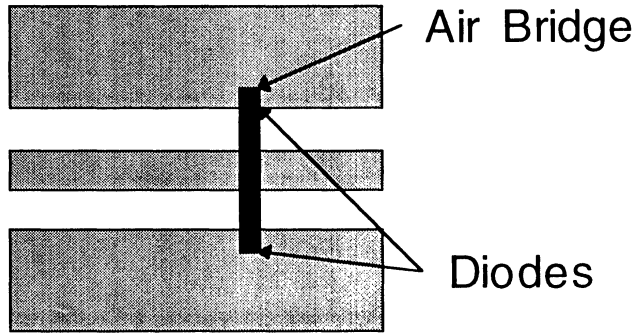


Figure 6

Diode Mounting Structure

- Inductive air bridges form diode anodes
- FDTD simulation provides frequency response of air bridge structure



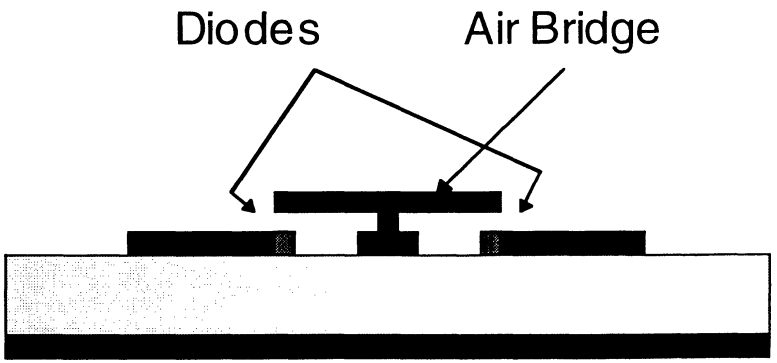


Figure 7

Modeling the Diode Structure

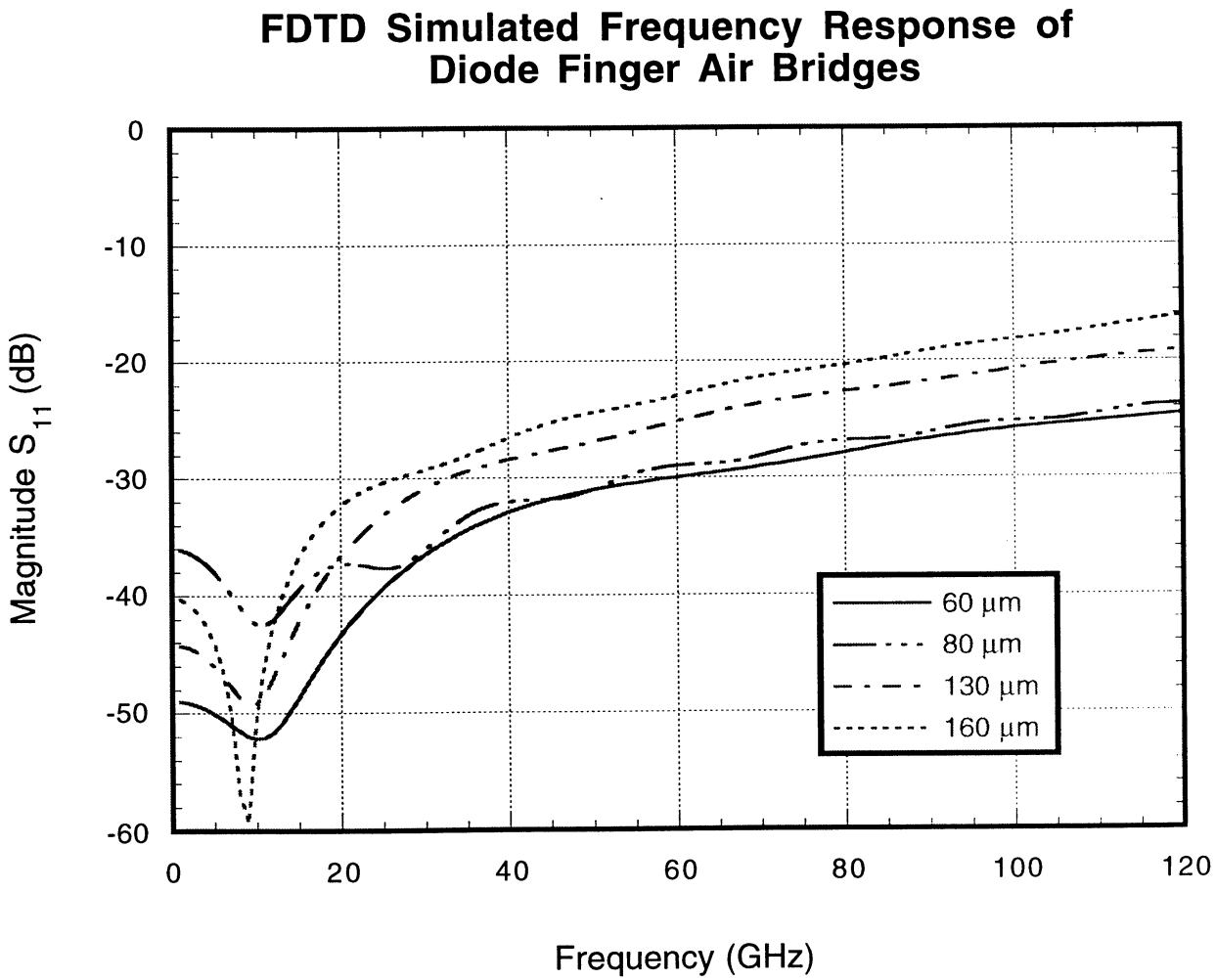
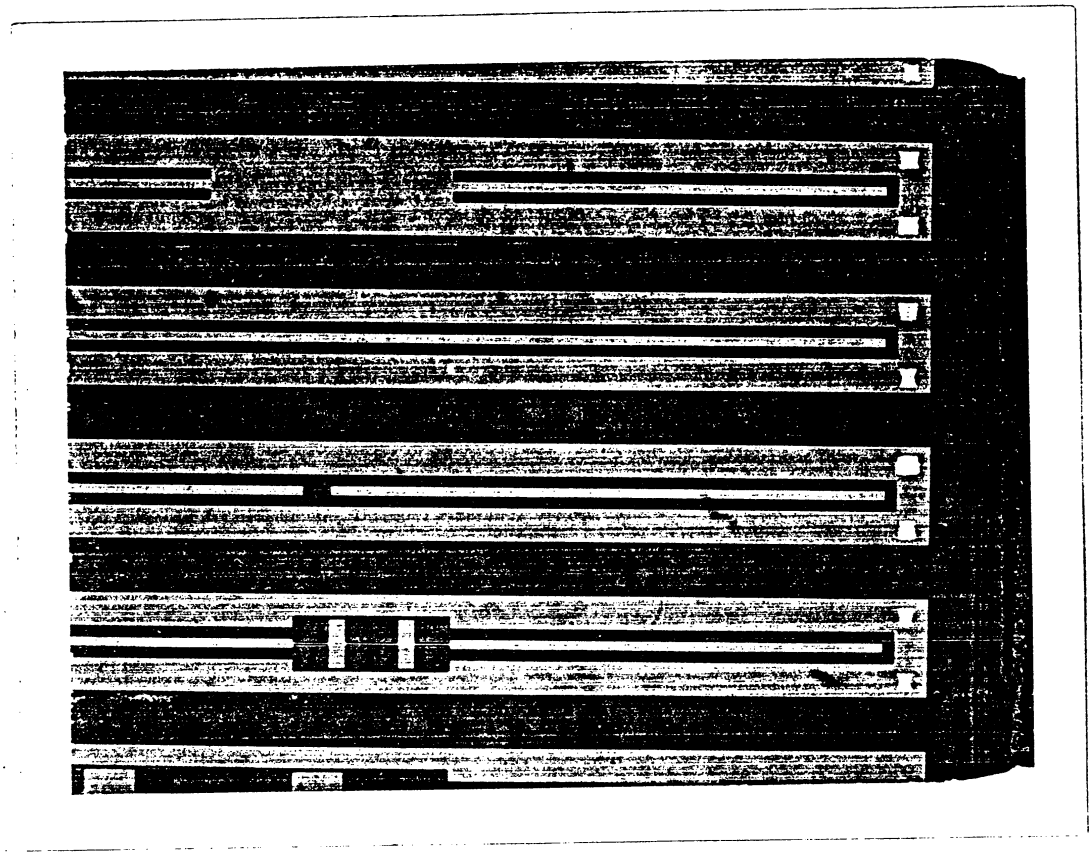


Figure 8

Finite Ground CPW Circuit Fabrication Process

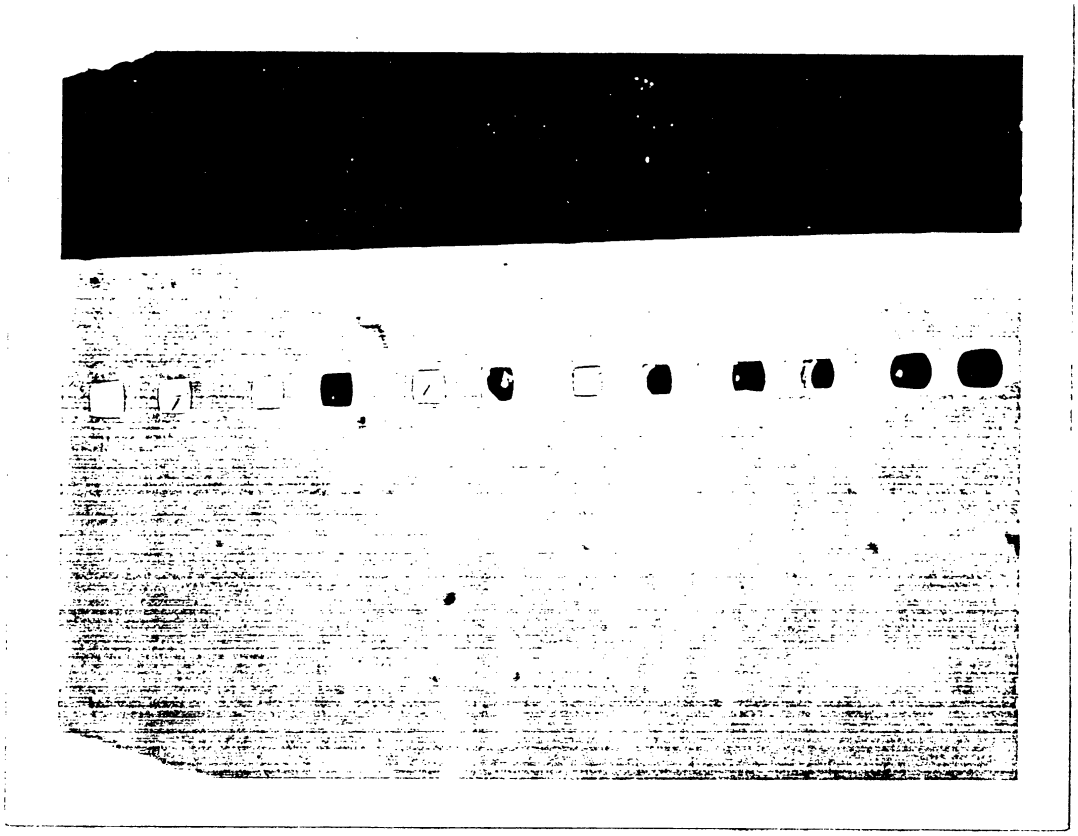
1. Lap substrate to 100μm
2. Define and metalize via holes
3. Make diodes and air bridges
4. Define and metalize circuit lines



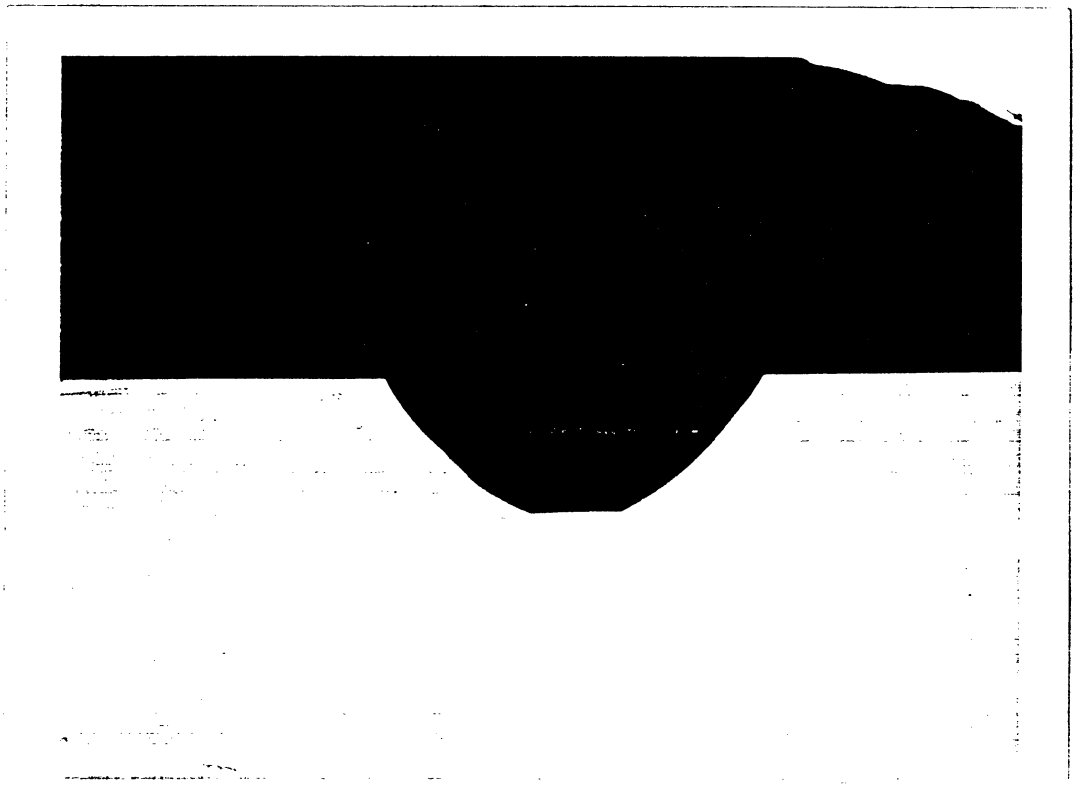
Circuit pattern with via holes

Figure 9

Via Hole Definition



Nonuniform etch



Cross Section View

Figure 10

Finite Ground CPW Test Structures

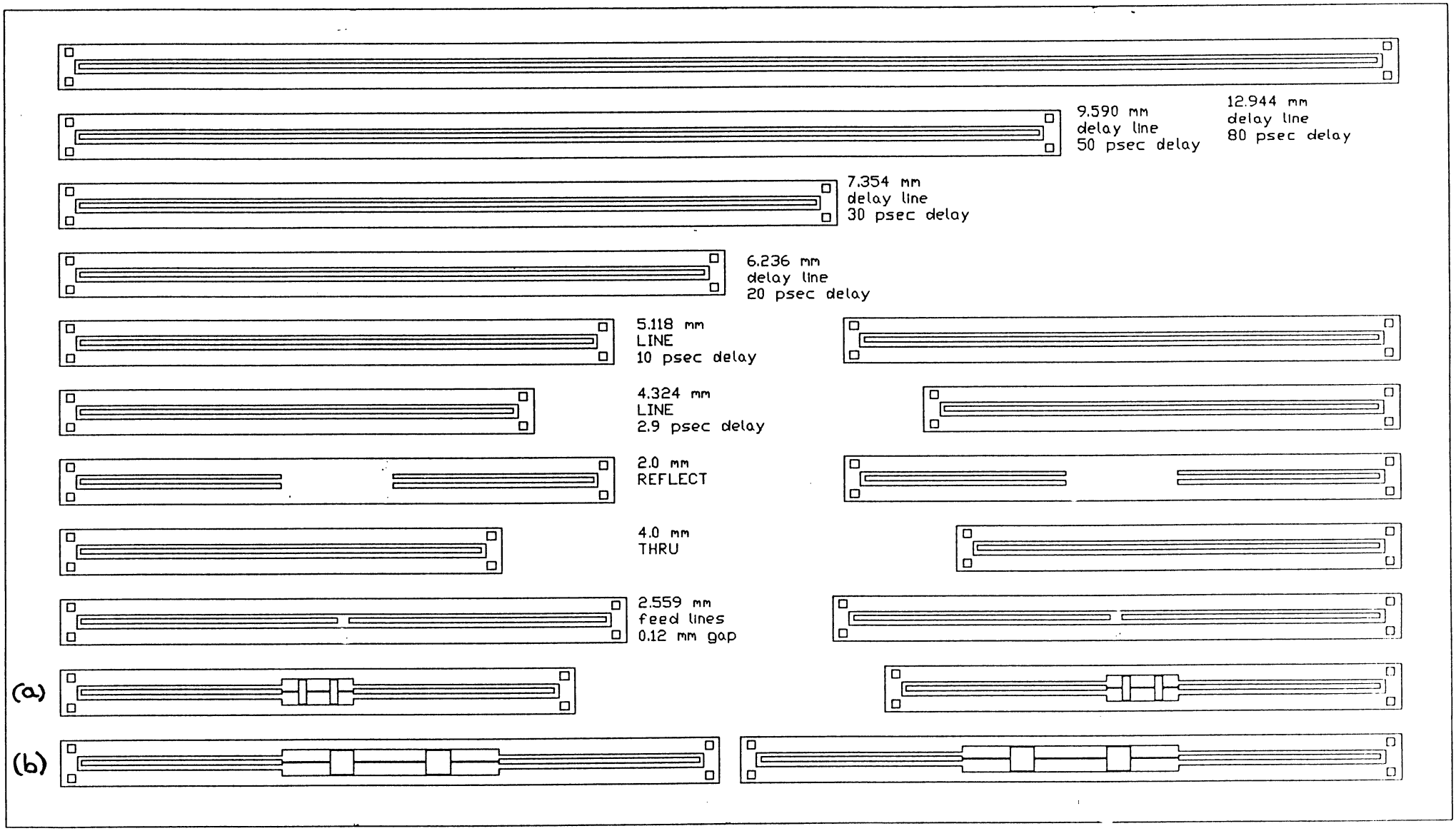


Figure 11

Losses in FGCPW

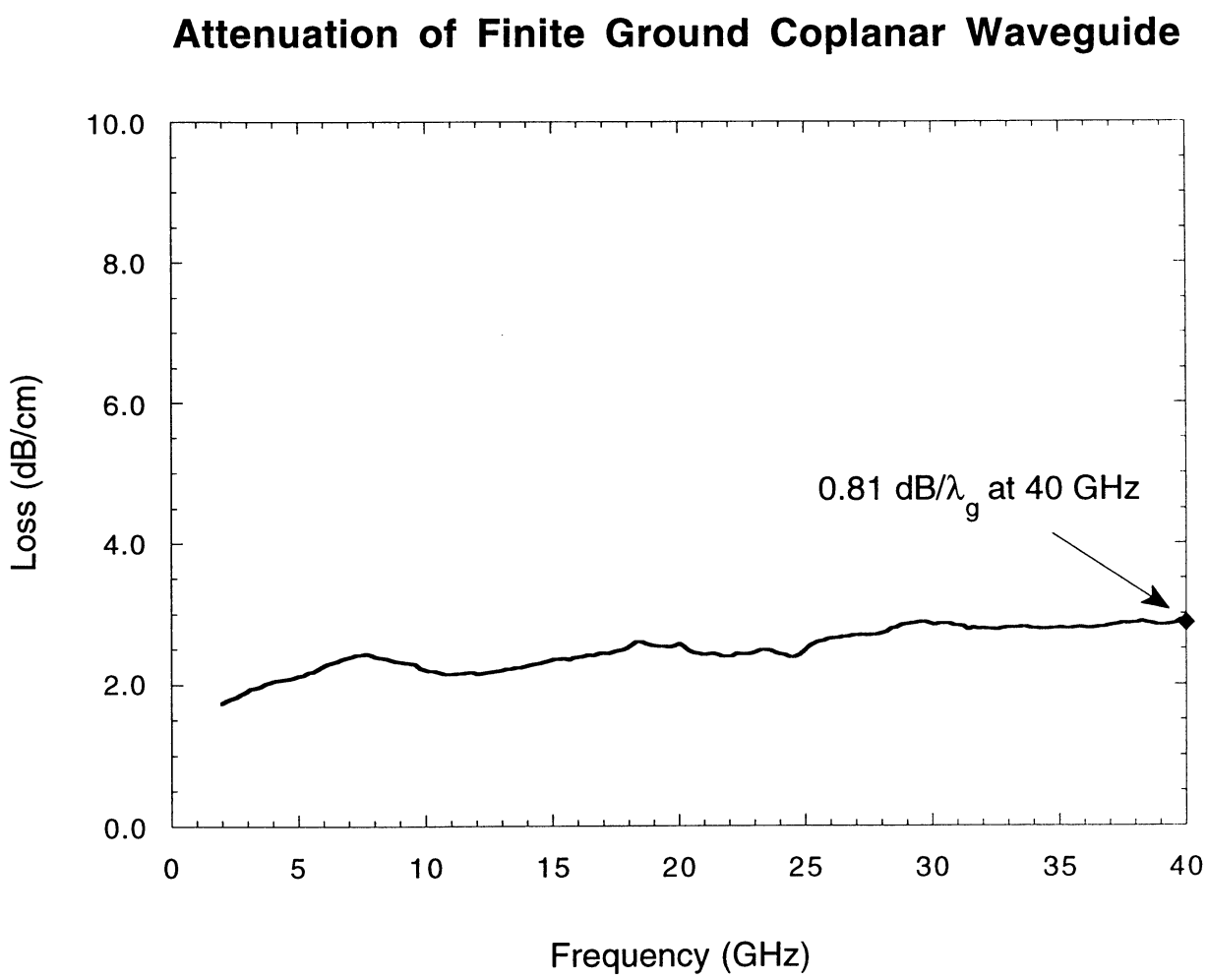


Figure 13

Open End FGCPW Stubs

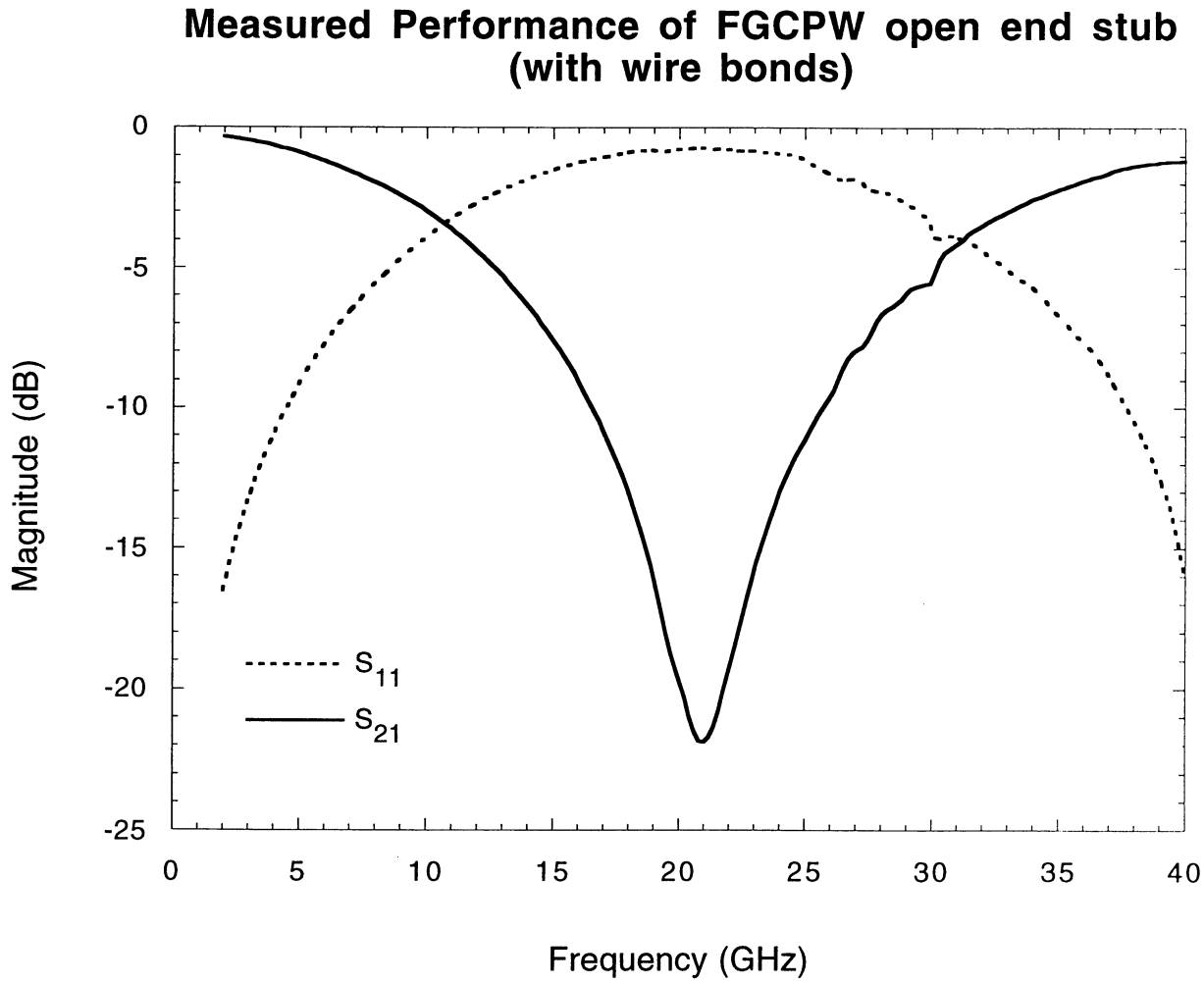


Figure 14

Low Pass Filter (b)

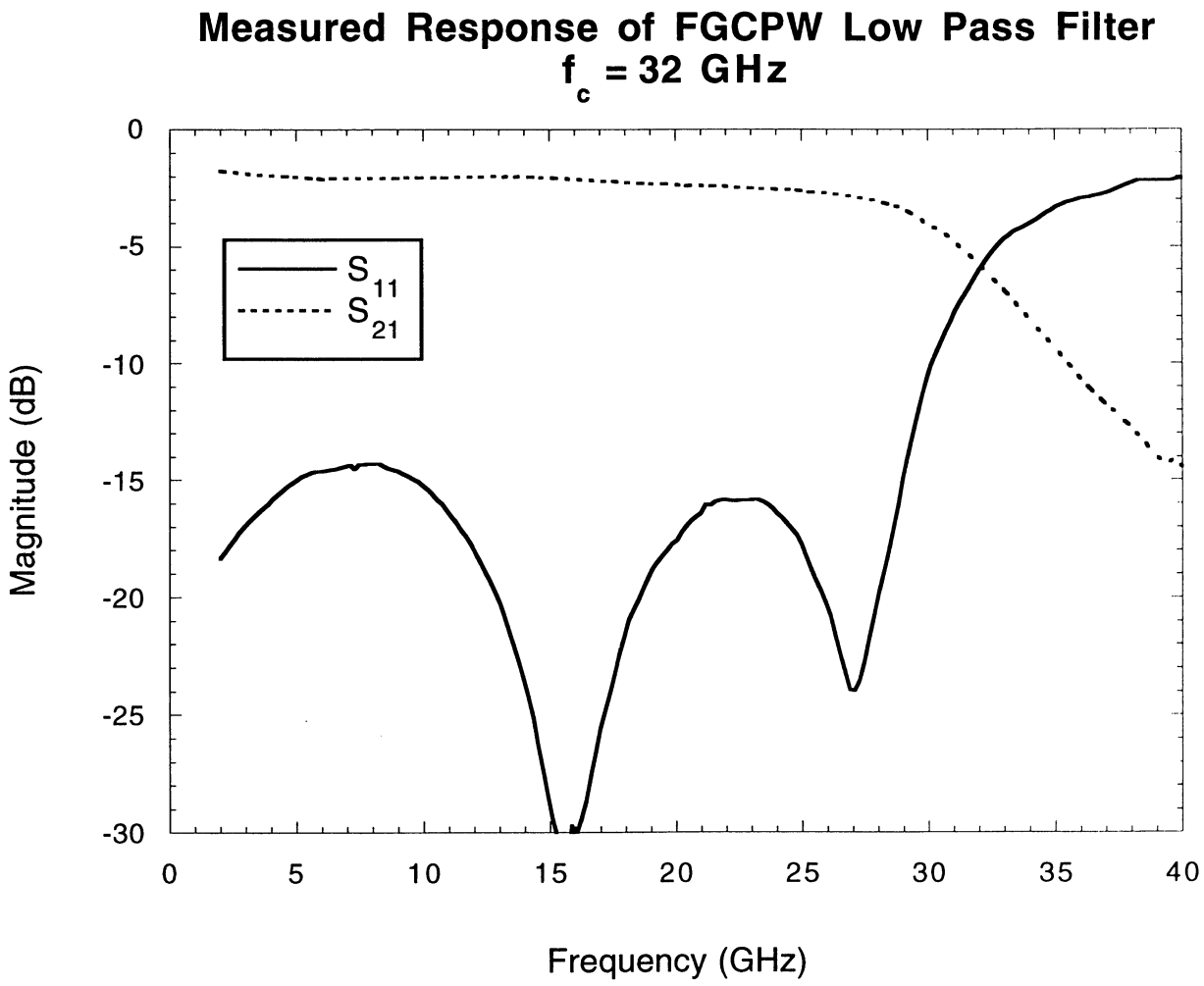


Figure 15

Low Pass Filter (a)

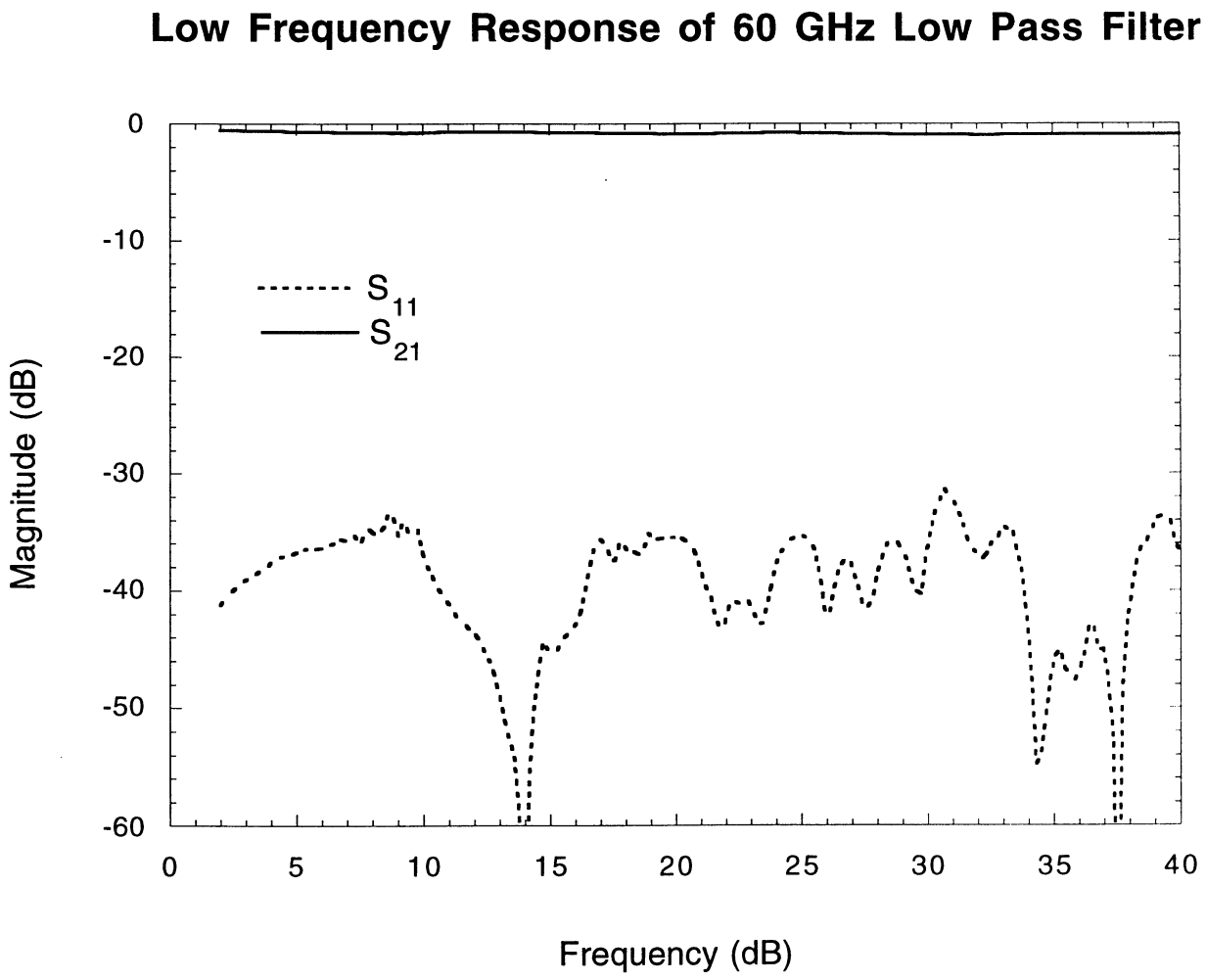
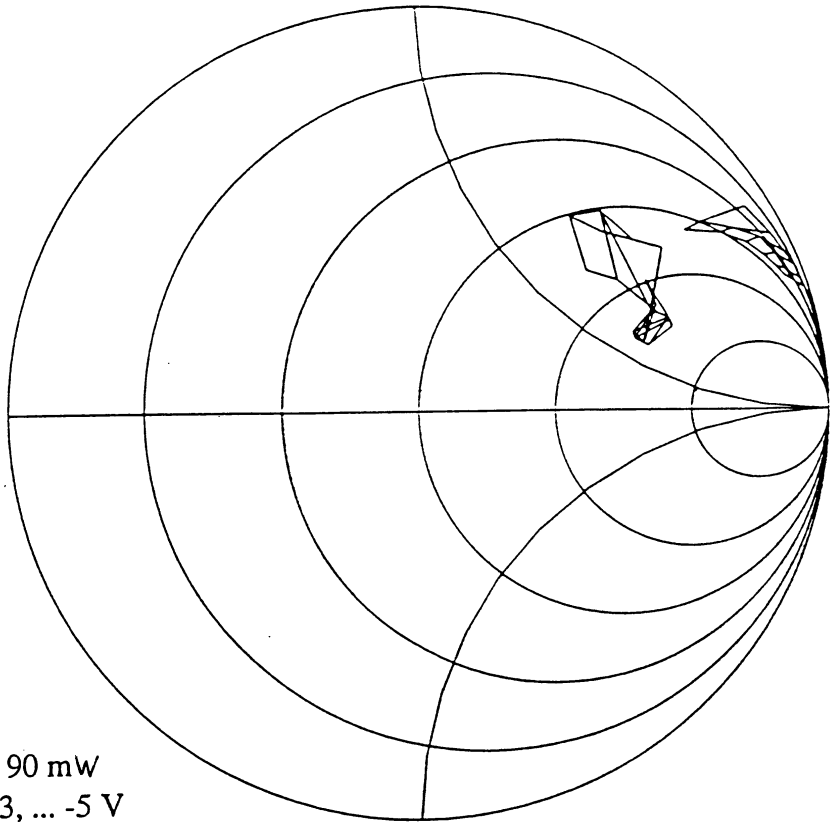


Figure 16

Harmonic Balance Impedance for a Multiplier

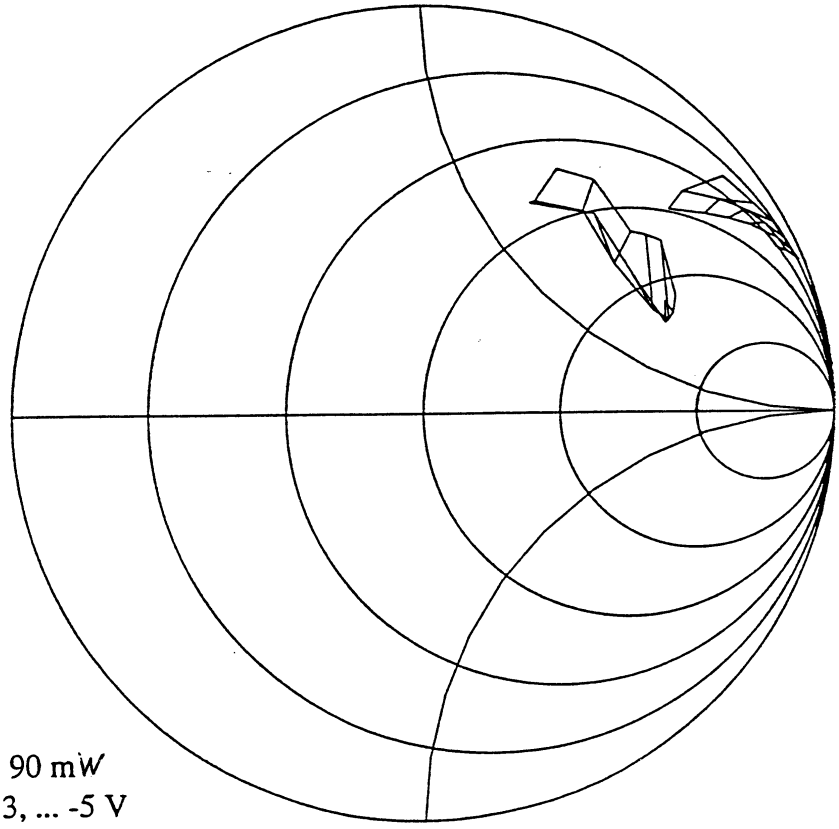
Area = 40e-8
Zc = 50 ohms



Input power: 10, 50, 90 mW
Bias voltage: -15, -13, ... -5 V

Harmonic Balance Impedance for a Multiplier

Area = 50e-8
Zc = 50 ohms



Input power: 10, 50, 90 mW
Bias voltage: -15, -13, ... -5 V

Figure 17