A CLOSED-LOOP DEEP BRAIN STIMULATION DEVICE WITH A LOGARITHMIC PIPELINE ADC

by

Jongwoo Lee

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in The University of Michigan
2008

Doctoral Committee:

Professor Daryl R. Kipke, Co-chair
Associate Professor Michael P. Flynn, Co-chair
Emeritus Professor David J. Anderson
Assistant Professor David Wentzloff

2008

To Mom and Dad

Acknowledgements

In the process of writing this dissertation, any single work was impossible without the inestimable support of many special people. I am deeply grateful to my research advisors Prof. Daryl Kipke and Prof. Michael Flynn for their encouragement and support. I want express my appreciation to all the other committee members, Prof. David Anderson, and Prof. David Wentzloff for their invaluable suggestions and time. I thank the Samsung Scholarship Foundation for the financial support for the entire Ph.D. period, and I also appreciate the support of WIMS ERC and the Catalyst Foundation.

I am deeply indebted to the people at the neural engineering laboratory for their supportive advice and the cordiality: Dr. Matt Johnson, Dr. Kevin Otto, Dr. David Pellinen, Dr. Jeyakumar Subbaroyan, Dr. Mark Lehmkuhle, K.C. Kong, Mohammad Reza Abidian, Nick Langhals, Rachel Miriani, Eugene Daneshvar, Greg Gage, Matt Gibson, Kip Ludwig, Tim Marzullo, Taegyun Moon, Hirak Parikh, Erin Purcell, John Seymour, Azaheh Yazdan, Takashi Yoshida, and Karen Coulter.

I thank all former and current members of Prof. Flynn's group for their assistance with their friendship: Dr. Jia-yi Chen, Dr. Sunghyun Park, Dr. Junhyung Park, Dr. Ivan Bogue, Dan Shi, Joshua Kang, Mark Ferriss, Shahrzad Naraghi, Andres Tamez, Chun Lee, Jorge Pernillo, David Lin, LiLi Lim, and Hyo-Gyuem Rhew.

I am grateful to my beloved family - father, mother, and my brother John for their love, encouragement, and prayer. I thank people at the Korean United Methodist Church,

especially to Rev. Isaac Shin, Dr. Joseph Won, Rev. Kisang Jun, Jason Um, Allison Kim and Jungho Lee. Thanks must also go to the hundreds of friends and teachers, who shaped my life and helped me learn the truth of life. Above all I thank God for His grace and providence.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

Acronym	Expansion
ADC	Analog to Digital converter
AGC	Automatic Gain Control
ASIC	Application Specific Integrated Circuit
CDBS	Closed-loop Deep Brain Stimulation
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog converter
DBS	Deep Brain Stimulation
DNL	Differential Non-linearity
DR	Dynamic Range
DSP	Digital Signal Processing
ESD	Electro-Static Discharge
FDA	Food and Drug Administration
FOM	Figure of Merit
GPe	Globus Palidus Externa
GPi	Globus Palidus Interna
IC	Integrated Circuit

Acronym	Expansion
INL	Integral Non-linearity
INSD	Input Noise Spectral Density
LFP	Local Field Potential
LNA	Low-noise Neural Amplifier
LSB	Least Significant Bit
MDAC	Multiplying Digital to Analog Converter
MiM	Metal-insulator-metal
MSB	Most Significant Bit
NEL	Neural Engineering Laboratory
NIH	National Institute of Health
Op Amp	Operational Amplifier
PCA	Principal Component Analysis
PCB	Printed Circuit Board
PSD	Power Spectral Density
SFDR	Spurious Free Dynamic Range
SN	Substantia Nigra
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
STN	Subthalamic Nucleus
THD	Total Harmonic Distortion

Abstract

This dissertation is a summary of the research on integrated closed-loop deep brain stimulation for treatment of Parkinson's disease. Parkinson's disease is a progressive disorder of the central nervous system affecting more than three million people in the United States. Deep Brain Stimulation (DBS) is one of the most effective treatments of Parkinson's symptoms. DBS excites the Subthalamic Nucleus (STN) with a high frequency electrical signal. The proposed device is a single-chip closed-loop DBS (CDBS) system. Closed-loop feedback of sensed neural activity promises better control and optimization of stimulation parameters than with open-loop devices.

Thanks to a novel architecture, the prototype system incorporates more functionality yet consumes less power and area compared to other systems. Eight front-end low-noise neural amplifiers (LNAs) are multiplexed to a single high-dynamic-range logarithmic, pipeline analog-to-digital converter (ADC). To save area and power consumption, a high dynamic-range log ADC is used, making analog automatic gain control unnecessary. The redundant 1.5b architecture relaxes the requirements for the comparator accuracy and comparator reference voltage accuracy. Instead of an analog filter, an on-chip digital filter separates the low frequency neural field potential signal from the neural spike energy. An on-chip controller generates stimulation patterns to control the 64 on-chip current-steering DACs. The 64 DACs are formed as a cascade of a

single shared 2-bit coarse current DAC and 64 individual bi-directional 4-bit fine DACs. The coarse/fine configuration saves die area since the MSB devices tend to be large.

A prototype device is fabricated in 0.18 μm CMOS with a MiM capacitor option and occupies 2.67 mm^2. The total power consumption of the entire system, including neural amplifiers, log ADC, current DAC, controller and digital filters, , reference generation, clock generation and biasing, is 112 μW in normal operation mode and 351 μW in configuration mode, which is significantly less than that of state-of–the-art stimulator circuits.

Real-time neural activity was recorded with the prototype device connected to microprobes that were chronically implanted in two Long Evans rats. The recorded *in-vivo* signal clearly shows neural spikes of 10.2 *dB* signal-to-noise ratio (SNR) as well as a periodic artifact from neural stimulation. The recorded neural information has been analyzed with single unit sorting and principal component analysis (PCA). The PCA scattering plots from multi-layers of cortex represent diverse information from either single or multiple neural sources. This exploits the benefits of a three-dimensional multi-layer neural probe such as the Michigan probe. The single-unit neural sorting analysis along with PCA verifies the feasibility of the implantable CDBS device for to *in-vivo* neural recording interface applications. To program an optimal closed-loop algorithm, further intensive studies will be necessary to examine the neural pattern changes related to the CDBS treatment. In addition, the CDBS device and implantable brain-machine interface (BMI) unit, has potential for the treatment of other neurological disorders such as stroke, epilepsy and seizure.

CHAPTER I

Introduction

Parkinson's disease is a progressive disorder of the central nervous system affecting more than three million people in the United States [1]. Although the cause of Parkinson's disease is still not fully understood, there have been reports of symptoms related to Parkinson's disease including: tremor at rest, rigidity, bradykinetic movement and postural instability [2]. Deep brain stimulation (DBS) is one of the most effective neurosurgical procedures to alleviate these symptoms. In this chapter, we discuss the biological background and the DBS method. An explanation of the proposed system follows.

1.1. Biological background

The basal ganglia consists of several groups of neuclei that function to process neural information sent from the cerebral motor cortex. The cerebral motor cortex can essentially be thought of as the conscious part of the brain, that is, the part of the brain that makes executive movement decisions. When a decision is made to move a muscle, the sensory-motor part of the cortex sends signals to the deep area of the brain. These signals are received by several regions including the thalamus, basal ganglia and cerebellum [3]. The thalamus is the region where the signals are then relayed down the spinal cord to the muscles, and further processing is done in the basal ganglia [4]. This

processing is subsequently relayed to the thalamus again. A simplified schematic of the neural connections involved with executing a command to move a muscle is shown in Figure 1.1.

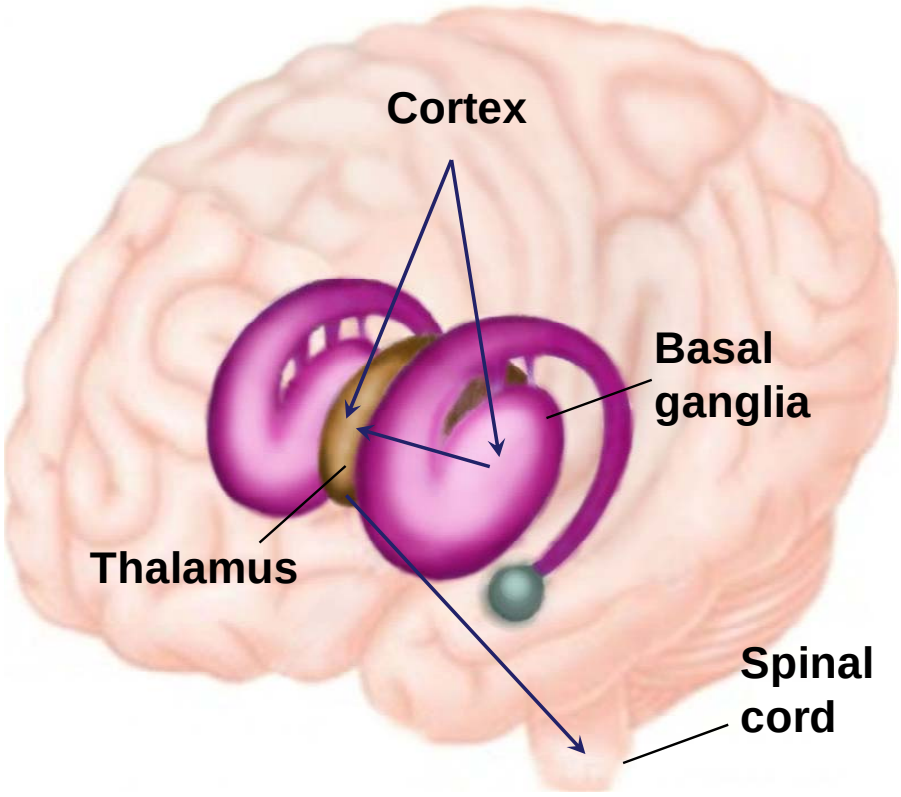


Figure 1.1: A simplified schematic of the neural connections [3].

The processing in the basal ganglia has many functions, among which is judging whether or not a movement is appropriate. In order to accomplish this goal, the basal ganglia have two internal loops, a direct loop that leads to excitatory action on the thalamus, and an indirect loop that leads to inhibitory action on the thalamus [4]. These two loops work side-by-side in order for the brain to properly control desired movements. The basal ganglia network is shown in Figure 1.2 where STN represents the Subthalamic

Nucleus, GPi represents the internal part of Globus pallidus, GPe represents the external part of Globus pallidus. Excitatory connections are shown in green and inhibitory connections in red [5-11].

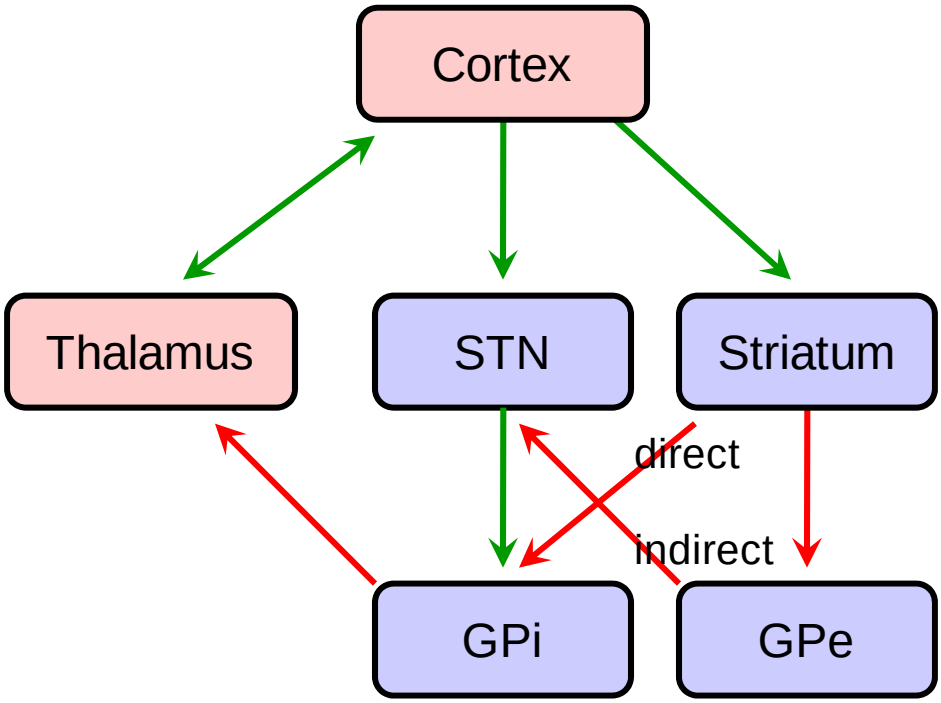


Figure 1.2: The basal ganglia loops [4].

The network shown in Figure 1.2 results in the two loops described above [4]. The excitatory loop is also called the direct loop because it passes directly from the striatum to the GPi and then to the thalamus, this loop contains two inhibitory connections, so the result is excitation of the thalamus. The inhibitory loop, because it has two extra connections, is also called the indirect loop. In this loop, signals pass from the striatum to the GPe, then to the STN and then to the GPi before ending at the thalamus. Because of the three inhibitory connections contained in this loop, the result is inhibition of the thalamus [5].

Because each of these loops is needed for proper function, pathologies occur when either one of them overpowers the other. If the direct pathway overpowers the indirect, there is an excess of excitation, resulting in a hyperkinetic state, such as Huntington's disease [6]. On the other hand, if the indirect pathway overpowers the direct, there is excessive inhibition of the thalamus, leading to a hypokinetic state, such as Parkinson's disease [6-8]. The symptoms of Parkinson's disease are revealed as inability to execute the desired movements introduced above. Parkinson's disease is correlated to a decrease in the functioning of another basal ganglia nucleus, the Substantia Nigra (SN)[9]. When SN function is limited, the result is an increased signal being passed between the striatum and the GPe and a decreased signal being passed between the striatum and the GPi. This leads to the excessive inhibition of the thalamus described above [10-11].

There are several treatments currently used to alleviate Parkinson's symptoms including medications and neurological surgeries. One is the administration of levodopa, a drug that is the precursor to the dopamine which is the neurotransmitter secreted by the SN [12]. This treatment has the side effect of exposing the body to high amounts of dopamine that can lead to other neurological problems such as nausea [12]. Another treatment is the ablation of the GPe to stop the indirect loop by removing one of its components. Clearly, the ablation of a group of brain cells is a very invasive procedure and can lead to many problems if any additional cells are destroyed. A treatment that is currently not used, but has promise in the future is transplantation, implanting new cells, or to use stem cells to create a new SN for the patient [2]. This method would function to restore normal dopamine levels in the area of the basal ganglia, but not throughout the

entire body as in the levodopa treatment [10-11]. While this method could work well in the future, it is several years off at best.

The other treatment for Parkinson's disease is DBS which delivers high-frequency electric stimulation to excite several parts of the basal ganglia including STN. DBS is a very effective neurosurgical procedure for the patients whose condition cannot be controlled with medications [12]. A thin, insulated wire or micro-machined electrode is surgically implanted into the deep brain target such as STN or GPi as shown in Figure 1.3. While the mechanism of the DBS works is still unknown, it seems that the high frequency nature of the signal acts to diminish the effectiveness of the inhibition on the thalamus.

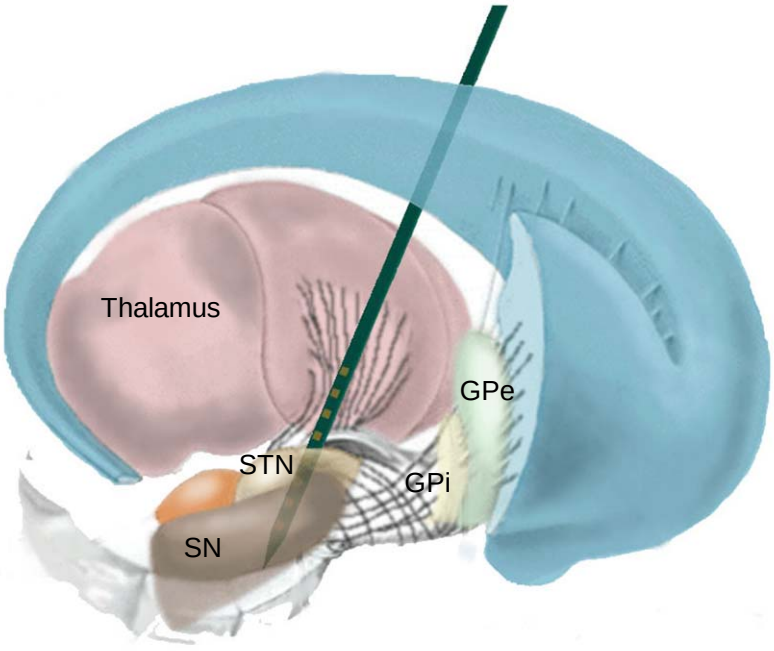


Figure 1.3: Placement of the DBS probe into STN [14].

1.2. Deep brain stimulation (DBS) system

DBS has become a widely applied treatment of advanced Parkinson's disease since 1997 when the United States Food and Drug Administration (FDA) approved unilateral DBS systems to treat Parkinson's disease [15-16]. A medical technology company named Medtronic [17], that is seen these days, supplies bilateral DBS devices. Bilateral DBS devices, which were approved by FDA in 2002, consists of two neurostimulators. One for each side of brain [15-16]. Similar to a cardiac pacemaker, the DBS uses a neurostimulator to generate and deliver high-frequency electric pulses into STN or GPi through extension wires and electrodes. The Soletra neurostimulator, introduced as the most advanced battery-operated device from Medtronic, has the dimension of 55 mm × 60 mm × 10 mm and the weight of 42 g as shown in Figure 1.4 [18].

Figure 1.4: Soletra neurostimulator and DBS lead [18].

The neurostimulator is fairly large size and is subcutaneously implanted under the clavicle as shown in Figure 1.5 [19]. An insulated extension wire runs up under the skin of the shoulder, neck, and head to deliver the stimulation pulses. The stimulation pulses are generated from the neurostimulator to the electrodes implanted into the deep brain area through a burrhole in the skull. Unfortunately, several hardware complications have been reported that affects more than 26% of the patients [20]; this includes infections during the surgery, extension erosion, lead wire fracture and malfunction of the neurostimulator. These surgical complications incidents may be reduced by a smaller size and stand-alone device which doesn't require any extension wire.

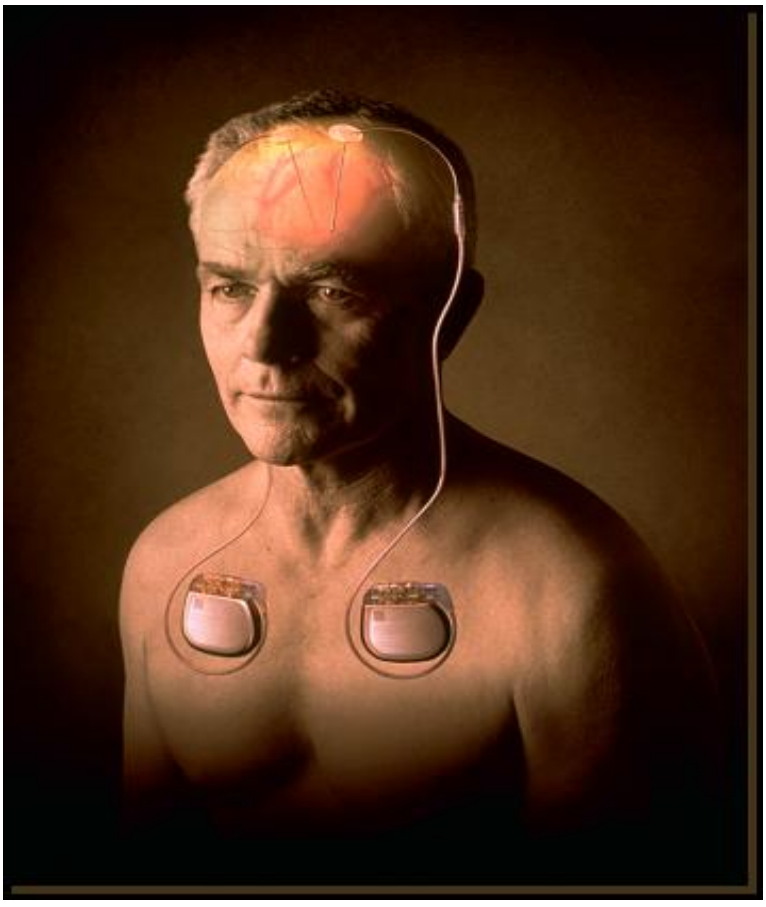


Figure 1.5: Placement of the Medtronic DBS™ system [19].

The Medtronic neurostimulator is programmed post-surgery by trained technicians to find the most effective signal parameters for alleviating Parkinson's symptoms. However, it can take up to one full year to find the best parameters for patients [21]. The effective signal parameters are amplitude, frequency, and pulse-width. This effective signal matching process is still not well understood. The only current feedback mechanism is the visual sign of tremor attenuation. Every patient has a unique set of signal amplitudes, frequencies, and pulse widths that are effective to treat their disease. Thus patients who are being implanted with DBS have to visit their doctors frequently to get fine tuned adjustments of their stimulation parameters. If any internal information from the brain in Parkinson's state is sensed, then the proper parameters can be found automatically by a dedicated microprocessor without the intricate travel to a medical center.

The strongest candidate for the internal feedback signal is an abnormal pattern change in neural spikes or field potentials from normal status when Parkinson's disease symptoms occur. Normally, it is shown that spike signals have bandwidths with 100 Hz to 10 kHz and amplitude levels up to ±500 μV, and local field potentials (LFPs) have bandwidths with 1 Hz to 50 Hz with amplitude levels up to ±10 mV. An excessive power of a 15 – 30 Hz low frequency field potential from the extracellular recording of rat's cortex has been delivered [22]. To measure the extracellular neural activities, multi-channel microprobes are used. It has an ability to record a neural population activity in the form spike trains as well as slower LFPs. Also, the microelectrodes must deliver the localized electric stimulation for an extended period up to 5 years without damaging brain tissue [23]. For the clinical usage in humans, the electrode should be at least 10 cm

in length and small cross-sectional area. This helps to minimize tissue damage and fits to standard stereotaxic tools with stable and biocompatible characteristics [24]. Also, the electrode should be stiff enough to resist insertion forces during surgery and be able to position the probe channels precisely closed to the small STN [25].

The collected neural signals from the microelectrodes should be conditioned using front-end circuits such as pre-amplifiers and analog-to-digital converters (ADCs). Due to the low-level amplitude of the neural spikes, integrated pre-amplifiers have been used to amplify the small signals before the data conversion [26]. The front-end design should be low-noise to guarantee the signal integrity, and low-power. During the last decade, several types of the front-end neural recording circuits have been proposed [27]. In the earliest work, Ji *et al*. [28] at the University of Michigan presented an active integration of the multi-channel microprobes with complementary metal-oxide semiconductor (CMOS) circuits. However, the pass-band gain is unstable and the dynamic range is limited by a large direct current (DC) offset [29] which depends on the electrode-tissue interface. To stabilize this random DC potential, Mohseni *et al*. employed a shunt resistor connected to the electrode input [27]. This parallel resistor provides a short path for DC signal while the alternating current (AC) gain change rarely. It can be used only for an acute neural recording since the impedance of the microprobes varies along the time for a long-term experiment. A single-chip integration of pre-amplifiers, an ADC and telemetry has been proposed by Song *et al*. at the Arizona State University [30]. Recently, more advanced wireless integration with 100 neural recording channels has been developed by Harrison *et al*. at the University of Utah [31].

However, most of the work focused only on the neural spike recording, and there is no truly stand-alone, small-scale system for recording both spikes and LFPs simultaneously, because of the challenges imposed by their signal characteristics. To cover the entire range of both small-signal neural spikes and large-signal LFPs, a high dynamic range ADC is needed to digitize all the desired neural information.

Unfortunately, many researchers are still trying to discover the DBS locations in the deep brain area where DBS are most effective in alleviating Parkinson's symptoms [32]. Also, accurate positioning of the DBS electrode is an active research field [25]. Multichannel stimulation distributed throughout the target nuclei with microelectrodes can be a good solution for this issue if the system provides precise independent site control with a programmable spatial stimulation. In spite of growing interests in DBS research, engineering development is only limited into DBS electrode.

1.3. Proposed closed-loop deep brain stimulation (CDBS) system

This project is focused on developing a small-size and implantable CDBS device that searches for unique parameters of electric stimulation to treat the Parkinson's disease. The proposed device has neural recording front-ends, fully programmable stimulating channels, and a microprocessor that runs a programmable algorithm that takes recorded neural signals as feedback and calculates the parameters that attenuate the symptoms of the disease. A 16 channel, single-shank recording electrode is implanted on rat's Motor cortex while a stimulating electrode is implanted on STN to provide stimulation current for Parkinson's disease treatment. Thus, the project hypothesized that

there is a specific neural pattern in the Parkinson's state and also there is the most effective stimulation parameters to alleviate the symptoms of abnormal patterns of neural information.

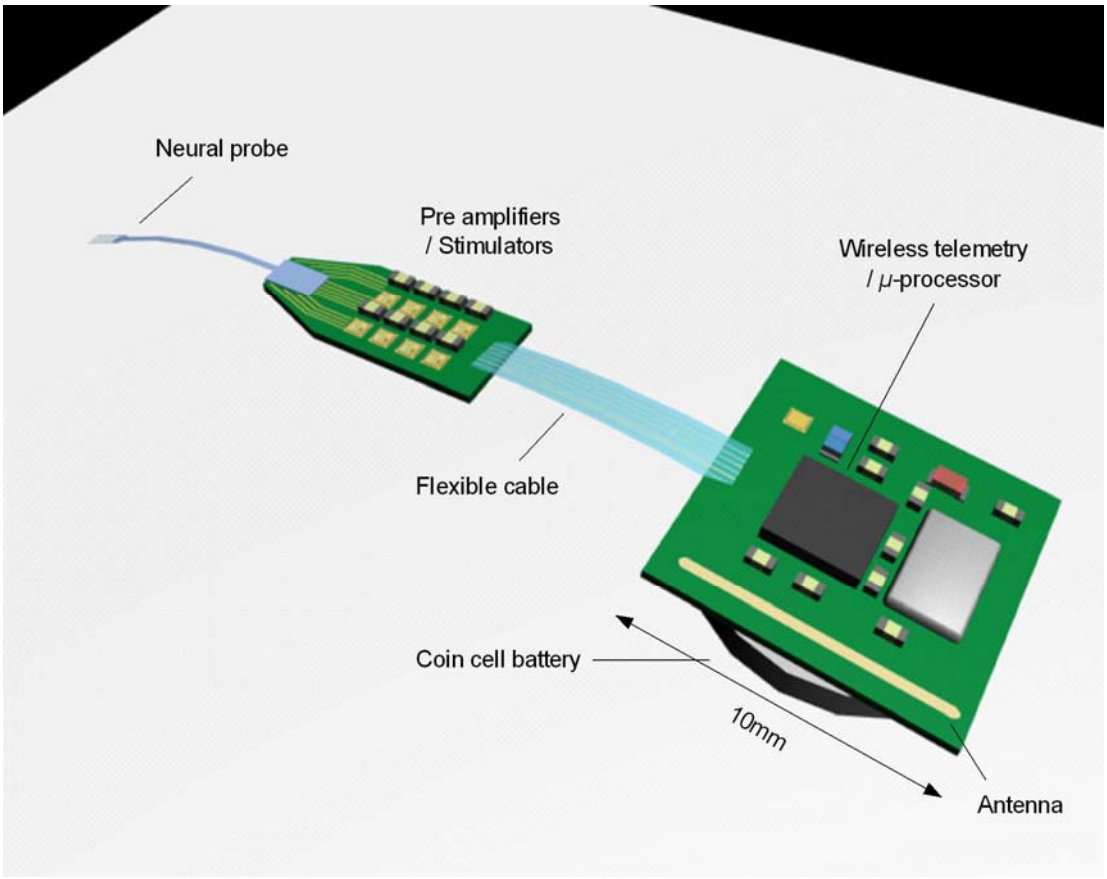


Figure 1.6: Prototype model of the first CDBS system.

The prototype system has been developed in two successive phases. The first system was built with commercially available parts, including instrumentation amplifiers, linear ADC, micro processor, wireless telemetry units for external monitoring and a coin cell battery as shown in Figure 1.6. The first generation device was used for the functional derivation of the closed-loop system. The second phase is an integrated single-

chip application-specific integrated circuit (ASIC) containing 64 channel programmable stimulating circuitry, eight channel neural front-end, high dynamic-range logarithmic ADC, and a dedicated controller to set the stimulation parameters.

This small-scale ASIC device have many advantages: the minimized surgical complications because of the removal of extensions, the self-configurative parameter setting with an advanced neural interface capable of simultaneous neural recording of spikes and LFPs, and the fully-controllable multi-channel stimulation for the precise target positioning, as discussed in the previous section.

Figure 1.7 shows a block diagram of the integrated CDBS device including a wireless transmission for the post analysis of processed neural data by an external inspector.

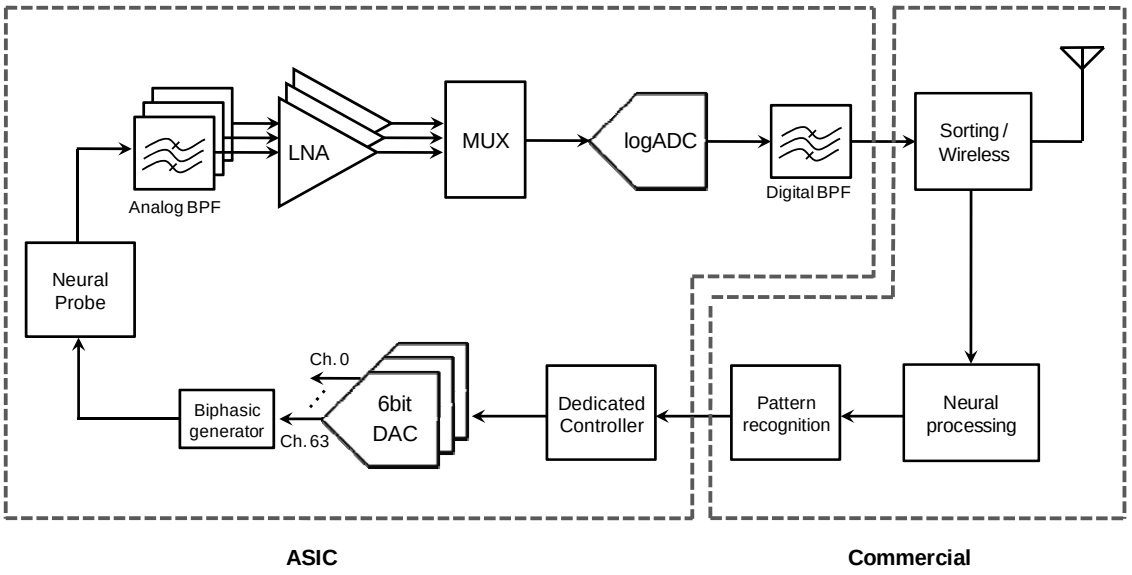


Figure 1.7: Block diagram of the proposed CDBS system

Two multi-channel neural probes were implanted in the Motor cortex and STN, respectively. These are used to deliver the sensed neural signals and the stimulation pulses. The recorded neural waves are fed through individual low-noise neural amplifiers (LNAs) containing analog band-pass filtering and multiplexed into a single high dynamic-range pipeline logarithmic ADC. The proposed logarithmic ADC exploits the fact that the neural spike characteristic works on a companding scale. The most suitable way of encoding neural spikes is to use a variable resolution depending on the signal amplitude. The desired dynamic range is the span of spike magnitudes from neighbor neurons which generate action-potentials (APs). Since a higher dynamic range can be achieved for a given word length with a properly designed logarithmic conversion [33], it provides more efficient way to cover the entire dynamic range of both neural APs and LFPs than conventional linear encoding. Digitally converted neural data is filtered out by finite-impulse-response (FIR) digital filters to separate the neural APs and LFPs for the post processing. The employment of the digital filters has the benefit of reducing power consumption.

A microprocessor analyzes the neural patterns to classify the Parkinson's state, and to search for the most effective stimulation variables for the multi-channel current stimulation. The parameters decide the pulse shape of the stimulation. A bi-phasic pattern is used to minimize the remainding charge supplied to the tissue. A 64 channel current steering digital-to-analog converter (DAC) is used to form the desired pulse generation. The 64 DACs are based on a new (2+4) bit structure formed as a cascade of a single shared 2-bit coarse DAC and 64 individual 4-bit fine DACs. This format saves as much as an order of magnitude circuit area and delivers sufficient stimulation performance.

Parkinson's disease needs to be better understood so a feedback algorithm can be designed. To facilitate research progress in this field, there is a need for the wireless monitoring link to an external host personal computer (PC) located outside the body. The wireless telemetry eliminates the large bundle of multi-channel wiring and the environmental noise from these cables. Also, it does not restrict movement of animals or humans [34]. The proposed system employs a 2.4 *GHz* radio-frequency (RF) transceiver capable of 1*Mbps* data rate communication for the physiological monitoring. The 2.4 *GHz* frequency band is allocated for industrial, scientific and medical (ISM) usage by US Federal Communications Commission (FCC) [35]. And, a 1*Mbps* data rate provides a sufficient bandwidth for the simultaneous multi-channel neural data streaming.

1.4. Dissertation outline

The biology of Parkinson's disease and the current DBS system is reviewed, and new architecture for the closed-loop techniques to improve performance has been introduced. This work is also relevant to other circuits and systems for the brain-machine interface systems that use neural interfaces.

Since the front-end circuitry of the proposed system is based on the micro-scale implantable neural interfaces, the research advances in multi-channel micro-electrode arrays and implantable neural recording devices in recent decades are reviewed in Chapter II. Also, a prototype of the multi-modal and cascaded switched-capacitor device provides simultaneous recording of both neural APs and LFPs with better noise performance, is discussed although it is not included in the CDBS ASIC, The logarithmic coding technique for high dynamic range is given in Chapter III. This high dynamic range provides the entire coverage of the neural APs and LFPs without need for the two-stage pre-amplifier introduced in Chapter II. The prototype circuit implementation of the CDBS ASIC device contains neural front-ends for both recording and stimulation as well as digital filters and controller, is presented in Chapter IV. The *in-vivo* test method and the measured neural data from an animal brain are described in Chapter V. Finally, the thesis is concluded in chapter VI with a summary and suggestions for future work.

CHAPTER II

Micro-scale implantable neural interface

Multi-channel microprobes are used to investigate the structure and mechanism of neural networks. These microprobes are capable of recording neural population activity in the form of spike trains as well as slower local field potentials (LFPs). Both of these signal types provide unique information about biologically relevant time and spike pattern predictions. In some cases, implantable pre-amplifiers have been used to amplify the weak neural signals for the post processing, but most applications utilize external signal conditioning. In this chapter we will review the research in the micro-machined neural electrodes and the integrated front-end circuit for processing spikes and LFPs. This is important background information for the front-end recording channels of the proposed closed-loop deep brain stimulation (CDBS). In addition, a prototype of the two-stage, multi-modal, and simultaneous neural recording device is presented.

2.1. Hybrid integration of neural probes

Implantable neural microprobe arrays enable sophisticated investigations of the structure and mechanisms of neural networks [36-37]. Recent studies in brain-machine interfaces have emphasized using LFPs as input signals, especially when chronically implanted devices lose their functionality for recording unit-spike activity [38-41].

Moreover, studies have also suggested that spikes and LFPs may encode different information [42, 43].

The development of micro electro-mechanical system (MEMS)-based implantable microelectrode arrays, which began with the seminal work of Wise, et al. [44], is an active research area in a number of laboratories [45]. Micro-fabricated probes provide a number of unique advantages including: precisely defined thickness and shape, customizable electrode size and configuration, and batch-fabrication. They also facilitate the use of many electrode sites, or in other words, many parallel recording channels.

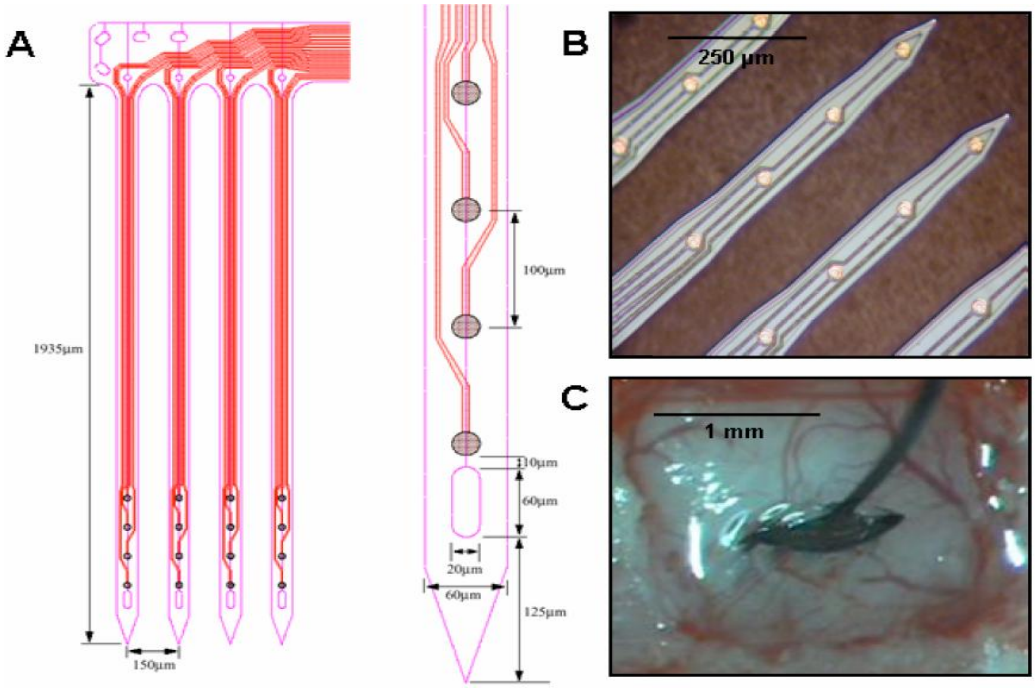


Figure 2.1: Neural microprobe (NEL, U of Michigan) [46].

Figure 2.1 shows the passive neural microprobes made by a MEMS process with thin film of sensing sites and conducting leads. The microprobes are fabricated with a

silicon substrate whose shape and thickness are precisely decided using boron etch-stop micromachining. The substrate contains a conducting array of metal recording sites and Polysilicon leads that are insulated by thin-film dielectrics. On the upper side of the dielectrics, there are metal exposures for the contact with the tissue and the bonding pads for the signal delivery to the interface devices [46]. The extensibility of the microprobe enables custom designs for various applications including the multi-plane arrays for the precise three-dimensional placement of recording sites in the brain [47], and the connection with a polymer ribbon-cable to intensify mechanical flexibility [48]. In addition, probe designs can expand containing micro-fluidic channels along the shanks for drug delivery through the blood-brain barrier [49].

The small size of complementary metal-oxide semiconductor (CMOS) integrated circuits makes this technology useful for large-scale processing of neurophysiological signals. The scalability of the micro-fabrication technology enables active integration with electronic circuits for signal conditioning. Since active probes employ front-end circuits, noise and distortion from the environment are buffered before transmitting the signal through wired or wireless links to a data acquisition system. In addition, active probes provide the possibility of digital signal processing (DSP) such as data compression and spike sorting at the front-end to enhance signal integrity and reduce the number of tethering wires. Active probes have two types of integration – substrate integration and hybrid integration. The substrate type of active probes integrates electronics onto the probe substrate [50] and the hybrid type integrates electronics on a separate chip [51-53]. However, while commercial CMOS circuit technologies have been reached at already impressive acceleration down to the sub-micron scale, the MEMS

processes for the electrode fabrication stays at the multi-micron phase that is basically little changed over the last two decades. The imprecision of the MEMS process limits the large-scale integration (LSI) circuitry in the substrate active integration.

For large channel count integration, the hybrid type integration is preferable through a mixed device in which the probe substrate and electronics are fabricated on separate wafers. The hybrid probe has several advantageous attributes including high-density integration to include on-chip electronics for DSP and wireless transmission for no tethering force [51]. Separate electronics with state-of-the art circuit technology increases the density of integration and the number of channels. For example, for a given circuit design, the circuit fabricated in 90 *nm* technology can contain 1000 times more electronics than that in substrate integration with 3 μm feature size. The front-end recording interface circuits are discussed in detail in the next section, as will a proposed simultaneous recording device.

Contrary to the neural recording probes, DBS electrodes deliver relatively large electric current pulses for stimulation. In order to apply DBS devices with the optimal functionality, diverse long-term stimulation research (in a proper animal model such as rats) is needed. Since a deep-set STN of a rat is tiny and is located in the deep brain area far away from the surface (about 10 *mm*), the DBS electrodes are designed to allow accurate positioning in the basal ganglia [23] and sufficient stiffness to resist insertion forces during surgery [24]. In addition, the electrodes must be bio-compatible to avoid chronic tissue response, have a sharp tip and a tapered shank for the minimally invasive design, and be stable enough not to migrate from the first implanted position [25].

Figure 2.2 shows an example of a multi-channel DBS neural probe that is able to

accurately stimulate the STN developed by NeuroNexus Technology [54]. The probe is based on silicon substrate in 15 μm thickness for minimally invasive tissue injury. It also has a conducting pattern of recording sites and leads deposited with iridium. The electrode has 32 channels to provide a diverse spatially distributed stimulation and is separated by a distance of 100µm for each of the recording sites. The channel impedances vary depending on the tissue response within 200 $k\Omega$ to 3 $M\Omega$ [54].

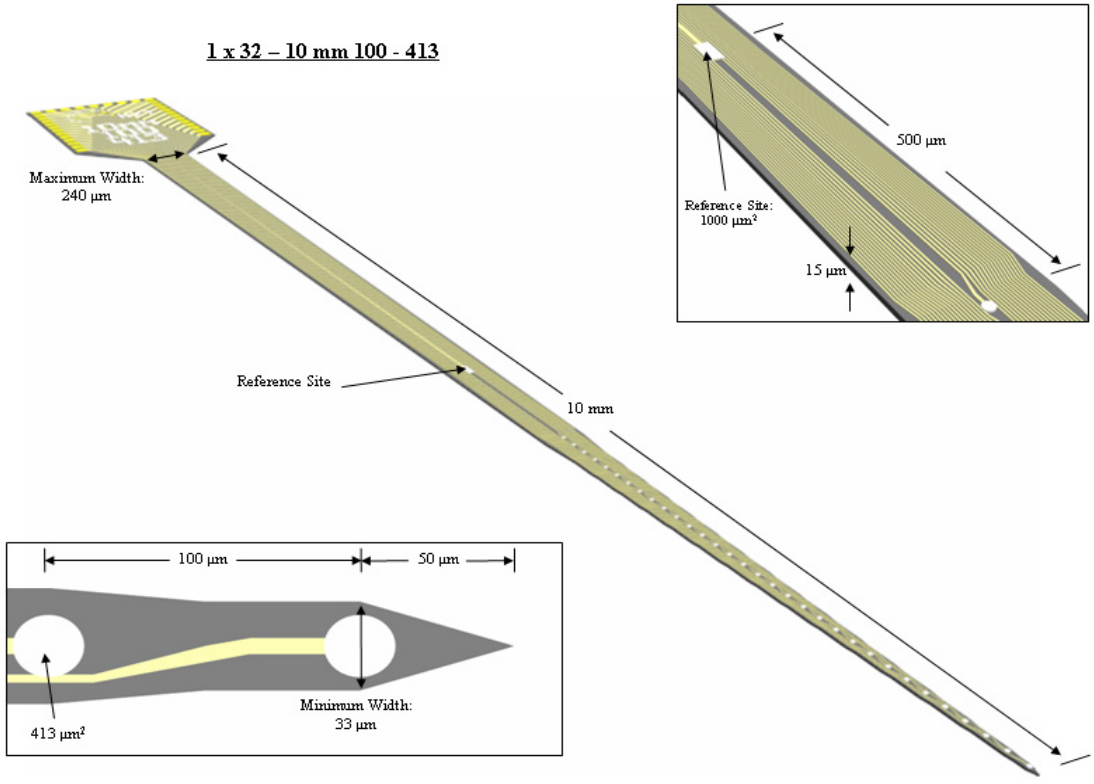


Figure 2.2: 32-channel silicon-substrate probes for DBS [54].

2.2. Switched-capacitor amplifying filter

As reviewed above, multi-channel microprobes are capable of recording neural population activity in the form of spike trains as well as slower LFPs. Both signal types provide unique information about biologically relevant time and spike pattern predictions [55].

However, there is no truly stand-alone, small-scale system for simultaneously recording both spikes and LFPs because of the challenges imposed by each of their signal characteristics. For the simultaneous recording of both neural signals, the amplifier system must exhibit a high dynamic range, which can be limited by the need for good noise performance and high ADC dynamic range (at least 16 bits). Together, these considerations inevitably limit the number of recording channels.

Here, a new architecture is introduced that uses a two-stage amplifier structure, which generates filtered LFP output at the first stage and processed spike output at the second stage as shown in Figure 2.2 [56]. The proposed device employs a switched-capacitor circuit to reduce flicker ($1/f$) noise and is less process dependent than a resistor based circuit. The first stage is designed as a low-Q bi-quad filter that passes a 10 *Hz* to 10 *kHz* frequency band with an amplification of 100 times for LFPs sensing. The second stage implements a high-Q bi-quad filter, which passes only 100 *Hz* to 10 *kHz* signals with an additional amplification of 10 times for spikes recording.

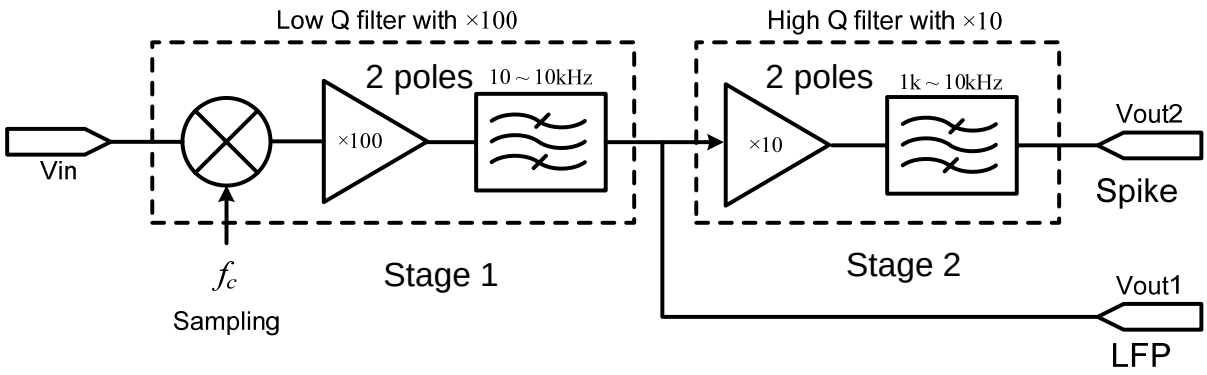


Figure 2.3: Basic architecture of the proposed system.

Figure 2.4 shows the equivalent electrical model of the neural microprobe, made by bulk micromachining and patterning of recording sites and lead wires. For the electrode-electrolyte interface, measurement of the Michigan probe shows that the spreading resistance, R_{sp} is 250 $k\Omega$, the electrode resistance, R_e is 200 $G\Omega$, the capacitance, C_e is 600 pF, and the interconnect resistance, R_i is 100 $k\Omega$. Because of the high electrode resistance, most currents flow through the capacitor except for extremely low frequency signals [27].

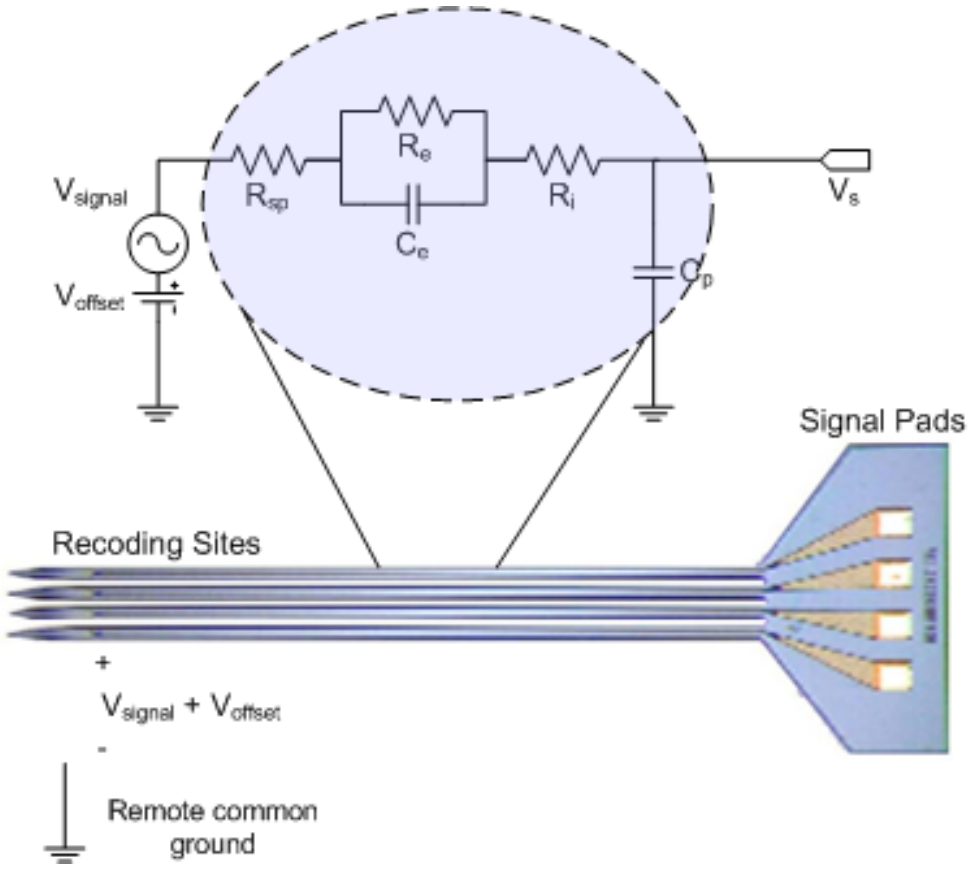


Figure 2.4: The simplified equivalent electrical model of the neural probe included a spreading resistance (Rsp), faradaic electrode resistance (Re), non-faradaic electrode capacitance (Ce), probe trace resistance (Ri), and shunt capacitance (Cp).

Band-pass charge amplifiers are generally used to connect to this type of probe, as shown in Figure 2.5 because capacitive matching provides more accuracy than resistive dividers.

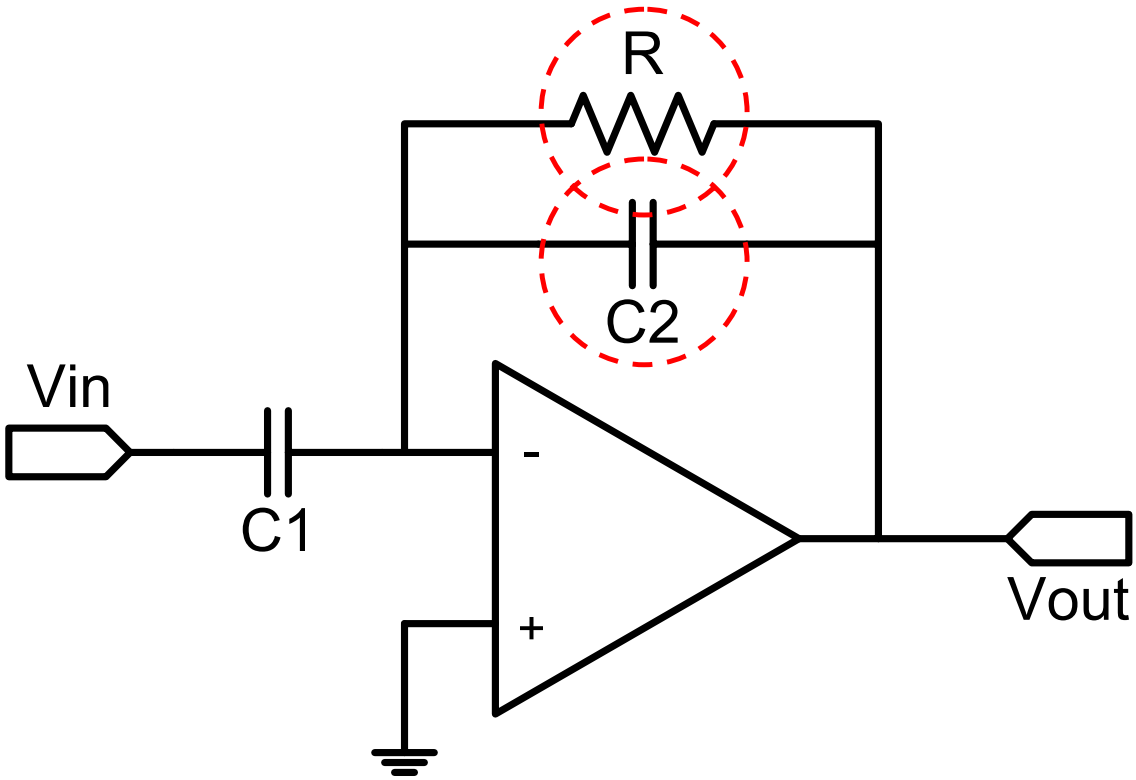


Figure 2.5: General band pass amplifier.

If the inputs to the charge amplifiers remain constant, the leakage currents that supply a constant current will saturate the output voltage to the supply limit. Hence, the voltage across the capacitor should be reset often enough so that leakage currents have no influence [57]. The switched-capacitor circuit refreshes the voltage across the capacitor frequently. Although this general charge amplifier works well, a very large feedback resistance, R, has been reported by R.H. Olsson *at el.* [58]. For example, for a 100 *Hz* high pass pole with 1 *pF* C2 capacitance , at least 1.6 *GΩ* resistance is indicated by Equation (2.1). Olsson *et al*. replaced the resistor with diode-connected transistors to form the large resistance. We describe another strategy to emulate a large resistance with a switched-capacitor technique.

$$R = \frac{1}{2\pi C_2 f_c} = \frac{1}{2\pi \times 1pF \times 100Hz} = 1.6G\Omega \tag{2.1}$$

As we scale down the transistor feature size, another issue arises since the 1/f noise of a MOSFET varies inversely with the transistor area (*WL*). The noise of a MOSFET consists of thermal noise and flicker (1/*f*) noise. Since 1/f noise is more important at lower frequencies, neural amplifier designs are focused on reducing this noise [59]. Empirically, PMOS transistors have about two to five times less 1/*f* noise than NMOS transistors and the first stage transistor is the dominant noise source. For example, input noise spectral density for a PMOS transistor is:

$$e_n^{\,2} = \frac{B}{fWL} = \frac{2.02\times10^{-22}(V-m)^2}{f\times1\mu m\times0.18\mu m} = \frac{11.22\times10^{-10}}{f}V^2/Hz \tag{2.2}$$

where the width (*W*) and length (*L*) of transistor is 1 μm and 0.18 μm, respectively and the 1/*f* noise constant of a PMOS transistor, *B*, is 2.02×10-22 $(V\text{-}m)^2$. To estimate the root-mean-square (RMS) noise in the bandwidth from 1 *Hz* to 1 *kHz*, we perform the integration as:

$$V_n(rms) = \sqrt{\int_1^{1000} \frac{11.22\times10^{-10}}{f} df} = 88\mu V_{rms} \tag{2.3}$$

Since this device noise may be too large for the neural recording, we apply circuit techniques to suppress the 1/*f* noise below the thermal noise with switched-capacitor modulation. The parallel switched capacitor equivalent resistor circuit in Figure 2.6 [60] consists of two controlled switches with control clock phases, φ_1 and φ_2, and a capacitor, C. The control clocks are non-overlapping complimentary signals. Hence, the input switch is shorted and the output switch is opened to charge the capacitor to the input voltage during phase, φ_1, and the input switch is opened and the output switch is shorted to deliver that stored charge to output during phase, φ_2.

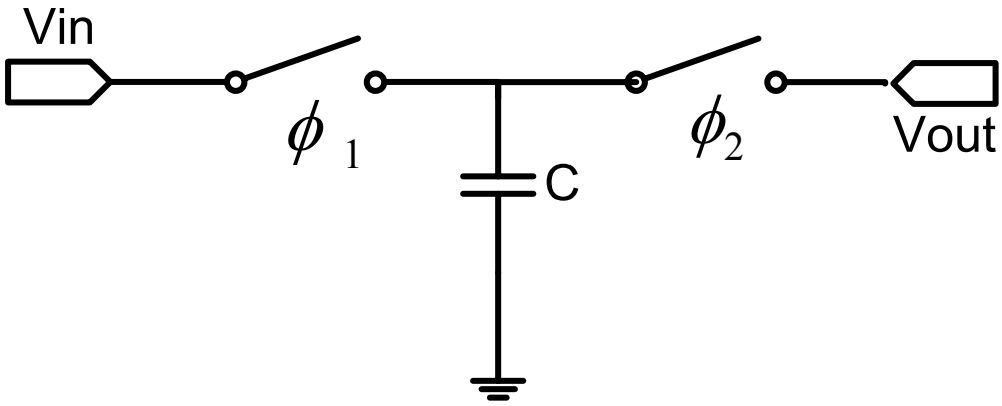


Figure 2.6: Resistor emulation with switched capacitor circuit.

This charge transfer works as a resistor with a periodic control clock. For example, with a 0.1 *pF* capacitor and a 1 *MHz* clock, the emulated resistance is given by:

$$R = \frac{V_{in}}{I} = \frac{V_{in}}{\Delta Q / \Delta t} = \frac{V_{in}}{\Delta Q \cdot f_c} = \frac{V_{in}}{C V_{in} \cdot f_c} = \frac{1}{C f_c} = \frac{1}{0.1pF \times 1MS/s} = 10M\Omega \tag{2.4}$$

The switched capacitor circuit modulates the signal to multiples of the sampling frequency as shown in Figure 2.7. Since 1/*f* noise at the sampling frequency is much less than that at the baseband, the switched capacitor circuit can be used to eliminate 1/*f* noise like a chopping amplifier [61-66].

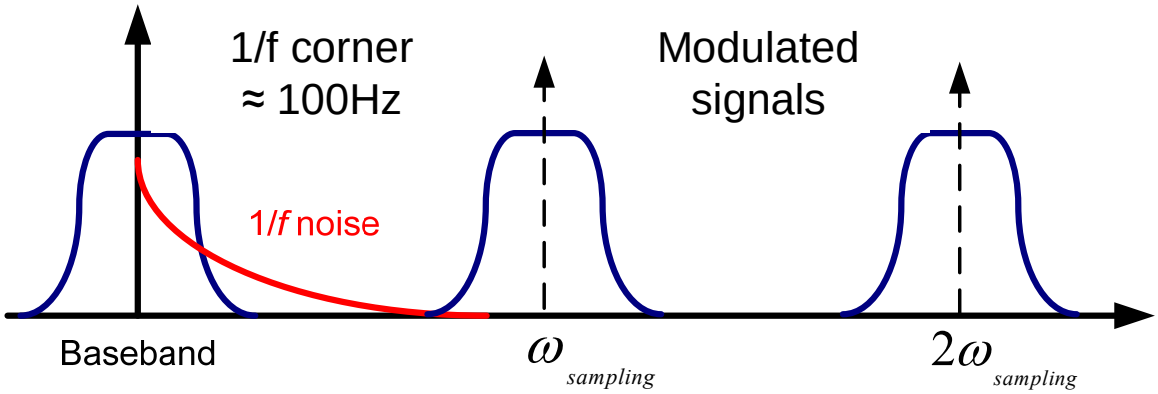


Figure 2.7: 1/*f* noise rejection by modulation with a switched capacitor circuit.

The 1/*f* noise with this sampling should be less than the wideband thermal noise. For this to occur, the sampling frequency has to be greater than the 1/*f* noise corner frequency and greater than twice the bandwidth of the input signal. The noise power spectral density (PSD) after sampling is given by [67],

$$S(f) = A_o^2 \left(\frac{2}{\pi}\right)^2 \sum_{\substack{-\infty \\ n \text{ is odd}}}^{+\infty} \frac{1}{n^2} S_n(f - nf_c) \tag{2.5}$$

where A_o is the amplifier gain, and f_c is the sampling frequency. The spectral density of the thermal noise of a transistor with 10 μS conductivity can be calculated by:

$$e_n^{\,2} = 2 \cdot \frac{8kT}{3g_m}[1+\sqrt{2}] = 2 \times 2.41 \times \frac{8 \times 1.38 \times 10^{-23} \times 300K}{3 \times 10\mu S} = 5.33 \times 10^{-15} V^2 / Hz \qquad (2.6)$$

Combining Equations (2.5) and (2.6) together, we can find the noise corner where the thermal noise is equal to the 1/*f* noise. For a PMOS input device with 1 μm width and 0.18 μm length,

$$f = \frac{11.22 \times 10^{-10} V^2 / Hz}{5.33 \times 10^{-15} V^2 / Hz} = 210.5kHz \qquad (2.7)$$

Since the general value of the noise corner frequency is 210.5 *kHz*, a sampling frequency of more than 500 *kS/s* is required to achieve complete elimination of 1/*f* noise. However, a 100 *kS/s* sampling frequency used for the prototype device is sufficient to get the desired signal-to-noise ratio (SNR) in simulation.

Second-order bi-quad circuits have the advantage of potentially realizing complex poles and zeros. A band-pass second order response in the continuous time domain can be written in general as:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-Ks}{s^2 + \frac{\omega_0}{Q}s + {\omega_0}^2} \tag{2.8}$$

Where ω_0 is the pole frequency, Q is the pole quality factor and K is coefficient for the amplification [68].

Charge injection and switching noise are non-idealities which need to be addressed when designing the switches. The amount of charge injected into the channel by the switching of the clock can be approximated as [69]:

$$\Delta q = \frac{WLC_{ox}}{2}(V_{ck} - V_{in} - v_{tn}) \tag{2.9}$$

Where W, L, C_{ox}, V_{tn}, are transistor parameters, V_{ck} and V_{in} are the clock and signal amplitudes respectively. If it is assumed that the charge splits equally between the source and drain, it follows that placing half-sized dummy transistors on either side controlled with an opposite clock absorbs most of this injected charge. In addition, the effect of switching noise can be eliminated by using a differential circuit implementation, because the noise equally affects both signal paths.

The differential circuit realization is shown in Figure 2.8 and the transfer function of the circuit is given by [63]:

$$H(s) = \frac{-Ks}{s^2 + \frac{\omega_0}{Q}s + {\omega_0}^2} = \frac{-\frac{\alpha_1}{T}s}{s^2 + \frac{\alpha_4}{T}s + \frac{\alpha_2\alpha_3}{T^2}} \tag{2.10}$$

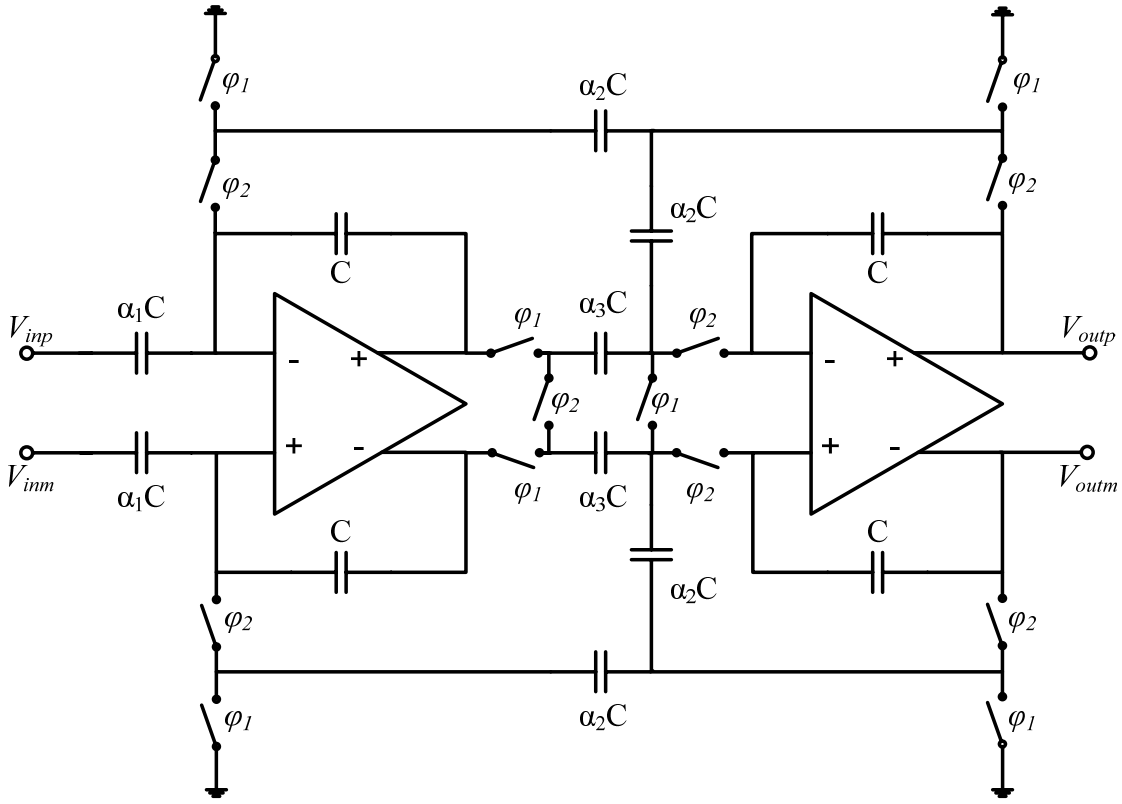


Figure 2.8: Low *Q* bi-quad with differential switched capacitor circuit.

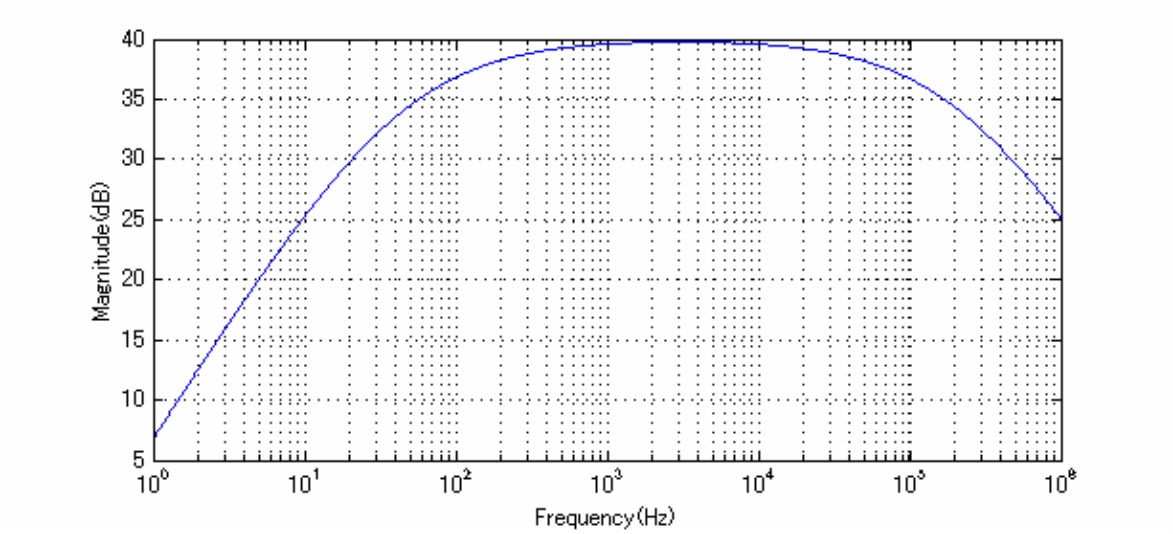


Figure 2.9: Frequency response of the low Q bi-quad.

To allow the circuit to pass all LFPs and spikes and limit direct current (DC) and high frequency noise, the coefficients are chosen as $\alpha_1 = 0.7\pi$, $\alpha_2 = \alpha_3 = 0.01\pi$, $\alpha_4 = 0.7\pi$, and $K = 100$ with a 100 *kS/s* sampling frequency. The simulated frequency transfer function is shown in Figure 2.9.

However, the pass band of the second stage, which passes spikes only, is narrow with a relatively high-Q value. If we use the circuit shown in Figure 2.8, we would need very large capacitors to meet this frequency range. Instead, we modify the circuit topology to high-Q circuit, to avoid large element spreads, as shown in Figure 2.10 and the transfer function is given by [63]:

$$H(s) = \frac{-Ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0^{\,2}} = \frac{-\frac{\alpha_1\alpha_3}{T}s}{s^2 + \frac{\alpha_3\alpha_4}{T}s + \frac{\alpha_2\alpha_3}{T^2}} \tag{2.11}$$

To pass spikes only and limit LFPs and high frequency noise, the coefficients are designed as $\alpha_1 = 0.75$, $\alpha_2 = 0.007\pi$, $\alpha_3 = 0.01\pi$, $\alpha_4 = 0.8$, and $K = 10$ with a 100 *kS/s* sampling frequency, and the simulated frequency transfer function is shown in Figure 2.11.

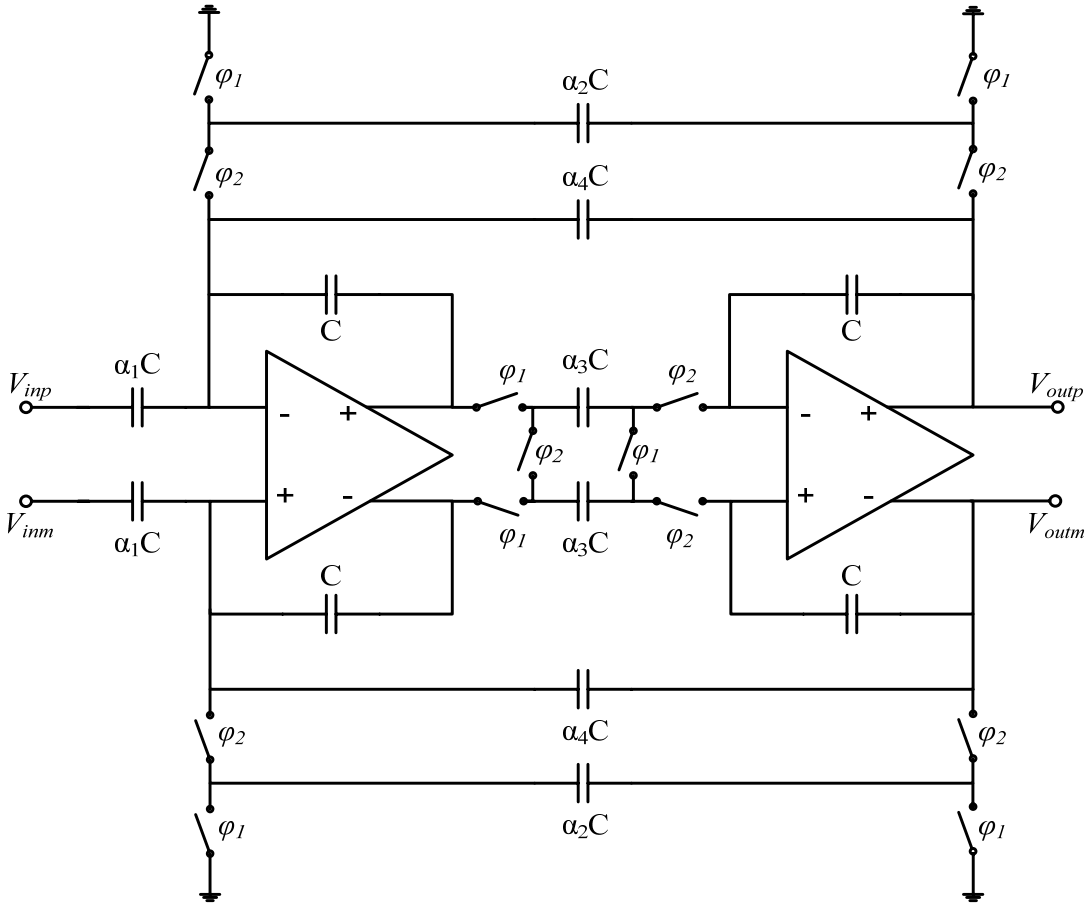


Figure 2.10: High *Q* bi-quad implemented with a differential switched capacitor circuit.

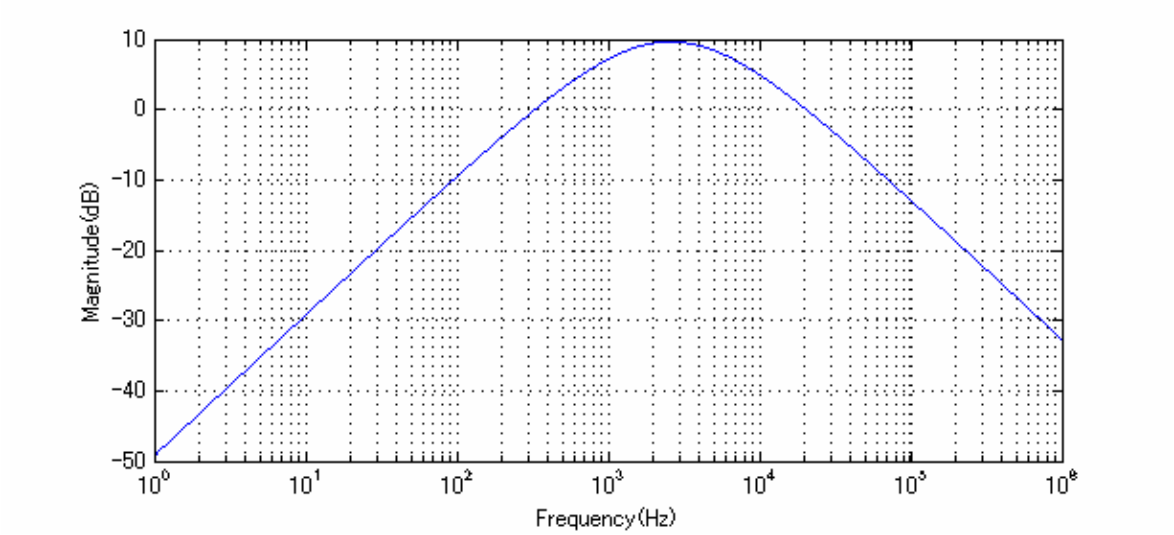


Figure 2.11: Frequency response of the high Q bi-quad.

The overall amplification is performed in two stages as shown in Figure 2.3 as presented above. The first one is modulated signal amplification with low-Q band pass filtering matched to 40 dB gain. The second stage has relatively low gain (20 dB) and high-Q band pass filtering.

2.3. Prototype implementation

The layout was made to be as symmetric as possible to eliminate mismatches between the differential paths. A die photograph of the fabricated circuit is shown in Figure 2.12. The prototype device is fabricated in 0.18 μm CMOS with a Metal-insulator-Metal (MiM) capacitor option and occupies 0.0032 mm^2 per each amplifying filter. The power consumption per each amplifier is 89 μW per channel.

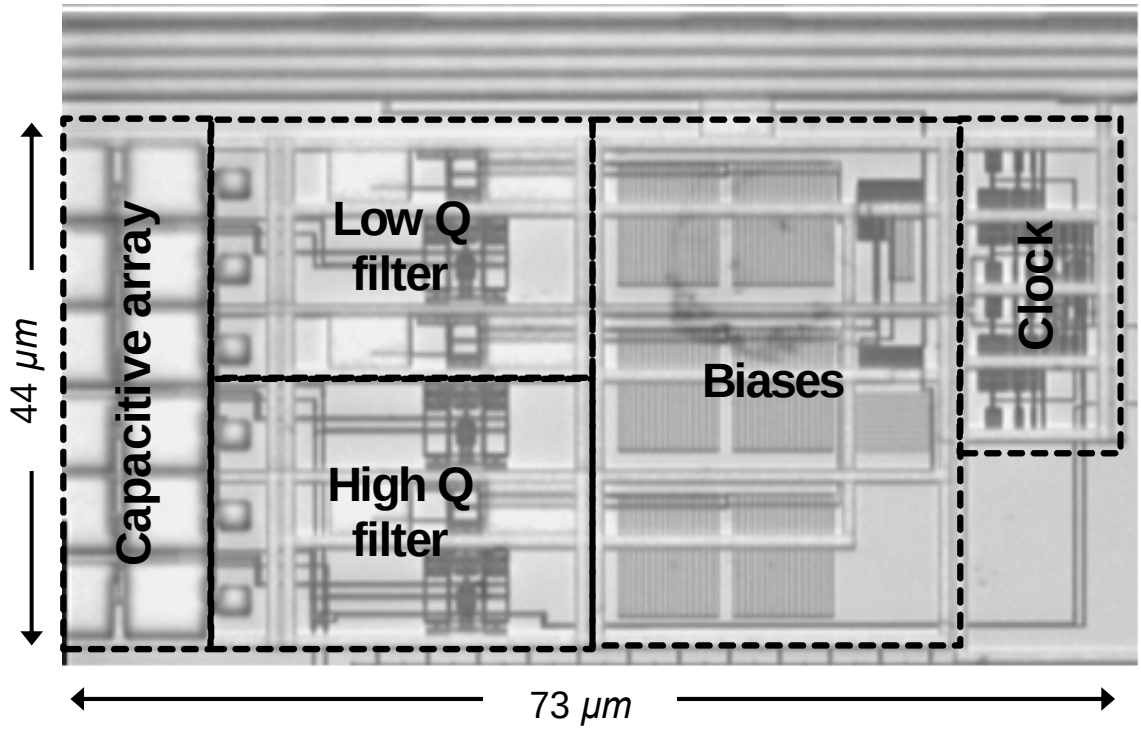
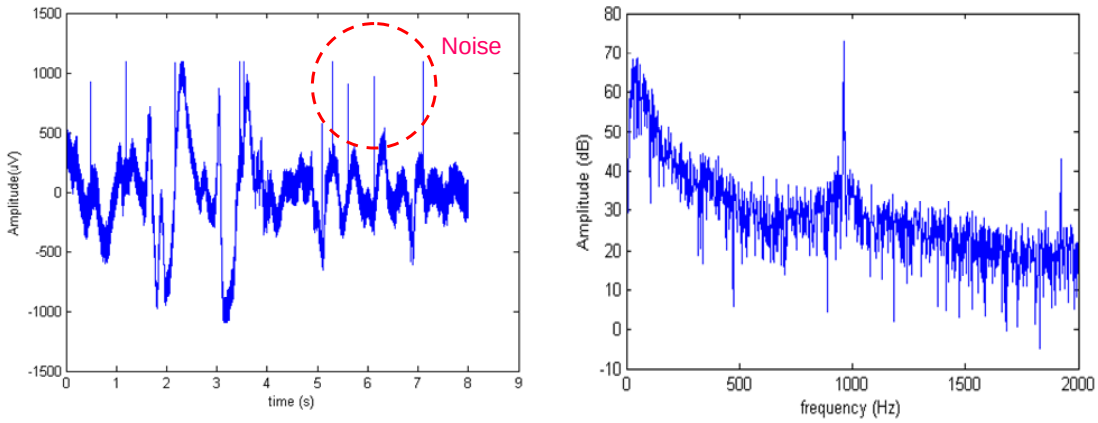


Figure 2.12: Die photograph of the fabricated device.

Testing was performed with pre-recorded neural data in the Neural Engineering laboratory (NEL) at the University of Michigan. Neural data were converted to an audio signal and supplied to the input of the prototype neural filter. The output of the circuit is delivered to an 8bit ADC and the ADC output is transmitted to a personal computer (PC) through a logic analyzer. The test board contains the fabricated neural amplifier, ADC, current sources and radio-frequency (RF) connectors for power and clock supplies. The acquired data is analyzed with a MATLAB tool.

Figure 2.13 show the pre-recorded real-time fast-recording raw data (a) and the frequency responses (b) which contain spikes, LFPs and noise. The signal amplitudes are laid within the range of $\pm 1\ mV$ and the frequency spectrum by Fast Fourier Transform

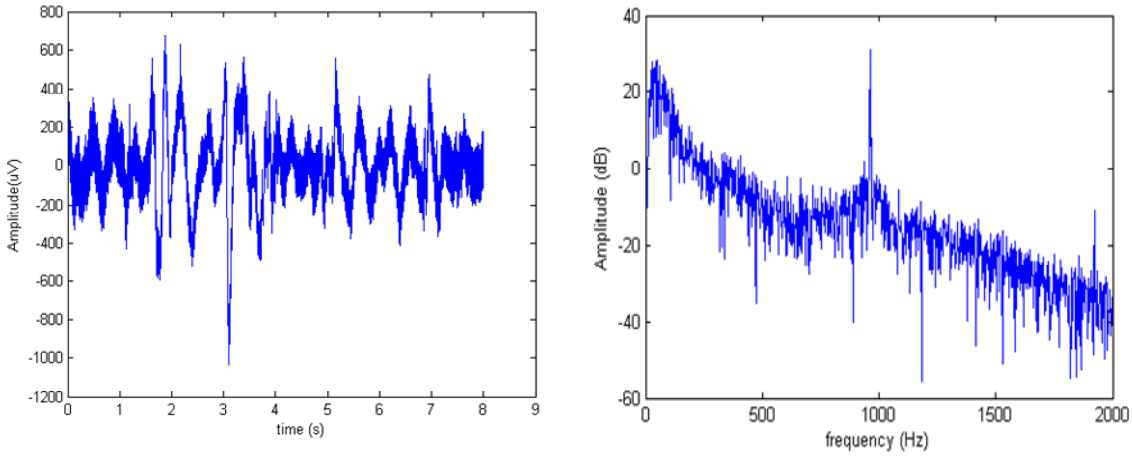
(FFT) in the MATLAB software shows clean spikes around 1 *kHz*, LFPs at low frequency and high frequency noises.



(a) Real-time recording (b) Frequency spectrum

Figure 2.13: Original neural signal.

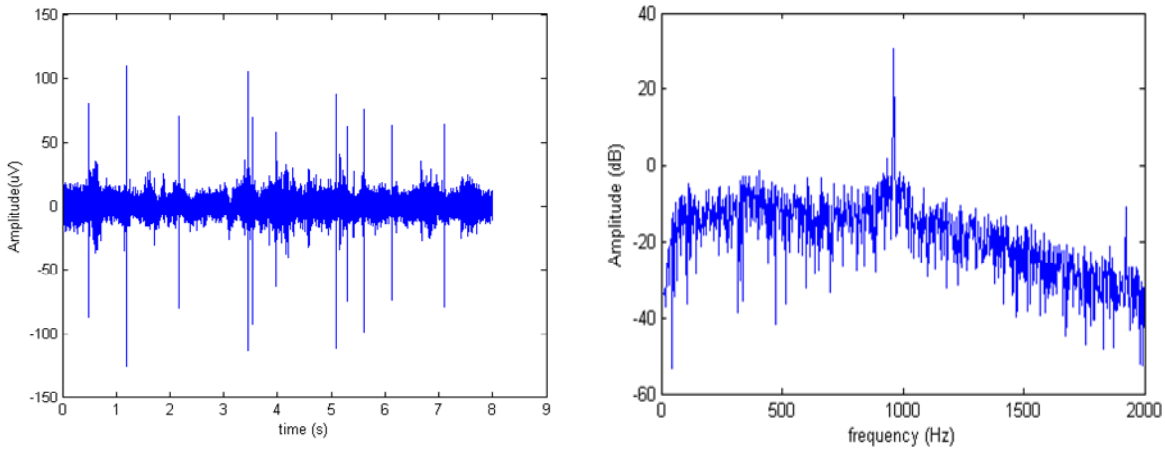
The output from the first stage shows a high frequency noise reduction as shown in Figure 2.14. The gain of the filter is measured as 870.96 (58.8 *dB*). After the amplitude adjustment, the magnitude range of the real-time neural signal (a) is placed between -1 *mV* to 0.7 *mV*. We can see the high frequency noise is suppressed below the 0 *dB* level in the FFT plot (b).



(a) Real-time recording (b) Frequency spectrum

Figure 2.14: *In-vitro* test output with low-*Q* bi-quad.

The output from the second stage shows spike trains with removing LFPs as shown in Figure 2.15. The measured gain is 90.16 (39.1 *dB*). After the amplitude adjustment, the real-time spike signal (a) range is between -125 μV to 115 μV. We can see the LFPs are decreased below the 0 *dB* level at the FFT plot (b).



(a) Real-time recording (b) Frequency spectrum

Figure 2.15: *In-vitro* test output with high *Q* bi-quad.

If we increase the time resolution of the real-time recording plotted in Figure 2.15 (a) in order to see spikes in details, we can see a very clean spike as shown in Figure 2.16. The duration of the spike is approximately 1 *ms* with an amplitude of 220 μVpp.

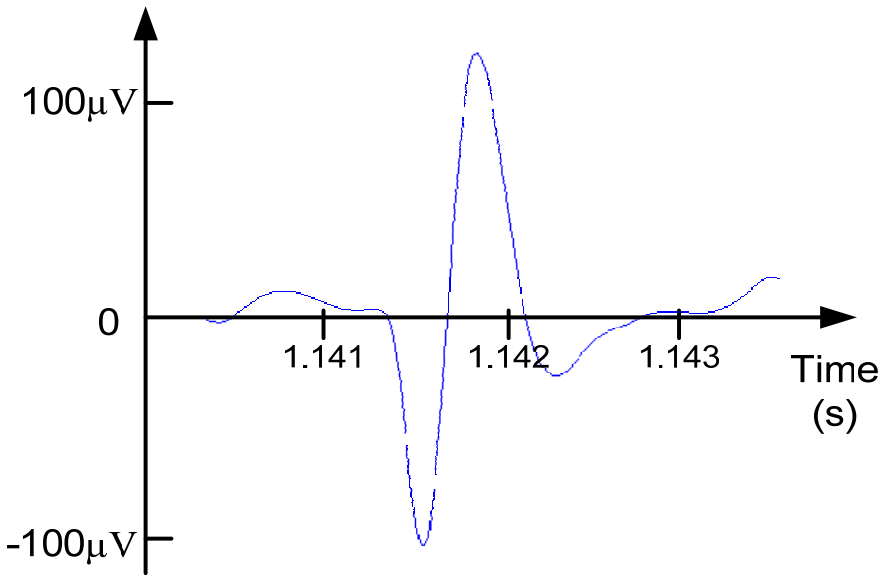


Figure 2.16: A single spike at the high-*Q* bi-quad output.

The noise performance is expressed in terms of an equivalent input noise, which gives the same output noise as the circuit under no other input. The device noise is measured at the output with the inputs shorted together. Then, the equivalent input noise spectral density (INSD) of the complete circuit is calculated by dividing the output noise by the gain. The measured output noise is 2.06mVrms and the equivalent input referred voltage as 2.36 $\mu Vrms$ and it represents INSD is 23.6 $nV/\sqrt{Hz}$. This value is less than

source signal power and we can achieve an SNR as much as 30 *dB*. The 1/*f* noise components are rejected by the modulation and the INSD is flat across the signal band, since there remains only frequency independent noise sources such as thermal and shot noises. Table 2.1 shows the summary of the device.

Table 2.1: Switched-capacitor filter performance.

Spec.	Measured data
Power supply	1.8 *V*
Sampling frequency	100 *kS/s*
Die size	44 μm × 73 μm
Power Consumption	89 μW */ch*.
INSD	23.6 $nV/\sqrt{Hz}$
Pass band gain for low *Q*	39.1 *dB*
Pass band gain for high *Q*	58.8 *dB*
Technology	CMOS 0.18 μm

CHAPTER III

Logarithmic ADC

For a simultaneous neural recording of the spikes and local field potentials (LFPs), a two-stage filtering device, that separates the recorded neural data into a low-frequency, low-resolution signal set and a high-frequency, high-resolution spike set, is proposed in the previous chapter. Instead, a high dynamic range logarithmic analog-to-digital converter (ADC) and digital filtering can replace the analog filtering saving power consumption and area.

Most natural signals, including light intensity and audio amplitude, are measured on a logarithmic scale. A properly designed logarithmic coding scheme is more efficient than conventional linear encoding, in that, a higher dynamic range can be represented for a given word length. For example, Figure 3.1 shows that logarithmic coding achieves better image quality than linear coding for the same number of bits.

Expansion of dynamic range is traditionally achieved through automatic gain control (AGC) or nonlinear compression [71]. However, an AGC amplifier cannot respond to rapidly fluctuating signals. A logarithmic amplifier can be used to compress the dynamic range of an input signal [72], but this approach requires a look-up table to precisely describe the device-derived non-linear characteristics. Alternatively, a back-end digital compander [73] can be combined with a high-resolution ADC. However, this method is power-hungry and complex. Direct logarithmic analog-to-digital conversion

has exactly the same beneficial characteristics as the combination of a logarithmic amplifier and linear ADC, but with potentially much lower power consumption.

(a) Linear 3bit coding **(b) Log 3bit coding**

Figure 3.1: Image quality comparison for standard image [70] with 3 bit linear and 3 bit logarithmic coding.

In this chapter, we describe a logarithmic pipeline ADC technique and present a prototype logarithmic ADC which demonstrates a high dynamic range of 80 *dB* [33]. This approach is advantageous for many applications where high dynamic range is required such as audio, imaging and sensing. A novel switched capacitor (SC) logarithmic pipeline ADC architecture, that does not require squaring or any other complex analog function, is introduced in this chapter. Unlike a conventional pipeline ADC, the pipeline stages do not include an MDAC, so that the required accuracy of the reference voltage is greatly relaxed. Performance metrics such as signal-to-noise-ratio (SNR) and dynamic range are also discussed.

3.1. Logarithmic pipeline architecture

With logarithmic coding, the LSB size varies with the input signal level. Similar to a companding digitizer, small signals are quantized at fine resolution, whereas changes in large signals are quantized at coarse resolution. Figure 3.2 shows an example of a 5 bit logarithmic companding characteristic. Larger voltage input results in larger least significant bit (LSB) size.

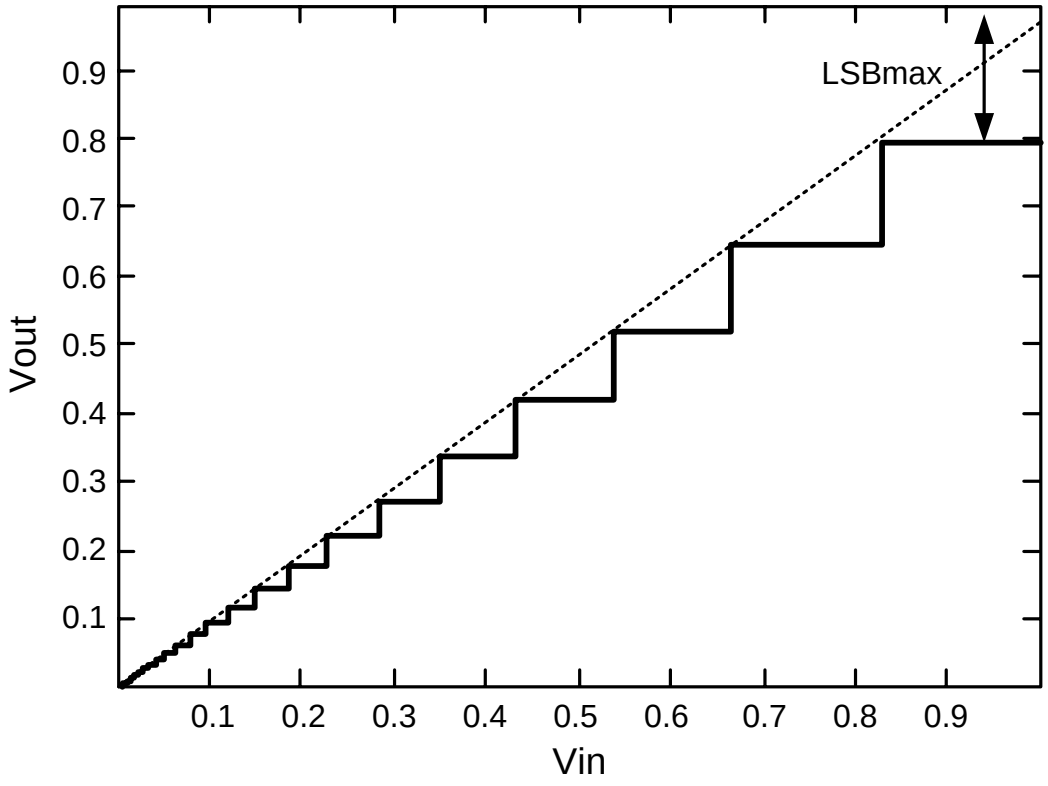


Figure 3.2: Companding characteristics of 5 bit logarithmic quantization.

An L-bit logarithmic ADC converts an input analog voltage (V_{in}) to a digital bit sequence (b_{L-1}, b_{L-2}, …, b_1, b_0), mapping to a logarithmic domain. This mapping equation is shown in Equation (3.1).

$$\log_{10}\left(\frac{V_{in}}{V_{range}}\times 10^{C}\right)=\frac{b_{L-1}2^{L-1}+\ldots+b_0}{2^{L}}C \tag{3.1}$$

In Equation (3.1), the input voltage V_{in} is divided by the full-scale ADC input range (V_{range}), mapping the input to a nominal range from 0 to 1. A *code efficiency* factor, C is introduced. Larger values of C result in a more logarithmic input-to-digital-output relationship, emphasizing smaller signals, and resulting in a higher dynamic range. Figure 3.3 illustrates how the code efficiency factor, C, affects the input-to-output relationship.

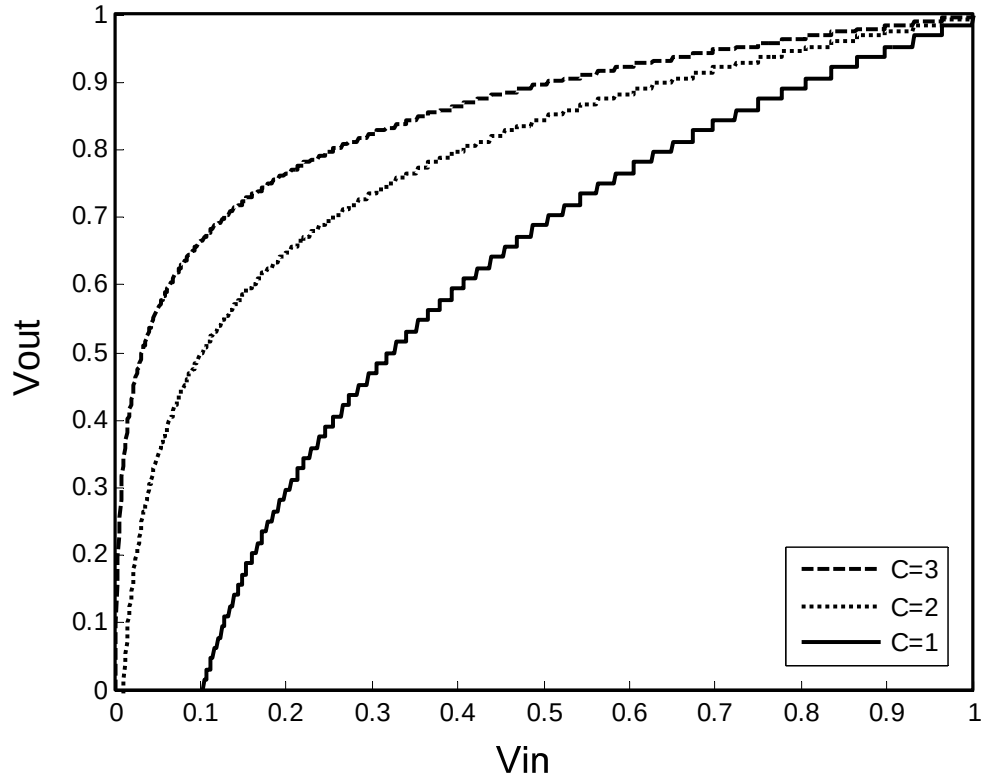


Figure 3.3: 6 bit logarithmic characteristics for three values of code efficiencies, C.

Although the LSB size of a conventional ADC, $V_{range}/2^{L}$, is constant over the entire input range, the logarithmic LSB size of a logarithmic ADC is $C/2^{L}$. As a result, the LSB size varies depending on the input amplitude. For the 8 bit logarithmic ADC, which is demonstrated in this work, C is set to 3, resulting in the minimum LSB size to $1.109\times10^{-4}\ V_{range}$. The theoretical dynamic range of considering only the positive polarity part of the logarithmic ADC range is 85 *dB*. A sign bit adds an extra 6 *dB*, resulting in a 91 *dB* theoretical dynamic range. The methodology for calculating theoretical dynamic range is presented later in this section.

Limited minimum detectable voltage due to noise, linearity, and device matching problems make practical circuit implementation with $C>3$ difficult. For example, with $C = 2$, and assuming V_{range} is 1 *V*, the minimum LSB size of 8bit ADC is 0.37 *mV*. On the other hand, with a code efficiency factor of 4 ($C = 4$), the minimum LSB size is only 7.5 μV, which makes noise and matching difficult and impractical to overcome.

By rewriting Equation (3.1), the analog input corresponding to a digital code is given by Equation (3.2).

$$v_{in} = V_{range}\cdot 10^{C\cdot\frac{Digital\ \ code}{2^{L}}-C} = V_{range}\cdot 10^{C\cdot\frac{b_{L-1}2^{L-1}+\cdots+b_{0}}{2^{L}}-C} \tag{3.2}$$

The varying LSB size is calculated by subtracting v_{in} values from Equation (3.2) for two adjacent digital codes. Subtracting analog input values for codes 0 and 1, results in the minimum LSB size. If we subtract the analog input values corresponding to the

maximum digital codes 2^L and 2^L-1, we obtain the maximum LSB size. Equation (3.3) includes both the minimum and maximum LSB sizes.

$$\begin{aligned} LSB_{\min} &= V_{range} \times (10^{\frac{C}{2^L}-C} - 10^{-C}), \\ LSB_{\max} &= V_{range} \times (1 - 10^{-\frac{C}{2^L}}) \end{aligned} \tag{3.3}$$

The dynamic range (DR) is defined as the ratio of the input range (V_{range}) to the smallest resolvable signal, or the smallest difference between adjacent codes, as:

$$DR = \frac{V_{range}}{\min_j (V_{trip,j+1} - V_{trip,j})} = \frac{V_{range}}{LSB_{\min}} \tag{3.4}$$

Then, by substituting Equation (3.3), dynamic range is calculated as:

$$DR = 20\log_{10}\frac{V_{range}}{LSB_{\min}} = -20\log_{10}\left(10^{\frac{C}{2^L}-C} - 10^{-C}\right) \ (dB) \tag{3.5}$$

The proposed logarithmic-domain pipeline ADC architecture is based on simple scalar multiplication and does not require cumbersome analog math operations such as squaring or exponents. A direct log-adaptation of a conventional linear 1.5-bit-per-stage, pipeline ADC would replace subtraction with division, and multiplication by 2 with

squaring [54]. Since $log_{10}V_{in}$ - $log_{10}V_{ref}$ = $log_{10}(V_{in}/V_{ref})$ in a logarithmic pipeline ADC, a conditional attenuation (or gain) replaces subtraction, depending on the decision of the sub-ADC. This pipeline stage differs from a conventional 1.5 bit pipeline ADC's multiplying digital-to-analog converter (MDAC), which uses a linear stage that subtracts one of three MDAC settings; Instead, the logarithmic 1.5-bit-per-stage architecture presented here sets three different inter-stage gains. These three gains are achieved by switching in different values of feedback capacitance across an OpAmp. Figure 4 shows the three gain setting from the previous stage output (V_{in}) to the current stage output ($V_{residue}$). The 1.5 bit sub-ADC determines the stage gain and the residue plot.

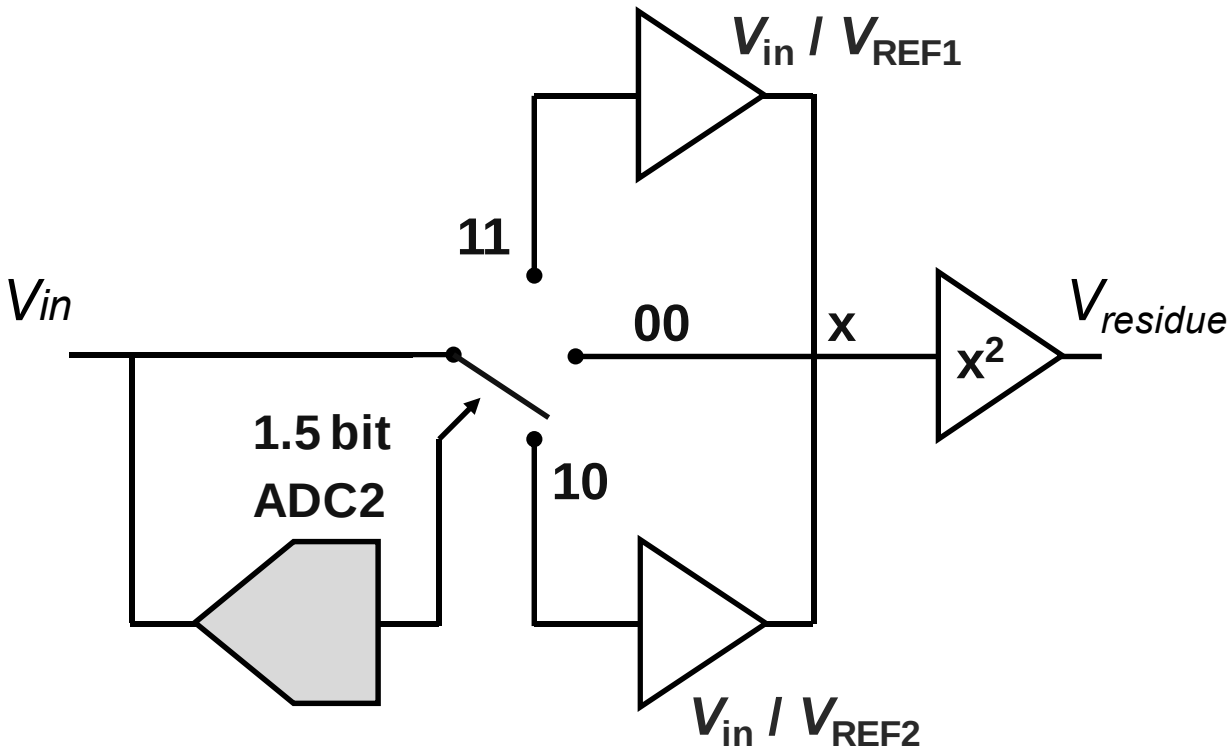


Figure 3.4: Implementation of the logarithmic pipeline.

Although figure 3.4 also includes a squarer, we see next how squaring is eliminated in this log ADC architecture. In a log ADC, squaring is equivalent to a multiplication by 2 in a radix-2 pipeline ADC. Instead of attempting precise analog squaring, we achieve the same overall result by scaling the comparator reference voltages and gain settings for each pipeline stage (A similar scheme is proposed in [74]). In a logarithmic pipeline ADC, the residue of each stage is scaled to the full-scale input voltage range of the next stage. Considering that $2 \times log_{10}(Vresidue) = log_{10}(Vresidue^2)$, this requires squaring of the residue, but accurate and reliable squaring is difficult in the analog domain.

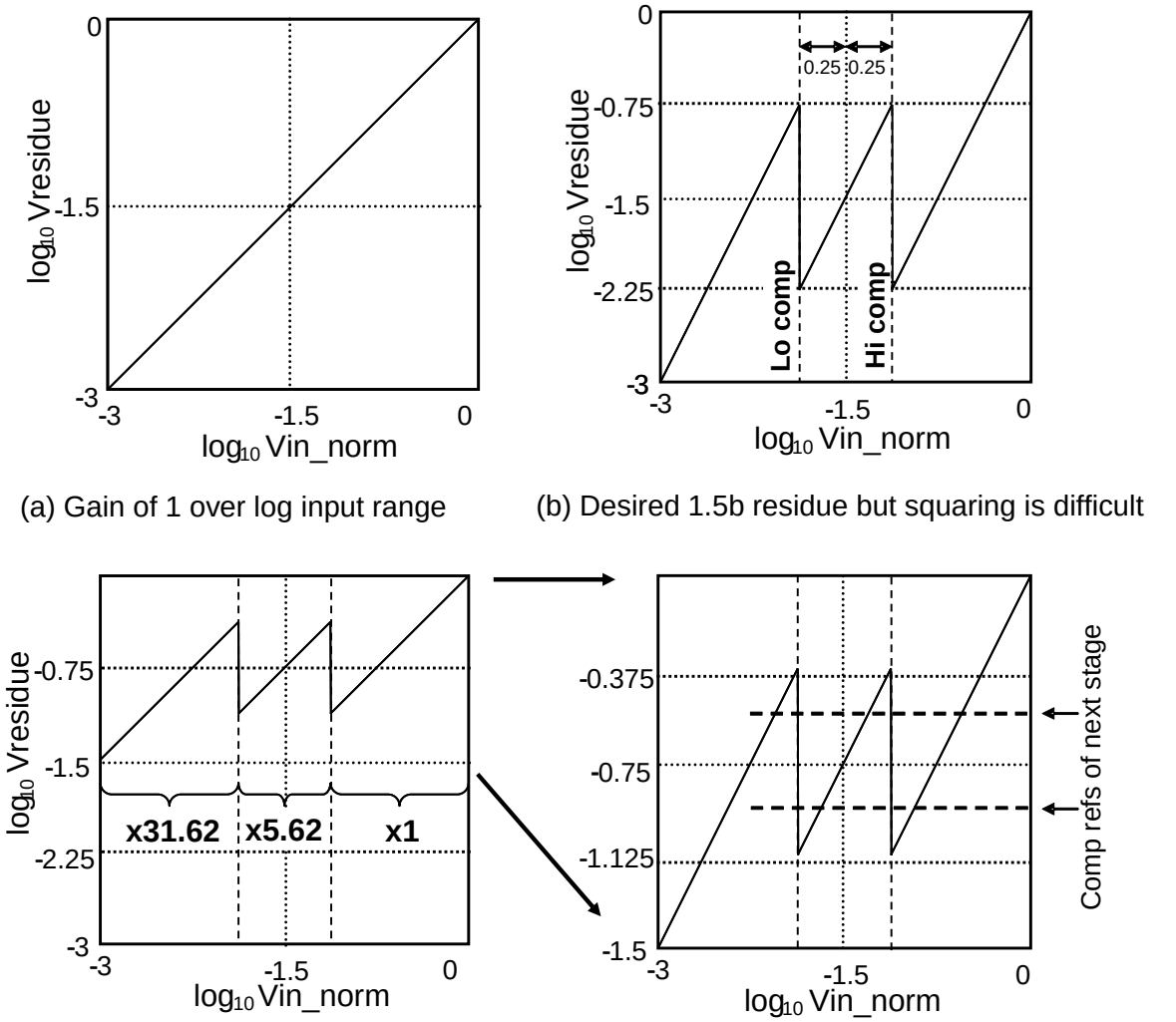


Figure 3.5: Logarithmic ADC residue plots.

Figure 3.5 (b) shows the residue characteristic of a 1.5 bit logarithmic ADC pipeline stage. For comparison, a direct linear relationship between input and output is plotted in Figure 3.5 (a). The residue plots are described on a logarithmic sale with a normalized $\log_{10}$ range from -3 to 0 (i.e. $C = 3$). The residue of figure 3.5 (b) is divided into three regions as there are two comparators. A modified approach in figure 3.5 (c)

uses the same comparator thresholds, but the gain settings are chosen so that the residue now falls entirely into the top vertical half (i.e. logarithmic range: -1.5 to 0, or a corresponding linear range: $10^{-1.5}$ to 1). Squaring of the residue of figure 3.5 (c) would double its logarithmic range to appear identical to the residue of figure 3.5 (b). However, instead of squaring, a different set of comparator reference voltages is chosen for the next stage. The reference voltages are set in the top half of figure 3.5 (c), effectively achieving a rescaled residue with the same shape (Figure 3.5 (d)). This approach is not only easier to implement but also advantageous since the reference and signal voltages become larger (i.e. closer to a normalized logarithmic value of 0) going down the pipeline. For example, the upper threshold of the second stage is 137 mV whereas, that of the first stage is 31.6 mV. Larger references are easier to generate and have more tolerance for comparator errors. [1]

The classic 1.5-bit-per-stage redundancy scheme used in linear pipeline ADCs [75] is adapted here to reduce the required accuracy of the comparators. Unlike the case with a linear pipeline, reference voltages are not used in MDAC stages, and therefore, redundancy significantly reduces the required accuracy of both the comparators and voltage references. In a 1.5 bit stage, the input range of each stage is divided into three regions, corresponding to the three possible outputs of the two comparators: “00”, “01” and “11”. Redundancy can correct for both comparator offset errors and reference voltage errors with a range given by Equation (3.6).

---

[1] This log ADC architecture is fundamentally different to a classical linear pipeline architecture. A 1 bit per stage pipe subtracts binary weighted values of the reference from the input, attempting to reach a final residue of zero. On the other hand, this log pipeline gains up the input at each stage, ultimately attempting to achieve a residue of full scale.

$$\Delta V_{in,correct} = log_{10}\, V_{ref} \pm (1/4)\, log_{10}\, V_{ref} \tag{3.6}$$

The easiest way to calculate the reference voltages is to begin on a logarithmic scale and then to return to linear scale. For the residue plot of i^{th} stage, the center of the x-axis is at $-C/2^i$ on a logarithmic scale. If Equation (3.6) for digital correction is applied, the reference voltages are defined as:

$$\log_{10}\frac{V_{ref}}{V_{range}} = -\frac{C}{2^i}\left(1 \pm \frac{1}{4}\right)$$

$$V_{ref1} = V_{range} \times 10^{-\frac{1.25C}{2^i}},\quad V_{ref2} = V_{range} \times 10^{-\frac{0.75C}{2^i}} \tag{3.7}$$

where $Vref_1$ is the lower threshold and $Vref_2$ is the upper threshold. Similarly, the gains for stage i are:

$$\log_{10} G_1 = \frac{C}{2^i},\quad \log_{10} G_2 = \frac{C}{2 \cdot 2^i},\quad \log_{10} G_3 = 0$$

$$G(v_{in}) = \begin{cases} G_1 = 10^{\frac{C}{2^i}} & , v_{in} \le V_{ref\,1} \\ G_2 = 10^{\frac{C}{2^{i+1}}} & , V_{ref\,1} < v_{in} \le V_{ref\,2} \\ G_3 = 1 & , V_{ref\,2} < v_{in} \le V_{range} \end{cases} \tag{3.8}$$

In Equation (3.8), G_1 is the highest gain setting for stage inputs less than $Vref_1$; G_2 is the gain for the stage inputs that lie between $Vref_1$ and $Vref_2$; and G_3 is the bypass gain for the stage inputs larger than $Vref_2$ for the i^{th} stage. Note that $G_1 = G_2^2$.

In a conventional pipeline ADC, gain errors are caused by capacitor mismatch, finite opamp gain, and incomplete settling of the residue amplifiers. These gain errors reduce the linearity of the ADC. While both MDAC errors and gain errors are sources of nonlinearity in a conventional pipeline ADC, only gain errors contribute to nonlinearity in this logarithmic pipeline structure because it does not include an MDAC.

Ideally, a stage output is the product of the input signal and the gain; $v_{out} = v_{in} G(v_{in})$, where $G(v_{in})$ is the ideal (closed-loop) gain of the interstage amplifier defined in Equation (3.8). If we express the total gain error as $\varepsilon(v_{in})$, then the actual gain is $G(v_{in})(1+\varepsilon(v_{in}))$. For example, without gain error, the mid-gain range of the first stage of the prototype ADC is 5.62, but varies from 5.57 and 5.68 with a ±1% capacitor mismatching error. If we express the relationship between the input and output of each pipeline stage in the logarithmic domain, the stage output or residue can be written as Equation (3.9):

$$\log_{10} v_{out} = \log_{10} v_{in} + \log_{10} G(v_{in}) + \log_{10}(1+\varepsilon(v_{in})) \tag{3.9}$$

If ε is small ($|\varepsilon(v_{in})| << 1$), we can approximate $\log_{10}(1+\varepsilon(v_{in})) \approx \varepsilon(v_{in})/e$, where e is the natural logarithmic constant ($e \approx 2.718$) giving:

$$\log_{10} v_{out} = \log_{10} v_{in} + \log_{10} G(v_{in}) + \varepsilon(v_{in})/e \tag{3.10}$$

A new residue plot considering gain error is drawn in Figure 3.6. The last term in this equation, $\varepsilon(v_{in})/e$, causes an undesired gain shift of $\varepsilon(v_{in})/e$ in logarithmic domain. The $\varepsilon(v_{in})/e$ term represents the input referred error in the logarithmic relationship between the stage input and output.

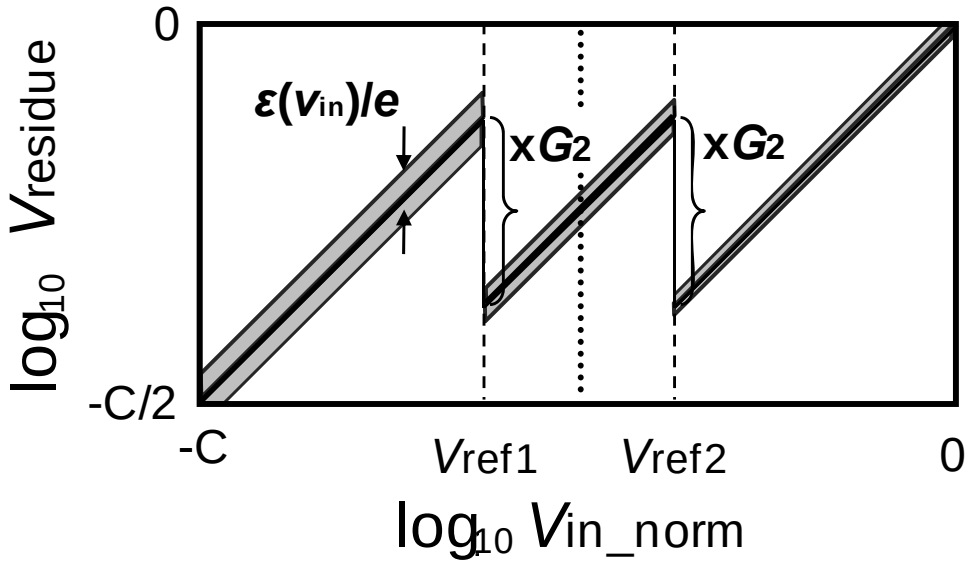


Figure 3.6: 1.5 bit residue plot and error due to finite gain

The gain error, $\varepsilon(v_{in})$, can be divided into a random component and a systematic component; $\varepsilon(v_{in}) = \varepsilon_r + \varepsilon_f(v_{in})$. The random part, ε_r, is due to device imperfections, in particular capacitor mismatch. On the other hand, the systematic component, $\varepsilon_f(v_{in})$, results from deficient amplifier gain and is inversely proportional to the feedback factor(β). In other words, the systematic component of gain error is predictable if we know the feedback factor and the operational amplifier (Op Amp) gain.

The systematic gain error can be derived from finite DC gain as:

$$\varepsilon_f(v_{in}) = \frac{1}{G(v_{in})} \cdot \frac{A_0}{1+\beta A_0} - 1 = -\frac{G(v_{in})}{G(v_{in})+A_0} \approx -\frac{G(v_{in})}{A_0} \qquad (3.11)$$

Where A_0 is the Op Amp gain, and we assume that β, the feedback factor is the inverse $G(v_{in})$, the ideal gain.

Using this approximation for gain error, Figure 3.7. plots the systematic component of the closed-loop stage gain error due to finite direct current (DC) gain. The gain error depends on the gain setting, and therefore there is a different gain error for each of the three input regions defined in Equation (3.8). The absolute value of gain error in the low-range is much larger than that in the mid-range since G_1 is the square of G_2.

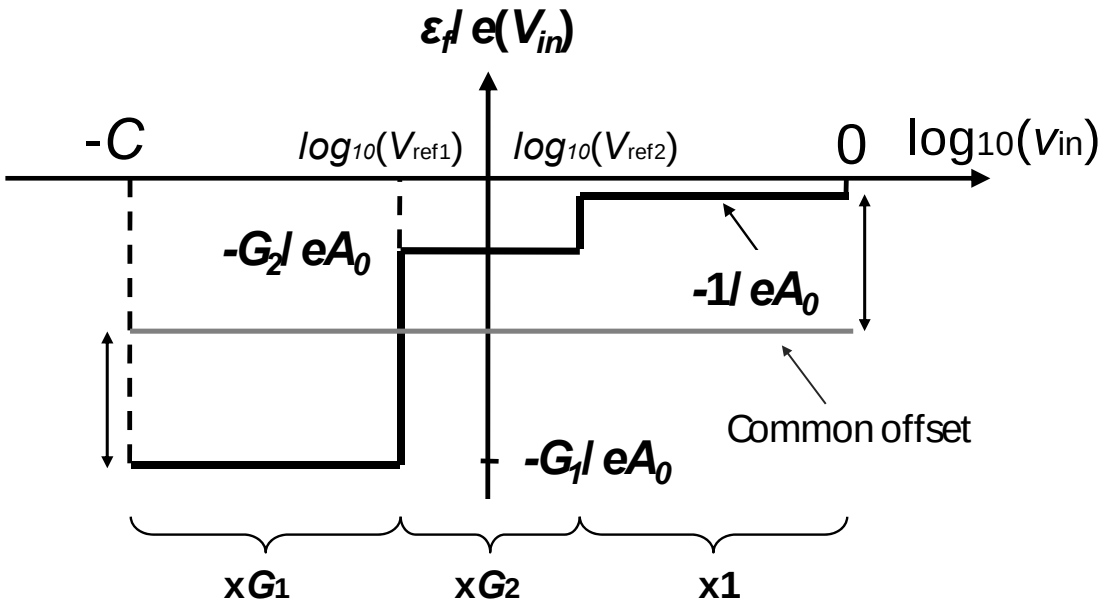


Figure 3.7: Input-referred systematic gain error due to finite OpAmp gain for a 1.5b logarithmic stage.

The grey line in the figure represents the common offset (-(G_1+1)/2eA_0) which is the average of the maximum gain error in the low range and the minimum gain error in the high range. Then, the distances from common line to the low range gain error and the high gain range error are same, and it leads to the effective systematic error which is the maximum distance from the errors to common offset as (G_1-1)/2eA_0.

To guarantee the overall ADC linearity, this effective systematic error should be less than the LSB size. Note that in an 8bit logarithmic ADC an LSB = $C/2^{L-1}$ = 0.023 in logarithmic domain. Combining with Equation (3.10), the effective gain error due to finite DC gain in the logarithmic domain is then expressed as ε_f/e(= (G_1-1)/2eA_0). To achieve an INL less than 0.5 LSB, the maximum gain error of the first stage can be up to 3.1%, compared to only 0.62% [76] in an 8bit linear ADC. Unlike a linear ADC the logarithmic ADC which does not include an MDAC, further reducing the requirements for linearity. The non-linearity error caused by MDAC is larger in practice than the non-linearity caused by gain error in linear ADCs [76]. From the above criteria, we can estimate the gain requirement of the Op Amp limited by the finite DC gain from feedback as:

$$\frac{G_1 - 1}{2eA_0} > \frac{LSB}{K} \quad \Rightarrow \quad A_0 > \frac{G_1 - 1}{2e} \cdot \frac{K}{LSB} = \frac{10^{\frac{C}{2^i}} - 1}{2e} \cdot \frac{K \cdot 2^{L-1}}{C} \qquad (3.12)$$

Where K is the number of inter-stage Op Amps which cause gain errors, C is the code efficiency factor. Since the effect of gain error is cumulative over all stages, the gain error margin should be spread over the pipeline stages as a factor of K. K is 5 for the

prototype 8bit logarithmic ADC and C is 3. As shown in Equation (3.12), the gain requirement decreases exponentially down the pipeline. To achieve an integral non-linearity (INL) less than 1 LSB, the minimum Op Amp gain of the first stage should be greater than 1202 (= 61.6 *dB*), but only 182 (= 45.2 *dB*) in the second stage.

The thermal noise of the first stage is the dominant source of noise, since the first stage gain is large enough to minimize the input referred noise contribution of other stages. The input referred noise of i^{th} stage of an SC amplifier is given by [77],

$$v_{ni}^{\ 2} = \frac{2kT}{C_i} + \frac{8kT}{g_{m1}} B_n = \frac{2kT}{C_i} + \frac{2kT}{(2+G_i)C_i} \tag{3.13}$$

Where C_i is the sampling capacitor of i^{th} stage, g_{m1} is the transconductance of input transistors and B_n is the noise bandwidth that is $g_{m1}/4(2+G_i)C_i$ [77] and G_i is the high gain of i^{th} stage. The first term is the sampling noise and the second is thermal noise in the hold phase. If we neglect the parasitic capacitances, the total input referred noise power can be calculate as:

$$v_n^{\ 2} = v_{n,SH}^{\ 2} + v_{n1}^{\ 2} + \frac{v_{n2}^{\ 2}}{G_1^{\ 2}} + \cdots \approx \frac{14\,kT}{3C_i} + \frac{2\,kT}{G_1^{\ 2}(2+G_i)C_i} \tag{3.14}$$

Where v_n^2 is the total input-referred noise power, $v_{n,SH}^2$ is the noise of the sample and hold amplifier, v_{n1}^2 is the noise of the first stage and v_{n2}^2 is the noise of the second stage. Since the gain of the first stage is relatively large, the noise contribution from

second stage can be ignored. For C = 3, the high gain of the first stage is 31.6 and then, the total input referred noise is $4.67kT/C_i$ (V^2). To sense the minimum detectable signal, 1.1×10^{-4} V_{range} , for C = 3 at room temperature, the minimum input capacitor size is obtained as,

$$C_i = \frac{4.67\ kT}{(1.1\times 10^{-4})^2} = 1.92\ pF \tag{3.15}$$

3.2. Logarithmic ADC implementation

A signed 8-bit, 6-stage, fully-differential, logarithmic pipeline converter is implemented as shown in Figure 3.8. The gain and references values, shown in the figure are derived using Equation (3.7) and (3.8) with C = 3. Much like a linear pipeline ADC, each stage includes a 1.5 bit sub-ADC. However, instead of a 3-level MDAC, one of three gain settings is selected by switching in different values of feedback capacitor across an operational amplifier, depending on the sub-ADC decision. As discussed above, the redundant 1.5 bit architecture relaxes the requirements for comparator and comparator reference voltage accuracy. The accuracy of stage residue is largely unaffected by errors or noise on a distributed reference since the residue is decided by a programmable gain and not MDAC subtraction.

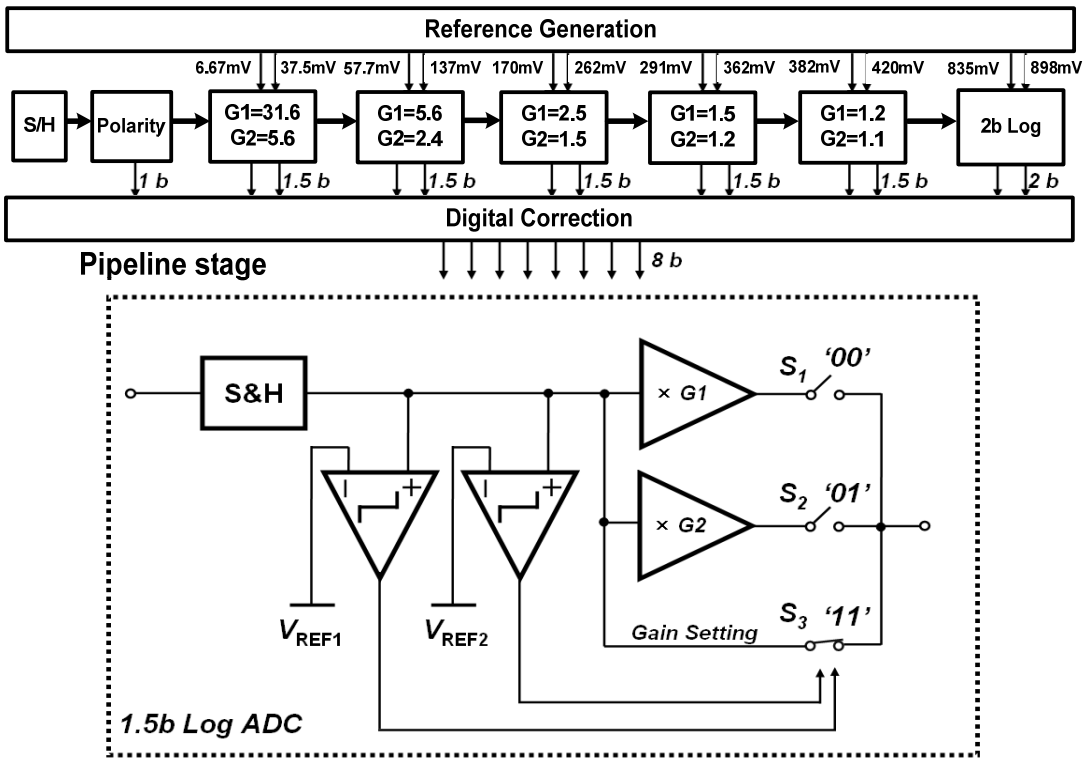


Figure 3.8: Logarithmic ADC architecture.

Figure 3.9 shows a fully differential pipeline stage controlled by two non-overlapping *Φ1* and *Φ2*. One of three feedback capacitors is selected to give one of three different gains depending on the sub-ADC decision. While *Φ1* is high, the stage input is sampled, and the feedback capacitor is reset**.** *Φ2* is the gain phase.

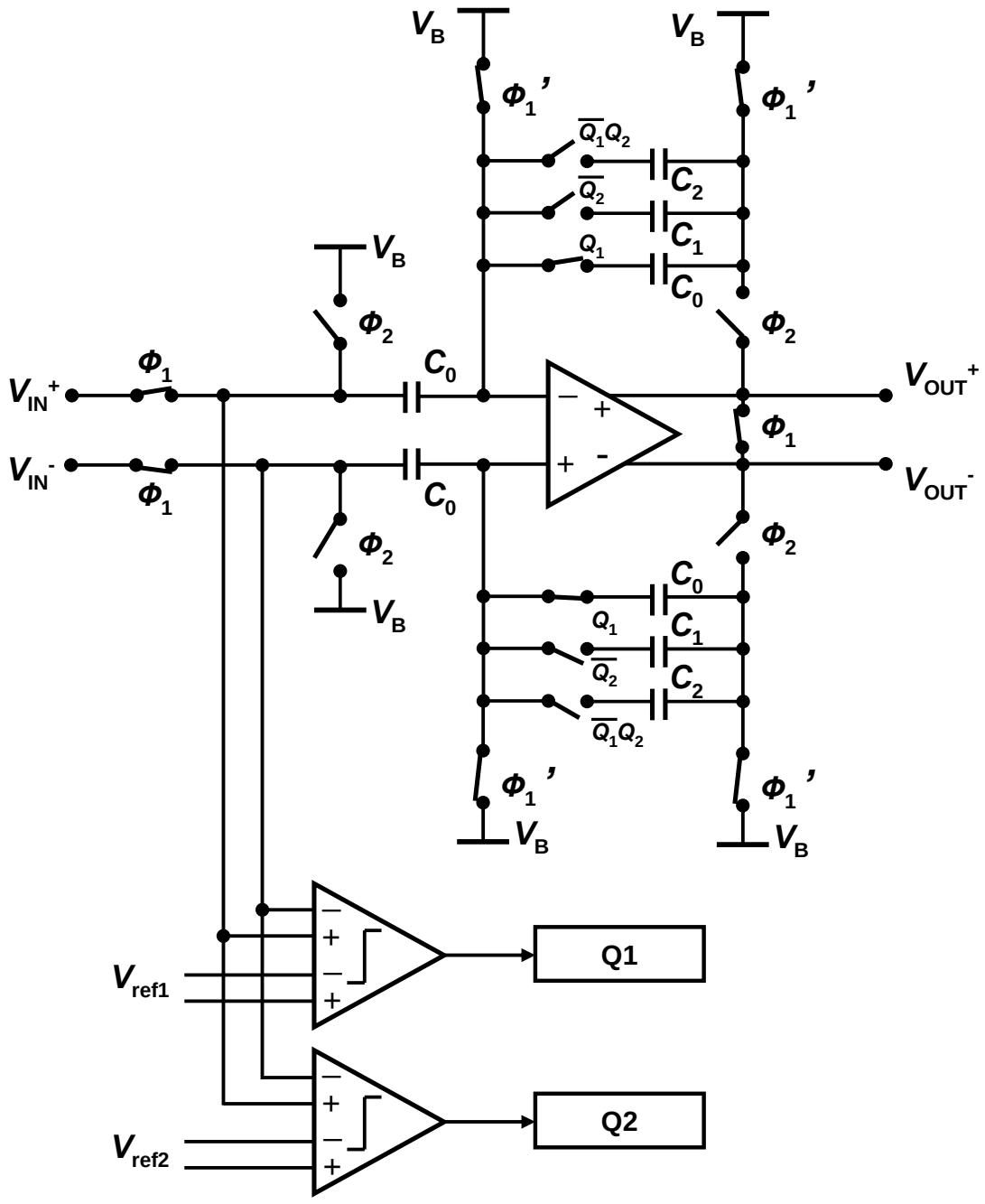


Figure 3.9: Logarithmic ADC stage.

Since this logarithmic stage does not use an MDAC, the reference voltage settling requirement is relaxed by the architecture. The common mode voltage, V_B, is only for the charge extraction for reset to common mode voltage which is 600 mV in the prototype.

The operational amplifiers are implemented as folded cascade telescopic amplifiers with PMOS input pairs. Since large signals are more coarsely quantized than small signals in logarithmic conversion, the logarithmic ADC is less sensitive to OpAmp gain non-linearity.

Since the highest gain setting for the first stage is 31.6 (gain settings are 31.6, 5.6 and 1) a cascade of two programmable SC gain stages is used to implement the first pipeline stage, as shown in Figure 3.10.

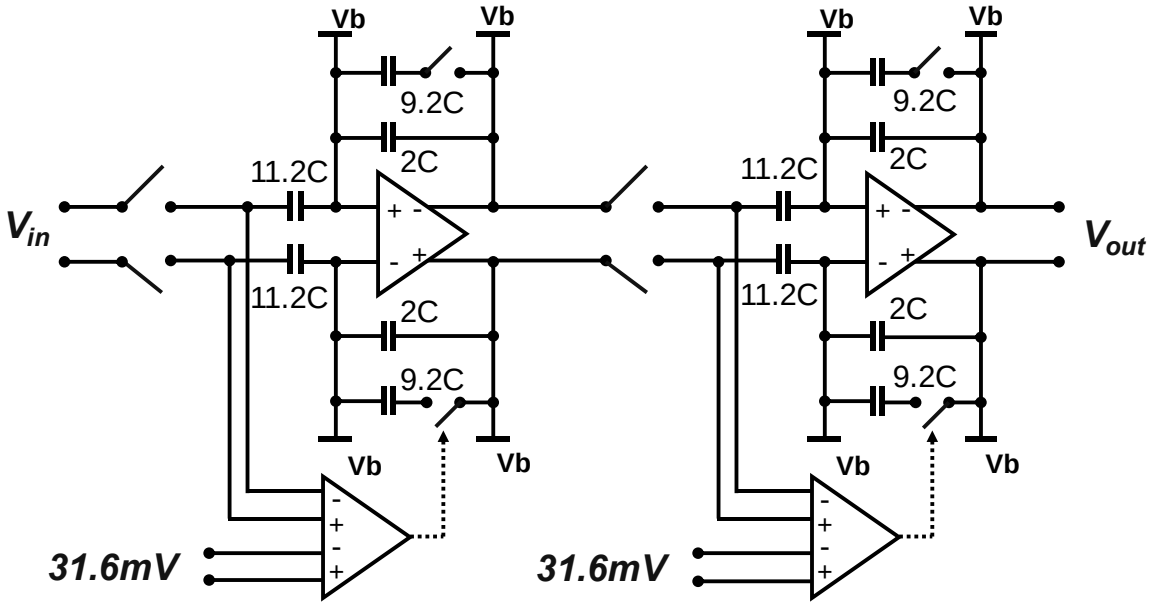


Figure 3.10: The first pipeline stage is comprised of a cascade of two SC amplifiers.

One of the two comparators for the first stage is placed in front of each amplifier. The amplification of the first SC gain stage allows the same reference voltage to be used for both comparators and also relaxes the accuracy required for lower reference voltage.

Subsequent pipeline stages require far less gain and are implemented with single SC amplifiers. The sixth stage of the pipeline is a 2-bit logarithmic flash ADC. All stage reference voltages are generated on-chip.

A logarithmic function does not define for negative inputs, but most differential natural signals have a polarity. To handle negative signals, a first sign decision is made at the front of the pipeline as shown in Figure 3.11. The sign stage determines the input polarity, and if necessary inverts the polarity of input to the remainder of the pipeline. This sign decision must ultimately be made at the full accuracy of the ADC. To achieve the required accuracy, the sign decision is made by a combination of two comparators; one after the front-end SHA and another at the output of the first stage. The second comparison is much more accurate because of the gain of the first stage. The estimate made by the front-end comparator is sufficiently accurate to allow the first stage to correctly process the input. For small inputs where the ADC is more sensitive to sign errors, the first stage is set to the high gain setting of 31.6, with each of the cascaded amplifiers providing a gain of 5.6. In the prototype device, the first decision has a tolerance equal to the lower threshold of the first stage (1.22 mV), whereas the second decision has a margin of 6.83 mV because the second decision is made after 5.6 times multiplication at the first stage. If the first decision is wrong, the second comparator corrects the polarity. An XOR of the first decision and the second decision generates the sign bit (MSB).

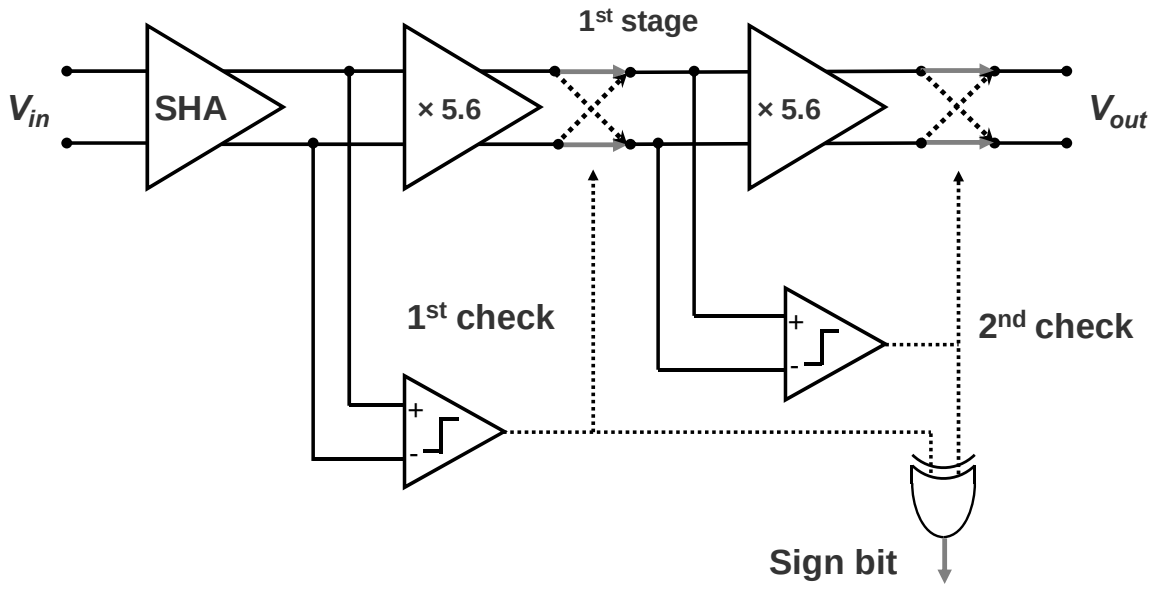


Figure 3.11: Polarity decision.

The sample and hold circuit uses a single capacitor between input differential signal and output nodes for fast and linear operation [69] as shown in Figure 3.12. The operational amplifier used in sample and hold circuit has the same folded cascoded structure as that of the amplifiers in the pipeline stages. To minimize the effect of charge injection, bottom plate sampling is used [78]. During the sampling phase, *Φ1*, common mode voltage is provided internally to reset the input nodes and output nodes to the common mode. At the amplifying phase, *Φ2*, the signal paths are flipped to the output nodes and the charge on the input nodes are transferred to output nodes.

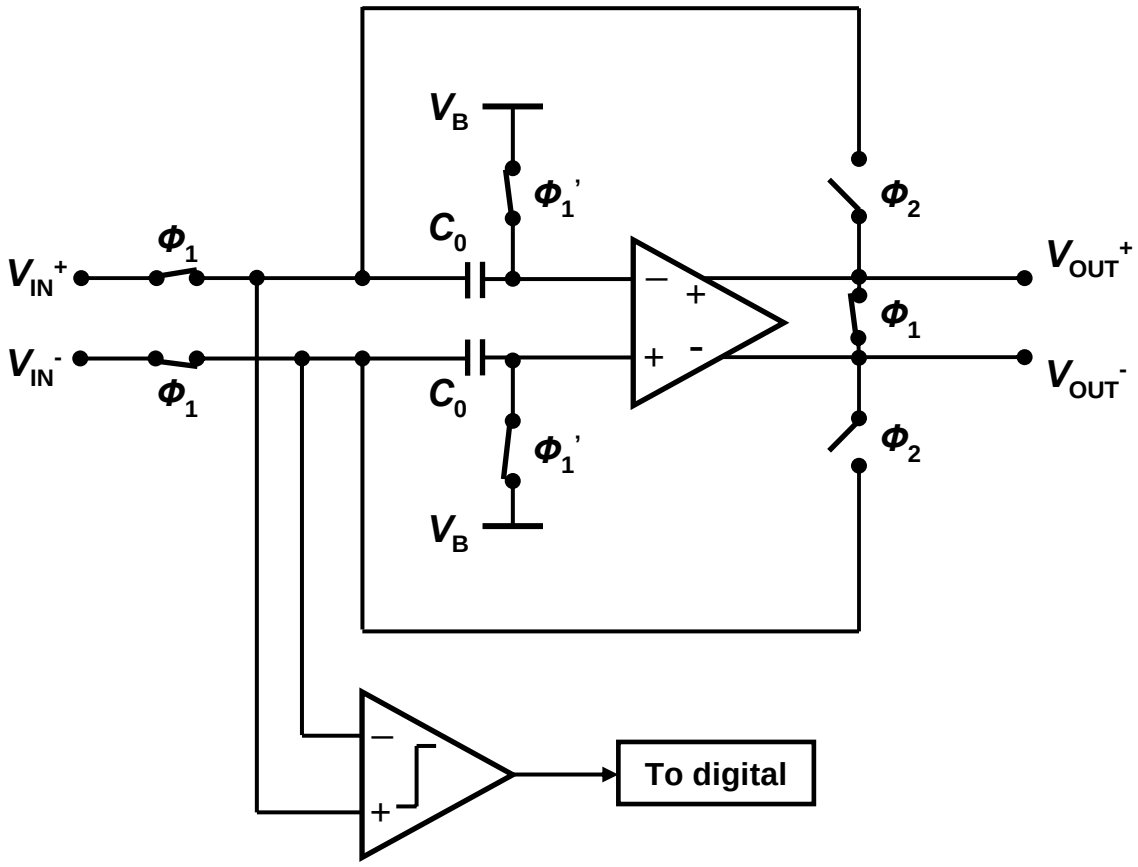


Figure 3.12: Sample and hold circuit, and first polarity check comparator.

A two-stage regenerative comparator technique based on [79] is employed. D flip-flops perform synchronization of data from different stages and a ripple-carry adder adds the synchronized data to produce the overall 8-bit digital output [80, 81].

3.3. Prototype measurements

A prototype device is fabricated in 0.18 μm CMOS with a metal-insulator-metal (MiM) capacitor option and occupies 0.56 mm^2 (2.1 mm^2 including I/O) as shown in Figure 3.13. The ADC consumes 2.54 mW at 22 MS/s (including clock, reference generation, biasing, and digital circuitry).

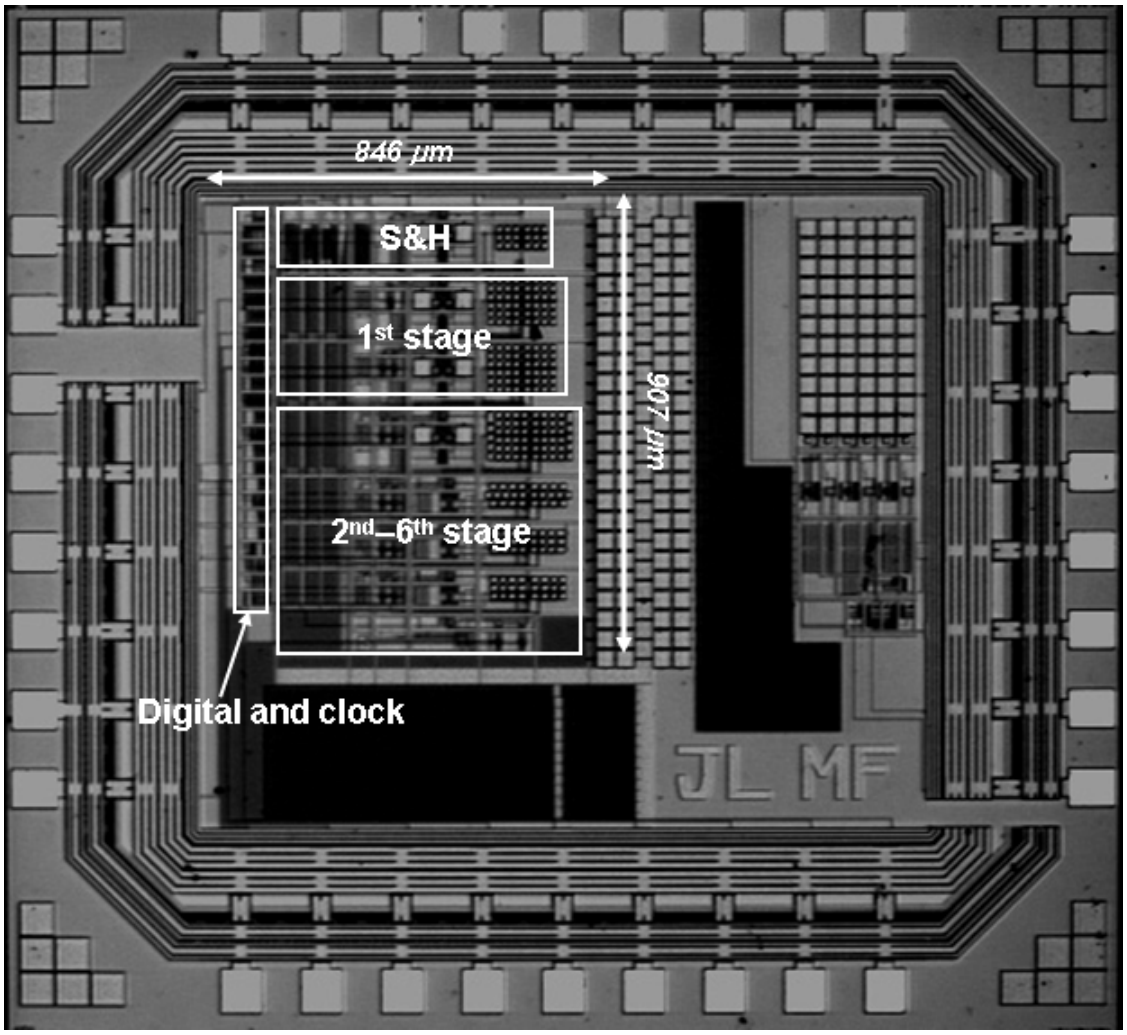


Figure 3.13: Logarithmic ADC die micrograph.

Plots of the DNL and INL values obtained from measurements of the prototype ADC are shown in Figure 3.14. The definitions of DNL and INL for a logarithmic ADC are similar to those for a linear ADC except that in a logarithmic ADC the ideal step size is different for each code.

$$DNL(j) = \frac{V_{trip} - V_{ideal}}{V_{ideal}}, \qquad INL(j) = \sum_{i=1}^{j} DNL(i)$$
$$, j \in \{x \mid x \in \mathrm{N}, \quad 1 \le x \le 2^L - 2\} \tag{3.16}$$

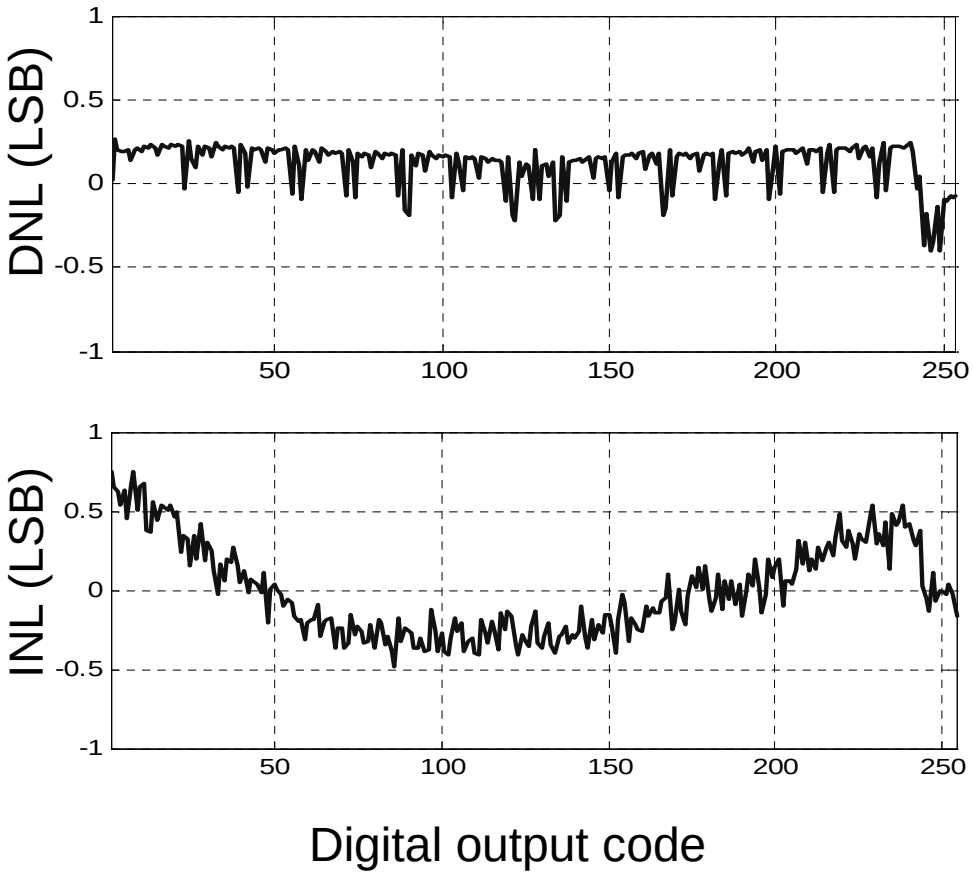


Figure 3.14: Measured DNL and INL of logarithmic ADC.

The major difference between a linear and a logarithmic ADC is that, for the latter, the LSB size varies along with the input signal (while the ratio of adjacent trip voltages remains constant). To measure DNL and INL, we exploit the fact that a logarithmic ADC with an exponential input voltage behaves like a linear ADC. The measured maximum |DNL| and |INL| are 0.22 LSB and 0.77 LSB, respectively.

Figure 3.15 shows the measured dynamic performance versus input amplitude. The peak measured DR, spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are 80 *dB*, 44 *dB* and 36 *dB*, respectively. The dynamic range is far greater than that of a linear ADC, however non-linear logarithmic conversion somewhat degrades peak SNDR. Nevertheless, the measured peak SNDR is close to the 37.9 *dB* ideal value for compression of $C = 3$ implemented in the prototype. Figure 3.16 and Figure 3.17 show the measured dynamic performance versus input frequency and sampling frequency, respectively.

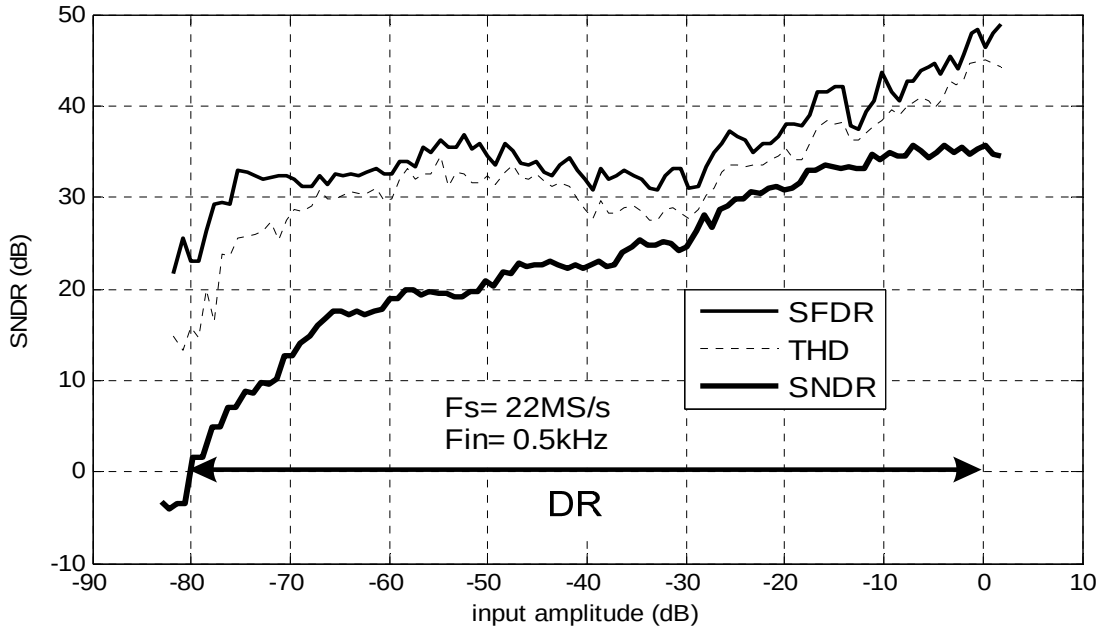


Figure 3.15: Measured SNDR, SFDR, and THD versus input amplitude.

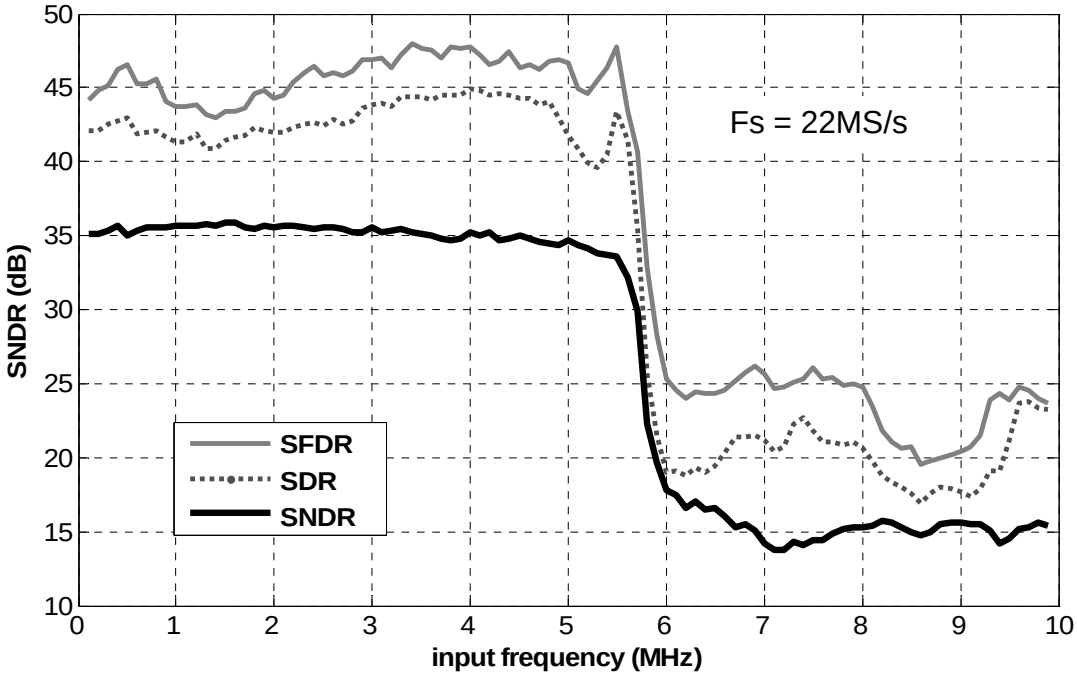


Figure 3.16: Measured SNDR, SFDR, and THD versus input frequency.

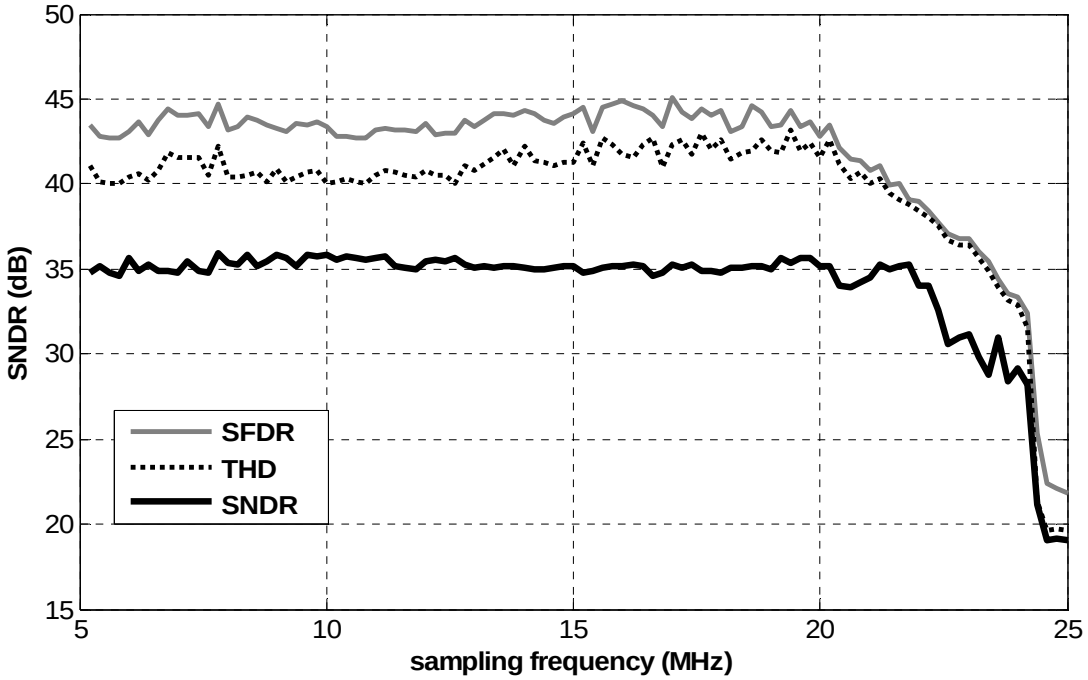


Figure 3.17: Measured SNDR, SFDR, and THD versus sampling frequency.

A logarithmic pipeline ADC architecture that does not rely on squaring or device exponential behavior is proposed and implemented. Since the pipeline does not include MDAC, the required accuracy of the reference voltage is relaxed. A prototype logarithmic ADC was fabricated in 0.18 μm CMOS technology and the measurements of the logarithmic ADC prototype show a high dynamic range, comparable to sigma-delta ADC, but achieved with a wide bandwidth and very low power consumption.

Two figures of merit are compared with recently published converters in Table 3.1. The figure of merit (FOM_1):

$$FOM_1 = \frac{Power}{2^{ENOB} \times Fs} J / conversion.step \tag{3.17}$$

(based on total power consumption including clock, reference generation, biasing, and digital circuitry) is 2.38 *pJ*/conversion step. The dynamic range figure of merit (FOM_2) is 174 *dB*.

$$FOM_2 = 20log_{10}(DR) + 10log_{10}(BW) - 10log_{10}(Power) = 174\ dB \tag{3.18}$$

Table 3.1: Performance comparison

	[72]	[82]	[83]	**This Work**
Dynamic Range	60*dB*	58.4*dB*	77*dB*	**80.2*dB***
Topology	log diode	Linear	∑Δ	**log pipeline**
Speed (2x BW*)	312.5*S/s*	30*MS/s*	20*MHz**	**22*MS/s***
SNDR	49*dB*	58.4 dB	69*dB*	**35.6*dB***
Power	3μW	4.7*mW*	56*mW*	**2.54*mW***
FOM_1 (*pJ*/con)	40.1	0.23	0.24	**2.38**
FOM_2 (*dB*)	137.2	156.5	162.5	**174**

CHAPTER IV

Closed-loop Deep Brain Stimulator

This chapter describes a 64 channel closed-loop deep brain stimulator that searches for the optimum treatment parameter of Parkinson's disease by sensing tremors in neural signals. The system provides programmable current stimulation and senses neural signal with 8 channel pre-amplifier and a 200 *kS/s* 8 bit logarithmic ADC. The entire device, implemented in 0.18 μm CMOS, occupies 2.67 mm^2, and consumes 112 μW in normal operation mode and 351 μW in configuration mode from a 1.8 V supply [84]. This device provides continuous stimulation pulses in normal operation mode, while in configuration mode it performs simultaneous neural recording for parameter settings as well as the current stimulation.

4.1. Closed-loop DBS device architecture

As discussed in Chapter 1, Parkinson's disease is a progressive neurological disorder, affecting more than three million people in the United States. Deep Brain Stimulation (DBS) is one of the most effective treatments of Parkinson symptoms. DBS excites the Subthalamic Nucleus (STN) with a high frequency electrical signal. This chapter describes a single-chip closed-loop DBS. Closed-loop feedback of sensed neural activity promises better control and optimization of stimulation parameters.

Thanks to a novel architecture, the prototype system incorporates more functionality while consuming less power and area compared to other systems. Eight front-end low-noise neural amplifiers (LNAs) are multiplexed to a single high-dynamic-range logarithmic pipeline analog-to-digital converter (ADC). Instead of an analog filter, an on-chip digital filter separates the low frequency neural field potential signal from the neural spike energy. To alleviate disease symptoms, a 64 digital-to-analog converter (DAC) stimulator channels generate independent, bi-phasic, stimulation current signals. An on-chip controller sets the stimulation pulse amplitude, duration and repetition rate, spanning the effective range of parameters for clinical usage.

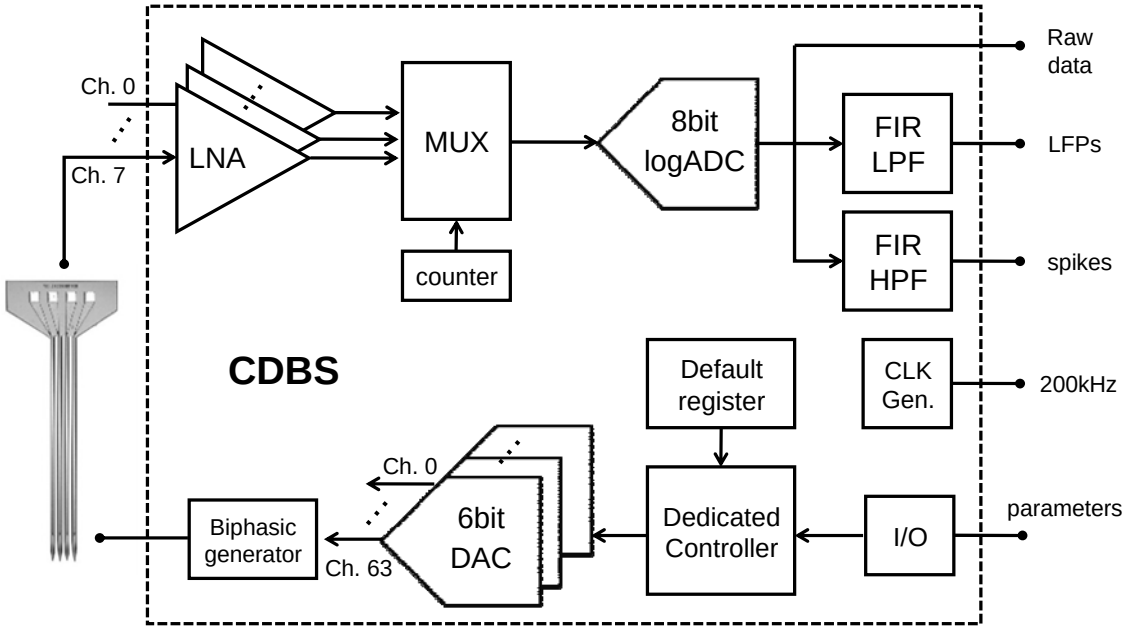


Figure 4.1: The system architecture of CDBS.

Figure 4.1 shows a block diagram of the device architecture. Low power consumption is the key for longer battery life. The device directly interfaces with recording and stimulation electrodes. Eight recording electrodes [46] are implanted in the motor cortex and 64 stimulating electrodes are implanted in the STN [85]. Important information is gained both from the neural voltage spikes (400 *Hz* to 5 *kHz,* with amplitude levels up to ±500 μV) and the low frequency field potential (10 *Hz* to 50 *Hz,* with amplitude levels up to ±10 *mV*). The eight channels are fed through individual LNAs and multiplexed into a single high dynamic-range pipeline logarithmic.

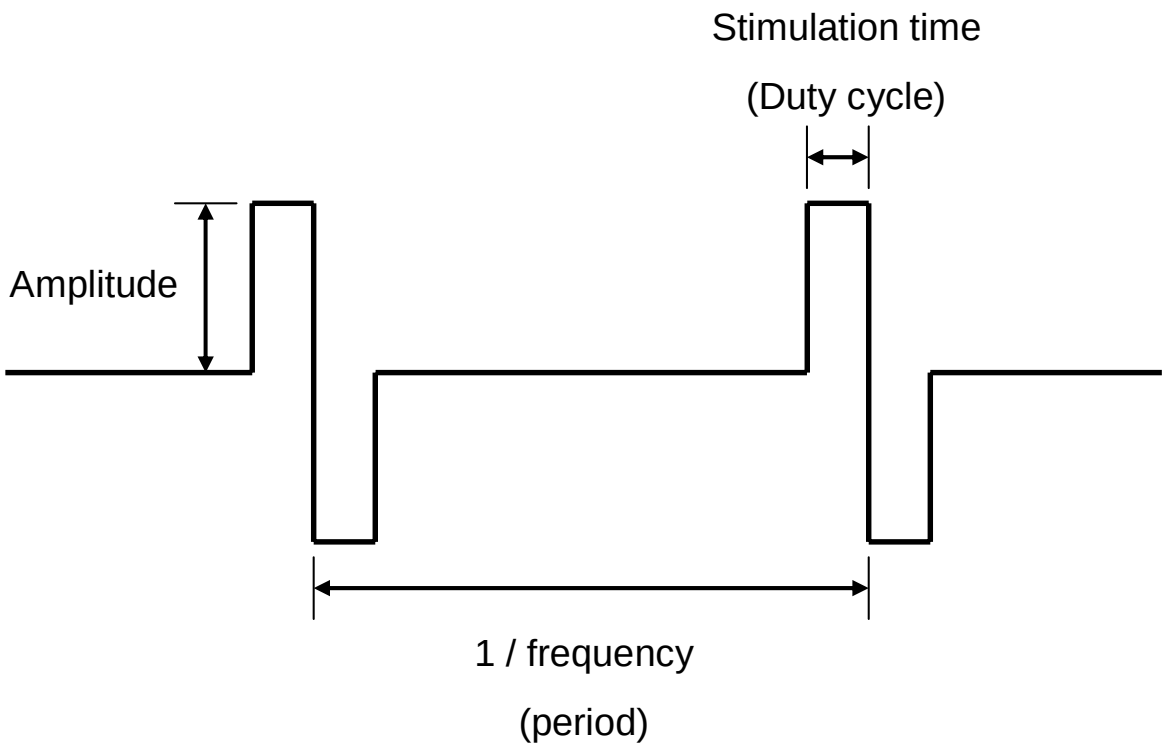


Figure 4.2: Signal parameters of stimulation.

An electrical current stimulation system has been developed to span the range of effective parameters for treatment of Parkinson's disease and Dystonia. Each of the electrical parameters including amplitude, pulse width and stimulating frequency (rate), as shown in Figure 4.2, must be optimized to treat the disorders.

In commercial voltage-stimulating devices, the amplitude for clinical use ranges from 0 V to 10.5 V. However, considering the optimization of battery life and efficacy for the implanted device, it is not necessary for the voltage to be above 3.6 V. An increase in voltage amplitude above 3.6 V may result in a minimal change in the clinical effects, yet drains battery and significantly reduces battery longevity [86]. However, since the impedance of the chronically implanted electrodes gradually increases by a reactive tissue response, the supplied charge to tissue with the voltage stimulation may decrease [87]. This may worsen the clinical efficacy. Therefore a current stimulation is superior to the voltage stimulation because the amount of charge injection never changes for the entire period of DBS treatment.

The pulse width range of the stimulation pulses is between 60 μs and 450 μs, with 60 μs being a default. With the Medtronics neurostimulators, if an amplitude of 3.6 V is not sufficiently effective and no stimulation-induced side effects are present, the pulse width can be increased to 90 μs. An increase from 60 μs to 90 μs leads to an increase in battery drainage by approximately 50%. Pulse widths of more than 90 μs are not generally recommended in STN stimulation; however, they are found to help patients with Dystonia [9, 85].

Although the range for stimulation frequency is between 2 Hz and 185 Hz, Medtronic states that as a rule, a frequency of 130 Hz should be used initially [9]. Other

studies suggest that the frequency be above 90 *Hz* [88]. On the contrary, no effect or even worsening of symptoms with stimulation frequencies lower than 50 *Hz* and plateau at 185 *Hz* has been reported from recent studies [9, 88-90]. An increase beyond the tableland may bring more benefit; however, it is important to maintain an optimal ratio of additional benefit to battery drainage.

4.2. Circuit implementation

The eight neural sensing channels are amplified by individual LNAs and are multiplexed into a single logarithmic pipeline ADC. Logarithmic encoding is well-suited to neural signals and is efficient, since a large dynamic-range can be represented with a short word-length. To save area and power consumption, a relatively large dynamic-range ADC is used, making analog automatic gain control unnecessary.

For the integrated logarithmic ADC as shown in Figure 4.3, the code efficiency factor [33] is set to 1 so that the LSB size is $1.8\times10^{-3}\ V_{range}$, indicating a dynamic range of 55 *dB*. Much like a linear switched-capacitor pipeline ADC, each stage includes a 1.5 bit sub-ADC. However, instead of a 3-level MDAC, one of three gain settings is selected by switching in different operational amplifier (Op Amp) feedback capacitors depending on the sub-ADC decision. The redundant 1.5 bit architecture relaxes the requirements for the comparator accuracy and comparator reference voltage accuracy. All ADC-stage reference voltages are generated on-chip. The sampling speed is 200 *kS*/s.

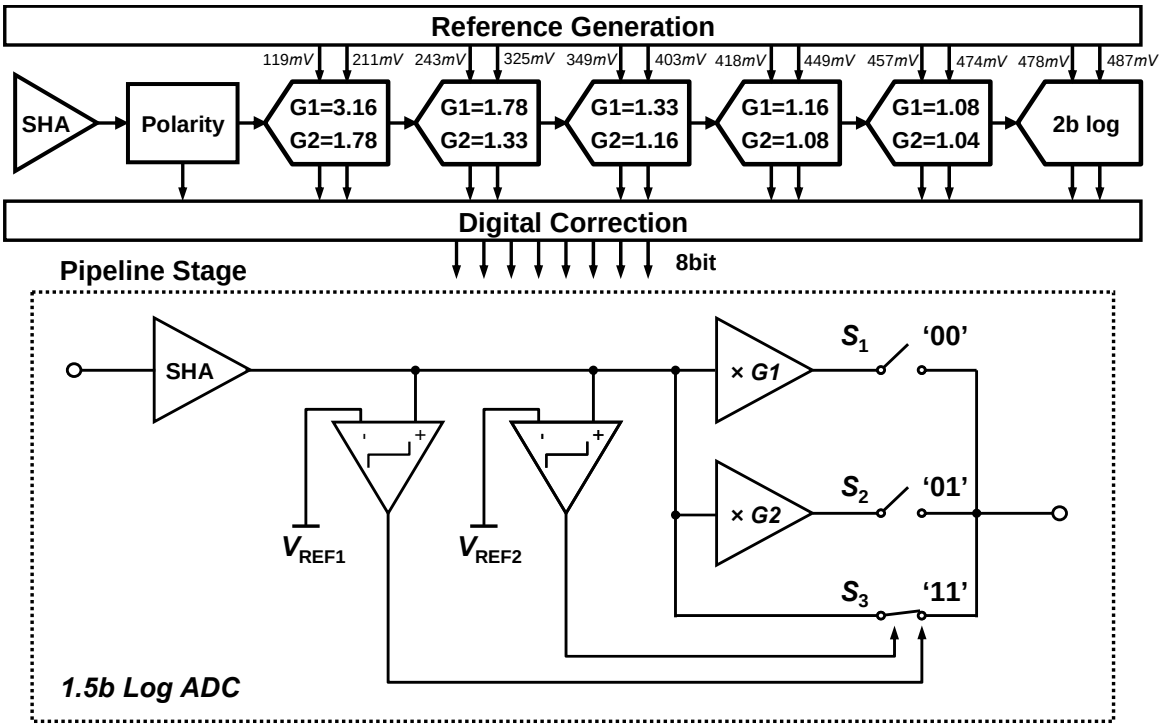


Figure 4.3: Logarithmic ADC integrated in CDBS.

The front-end band-pass LNAs (similar to [31]), have a gain of 100 as shown in Figure 4.4. To minimize 1/*f* noise, PMOS input pairs are used and the gain of the first stage is made large enough, giving an pass-band RMS noise of 5.29 $\mu Vrms$. The high pass zero and the low pass pole are given [50]:

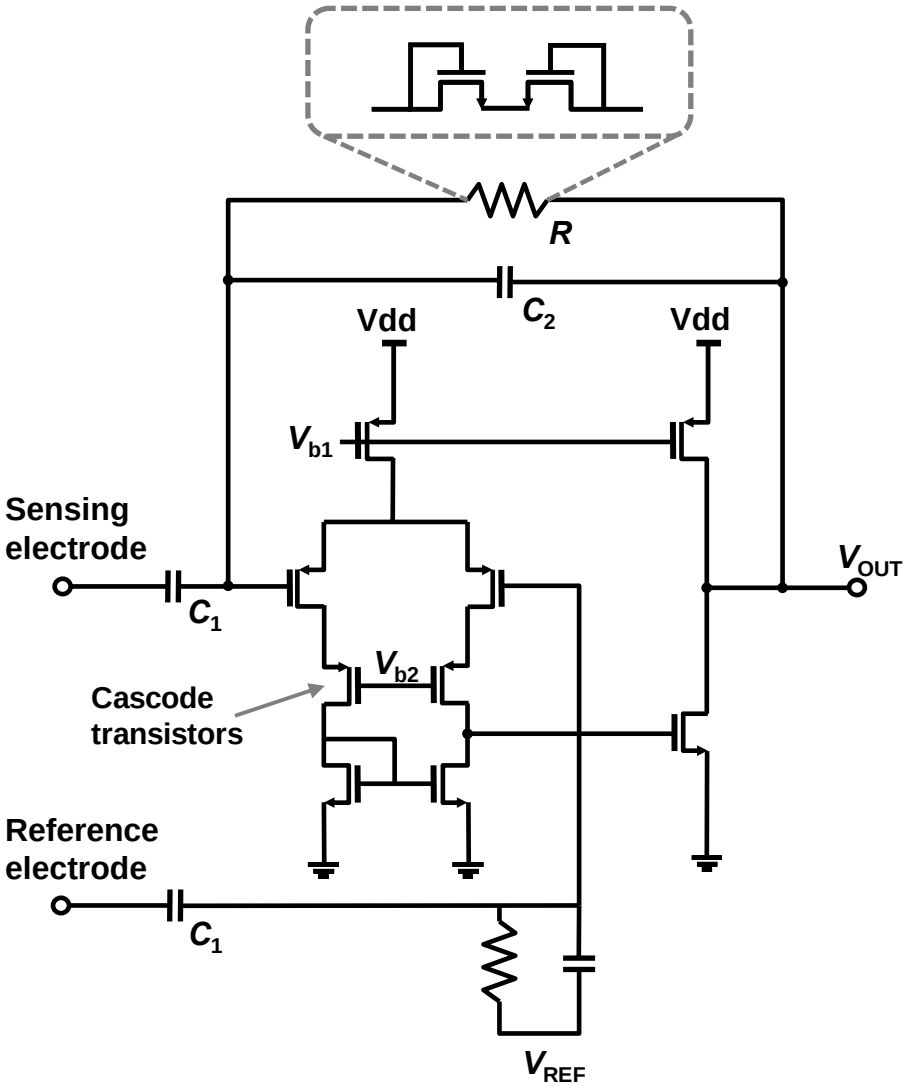


Figure 4.4: Front-end low noise neural amplifier.

$$f_{HF} = \frac{g_m C_2}{2\pi(C_1 + C_2)(C_1 + C_L)}$$

$$f_{LF} = \frac{1}{2\pi R C_2} \tag{4.1}$$

$$A = \frac{C_1}{C_2}$$

Important information for the feedback algorithm is gained not only from the neural voltage spikes (400 *Hz* to 5 *kHz,* with amplitude levels up to ±500 μV), but also from the low frequency field potential (10 *Hz* to 50 *Hz,* with amplitude levels up to ±10 *mV*). The low-frequency LNA pass-band zero is set at 15.8 *Hz*, and the high frequency pole at 5.31 *kHz* so that the LNA pass-band covers both the field potential activity and the spike energy. (From Equation (4.1), C_1 = 10 *pF*, C_2 = 100 *fF,* R = 100 $M\Omega$, g_m = 0.1 μS.) Since a practical implementation of the high resistance consumes too much area in silicon, a diode-connected transistor pair is used to form such a large resistor [58]. In addition, a cascode transistor pair is added to increase the power supply rejection ratio (PSRR).

Separation of the low-frequency field potential from the higher frequency spike energy is done with an on-chip 22 taps finite-impulse-response (FIR) Butterworth type digital filter. Using digital filters instead of analog or mixed-signal filters provide many advantages. First of all, a digital filter is programmable so that its operation may be adjusted without modifying hardware while generally an analog filter may be changed only by modifying the design. A digital filter is used for diplexers to separate two frequency bands of spikes and LFPs. While analog filter circuits are subject to drift and are dependent on temperature, a digital filter does not suffer from these issues, and is extremely robust with respect to both time and temperature.

Unlike an analog counterpart, a digital filter can easily implement higher order filtering with extremely low power consumption. With a use of digital filter, the filter power consumption may be reduced by an order of magnitude. The transfer function of the high-pass digital filter for the spike detection and that of the low-pass digital filter for

the field potential used in the system are shown in Figure 4.5 and Figure 4.6, respectively.

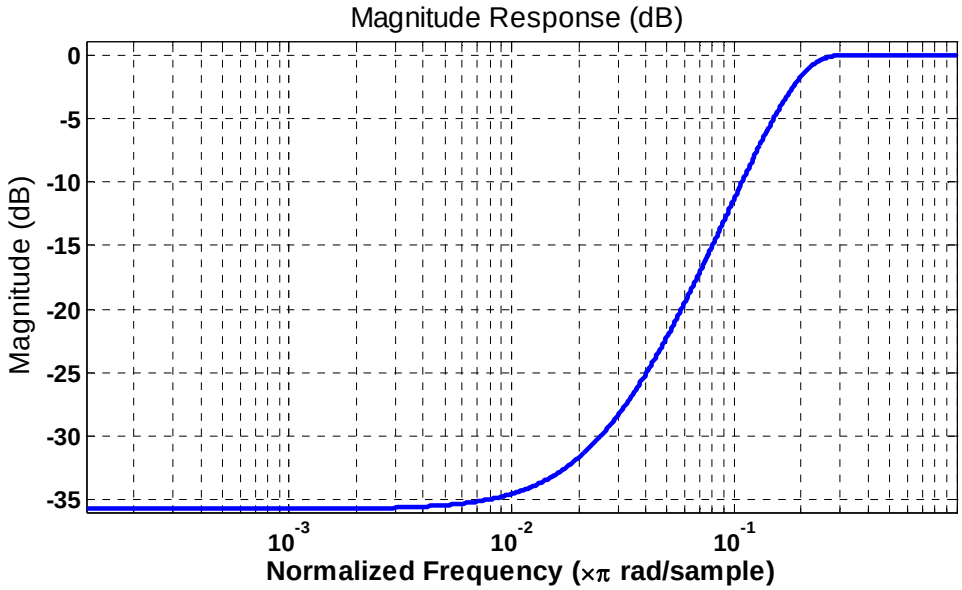


Figure 4.5: High-pass digital filter for the spike detection.

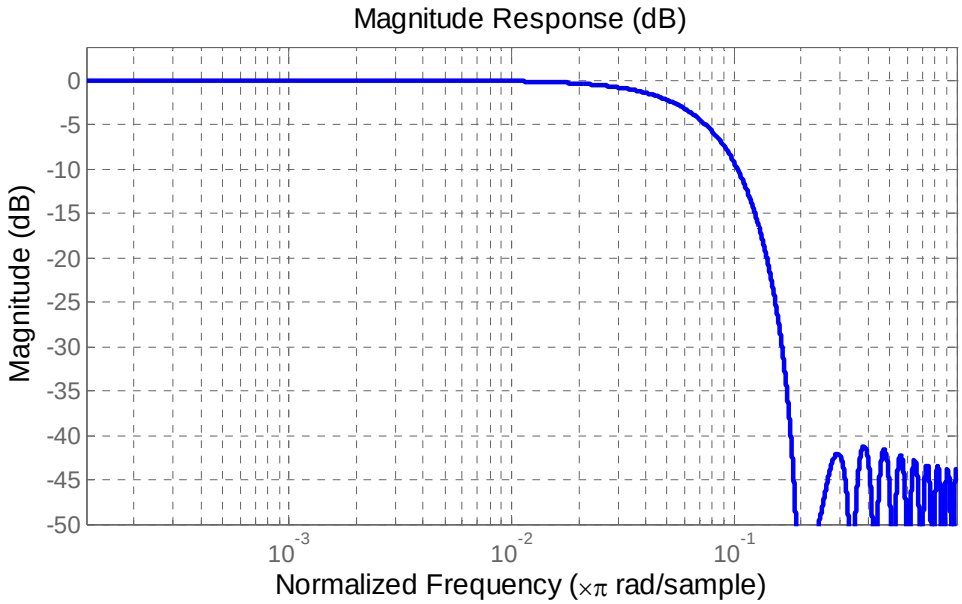


Figure 4.6: Low-pass digital filter for the spike detection.

The stimulation parameters are supplied to the on-chip stimulation controller via an I/O channel. This on-chip controller generates stimulation patterns to control the 64 on-chip current steering DACs. All clocks are generated internally from a single 200 *kHz* external reference.

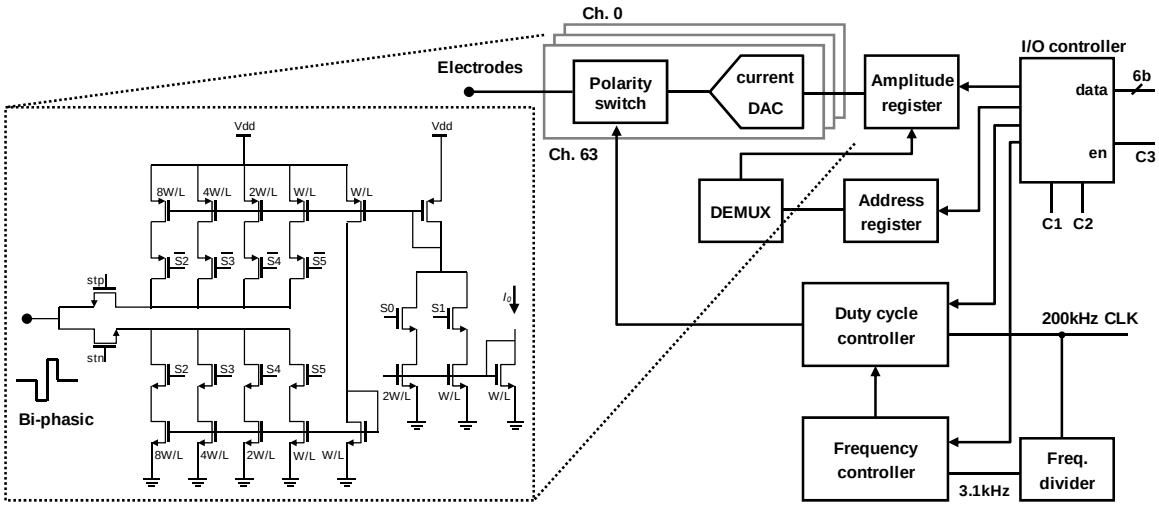


Figure 4.7: 64 channel current DAC controller architecture.

The electrical stimulator generates 64 channels of biphasic charge-balanced current stimulation as shown in Figure 4.7. The stimulation frequency is programmable in the range from 31 *Hz* to 1 *kHz*. The stimulation time (duty cycle) can be set from 5 μs to 320 μs in 5 μs steps. The stimulation current is programmable in 3 μA steps up to a maximum value of 135 μA and the default current amplitude of 100 μA. The stimulation-parameter data registers contain chronological information, such as frequency and duty cycle, and are programmed through a shared 6 bit I/O channel controlled by three control

register pins (C1, C2 and C3). The stimulation parameters are writable through 6 bit I/O, generally in four cycles, depending on the control pins, (see the Table 4.1).

Table 4.1: Stimulation control register operation mode

C3	C2	C1	Functions
0	0	0	Normal recording mode
0	0	1	Low pass filtered recording
0	1	0	High pass filtered recording
0	1	1	Default set up (130Hz, 90μs, 100μA)
1	0	0	Select the channel address to be modified
1	0	1	Set the stimulation current amplitude
1	1	0	Define the duty cycle (stimulation period)
1	1	1	Define the frequency

The 64 DACs are formed as a cascade of a single shared 2-bit coarse current DAC and 64 individual bi-directional 4-bit fine DACs as shown in Figure 4.8. The coarse/fine configuration saves die area since the MSB devices tend to be large. Because the shared 2 MSB DAC operates as a pre-scaler, 48 current values are possible. In the fine ADC, a polarity switch selects the positive or negative DAC output to achieve charge-balanced bi-phasic stimulation, helping to reduce the risk of long-term tissue damage.

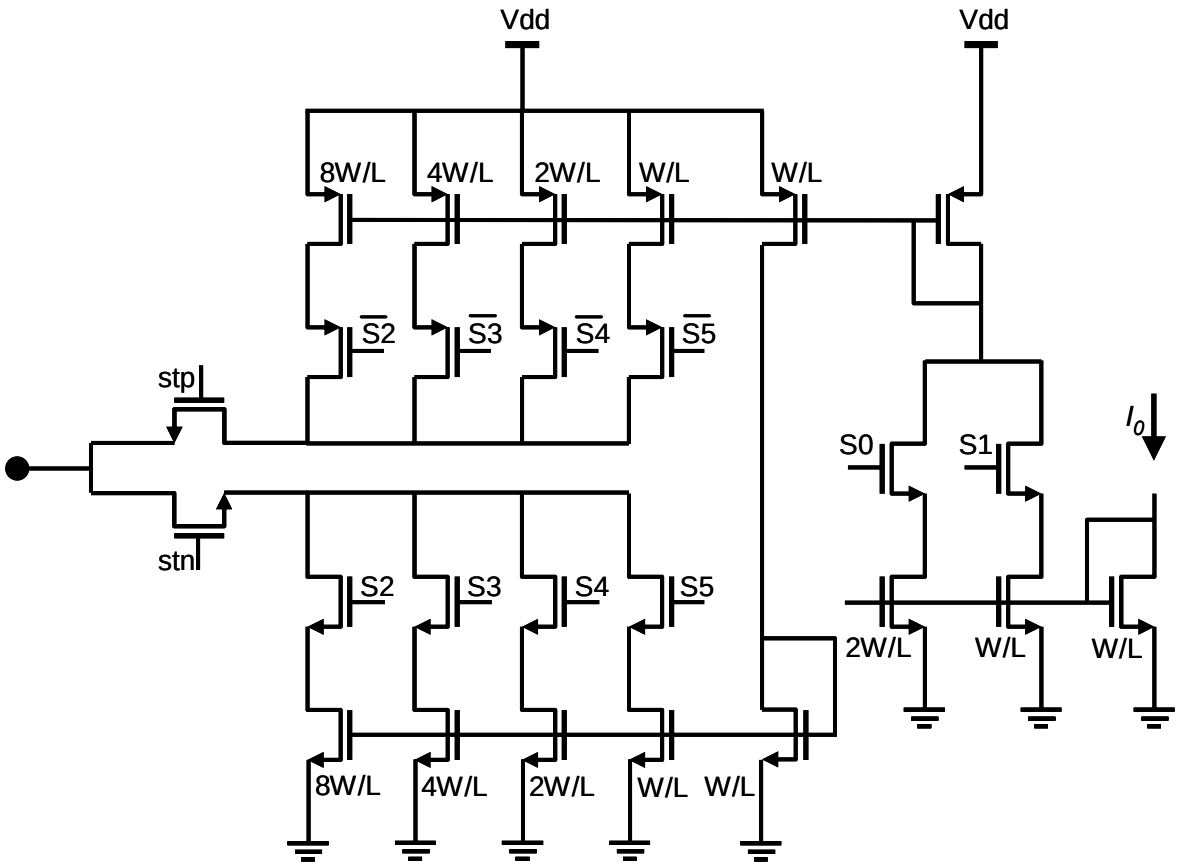


Figure 4.8: MSB shared (2+4) bit bi-phasic current DAC.

4.3. Prototype measurements

A prototype device is fabricated in 0.18 μm CMOS with a MiM capacitor option and occupies 2.67 mm^2 (4.48 mm^2 including I/O) as shown in Figure 4.9. Eight stimulation output has been selected out of total 64 channel DACs since the number of I/O pads are limited. During the configuration mode when the signal patterns to achieve an optimal stimulation are determined, the total power consumption of the entire system, including neural amplifiers, logarithmic ADC, current DAC, controller, digital filters, the reference generation, clock generation and biasing, is 351 μW, which is significantly less

than that of state-of–the-art stimulator circuits. In normal operation mode, an 1.8 V analog supply is turned off so that only current DACs and digital logics are in active because the recording devices do not need to work all the time except during the period of parameter matching. In this mode, the power consumption is only 112 μW.

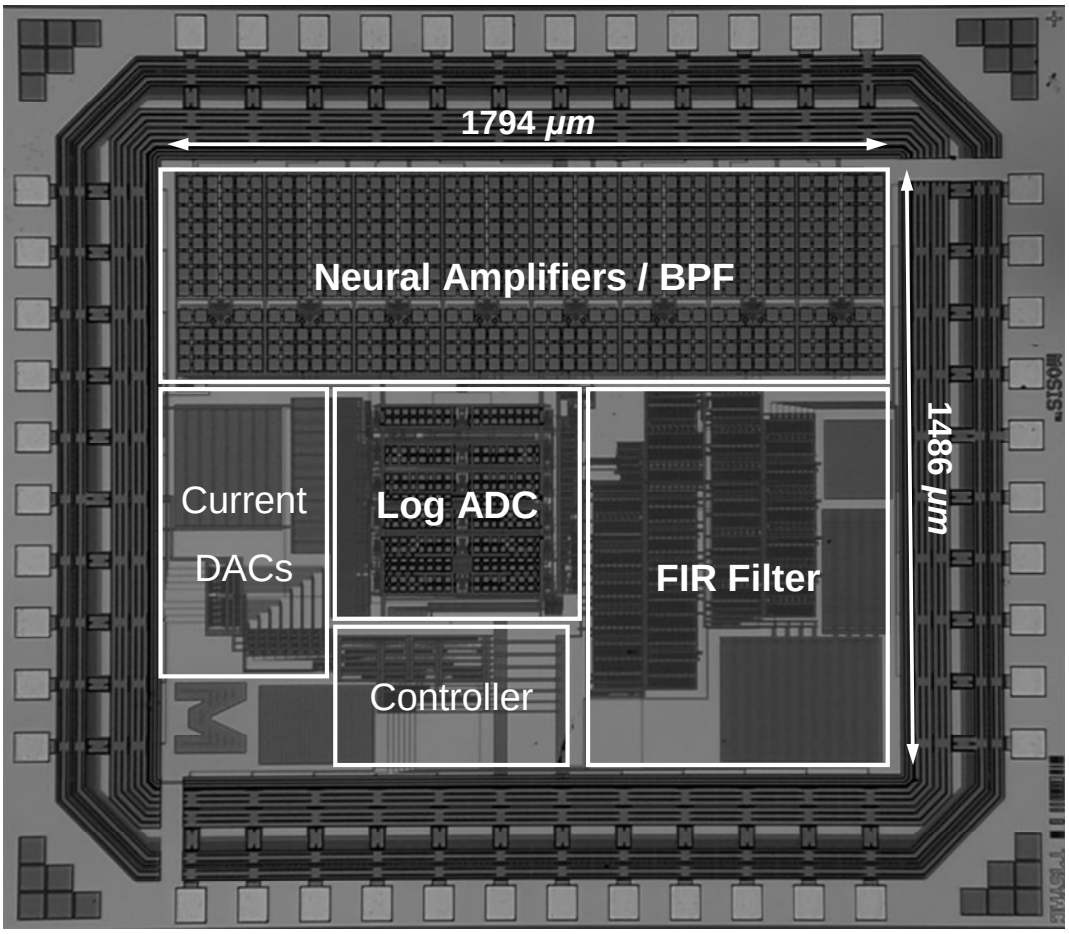


Figure 4.9: Closed-loop DBS die micrograph.

Plots of the measured signal-to-noise and distortion ratio (SNDR) of the combination of front-end neural amplifier and log ADC, as well as the measured DNL/INL of the log ADC, are shown in Figure 4.10 and Figure 4.11, respectively. To measure the frequency response of the recording front-end, the frequency of the input

signal has been swept from 0.5 *Hz* to 10 *kHz* with an increment of 0.1 *Hz*. Since the front-end neural amplifier has a gain of 100, the normalized pass-band gain is measured at 40 *dB*. At 200 *kS/s*, the log pipeline ADC achieves a peak measured SNDR of 44 *dB* for a 1 *kHz* sinusoidal input. The pass-band is lied between 10.8 *Hz* and 5.7 *kHz* similar to the range calculated by Equation 4.1, and covering the frequency of interests.

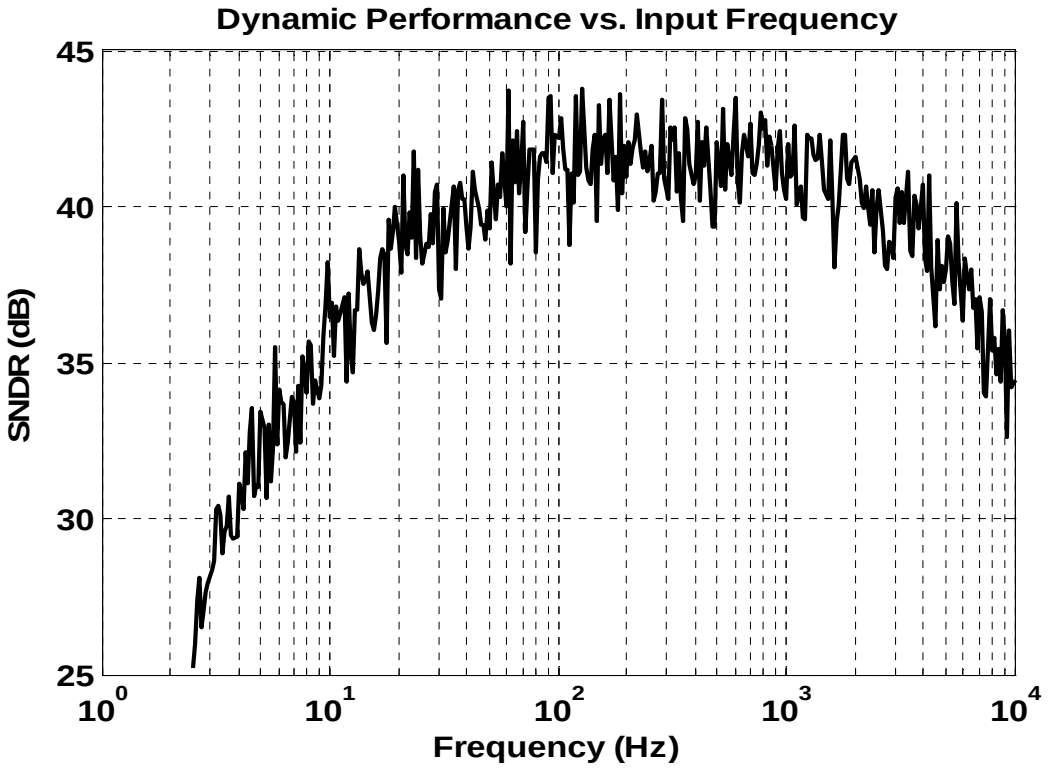


Figure 4.10: Measured SNDR of the combination of the neural amplifier and the log ADC.

The DNL and INL are calculated based on Equation 3.16 and the maximum measured |DNL| is 0.25 LSB and the maximum |INL| is 0.47 LSB.

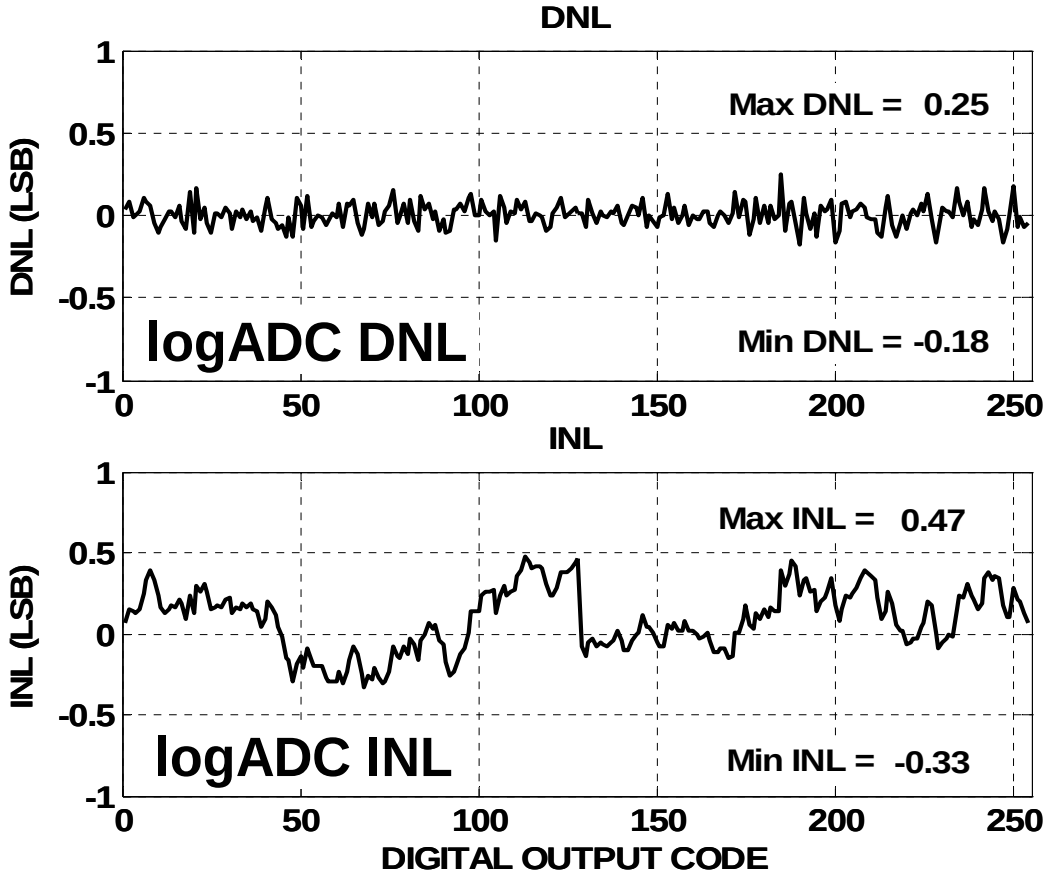


Figure 4.11: Measured DNL and INL of the logarithmic ADC.

To measure stimulation patterns, a 1 $k\Omega$ load is connected to emulate the tissue environment. Figure 4.12 shows the measured output of stimulation DAC with a bi-phasic pattern. With 1 $k\Omega$ load, the measured voltage is around 100 mV indicating that a peak stimulation current is 100 μA for the default set-up. The area under the plot represents the amount of sourced or sinked charge by the stimulator. The measured amount of the supplied charge to the load and the absorbed charge from the load are well matched with 0.1% accuracy.

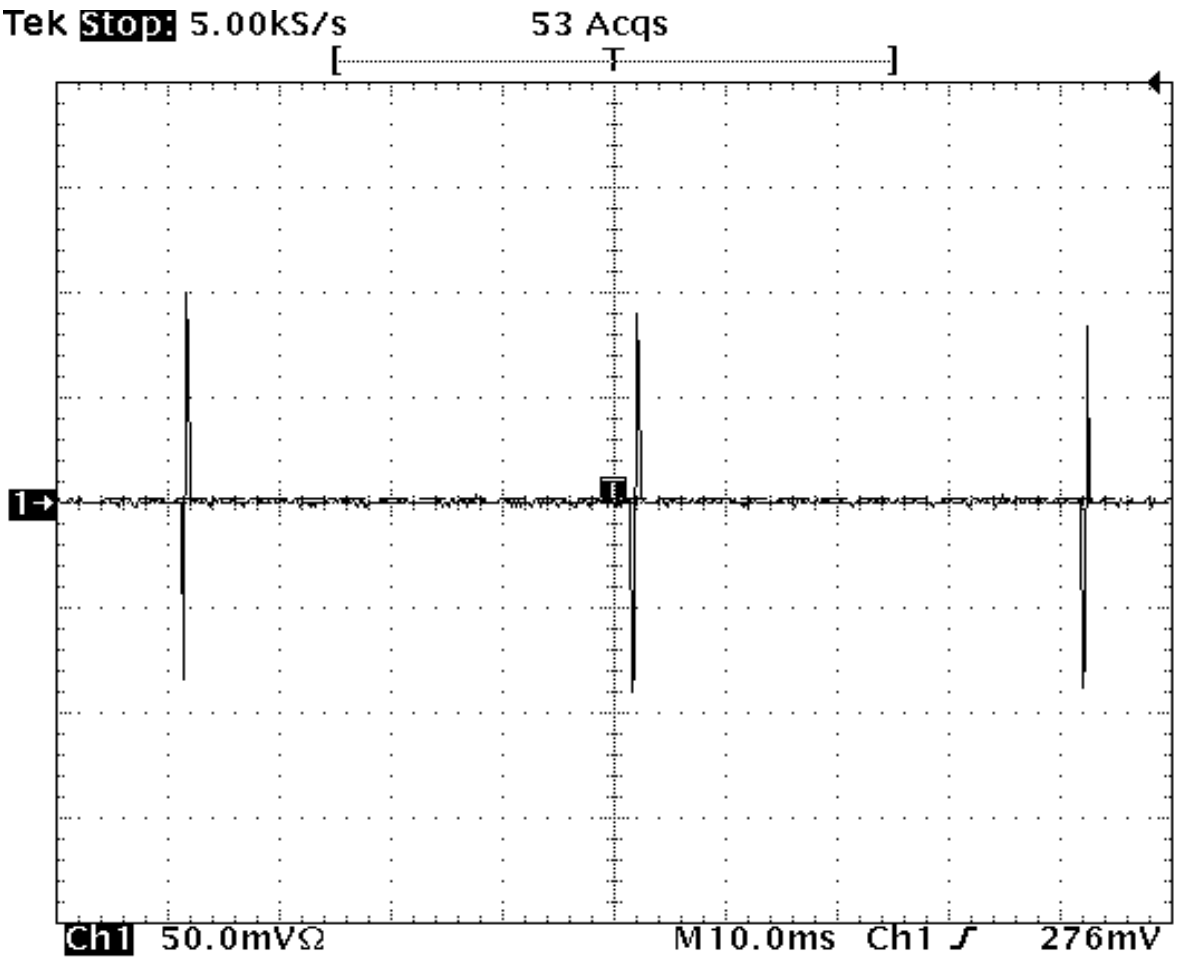


Figure 4.12: Measured output of the stimulation DAC.

Physiological sodium chloride solution (0.9% NaCl) was used for the electrolytic testing of the DACs. Two Platinum electrodes with 5 *mm* length and 0.2 *mm* diameter are put into the chemical solution for the stimulation and reference sites, respectively. The electric potential at the stimulation site is recorded to measure the impedance and the stimulation pattern. The impedance of the electrolytic platinum contact is measured as 1012 Ω at 1 *kHz*. A fine plot of the stimulation output on the electrolytic condition has been showed in Figure 4.13. The stimulation parameters are at default.

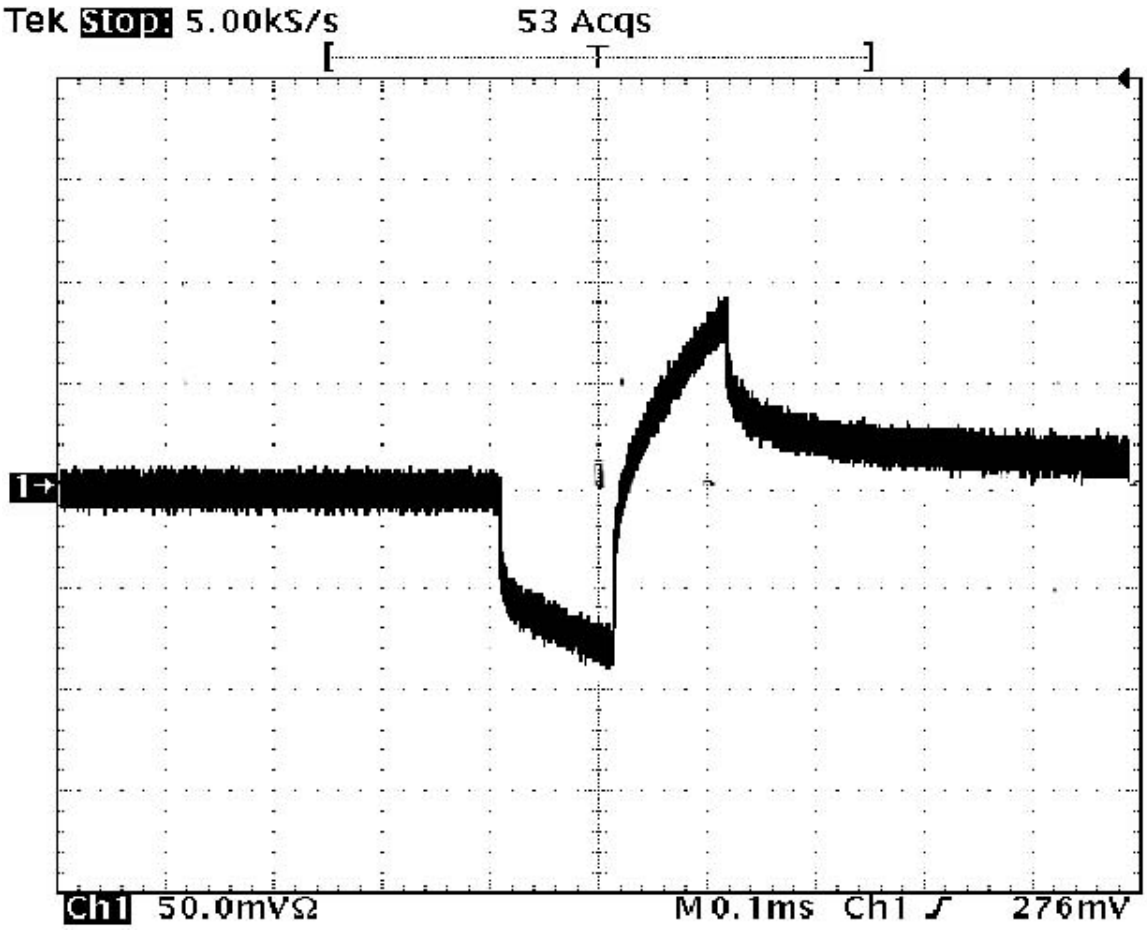


Figure 4.13: Measured output of the stimulation DAC.

The electrolytic measurement of the stimulation device shows some capacitive latency and reaches up to 89% of the final values. However, it still provides balanced bi-phasic stimulation to eliminate the injected charges for electrical safety.

The DNL and INL of the current DAC have been measured by voltage change across the load resistor with amplitude parameter sweeping as shown in Figure 4.14. The current DAC has a maximum measured |DNL| of 0.37 LSB and a maximum measured |INL| of 0.48 LSB.

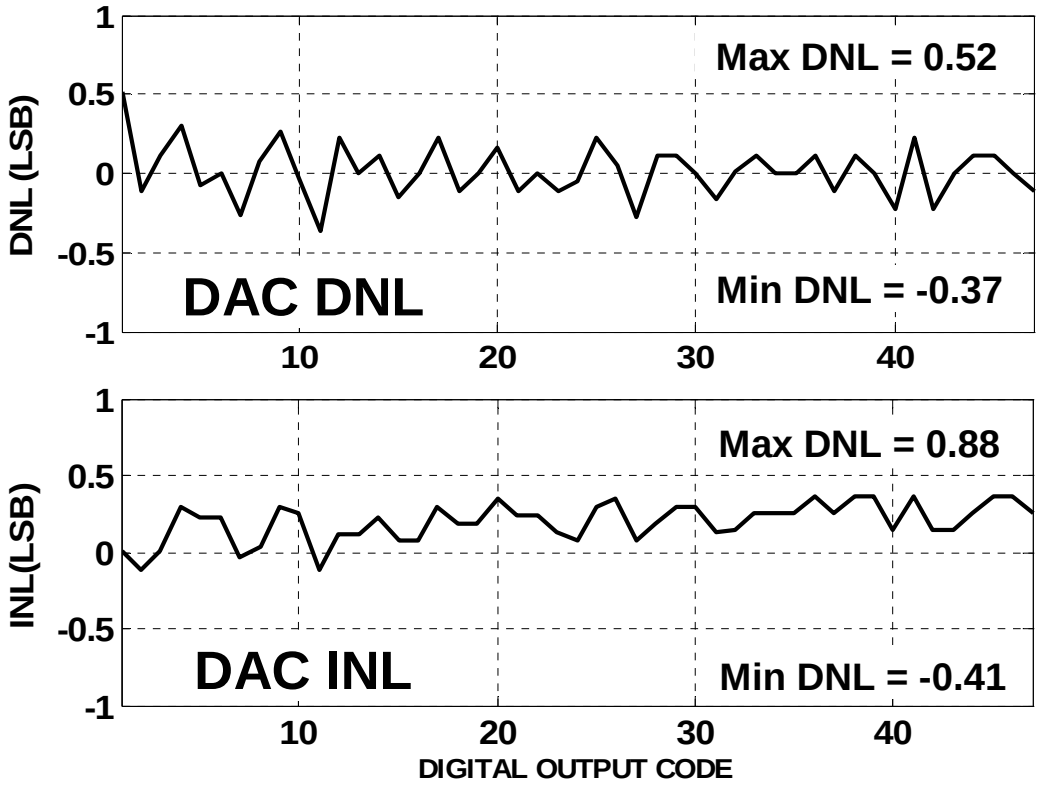


Figure 4.14: Measured DNL and INL of the logarithmic ADC.

Figure 4.15 shows the measured overall frequency responses of the combined front end, ADC and digital filters. The LPF passes only the low frequency field potential information, while the HPF filters out the low frequency signals, passing spikes only. Along with the application of pre-recorded analog brain signals, the high-pass-filter (HPF) output clearly shows neural spikes as well as a periodic stimulation artifact.

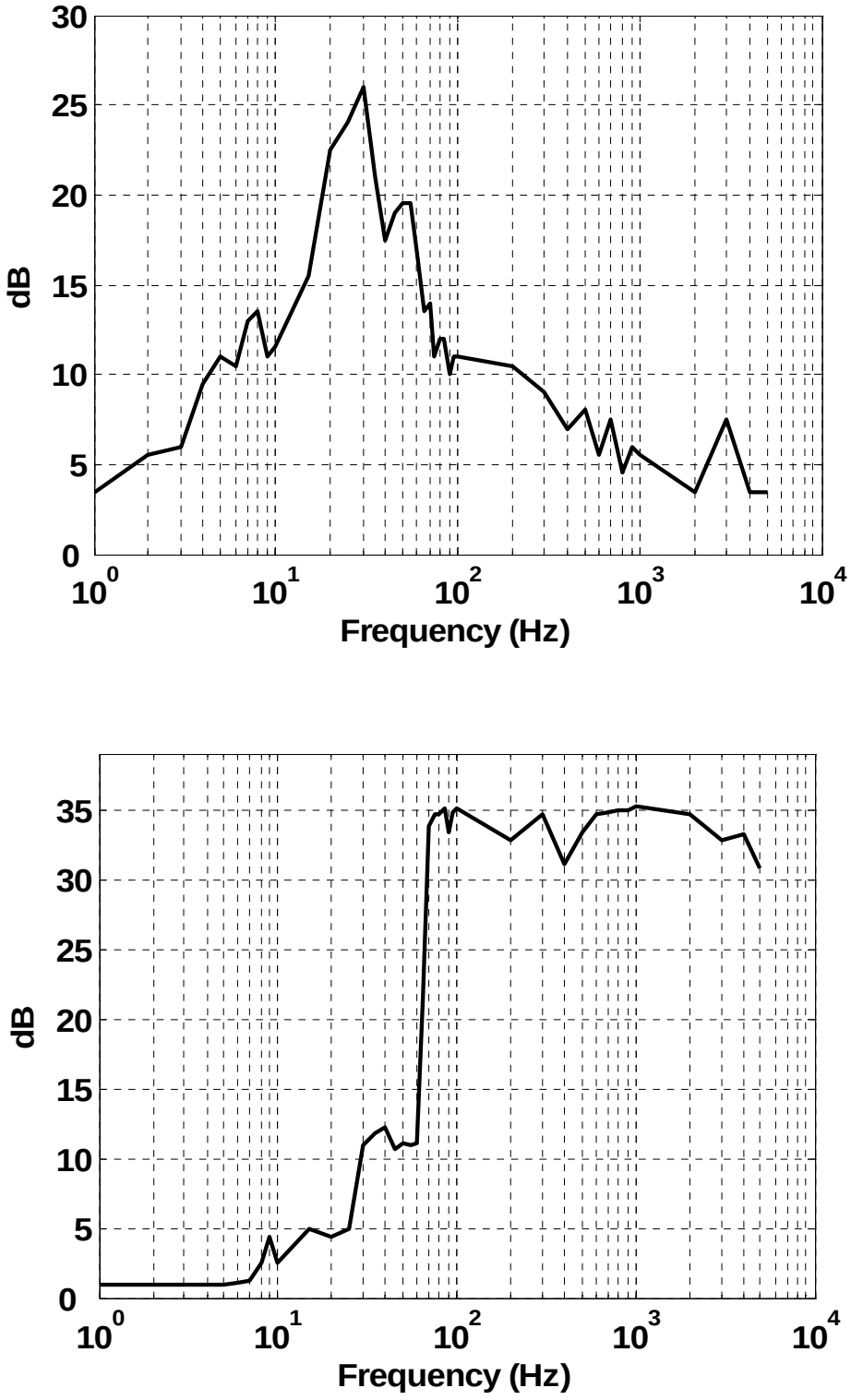


Figure 4.15: Frequency response of neural amplifiers, logarithmic ADC, low pass digital filter (above) and high pass digital filter (below) output.

The device specifications are compared with recently published neural interface systems in Table 4.2. There are two neural recording devices ([31], [92]) and two stimulators ([93], [94]) for the comparison. Harrison et al. has reported a fully integrated neural recording system with a 433 *MHz* frequency shift keying (FSK) transmitter at [31]. The device incorporates low-noise 100-channel neural recording from an implanted Utah electrodes [95]. However, the low data rate (330 *kbps*) delivers only one-bit digitized spike trains which can be used for limited neural applications. In addition, the real three-dimensional (3-D) multi-layer neural recording is impossible with this device, because the Utah probes are coplanar channels. Recently, Chae et el. has presented a 128-channel neural system which has an ultra-wide band (UWB) wireless telemetry with 90 *Mbps* data rate. It can transmit full-scale neural data including the spike shape, spatial and temporal information without any sacrifice of active channels. However, there is still no genuine stand-alone, integrated, and simultaneous device which provides both neural recording and stimulation functionality.

Since the target application of the proposed device is different from general brain-machine interface (BMI) systems described in [31] and [93], only eight numbers of recording channels are sufficient. However, the power consumption of each LNA channel is dramatically reduced by the mixed-signal filters which relax the front-end analog filtering requirements. Also, integration of the efficient high dynamic range log ADC significantly saves power consumption of the whole system.

The stimulating performance of the CDBS is more advanced. It provides a flexible stimulation with 64 independently programmable channel DACs. Also, the device has only 7.4 μW power consumption for each stimulation channels, increasing

efficacy and longevity of a battery life. The total power consumption in full-configuration mode is comparable to the commercial Medtronics neurostimulator, but the proposed system has a larger number of stimulation channels as well as an eight-channel recording unit. The device was designed and fabricated in sub-micron CMOS circuit technology, and the feasibility of state-of-the-art semiconductor technology and emerging biotechnology was verified.

Table 4.2: Performance comparison

	[31]	[92]	[93]	[94]	**This work**
Application	Recording	Recording	Stimulator	Stimulator	**Recording + stimulation**
Electrodes	Cortex	Cortex	Cortex	Retina	**STN**
LNA Channels	100	128	0	0	**8**
LNA Pow/Ch.	45.4μW	23.9μW	N/A	N/A	**9μW**
Filter	Analog	Analog	None	None	**Analog/digital**
ADC	10b SAR	6-9b SAR	N/A	N/A	**8b log pipeline**
Stim. # of Ch.	0	0	32	15	**64**
Stim. # of bits	N/A	N/A	6bit	5bit	**7bit**
Stim. Pow/Ch.	N/A	N/A	258μW	87μW	**7.4μW**
Total power	13.5mW	6mW	8.3mW	1.3mW	**0.35mW**
Process tech.	0.5μm	0.35μm	1.5μm	0.5μm	**0.18μm**
Die Size (mm^2)	4.7×5.9	8.8×7.2	4.6×4.6	2.3×3.0	**1.8×1.5**

CHAPTER V

In-vivo neural test

The prototype testing systems were developed in two phases. The first system was developed to measure the electrical performance as described in the previous chapter and evaluate the functionality of the system when applied to an animal. This benchtop system was built with a relatively large printed circuit board (PCB) with conventional instruments including power supplies and logic analyzer as shown in Figure 5.1. The second prototype was then constructed using the wearable version of the PCB and incorporating a wireless telemetry system.

5.1. Benchtop prototype

The benchtop prototype board consists of a CDBS integrated circuit (IC), an 8051 based micro-controller and passive components. Three independent power sources supply 1.8 *V* digital, 1.8 *V* analog and 3.3 *V* electro-static discharge (ESD) protection supplies. During each experimental session, neural electrophysiological data from an eight-channel chronically implanted microprobe were sampled at 25 *kHz*. Recorded data sets were typically 30 *s*ec in duration and repeated ten times a day. Recordings were referenced differentially to a body potential from an anchored screw. These signals were simultaneously amplified and band-pass filtered by the CDBS IC.

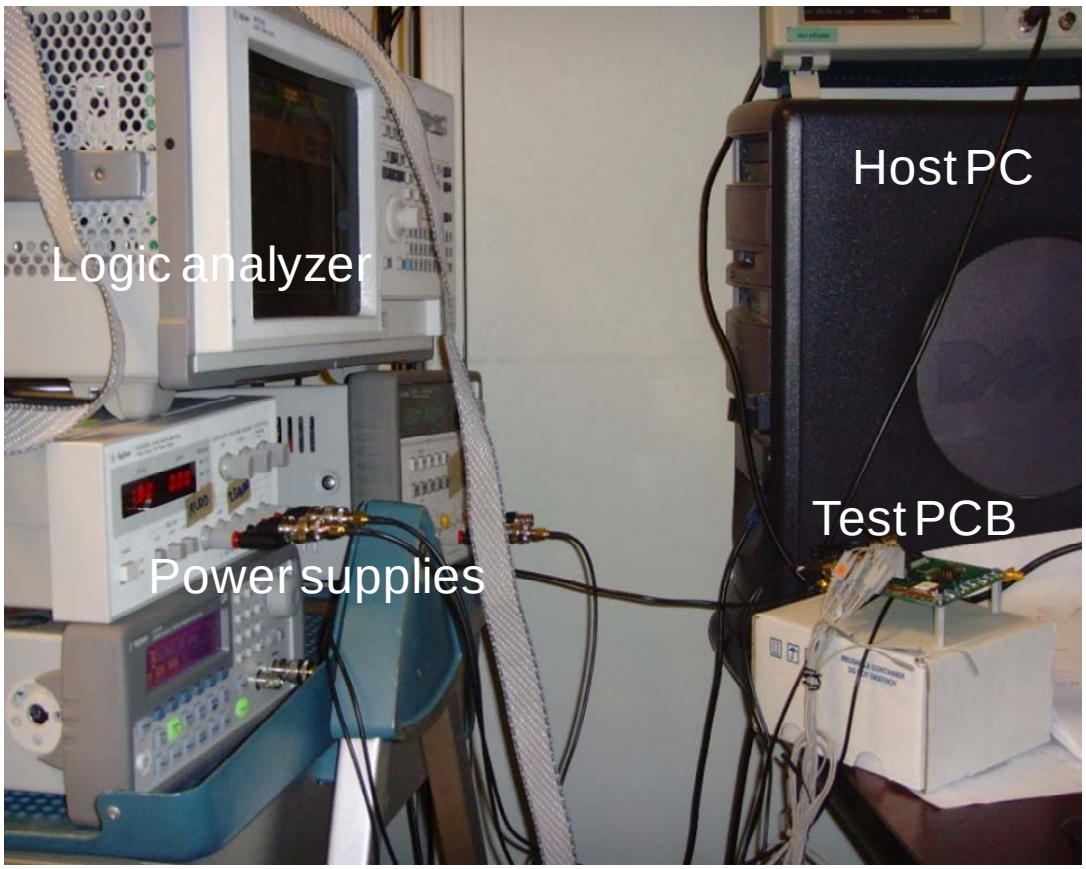


Figure 5.1: Test bench.

The neural information was processed in the CDBS chip, and then, the digitally converted signal was sampled by a logic analyzer which is connected to a host personal computer (PC) with a general purpose interface bus (GPIB) protocol. An ADuC841 chip [96] which is a 8051 based micro controller from Analog Device Inc. is used for the mode control to set up the stimulation parameters and configure the recording filters as described in Table 4.1.

In-vivo intra-cortical neural recording interface was chronically implanted in Long Evans rats for long-term neural data collection as shown in Figure 5.2.

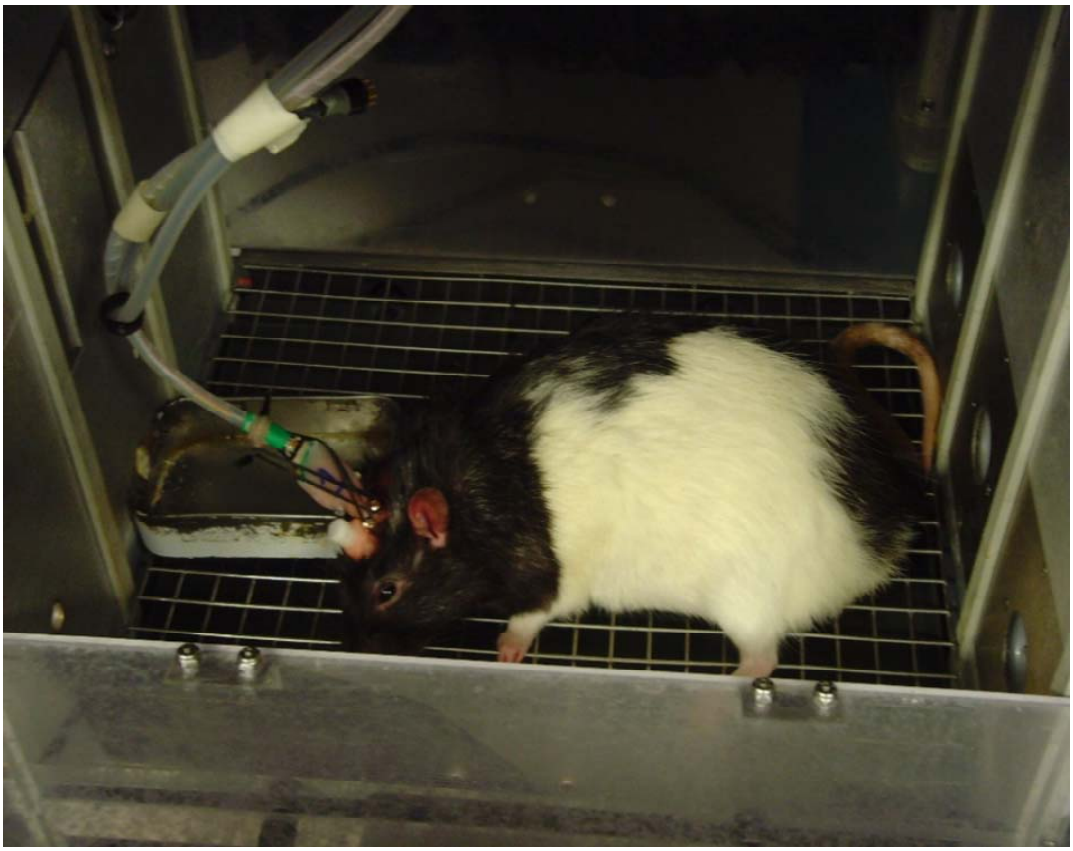


Figure 5.2: Animal test: unit NS-11 (*Long Evans*).

Male *Long Evans* rats (~350 *g*) were anesthetized with an intraperitoneal injection of a mixture of ketamine, xylazine, and acepromazine and maintained with ketamine updates [97]. A single craniotomy was made in each rat and a chronic channel printed circuit board (NeuroNexus Inc. [98]) connected with 16-channel single shank microelectrode and a 16-pin Omnetics nano-connector [99] was mounted near the craniotomy and anchored to the skull with a bone screw and dental acrylic. A microprobe was implanted into the primary motor cortex on the rat's brain. All procedures were

carried out following the National Institute of Health (NIH) guidelines [100] for the care and use of laboratory animals and were approved by the University of Michigan Committee on Use and Care of Animals (UCUCA) [101].

A measured neural signal with a digital high-pass filter setting for spikes selection is plotted in Figure 5.3. Undesired high-frequency noise and low-frequency field potentials were blocked by both analog and digital filters, and clear neural spikes were recorded from the device. The stimulation parameters are fixed at default mode (100 μA amplitude, 130 *Hz* frequency and 90 μs stimulation time). Although most of the stimulation signal is filtered out, stimulation artifacts with exact 7.69 *ms* period (130 *Hz*) are still apparent.

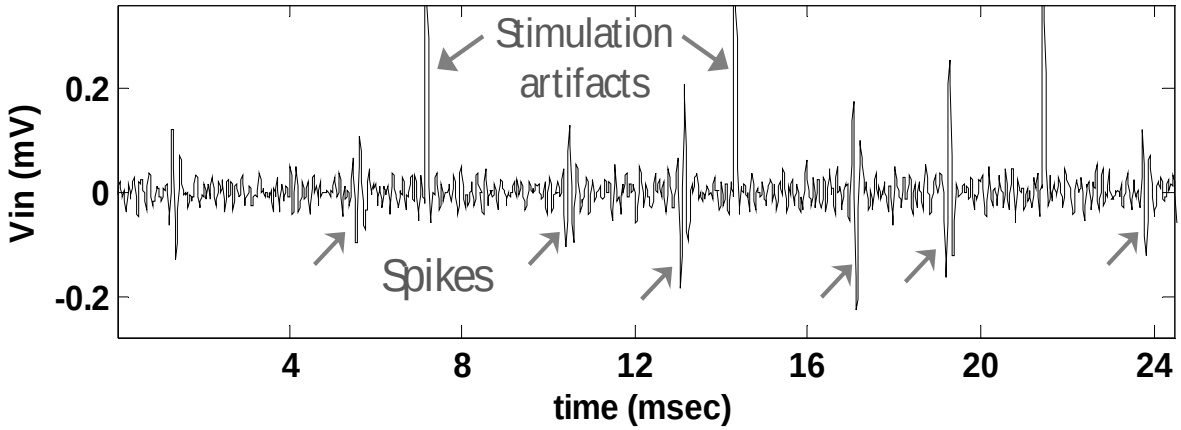


Figure 5.3: Measured neural signals.

Figure 5.4 shows the frequency response of the measured neural information computed by the Fast Fourier Transform (FFT). The fundamental 1 *kHz* frequency of neural spikes is clearly shown.

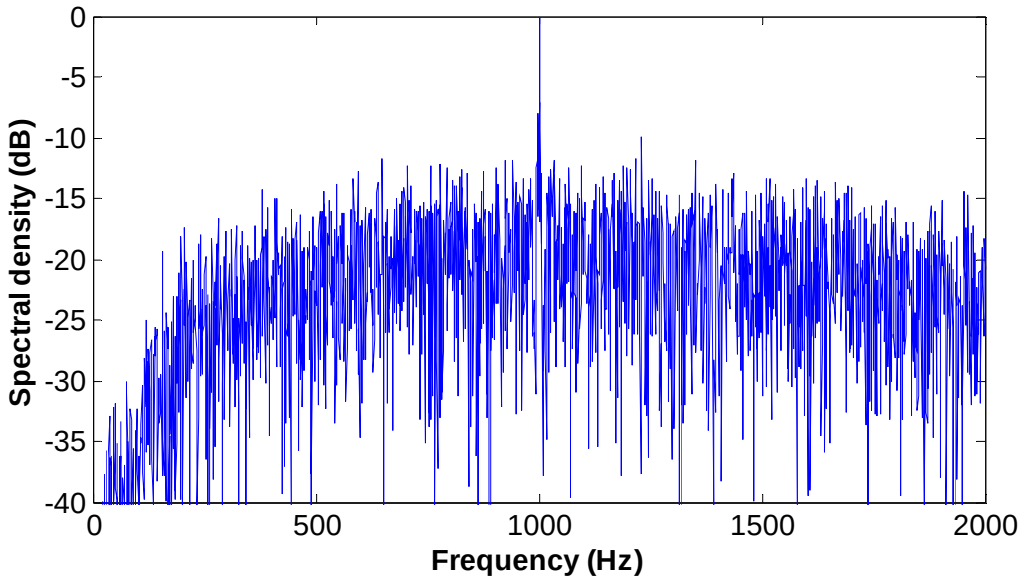


Figure 5.4: Frequency response of the neural signal.

An important metric of the signal quality is signal-to-noise ratio (SNR) which is calculated by the estimate ratio of spike amplitude to the background noise level [42]. The background noise may come from instruments, floating body potential, and tethered wires affected by external noise sources such as 60 *Hz* power noise. Amplitude thresholding is used for the classification of neural spikes from background noise, and the threshold is set by a manual input. During a 10-*second* time-window of the real-time fast-recording, 292 neural spikes (Firing rate of 29.2 *Spikes/sec*) are detected with 50 μV thresholding, and the average signal peak is calculated as 87.1 μV. The root-mean-square (RMS) value of background noise which absolute amplitude is under 50 μV is measured as 17.2 μV, and it gives SNR of 14.2 *dB*.

5.2. Wearable device

The electrical performance and functionality of the CDBS design was evaluated using the benchtop system described above. However, a small size, wearable system with wireless telemetry is required for a clinical use. Miniaturized PCBs were designed with low-noise and low-power consumption to deliver the neural stimulation signal via wireless telemetry to the front-end microelectrode device. Two separate PCB designs function as transmitter and receiver, respectively, as shown in Figure 5.5.

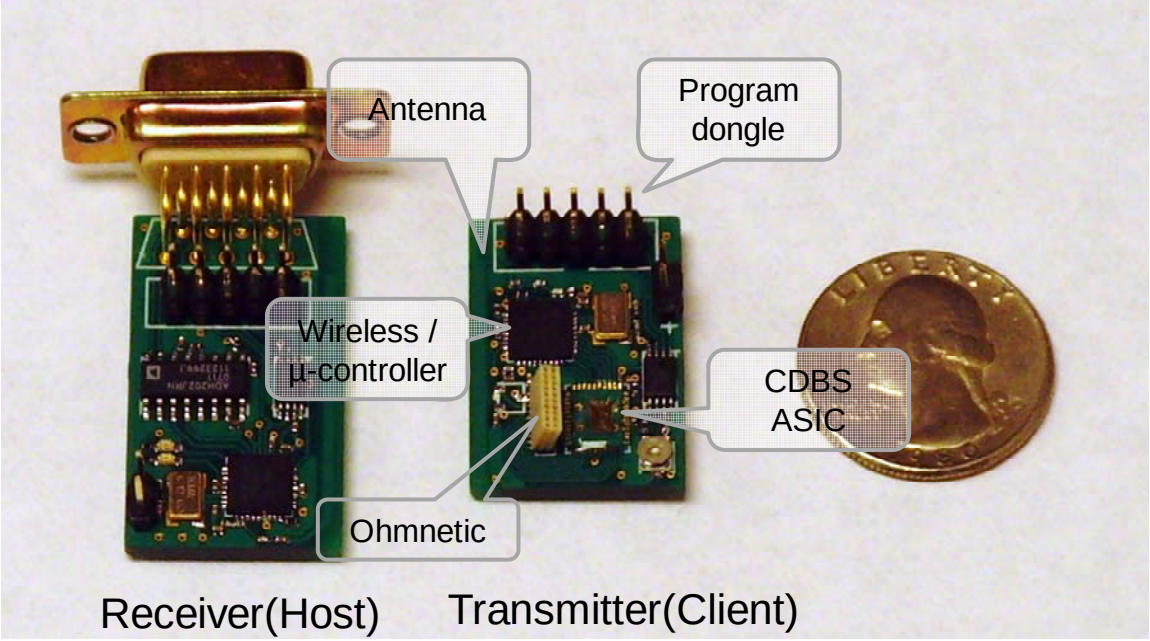


Figure 5.5: Implantable printed circuit boards.

The transmitter PCB consists of a CDBS ASIC described above, a micro controller including wireless transceiver [102] and Omnetics nano-connector [99] as well as an on-board wireless antenna and programming dongle connector. The transmitter

PCB was mounted on top of the rat's head using dental acrylic anchored to a bone screw. The transmitter PCB has a size of 19 *mm* by 26 *mm* and weighs 3 *g* making it well suited for the animal implantation. The receiver board includes the same wireless transceiver to receive the transmitted neural data and send control signals. The control signals are generated by a host PC connected with a universal asynchronous receiver and transmitter (UART) serial interface [103].

An nRF24E1 chip from Nordic Semiconductor Inc. [102] was used for the neural analysis and wireless delivery. It is a single chip 8051 compatible microcontroller which contains internal voltage regulators and an nRF2401 2.4 *GHz* radio-frequency (RF) transceiver capable of 1 *Mbps* data rate communication over 125 multi-channels.

The schematic of the nRF24E1 chip is shown in Figure 5.6. The only external components required to build a complete system are a 16 *Mhz* crystal, decoupling capacitors, and an external 32 *kByte* Electrically Erasable Programmable Read-Only Memory (EEPROM). The microcontroller has a 256 *Byte* data Random Access Memory (RAM) and a 512 *Byte* ROM which contains a bootstrap loader executed automatically after power-on reset or software request. The custom program is loaded into a 4 *kByte* RAM from the external serial EEPROM by the bootstrap loader.

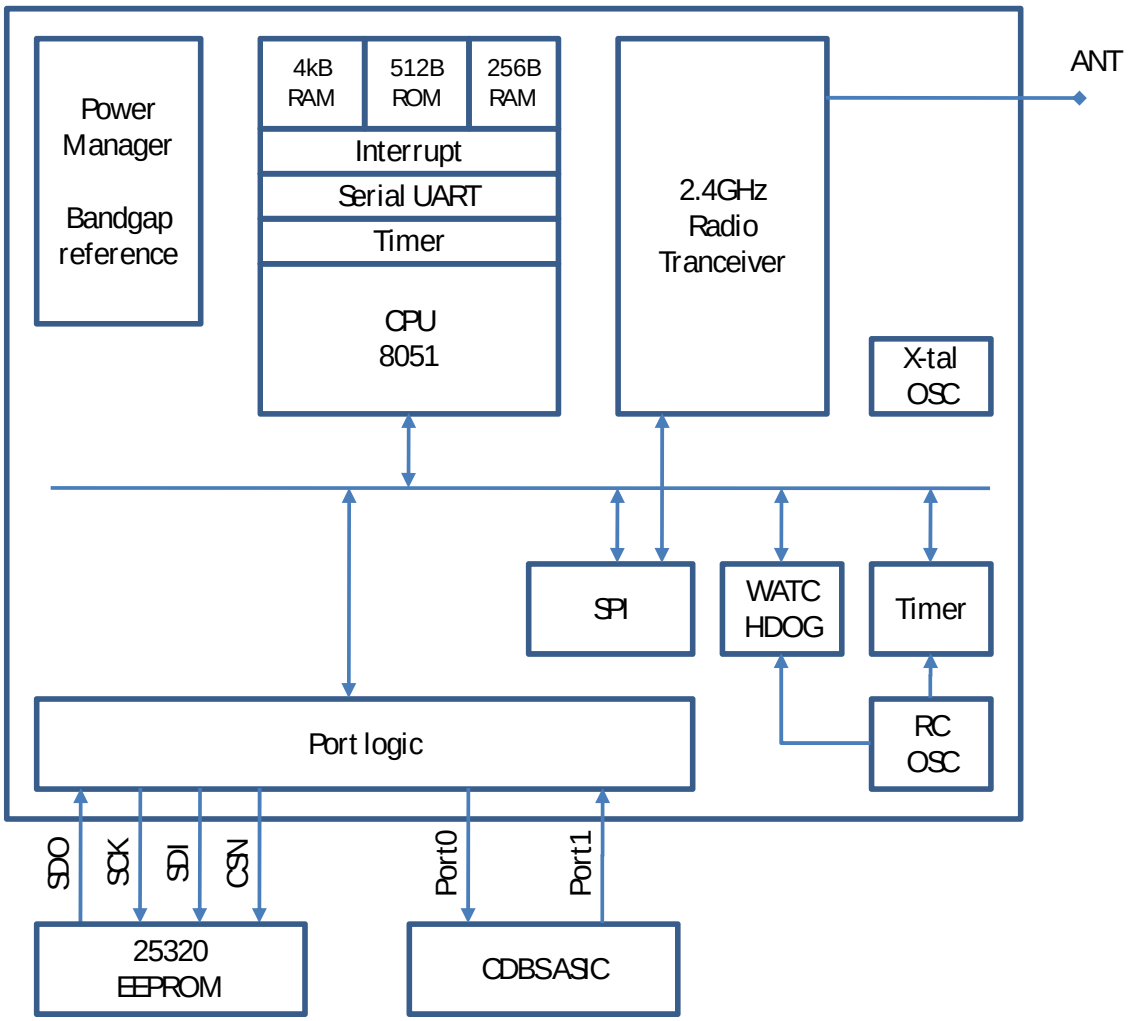


Figure 5.6: The structure of nRF24E1 [102].

The nRF24E1 has two general purpose bi-directional CMOS I/O ports. Port 0 is used to configure the CDBS operation modes, and port 1 reads neural data from the CDBS ASIC. The RADIO port controls the wireless transceiver functions.

The implantable system mounted on top of a male *Long Evans* rat's (342 *g*) brain is shown in Figure 5.7. A 3.6 *V*-720 *mAh* Lithium-ion rechargeable battery supplies power. The estimated battery life is 68 *hours* for the configuration mode with full-operation of the microcontroller and wireless communication, and 923 *hours* for the

normal operation mode that provides a stimulation-only function without wireless monitoring.

Figure 5.7: The implantable prototype system (unit NS-17).

During the analysis of each recording session, units on each electrode channel were identified using software-defined thresholding, template-matching, and principal component analysis. Software written in Matlab [104] was used for neural decoding and the parameter control.

A measured real-time neural signal from the implanted device is plotted in Figure 5.8. A time-window that contains relatively large number of neural spikes has been selected, although the average firing rate was calculated as 47.2 *spikes/sec* at 10 *sec* continuous time-window with a 50 μV thresholding. Similar to the previous setting, the

stimulation parameters were set on the default mode, and there remains the stimulation artifacts with 7.69 *ms* period (130 *Hz*). The overall signal patterns are same with the electronic test-bench described above except that there seems to be more noisy data sensed together. While the average neural peak is 93.5 μV, the noise level is measured as 28.9 μV that gives the SNR of 10.2 *dB*. Although the external noise from the tethered connections is minimized at the implantable device, closely located mixed-signal components affect each other, increasing a possibility of more noise. For example, the residue of digital clocking at the microcontroller may contaminate the signal quality of the analog front-end.

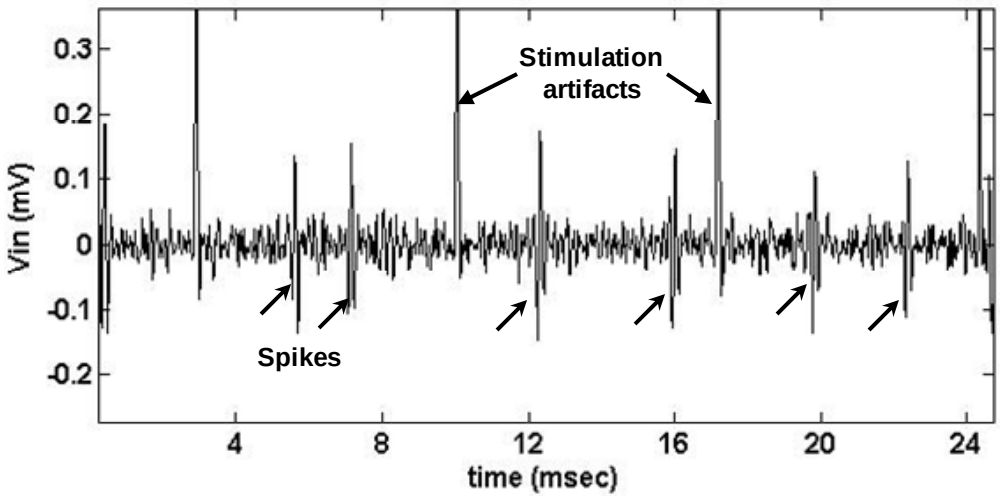


Figure 5.8: Measured neural signals

Figure 5.9 shows the frequency response of the measured information by FFT. The fundamental neural spikes still lie in around 1 *kHz* frequency.

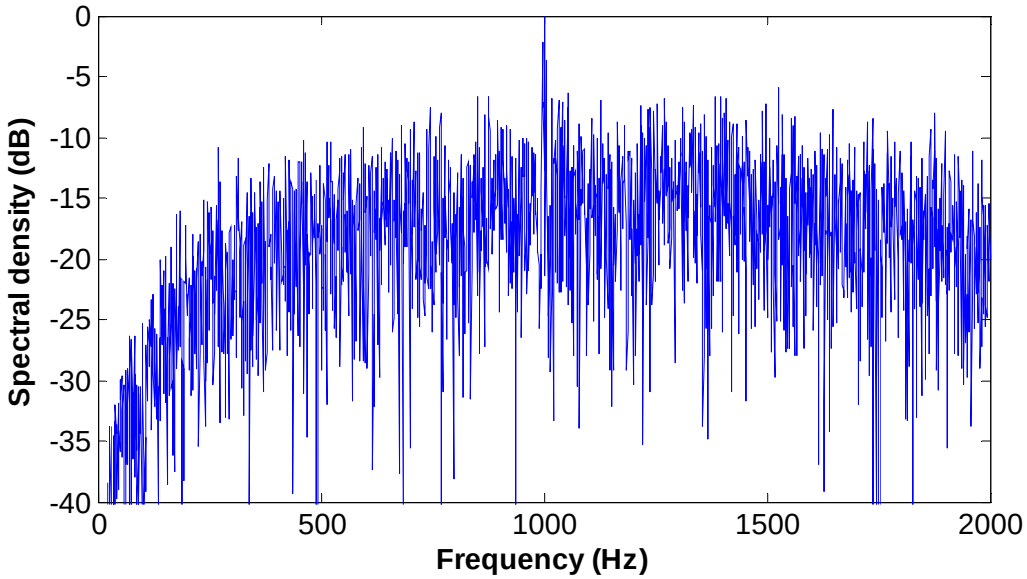


Figure 5.9: Frequency response of the neural signals.

For the post-processing such as neural decoding, a single-unit spike sorting is a widely-used method in neuroscience research. A well-sorted neural information provides a better decoding accuracy, correspondent neural sources (the number of neurons near the recording sites), and systematic changes of an organic condition [105].

A raster of the spike train outputs from the 74 sorted single clusters at a channel 5 is shown in Figure 5.10. The threshold is set to 50 μV, and the average peak is measured at 105 μV with the maximum apex of 267 μV. Figure 5.11 shows another sorted single-unit plot from a channel 8 that is located in a lower brain layer.

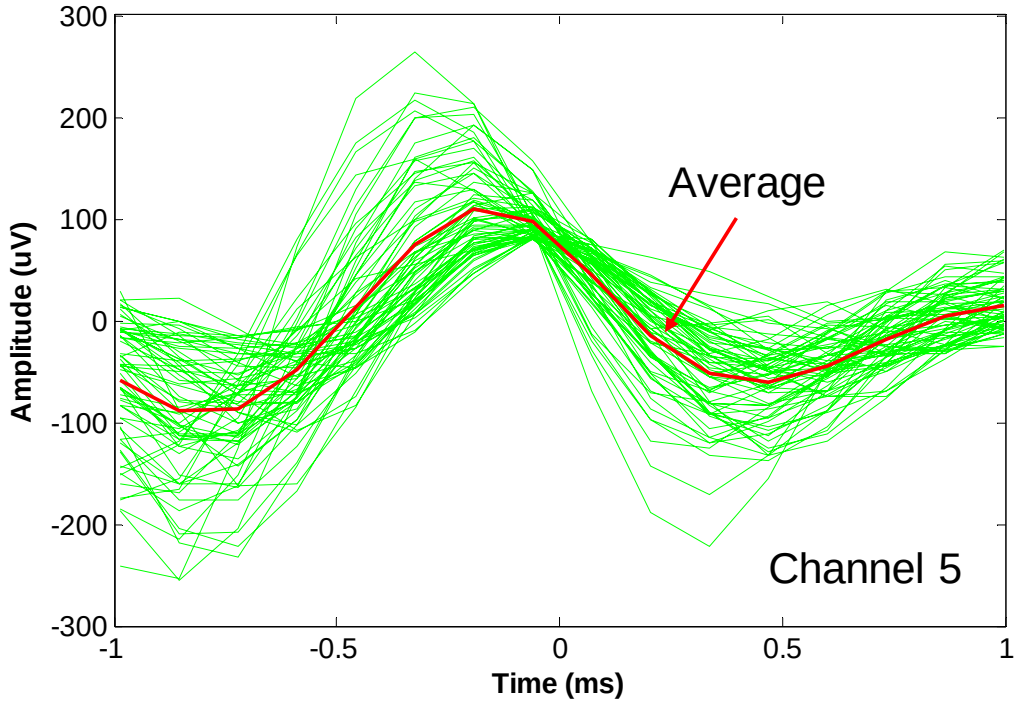


Figure 5.10: Single-unit neural spike sorting (Channel 5).

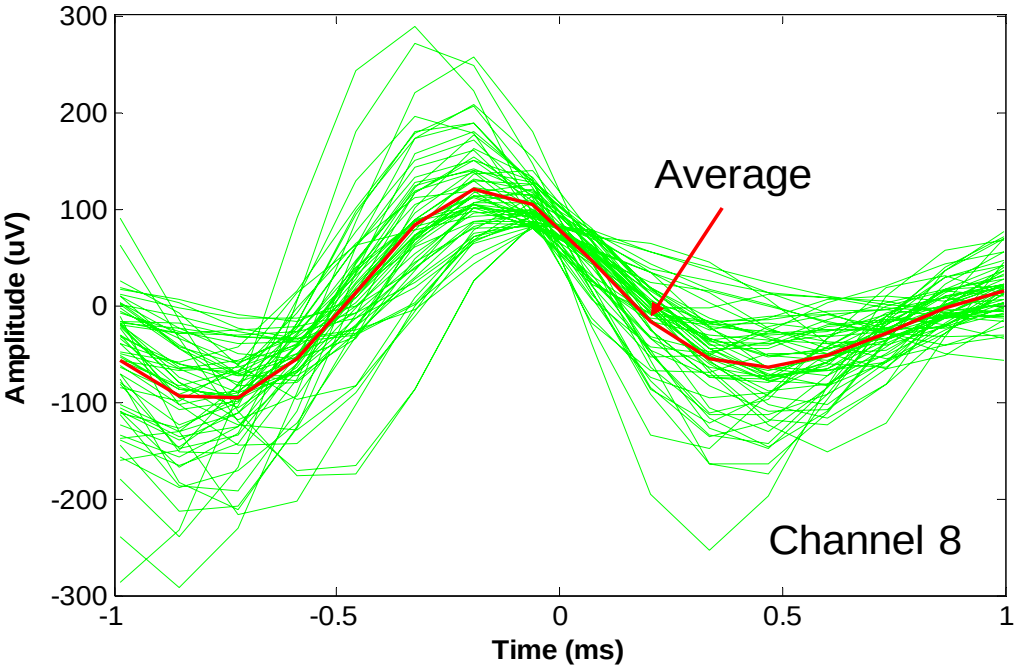


Figure 5.11: Single-unit neural spikes sorting (Channel 8).

In many neural interface studies, Principal-Component analysis (PCA) is a standard neural sorting procedure [106]. PCA is a useful technique to simplify the high dimensionality of large data sets [107] such as correlated single-unit neural spikes. PCA can also be used to find desired spikes in noisy data. Each principal component is a linear superposition of the original variables so that all the principal components are orthogonal to each other to avoid any redundancy. A feature classification by PCA provides the spatial and temporal neural information, and enables further analysis such as a movement prediction [108].

Figure 5.12 shows a scatter plot of the single-unit recording from the channel number 5. The plot shows the neural signal amplitudes data projected onto the first two principal components. There is a unit cluster of strongly correlated neural activities seemingly coming from a single neuron which is located near the channel 5.

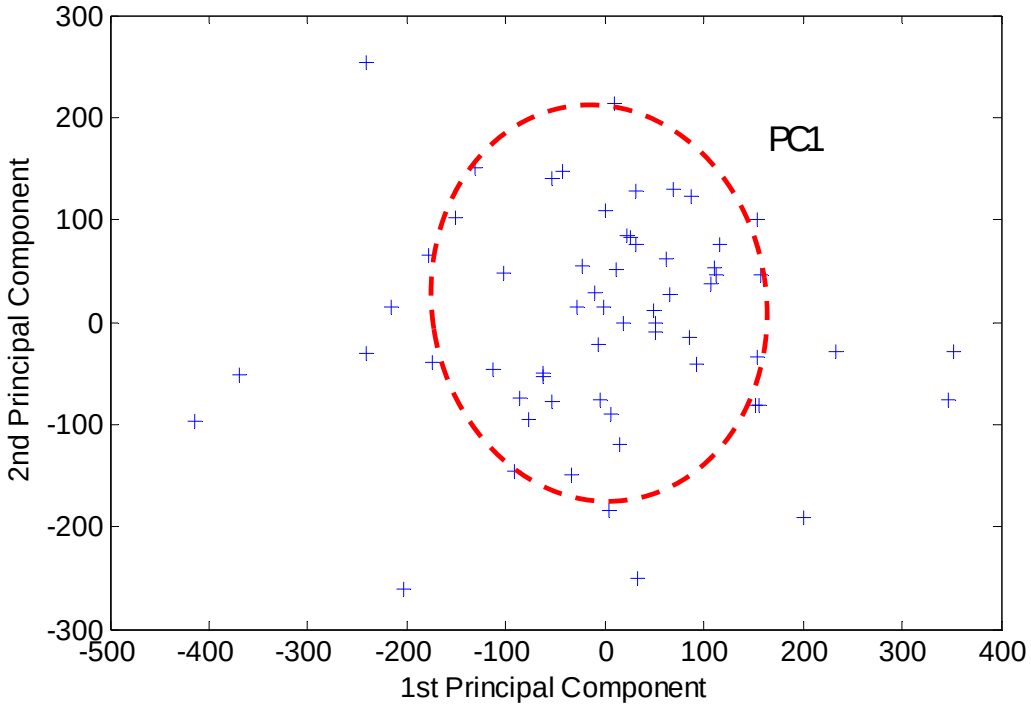


Figure 5.12: The Principal Component Analysis of the neural signals from channel 5.

Figure 5.13 shows another scattering plot from the channel 8. The unit plot of the first two principal components shows that there are two distinct regions as circled with a red dotted line and a green dotted line. This represents solid evidence of two independent neural sources from different neurons.

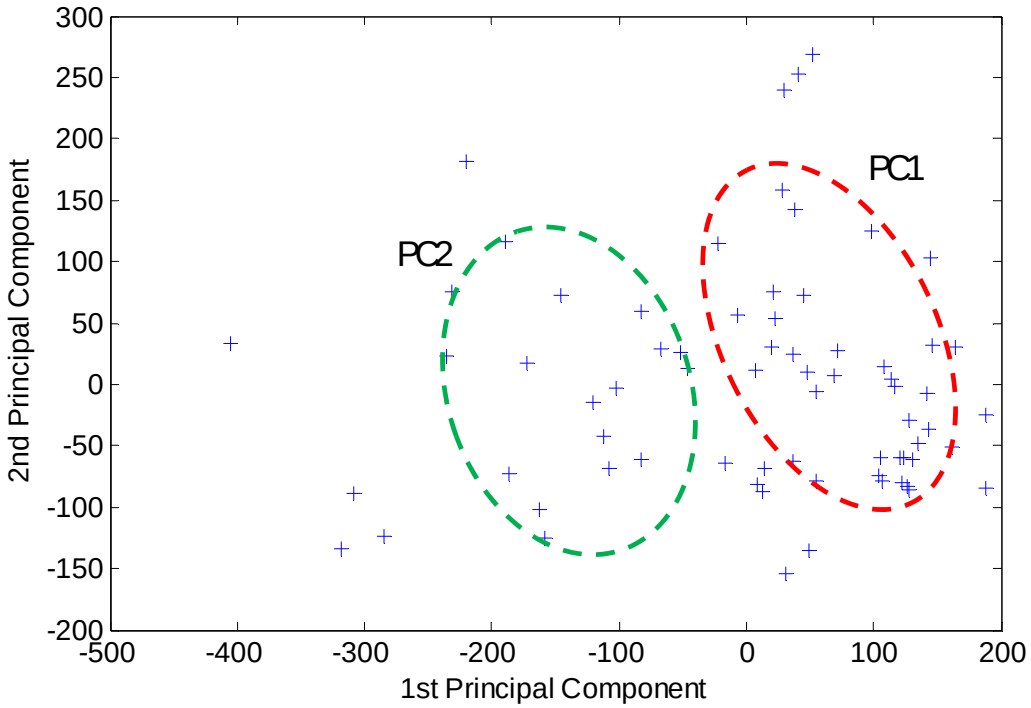


Figure 5.13: The Principal Component Analysis of the neural signals from channel 5.

The single-unit neural sorting analysis along with PCA verified the feasibility of the implantable CDBS device as an application to *in-vivo* neural recording interface. To analyze an applied closed-loop algorithm, it would be necessary to examine the principal components change when the stimulation current varies. Also, more data sets from multiple rats should be collected to build a strong statistic model.

CHAPTER VI
Conclusion and future work

6.1. Conclusion

In this dissertation, the biological background of Parkinson's disease and the efficacy of deep brain stimulation (DBS) for the treatment of Parkinson's disease have been discussed. DBS is an emerging therapeutic technology for hypokinetic neurological disorders, such as Parkinson's disease. In order to reach the most effective treatment results, the stimulation parameters should be adjusted based on the individual patient's condition, which can be achieved by a neuro-physiological feedback algorithm. A single-chip closed-loop DBS (CDBS) device, which senses a tremor in neural activities, has been proposed for the self-configuration of stimulation parameters. The noteworthy neural information includes both high-frequency neural spikes and low-frequency local field potentials (LFPs) that have different amplitude levels. For the simultaneous recording of both neural ensembles, a high dynamic range device is required. It can be achieved either by separating the two signal bands with a cascaded analog front-end, as described in Chapter 2, or by an implementation of a new logarithmic analog-to-digital converter (ADC), which provides a high dynamic range efficiently, as proposed in Chapter 3.

For the first approach, a two stage bi-quad pre-amplifier design is introduced for a simultaneous, multi-modal recording of extracellular neural action potentials and LFPs. A

switched capacitor technique is used for resistor emulation and 1/*f* noise reduction. The switched capacitor circuit modulates the signal so that 1/*f* noise may be reduced to below thermal noise. The switched-capacitor amplifying filter prototype performs well in recording neural spikes and field potential, simultaneously.

However, a logarithmic coding technique is a more sophisticated way of the simultaneous neural recording. This approach is ideal where a high dynamic range, but not a high peak SNDR, is required as in neural encoding. A switched-capacitor logarithmic pipeline ADC scheme, which depends on simple scaling functions, has been proposed. To verify the feasibility of the logarithmic pipeline conversion technique, a signed, 8-bit 1.5 bit-per-stage prototype ADC is implemented in 0.18 μm CMOS. The 22 *MS/s* ADC has a measured dynamic range of 80 *dB* and a measured dynamic range figure of merit (FOM) of 174 *dB*. The measurement of the logarithmic ADC prototype shows an excessively high dynamic range covering the entire neural signal range.

The novel logarithmic ADC has been integrated into CDBS device with other advanced neural front-ends. The CDBS system generates independently programmable stimulation currents. In addition, it senses and filters neural activities recorded with an eight channel low-noise neural amplifier (LNA), and a 200 *kS/s* 8 bit logarithmic pipeline ADC. A new (2+4) bit current DAC and parameter controller for effective biphasic stimulation has been designed. The 64 channel point-controllable stimulation enables the formation of various stimulus patterns for the most effective treatment of Parkinson's symptoms. The entire system is implemented in 0.18 μm CMOS with a MiM capacitor option, occupies 2.67 mm^2 while consuming 112 μW in the simulation-only normal operation mode and 351 μW under the full configuration mode from a 1.8 *V* supply. In

practice, CDBS systems are useful for self-configuration of stimulation parameters. Well-matched parameters by CDBS maximize the effectiveness of stimulating treatment and save power consumption, increasing battery life. In addition, the CDBS is an integrated single-chip, micro-scale and implantable device that reduces potential hardware complications significantly. Also, the invasive surgical area has been minimized, thus the degree of tissue damage and likelihood of infection has been reduced.

The electrical performance of a prototype CDBS Application-specific Integrated Circuit (ASIC) has been tested, and it satisfies the criteria of neural interface devices with huge reduction of the power consumption compared to the state-of-the-art neural interface circuits. The prototype ASIC has been integrated into a miniature printed circuit board (PCB) that contains a 2.4 *GHz* Industrial, Scientific and Medical (ISM) band transceiver as well as an on-board printed antenna. The wireless telemetry is used to identify the feedback algorithm by monitoring neural activities; it will enhance the knowledge of the mechanism of Parkinson's disease and DBS treatment.

In-vivo neural data are presented and analyzed with real-time fast recording, single-unit sorting and the principal-component analysis (PCA) tool. They were done by the extracellular neural recording from the motor cortex of two *Long Evans* rats, which were implanted with a 16-channel chronic neural electrode. This device verifies the feasibility of CDBS ASIC for the expanded neural applications, such as a neuro-physiological data acquisition system for chronic monitoring and a brain-machine interface for the visual, auditory and paralysis prosthetics.

6.2. Future work

Future research should be focused on investigating the parameters related to the neuro-physiological condition. The feedback algorithm for the optimal stimulation for Parkinson's disease treatment will be programmed based on the research of the neural mechanism for Parkinson's disease and DBS efficacy. For the clinical study, it will be useful to examine a well-defined animal model with a neurological disorder. A widely-used tool for dopamine neurons research is lesioning with the neurotoxin 6-hydroxydopamine (6-OHDA) [109]. This method has also been applied in investigations of the effects of experimental and clinical approaches related to the treatment of Parkinson's disease. Future research may employ this same technique to develop a Parkinson's state in a rat in order to validate the effectiveness of the treatment that the CDBS device provides.

Multi-channel stimulation should be tested to evaluate diverse patterns of stimuli. The effective patterns are generated by either a manual or an automatic programming of stimulation parameters, depending on the result of the neuro-pathological model. Also, a genuine single-chip solution, which integrates all CDBS functions and an embedded digital signal processor for neural decoding, will be beneficial in that it will further reduce the device dimensions, minimizing invasive exposure to potential infection.

Since DBS devices are considered to have potential hazards [110], the CDBS should have sufficient in-vivo data not only to prove the hardware functionality and the

clinical efficacy, but also to ensure the safety and the long-term durability. In addition, the applications of CDBS can be extended to other neurological disorders, such as epilepsy and seizure [111]. However, the DBS research for the treatment of these pathologies is at an early stage, and the effective stimulating patterns and the target location in brain need to be examined in depth.

BIBLOGRAPHY

[1] http://apdaparkinson.org/user/AboutParkinson.asp

[2] http://parkinsons.bsd.uchicago.edu/Overview/Symptoms.htm

[3] http://thalamus.wustl.edu/course/cerebell.html

[4] P. Bolam, C. Ingham and P. Magill, "Dynamic Model of Basal Ganglia Functions and Parkinson's Disease", *The Basal Ganglia* VIII, *Advances in Behavioral Biology*, Vol. 56, 2005

[5] P. Limousin, P. Krack, P. Pollak, A. Benazzouz, C. Ardouin, D. Hoffmann, et al. "Electrical stimulation of the subthalamic nucleus in advanced Parkinson's disease", *Journal of Neural Engineering Method*, 1998; 339:1105-1111.

[6] J. Houeto, P. Damier, P. Bejjani, C. Staedler, A. Bonnet, I. Arnulf, et al., "Subthalamic stimulation in Parkinson disease. A multidisciplinary approach", *Arch Neurology*, 2000; 57:461-465.

[7] P. Pollak, A. Benabid, P. Krack, P. Limousin, A. Benazzouz, J. Jankovic and E. Tolosa, "Deep brain stimulation: Parkinson's disease and movement disorders", *Williams & Wilkins*, 1998: 1085-1101.

[8] M. Pötter, M. Illert, R. Wenzelburger, G. Deuschl and J. Volkmann, "The effect of subthalamic nucleus stimulation on autogenic inhibition in Parkinson disease", *Neurology*, 2004;63;1234-1239

[9] A.L. Benabid, P. Pollak, C. Gervason, D. Hoffmann, D. M. Gao, M. Hommel, et al., "Long-term suppression of tremor by chronic stimulation of the ventral intermediate thalamic nucleus", *Lancet*, 1991; 337:403-406.

[10] P. Limousin, P. Pollak, A. Benazzouz, D. Hoffmann, J. F. Lebas, E. Brousolle, et al., "Effect on parkinsonian signs and symptoms of bilateral subthalamic nucleus stimulation", *Lancet*, 1995; 345:91-95.

[11] P. Hitchcock, "Motor III, Basal Ganglia", *Neuroscience*, Lecture notes, Feb 9th 2006.

[12] http://parkinsons.bsd.uchicago.edu/Overview/Medications.htm

[13] http://www.ninds.nih.gov/disorders/deep_brain_stimulation/deep_brain_stimulation.htm

[14] http://www.prometheus.uni-tuebingen.de/sec/vl/documents/42/bgana_normal.gif

[15] C. Haberler, F. Alesch, P. Mazal, P. Pilz, K. Jellinger, M. Pinter, J. Hainfellner, and H. Budka, "No tissue damage by chronic deep brain stimulation in Parkinson's disease", *Ann Neurol*, Vol. 48, pp. 372-376, 2000

[16] M. Kitagawa, J. Murata, S. Kikuchi, Y. Sawamura, H. Saito, H. Sasaki, and K. Tashiro, "Deep brain stimulation of subthalamic area for severe proximal tremor", *Neurology*, Vol. 55, pp. 114-116, 2000

[17] http://www.medtronics.com

[18] http://www.medtronic.com/physician/activa/surg_components.html

[19] http://www.swnsa.com/DBS.htm

[20] K. Lyons, S. Wilkinson, J. Overman, and R. Pahwa, "Surgical and hardware complications of subthalamic stimulation: A series of 160 procedures", *Neurology*, Vol. 3, pp. 612-616, August 2004

[21] I. Lambarri, E. Lezcano, J.C. Gomez, G. Bilbao, P. Madoz, and J. Zarranz, , "Pre- and postsurgical polysommography in Parkinson's disease", 7th *International Congress of Parkinson's Disease and Movement Disorders*, Vol. 17, Suppl. 5, 2002

[22] M.J. Lehmkuhle, S.S. Bhangoo, and D.R. Kipke, "The Electrocorticogram as a Feedback Control Signal for Deep Brain Stimulation of the Subthalamic Nucleus in the hemi-Parkinsonian Rat", *3rd International IEEE/EMBS Conference on Neural Engineering, CNE '07*, Page(s):386 – 389, 2-5 May 2007

[23] D. McCreery, A. Lossinsky, V. Pikov, and X. Liu, "Microelectrode Array for Chronic Deep-Brain Microstimulation and Recording", *IEEE Transactions of Biomedical Engineering*, Vol. 53, No. 4, April 2006

[24] U. Hofmann, C. Moll, G. Engler, A. Engel, M. Bar, D. Hohl, U. Thomas, and P. Detemple, "Multisite Microelectrodes for Use in Human Deep Brain Stimulation", *Proceedings of 2006 International Conference on Micro-technologies in Medicine and Biology*, Okinawa, Japan, May 2006

[25] P. Motta, and J. Judy, "Multielectrode Microprobes for Deep-Brain Stimulation Fabricated With a Customizable 3-D Electroplating Process", *IEEE Transactions on Biomedical Engineering*, Vol. 52, No. 5, MAY 2005

[26] K. D. Wise, "A multi-channel microprobe for biopotential recording", *Ph.D. dissertation*, Stanford Univ., Stanford, CA, 1969.

[27] P. Mohseni, and K. Najafi, "A Fully Integrated Neural Recording Amplifier With DC Input Stabilization", *IEEE Transactions on Biomedical Engineering*, Vol. 51, No. 5, May 2004.

[28] J. Ji and K. D. Wise, "An implantable CMOS circuit interface for multiplexed microelectrode recording arrays", *IEEE Journal of Solid-State Circuits*, Vol. 27, pp. 433–443, Mar. 1992.

[29] K. D. Wise and J. B. Angell, "A low-capacitance multi-electrode probe for use in extracellular neurophysiology", *IEEE Transactions on Biomedical Engineering*, Vol. 22, pp. 212–219, May 1975.

[30] H. J. Song, D. R. Allee, and K. T. Speed, "Single chip system for bio-data acquisition, digitization and telemetry", *IEEE International Symposium on Circuits and Systems*, Vol. 3, pp. 1848–1851, Hong Kong, Jun. 9–12, 1997.

[31] R. Harrison et el, "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System", *Journal of Solid State Circuit*, Jan. 2007.

[32] http://www.ninds.nih.gov/disorders/deep_brain_stimulation/deep_brain_stimulation.htm

[33] J. Lee, S. Park, J. Kang, J.S. Seo, J. Anders, and M.P. Flynn, "A 2.5mW 80dB DR 36dB SNDR 22MS/s Logarithmic Pipeline ADC", *IEEE Symposium on VLSI circuits*, June 2007.

[34] M.R. Yuce, L. Wentai, M. Chae, J. S. Kim, , "A Wideband Telemetry Unit for Multi-Channel Neural Recording Systems", *IEEE International Conference on Ultra-Wideband*, Sept. 2007

[35] http://www.fcc.gov/mb/engineering/usallochrt.pdf

[36] M.A. Nicolelis, N. Birbaumer, K. Muller, "Editorial", *IEEE Transactions on Biomedical Engineering*, Volume 51, Issue 6, June 2004 pp. 877 – 880

[37] J. Pine, M. Maher, S. Potter, Yu-Chong Tai, S. Tatic-Lucic, J. Wright, G. Buzsaki, A. Bragin, "A cultured neuron probe", *IEEE Proceedings of the 18th Annual International Conference of Engineering in Medicine and Biology Society*, Volume 5, Oct. 1996

[38] K.J. Otto, M.D. Johnson, D.R. Kipke, "Voltage pulses change neural interface properties and improve unit recordings with chronically implanted microelectrodes", *IEEE Transactions on Biomedical Engineering*, Volume 53, Issue 2, Feb. 2006, pp. 333 – 340

[39] R.J. Vetter, R.M. Miriani, B.E. Casey, K. Kong, J.F. Hetke, D.R. Kipke, "Development of a Microscale Implantable Neural Interface (MINI) Probe System", IEEE 27th *Annual International Conference of the Engineering in Medicine and Biology Society*, Sept. 2005

[40] R.R. Harrison, G. Santhanam, K.V. Shenoy, "Local field potential measurement with low-power analog integrated circuit", 26th *Annual International Conference of the Engineering in Medicine and Biology Society*, Volume 2, 2004

[41] A. Lorincz, G. Buzsaki, "Computational model of the entorhinal-hippocampal region derived from a single principle", *International Joint Conference on Neural Networks*, Volume 1, July 1999

[42] R.J. Vetter, J.C. Williams, J.F. Hetke, E.A. Nunamaker, D.R. Kipke, "Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex", *IEEE Transactions on Biomedical Engineering*, Volume 51, Issue 6, pp. 896 - 904, June 2004

[43] D.M. Taylor, S.I. Tillery, A.B. Schwartz, "Direct Cortical Control of 3D Neuroprosthetic Devices", *Science*, Vol. 296. June 2002, pp. 1829 – 1832

[44] K. Najafi, K.D. Wise, "An implantable multielectrode array with on-chip signal processing", *IEEE Journal of Solid-State Circuits*, Volume 21, Issue 6, Dec 1986 pp. 1035 – 1044

[45] R.A. Andersen, J.W. Burdick, S. Musallam, H. Scherberger, B. Pesaran, D. Meeker, B.D. Corneil, I. Fineman, Z. Nenadic, E. Branchaud, J.G. Cham, B.

Greger, Y.C. Tai, M.M. Mojarradi, "Recording advances for neural prosthetics", 26th *Annual International Conference of the Engineering in Medicine and Biology Society*, 2004. Volume 2, 2004 pp.5352 – 5355

[46] D.R. Kipke, "Implantable neural probe systems for cortical neuroprostheses", Engineering in Medicine and Biology Society, 26th *Annual International Conference of EMBC*, Volume 2, 2004 Page: 5344 – 5347

[47] T. Yoon, et al., "A Micromachined Silicon Depth probe for. Multichannel neural Recording", *IEEE Transaction of Biomedical Engineering*, 47: p. 1082-1087, 2000.

[48] D.T. Kewleya, M.D. Hillsb, D.A. Borkholderb, I.E. Oprisb, N.I. Malufb, C.W. Stormentb, J.M. Bowera and G.T.A. Kovacsb, "Plasma-etched neural probes", *Sensors and Actuators* A, 58(1): p. 27-35, 1997.

[49] X. Cui, V. A. Lee, Y. Raphael, J. A. Wiler, J. F. Hetke, D. J. Anderson, and D. C. Martin, "Surface modification of neural recording electrodes with conducting polymer/biomolecule blends", *Journal of Biomedical Materials Research*, Vol. 56, pp. 261-72, 2001.

[50] R.H. Olsson III, A.N. Gulari, K.D. Wise, "A fully-integrated bandpass amplifier for extracellular neural recording", *First International IEEE EMBS Conference on Neural Engineering*, 2003.

[51] P.T. Watkins, R.J. Kier, R.O. Lovejoy, D.J. Black, R.R. Harrison, "Signal Amplification, Detection and Transmission in a Wireless 100-Electrode Neural

Recording System", *IEEE International Symposium on Circuits and Systems*, May 2006

[52] P. Mohseni, K. Najafi, "A low power fully integrated bandpass operational amplifier for biomedical neural recording applications", *24th Annual Conference and the Engineering in Medicine and Biology*, Volume 3, 23-26 Oct. 2002 pp. 2111-2112

[53] A. Jackson, C.T. Moritz, J. Mavoori, T.H. Lucas, E.E. Fetz, "The neurochip BCI: towards a neural prosthesis for upper limb function", *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, Volume 14, Issue 2, June 2006 pp. 187-190

[54] http://www.neuronexustech.com

[55] T.C. Marzullo, J.R. Dudley, C.R. Miller, L. Trejo, D.R. Kipke, "Spikes, Local Field Potentials, and Electrocorticogram Characterization during Motor Learning in Rats for Brain Machine Interface Tasks", *IEEE 27th Annual International Conference of the Engineering in Medicine and Biology Society*, Sept.6, 2005

[56] J. Lee, M. Johnson, D.R. Kipke, "Simultaneous Neural Recording of Spikes and LFPs", *IEEE Annual International Conference of the Biomedical Engineering Society* (BMES), Oct. 2006

[57] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design", *Oxford University Press*, pp. 509-511, 2002

[58] R.H. Olsson III, D.L. Buhl, A.M. Sirota, G. Buzsaki, K.D. Wise, "Band-tunable and multiplexed integrated circuits for simultaneous recording and stimulation with microelectrode arrays", *IEEE Transactions on Biomedical Engineering*, Volume 52, Issue 7, pp. 1303 - 1311, July 2005

[59] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design", *Oxford University Press*, pp. 402-408, 2002

[60] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design", *Oxford University Press*, pp. 492-501, 2002

[61] S. McKennoch and D. M. Wilson, "Electronic interface modules for solid-state chemical sensors", *Proceedings of IEEE Sensors*, 2002.

[62] D. J. Yonce, P. P. Bey, Jr., and T. L. Fare, "A DC autonulling bridge for real-time resistance measurement", *Circuits and Systems I*: Fundamental Theory and Applications, *IEEE Transactions on Circuits and Systems* I: Regular Papers, vol. 47, pp. 273-278, 2000.

[63] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset", *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1877-1883, 2000.

[64] J. H. Nielsen and E. Bruun, "A CMOS Low-Noise Instrumentation Amplifier Using Chopper Modulation", *Analog Integrated Circuits and Signal Processing*, vol. 42, pp. 65-76, 2005.

[65] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization", *IEEE Proceedings*, vol. 84, pp. 1584-1614, 1996.

[66] S.Y. Lee, S.C. Lee, "Design of low-power switched-capacitor filter with switched-opamp technique", *IEEE Asia-Pacific Conference on Circuits and Systems*, Volume 1, 6-9, Dec. 2004

[67] P.R. Grey, and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits", *John Wiley & Sons, Inc.*, 1990.

[68] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design", *Oxford University Press*, pp. 550-561, 2002

[69] Y. Park, S. Karthikeyan, F. Tsay, E. Bartolome, "A low power 10 bit, 80MS/s CMOS pipelined ADC at 1.8V power supply", 2001 *IEEE International Symposium on Circuits and Systems*, Volume 1, May 2001

[70] D. Munson, "A Note on Lena", *IEEE Transaction on Image Processing*, vol. 5, No.1, Jan. 1996.

[71] F. Serra-Graells and J. Huertas, "Low-voltage CMOS subthreshold logarithmic amplification and AGC", *IEEE Proceeding of Circuits, Devices and Systems*, vol. 152, pp. 61-70, Feb. 2005.

[72] J. Sit and R. Sarpeshkar, "A Micropower Logarithmic A/D With Offset and Temperature Compensation," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 308-319, Feb., 2004.

[73] J. Candy, W. Ninke and B. Wooley, "A Per-Channel A/D Converter Having 15-

Segment μ-255 Companding", *IEEE Transactions on Communications*, vol. 24, pp. 33-42, Jan 1976.

[74] J. Guilherme and J. Franca, "New CMOS Logarithmic A/D Converters Employing Pipeline and Algorithmic Architecture," *Proceeding of IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 529-532, May, 1995.

[75] S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter", *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 954-961, Dec 1987.

[76] G. Nikandish, B. Sedighi and M. Bakhtiar, "INL Prediction Method in Pipeline ADCs", *IEEE Asia-Pacific Conference on Circuits and Systems*, Dec. 2006.

[77] J. Guilherme et el, "Design considerations for high resolution pipeline ADCs in digital CMOS technology", *IEEE ICECS*, Vol. 1, Sep. 2001

[78] R. C. Taft and M. R. Tursi, "A 100-MS/s 8-b CMOS subranging ADC with sustained parametric performance from 3.8 V down to 2.2V", *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 331-338, March 2001.

[79] G. Yin, F. Eynde and W. Sansen, "A High Speed CMOS Comparator with 8-b Resolution*", IEEE Journal of Solid State Circuits*, vol. 27, No.2, February 1992.

[80] S. Lewis, S. Fetterman, and G. Gross, "A 10-b 20-Msample/s ADC," *IEEE Journal of Solid-State Circuits*, vol. 27. no. 3, 1992.

[81] A. Abo and P. Gray, "A 1.5 V, 10-bit, 14.3MS/s CMOS Pipeline ADC," *IEEE Journal of Solid-State Circuit*, vol. 34, no. 5, pp. 599-606, May., 1999.

[82] Y. Jeon, S. Lee, K. Kim, J. Kwon and J. Kim, "A 4.7mW 0.32mm^2 10b 30MS/s Pipelined ADC Without a Front-End S/H in 90nm CMOS", *IEEE International Solid State Circuit Conference*, Feb., 2007.

[83] L. Breems, R. Rutten, R. Veldhoven, G. Veide and H. Termeer, "A 56mW CT Quadrature Cascaded ∑Δ Modulator with 77dB DR in a Near Zero-IF 20MHz Band", *IEEE International Solid State Circuit Conference*, Feb., 2007.

[84] J. Lee, H. Rhew, D.R. Kipke, and M.P. Flynn, "A 64 Channel Closed-loop Deep Brain Stimulator with a 8 Channel Neural Recording and a Logarithmic ADC", *IEEE Symposium on VLSI circuits*, June 2008.

[85] V. Fraix, and P. Pollak, "Stimulation of the Internal Globus Pallidus and the Subthalamic Nucleus for Parkinson's Disease", *Journal of Neural Engineering Med*, pp. 956-963, 2001

[86] http://www.medtronic.com/physician/activa/downloadablefiles/M221233A_b_004.pdf

[87] V.S. Polikova, P.A. Trescob and W.M. Reicherta, "Response of brain tissue to chronically implanted neural electrodes", *Journal of Neuroscience Methods*, Volume 148, Issue 1, Pages 1-18, October 2005

[88] V. Fraix and P. Pollak, "Stimulation of the Internal Globus Pallidus and the Subthalamic Nucleus for Parkinson's Disease", *Journal of Neural Engineering Med*, pp. 956-963, 2001

[89] M.J. Birdno, S.E. Cooper, A.R. Rezai, and W.M. Grill, "Pulse-to-Pulse Changes in the Frequency of Deep Brain Stimulation Affect Tremor and Modeled Neuronal Activity", *Journal of Neurophysiology*, pp. 1675-1684, 2007.

[90] A.M. Kuncel, S.E. Cooper, B.R. Wolgamuth, M.A. Clyde, S.A. Snyder, E.B. Montgomery, A.R. Rezai, W.M. Grill, "Clinical response to varying the stimulus

parameters in deep brain stimulation for essential tremor", *Movement Disorder* Vol. 21, pp. 1920–1928, 2006.

[91] M. Ushe, J.W. Mink, F.J. Revilla, A. Wernle, G.P. Schneider, L. McGee-Minnich, M. Hong, K.M. Rich, K.E. Lyons, R. Pahwa, J.S. Perlmutter, "Effect of stimulation frequency on tremor suppression in essential tremor", *Movement Disorder*, Vol. 21, pp. 1163–1168, 2004.

[92] M. Chae, W. Liu, Z. Yang, T. Chen, J. Kim, M. Sivaprakasam and M. Yuce, "A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Transmitter", *IEEE International Solid State Circuit Conference,* Feb. 2008.

[93] M. Ghovanloo and K. Najafi, "A Modular 32-site Wireless Neural Stimulation Microsystem", *IEEE International Solid State Circuit Conference*, Feb. 2004

[94] L. Theogarajan, J. Wyatt, J. Rizzo, B. Drohan, M. Markova, S. Kelly, G. Swider, M. Raj, D. Shire, M. Gingerich, J. Lowenstein and B. Yomtov, "Minimally Invasive Retinal Prosthesis", *IEEE International Solid State Circuit Conference,* Feb. 2006.

[95] P.K. Campbell, K.E. Jones, R.J. Huber, K.W. Horchand R.A. Normann, "A silicon-based, three-dimensional neural interface: manufacturing processes for an intracortical electrode array", IEEE Transactions on Biomedical Engineering, Vol. 38, Issue 8, Page(s):758 - 768, Aug. 1991.

[96] http://www.analog.com/en/prod/0,,762_0_ADUC841%2C00.html

[97] M. Johnson, O. Kao, and D.R. Kipke, "Spatiotemporal pH dynamics following insertion of neural microelectrode arrays", *Journal of Neuroscience Method*, 160(2):276-87, Mar 15, 2007

[98] http://www.neuronexustech.com/Products/ChronicProbe.aspx

[99] http://www.omnetics.com/index-1.asp

[100] Institute of Laboratory Animal Resources Commission on Life Sciences , "Guide for the Care and Use of Laboratory Animals", *National Academy Press*, Washington, D.C., 1996

[101] http://www.ucuca.umich.edu/guide.htm

[102] http://www.nordicsemi.com/files/Product/data_sheet/Product_Specification_nRF24E1_1_3.pdf

[103] H02162-0-7/03(E), "Embedded Modem Chipsets – Serial UART Interface", Analog Device Inc., 2003

[104] http://www.mathworks.com/products/matlab/

[105] D.S. Won, D.Y. Chong and P.D. Wolf, "Effects of spike sorting error on information content in multi-neuron recordings", *Conference Proceedings of First International IEEE EMBS Conference on Neural Engineering*, Pages: 618 - 621, March 2003

[106] J. Hu, J. Si, B.P. Olson and J. He, "Feature Detection in Motor Cortical Spikes by Principal Component Analysis", *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 2005

[107] R.C.T. Lee, Y.H. Chin, and S.C. Chang, "Application of Principal Component

Analysis to Multikey Searching", *IEEE Transactions on Software Engineering*, Volume SE-2, Issue 3, Page(s):185 – 193, Sept. 1976

[108] B.J. Richmond and L.M. Optican, "Temporal encoding of two-dimensional patterns by single units in primate inferior temporal cortex. II. Quantification of response waveform", *Journal of Neurophysiology*, Vol. 57, No. 1, pp. 147–161, 1987.

[109] V. Vorobyov, N. Schibaev, M. Morelli, A. Carta, "EEG modification in the cortex and striatum after dopaminergic priming in the 6-hyroxydopmain rat model of Parkinson's disease", *Brain Research* 972, 177-185, 2003

[110] C. Pea, K. Bowsher, A. Costello, R. De Luca, S. Doll, K. Li, M. Schroeder and T. Stevens, "An Overview of FDA Medical Device Regulation as it Relates to Deep Brain Stimulation Devices", *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, Volume 15, Issue 3, Page(s):421 - 424, Sept. 2007

[111] R.S. Fisher, S. Uematsu, G.L. Krauss, et al, "Placebo-controlled pilot study of centromedian thalamic stimulation in treatment of intractable seizures", *Epilepsia*, Vol. 3, pp: 841-851, 1992